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# RS690M02 uATX (Version: Fab A)

**CPU:** AMD Athlon64 / Athlon64 FX / Athlon64 X2 / Sempron series(AM2)

**System Chipset:**

ATI RS690 ... North Bridge  
ATI SB600 ... South Bridge

**Main Memory:**

Dual Channel / DDR-II \* 2 (Max 4GB)

**On Board Device:**

Clock Generator ... ICS 951464(TSSOP56)  
Super I/O ... Fintek F71882  
PCI I/F LAN ... RTL8101E(10/100) / 81111C(Giga)  
Azalia Codec ... ALC662  
BIOS ... SPI ROM / 4M

**Expansion Slots:**

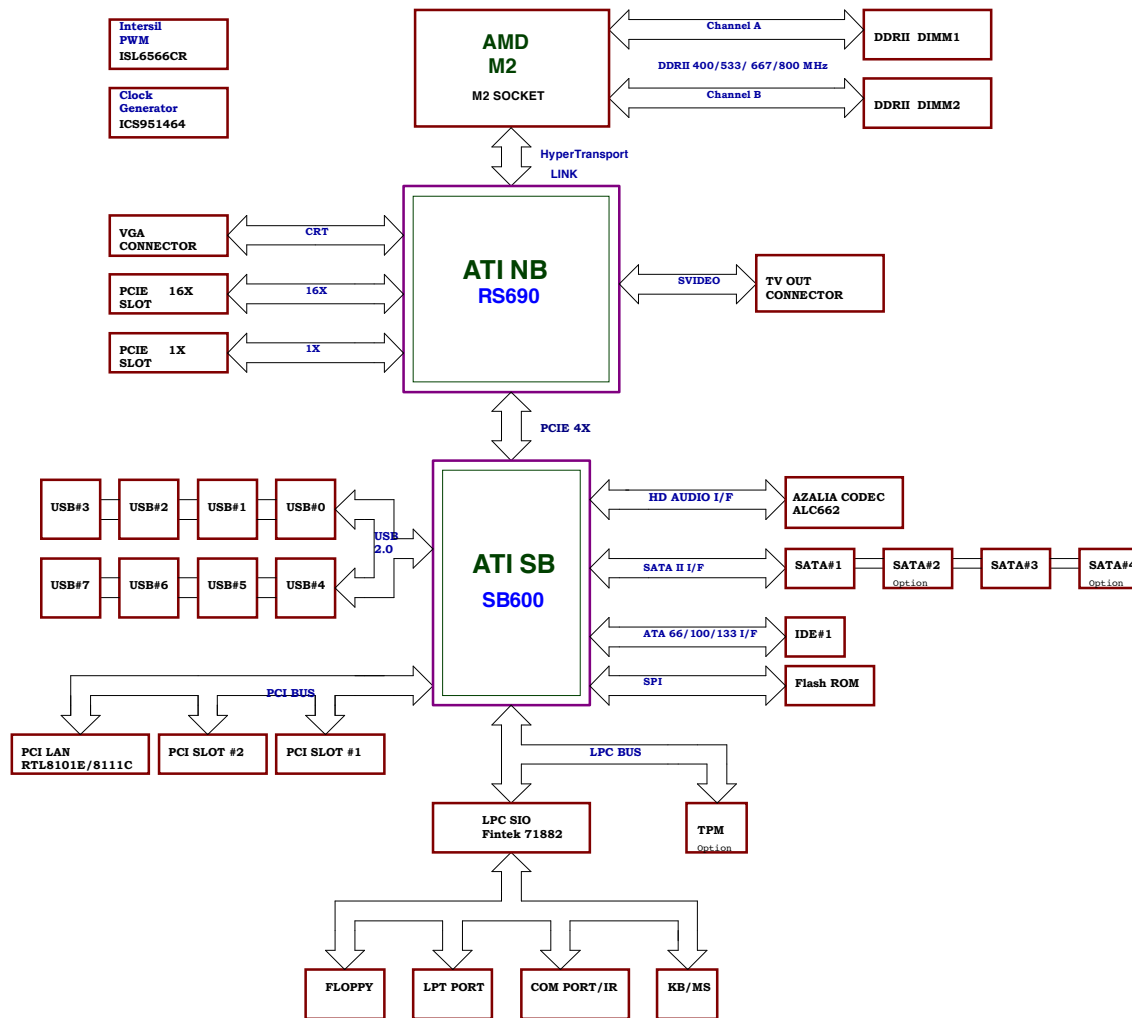
PCI EXPRESS 16X SLOT \*1  
PCI EXPRESS 1X SLOT \* 1  
PCI SLOT \* 2

**Intersil PWM:**

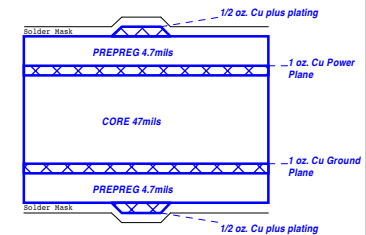
Controller ... ISL6566CR(3Phase)

Version	Function	SKU	BOM
FAB A	AM2/RS690/SB600/F71882/ALC662/RTL8101E	6LRS2H (CLONE)	

<b>FOXCONN®</b>			
<b>FOXCONN PCEG</b>			
<b>Title</b>			
<b>Cover Sheet</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	<b>A</b>
C	<b>RS690M02</b>		
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**Board Stack-up**  
(2116 Prepreg Considerations)

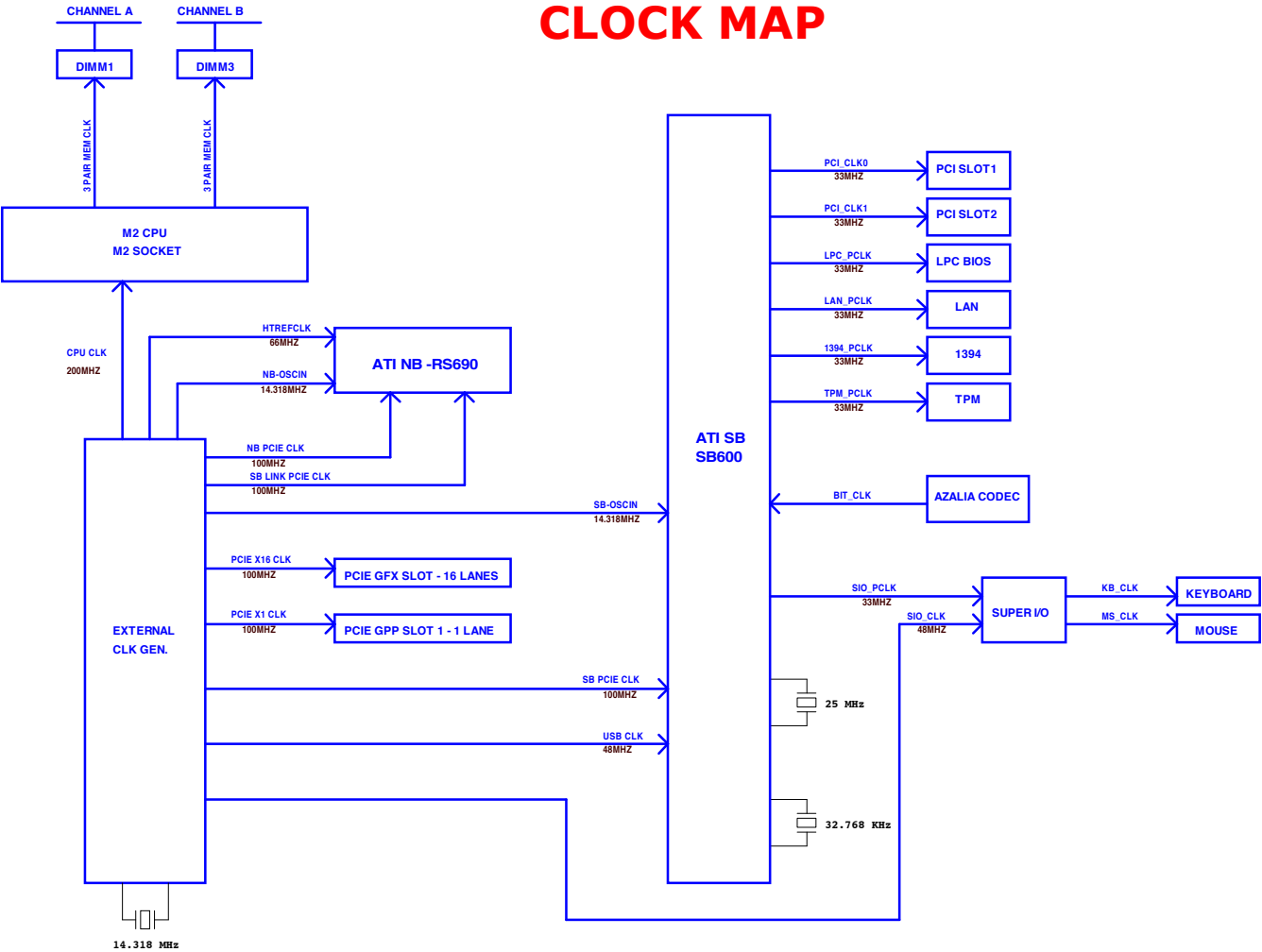


Single End 60ohm Top/Bottom : 5mils  
 IEEE1394 - 110ohm Top : 5/12/5  
 PCIE, LAN, SATA - 100ohm Top : 5/7/5  
 USB2.0 - 90ohm Top : 7/8/7

**FOXCONN**  
**FOXCONN PCEG**

File: **Block Diagram**  
 Size C Document Number: **RS690M02** Rev A  
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# CLOCK MAP



<b>FOXCONN PCEG</b>		
<b>Clock Distribution</b>		
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AM2	
0.8V-1.55V VDDCORE	- 80A
2.5V VDDA	- 0.1A
1.8V DDRII VDD	- 3A
0.9V DDRII VTT	- 0.125A
1.2V VLDT	- 0.5A

RS690	
1.2V VDDHT	- 0.5A
1.2V NB Core VDDC	- 5A
1.2V PCI-E&VCO&I/O&PLL	- 2.25A
1.8V DAC	- 200mA
1.8V LVDS	- 300mA
1.8V PLL&DAC-Q	- 100mA
1.8V PCI-E PLL	-

SB600	
1.2V SB CORE	- 0.6A
1.2V PCI-E X4	- 0.8A
1.2V PCI-E PVDD	- 80mA
1.2V ATA I/O	- 0.2A
1.2V ATA PLL	- 10mA
1.2V S5 PW(S5)	- 0.22A
1.2V USB CORE I/O(S5)	- 0.2A
3.3V S5 PW(S5)	- 10mA
3.3V I/O	- 0.45A

HD Audio ALC888	
3.3V AUDIO	- 40mA
5V AUDIO	- 200mA

ICS951464	
3.3V VDD/VDDA	- 400mA
0.3V - 1V CPU/SRC/PLL	- 70mA

RTL8100C/8110SC	
3.3V_SB I/O & LED	- 620mA
1.8V ANALOG	- 660mA

ISL6566	
+V_CPU VRM 10	
0.8V-1.55V 80A	
3-Phase Switch	

W83310DS	
VTT_DDR	
0.9V Linear	2.5A

TIGER ONE	
VCC_DDR	
1.8V Switch	10A
+1.2V_NB	
1.2V Switch	11A
+1.8V_NB	
1.8V Linear	1A
+1.2VSB	
1.2V Linear	0.5A
+1.2V_HT	
1.2V Linear	1A
VDDA_25	
2.5V Linear	0.1A
5V_DUAL	
5V Switch	4A
5VSB Switch	1A
VCC3_SB	
3.3V Linear	3A

DDRII x4 & TERMINATOR	
0.9V VTT_DDR	-2A
1.8V VCC_DDR (S0,S1)	-6A
1.8V VCC_DDR (S3)	-400mA

PCI Express x16 slot	
+12V	- 5.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

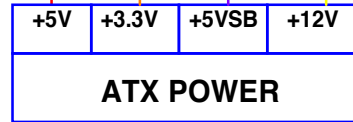
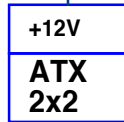
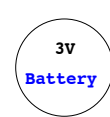
PCI Express x 1 slot	
+12V	- 0.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

PCI slot x2	
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 7.6A
+5V	- 5.0A
+12V	- 0.5A

USB x8	
+5V (S0,S1)	- 4.0A
+5V (S3)	- 20mA

PS2	
+5V (S0,S1)	- 345mA
+5V (S3)	- 2.0mA

5VAudio	
+5VR	
500mA	



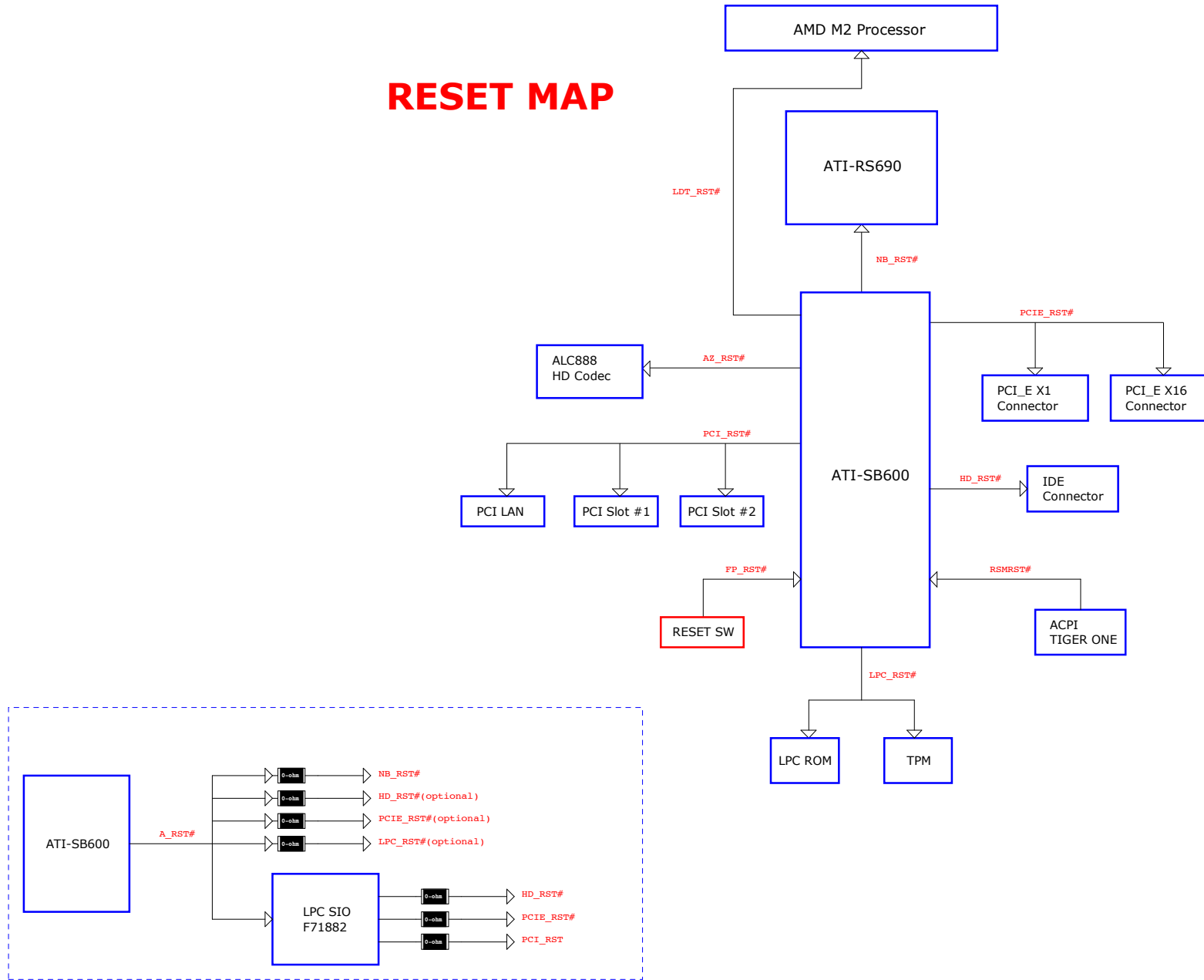
**FOXCONN**  
FOXCONN PCEG

File: **Power Delivery**

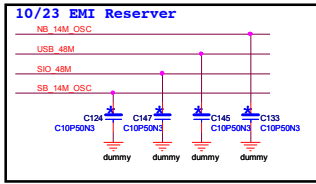
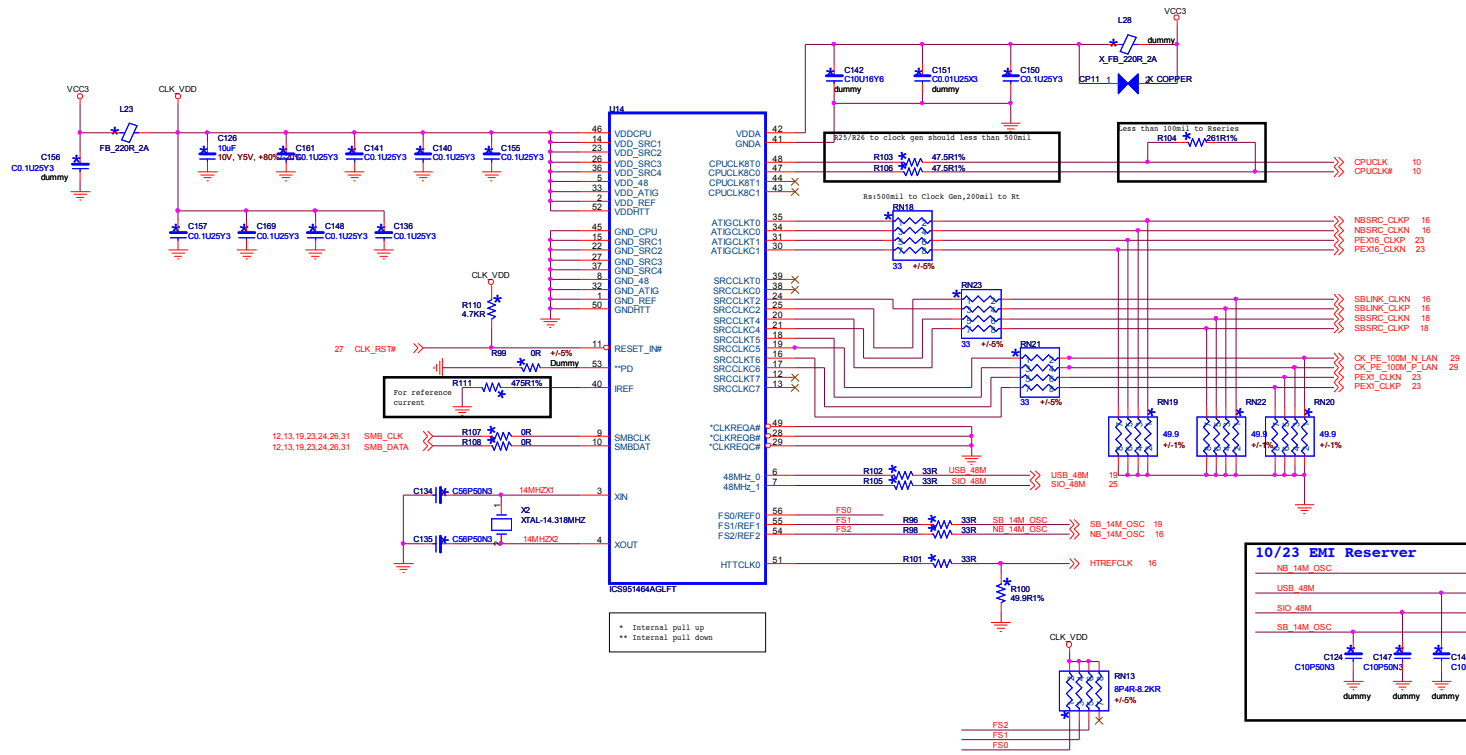
Size C Document Number: **RS690M02** Rev 1.0

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# RESET MAP



<b>FOXCONN</b> FOXCONN PCEG		
File: <b>Reset Map</b>		
Size: C	Document Number: <b>RS690M02</b>	Rev: 1.0
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EXT CLK FREQUENCY SELECT TABLE(MHZ)

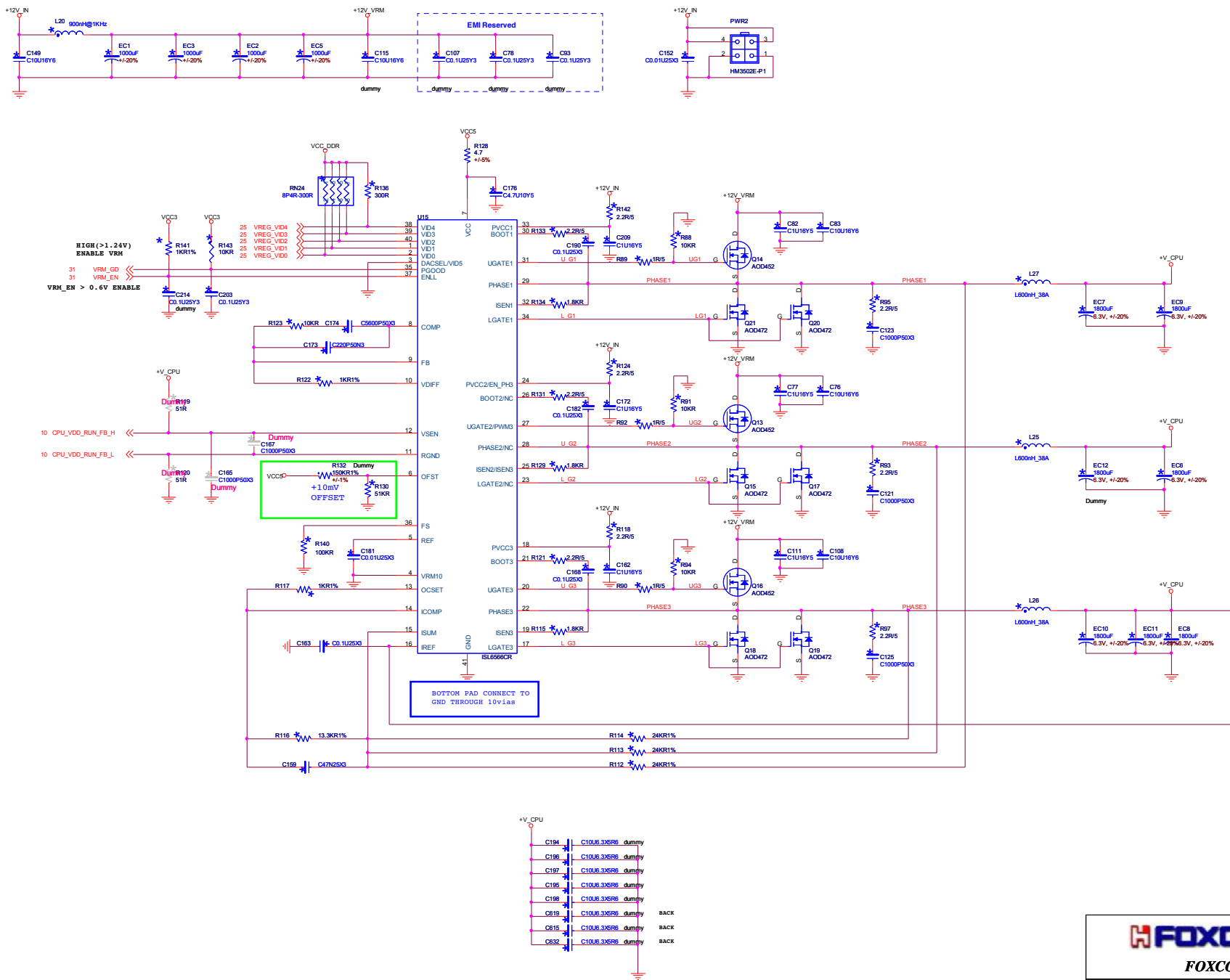
FS2	FS1	FS0	CPU	HTT	SRC	ATIG	USB
0	0	0	Hi-Z	Hi-Z	100.00	100.00	48.00
0	0	1	X/2	X/3	100.00	100.00	48.00
0	1	0	230.00	76.67	100.00	100.00	48.00
0	1	1	240.00	80.00	100.00	100.00	48.00
1	0	0	100.00	66.66	100.00	100.00	48.00
1	0	1	133.33	66.66	100.00	100.00	48.00
1	1	0	166.67	66.66	100.00	100.00	48.00
1	1	1	200.00	66.66	100.00	100.00	48.00

**FOXCONN**  
FOXCONN PCEG

File: **Clock Generator**

Size C Document Number: **RS690M02** Rev A

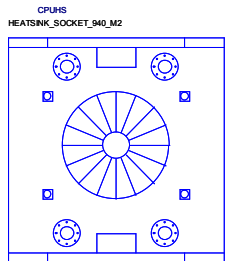
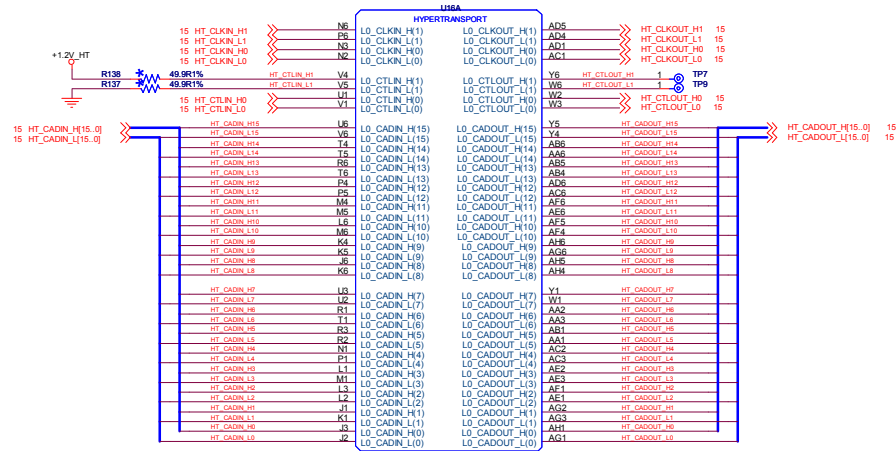
Date: Tuesday, September 11, 2007 Sheet 6 of 36



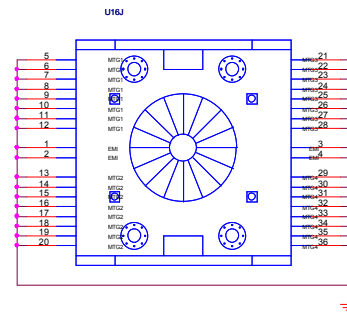
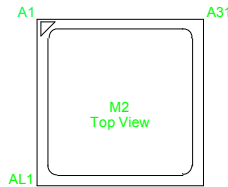
**FOXCONN**  
FOXCONN PCEG

File: VRM-ISL6566CR  
 Size C Document Number: RS690M02  
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# Processor Hyper Transport Interface



- Layout Notice:**  
Add stitching caps if crossing plane split
- HyperTransport Net Naming Convention:**  
HT\_"link driver"\_"link receiver"\_"function"\_"polarity"\_"number"



**FOXCONN**  
FOXCONN PCEG

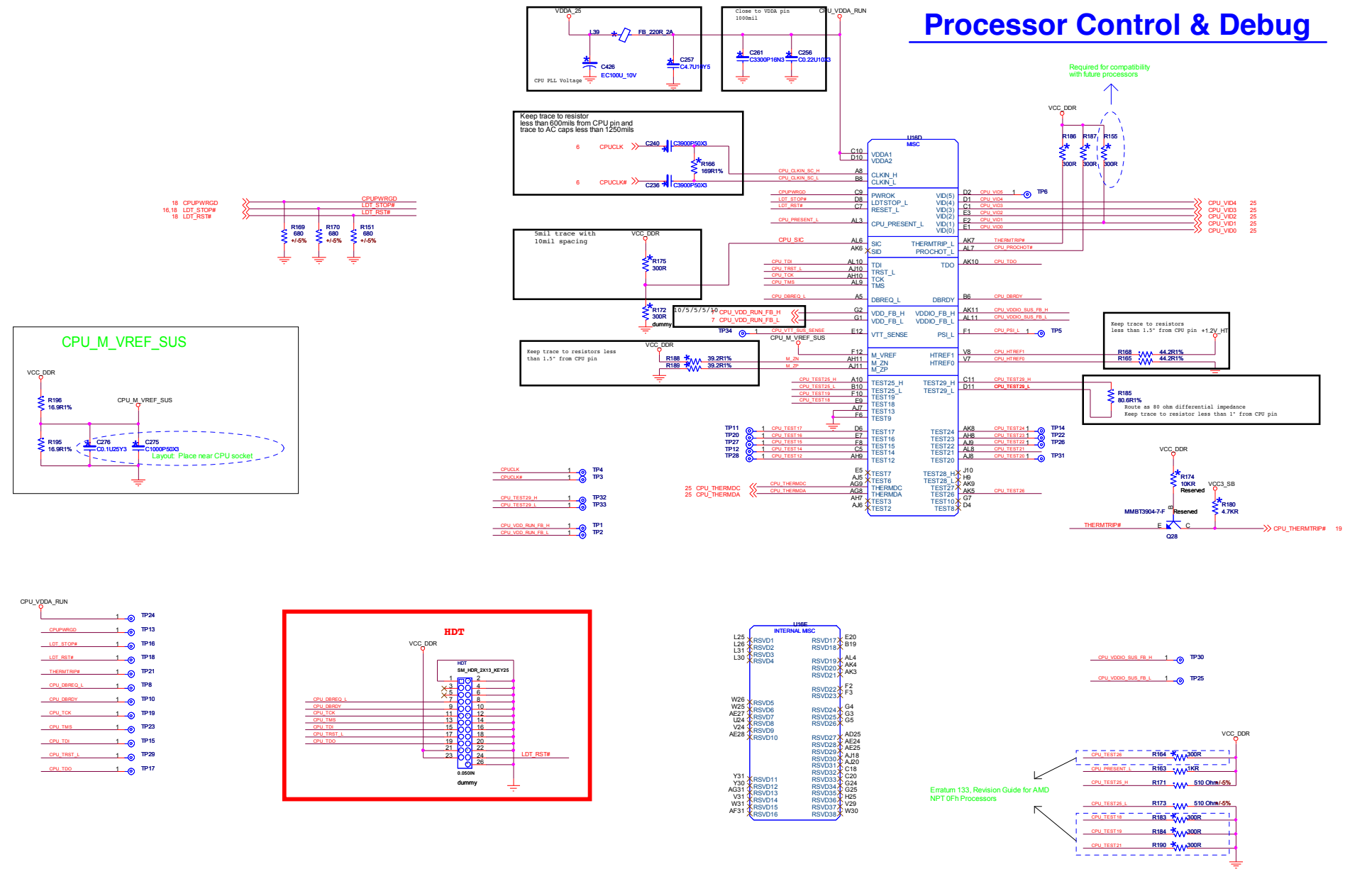
File: **M2-HT**

Size C Document Number: **RS690M02** Rev A

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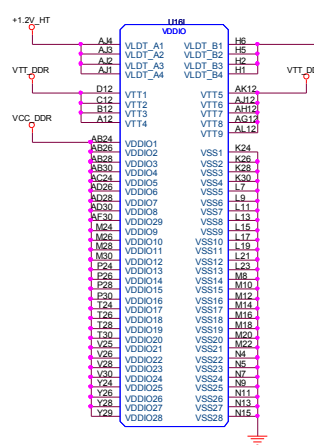
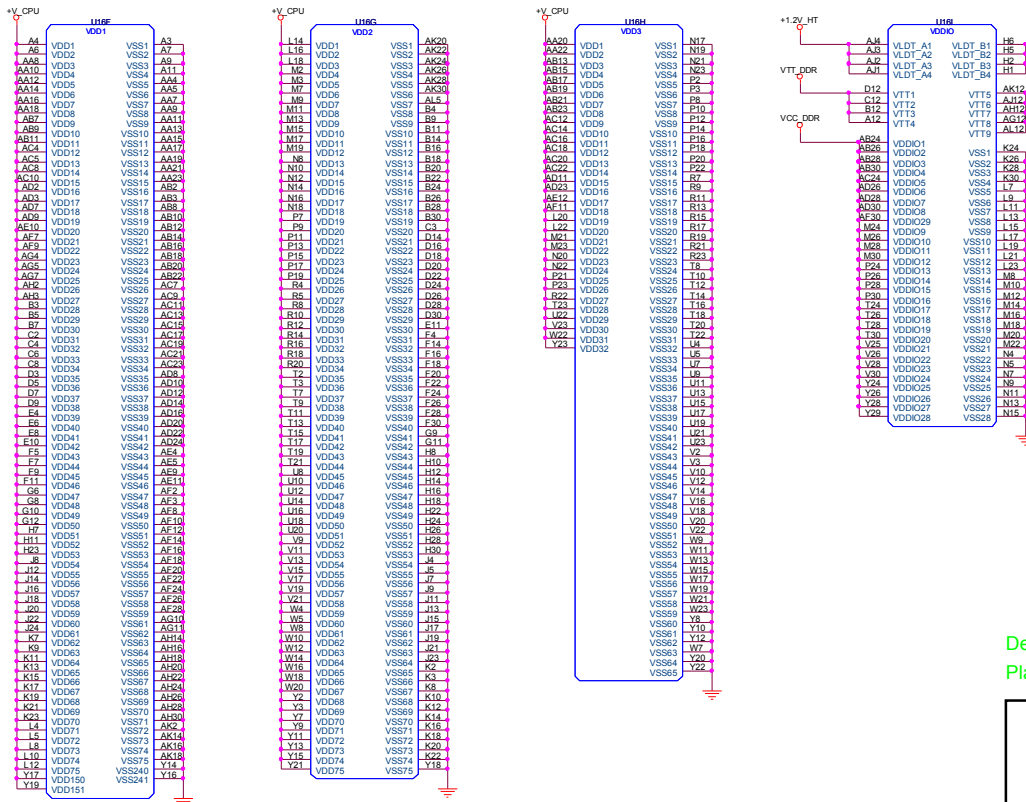
# Processor Control & Debug



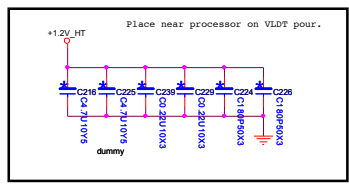
**FOXCONN**  
**FOXCONN PCEG**

File: **M2-CTRL/MISC**  
 Size C Document Number: **RS690M02** Rev 1.0  
 Date: Tuesday, September 11, 2007 Sheet 10 of 38

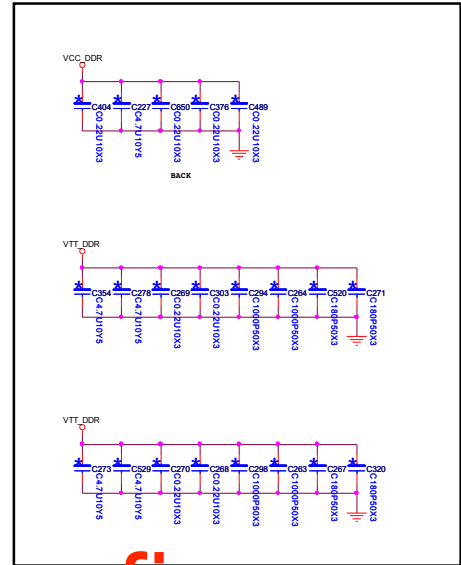
# Processor Power & Ground



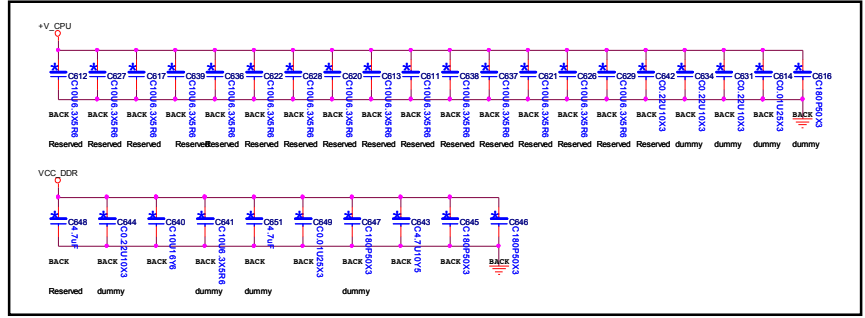
VLT\_RUN\_B is connected to the VLT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Decoupling Between Processor and DIMMs  
Place as close to processor as possible.



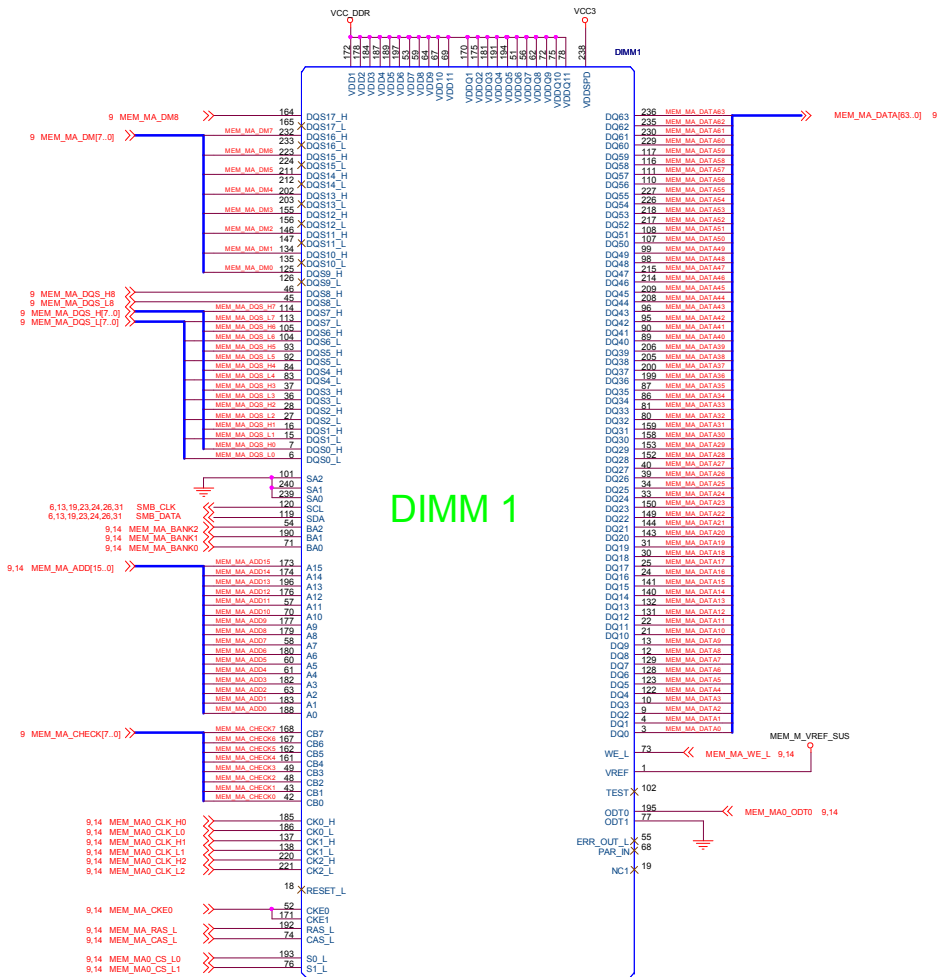
## Bottomside Decoupling



**FOXCONN**  
FOXCONN PCEG

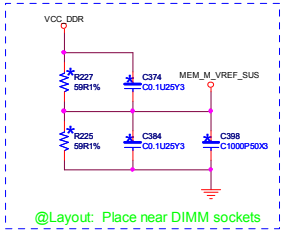
File: **M2-Power/Gnd**  
Size: **C** Document Number: **RS690M02** Rev: **1.0**  
Date: **Tuesday, September 11, 2007** Sheet: **11** of **38**

# DDRII CHANNEL A



DIMM 1

MEM\_M\_VREF\_SUS

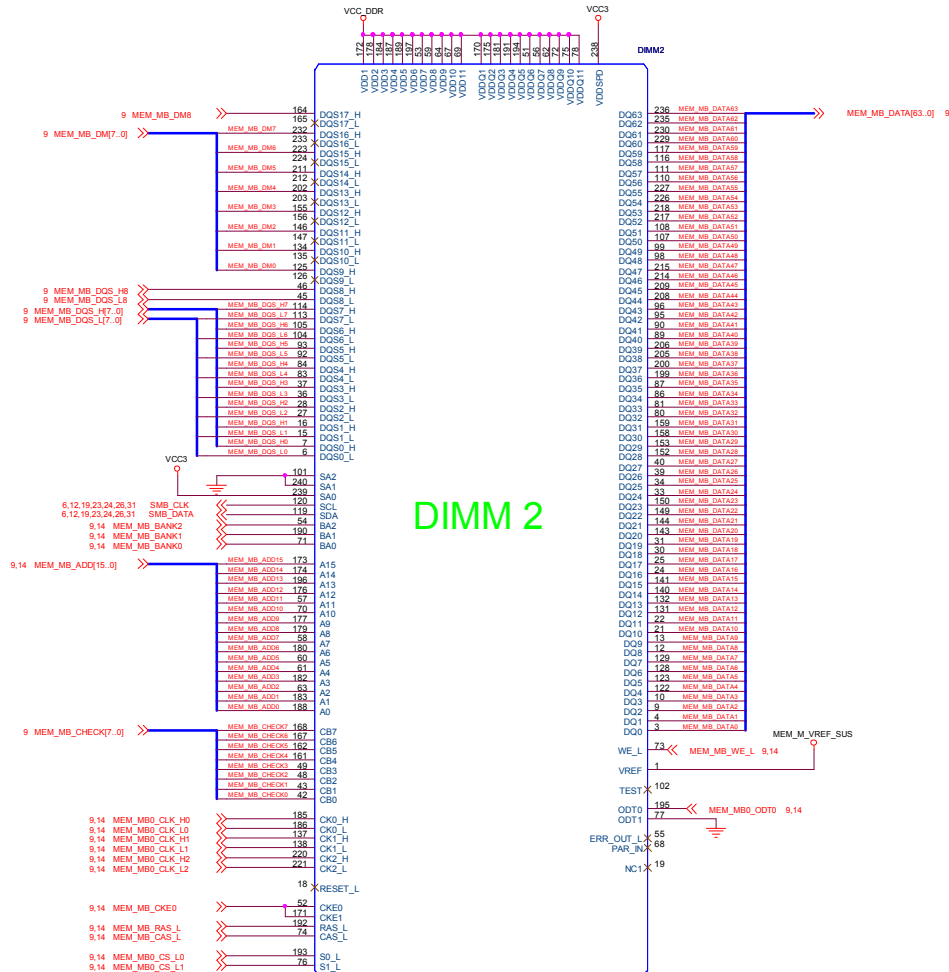


@Layout: Place near DIMM sockets

**FOXCONN**  
**FOXCONN PCEG**

File: **DDRII-CHA/DIMM 1**  
 Size C Document Number: **RS690M02** Rev 1.0  
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# DDRII CHANNEL B



DIMM 2

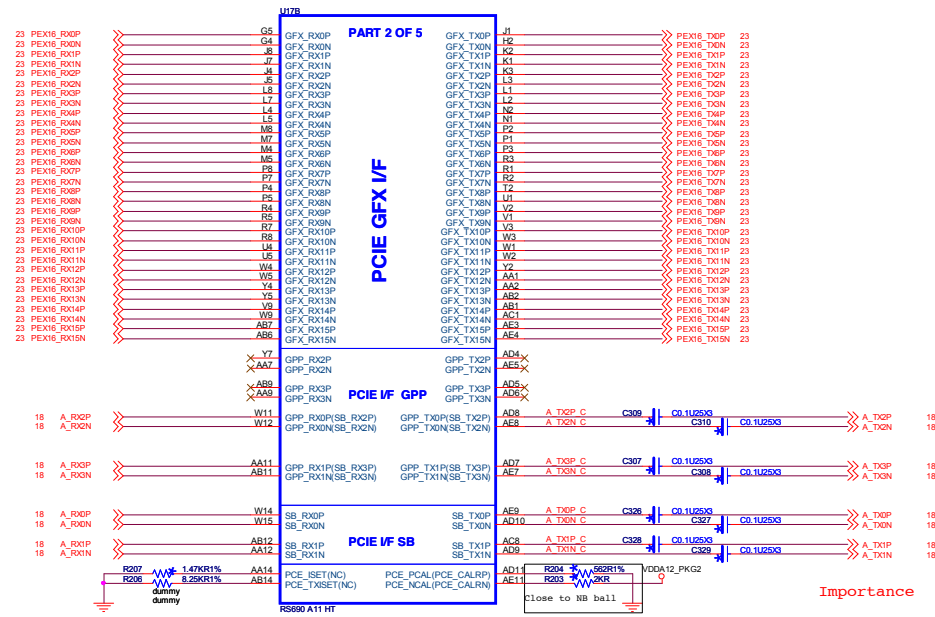
**FOXCONN**  
**FOXCONN PCEG**

File: **DDRII-CHB/DIMM 2**

Size C Document Number: **RS690M02** Rev 1.0

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**FOXCONN**

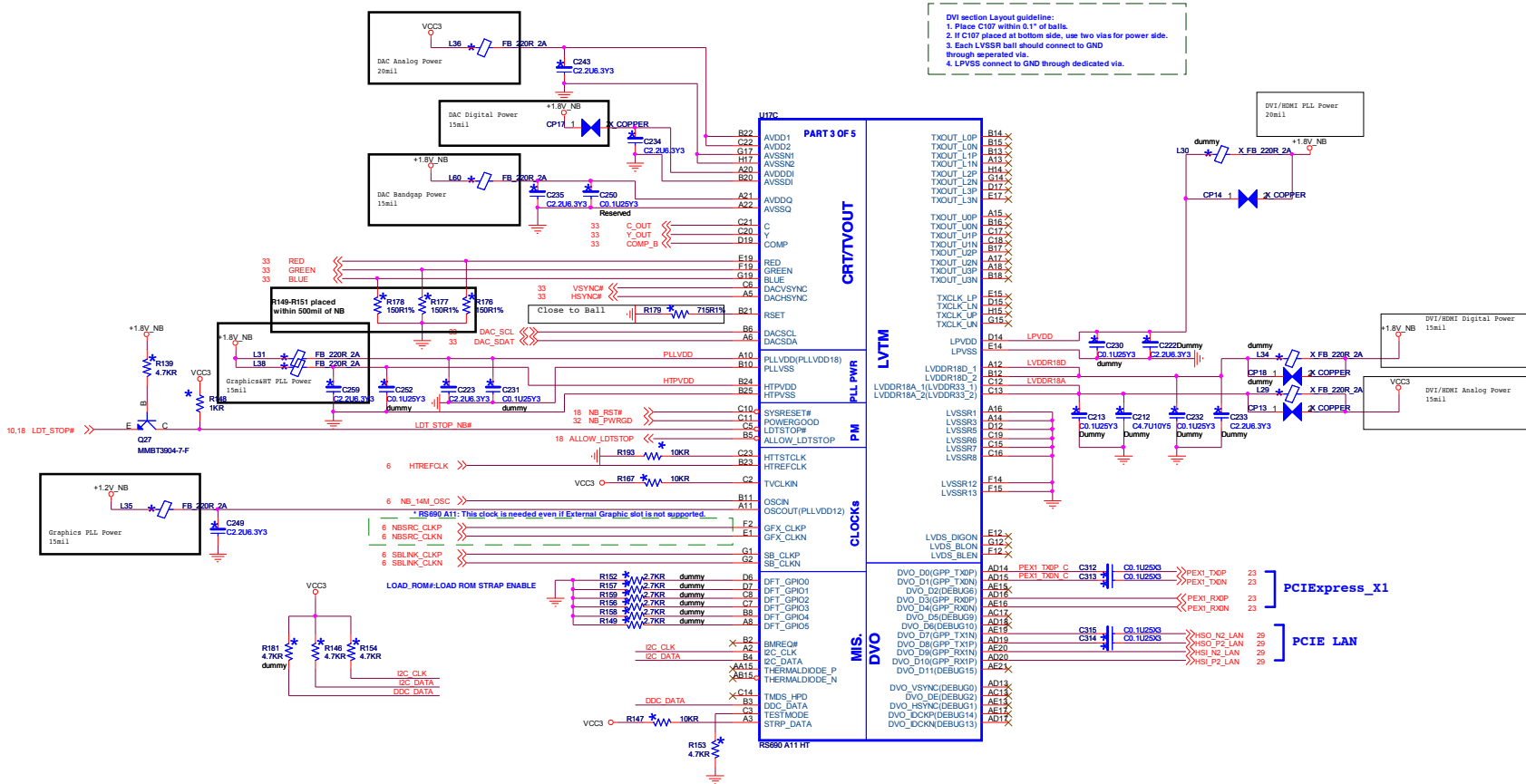
**FOXCONN PCEG**

Title: **RS690-HT/PCIe**

Document Number: **RS690M02**

Rev: 1.0

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		RS690 only (NC for RS485)			
		DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Bypass the loading of EEPROM straps and use Hardware default values	Memory side port not available	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1-1 Config E		Enable debug bus via the memory IO pads, if available in the package  use default values
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	Memory side port available	others: register defined (register default to Config E)		use the memory data bus to output the debug bus

**FOXCONN**  
FOXCONN PCEG

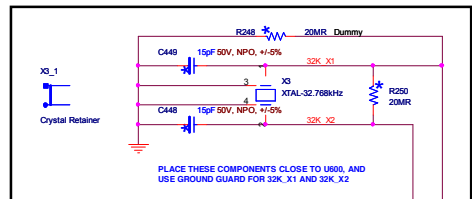
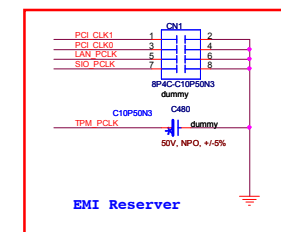
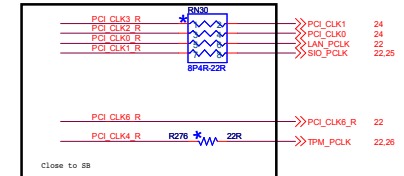
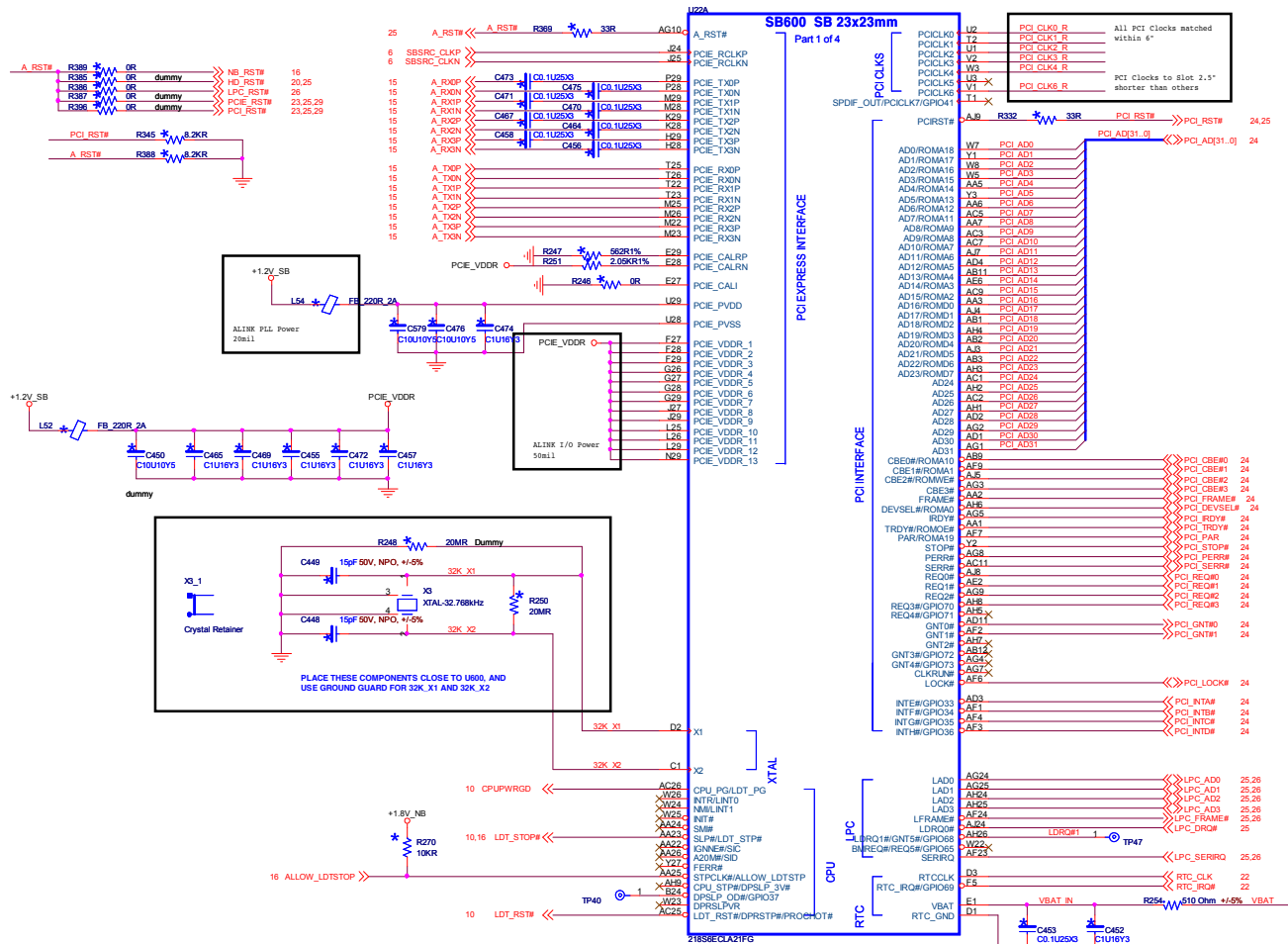
Title: **RS690-System**

Document Number: **RS690M02**

Rev: 1.0

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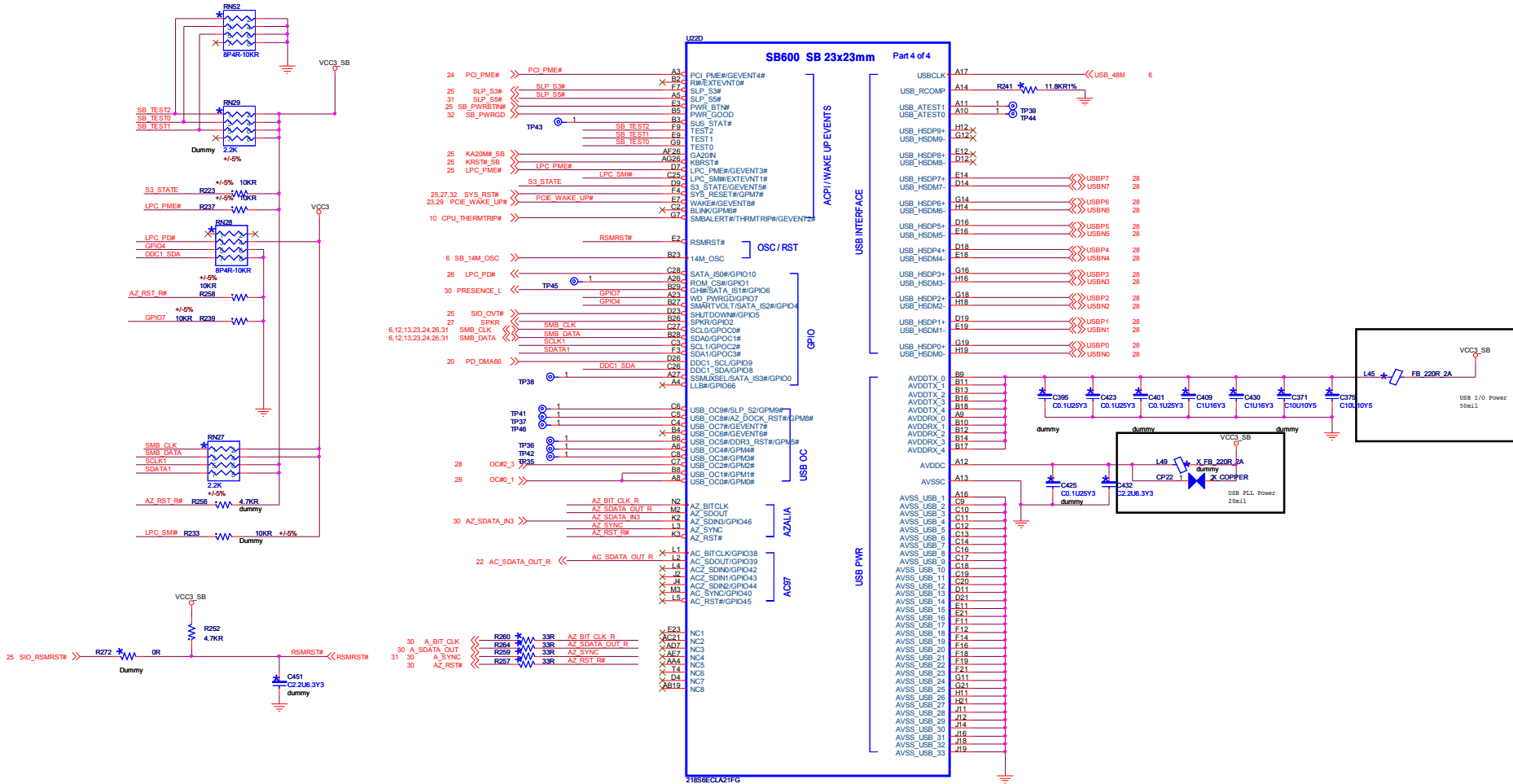


**JUMPER SETTING**

CLR_CMOS	Clone define	
(1-2)	CLEAR	
(2-3)	NORMAL	

**FOXCONN**  
FOXCONN PCEG

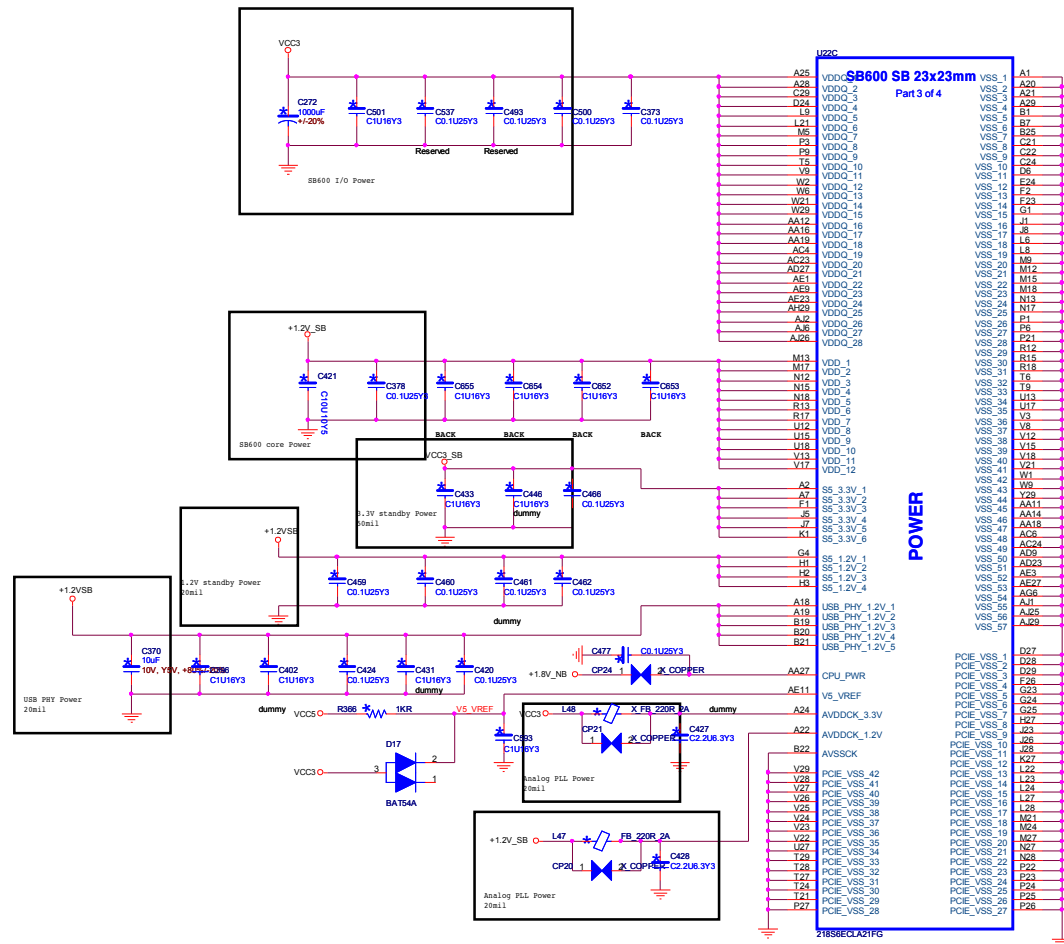
File: **SB600-CPU/PCIE/LPC/PCI**  
 Size C Document Number: **RS690M02** Rev 1.0  
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**FOXCONN**  
FOXCONN PCEG

File: **SB600-USB/Azalia/GPIO**  
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**POWER**

**FOXCONN**  
FOXCONN PCEG

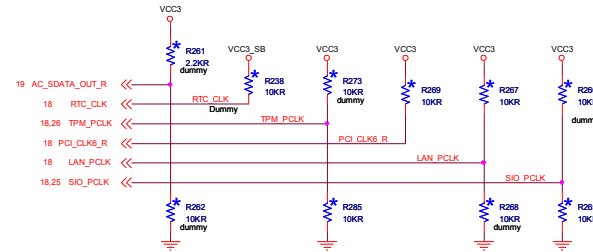
File: **SB600-Power/Decoupling**

Size C Document Number: **RS690M02** Rev 1.0

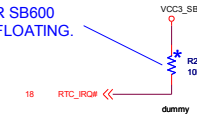
Date: Tuesday, September 11, 2007 Sheet 21 of 36

## REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT,  
15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS  
NOT REQUIRED;



NOTE: R98 PU RESISTOR FOR  
RTC\_IRQ# IS REQUIRED FOR SB600  
TO KEEP THE INPUT FROM FLOATING.



	AC_SDOUT	RTC_CLK	TPM_PCLK	LPC_PCLK	LAN_PCLK	SIO_PCLK
<b>PULL HIGH</b>	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM L, L = SPI ROM	DEFAULT
<b>PULL LOW</b>	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	L, H = LPC ROM L, L = FW ROM	

## DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

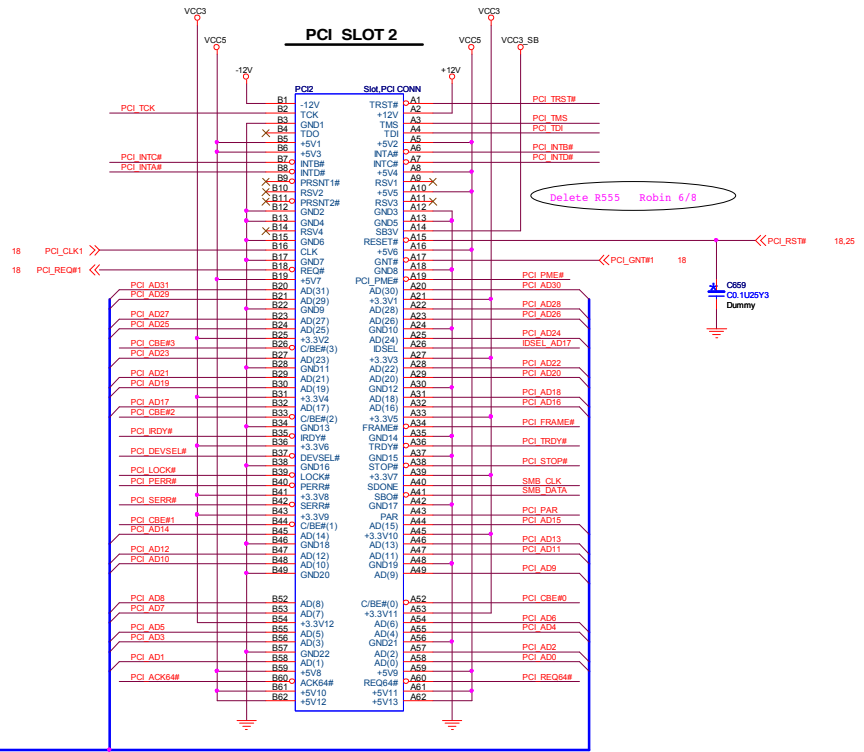
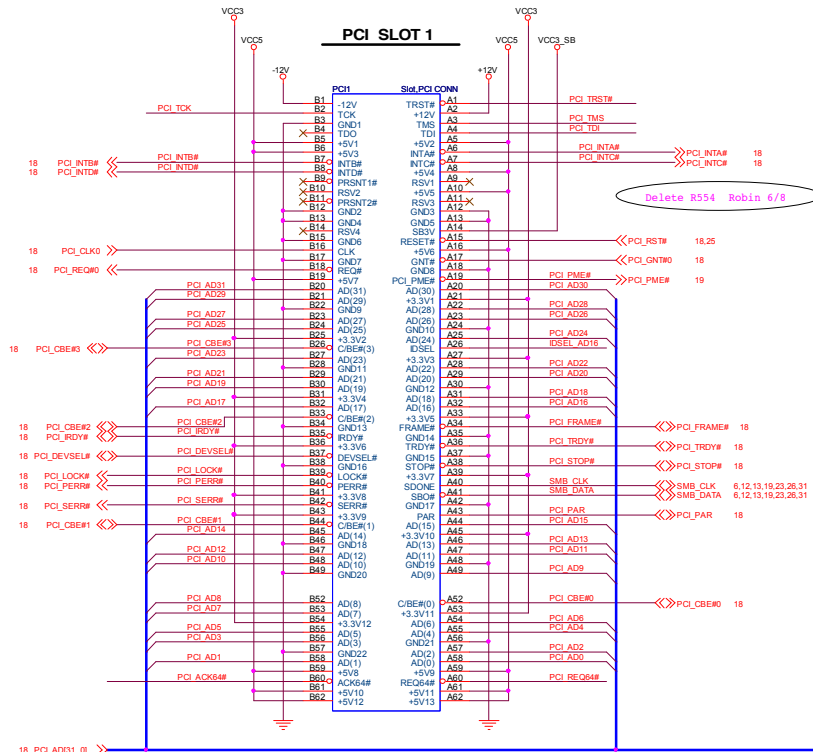
**FOXCONN®**  
FOXCONN PCEG

File: **SB600-Strapping**

Size C Document Number: **RS690M02** Rev 1.0

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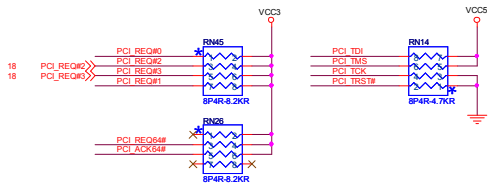


**IDSEL = AD16**  
**MASTER = PCI\_REQ#0**  
**PCI\_INTA#**

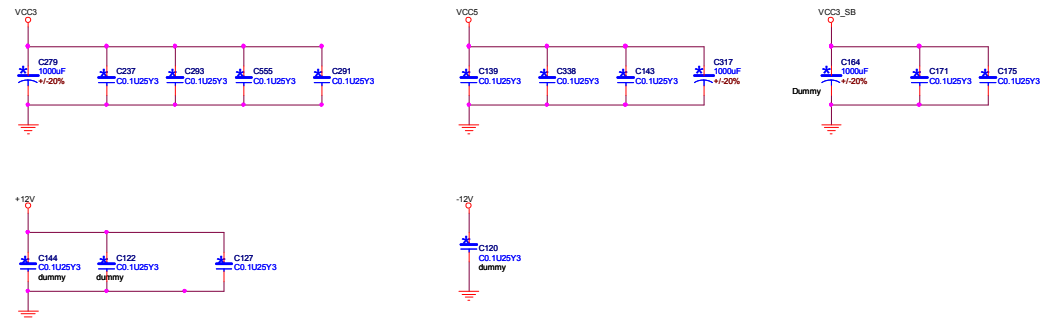
PCI AD16 R145 \*W100R IDSEL AD16  
 PCI AD17 R144 \*W100R IDSEL AD17

**IDSEL = AD17**  
**MASTER = PCI\_REQ#1**  
**PCI\_INTB#**

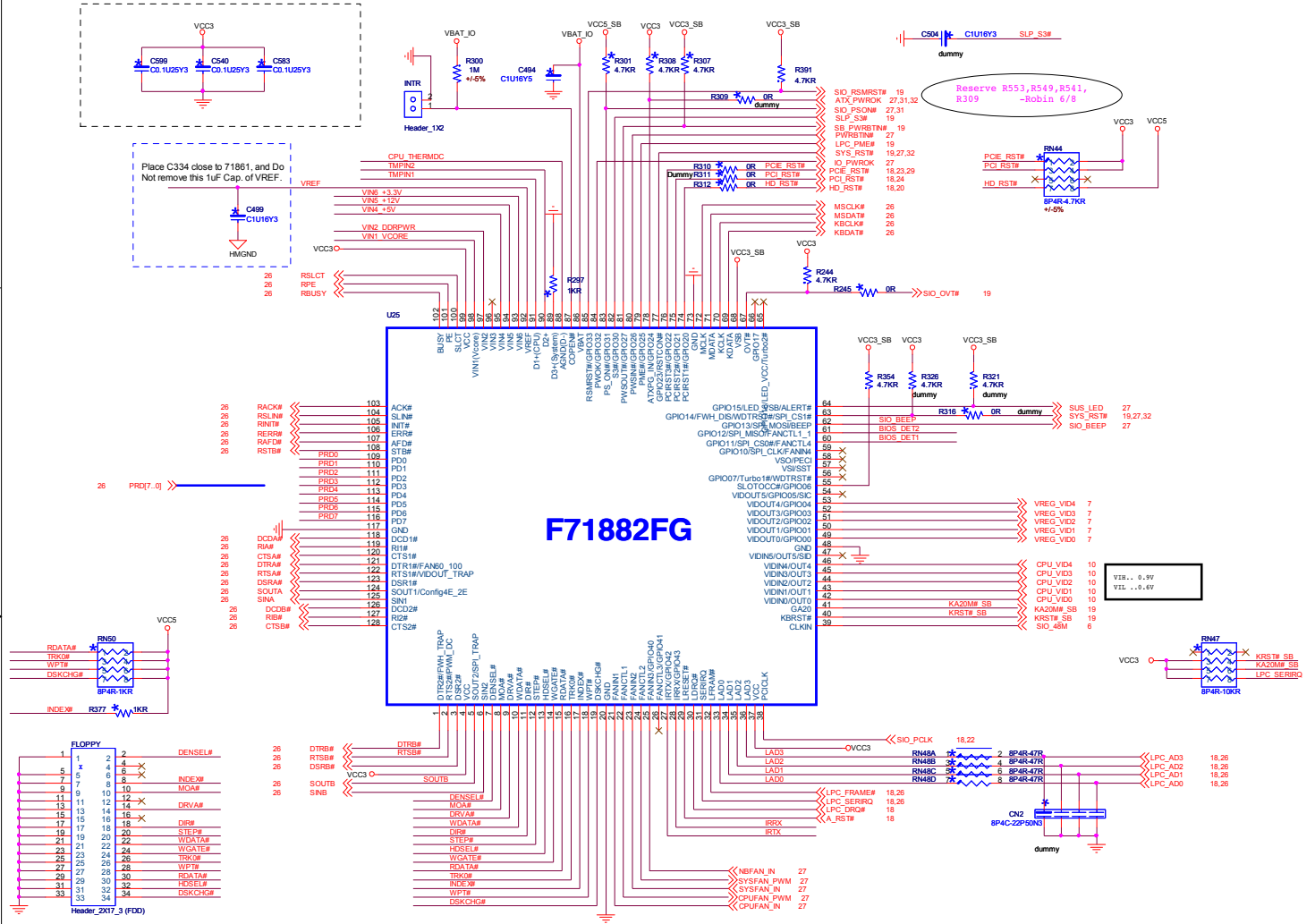
**PCI PULL-UP / DOWN RESISTORS**



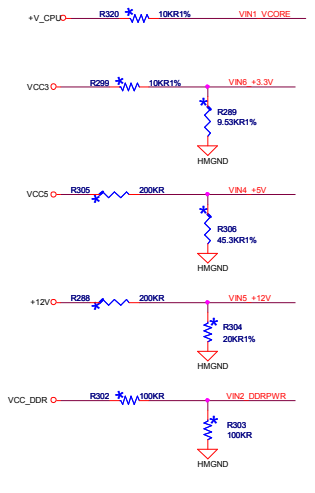
**PCI SLOT DECOUPLING CAPACITORS**



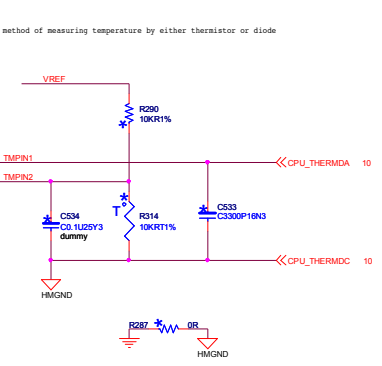
**FOXCONN**  
**FOXCONN PCEG**  
 Title: **PCI Slot 1 & 2**  
 Size C Document Number: **RS690M02** Rev: 1.0  
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### HW Monitor

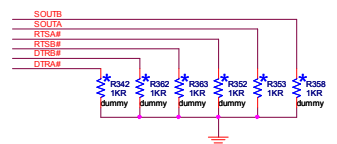


### Temperature Monitor



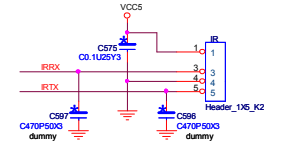
Choosing method of measuring temperature by either thermistor or diode

### Power on Strapping



	Dummy	Stuff
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
SOUTB/DTRB#	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN_START DUTY 60%	FAN_START DUTY 100%

### IR Connector

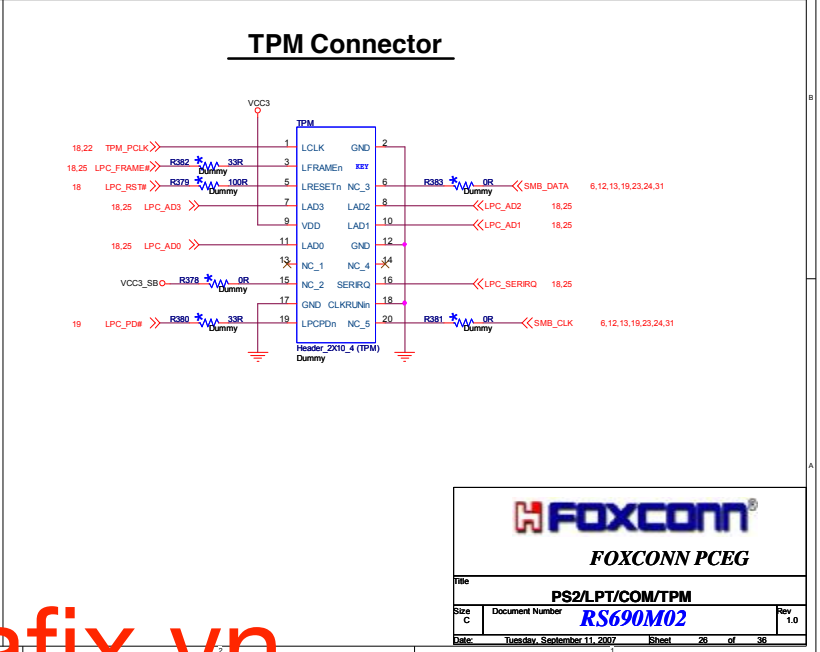
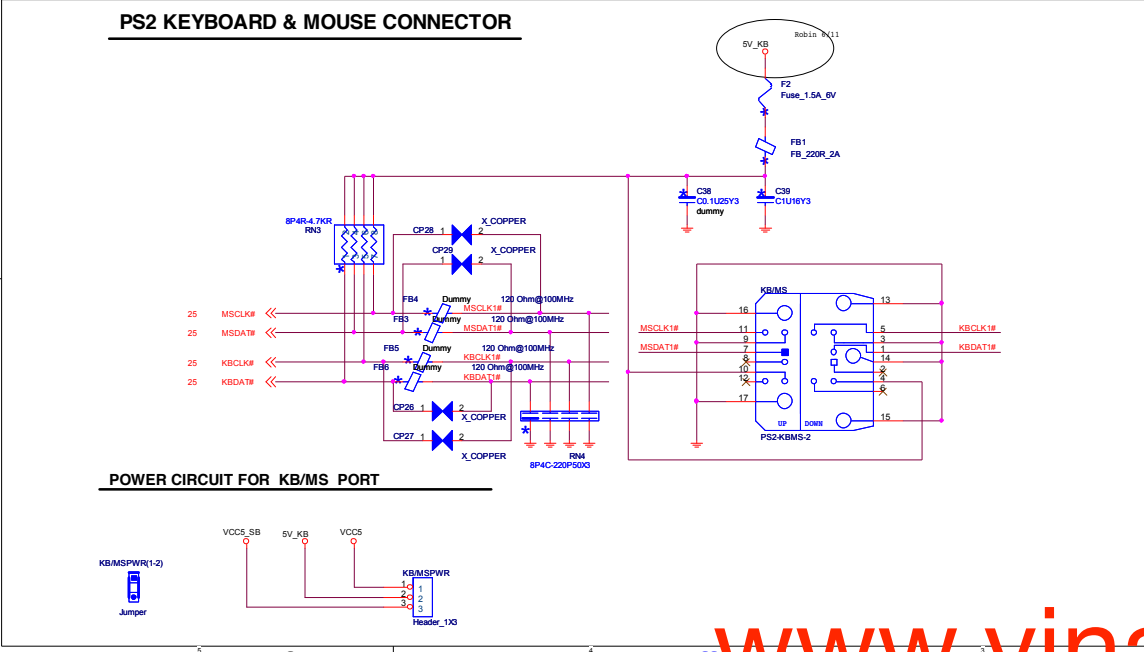
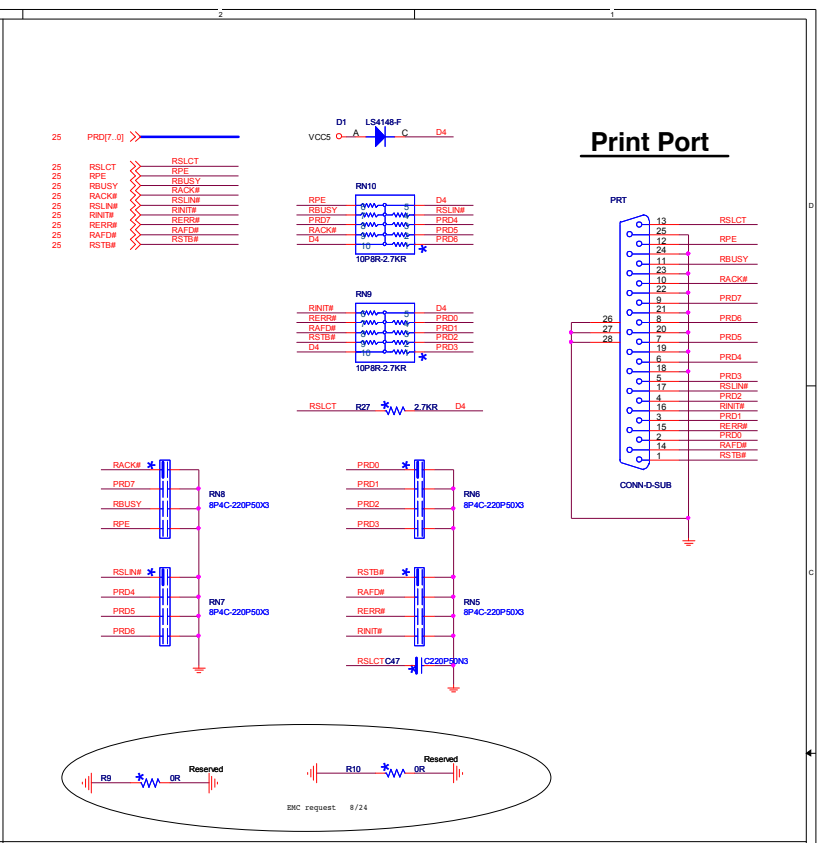
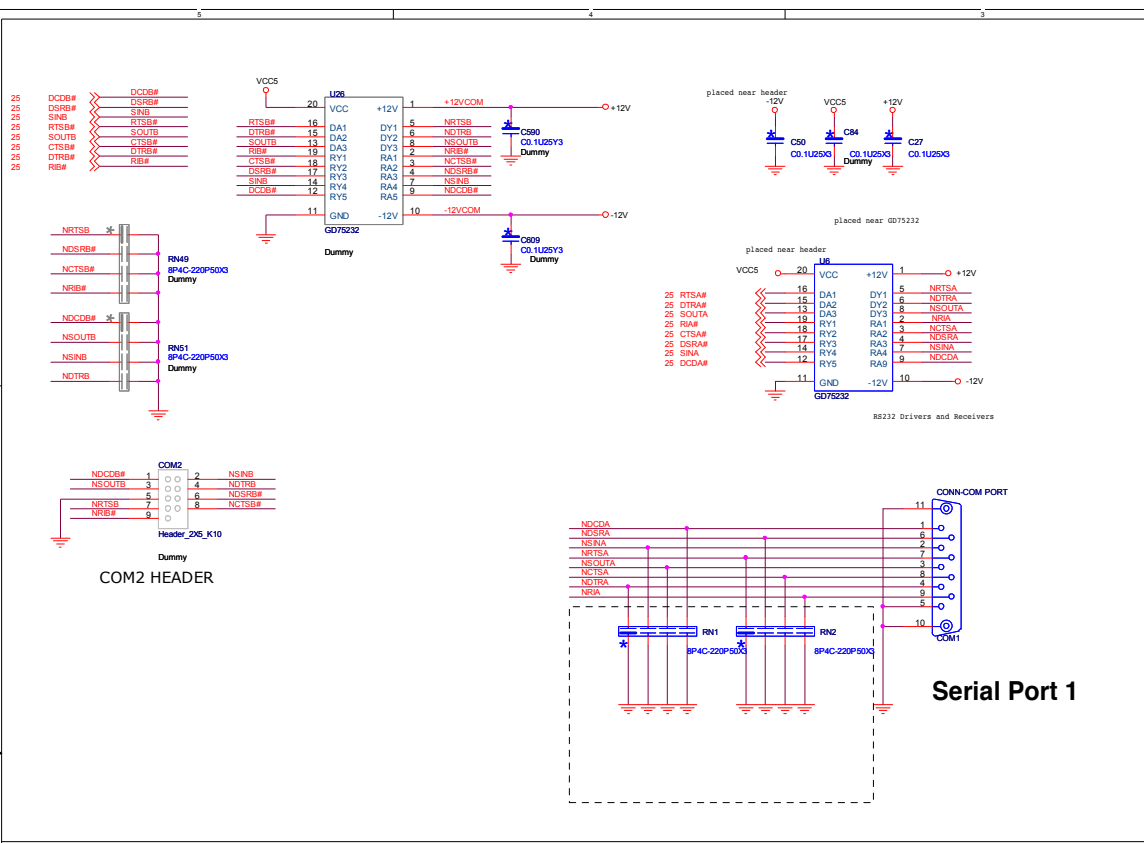


File: **SIO-F71882/FDD/LPC/TPM**

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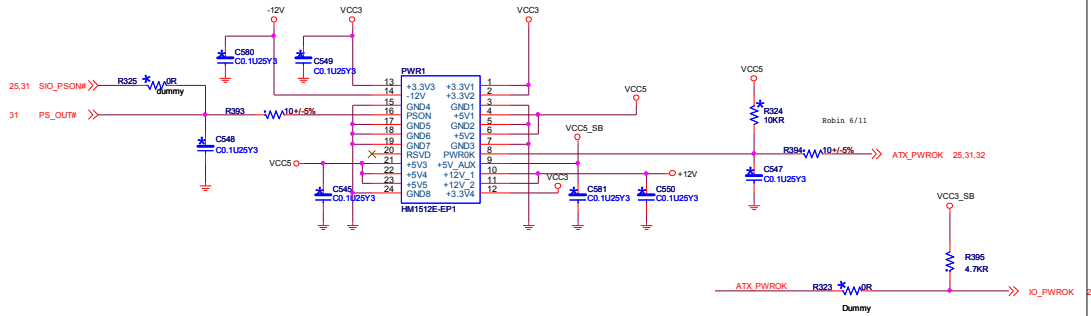
**FOXCONN PCEG**

File: **PS2/LPT/COM/TPM**

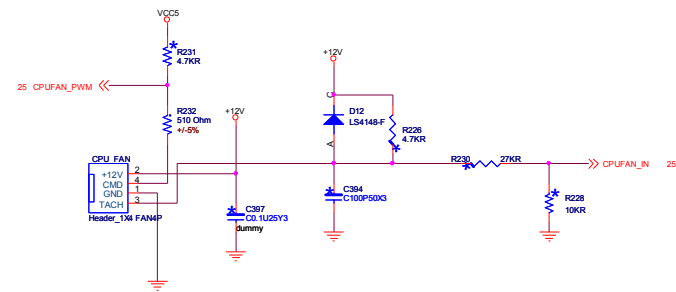
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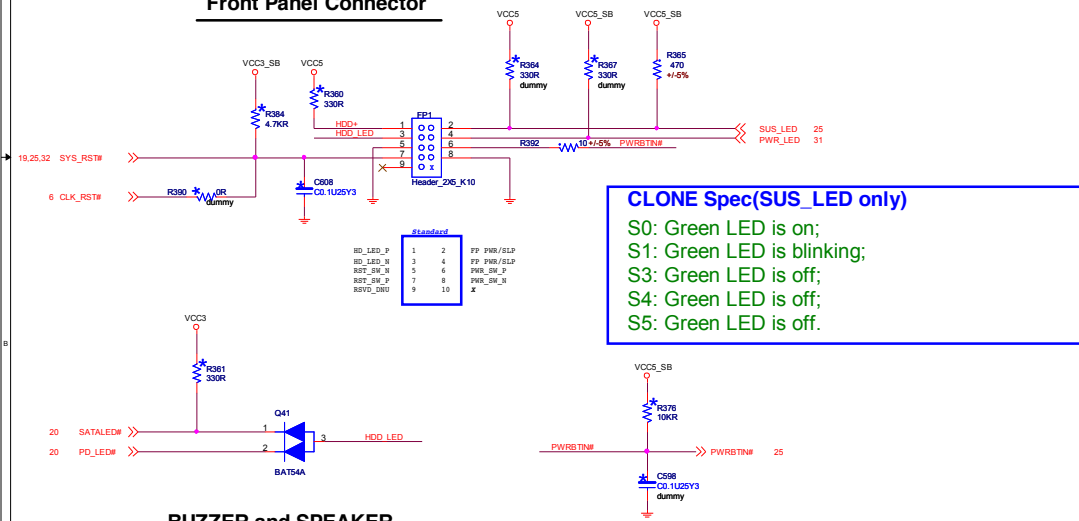
## ATX Connector



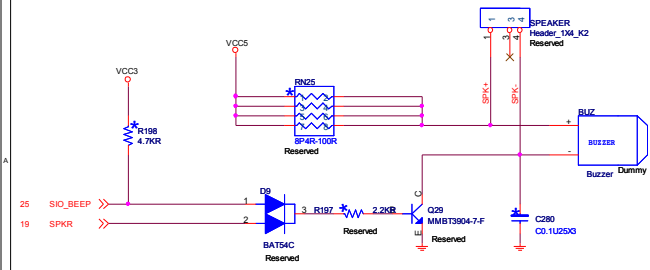
## CPU FAN



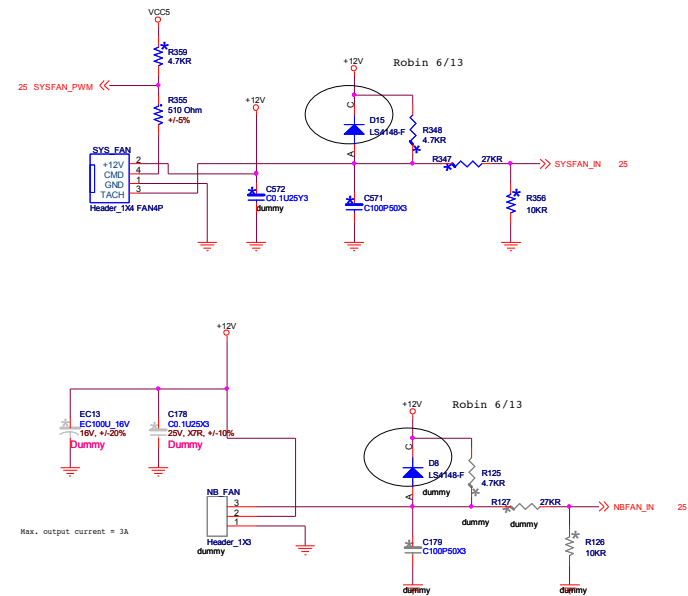
## Front Panel Connector



## BUZZER and SPEAKER



## SYSTEM FAN



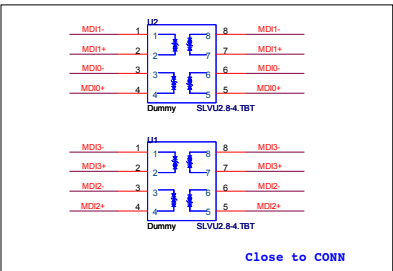
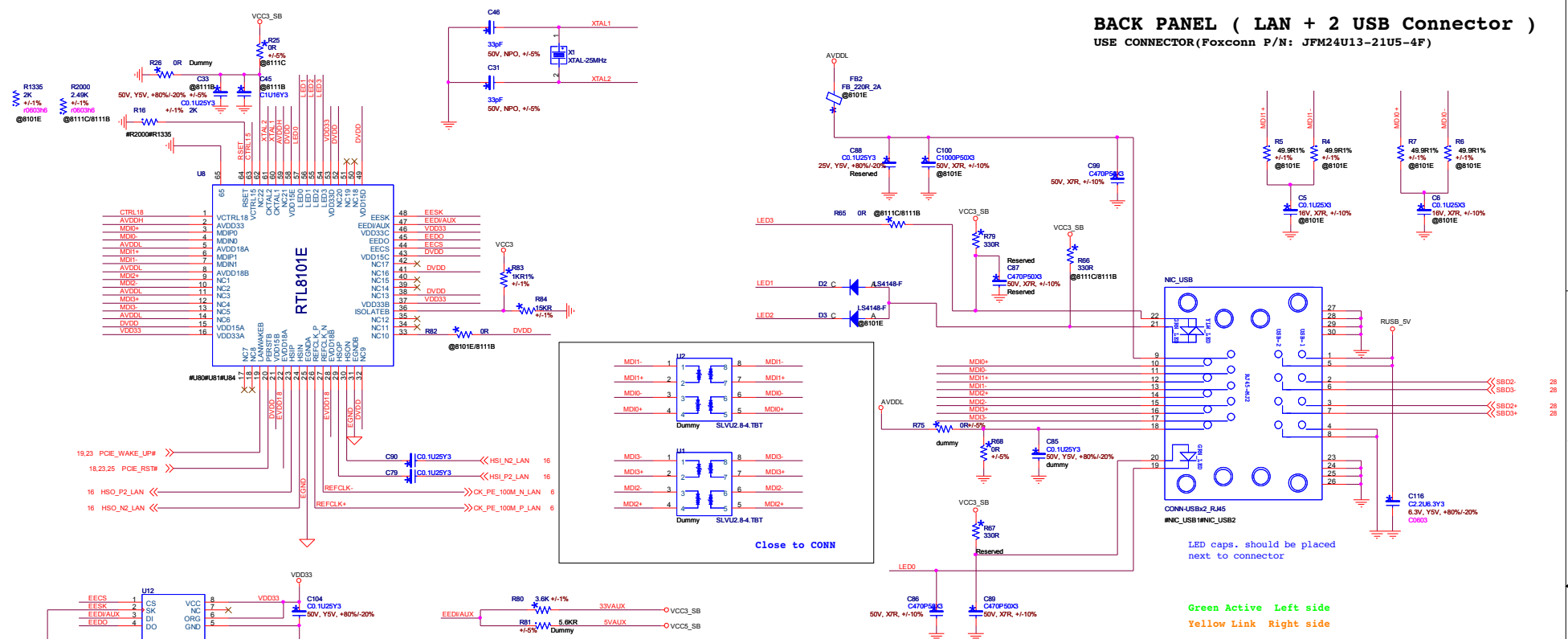


**FOXCONN PCEG**

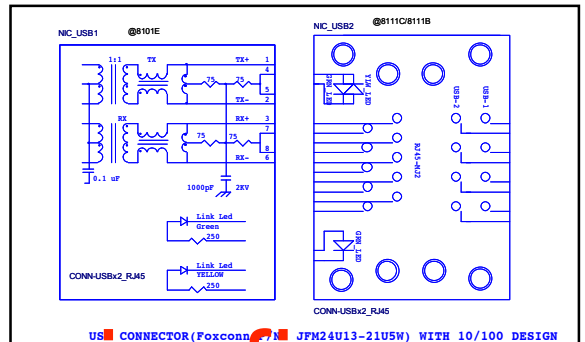
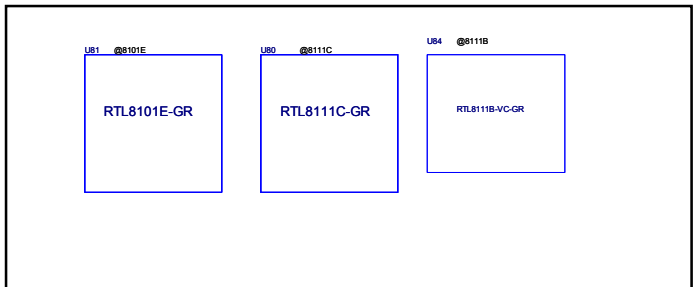
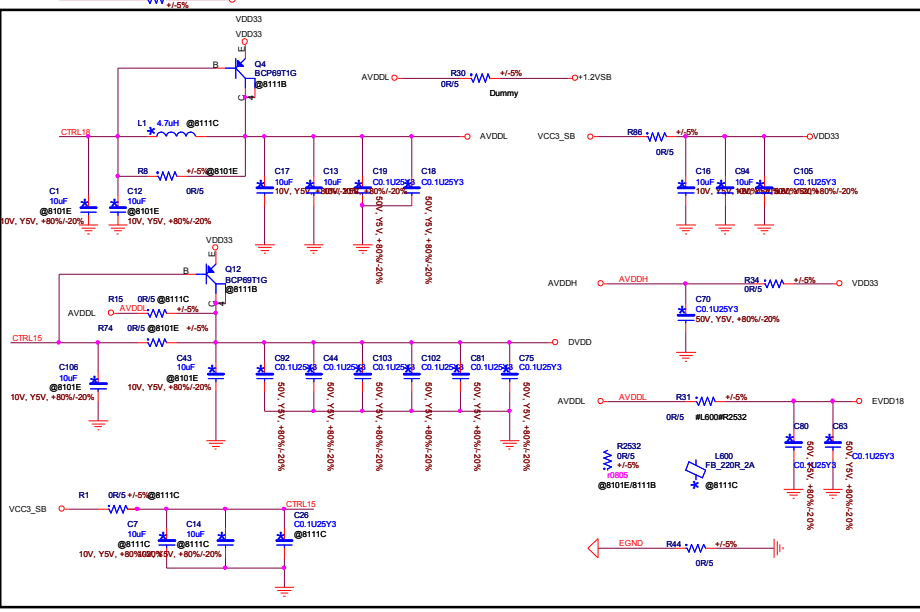
File	
ATX/Front Panel/Fan CTRL	
Size C	Document Number
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**BACK PANEL ( LAN + 2 USB Connector )**  
**USE CONNECTOR (Foxconn P/N: JFM24U13-21U5-4F)**



Green Active Left side  
 Yellow Link Right side



**FOXCONN PCEG**

File: LAN-RTL8101E/8111C  
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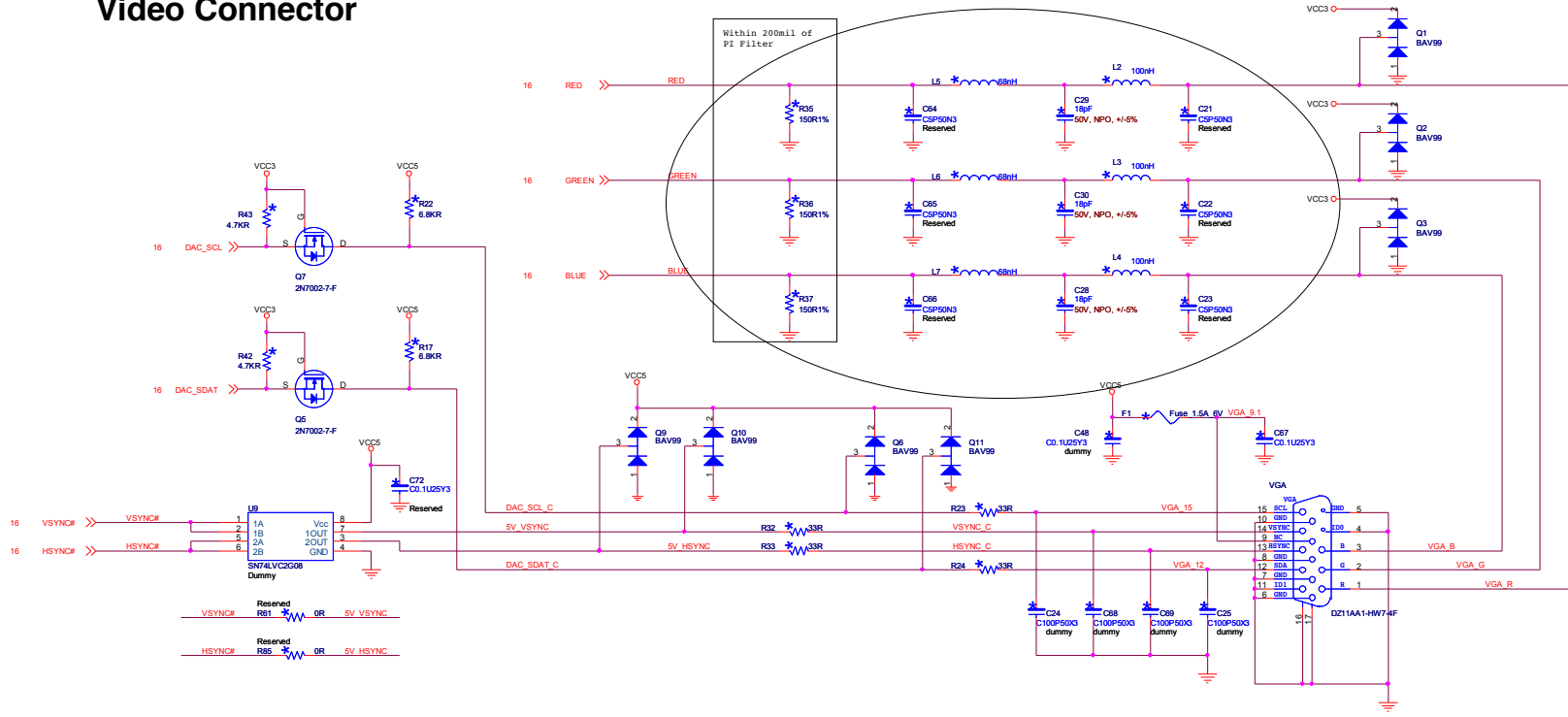




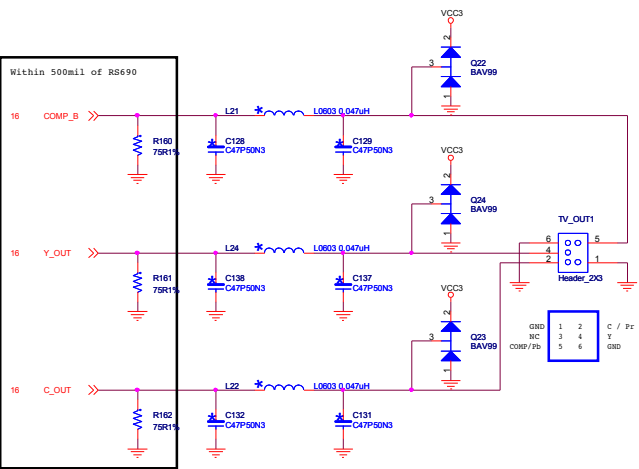


# Video Connector

Change L2, L3, L4 from dummy to 0.1uH inductor; Change C21, C22, C23 from dummy to 5pf; Change C29, C30, C31 from 3.3pf to 18pf; Change C64, C65, C66 from dummy to 5pf; EMC request

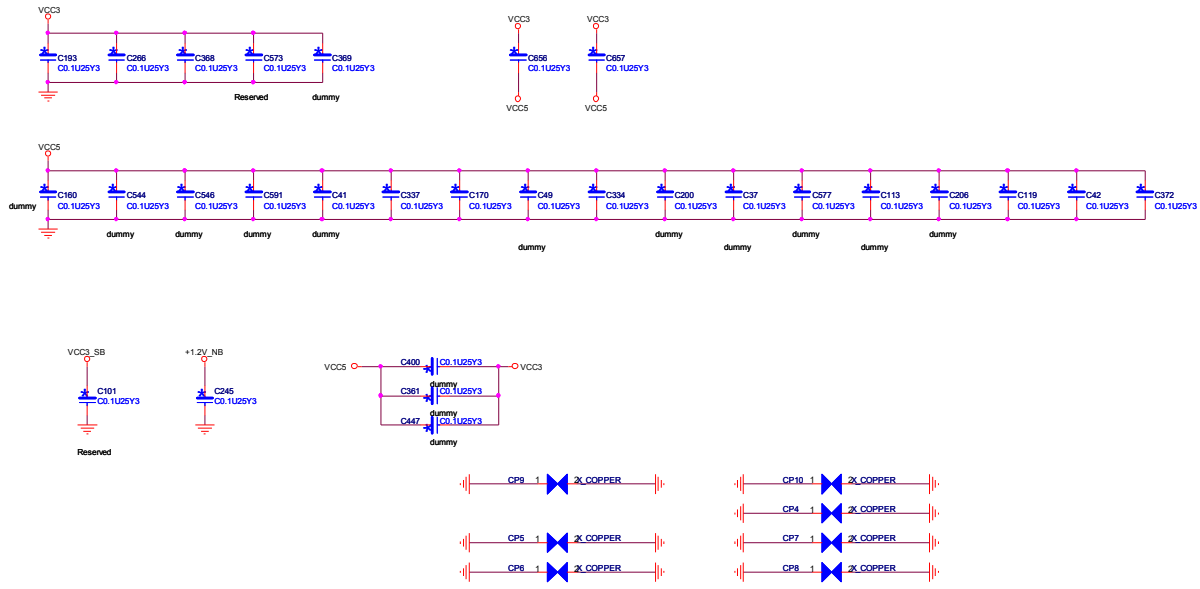


# TV-OUT Connector

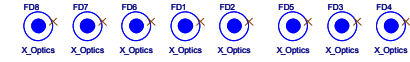


**FOXCONN**  
FOXCONN PCEG

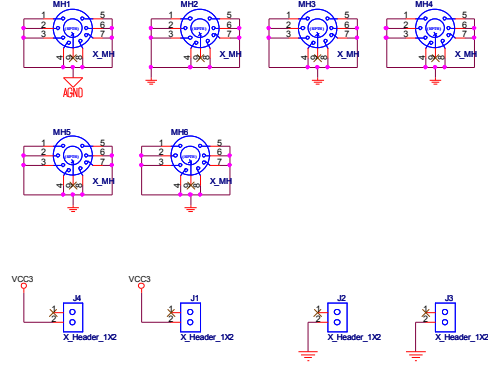
File: **D-Sub/DW/TV-OUT Connector**  
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**Optics Orientation Holes**



**Mounting Holes**



**FOXCONN**  
FOXCONN PCEG

File: **EMI Reserved/F Audio**

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## SB600

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO_[7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO_9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO_10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO_14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO_19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO_21
GPIO[22]	SLOCK		I/O	Core	Y		3.3V	GPI	GPIO_22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO_36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO_37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO_38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO_39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO_48
GPIO[49]	CPUPWRGD		I/O	V CPU IO				Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	PCI_REQ#0 PCI_GNT#0	PCI_AD16	PCI_CLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	PCI_REQ#1 PCI_GNT#1	PCI_AD17	PCI_CLK1
LAN	PCI_INTC#	PCI_REQ#2 PCI_GNT#2	PCI_AD20	LAN_PCLK
1394	PCI_INTD#	PCI_REQ#3 PCI_GNT#3	PCI_AD19	1394_PCLK

## PCI RESET DEVICE

Signals	Target
PCI_RST#	PCI_SLOT1&2, LAN, 1394
PCIE_RST#	PCI-E-16X & PCI-E-1X
NB_RST#	RS690
LPC_RST#	BIOS, TPM
HD_RST#	P-IDE
A_RST#	SIO

## DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0
		MCLK_A1/MCLK_A#1
		MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3
		MCLK_A4/MCLK_A#4
		MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0
		MCLK_B1/MCLK_B#1
		MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3
		MCLK_B4/MCLK_B#4
		MCLK_B5/MCLK_B#5

## JUMPER SETTING

CLR_CMOS	Clone define	TF define
(1-2)	CLEAR	NORMAL
(2-3)	NORMAL	CLEAR

	
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