S-series 14.0" Popeye & 15.6" Pebble

UMA/DIS Muxless Schematic
AMD TRINITY APU FS1r2
Thames Pro M2 package
FCH HUDSON M3

REV:1

2012-02-24

<Variant Name>

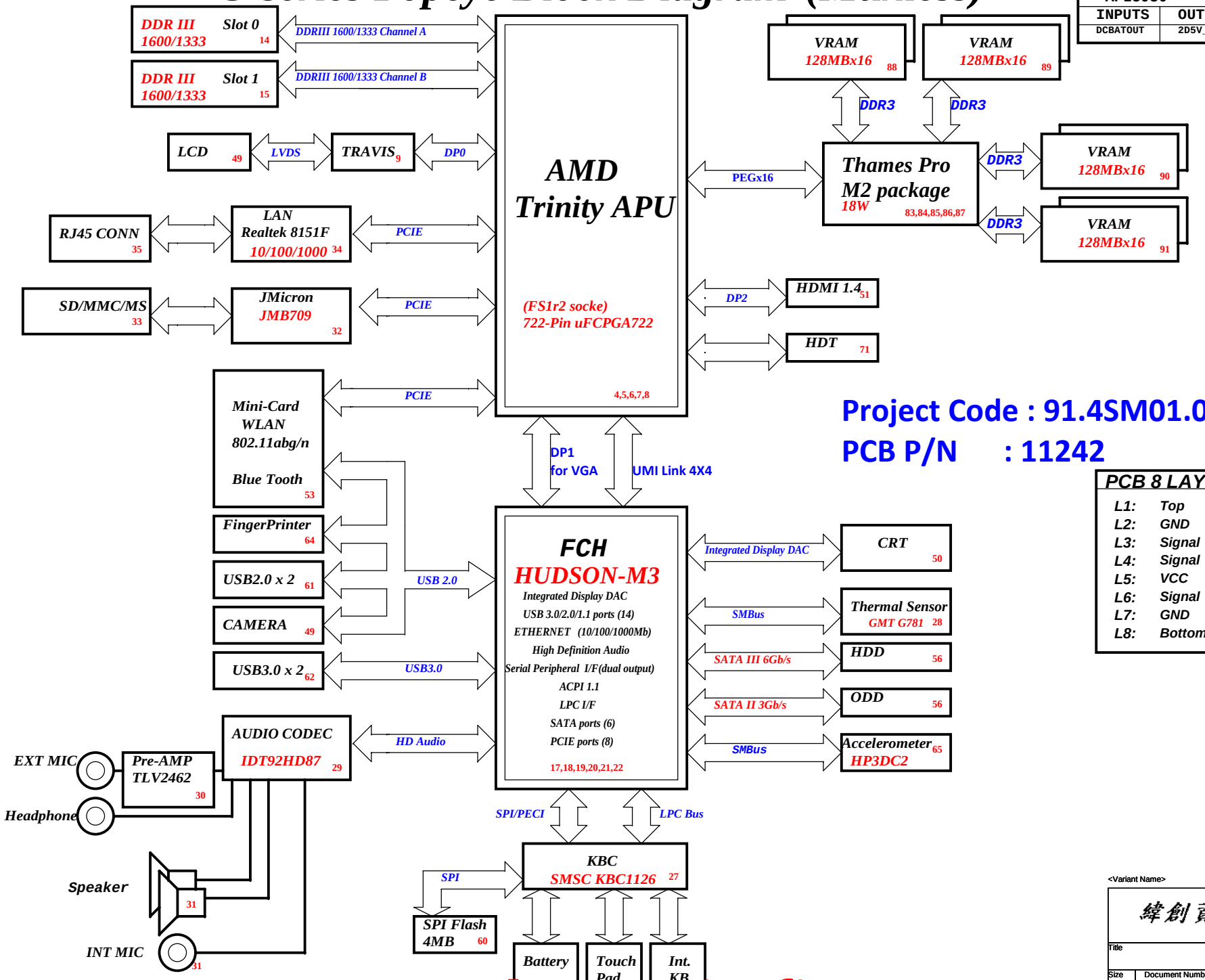
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size	Document Number	Rev
A4	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 1 of 103

S-series Popeye Block Diagram (Muxless)



Project Code : 91.4SM01.001

PCB P/N : 11242

SYSTEM DC/DC APL5930 48	
INPUTS	OUTPUTS
DCBATOUT	2D5V_S0

CPU DC/DC ISL6277 42~43	
INPUTS	OUTPUTS
DCBATOUT	APU_VDD

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S0

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

VGA UP1527 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC APL5930 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S3	1D8V_VGA_S0 1V_VGA_S0

SYSTEM DC/DC DMN3404 93	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

<Variant Name>

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Title: Block Diagram

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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S5+ feature

	S0	S3	S5(AC)	S5(DC)		
3D3V_AUX_S5	X	X	X	X	Used	EC
5V_AUX_S5	X	X	X	X	Used	Not used
15V_S5	X	X	X			
5V_S5	X	X	X			
3D3V_S5	X	X	X			
1D1V_S5	X	X	X			
1D5V_S3	X	X				
1D2V_S0	X					
2D5V_S0	X					
0D75V_S0	X					
APU_VDD	X					
APU_VDDNB	X					
5V_S0	X					
3D3V_S0	X					
1D5V_S0	X					
1D1V_S0	X					
3D3V_VGA_S0	X					
VGA_CORE	X					
1V_VGA_S0	X					
1D5V_VGA_S0	X					
1D8V_VGA_S0	X					

USB Table

USB2.0	
Pair	Device
0	USB 2.0 PORT 0 (Right side DB)
1	NA
2	WLAN (WLAN / BT COMBO)
3	USB 2.0 PORT 3 (Right side DB)
4	Camera
5	NA
6	NA
7	NA
8	NA
9	NA
10	NA
11	NA
12	USB 2.0 PORT 12 (USB3.0 CONN)
13	USB 2.0 PORT 13 (USB3.0 CONN)
14	NA
15	FINGER PRINTER

USB3.0	
Pair	Device
0	NA
1	NA
2	USB 3.0 PORT 2
3	USB 3.0 PORT 3

PCIe Routing

	APU PCIE
LANE0	LAN
LANE1	CardReader
LANE2	NA
LANE3	WLAN

	FCH PCIE
LANE0	NA
LANE1	NA
LANE2	NA
LANE3	NA

<Variant Name>

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Title: Table of Content

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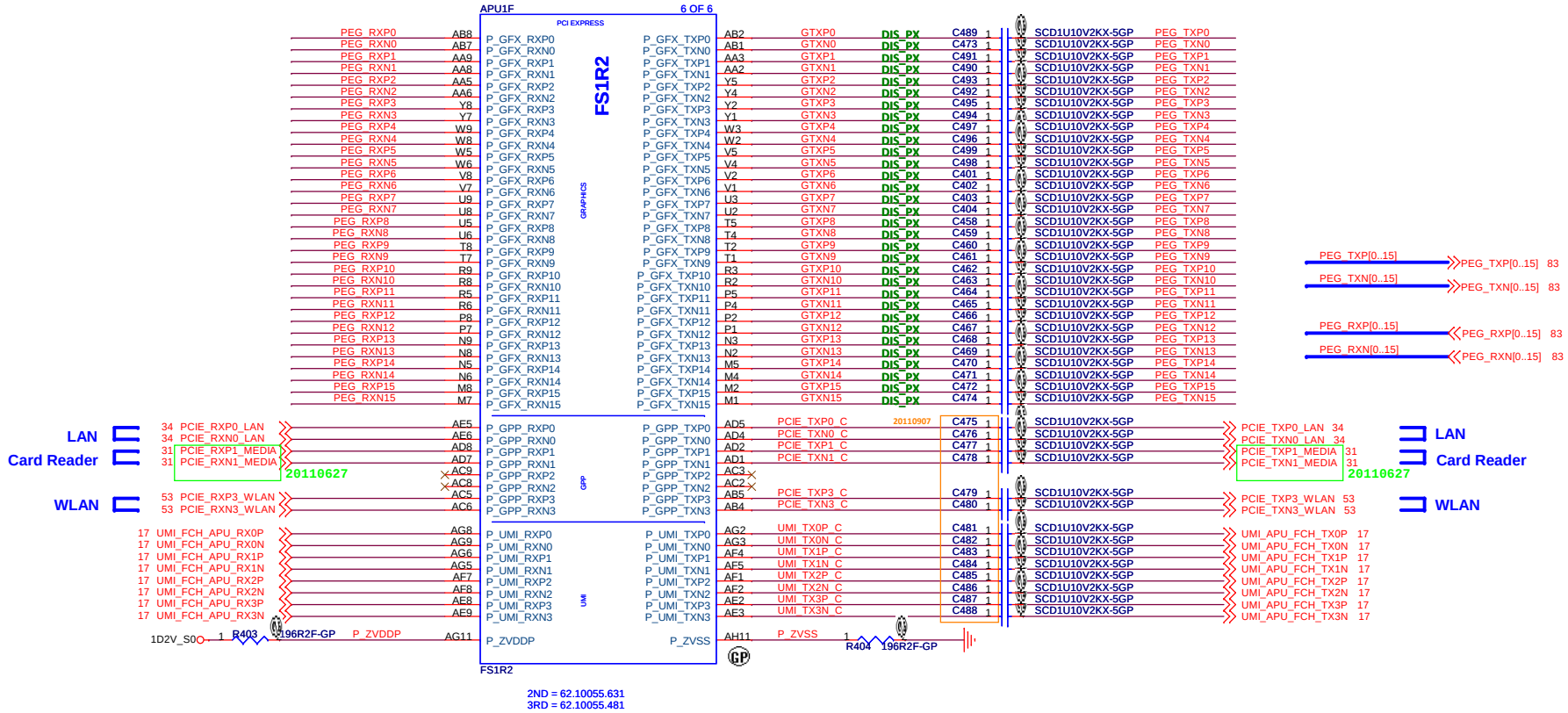
20110713 change to 16 lanes



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APU_PCIE(1/5)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SB

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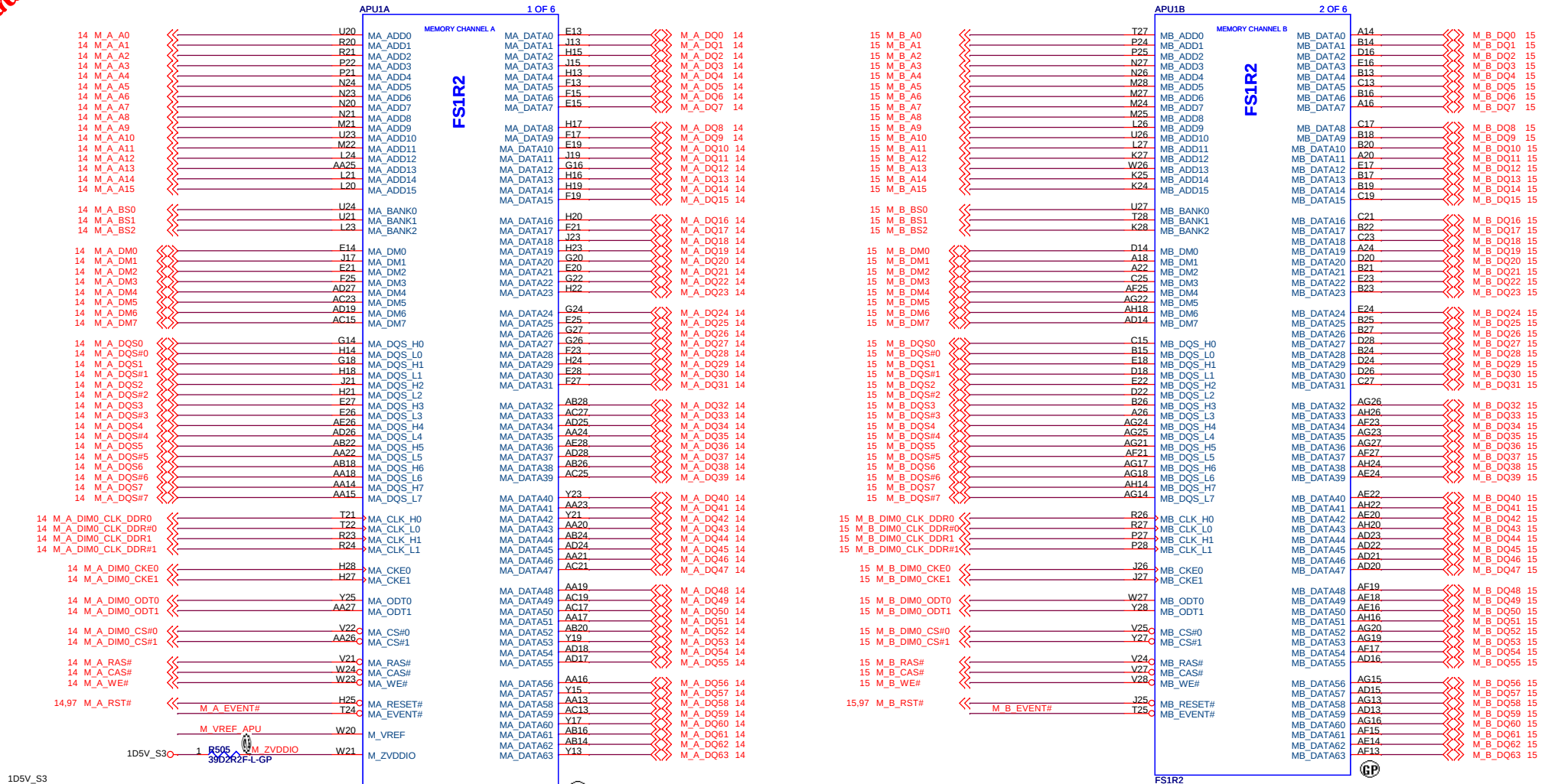

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: APU_DDR(2/5)

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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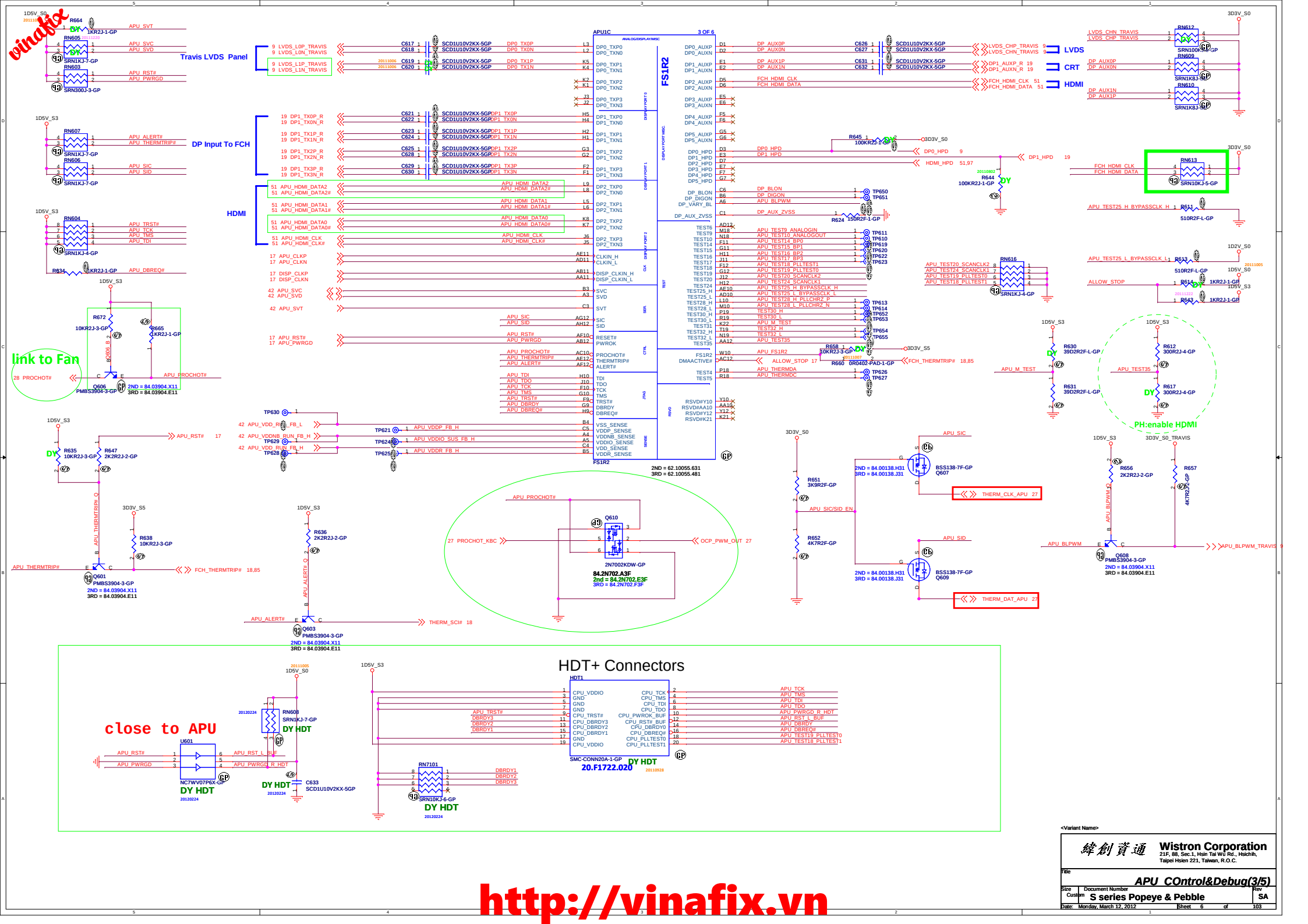
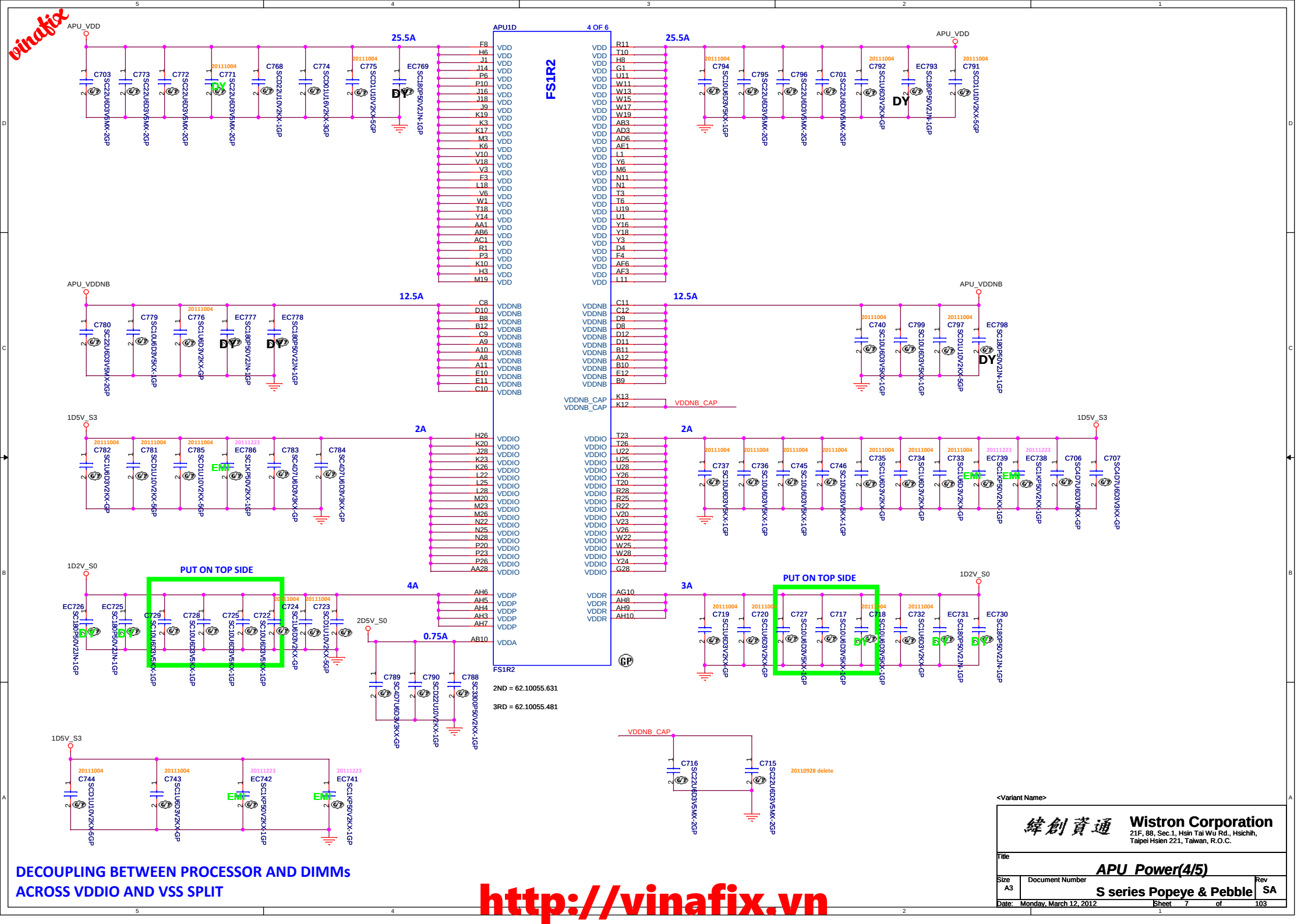
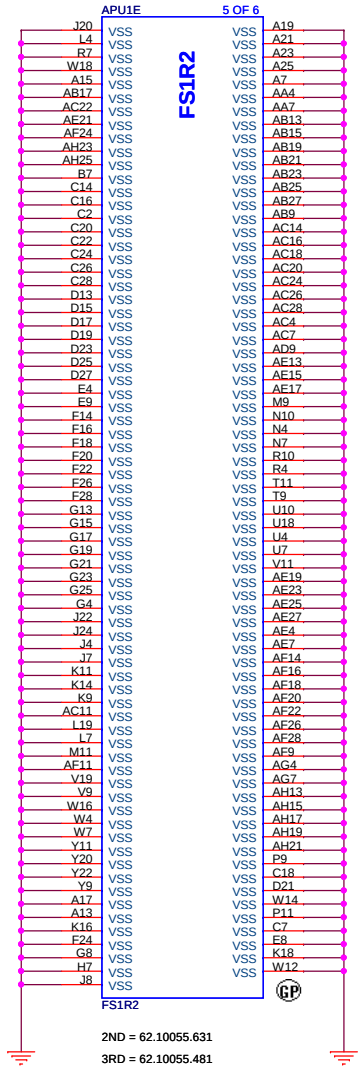

Travis LVDS Panel
DP Input To FCH
HDMI
link to Fan
close to APU
HDT+ Connectors
PH:enable HDMI
LVDS
CRT
HDMI
APU1C
FS1R2
3 OF 6
SCD1U10V2KX-5GP
SRN1KJ-7-GP
SRN300J-3-GP
SRN10KJ-5-GP
SRN1KJ-4-GP
SRN10KJ-6-GP
PMBS3904-3-GP
BSS138-7F-GP
2N7002KDW-GP
SMC-CONN20A-1-GP
NC7WV07P6X-GP
DY HDT
20.F1722.020
84.2N702.A3F
2nd = 84.2N702.E3F
3RD = 84.2N702.F3F
2ND = 62.10055.631
3RD = 62.10055.481
2ND = 84.03904.X11
3RD = 84.03904.E11
2ND = 84.00138.H31
3RD = 84.00138.J31
THERM_CLK_APU 27
THERM_DAT_APU 27
APU_BLPWM_TRAVIS 9
FCH_THERMTRIP# 18,85
THERM_SCI# 18
OCP_PWM_OUT 27
ALLOW_STOP 17
HDMI_HPD 51,97
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
APU_COntrol&Debug(3/5)
S series Popeye & Pebble
Monday, March 12, 2012
http://vinafix.vn


APU_VDD
25.5A
APU1D
4 OF 6
FS1R2
APU_VDDNB
12.5A
1D5V_S3
2A
1D2V_S0
PUT ON TOP SIDE
4A
2D5V_S0
0.75A
VDDNB_CAP
3A
2ND = 62.10055.631
3RD = 62.10055.481
20110928 delete
DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDIO AND VSS SPLIT
http://vinafix.vn
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
APU Power(4/5)
S series Popeye & Pebble
Monday, March 12, 2012



<Variant Name>

緯創資通 Wistron Corporation
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Title: APU_Power(5/5)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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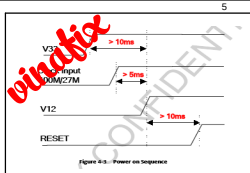
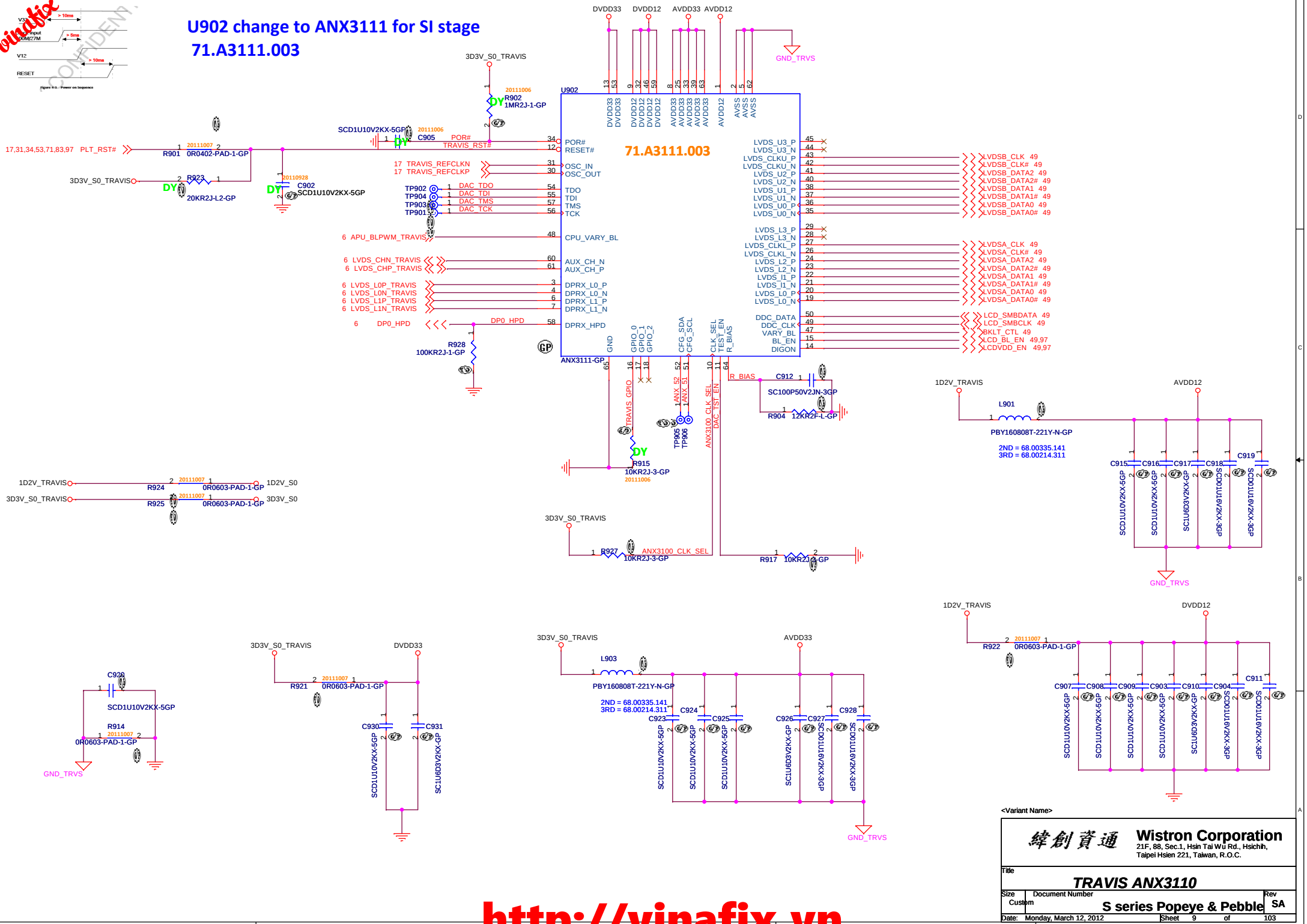


U902 change to ANX3111 for SI stage
71.A3111.003



Variant Name	
Company	緯創資通 Wistron Corporation, 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TRAVIS ANX3110
Size	Custom
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<Variant Name>

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Title
Reserved

Size	Document Number	Rev
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<Variant Name>

緯創資通 Wistron Corporation
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Title: *Reserved*

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A3	S series Popeye & Pebble	SA

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<Variant Name>

緯創資通 Wistron Corporation
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Title: *Reserved*

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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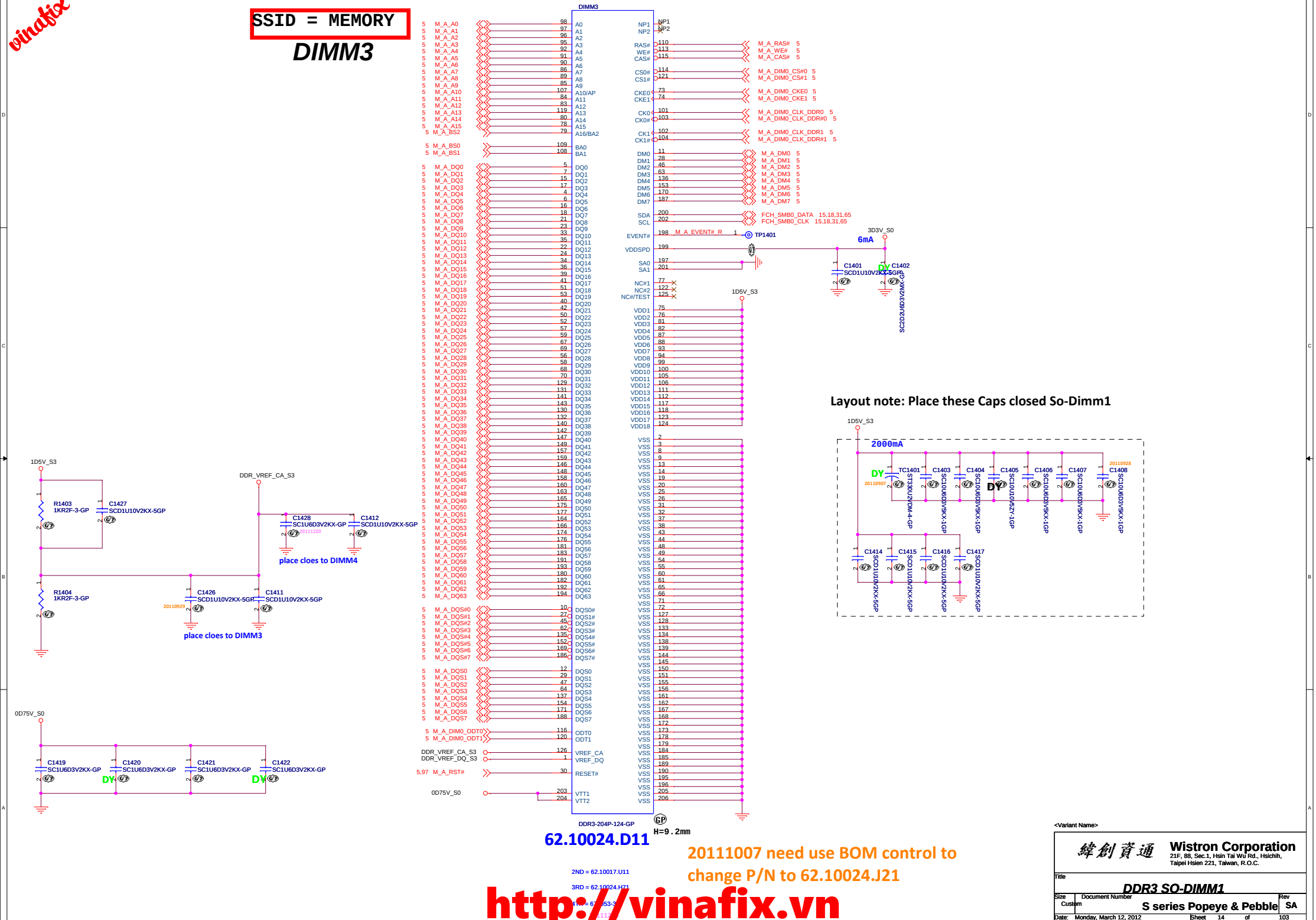
SSID = MEMORY

DIMM3



20111007 need use BOM control to change P/N to 62.10024.J21

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM1

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

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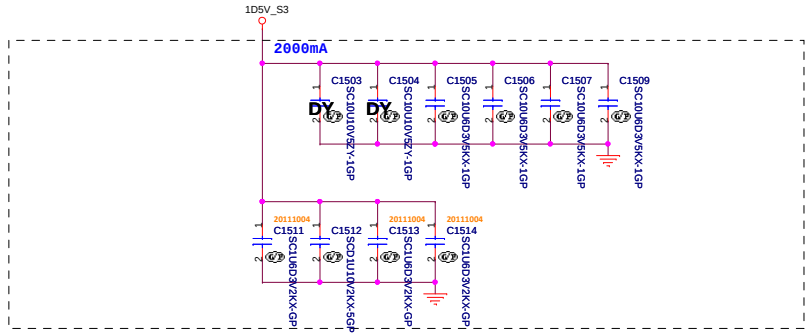
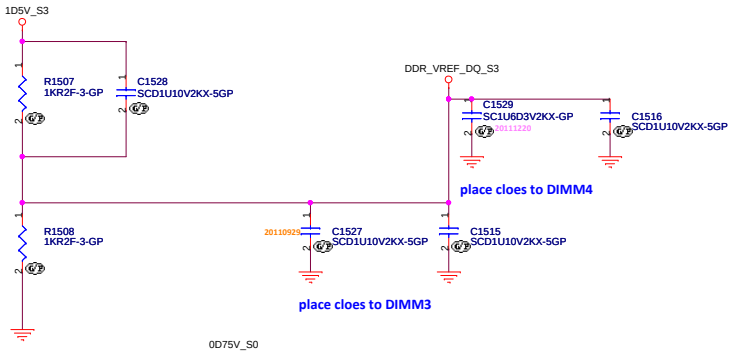
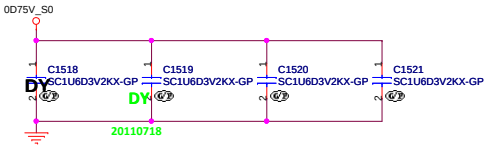
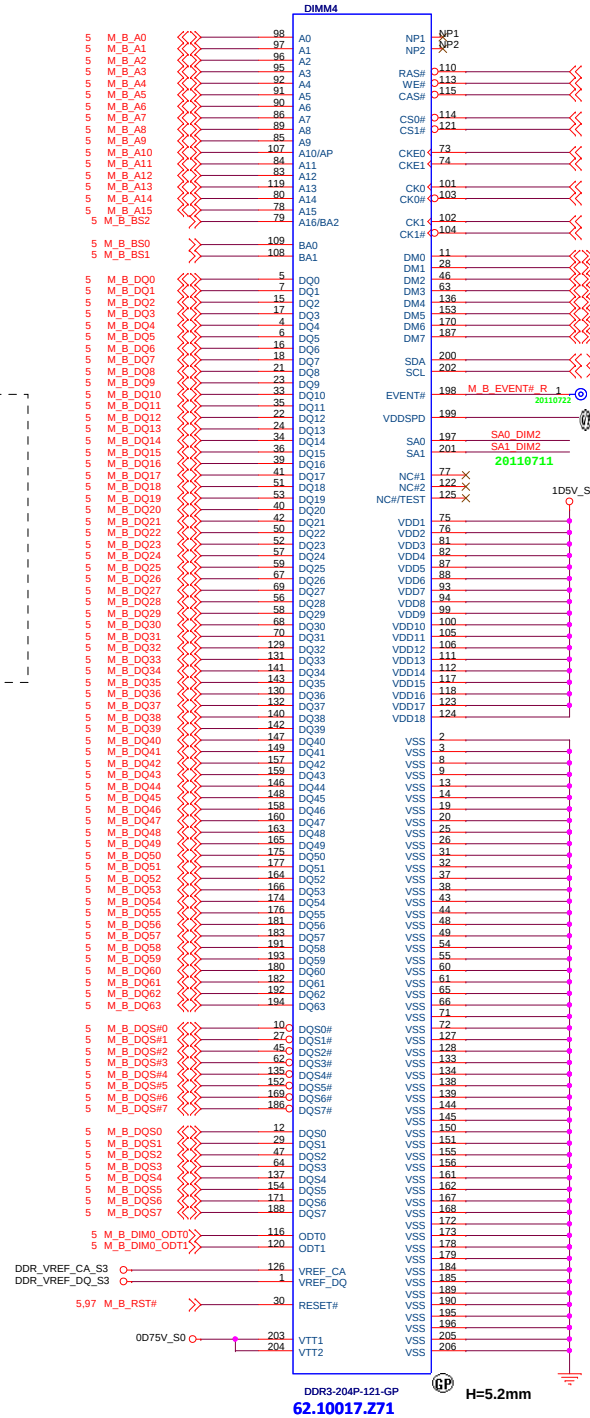
20110722

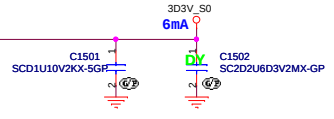
Layout note: Place these Caps closed So-Dimm1

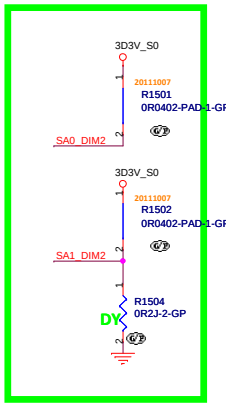












follow SS11

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: DDR3 SO-DIMM2

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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

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FCH1E

Part 5 of 5

closed to FCH

Connect to HP debug board!!

Connect to KBC

Ext. Clock_Gen

LAN

CARD

WLAN

82.30020.G71

71.HUDM2.M01

RTC Battery

23.22063.001	JHT	RTC CR2032
23.22065.001	DBV	RTC CR2032
23.20068.001	KTS	RTC CR2032

<Variant Name>

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Title: HUDSON-M2(1/6)

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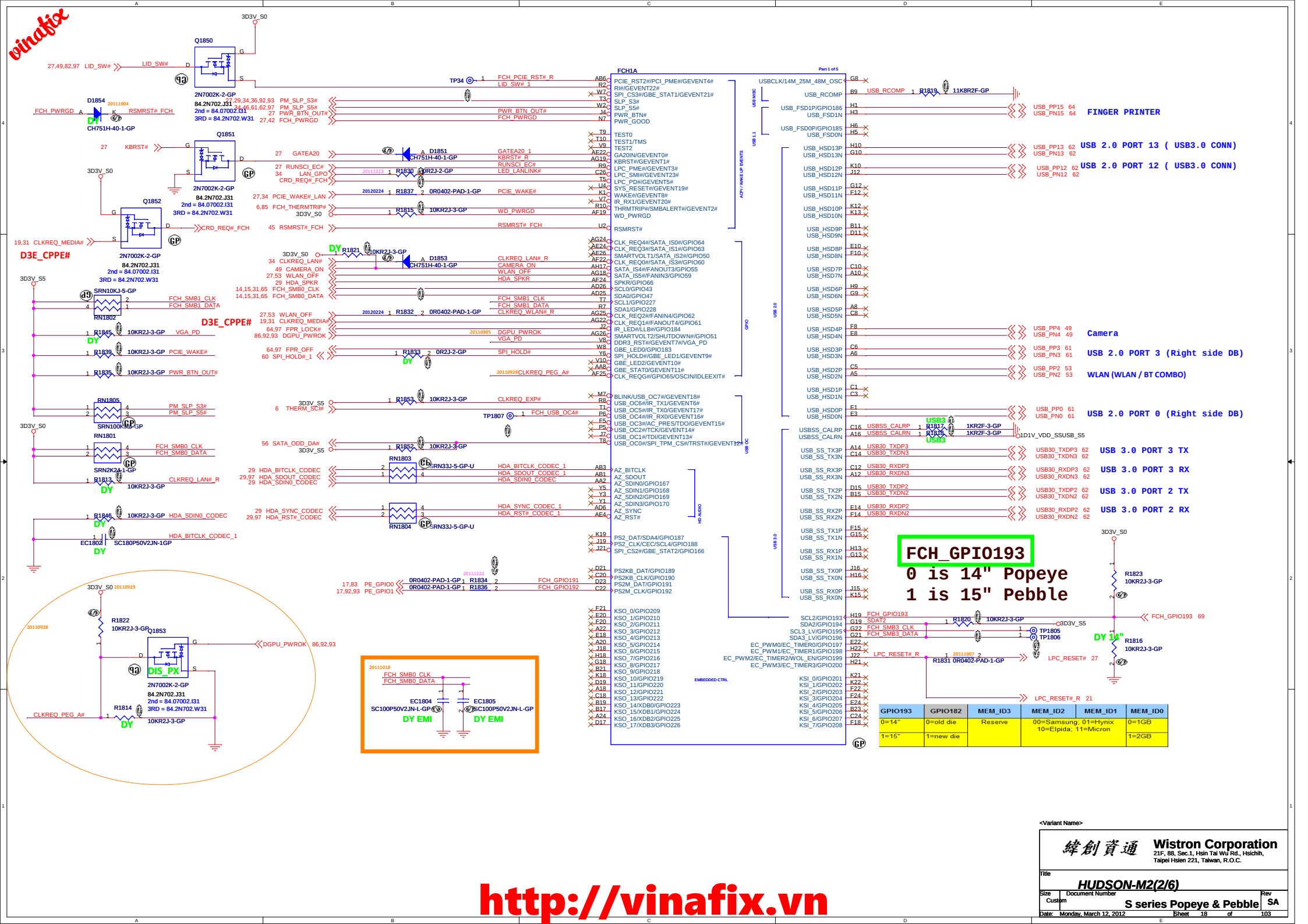

<Variant Name>

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Title: HUDSON-M2(2/6)

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FCH1B

Part 2 of 5

1st SATA HDD

SATA ODD

SATA_TX0P / SATA_TX0N
SATA_RX0N / SATA_RX0P
SATA_TX1P / SATA_TX1N
SATA_RX1N / SATA_RX1P
SATA_TX2P / SATA_TX2N
SATA_RX2N / SATA_RX2P
SATA_TX3P / SATA_TX3N
SATA_RX3N / SATA_RX3P
SATA_TX4P / SATA_TX4N
SATA_RX4N / SATA_RX4P
SATA_TX5P / SATA_TX5N
SATA_RX5N / SATA_RX5P
NC#AL29 / NC#AN31
NC#AL31 / NC#AL33
NC#AH33 / NC#AH31
NC#AJ33 / NC#AJ31

SATA_CALRP / SATA_CALRN
SATA_ACT#/GPIO67
SATA_X1
SATA_X2

1D1V_SATA_S0
R1901 1KR2F-3-GP SATA_CALP
R1902 931R2F-1-GP SATA_CALN
3D3V_S0
R1950 10KR2J-3-GP
68 SATA_LED#

WLAN
BLUETOOTH
20110712
53 WLAN_TRANSMIT_OFF#
53,97 BT_OFF
31 D3E_WAKE#
20110707
68 HDD_HALTLED
18,31 CLKREQ_MEDIA#

D3E_CPPE#

FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174
FCH_GPIO171_3D3V_S5

SD_CLK/SCLK_2/GPIO73
SD_CMD/SLOAD_2/GPIO74
SD_CD#/GPIO75
SD_WP/GPIO76
SD_DATA0/SDATI_2/GPIO77
SD_DATA1/SDATO_2/GPIO78
SD_DATA2/GPIO79
SD_DATA3/GPIO80

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE_MDIO
20110722
R1951 10KR2J-3-GP
3D3V_S5
GBE_PHY
R1909 10KR2J-3-GP

SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/SPI_WP#/GPIO161

FCH_SPI_MISO
FCH_SPI_MOSI
FCH_SPI_CLK
FCH_SPI_CS#0
FCH_SPI_WP#_R
R1952 0R2J-2-GP
DY
FCH_SPI_MISO 60
FCH_SPI_MOSI 60
FCH_SPI_CLK 60
FCH_SPI_CS#0 60
SPI_WP#_1 27,60

VGA_RED
VGA_GREEN
VGA_BLUE
20110715
R1921 150R2F-1-GP
R1922 150R2F-1-GP
R1923 150R2F-1-GP
FCH_RED 50
FCH_GREEN 50
FCH_BLUE 50

VGA_HSYNC/GPO68
VGA_VSYNC/GPO69
CRT_HSYNC 50
CRT_VSYNC 50

VGA_DDC_SDA/GPO70
VGA_DDC_SCL/GPO71
CRT_DDC_DATA 50
CRT_DDC_CLK 50

VGA_DAC_RSET
HUDSON_DAC_RESET
R1907 715R2F-GP

AUX_VGA_CH_P
AUX_VGA_CH_N
DP1_AUXP_R 6
DP1_AUXN_R 6

AUXCAL
R1913 100R2F-L1-GP-U
1D1V_VDDAN_ML_S0

ML_VGA_L0P
ML_VGA_L0N
ML_VGA_L1P
ML_VGA_L1N
ML_VGA_L2P
ML_VGA_L2N
ML_VGA_L3P
ML_VGA_L3N
DP1_TX0P_R 6
DP1_TX0N_R 6
DP1_TX1P_R 6
DP1_TX1N_R 6
DP1_TX2P_R 6
DP1_TX2N_R 6
DP1_TX3P_R 6
DP1_TX3N_R 6

ML_VGA_HPD/GPIO229
R1908 100KR2J-1-GP
3D3V_S0 20110803
DP1_HPD 6
RN1902 SRN10KJ-5-GP
DY
3D3V_S5
3D3V_S0

VIN0/GPIO175
VIN1/GPIO176
VIN2/SDATI_1/GPIO177
VIN3/SDATO_1/GPIO178
VIN4/SLOAD_1/GPIO179
VIN5/SCLK_1/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182
FCH_GPIO175
GPS_XMIT_OFF#
SATA_ODD_PWR_EN
FCH_VM_GPIO181
FCH_VM_GPIO182
FCH_GPIO178
20110928
20110722
SATA_ODD_PWR_EN 56,97
R1936 100KR2J-1-GP
3D3V_S0

NC#AG16
NC#AH10
NC#A28
NC#G27
NC#L4

71.HUDM2.M01

20110715
for layout
R1921 R1922 R1923 closed to FCH

3D3V_S0
DP1_AUXN_R
R1971 100KR2J-1-GP DY
20110804
DP1_AUXP_R
R1972 100KR2J-1-GP DY

3D3V_S5
20110715
DIS_PX
R2220 10KR2J-3-GP
R2224 10KR2J-3-GP
DY VRAM new die
FCH_VM_GPIO181
FCH_VM_GPIO182
20110907
UMA
R2223 10KR2J-3-GP
R2225 10KR2J-3-GP
DIS_PX VRAM old die

3D3V_S5
RN1901 SRN10KJ-5-GP
FCH_GPIO171_3D3V_S5
FCH_GPIO178
20110630

<Variant Name>

緯創資通 Wistron Corporation
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Title: HUDSON-M2(3/6)
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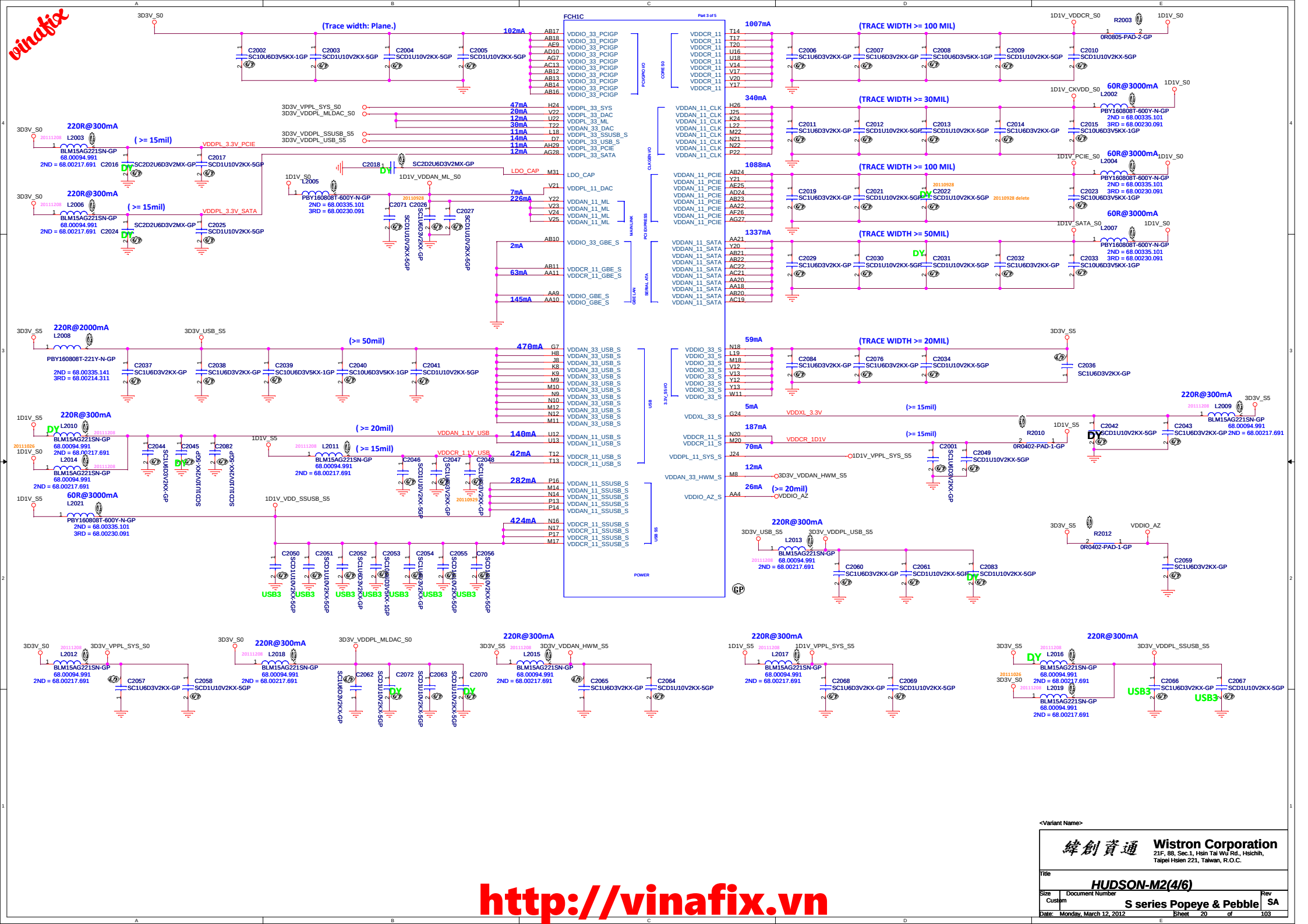


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(4/6)

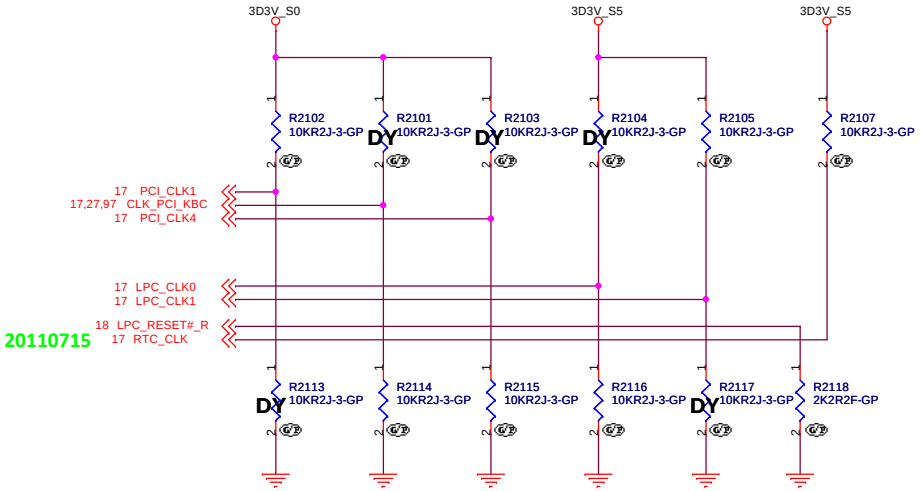
Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 20 of 103

SSID = S.B

REQUIRED STRAPS

20110707



REQUIRED SYSTEM STRAPS

	LPC_RESET# PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_KBC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

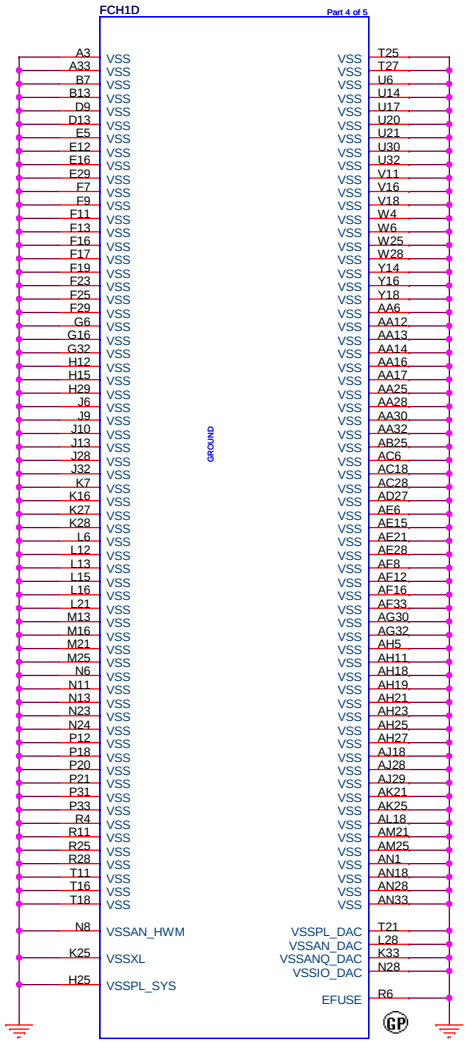
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(5/6)

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 21 of 103



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HUDSON-M2(6/6)***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 22 of 103

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 23 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 24 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 25 of 103

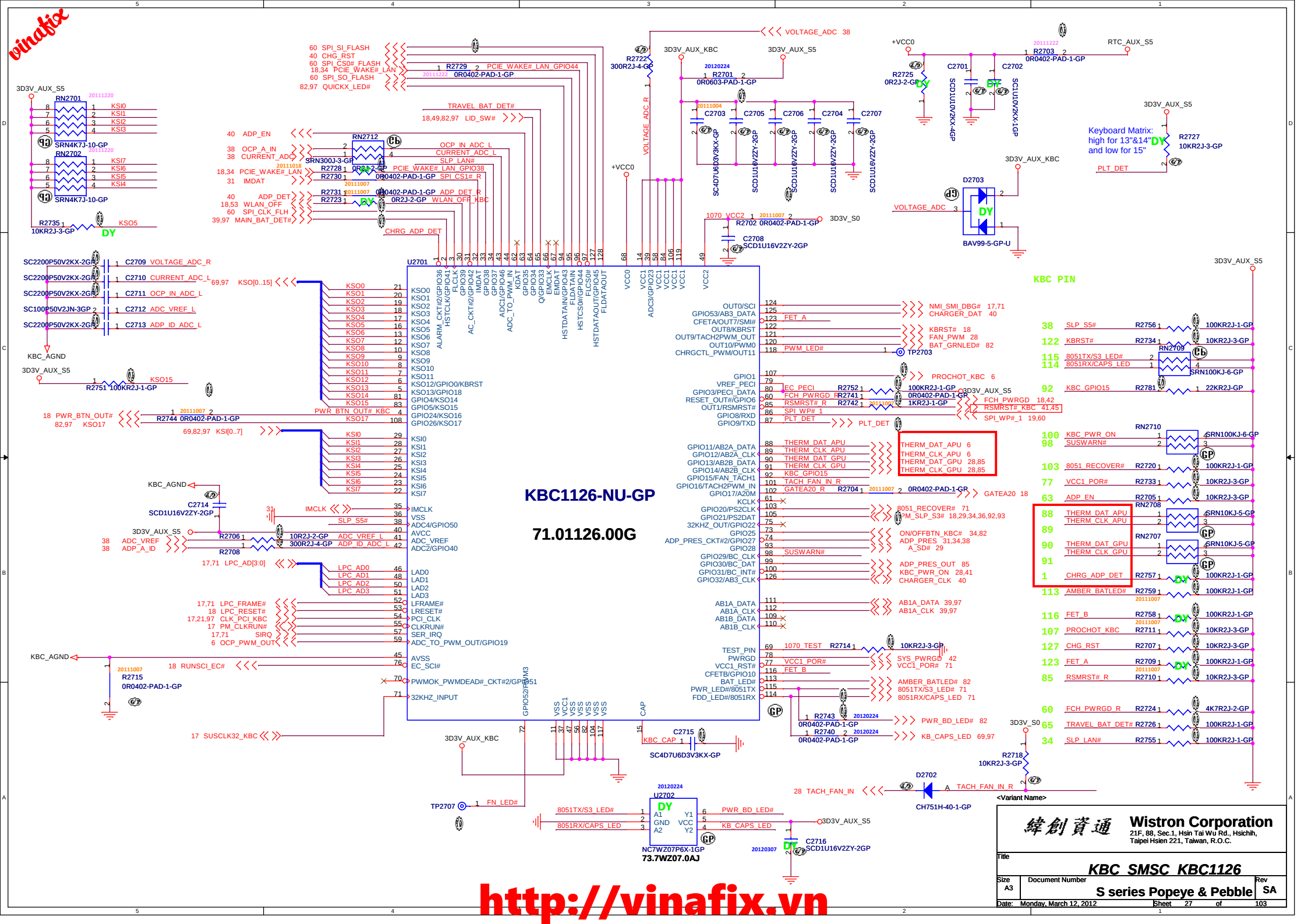
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 26 of 103


KBC1126-NU-GP
71.01126.00G
KBC PIN
Keyboard Matrix:
high for 13"&14"
and low for 15"
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_SMSC_KBC1126
S series Popeye & Pebble
Monday, March 12, 2012
http://vinafix.vn

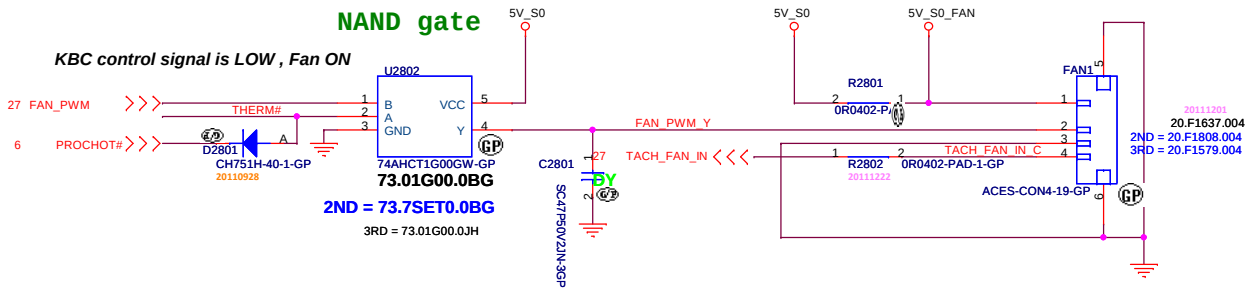
4 WIRE PWM Fan Control circuit

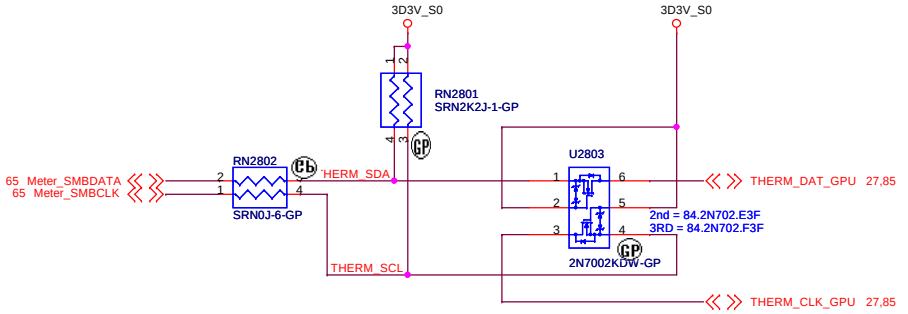
FAN PWM LEVEL = 5V

20mil

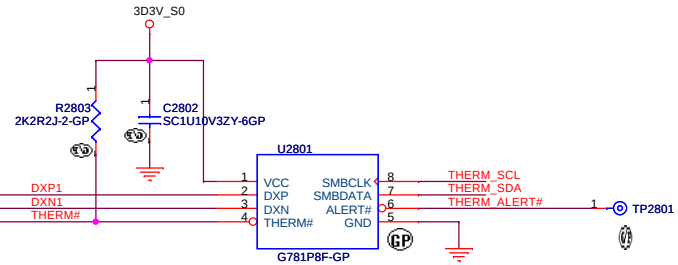
NAND gate

KBC control signal is LOW , Fan ON





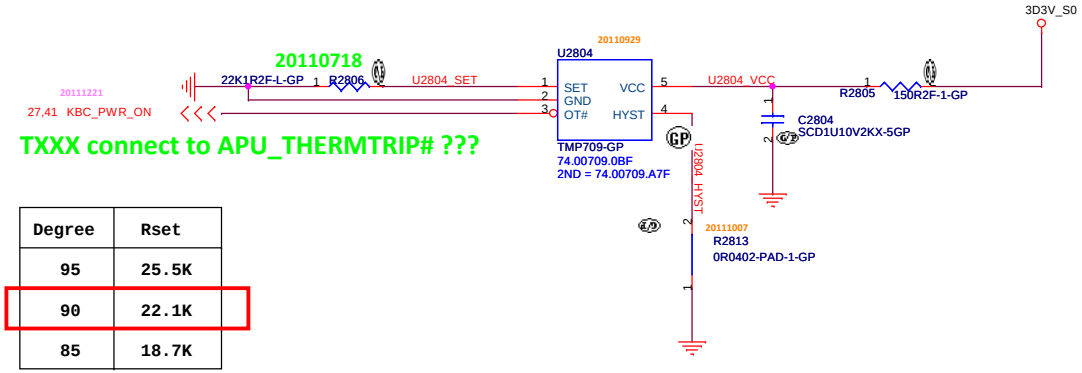
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



Thermal IC Control circuit

T8 H/W Shutdown Control circuit

90 ◦ C



Degree	Rset
95	25.5K
90	22.1K
85	18.7K

<Variant Name>

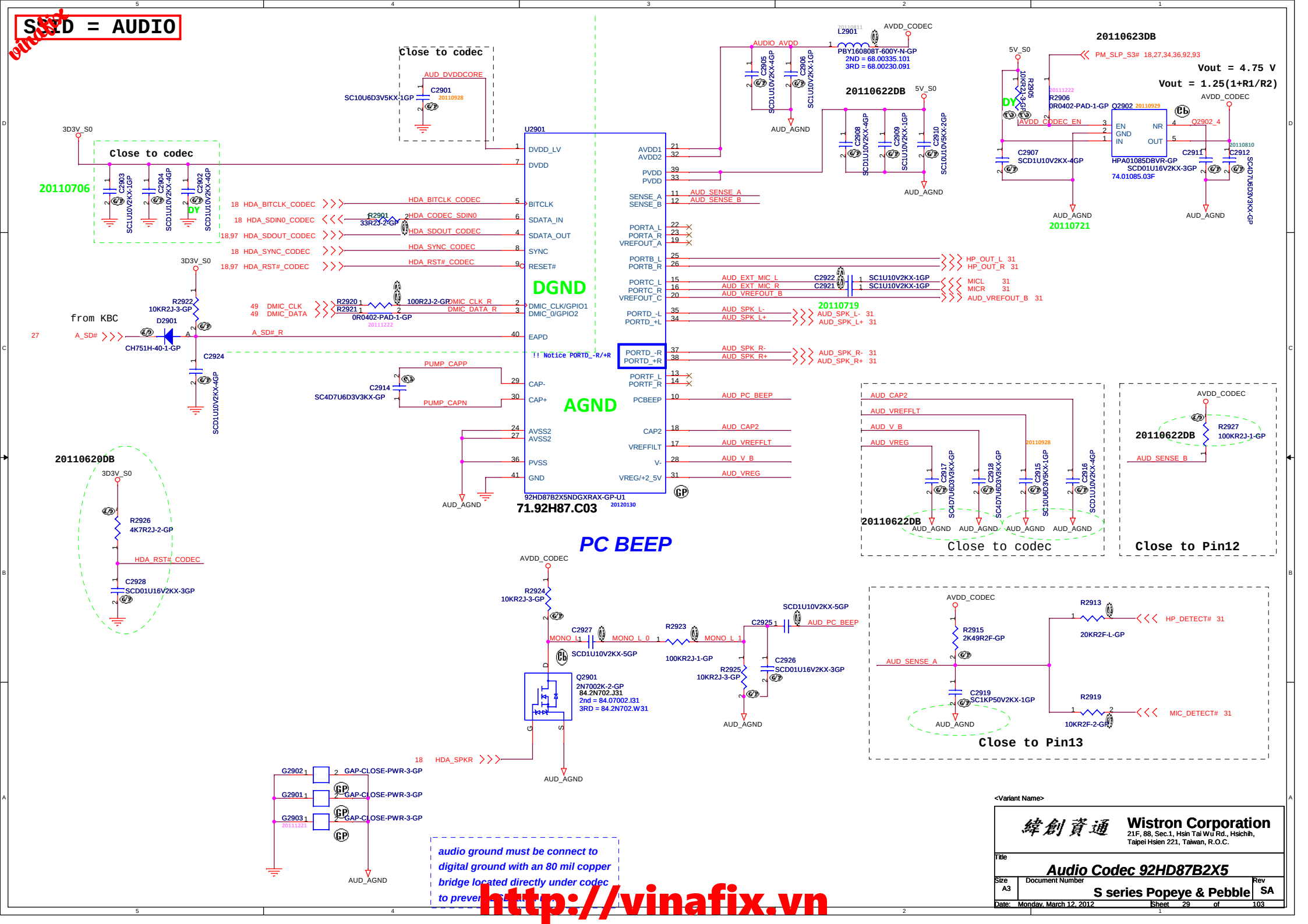
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal G781 / FAN

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 28 of 103

SSID = AUDIO



0622-2 SA Change to ADUIO BOARD page3

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: External MIC Pre-Amp

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 30 of 103

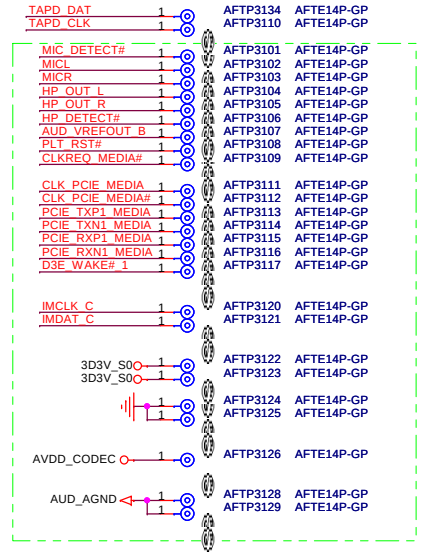
Audio Board +Touch Pad Connector

HeadPhone OUT

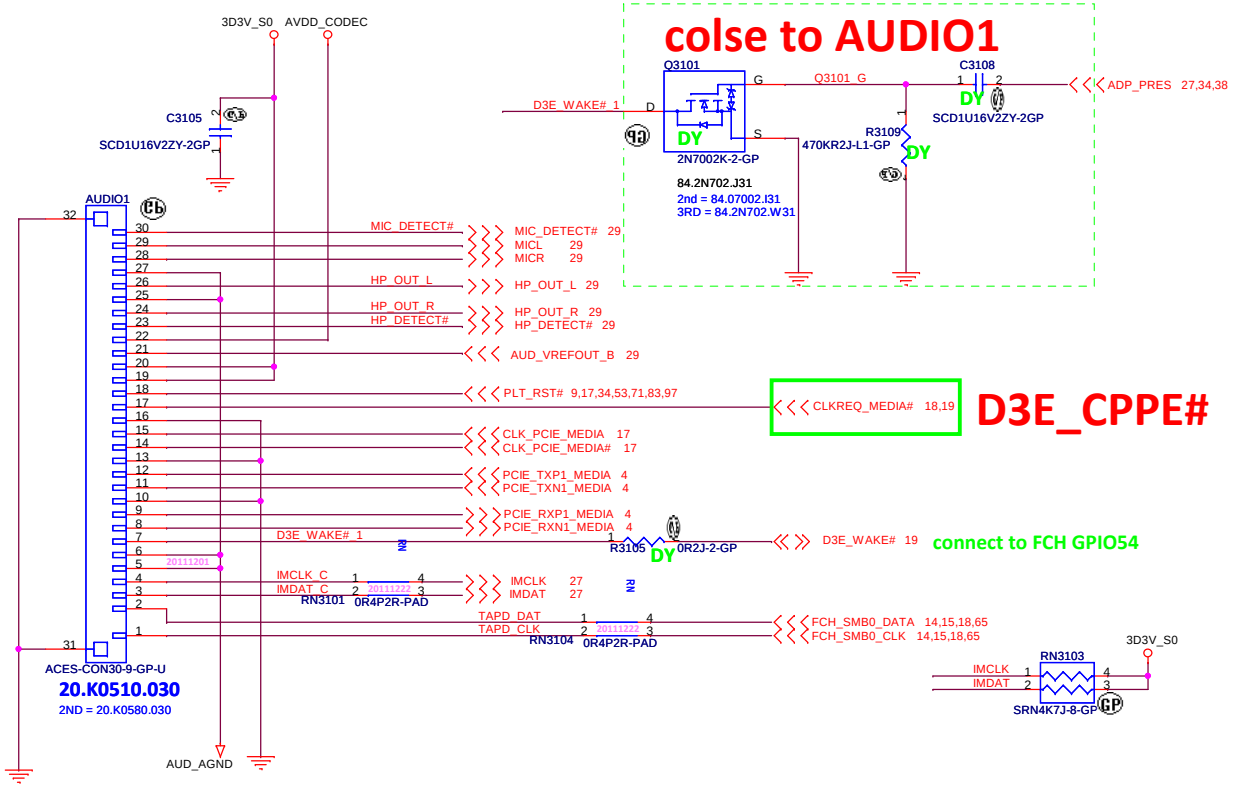
0621 SA Change to ADUIO BOARD page4

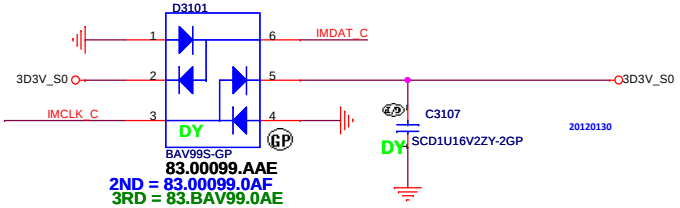
Jack Detect

0621 SA Change to ADUIO BOARD page4

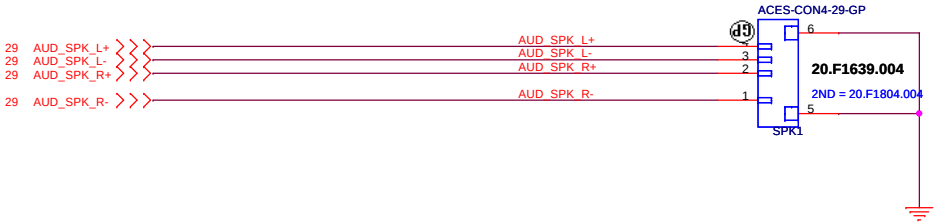


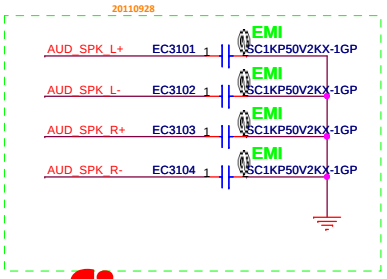
colse to AUDIO1

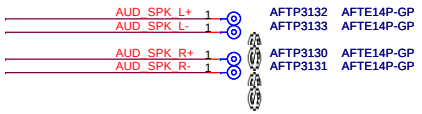




Speaker Connector







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO Connector

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 31 of 103

CardReader JMicron JMB709

0622-2 SA Change to ADUIO BOARD page1

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-JMB 709

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 32 of 103

0622-2 SA Change to ADUIO BOARD page2

<Variant Name>

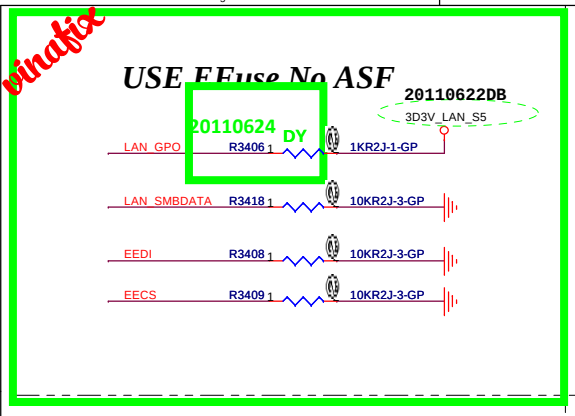
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

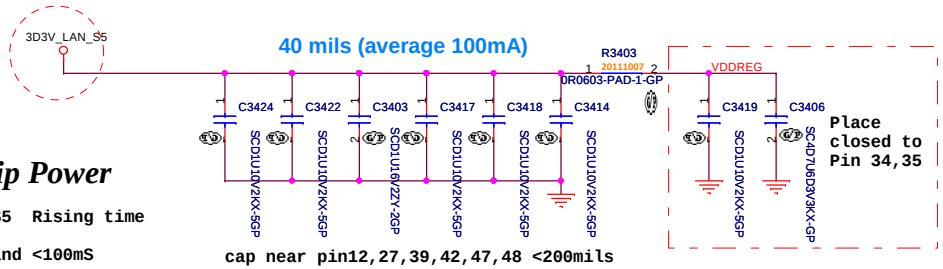
Title: SD/MS/MMC CONNECTOR

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 33 of 103

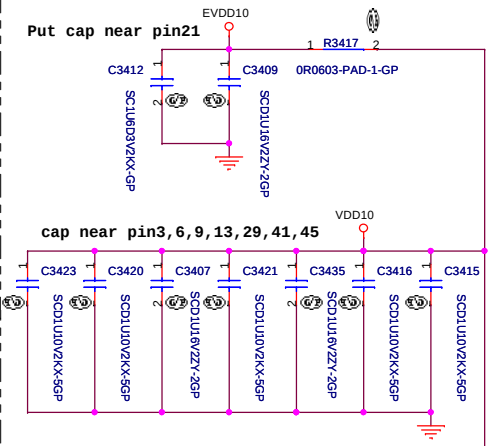
LAN CHIP-RTL8111E

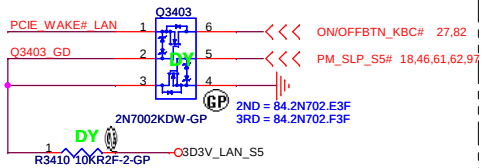


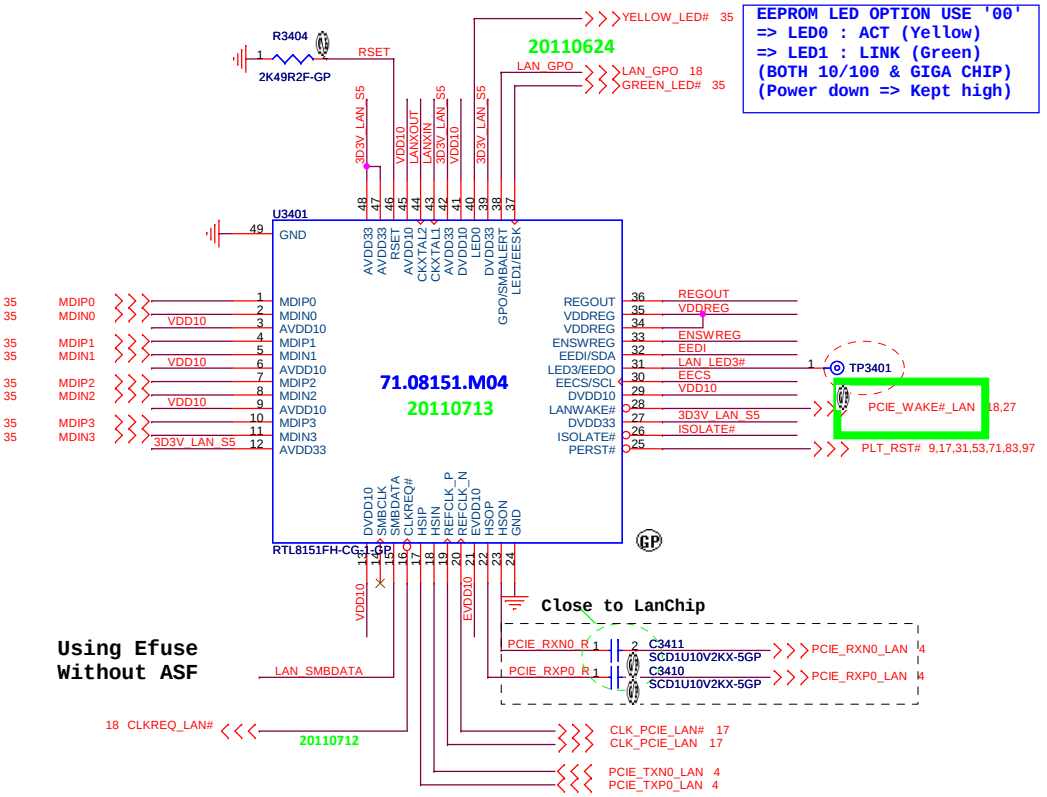


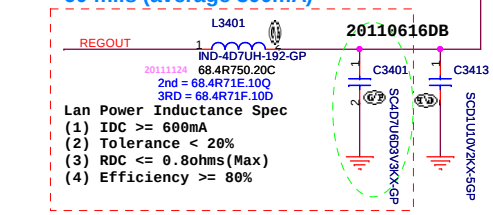
LanChip Power

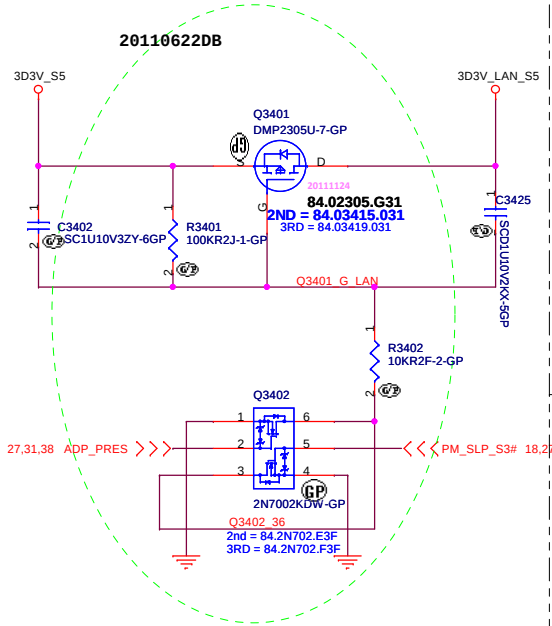
+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS





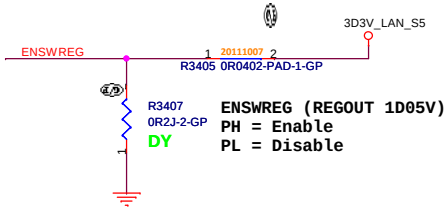




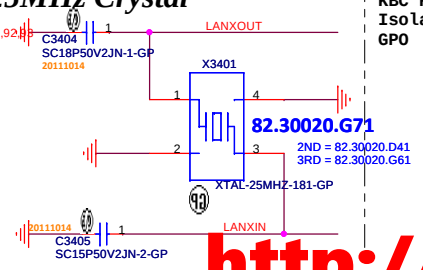


Using Efuse Without ASF

Regout Switch

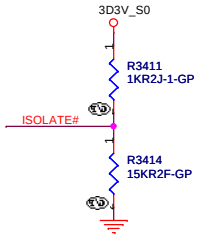


25MHz Crystal



KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

Isolate Strap Pin



<Variant Name>

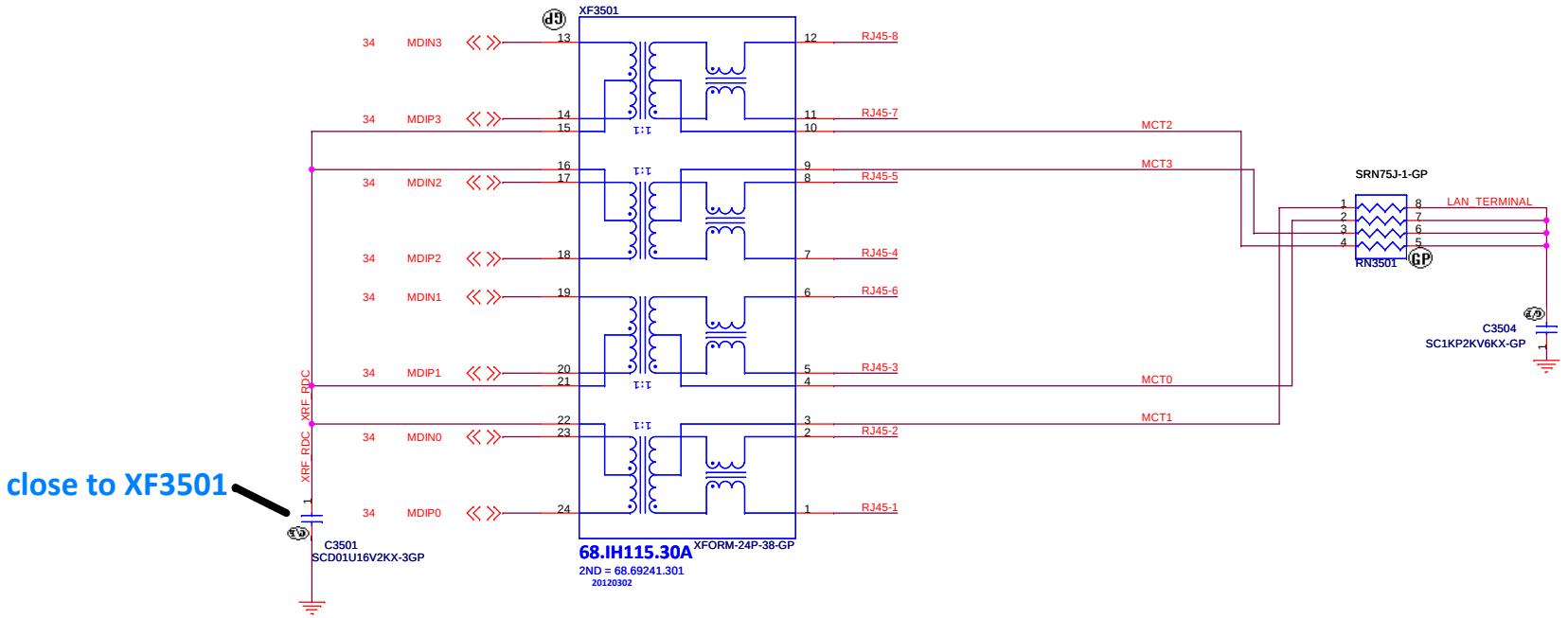
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151FH

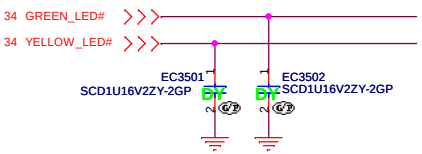
Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

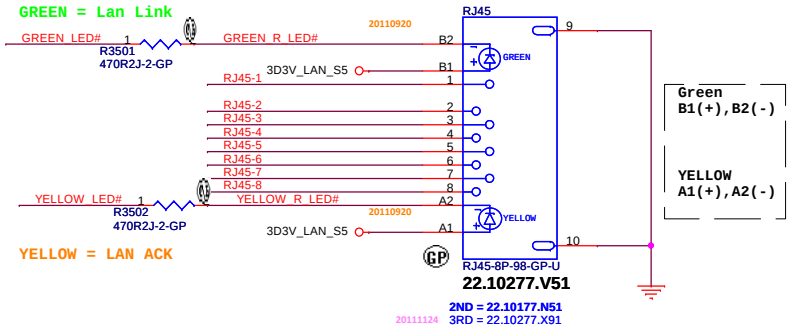
Date: Monday, March 12, 2012 | Sheet 34 of 103

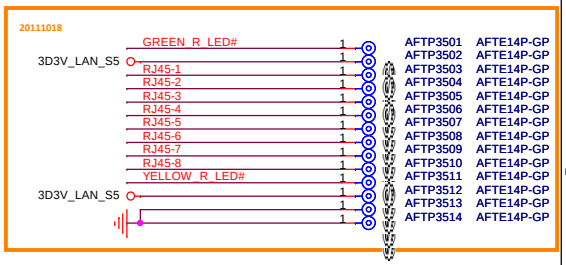
White LED for connectivity and Amber LED for activity located on RJ-45 connector



RJ45 Connector







(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

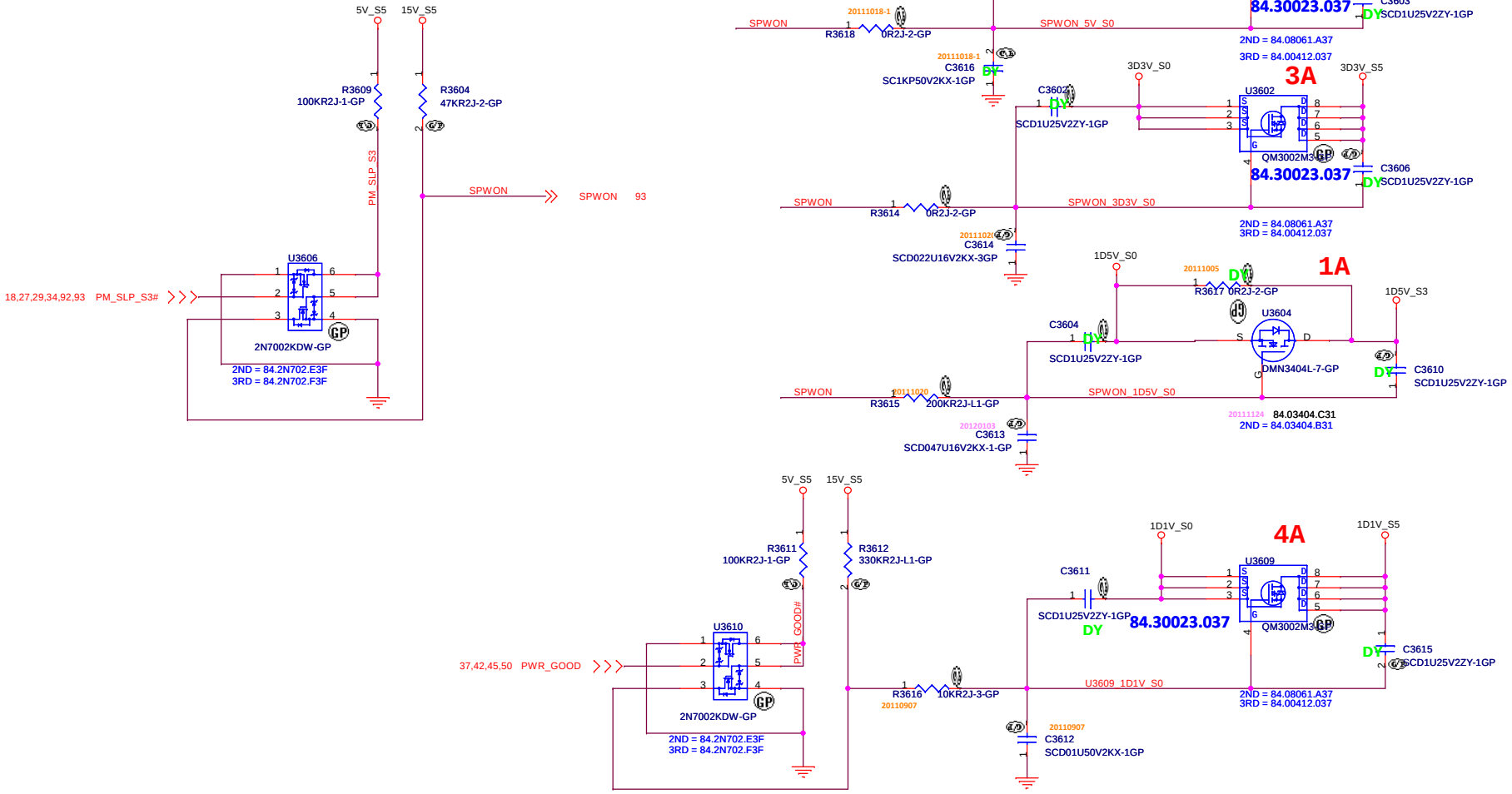
<Variant Name>

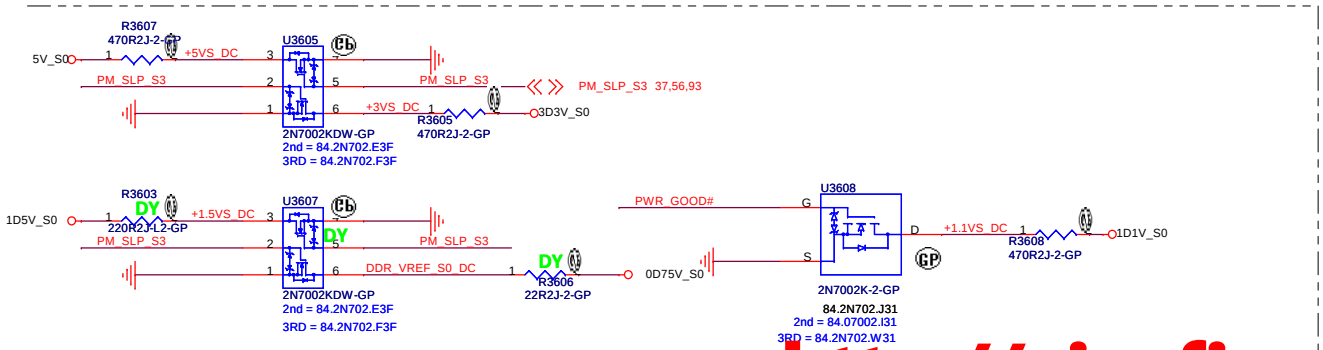
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN RJ45	
Size A3	Document Number S series Popeye & Pebble	Rev SA
Date: Monday, March 12, 2012	Sheet 35 of 103	

Run Power

5V_S5 to 5V_S0 Transfer
3D3V_S5 to 3D3V_S0 Transfer
1D5V_S3 to 1D5V_S0 Transfer
1D1V_S5 to 1D1V_S0 Transfer





<Variant Name>

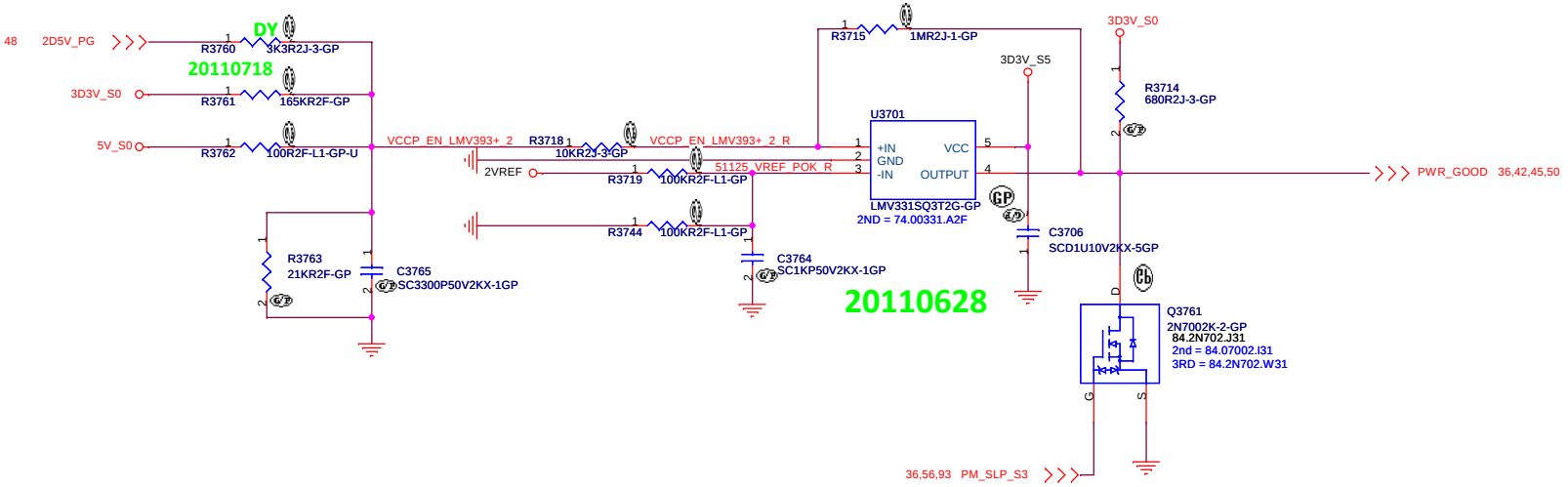
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 36 of 103

POK

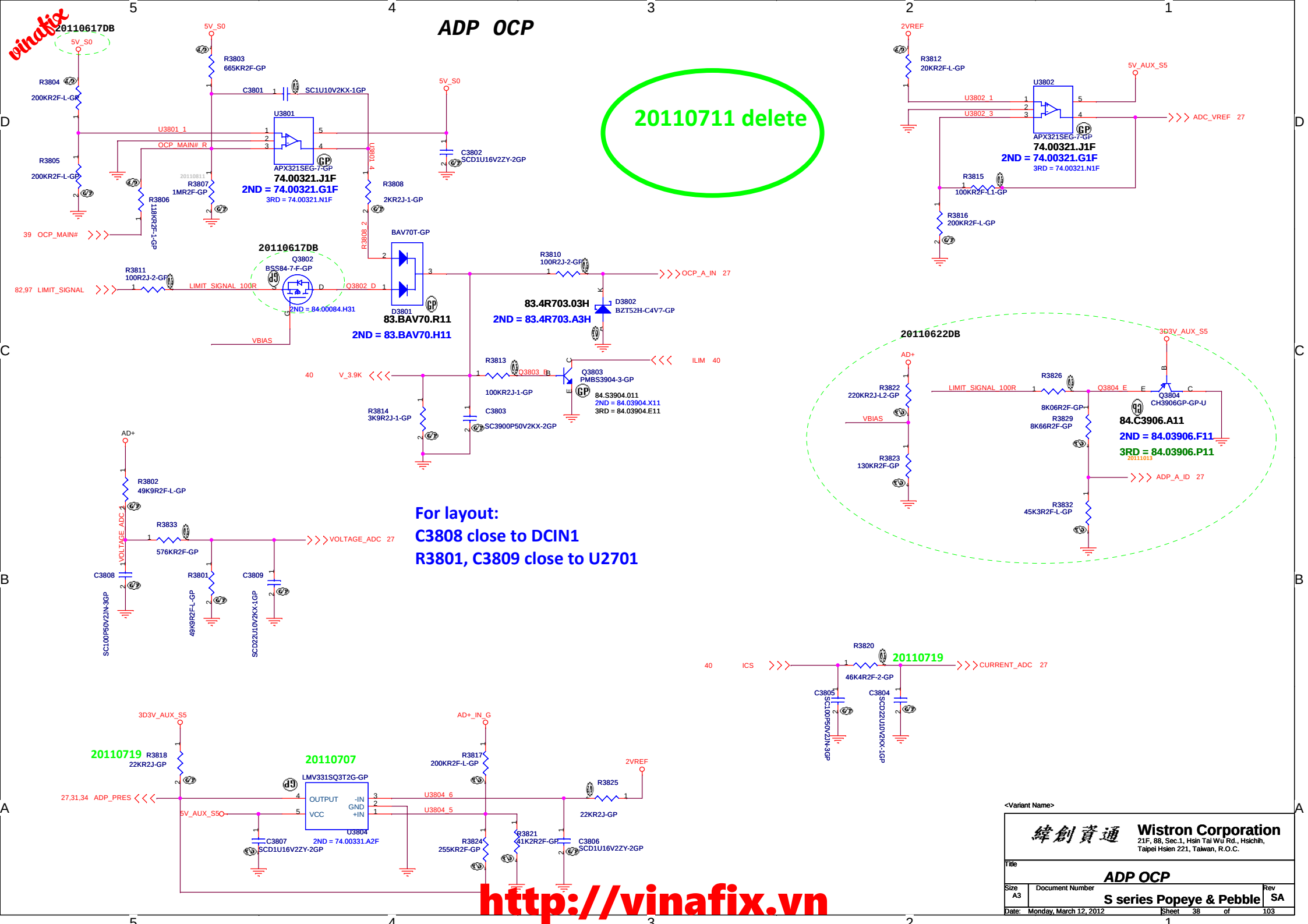


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POK	
Size A3	Document Number S series Popeye & Pebble	Rev SA
Date: Monday, March 12, 2012	Sheet 37 of 103	

ADP OCP



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP OCP

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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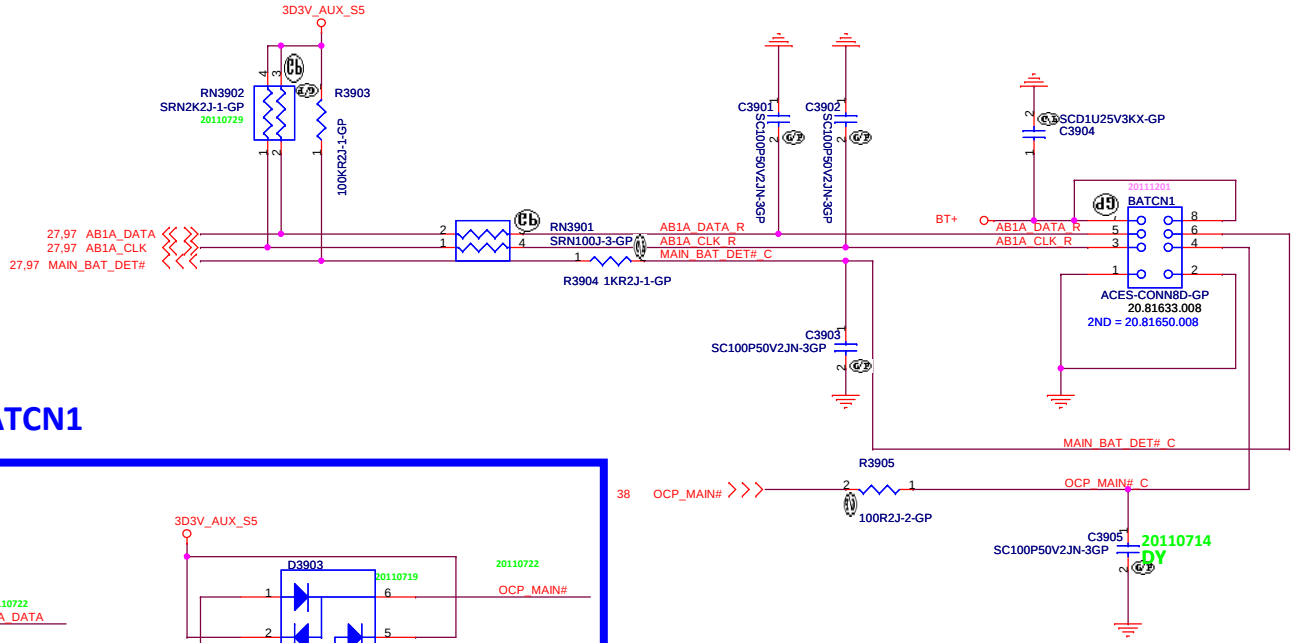
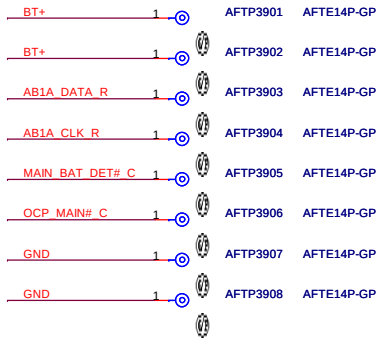
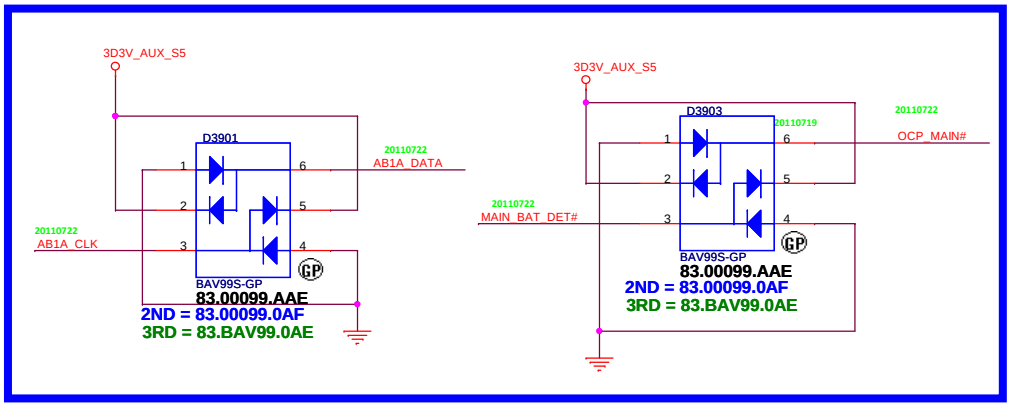
Battery Connector





colse to BATCN1



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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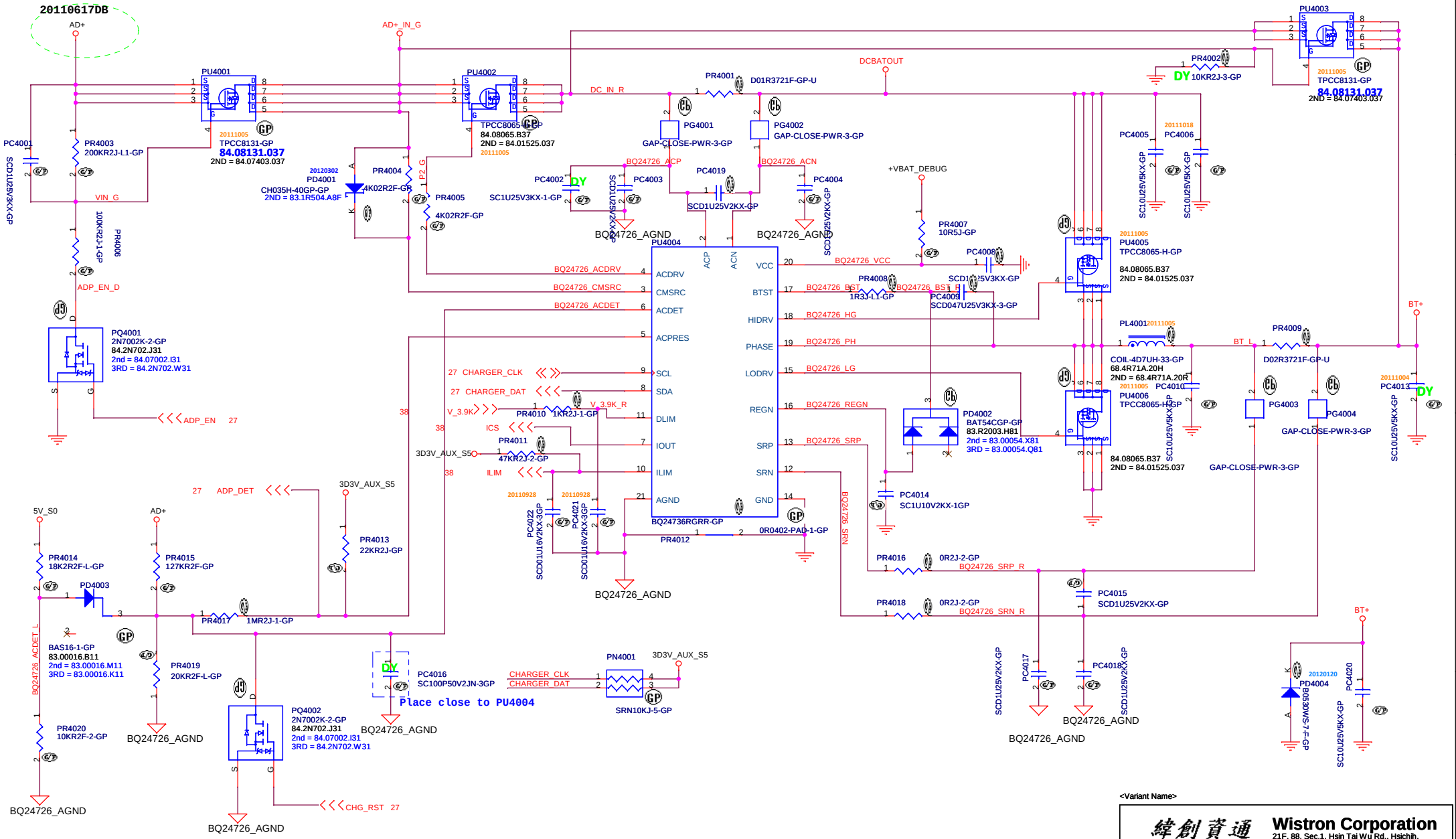
BQ24736 for CHARGER



<Variant Name>

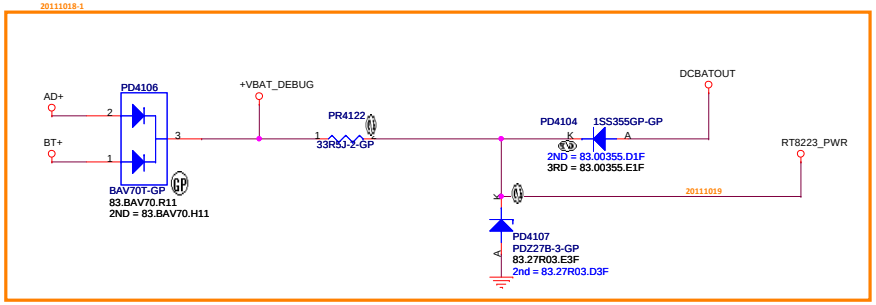
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

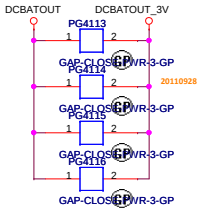
Title: Charger BQ24736

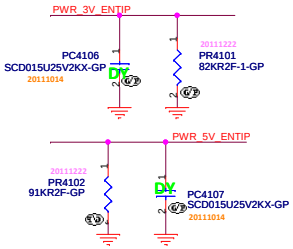
Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

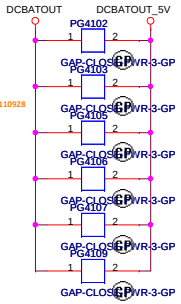
Date: Monday, March 12, 2012 | Sheet 40 of 103

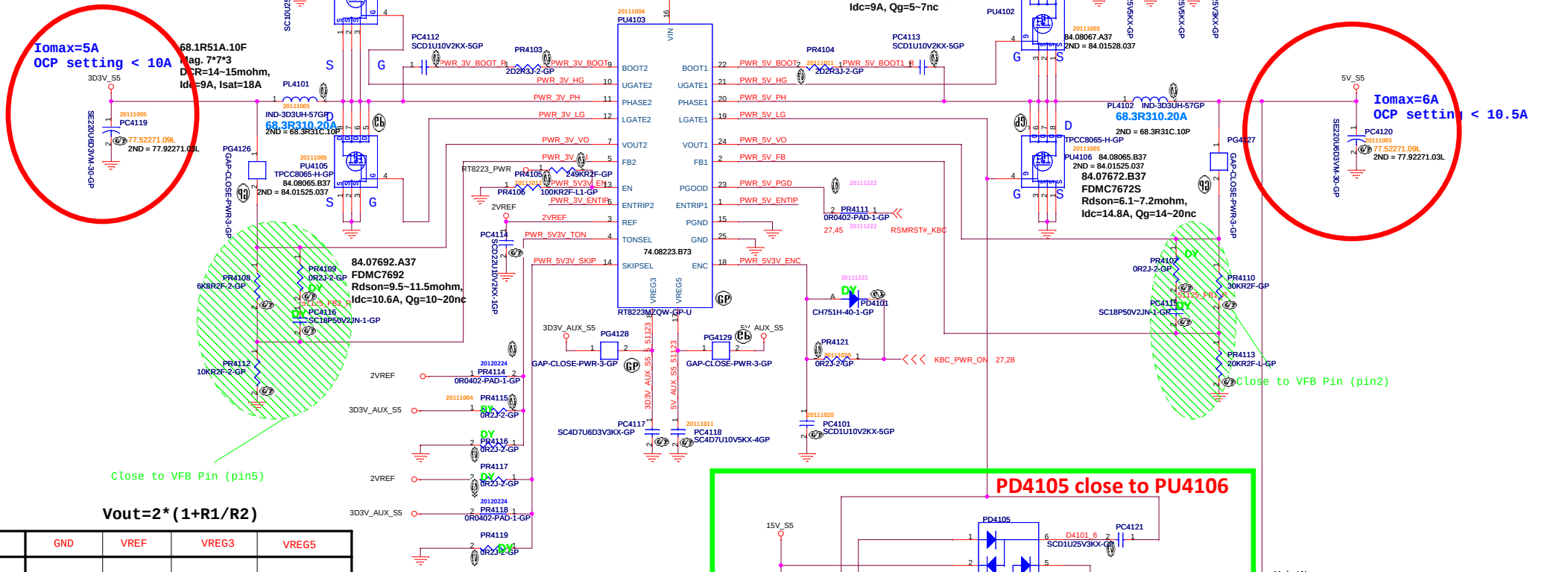
RT8223 for 3V5V



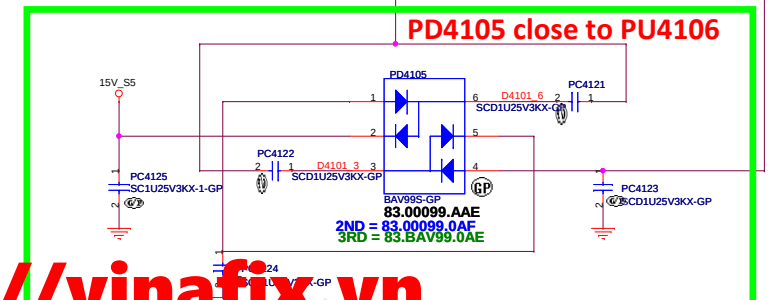








	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



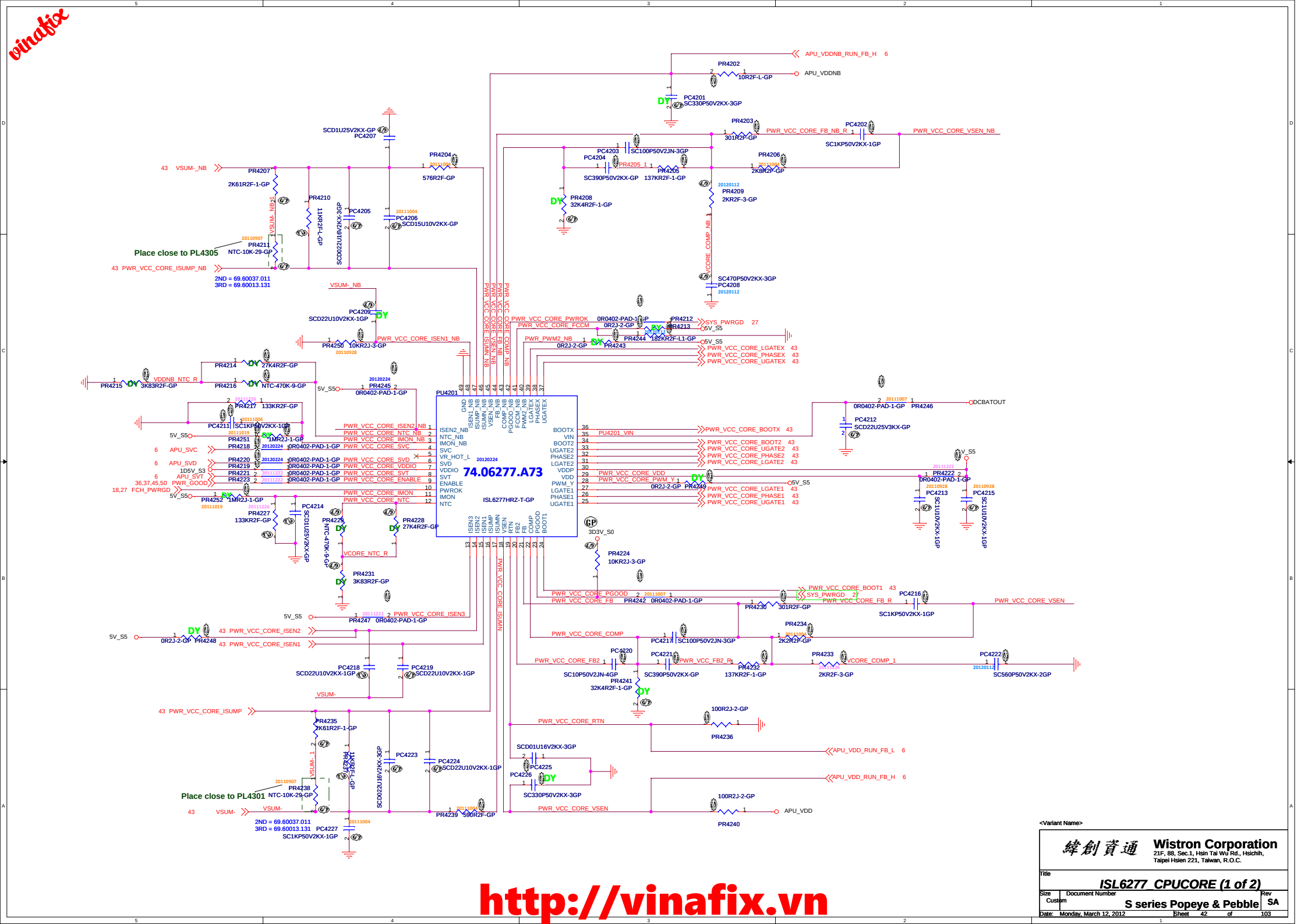
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223 5V/3D3V

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 41 of 103



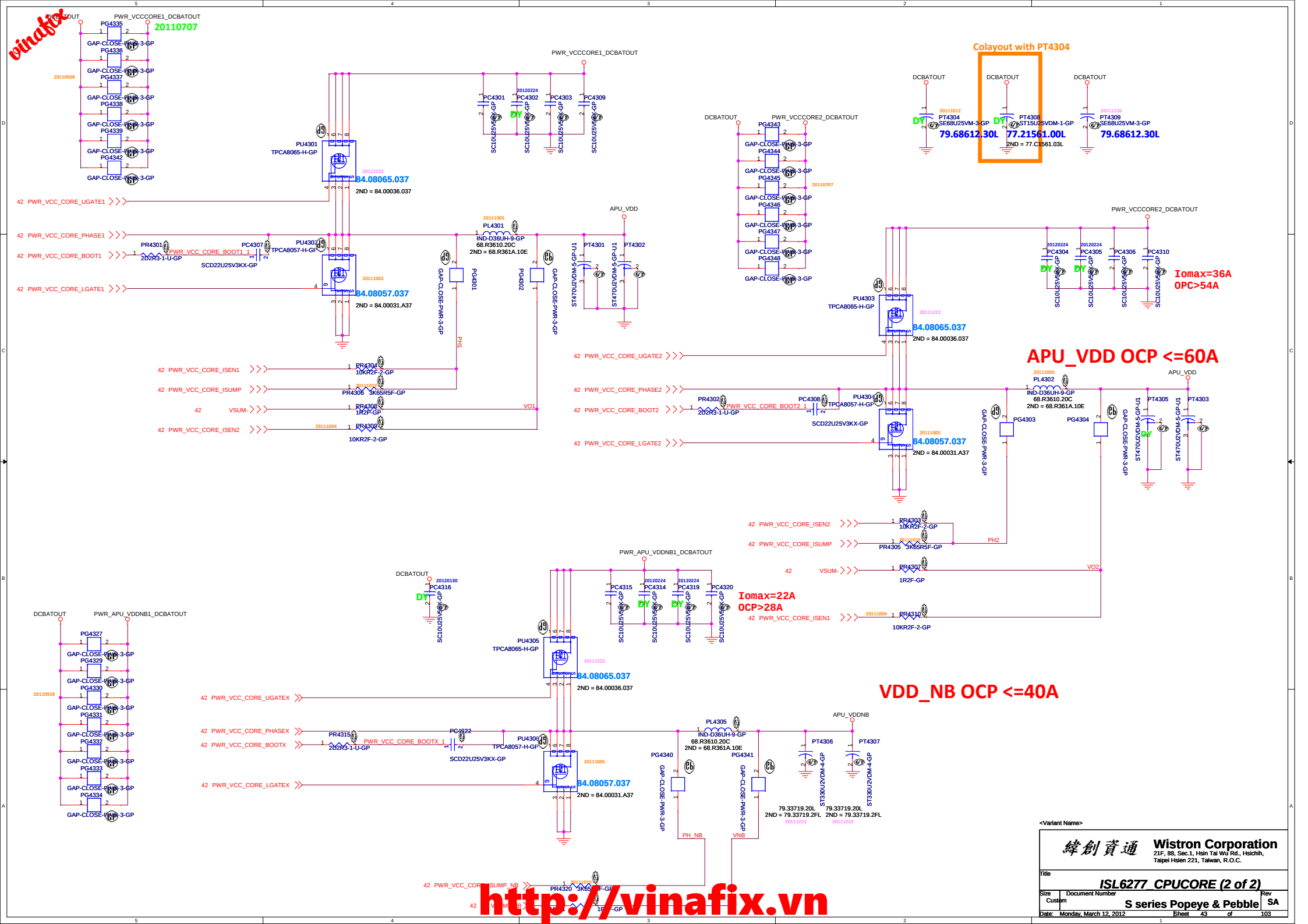
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6277_CPUCORE (1 of 2)

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 42 of 103


Colayout with PT4304
APU_VDD OCP <=60A
VDD_NB OCP <=40A
Iomax=36A
OPC>54A
Iomax=22A
OCP>28A
PWR_VCCCORE1_DCBATOUT
PWR_VCCCORE2_DCBATOUT
PWR_APU_VDDNB1_DCBATOUT
DCBATOUT
APU_VDD
APU_VDDNB
20110707
PU4301 TPCA8065-H-GP
PU4302 TPCA8057-H-GP
PU4303 TPCA8065-H-GP
PU4304 TPCA8057-H-GP
PU4305 TPCA8065-H-GP
PU4306 TPCA8057-H-GP
84.08065.037
2ND = 84.00036.037
84.08057.037
2ND = 84.00031.A37
PL4301 IND-D36UH-9-GP 68.R3610.20C 2ND = 68.R361A.10E
PL4302 IND-D36UH-9-GP 68.R3610.20C 2ND = 68.R361A.10E
PL4305 IND-D36UH-9-GP 68.R3610.20C 2ND = 68.R361A.10E
79.68612.30L
79.77.21561.00L
2ND = 77.C1561.03L
79.33719.20L
2ND = 79.33719.2FL
42 PWR_VCC_CORE_UGATE1
42 PWR_VCC_CORE_PHASE1
42 PWR_VCC_CORE_BOOT1
42 PWR_VCC_CORE_LGATE1
42 PWR_VCC_CORE_UGATE2
42 PWR_VCC_CORE_PHASE2
42 PWR_VCC_CORE_BOOT2
42 PWR_VCC_CORE_LGATE2
42 PWR_VCC_CORE_UGATEX
42 PWR_VCC_CORE_PHASEX
42 PWR_VCC_CORE_BOOTX
42 PWR_VCC_CORE_LGATEX
42 PWR_VCC_CORE_ISEN1
42 PWR_VCC_CORE_ISEN2
42 PWR_VCC_CORE_ISUMP
42 PWR_VCC_CORE_ISUMP_NB
42 VSUM-
PR4304 10KR2F-2-GP
PR4305 3K65R5F-GP
PR4306 3K65R5F-GP
PR4307 1R2F-GP
PR4308 1R2F-GP
PR4309 10KR2F-2-GP
PR4310 10KR2F-2-GP
PR4320 3K65R5F-GP
PR4321 1R2F-GP
PH1
PH2
PH_NB
VNB
VO1
VO2
PWR_VCC_CORE_BOOT1_1
PWR_VCC_CORE_BOOT2_1
PWR_VCC_CORE_BOOTX_1
2D2R3-1-U-GP
SCD22U25V3KX-GP
GAP-CLOSE-PWR-3-GP
ST470U2VDM-5-GP-U1
ST330U2VDM-4-GP
SC10U25V5KX-GP
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6277_CPUCORE (2 of 2)
S series Popeye & Pebble
Size: Custom
Document Number
Rev: SA
Date: Monday, March 12, 2012
Sheet 43 of 103
<Variant Name>
http://vinafix.vn

<Variant Name>

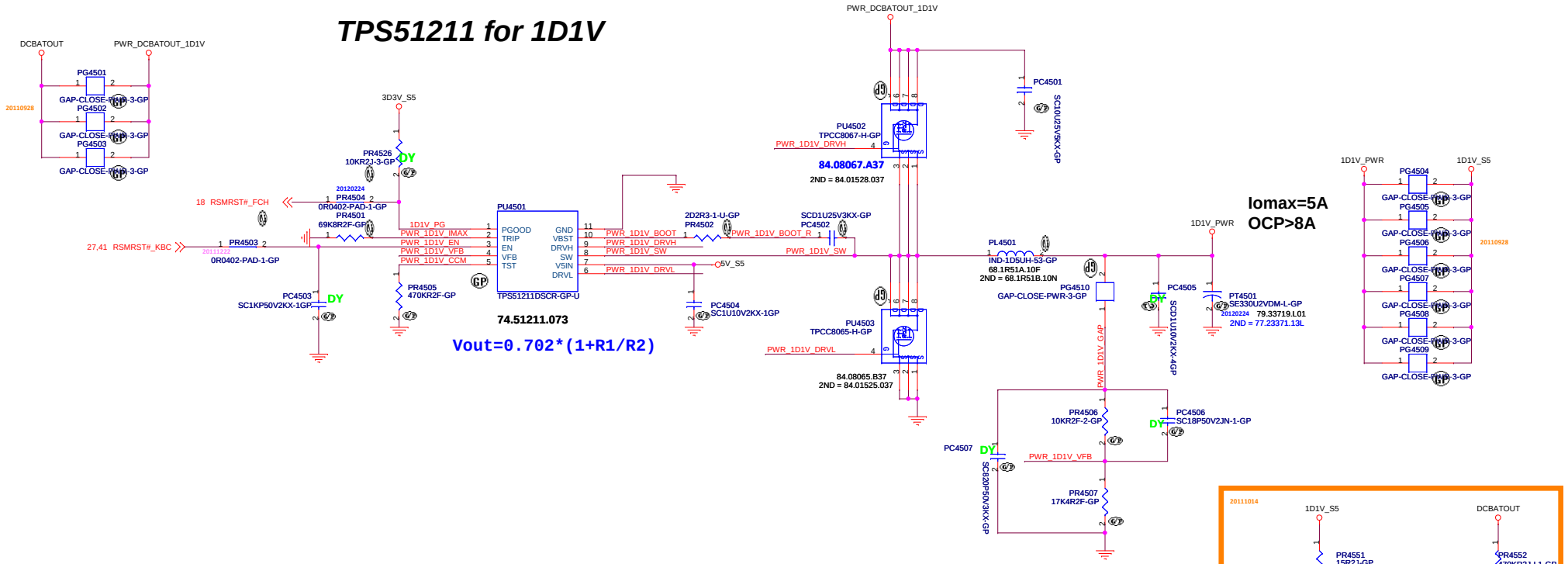
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

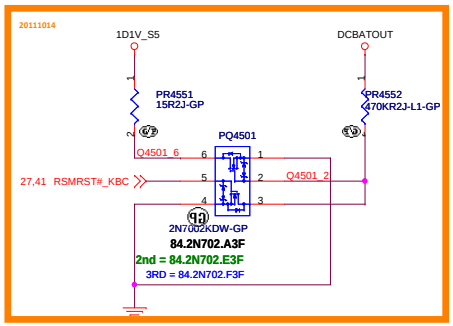
Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

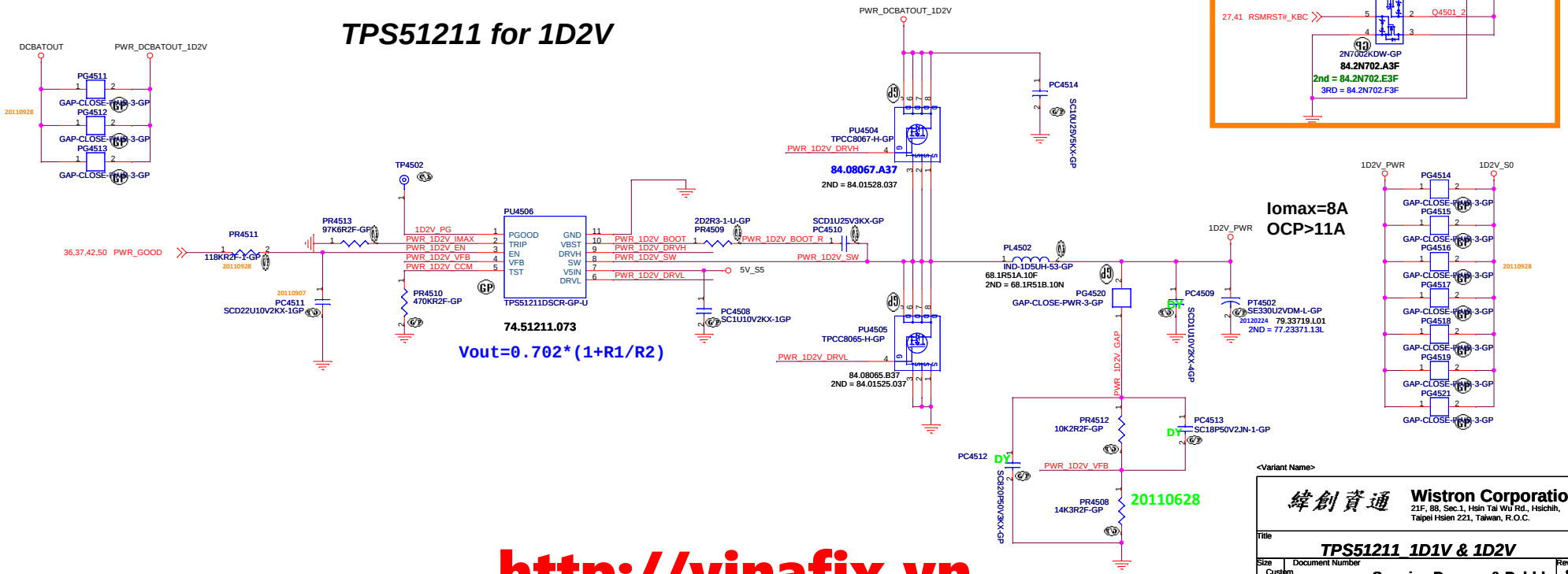
Date: Monday, March 12, 2012 Sheet 44 of 103

TPS51211 for 1D1V





TPS51211 for 1D2V



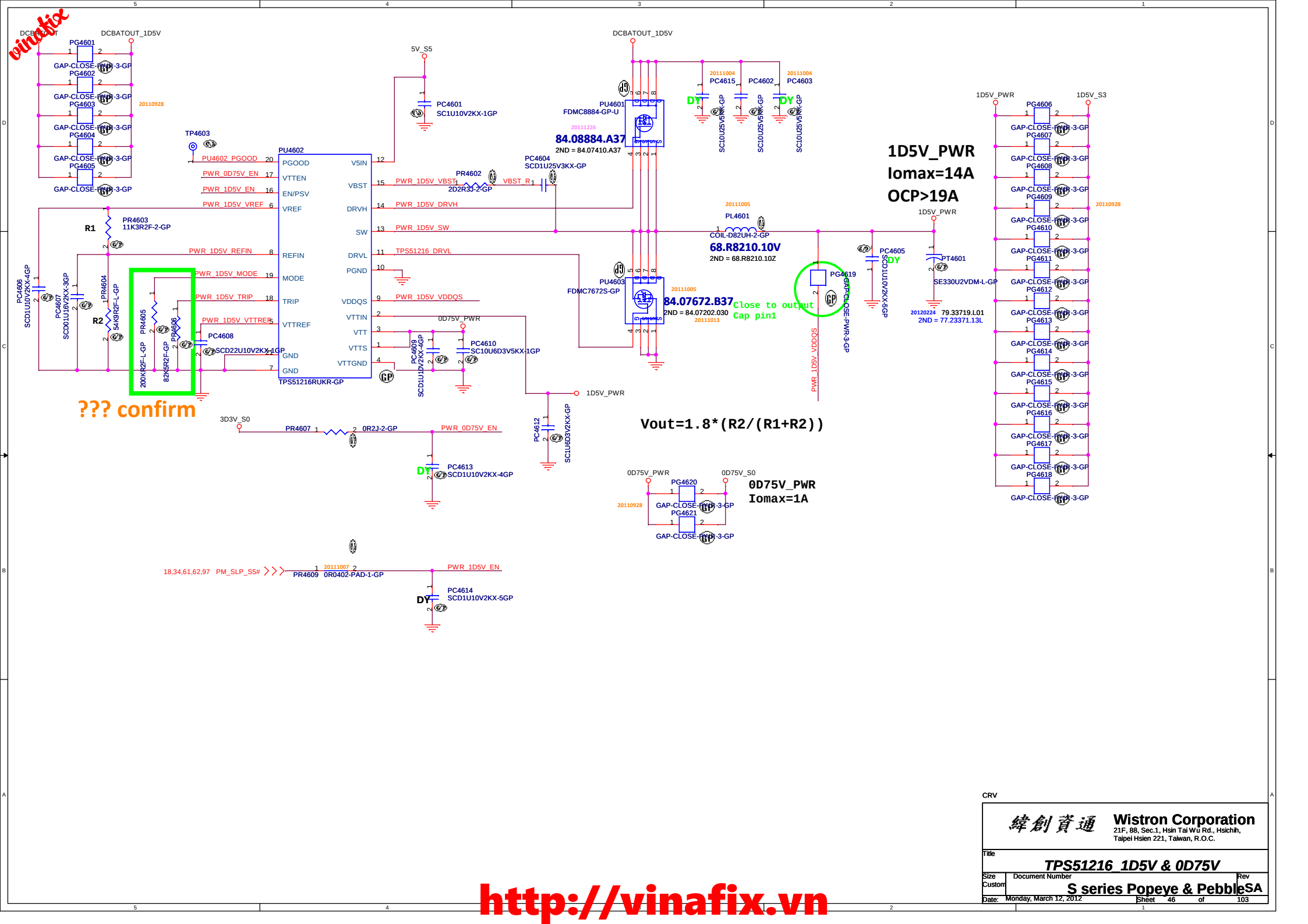
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51211_1D1V & 1D2V*

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 45 of 103



CRV

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_1D5V & 0D75V

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 46 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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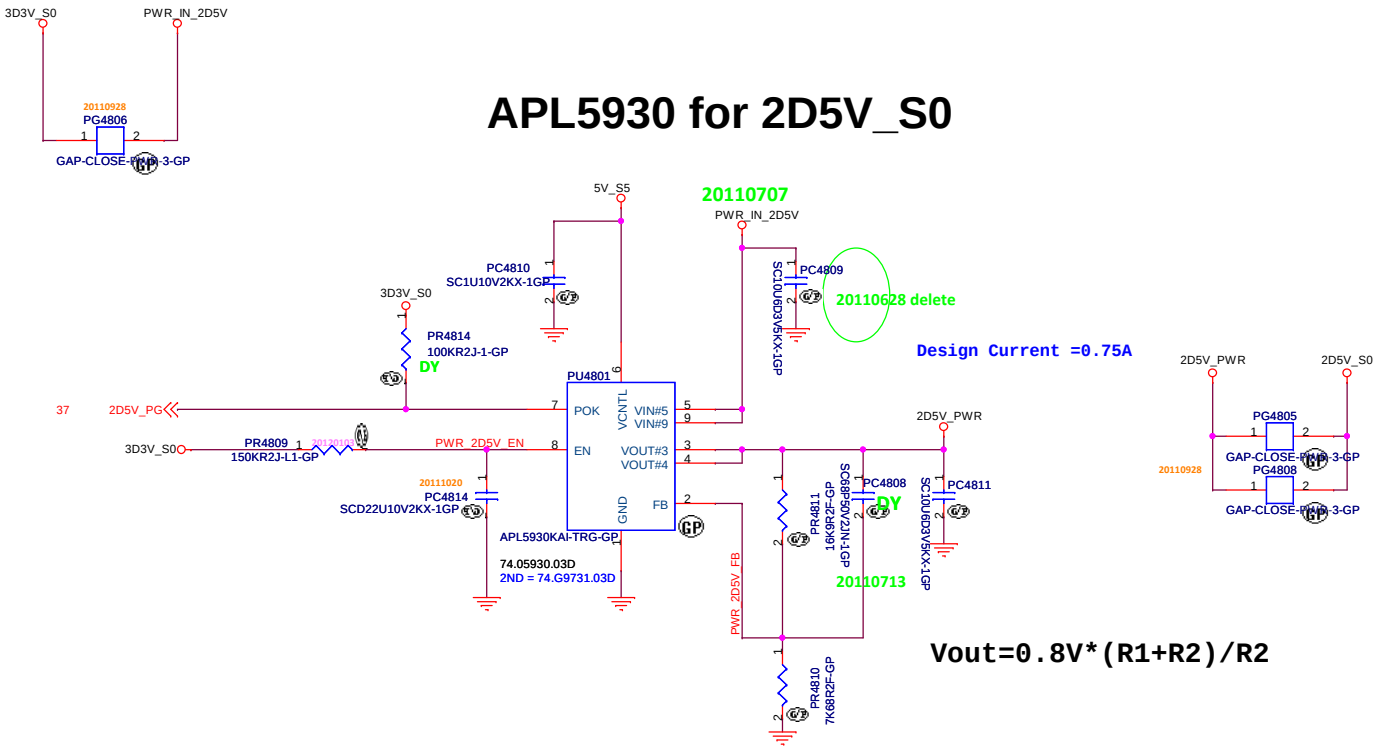
APL5930 for 2D5V_S0



Vout=0.8V*(R1+R2)/R2

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 2D5V

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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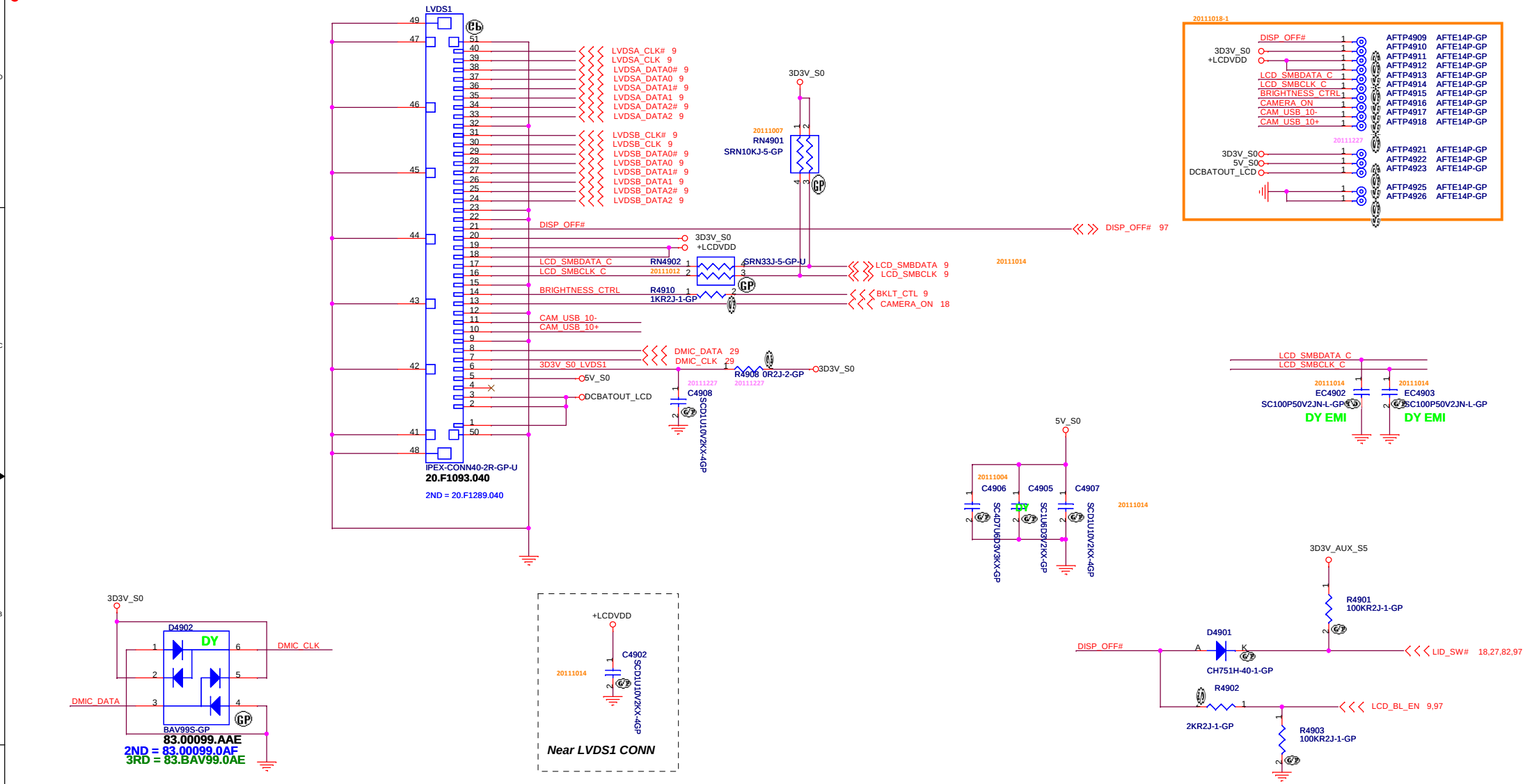
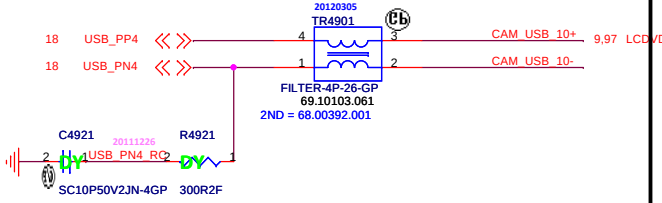
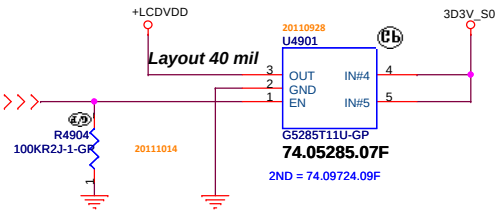
LCD Connector



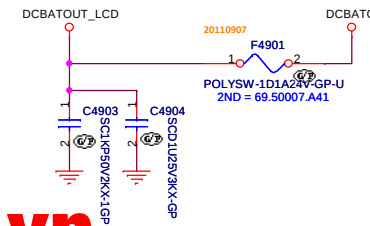
CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER



<Variant Name>

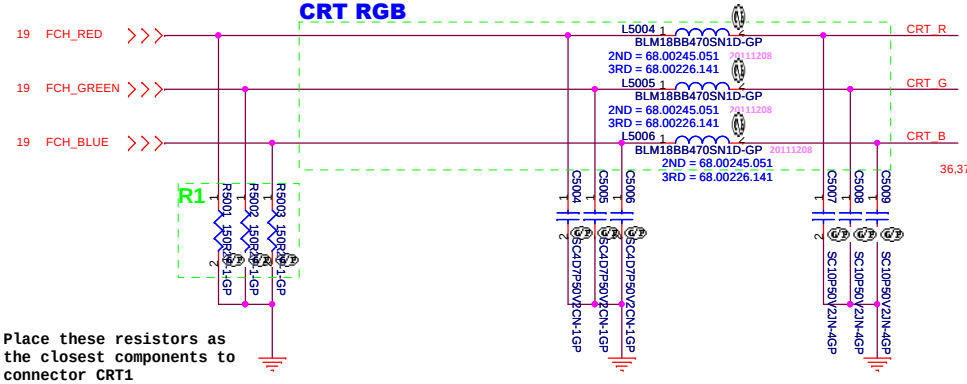
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA
Date: Monday, March 12, 2012 | Sheet 49 of 103

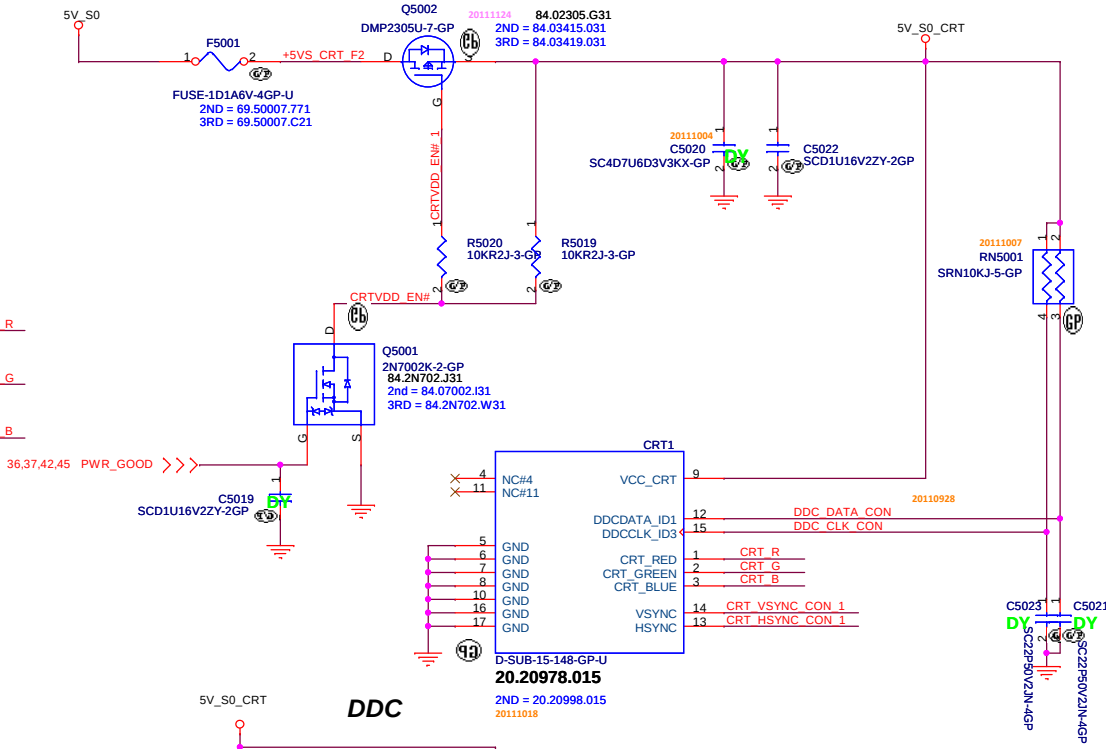
CRT Connector

FCH RGB to first R is 37.5 ohm with in 500 mil
First R to second R is 50 ohm
Second R to filter is 75 ohm(>50 ohm) to connector
Final CAP side to connector with 200 mil
ESD part to connector with 300 mil,width is 20mil

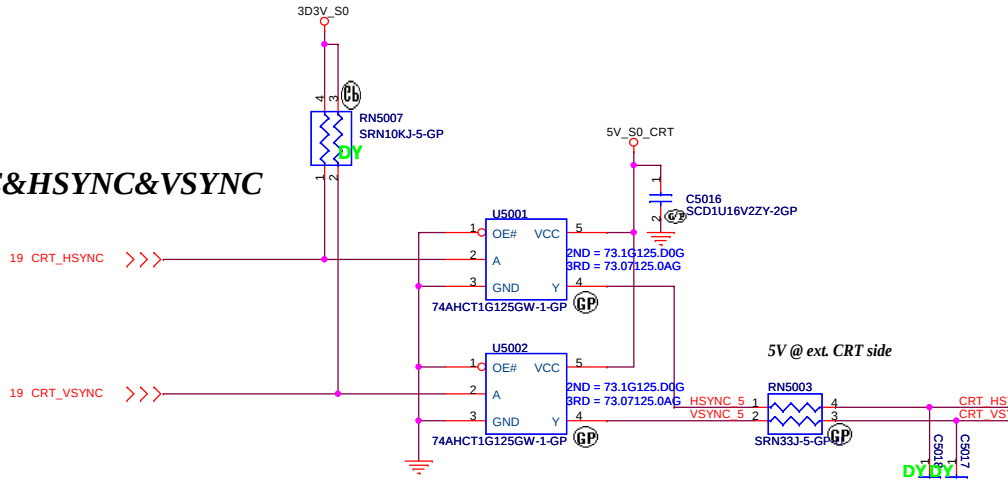
CRT RGB



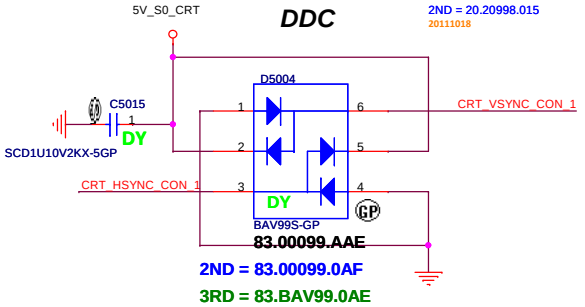
Place these resistors as the closest components to connector CRT1

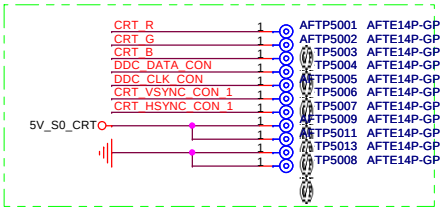


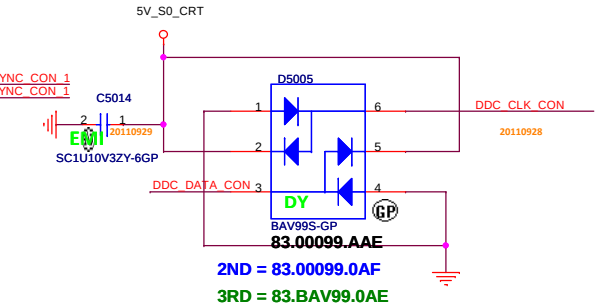
DDC&HSYNC&VSYNC

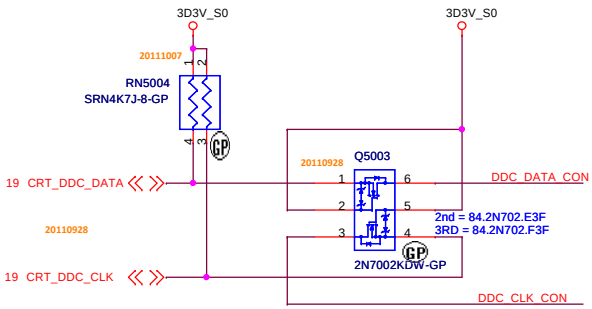


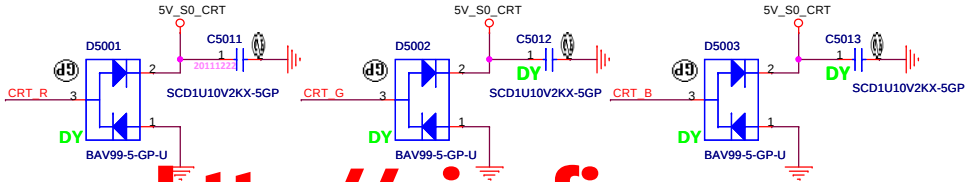
DDC











<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: A3
Document Number: S series Popeye & Pebble
Rev: SA
Date: Monday, March 12, 2012
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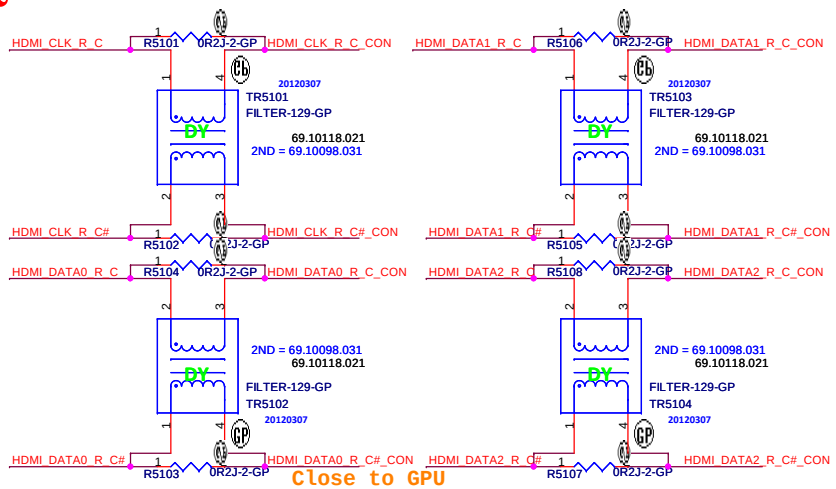
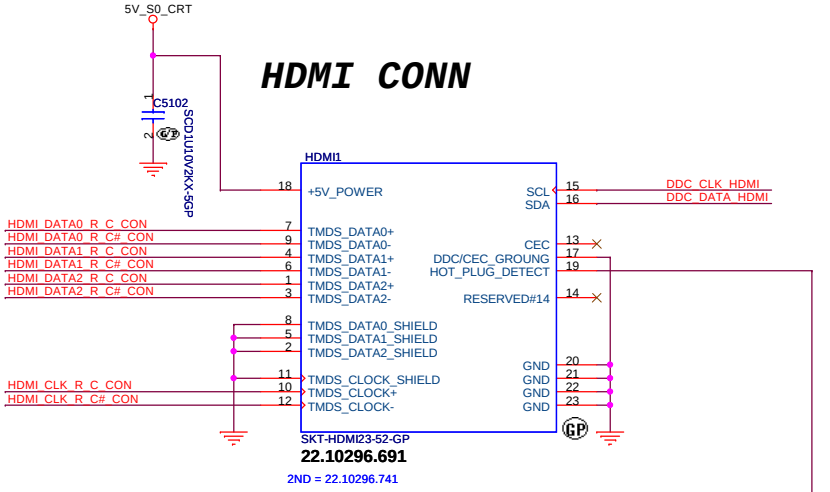
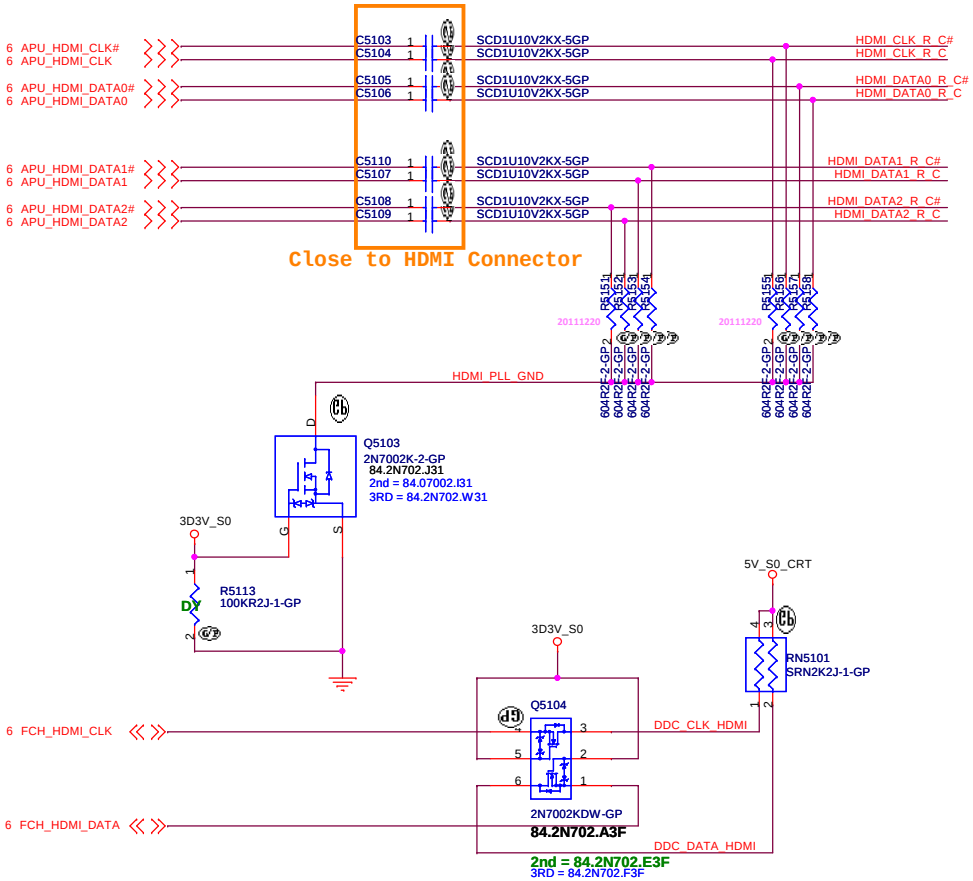
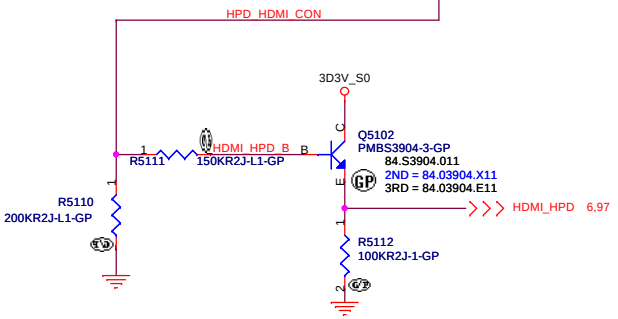
HDMI Connector



HDMI CONN







Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDMI Level Shifter/Conn
Size: A3	Document Number: S series Popeye & Pebble
Rev: SA	
Date: Monday, March 12, 2012	Sheet 51 of 103

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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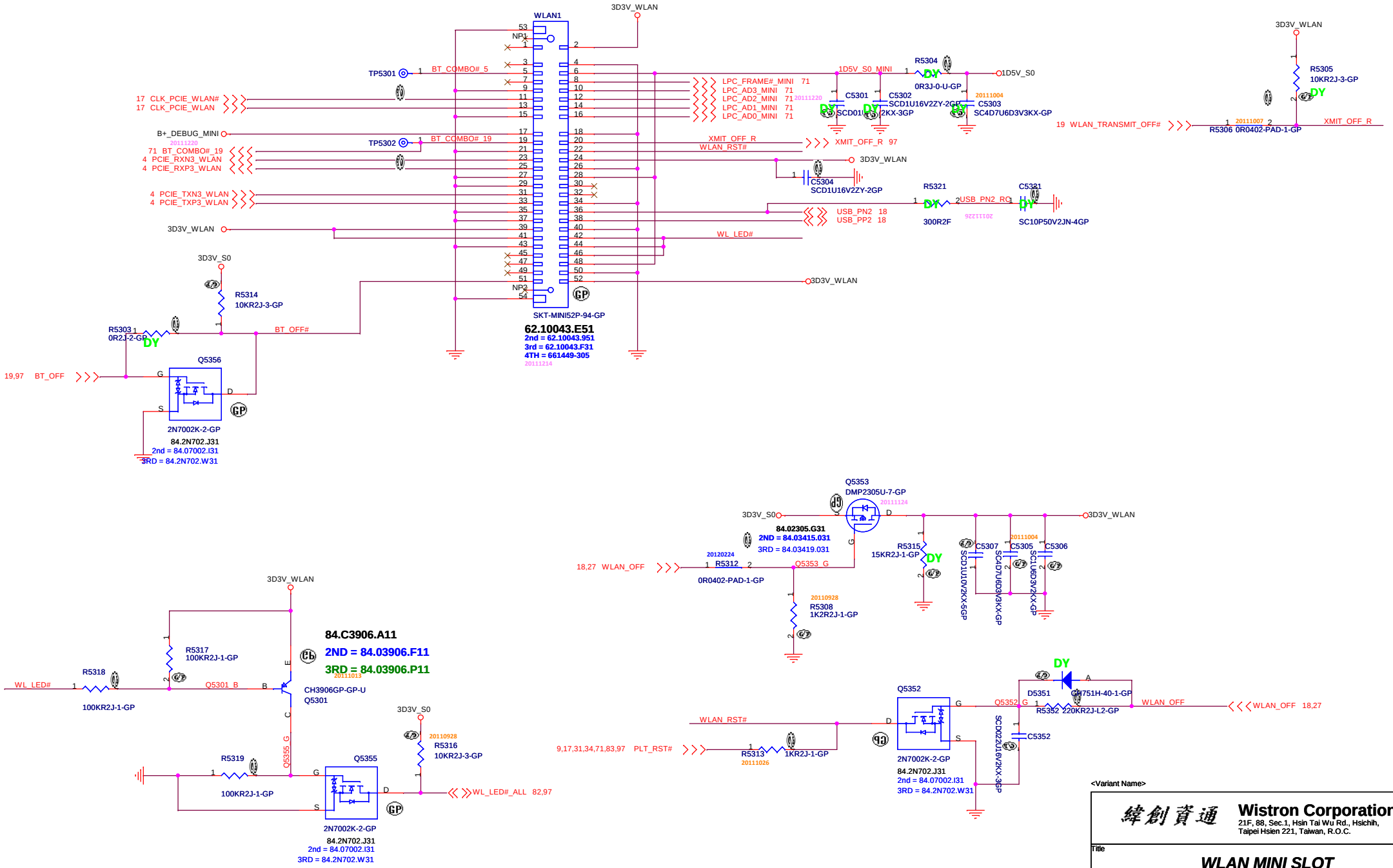
WLAN Connector

Mini-Card--WLAN (Half)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN MINI SLOT

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 53 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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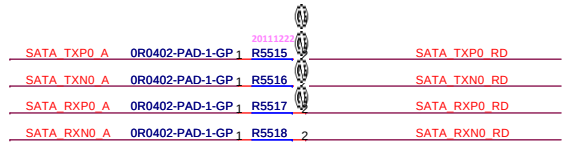
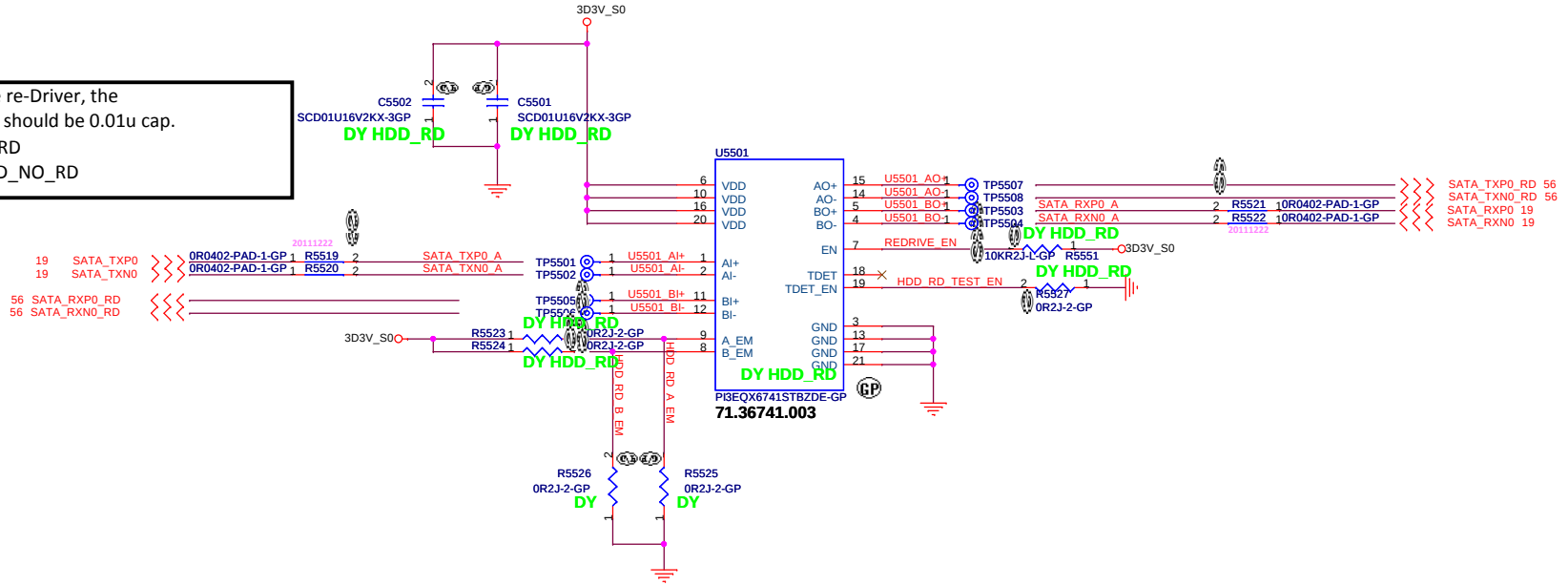
0624 SA
Rocky Only



Please put under re-Driver IC botton side.

If we use the re-Driver, the
R5519~5522 should be 0.01u cap.
Install HDD_RD
DUMMY HDD_NO_RD



Configuration Table - Output Emphasis/Swing Setting

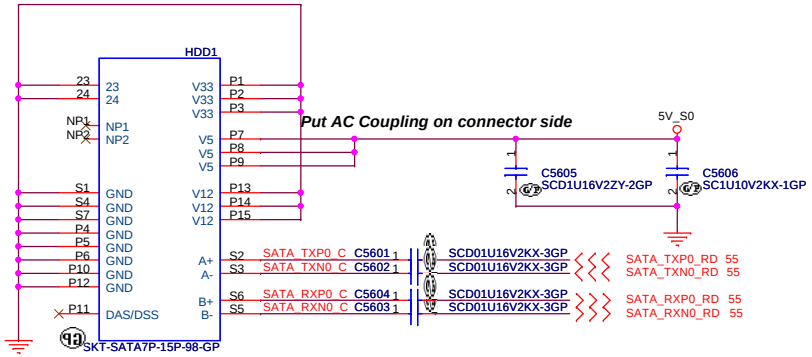
A_EM/B_EM	3 Gb/s	6 Gb/s
0	500mV pp	600mV pp
1	500mV pp + 3dB	600mV pp + 1.5dB

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA re-driver
Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA
Date: Monday, March 12, 2012 | Sheet 55 of 103

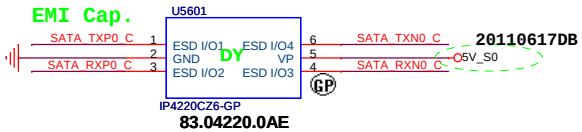
HDD Connector



22.10300.E31

2ND = 22.10300.F41

20111124 3RD = 22.10300.G71

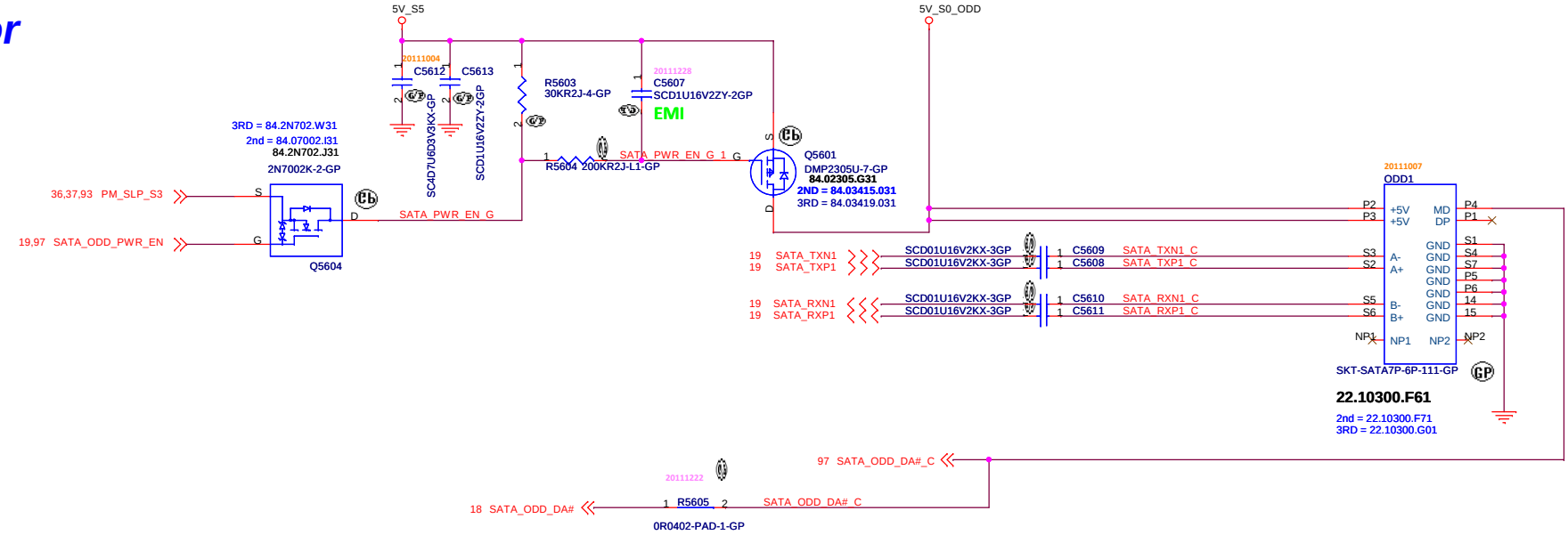


83.04220.0AE

2ND = 83.09904.AAE

3RD = 83.02304.0AE

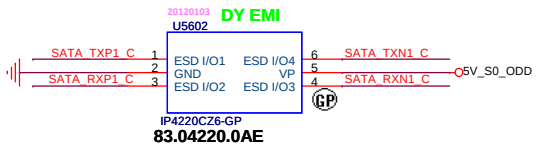
ODD Connector



22.10300.F61

2nd = 22.10300.F71

3RD = 22.10300.G01



83.04220.0AE

2ND = 83.09904.AAE

3RD = 83.02304.0AE

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 56 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 57 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 58 of 103

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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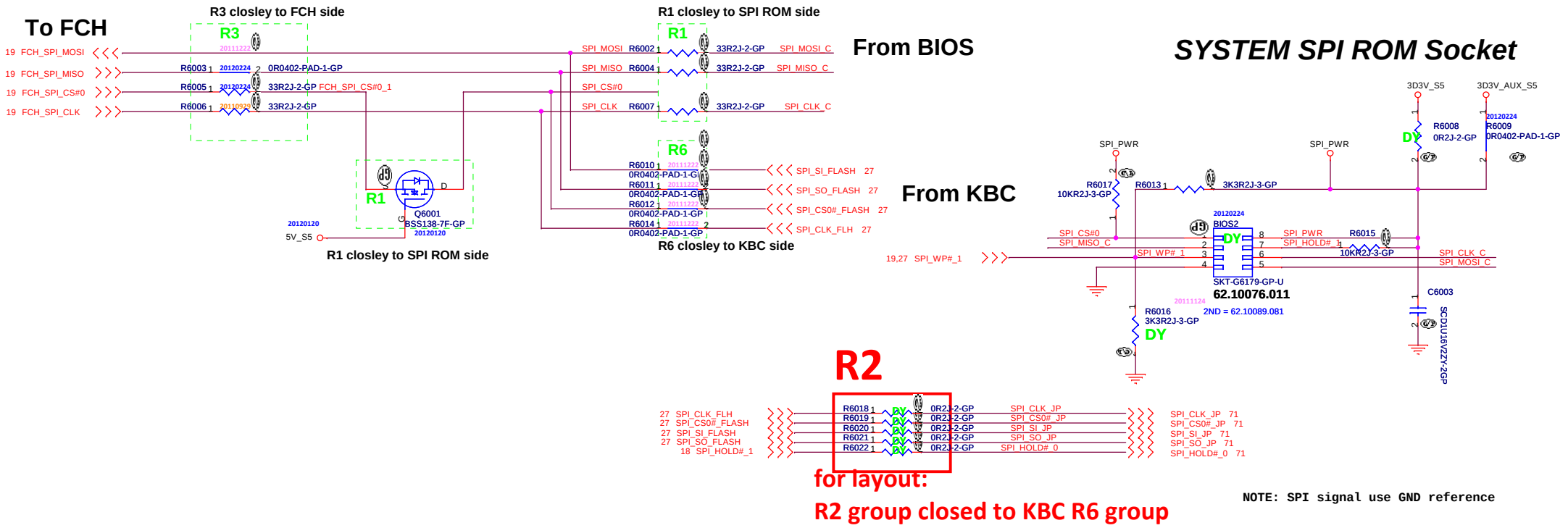
SSID = Flash.ROM



R2

for layout:
R2 group closed to KBC R6 group

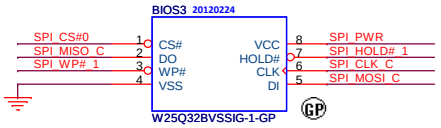
NOTE: SPI signal use GND reference

SS AMD Qualification plan in DB/SI1/PV build:				
Stage	1st	2nd	3rd	4th
DB	MX25L3206EM2I-12G			
SI	MX25L3206EM2I-12G	W25Q32BVSSIG		
PV	72.25032.F01 (SST)	72.25Q32.A01 (Winbond)	72.02532.A01 (AMIC)	72.25Q32.A01 (Winbond)

20111220

20120224

SYSTEM SPI ROM for MV



72.25Q32.A01

for layout:
BIOS3 co-layout with BIOS2 for MV

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

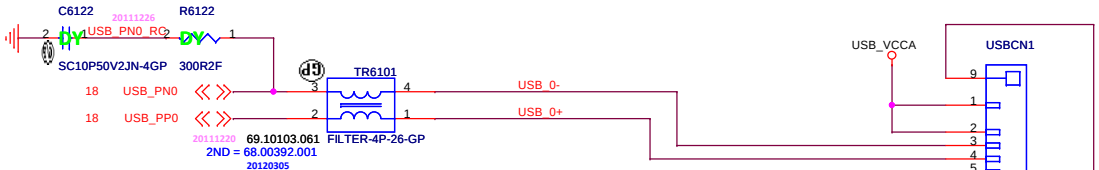
Title: ***Flash***

Size: A3 | Document Number: **S series Popeye & Pebble** | Rev: SA

Date: Monday, March 12, 2012 | Sheet 60 of 103

Right Side USB 2.0 Connector

USB 2.0 PORT 0 (Right side DB)



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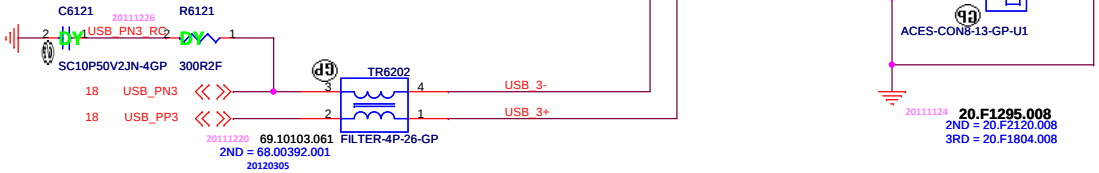
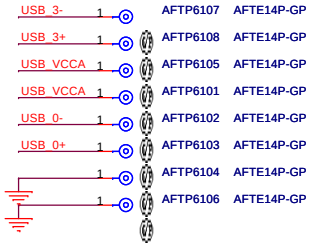
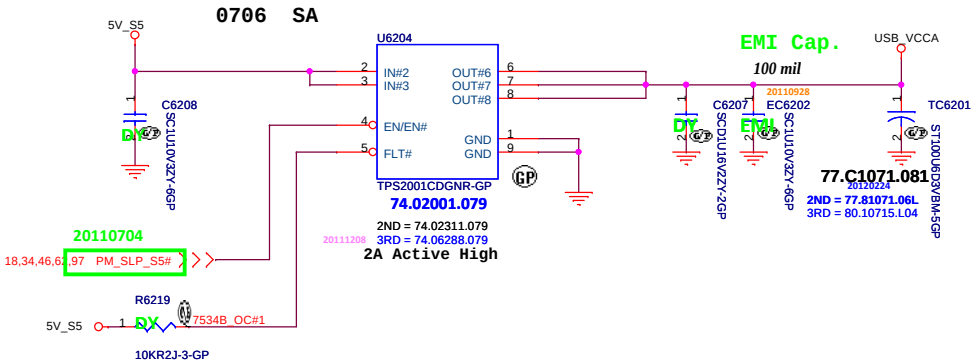
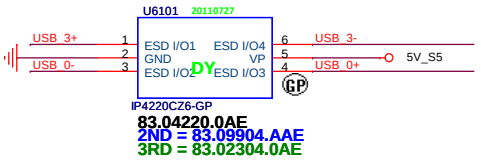




USB POWER

0706 SA





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: USB Power SW

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A3	S series Popeye & Pebble	SA

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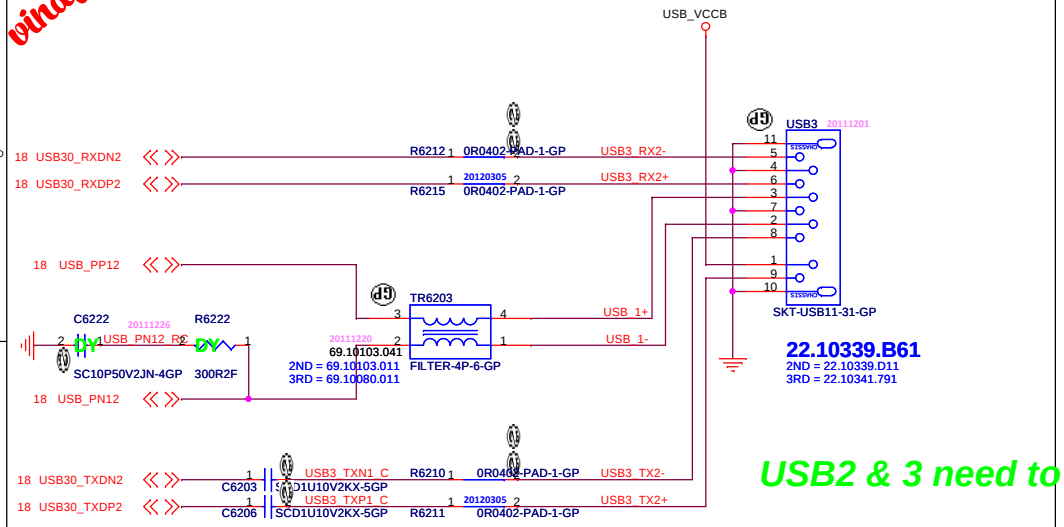
Left Side USB 3.0 Connector

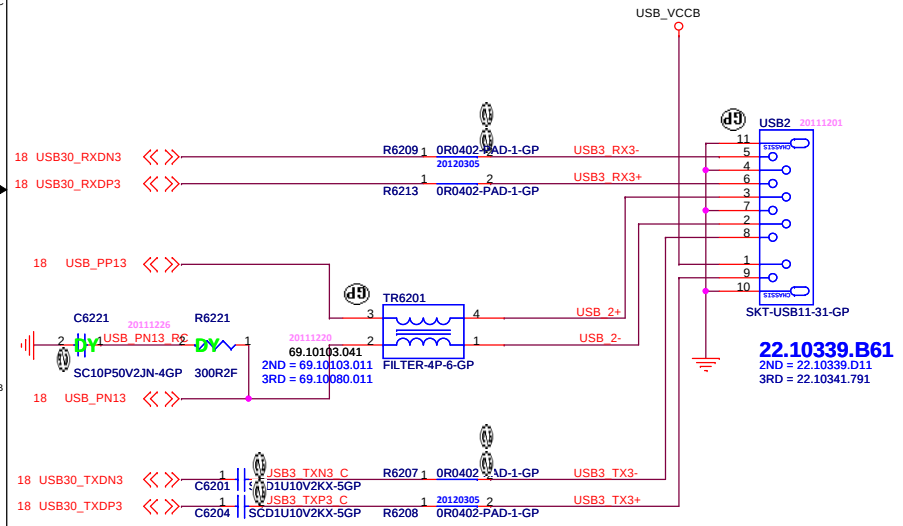


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

0622-2 SA

USB2 & 3 need to confirm???

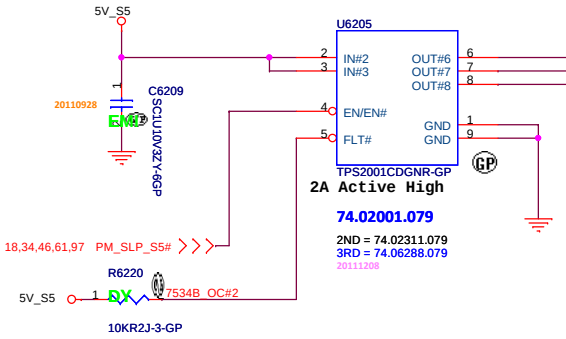
0706 SA Delete Test point

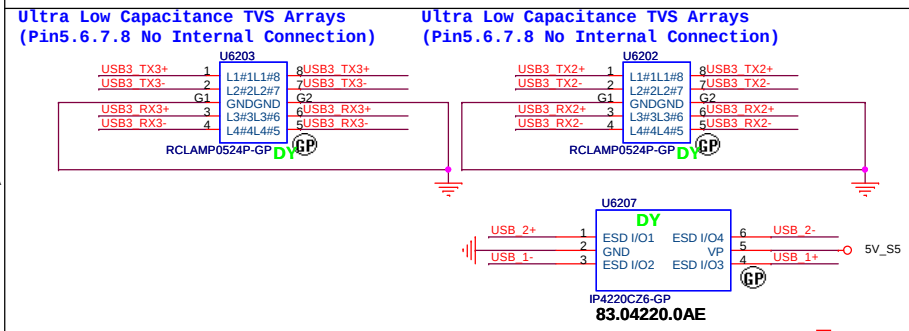


USB POWER

0622-2 SA

0706 SA





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A3	S series Popeye & Pebble	SA

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<Variant Name>

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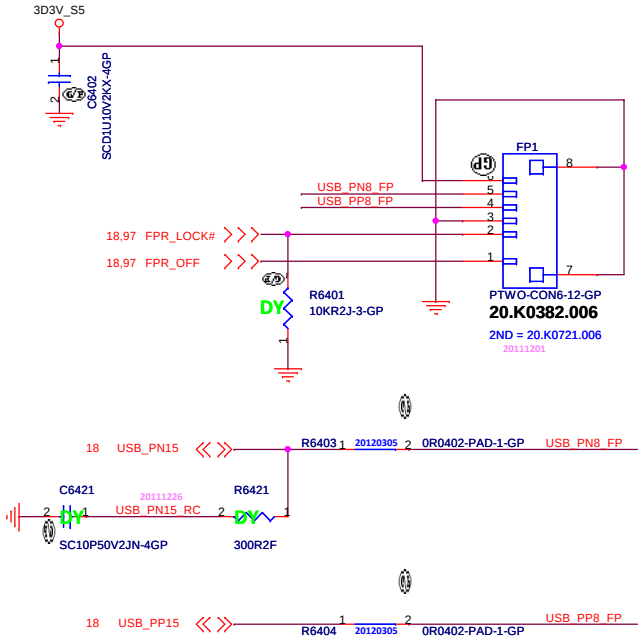
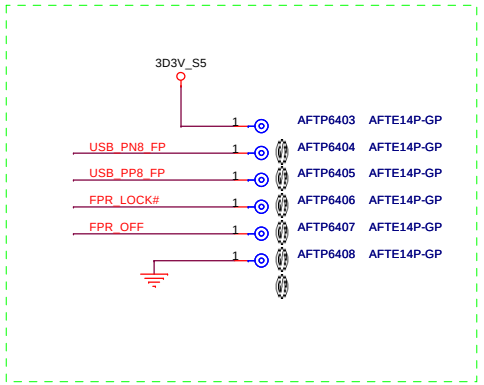
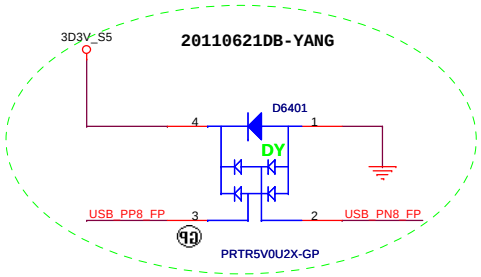
Finger Printer Connector







<Variant Name>

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Title	Finger Print Conn	
Size A3	Document Number S series Popeye & Pebble	Rev SA
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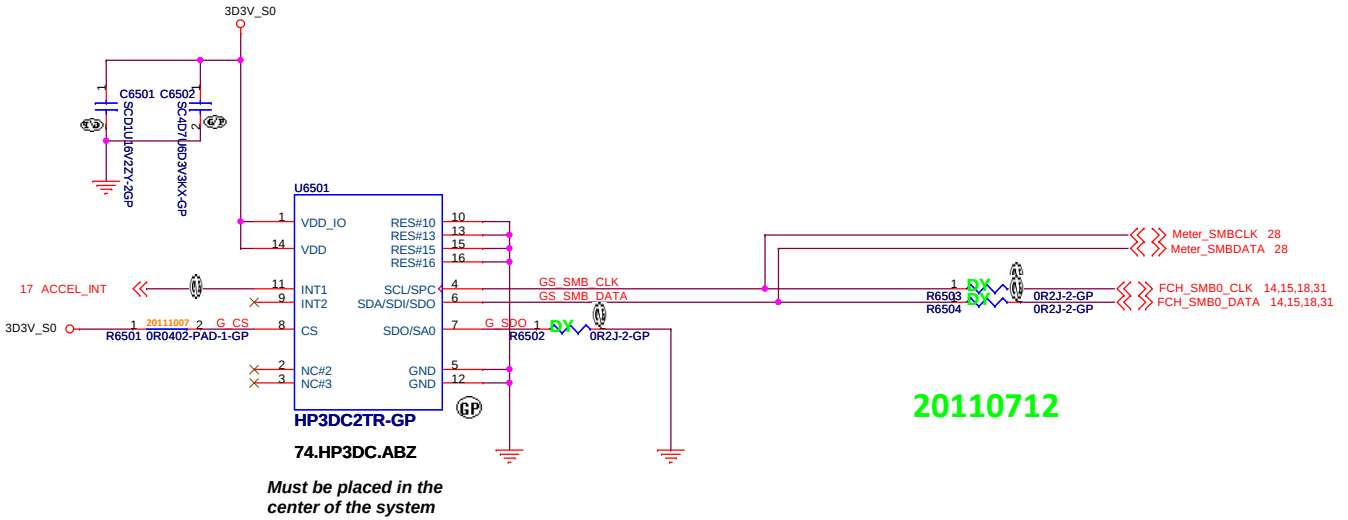
ACCELEROMETER



20110712

<Variant Name>

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Title	ACCELEROMETER
Size A3	Document Number: S series Popeye & Pebble
Rev	SA
Date: Monday, March 12, 2012	Sheet 65 of 103

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Title: *Reserved*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

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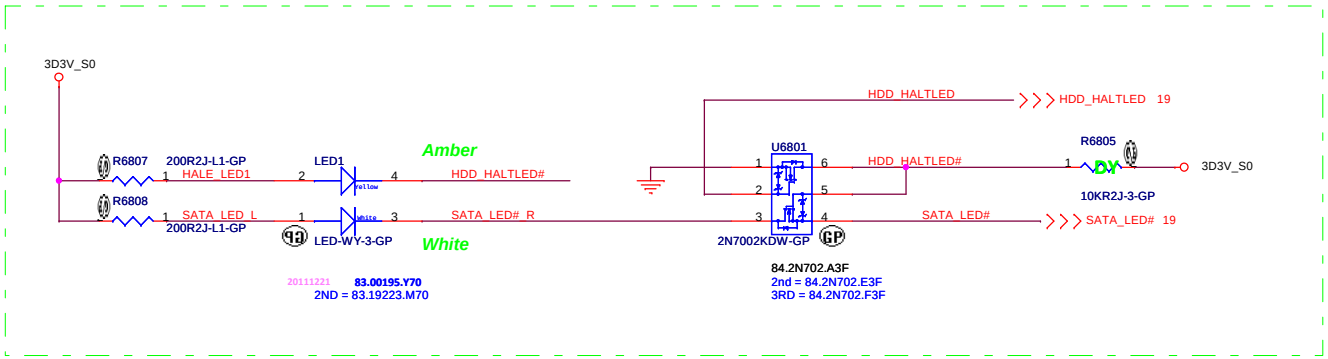
WLAN / WWAN POWER LED

HDD LED



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Control

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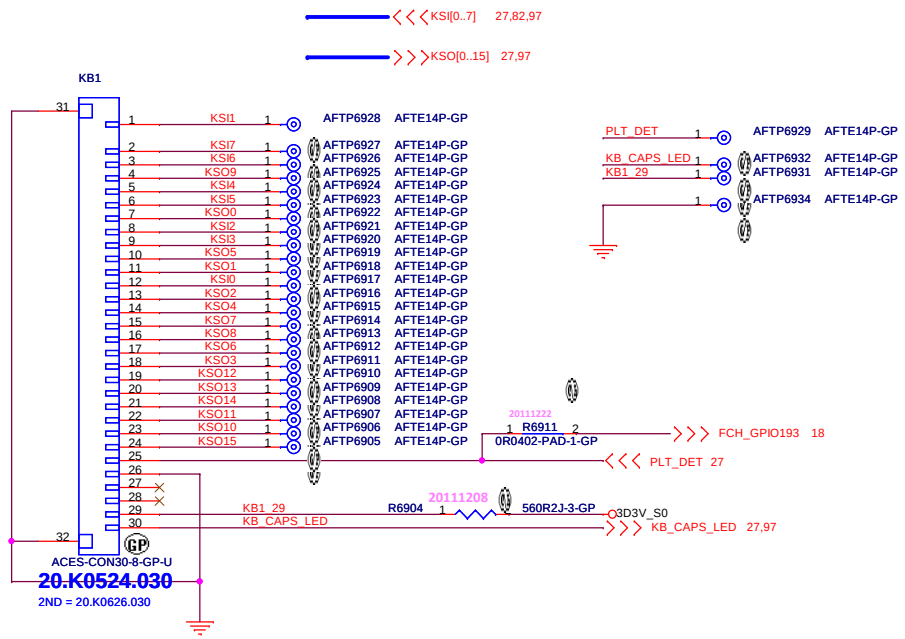
Keyboard Connector



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

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Title

(Reserved)

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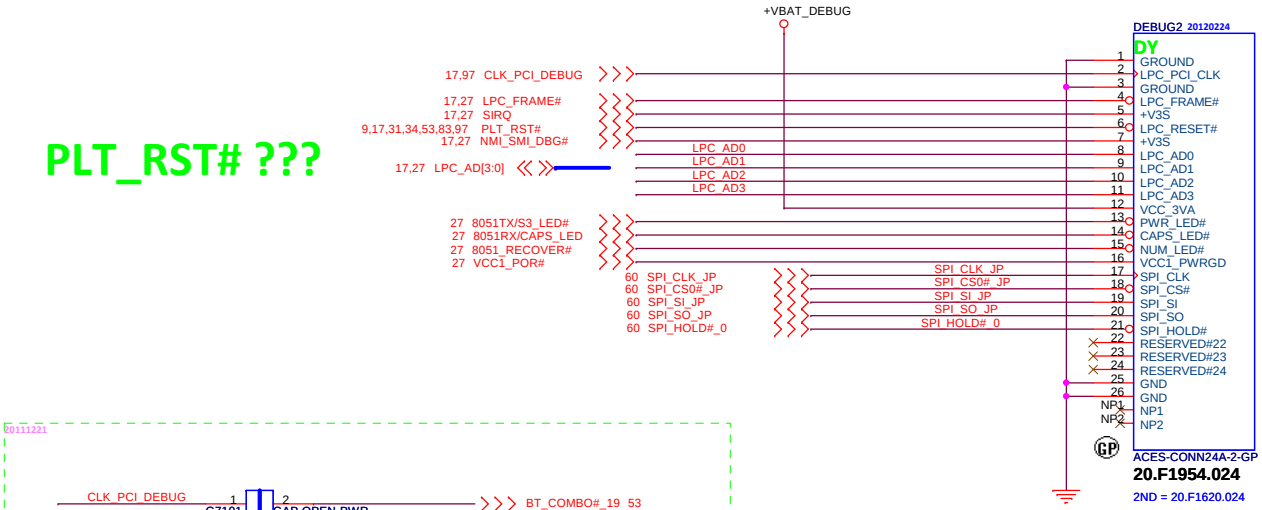
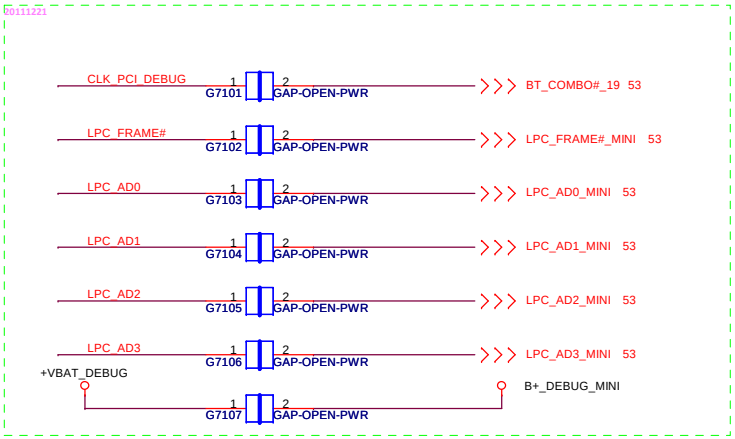
24 PIN LPC DEBUG CONN.

PLT_RST# ???





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Title: Dubug connector

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

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Title: *Reserved*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 72 of 103

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

Date: Monday, March 12, 2012 Sheet 75 of 103

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<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPM***

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A3	S series Popeye & Pebble	SA

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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A3	S series Popeye & Pebble	SA

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

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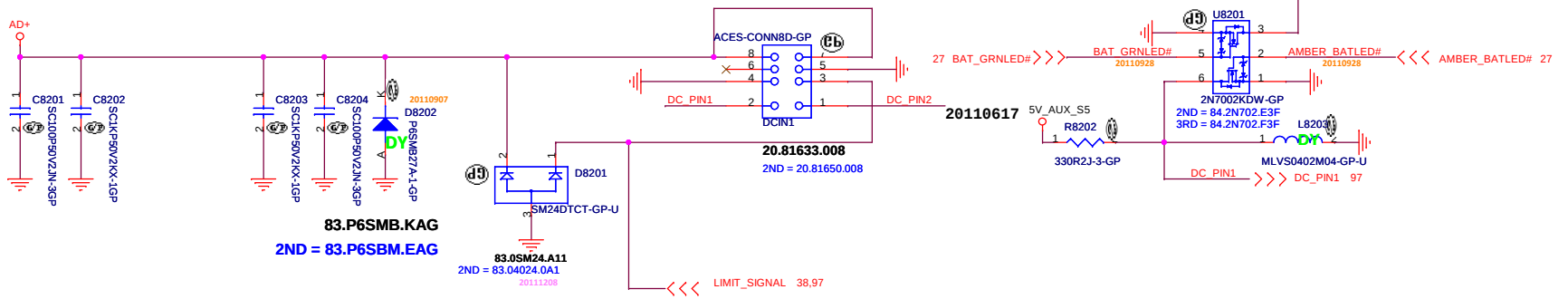
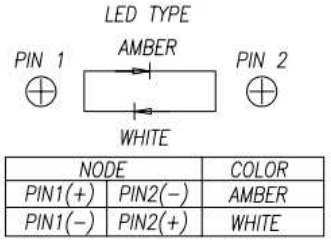
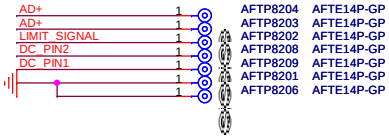
Adaptor in to generate DCBATOUT



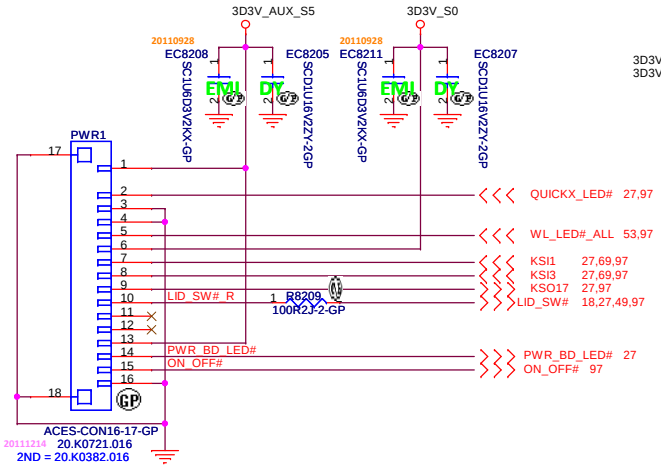
	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low

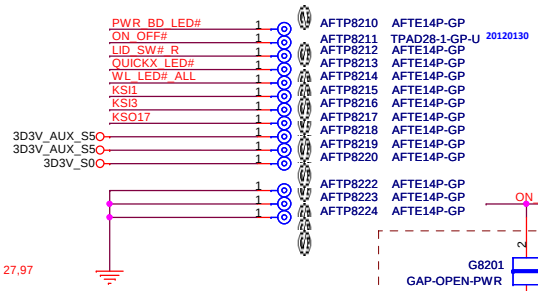


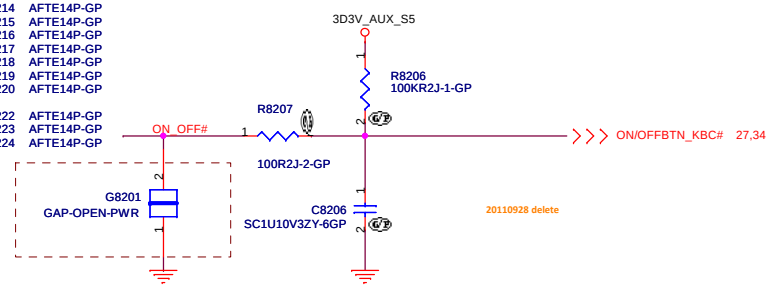
NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE



Power Button +Quick Lanch board







For layout: G8201

Under PWR1 and put on bottom side

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: POWER Button/ DCIN Connector

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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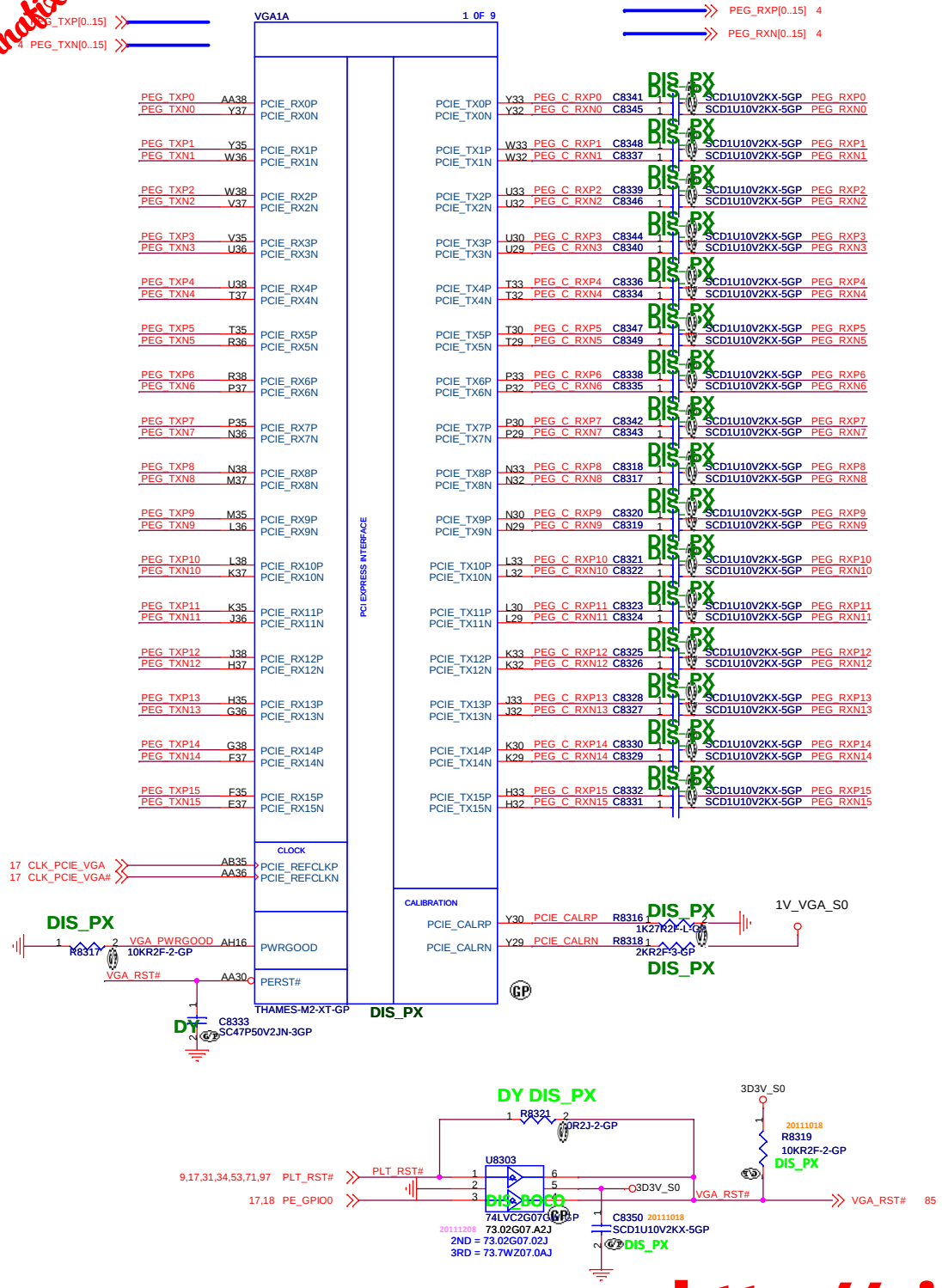
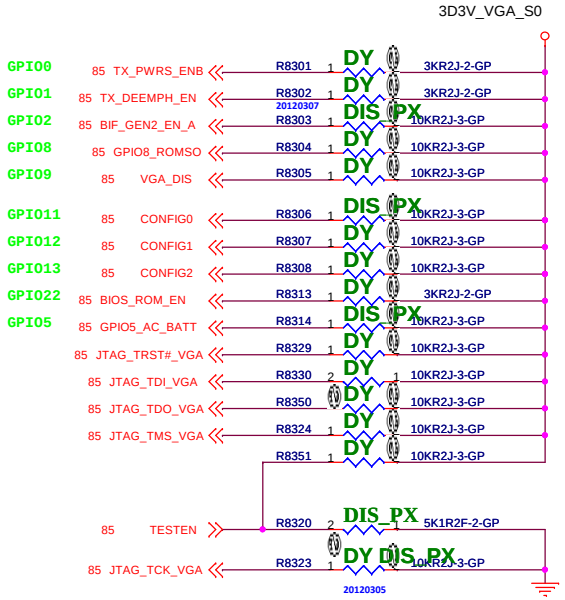


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	1
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

<Variant Name>

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Title: **GPU PCIE/STRAPPING(1/5)**

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VGA1C 3 OF 9 — GDDR5/DDR3 — MEMORY INTERFACE A

MDA0	C37	DQA0_0	MAA0_0	G24	MAA0	88,89	
MDA1	C35	DQA0_1	MAA0_1	J23	MAA1	88,89	
MDA2	A35	DQA0_2	MAA0_2	H24	MAA2	88,89	
MDA3	E34	DQA0_3	MAA0_3	J24	MAA3	88,89	
MDA4	G32	DQA0_4	MAA0_4	H26	MAA4	88,89	
MDA5	D33	DQA0_5	MAA0_5	J26	MAA5	88,89	
MDA6	F32	DQA0_6	MAA0_6	H21	MAA6	88,89	
MDA7	E32	DQA0_7	MAA0_7	G21	MAA7	88,89	
MDA8	D31	DQA0_8	MAA1_0	H19	MAA8	88,89	
MDA9	F30	DQA0_9	MAA1_1	H20	MAA9	88,89	
MDA10	C30	DQA0_10	MAA1_2	L13	MAA10	88,89	
MDA11	A30	DQA0_11	MAA1_3	G16	MAA11	88,89	
MDA12	F28	DQA0_12	MAA1_4	J16	MAA12	88,89	
MDA13	C28	DQA0_13	MAA1_5	H16	A_BA2	88,89	
MDA14	A28	DQA0_14	MAA1_6	J17	A_BA0	88,89	
MDA15	E28	DQA0_15	MAA1_7	H17	A_BA1	88,89	
MDA16	D27	DQA0_16					
MDA17	F26	DQA0_17	WCKA0_0	A32	DQMA0	88	
MDA18	C26	DQA0_18	WCKA0_0#	C32	DQMA1	88	
MDA19	A26	DQA0_19	WCKA0_1	D23	DQMA2	88	
MDA20	F24	DQA0_20	WCKA0_1#	E22	DQMA3	88	
MDA21	C24	DQA0_21	WCKA1_0	C14	DQMA4	89	
MDA22	A24	DQA0_22	WCKA1_0#	A14	DQMA5	89	
MDA23	E24	DQA0_23	WCKA1_1	E10	DQMA6	89	
MDA24	C22	DQA0_24	WCKA1_1#	D9	DQMA7	89	
MDA25	A22	DQA0_25					
MDA26	F22	DQA0_26	EDCA0_0	C34	QSAP_0	88	
MDA27	D21	DQA0_27	EDCA0_1	D29	QSAP_1	88	
MDA28	A20	DQA0_28	EDCA0_2	D25	QSAP_2	88	
MDA29	F20	DQA0_29	EDCA0_3	E20	QSAP_3	88	
MDA30	D19	DQA0_30	EDCA1_0	E16	QSAP_4	89	
MDA31	E18	DQA0_31	EDCA1_1	E12	QSAP_5	89	
MDA32	C18	DQA1_0	EDCA1_2	J10	QSAP_6	89	
MDA33	A18	DQA1_1	EDCA1_3	D7	QSAP_7	89	
MDA34	F18	DQA1_2					
MDA35	D17	DQA1_3	DDBIA0_0	A34	QSAN_0	88	
MDA36	A16	DQA1_4	DDBIA0_1	E30	QSAN_1	88	
MDA37	F16	DQA1_5	DDBIA0_2	E26	QSAN_2	88	
MDA38	D15	DQA1_6	DDBIA0_3	C20	QSAN_3	88	
MDA39	E14	DQA1_7	DDBIA1_0	C16	QSAN_4	89	
MDA40	F14	DQA1_8	DDBIA1_1	C12	QSAN_5	89	
MDA41	D13	DQA1_9	DDBIA1_2	J11	QSAN_6	89	
MDA42	F12	DQA1_10	DDBIA1_3	F8	QSAN_7	89	
MDA43	A12	DQA1_11					
MDA44	D11	DQA1_12	ADBIA0	J21	ODTA0	88	
MDA45	F10	DQA1_13	ADBIA1	G19	ODTA1	89	
MDA46	A10	DQA1_14					
MDA47	C10	DQA1_15	CLKA0	H27	CLKA0	88	
MDA48	G13	DQA1_16	CLKA0#	G27	CLKA0#	88	
MDA49	H13	DQA1_17					
MDA50	J13	DQA1_18	CLKA1	J14	CLKA1	89	
MDA51	H11	DQA1_19	CLKA1#	H14	CLKA1#	89	
MDA52	G10	DQA1_20					
MDA53	G8	DQA1_21	RASA0#	K23	RASA0#	88	
MDA54	K9	DQA1_22	RASA1#	K19	RASA1#	89	
MDA55	K10	DQA1_23					
MDA56	G9	DQA1_24	CASA0#	K20	CASA0#	88	
MDA57	A8	DQA1_25	CASA1#	K17	CASA1#	89	
MDA58	C8	DQA1_26					
MDA59	E8	DQA1_27	CSA0_0#	K24	CSA0#	88	
MDA60	A6	DQA1_28	CSA0_1#	K27			
MDA61	C6	DQA1_29					
MDA62	E6	DQA1_30	CSA1_0#	M13	CSA1#	89	
MDA63	A5	DQA1_31	CSA1_1#	K16			
MVREFDA	L18	MVREFDA	CKEA0	K21	CKEA0	88	
MVREFSA	L20	MVREFSA	CKEA1	J20	CKEA1	89	
MEM_CALRN0	L27	MEM_CALRN0	WEA0#	K26	WEA0#	88	
MEM_CALRN1	N12	MEM_CALRN1	WEA1#	L15	WEA1#	89	
MEM_CALRN2	AG12	MEM_CALRN2					
MEM_CALRP1	M12	MEM_CALRP1	MAA0_8	H23	MAA13	88,89	
MEM_CALRP0	M27	MEM_CALRP0	MAA1_8	J19	MAA14	88,89	
MEM_CALRP2	AH12	MEM_CALRP2	NC#M21	M21			
			NC#M20	M20			

DIS_PX

THAMES-M2-XT-GP

VGA1D 4 OF 9 — GDDR5/DDR3 — MEMORY INTERFACE B

MDB0	C5	DQB0_0	MAB0_0	P8	MAB0	90,91	
MDB1	C3	DQB0_1	MAB0_1	T9	MAB1	90,91	
MDB2	E3	DQB0_2	MAB0_2	P9	MAB2	90,91	
MDB3	F1	DQB0_3	MAB0_3	N7	MAB3	90,91	
MDB4	F1	DQB0_4	MAB0_4	N8	MAB4	90,91	
MDB5	F3	DQB0_5	MAB0_5	N9	MAB5	90,91	
MDB6	F5	DQB0_6	MAB0_6	U9	MAB6	90,91	
MDB7	G4	DQB0_7	MAB0_7	U8	MAB7	90,91	
MDB8	H5	DQB0_8	MAB1_0	Y9	MAB8	90,91	
MDB9	H6	DQB0_9	MAB1_1	W9	MAB9	90,91	
MDB10	J4	DQB0_10	MAB1_2	AC8	MAB10	90,91	
MDB11	K6	DQB0_11	MAB1_3	AC9	MAB11	90,91	
MDB12	K5	DQB0_12	MAB1_4	AA7	MAB12	90,91	
MDB13	L4	DQB0_13	MAB1_5	AA8	B_BA2	90,91	
MDB14	M6	DQB0_14	MAB1_6	Y8	B_BA0	90,91	
MDB15	M1	DQB0_15	MAB1_7	AA9	B_BA1	90,91	
MDB16	M3	DQB0_16					
MDB17	M5	DQB0_17	WCKB0_0	H3	DQMB0	90	
MDB18	N4	DQB0_18	WCKB0_0#	H1	DQMB1	90	
MDB19	P6	DQB0_19	WCKB0_1	T3	DQMB2	90	
MDB20	P5	DQB0_20	WCKB0_1#	T5	DQMB3	90	
MDB21	R4	DQB0_21	WCKB1_0	AE4	DQMB4	91	
MDB22	T6	DQB0_22	WCKB1_0#	AF5	DQMB5	91	
MDB23	T1	DQB0_23	WCKB1_1	AK6	DQMB6	91	
MDB24	U4	DQB0_24	WCKB1_1#	AK5	DQMB7	91	
MDB25	V6	DQB0_25					
MDB26	V1	DQB0_26	EDCB0_0	F6	QSBP_0	90	
MDB27	V3	DQB0_27	EDCB0_1	K3	QSBP_1	90	
MDB28	Y6	DQB0_28	EDCB0_2	P3	QSBP_2	90	
MDB29	Y1	DQB0_29	EDCB0_3	V5	QSBP_3	90	
MDB30	Y3	DQB0_30	EDCB1_0	AB5	QSBP_4	91	
MDB31	Y5	DQB0_31	EDCB1_1	AH1	QSBP_5	91	
MDB32	AA4	DQB1_0	EDCB1_2	AJ9	QSBP_6	91	
MDB33	AB6	DQB1_1	EDCB1_3	AM5	QSBP_7	91	
MDB34	AB1	DQB1_2					
MDB35	AB3	DQB1_3	DDBIB0_0	G7	QSBN_0	90	
MDB36	AD6	DQB1_4	DDBIB0_1	K1	QSBN_1	90	
MDB37	AD1	DQB1_5	DDBIB0_2	P1	QSBN_2	90	
MDB38	AD3	DQB1_6	DDBIB0_3	W4	QSBN_3	90	
MDB39	AD5	DQB1_7	DDBIB1_0	AC4	QSBN_4	91	
MDB40	AF1	DQB1_8	DDBIB1_1	AH3	QSBN_5	91	
MDB41	AF3	DQB1_9	DDBIB1_2	AJ8	QSBN_6	91	
MDB42	AF6	DQB1_10	DDBIB1_3	AM3	QSBN_7	91	
MDB43	AG4	DQB1_11					
MDB44	AH5	DQB1_12	ADBIB0	T7	ODTB0	90	
MDB45	AH6	DQB1_13	ADBIB1	W7	ODTB1	91	
MDB46	AJ4	DQB1_14					
MDB47	AK3	DQB1_15	CLKB0	L9	CLKB0	90	
MDB48	AF8	DQB1_16	CLKB0#	L8	CLKB0#	90	
MDB49	AF9	DQB1_17					
MDB50	AG8	DQB1_18	CLKB1	AD8	CLKB1	91	
MDB51	AG7	DQB1_19	CLKB1#	AD7	CLKB1#	91	
MDB52	AK9	DQB1_20					
MDB53	AL7	DQB1_21	RASB0#	T10	RASB0#	90	
MDB54	AM8	DQB1_22	RASB1#	Y10	RASB1#	91	
MDB55	AM7	DQB1_23					
MDB56	AK1	DQB1_24	CASB0#	W10	CASB0#	90	
MDB57	AL4	DQB1_25	CASB1#	AA10	CASB1#	91	
MDB58	AM6	DQB1_26					
MDB59	AM1	DQB1_27	CSB0_0#	P10	CSB0#	90	
MDB60	AN4	DQB1_28	CSB0_1#	L10			
MDB61	AP3	DQB1_29					
MDB62	AP1	DQB1_30	CSB1_0#	AD10	CSB1#	91	
MDB63	AP5	DQB1_31	CSB1_1#	AC10			
MVREFDB	Y12	MVREFDB	CKEB0	U10	CKEB0	90	
MVREFSB	AA12	MVREFSB	CKEB1	AA11	CKEB1	91	
			WEB0#	N10	WEB0#	90	
			WEB1#	AB11	WEB1#	91	
			MAB0_8	T8	MAB13	90,91	
			MAB1_8	W8	MAB14	90,91	
			NC#U12	U12			
			NC#V12	V12			
DRAM_RST	AH11	DRAM_RST					

DIS_PX

THAMES-M2-XT-GP

90 MDB[0..31]

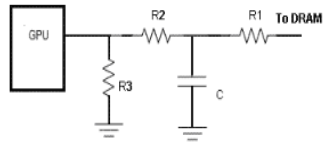
91 MDB[32..63]

89 MDA[32..63]

88 [illegible]

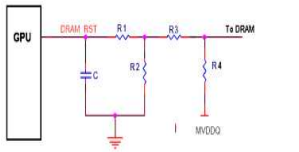
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

Vancouver



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

Mannhatton



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

20110618 delete

R8420 10R2J-2-GP — DRAM_RST_RC — R8402 51R2J-2-GP — MEM_RST 88,89,90,91

R8404 5K1R2F-2-GP

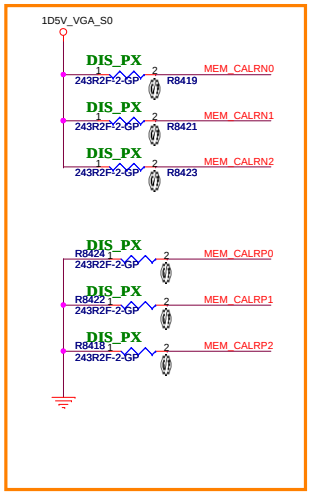
C8401 SC120P50V2JN-1GP

if for Mannhatton,have to change to other value

VANCOUVER

This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

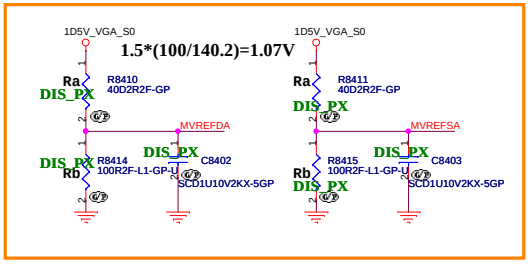
Need check reference circuit not match checklist



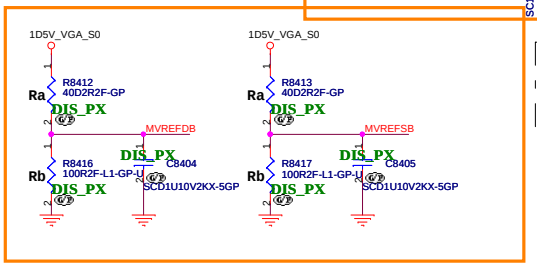
NOTES:

1.Seymour-S3 uses memory group A only.

2.Seymour-M2 uses memory group B only.



Robson_Seymour_Whistler Need Pop



Robson_Seymour_Whistler Need Pop

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	40.2R	40.2R	40.2R

Notes:

All signals in this interface can be unconnected if not used, with the exception of all MVREFDA/MVREFSA/MVREFDB/MVREFSB signals and MEM_CALRN0/MEM_CALRP0/MEM_CALRN1/MEM_CALRP1 which must remain connected.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 84 of 103

VBIOS	GPIO101	GPIO102	MEM_ID3 R8521	MEM_ID2 R8522	MEM_ID1 R8520	MEM_ID0 R8519	Brand	Size	Part Number	Die Ver.	Wistron PN	HP PN
VBIOS#1 14" Popeye Old Die	0	0		0	0	0	Samsung	1G (64Mx16)	K4W1G1646G-BC11	G die		506474-945
				0	0	1	Samsung	2G (128Mx16)	K4W2G1646C-HC11	C die		601498-953
				0	1	0	Hynix	1G (64Mx16)	H5TQ1G63DFR-11C	D die		506474-344
				0	1	1	Hynix	2G (128Mx16)	H5TQ2G63DFR-11C	B die		
				1	1	0	Micron	1G (64Mx16)	MT41J64M16JT-107G	G die		506474-642
				1	1	1	Micron	2G (128Mx16)	MT41J128M16HA-107G	D die		601498-652
VBIOS#3 14" Popeye New Die	0	1		0	0	0	Samsung	1G (64Mx16)				
				0	0	1	Samsung	2G (128Mx16)	K4W2G1646E-HC11	E die		601498-954
				0	1	0	Hynix	1G (64Mx16)				
				0	1	1	Hynix	2G (128Mx16)	H5TQ2G63DFR-11C	D die		601498-353
				1	1	0	Micron	1G (64Mx16)				
				1	1	1	Micron	2G (128Mx16)	MT41J128M16JT-107G	K die		
	0=15" 1=14"	0=old die 1=new die	Reserve	00=Samsung; 01=Hynix 10=Elpida; 11=Micron			0=1GB 1=2GB					

20120305

Set DVP as 1.8-V (VDDR4/5) general I/O

20110706

CTF setpoint is 118°C, and is programmed during ASIC initialization.

PX_EN is tri-state before internal PWRGOOD is asserted and PERSTb is de-asserted.

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

VREFG = 1.80 V / 3 (or 0.60 V typ)

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

LVDS Interface

20110625 link to KBC!!!

20110620 need to confirm???

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 85 of 103

dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DP[F:E]_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 , and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF

For DDR3/GDDR5, MVDDQ = 1.5V

(1.5V@1500mA VDDR1)

1.5A

120R@300mA

(1.8V@219mA VDD_CT)

17mA

60mA

170mA

(1.8V@400mA PCIE_VDDR)

440mA

(1.0V@1100mA PCIE_VDDC)

1.1A

150mA

(0.95~1.12V@12900mA VDDC+VDDCI)

4A

20110620

	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##	
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA_S0

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE

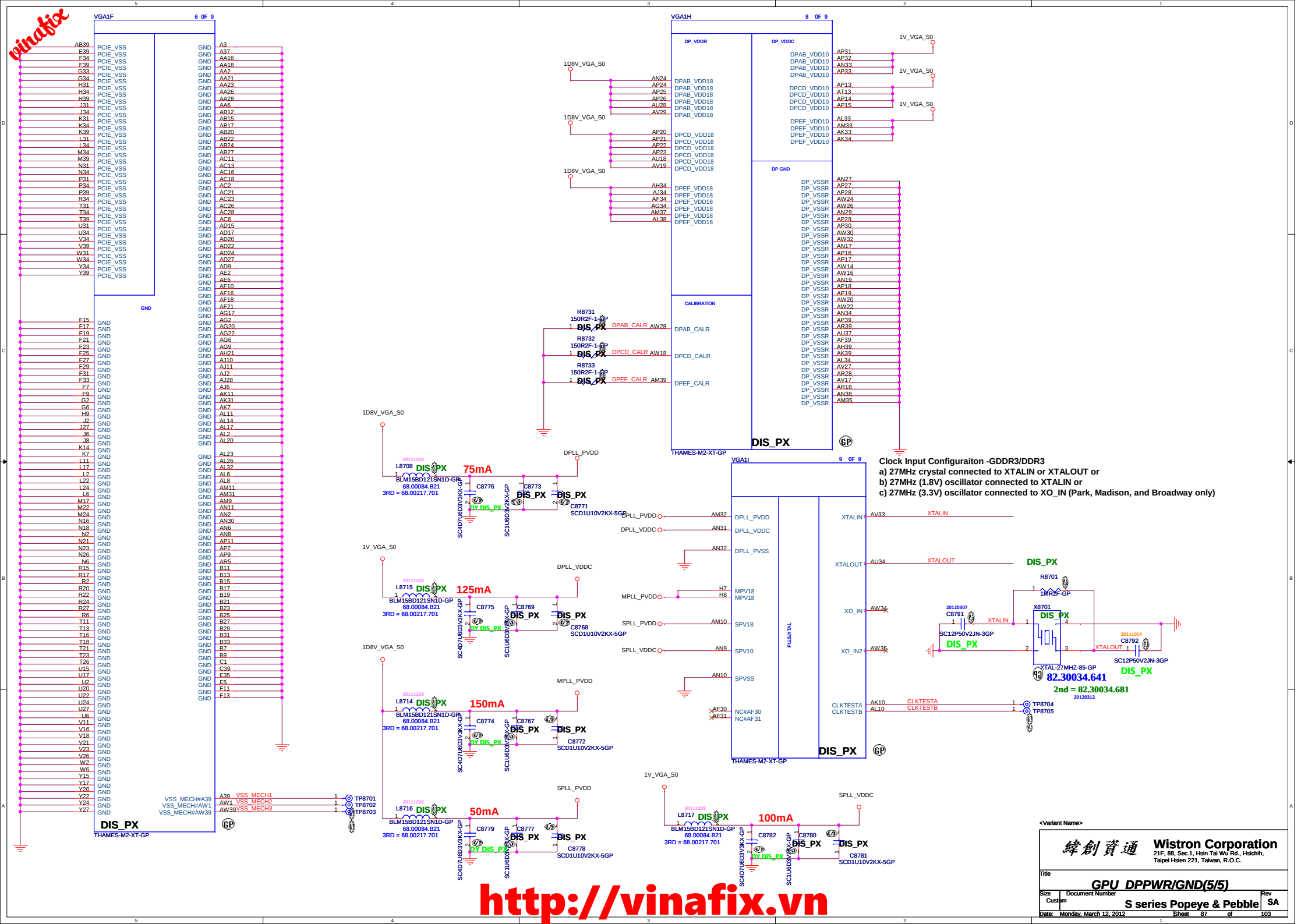
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

Date: Monday, March 12, 2012 | Sheet 86 of 103



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU DPPWR/GND(5/5)

Size: Custom | Document Number: S series Popeye & Pebble | Rev: SA

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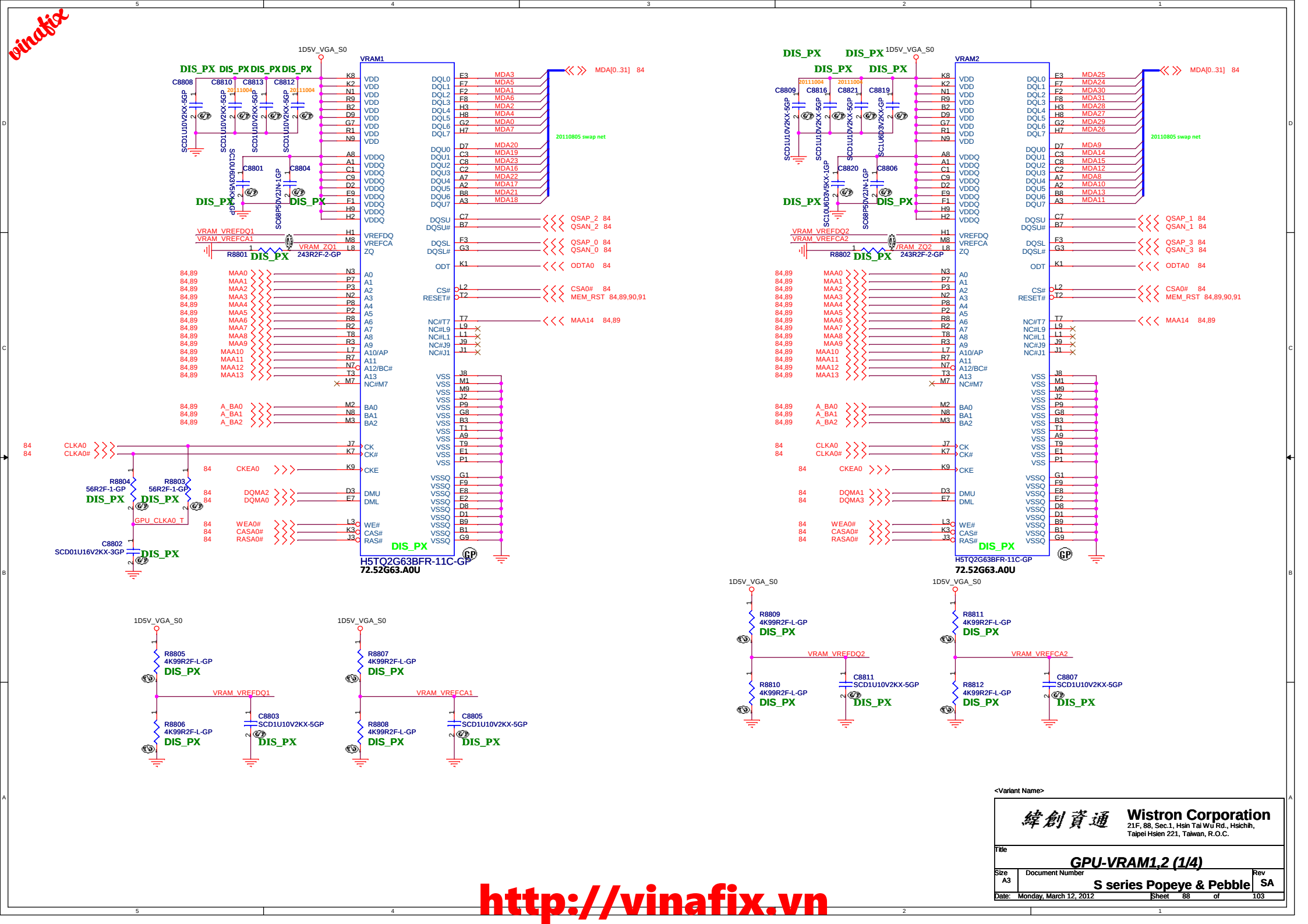

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: S series Popeye & Pebble | Rev: SA

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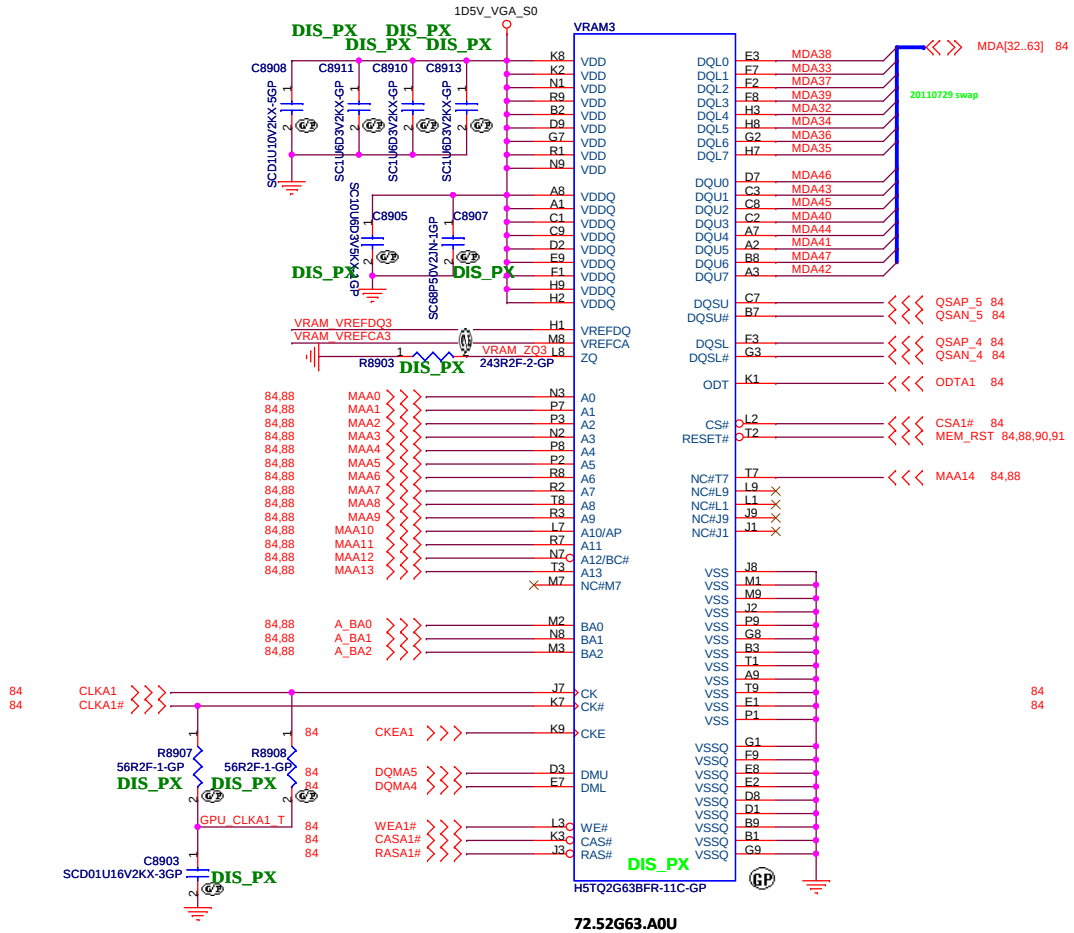

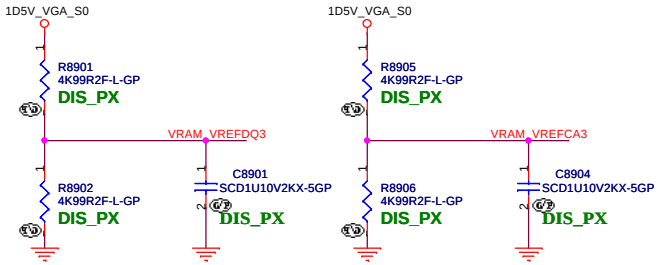

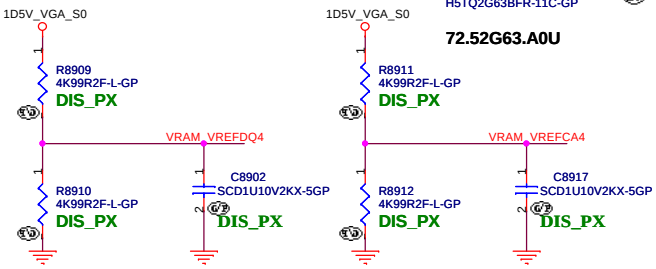

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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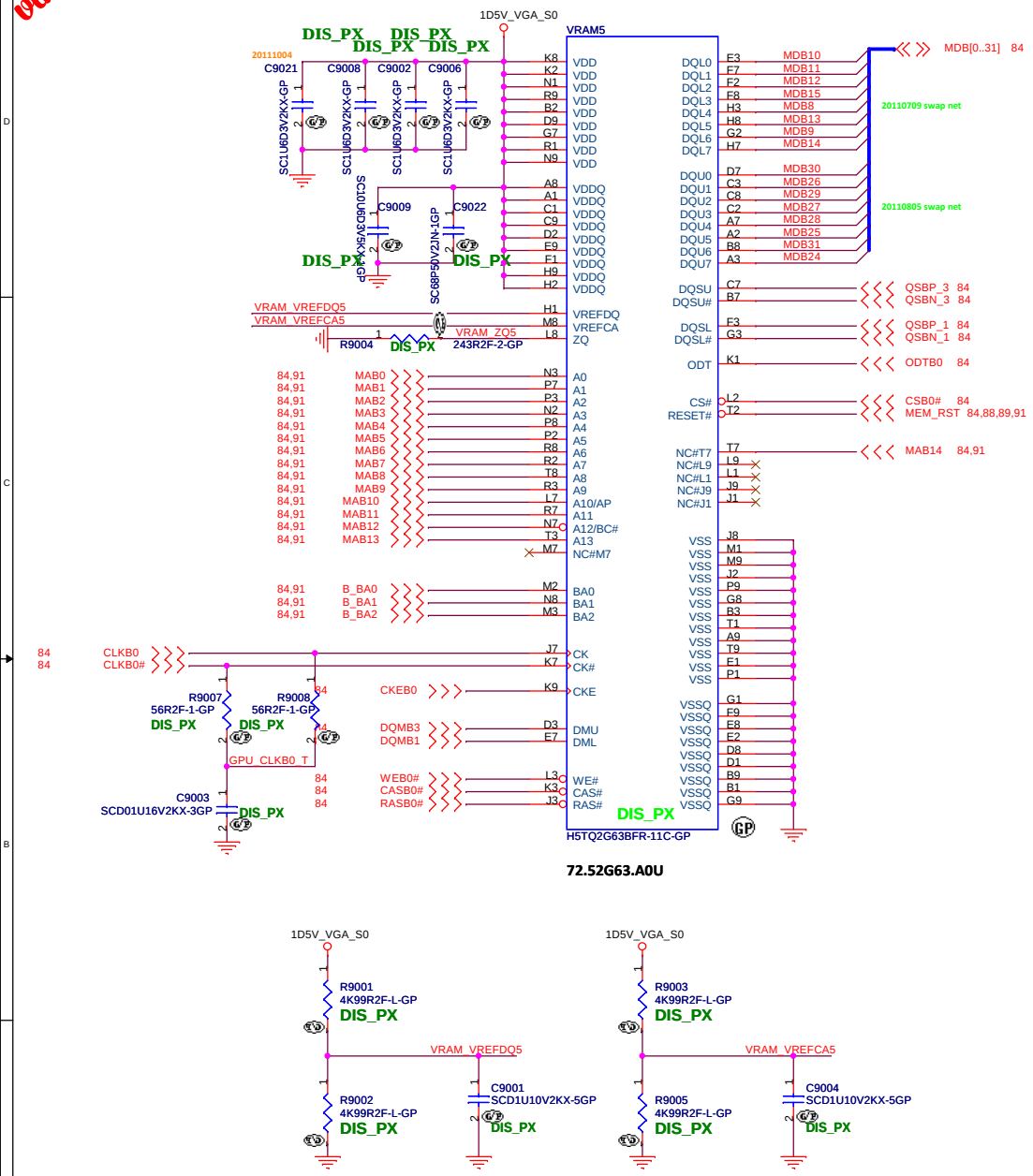

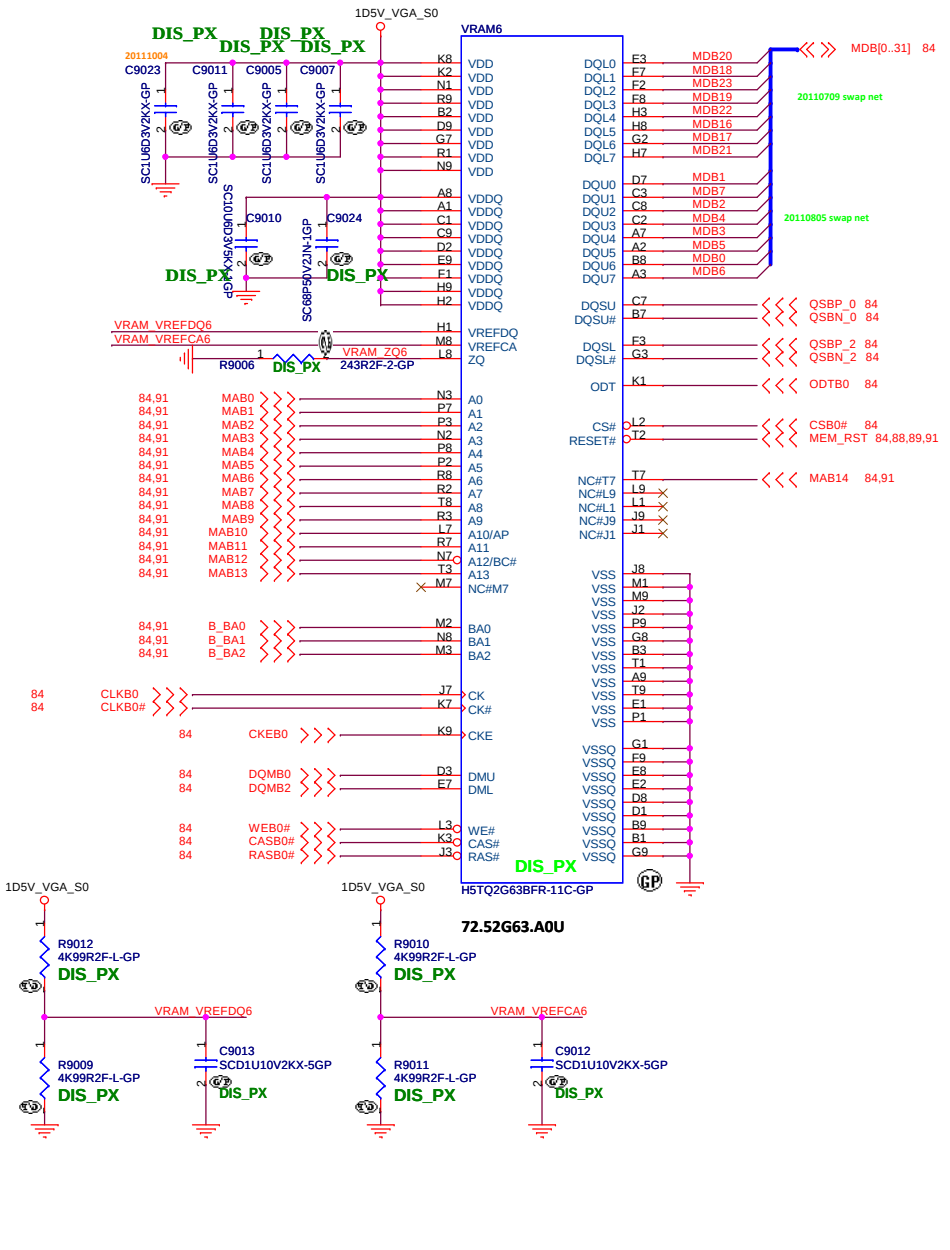

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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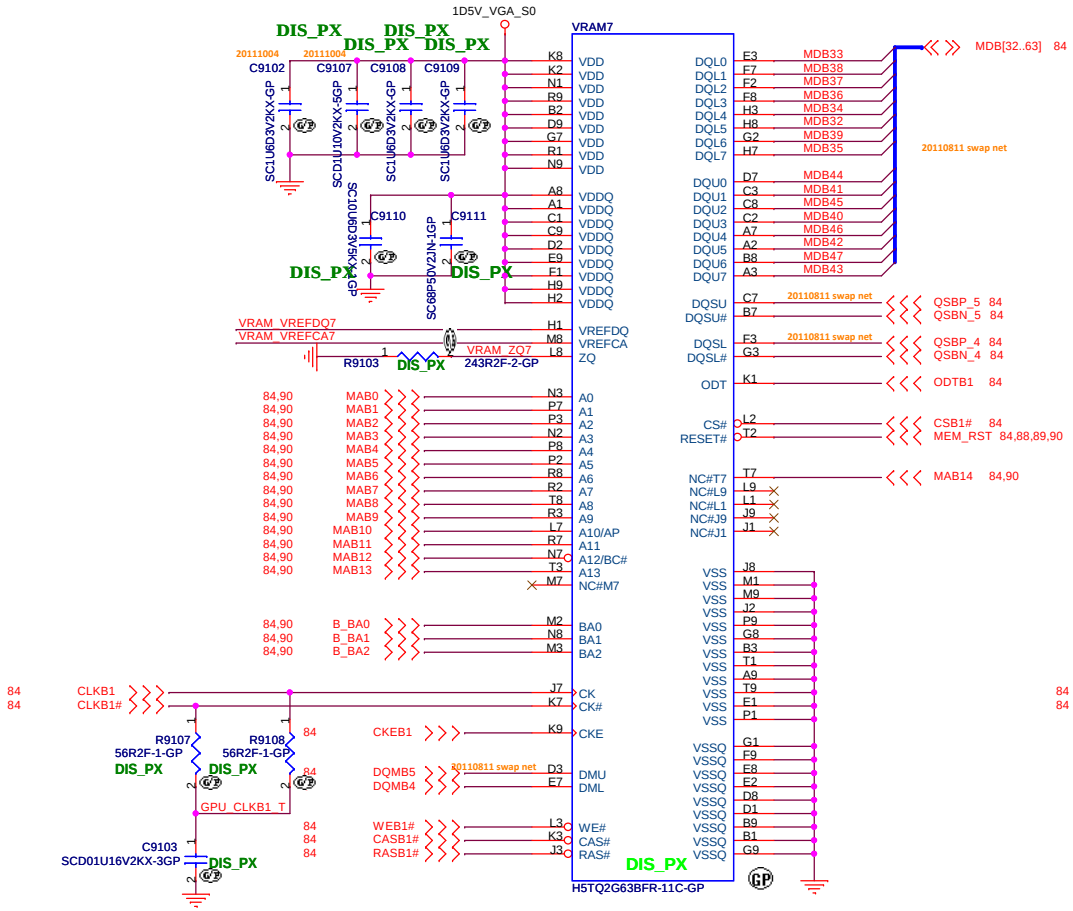

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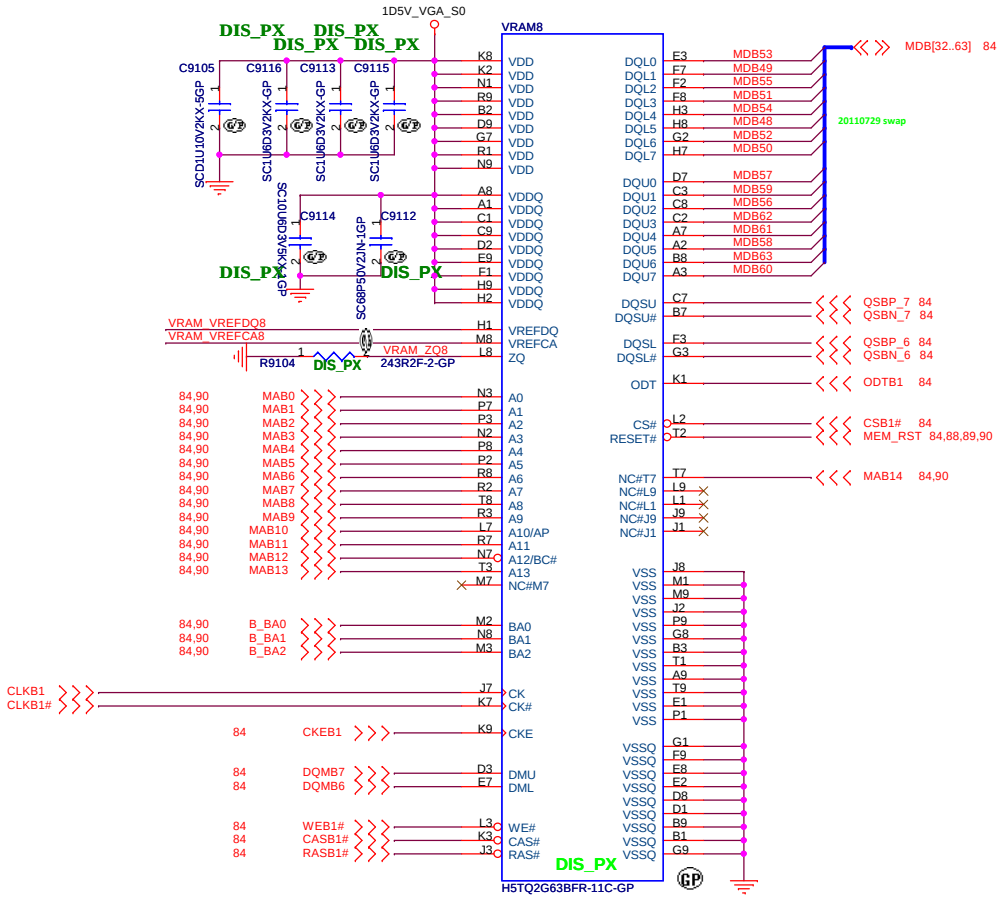

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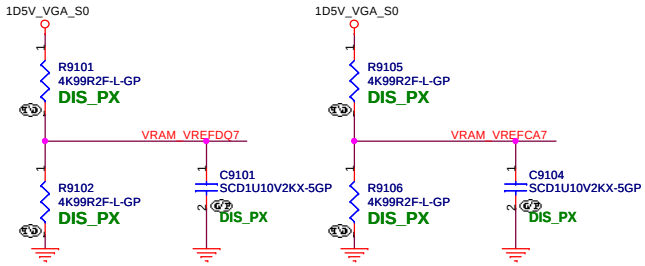

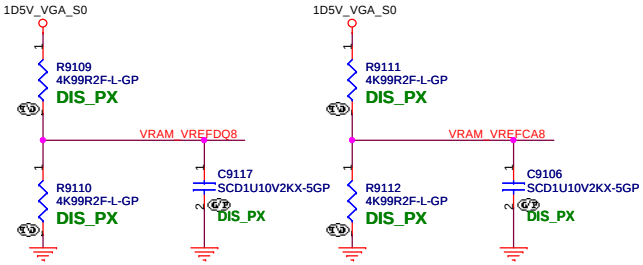

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	S series Popeye & Pebble	SA

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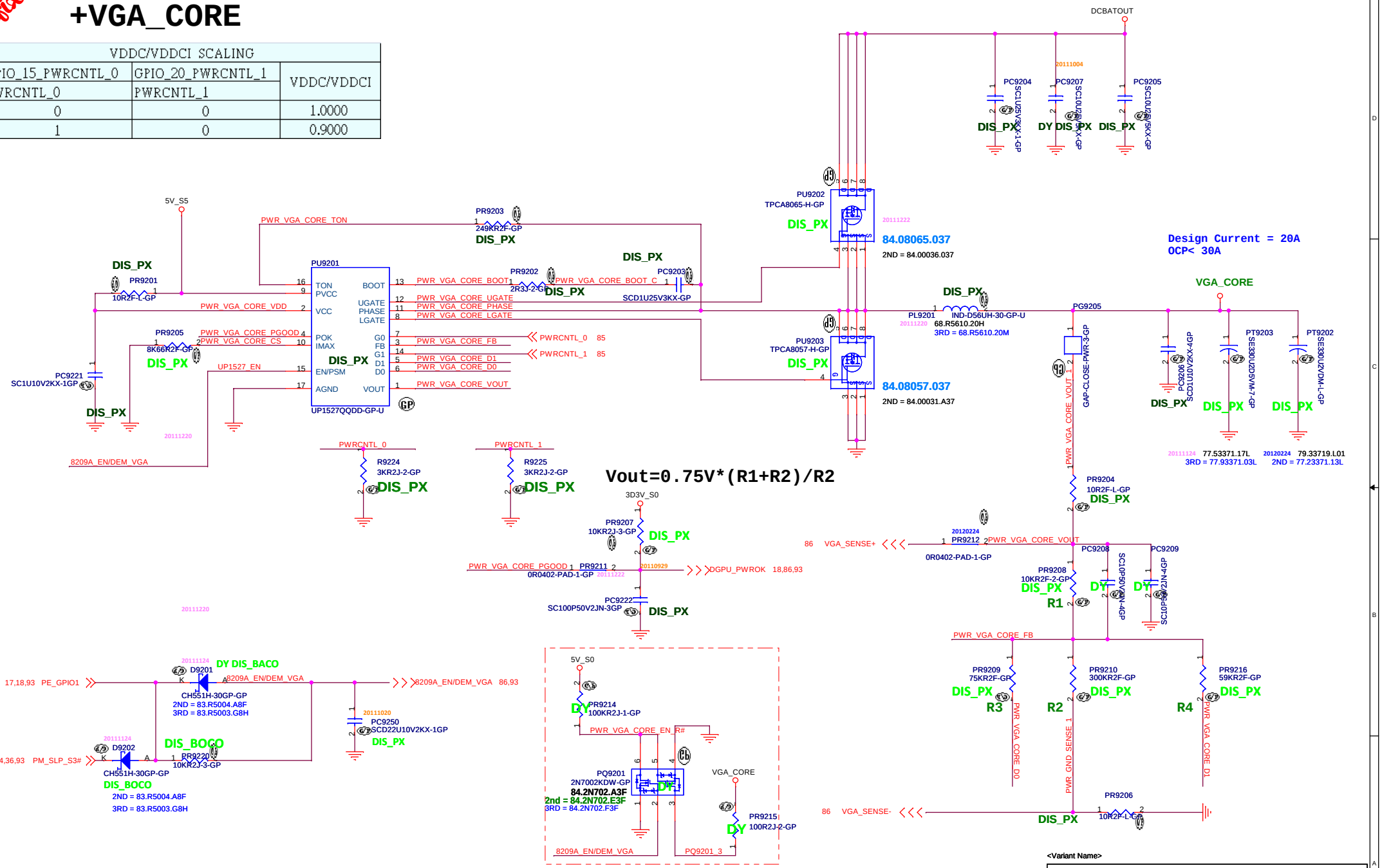
+VGA_CORE

VDDC/VDDCI SCALING		
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VDDC/VDDCI
PWRCNTL_0	PWRCNTL_1	
0	0	1.0000
1	0	0.9000



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	UP1527_VGACORE
Size A3 / Document Number	S series Popeye & Pebble / Rev SA
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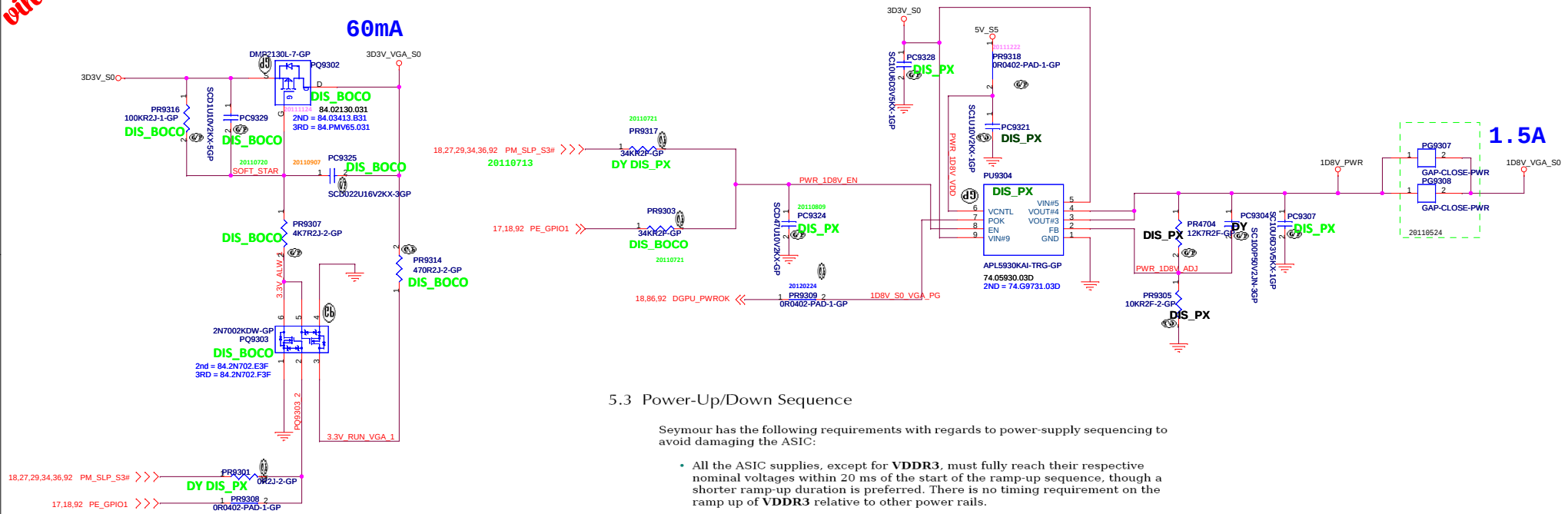
3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0

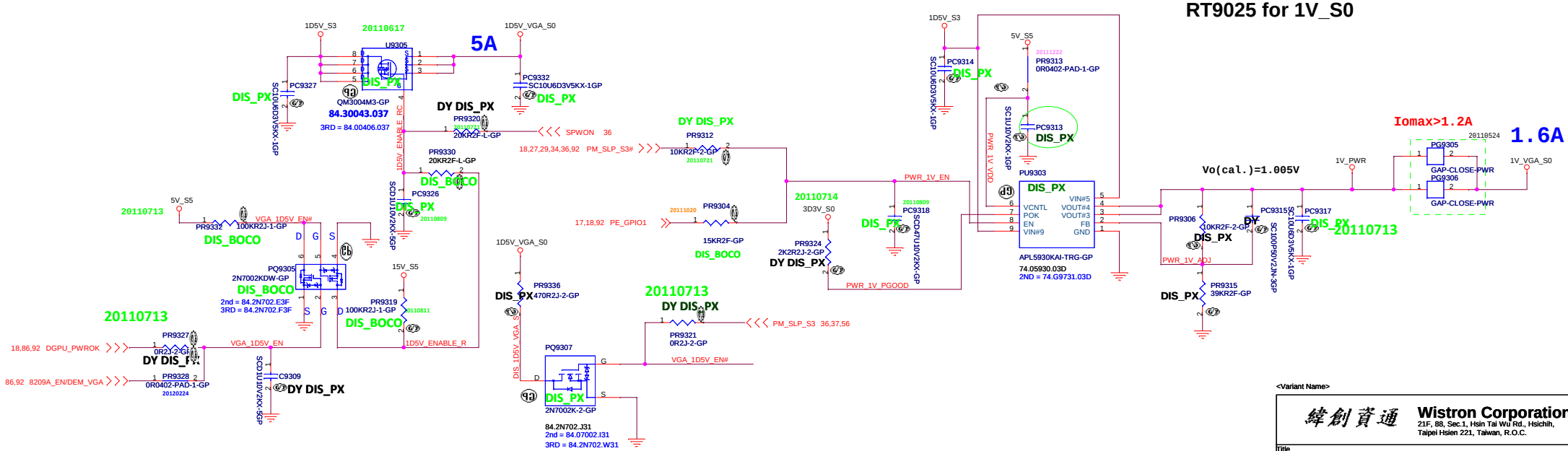


5.3 Power-Up/Down Sequence

Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for **VDDR3**, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of **VDDR3** relative to other power rails.
- The external pull-up resistors on the **DDC/AUX** signals (if applicable) should ramp up before or after both **VDDC** and **VDD_CT** have ramped up.
- **VDDC** and **VDD_CT** should not ramp up simultaneously. For exmaple, **VDDC** should reach 90% before **VDD_CT** starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

1D5V_VGA_S0



<Variant Name>

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Title: DISCRETE VGA POWER

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<Variant Name>

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Title: *Reserved*

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<Variant Name>

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Title: *Reserved*

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<Variant Name>

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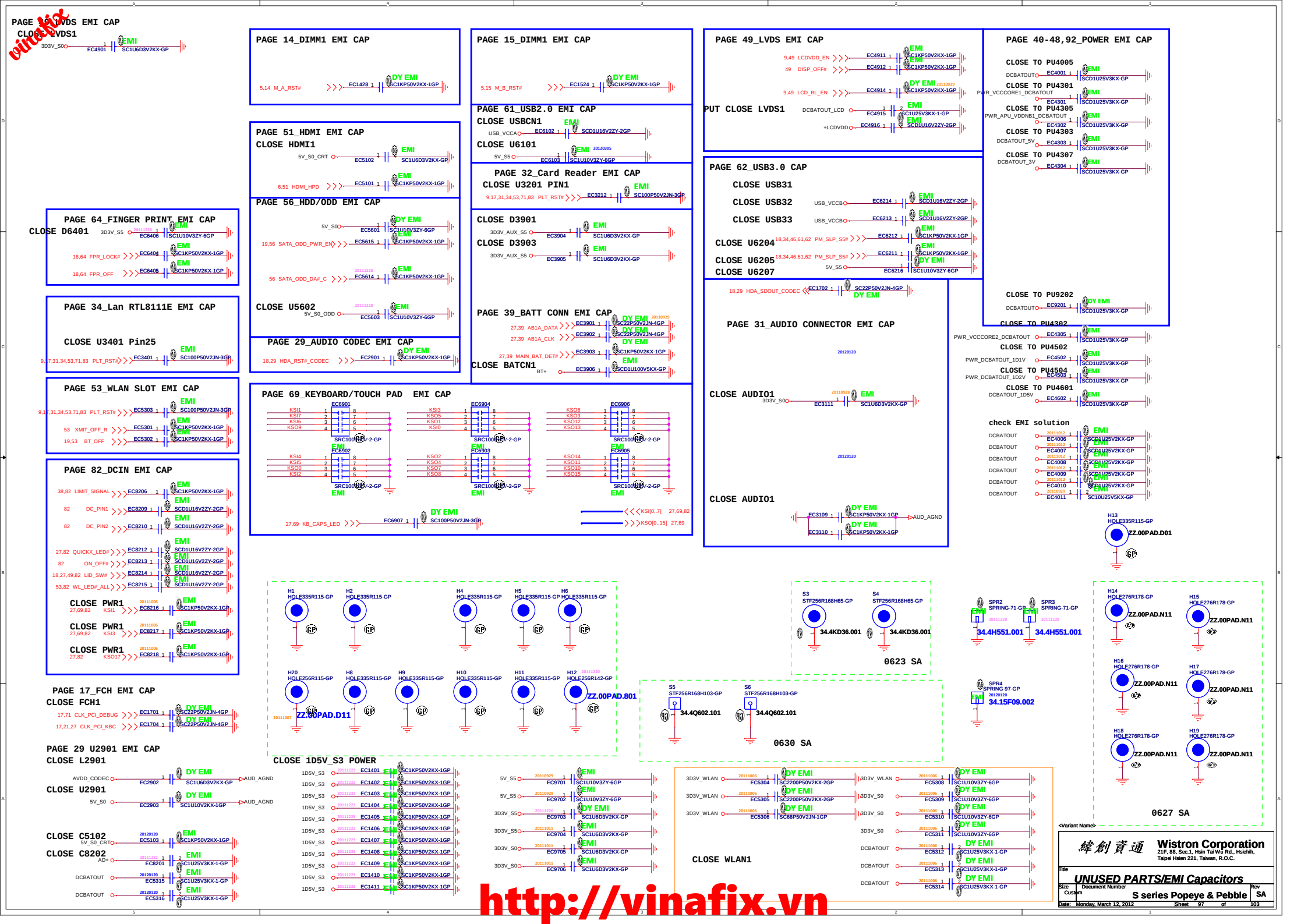
PAGE 50_LVDS EMI CAP
CLOSE LVDS1
PAGE 14_DIMM1 EMI CAP
PAGE 15_DIMM1 EMI CAP
PAGE 61_USB2.0 EMI CAP
CLOSE USBCN1
CLOSE U6101
PAGE 32_Card Reader EMI CAP
CLOSE U3201 PIN1
PAGE 51_HDMI EMI CAP
CLOSE HDMI1
PAGE 56_HDD/ODD EMI CAP
CLOSE U5602
PAGE 29_AUDIO CODEC EMI CAP
PAGE 64_FINGER PRINT EMI CAP
CLOSE D6401
PAGE 34_Lan RTL8111E EMI CAP
CLOSE U3401 Pin25
PAGE 53_WLAN SLOT EMI CAP
PAGE 82_DCIN EMI CAP
CLOSE PWR1
CLOSE PWR1
CLOSE PWR1
PAGE 17_FCH EMI CAP
CLOSE FCH1
PAGE 29 U2901 EMI CAP
CLOSE L2901
CLOSE U2901
CLOSE C5102
CLOSE C8202
PAGE 69_KEYBOARD/TOUCH PAD EMI CAP
CLOSE D3901
CLOSE D3903
PAGE 39_BATT CONN EMI CAP
CLOSE BATCN1
PAGE 49_LVDS EMI CAP
PUT CLOSE LVDS1
PAGE 62_USB3.0 CAP
CLOSE USB31
CLOSE USB32
CLOSE USB33
CLOSE U6204
CLOSE U6205
CLOSE U6207
PAGE 31_AUDIO CONNECTOR EMI CAP
CLOSE AUDIO1
CLOSE AUDIO1
PAGE 40-48,92_POWER EMI CAP
CLOSE TO PU4005
CLOSE TO PU4301
CLOSE TO PU4305
CLOSE TO PU4303
CLOSE TO PU4307
CLOSE TO PU9202
CLOSE TO PU4302
CLOSE TO PU4502
CLOSE TO PU4504
CLOSE TO PU4601
check EMI solution
0623 SA
0630 SA
0627 SA
CLOSE 1D5V_S3 POWER
CLOSE WLAN1
H1 HOLE335R115-GP
H2 HOLE335R115-GP
H4 HOLE335R115-GP
H5 HOLE335R115-GP
H6 HOLE335R115-GP
H20 HOLE256R115-GP
H8 HOLE335R115-GP
H9 HOLE335R115-GP
H10 HOLE335R115-GP
H11 HOLE335R115-GP
H12 HOLE256R142-GP
ZZ.00PAD.D11
ZZ.00PAD.801
H13 HOLE335R115-GP
ZZ.00PAD.D01
H14 HOLE276R178-GP
H15 HOLE276R178-GP
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H17 HOLE276R178-GP
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H19 HOLE276R178-GP
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S3 STF256R168H65-GP
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S5 STF256R168H103-GP
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SPR2 SPRING-71-GP
SPR3 SPRING-71-GP
34.4H551.001
SPR4 SPRING-97-GP
34.15F09.002
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http://vinafix.vn

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AMD Power Sequence

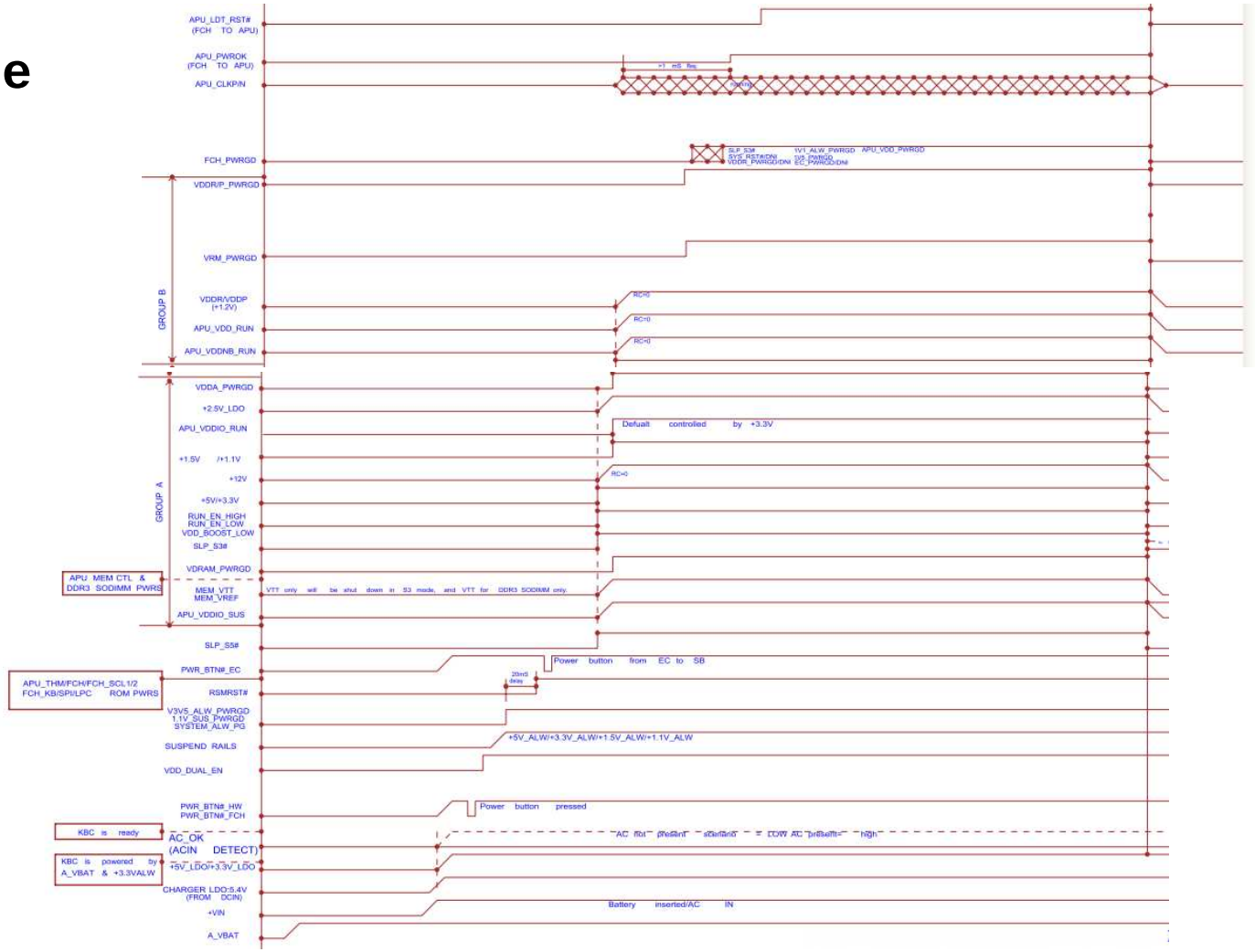
Power on Sequence required:

HUDSON-M3:

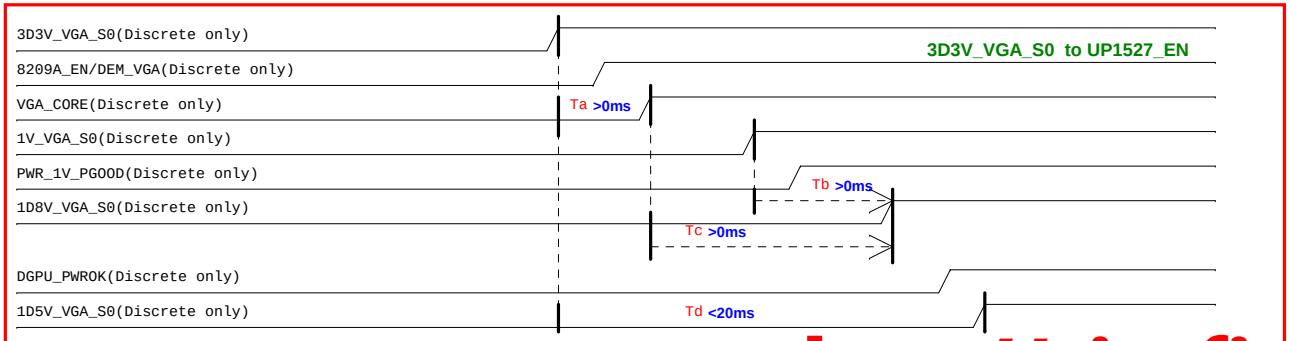
1, +3.3V_ALW ramp before +1.1V_ALW
2, +3.3V_RUN ramp before +1.1V_RUN
3, +3.3V_LDO/ALW_R ramping down time > 300us
4, 50uS <= All power rails except +3.3V_LDO/ALW_R <= 40mS
5, 100uS <= +3.3V_LDO/ALW_R <= 40mS

APU:

1, GROUP A(VDDIO,VDDA) ramp before GROUP B (VDD_RUN, VDDNB_RUN, VDDP, VDDR)



THAMES-M2 XT Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

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Title: Power Sequence

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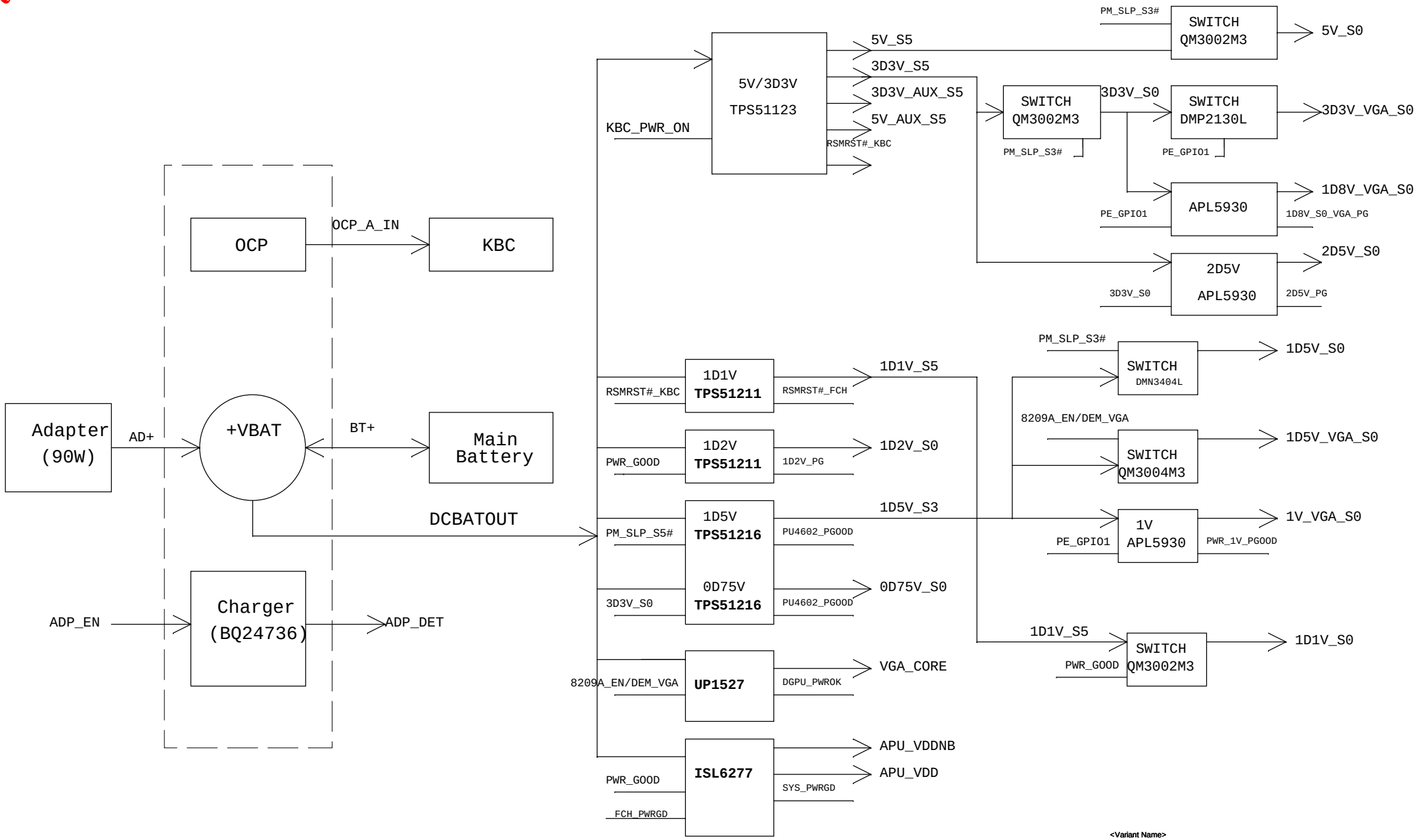

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Title: ***Power Block Diagram***

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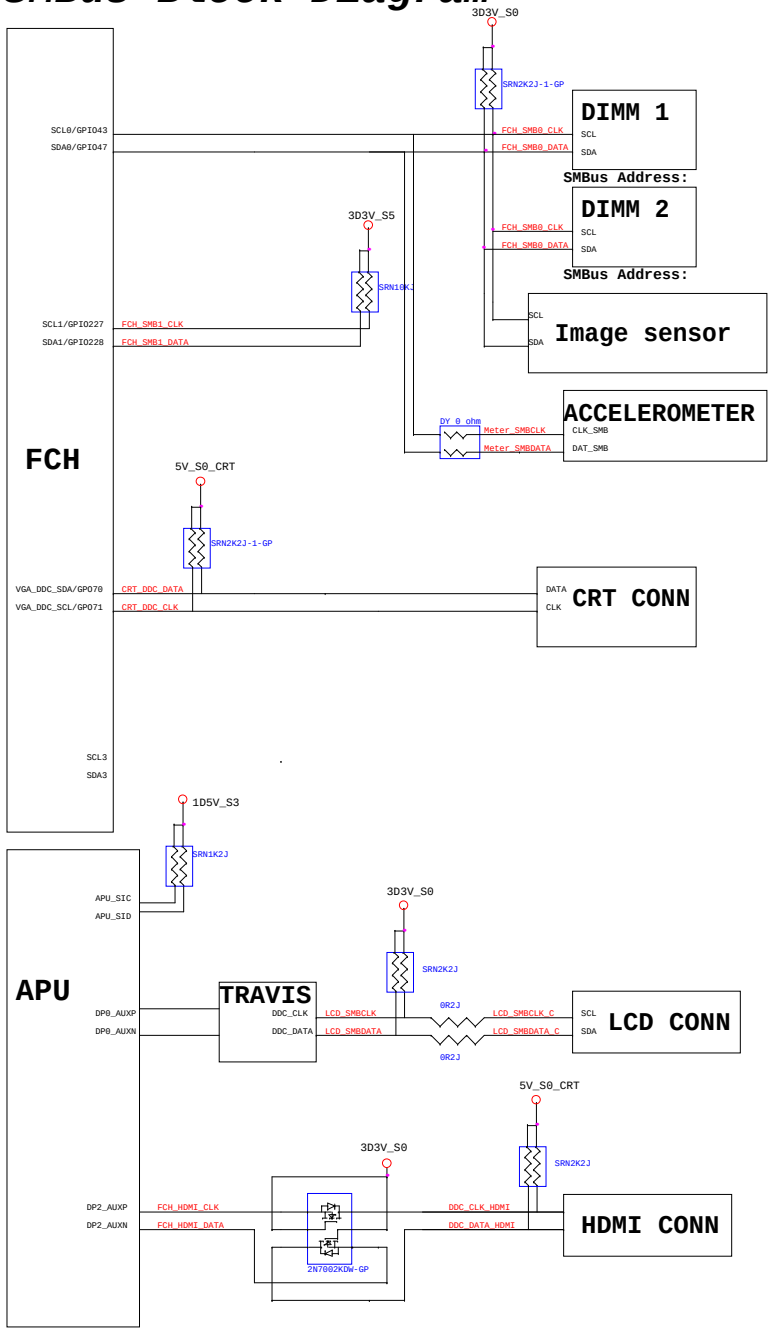
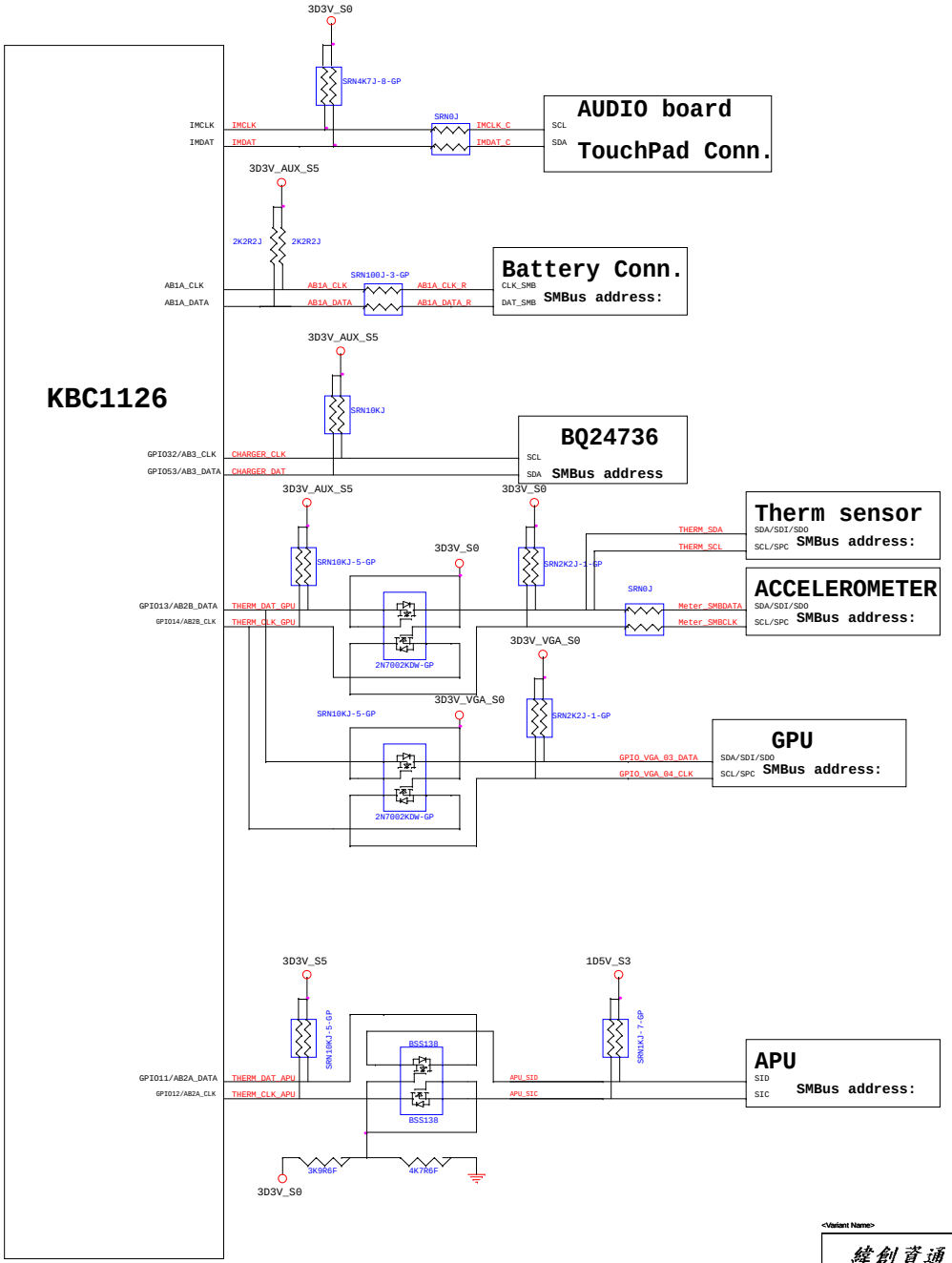
FCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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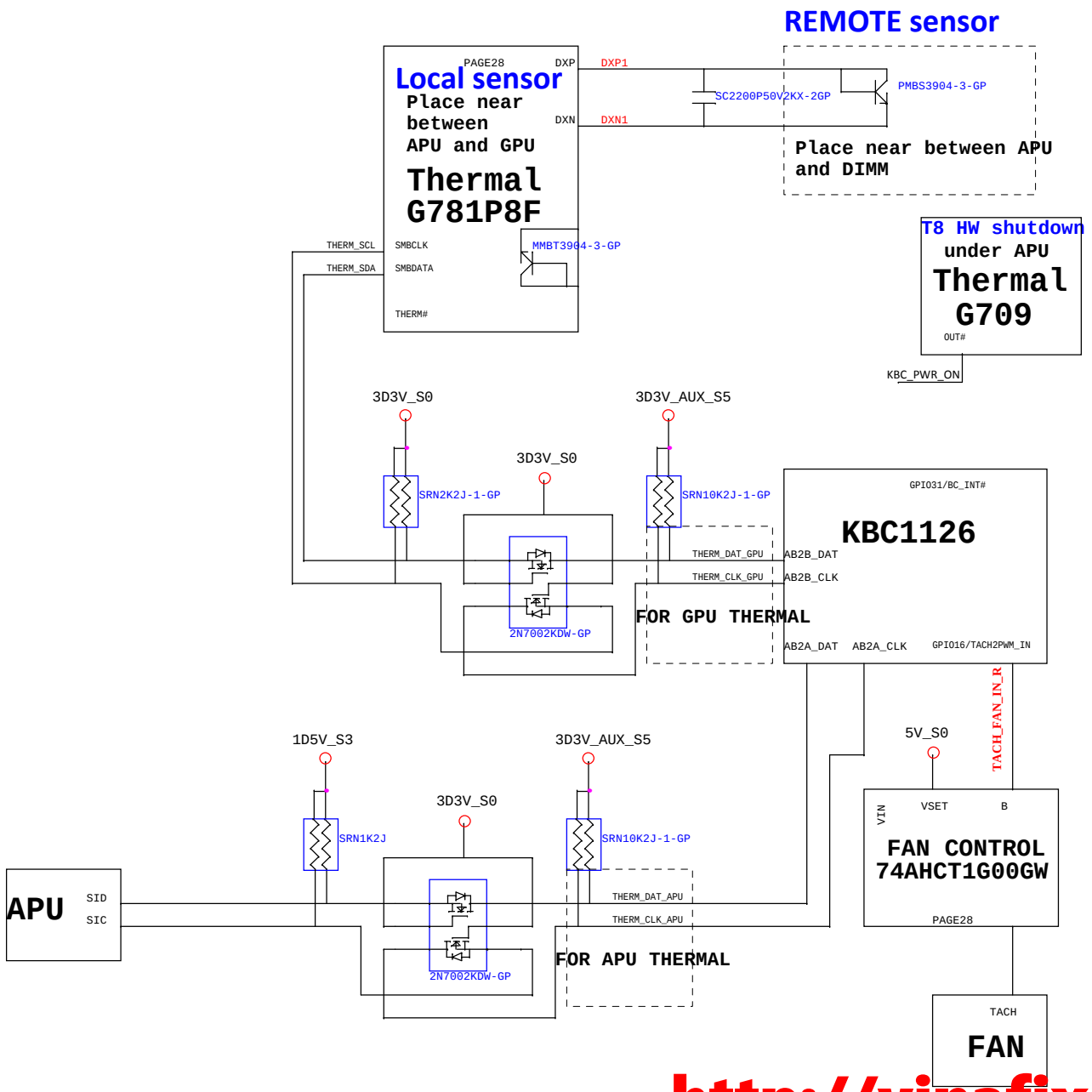
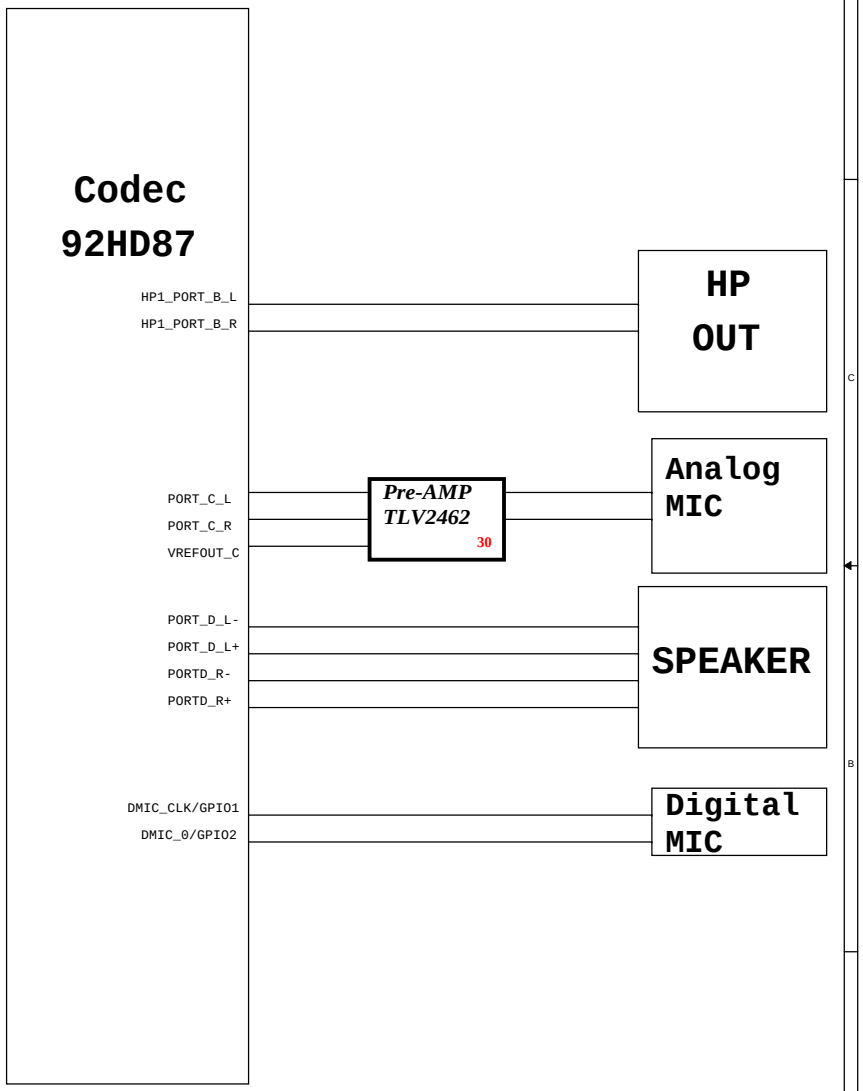
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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