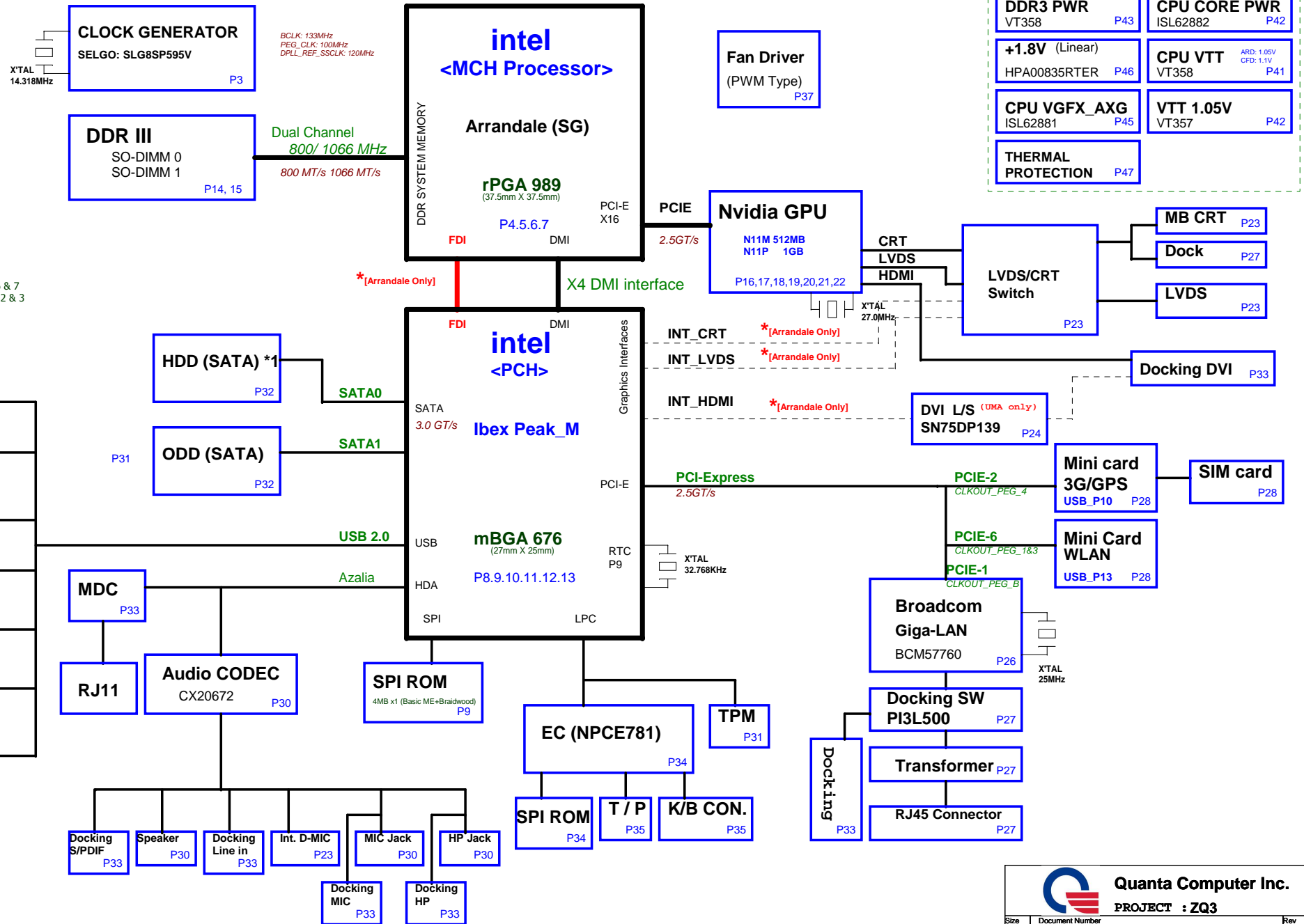
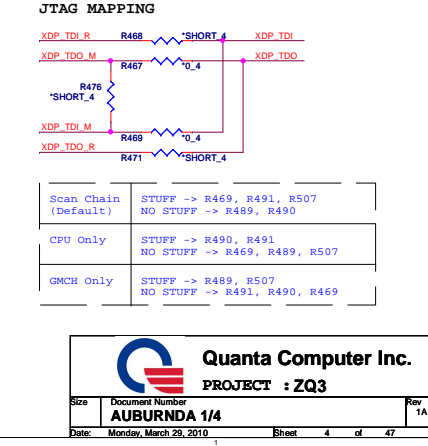
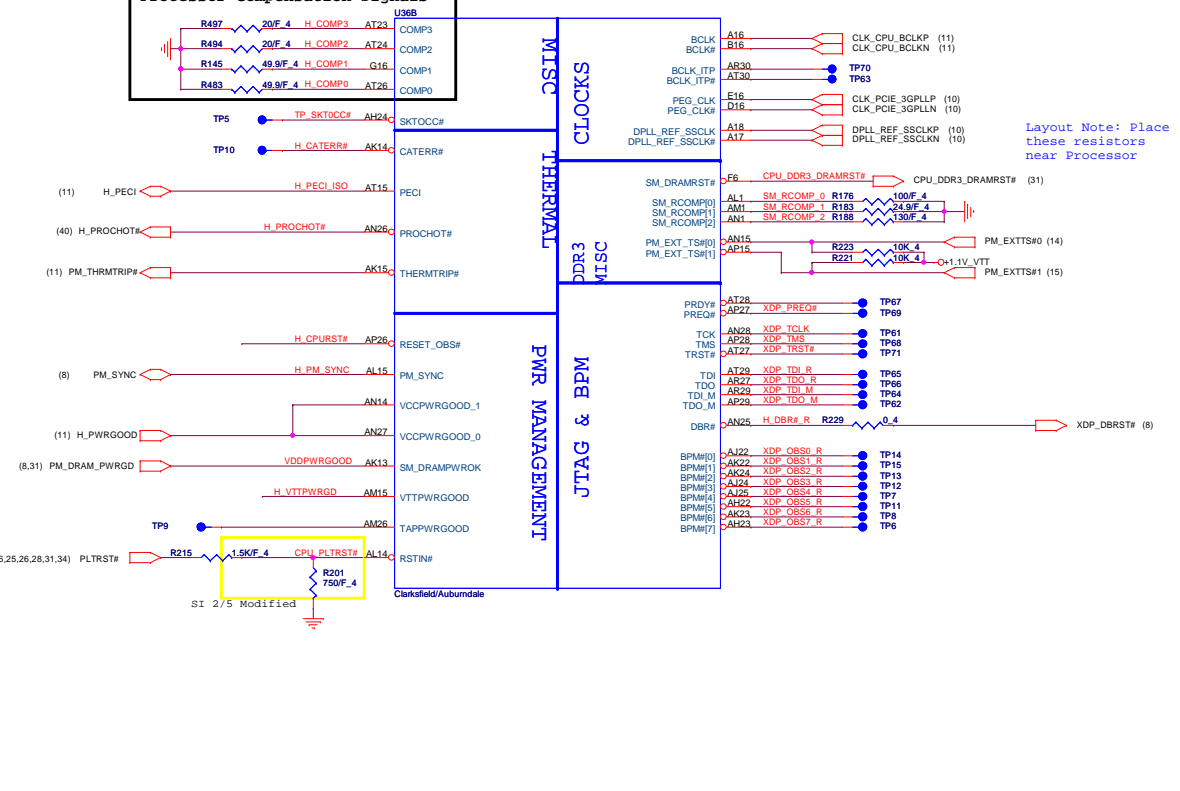
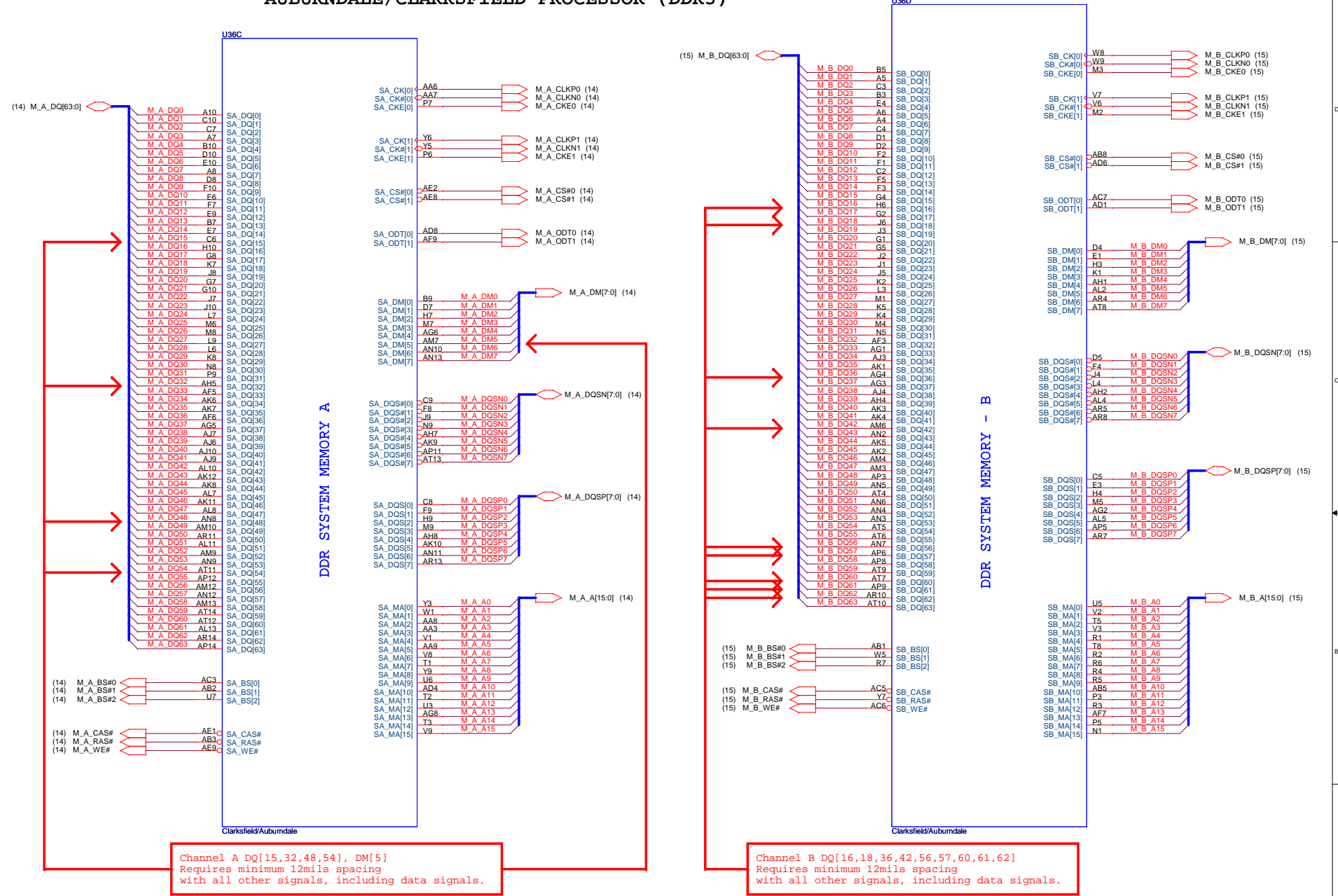


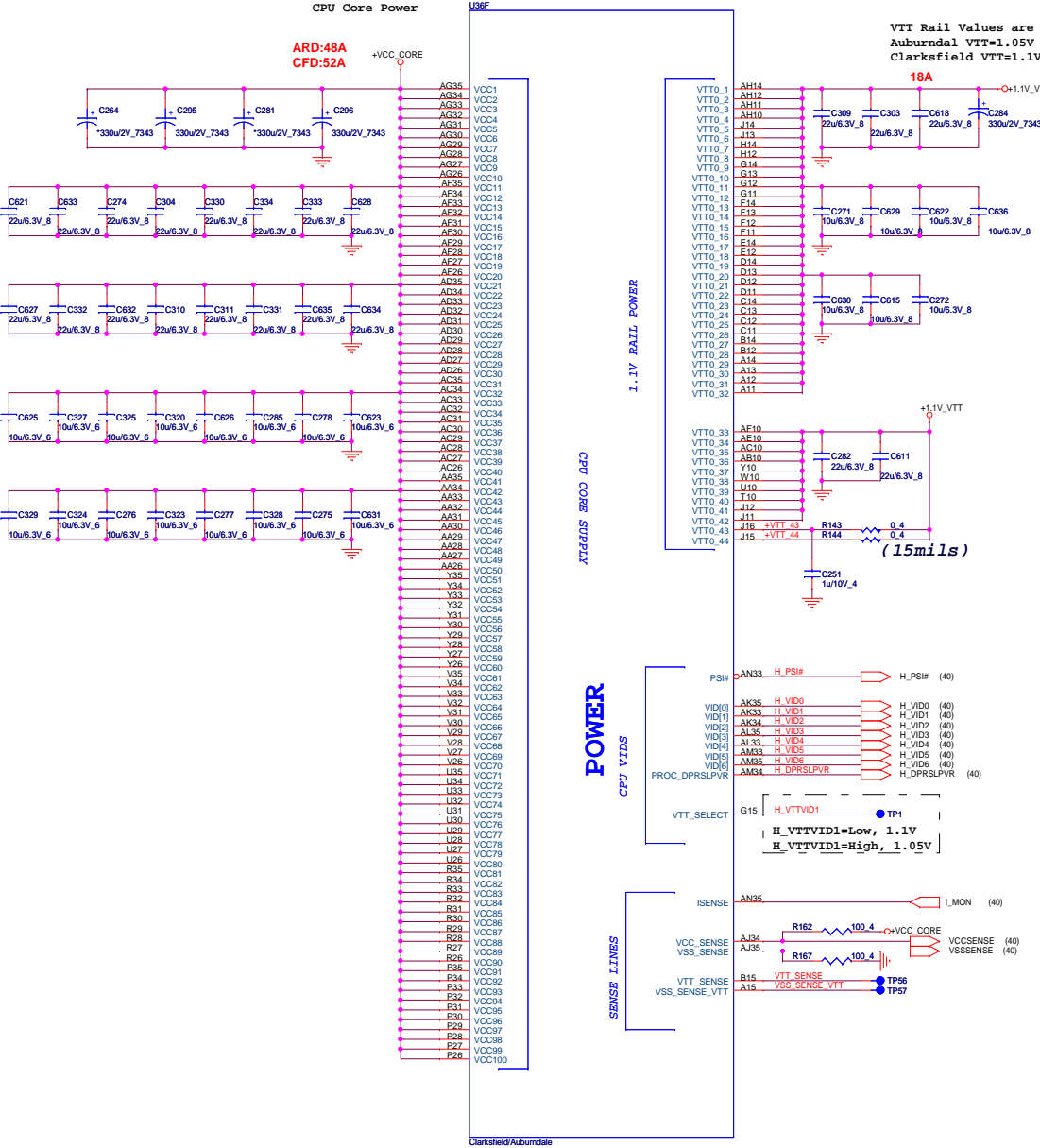
Calpella Switchable Graphic BLOCK DIAGRAM



Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

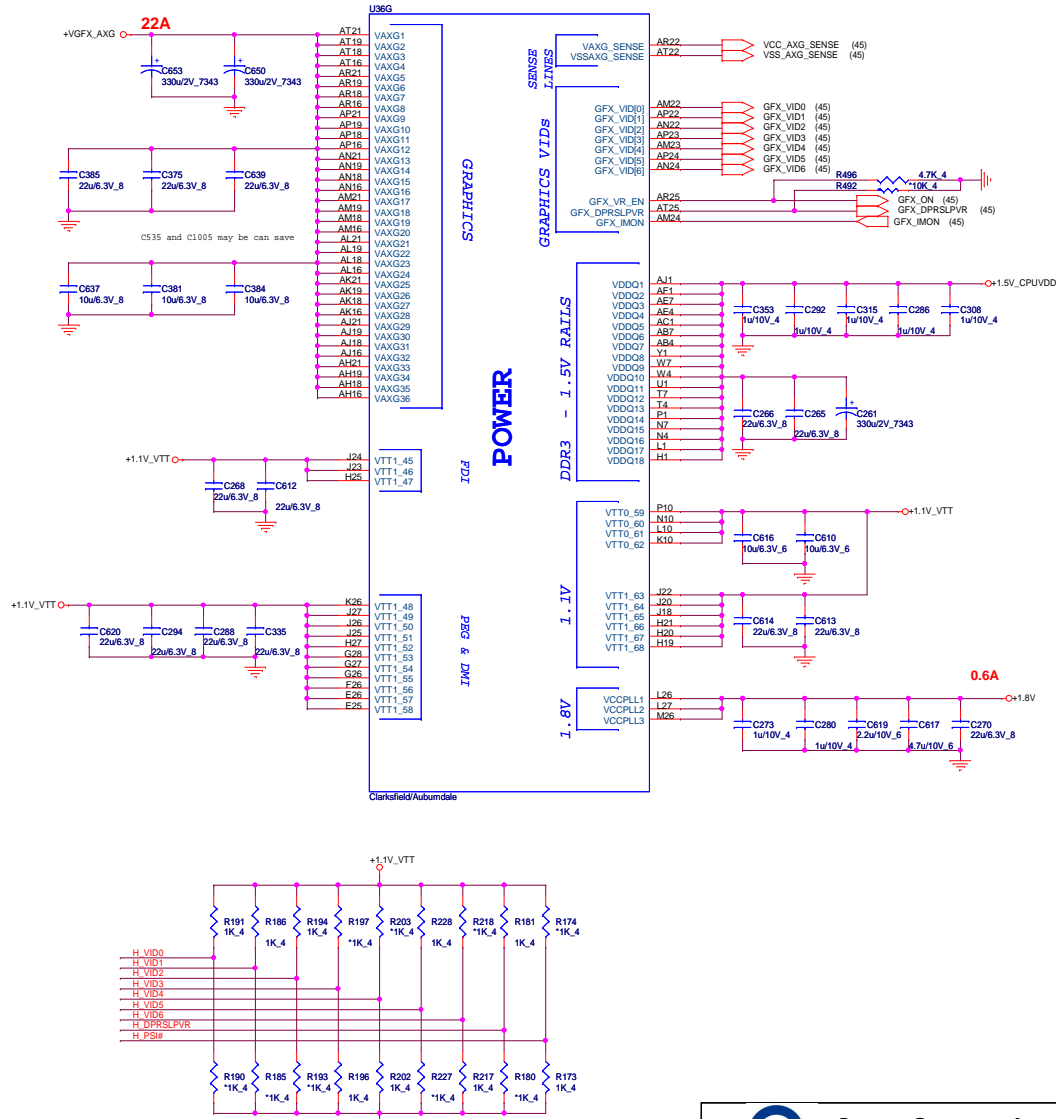






AUBURNDAL/CLARKSFIELD PROCESSOR (POWER)

AUBURNDAL/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

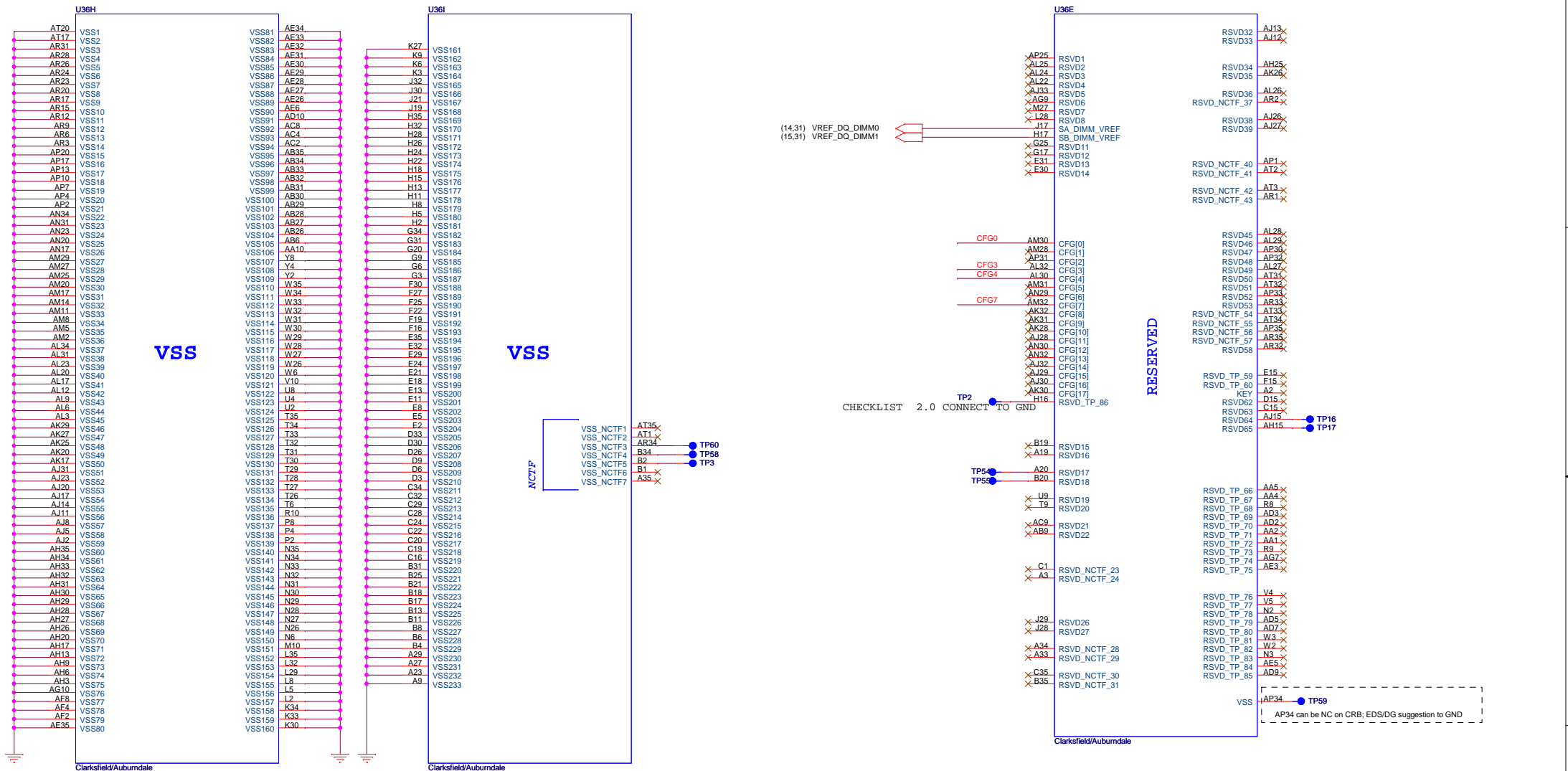


H_VID0 : Max 1.4V
LFM_VID : Min 0.65V

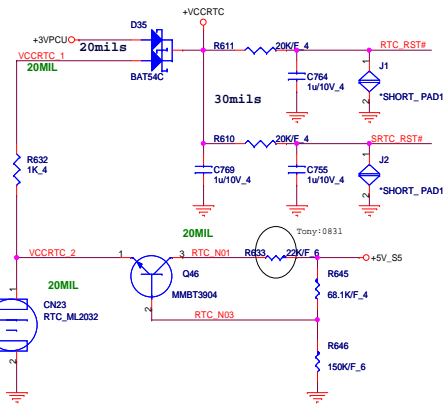
Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

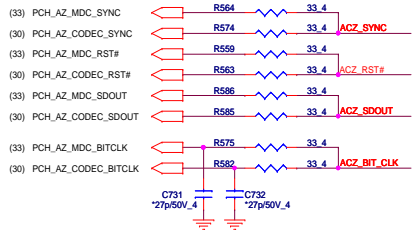
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



RTC Circuitry(RTC)

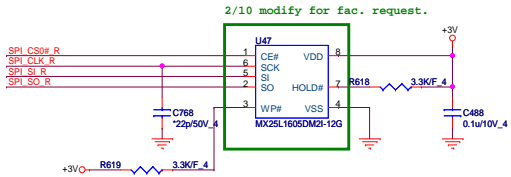


HDA Bus(CLG)



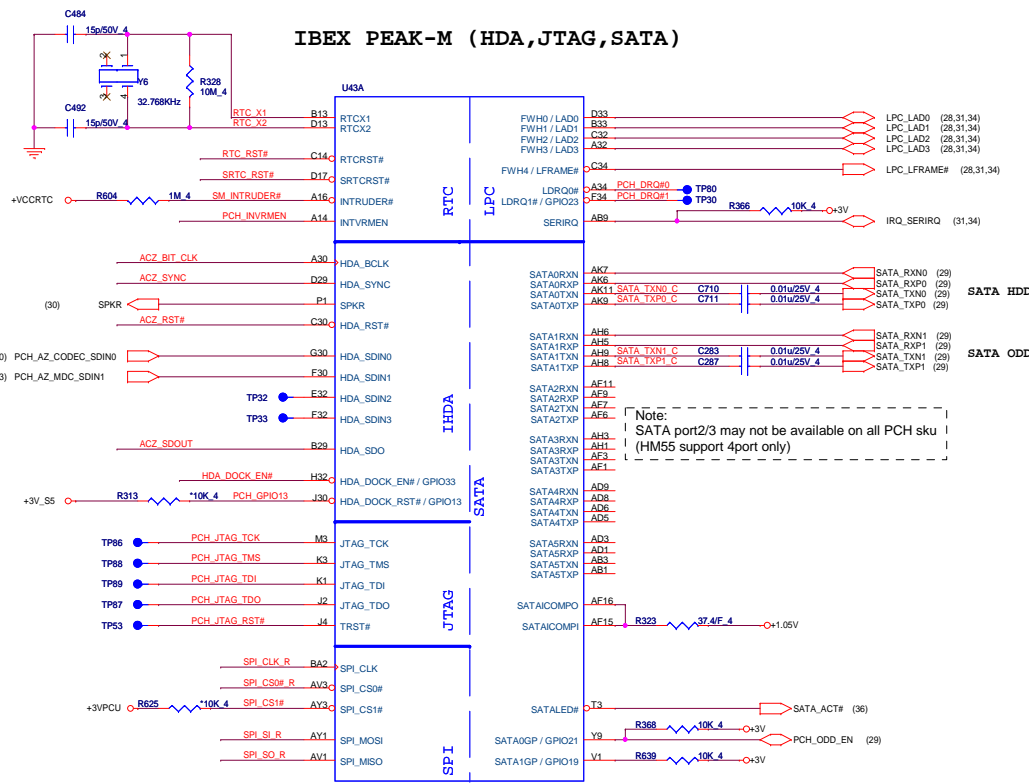
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)




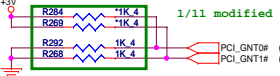





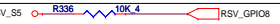




PCH2(CLG)

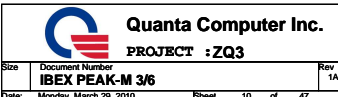
HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.5V (default)
external pull-up
VCCVRM=>+1.5V



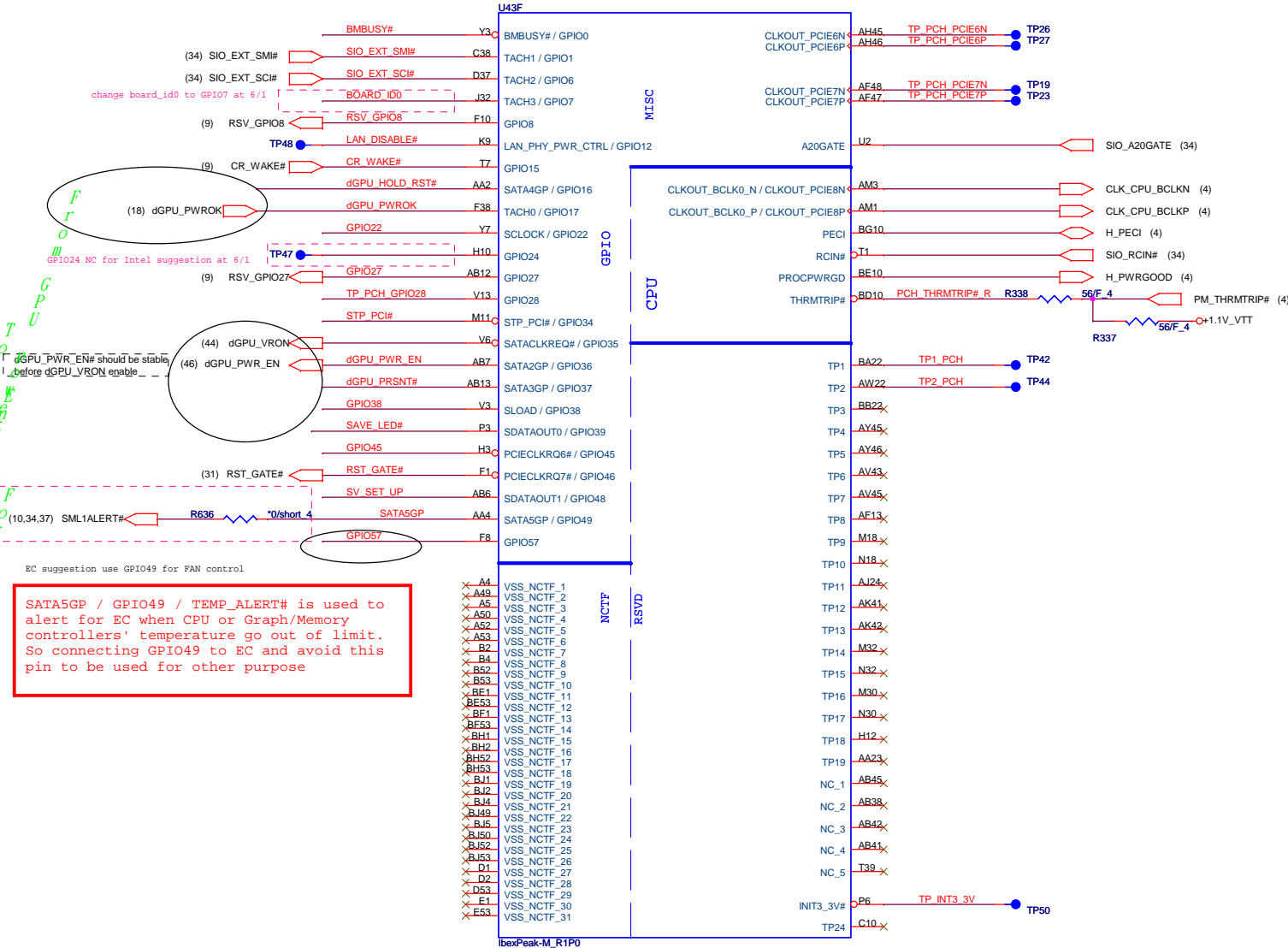
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V 												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)													
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC 												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p> 
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)													
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V 												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V 												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)													
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V 												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 												

IBEX PEAK-M (PCI-E,SMBUS,CLK)

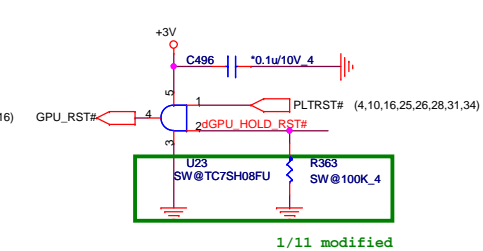


PCH4 (CLG)

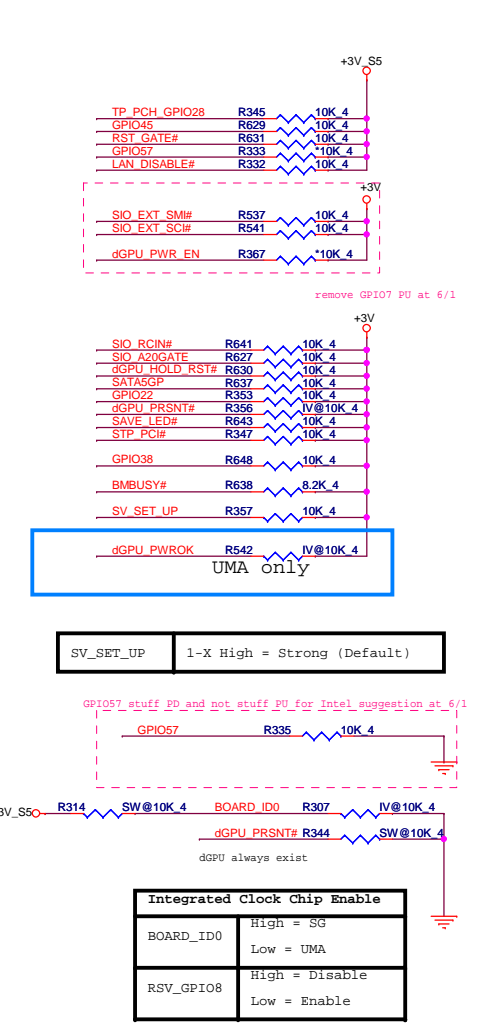


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#(CLG)

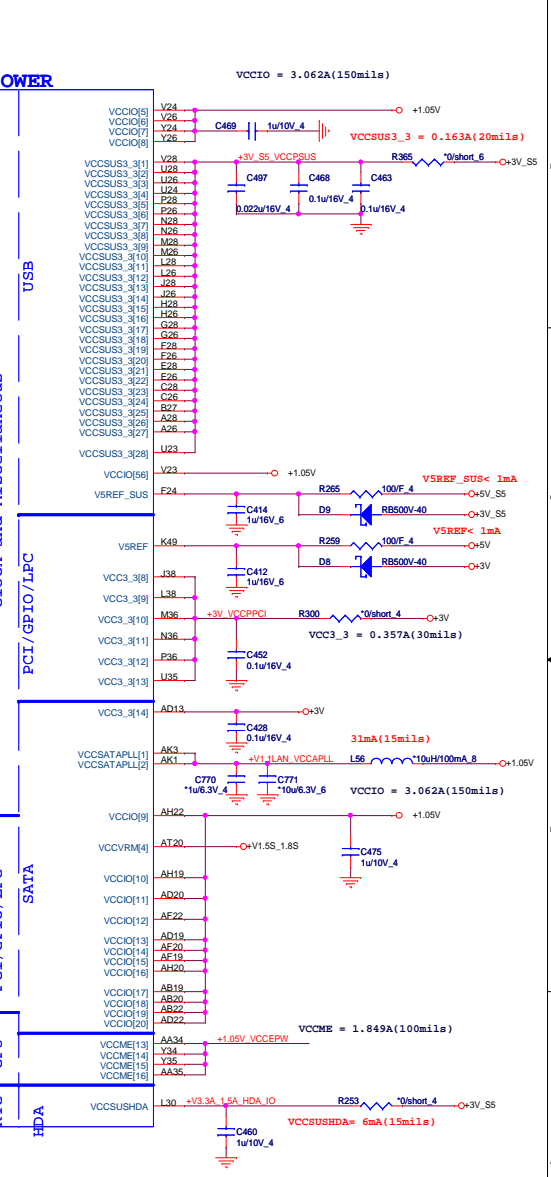
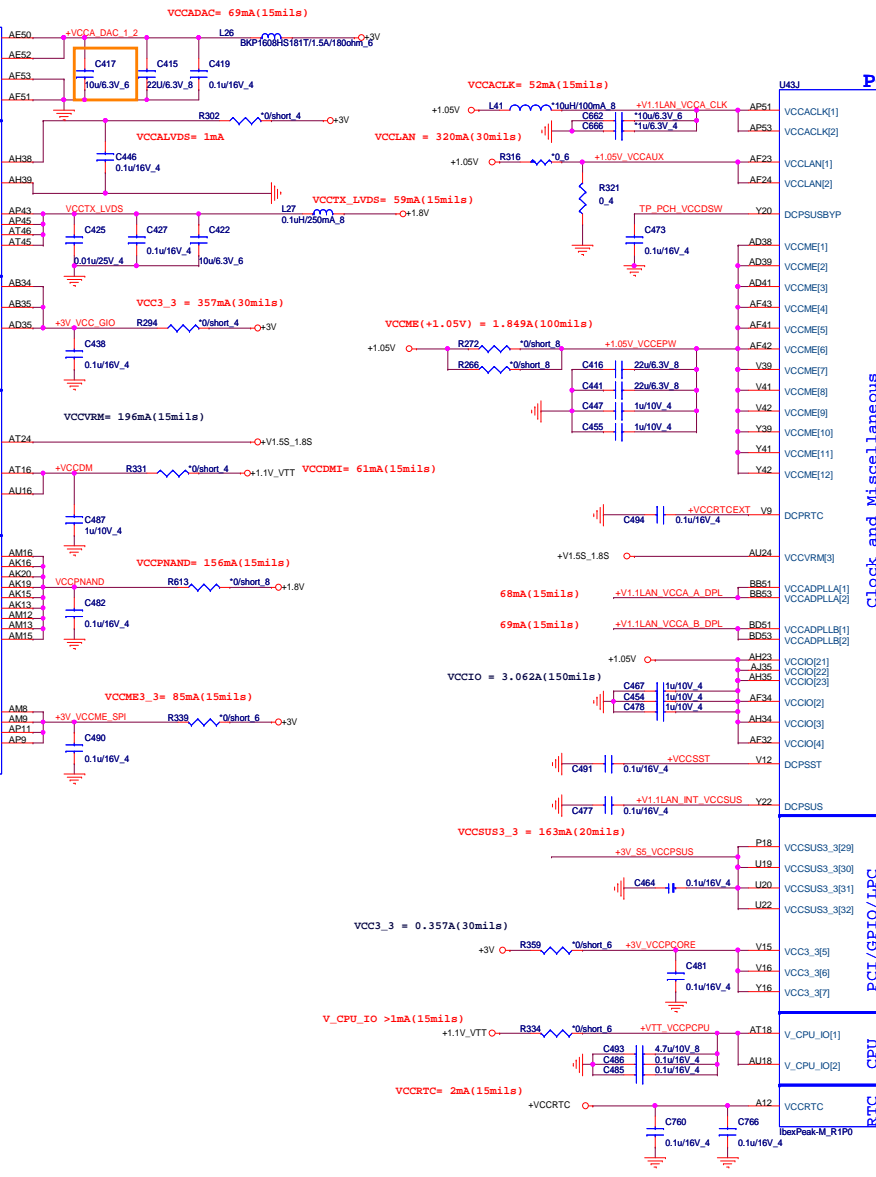
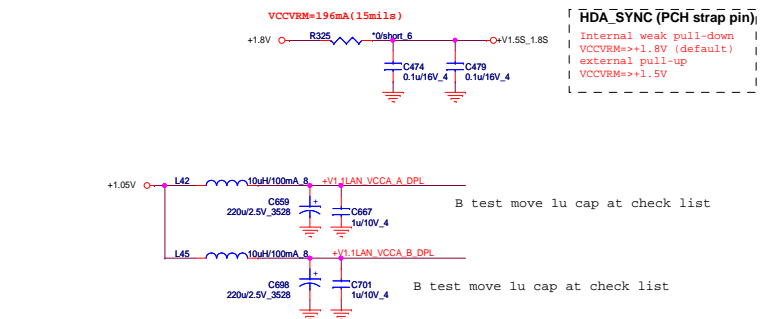


GPIO Pull-up/Pull-down(CLG)

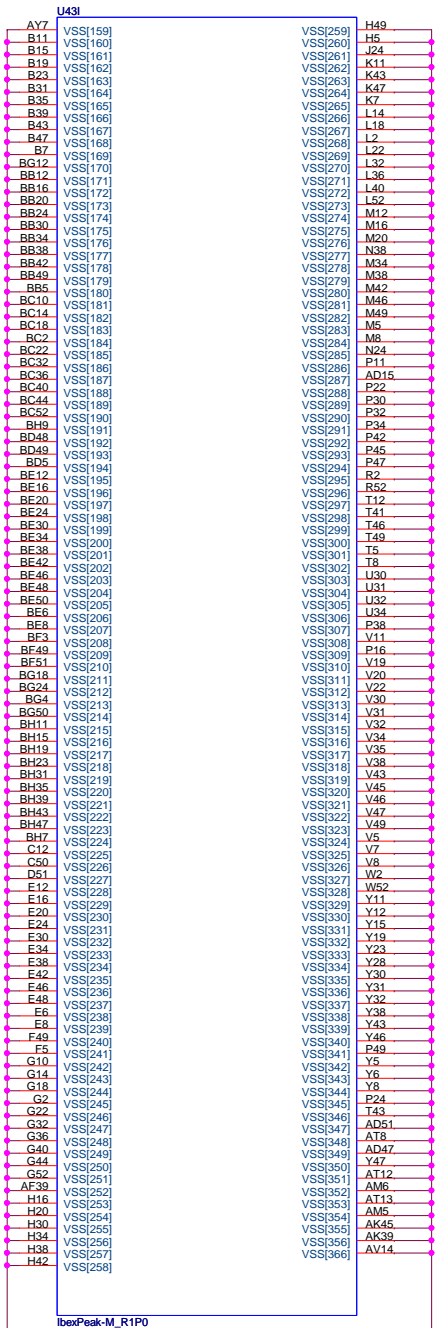
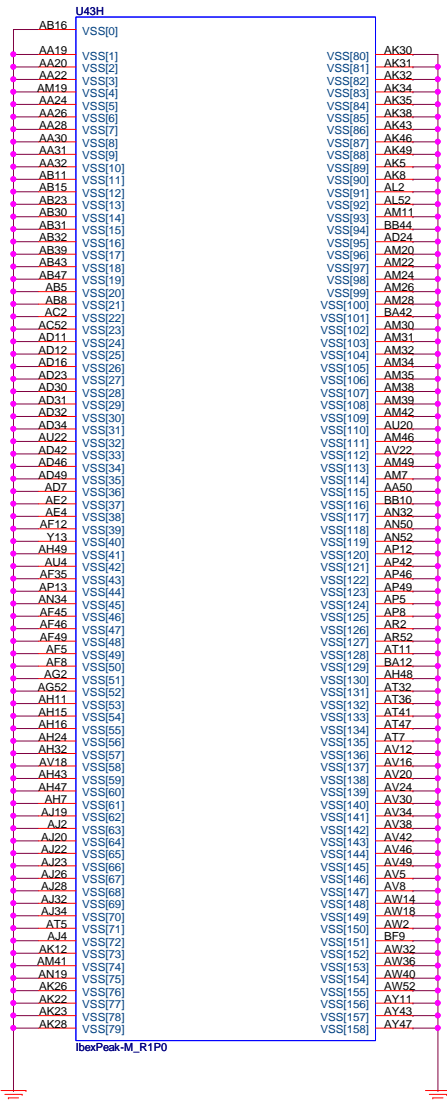


Integrated Clock Chip Enable	
BOARD_ID0	High = SG Low = UMA
RSV_GPIO8	High = Disable Low = Enable

IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)

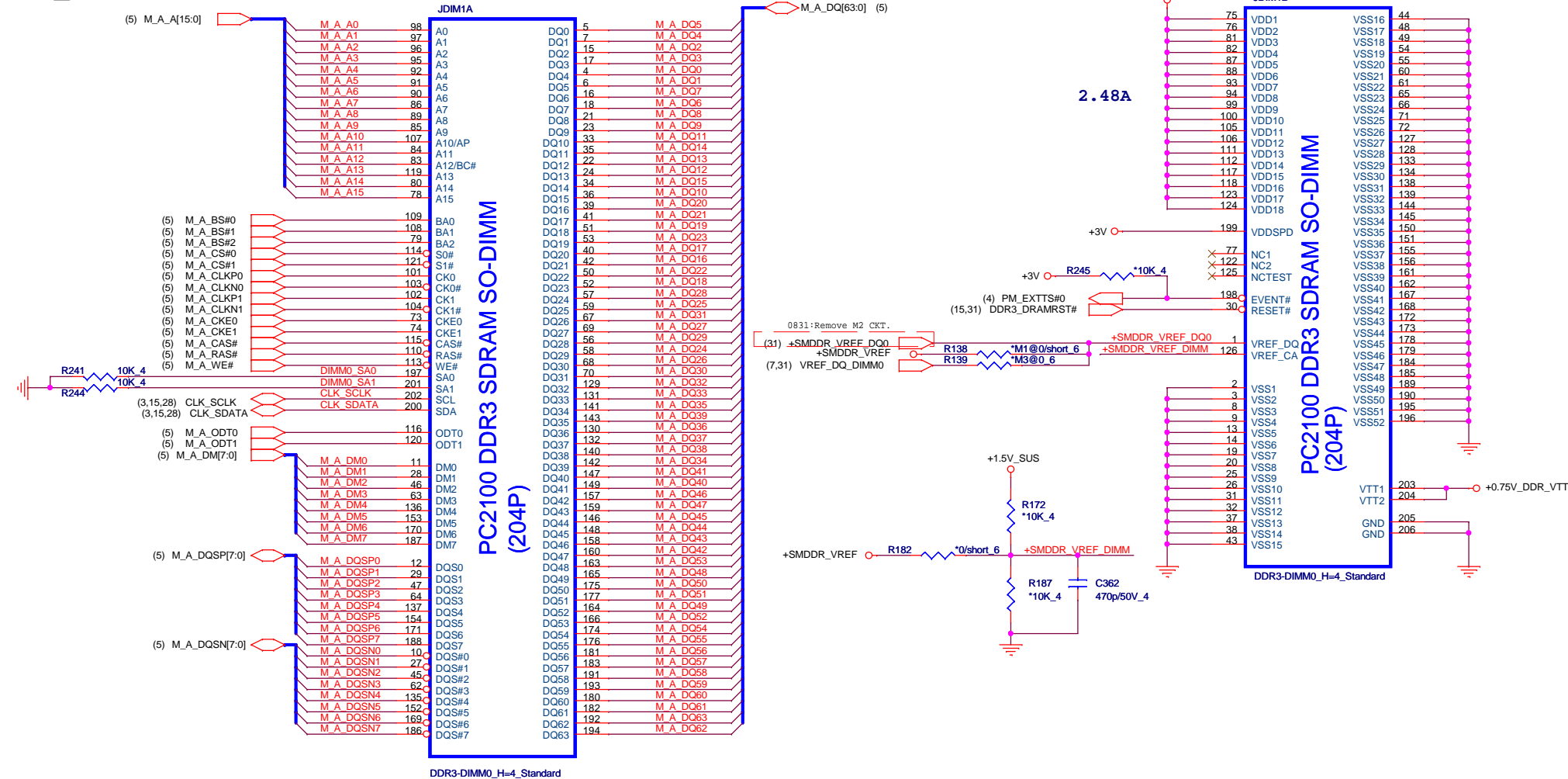


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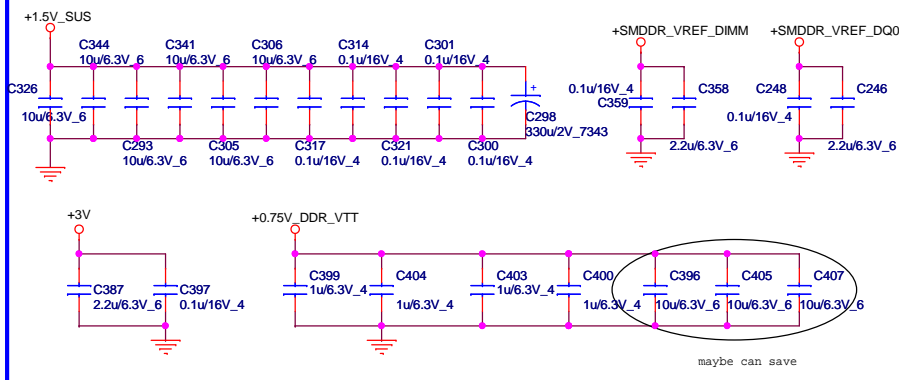
PROJECT :ZQ3

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date:	Monday, March 29, 2010	Sheet 13 of 47

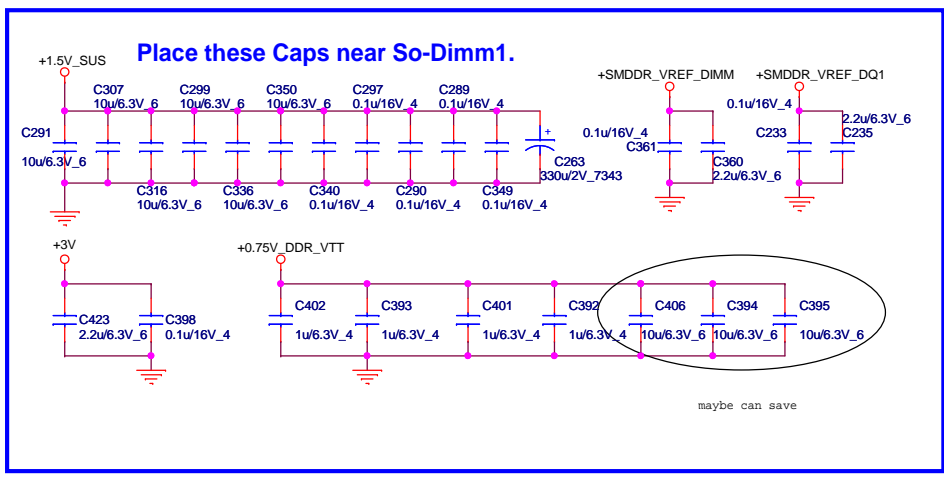
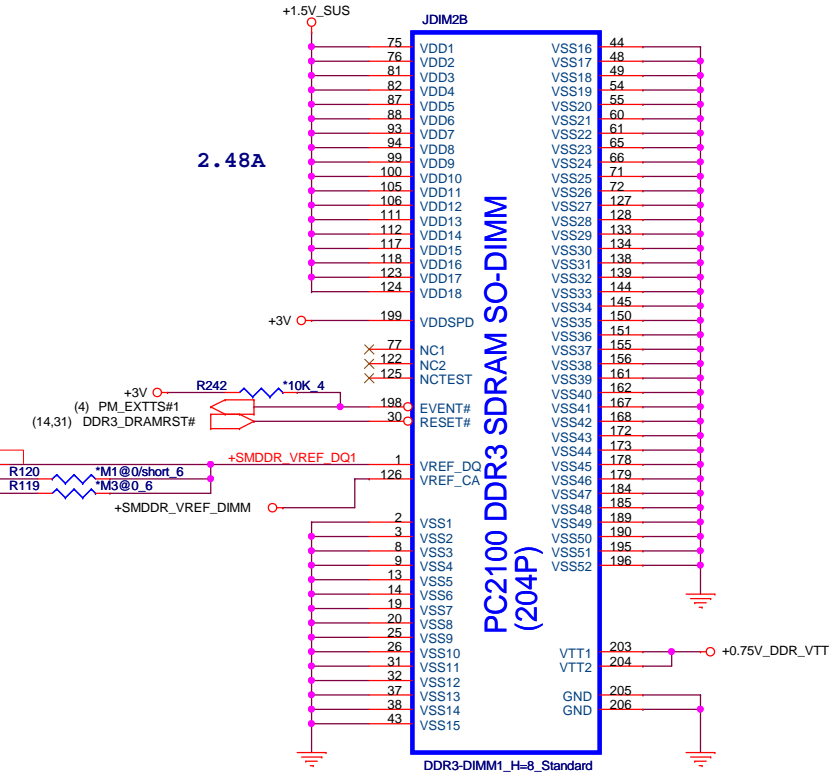
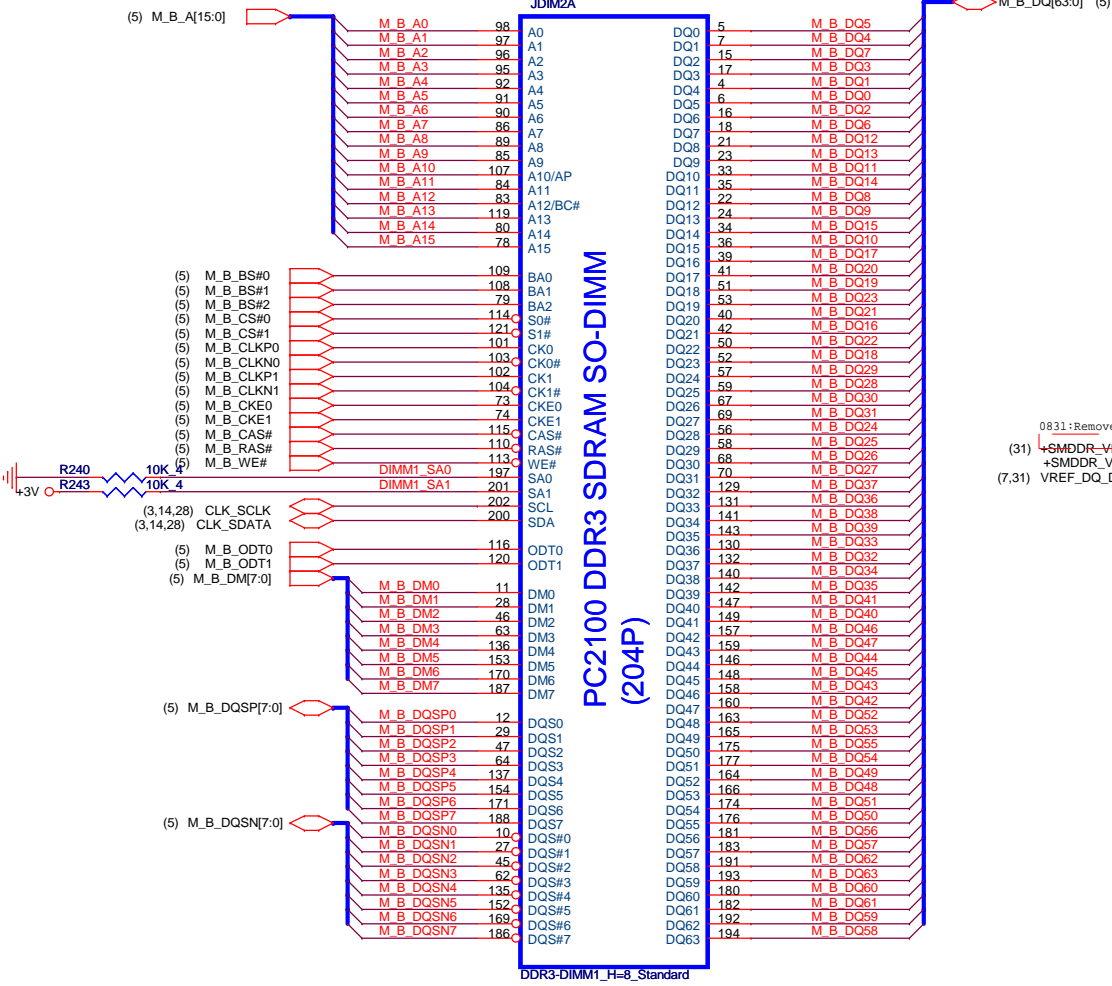
DDR_STD (DDR)



Place these Caps near So-Dimm0.



DDR_STD(DDR)



GPU_1(VGA)

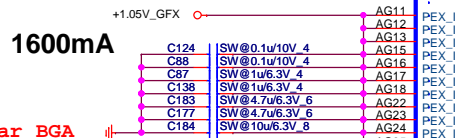
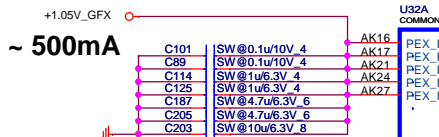
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A

N11P GPU : AJON11P0T05

N11M GPU : AJON11M0T07

N11P_A2 GPU : AJON11P0T20

N11M_B1 GPU : AJON11M0T22

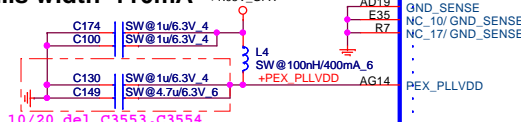


Near BGA



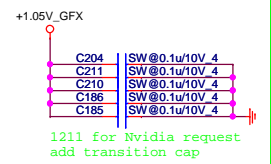
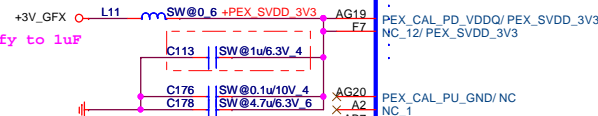
10/20 add

12~16 mils width 110mA



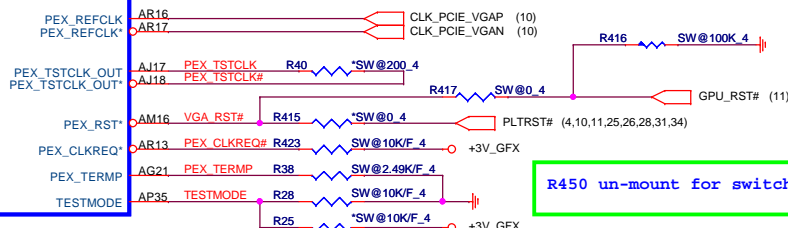
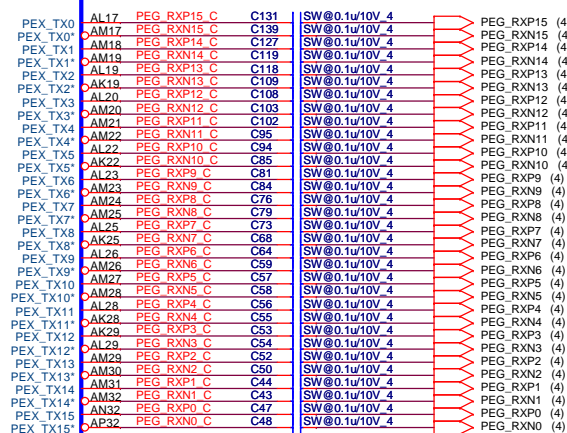
12~16 mils width

10/20 Modify to 1uF



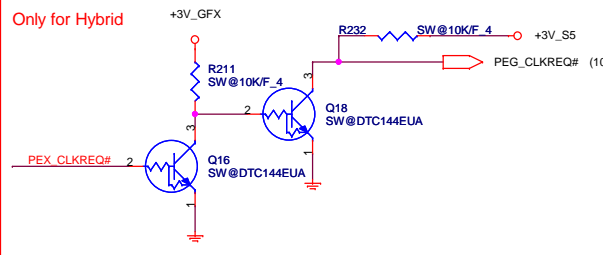
1211 for Nvidia request add transition cap

PCI EXPRESS

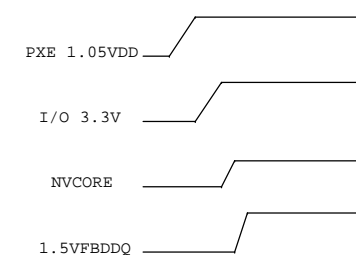
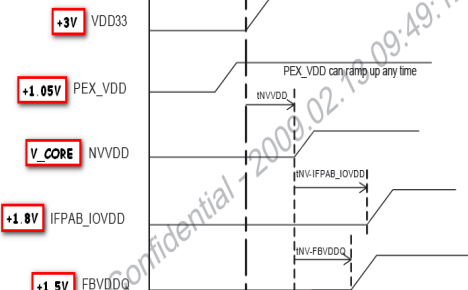


R450 un-mount for switchable function

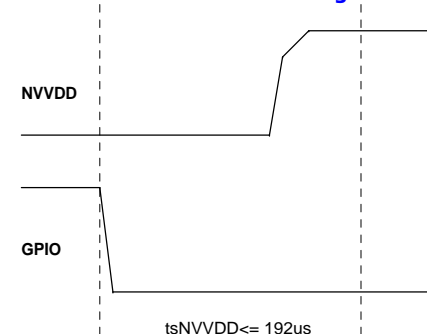
Only for Hybrid



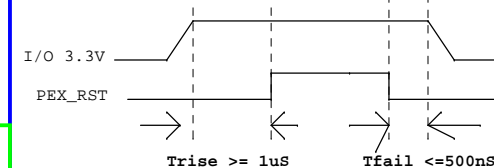
power up sequence



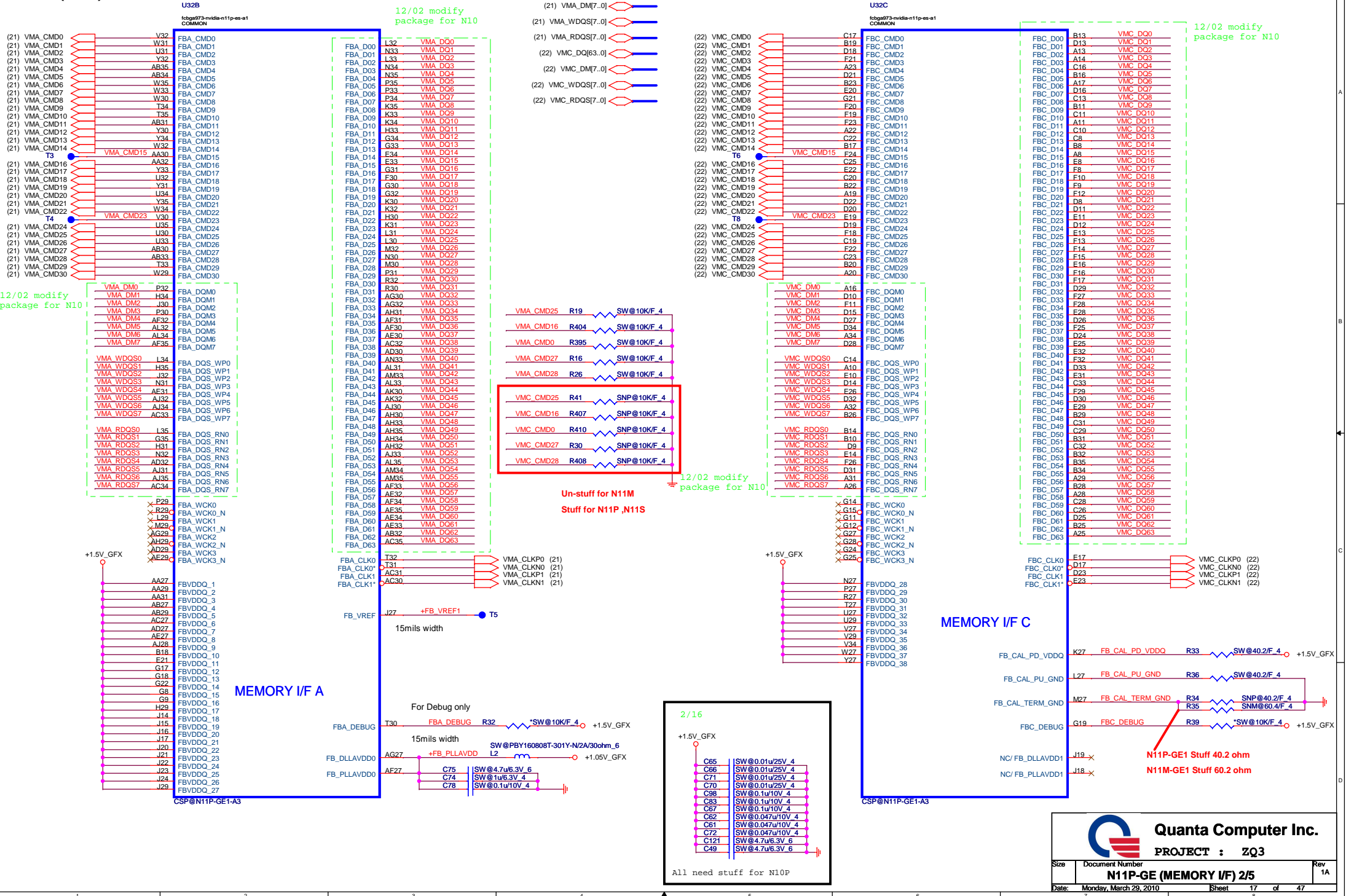
NB9M: VGACORE +0.90V (Normal) , +1.09V NVVDD Maximum Settling Time

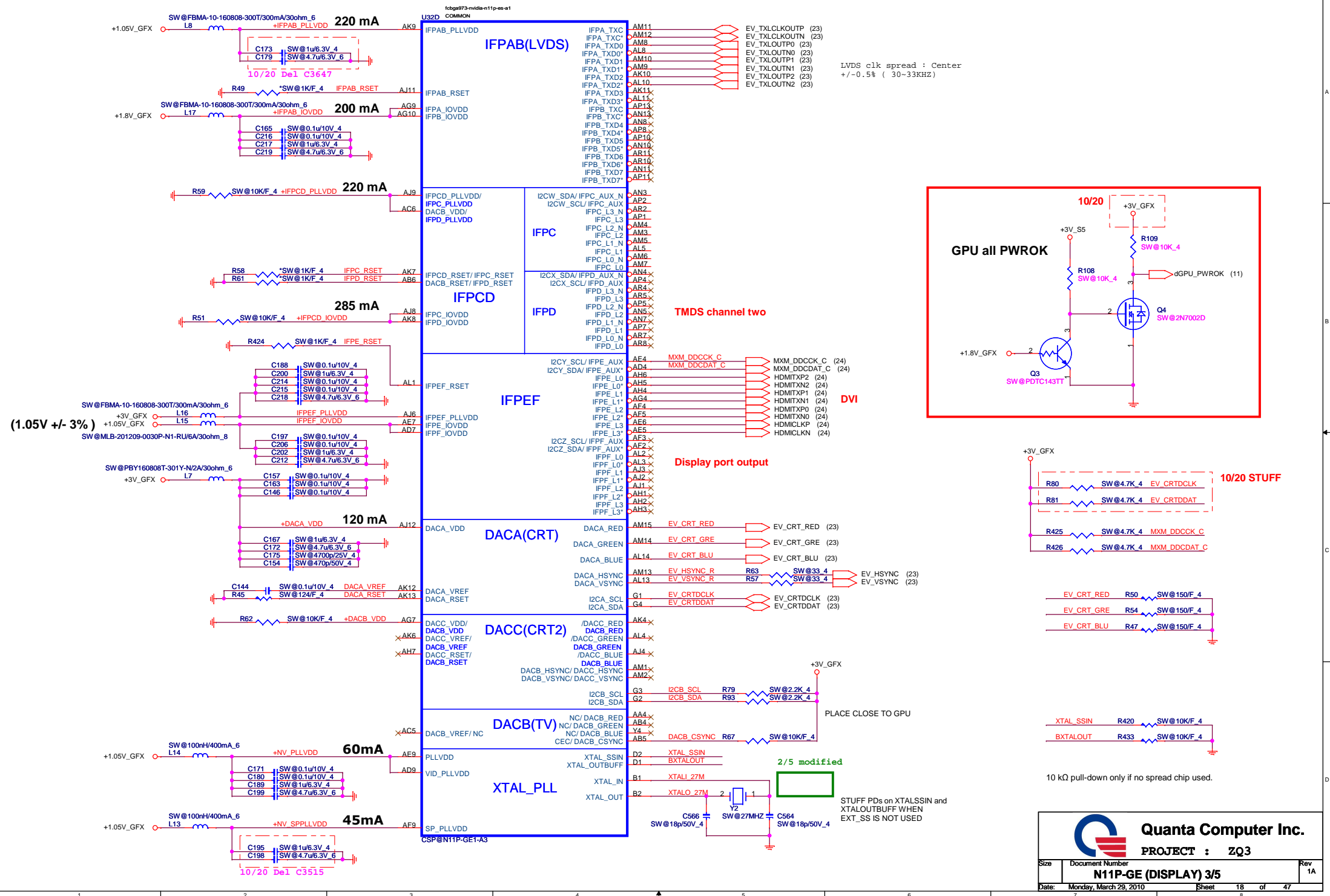


PEX_RST timing

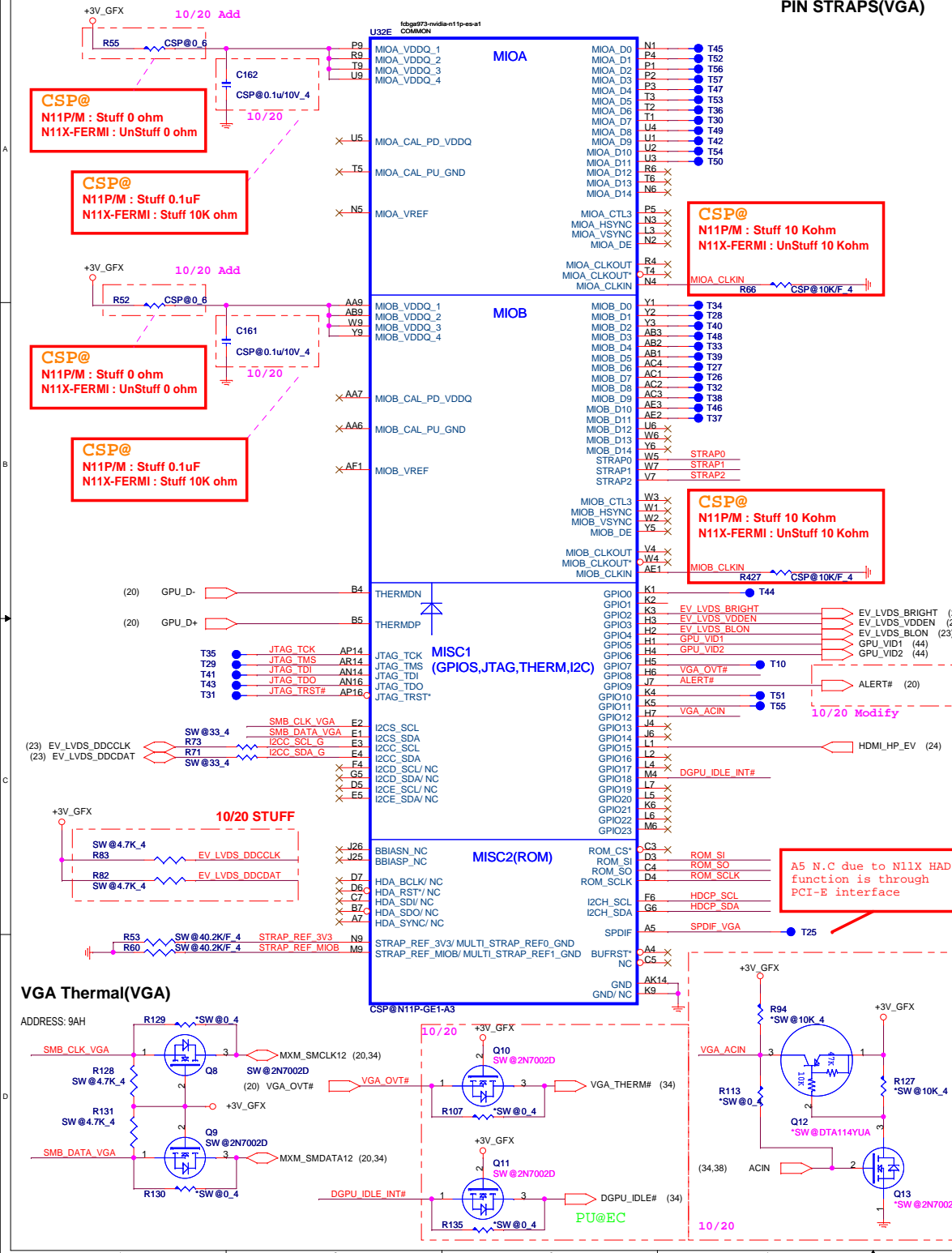


GPU_2(VGA)



GPU_3(VGA)

PIN STRAPS(VGA)

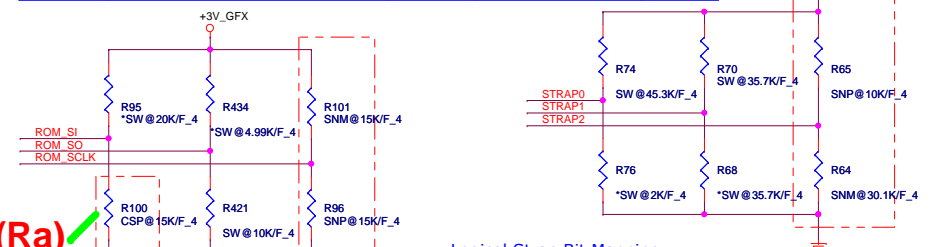


	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SIZE
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 101
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix	H5TQ1G63BFR-12C	PD 150
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung	K4W1G1646E-HC12	PD 201
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

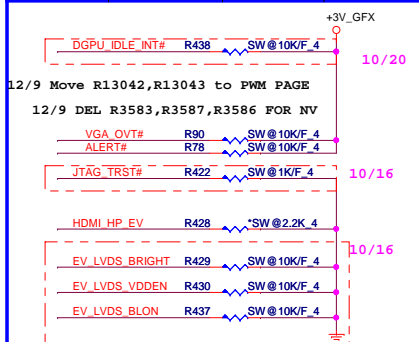


Logical Strap Bit Mapping

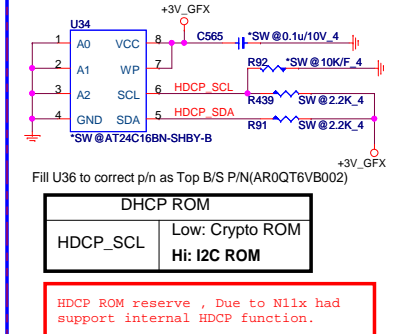
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM
Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

CHIP	ROM_SCLK	STRAP2	PCI_DEVICE
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PD 15K	PU 10K	0x0A29



HDCP ROM (VGA)



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

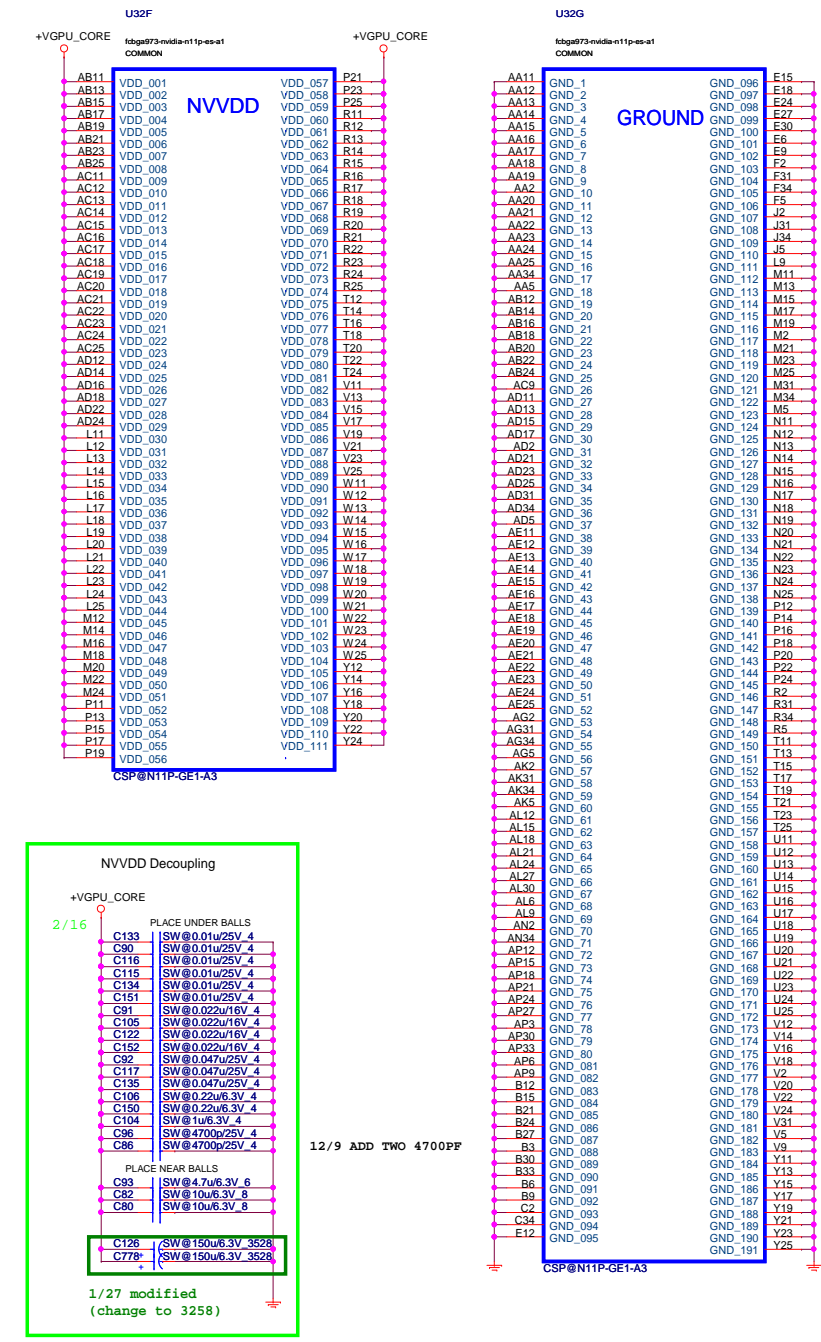


Quanta Computer Inc.

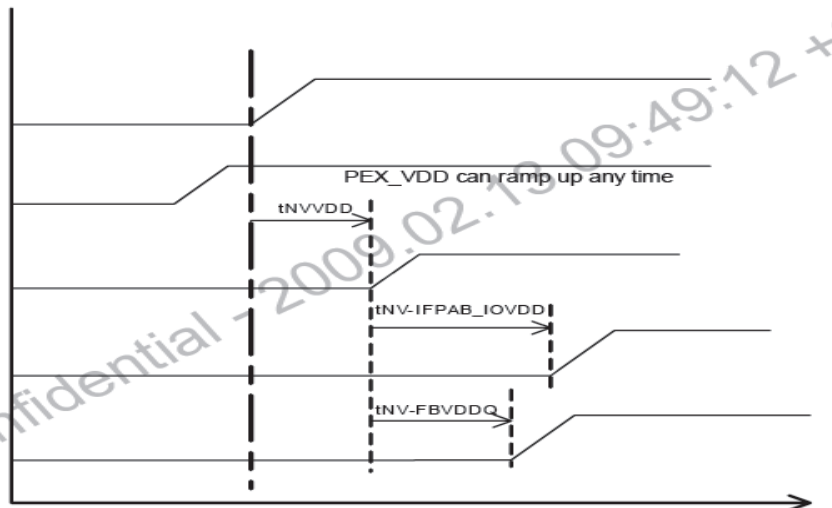
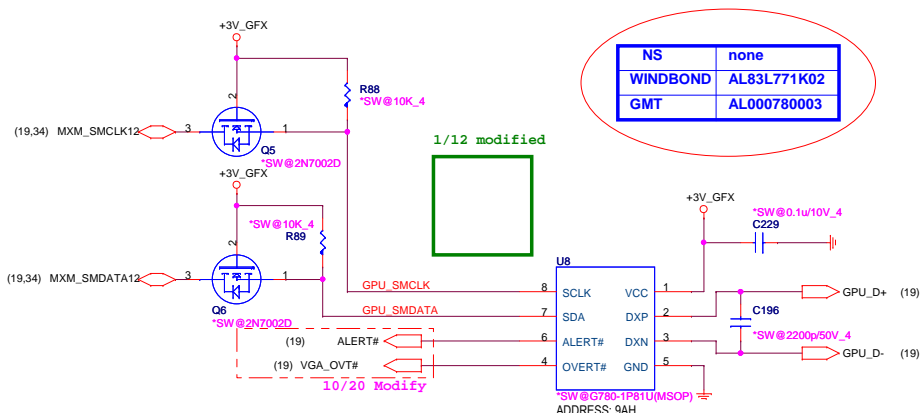
PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE (GPIO&STRAPS) 4/5	1A
Date:	Monday, March 29, 2010	Sheet 19 of 47

GPU_4(VGA)



Thermal Sensor(VGA)

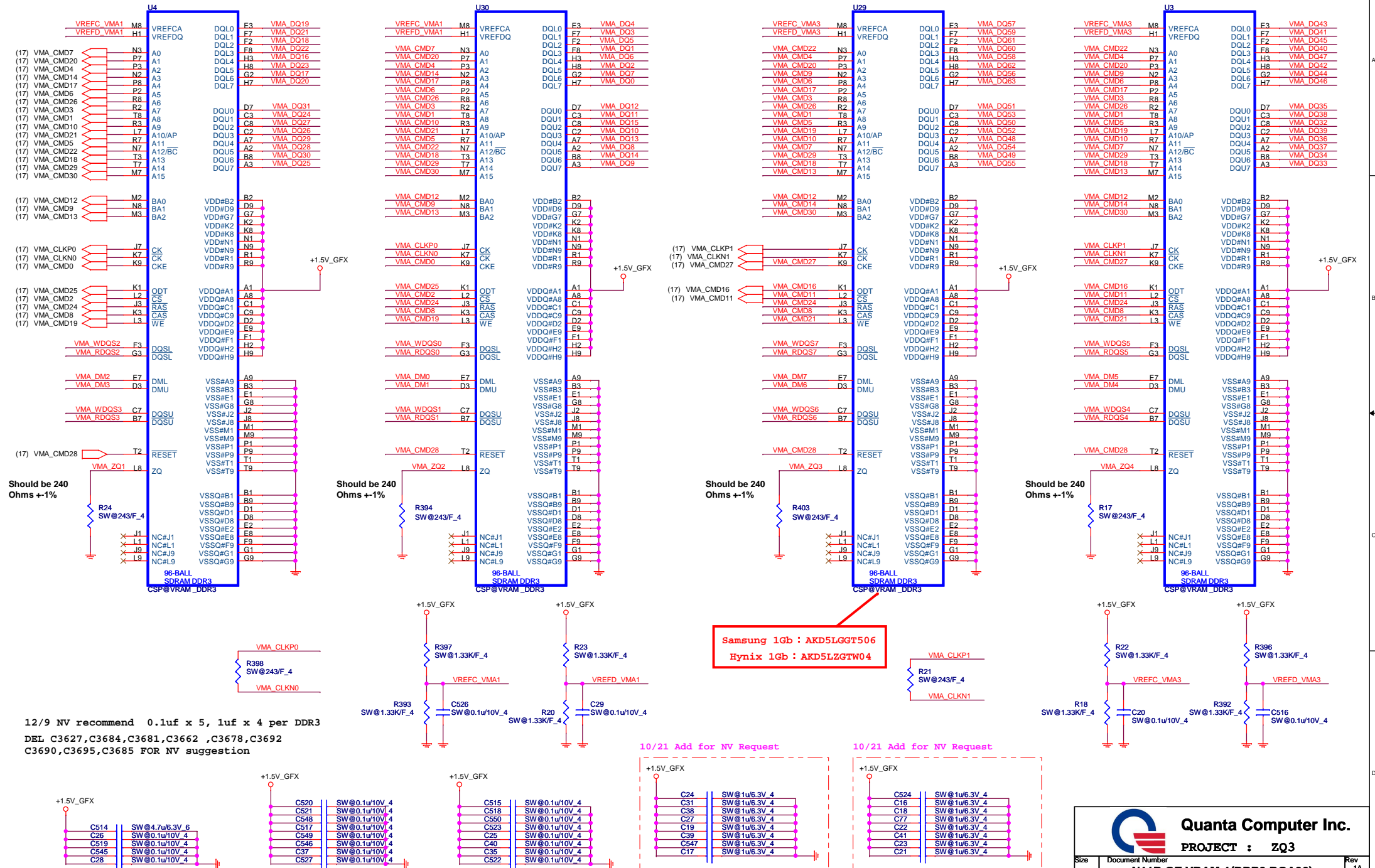


VRAM_A(VGA)

```
(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]
```

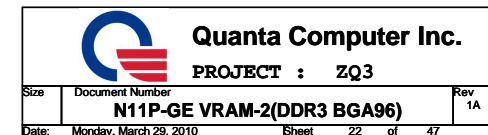
CHANNEL A: 256MB/512MB DDR3

(17,22,46) +1.5V_GFX ☐



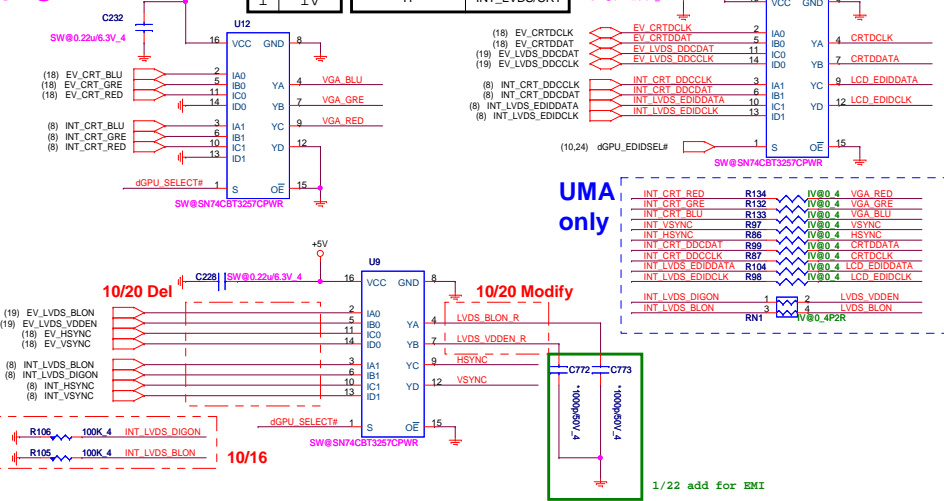
```
(17) VMC_DQ[63..0]
(17) VMC_DM[7..0]
(17) VMC_WDQS[7..0]
(17) VMC_RDQS[7..0]
```

(17,21,46) +1.5V_GFX

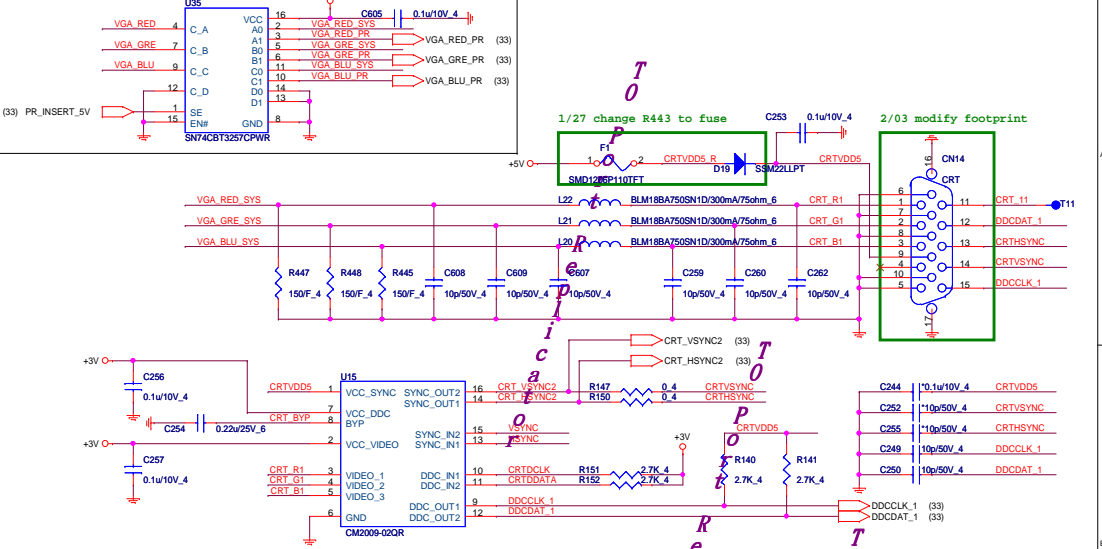


CRT Switch(CRT)

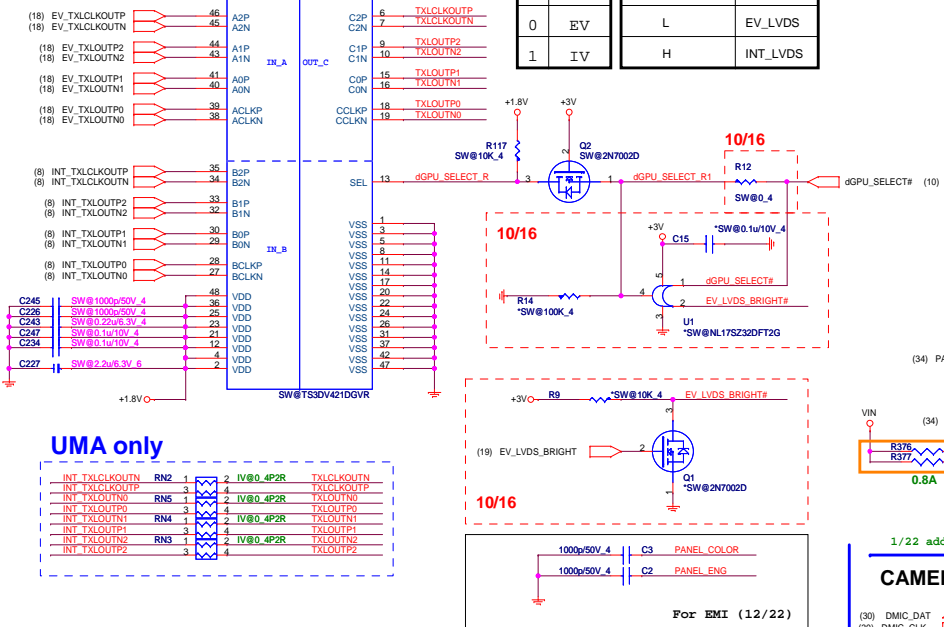
IV@
SW@



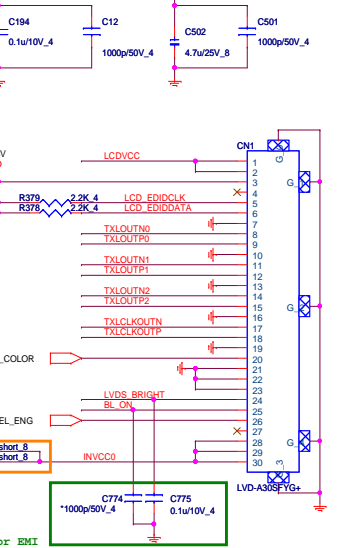
CRT SWITCH (DOK)



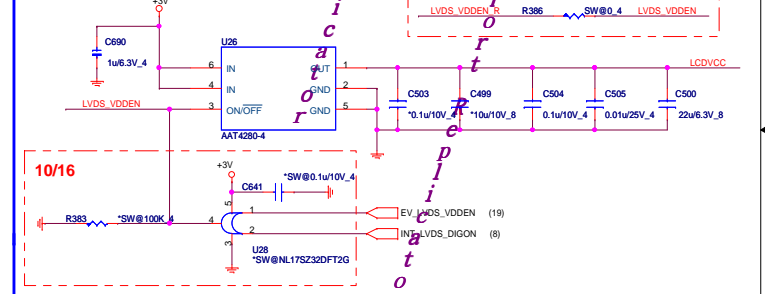
LVDS Switch (LDS)



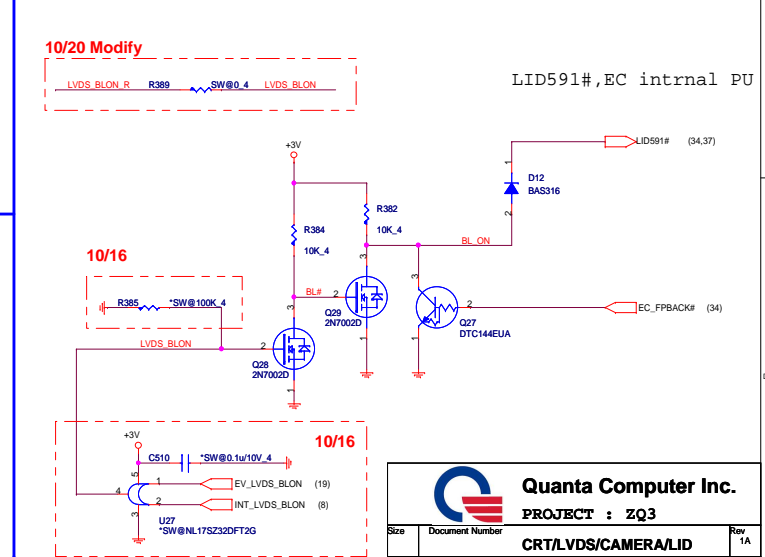
LVDS



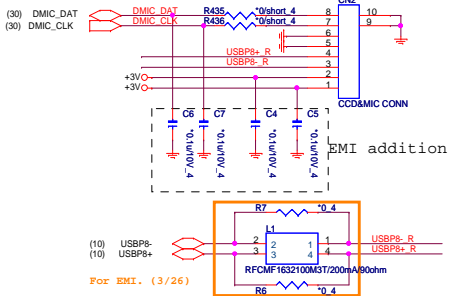
LCD Power(LDS)



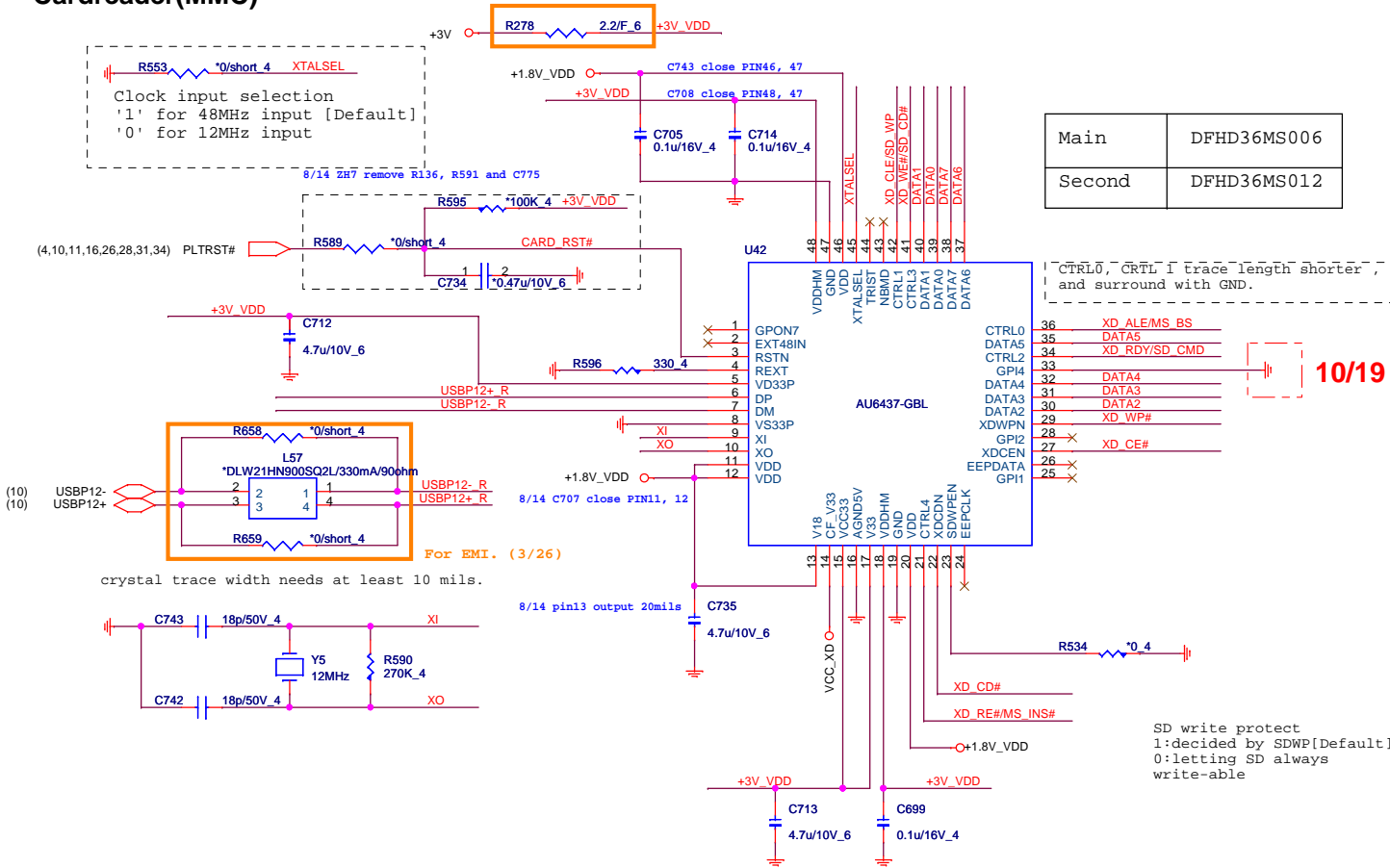
Backlight Control (LDS)



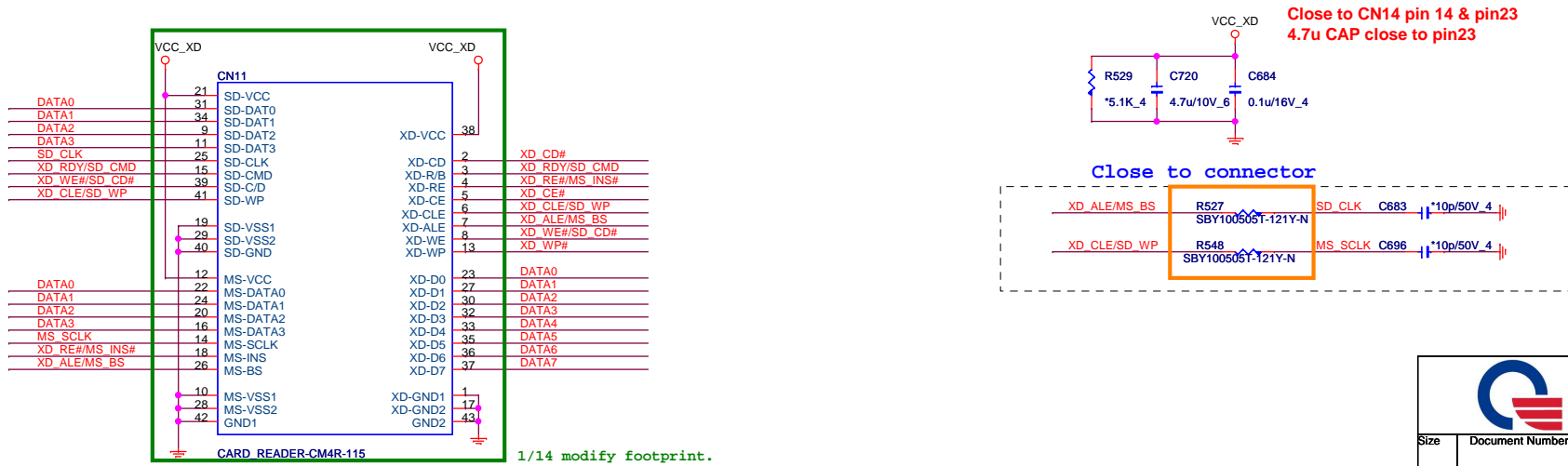
CAMERA Module(CCD)

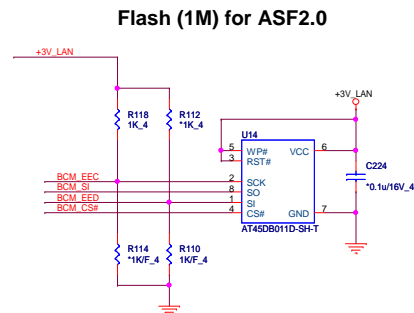


Cardreader(MMC)

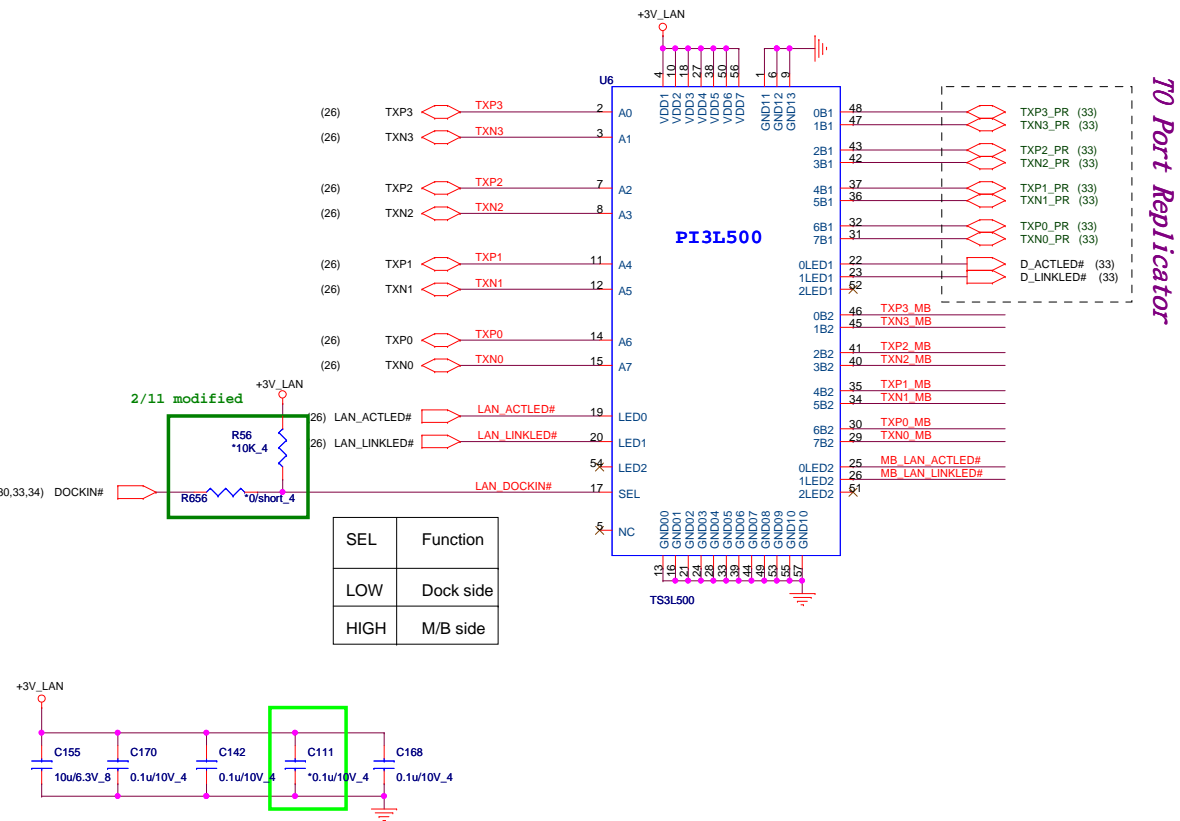


4 IN 1 CARD READER (MMC)



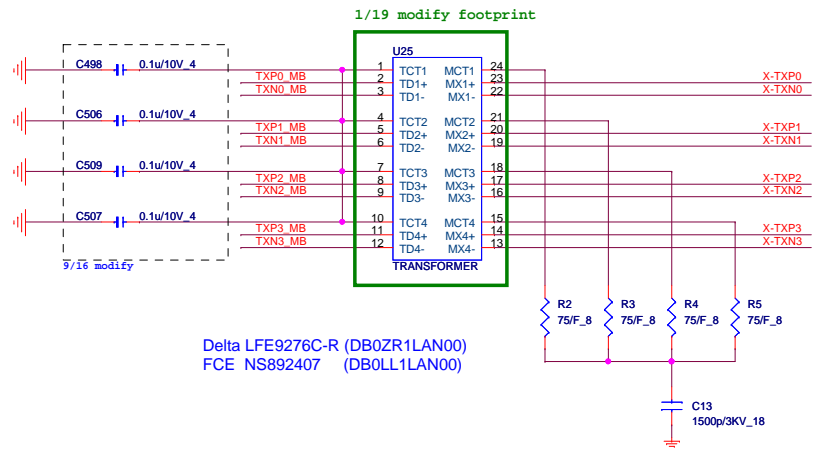


LAN SWITCH (DOK)



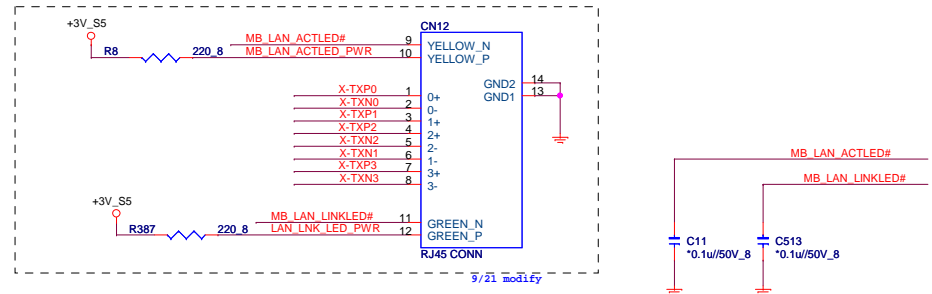
SEL	Function
LOW	Dock side
HIGH	M/B side

TRANSFORMER (LAN)

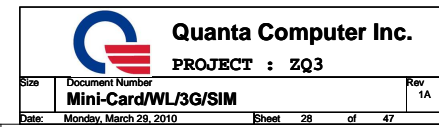


Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

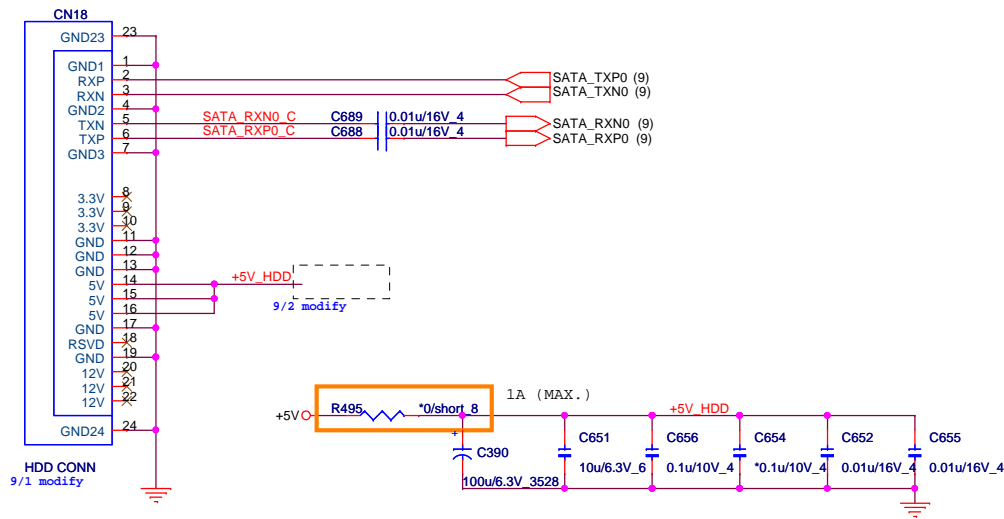
RJ45(LAN)



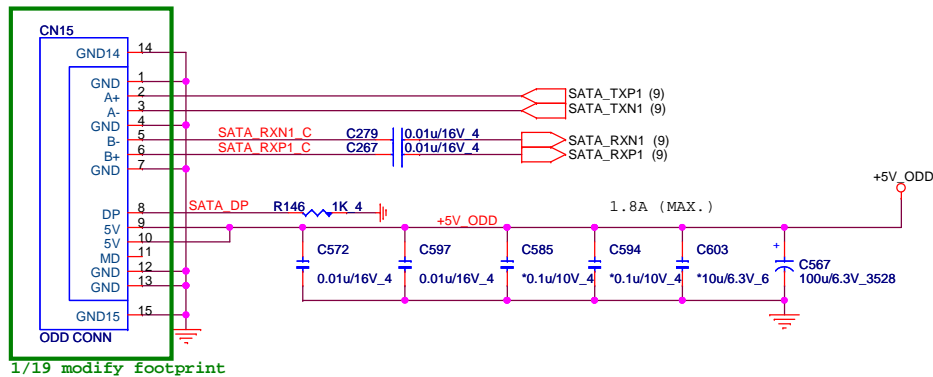
MINI-CARD WLAN/WMAX(MPC)



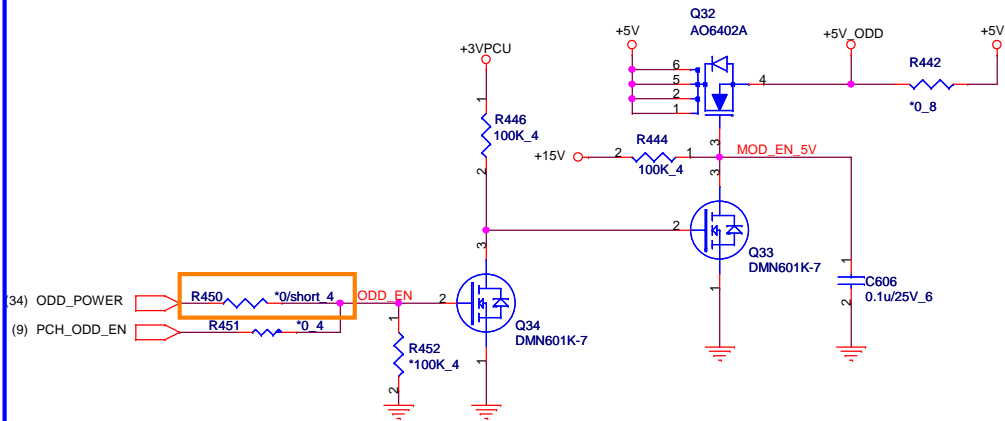
SATA HDD(HDD)



SATA ODD (ODD)

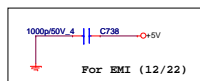


ODD POWER(ODD)



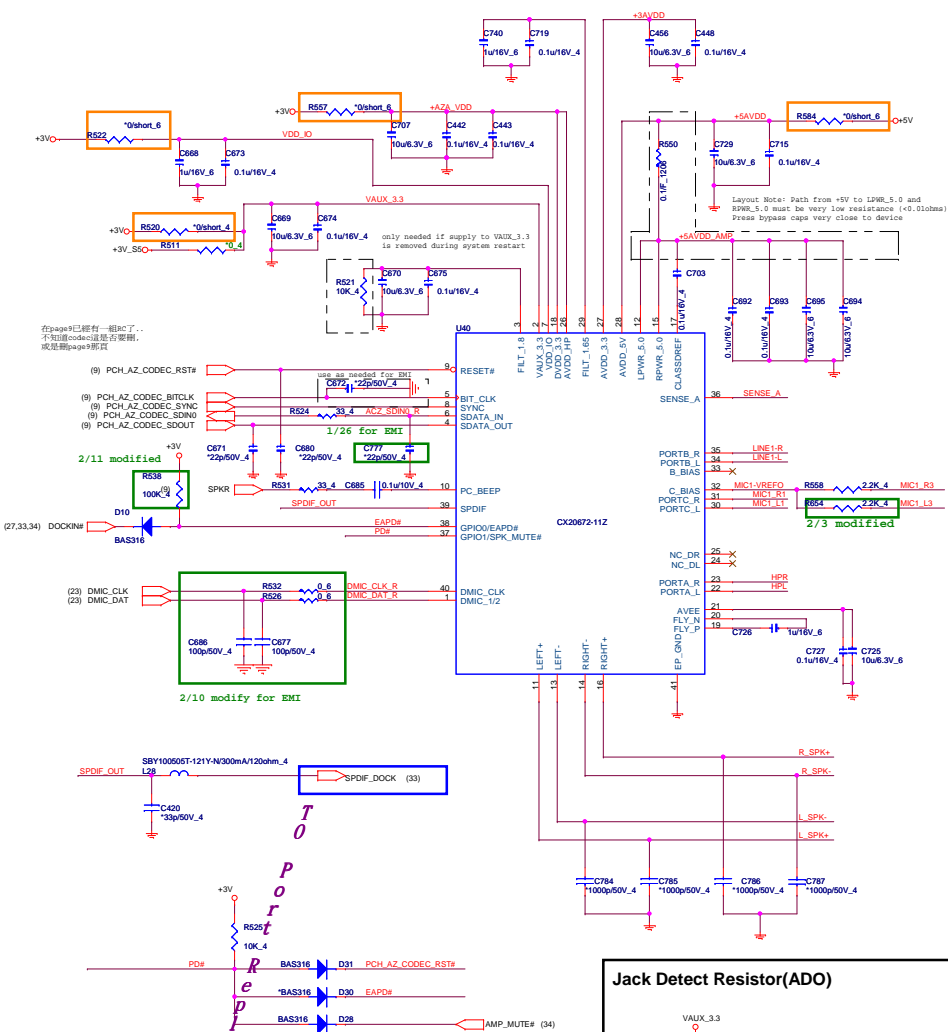
Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Codec(ADO)



For EMI (12/22)

internal LDO from 5v to 3.3v for analog power



INT SPEAKER CONN(AMP)

40nM for each signal 0 1/27 modified



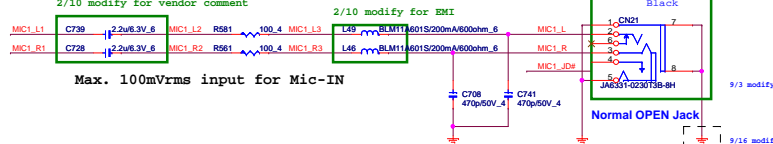
EXTERNAL MIC (AMP)

conn and 線路 follow Z01 and Z06, 但 C and R 值 follow conexas

2/10 modify for vendor comment

2/10 modify for EMI

1/22 modify footprint.



Docking MIC-IN(DOK)

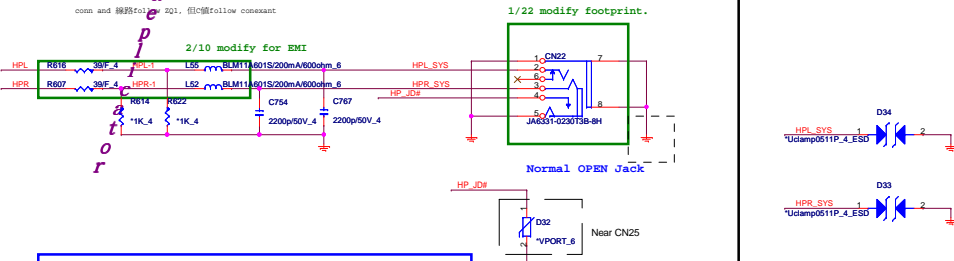
L48 BLM11A601S/200mA/600ohm_6 AU_MIC_IN_L
L47 BLM11A601S/200mA/600ohm_6 AU_MIC_IN_R
2/10 modify for EMI

LINE-OUT/SPDIFO(AMP)

conn and 線路follow ZQ1, 但C值follow conexant

2/10 modify for EMI

1/22 modify footprint.

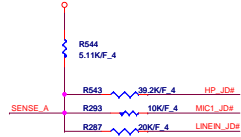


Docking LINE OUT/SPDIF (DOK)

2/10 modify for EMI

Jack Detect Resistor(ADO)

VAUX_3:

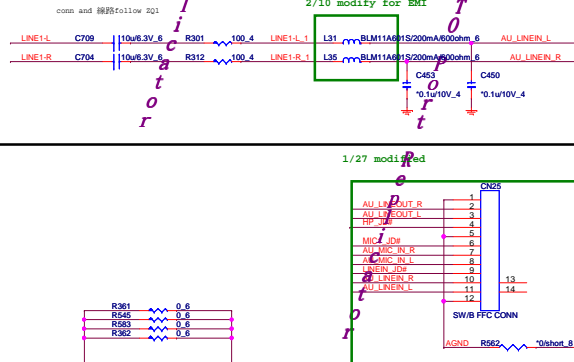


Docking LINE-IN (DOK) *P*

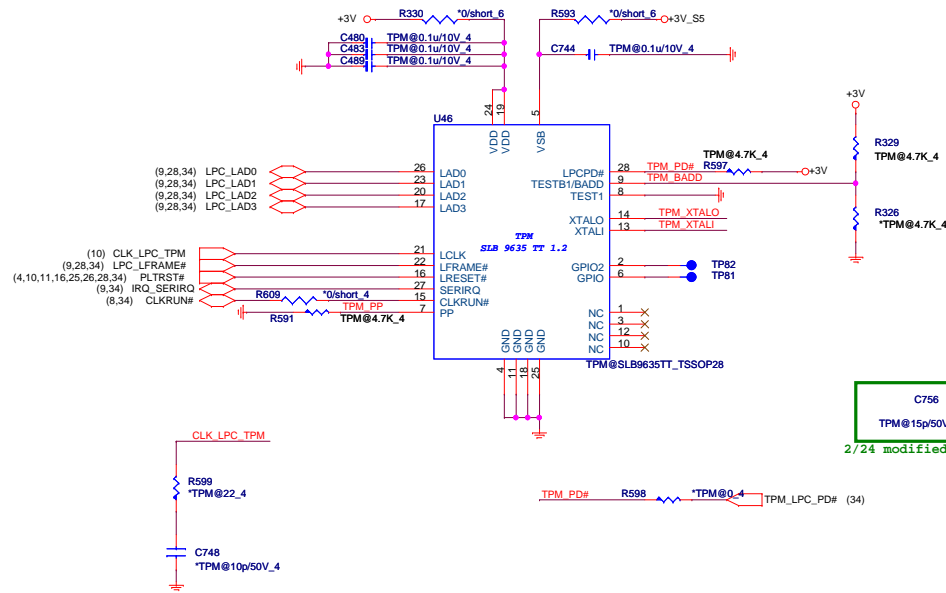
conn and 線路follow 2Q1

2/10 modify for EMI

1/27 modified



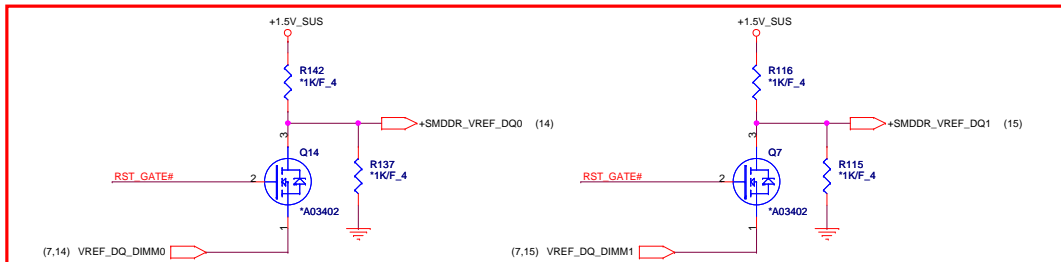
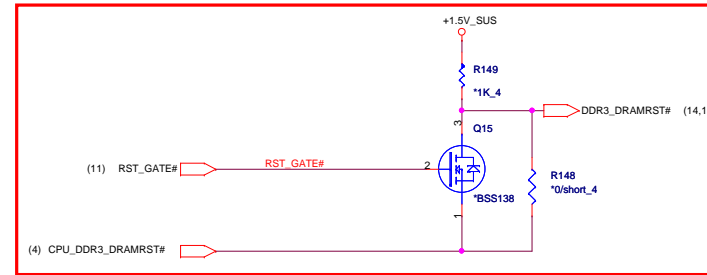
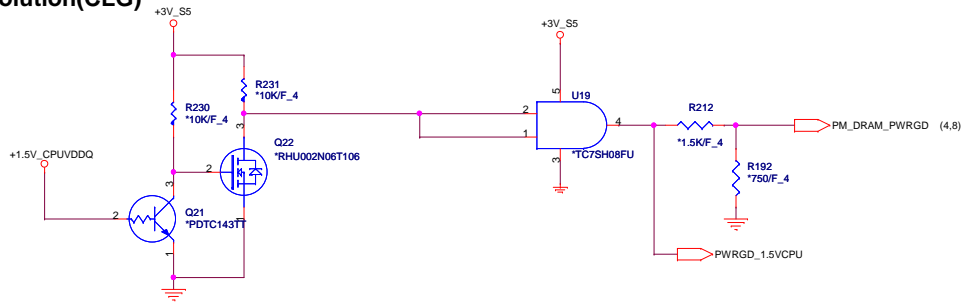
(TPM)

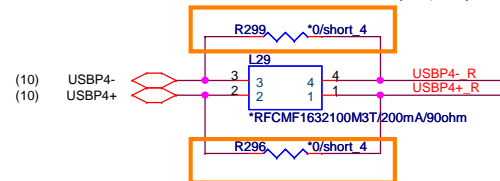
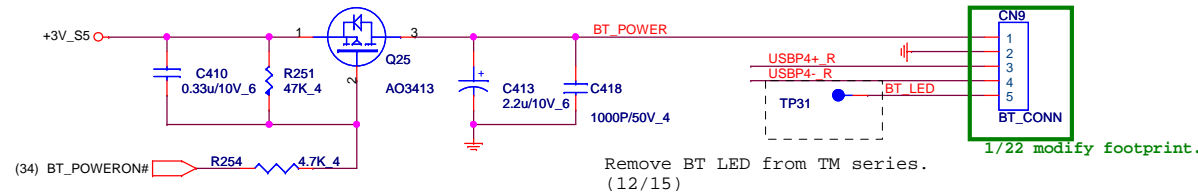
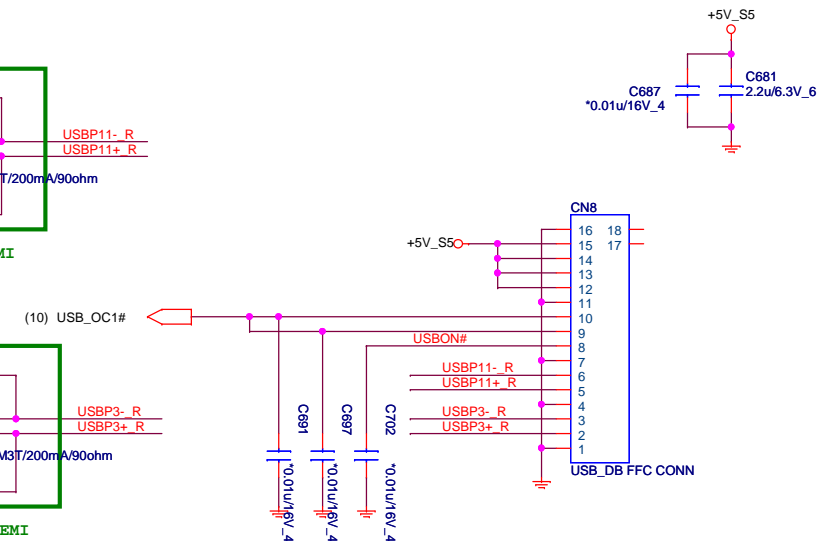
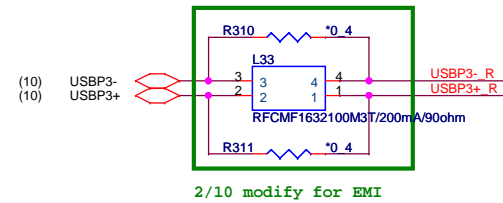
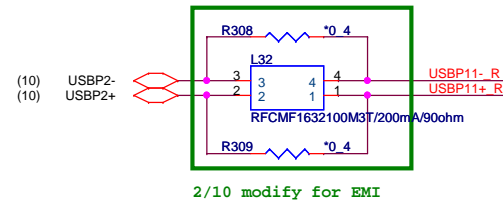
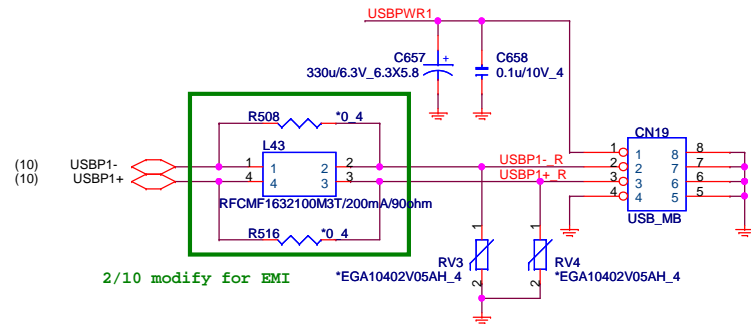
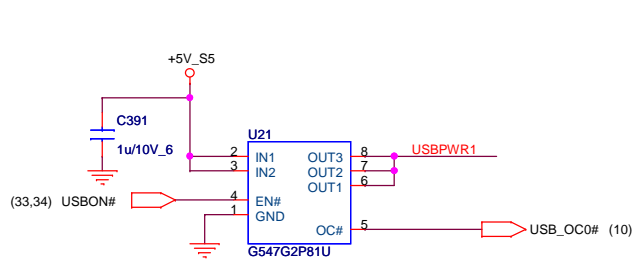


	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

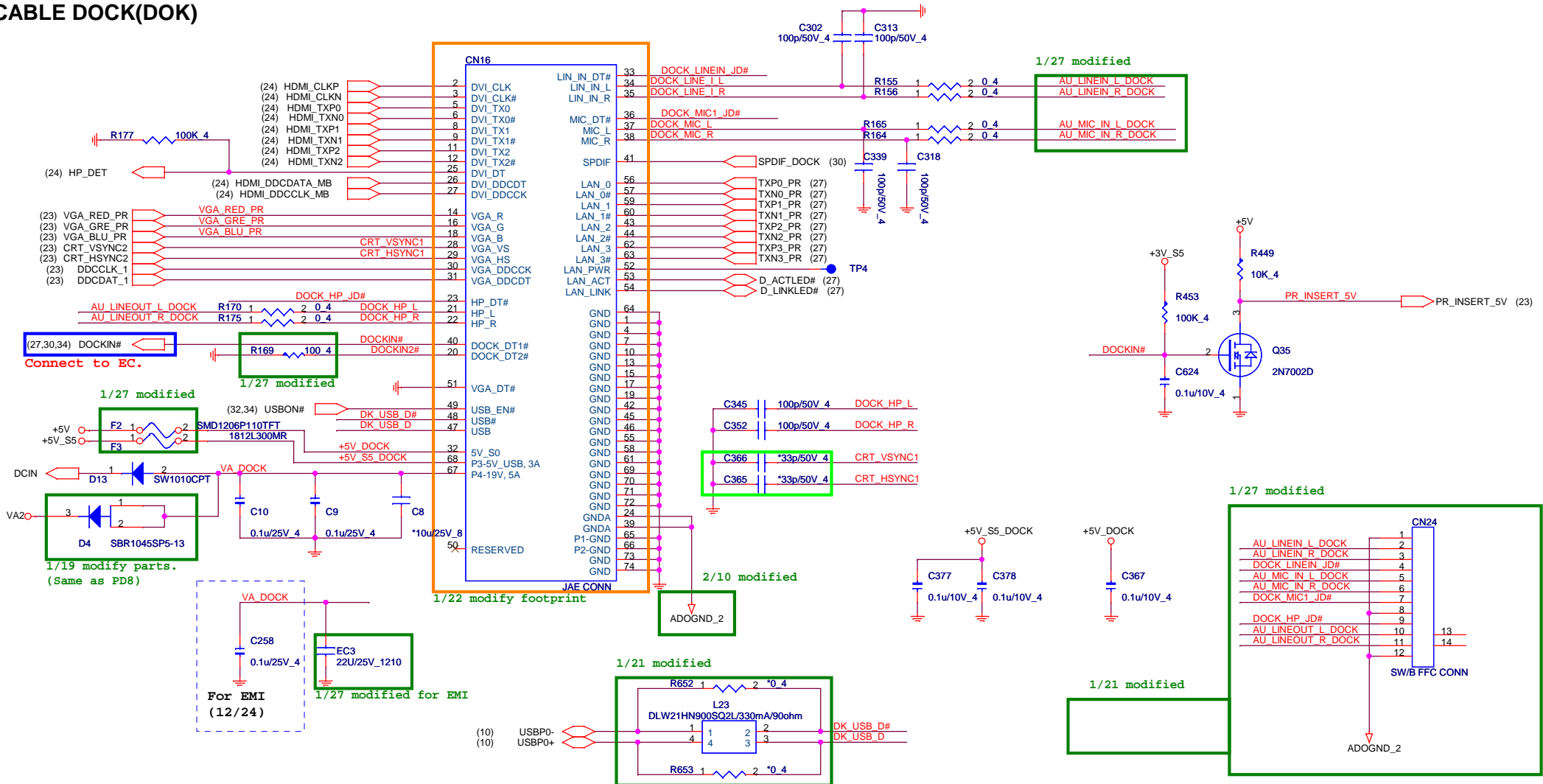


S3 leakage solution(CLG)

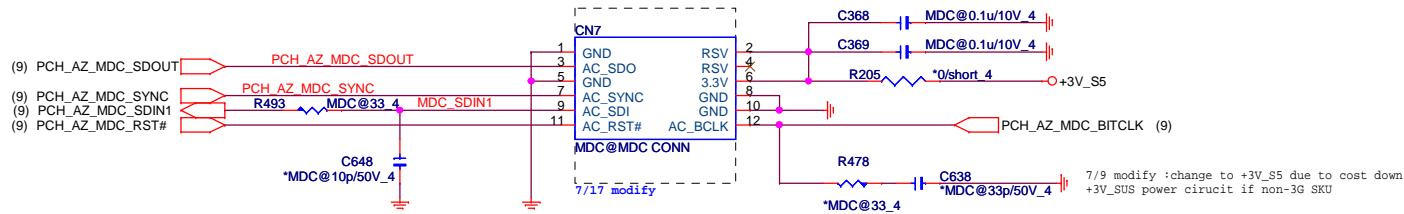





CABLE DOCK(DOK)

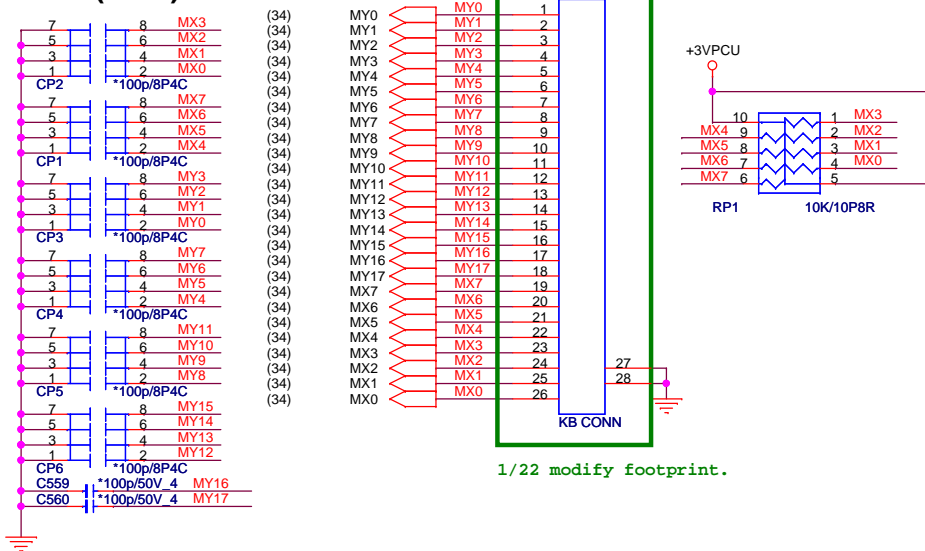


MDC(MDM)

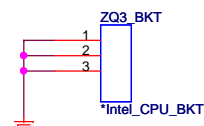
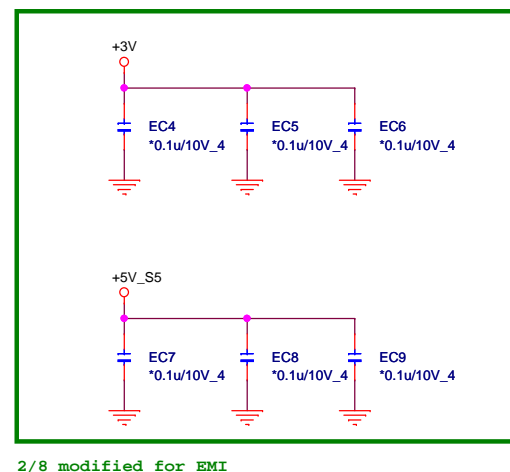
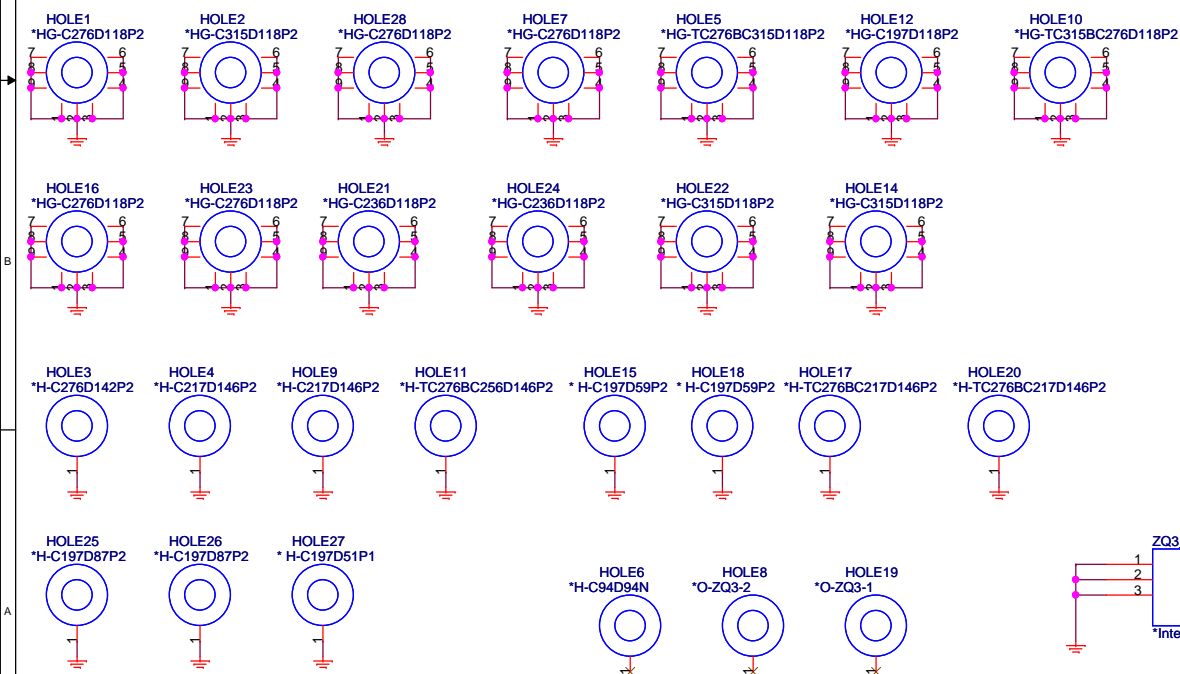
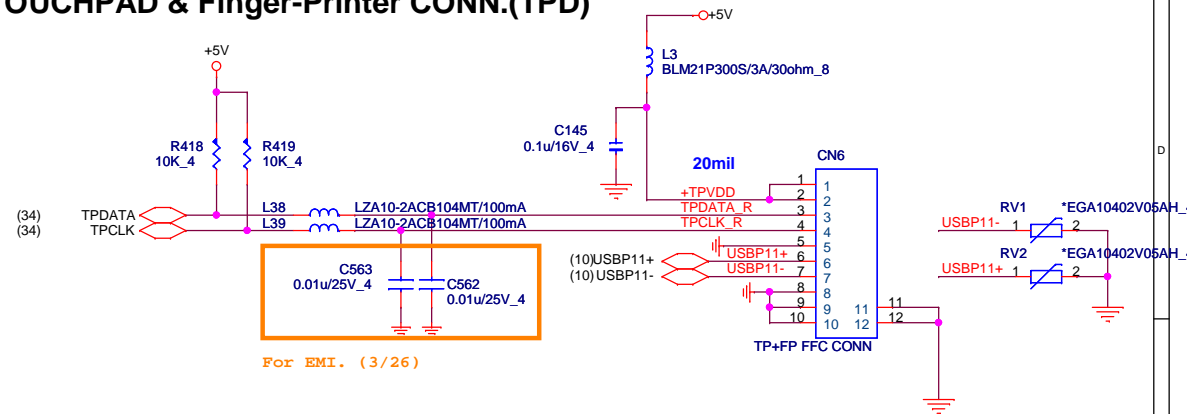


 Quanta Computer Inc. PROJECT : ZQ3		Rev 1A
Size	Document Number	
Docking		
Date:	Monday, March 29, 2010	Sheet 33 of 47

INT K/B (KBC)



TOUCHPAD & Finger-Printer CONN.(TPD)

**Quanta Computer Inc.**

PROJECT : ZQ3

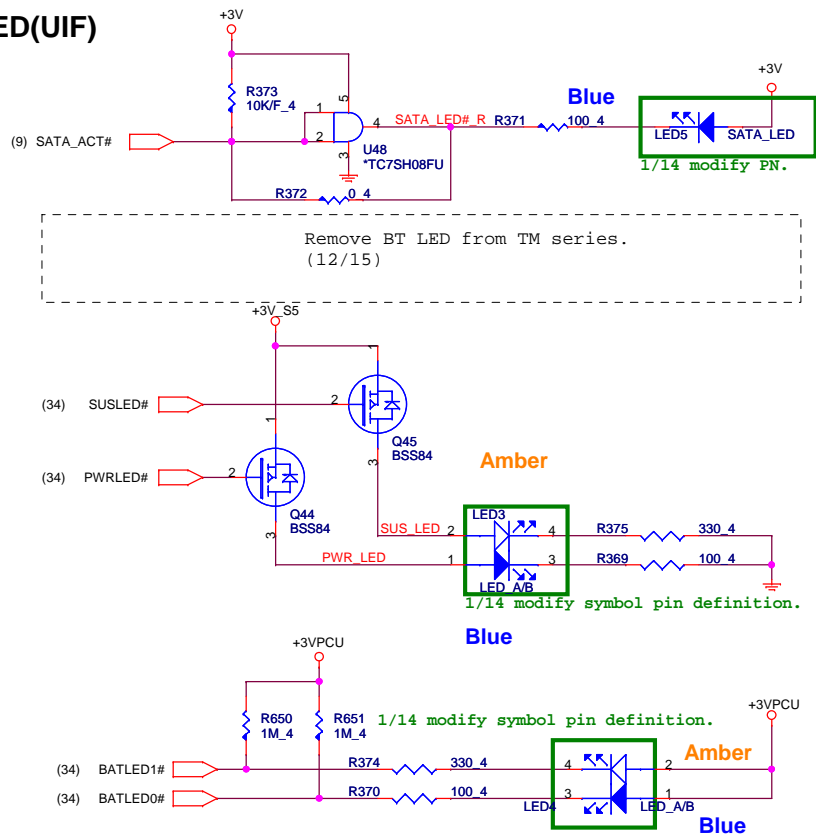
Size	Document Number
	KB/TP+FP/CIR/BT/TPScreen

Rev
1A

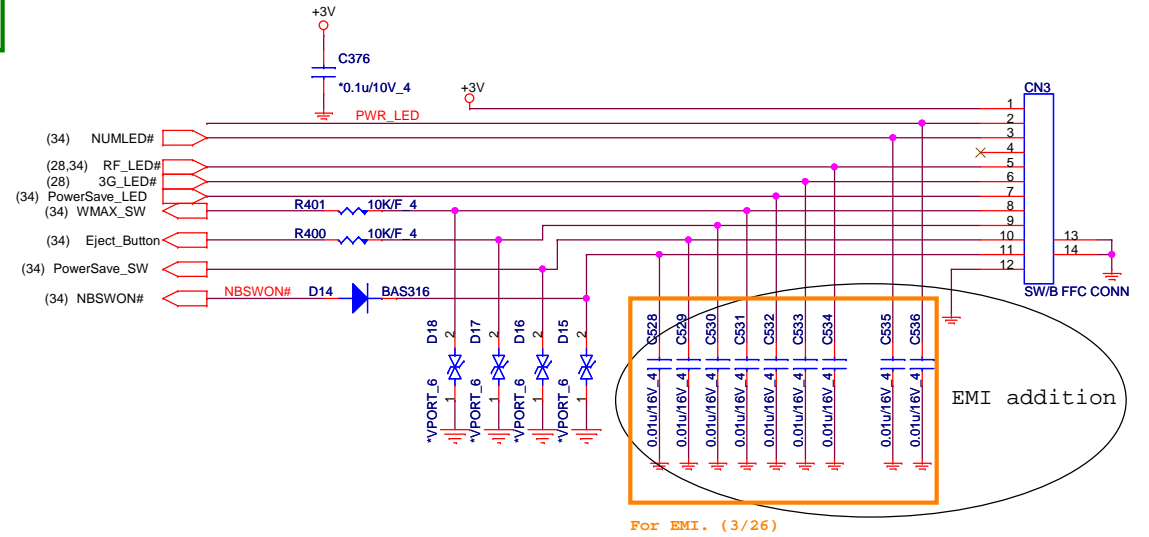
Date: Monday, March 29, 2010

Sheet 35 of 47

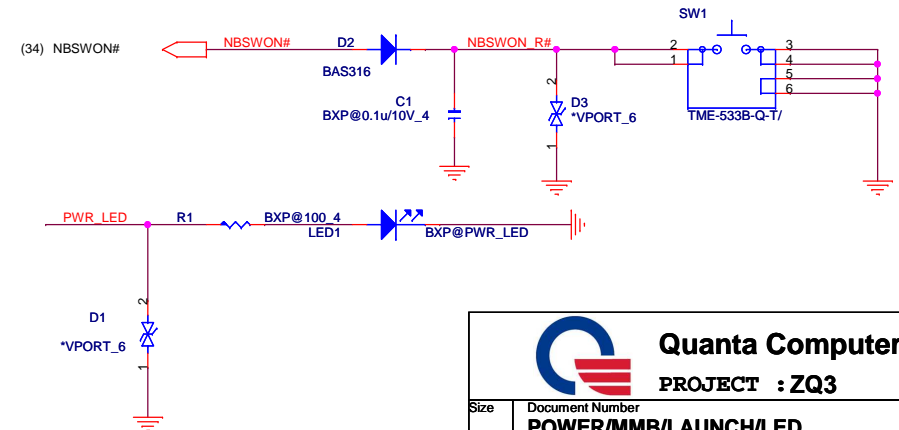
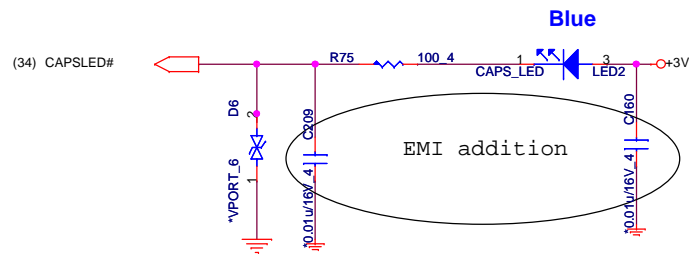
M/B LED(UIF)



SW BOARD CONNECTOR(UIF)



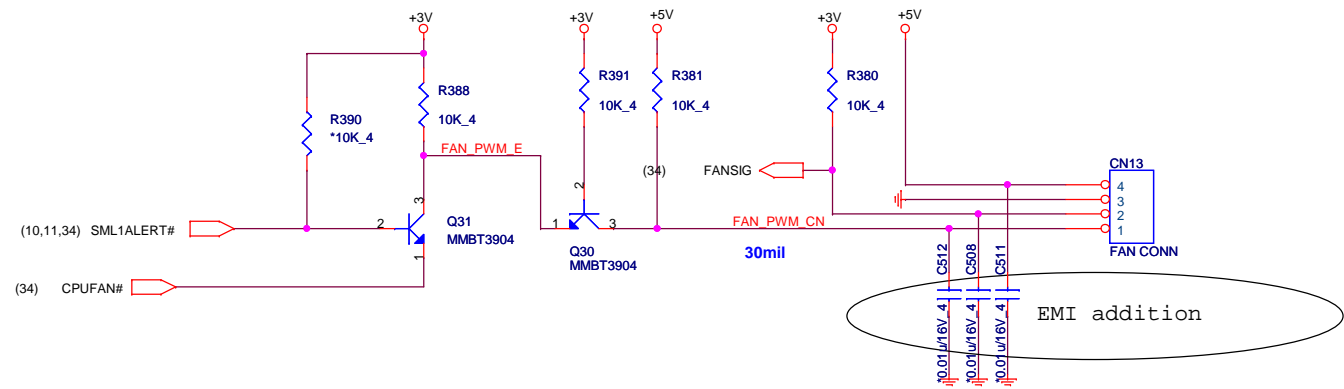
M/B LED(UIF)



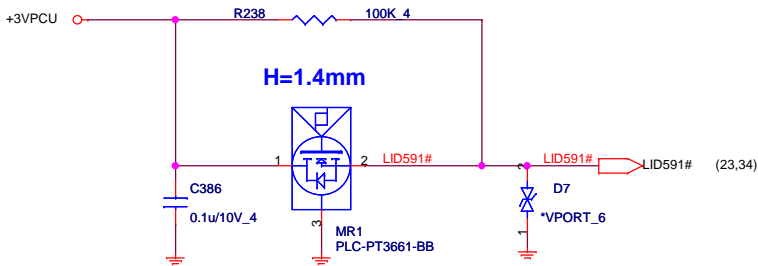
Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date:	Monday, March 29, 2010	Sheet 36 of 47

CPU FAN(THM)

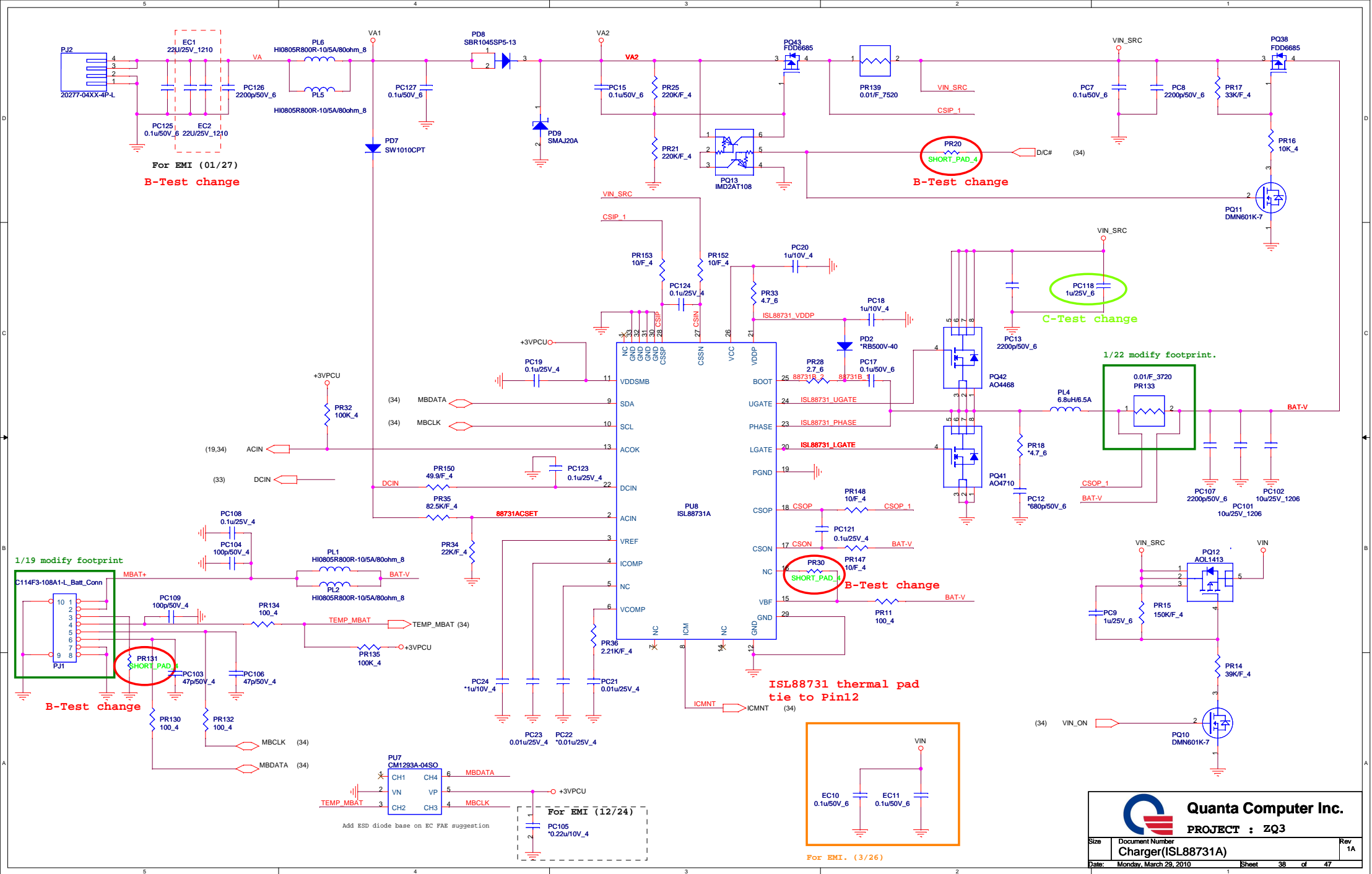


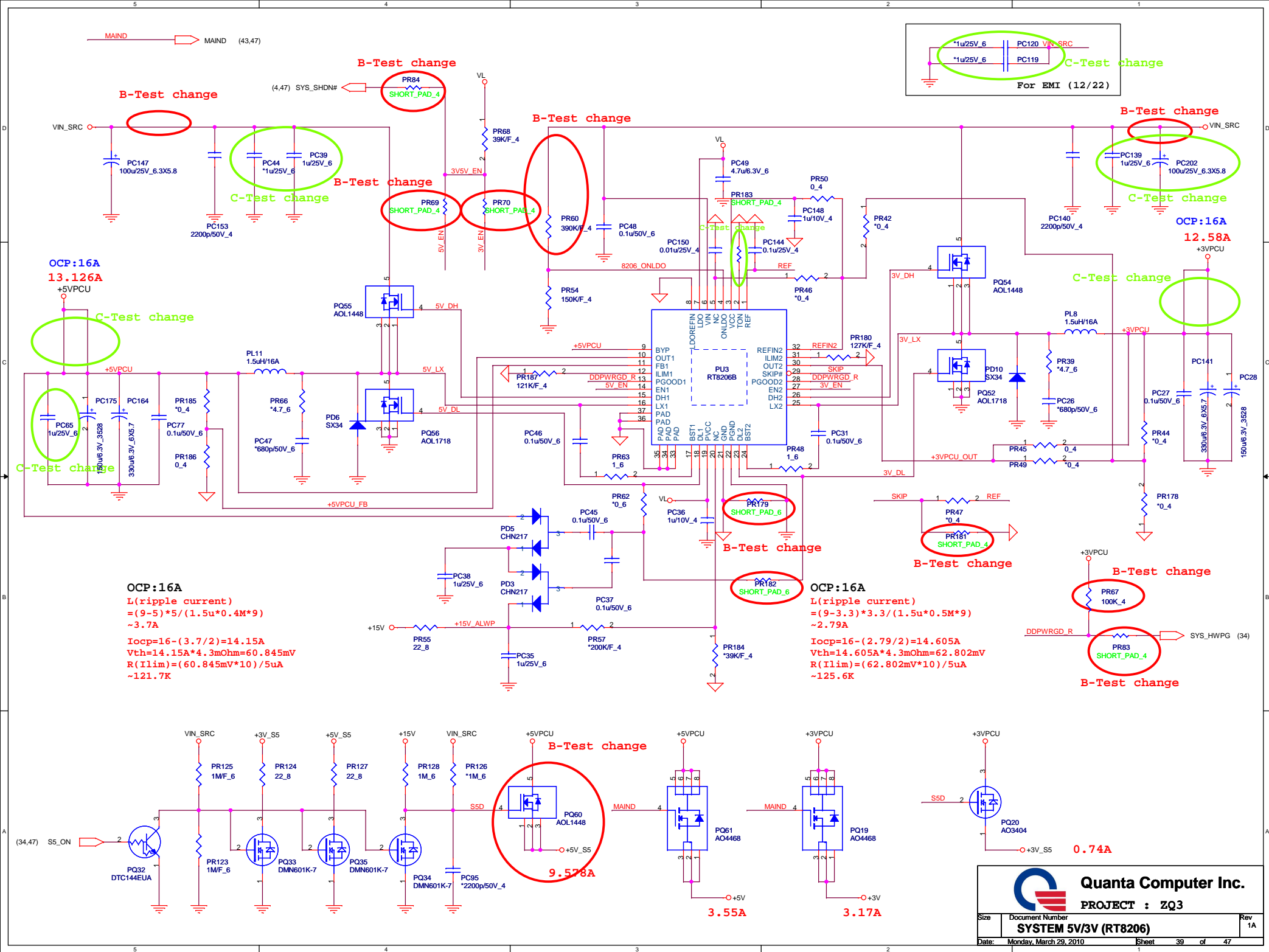
HALL SENSOR(HSR)

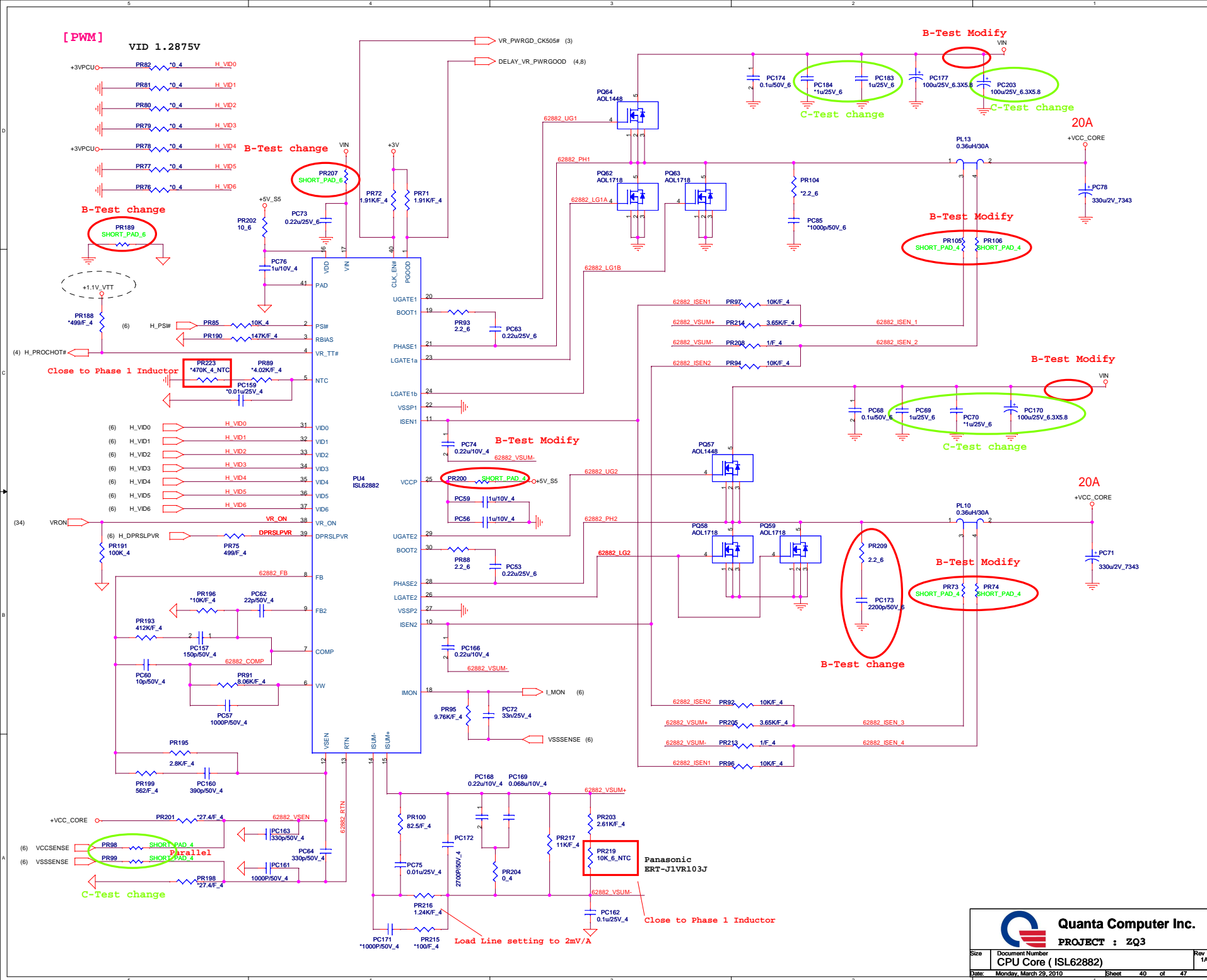


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PROJECT : ZQ3

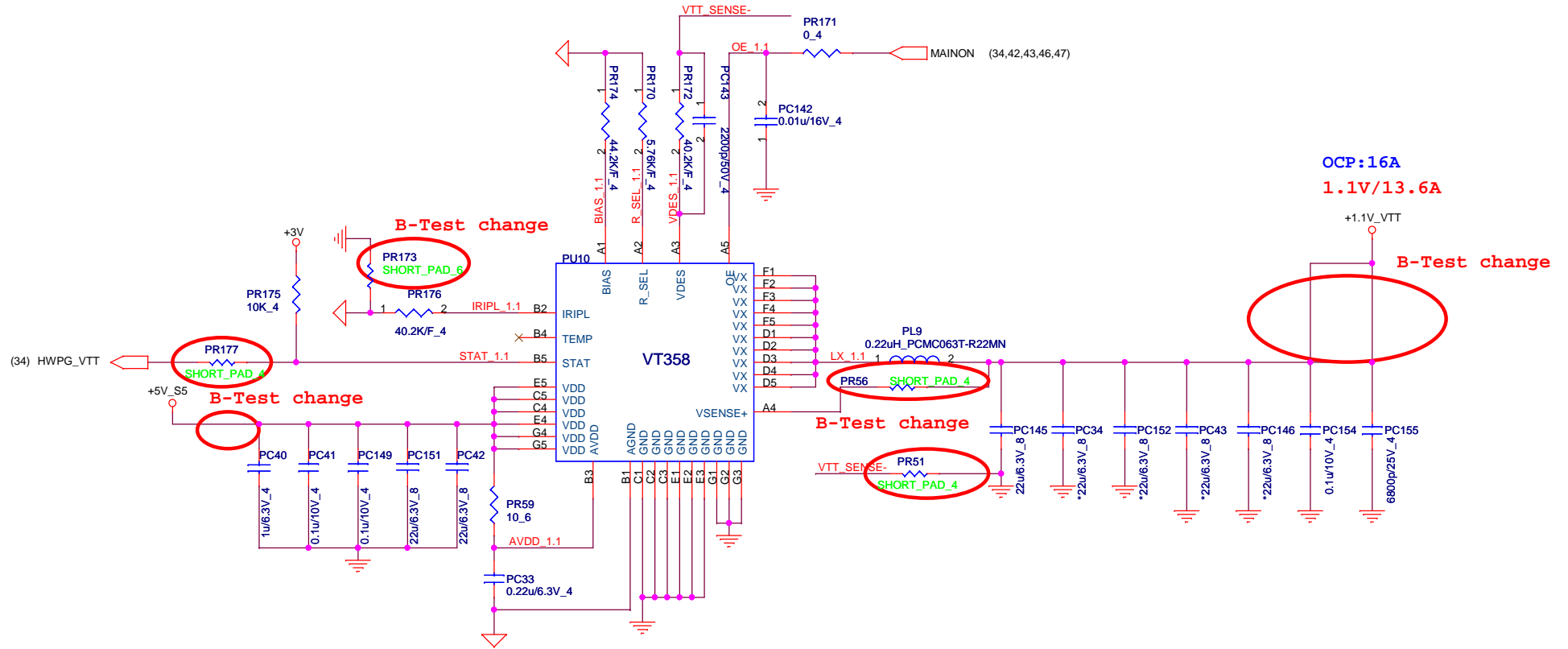
Size	Document Number	Rev
	FAN/Thermal Protection	1A
Date:	Monday, March 29, 2010	Sheet 37 of 47





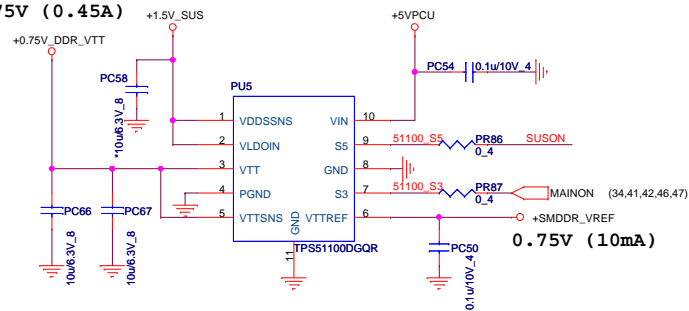
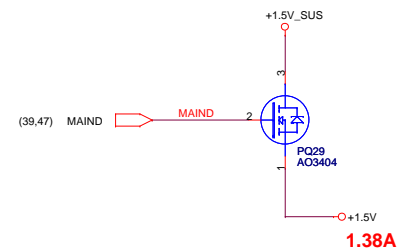


[PWM]



Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date:	Monday, March 29, 2010	Sheet 41 of 47



	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

