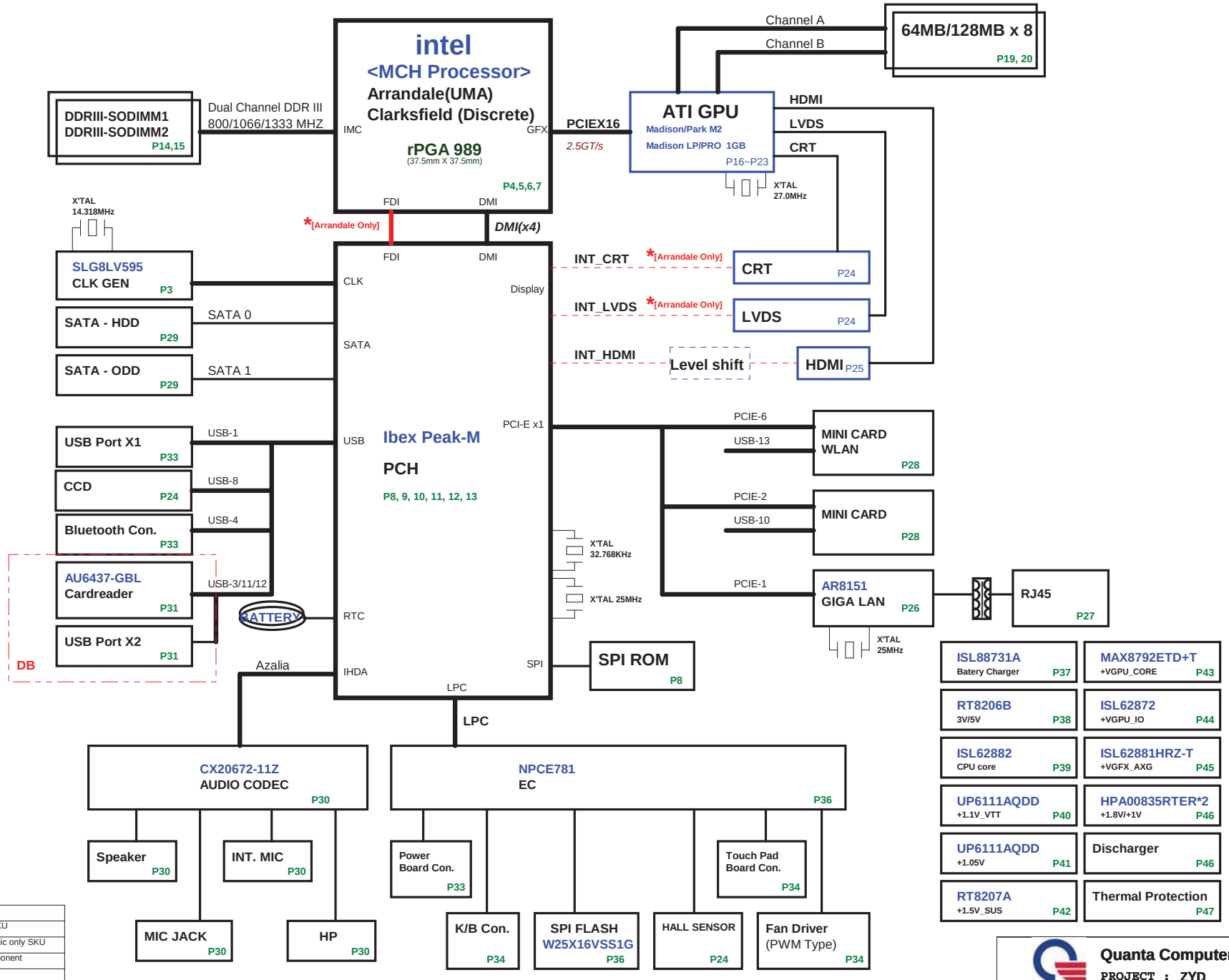
ZYD SYSTEM BLOCK DIAGRAM

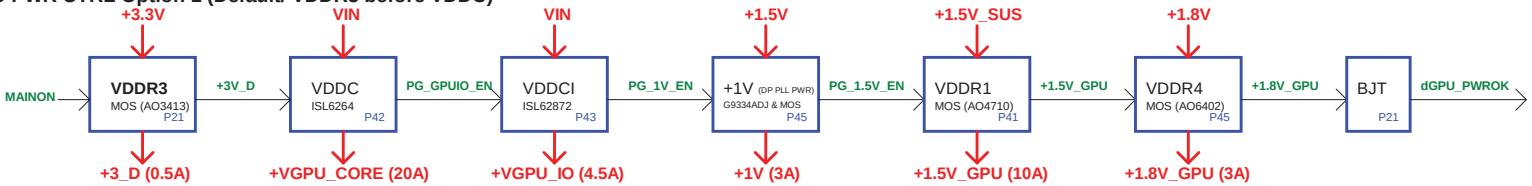


BOM Option Table

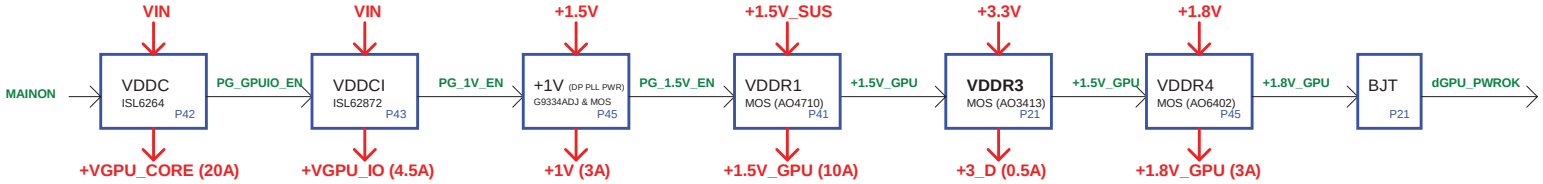
Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
SP@	special case component
*	do not stuff

Quanta Computer Inc.
PROJECT : ZYD
Size: Document Number: Block Diagram Rev: 3B
Date: Tuesday, April 06, 2010 Sheet 1 of 50

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



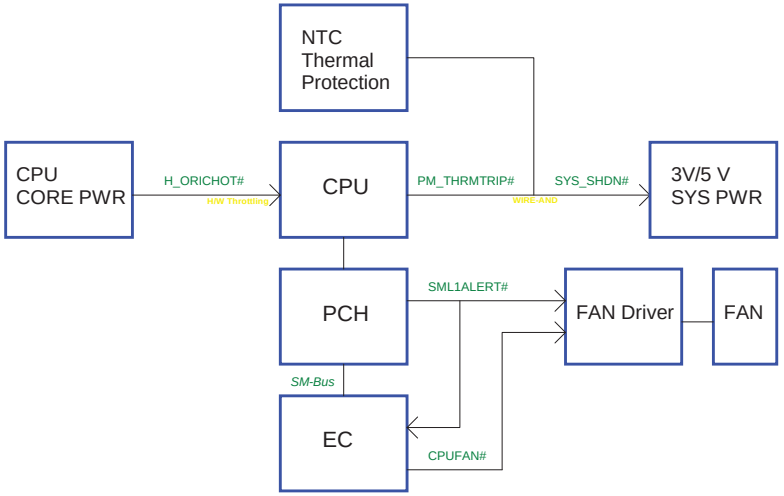
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



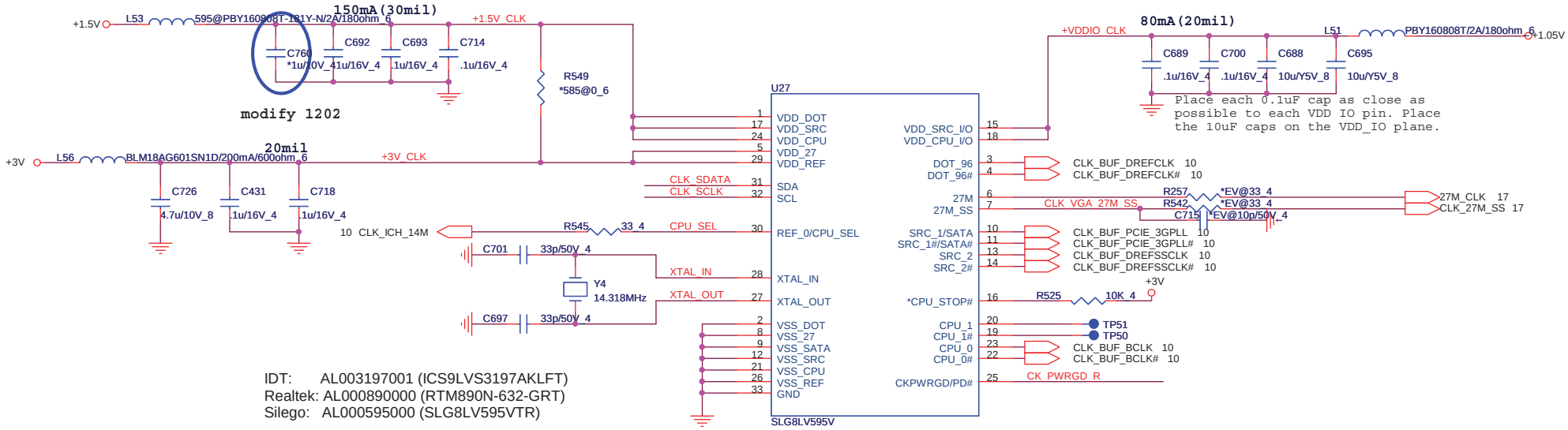
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/PCH	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT	MAINON	S0
+3V	+3.3V	CLK GEN/PCH/GPU/LVDS/Mini card/Codec/card reader	MAINON	S0
+1.5V_SUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+3V_D	+3.3V	I/O POWER for 3.3V pins	dGPU_VRON	Discrete enable
+VGPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+VGPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable

Thermal Follow Chart

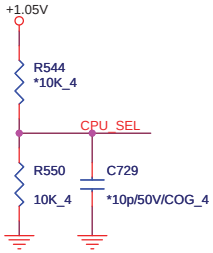


Quanta Computer Inc.
PROJECT : ZYD
Size: Document Number: PWR Status & GPU PWR CRL & THRM
Rev: 3B
Date: Tuesday, April 06, 2010
Sheet 2 of 50



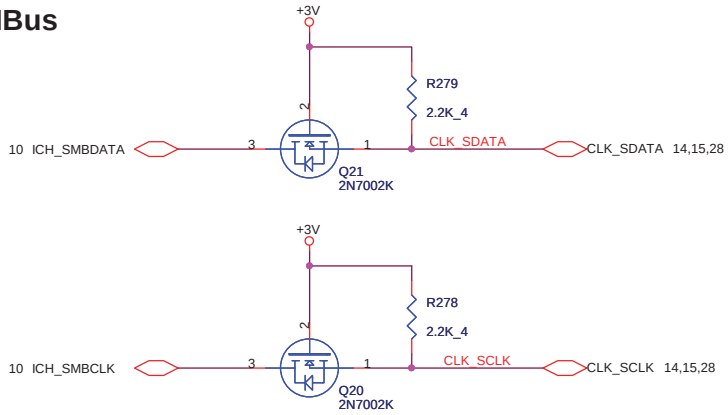
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

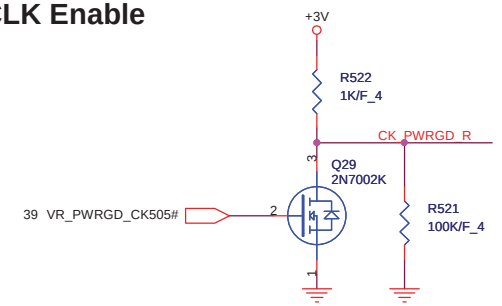


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



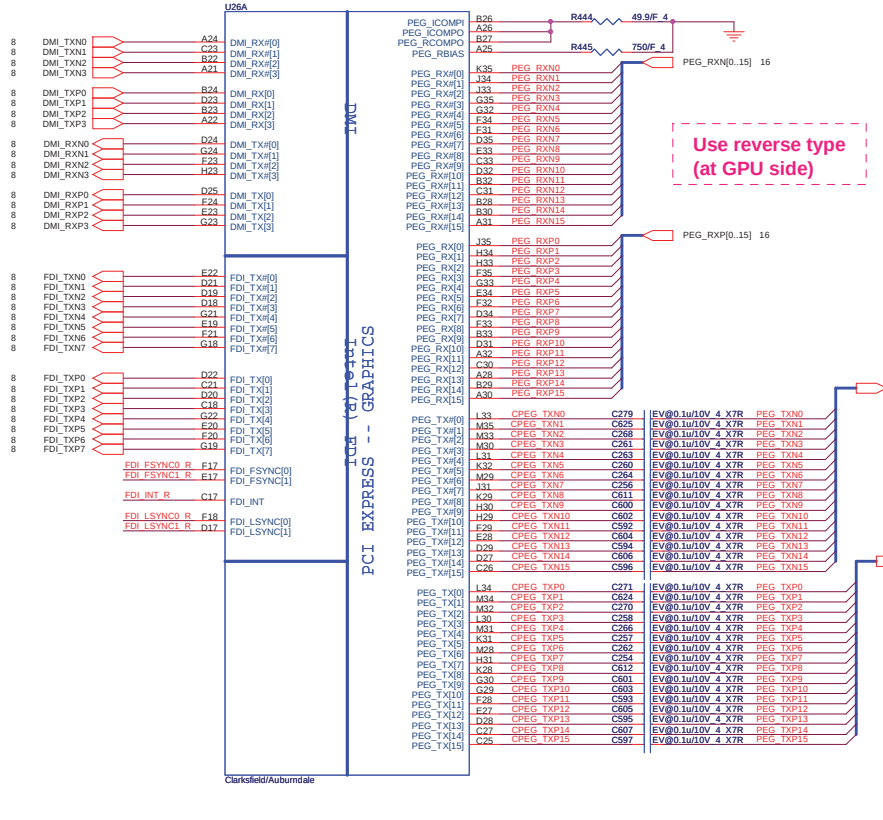
CLK Enable



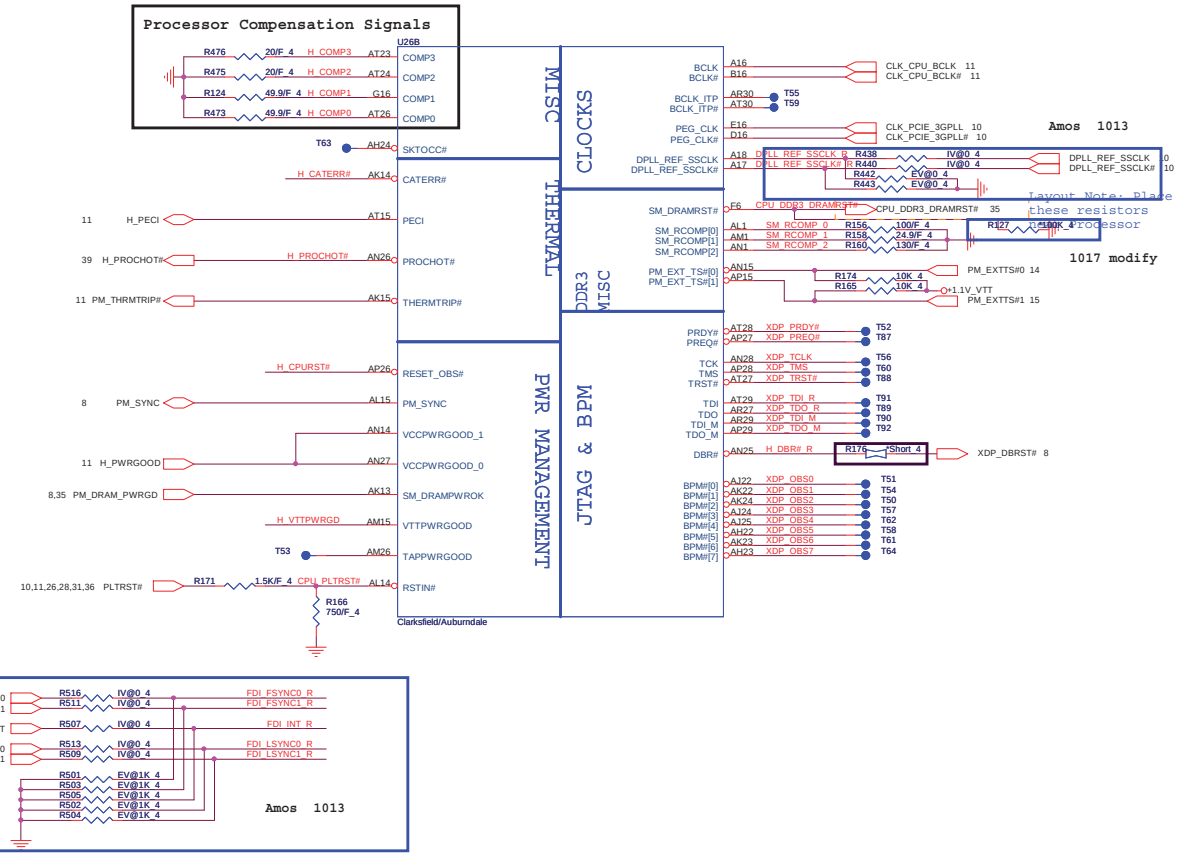
Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Clock Generator	3B
Date: Tuesday, April 06, 2010	Sheet 3 of 50	

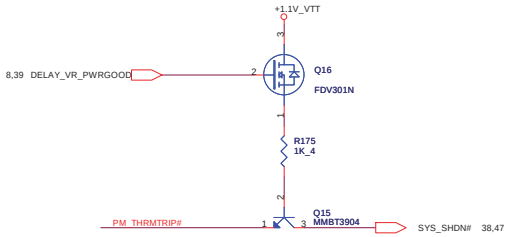
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



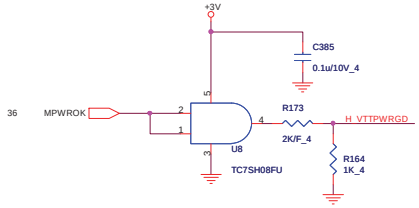
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



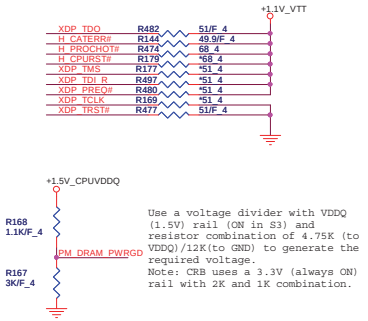
Thermaltrip protect



VTT PWR_Good

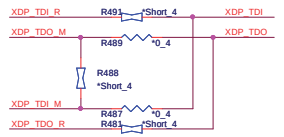


Processor pull-up



PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

JTAG MAPPING

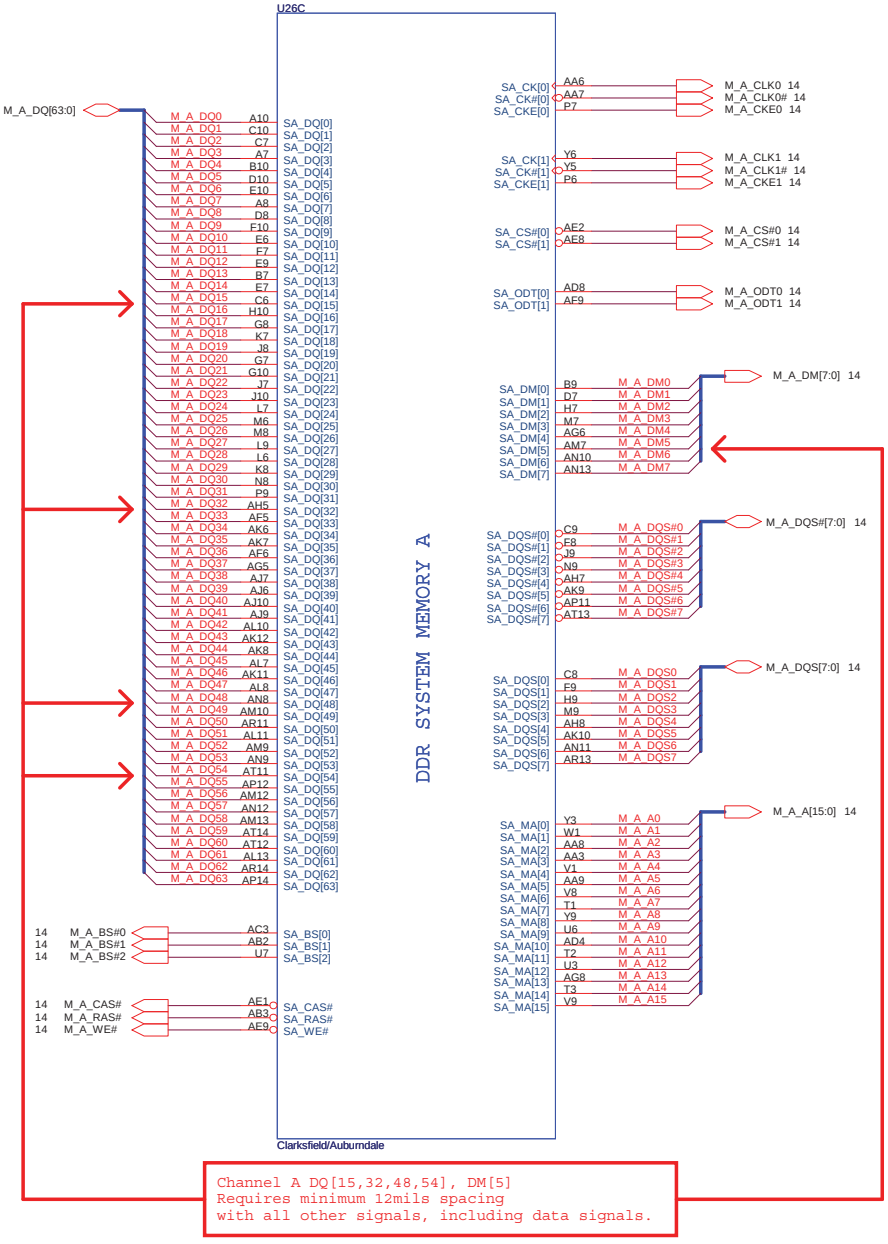


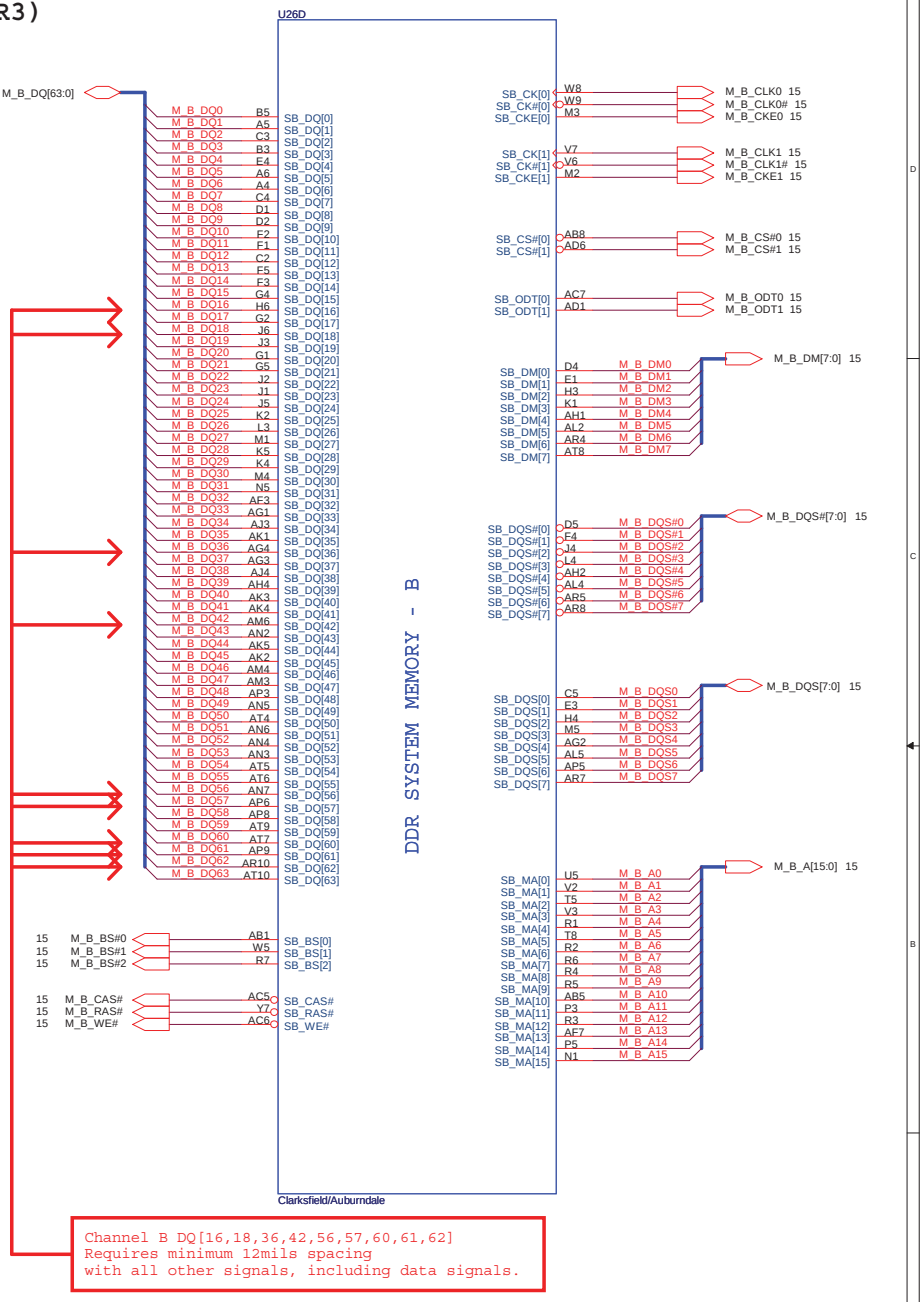
Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

Quanta Computer Inc.
PROJECT : ZYD

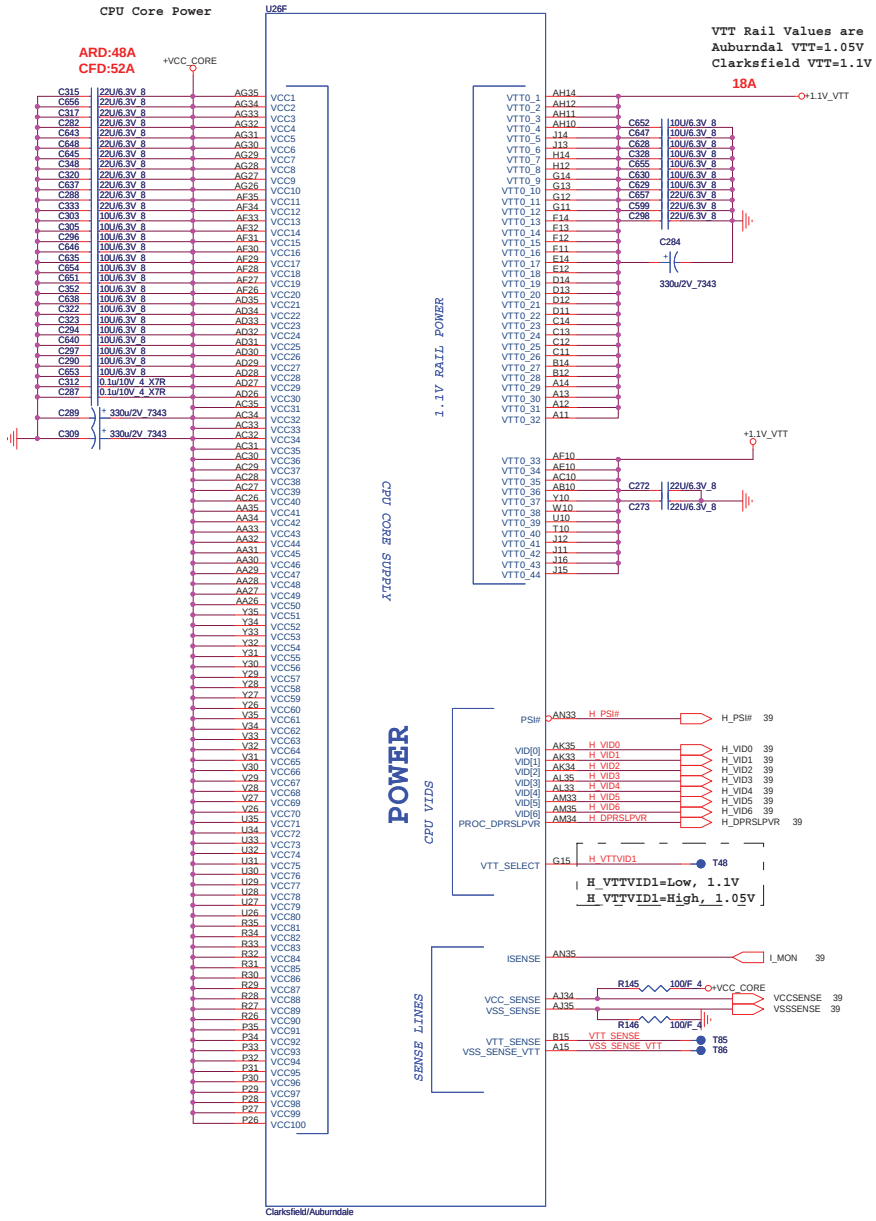
Size	Document Number	Rev
	AUBURNDA 1/4	3B
Date: Tuesday, April 06, 2010	Sheet 4 of 50	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

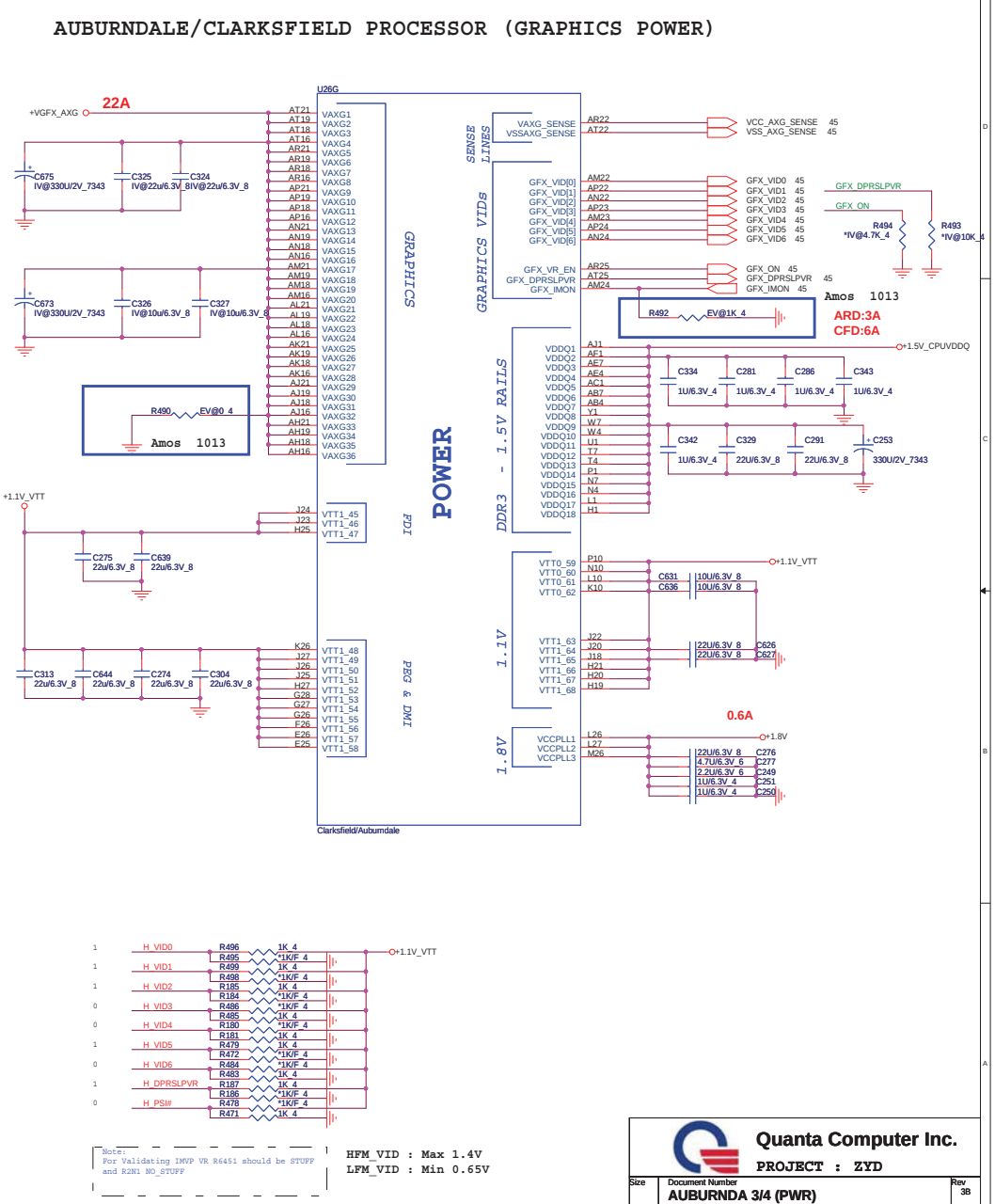




Quanta Computer Inc.			
PROJECT : ZYD			
Size	Document Number		Rev
	AUBURNDALE 2/4		3B
Date: Tuesday, April 06, 2010		Sheet 5 of 50	

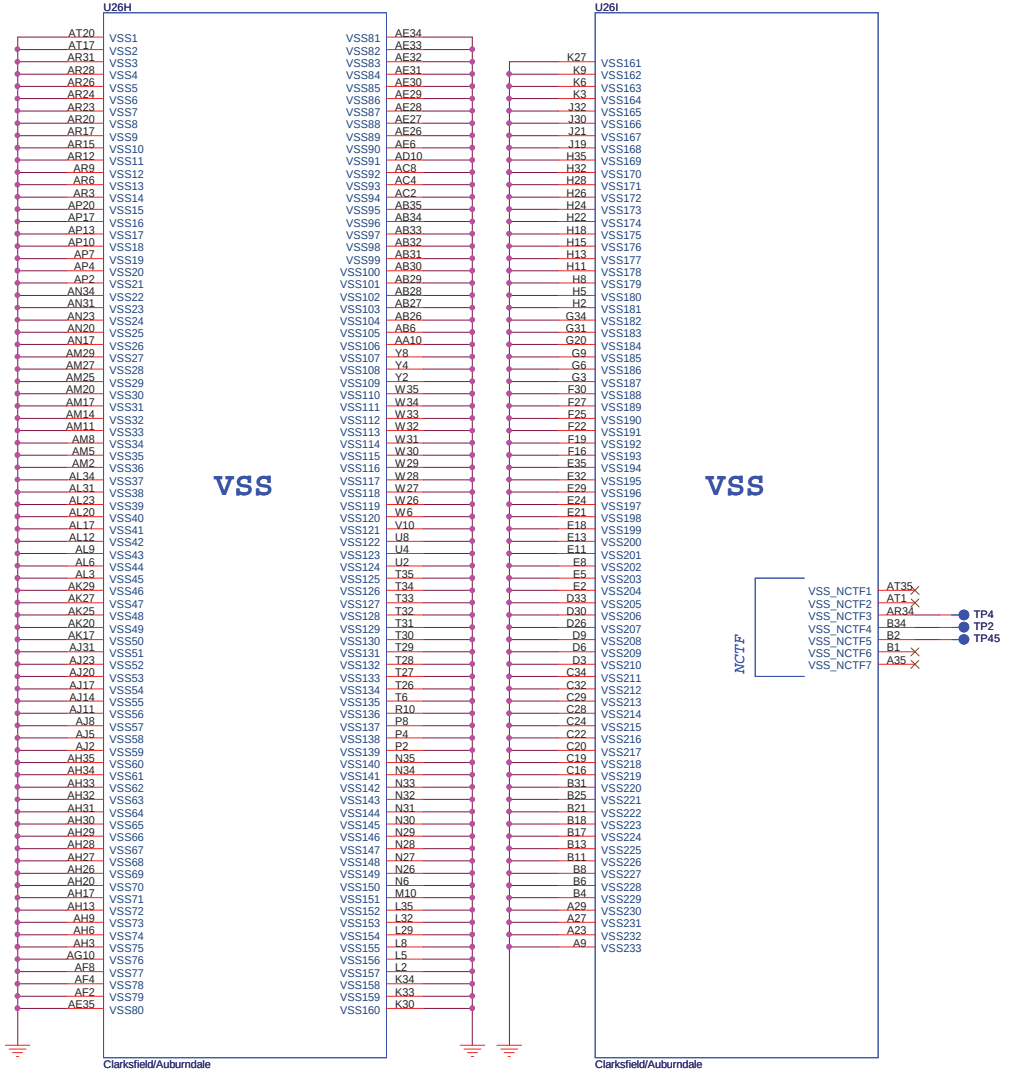


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

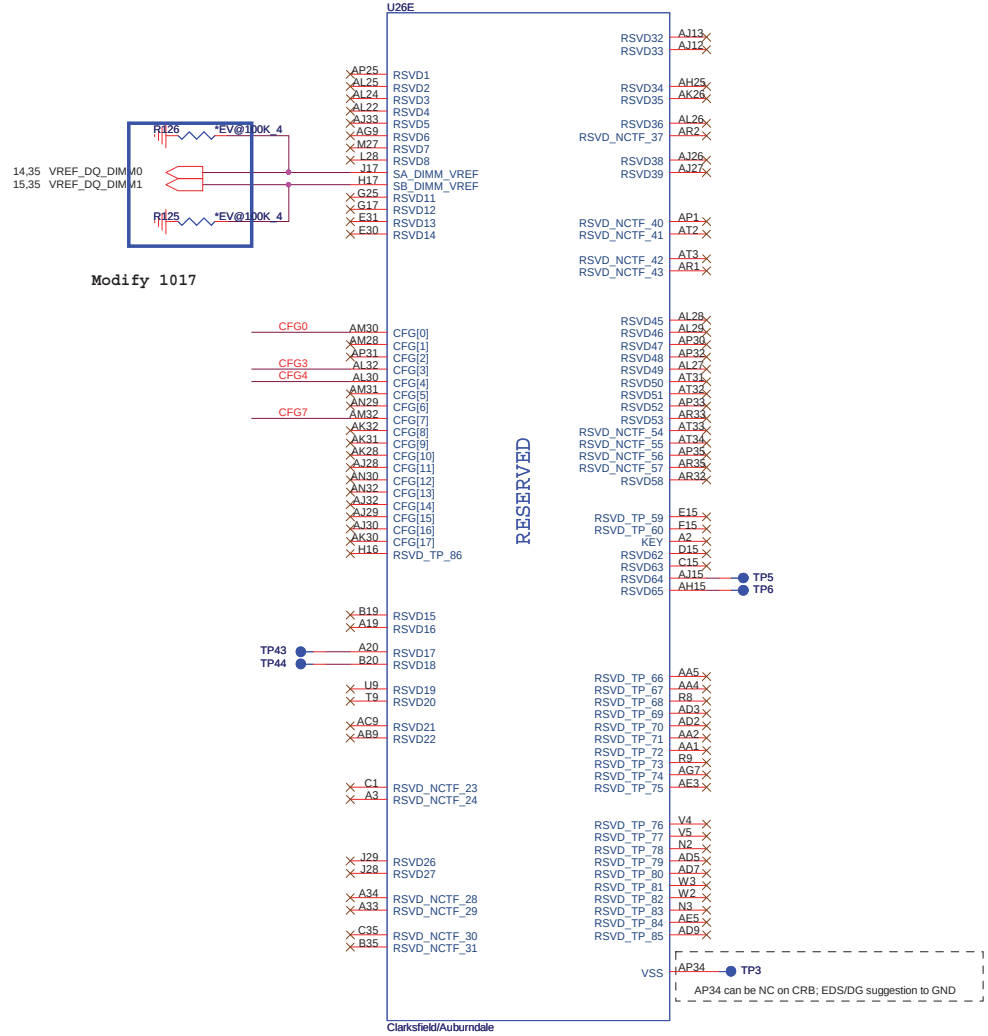


Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number: AUBURNDA 3/4 (PWR) | Rev: 3B
Date: Tuesday, April 06, 2010 | Sheet 6 of 50

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



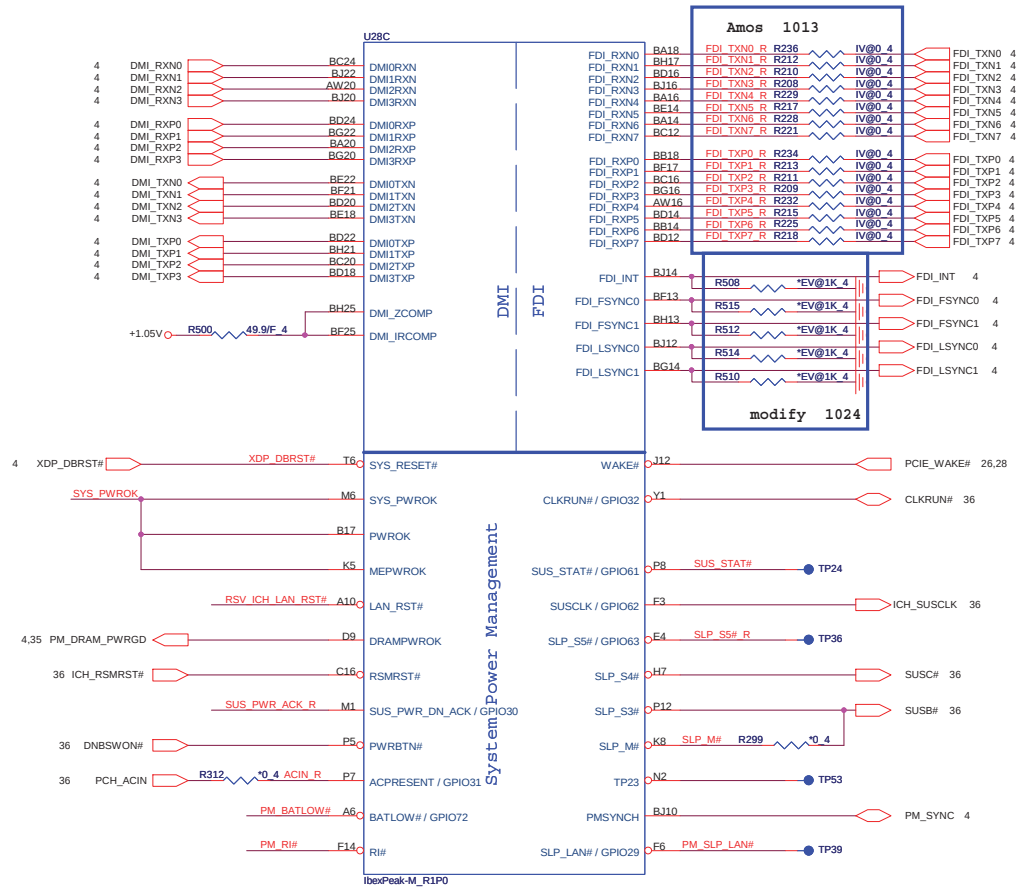
Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R172 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R159 *3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R157 *3.01K
Thermal Sensor Address				CFG7 R161 *3.01K/F_4

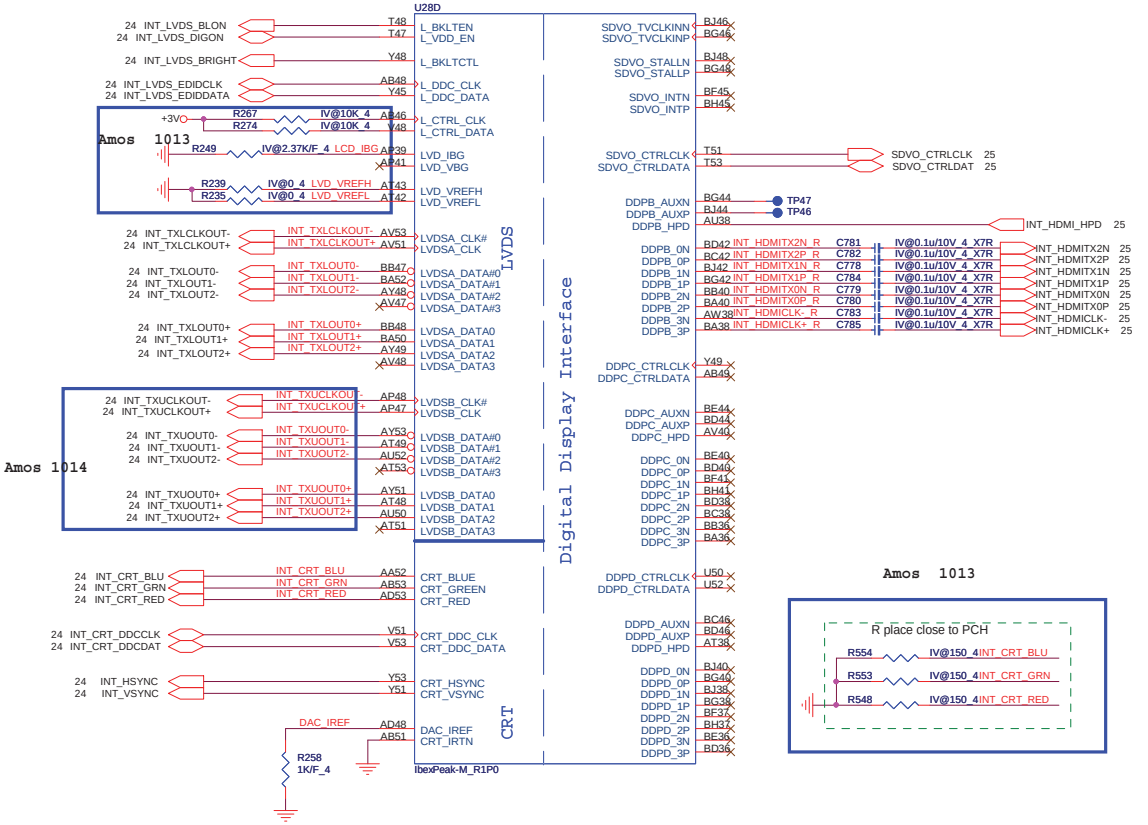
Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	AUBURNDA 4/4	3B
Date: Tuesday, April 06, 2010	Sheet 7 of 50	

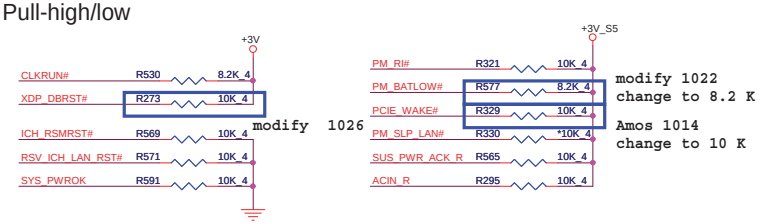
IBEX PEAK-M (DMI,FDI,GPIO)



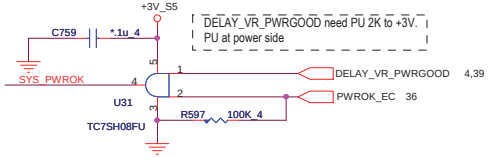
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



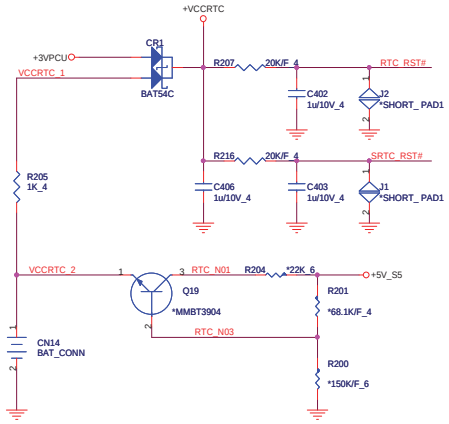
Quanta Computer Inc.

PROJECT : ZYD

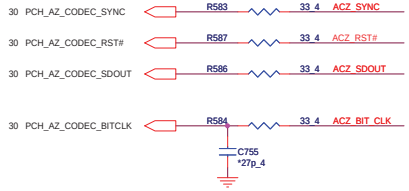
Size	Document Number	Rev
	IBEX PEAK-M 1/6	3B

Date: Tuesday, April 06, 2010 Sheet 8 of 50

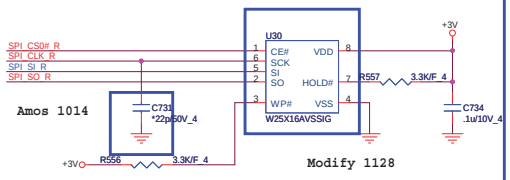
RTC Circuitry



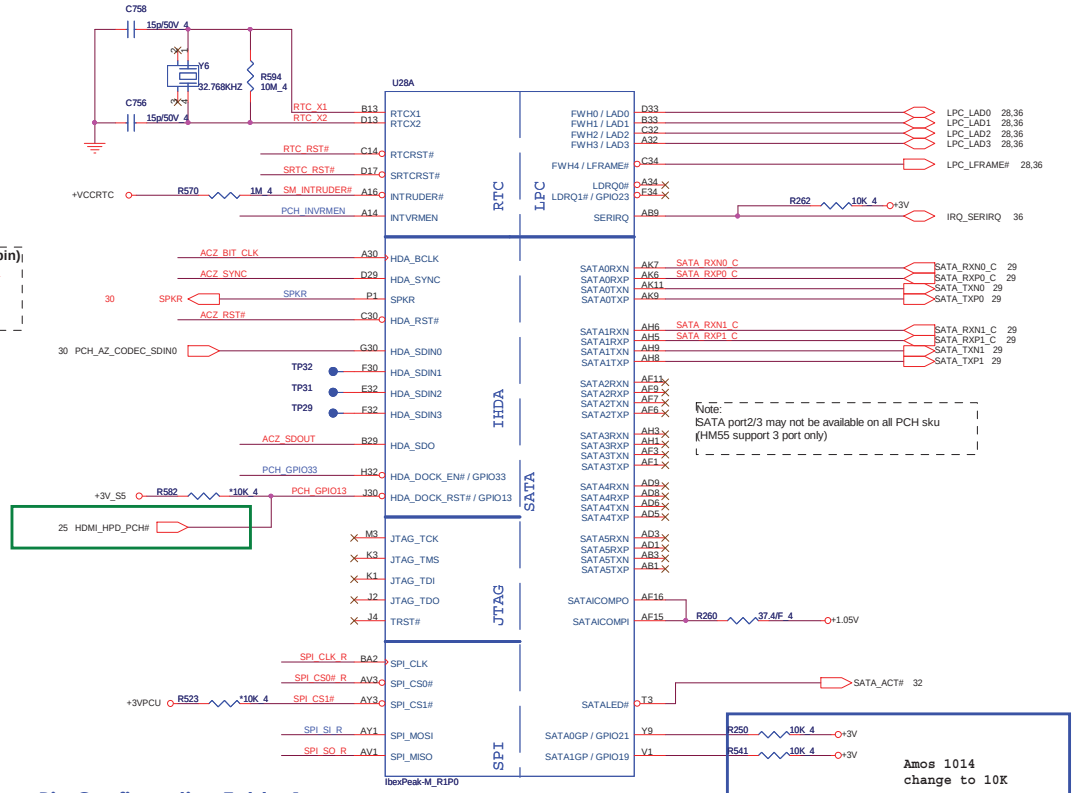
HDA Bus



MDC Bus



PCH SPI

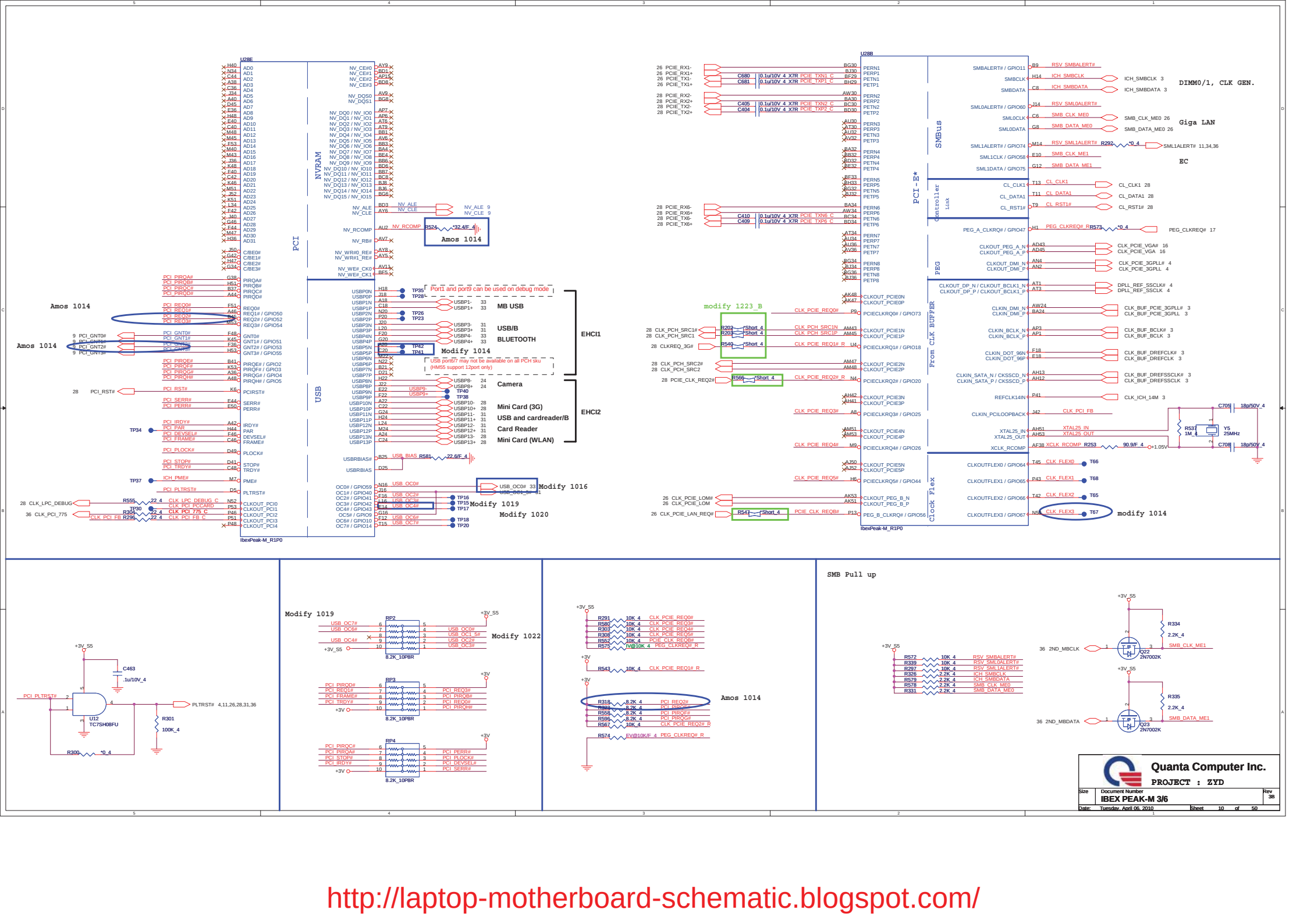


PCH Strap Pin Configuration Table-1

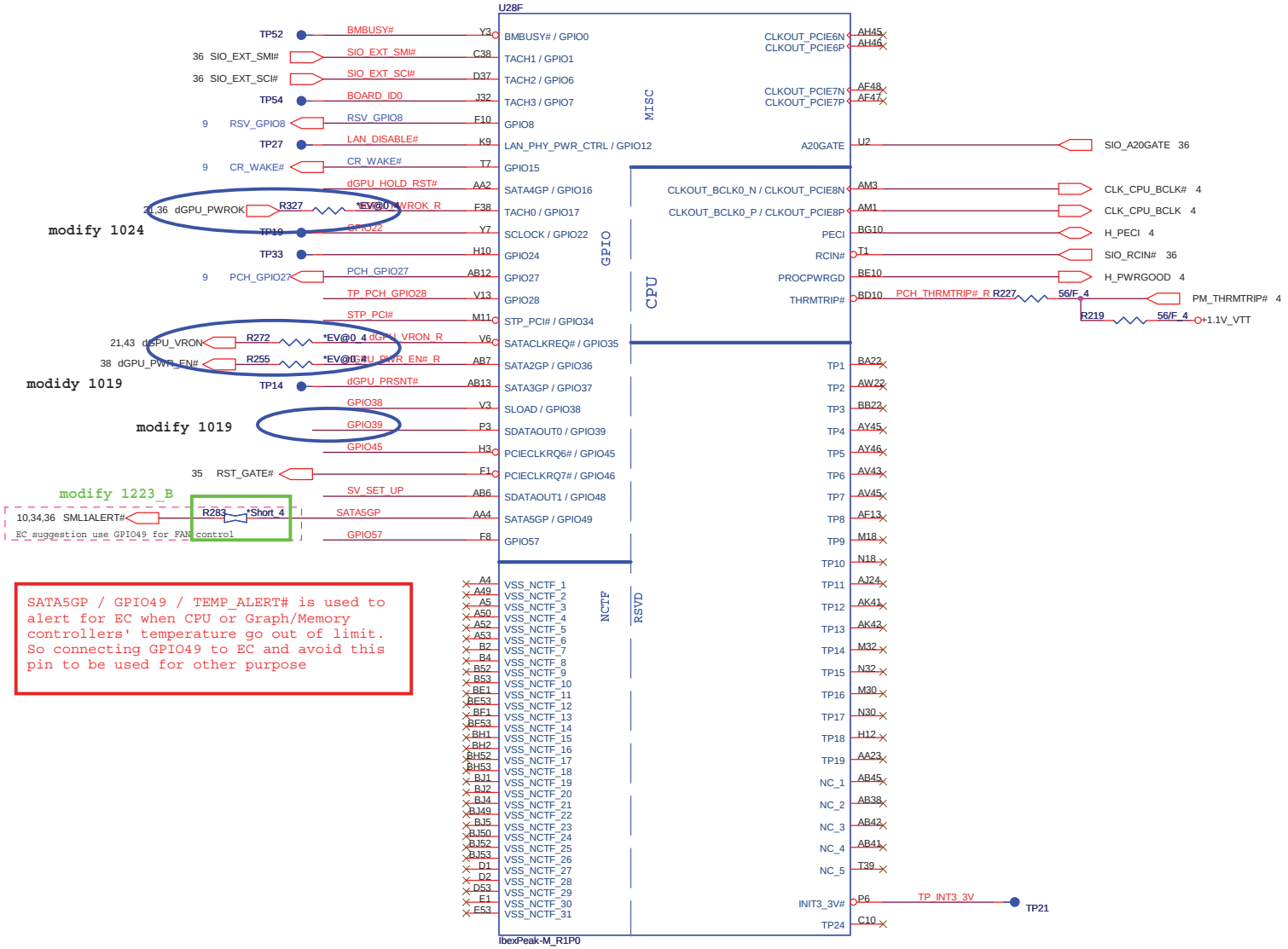
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R559 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R307 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J3 *SHORT_PAD1 R322 10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCI_GNT0# R315 1K_4 10 PCI_GNT1# R310 1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only Modify 1019	10 PCI_GNT2# R313 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCI_GNT3# R560 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R231 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R230 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 R325 10K_4 +3V_S5 R320 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# R282 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R263 *10K_4

Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number: IBEX PEAK-M 2/6 | Rev: 3B
Date: Tuesday, April 06, 2010 | Sheet 9 of 50

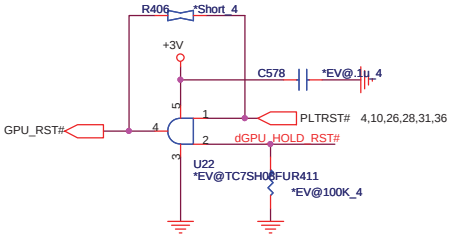


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

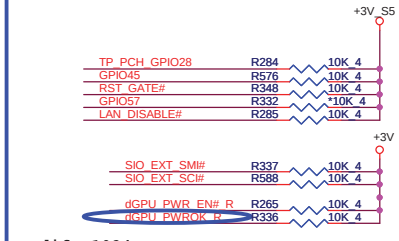


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

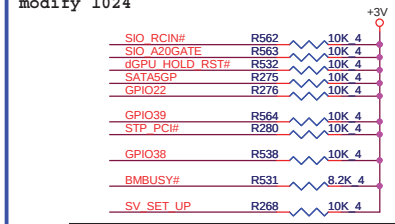
GPU RST#



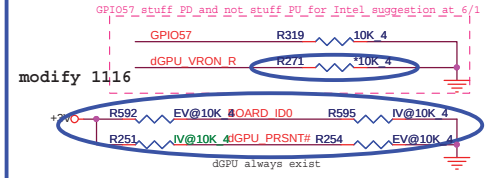
GPIO Pull-up/Pull-down



modify 1024



SV_SET_UP	1-X High = Strong (Default)



modify 1116

modify 1116

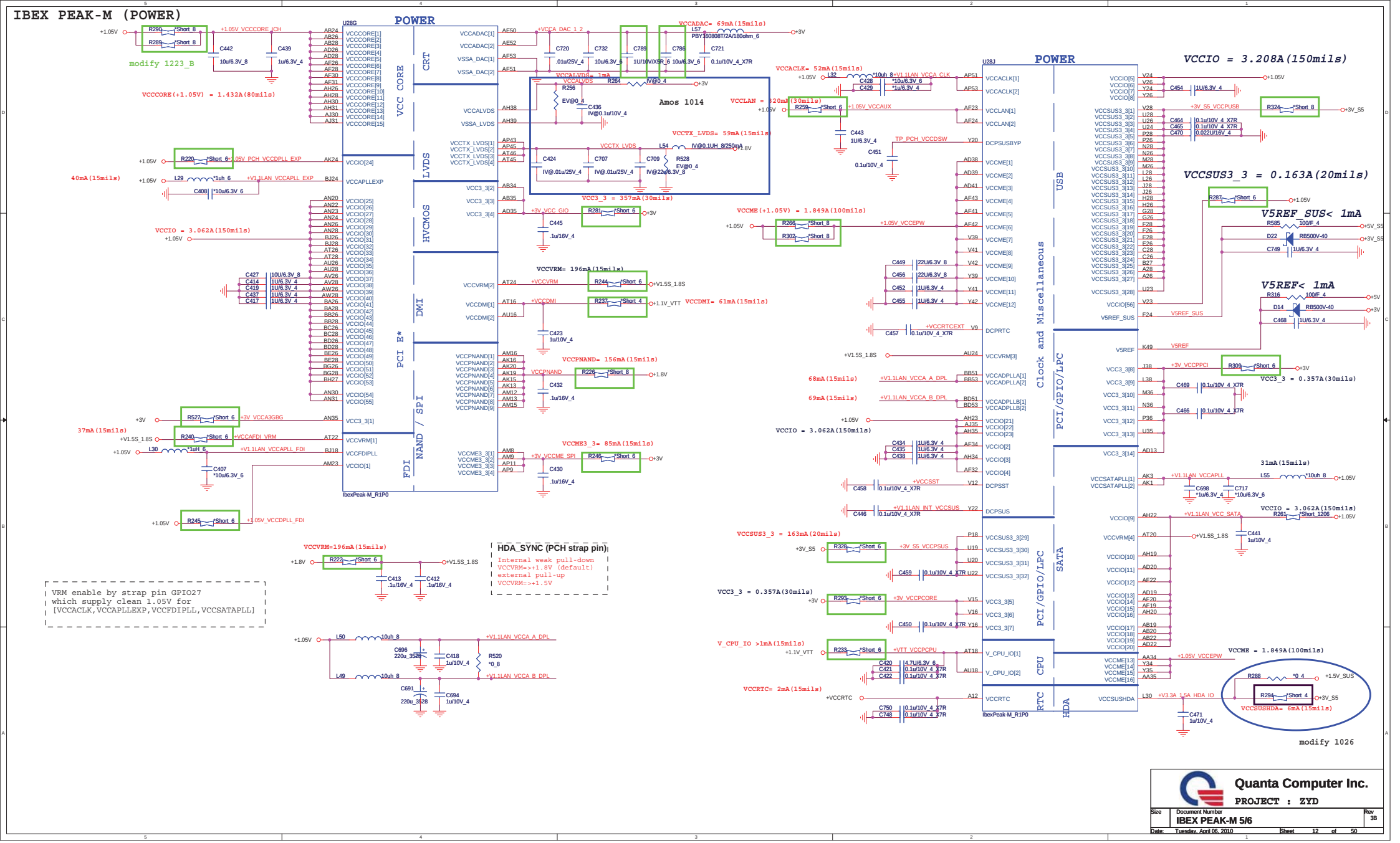
Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = IV
RSV_GPIO8	High = Disable Low = Enable

Quanta Computer Inc.

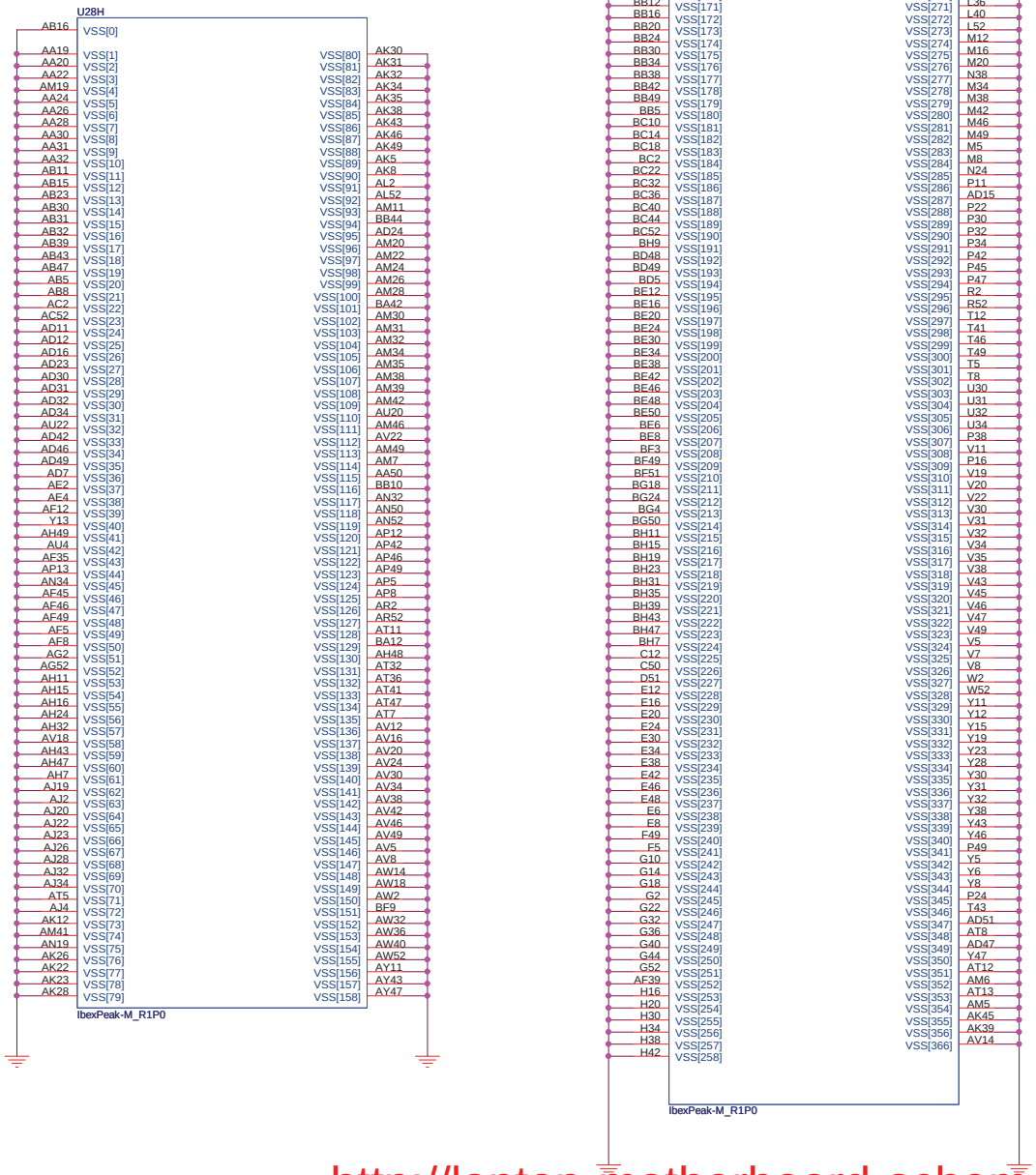
PROJECT : ZYD

Size	Document Number	Rev
	IBEX PEAK-M 4/6	3B

Date: Tuesday, April 06, 2010 Sheet 11 of 50



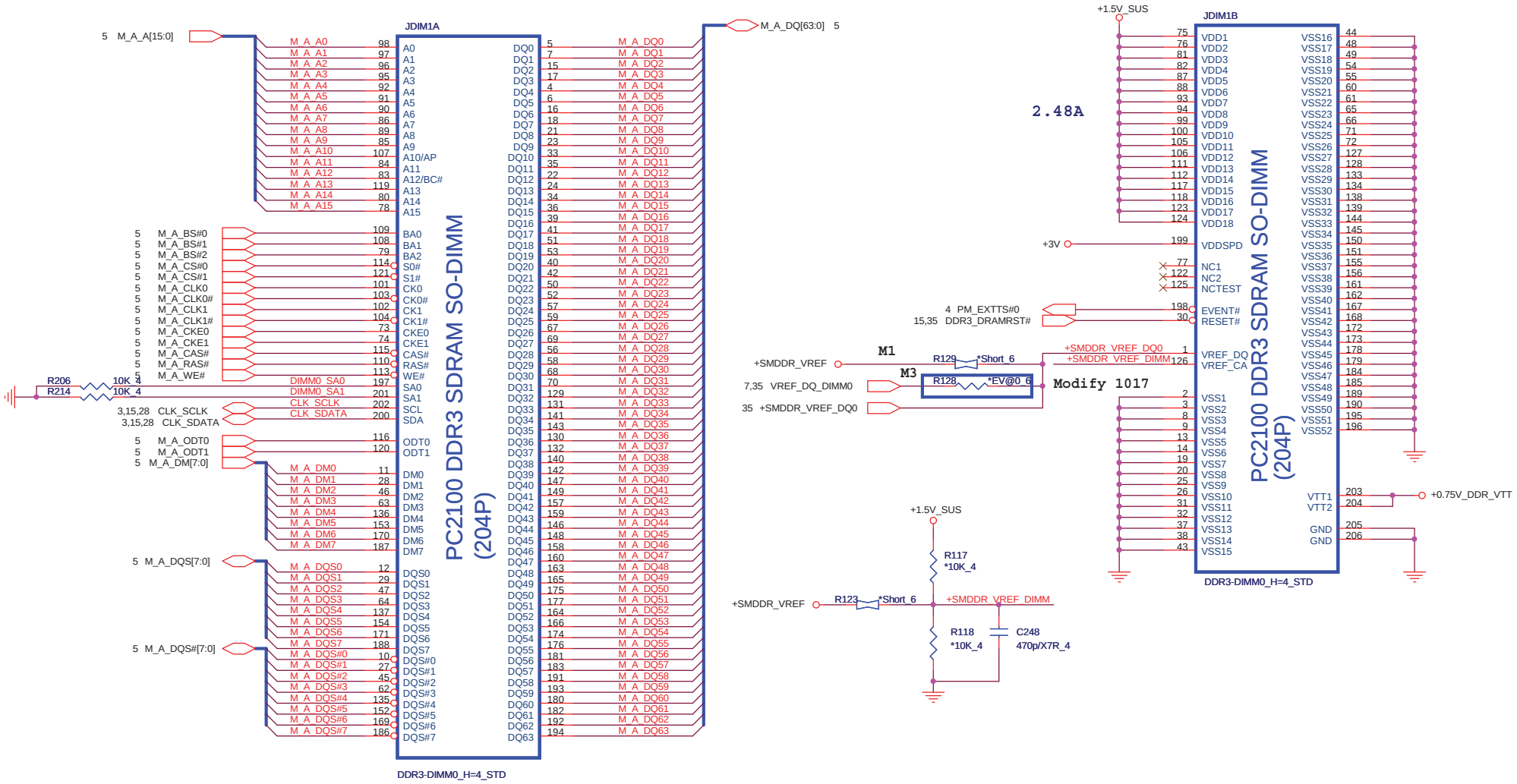
IBEX PEAK-M (GND)



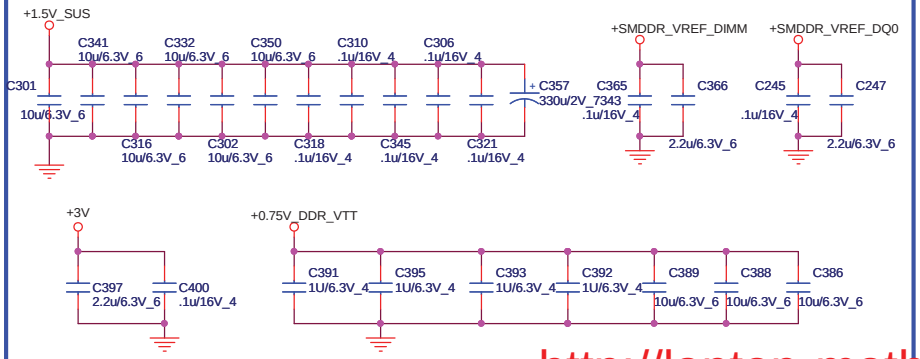
Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	IBEX PEAK-M 6 6	3B
Date: Tuesday, April 06, 2010	Sheet 13 of 50	



Place these Caps near So-Dimm0.



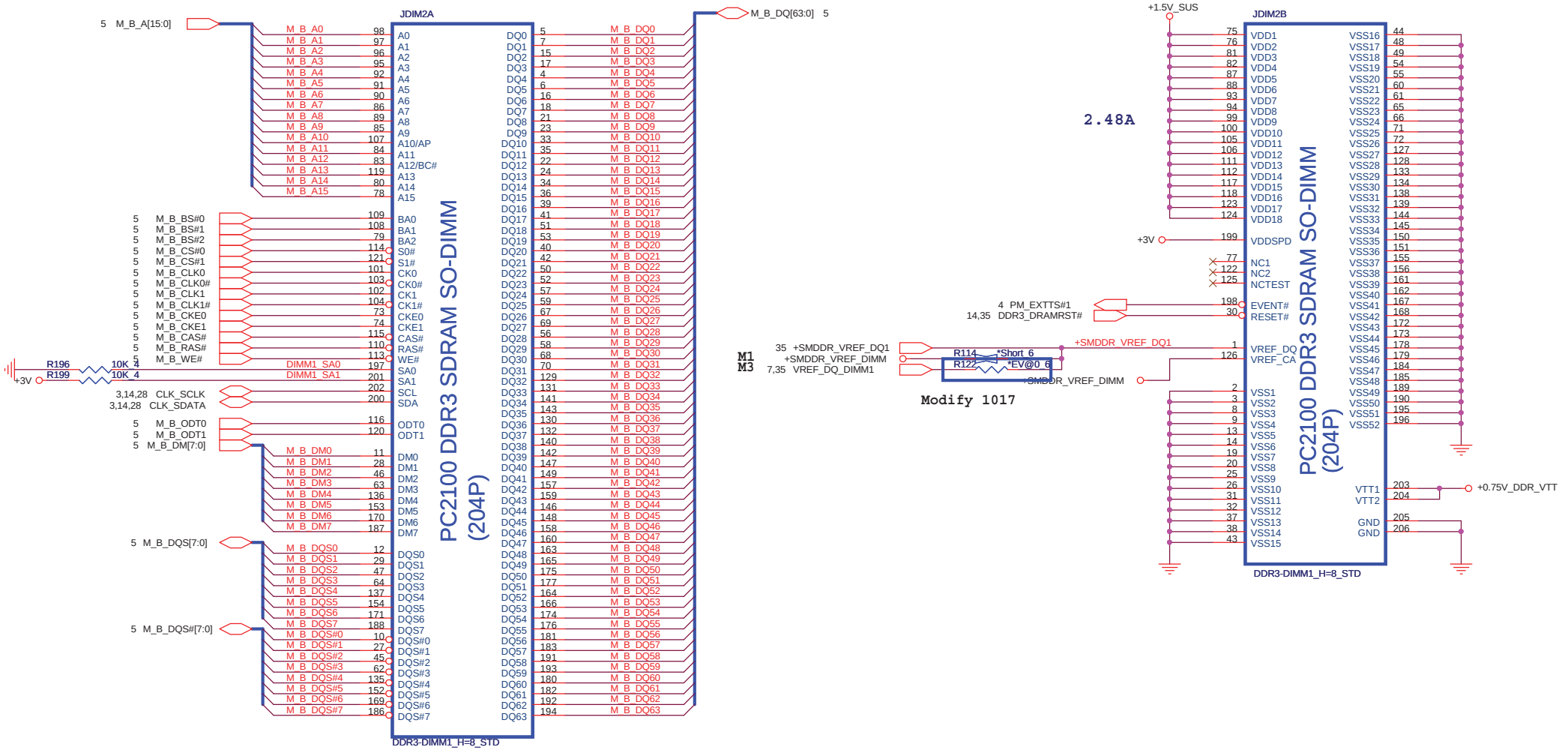
For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

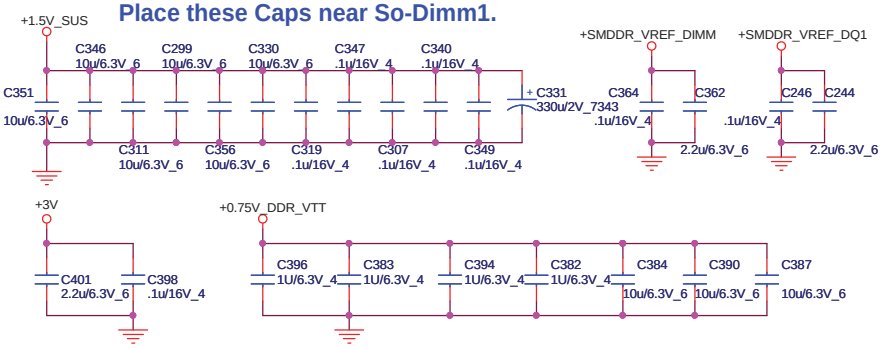
Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	DDRIII SO-DIMM-0	3B
Date: Tuesday, April 06, 2010	Sheet 14 of 50	

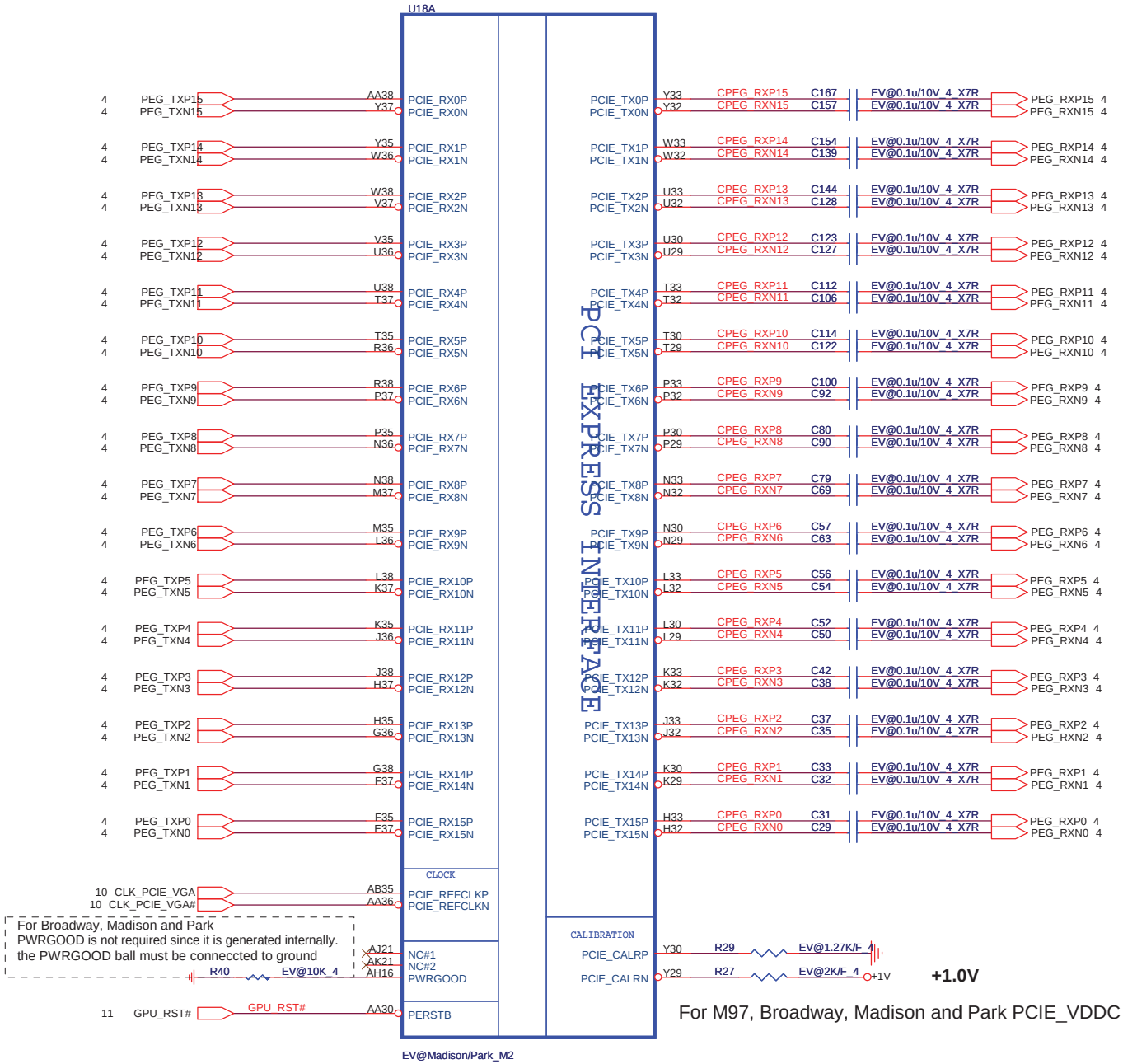


Place these Caps near So-Dimm1.




```
For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.
```

Quanta Computer Inc.			
PROJECT : ZYD			
Size	Document Number		Rev
	DDRIII SO-DIMM-1		3B
Date: Tuesday, April 06, 2010		Sheet 15 of 50	



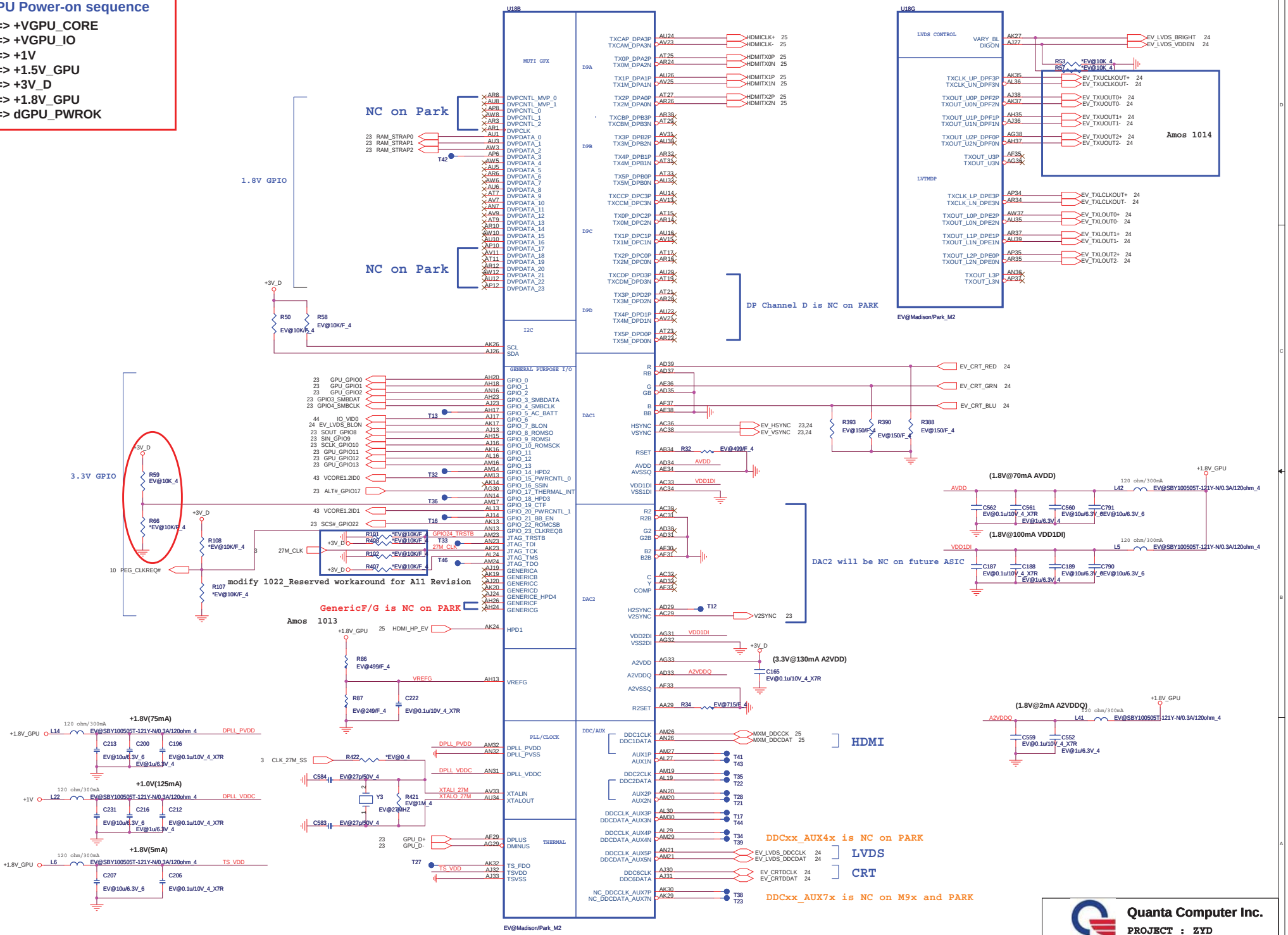
+1.0V

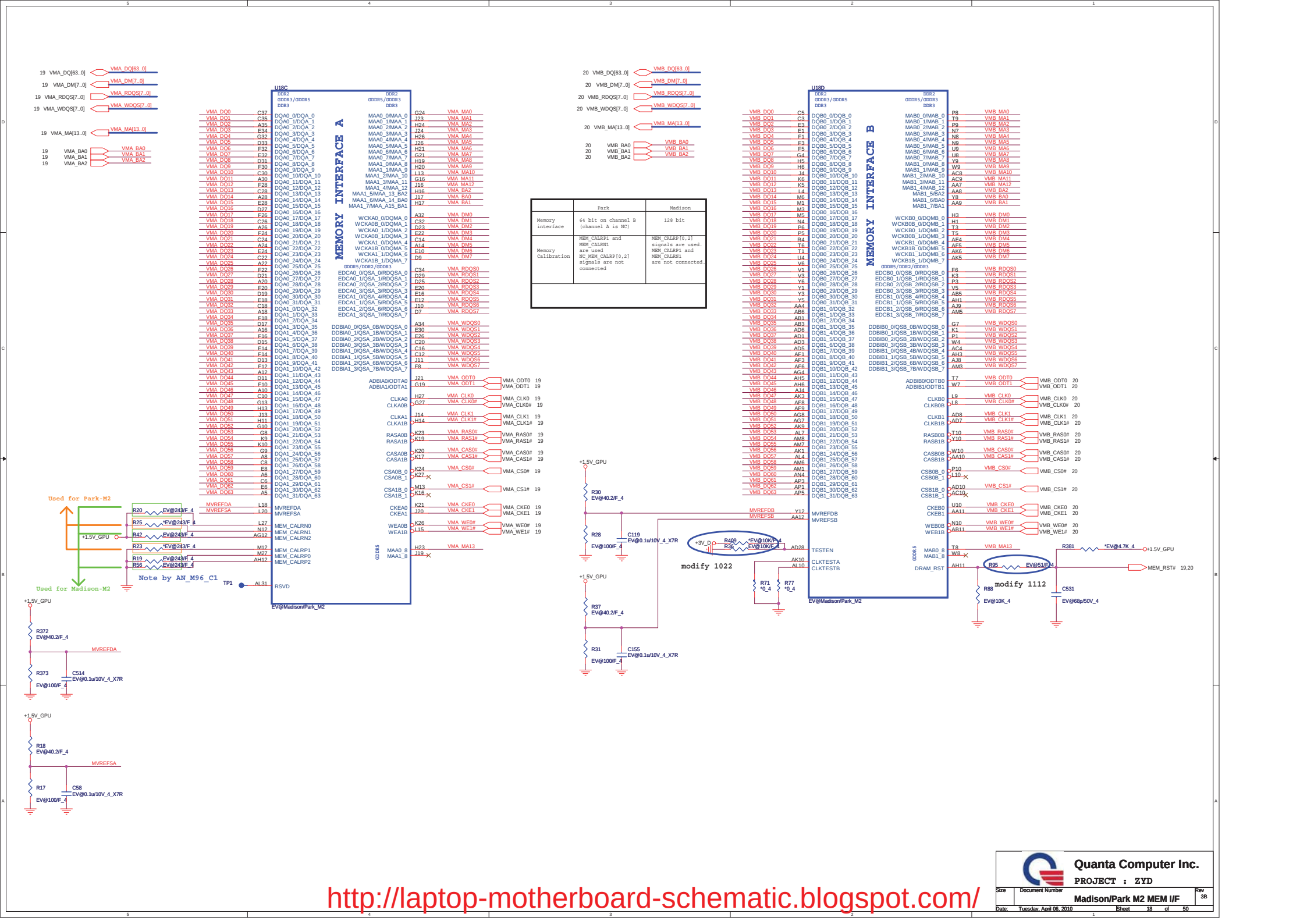
For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.			
PROJECT : ZYD			
Size	Document Number		Rev
	Madison/Park M2 PCIE I/F		3B
Date: Tuesday, April 06, 2010		Sheet 16 of 50	

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

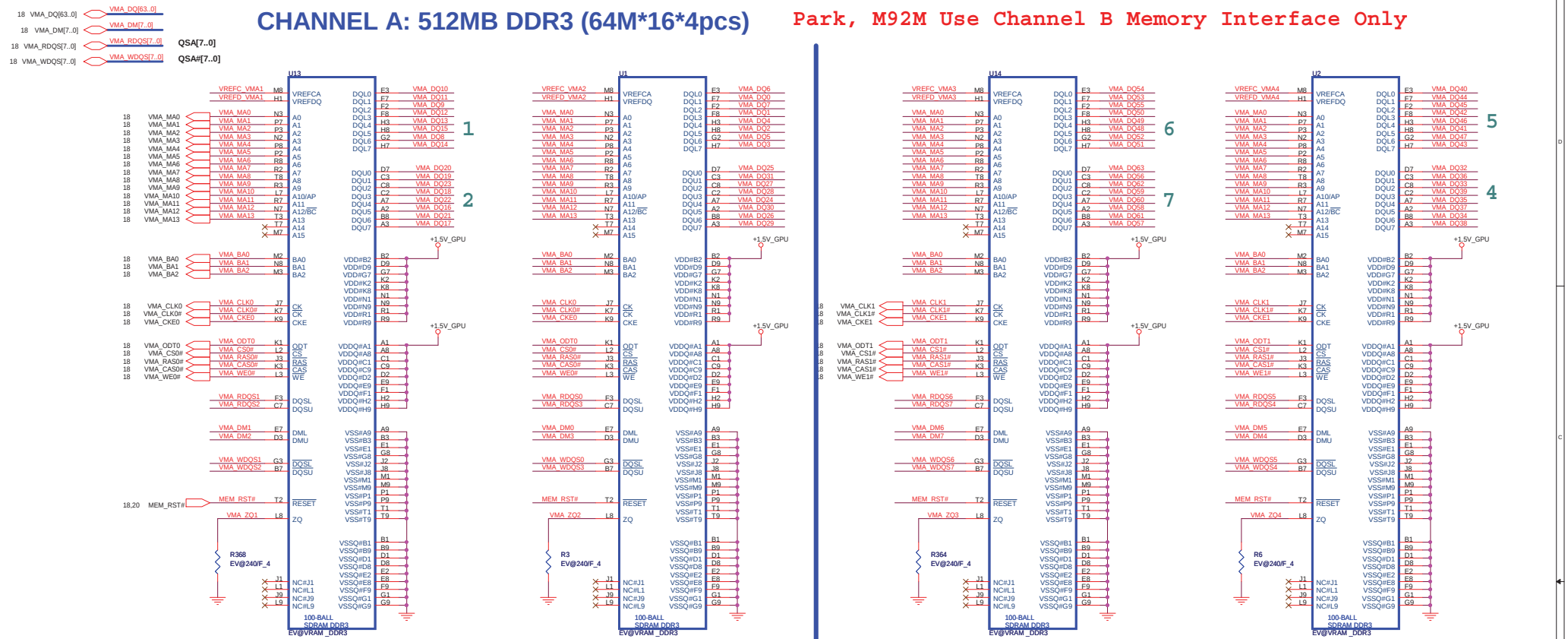




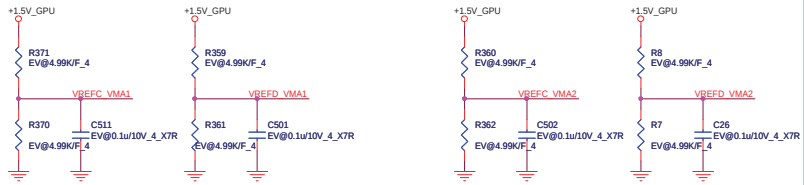
Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number | Rev 3B
Madison/Park M2 MEM I/F
Date: Tuesday, April 06, 2010 | Sheet 18 of 50

CHANNEL A: 512MB DDR3 (64M*16*4pcs)

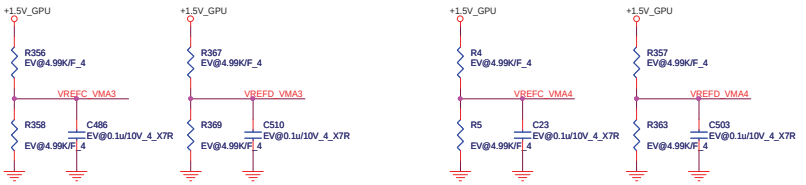
Park, M92M Use Channel B Memory Interface Only



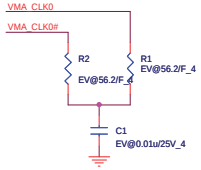
Group-A0 VREF



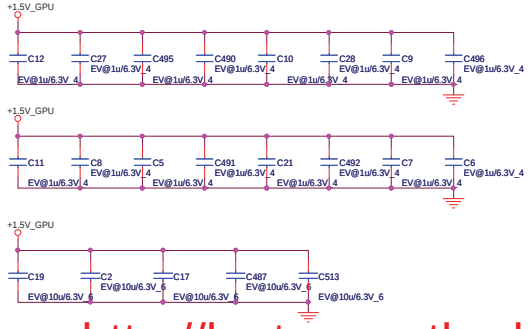
Group-A1 VREF



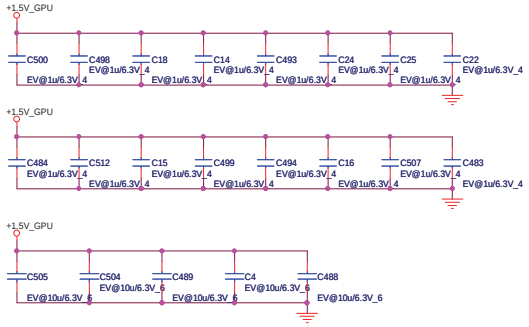
MEM_A0 CLK



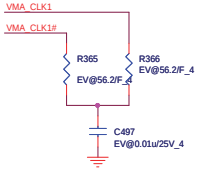
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

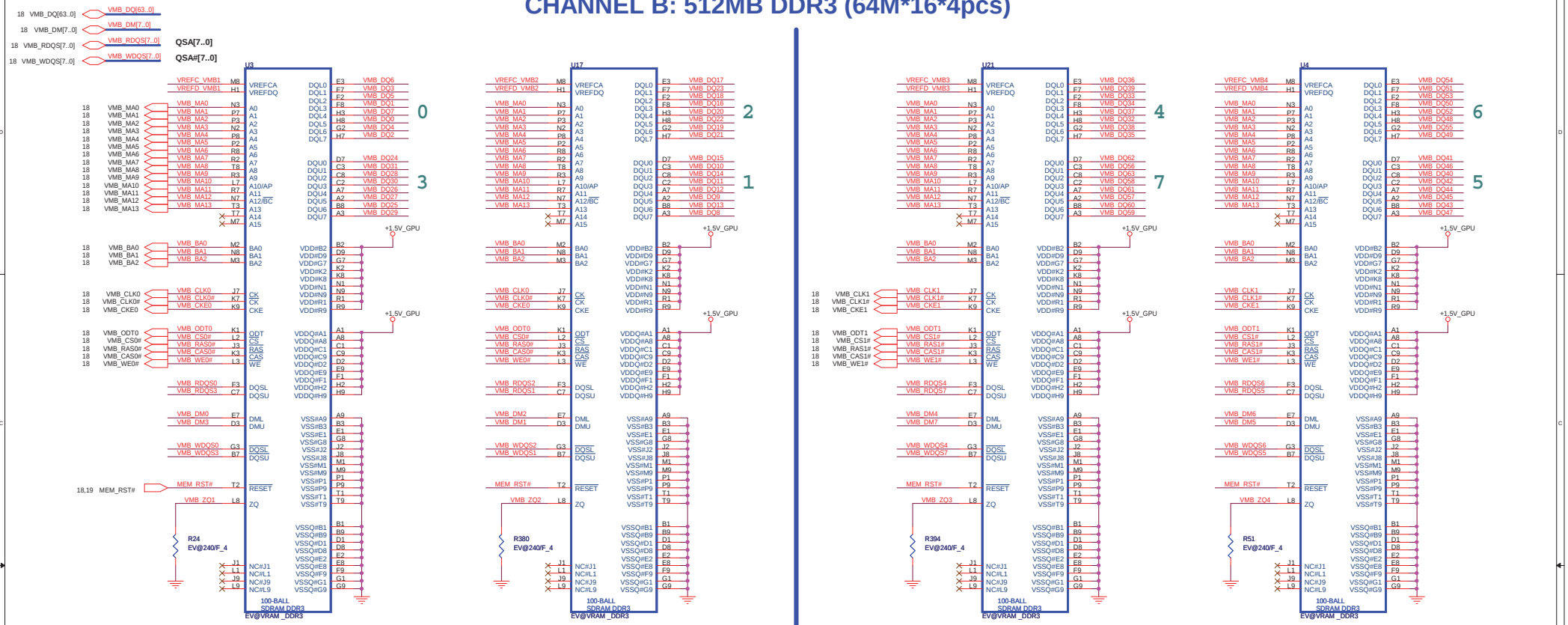


Quanta Computer Inc.

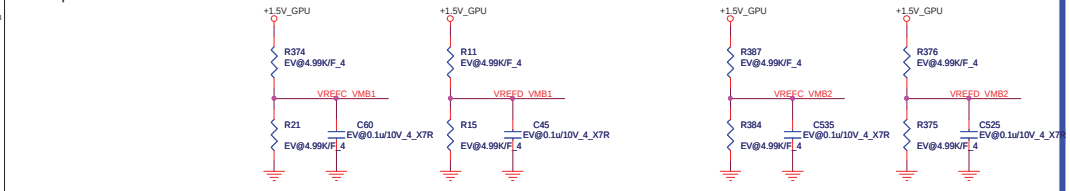
PROJECT : ZYD

Size	Document Number	Rev
	MEMORY 1 channel A	3B
Date: Tuesday, April 06, 2010	Sheet 19 of 50	

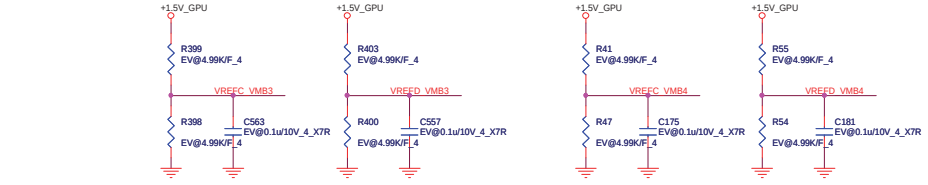
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



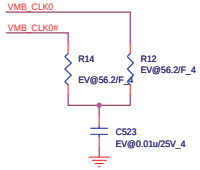
Group-B0 VREF



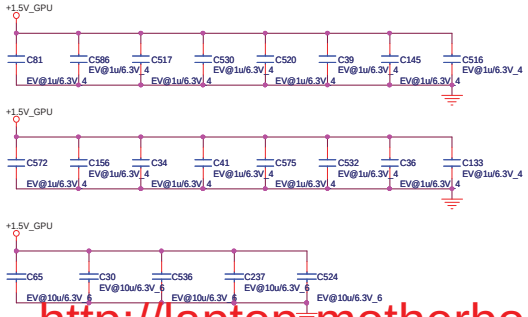
Group-B1 VREF



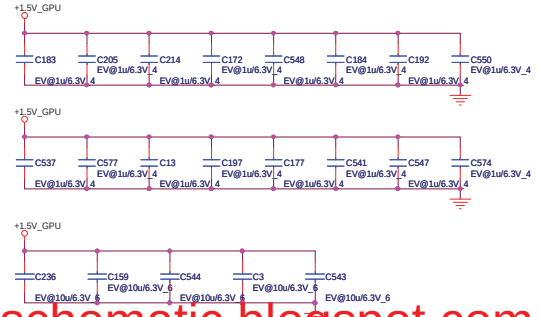
MEM_B0 CLK



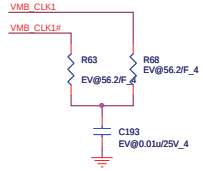
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	MEMORY 2 channel B	3B
Date: Tuesday, April 06, 2010	Sheet 20 of 50	

For DDR3, MVDDQ = 1.5V (7.5A)

+1.5V_GPU

U18E

MEM I/O

POWER

PCIE

CORE

LEVEL TRANSLATION

I/O

PLL

VOLTAGE SENSE

ISOLATED CORE I/O

(1.8V@110mA VDD_CT)

(3.3V@60mA))

(For M97, Broadway, Madison and Park SPV10 = 1.0V)

(1.8V@40mA PCIE_PVDD)

(1.8V@75mA/Park & 150mA/Madison MPV18)

(1.8V@75mA SPV18)

(1.0V@120mA SPV10)

EV@Madison/Park_M2

VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair

(1.8V@400mA PCIE_VDDR)

(1.0V@1.1A PCIE_VDDC)

(30A or more)

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
Connect to VDDC in non-PowerXpress designs.

PIN different between Broadway and Madison

Pin	Broadway	Madison
N27 T27	VDDC	BIF_VDDC

Modify 1022

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

VDDC and VDDCI are assigned to different sets of balls on M97, Madison and Park. As a result, VDDC and VDDCI will be shorted when a M96 is populated on a compatible design.

(DDR3 1.12V@4A VDDCI) or more

modify 1230_B

GND

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high "3.3V" will turn the regulators OFF. An output low "0V" will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

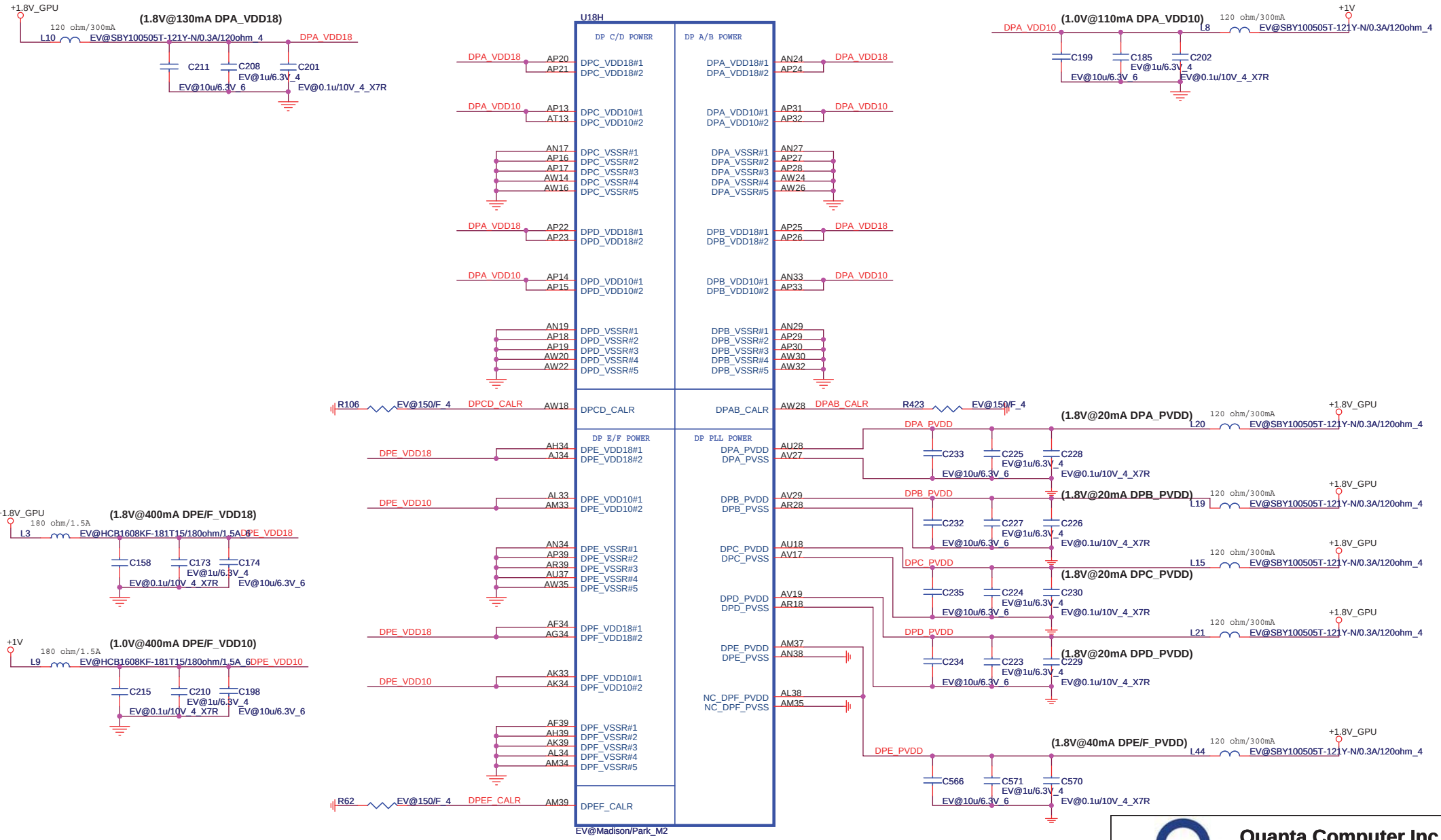
Modify 1022

GPU +3V power

GPU all PWROK

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 MEM I/F	3B
Date: Tuesday, April 06, 2010	Sheet 21 of 50	

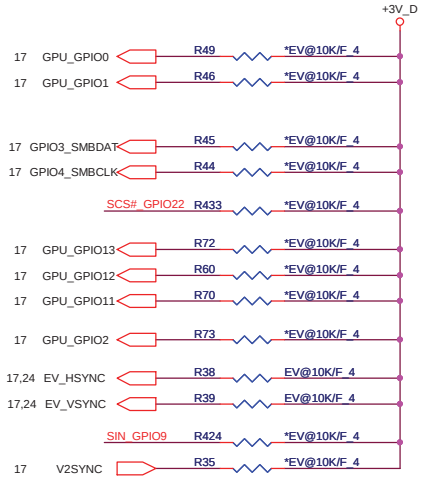


Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 DPPW_GND	3B
Date: Tuesday, April 06, 2010	Sheet 22 of 50	

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

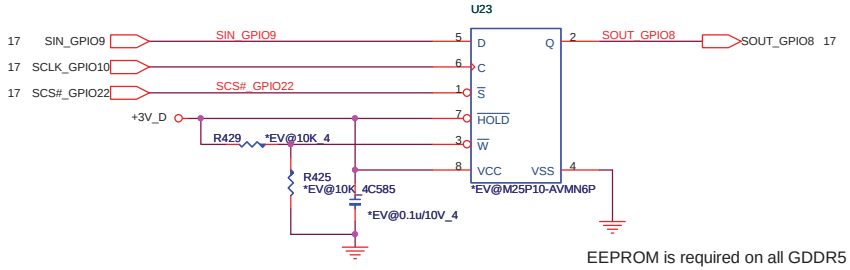
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

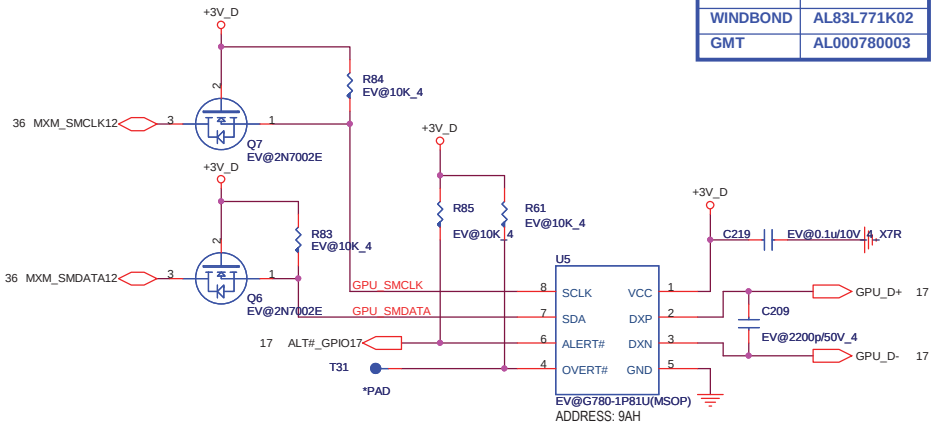
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



EEPROM is required on all GDDR5 designs

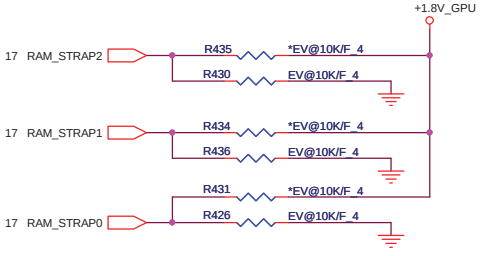
Thermal Sensor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

DDR3 Memory Aperture size

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	0	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700		0	1	0



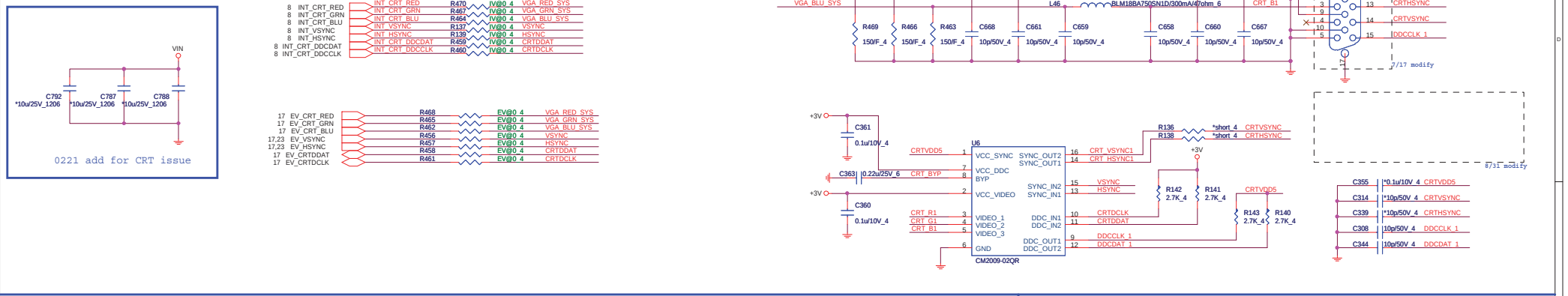
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.

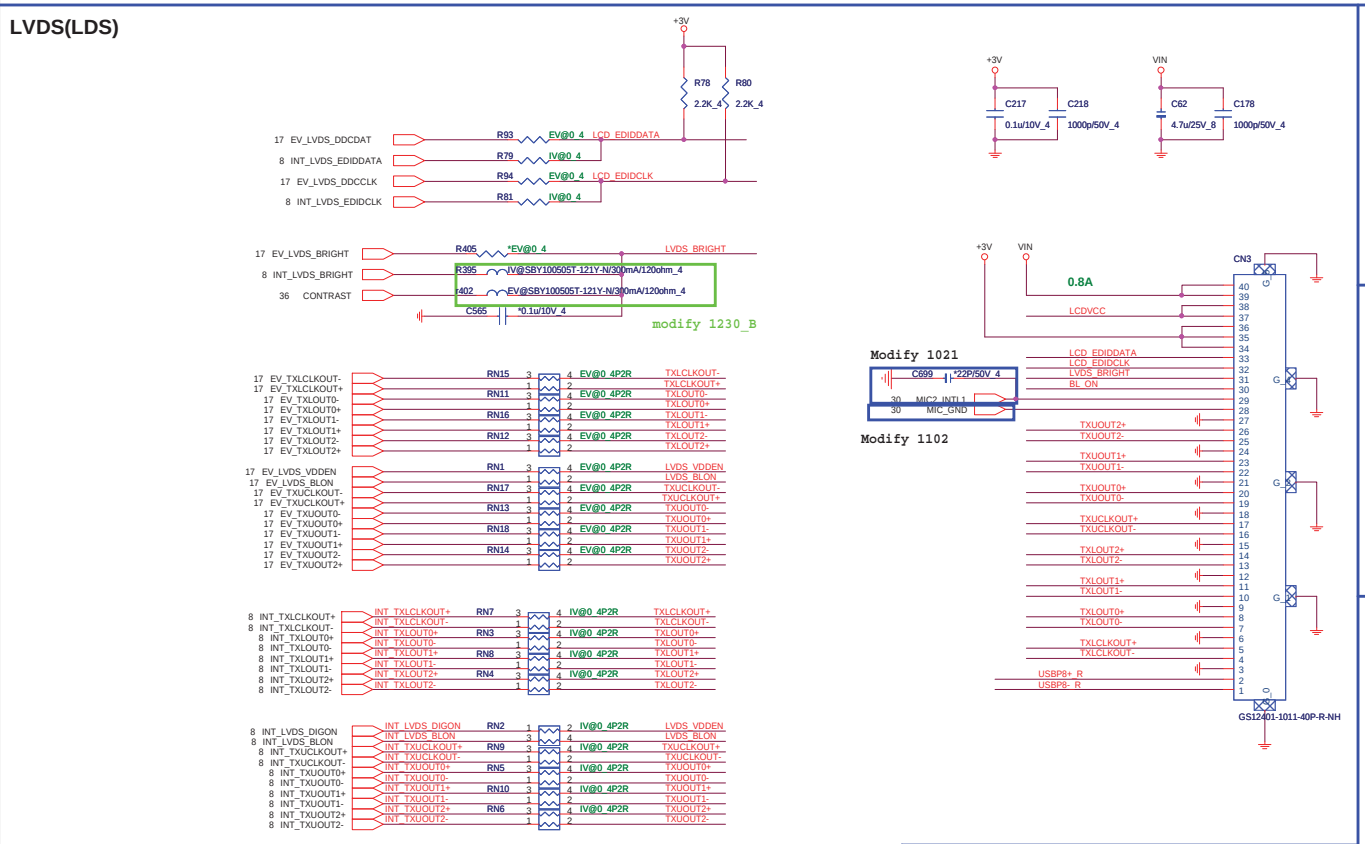
PROJECT : ZYD

Size	Document Number	Rev
	Strip/Thermal	3B
Date: Tuesday, April 06, 2010	Sheet 23 of 50	

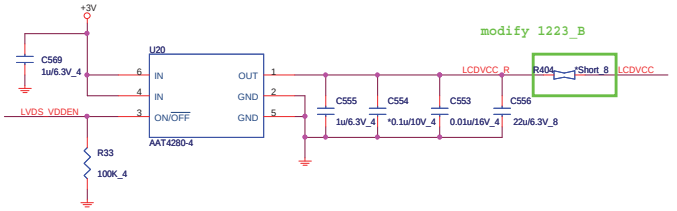
CRT(CRT)



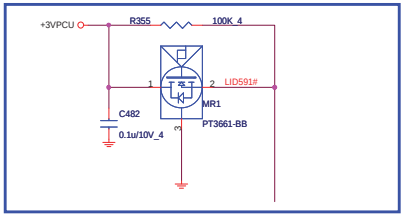
LVDS(LDS)



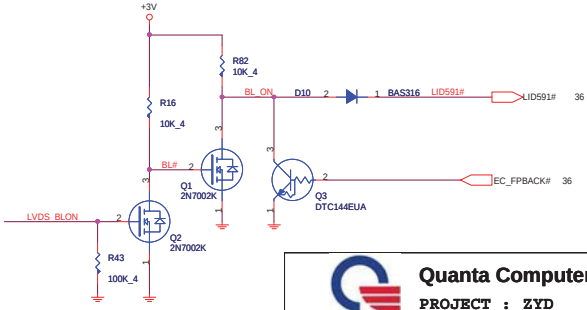
LCD Power(LDS)



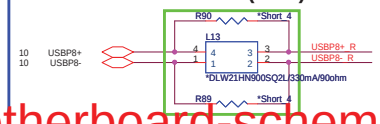
Hall Sensor(HSR)



Backlight Control(LDS)

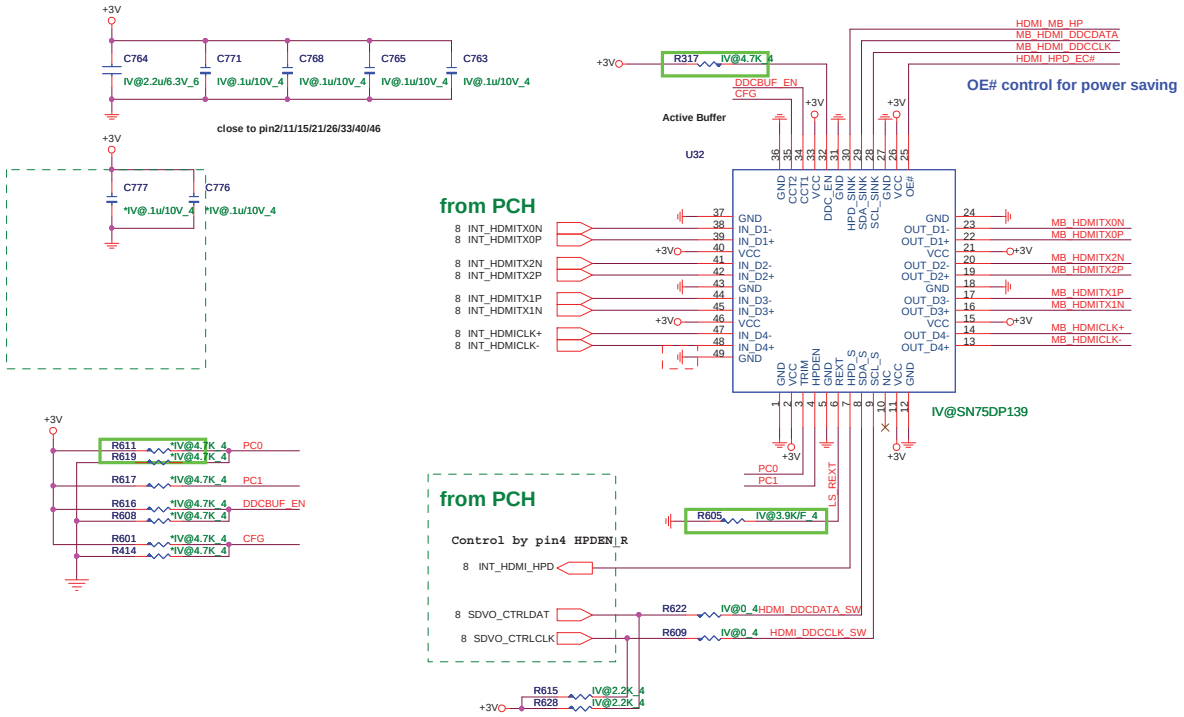


CAMERA Module(CCD)

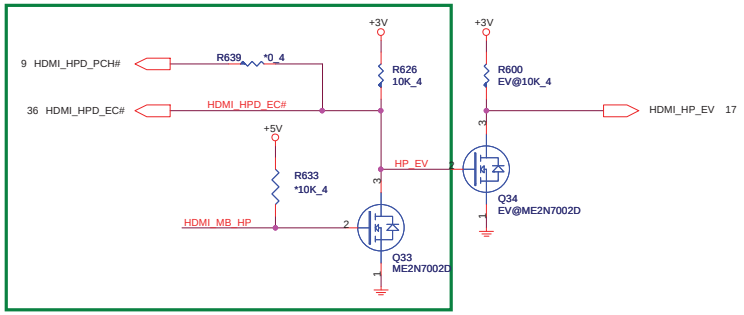


Quanta Computer Inc. PROJECT : ZYD			
Size	Document Number	CRT/LVDS	Rev 3B
Date: Tuesday, April 06, 2010		Sheet 24 of 50	

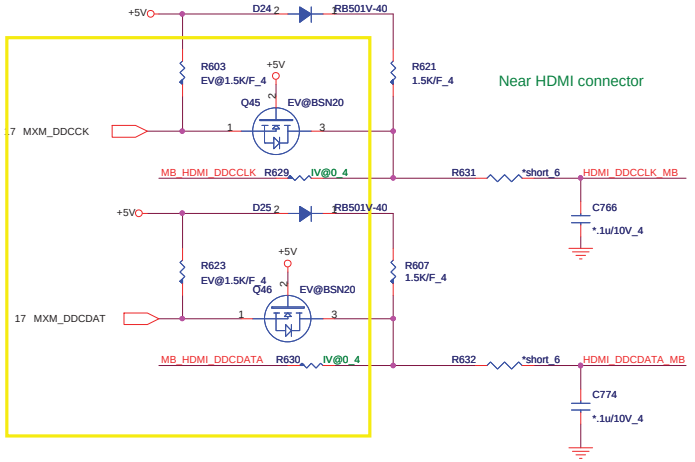
IV@ HDMI LEVEL SHIFTER



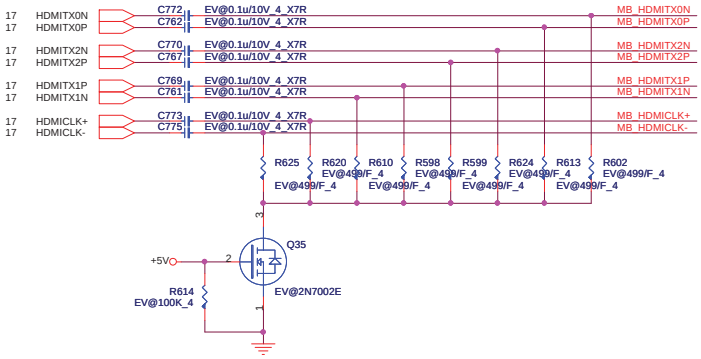
HDMI-detect



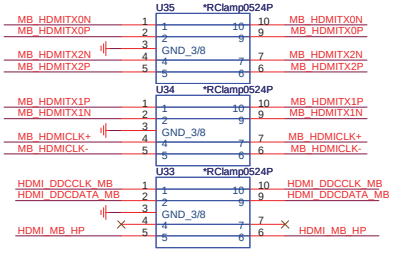
I2C



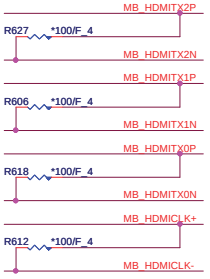
External Graphic HDMI source



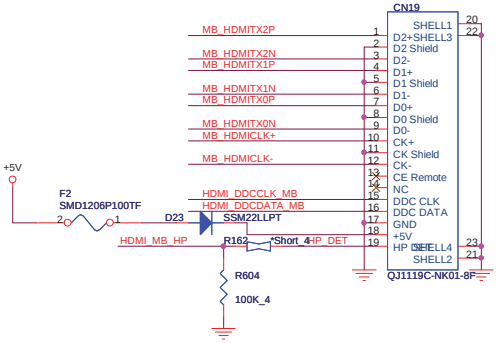
ESD Protect



EMI

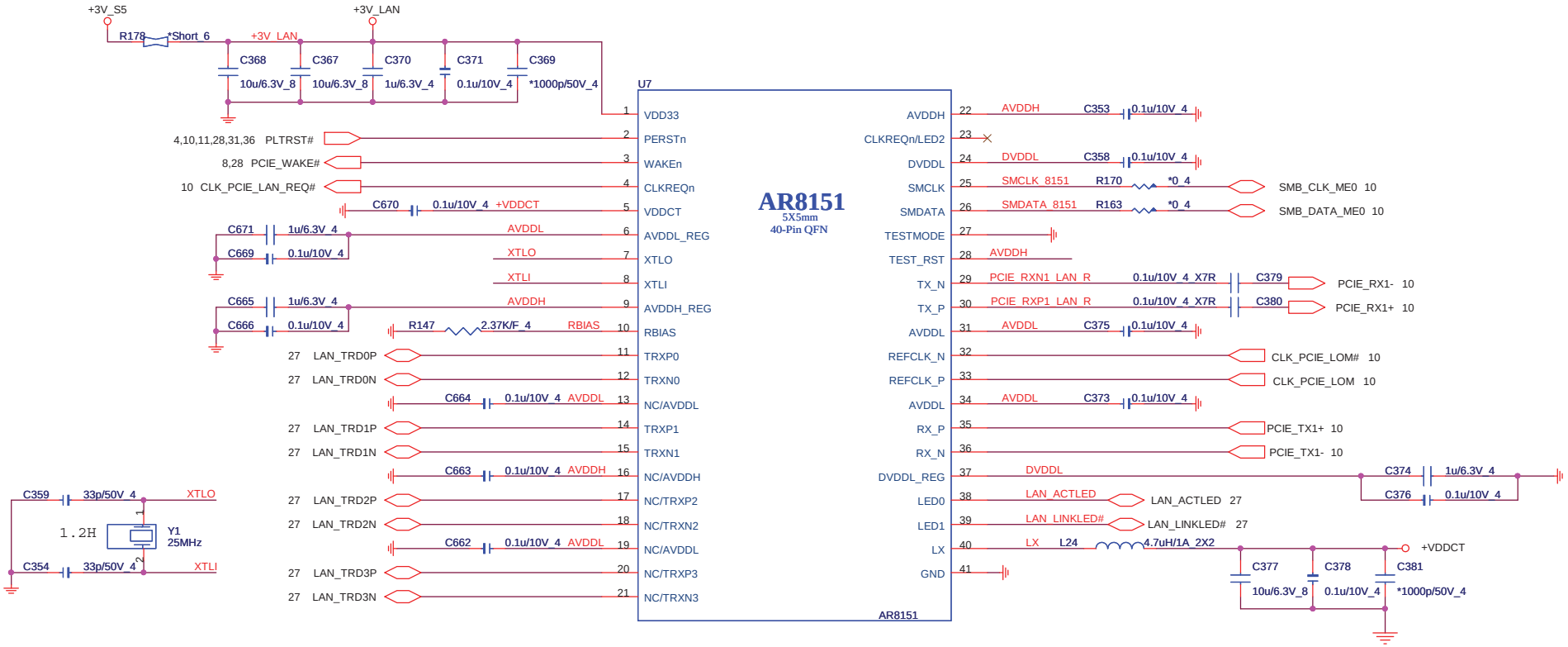


HDMI connector



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number	Rev
	HDMI (SN75DP139)	3B
Date: Tuesday, April 06, 2010	Sheet 25 of 50	

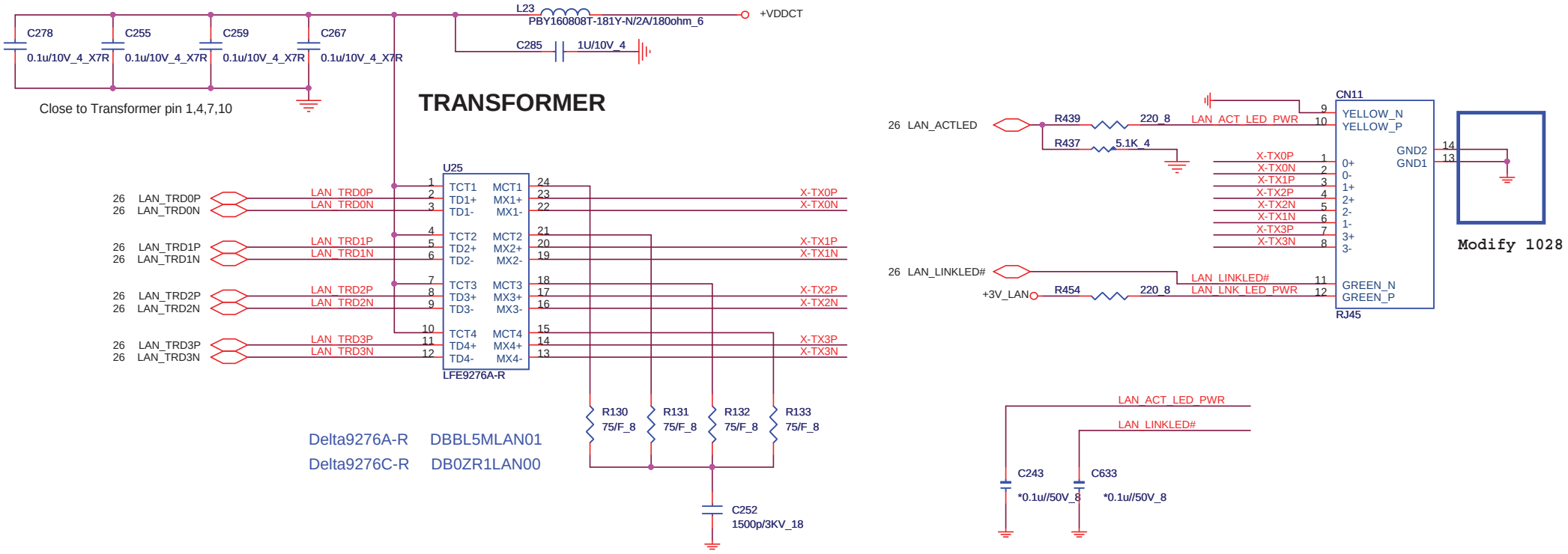
Giga-LAN AR8151



Quanta Computer Inc.

PROJECT : ZYD

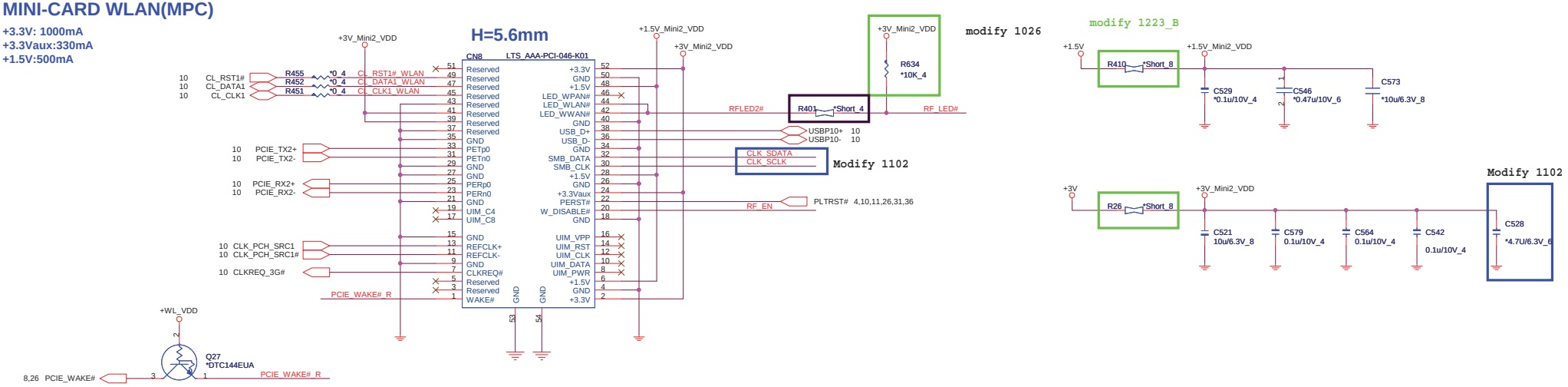
Size	Document Number	Rev
	GLAN BCM57780	3B
Date: Tuesday, April 06, 2010	Sheet 26 of 50	



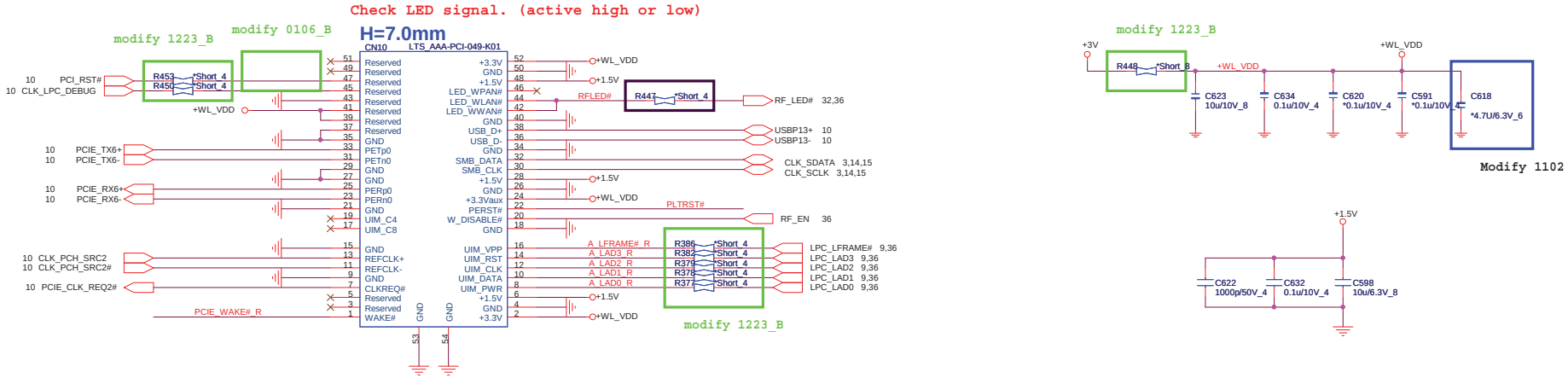
Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: LAN Transformer and RJ45	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 27 of 50	

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

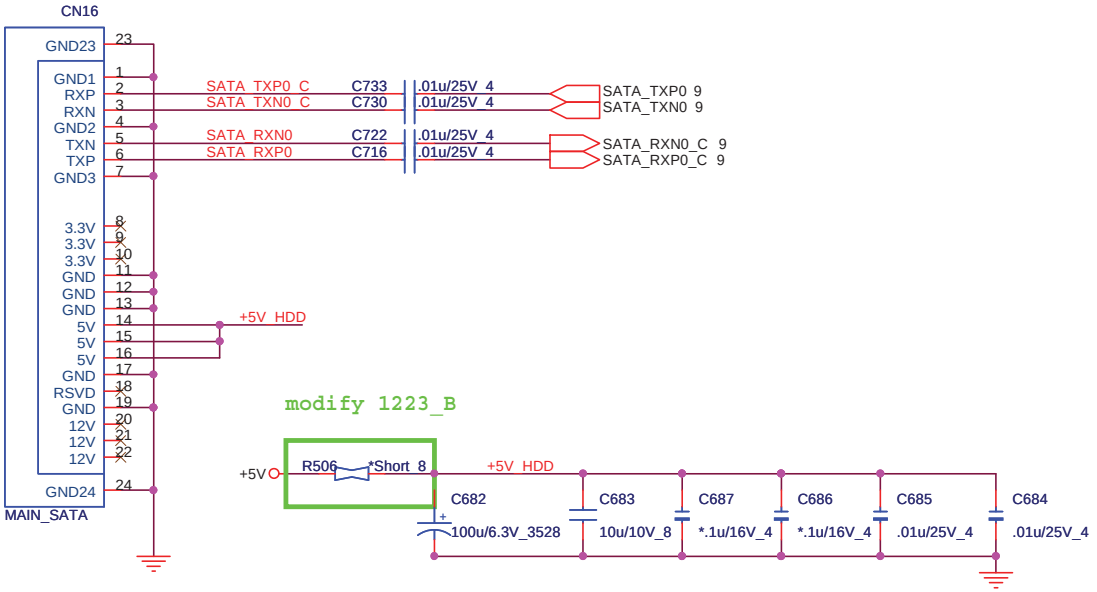


MINI-CARD (MNC)Reserve for BA70

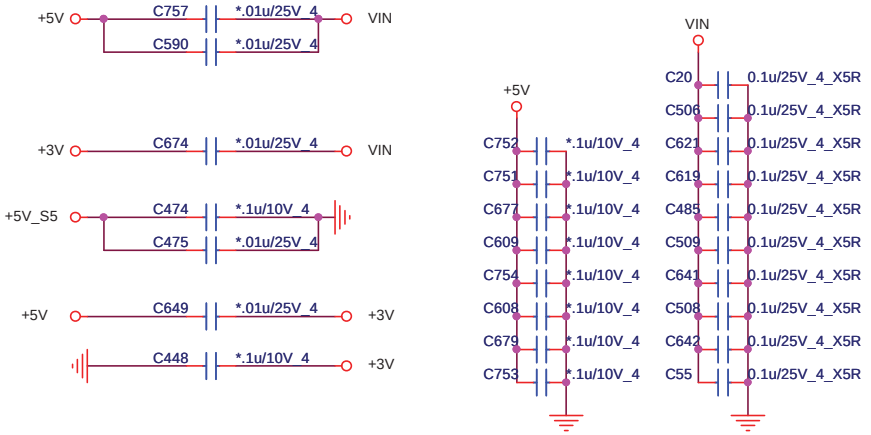


Quanta Computer Inc.			
PROJECT : ZYD			
Size	Document Number	MINI PCI-E card/TV	Rev 3B
Date: Tuesday, April 06, 2010	Sheet 28 of 50		

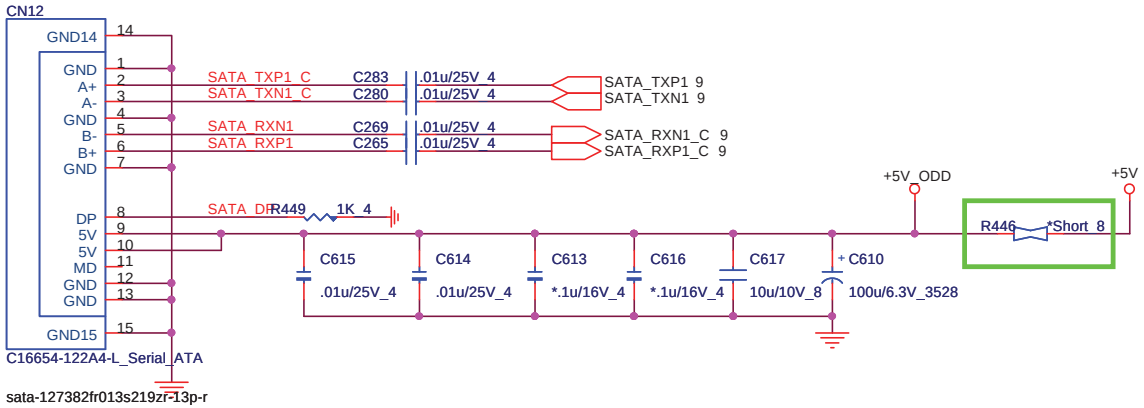
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)

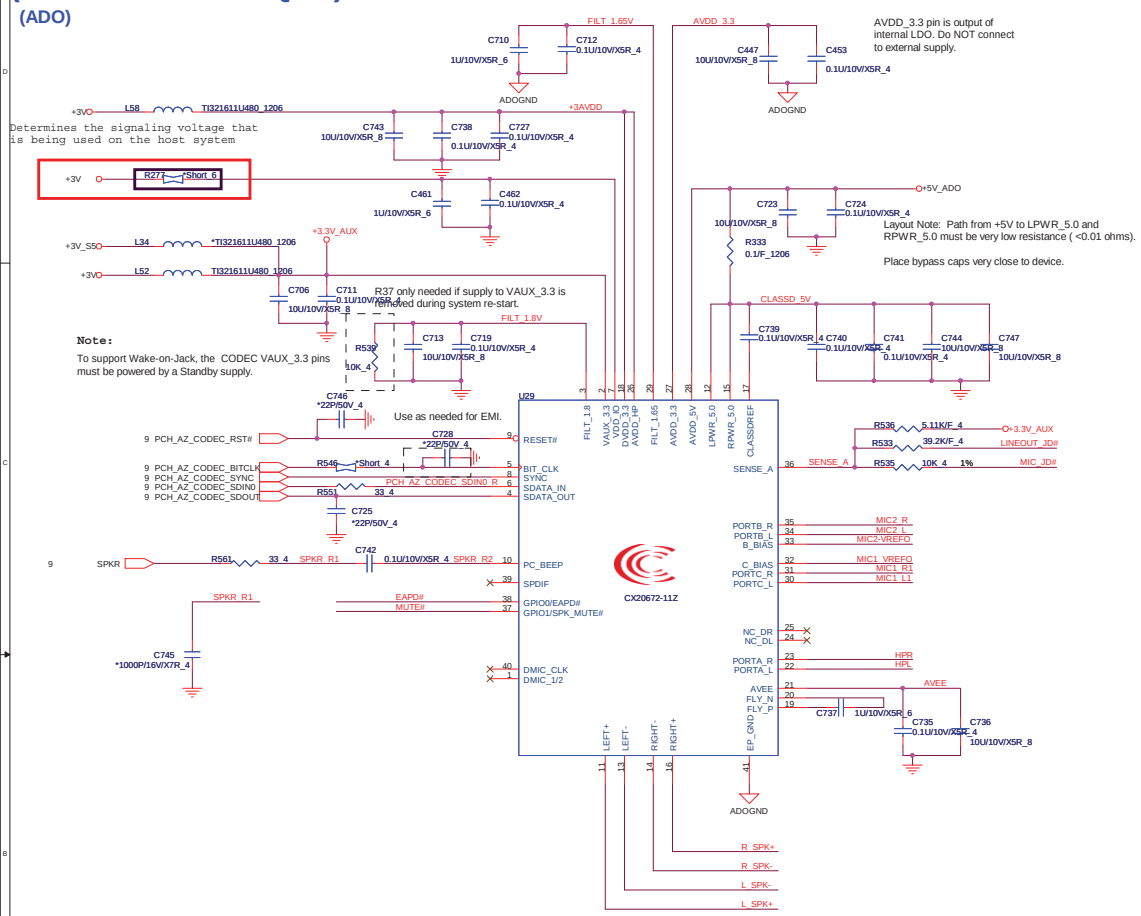


Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: SATA-HDD/ODD/USB-ESATA	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 29 of 50	

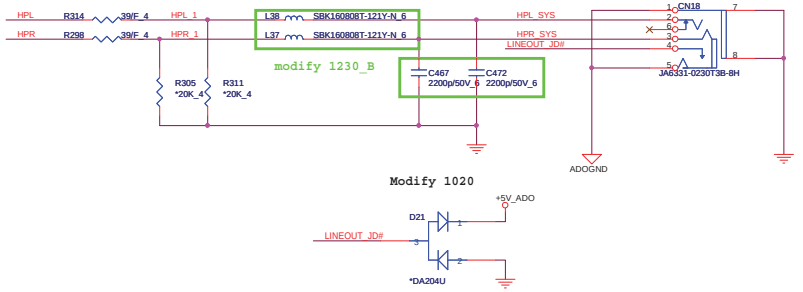
Codec(ADO)

(CX20672-11Z for QFN)

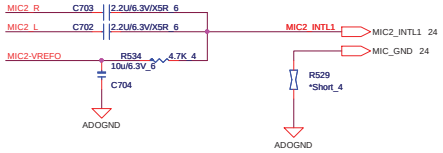
(ADO)



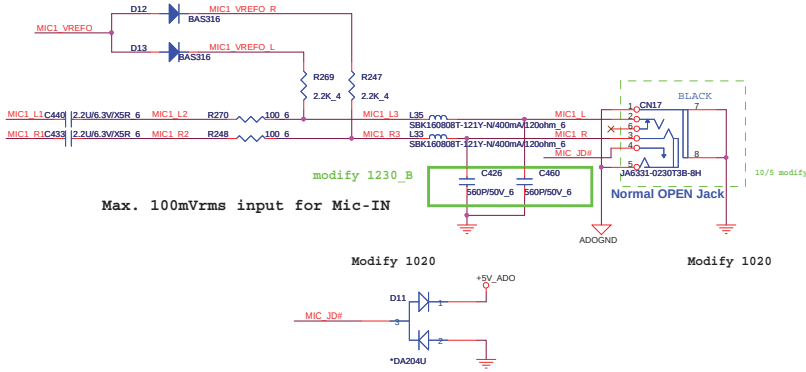
Headphone



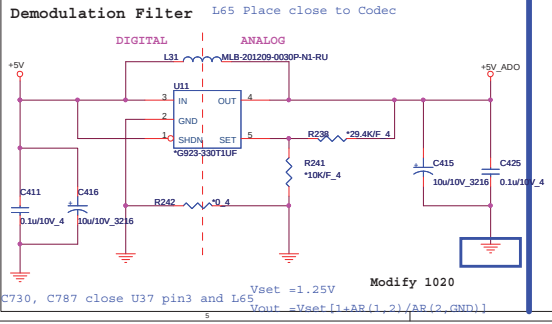
INT. MIC



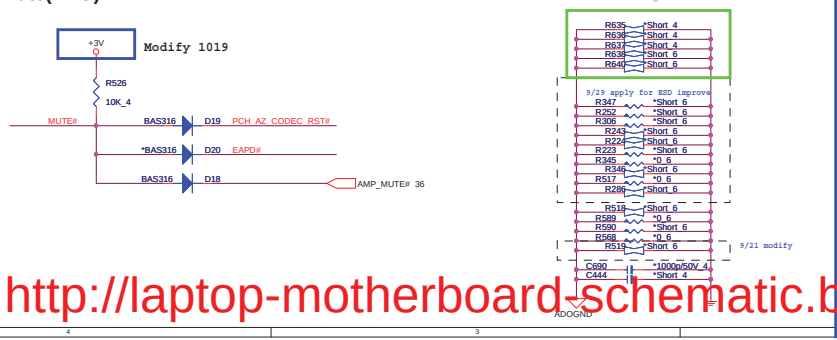
EXT. MIC



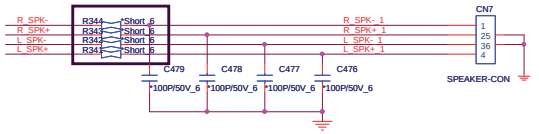
Power (ADO)



Mute(ADO)

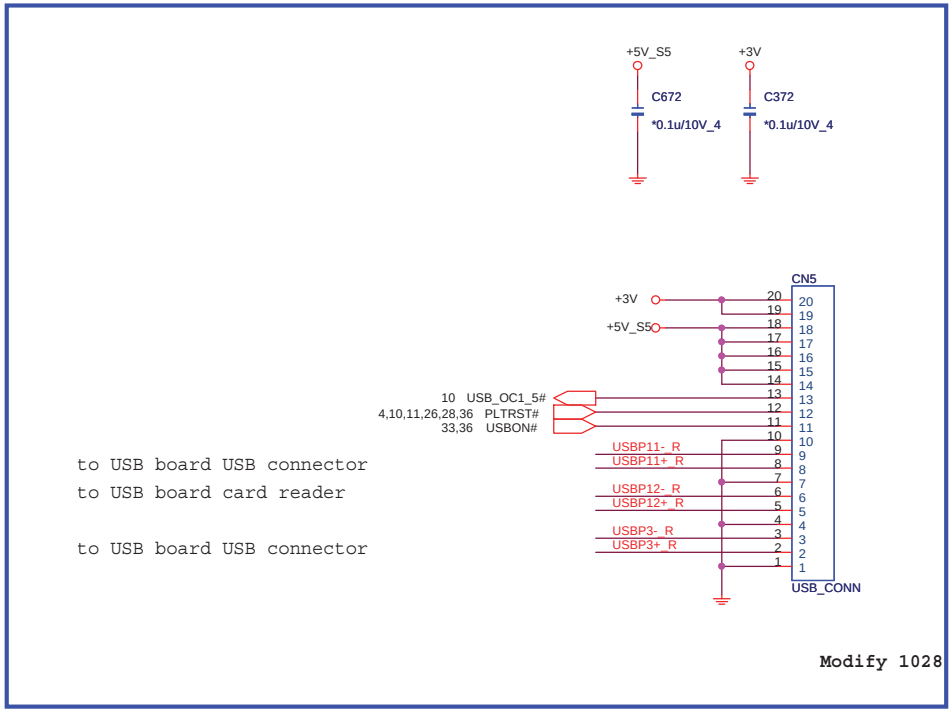


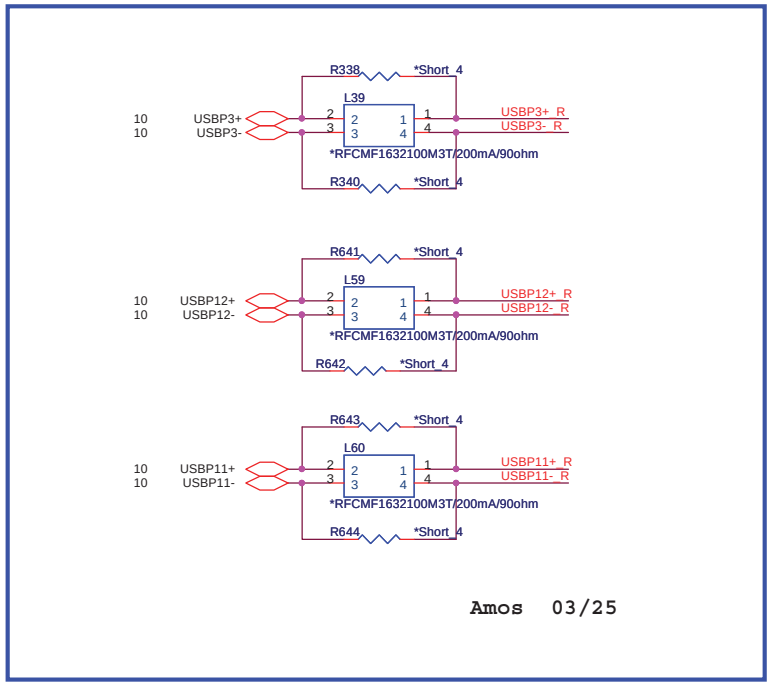
Internal Speaker(AMP)



Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number | Rev
CX20672-11Z | 3B
Date: Tuesday, April 06, 2010 | Sheet 30 of 50

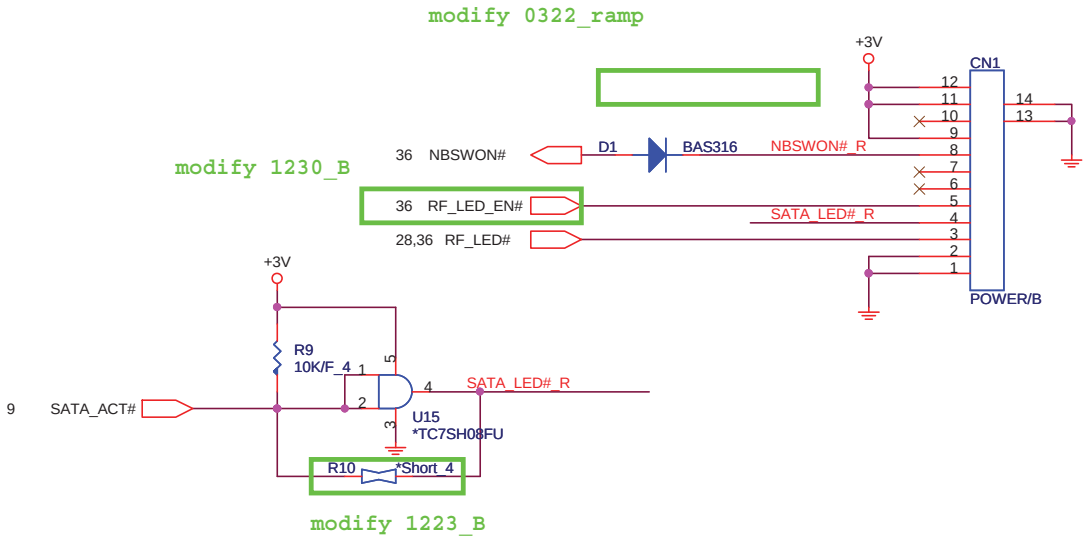
Cardreader CONN(MMC)



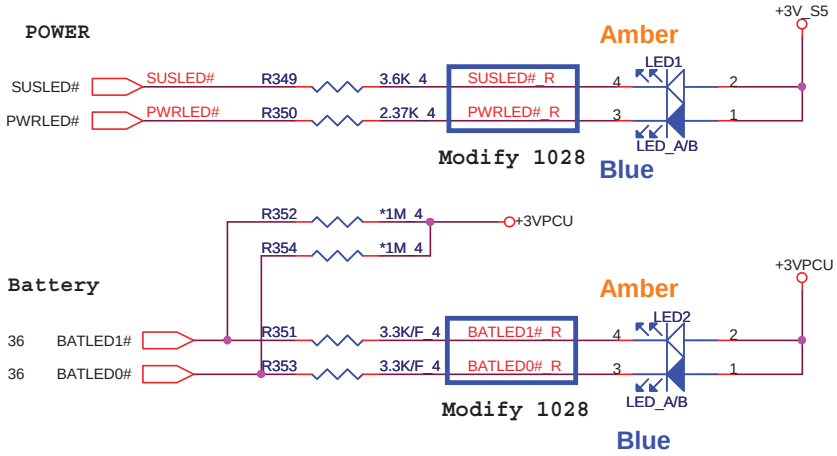


Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number | CardReader &USB/B | Rev 3B
Date: Tuesday, April 06, 2010 | Sheet 31 of 50

POWER BOARD CONN(UIF)



LED(UIF)



Quanta Computer Inc.

PROJECT : ZYD

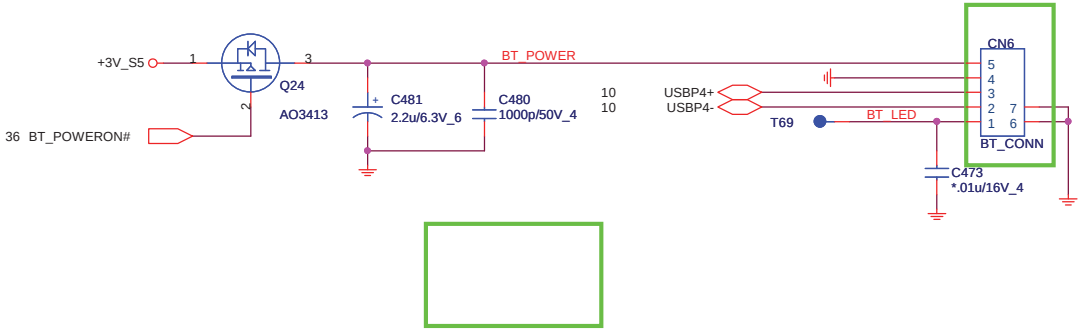
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3B

Date: Tuesday, April 06, 2010 Sheet 32 of 50

Modify 1022

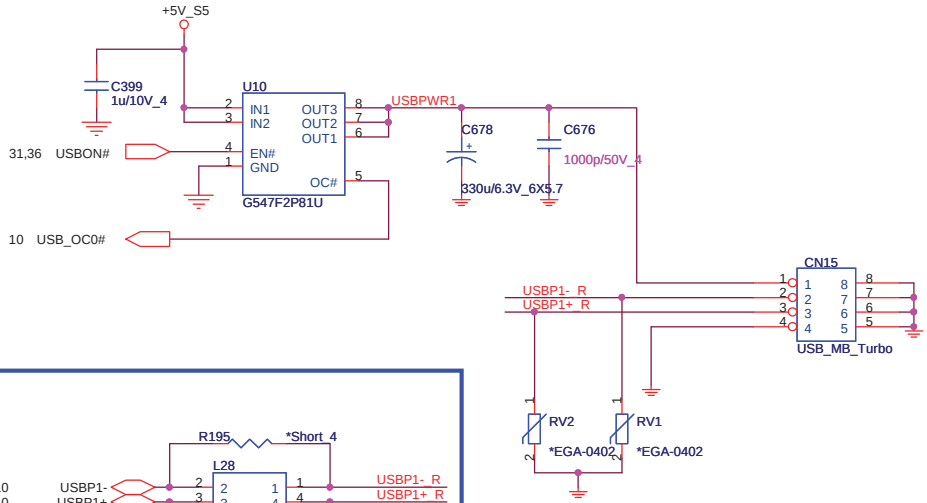
BLUETOOTH CONNECTOR(BTM)

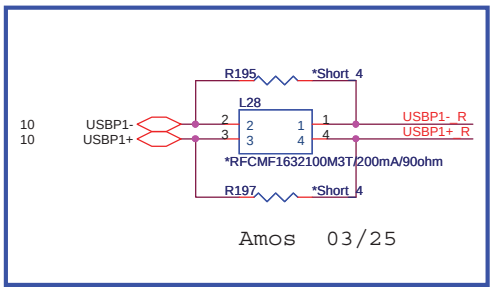
modify 1223_B



modify 0224_C

USBX1(USB)



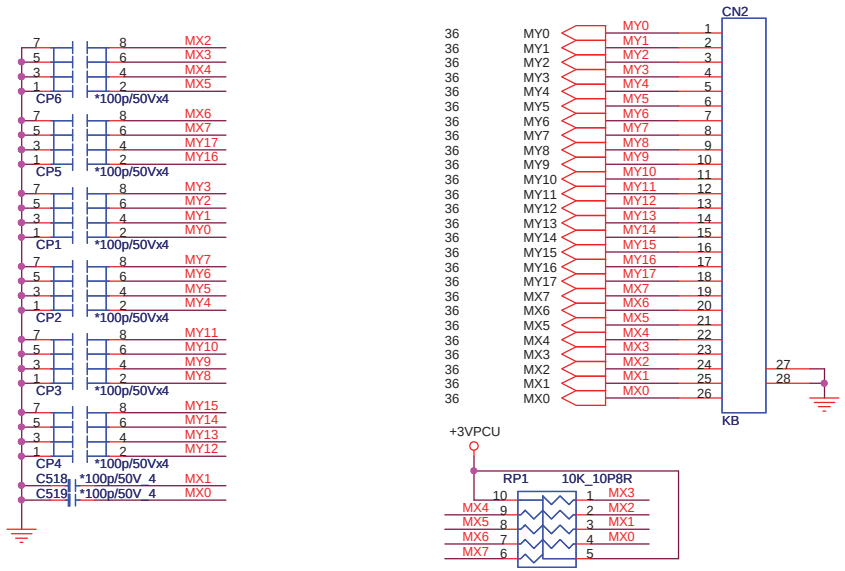


Quanta Computer Inc.

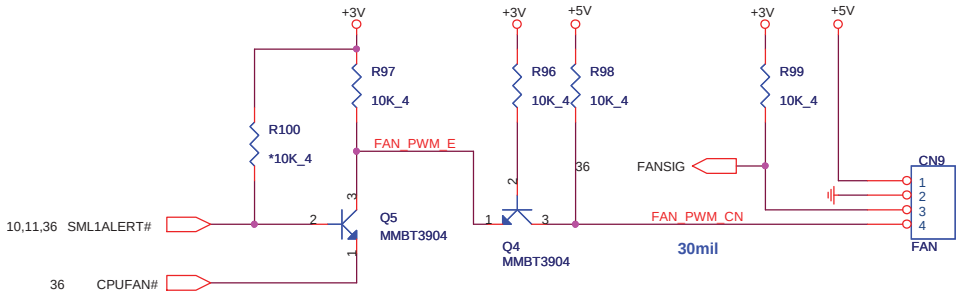
PROJECT : ZYD

Size	Document Number	Rev
	USB/ BT	3B
Date: Tuesday, April 06, 2010	Sheet 33 of 50	

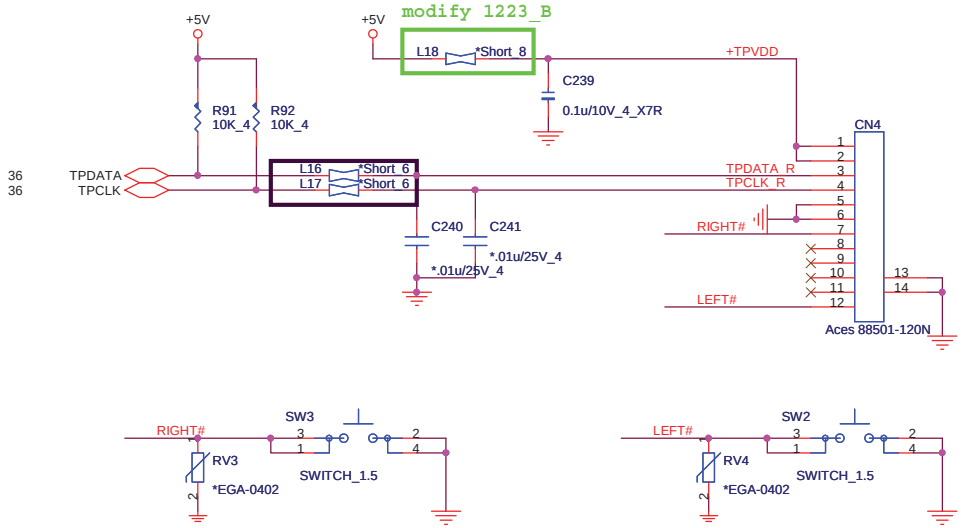
K/B

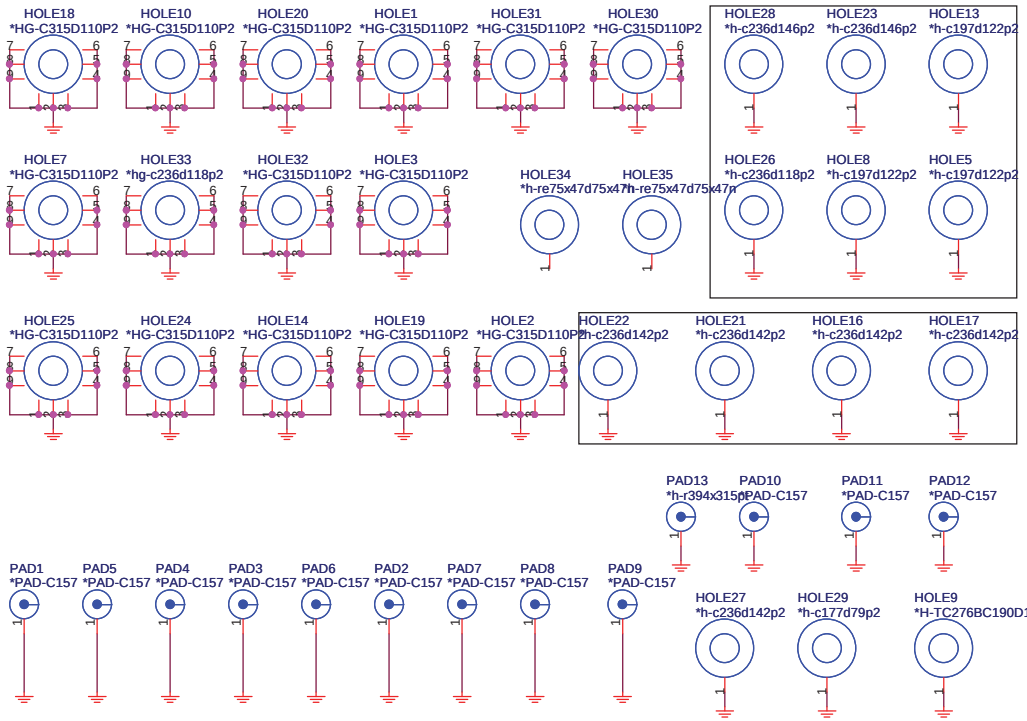


CPU FAN(THM)



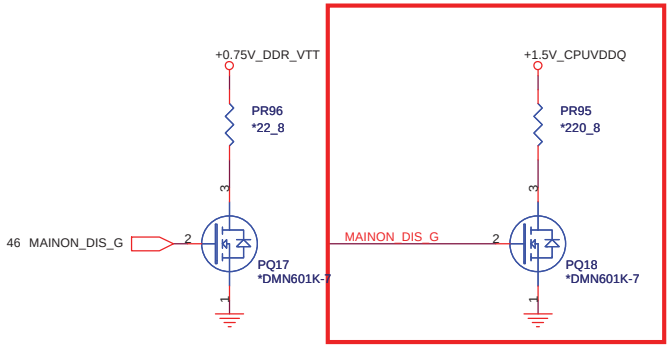
TOUCHPAD & Switch CONN.(TPD)



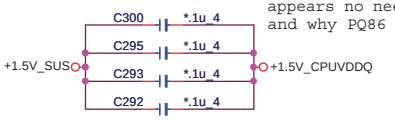


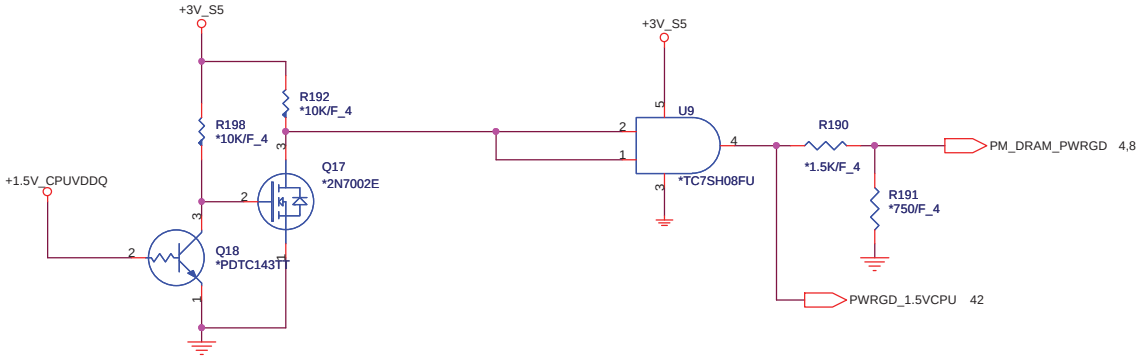
Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number	Rev
	KB/FAN/TP+FP	3B
Date: Tuesday, April 06, 2010	Sheet 34 of 50	

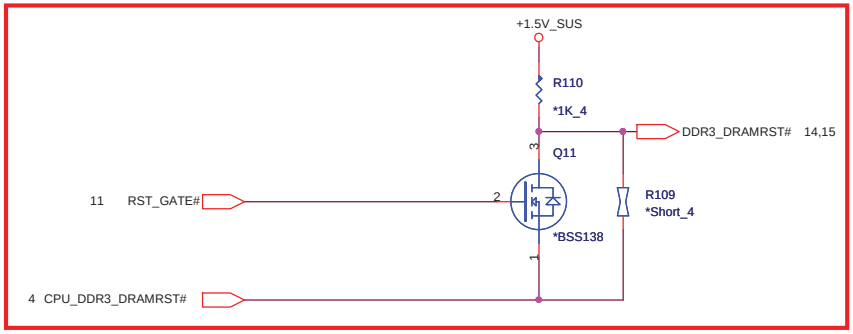
SM_DRAMRST# signal (to system memory) to be driven high
CKE signals (to system memory) to be driven low
VREFDQ and VREFCA voltage (on system memory) needs to be maintained
1.5-V power rail to system memory to be maintained.
All other DDR3 memory interface signals are don't care during S3 state for
memory self refresh.
SM_DRAMPWROK (to processor) is driven low during S3 as Processor VDDQ (1.5 V)
is turned off with this implementation.

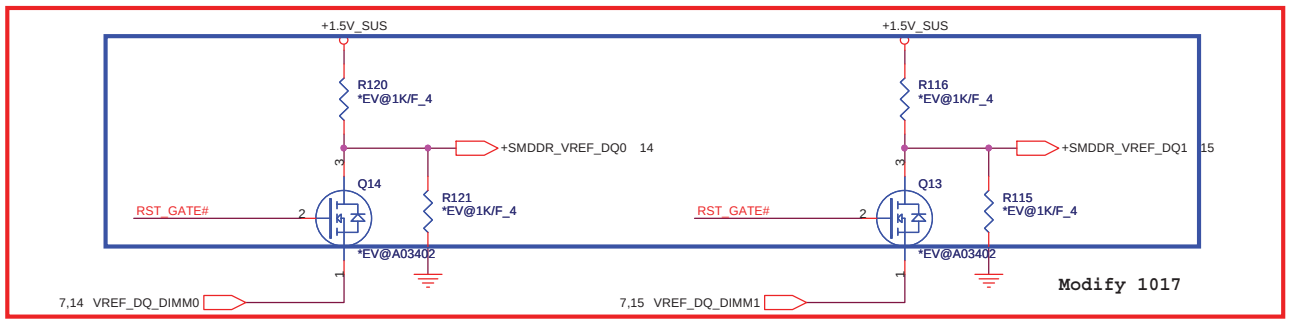


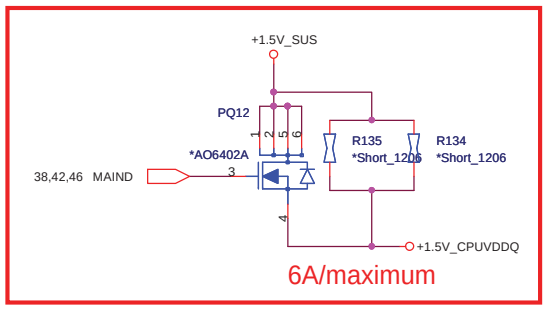
appears no need stuff if PQ12 don't stuff
and why PQ86 is 220ohm









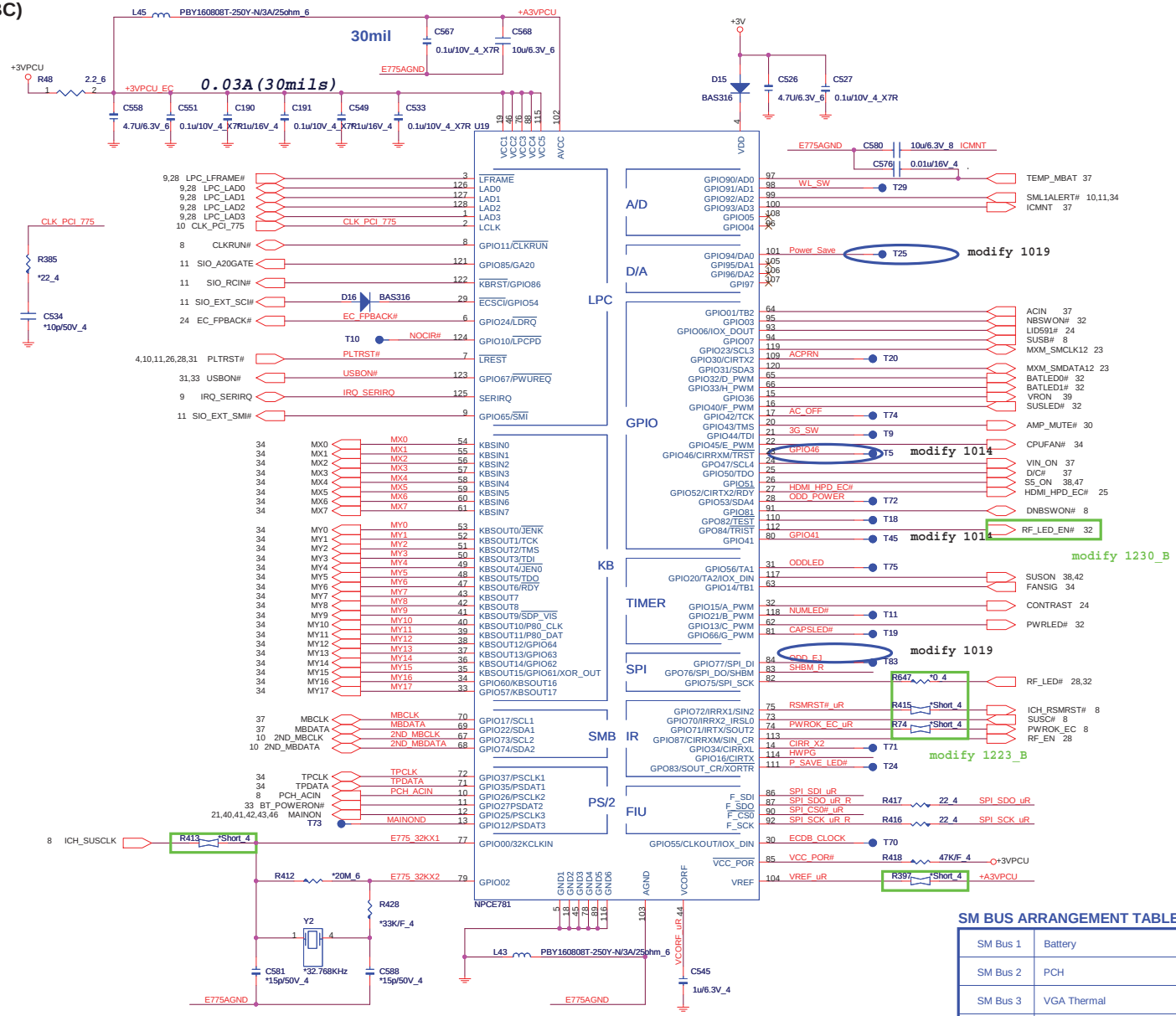


These isolation FETs are not required for ARD-only
designs. Only CFD and common motherboard designs need to implement this circuit to
meet the DDR3 VREF specification during S3.

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	S3 power saving	3B
Date: Tuesday, April 06, 2010	Sheet 35 of 50	

EC(KBC)



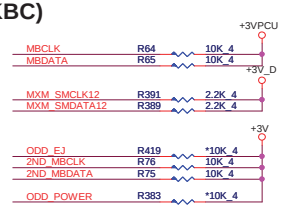
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

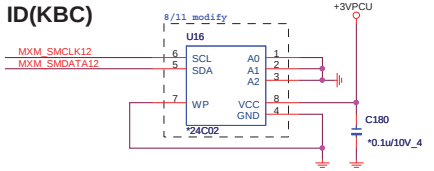
SHBM — SHBM_R — R420 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

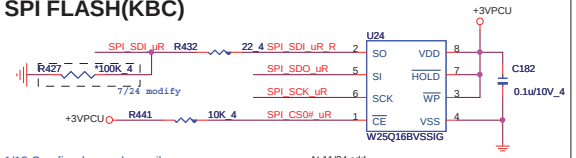
SM BUS PU(KBC)



ACER ID(KBC)



SPI FLASH(KBC)

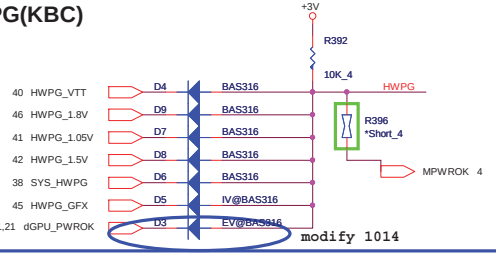


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

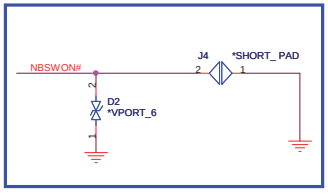
HWPG(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

POWER-ON Switch(KBC)

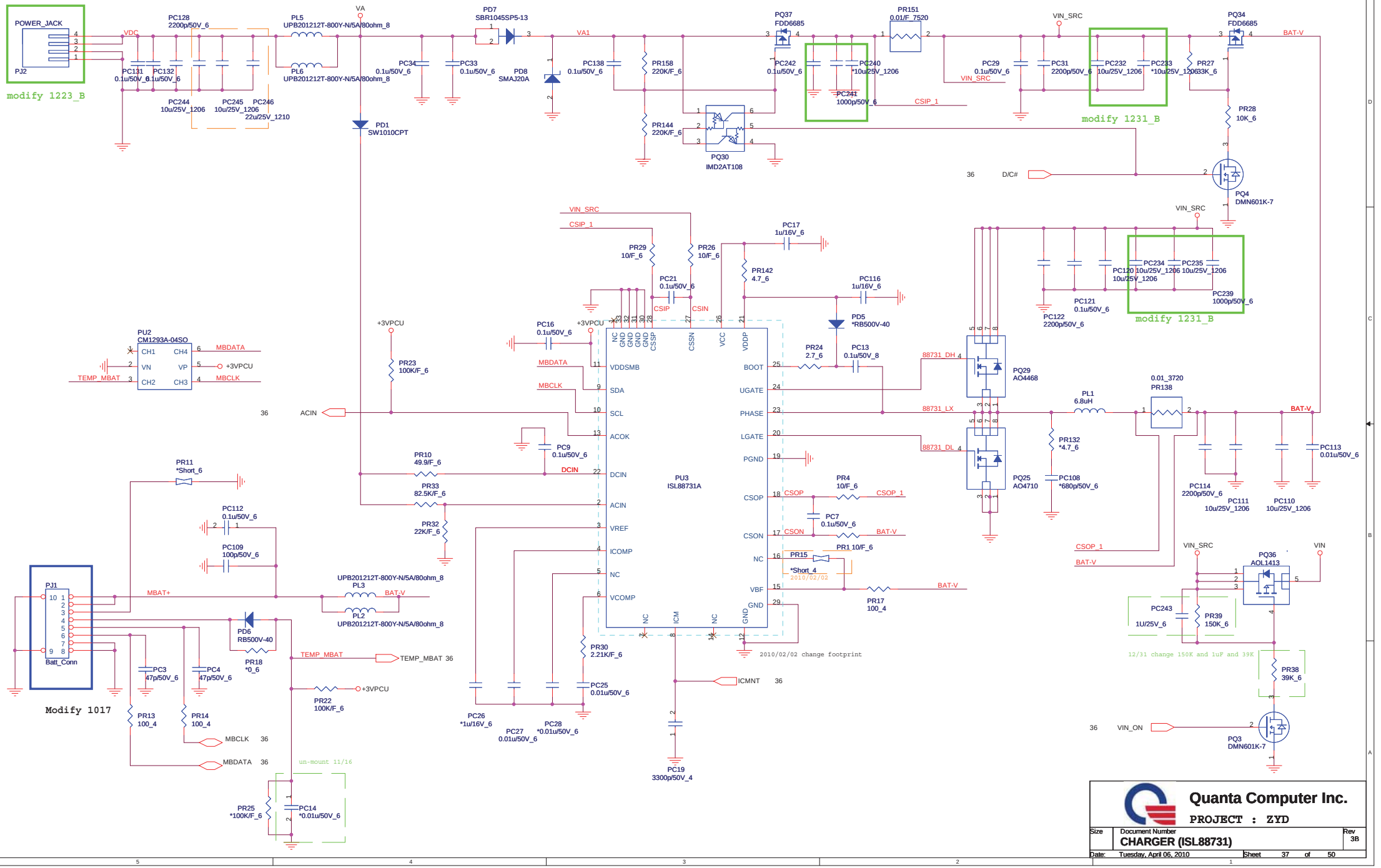


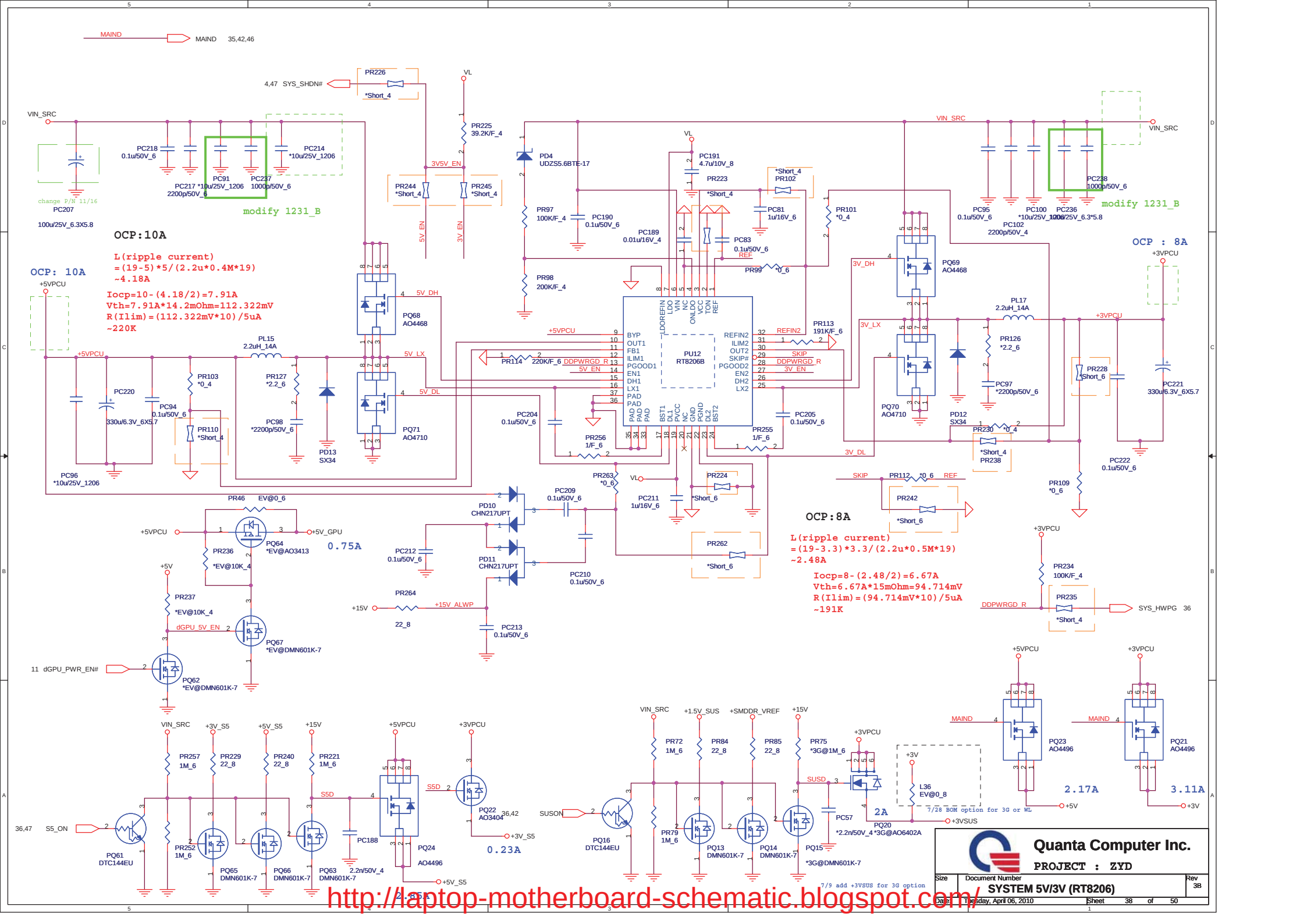
Modify 1028

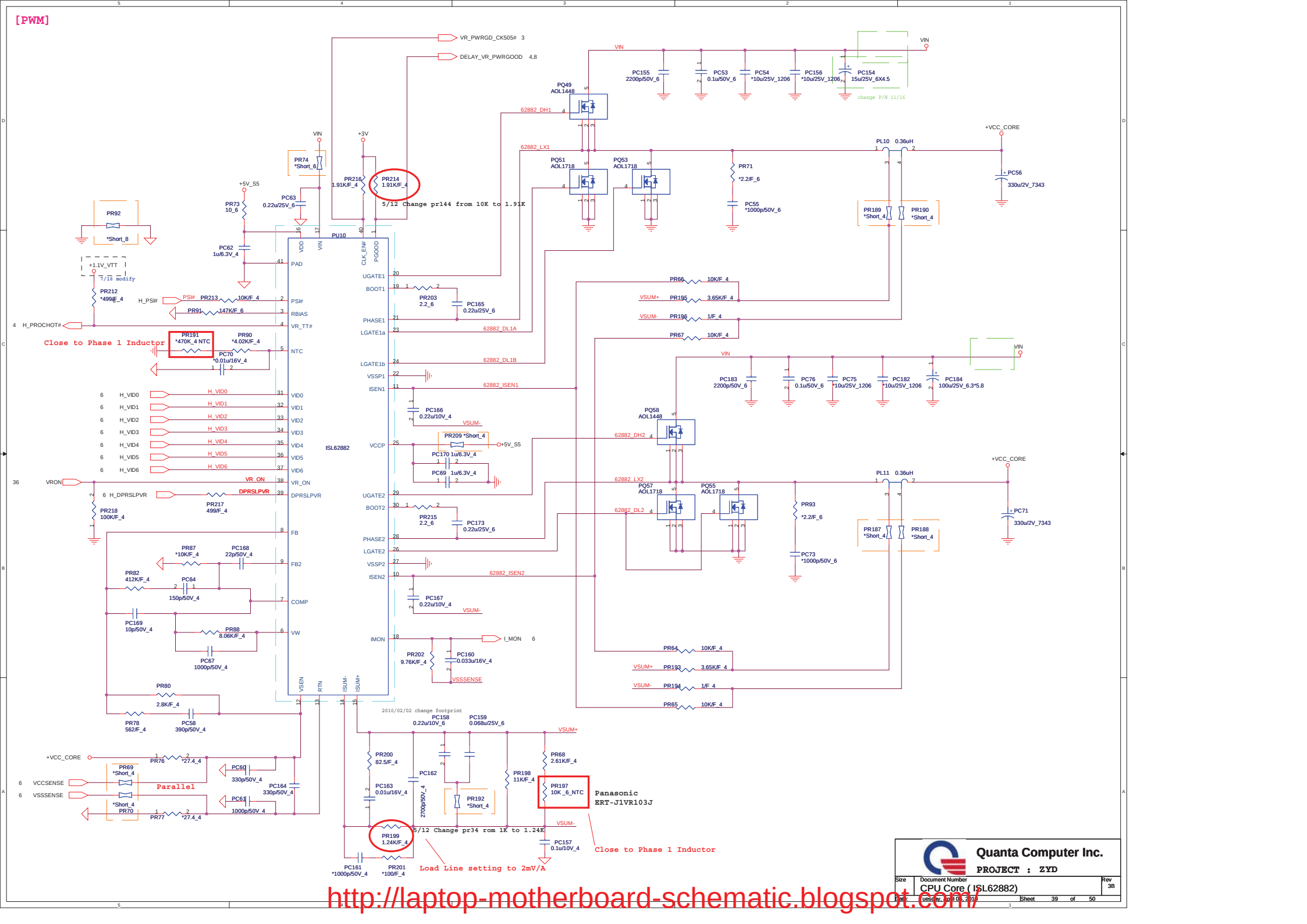
INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZYD

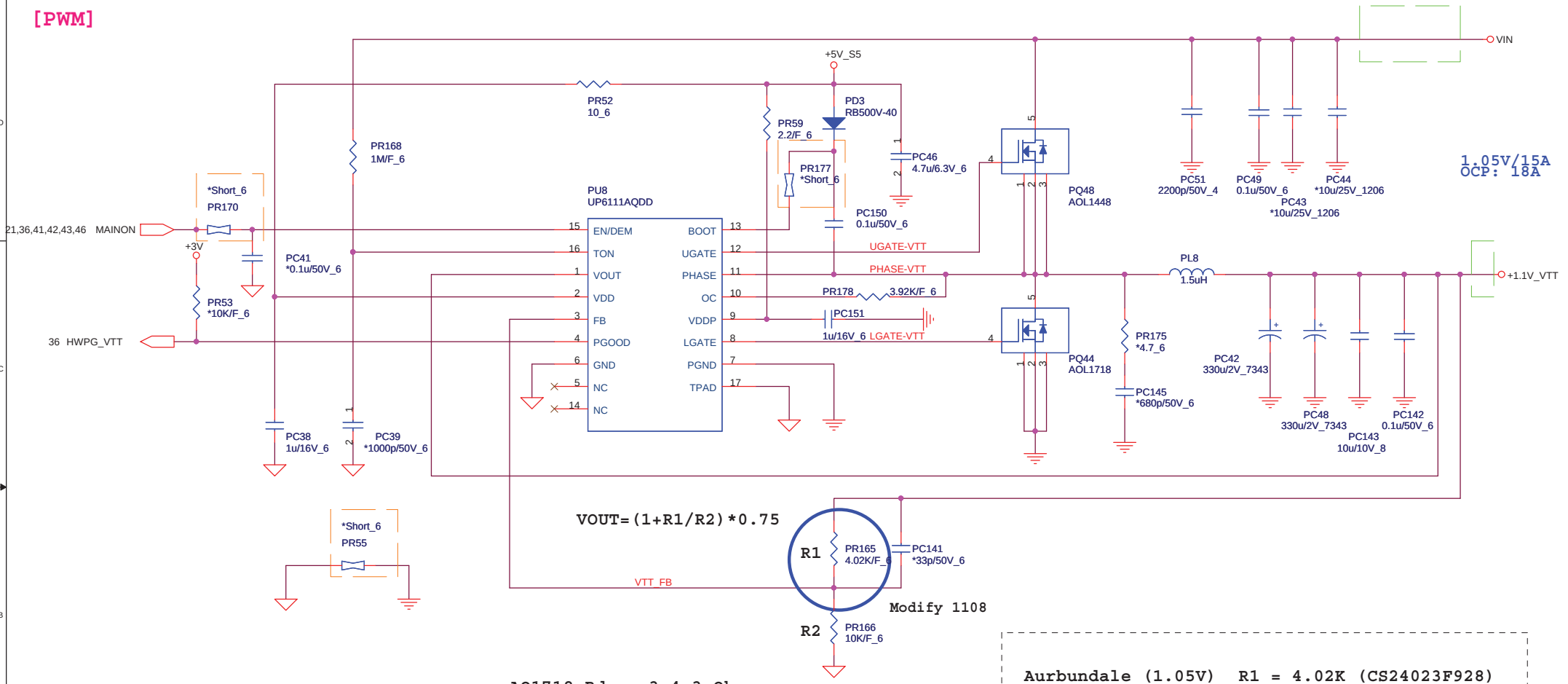
Size	Document Number	Rev
	WPCE781 & FLASH	3B
Date: Tuesday, April 06, 2010	Sheet 36 of 50	






[PWM]
VR_PWRGD_CK505# 3
DELAY_VR_PWRGOOD 4,8
ISL62882
PU10
5/12 Change pr144 from 10K to 1.91K
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
5/12 Change pr34 rom 1K to 1.24K
Close to Phase 1 Inductor
Load Line setting to 2mV/A
2010/02/02 change footprint
change P/N 11/16
Quanta Computer Inc.
PROJECT : ZYD
CPU Core (ISL62882)
http://laptop-motherboard-schematic.blogspot.com/

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

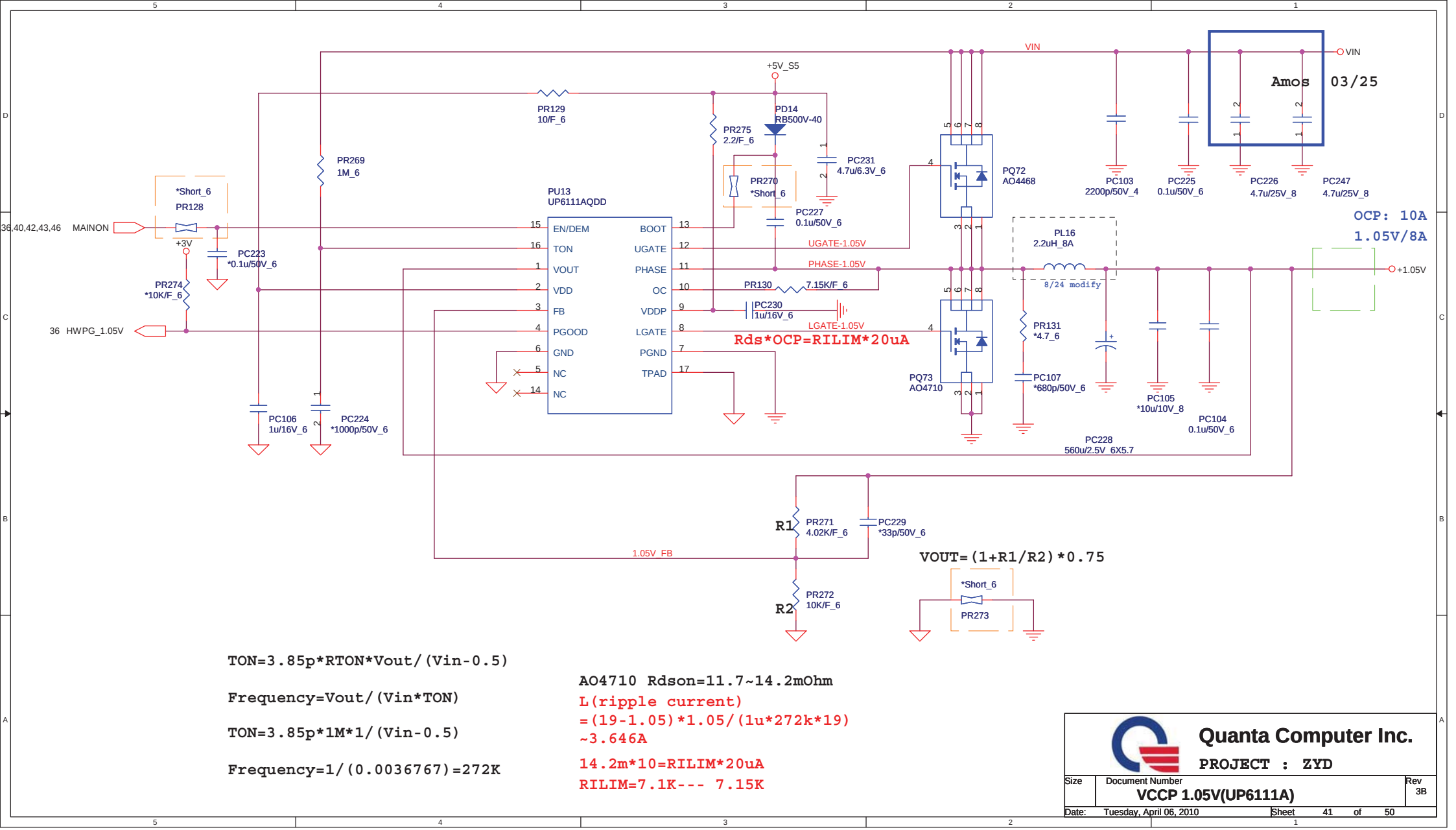
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Aurbundale (1.05V)	R1 = 4.02K (CS24023F928)
Clarksfield(1.1V)	R1 = 4.75K (CS24753F919)

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VTT (UP6111A)	3B
Date: Tuesday, April 06, 2010	Sheet 40 of 50	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

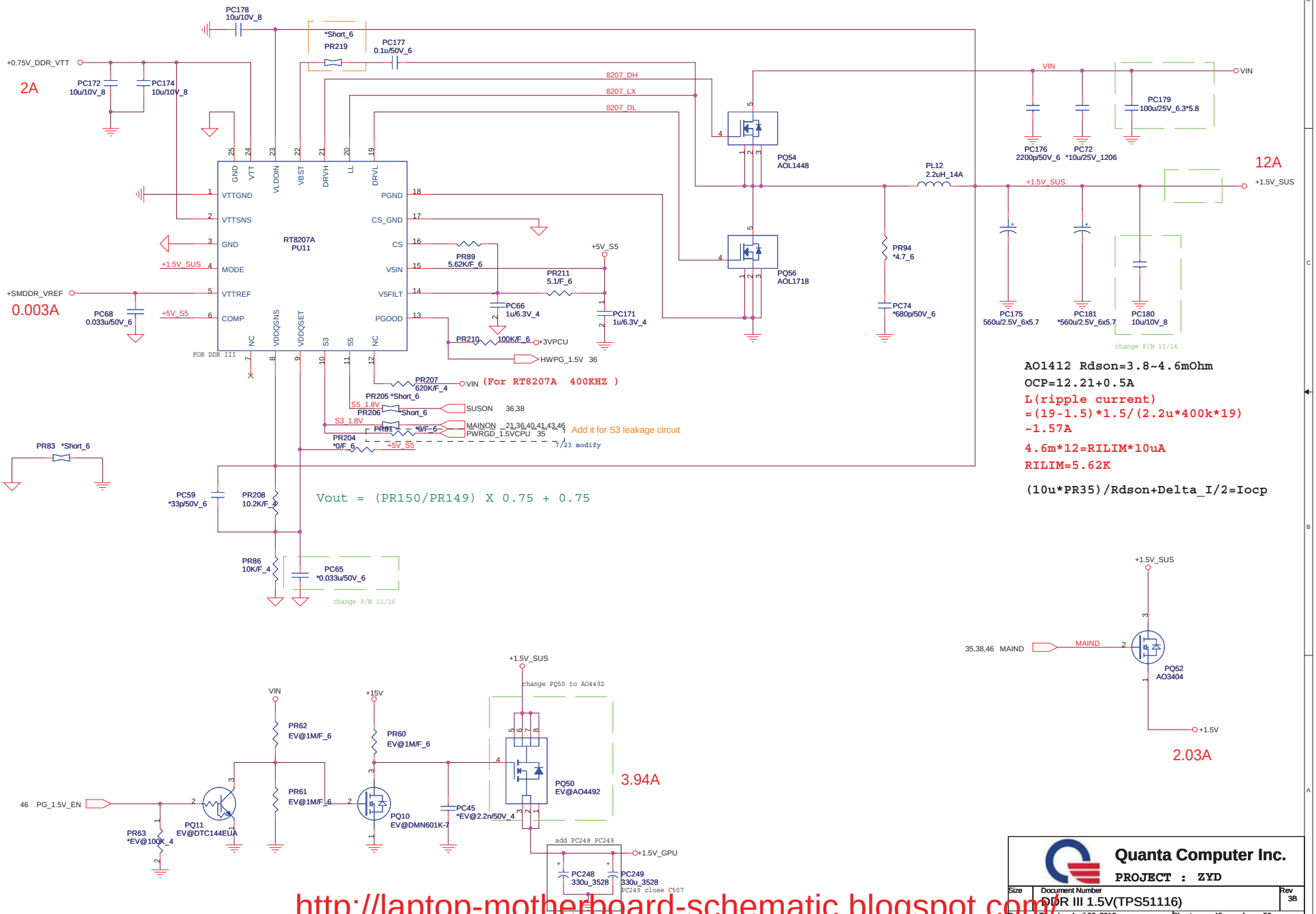
AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

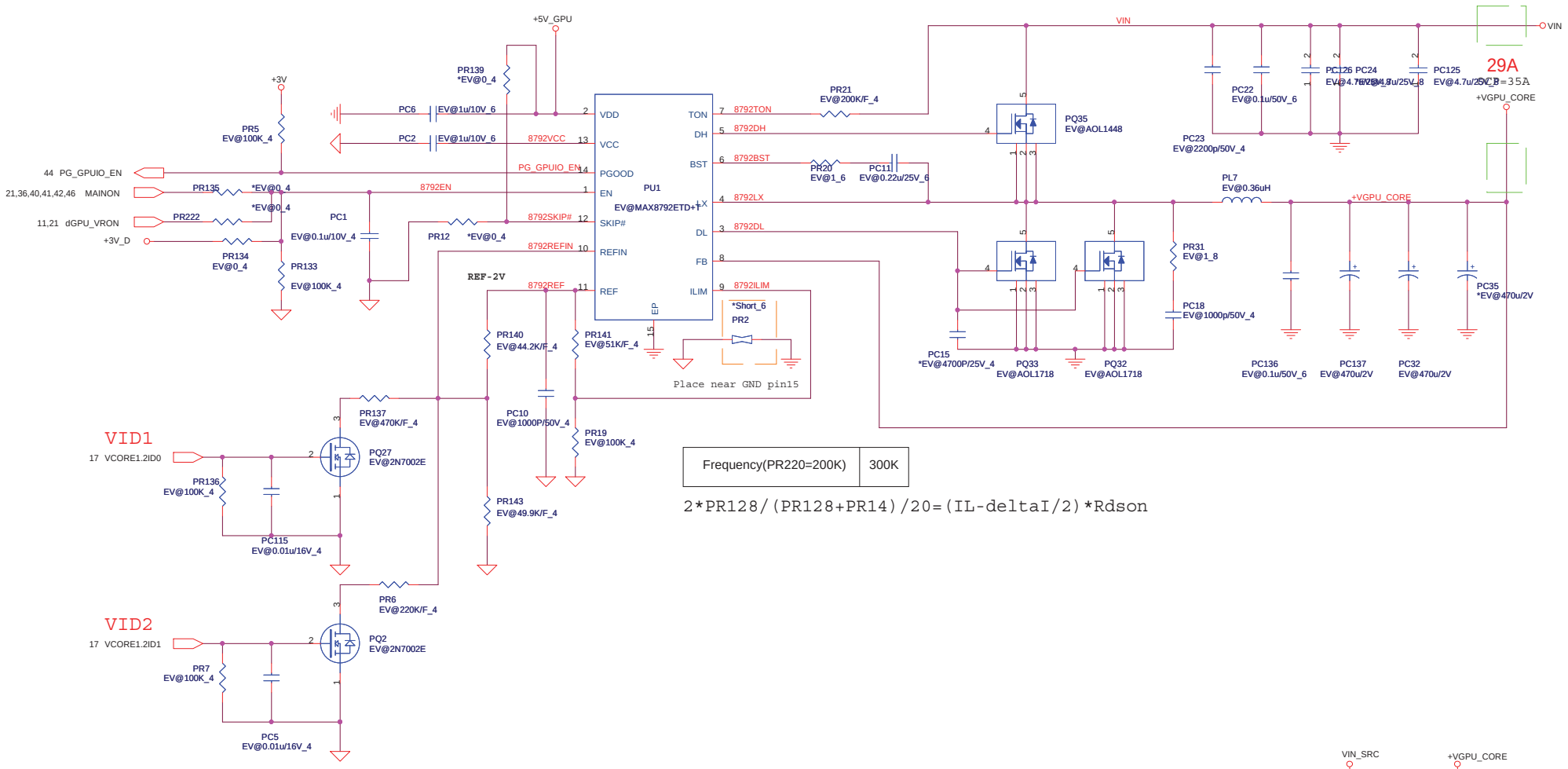
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	3B
Date: Tuesday, April 06, 2010	Sheet 41 of 50	



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: DDR III 1.5V(TPS51116)	Rev 3B
Date: Tuesday, April 06, 2010	Sheet 42 of 50	



Frequency(PR220=200K)	300K

2*PR128/(PR128+PR14)/20=(IL-deltaI/2)*Rdson

Madison VID Table

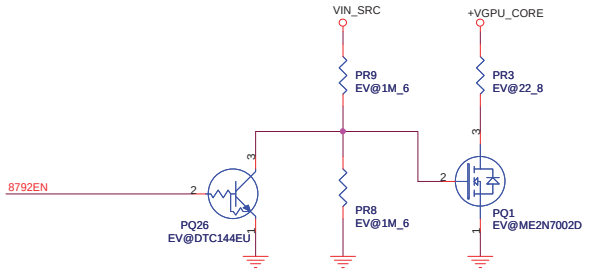
VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.05V
HIGH (1)	LOW (0)		1.0V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR140 = 44.2K
PR143 = 49.9K
PR137 = 470K
PR6= 220K

PARK XT VID Table

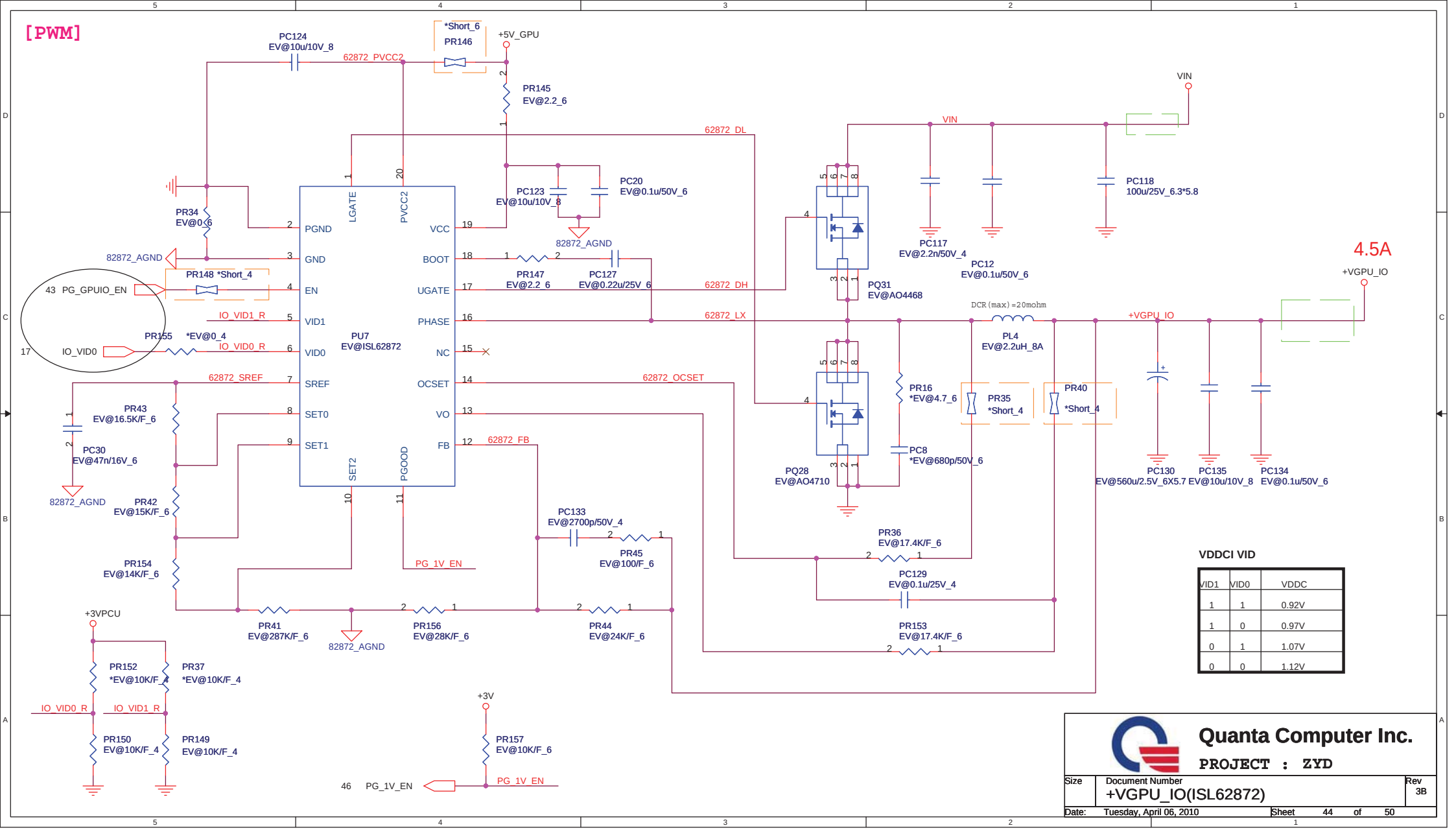
VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.12V
HIGH (1)	LOW (0)		1.05V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR140= 39.2K CS33922FB15
PR143 = 49.9K
PR137 = 332K CS43322FB15
PR6 = 130K CS41302FB00

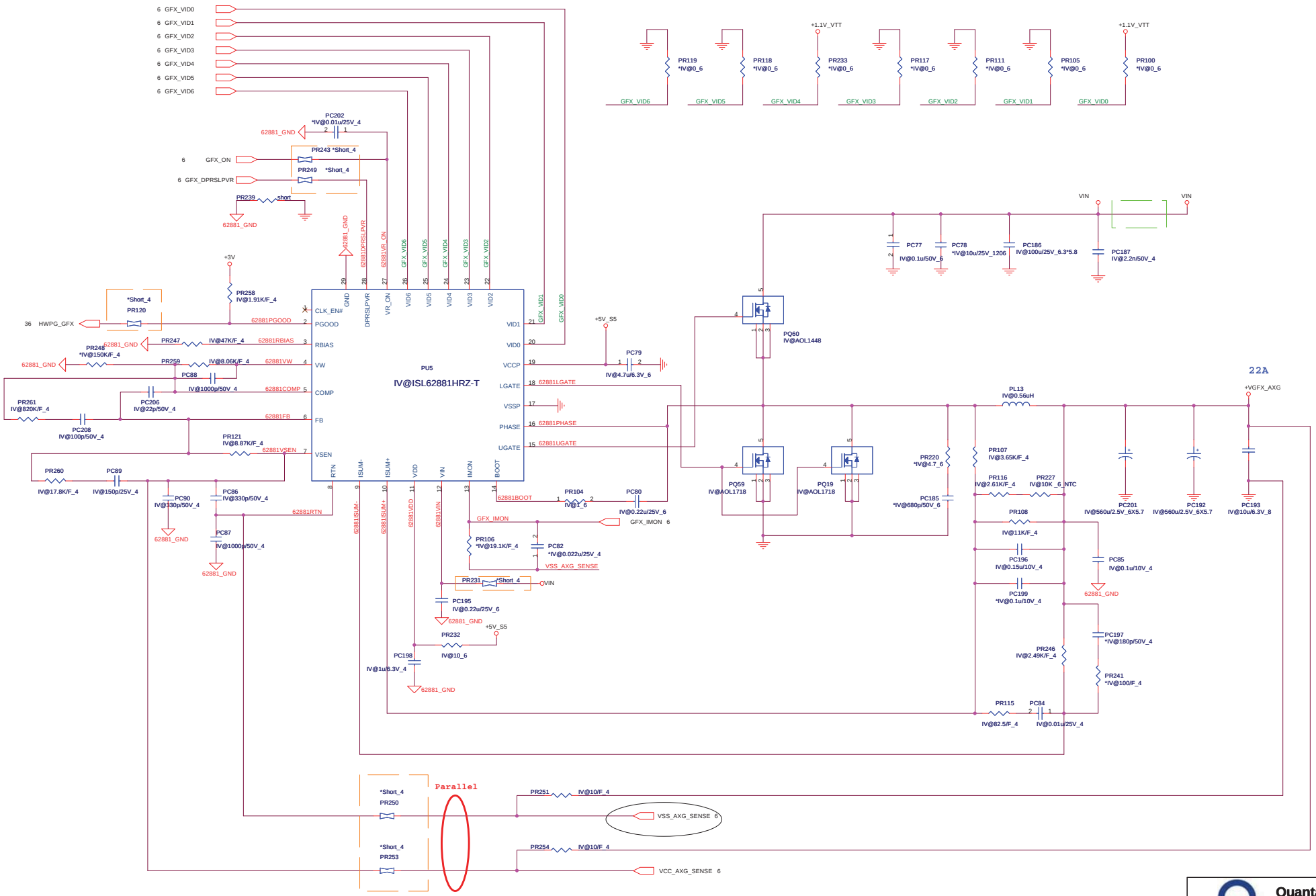


Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	GPU CORE(MAX8792)	3B
Date: Tuesday, April 06, 2010	Sheet 43 of 50	



Int_VGA [PWM]

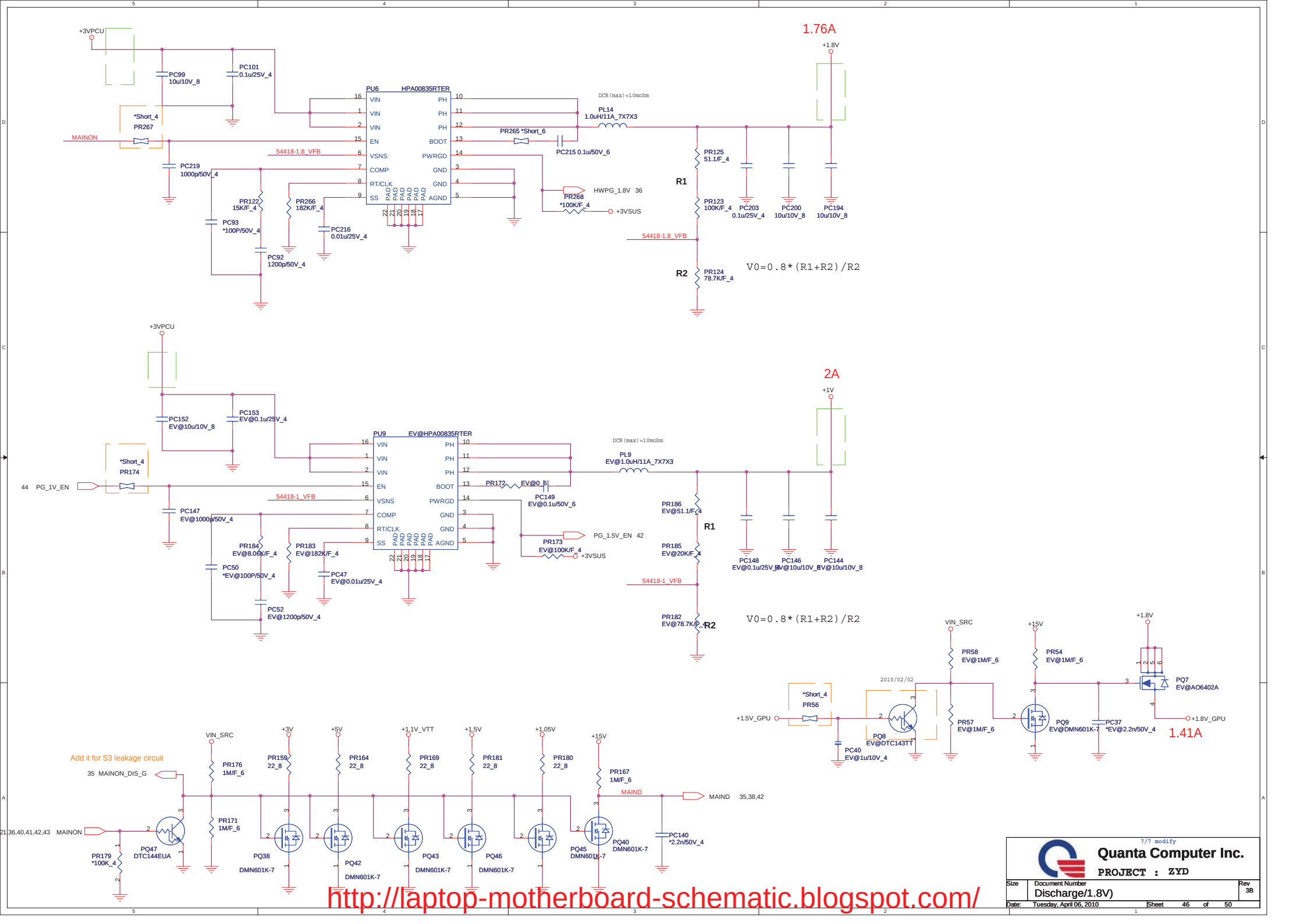


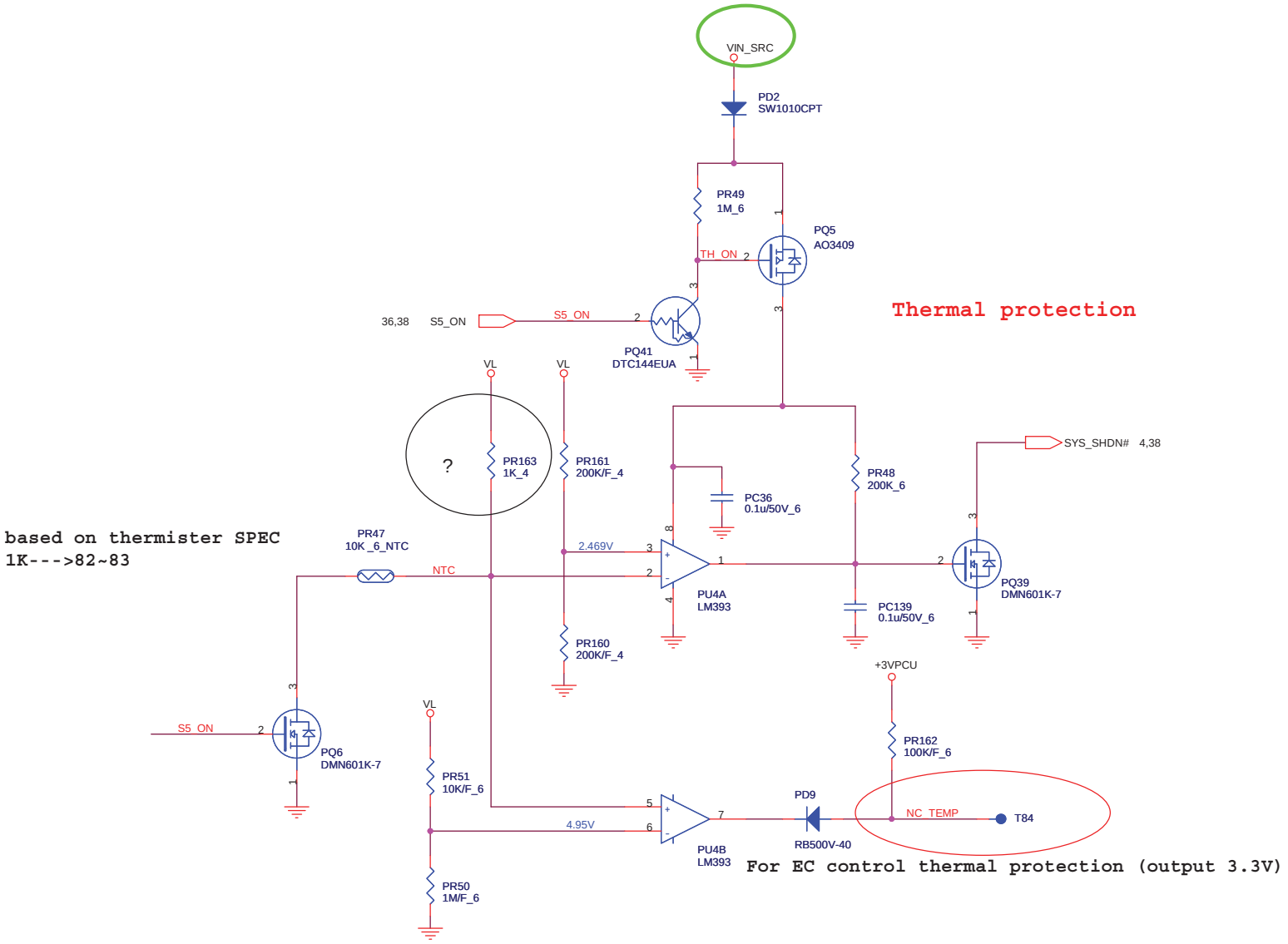
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	3B

Date: Tuesday, April 06, 2010 Sheet 45 of 50

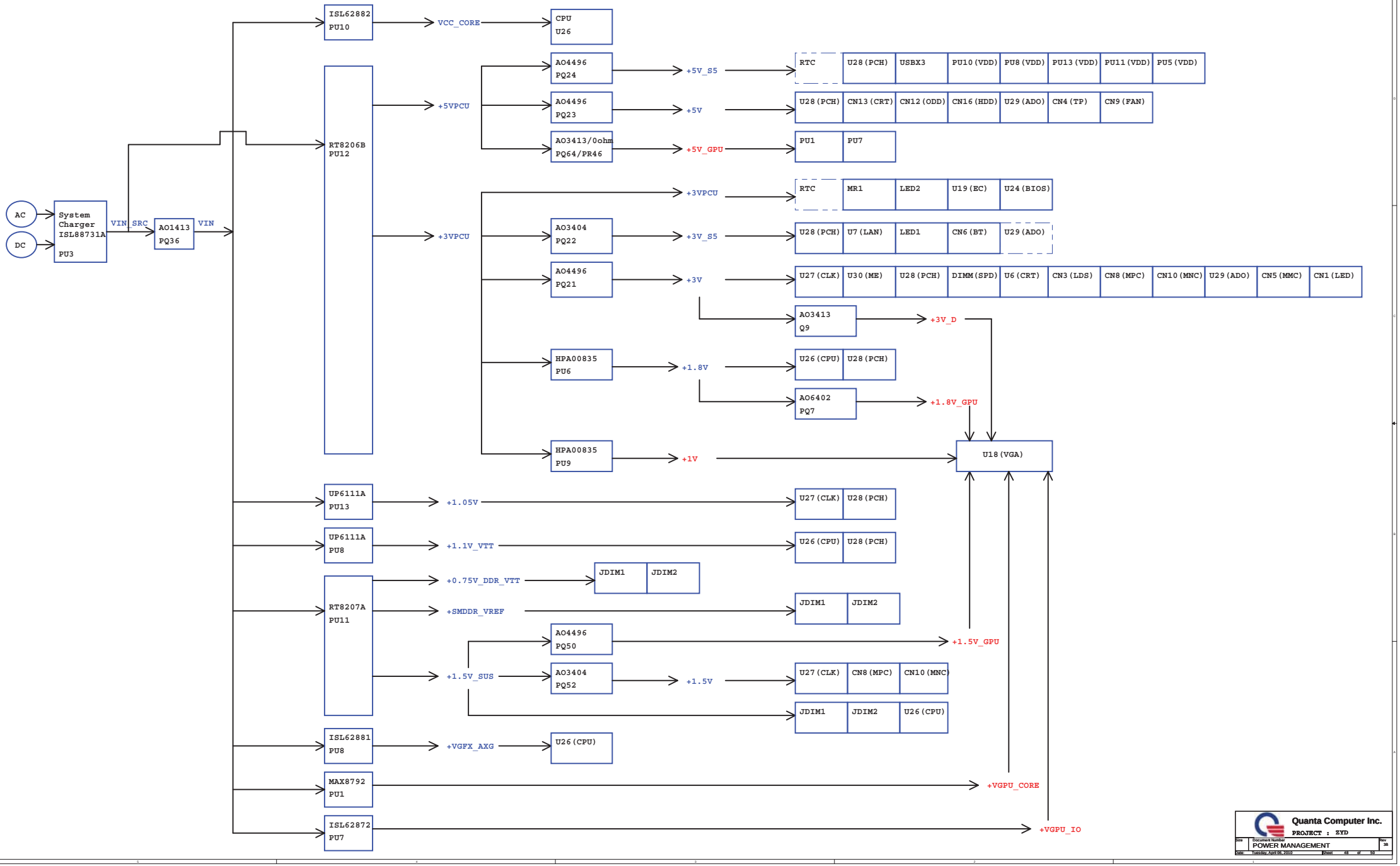




Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	Thermal Protection	3B
Date: Tuesday, April 06, 2010	Sheet 47 of 50	



Model	REV	CHANGE LIST	MODEL	ZYD FROM	ZYD To
ZYD MB	1A	20091028 Page 30, Move the resisters and common chokes from M/B to daughter board		X	1A
		20091028 Page 30, Move the R1027 and R1059 to daughter board and change to 0402 (place closer).		X	1A
		20091028 Page 30, Move USB Power switch to daughter board		X	1A
		20091028 Page 30, Change card reader&USB board CONN P/N to DFFC20FR255		X	1A
		20091028 Page 26, Delete R203 and R171 to leave RJ45 chasiss contact to GND directly		X	1A
		20091028 Page 31, Add net name susled#_R, Pwrled#_R,BATLED0#_R, BATLED1#_R,RFLED#_R,RFLED2#_R		X	1A
		20091028 Page 35, Add SW1 for debug purpose		X	1A
		20091028 Page 33, update Hole footprints		X	1A
		20091029 Page 41, Change PR199, PR200 P/N from CS00003J951 to CS00003F916		X	1A
		20091102 Page 24, 29, Add Mic_GND for internal analog MIC		X	1A
		20091102 Page 27, Delete C204, C208, C558, R411, R385, R373, RP3, Q27, Q26. and change C578 from 0.47u to 4.7u		X	1A
		20091102 Page 10, Stuff R1001, R1002, R503		X	1A
		20091103 Page 33, Delete Hole4, Hole5, Hole8, Hole18		X	1A
		20091104 Page 33, update power schematic		X	1A
		20091104 Page 30, swap L38,L39,L58 USB nets for layout request.		X	1A
		20091108 Page 45, delete net name MAINON_G		X	1A
		20091108 Page 39, Change PR151 P/N from CS24703F908 to CS24023F928 for support Arrandale only		X	1A
		20091108 Page 33, Delete Hole36		X	1A
		20091110 Page 31, Move Wi-Fi LED to PB		X	1A
		20091111 Page 39, Delete Pl8 and Change PL9 footprint and value(1.5uH footprint:CHOKE-ETQP4LR36WFC-NB4)		X	1A
		20091111 Page 41, Stuff +1.5V_GPU power source for EV# only		X	1A
		20091111 Page 37, reserve PR275 for GPU power		X	1A
		20091112 Page 18, Follow ATI suggestion to modify R419 from 680ohm to 51 ohm.		X	1A
		20091112 Page 27, Remove LPC from Mini PCIE port CN24		X	1A
		20091112 Page 37,45, unstuff +3V_SUS components		X	1A
		20091113 Page 27, Two Wi-Fi LED share one net RF_LED#		X	1A
		20091113 Page 31, Delete Q21,Q23, R347		X	1A
		20091113 Page 29, Reserve three more resistors R373, R368, R385 for ESD solution		X	1A
		20091116 Page 34, unstuff PR95, PR96, PQ17, PQ15		X	1A
		20091116 Page 24, Change C650 from 0.22u/6.3V_4 to 0.22u/10V_4		X	1A
		20091116 Page 32, Change C399 from 1U/6.3V_4 to 1u/10V_4		X	1A
		20091116 Page 7, unstuff R159		X	1A
		20091116 Page 11, stuff R592 for DIS and stuff R595 for UMA		X	1A
		20091116 Page 11, Reserve pull low for unused pin dGPU_VRON_R		X	1A
		20091116 Page 8, Delete R414		X	1A
		20091116 Page 25, Delete R162		X	1A
		20091116 Page 36-45, PC14 un-mount; PC207 change P/N; PC154 change P/N and value.; PC155 un-mount; PC180 change P/N; PC119 change P/N; PC118 change P/N		X	1A
	2A	20091119 Page 36, Modify Bat CONN P/N and footprint		1A	2A
		20091119 Page 29, Modify Speaker CN7 P/N from DFHD04MR779 to DFHD04MR057		1A	2A
		20091120 Page 8~13, Modify PCH P/N from AJ0QMGS0T05 to AJSLGZS0T07		1A	2A
		20091124 Page 27, Short Pin42 and Pin44 of CN8 and CN10 to support Intel WiMAX/WiFi combo module		1A	2A
		20091128 Page 37, stuff L36 for discrete sku		1A	2A
		20091128 Page 9, change U30(ME ROM) P/N from AKE391P0N00 to AKE38ZP0N01		1A	2A
		20091202 Page 3, reserve 1U for CLK GEN +1.5V power		1A	2A
		20091203 Page 27, Stuff Q26 and Q28; unstuff R401 and R447; and add LPC bus to CN24 for debug purpose		1A	2A
		20091209 Page 42, add VID table for Park XT		1A	2A
		20091209 Page 3, change R257 from 0ohm to 33ohm		1A	2A
		20091209 Page 3,17,18 follow AMD suggestion to stuff R257, R101, R407,R409 amd remove R36 to fix AMD pre-production silicon bug		1A	2A
		20091214 Page 9, change R317 to a JP and stuff R322		1A	2A
		20091214 Page 32, change CN6 from DFHD05MRD98 to DFWF05MR027		1A	2A
		20091221 Page 29, change R533 from CS03923F916 to CS33922FB15		1A	2A
		20091223 Page 10, change R202, R203, R540, R566, R547 to short pad		1A	2A
		20091223 Page 36, change DC jack P/N to DFHS04FR741		1A	2A
		20091223 Page 32, change CN6 P/N to DFWF05MR012		1A	2A
		20091225 Page 50, change CN19 P/N to DFHD19MR083		1A	2A
		20091230 Page 12, Add C786 for CRT flicker issue		1A	2A
		20091230 Page 27, change transformer footprint to TRF-10-1-24P-SMT		1A	2A
		20091230 Page 17, change VGFU_CORE VID control pin		1A	2A
		20091230 Page 28, Exchange P/N for cn8 and cn10		1A	2A
		20091230 Page 28, Move controller link from CN10 to CN8		1A	2A
	3A	20100129 Page 32, remove power LED MOS Q25		2A	3A
		20100130 Page 18, Remove AMD option 2 workaround for Madison and Park; and change R36 from 1K to 10K		2A	3A
		20100130 Page 28, Change Mini card footprint to MIPCI-800055FB052GX-52P-LDV-NB4		2A	3A
		20100201 Page 32, restore power LED MOS Q25		2A	3A
		20100201 Page 25, Change Q33,Q34 to ESD protection part		2A	3A
		20100222 Page 24, Reserve C787 and C788 for CRT flicker issue		2A	3A
		20100222 Page 36, Remove SW1		2A	3A
		20100222 Page 12, Add C789 for VCCADAC		2A	3A
		20100222 Page 17, Reserve 10U*2 caps for +1.8V_GPU		2A	3A
		20100222 Page 30, Add short Pad R635,R636,R637,R638,R640 for EMI		2A	3A
		20100222 Page 24, unstuff L13 and stuff R89 and R90		2A	3A

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Change list2	3B

Date: Tuesday, April 06, 2010 Sheet 49 of 50

DOC NO.	PROJECT MODEL :	ZYD	APPROVED BY:		DATE:	2010/3/25
	PART NUMBER:		DRAWING BY:		REVISON:	3B

Model	REV	CHANGE LIST
ZYD MB	3B	20100322 Page 32, delete Q25 20100322 Page 44,45 modify PU5,PU7 footprint 20100324 Page 44,45 change PC184,PC179,PC207,PC125,PC236,PC118,PC186 P/N to CC71004MZ04 20100324 Page 43 change PC126, PC24, PC125 to CH5474KEA06(4.7uF 25V 0805) 20100324 Page 30 change R298,R314 to 39ohm 20100325 reserved EMI chock lacation for USB 1/3/11/12/8 20100325 Page 41 change PC226 to 0805 4.7uF/25V,and add PC247 ,BOM stuff. 20100325 Page 30 change R223,R347,C444,R252, R590 and R306 to short pad.

MODEL	ZYD	
	FROM	To
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Change list2	3B

Date: Wednesday, April 07, 2010 Sheet 50 of 50

DOC NO.	PROJECT MODEL :	ZYD	APPROVED BY:		DATE:	2010/3/25
	PART NUMBER:		DRAWING BY:		REVISION:	3B