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| 13 | PCH DMI/PCIE/USB |
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| 18 | PCH POWER |
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| 22 | HDMI |
| 23 | SIO IT8613E |
| 24 | SATA/FAN |
| 25 | REAR USB |
| 26 | FRONT USB |
| 27 | LAN RTL8111H/8106E |
| 28 | AUDIO CODEC ALC887 |
| 29 | AUDIO CONNECTOR |
| 30 | ACPI POWER |
| 31 | MEMORY DC-DC |
| 32 | V_1P0_PCH |
| 33 | RESUME RESET LOGIC |
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| 36 | SPI ROM/RTC/BAT |
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| 39 | RT3606_PHASE |
| 40 | BOM |

# IH11D-MHS VER 7.0

## CPU:

Intel Skylake S 42 in LGA1151 Package 80W

## System Chipset:

H110

## Main Memory:

Dual Channel/DDR-III*2(Max 16GB) 1066/1333/1600

## Onboard Device:

Super I/O:IT8613E

LAN:Realtek 8111H

HD Codec:ALC887

## Power solution:

CPU Voltage Regulators:3phase by RT3606

GT Voltage Regulators:1phase by RT3606

DDR Voltage Regulators:1Phase by UP1514

## Expansion Slots:

PCI EXPRESS 16X SLOT *1

PCI EXPRESS 1X SLOT *1

## REAR IO:

PS/2 PORT

HDMI Port

VGA Port

USB3.0 PORT

Gb RJ-45 +2 layer USB2.0 Port

Audio Jackets (3 PORT)

## Front I/O:

SATA3 *4

USB 2.0 Header * 2

USB 3.0 Header * 1

CPU FAN *1

System FAN *1

Front Audio Header

TPM14 Header * 1

HW ELI



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| | | |
|---|---|---|
| Title: INDEX | | |
| Size: B | Document Number: IH11D-MHS | Rev: 7.0 |
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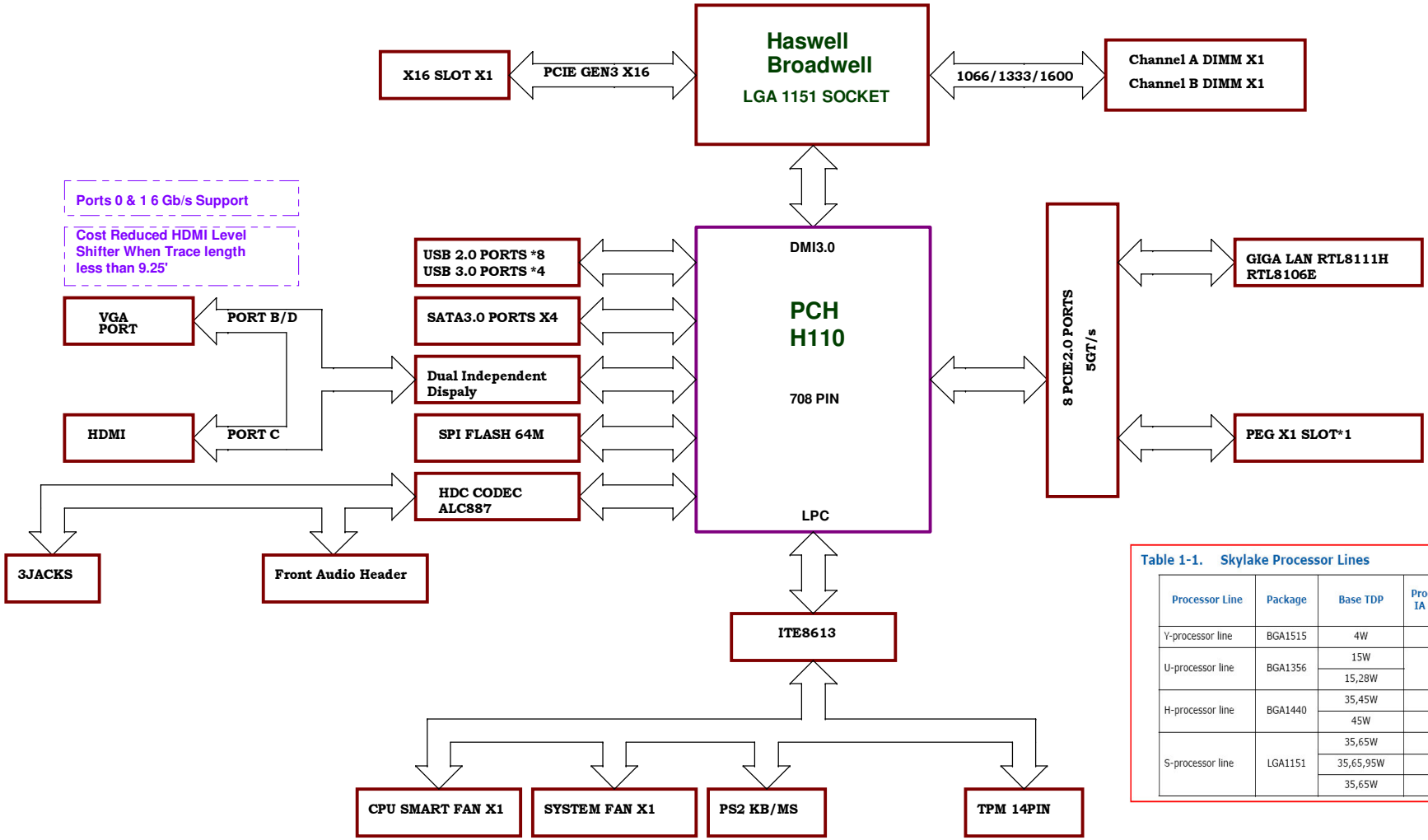


Table 1-1. Skylake Processor Lines

| Processor Line | Package | Base TDP | Processor IA Cores | Maximum Graphics Configuration | On Package Cache | Platform Type |
|---|---|---|---|---|---|---|
| Y-processor line | BGA1515 | 4W | 2 | GT2 | N/A | 1-Chip |
| U-processor line | BGA1356 | 15W | 2 | GT2 | N/A | 1-Chip |
| | | 15,28W | | GT3 | 64 MB | |
| H-processor line | BGA1440 | 35,45W | 4 | GT2 | N/A | 2-Chip |
| | | 45W | 4 | GT4 | 128 MB | |
| S-processor line | LGA1151 | 35,65W | 2 | GT2 | N/A | 2-Chip |
| | | 35,65,95W | 4 | GT2 | | |
| | | 35,65W | 4 | GT4 | 64 MB | |



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Title: BLOCK DIAGRAM

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| Title | POWER DELIVERY | |
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1.VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

2.VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

3.VER0.60:CHANGE CPU POWER CONN TO 2*2(PAGE39)

4.VER0.60:NEW ADD COLAY FOR V_SA_IO(PAGE38)

5.VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

6.VER0.6:COST DOWN(REMOVE CT6)(PAGE26)

7.VER0.6:COST DOWN(MODIFY F6/GF3 SIZE)(PAGE21/34)

8.VER0.6:COST DOWN(MODIFY MC36 SIZE)(PAGE11)

9.VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF)(PAGE31/32)

10.VER0.6:COST DOWN(MC38 /NI)(PAGE11)

11.VER0.6:COST DOWN(YC23 /NI)(PAGE18)

12.VER0.6:COST DOWN(YC16/17/21 /NI)(PAGE18)

13.VER0.6:COST DOWN(LC18/MC5/6 CHANGE TO 10UF 0603 SIZE)(PAGE11/27)

14.VER0.6:COST DOWN(PC155 CHANGE TO 10UF 0603 SIZE)(PAGE39)

15.VER0.6:COST DOWN(C165/MC9 CHANGE TO 1UF 0805 SIZE)(PAGE31/38)

16.VER0.6:COST DOWN(YC11/26 /NI)(PAGE18)

17.VER0.6:COST DOWN(CHANGE TO RN 8P4R)(PAGE17)

18.VER0.6:ATXPG MODIFY(PAGE23/36)

19.VER0.6:COST DOWN(PAGE33)

20.VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904)(PAGE30/33/39)

21.VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)

22.VER0.6:COST DOWN(SHORT 0805)(PAGE18/37/39/40)

23.VER0.6:COST DOWN(BEAD COLAY)(PAGE29)

24.VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606)(PAGE39/40/41)

25.VER0.6:COST DOWN(POWER_JUSB4/POWER_JUSB5 COLAY)(PAGE25/34)

26.VER0.6:MIC MODIFY BY KEVIN(PAGE28)

27.VER0.6:ACPI MODIFY BY KEVIN(PAGE30)



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Title: CHANGELIST

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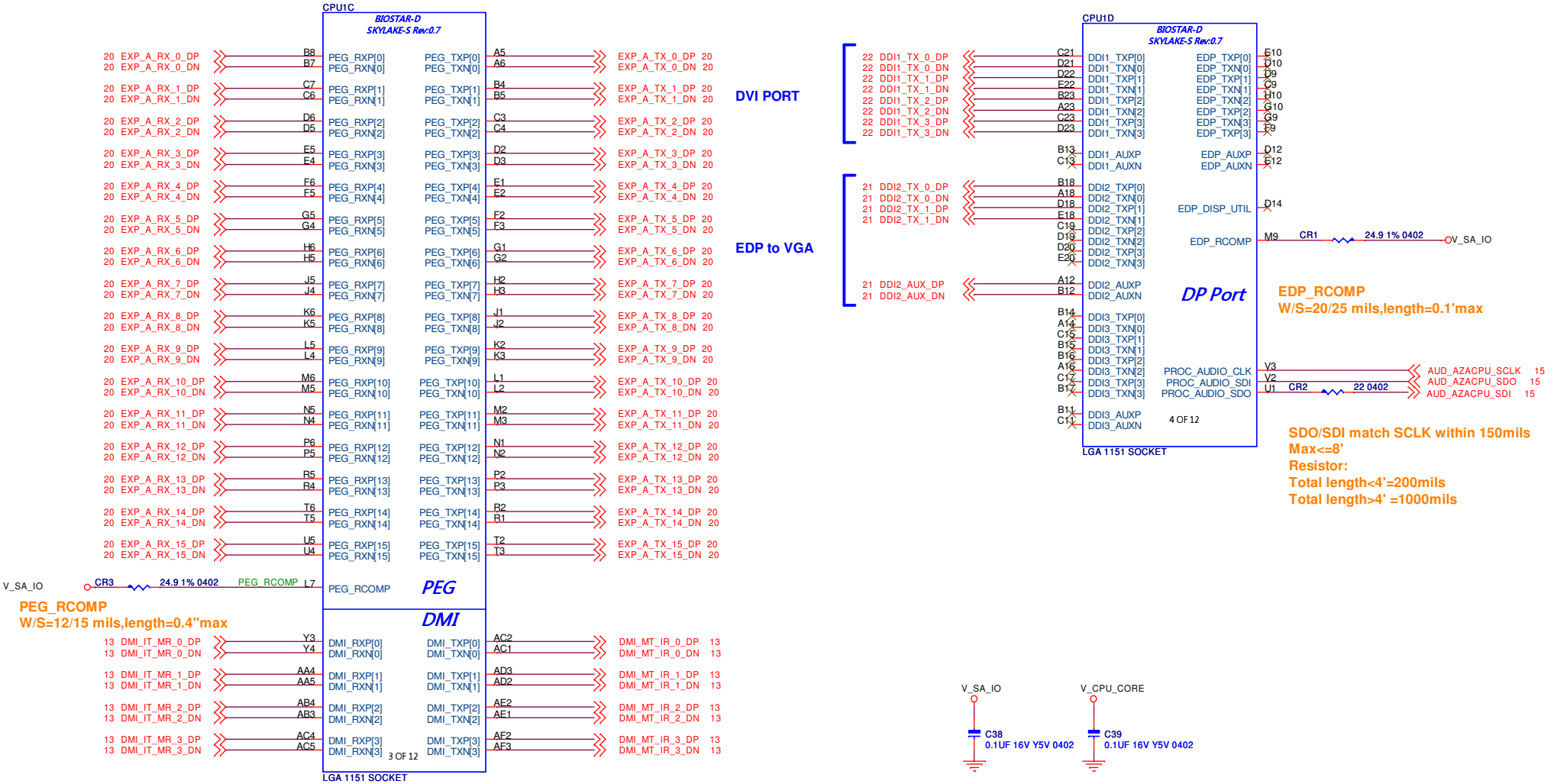


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Title: CPU PCIEX16/DMI/FDI

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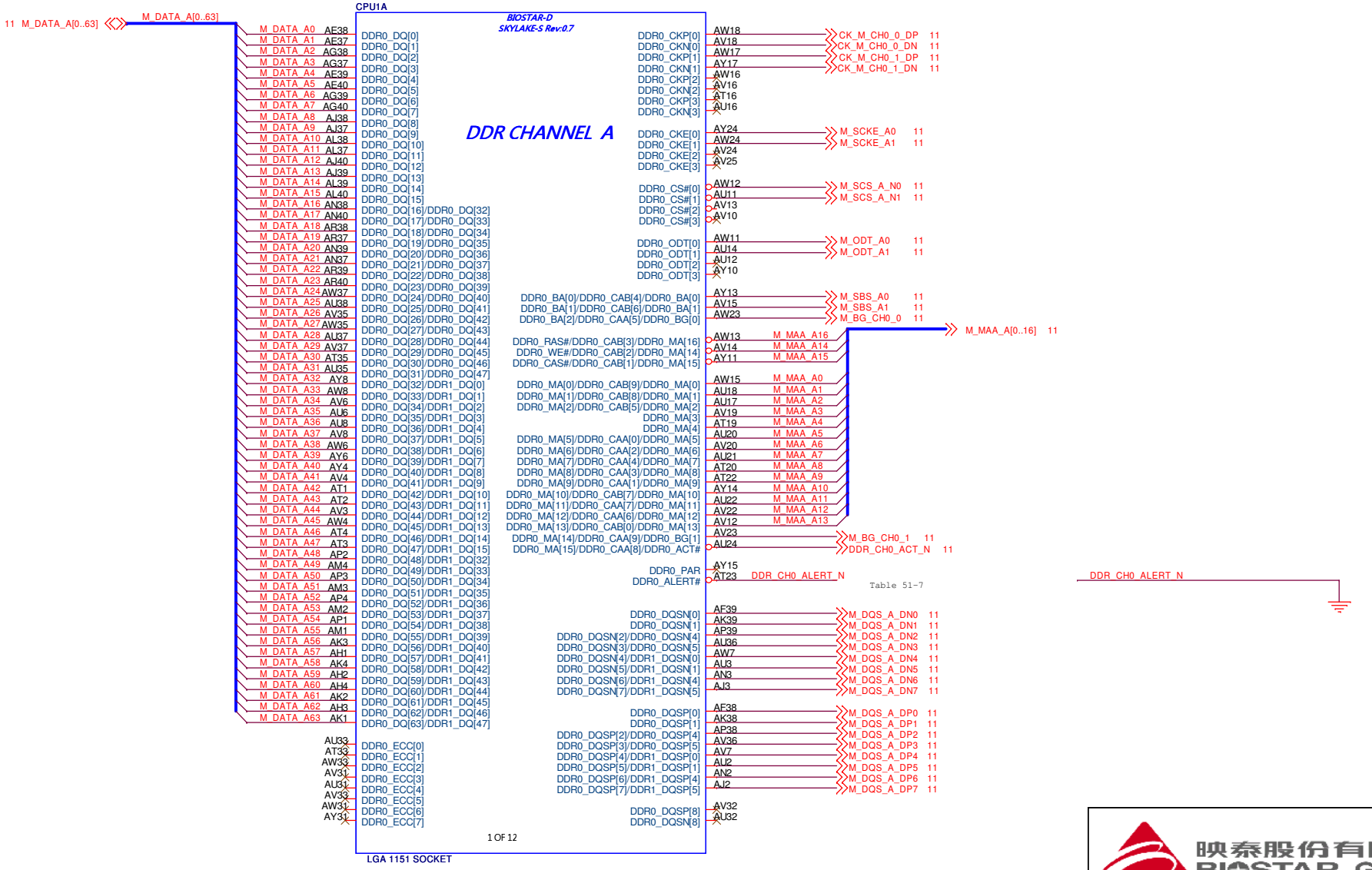


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| | | |
|---|---|---|
| Title | CPU DDR3 CHANNEL A | |
| Size B | Document Number IH11D-MHS | Rev 7.0 |
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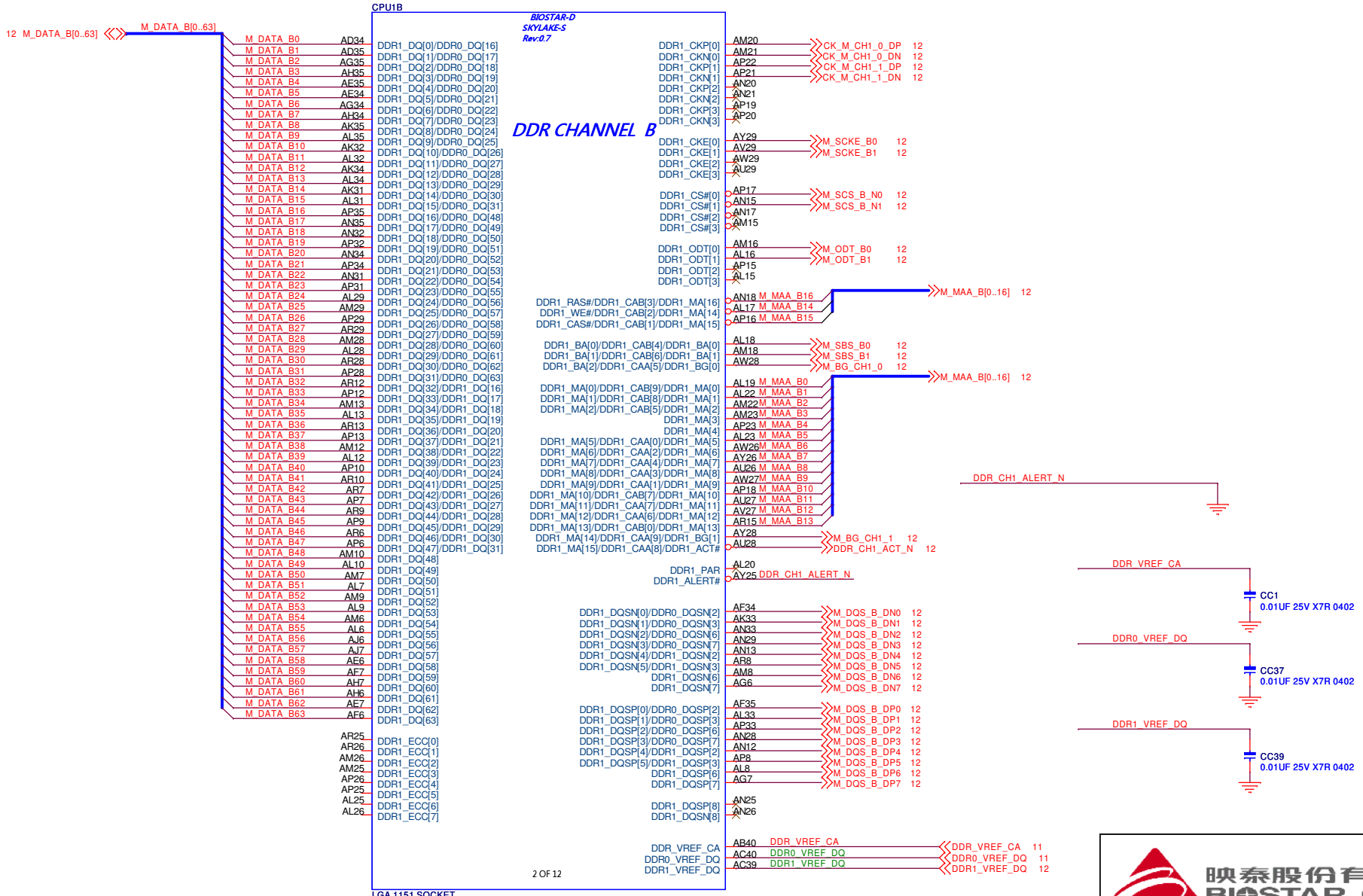
CPU1B
BIOSTAR-D
SKYLAKE-S
Rev:0.7
DDR CHANNEL B
2 OF 12
LGA 1151 SOCKET
12 M_DATA_B[0..63]
M_DATA_B[0..63]
M_DATA_B0 AD34 DDR1_DQ[0]/DDR0_DQ[16]
M_DATA_B1 AD35 DDR1_DQ[1]/DDR0_DQ[17]
M_DATA_B2 AG35 DDR1_DQ[2]/DDR0_DQ[18]
M_DATA_B3 AH35 DDR1_DQ[3]/DDR0_DQ[19]
M_DATA_B4 AE35 DDR1_DQ[4]/DDR0_DQ[20]
M_DATA_B5 AE34 DDR1_DQ[5]/DDR0_DQ[21]
M_DATA_B6 AG34 DDR1_DQ[6]/DDR0_DQ[22]
M_DATA_B7 AH34 DDR1_DQ[7]/DDR0_DQ[23]
M_DATA_B8 AK35 DDR1_DQ[8]/DDR0_DQ[24]
M_DATA_B9 AL35 DDR1_DQ[9]/DDR0_DQ[25]
M_DATA_B10 AK32 DDR1_DQ[10]/DDR0_DQ[26]
M_DATA_B11 AL32 DDR1_DQ[11]/DDR0_DQ[27]
M_DATA_B12 AK34 DDR1_DQ[12]/DDR0_DQ[28]
M_DATA_B13 AL34 DDR1_DQ[13]/DDR0_DQ[29]
M_DATA_B14 AK31 DDR1_DQ[14]/DDR0_DQ[30]
M_DATA_B15 AL31 DDR1_DQ[15]/DDR0_DQ[31]
M_DATA_B16 AP35 DDR1_DQ[16]/DDR0_DQ[48]
M_DATA_B17 AN35 DDR1_DQ[17]/DDR0_DQ[49]
M_DATA_B18 AN32 DDR1_DQ[18]/DDR0_DQ[50]
M_DATA_B19 AP32 DDR1_DQ[19]/DDR0_DQ[51]
M_DATA_B20 AN34 DDR1_DQ[20]/DDR0_DQ[52]
M_DATA_B21 AP34 DDR1_DQ[21]/DDR0_DQ[53]
M_DATA_B22 AN31 DDR1_DQ[22]/DDR0_DQ[54]
M_DATA_B23 AP31 DDR1_DQ[23]/DDR0_DQ[55]
M_DATA_B24 AL29 DDR1_DQ[24]/DDR0_DQ[56]
M_DATA_B25 AM29 DDR1_DQ[25]/DDR0_DQ[57]
M_DATA_B26 AP29 DDR1_DQ[26]/DDR0_DQ[58]
M_DATA_B27 AR29 DDR1_DQ[27]/DDR0_DQ[59]
M_DATA_B28 AM28 DDR1_DQ[28]/DDR0_DQ[60]
M_DATA_B29 AL28 DDR1_DQ[29]/DDR0_DQ[61]
M_DATA_B30 AR28 DDR1_DQ[30]/DDR0_DQ[62]
M_DATA_B31 AP28 DDR1_DQ[31]/DDR0_DQ[63]
M_DATA_B32 AR12 DDR1_DQ[32]/DDR1_DQ[16]
M_DATA_B33 AP12 DDR1_DQ[33]/DDR1_DQ[17]
M_DATA_B34 AM13 DDR1_DQ[34]/DDR1_DQ[18]
M_DATA_B35 AL13 DDR1_DQ[35]/DDR1_DQ[19]
M_DATA_B36 AR13 DDR1_DQ[36]/DDR1_DQ[20]
M_DATA_B37 AP13 DDR1_DQ[37]/DDR1_DQ[21]
M_DATA_B38 AM12 DDR1_DQ[38]/DDR1_DQ[22]
M_DATA_B39 AL12 DDR1_DQ[39]/DDR1_DQ[23]
M_DATA_B40 AP10 DDR1_DQ[40]/DDR1_DQ[24]
M_DATA_B41 AR10 DDR1_DQ[41]/DDR1_DQ[25]
M_DATA_B42 AR7 DDR1_DQ[42]/DDR1_DQ[26]
M_DATA_B43 AP7 DDR1_DQ[43]/DDR1_DQ[27]
M_DATA_B44 AR9 DDR1_DQ[44]/DDR1_DQ[28]
M_DATA_B45 AP9 DDR1_DQ[45]/DDR1_DQ[29]
M_DATA_B46 AR6 DDR1_DQ[46]/DDR1_DQ[30]
M_DATA_B47 AP6 DDR1_DQ[47]/DDR1_DQ[31]
M_DATA_B48 AM10 DDR1_DQ[48]
M_DATA_B49 AL10 DDR1_DQ[49]
M_DATA_B50 AM7 DDR1_DQ[50]
M_DATA_B51 AL7 DDR1_DQ[51]
M_DATA_B52 AM9 DDR1_DQ[52]
M_DATA_B53 AL9 DDR1_DQ[53]
M_DATA_B54 AM6 DDR1_DQ[54]
M_DATA_B55 AL6 DDR1_DQ[55]
M_DATA_B56 AJ6 DDR1_DQ[56]
M_DATA_B57 AJ7 DDR1_DQ[57]
M_DATA_B58 AE6 DDR1_DQ[58]
M_DATA_B59 AF7 DDR1_DQ[59]
M_DATA_B60 AH7 DDR1_DQ[60]
M_DATA_B61 AH6 DDR1_DQ[61]
M_DATA_B62 AE7 DDR1_DQ[62]
M_DATA_B63 AF6 DDR1_DQ[63]
AR25 DDR1_ECC[0]
AR26 DDR1_ECC[1]
AM26 DDR1_ECC[2]
AM25 DDR1_ECC[3]
AP26 DDR1_ECC[4]
AP25 DDR1_ECC[5]
AL25 DDR1_ECC[6]
AL26 DDR1_ECC[7]
DDR1_CKP[0] AM20 CK_M_CH1_0_DP 12
DDR1_CKN[0] AM21 CK_M_CH1_0_DN 12
DDR1_CKP[1] AP22 CK_M_CH1_1_DP 12
DDR1_CKN[1] AP21 CK_M_CH1_1_DN 12
DDR1_CKP[2] AN20
DDR1_CKN[2] AN21
DDR1_CKP[3] AP19
DDR1_CKN[3] AP20
DDR1_CKE[0] AY29 M_SCKE_B0 12
DDR1_CKE[1] AV29 M_SCKE_B1 12
DDR1_CKE[2] AW29
DDR1_CKE[3] AU29
DDR1_CS#[0] AP17 M_SCS_B_N0 12
DDR1_CS#[1] AN15 M_SCS_B_N1 12
DDR1_CS#[2] AN17
DDR1_CS#[3] AM15
DDR1_ODT[0] AM16 M_ODT_B0 12
DDR1_ODT[1] AL16 M_ODT_B1 12
DDR1_ODT[2] AP15
DDR1_ODT[3] AL15
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AN18 M_MAA_B16
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AL17 M_MAA_B14
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AP16 M_MAA_B15
M_MAA_B[0..16] 12
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] AL18 M_SBS_B0 12
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] AM18 M_SBS_B1 12
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AW28 M_BG_CH1_0 12
M_MAA_B[0..16] 12
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] AL19 M_MAA_B0
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AL22 M_MAA_B1
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AM22 M_MAA_B2
DDR1_MA[3] AM23 M_MAA_B3
DDR1_MA[4] AP23 M_MAA_B4
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AL23 M_MAA_B5
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] AW26 M_MAA_B6
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AY26 M_MAA_B7
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] AU26 M_MAA_B8
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AW27 M_MAA_B9
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AP18 M_MAA_B10
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AU27 M_MAA_B11
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AV27 M_MAA_B12
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] AR15 M_MAA_B13
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AY28 M_BG_CH1_1 12
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AU28 DDR_CH1_ACT_N 12
DDR_CH1_ALERT_N
DDR1_PAR AL20
DDR1_ALERT# AY25 DDR_CH1_ALERT_N
DDR_VREF_CA
CC1
0.01UF 25V X7R 0402
DDR0_VREF_DQ
CC37
0.01UF 25V X7R 0402
DDR1_VREF_DQ
CC39
0.01UF 25V X7R 0402
DDR1_DQSN[0]/DDR0_DQSN[2] AF34 M_DQS_B_DN0 12
DDR1_DQSN[1]/DDR0_DQSN[3] AK33 M_DQS_B_DN1 12
DDR1_DQSN[2]/DDR0_DQSN[6] AN33 M_DQS_B_DN2 12
DDR1_DQSN[3]/DDR0_DQSN[7] AN29 M_DQS_B_DN3 12
DDR1_DQSN[4]/DDR1_DQSN[2] AN13 M_DQS_B_DN4 12
DDR1_DQSN[5]/DDR1_DQSN[3] AR8 M_DQS_B_DN5 12
DDR1_DQSN[6] AM8 M_DQS_B_DN6 12
DDR1_DQSN[7] AG6 M_DQS_B_DN7 12
DDR1_DQSP[0]/DDR0_DQSP[2] AF35 M_DQS_B_DP0 12
DDR1_DQSP[1]/DDR0_DQSP[3] AL33 M_DQS_B_DP1 12
DDR1_DQSP[2]/DDR0_DQSP[6] AP33 M_DQS_B_DP2 12
DDR1_DQSP[3]/DDR0_DQSP[7] AN28 M_DQS_B_DP3 12
DDR1_DQSP[4]/DDR1_DQSP[2] AN12 M_DQS_B_DP4 12
DDR1_DQSP[5]/DDR1_DQSP[3] AP8 M_DQS_B_DP5 12
DDR1_DQSP[6] AL8 M_DQS_B_DP6 12
DDR1_DQSP[7] AG7 M_DQS_B_DP7 12
DDR1_DQSP[8] AN25
DDR1_DQSN[8] AN26
DDR_VREF_CA AB40 DDR_VREF_CA DDR_VREF_CA 11
DDR0_VREF_DQ AC40 DDR0_VREF_DQ DDR0_VREF_DQ 11
DDR1_VREF_DQ AC39 DDR1_VREF_DQ DDR1_VREF_DQ 12
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Title
CPU DDR3 CHANNEL B
Size B
Document Number
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Date: Thursday, November 19, 2015
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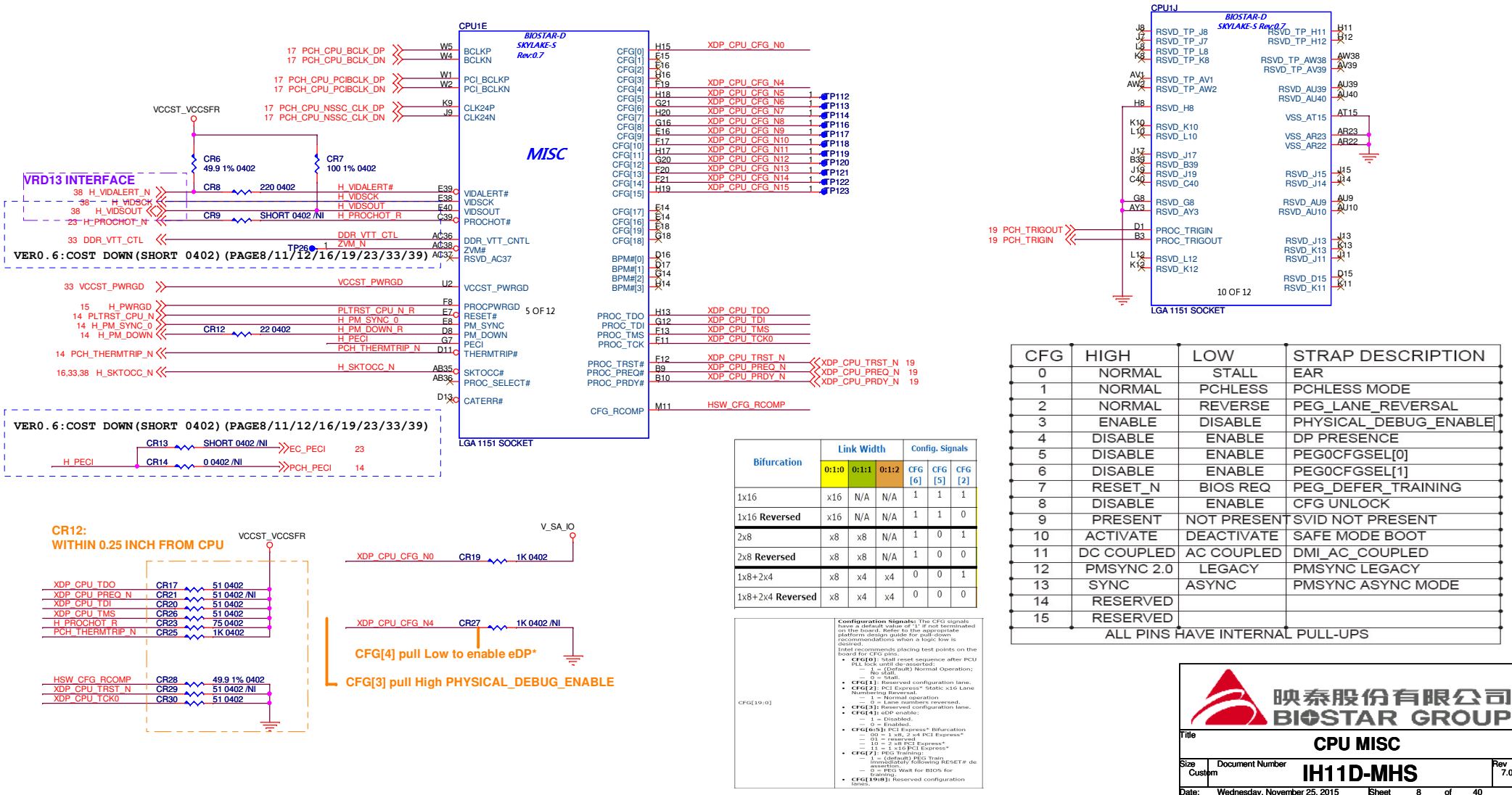


| Bifurcation | Link Width | | | Config. Signals | | |
|---|---|---|---|---|---|---|
| | 0:1:0 | 0:1:1 | 0:1:2 | CFG [6] | CFG [5] | CFG [2] |
| 1x16 | x16 | N/A | N/A | 1 | 1 | 1 |
| 1x16 **Reversed** | x16 | N/A | N/A | 1 | 1 | 0 |
| 2x8 | x8 | x8 | N/A | 1 | 0 | 1 |
| 2x8 **Reversed** | x8 | x8 | N/A | 1 | 0 | 0 |
| 1x8+2x4 | x8 | x4 | x4 | 0 | 0 | 1 |
| 1x8+2x4 **Reversed** | x8 | x4 | x4 | 0 | 0 | 0 |

CFG[19:0]

**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.

- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted.
  — 1 = (Default) Normal Operation; No stall.
  — 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  — 1 = Normal operation
  — 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  — 1 = Disabled.
  — 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  — 00 = 1 x8, 2 x4 PCI Express*
  — 01 = reserved
  — 10 = 2 x8 PCI Express*
  — 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
  — 1 = (default) PEG Train immediately following RESET# de-assertion.
  — 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

| CFG | HIGH | LOW | STRAP DESCRIPTION |
|---|---|---|---|
| 0 | NORMAL | STALL | EAR |
| 1 | NORMAL | PCHLESS | PCHLESS MODE |
| 2 | NORMAL | REVERSE | PEG_LANE_REVERSAL |
| 3 | ENABLE | DISABLE | PHYSICAL_DEBUG_ENABLE |
| 4 | DISABLE | ENABLE | DP PRESENCE |
| 5 | DISABLE | ENABLE | PEG0CFGSEL[0] |
| 6 | DISABLE | ENABLE | PEG0CFGSEL[1] |
| 7 | RESET_N | BIOS REQ | PEG_DEFER_TRAINING |
| 8 | DISABLE | ENABLE | CFG UNLOCK |
| 9 | PRESENT | NOT PRESENT | SVID NOT PRESENT |
| 10 | ACTIVATE | DEACTIVATE | SAFE MODE BOOT |
| 11 | DC COUPLED | AC COUPLED | DMI_AC_COUPLED |
| 12 | PMSYNC 2.0 | LEGACY | PMSYNC LEGACY |
| 13 | SYNC | ASYNC | PMSYNC ASYNC MODE |
| 14 | RESERVED | | |
| 15 | RESERVED | | |
| ALL PINS HAVE INTERNAL PULL-UPS | | | |

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| | | |
|---|---|---|
| Title | CPU MISC | |
| Size: Custom | Document Number: IH11D-MHS | Rev: 7.0 |
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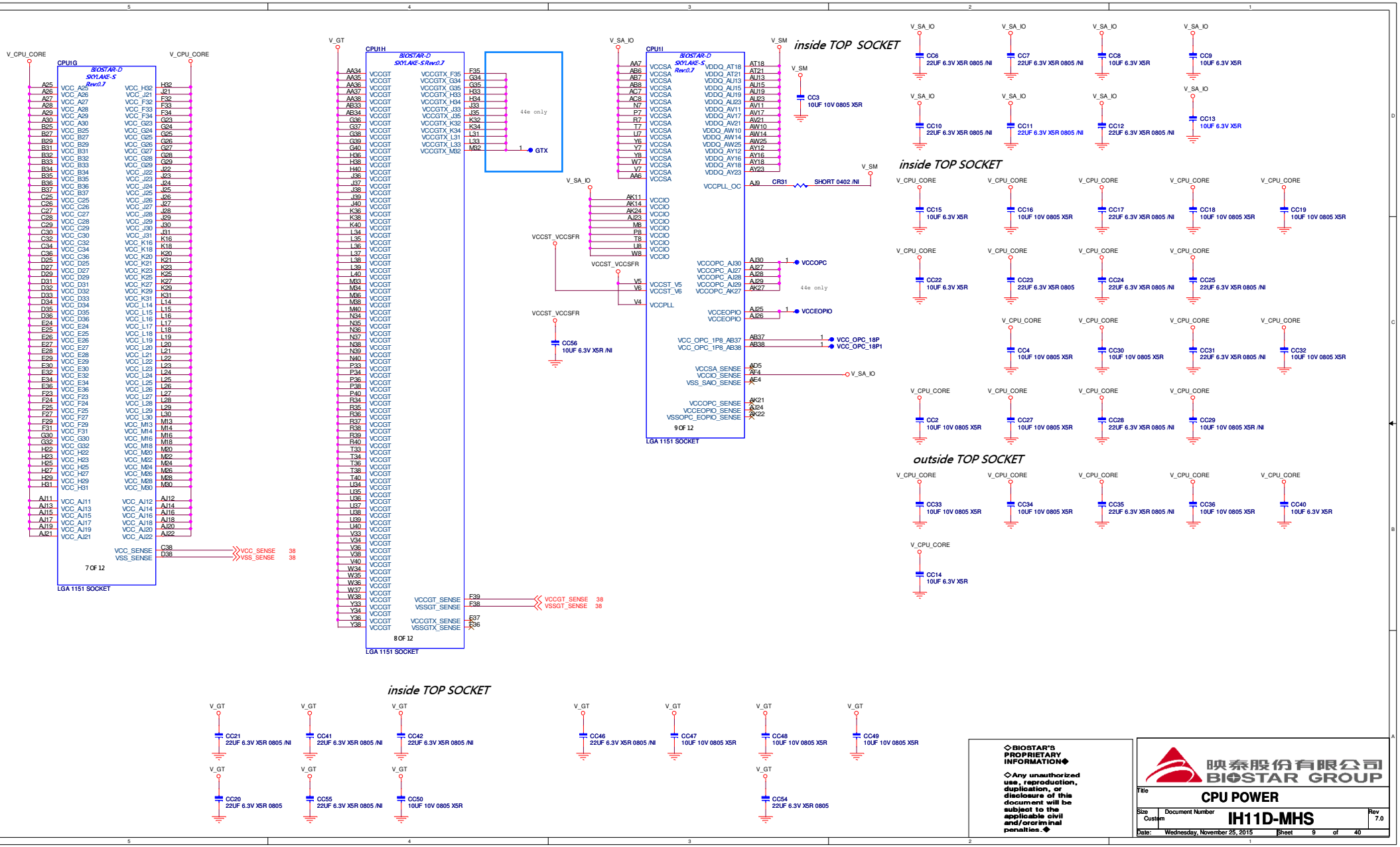
CPU1G
BIOSTAR-D SKYLAKE-S Rev0.7
LGA 1151 SOCKET
7 OF 12
CPU1H
BIOSTAR-D SKYLAKE-S Rev0.7
LGA 1151 SOCKET
8 OF 12
CPU1I
BIOSTAR-D SKYLAKE-S Rev0.7
LGA 1151 SOCKET
9 OF 12
inside TOP SOCKET
outside TOP SOCKET
44e only
SHORT 0402 /NI
CC3 10UF 10V 0805 X5R
CC56 10UF 6.3V X5R /NI
CC6 22UF 6.3V X5R 0805 /NI
CC7 22UF 6.3V X5R 0805 /NI
CC8 10UF 6.3V X5R
CC9 10UF 6.3V X5R
CC10 22UF 6.3V X5R 0805 /NI
CC11 22UF 6.3V X5R 0805 /NI
CC12 22UF 6.3V X5R 0805 /NI
CC13 10UF 6.3V X5R
CC15 10UF 6.3V X5R
CC16 10UF 10V 0805 X5R
CC17 22UF 6.3V X5R 0805 /NI
CC18 10UF 10V 0805 X5R
CC19 10UF 10V 0805 X5R
CC22 10UF 6.3V X5R
CC23 22UF 6.3V X5R 0805
CC24 22UF 6.3V X5R 0805 /NI
CC25 22UF 6.3V X5R 0805 /NI
CC4 10UF 10V 0805 X5R
CC30 10UF 10V 0805 X5R
CC31 22UF 6.3V X5R 0805 /NI
CC32 10UF 10V 0805 X5R
CC2 10UF 10V 0805 X5R
CC27 10UF 10V 0805 X5R
CC28 22UF 6.3V X5R 0805 /NI
CC29 10UF 10V 0805 X5R /NI
CC33 10UF 10V 0805 X5R
CC34 10UF 10V 0805 X5R
CC35 22UF 6.3V X5R 0805 /NI
CC36 10UF 10V 0805 X5R
CC40 10UF 6.3V X5R
CC14 10UF 6.3V X5R
CC21 22UF 6.3V X5R 0805 /NI
CC41 22UF 6.3V X5R 0805 /NI
CC42 22UF 6.3V X5R 0805 /NI
CC20 22UF 6.3V X5R 0805
CC55 22UF 6.3V X5R 0805 /NI
CC50 10UF 10V 0805 X5R
CC46 22UF 6.3V X5R 0805 /NI
CC47 10UF 10V 0805 X5R
CC48 10UF 10V 0805 X5R
CC54 22UF 6.3V X5R 0805
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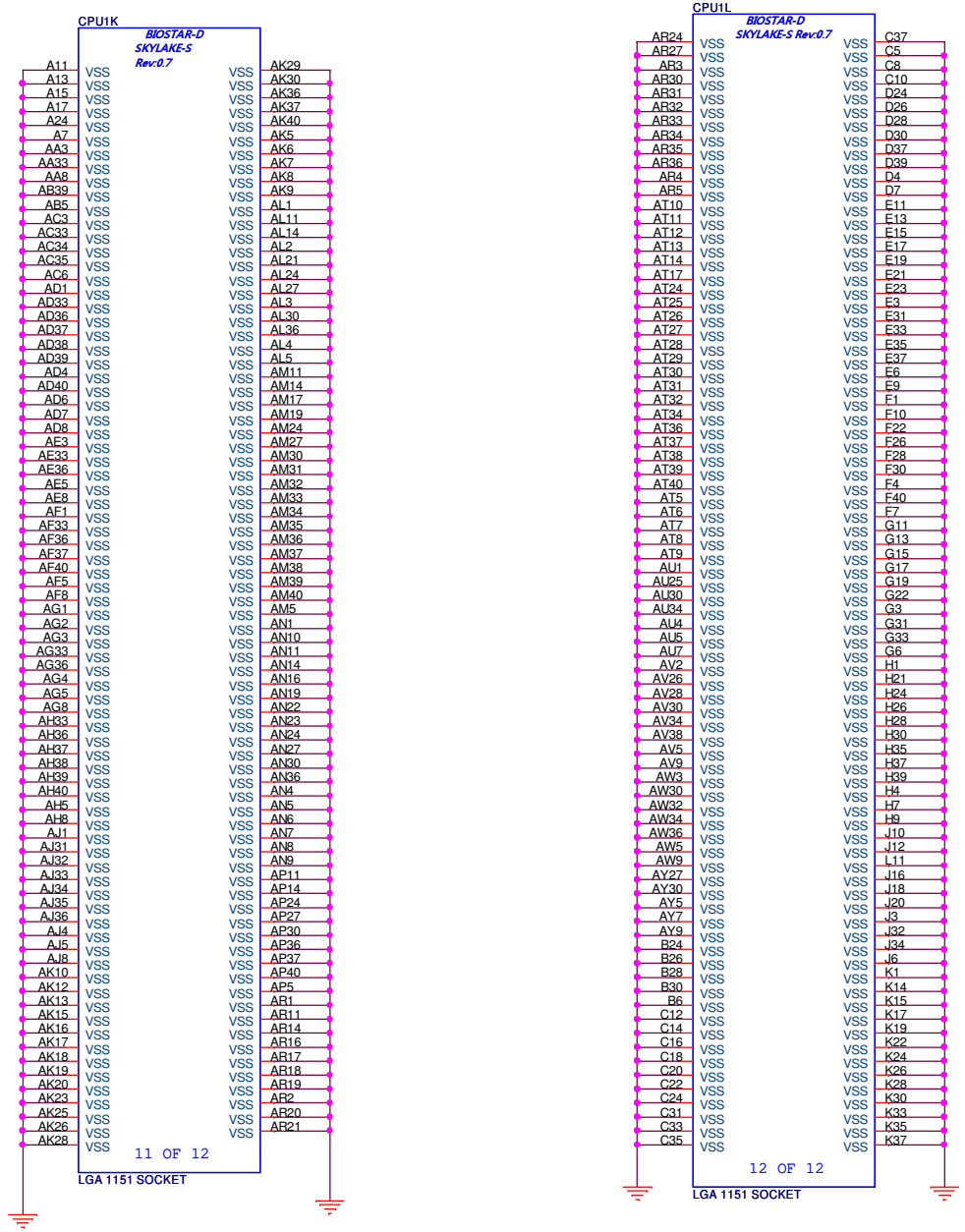
Title
CPU POWER
Size Custem
Document Number
IH11D-MHS
Rev 7.0
Date: Wednesday, November 25, 2015
Sheet 9 of 40



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Title: CPU GND

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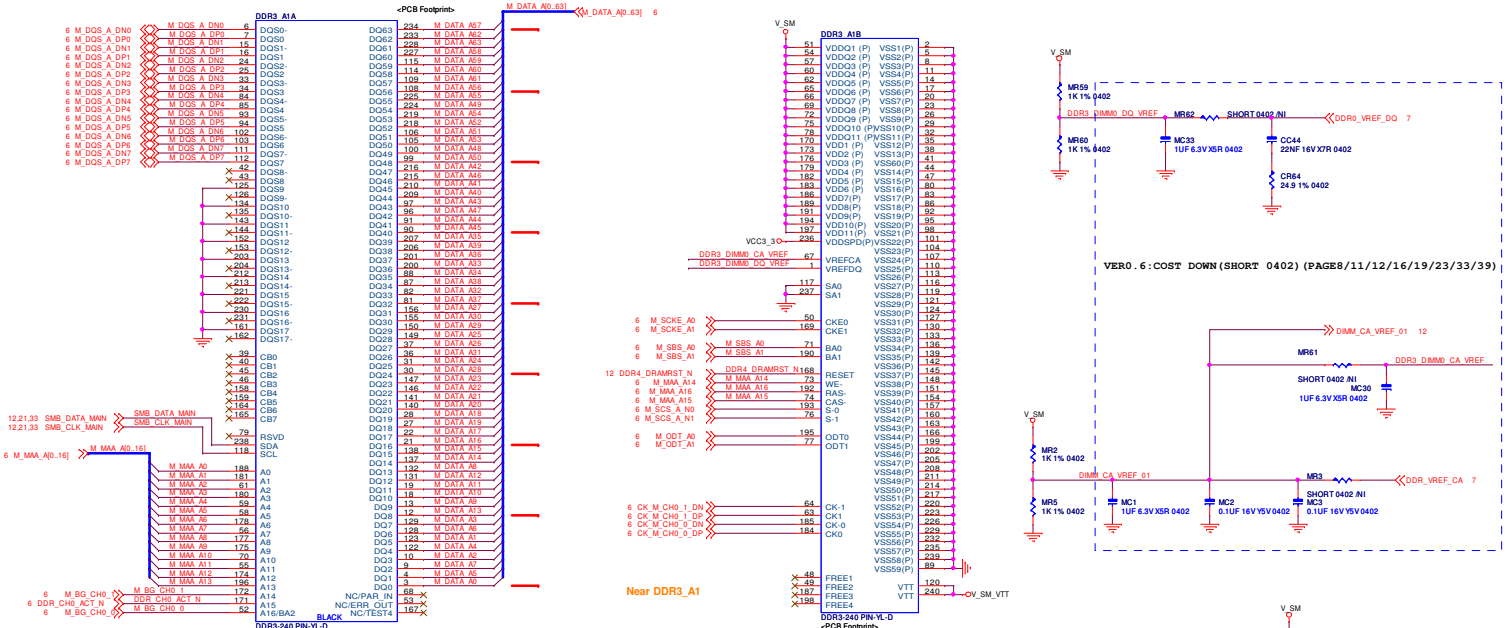
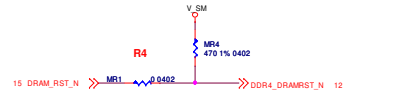
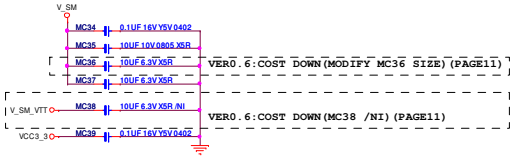


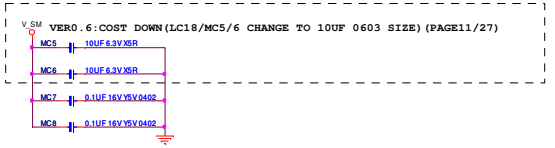







*DIMM1(CHANNEL-A1)*
*ADDRESS = 0:0:0 [SA2:SA1:SA0]*
*DIMM1 CH0 ADDRESS HEX:0XA0*



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Title: DDR3L DIMMA1

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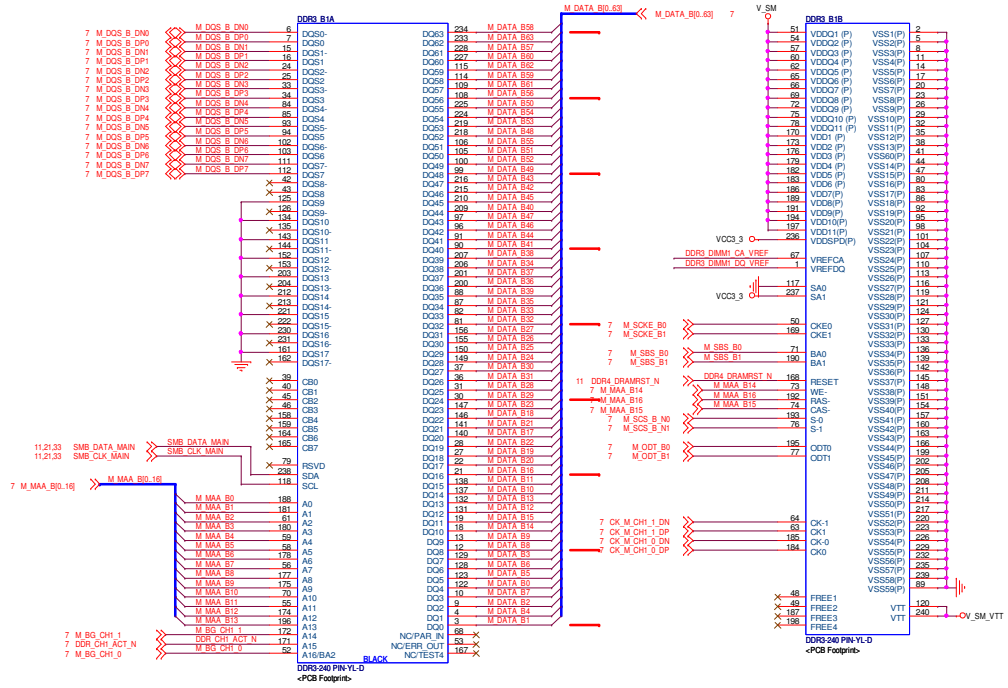


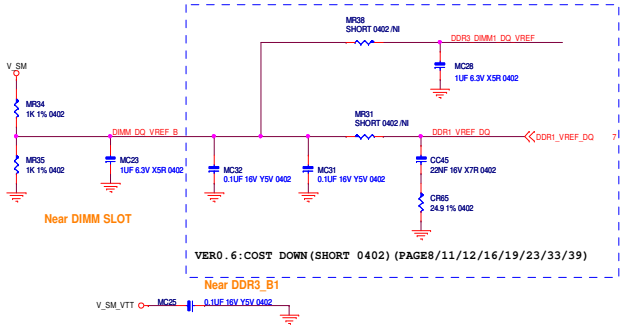


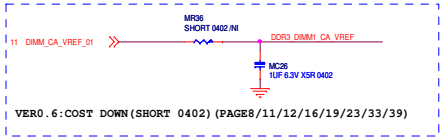




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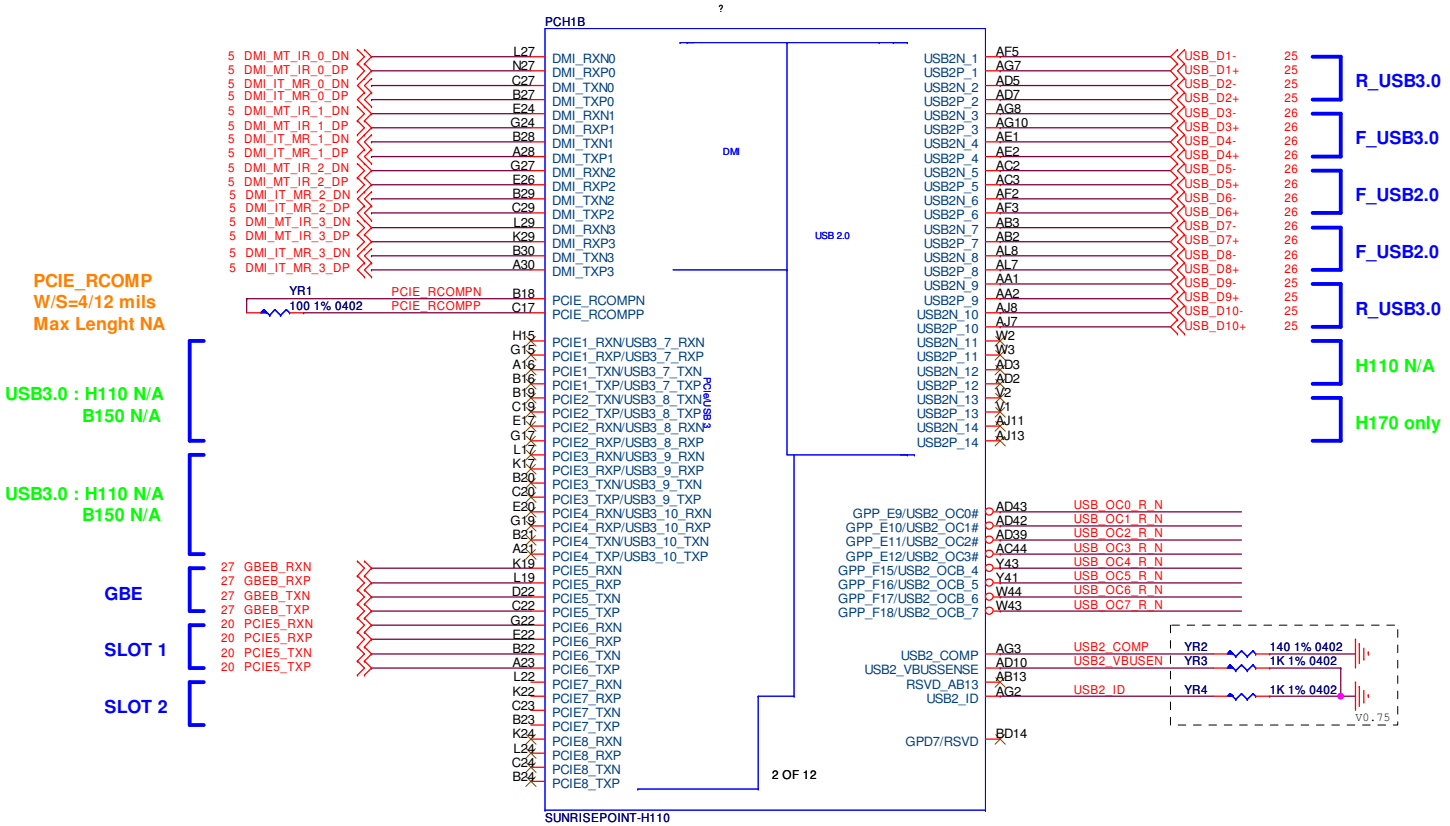
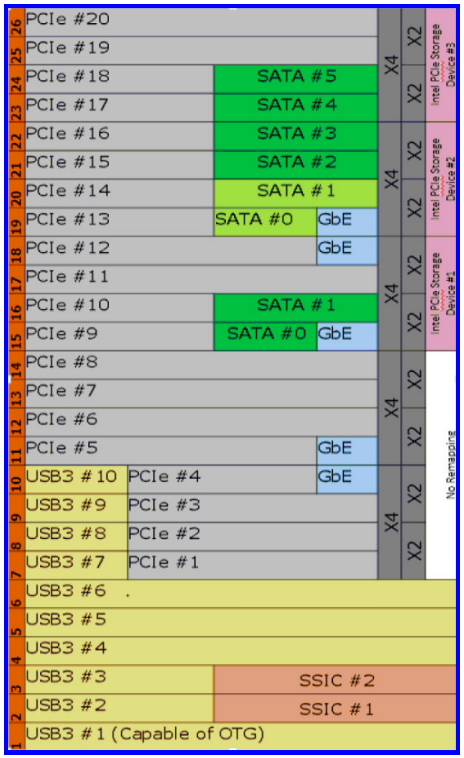
| | | |
|---|---|---|
| Title | DDR3L DIMMB1 | |
| Size: Custom | Document Number: IH11D-MHS | Rev: 7.0 |
| Date: Thursday, November 19, 2015 | Sheet 12 of 40 | |

# PCH PART: Y+Reference




| | |
|---|---|
| Title | PCH DMI/PCIE/USB |
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| Date: Thursday, November 19, 2015 | Sheet 13 of 40 |

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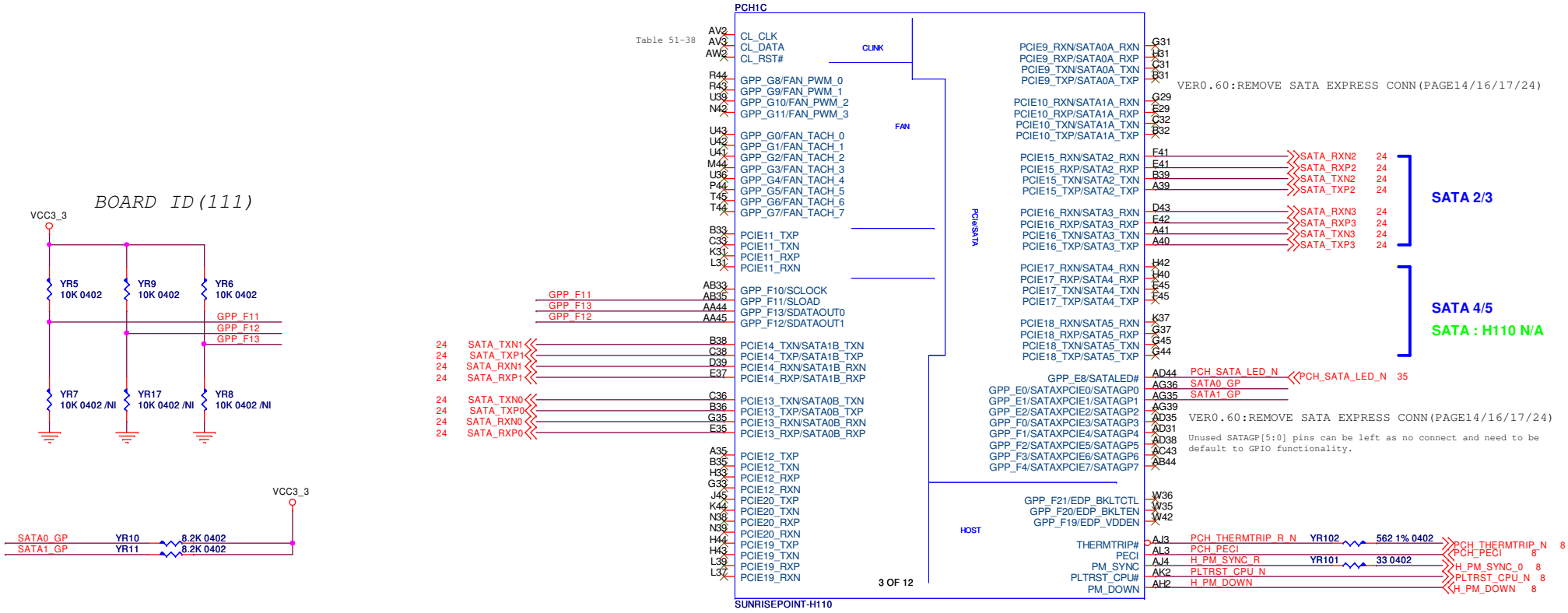
# PCH PART: Y+Reference




*BOARD ID(111)*








**GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.**



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| | | |
|---|---|---|
| Title | PCH CLINK/SATA/CPU HOST | |
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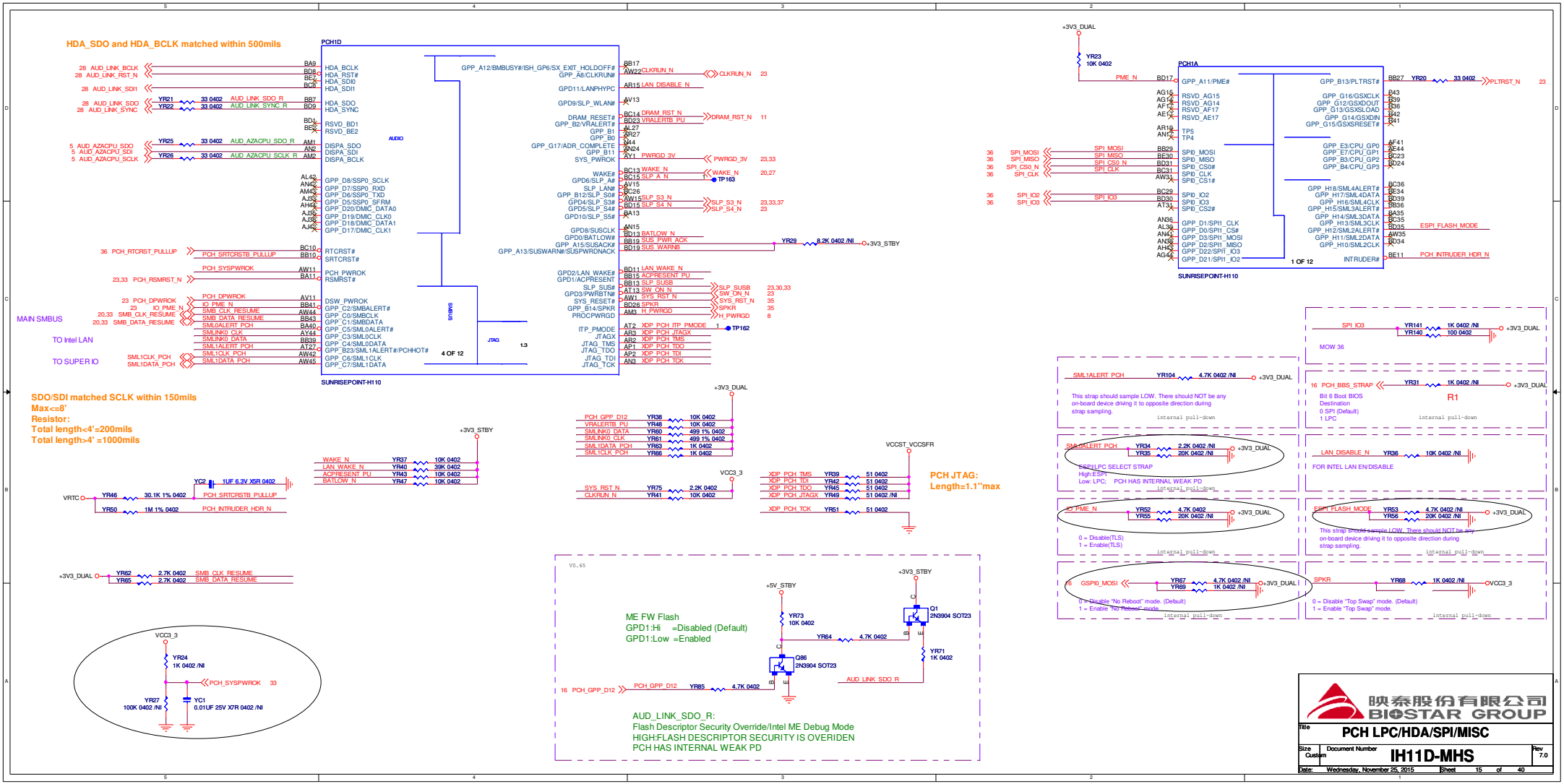
| Date: Thursday, November 19, 2015 | Sheet 14 of 40 | |


HDA_SDO and HDA_BCLK matched within 500mils
PCH1D
SUNRISEPOINT-H110
MAIN SMBUS
TO Intel LAN
TO SUPER IO
SDO/SDI matched SCLK within 150mils
Max<=8'
Resistor:
Total length<4'=200mils
Total length>4' =1000mils
PCH JTAG:
Length=1.1"max
ME FW Flash
GPD1:Hi =Disabled (Default)
GPD1:Low =Enabled
AUD_LINK_SDO_R:
Flash Descriptor Security Override/Intel ME Debug Mode
HIGH:FLASH DESCRIPTOR SECURITY IS OVERIDEN
PCH HAS INTERNAL WEAK PD
PCH1A
SUNRISEPOINT-H110
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
ESPI/LPC SELECT STRAP
High:ESPI
Low: LPC; PCH HAS INTERNAL WEAK PD
0 = Disable(TLS)
1 = Enable(TLS)
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC
R1
FOR INTEL LAN EN/DISABLE
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
internal pull-down
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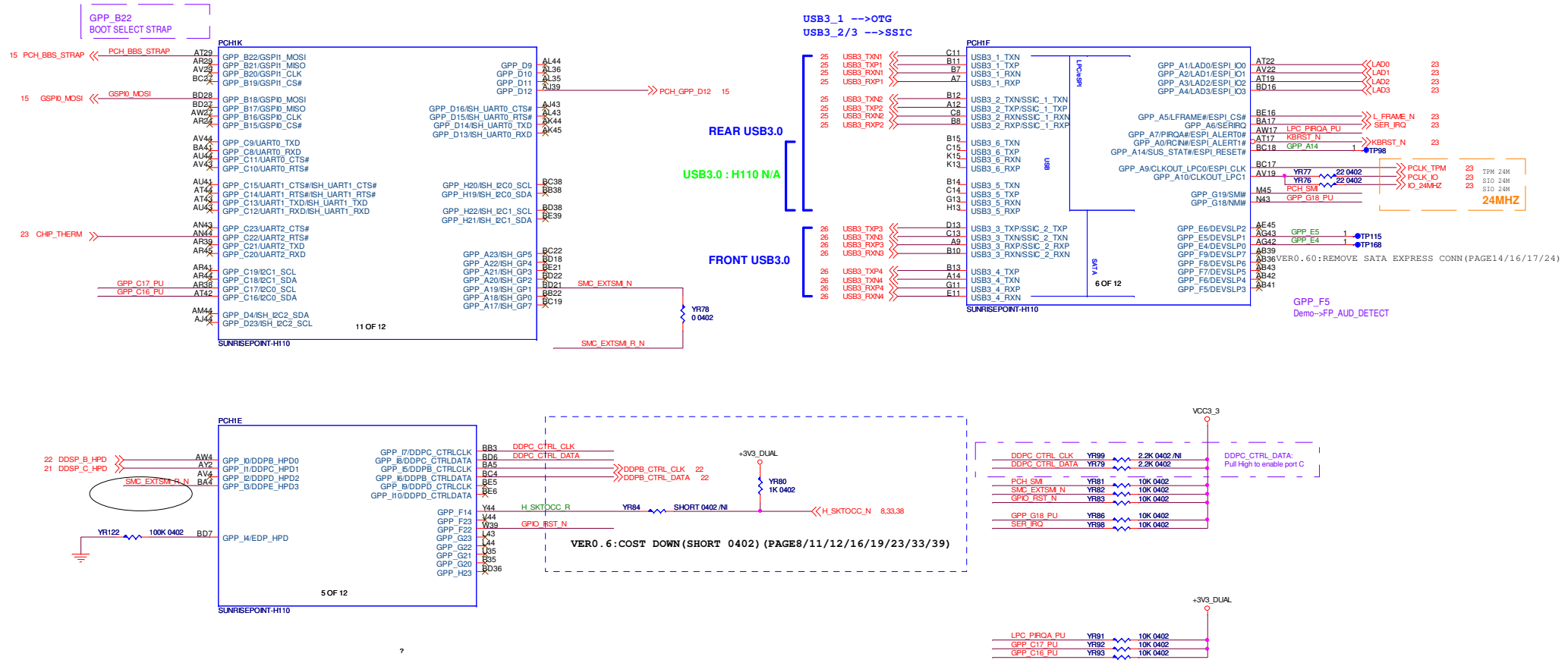
BIOSTAR GROUP
PCH LPC/HDA/SPI/MISC
IH11D-MHS
Wednesday, November 25, 2015

# PCH PART: Y+Reference



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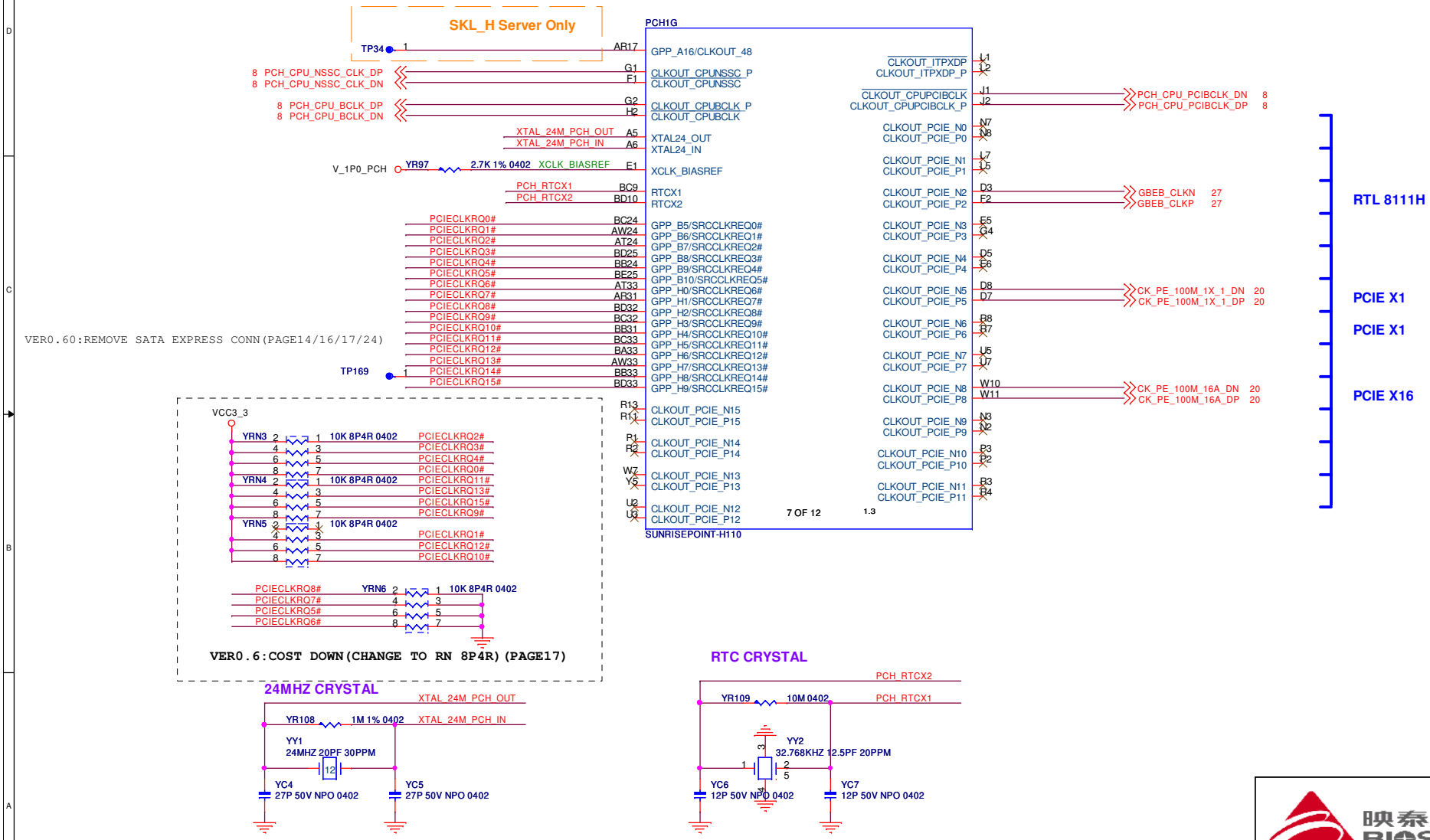
| | | |
|---|---|---|
| Title | PCH LPC/DP/USB3/UART | |
| Size: Custom | Document Number: IH11D-MHS | Rev: 7.0 |
| Date: Wednesday, November 25, 2015 | Sheet 16 of 40 | |

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| | | |
|---|---|---|
| Title | PCH CLOCK BUFFER | |
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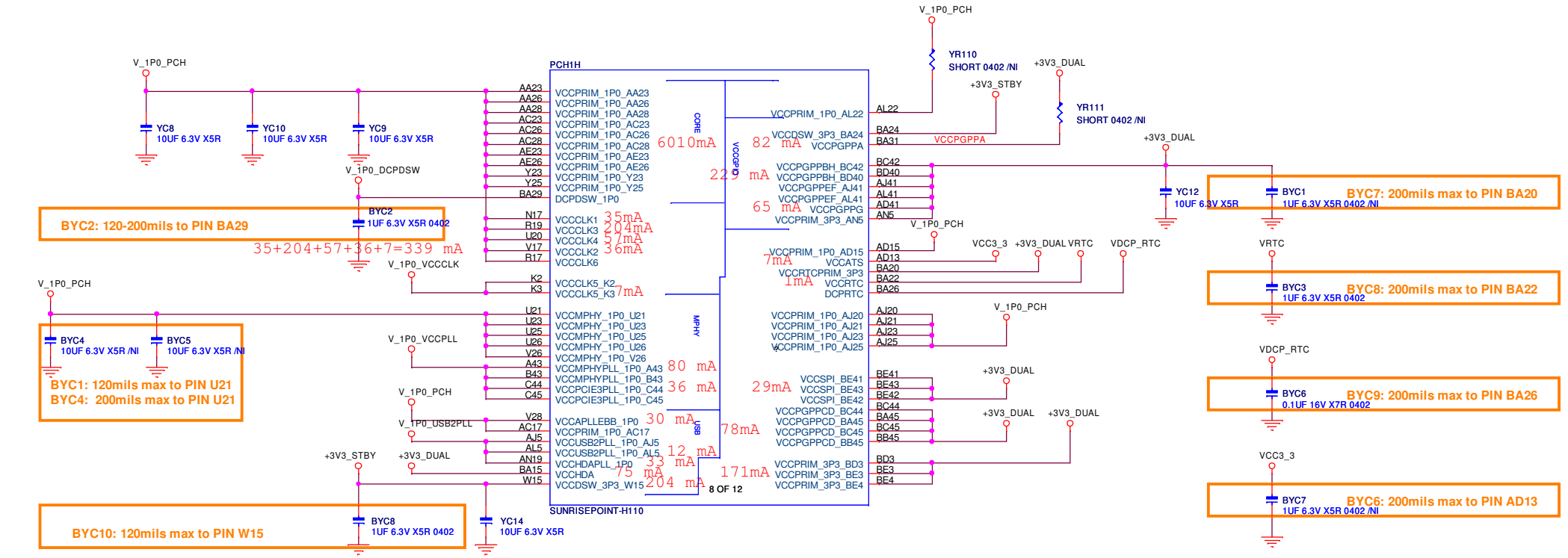


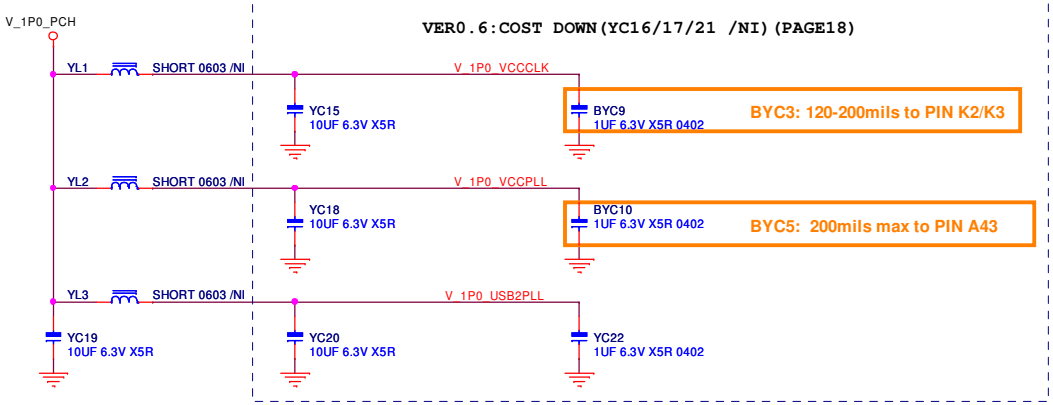


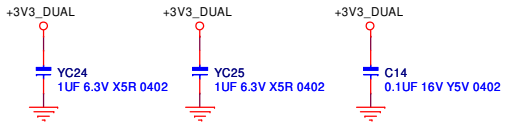


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| | | |
|---|---|---|
| Title | PCH POWER | |
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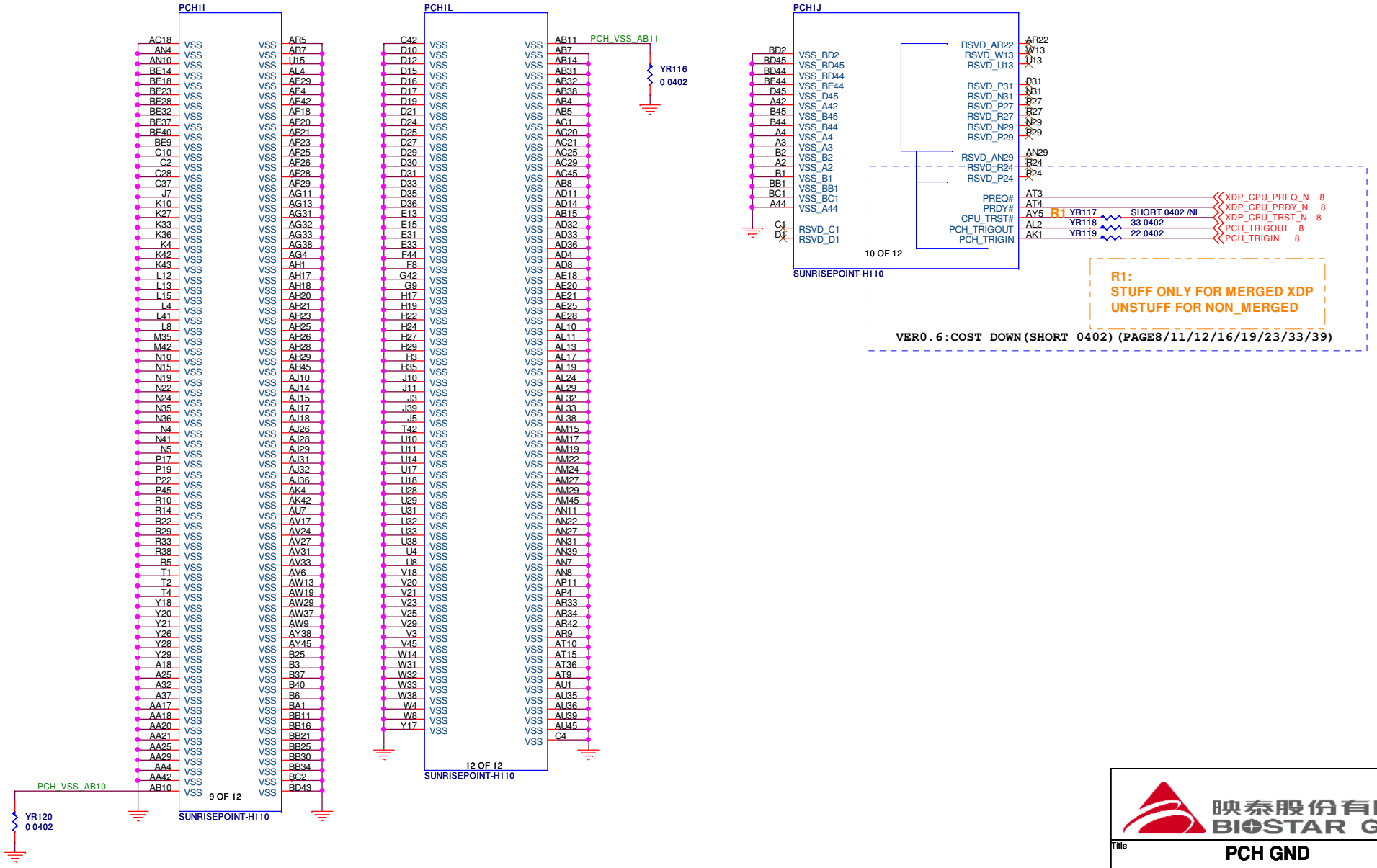
| Date: Thursday, November 19, 2015 | Sheet 18 of 40 | |

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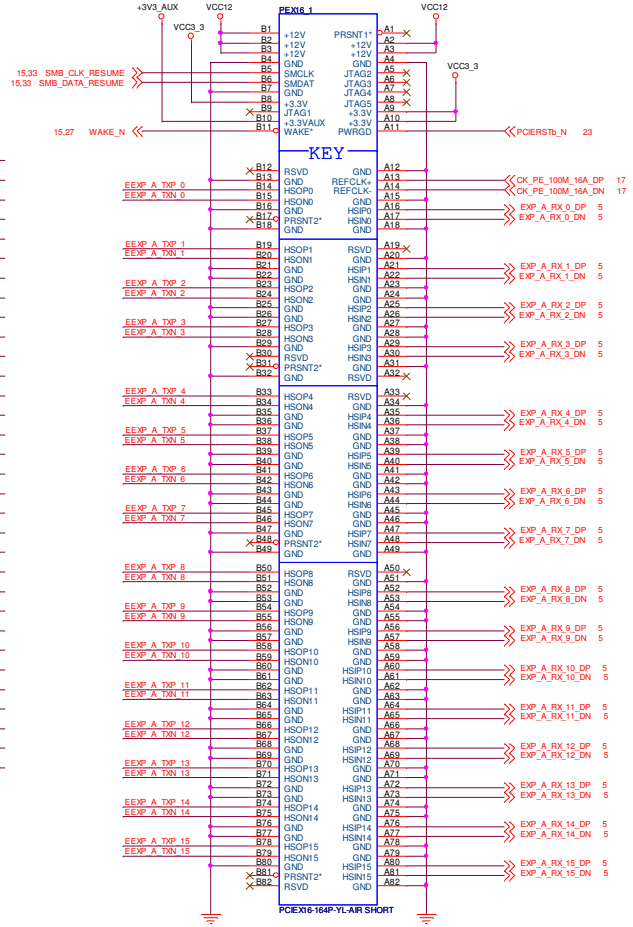
| | | | |
|---|---|---|---|
| Title | PCH GND | | |
| Size B | Document Number IH11D-MHS | | Rev 7.0 |
| Date: Thursday, November 19, 2015 | Sheet 19 of 40 | | |

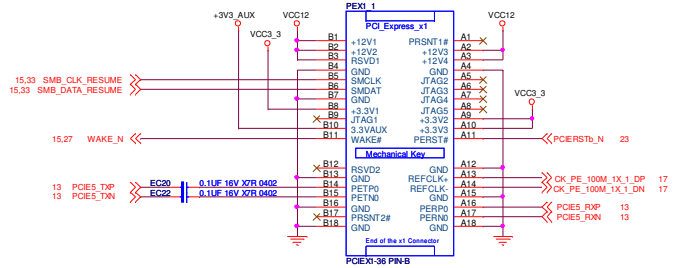
# SLOT PART: E+Reference

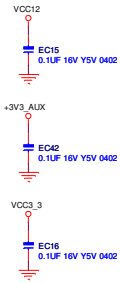
Value:180 nF - 265 nF

450 mils max to connector pin

| | | | | |
|---|---|---|---|---|
| 5 EXP_A_TX_0_DP | EC1 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_0 | |
| 5 EXP_A_TX_0_DN | EC2 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_0 | |
| 5 EXP_A_TX_1_DP | EC3 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_1 | |
| 5 EXP_A_TX_1_DN | EC4 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_1 | |
| 5 EXP_A_TX_2_DP | EC5 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_2 | |
| 5 EXP_A_TX_2_DN | EC6 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_2 | |
| 5 EXP_A_TX_3_DP | EC7 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_3 | |
| 5 EXP_A_TX_3_DN | EC8 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_3 | |
| 5 EXP_A_TX_4_DP | EC9 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_4 | |
| 5 EXP_A_TX_4_DN | EC10 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_4 | |
| 5 EXP_A_TX_5_DP | EC11 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_5 | |
| 5 EXP_A_TX_5_DN | EC12 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_5 | |
| 5 EXP_A_TX_6_DP | EC13 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_6 | |
| 5 EXP_A_TX_6_DN | EC14 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_6 | |
| 5 EXP_A_TX_7_DP | EC19 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_7 | |
| 5 EXP_A_TX_7_DN | EC28 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_7 | |
| 5 EXP_A_TX_8_DP | EC49 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_8 | |
| 5 EXP_A_TX_8_DN | EC50 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_8 | |
| 5 EXP_A_TX_9_DP | EC30 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_9 | |
| 5 EXP_A_TX_9_DN | EC29 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_9 | |
| 5 EXP_A_TX_10_DP | EC33 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_10 | |
| 5 EXP_A_TX_10_DN | EC35 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_10 | |
| 5 EXP_A_TX_11_DP | EC32 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_11 | |
| 5 EXP_A_TX_11_DN | EC31 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_11 | |
| 5 EXP_A_TX_12_DP | EC37 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_12 | |
| 5 EXP_A_TX_12_DN | EC38 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_12 | |
| 5 EXP_A_TX_13_DP | EC36 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_13 | |
| 5 EXP_A_TX_13_DN | EC34 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_13 | |
| 5 EXP_A_TX_14_DP | EC39 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_14 | |
| 5 EXP_A_TX_14_DN | EC48 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_14 | |
| 5 EXP_A_TX_15_DP | EC40 | 0.22UF 10V X5R 0402 | EEXP_A_TXP_15 | |
| 5 EXP_A_TX_15_DN | EC41 | 0.22UF 10V X5R 0402 | EEXP_A_TXN_15 | |



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Title: PCIEX16 SLOT

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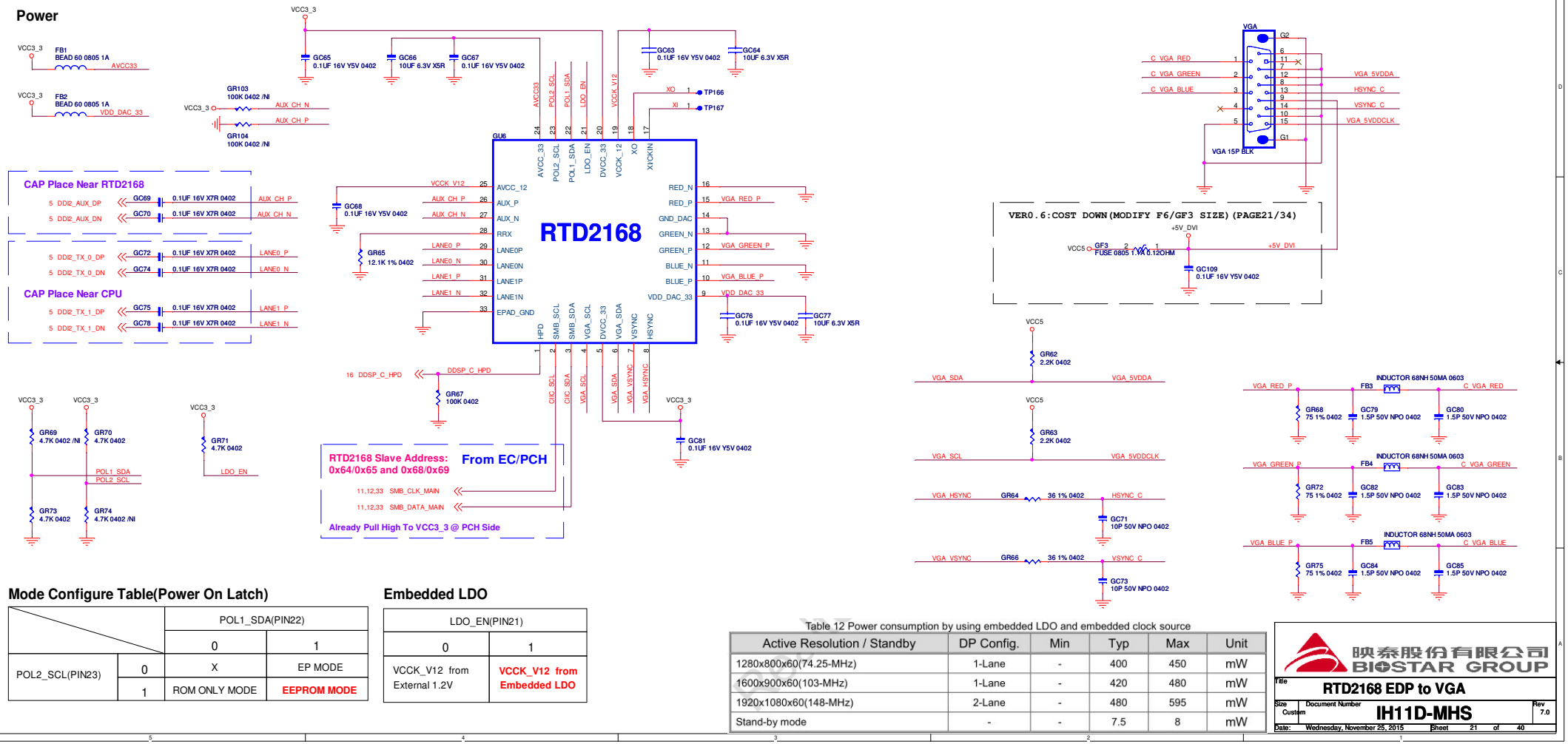


## Mode Configure Table(Power On Latch)

| | | POL1_SDA(PIN22) | |
|---|---|---|---|
| | | 0 | 1 |
| POL2_SCL(PIN23) | 0 | X | EP MODE |
| | 1 | ROM ONLY MODE | **EEPROM MODE** |

## Embedded LDO

| LDO_EN(PIN21) | |
|---|---|
| 0 | 1 |
| VCCK_V12 from External 1.2V | **VCCK_V12 from Embedded LDO** |

Table 12 Power consumption by using embedded LDO and embedded clock source

| Active Resolution / Standby | DP Config. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1280x800x60(74.25-MHz) | 1-Lane | - | 400 | 450 | mW |
| 1600x900x60(103-MHz) | 1-Lane | - | 420 | 480 | mW |
| 1920x1080x60(148-MHz) | 2-Lane | - | 480 | 595 | mW |
| Stand-by mode | - | - | 7.5 | 8 | mW |

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Title: **RTD2168 EDP to VGA**

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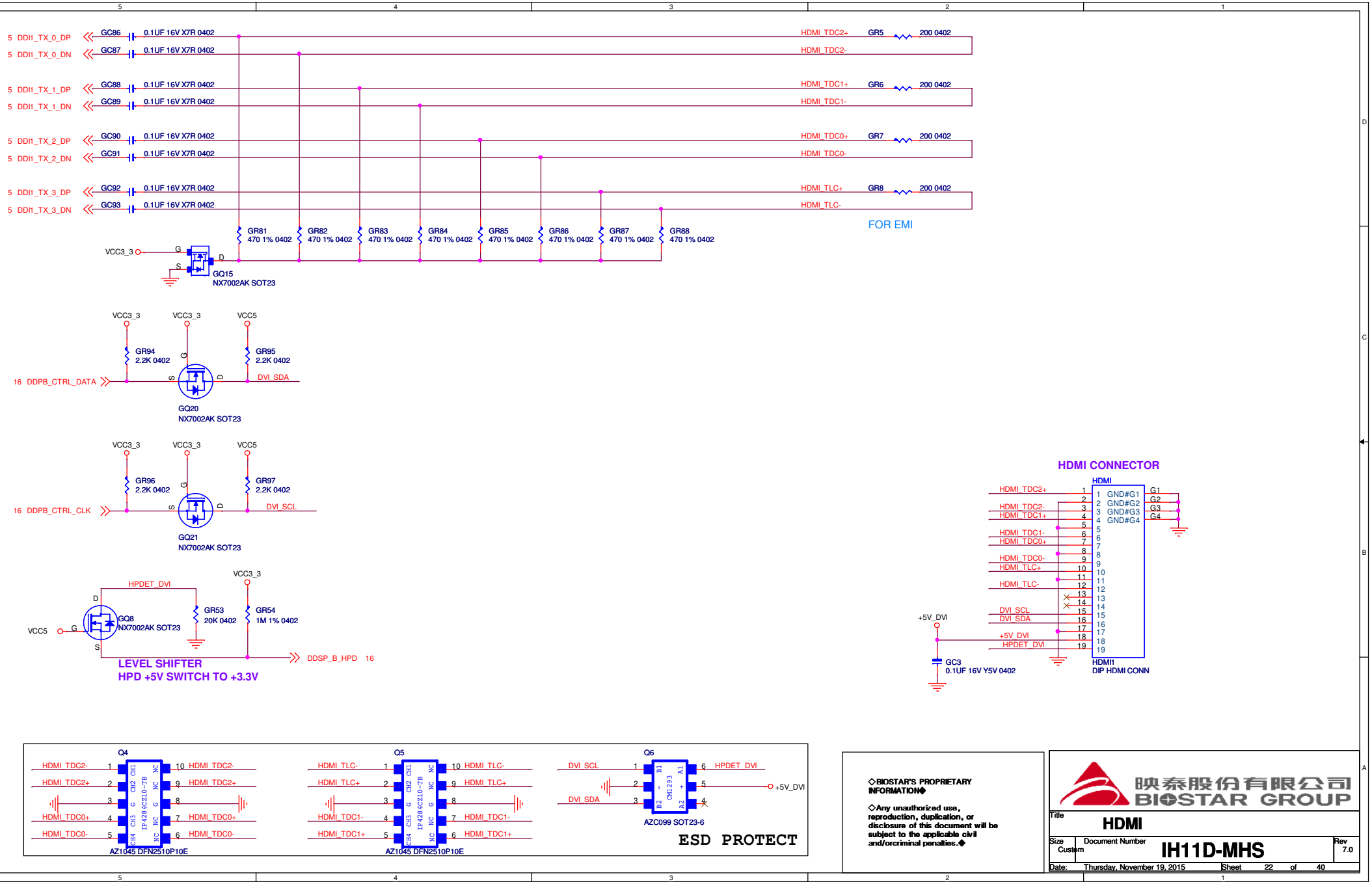
Date: Wednesday, November 25, 2015 | Sheet 21 of 40



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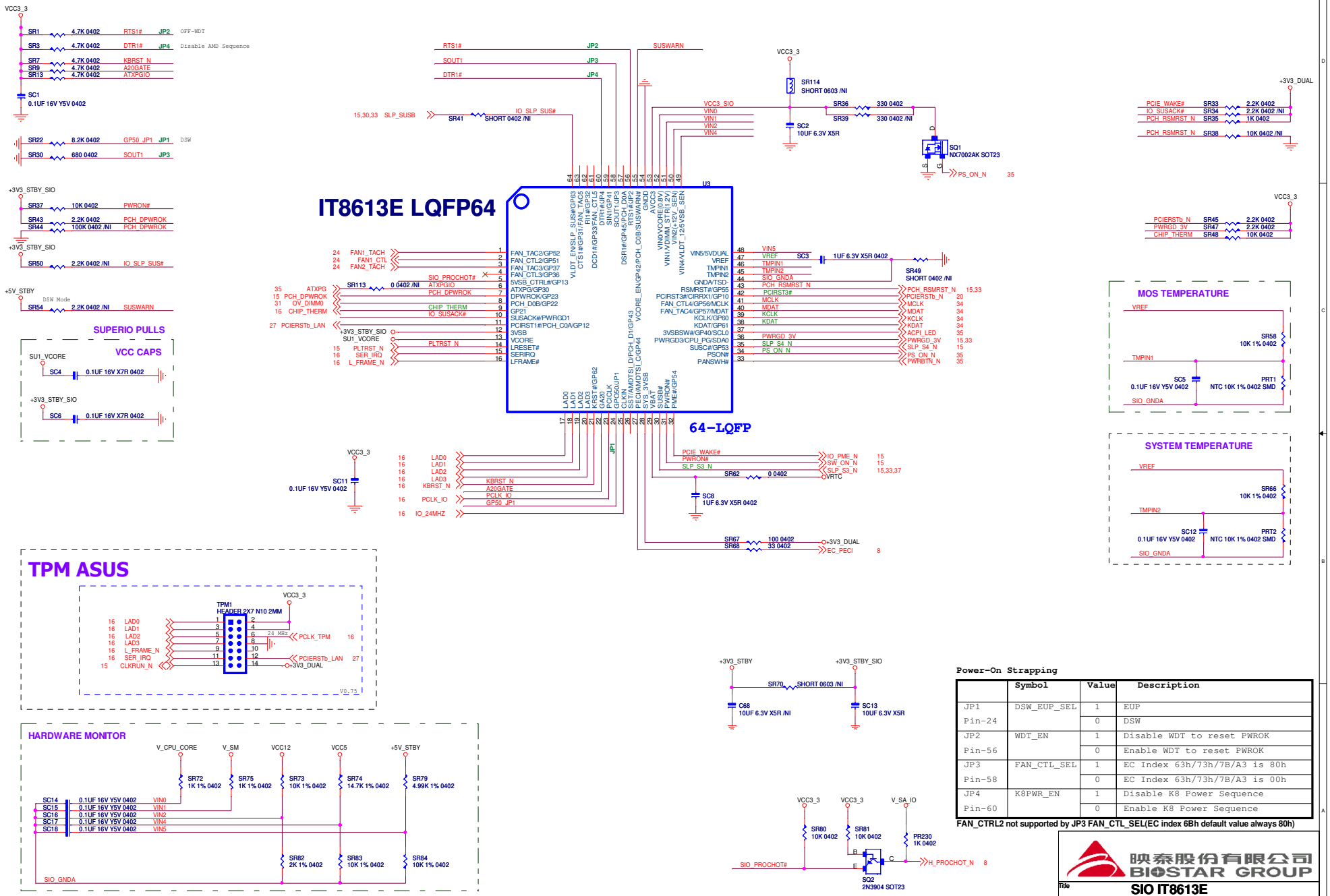
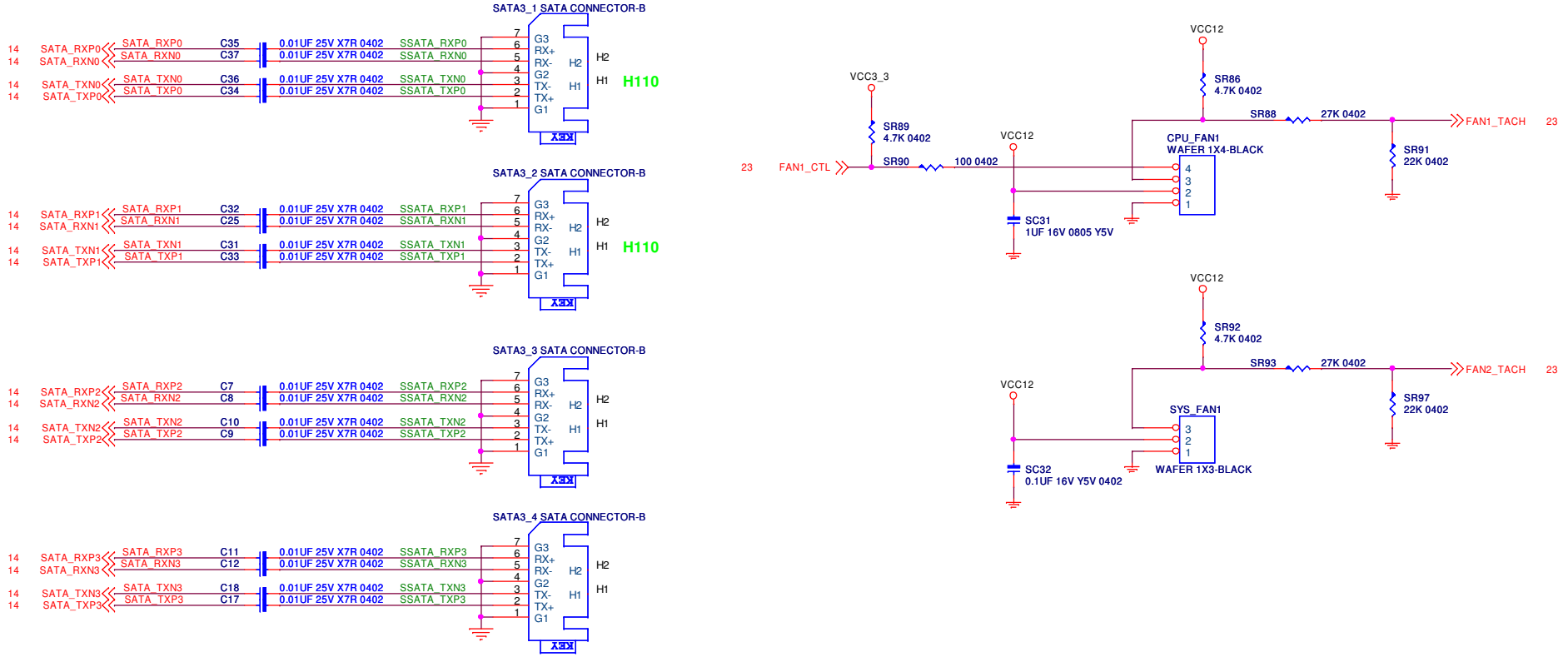
Title: HDMI

Size: Custom | Document Number: IH11D-MHS | Rev: 7.0

Date: Thursday, November 19, 2015 | Sheet 22 of 40


IT8613E LQFP64
64-LQFP
SUPERIO PULLS
VCC CAPS
TPM ASUS
HARDWARE MONITOR
MOS TEMPERATURE
SYSTEM TEMPERATURE
SIO IT8613E
IH11D-MHS
Power-On Strapping
FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)
Date: Thursday, November 19, 2015
Sheet 23 of 40

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| | | |
|---|---|---|
| Title | SATA/FAN | |
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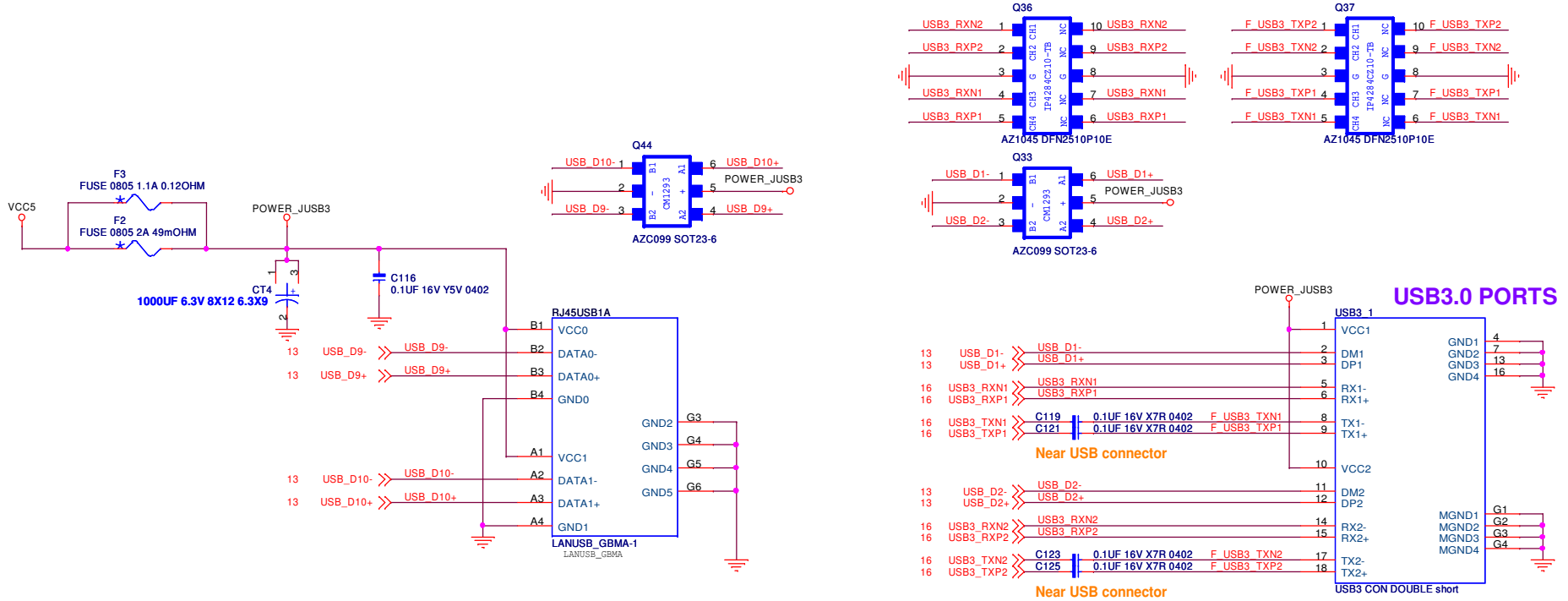
| Date: Thursday, November 19, 2015 | Sheet 24 of 40 | |







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| | | |
|---|---|---|
| Title | REAR USB | |
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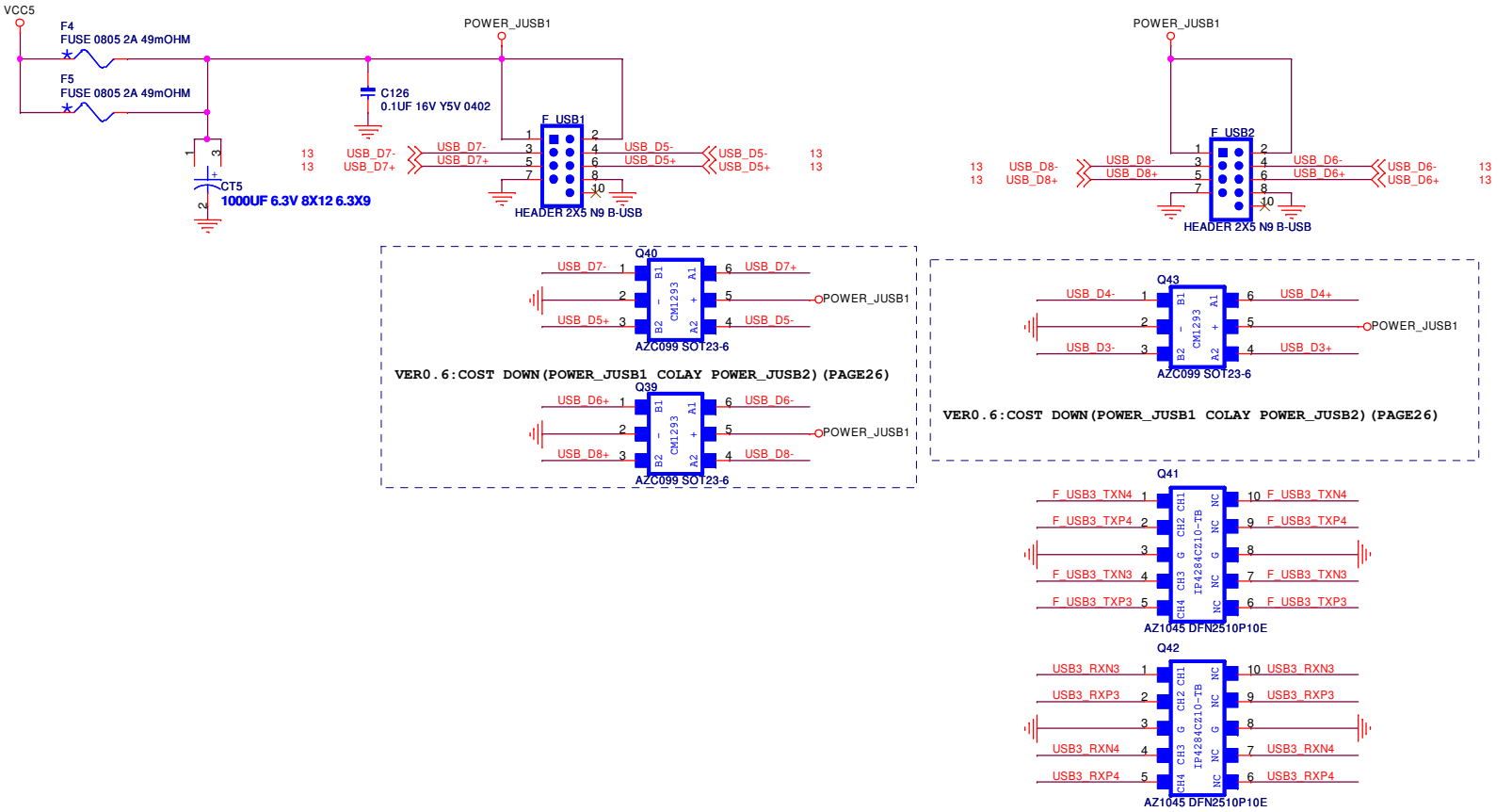
| Date: Thursday, November 19, 2015 | Sheet 25 of 40 | |

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| | | |
|---|---|---|
| Title | FRONT USB | |
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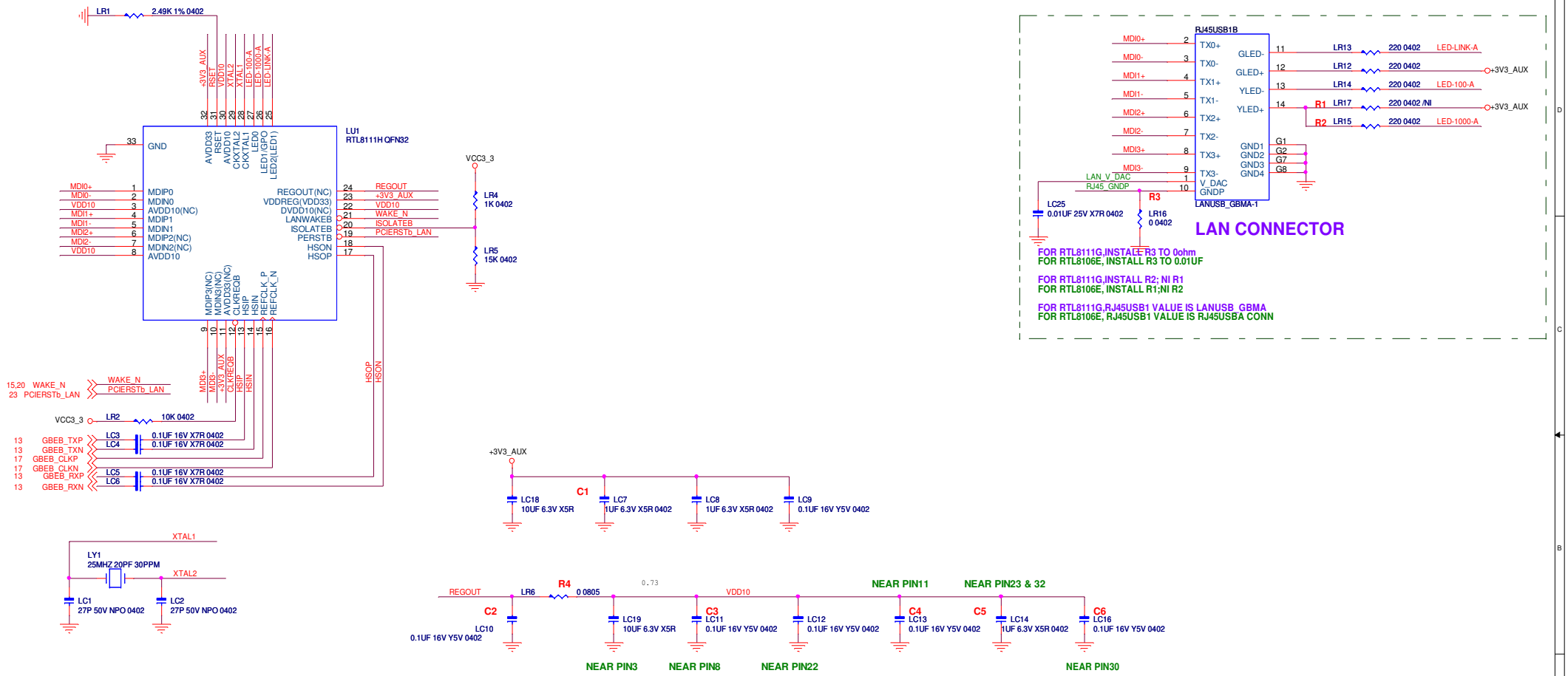


## COMPONENT CONTRAST LIST

| LAN PARTS | R1 | R2 | R3 | R4 | C1 | C2 | C3 | C4 | C5 | C6 | RJ45 CONN |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RTL8111H | X | O | 0ohm | O | O | O | O | O | O | X | LANUSB_GBMA |
| RTL8106E | O | X | 0.01uF | O | | | | | | O | RJ45USBA CONN |

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| | | |
|---|---|---|
| Title | RTL8111H/8106E | |
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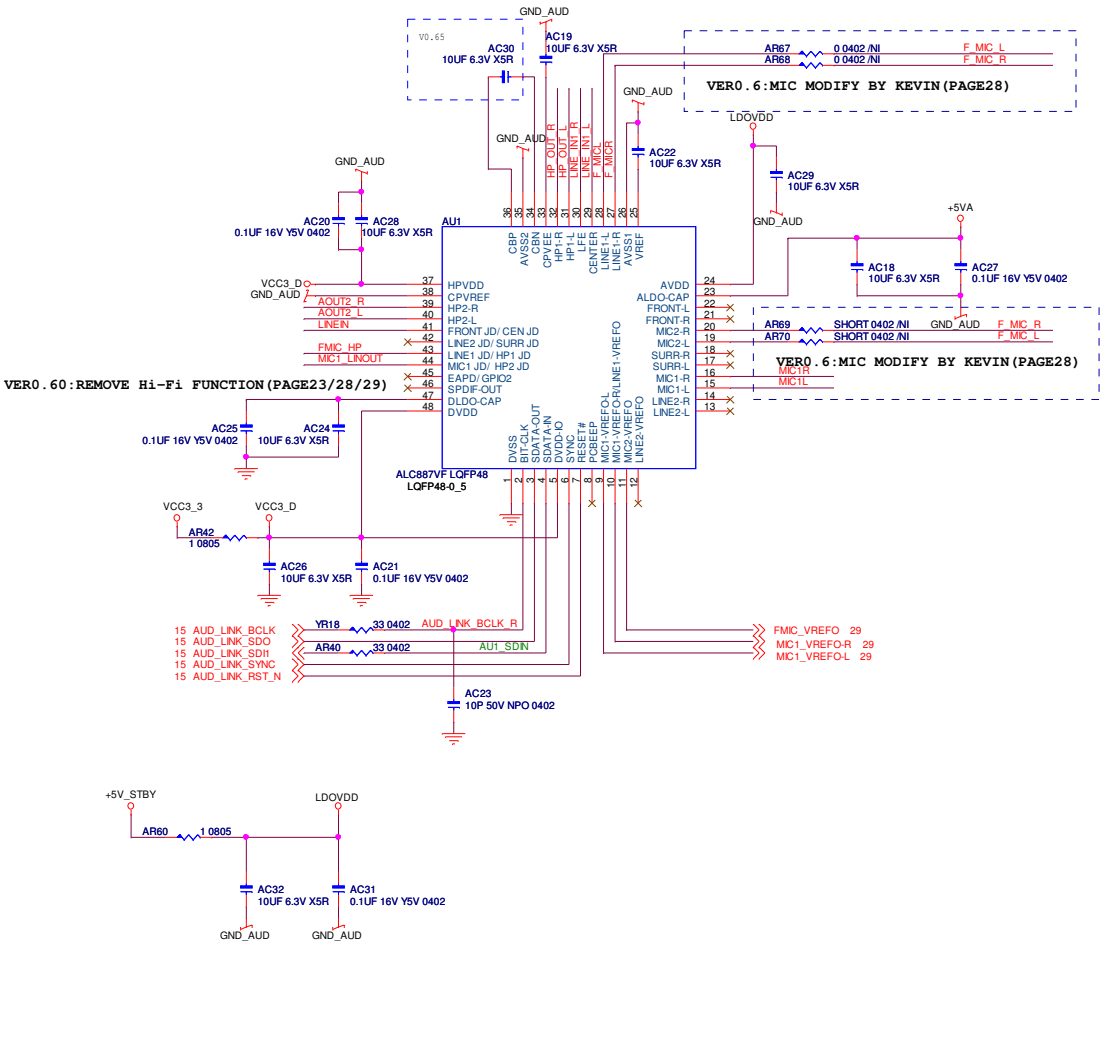
| Date: Thursday, November 19, 2015 | Sheet 27 of 40 | |




## FRONT CHANNEL

VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

HP_OUT_L — AR58 18 1% 0402 — AR53 47 0402 — HPOUT_L 29

HP_OUT_R — AR59 18 1% 0402 — AR55 47 0402 — HPOUT_R 29

F_MIC_L — AC15 10UF 6.3V X5R — AR33 75 0402 — FMIC_L 29

VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

F_MIC_R — AC14 10UF 6.3V X5R — AR32 75 0402 — FMIC_R 29

## REAR CHANNEL

MIC1L — AC13 10UF 6.3V X5R — AR31 1K 0402 — MIC1_L 29

MIC1R — AC12 10UF 6.3V X5R — AR30 1K 0402 — MIC1_R 29

LINE_IN1_L — AC11 10UF 6.3V X5R — AR29 1K 0402 — LINE1_L 29

LINE_IN1_R — AC10 10UF 6.3V X5R — AR28 1K 0402 — LINE1_R 29

AOUT2_L — AR56 47 0402 — LINEOUT_L 29

AOUT2_R — AR57 47 0402 — LINEOUT_R 29

VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

## JD Group

as close as possible to AU1

VCC3_3

AR35 100K 1% 0402 — LINEIN

AR36 100K 1% 0402 — MIC1_LINOUT

AR34 100K 1% 0402 — FMIC_HP

AR13 200K 1% 0402 — 29 LINE1_JD

AR51 100K 1% 0402

AR45 200K 1% 0402

AR2 100K 1% 0402

AR3 200K 1% 0402

29 MIC1_JD

29 LINEOUT_JD

29 FMIC_JD

29 HP_JD

AR20 0 0805 — GND_AUD

AR48 SHORT 0805 /NI — GND_AUD



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Title: AUDIO CODEC ALC887

Size: Custom | Document Number: IH11D-MHS | Rev: 7.0

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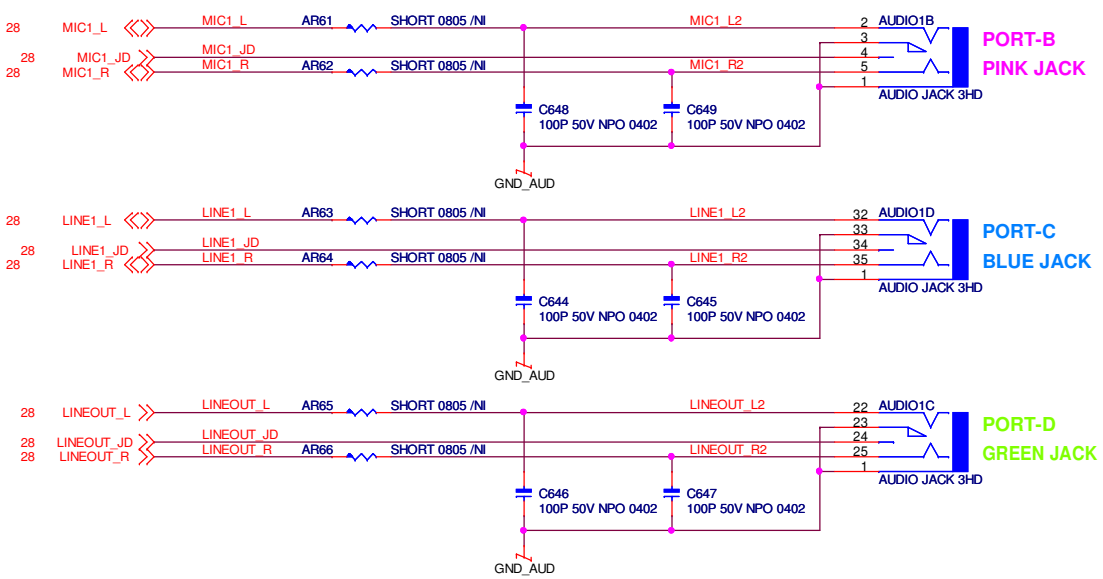


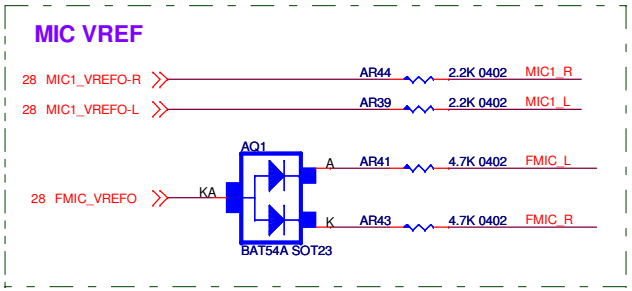


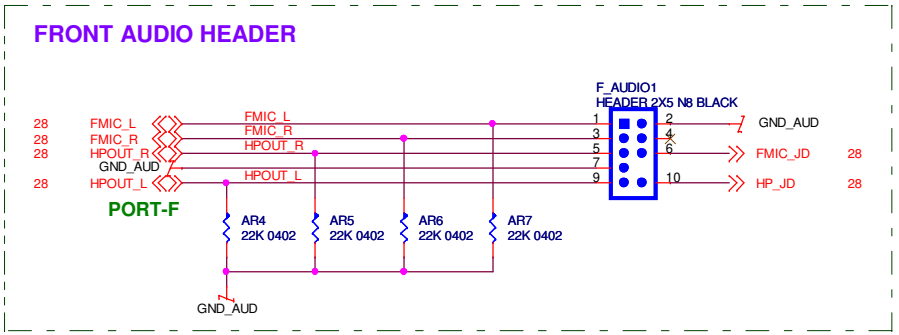


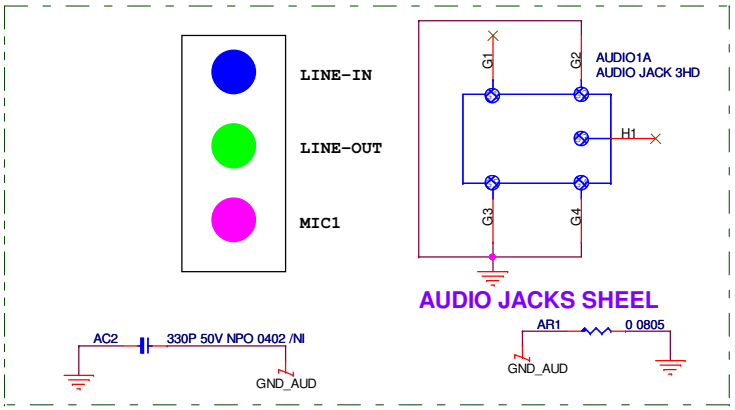


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Title: AUDIO CONNECTOR

| Size | Document Number | Rev |
|---|---|---|
| Custom | IH11D-MHS | 7.0 |

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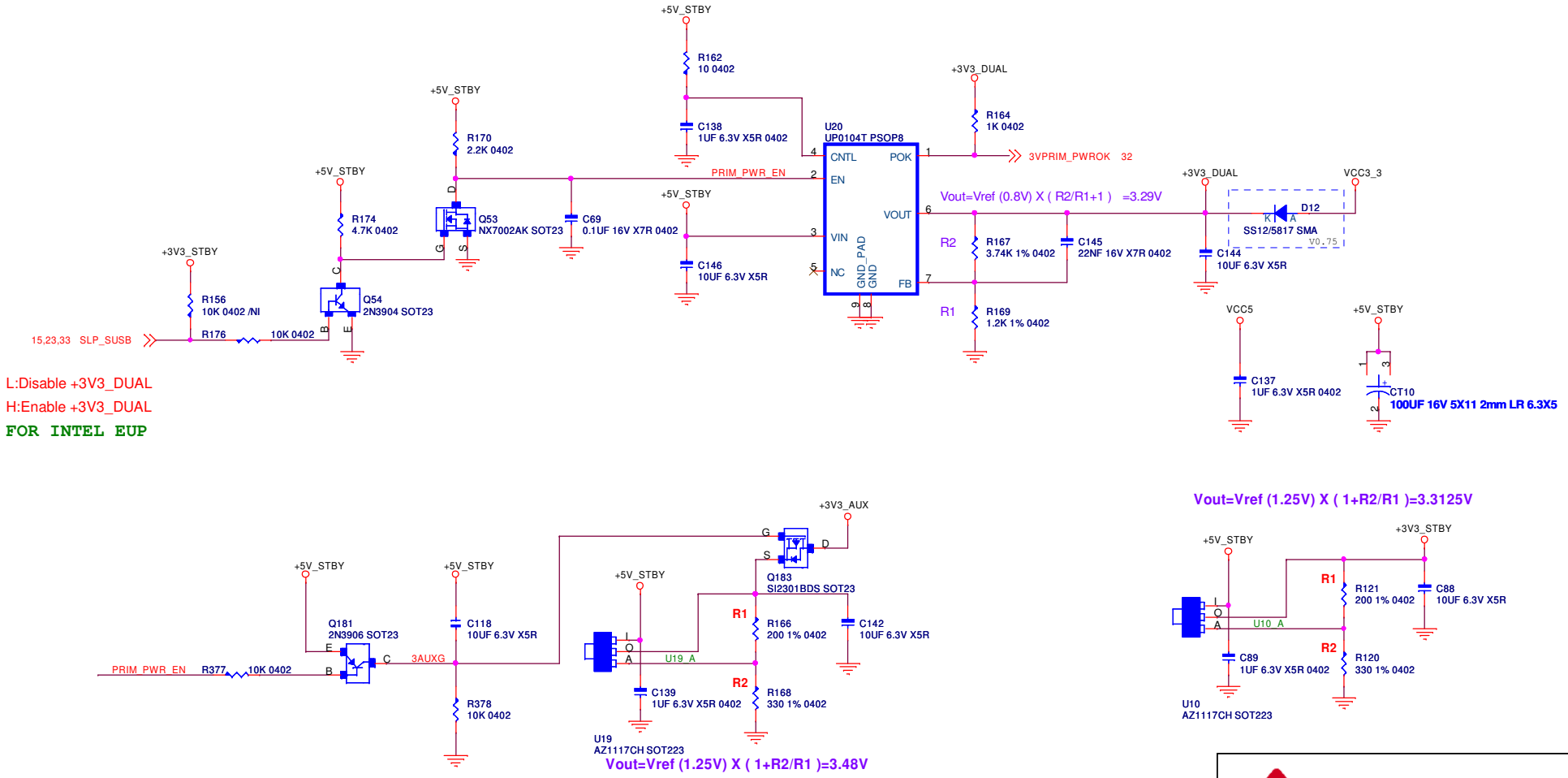


映泰股份有限公司
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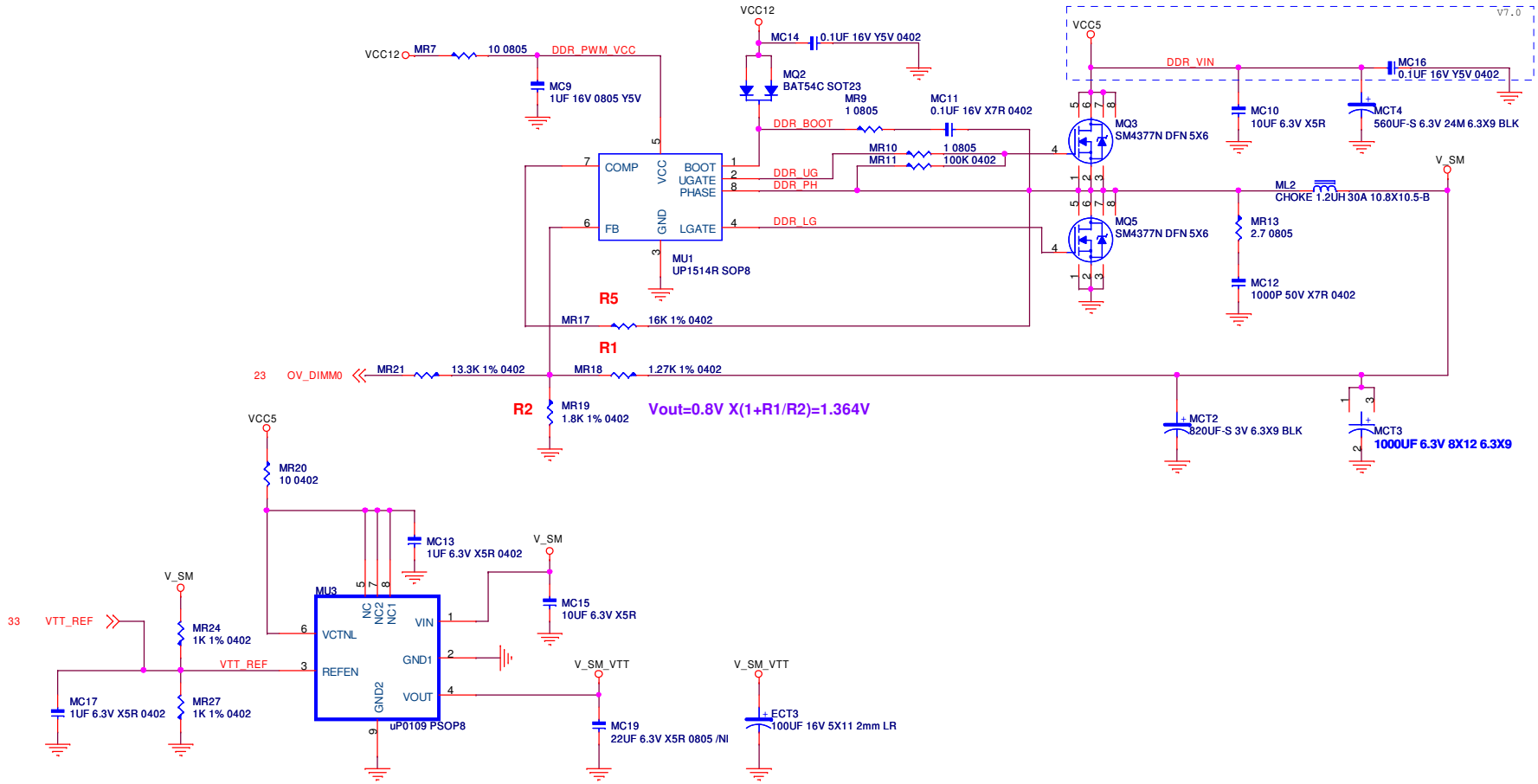
| | | |
|---|---|---|
| Title | ACPI POWER | |
| Size B | Document Number IH11D-MHS | Rev 7.0 |
| Date: Thursday, November 19, 2015 | Sheet 30 of 40 | |

# MEMORY PART:M+Reference



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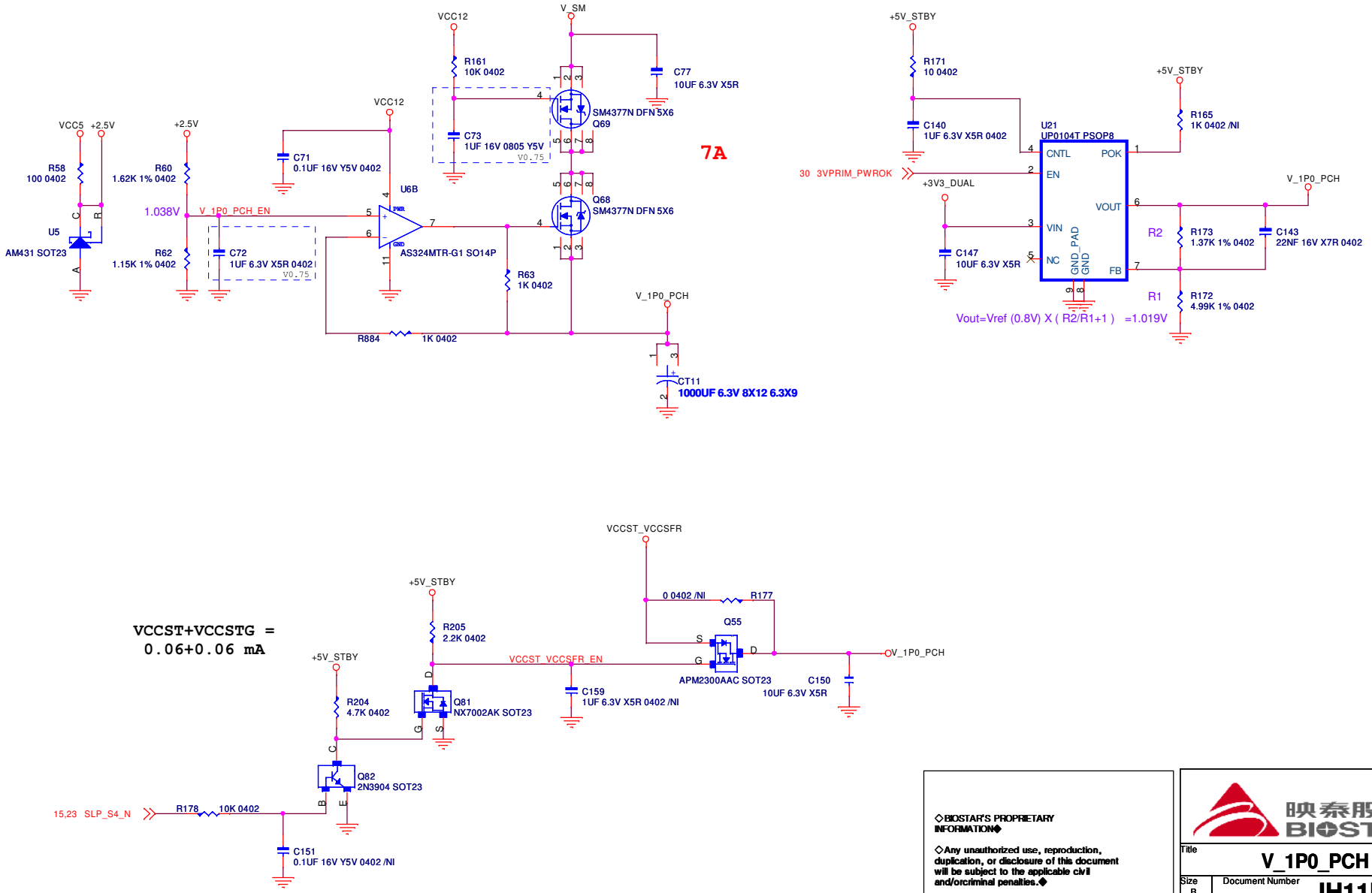
| | | |
|---|---|---|
| Title | MEMORY DC-DC | |
| Size B | Document Number IH11D-MHS | Rev 7.0 |
| Date: Thursday, November 19, 2015 | Sheet 31 of 40 | |



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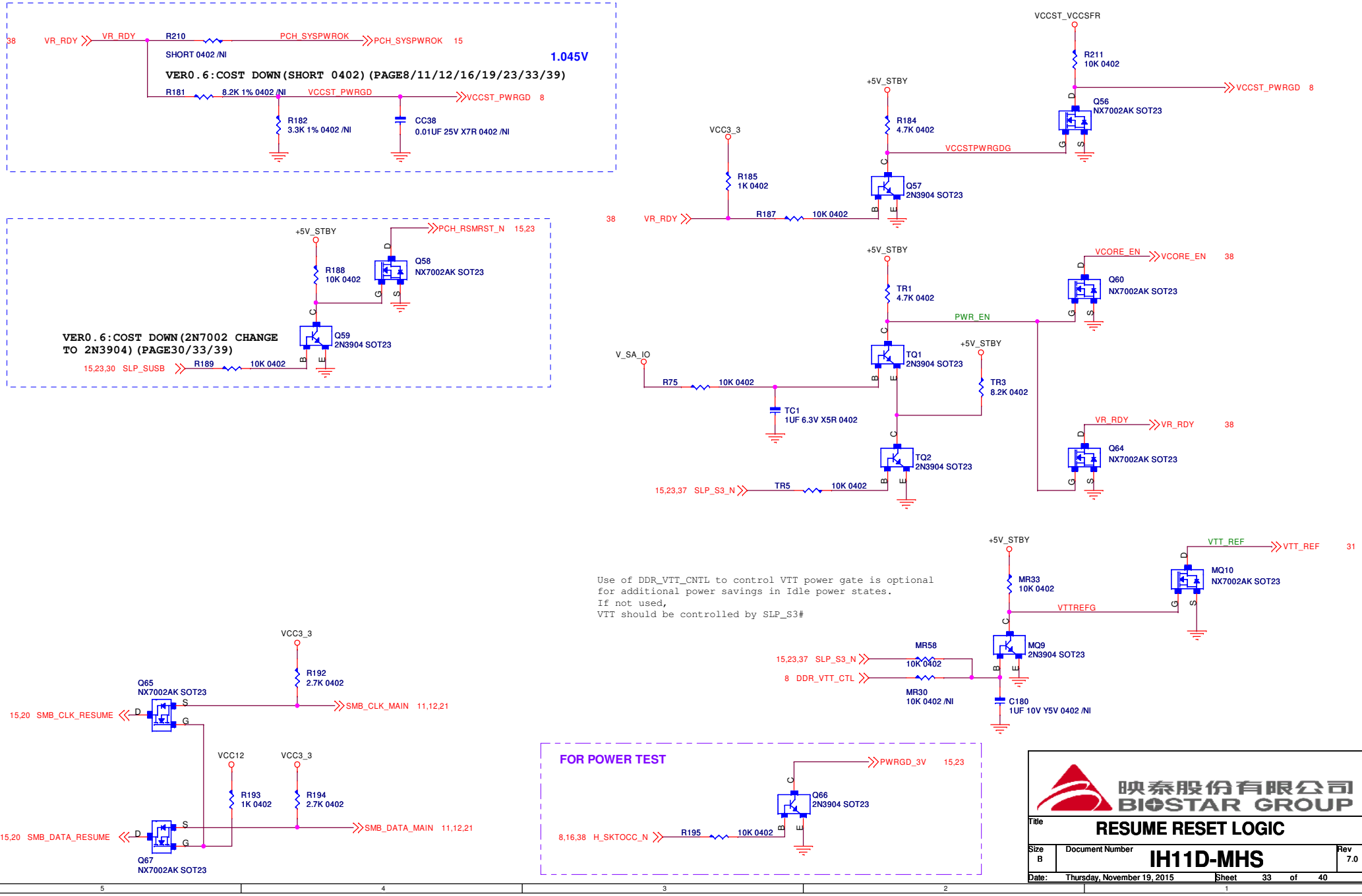
| | | |
|---|---|---|
| Title | V_1P0_PCH | |
| Size B | Document Number IH11D-MHS | Rev 7.0 |
| Date: Thursday, November 19, 2015 | Sheet 32 of 40 | |


38 VR_RDY
VR_RDY
R210
SHORT 0402 /NI
PCH_SYSPWROK
PCH_SYSPWROK 15
1.045V
VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)
R181
8.2K 1% 0402 /NI
VCCST_PWRGD
VCCST_PWRGD 8
R182
3.3K 1% 0402 /NI
CC38
0.01UF 25V X7R 0402 /NI
VCCST_VCCSFR
R211
10K 0402
VCCST_PWRGD 8
Q56
NX7002AK SOT23
+5V_STBY
R184
4.7K 0402
VCCSTPWRGDG
VCC3_3
R185
1K 0402
Q57
2N3904 SOT23
38 VR_RDY
R187
10K 0402
+5V_STBY
PCH_RSMRST_N 15,23
R188
10K 0402
Q58
NX7002AK SOT23
VER0.6:COST DOWN(2N7002 CHANGE
TO 2N3904)(PAGE30/33/39)
Q59
2N3904 SOT23
15,23,30 SLP_SUSB
R189
10K 0402
+5V_STBY
VCORE_EN
VCORE_EN 38
TR1
4.7K 0402
Q60
NX7002AK SOT23
PWR_EN
V_SA_IO
TQ1
2N3904 SOT23
+5V_STBY
R75
10K 0402
TR3
8.2K 0402
TC1
1UF 6.3V X5R 0402
VR_RDY
VR_RDY 38
Q64
NX7002AK SOT23
TQ2
2N3904 SOT23
15,23,37 SLP_S3_N
TR5
10K 0402
Use of DDR_VTT_CNTL to control VTT power gate is optional
for additional power savings in Idle power states.
If not used,
VTT should be controlled by SLP_S3#
+5V_STBY
VTT_REF
VTT_REF 31
MR33
10K 0402
MQ10
NX7002AK SOT23
VTTREFG
MQ9
2N3904 SOT23
15,23,37 SLP_S3_N
MR58
10K 0402
8 DDR_VTT_CTL
MR30
10K 0402 /NI
C180
1UF 10V Y5V 0402 /NI
VCC3_3
R192
2.7K 0402
Q65
NX7002AK SOT23
15,20 SMB_CLK_RESUME
SMB_CLK_MAIN 11,12,21
VCC12
VCC3_3
R193
1K 0402
R194
2.7K 0402
15,20 SMB_DATA_RESUME
SMB_DATA_MAIN 11,12,21
Q67
NX7002AK SOT23
FOR POWER TEST
PWRGD_3V 15,23
Q66
2N3904 SOT23
8,16,38 H_SKTOCC_N
R195
10K 0402
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BIOSTAR GROUP
Title
RESUME RESET LOGIC
Size B
Document Number
IH11D-MHS
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Date: Thursday, November 19, 2015
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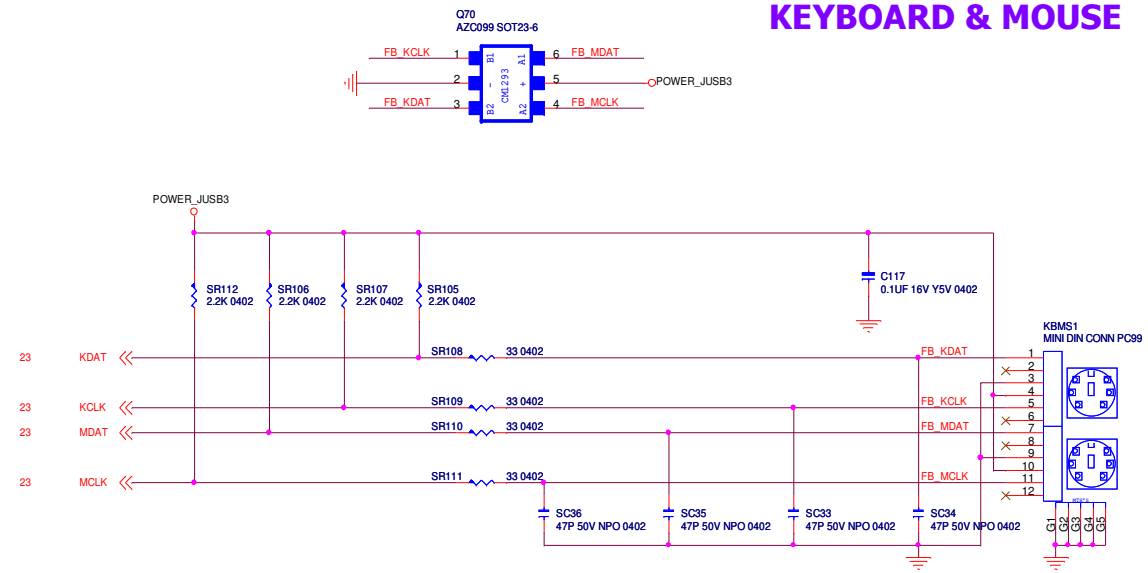
# KEYBOARD & MOUSE



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Title: PS2 CONN

Size: Custom | Document Number: IH11D-MHS | Rev: 7.0

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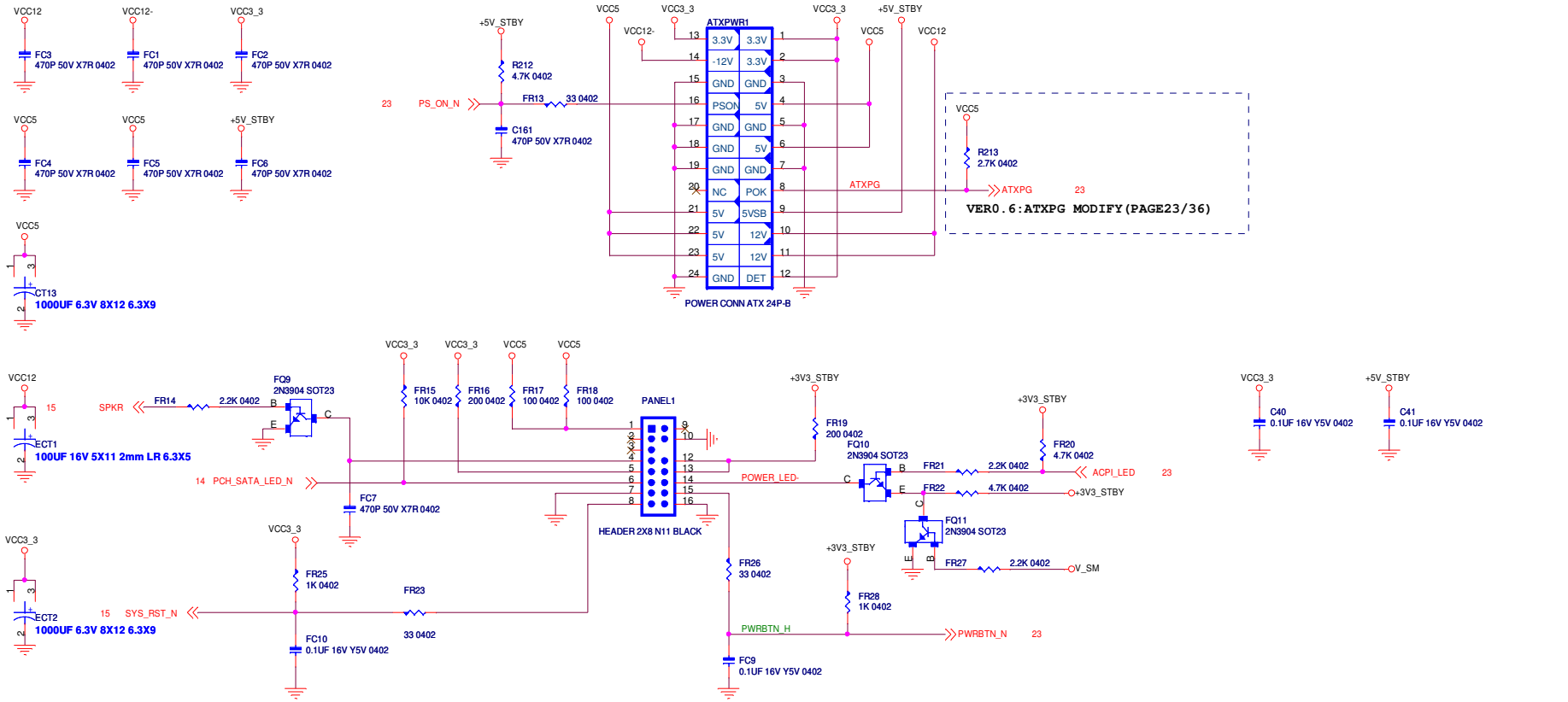
# FP PART: F+Reference



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Title: 24PIN CONN & FP

| Size | Document Number | Rev |
|---|---|---|
| Custom | IH11D-MHS | 7.0 |

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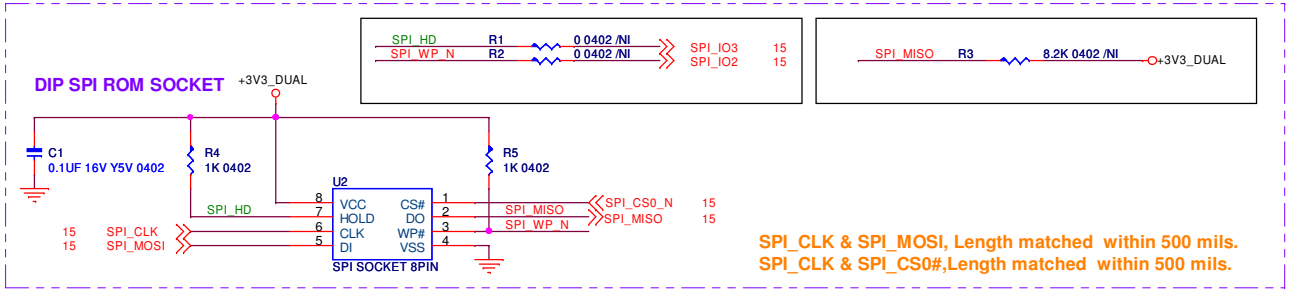


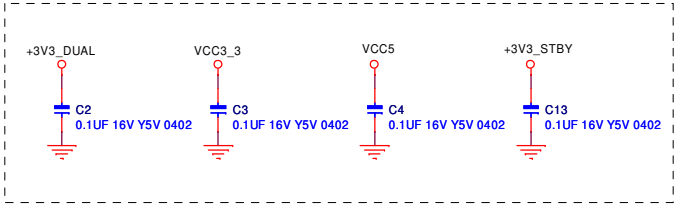


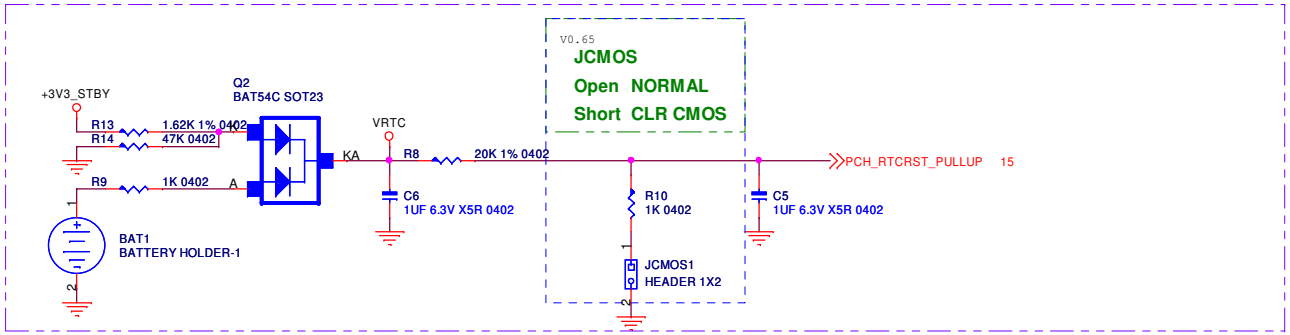




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Title: SPI ROM/RTC/BAT

| Size | Document Number | Rev |
|---|---|---|
| B | IH11D-MHS | 7.0 |

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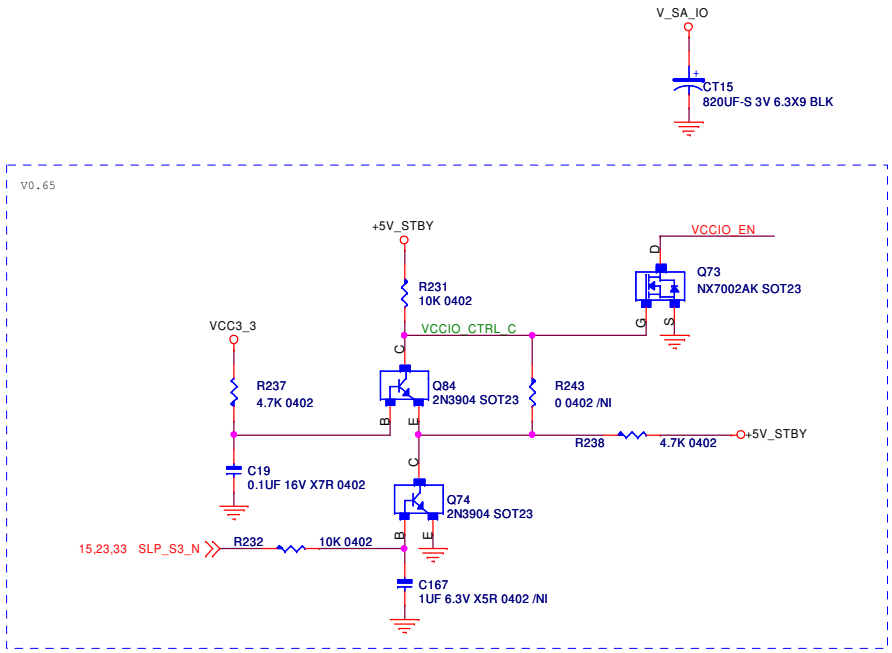


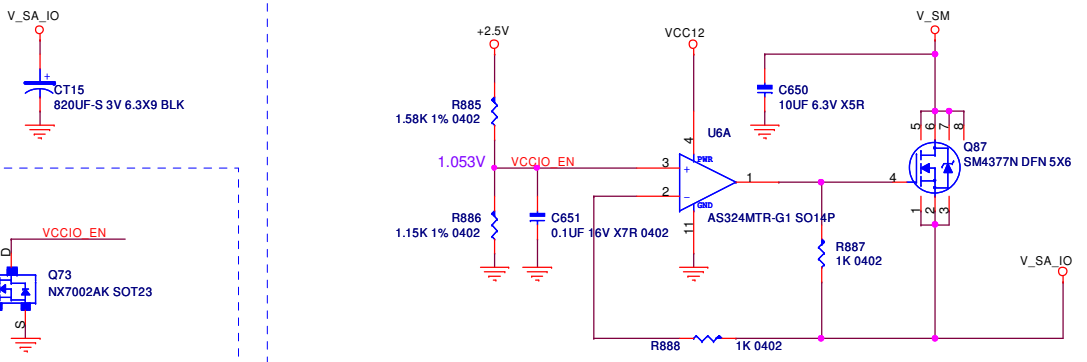







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Title: VCCIO/VCCSA

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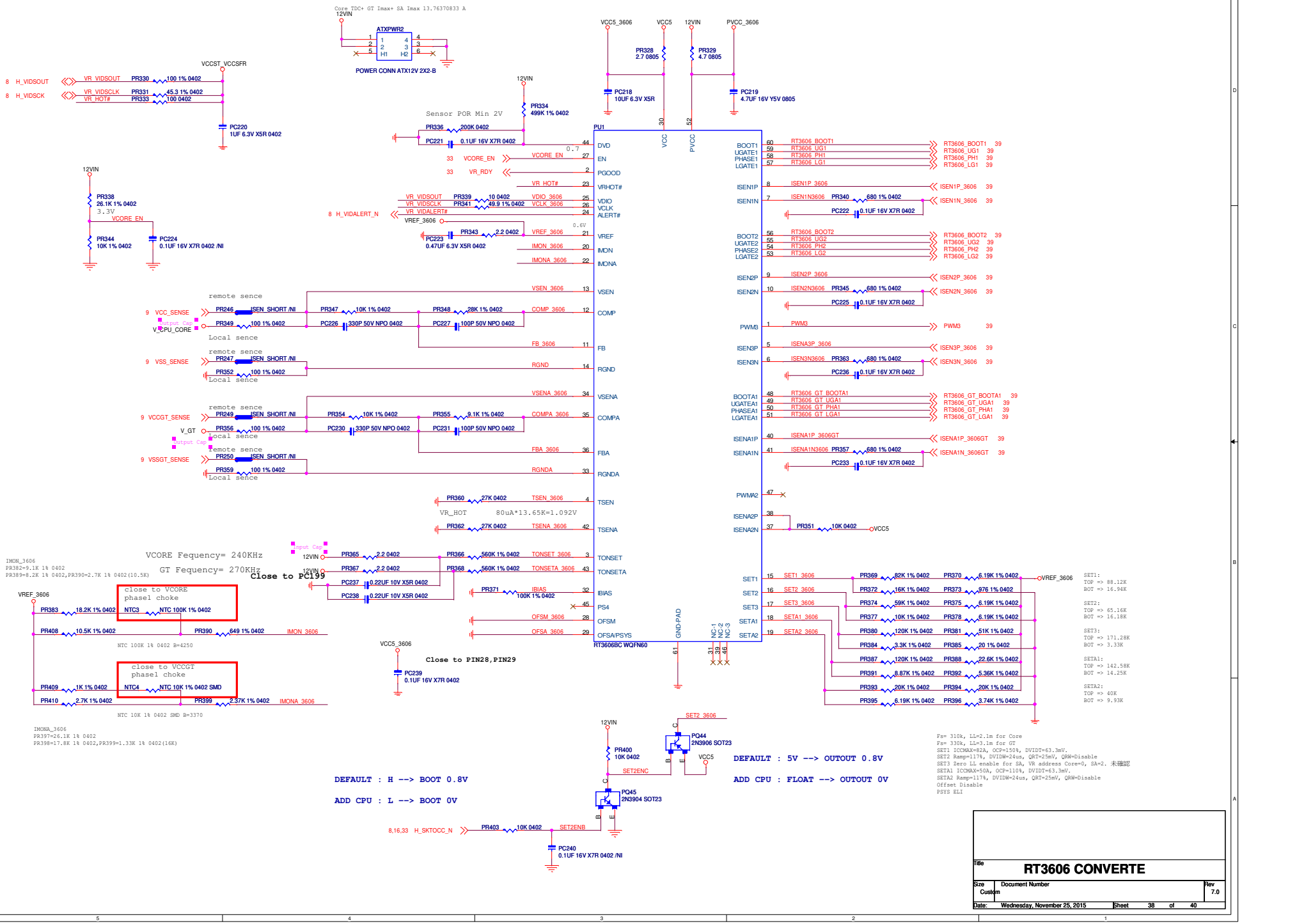
Core TDC+ GT Imax+ SA Imax 13.76370833 A
12VIN
ATXPWR2
POWER CONN ATX12V 2X2-B
VCCST_VCCSFR
8 H_VIDSOUT
8 H_VIDSCK
VR_VIDSOUT PR330 100 1% 0402
VR_VIDSCLK PR331 45.3 1% 0402
VR_HOT# PR333 100 0402
PC220 1UF 6.3V X5R 0402
VCC5_3606
VCC5
PVCC_3606
PR328 2.7 0805
PR329 4.7 0805
PC218 10UF 6.3V X5R
PC219 4.7UF 16V Y5V 0805
Sensor POR Min 2V
PR334 499K 1% 0402
PR336 200K 0402
PC221 0.1UF 16V X7R 0402
PU1
PR338 26.1K 1% 0402
3.3V
VCORE_EN
PR344 10K 1% 0402
PC224 0.1UF 16V X7R 0402 /NI
33 VCORE_EN
33 VR_RDY
VR_HOT#
VR_VIDSOUT PR339 10 0402 VDIO_3606
VR_VIDSCLK PR341 49.9 1% 0402 VCLK_3606
8 H_VIDALERT_N
VR_VIDALERT#
VREF_3606
PR343 2.2 0402
PC223 0.47UF 6.3V X5R 0402
IMON_3606
IMONA_3606
DVD
EN
PGOOD
VRHOT#
VDIO
VCLK
ALERT#
VREF
IMON
IMONA
VSEN_3606
VSEN
remote sence
9 VCC_SENSE
PR246 ISEN_SHORT /NI
PR349 100 1% 0402
V_CPU_CORE
Output Cap
Local sence
PR347 10K 1% 0402
PR348 28K 1% 0402
PR226 330P 50V NPO 0402
PR227 100P 50V NPO 0402
COMP_3606
COMP
FB_3606
FB
9 VSS_SENSE
PR247 ISEN_SHORT /NI
PR352 100 1% 0402
RGND
VSENA_3606
VSENA
9 VCCGT_SENSE
PR249 ISEN_SHORT /NI
PR356 100 1% 0402
V_GT
PR354 10K 1% 0402
PR355 9.1K 1% 0402
PR230 330P 50V NPO 0402
PR231 100P 50V NPO 0402
COMPA_3606
COMPA
FBA_3606
FBA
9 VSSGT_SENSE
PR250 ISEN_SHORT /NI
PR359 100 1% 0402
RGNDA
PR360 27K 0402
TSEN_3606
TSEN
VR_HOT 80uA*13.65K=1.092V
PR362 27K 0402
TSENA_3606
TSENA
VCORE Fequency= 240KHz
GT Fequency= 270KHz
Close to PC199
PR365 2.2 0402
PR367 2.2 0402
PC237 0.22UF 10V X5R 0402
PC238 0.22UF 10V X5R 0402
PR366 560K 1% 0402
PR368 560K 1% 0402
TONSET_3606
TONSETA_3606
PR371 100K 1% 0402
IBIAS
PS4
OFSM_3606
OFSA_3606
OFSM
OFSA/PSYS
RT3606BC WQFN60
GND-PAD
NC-1
NC-2
NC-3
IMON_3606
PR382=9.1K 1% 0402
PR389=8.2K 1% 0402,PR390=2.7K 1% 0402(10.5K)
VREF_3606
close to VCORE
phasel choke
PR383 18.2K 1% 0402
NTC3
NTC 100K 1% 0402
PR408 10.5K 1% 0402
PR390 649 1% 0402
IMON_3606
NTC 100K 1% 0402 B=4250
close to VCCGT
phasel choke
PR409 1K 1% 0402
NTC4
NTC 10K 1% 0402 SMD
PR410 2.7K 1% 0402
PR399 2.37K 1% 0402
IMONA_3606
NTC 10K 1% 0402 SMD B=3370
IMONA_3606
PR397=26.1K 1% 0402
PR398=17.8K 1% 0402,PR399=1.33K 1% 0402(16K)
VCC5_3606
Close to PIN28,PIN29
PC239 0.1UF 16V X7R 0402
DEFAULT : H --> BOOT 0.8V
ADD CPU : L --> BOOT 0V
PR400 10K 0402
SET2ENC
PQ44 2N3906 SOT23
PQ45 2N3904 SOT23
8,16,33 H_SKTOCC_N
PR403 10K 0402
SET2ENB
PC240 0.1UF 16V X7R 0402 /NI
DEFAULT : 5V --> OUTOUT 0.8V
ADD CPU : FLOAT --> OUTOUT 0V
BOOT1 RT3606_BOOT1
UGATE1 RT3606_UG1
PHASE1 RT3606_PH1
LGATE1 RT3606_LG1
ISEN1P ISEN1P_3606
ISEN1N ISEN1N3606 PR340 680 1% 0402
PC222 0.1UF 16V X7R 0402
BOOT2 RT3606_BOOT2
UGATE2 RT3606_UG2
PHASE2 RT3606_PH2
LGATE2 RT3606_LG2
ISEN2P ISEN2P_3606
ISEN2N ISEN2N3606 PR345 680 1% 0402
PC225 0.1UF 16V X7R 0402
PWM3
ISEN3P ISENA3P_3606
ISEN3N ISEN3N3606 PR363 680 1% 0402
PC236 0.1UF 16V X7R 0402
BOOTA1 RT3606_GT_BOOTA1
UGATEA1 RT3606_GT_UGA1
PHASEA1 RT3606_GT_PHA1
LGATEA1 RT3606_GT_LGA1
ISENA1P ISENA1P_3606GT
ISENA1N ISENA1N3606 PR357 680 1% 0402
PC233 0.1UF 16V X7R 0402
PWMA2
ISENA2P
ISENA2N PR351 10K 0402 VCC5
SET1_3606
SET2_3606
SET3_3606
SETA1_3606
SETA2_3606
PR369 82K 1% 0402
PR370 6.19K 1% 0402
PR372 16K 1% 0402
PR373 976 1% 0402
PR374 59K 1% 0402
PR375 6.19K 1% 0402
PR377 10K 1% 0402
PR378 6.19K 1% 0402
PR380 120K 1% 0402
PR381 51K 1% 0402
PR384 3.3K 1% 0402
PR385 20 1% 0402
PR387 120K 1% 0402
PR388 22.6K 1% 0402
PR391 8.87K 1% 0402
PR392 5.36K 1% 0402
PR393 20K 1% 0402
PR394 20K 1% 0402
PR395 6.19K 1% 0402
PR396 3.74K 1% 0402
SET1: TOP => 88.12K BOT => 16.94K
SET2: TOP => 65.16K BOT => 16.18K
SET3: TOP => 171.28K BOT => 3.33K
SETA1: TOP => 142.58K BOT => 14.25K
SETA2: TOP => 40K BOT => 9.93K
Fs= 310k, LL=2.1m for Core
Fs= 330k, LL=3.1m for GT
SET1 ICCMAX=82A, OCP=150%, DVIDT=63.3mV.
SET2 Ramp=117%, DVIDW=24us, QRT=25mV, QRW=Disable
SET3 Zero LL enable for SA, VR address Core=0, SA=2. 未確認
SETA1 ICCMAX=50A, OCP=110%, DVIDT=63.3mV.
SETA2 Ramp=117%, DVIDW=24us, QRT=25mV, QRW=Disable
Offset Disable
PSYS ELI
Title
RT3606 CONVERTE
Size Custom
Document Number
Rev 7.0
Date: Wednesday, November 25, 2015
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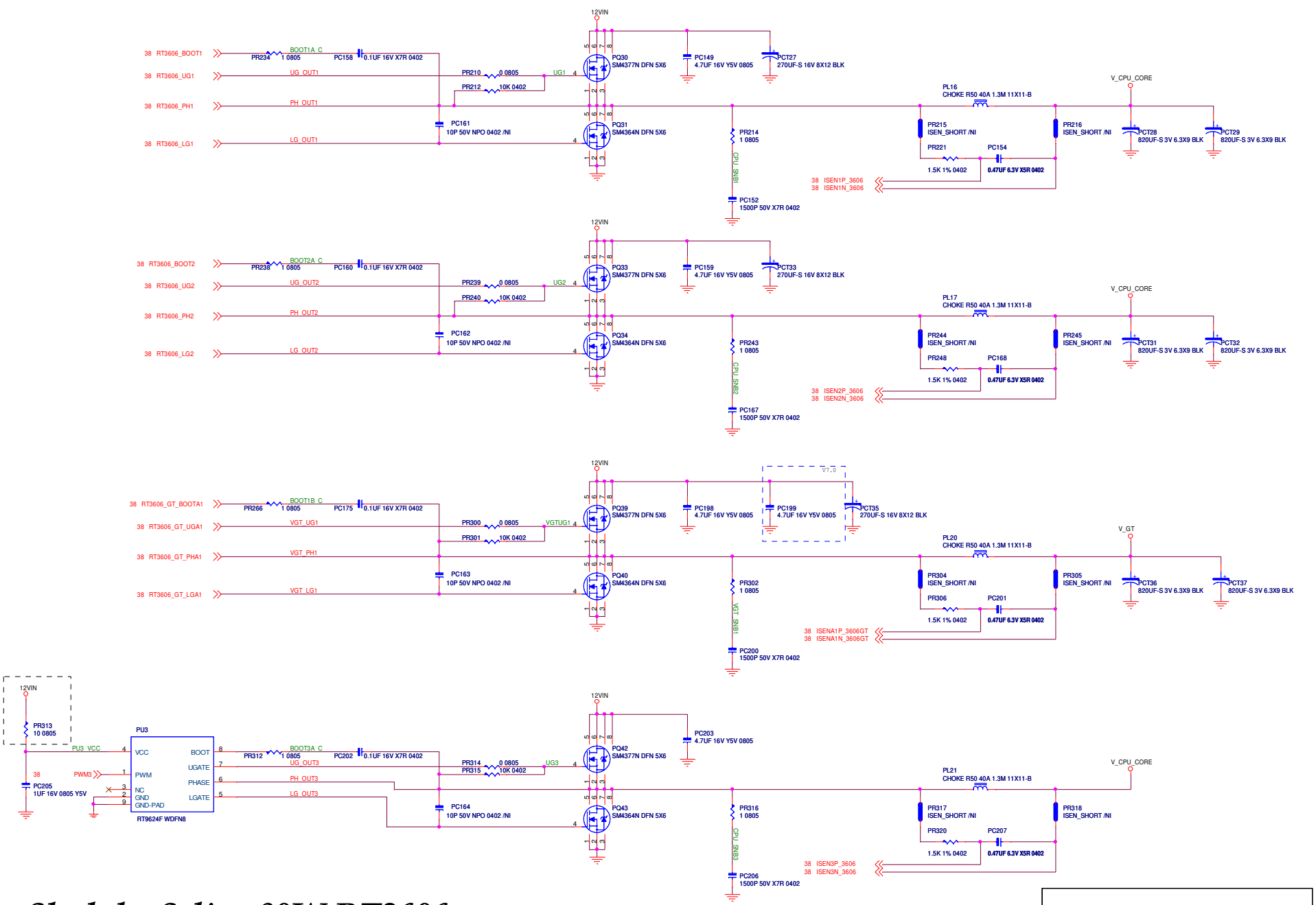


# *Skylake S-line 80W RT3606*

| | | |
|---|---|---|
| Title | RT3606_VCORE_PHASE | |
| Size: Custom | Document Number | Rev: 7.0 |
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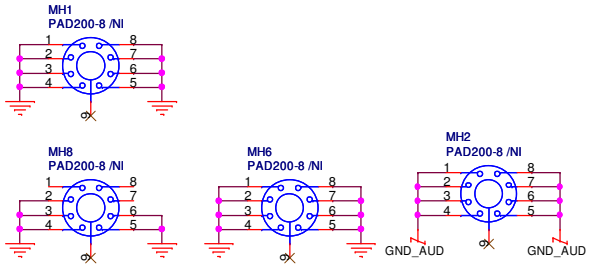
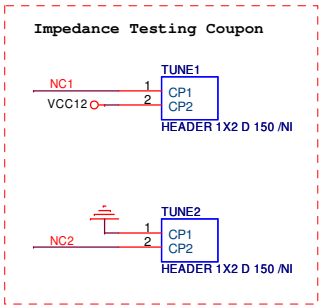
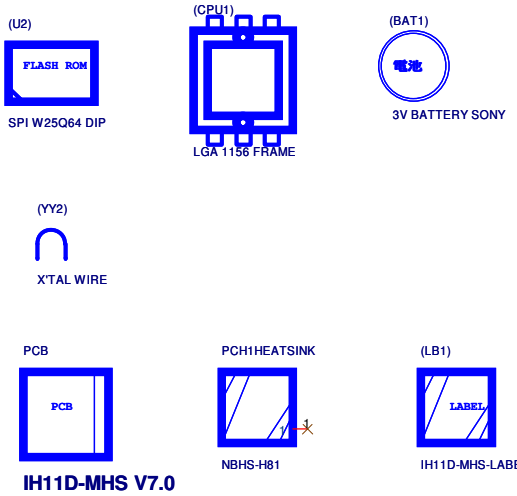



98-IH11DMHS-R01P
86-IH11DMHS-R01P-70
96-IH11DMHS-R01P-70

15-Y84-170050R1 IH11D-MHS VER:7.0 /OSP/BLACK/(170.03*189.99*1.5)mm/4L /P&Q

98-IH11GMHS-R01P
86-IH11GMHS-R01P-70
96-IH11GMHS-R01P-70




SKL S 42 65W
PL1 PL2 PL4
69W 82-87W 99W

SKL S 42 80W
PL1 PL2 PL4
82W 82-87W 102W

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| | | |
|---|---|---|
| Title: BOM | | |
| Size: B | Document Number: IH11D-MHS | Rev: 7.0 |
| Date: Friday, November 20, 2015 | Sheet 40 of 40 | |