2016 Apollo Lake Ironhide_APL"

Schematics Document

EMMC

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

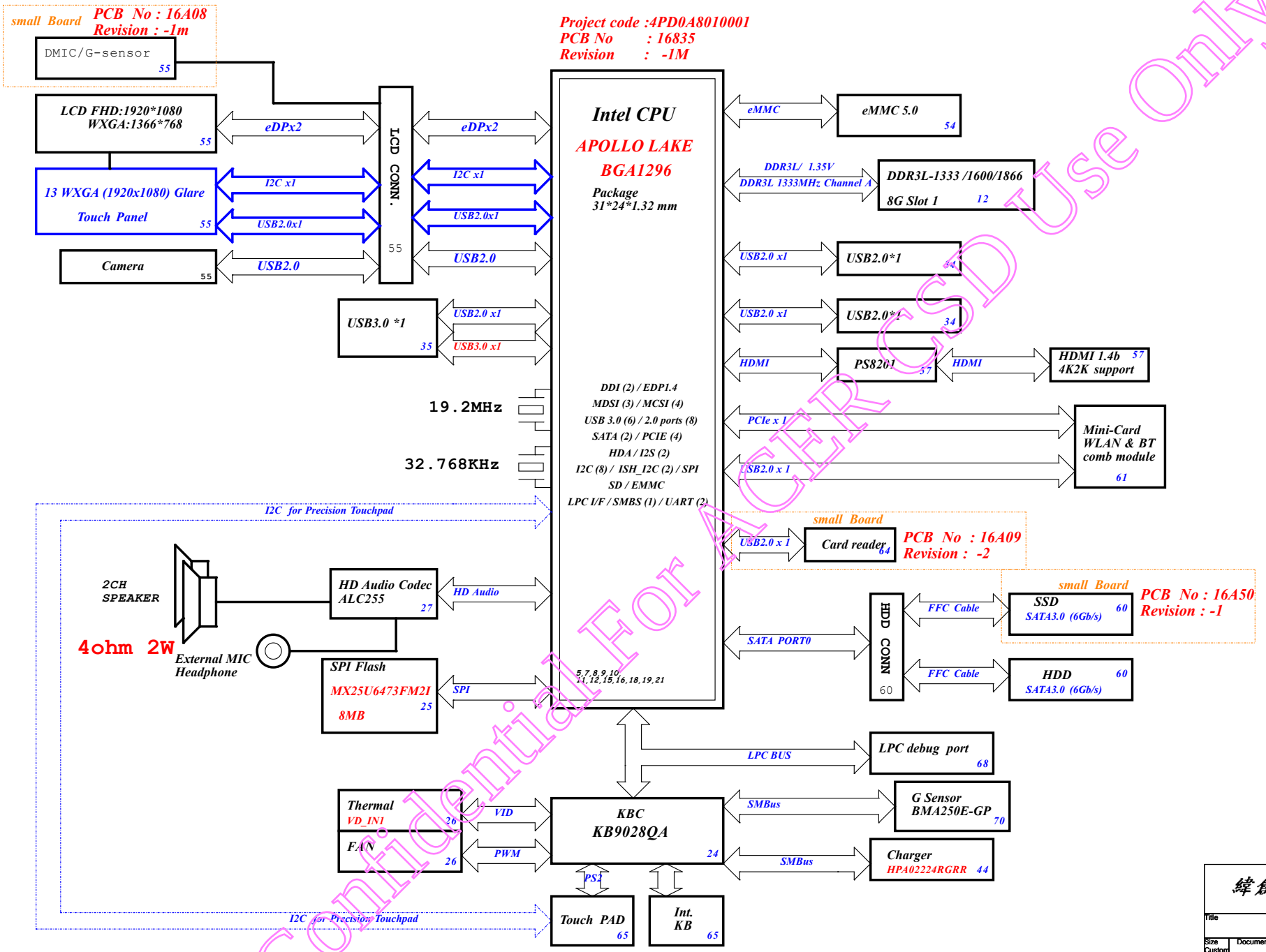
Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 1 of 106

Ironhide_APL Board Block Diagram

small Board PCB No : 16A08
Revision : -1m

Project code :4PD0A8010001
PCB No : 16835
Revision : -1M



CHARGER HPA02224	44
INPUTS	OUTPUTS
19V_DCBATOUT	BT+

SYSTEM DC/DC RT6575DGQW	45
INPUTS	OUTPUTS
19V_DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC RT5073AGQW-GP	46
INPUTS	OUTPUTS
19V_DCBATOUT	1D8V_S5 1D24V_S5 1D05V_S0
PWR_VDDQ	PWR_VTT

SYSTEM DC/DC RT9610BZQW-GP	47
INPUTS	OUTPUTS
5V_S5	1V_CPU_VCGI

CPU DC/DC RT9610BZQW-GP	50
INPUTS	OUTPUTS
5V_S5	1V_CPU_VNN

CPU DC/DC RT9610BZQW-GP	51
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ

SYSTEM Load switch APE8910	40
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3V_S0
1D8V_S5	1D8V_S0

SYSTEM DC/DC TL70215	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

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SSID = CPU

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SSID = CPU

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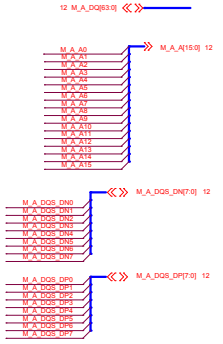
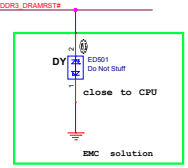
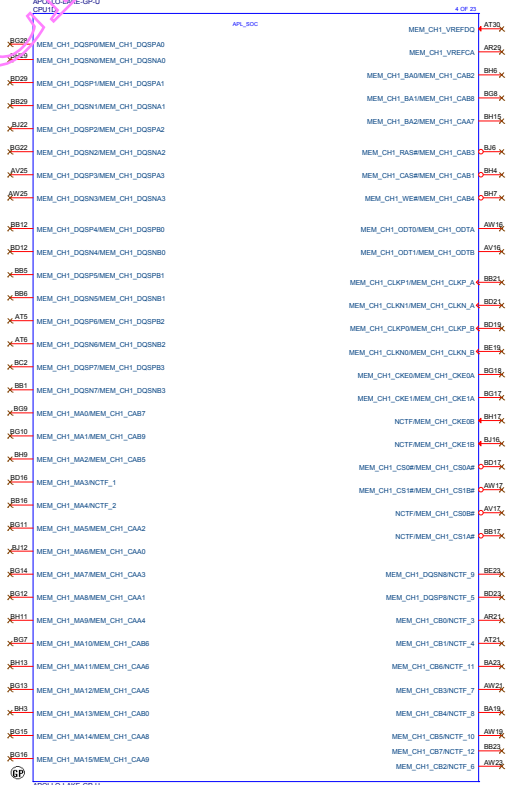
SSID = CPU







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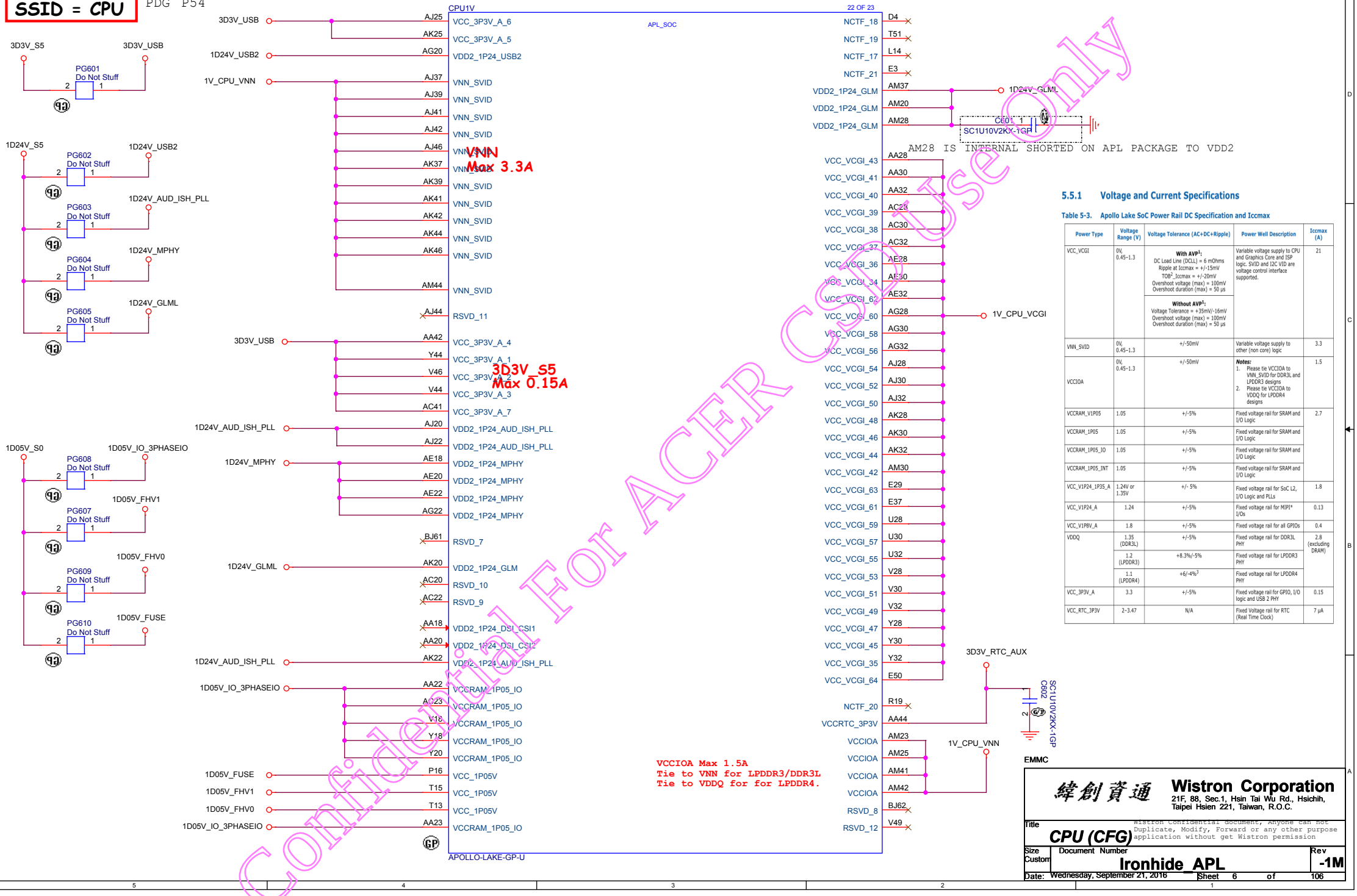
Title: CPU (DDR)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 5 of 106

SSID = CPU PDG P54



5.5.1 Voltage and Current Specifications

Table 5-3. Apollo Lake SoC Power Rail DC Specification and Iccmax

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0V, 0.45~1.3	**With AVP[1]:** DC Load Line (DCLL) = 6 mOhms Ripple at Iccmax = +/-15mV TOP[2] Iccmax = +/-20mV Overshoot voltage (max) = 100mV Overshoot duration (max) = 50 µs **Without AVP[1]:** Voltage Tolerance = +35mV/-16mV Overshoot voltage (max) = 100mV Overshoot duration (max) = 50 µs	Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I2C VID are voltage control interface supported.	21
VNN_SVID	0V, 0.45~1.3	+/-50mV	Variable voltage supply to other (non core) logic	3.3
VCCIOA	0V, 0.45~1.3	+/-50mV	**Notes:** 1. Please tie VCCIOA to VNN_SVID for DDR3L and LPDDR3 designs 2. Please tie VCCIOA to VDDQ for LPDDR4 designs	1.5
VCCRAM_V1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	2.7
VCCRAM_1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCCRAM_1P05_IO	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCCRAM_1P05_INT	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	Fixed voltage rail for SoC L2, I/O Logic and PLLs	1.8
VCC_V1P24_A	1.24	+/-5%	Fixed voltage rail for MIPI* I/Os	0.13
VCC_V1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VDDQ	1.35 (DDR3L)	+/-5%	Fixed voltage rail for DDR3L PHY	2.8 (excluding DRAM)
	1.2 (LPDDR3)	+8.3%/-5%	Fixed voltage rail for LPDDR3 PHY	
	1.1 (LPDDR4)	+6/-4%[3]	Fixed voltage rail for LPDDR4 PHY	
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic and USB 2 PHY	0.15
VCC_RTC_3P3V	2~3.47	N/A	Fixed Voltage rail for RTC (Real Time Clock)	7 µA

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Size: Custom	Document Number: **Ironhide_APL**		Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 6 of 106		

SSID = CPU

CPU1W

APL_SOC

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APOLLO-LAKE-GP-U

1D05V_S0

1D8V_S5

1D35V_S3

46 VSSGI_SENSE

46 VCCGI_SENSE

46 VNNCORE_SENSE

1D8V_S5
Max 0.4A

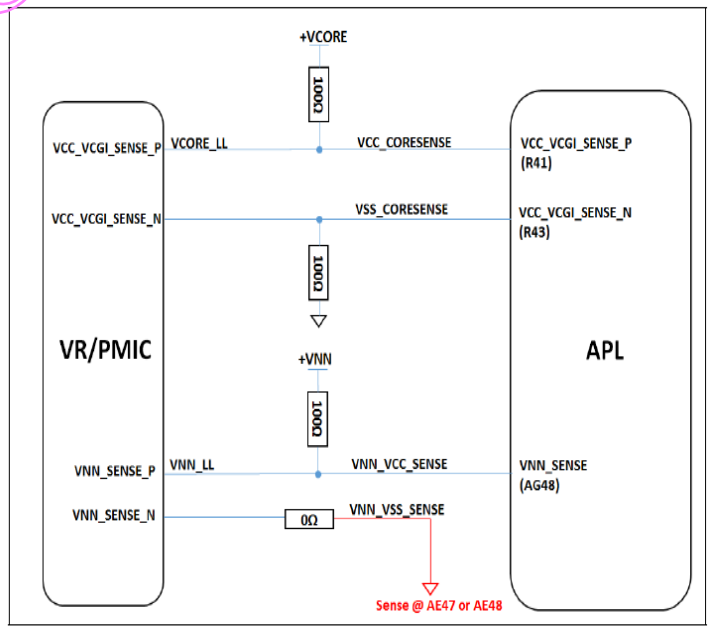
1D05V_S0
Max 2.7A

VDDQ
Max 2.8A

1V_CPU_VCGI

E6	NCTF_16		VCC_1P8V_A_1	AE42	
AA25	VCCRAM_1P05		VCC_1P8V_A_2	AE44	
AC25	VCCRAM_1P05		VCC_1P8V_A_3	AA46	1D8V_S5
AE25	VCCRAM_1P05		VCC_1P8V_A_4	AC42	
U22	VCCRAM_1P05		VCC_1P8V_A_5	AC44	
U23	VCCRAM_1P05		VCC_1P8V_A_6	AC46	
V22	VCCRAM_1P05		VCC_1P8V_A_7	AE46	
V23	VCCRAM_1P05		VCC_1P8V_A_8	AG25	
V25	VCCRAM_1P05		NCTF_13	R17	
Y23	VCCRAM_1P05		VCC_VCGI_32	F29	1V_CPU_VCGI
			VCC_VCGI_31	E35	
U20	VCCRAM_1P05		VCC_VCGI_33	AK34	
U25	VCCRAM_1P05				
Y25	VCCRAM_1P05		VCC_VCGI_30	E45	
			VCC_VCGI_27	AC37	
AM32	RSVD_4		VCC_VCGI_24	AE36	
AN32	RSVD_6		VCC_VCGI_21	AE37	
D1	RSVD_2		VCC_VCGI_18	AG36	
BG63	RSVD_1		VCC_VCGI_15	E43	
			VCC_VCGI_12	E48	
V48	RSVD_3		VCC_VCGI_9	R45	
VSSGI_SENSE R43	VCC_VCGI_SENSE_N		VCC_VCGI_7	R47	
			VCC_VCGI_6	U36	
VCCGI_SENSE R41	VCC_VCGI_SENSE_P		VCC_VCGI_3	U37	
VNNCORE_SENSE AG48	VNN_SENSE		VCC_VCGI_1	U39	
			VCC_VCGI_28	U41	
AN18	VDDQ_15		VCC_VCGI_25	U42	
AN20	VDDQ_14		VCC_VCGI_22	U44	
AN22	VDDQ_13		VCC_VCGI_19	U46	
AN23	VDDQ_12		VCC_VCGI_16	U47	
AN41	VDDQ_11		VCC_VCGI_13	U48	
AN42	VDDQ_10		VCC_VCGI_10	V36	
AN44	VDDQ_9		VCC_VCGI_8	V37	
AN46	VDDQ_8		VCC_VCGI_5	V39	
AR17	VDDQ_6		VCC_VCGI_4	V41	
AR47	VDDQ_7		VCC_VCGI_2	Y36	
AT13	VDDQ_5		VCC_VCGI_29	Y37	
AT17	VDDQ_4		VCC_VCGI_26	Y39	
AT47	VDDQ_3		VCC_VCGI_23	Y41	
AT51	VDDQ_2		VCC_VCGI_20	AC36	
AV14	VDDQ_1		VCC_VCGI_17	AA36	
AV50	VDDQ_16		VCC_VCGI_14	AA37	
F23	NCTF_14		VCC_VCGI_11	AA39	
E23	NCTF_15				
BJ3	RSVD_5				

Figure 3-4. VCGI, VSS, VNN Sense Guideline



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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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SSID = CPU

HDMI

57 HDMI_CLK_CPU
57 HDMI_DATA_CPU
57 HDMI_DATA_CPU_P2
57 HDMI_DATA_CPU_N2
57 HDMI_DATA_CPU_P1
57 HDMI_DATA_CPU_N1
57 HDMI_DATA_CPU_P0
57 HDMI_DATA_CPU_N0
57 HDMI_DATA_CPU_P3
57 HDMI_DATA_CPU_N3
57 HDMI_DET_CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU
18,55 eDP_HPD_CPU

HDMI

1D8V_S0
RN888
DY
Do Not Stuff
Vth(max)=1.1V
Q804
PJT138KA-GP
075.00138.0A7C
HDMI_CLK_CPU
HDMI_DATA_CPU
HDMI_CLK_CPU_R
HDMI_DATA_CPU_R
RN801
SRN2K2J-1-GP
3D3V_S0
CPU1E
APL_SOC
5 OF 23
DDI0_DDC_SCL
DDI0_DDC_SDA
DDI1_DDC_SCL
DDI1_DDC_SDA
1.8V
DDI0_TXP_0
DDI0_TXN_0
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_3
DDI0_TXN_3
DDI0_RCOMP_P
DDI0_RCOMP_N
DDI0_AUXP
DDI0_AUXN
HDMI_DATA_CPU_P2
HDMI_DATA_CPU_N2
HDMI_DATA_CPU_P1
HDMI_DATA_CPU_N1
HDMI_DATA_CPU_P0
HDMI_DATA_CPU_N0
HDMI_DATA_CPU_P3
HDMI_DATA_CPU_N3
1.05V
R801
DY
Do Not Stuff
only for DP

EDP

eDP_AUX_CPU_P
eDP_AUX_CPU_N
R802
402R2F-GP
EDP_RCOMP_N
EDP_RCOMP_P
EDP_TX_CPU_P0
EDP_TX_CPU_N0
EDP_TX_CPU_P1
EDP_TX_CPU_N1
EDP_AUXP
EDP_AUXN
EDP_RCOMP_N
EDP_RCOMP_P
EDP_TXP_0
EDP_TXN_0
EDP_TXP_1
EDP_TXN_1
EDP_TXP_2
EDP_TXN_2
EDP_TXP_3
EDP_TXN_3
1.05V
DDI1_AUXP
DDI1_AUXN
DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
1.05V
APOLLO-LAKE-GP-U

eDP* Channel
eDP Connector
Panel Power Control Circuit
Panel Backlight Power Control Circuit
Panel Backlight Control Circuit
HPD Circuit
402 ohm/1%
ATL SoC

CPU1F
6 OF 23
MDSI_A_DP_0
MDSI_A_DN_0
MDSI_A_DP_1
MDSI_A_DN_1
MDSI_A_DP_2
MDSI_A_DN_2
MDSI_A_DP_3
MDSI_A_DN_3
MDSI_A_CLKP
MDSI_A_CLKN
1.24V
MDSI_C_DP_0
MDSI_C_DN_0
MDSI_C_DP_1
MDSI_C_DN_1
MDSI_C_DP_2
MDSI_C_DN_2
MDSI_C_DP_3
MDSI_C_DN_3
MDSI_C_CLKP
MDSI_C_CLKN
1.24V
MIPI_I2C_SDA
MIPI_I2C_SCL
GPIO_199/HV_DDI1_HPD
GPIO_203/HV_DDI0_HPD
MDSI_A_TE
MDSI_C_TE
1.8V
PNL0_VDDEN
PNL0_BKLTEN
PNL0_BKLTCTL
PNL1_VDDEN
PNL1_BKLTEN
PNL1_BKLTCTL
1.8V
eDP_VDDEN_CPU
eDP_BLEN_CPU
R804
Do Not Stuff
DY
R803
1MR2J-L3-GP
R805
Do Not Stuff
DY
R827
Do Not Stuff
DY
RN827
SRN2K2J-1-GP
L_BKLT_CTRL_B
eDP_BLCTRL_CPU_RR
eDP_BLCTRL_CPU
Q801
LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.T3904.C11

close to connector
HDMI_DET_CPU
Q803
2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.06587.0031
R844
10KR2J-L-GP
HDMI_DET_CPU_RR
R815
100KR2J-4-GP

DDI0_RCOMP_P/N	O	V1P05	Display PHY	Port 0/1: This signal is used for pre-driver slew rate compensation. **Note:** The SoC will use the eDP_RCOMP value for DDI Port 0/1 as well. Please ensure that the eDP_RCOMP pin is populated with the correct value. There is no need to have this DDI0_RCOMP on the platform.

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Title: CPU (DDI/EDP/GPIO)

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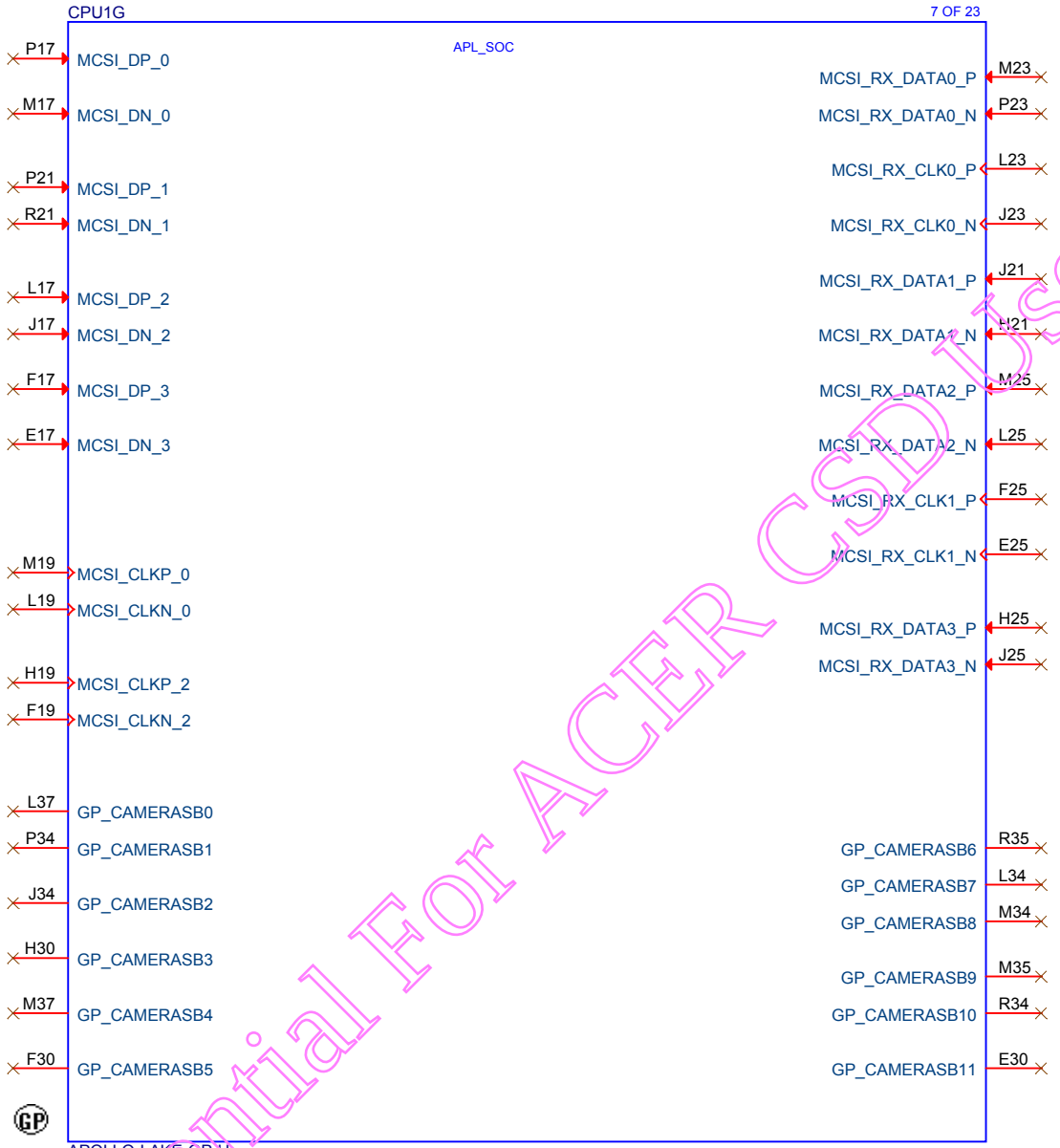
Date: Wednesday, September 21, 2016 | Sheet 8 of 106

SSID = CPU



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Title: **CPU (VSS)**

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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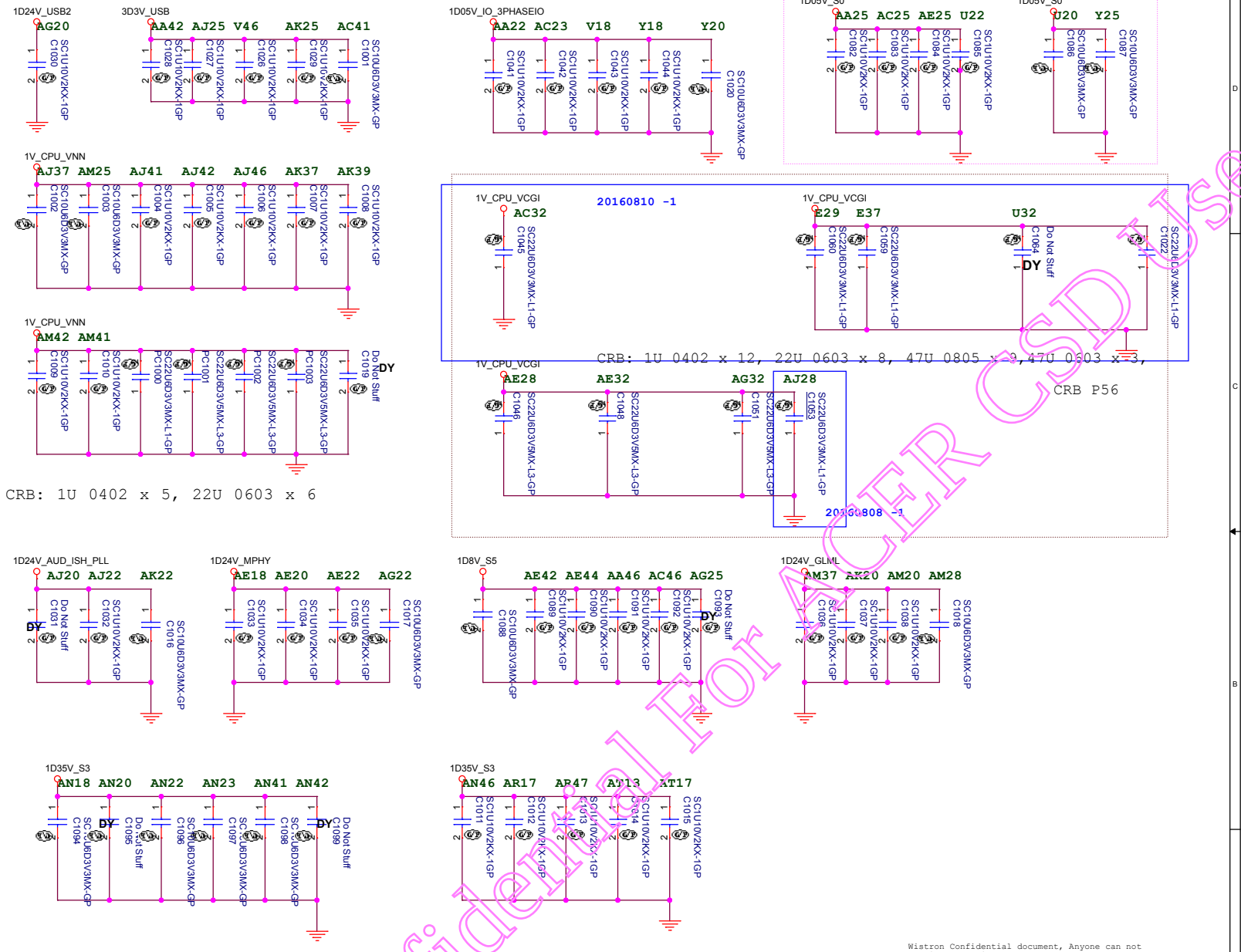
SSID = CPU



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Title: CPU (Power CAP1)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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SSID = CPU

Blanking

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Title: CPU (Power CAP2)

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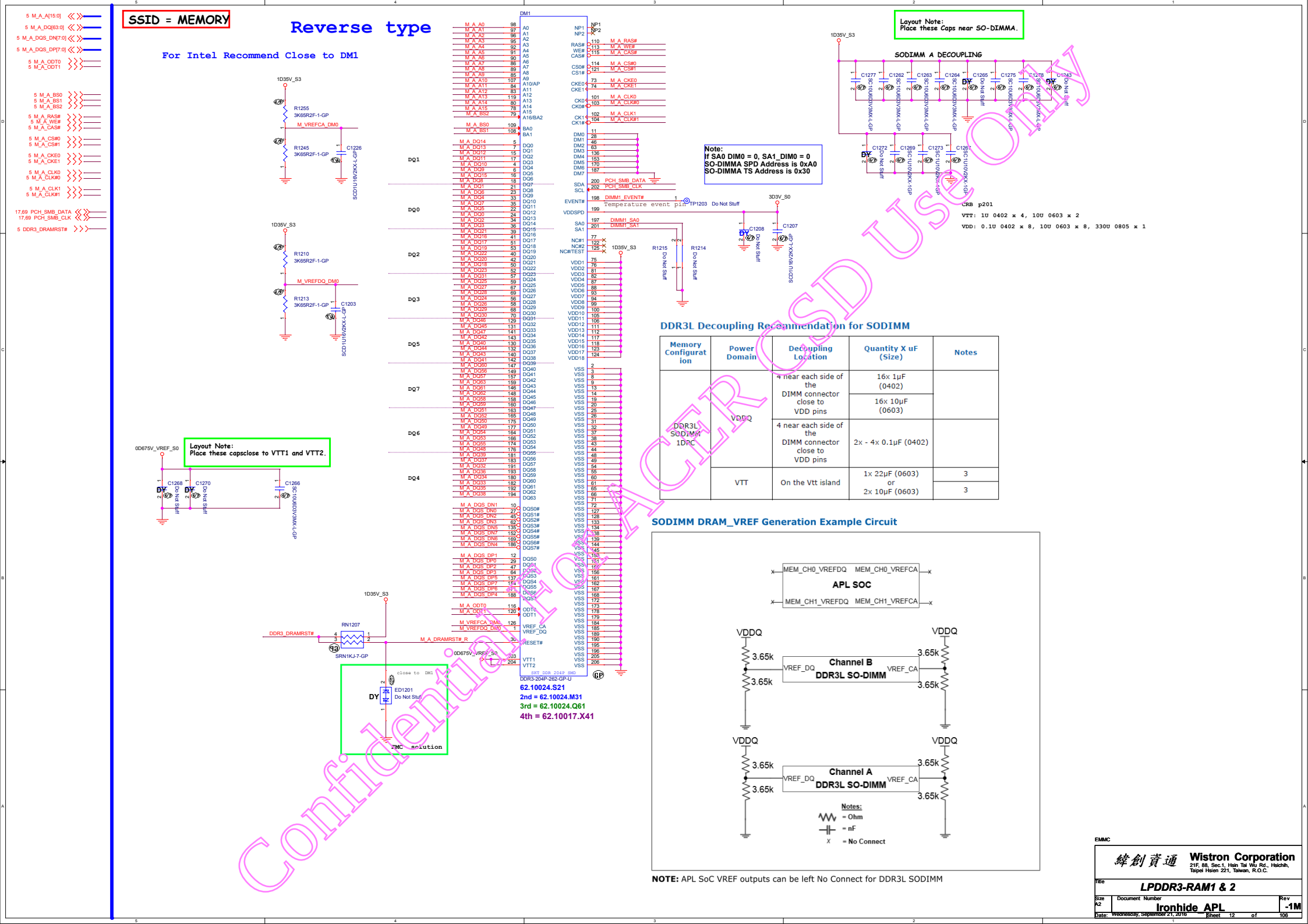
SSID = MEMORY

Reverse type

For Intel Recommend Close to DM1



DDR3L Decoupling Recommendation for SODIMM

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR3L SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
			16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	2x - 4x 0.1µF (0402)	
	VTT	On the Vtt island	1x 22µF (0603) or 2x 10µF (0603)	3
				3

SODIMM DRAM_VREF Generation Example Circuit

NOTE: APL SoC VREF outputs can be left No Connect for DDR3L SODIMM

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Title: LPDDR3-RAM1 & 2

Size	Document Number	Rev
A2	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 12 of 106

SSID = MEMORY

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Title: *LPDDR3-RAM1 & 2*

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 13 of 106

SSID = CPU

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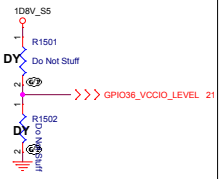
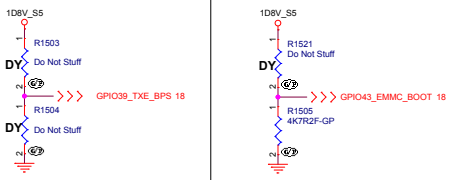
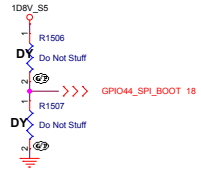
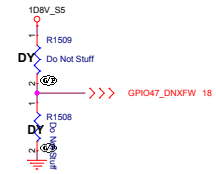
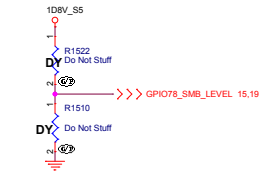
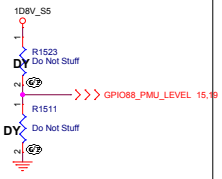
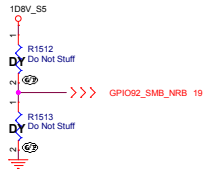
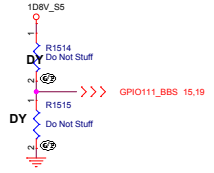
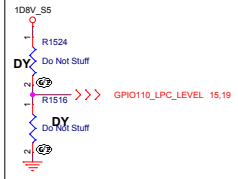
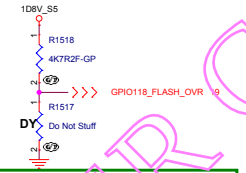
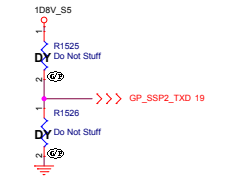
Title: (Reserved)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 14 of 106

SSID = STRAP

GPIO	GPIO_36	GPIO_39	GPIO_43	GPIO_44	GPIO_47	GPIO_78
Schematic						
High	VCCIO used for B-step	enable CSE ROM bypass	enable EMMC Boot Weak internal pull-up	default (allow SPI as a boot source) Weak internal pull-up	force DNX FW Load	Weak internal pull-up SMBus 1.8V mode select
Low	default (A-step) Weak internal pull-down	default (disable bypass) Weak internal pull-down	Not allow eMMC as a boot source	disable	default (don't force DNX FW Load) Weak internal pull-down	SMBus 3.3V mode select

GPIO	GPIO_88	GPIO_92	GPIO_111	GPIO_110	GPIO_118	GPIO_120	GPIO_123
Schematic							
High	Weak internal pull-up PMU 1.8V mode select	SMBS No-reboot enable	Do not boot from SPI Weak internal pull-up	Weak internal pull-up LPC 1.8V mode select	Flash Descriptor Override	Two SWAP override enable	RSVD (Internal 20K PU)
Low	PMU 3.3V mode select	default (SMBus No Re-Boot Disable) Weak internal pull-down	boot from SPI	LPC 3.3V mode select	No Override (Normal Operation) Weak internal pull-down	default (Disable top swap override) Weak internal pull-down	RSVD

0921

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) ***Note:*** This strap will only be used for B-step. For A-step this rails should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** Apollo Lake supports TXE3.0 (this is also called CSE) ***Note:*** This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Note:*** DnX: Download and Execute ***Note:*** This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PD	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

Note: All the straps are sampled at Rising Edge of RSM_RST_N

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 15 of 106

SSID = PCH

Apollo Lake		2016 Ironhide
SATA P0		HDD/SSD
SATA P1	USB3 Port5	
PCIe Port 0		
PCIe Port 1		
PCIe Port 2		
PCIe Port 3	USB3 Port4	WIFI
PCIe Port 4	USB3 Port3	
PCIe Port 5	USB3 Port2	
USB3	USB3 Port1	
USB2	USB3 Port0 (OTG)	USB 3 I/O
USB2	USB2 Port0	USB 3 I/O
USB2	USB2 Port1	
USB2	USB2 Port2	USB 2 I/O
USB2	USB2 Port3	USB 2 I/O
USB2	USB2 Port4	BT
USB2	USB2 Port5	TS
USB2	USB2 Port6	CCD
USB2	USB2 Port7	CR
USB3	USB SSIC	
eMMC	eMMC	eMMC
SDIO	SDIO	

USB3.0 port1

35 USB1_USB30_TX_P
35 USB1_USB30_TX_N
35 USB1_USB30_RX_P
35 USB1_USB30_RX_N

HDD

60 HDD_SATA_TX_N
60 HDD_SATA_TX_P
60 HDD_SATA_RX_N
60 HDD_SATA_RX_P

WLAN

61,89 WLAN_PCIE_TX_P
61,89 WLAN_PCIE_TX_N
61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_CLK_CPU
61,89 WLAN_CLK_CPU#
61,89 WLAN_CLKREQ_CPU#

18,24,61,89 PCIE_WAKE#

CPU1I — 9 OF 23 — APL_SOC — APOLLO-LAKE-GP-U

WLAN_PCIE_TX_P — C1616 SCD1U16V2KX-L-GP — WLAN_CPU_TX_P — P3 PCIE_P3_USB3_P4_TXP
WLAN_PCIE_TX_N — C1617 SCD1U16V2KX-L-GP — WLAN_CPU_TX_N — P2 PCIE_P3_USB3_P4_TXN
WLAN_PCIE_RX_P — P12 PCIE_P3_USB3_P4_RXP
WLAN_PCIE_RX_N — P10 PCIE_P3_USB3_P4_RXN

R1601 402R2F-GP: PCIE_OBSP_CPU — F6 PCIE2_USB3_SATA3_RCOMP_P; PCIE_OBSN_CPU — F5 PCIE2_USB3_SATA3_RCOMP_N

L2 PCIE_P5_USB3_P2_TXP; L1 PCIE_P5_USB3_P2_TXN; K7 PCIE_P5_USB3_P2_RXP; M7 PCIE_P5_USB3_P2_RXN
N2 PCIE_P4_USB3_P3_TXP; M2 PCIE_P4_USB3_P3_TXN; H5 PCIE_P4_USB3_P3_RXP; H6 PCIE_P4_USB3_P3_RXN

1.24V

PCIE_P2_TXP T2; PCIE_P2_TXN T3; PCIE_P2_RXP M5; PCIE_P2_RXN M6
PCIE_P1_TXP R1; PCIE_P1_TXN R2; PCIE_P1_RXP T10; PCIE_P1_RXN T12
PCIE_P0_TXP V3; PCIE_P0_TXN V2; PCIE_P0_RXP P7; PCIE_P0_RXN P6

1.24V

PCIE_WAKE3# N62 — PCIE_WAKE3_CPU — R1602 (1, 2, Do Not Stuff) — PCIE_WAKE#
PCIE_WAKE2# P61 — PCIE_WAKE2_CPU
PCIE_WAKE1# P62 — PCIE_WAKE1_CPU
PCIE_WAKE0# R62 — PCIE_WAKE0_CPU

1.8V

1D8V_S5 — RN1655 (PCIE_WAKE3_CPU, PCIE_WAKE2_CPU, PCIE_WAKE1_CPU, PCIE_WAKE0_CPU) — SRN10KJ-12-GP

CPU1J — 10 OF 23 — APL_SOC — APOLLO-LAKE-GP-U

USB3.0 port1

USB1_USB30_TX_P — J1 USB3_P0_TXP
USB1_USB30_TX_N — J2 USB3_P0_TXN
USB1_USB30_RX_P — K9 USB3_P0_RXP
USB1_USB30_RX_N — K10 USB3_P0_RXN

K3 USB3_P1_TXP; K2 USB3_P1_TXN; F2 USB3_P1_RXP; G2 USB3_P1_RXN

1.24V

HDD

HDD_SATA_TX_P — Y3 SATA_P0_TXP
HDD_SATA_TX_N — Y2 SATA_P0_TXN
HDD_SATA_RX_P — T9 SATA_P0_RXP
HDD_SATA_RX_N — T7 SATA_P0_RXN

W1 SATA_P1_USB3_P5_TXP; W2 SATA_P1_USB3_P5_TXN; T5 SATA_P1_USB3_P5_RXP; T6 SATA_P1_USB3_P5_RXN

PCIE_CLKOUT3P B7 — WLAN_CLK_CPU
PCIE_CLKOUT3N B5 — WLAN_CLK_CPU#
PCIE_CLKOUT2P A7
PCIE_CLKOUT2N B8
PCIE_CLKOUT1P C10
PCIE_CLKOUT1N A10
PCIE_CLKOUT0P C11
PCIE_CLKOUT0N B11

1.05V

PCIE_CLKREQ3# AJ62 — WLAN_CLKREQ_CPU#
PCIE_CLKREQ2# AH61 — PCIE_CLKREQ2#
PCIE_CLKREQ1# AH62 — PCIE_CLKREQ1#
PCIE_CLKREQ0# AK62 — PCIE_CLKREQ0#

1.8V

USB_SSIC_0_TX_P AH13
USB_SSIC_0_TX_N AH12
USB_SSIC_0_RX_P AG16
USB_SSIC_0_RX_N AG15

1.05V

1D8V_S5 — RN1601 (PCIE_CLKREQ2#, PCIE_CLKREQ1#, WLAN_CLKREQ_CPU#, PCIE_CLKREQ0#) — SRN10KJ-12-GP

WLAN

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (USB/LPC/GPIO)
Size: Custom | Document Number: Ironhide_APL | Rev: -1M
Date: Wednesday, September 21, 2016 | Sheet 16 of 106

SSID = CPU

12,69 PCH_SMB_DATA
12,69 PCH_SMB_CLK

64 CARD1_USB20_P
64 CARD1_USB20_N — Card reader

61,89 BT_USB20_P
61,89 BT_USB20_N — BT

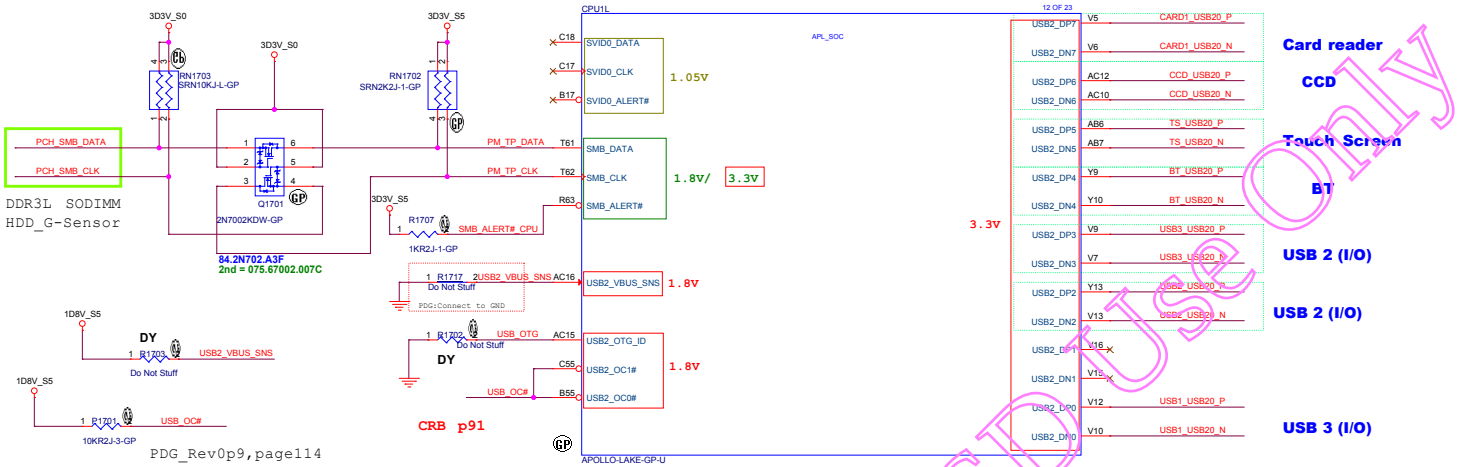
55 TS_USB20_N
55 TS_USB20_P — Touch Screen

55 CCD_USB20_P
55 CCD_USB20_N — CCD

34 USB3_USB20_P
34 USB3_USB20_N — USB2.0 Port2

34 USB2_USB20_P
34 USB2_USB20_N — USB2.0 Port1

35 USB1_USB20_P
35 USB1_USB20_N — USB3.0 Port1



Card reader
CCD
Touch Screen
BT
USB 2 (I/O)
USB 2 (I/O)
USB 3 (I/O)

Table 61. Over current Pin Default Usage

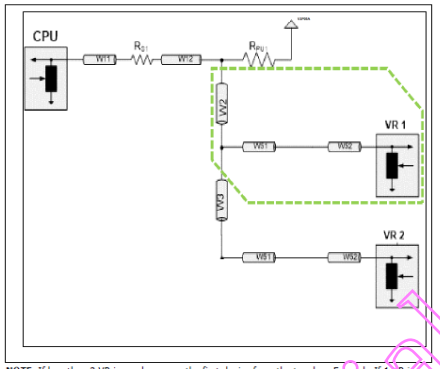
Pin	Default Port Mapping
OC0#	Port 0
OC1#	Port 1-7

Table 62. Over current Pin Example Configuration

Location	Number of USB Ports	USB Ports Number	OC Pins Used
External Topology	1	0	OC0#
External Topology	4	1,2,3,4	OC1#

NOTE: All USB ports routed out of the package must have over current protection. It is the system BIOS responsibility to ensure all used ports have OC protection.

Routing Illustration for SVID0_ALERT_N



NOTE: If less than 2 VR is used, remove the first device from the topology.Example:If 1 VR is used, remove from W2 to VR1 from the topology (as illustrated by dotted line).

Figure 3-3. USB2 and USB3 Port Mapping

Notes:
There are 8x USB Ports supported on Apollo Lake. USB Ports [5:0] can be used as USB2 and USB3 and are mutually exclusive. USB Port 6 and Port 7 can only be used as USB2.

Apollo Lake		2016 Ironhide
SATA P0		HDD/SSD
SATA P1	USB3 Port5	
PCIe Port 0		
PCIe Port 1		
PCIe Port 2		
PCIe Port 3	USB3 Port4	WIFI
PCIe Port 4	USB3 Port3	
PCIe Port 5	USB3 Port2	
USB3	USB3 Port1	
USB3	USB3 Port0 (OTG)	USB 3 I/O
USB2	USB2 Port0	USB 3 I/O
USB2	USB2 Port1	
USB2	USB2 Port2	USB 2 I/O
USB2	USB2 Port3	USB 2 I/O
USB2	USB2 Port4	BT
USB2	USB2 Port5	TS
USB2	USB2 Port6	CCD
USB2	USB2 Port7	CR
USB3	USB SSIC	
eMMC	eMMC	eMMC
SDIO	SDIO	

EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 17 of 105

SSID = PCH

N/A	PMC_SPI_FS1	1.8V	20K PU	LSMV	CMOS	PMC_SPI_FS1/ Out	Func2: HV_DDI2_HPD/Input

SUSPWRDNACK[1]	CMOS	O	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.

Table 2-30. Apollo Lake PM Interface Signals (Sheet 1 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_BATLOW_N	I/O	V1P8/V3P3	GPIO	**Battery Low:** This signal indicates that there is insufficient power to boot the system. Assertion will prevent wake from S3–S5 state. This signal can also be enabled to cause an SMI# when asserted.
PMU_PLTRST_N	I/O	V1P8/V3P3	GPIO	**Platform Reset:** This signal is used to reset devices on the platform (such as SIO, LAN, processor, and so forth.). This signal is asserted during power-up and when S/W initates a hard reset sequence through the Reset Control register (I/O port CF9h). The SoC drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h)
PMU_PWRBTN_N	I/O	V1P8/V3P3	GPIO	**Power Button:** Power button input signal. Used to wake the SoC from power button press. The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3–S4 states. This signal has an internal 16 ms de-bounce on the input.
PMU_RSTBTN_N	I/O	V1P8/V3P3	GPIO	**Reset Button:** Reset button input signal.
PMU_SLP_S0_N	I/O	V1P8/V3P3	GPIO	**S0 Sleep Control:** Controls power delivery subsystem. Asserted low in S0ix and G3 state.
PMU_SLP_S3_N	I/O	V1P8/V3P3	GPIO	**S3 Sleep Control:** Controls power delivery subsystem. Asserted low in S3 and lower
PMU_SLP_S4_N	I/O	V1P8/V3P3	GPIO	**S4 Sleep Control:** Controls power delivery subsystem. Asserted low in S4 and lower

Table 2-30. Apollo Lake PM Interface Signals (Sheet 2 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_SUSCLK	I/O	V1P8/V3P3	GPIO	**Suspend Clock:** Primary RTC clock output.
SUS_STAT_N		V1P8/V3P3	GPIO	**Suspend Status:** Asserted to indicate that the system will be entering a Sx state.
SUSPWRDNACK		V1P8/V3P3	GPIO	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.
SOC_PWROK	I	V1P8/V3P3	RTC	**SoC Power OK:** When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for at least 5 ms. This signal can be driven asynchronously. Then this signal is negated, the SOC asserts PLTRST#.

Note: The I/O voltage selection is done by using Hardware Strap GPIO_88

Vth(max)=1.1V

APS debug port

Do Not Stuff APS1801 PM_SLP_S3#
Do Not Stuff APS1802 PM_SLP_S4#
Do Not Stuff APS1803 RTC_RST#
Do Not Stuff APS1804 KBC_PWRBTN# 24,64,89
Do Not Stuff APS1806 PM_SLP_S0#

EMMC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size: Custom | Document Number: Ironhide APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 18 of 106

SSID = PCH

SPI ROM
24,25 SPI_SI_ROM
24,25 SPI_SO_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24,25 SPI_CS_CPU_N0
24,25,90 SPI_CLK_ROM

OTHER
90 HDA_RST#_CPU
24,68 INT_SERIRQ
24,68 LPC_FRAME#_CPU
24 PM_CLKRUN#_EC
24,90 LPC_CLK_KBC
68,90 LPC_CLK_DBG
24,68 LPC_AD_CPU_P3
24,68 LPC_AD_CPU_P2
24,68 LPC_AD_CPU_P1
24,68 LPC_AD_CPU_P0
27 HDA_RST#_CODEC
24 ME_UNLOCK

STRAP
15 GPIO92_SMB_NRB
15 GPIO111_BBS
15 GPIO118_FLASH_OVR
15 GPIO120_BIOS_SWAP
15 GPIO110_LPC_LEVEL
15 GPIO88_PMU_LEVEL
15 GPIO78_SMB_LEVEL

24 GS_I2C5_SDA_KBC
24 GS_I2C5_SCL_KBC
65 TP_I2C4_SDA
65 TP_I2C4_SCL
55 TS_I2C3_SDA
55 TS_I2C3_SCL

15 GP_SSP2_TXD

CPU1K
APL_SOC
11 OF 23
APOLLO-LAKE-GP-U

M52 AVS_DMIC_DATA_2
M54 AVS_DMIC_DATA_1
P52 AVS_DMIC_CLK_B1
M55 AVS_DMIC_CLK_AB2
P54 AVS_DMIC_CLK_A1
M61 AVS_I2S3_WS_SYNC
GPIO92_SMB_NRB L63 AVS_I2S3_SDO
L62 AVS_I2S3_SDI
M62 AVS_I2S3_BCLK
M57 AVS_I2S2_WS_SYNC
GPIO88_PMU_LEVEL M58 AVS_I2S2_SDO
K59 AVS_I2S2_SDI
HDA_RST#_CODEC R1901 33R2J-2-GP HDA_RST#_CPU K58 AVS_I2S2_MCLK/AVS_HDA_RST#
C1903 Do Not Stuff DY
H59 AVS_I2S2_BCLK
J62 AVS_I2S1_WS_SYNC
GPIO78_SMB_LEVEL K62 AVS_I2S1_SDO
K61 AVS_I2S1_SDI
G62 AVS_I2S1_MCLK
H63 AVS_I2S1_BCLK

Strap GPIO_82
Strap pin
Strap pin
Strap pin
1.8V

3.3V /1.8V
1.8V

LPC_SERIRQ AB62 INT_SERIRQ
LPC_FRAME# V61 LPC_FRAME#_CPU
LPC_CLKRUN# V62 PM_CLKRUN#_EC
LPC_CLKOUT1 AA62
LPC_CLKOUT0 AB61 LPC_CLK_CPU_P0
LPC_AD3 W63 LPC_AD_CPU_P3
LPC_AD2 W62 LPC_AD_CPU_P2
LPC_AD1 Y62 LPC_AD_CPU_P1
LPC_AD0 Y61 LPC_AD_CPU_P0

OSCOUT P29 XTL_19D2M_X1_CPU
OSCIN R27 XTL_19D2M_X2_CPU
OSC_CLK_OUT_4 AF62
OSC_CLK_OUT_3 AF60
OSC_CLK_OUT_2 AG63
OSC_CLK_OUT_1 AF61
OSC_CLK_OUT_0 AG62

R1905 33R2J-2-GP LPC_CLK_KBC
R1904 Do Not Stuff LPC_CLK_DBG
Debug

C1901 SC3D9P50V2CN-1GP
X1901 XTAL-48D2MHZ-21-GP SPEC CL=7pF,10PPM
082.30001.0061
2nd = 82.30071.131
R1912 200K2R2F-L-GP
C1902 SC3D9P50V2CN-1GP

R put near ROM side

CPU1M
APL_SOC
13 OF 23
APOLLO-LAKE-GP-U

SPI_SI_ROM A58 FST_SPI_MOSI_IO0
SPI_SO_ROM B58 FST_SPI_MISO_IO1
SPI_WP_ROM B60 FST_SPI_IO2
SPI_HOLD_ROM B61 FST_SPI_IO3
C57 FST_SPI_CS1#
SPI_CS_CPU_N0 B57 FST_SPI_CS0#
SPI_CLK_ROM C56 FST_SPI_CLK
GP_SSP2_TXD E62 SIO_SPI_2_TXD
C62 SIO_SPI_2_RXD
D59 SIO_SPI_2_FS2
GPIO120_BIOS_SWAP E56 SIO_SPI_2_FS1
D61 SIO_SPI_2_FS0
GPIO118_FLASH_OVR F62 SIO_SPI_2_CLK
ME_UNLOCK 2 R1913 1 Do Not Stuff
H58 SIO_SPI_1_TXD
H57 SIO_SPI_1_RXD
F61 SIO_SPI_1_FS1
K55 SIO_SPI_1_FS0
GPIO111_BBS F53 SIO_SPI_1_CLK
GPIO110_LPC_LEVEL J52 SIO_SPI_0_TXD
H54 SIO_SPI_0_RXD
H52 SIO_SPI_0_FS1
F52 SIO_SPI_0_FS0
F54 SIO_SPI_0_CLK

Strap pin
Strap GPIO_121
Strap pin
Strap pin
Strap GPIO_117
Strap GPIO_116
Strap GPIO_113
Strap GPIO_112
Strap pin
Strap pin
Strap GPIO_106
Strap GPIO_105
Strap GPIO_104

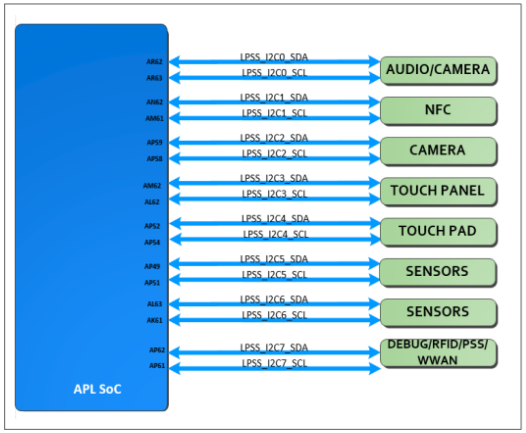
1.8V
1.8V

LPSS_I2C7_SDA/ISH_I2C2_SDA AP62
LPSS_I2C7_SCL/ISH_I2C2_SCL AP61
LPSS_I2C6_SDA/ISH_I2C1_SDA AL63
LPSS_I2C6_SCL/ISH_I2C1_SCL AK61
LPSS_I2C5_SDA/ISH_I2C0_SDA AP49 GS_I2C5_SDA
LPSS_I2C5_SCL/ISH_I2C0_SCL AP51 GS_I2C5_SCL
LPSS_I2C4_SDA AP52 TP_I2C4_SDA
LPSS_I2C4_SCL AP54 TP_I2C4_SCL
LPSS_I2C3_SDA AM62 TS_I2C3_SDA
LPSS_I2C3_SCL AL62 TS_I2C3_SCL
LPSS_I2C2_SDA AP59
LPSS_I2C2_SCL AP58
LPSS_I2C1_SDA AN62
LPSS_I2C1_SCL AM61
LPSS_I2C0_SDA AR62
LPSS_I2C0_SCL AR63

Rotate G_Sensor
Touch Pad
Touch Panel

3D3V_S5 RN1901 SRN2K2J-1-GP GSENSOR_1
Vth(max)=1.1V GSENSOR_1
RN1902 SRN2K2J-1-GP GSENSOR_1 1D8V_S5
Q1901 PJT138KA-GP 075.00138.0A7C
GS_I2C5_SDA_KBC GS_I2C5_SDA
GS_I2C5_SCL GS_I2C5_SCL_KBC
1D8V_S5

Figure 203. I²C Interface Topology



To configure the I²C ports, follow the pin muxing options listed out in the Apollo Lake SoC – External Design Specification (EDS) Volume 1 of 4 [CDI#: 557555].

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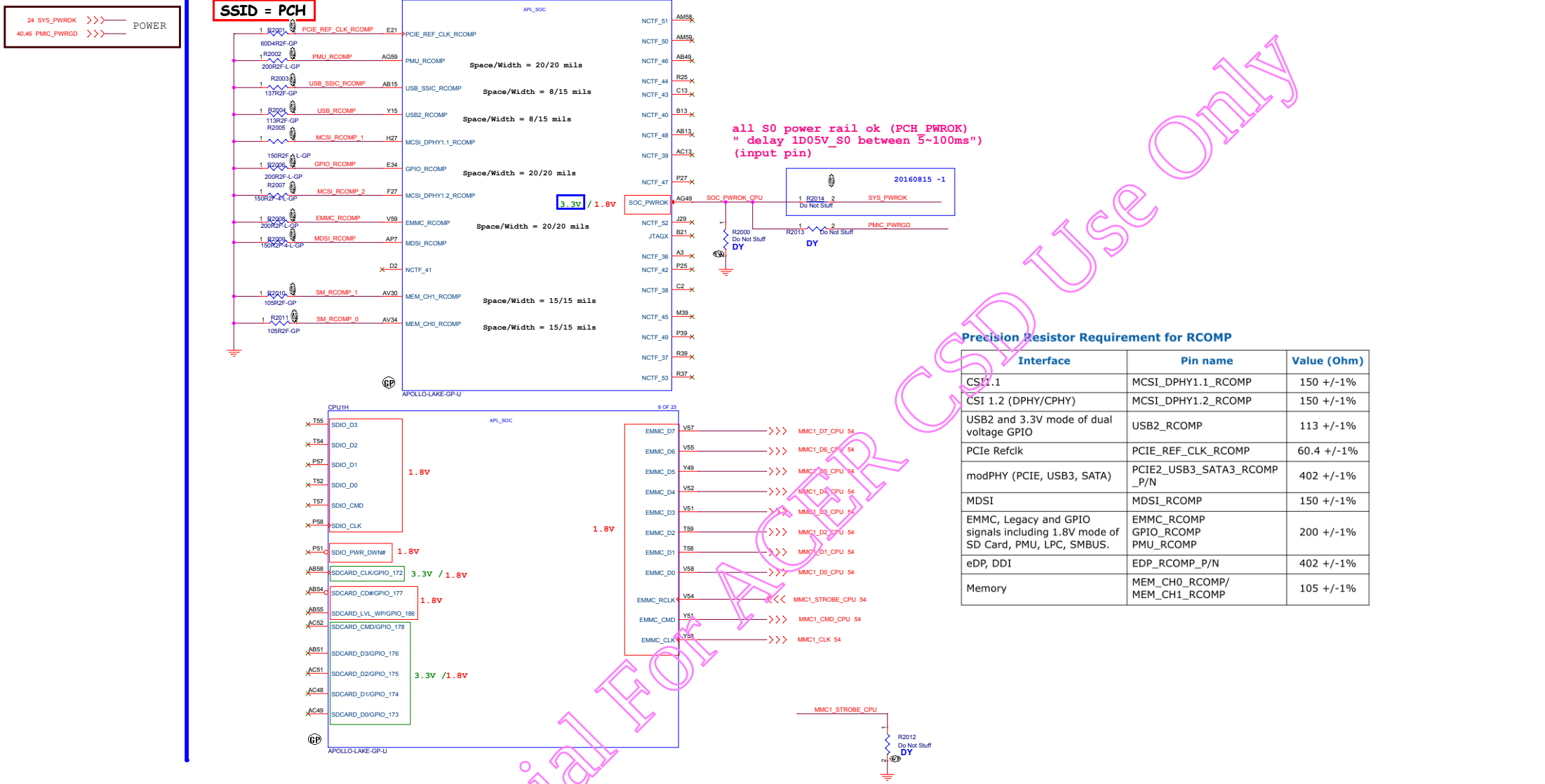
Title: CPU (SATA/PCIE/IHDA)
Size: Custom | Document Number: Ironhide_APL | Rev: -1M
Date: Wednesday, September 21, 2016 | Sheet 19 of 106



Precision Resistor Requirement for RCOMP

Interface	Pin name	Value (Ohm)
CSI1.1	MCSI_DPHY1.1_RCOMP	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSI_DPHY1.2_RCOMP	150 +/-1%
USB2 and 3.3V mode of dual voltage GPIO	USB2_RCOMP	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	60.4 +/-1%
modPHY (PCIE, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP _P/N	402 +/-1%
MDSI	MDSI_RCOMP	150 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode of SD Card, PMU, LPC, SMBUS.	EMMC_RCOMP GPIO_RCOMP PMU_RCOMP	200 +/-1%
eDP, DDI	EDP_RCOMP_P/N	402 +/-1%
Memory	MEM_CH0_RCOMP/ MEM_CH1_RCOMP	105 +/-1%

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Title: (Reserved)

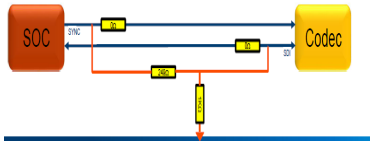
Size	Document Number	Rev
A2	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 20 of 106

SSID = CPU

AUDIO
27 HDA_SPKR
27 HDA_SDIN0_CODEC
27,90 HDA_SDOUT_CODEC
27,90 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27,90 HDA_BITCLK_CODEC

46 PMIC_IRQ#
15 GPIO36_VCCIO_LEVEL
65 TP_IN#
68 LPSS_UART2_TXD
68 LPSS_UART2_RXD
69 GSR_HDD_INT1
24 EC_SCI#
24 SH_INT#
55 TOUCH_DET#
55 TOUCH_RST#_CPU
55 TOUCH_INT#_CPU
25 RTC_DET#



CPU1O — APL_SOC — 15 OF 23 — APOLLO-LAKE-GP-U

HDA_SPKR — AK57 ISH_GPIO_9/SPKR
AM52 ISH_GPIO_8/MEMHOT#
AM55 ISH_GPIO_7/AVS_I2S5_SDO/LPSS_UART2_CTS#
AM57 ISH_GPIO_6/AVS_I2S5_SDI/LPSS_UART2_RTS#
LPSS_UART2_TXD — AM49 ISH_GPIO_5/AVS_I2S5_WS_SYNC/LPSS_UART2_TXD
LPSS_UART2_RXD — AM51 ISH_GPIO_4/AVS_I2S5_BCLK/LPSS_UART2_RXD
AM54 ISH_GPIO_3/AVS_I2S6_SDO/AVS_HDA_SDO
AK51 ISH_GPIO_2/AVS_I2S6_SDI/AVS_HDA_SDI
AK58 ISH_GPIO_1/AVS_I2S6_WS_SYNC/AVS_HDA_WS_SYNC
AM48 ISH_GPIO_0/AVS_I2S6_BCLK/AVS_HDA_BCLK
1.8V

F34 GPIO_33/ISH_GPIO_15/SUS_CLK3
F35 GPIO_32/ISH_GPIO_14/SUS_CLK2
H34 GPIO_31/ISH_GPIO_13/SUS_CLK1
C37 GPIO_30/ISH_GPIO_12
H35 GPIO_29/ISH_GPIO_11
B37 GPIO_28/ISH_GPIO_10
C29 GPIO_27
C31 GPIO_26/SATA_LED#
C27 GPIO_25/SATA_DEVSLP1
1.8V

J39 GPIO_18 — TP_IN#
C25 GPIO_24/SATA_DEVSLP0
B25 GPIO_23/SATA_GP1
A26 GPIO_22/SATA_GP0
C26 GPIO_21
B27 GPIO_20
C33 GPIO_19 — SH_INT#
A30 GPIO_9
C35 GPIO_7 — TOUCH_INT#_CPU
C36 GPIO_16 — GSR_HDD_INT1
F39 GPIO_15 — TOUCH_DET_CPU
C38 GPIO_14 — TOUCH_RST#_CPU
C30 GPIO_13
E39 GPIO_12 — SOC_WAKE_SCI#
C34 GPIO_11 — EC_SCI#
L39 GPIO_10
A38 GPIO_0
B29 GPIO_8
H39 GPIO_7
B31 GPIO_6
A34 GPIO_5
B35 GPIO_4
B39 GPIO_3
C39 GPIO_2
B33 GPIO_1
1.8V

HDA_SDIN0_CPU
HDA_SDIN0_CODEC — R2103 — ES-CPU — Do Not Stuff
R2106 Do Not Stuff — ES-CPU
Doc#560733-HD audio SDI pin issue
HDA_SYNC_CODEC — HDA_SYNC_CPU
HDA_BITCLK_CODEC — HDA_BITCLK_CPU
HDA_SDOUT_CODEC — HDA_SDOUT_CPU
RN2102 — SRN33J-L-GP
1D8V_S5
R2101 Do Not Stuff DY
PMIC_IRQ# — R2102 Do Not Stuff — PMIC_IRQ#_CPU

20150804 -1
1D8V_S5 — R2104 10KR2F-L1-GP — TP_IN#
1D8V_S5 — R2108 10KR2F-L1-GP — SH_INT#
3D3V_S0 — R2107 Do Not Stuff DY
1D8V_S0 — R2105 10KR2F-L1-GP TS
Q2102 DY — TOUCH_DET# — TOUCH_DET_CPU — Do Not Stuff
Do Not Stuff
2nd = 084.27002.0L31
3rd = 084.06587.0031

1D8V_S5
EC_SCI# — SOC_WAKE_SCI# — RN2101 — SRN10KJ-L-GP

CPU1O — APL_SOC — 17 OF 23 — APOLLO-LAKE-GP-U

M16 NCTF_59
L16 NCTF_60
F16 NCTF_63
E16 NCTF_54
J16 NCTF_66
H16 NCTF_58
H12 NCTF_68
F12 NCTF_56
M12 NCTF_65
M10 NCTF_62
F14 NCTF_57
H14 NCTF_55

L30 GPIO_219
M30 GPIO_218
M29 GPIO_217
P30 GPIO_216
AP57 NCTF_67
E41 PWM3
F41 PWM2 — GPIO36_VCCIO_LEVEL
C41 PWM1
B41 PWM0
C63 NCTF_64
E63 NCTF_61
1.8V

Strap pin
Strap GPIO_35
Strap GPIO_34

20160715 -1
RTC_DET#
PSW_CLR# — G2101 Do Not Stuff
20160728 -1

20160728 -1
RTC_DET# — RN2103 — SRN10KJ-L-GP — 1D8V_S5
PSW_CLR#

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Title: CPU (POWER1)
Size: Custom | Document Number: Ironhide_APL | Rev: -1M
Date: Wednesday, September 21, 2016 | Sheet 21 of 106

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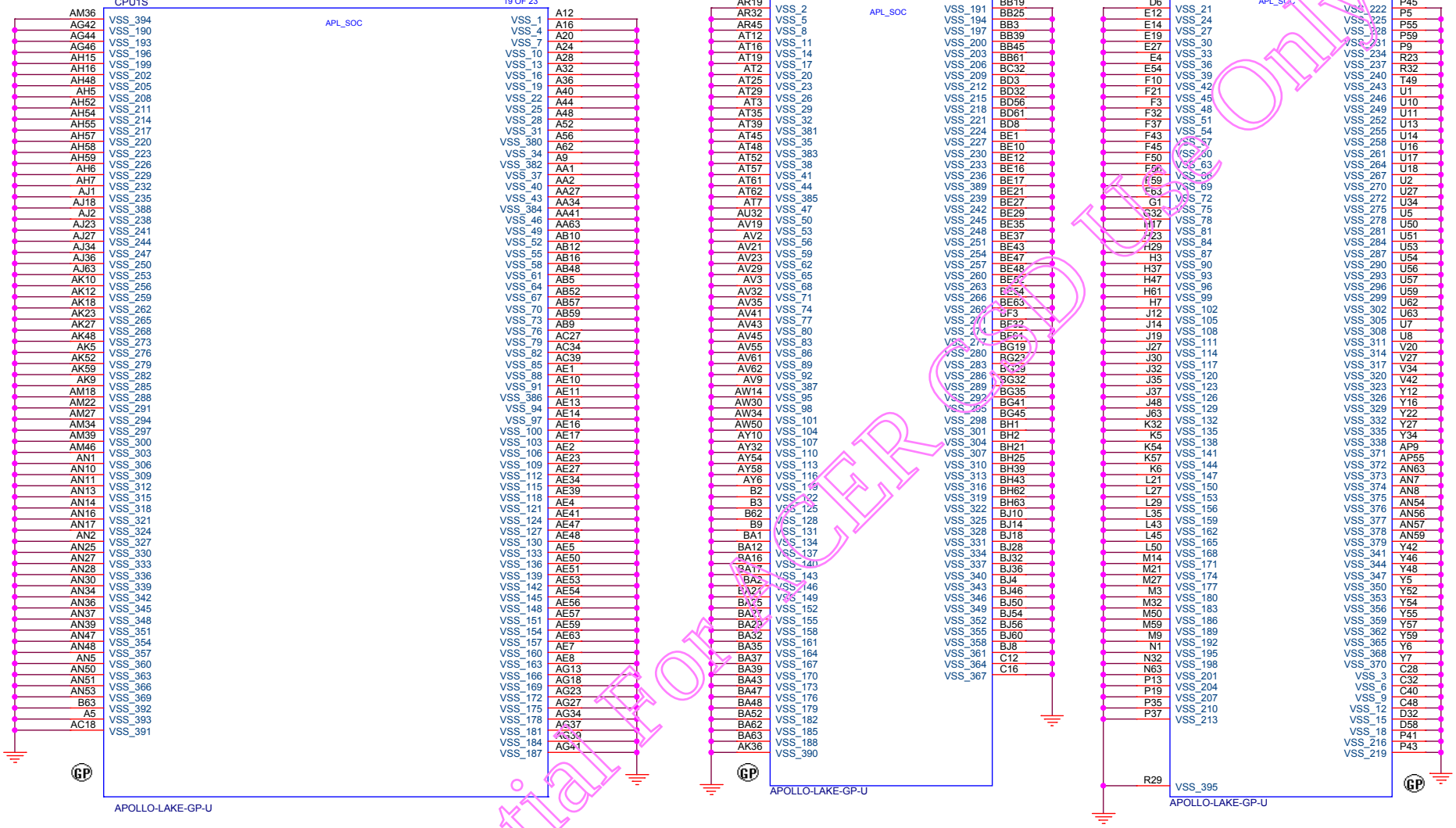
Title: *(Reserved)*

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 22 of 106

SSID = CPU



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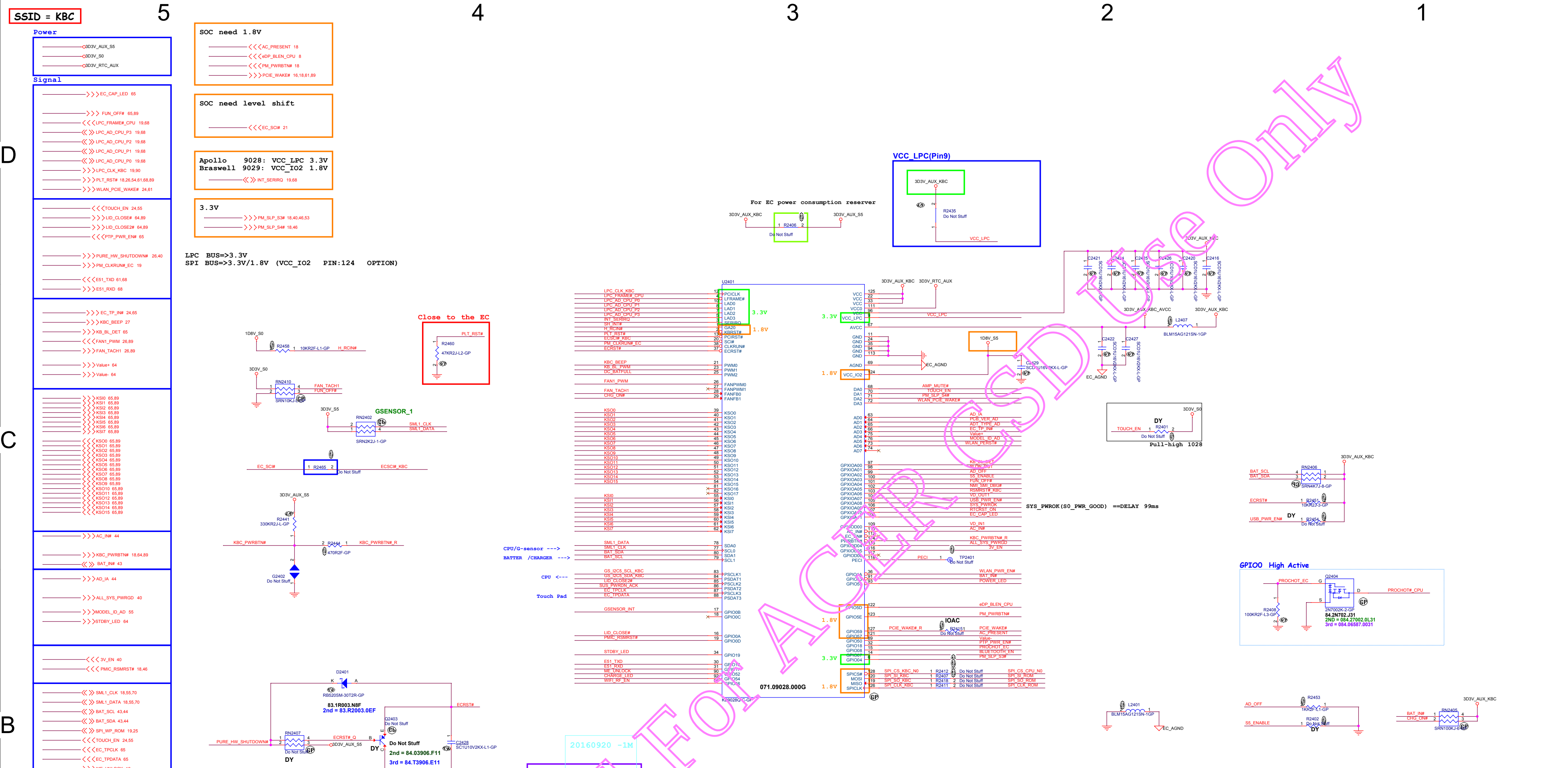
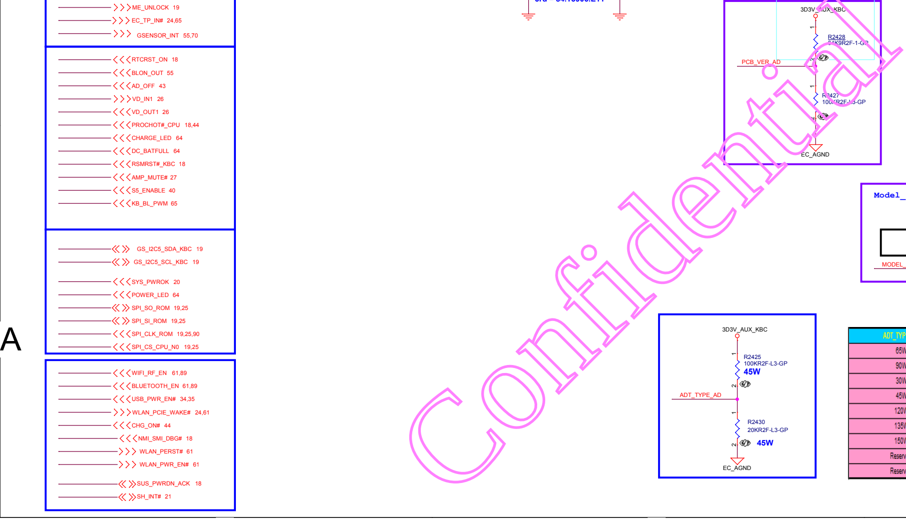
Taipei Hsien 221, Taiwan, R.O.C.

Title: VSS

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 23 of 106





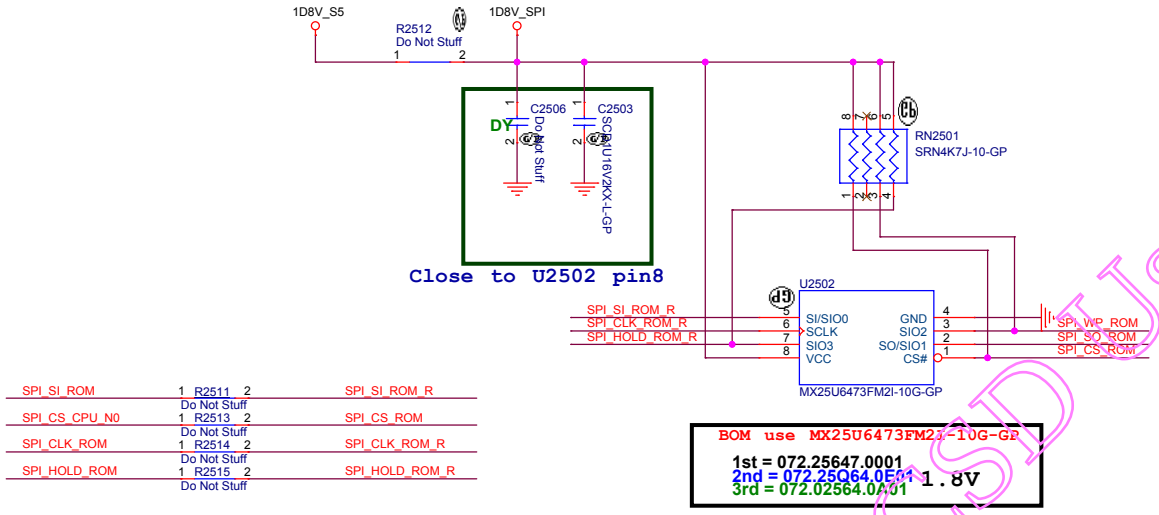
PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use -1M	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

Model_ID	High	Low
Ironhide_APL_11	V	
Drift_APL_13		V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

SSID = Flash.ROM

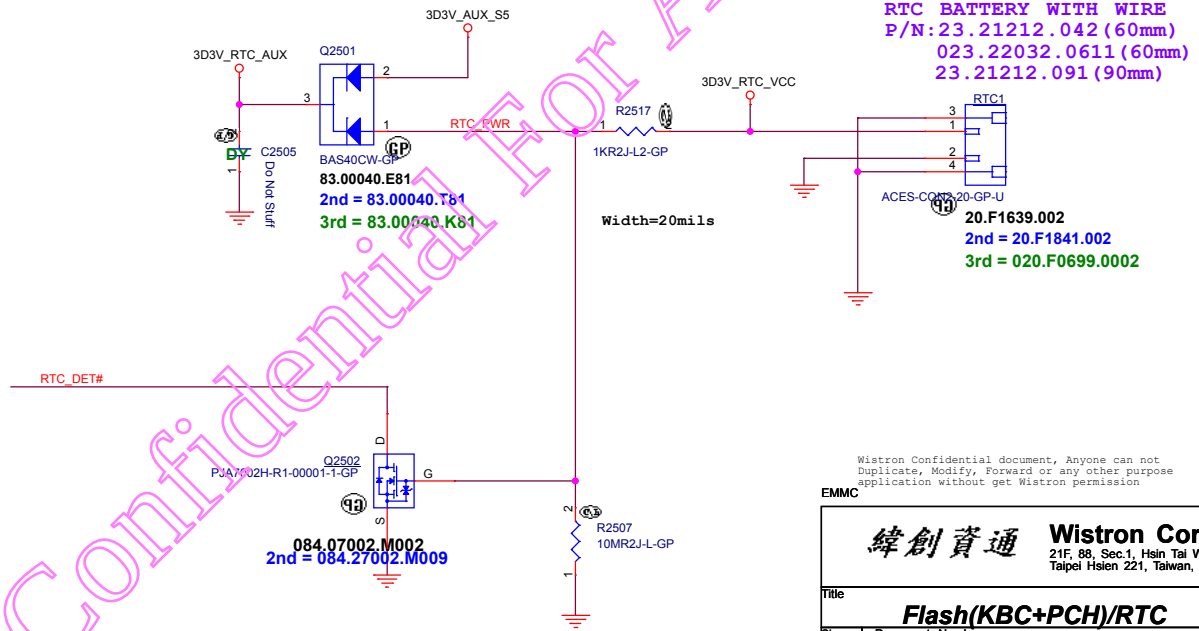
SPI FLASH ROM (8M byte) for PCH



19,24 SPI_SO_ROM
19,24 SPI_SI_ROM
19,24 SPI_CS_CPU_N0
19,24,90 SPI_CLK_ROM
19 SPI_HOLD_ROM
19 SPI_WP_ROM

SPI_SI_ROM	R2511 Do Not Stuff	SPI_SI_ROM_R
SPI_CS_CPU_N0	R2513 Do Not Stuff	SPI_CS_ROM
SPI_CLK_ROM	R2514 Do Not Stuff	SPI_CLK_ROM_R
SPI_HOLD_ROM	R2515 Do Not Stuff	SPI_HOLD_ROM_R

SSID = RBAT



21 RTC_DET#

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Title: Flash(KBC+PCH)/RTC

Size	Document Number	Rev
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SSID = Thermal

Layout 15 mil

24 VD_IN1
24,89 FAN1_PWM
24,89 FAN_TACH1
24,40 PURE_HW_SHUTDOWN#
24 VD_OUT1
40 IMVP_PWRGD
89 FAN_TACH1_C
18,46 PMIC_THERMTRIP#
18,24,54,61,68,89 PLT_RST#

3D3V_AUX_S5
R2611 16KR2F-GP
VD_IN1
RT2601 NTC-100K-11-GP-U
C2607 SCD1U16V2KX-L-GP
C2608 SC100P50V2JN-L-GP
T8

RT2601 close CPU and Vcore chock

5V_S0
D2601 RB551V30-GP
83.R5003.H8H
C2603 SC4D7U25V6KX-L2-GP
C2602 Do Not Stuff
FAN
DY

FAN
D2602 RB551V30-GP
83.R5003.H8H
FAN_TACH1
FAN1_PWM
FAN_TACH1_C
5V_S0
FAN1 ACES-CON4-29-GP
FAN
20.F1639.004
2nd = 20.F1804.004
3rd = 020.F0700.0004

3D3V_S0
R2606 2KR2F-L1-GP
Q2603 2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.06587.0031
THERM_SYS_SHDN#_R
R2610 Do Not Stuff
VD_OUT1
PURE_HW_SHUTDOWN#
R2608 Do Not Stuff
C2606 Do Not Stuff
DY
20160815 -1
R2603 Do Not Stuff
3D3V_S0
IMVP_PWRGD_G
R2609 Do Not Stuff
IMVP_PWRGD
DY

20160801 -1
PMIC_THERMTRIP#
PLT_RST#
R2602 Do Not Stuff
H_PWRGD_R
Q2604 Do Not Stuff
R2601 Do Not Stuff
C2609 Do Not Stuff
DY
Do Not Stuff
2nd = 084.02222.0011
PURE_HW_SHUTDOWN#

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Title: Thermal 7718/Fan Controllor P2793
Size: A3
Document Number: Ironhide_APL
Rev: -1M
Date: Wednesday, September 21, 2016
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SSID = AUDIO

29 AUD_HP1_JACK_L2
29 AUD_HP1_JACK_R2
24 AMP_MUTE#
29 AUD_SPK_L+
29 AUD_SPK_L-
29 AUD_SPK_R-
29 AUD_SPK_R+
55 DMIC_DATA_CON
55 DMIC_CLK_CON
21,90 HDA_SDOUT_CODEC
21,90 HDA_BITCLK_CODEC
21,90 HDA_SDIN0_CPU
21 HDA_SYNC_CODEC
19 HDA_RST#_CODEC
29 AUD_HP1_JD#
27,29,89 SELEEVE
27,29,89 RING2
24 KBC_BEEP
21 HDA_SPKR
21 HDA_SDIN0_CODEC

EC2701 1DY Do Not Stuff
EC2702 1DY Do Not Stuff
AUD_AGND

G2703 G2701 G2702 Do Not Stuff
AUD_AGND close to codec IC

placed nearby codec PIN12
C2725 SCD1U16V2KX-L-GP
AUDIO_PC_BEEP
KBC_BEEP_C
RN2704 SRN47K-2-GP-U
KBC_BEEP
HDA_SPKR
R2730 10KR2F-L1-GP

3D3V_S0
C2701 SC4D7U6D3V3KX-L-GP Close pin36
AUD_HP1_JACK_L2
AUD_HP1_JACK_R2
3V_MIC2V
AUD_AGND
C2704 SC2D2U10V3KX-L-GP
C2705 SC10U6D3V3MX-L-GP
C2702 SCD1U16V2KX-L-GP
R2711 100KR2F-L3-GP
5V_PVDD2
C2710 SCD1U16V2KX-L-GP
Layout Note: Place close to Pin 26
1D5V_S0
R2766 Do Not Stuff
1D5V_AVDD_S0
C2715 SC4D7U6D3V3KX-L-GP Close pin40
AUD_AGND
R2748 Do Not Stuff
3D3V_S0
C2714 SCD1U16V2KX-L-GP
C2703 SC10U6D3V3MX-L-GP
U2701
R2755 Do Not Stuff
5V_S0
AUD_AGND
RN2703 SRN4K7J-8-GP
LINE1_VREFO_L
LINE1_VREFO_R
3V_MIC2V
RN2702 SRN2K2J-5-GP
3D3V_S5
C2712 SC10U6D3V3MX-L-GP
1D5V_AVDD_S0
5V_PVDD
AUD_AGND
C2723 SC4D7U6D3V3KX-L-GP
AUD_HP1_JACK_R2
R2712 Do Not Stuff
C2713 SC10U6D3V3MX-L-GP
SELEEVE 27,29,89
RING2 27,29,89
AMP_MUTE#
R2754 Do Not Stuff
5V_PVDD
R2708 is need to connect.To prvent the beep sound
071.00255.0003
R2713 200KR2F-L3-GP
AUD_HP1_JD#
Layout Note: Place close to Pin 13
Layout Note: Width>40mil, to improve Headpohone Crosstalk noise Change it to sharp will be better. Add 2 vias (>0.5A) when trace layer change.
ALC255-CG-GP-U
3D3V_AUDIO_DVDD
C2717 SC10U6D3V3MX-L-GP
C2716 SCD1U16V2KX-L-GP
Close to Pin1
3D3V_S0
R2720 Do Not Stuff
3D3V_AUDIO_DVDD
DVDD_IO
R2714 Do Not Stuff
1D8V_S0
20160801 -1
C2720 SC10U6D3V3MX-L-GP
AUD_SENSE_A
R2722 100KR2F-L3-GP
3D3V_S0
ED2701 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.08212.007D
EMC solution
DMIC_DATA_CON
DMIC_CLK_CON
EL2701 MCB1005S601FBP-GP-U
DMIC_CLK_AUD
close to CODEC
AUDIO_PC_BEEP
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC
HDA_SDIN0_CPU
R2718 33R2J-L1-GP
HDA_SDIN0_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
AUD_HP1_JACK_L2
AUD_HP1_JACK_R2
ED2702 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.08212.007D
5V_S0
R2719 Do Not Stuff
5V_PVDD
C2709 SCD1U16V2KX-L-GP
C2708 SC10U6D3V3MX-L-GP
Close to Pin46
C2707 SCD1U16V2KX-L-GP
C2706 SC10U6D3V3MX-L-GP
Close to Pin41

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Title: Audio Codec ALC255
Size: A2 | Document Number: Ironhide_APL | Rev: -1M
Date: Wednesday, September 21, 2016 | Sheet 27 of 106

Blanking

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Title

Reserved

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 28 of 106

89 AUD_SPK1_L-_CON
89 AUD_SPK1_L+_CON
89 AUD_SPK1_R-_CON
89 AUD_SPK1_R+_CON

89 AUD_HP1_JD#_R
89 AUD_HP1_JACK_R1
89 AUD_HP1_JACK_L1
89 AUD_HP1_JD#_TYPE

27 AUD_SPK_L-
27 AUD_SPK_L+
27 AUD_SPK_R-
27 AUD_SPK_R+

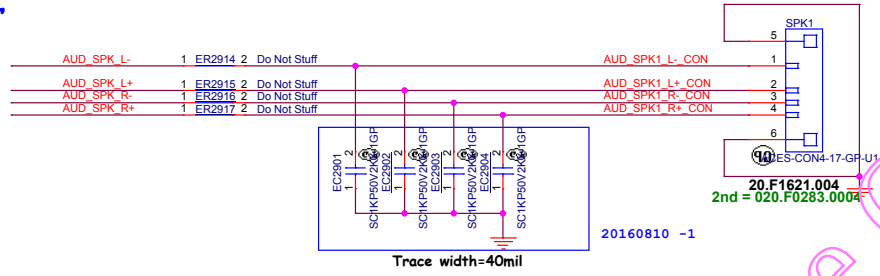
27 AUD_HP1_JD#

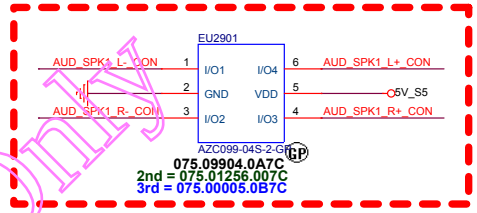
27,89 RING2
27 AUD_HP1_JACK_L2

27 AUD_HP1_JACK_R2
27,89 SELEEVE

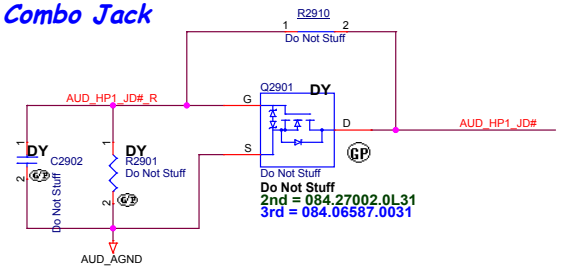
SSID = AUDIO

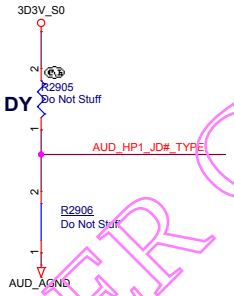
Speaker

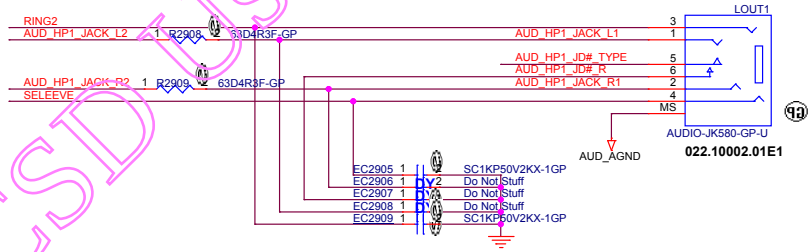




Combo Jack







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Title: **Speaker/HPMIC**

Size: Custom | Document Number: **Ironhide_APL** | Rev: **-1M**

Date: Wednesday, September 21, 2016 | Sheet 29 of 106

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Title: ***LAN(RTL8111)***

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A	Ironhide_APL	-1M

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Title

(LAN+VGA) CONNECTOR

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Title: *RTS5170(CARD READER)*

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 32 of 106

SSID = SDIO

SD//MS Card Reader

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Title: CARD Reader CONN

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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24,35 USB_PWR_EN#

17 USB2_USB20_N
17 USB2_USB20_P
17 USB3_USB20_N
17 USB3_USB20_P

89 USB2_CON_USB20_N
89 USB2_CON_USB20_P
89 USB3_CON_USB20_N
89 USB3_CON_USB20_P

Low Active 2A

5V_S5

U3401
IN
EN#
OUT
GND
OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

C3401
SC1U10V2KX-L1-GP

USB_PWR_EN#

5V_USB20

C3402
SC1U16V2KX-L-GP

C3403
SC100U6D3V6MX-GP

C3405
Do Not Stuff
DY

C3406
Do Not Stuff
DY

C3404
Do Not Stuff
DY

USB2
VBUS
D-
D+
GND
SHELL#5
SHELL#6
SHELL#7
SHELL#8
USB2.0
SKT-USB8-195-GP-U
022.10005.00Q1
2nd = 22.10254.721

USB2_CON_USB20_N
USB2_CON_USB20_P

EL3403
FILTER-4P-137-GP-U
68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

USB2_USB20_N
USB2_USB20_P

USB3
VBUS
D-
D+
GND
SHELL#5
SHELL#6
SHELL#7
SHELL#8
USB2.0
SKT-USB8-195-GP-U
022.10005.00Q1
2nd = 22.10254.721

USB3_CON_USB20_N
USB3_CON_USB20_P

EL3404
FILTER-4P-137-GP-U
68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

USB3_USB20_N
USB3_USB20_P

EU3402
I/O1
GND
I/O2
I/O4
VDD
I/O3
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 075.00005.0B7C

USB2_CON_USB20_P
USB3_CON_USB20_P
USB2_CON_USB20_N
USB3_CON_USB20_N
5V_S5

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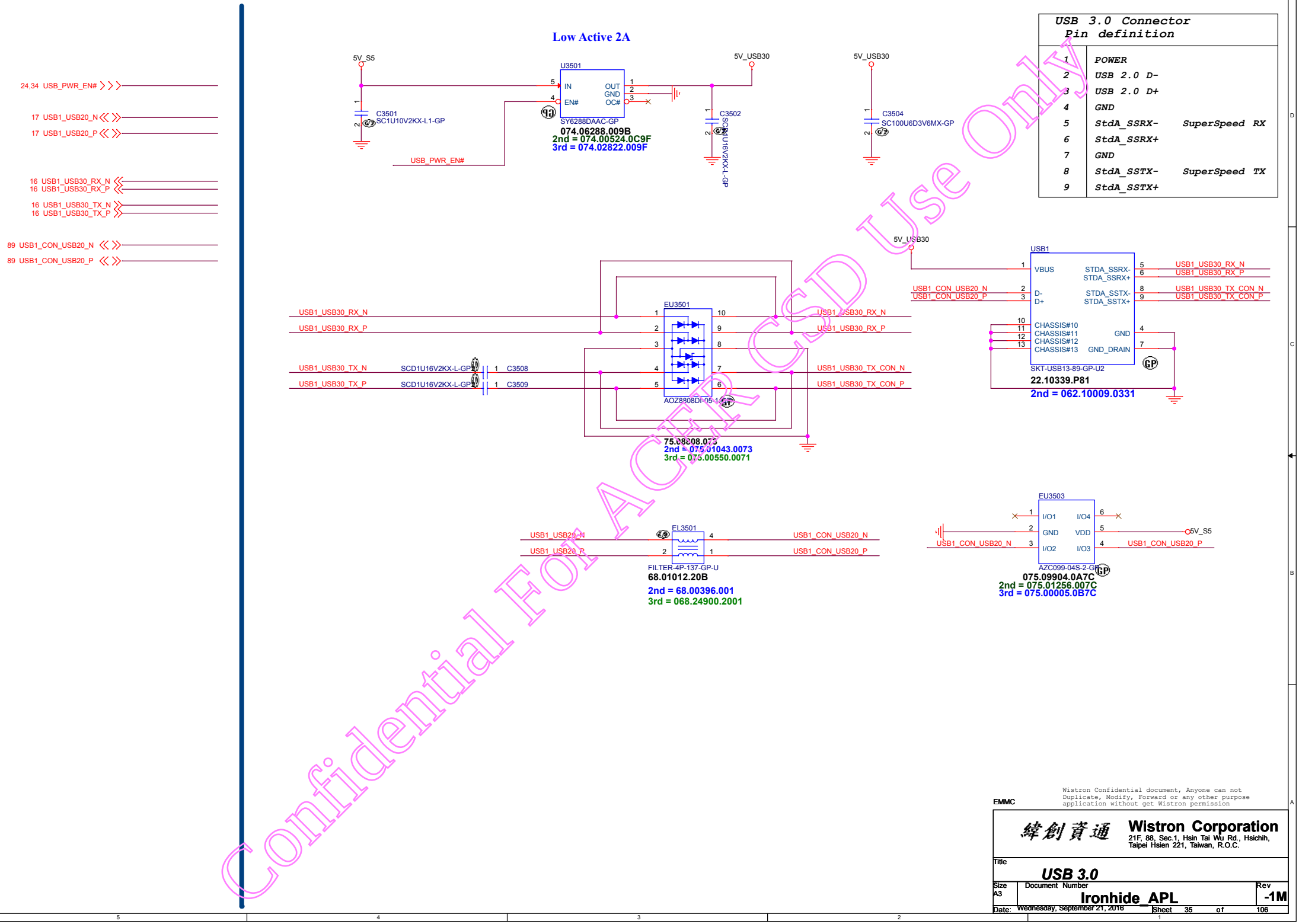
Title: USB2.0

Size: A3 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 34 of 106



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Title: USB 3.0

Size	Document Number	Rev
A3	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 35 of 106

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Title	***Reserved***	
Size: A	Document Number: **Ironhide_APL**	Rev: **-1M**
Date: Wednesday, September 21, 2016	Sheet 36 of 106	

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Title
ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A4	Ironhide_APL	-1M
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Title: USB HUB

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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Title

Reserved

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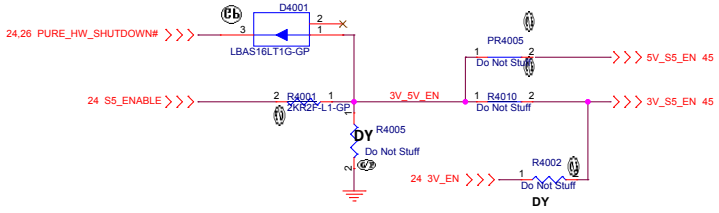
A4	Ironhide_APL	-1M

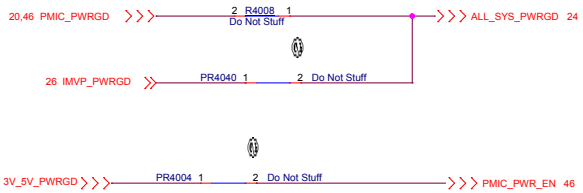
Date: Wednesday, September 21, 2016 Sheet 39 of 106

SSID = Reset.Suspend

Power Sequence

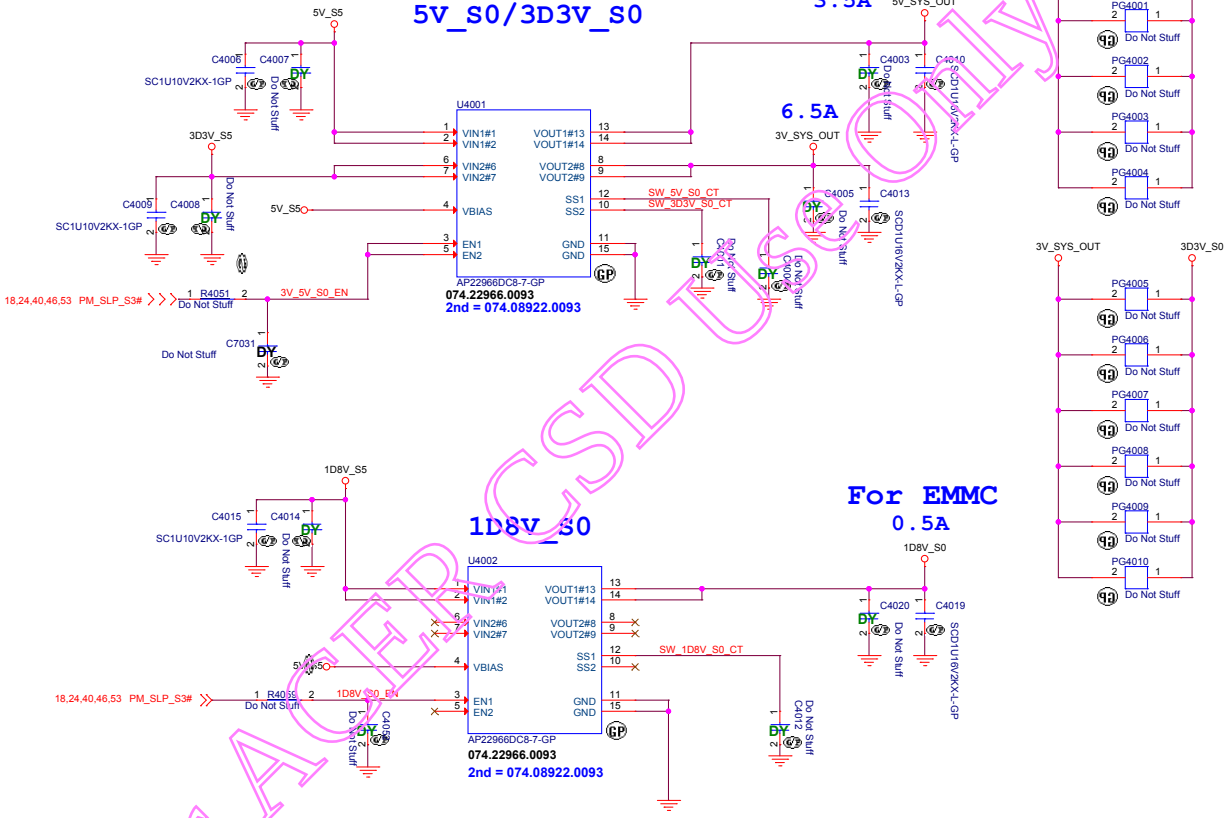


ALL_SYS_PWRGD To EC



RUN Power

5V_S0/3D3V_S0



1D8V_S0

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Title: Power Plane Enable & SEQUENCE

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Title: ***Reserved***

Size	Document Number	Rev
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Date: Wednesday, September 21, 2016 Sheet 41 of 106

ANNIE solution

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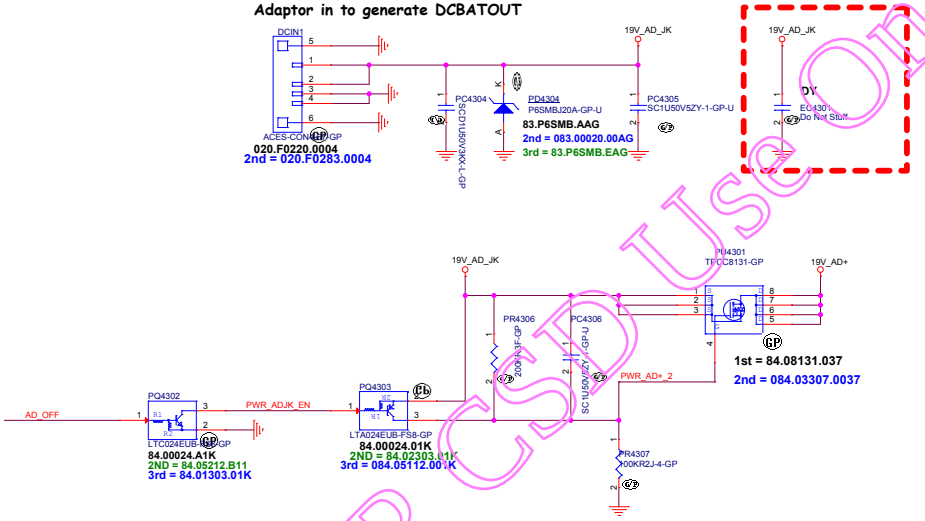
Title: Reserved

Size	Document Number	Rev
A4	Ironhide_APL	-1M

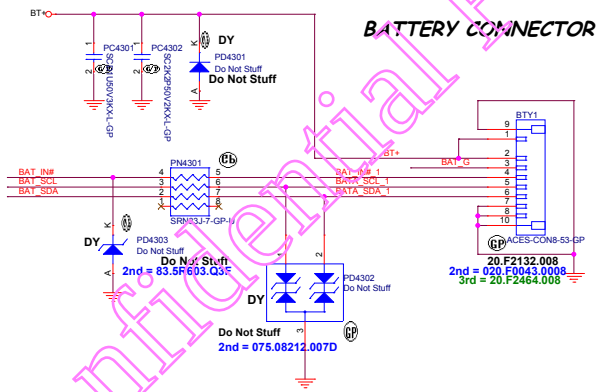
Date: Wednesday, September 21, 2016 Sheet 42 of 106

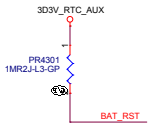
ANNIE solution

Adaptor in to generate DCBATOUT

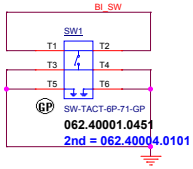


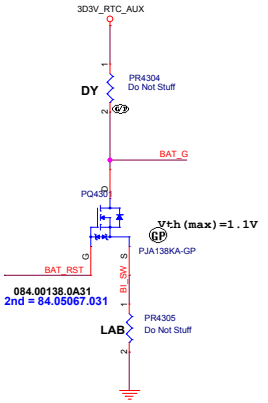
BATTERY CONNECTOR





Battery Insert





24 AD_OFF

24 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA

89 BAT_G

89 BAT_IN#_1
89 BATA_SCL_1
89 BATA_SDA_1

64 BAT_RST

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Title: BATT CONN

Size: A2 | Document Number: Ironhide_APL | Rev: -1M

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SSID = Charger

CHARGER ENABLE CONTROL

24,44 CHG_ON#

Others

24,43 BAT_SCL
24,43 BAT_SDA
24,44 AC_IN#
24,44 AD_IA
18,24,44 PROCHOT#_CPU

Id= -10A
Qg= -22nC
Rdson=14~22mohm

19V_AD+
PU4407 TPCC8131-GP
1st = 84.08131.037
2nd = 084.03307.0037
PR4403 100KR2J-1-GP
PR4404 10KR2F-2-GP
PR4405 49K9R2F-L-GP
AD+_G_2
DCIN_D
AD+
PQ4402 2N7002KDW-GP
AC_IN
84.2N702.A3F
2nd = 075.67002.007C

AD+_TO_SYS
19V_DCBATOUT
PR4402 D02R3721F-GP-U
PG4402 Do Not Stuff
PG4401 Do Not Stuff
PC4402 SCD1U50V3KX-L-GP
PC4403 SCD1U50V3KX-L-GP
PC4404 SCD1U50V3KX-L-GP
CHG_AGND
PR4414 20R5F-1GP
PR4407 20R5F-1GP
PWR_CHG_VCC
PC4408 SC1U50V5ZY-1-GP-U
PWR_CHG_ACP
PWR_CHG_ACN

PU4404 HPA02224RGRR-1-GP
VCC
ACDET
CMPOUT
CMPIN
SCL
SDA
ILIM
BM#
ACOK#
BTST
REG
HIDRV
PHASE
LODRV
SRP
SRN
IOUT
GND
74.02224.073

PWR_CHG_ACDET
AC_Protect
PWR_CHG_CMPIN
PWR_CHG_CLK
PWR_CHG_DATA
PWR_CHG_ILIM
PWR_CHG_BM#
PWR_CHG_IOUT
PWR_CHG_Boot
PWR_CHG_HG
PWR_CHG_PH
PWR_CHG_LG
PWR_CHG_SRP
PWR_CHG_SRN
PWR_CHG_REGN

PR4425 100KR2J-4-GP
PR4410 60K4R2F-GP
PR4416 3D3MR2J-GP
PR4411 Do Not Stuff
PR4415 Do Not Stuff
PR4412 49K9R2F-L-GP
PC4411 SCD01U50V2KX-L-GP
PR4413 100KR2F-L1-GP
R1
R2
BAT_SCL
BAT_SDA

PR4408 324KR2F-GP
PR4409 1D5R2F-GP
PD4401 RB520SM-30T2R-GP
PC4409 SC1U10V2KX-L1-GP
PC4410 SCD1U50V3KX-L-GP
PR4418 10R2F-L-GP
PR4420 7D5R2F-GP
PR4422 Do Not Stuff
PR4421 Do Not Stuff
PR4419 100KR2J-1-GP
PR4423 Do Not Stuff
PR4424 100KR2J-1-GP
PR4427 100KR2J-1-GP
PR4428 100KR2J-1-GP
PR4401 Do Not Stuff
PC4416 SCD1U50V3KX-L-GP
PC4417 SCD1U16V2KX-L-GP
PC4418 SCD1U25V2KX-L-GP
PWR_CHG_SRP_1
PWR_CHG_SRN_1
AD_IA 24,44
CHG_ON# 24,44
AC_IN#
3D3V_AUX_S5

PQ4401 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031
PQ4404 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.06587.0031

PU4403 AON7410-GP
84.07410.A37
2nd = 84.08067.A37
PU4409 AON7410-GP
84.07410.A37
2nd = 84.08067.A37
PC4405 SCD1U25V2KX-L-GP
PC4406 SC10U25V5KX-GP
PC4407 Do Not Stuff
DY

Charger Current=1.4~3.6A

PL4401 IND-4DYUH-173-GP-U
68.4R71C.10K
2nd = 68.4R71A.20H
PR4417 D01R3721F-GP-U
PG4403 Do Not Stuff
PG4404 Do Not Stuff
PC4412 SC10U25V5KX-GP
PC4413 Do Not Stuff
PC4421 SC10U25V5KX-GP
PC4422 Do Not Stuff
PC4414 SCD1U25V2KX-L-GP

PU4408 TPCC8133-GP
BT+
SC1KF50V2KX-L-1-GP
PC4419
PR4406 470KR2J-2-GP
FC4419 is close to PU4401 PIN#4
1st = 84.08131.037
2nd = 084.03307.0037
Id= -10A
Qg= -22nC
Rdson=14~22mohm

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect.ptest (85% x 120%)	AC_Protect Current	PR4404 Sense resistor	Current to Volta...	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	10 m?ohm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	10 m?ohm	0.96696	50.4	100
60W	AC + Battery	High	3.42	102%	3.4884	10 m?ohm	0.96796	34.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10 m?ohm	0.96696	50.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10 m?ohm	1.28724	113	100
154W	AC + Battery	High	7.1	102%	7.242	10 m?ohm	1.4484	180	100

AC_Protect
PQ4408 2N7002KDW-GP
84.2N702.A3F
2nd = 075.67002.007C
PR4446 Do Not Stuff
PR4442 Do Not Stuff
AC_Protect_R1
AC_Protect_R
18,24,44 PROCHOT#_CPU
PC4426 Do Not Stuff
DY

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Title: Charger HPA02224RGRR
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5V/3V ENABLE CONTROL

40,45 5V_S5_EN

40,45 3V_S5_EN

5V/3V POWER GOOD

40 3V_5V_PWRGD

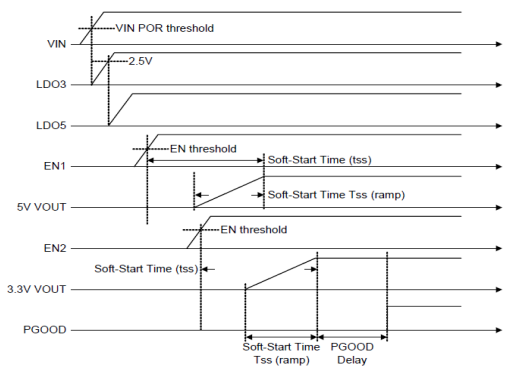

Figure 6. RT6575B Timing

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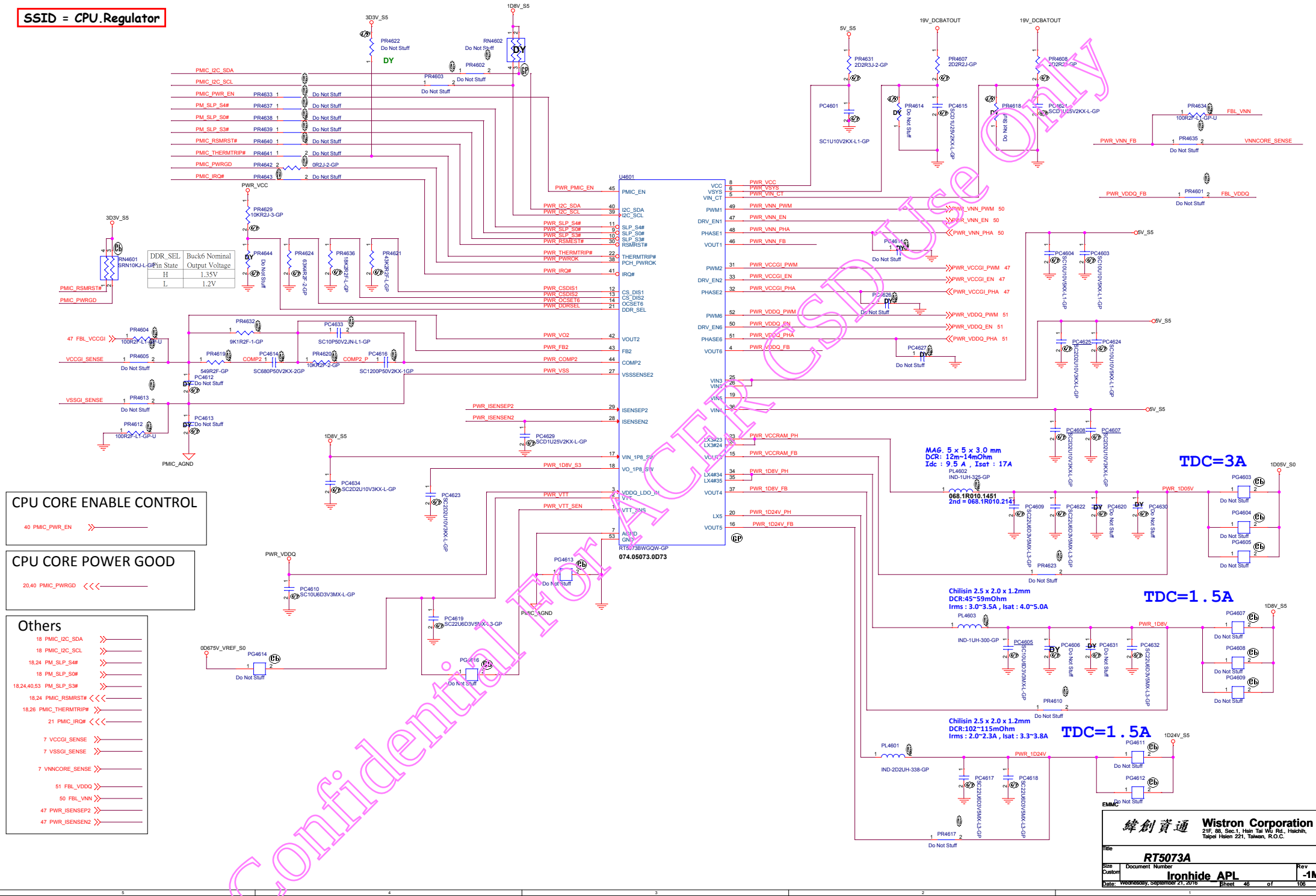
Title: RT6575D_5V/3D3V

Size: Custom | Document Number | Rev

Date: Wednesday, September 21, 2016 | Sheet 45 of 106

SSID = CPU.Regulator



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT5073A
Size: Custom	Document Number: Ironhide_APL
Rev	-1M
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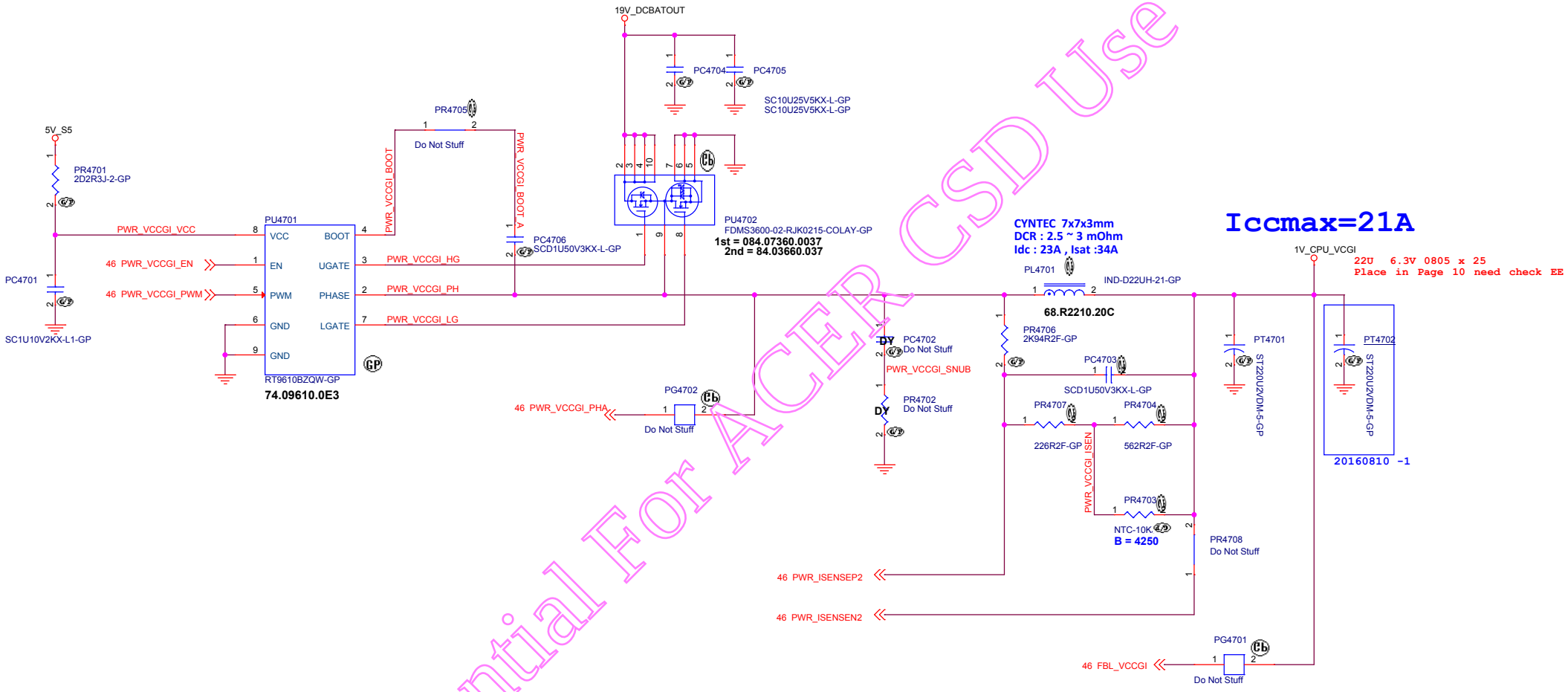

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Title: RT5073A_VCCGI

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Title: RT8171B_CPUCORE(2/3)

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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Title: Reserved

Size	Document Number	Rev
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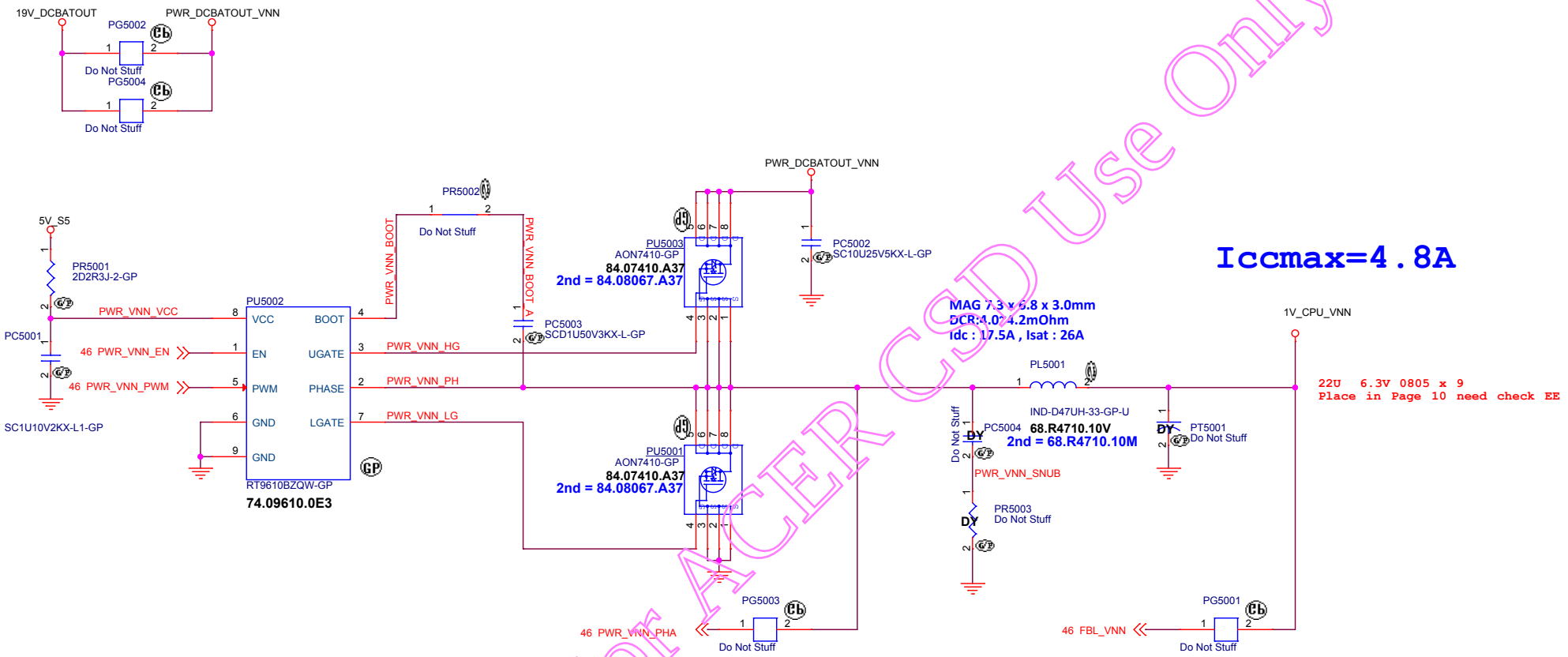

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Title: RT5073A_VNN

Size: B | Document Number: Ironhide_APL | Rev: -1M

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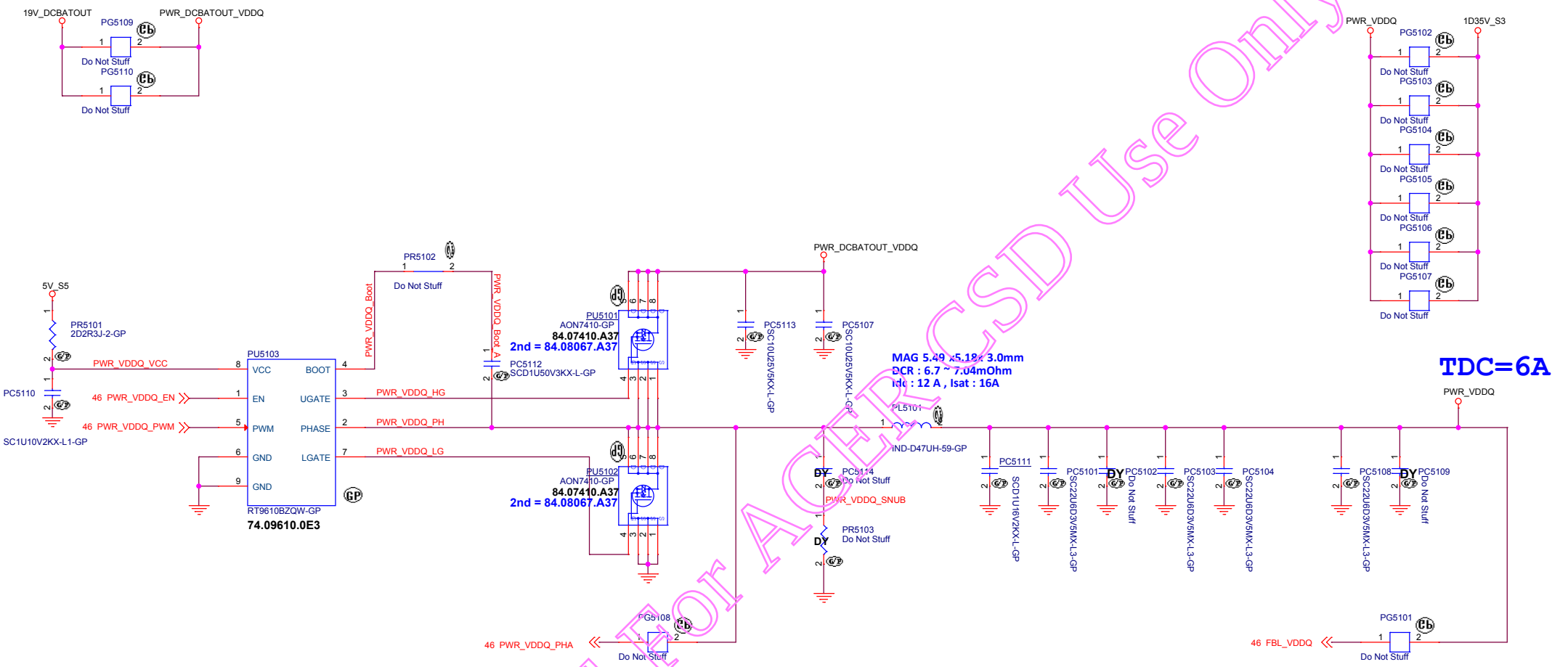

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Title: ***RT5073A_VDDQ***

Size	Document Number	Rev
A3	Ironhide_APL	-1M

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Title: *(Reserved)*

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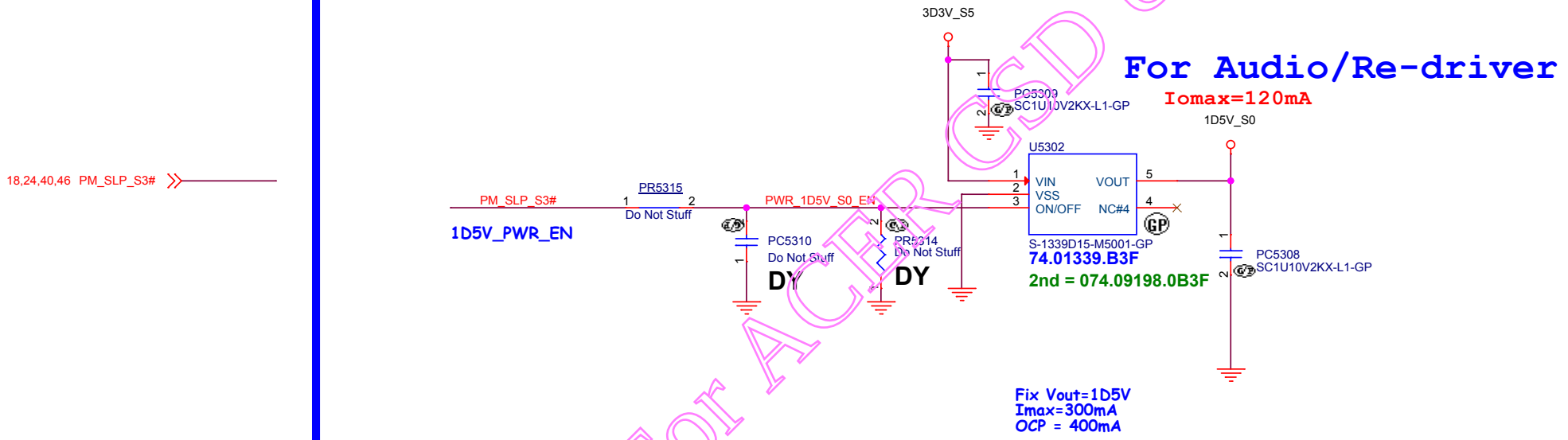
Date: Wednesday, September 21, 2016 Sheet 52 of 106

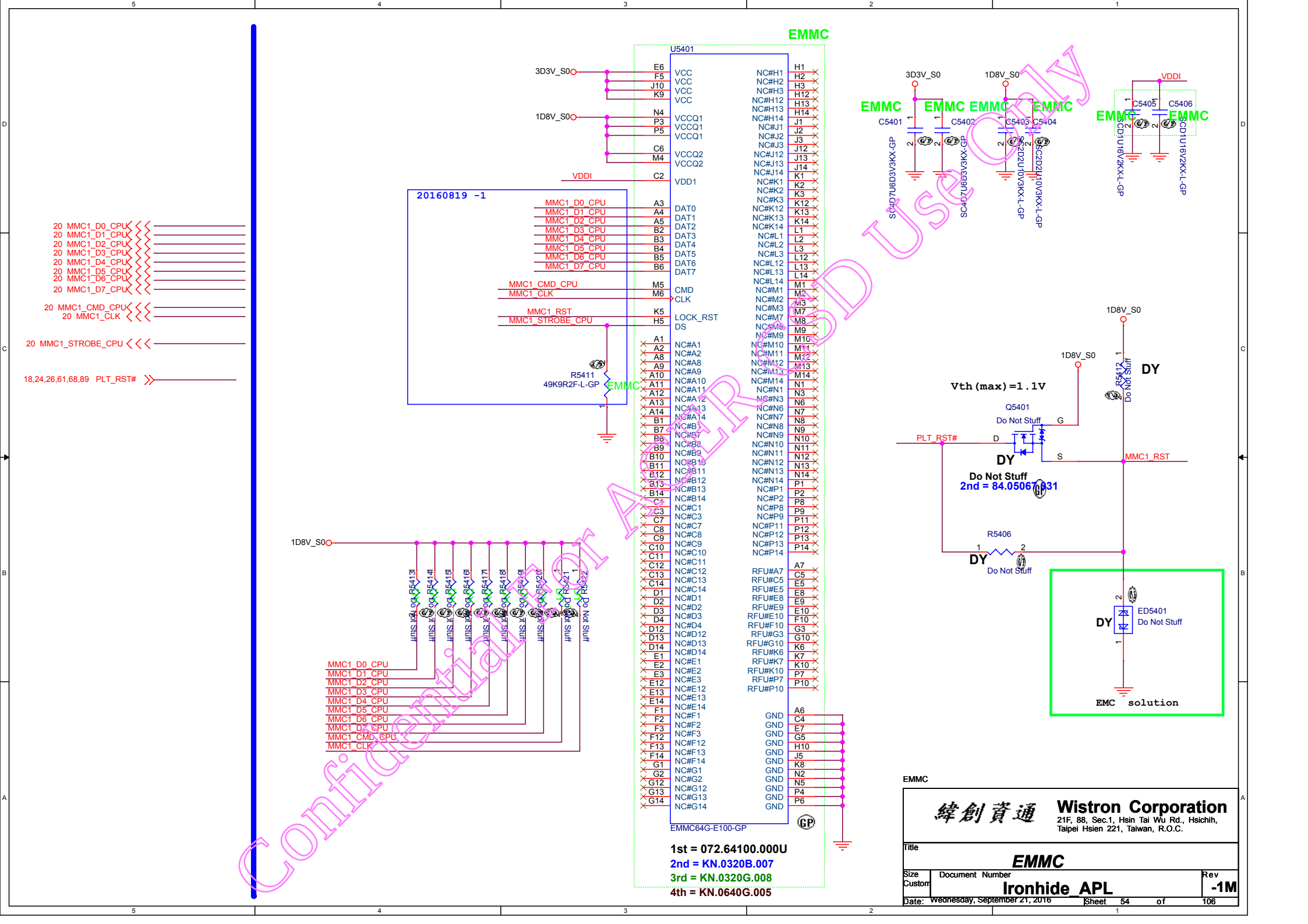
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

For HDMI re-driver and audio codec

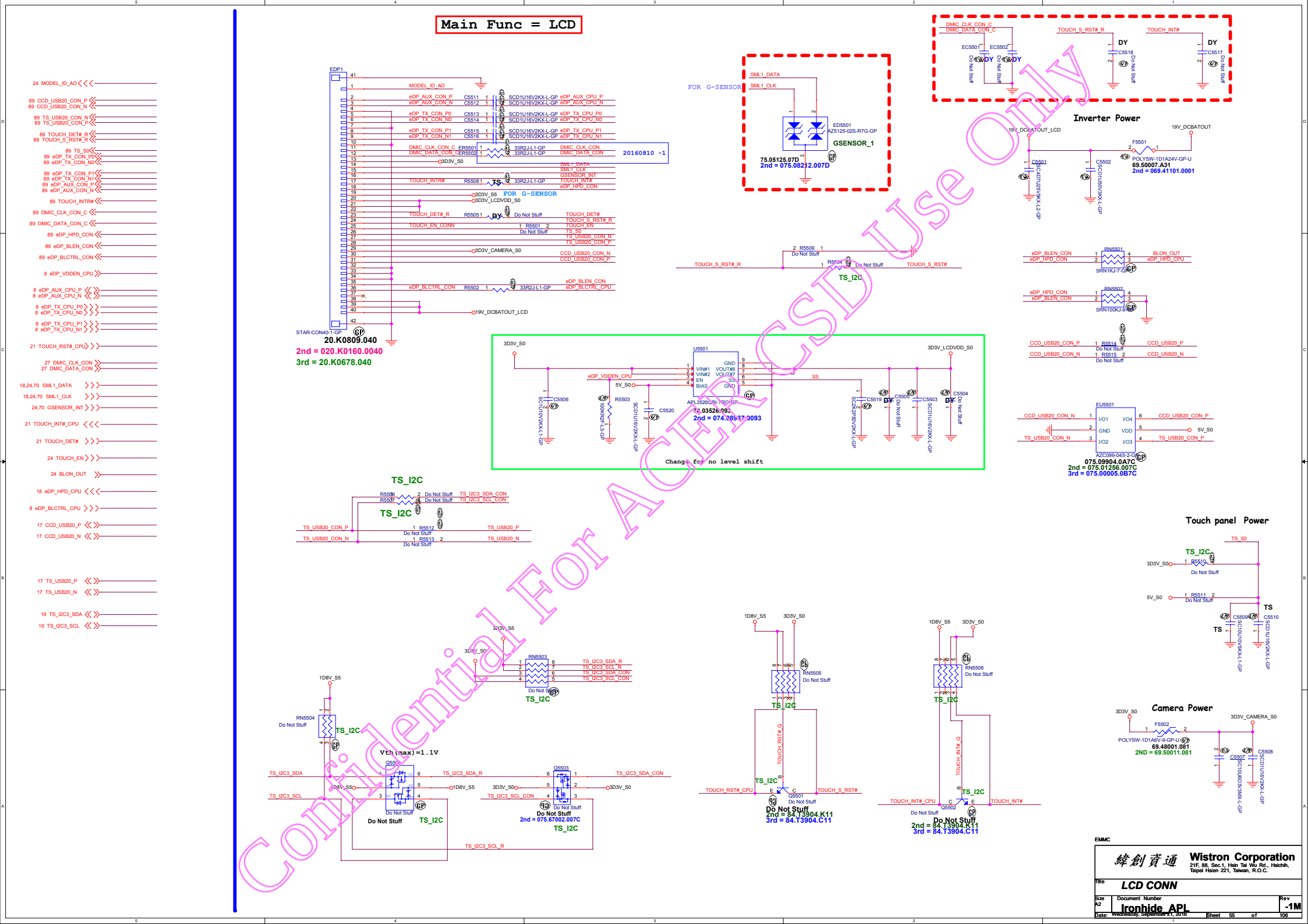


EMMC

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V_S0		
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 53 of 106	


EMMC
U5401
20160819 -1
EMMC64G-E100-GP
1st = 072.64100.000U
2nd = KN.0320B.007
3rd = KN.0320G.008
4th = KN.0640G.005
Vth(max)=1.1V
Q5401
Do Not Stuff
2nd = 84.05067.031
ED5401
EMC solution
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMMC
Ironhide_APL
-1M
Wednesday, September 21, 2016
Sheet 54 of 106
Confidential for ALPS Use Only

Main Func = LCD



SSID = mSATA

Blanking

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Title: *Reserved*

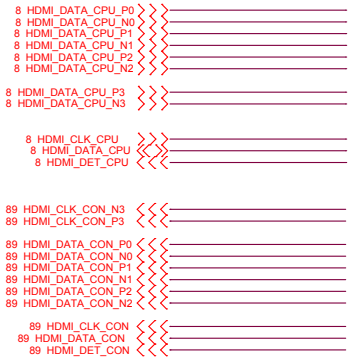
Size	Document Number	Rev
A4	Ironhide_APL	-1M

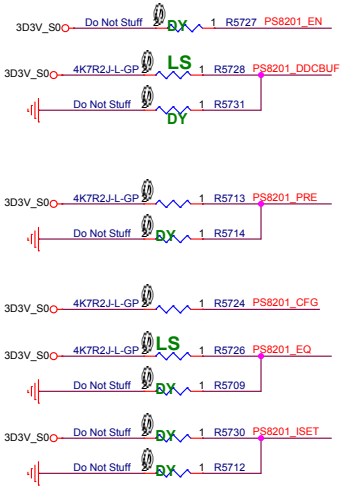
Date: Wednesday, September 21, 2016 Sheet 56 of 106

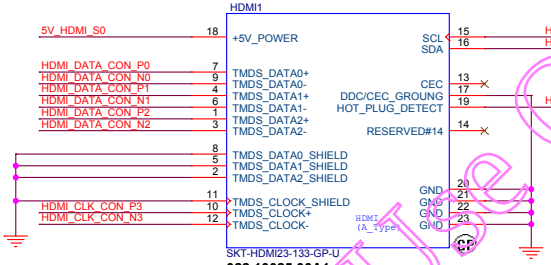
SSID = VIDEO

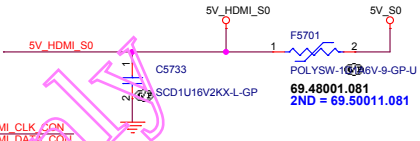
HDMI Level Shifter & CONNECTOR

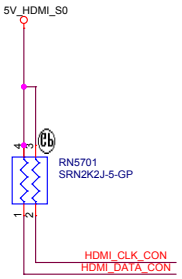
HDMI CONN

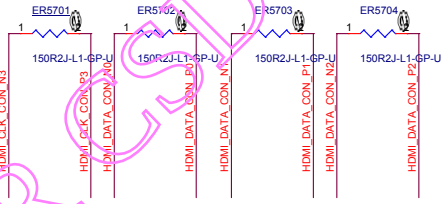


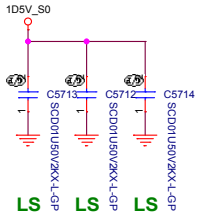


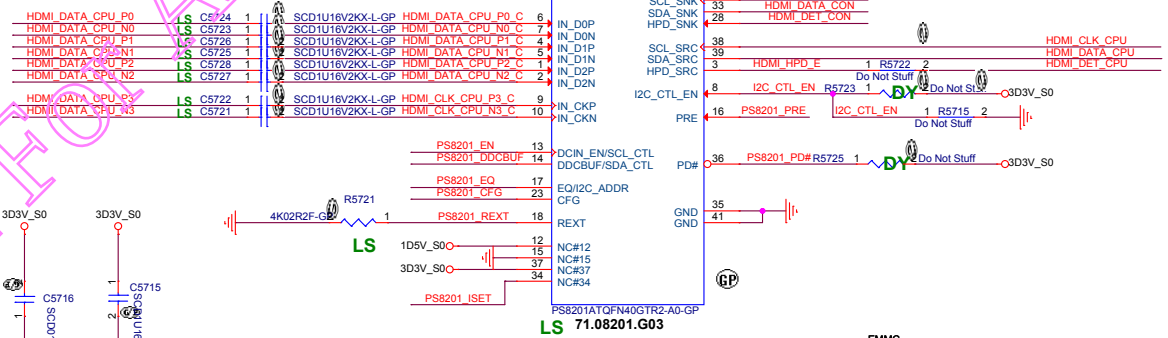


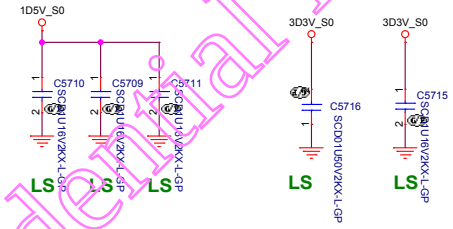












EMMC

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Title: HDMI Level Shifter/Connector		
Size: Custom	Document Number: Ironhide_APL	Rev: -1M
Date: Wednesday, September 21, 2016	Sheet 57 of 106	

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Title

Hall Sensor

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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SSID = 3G

Mini Card Connector(WWAN)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN CONN

Size	Document Number	Rev
A4	Ironhide_APL	-1M

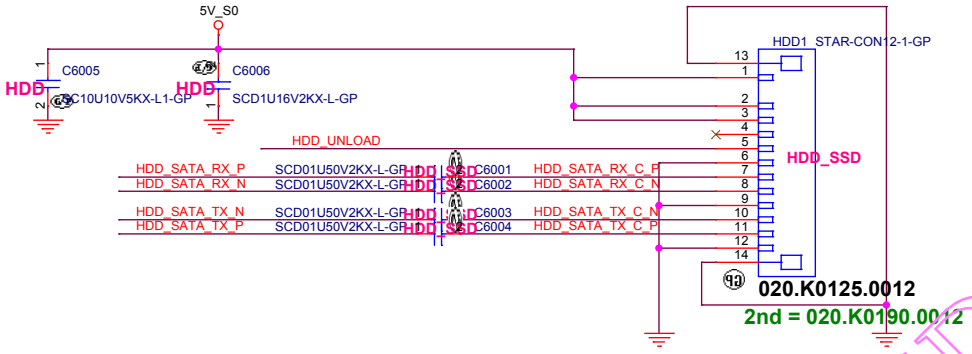
Date: Wednesday, September 21, 2016 Sheet 59 of 106

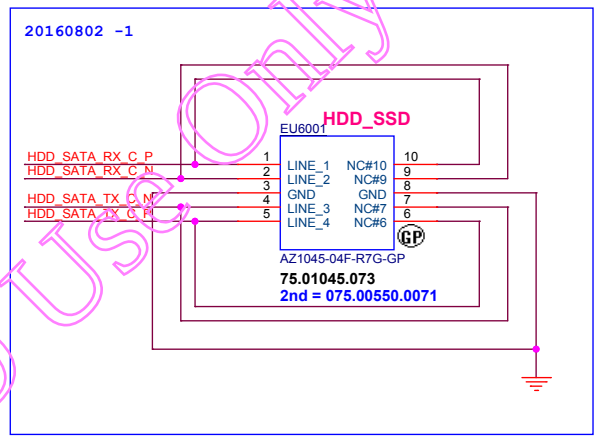
SSID = SATA

SATA HDD Connector

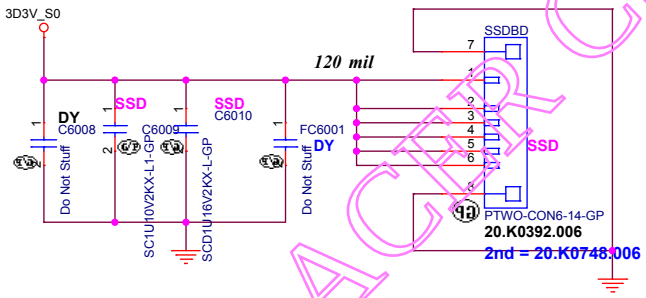
HDD_SATA_RX_P 16
HDD_SATA_RX_N 16
HDD_SATA_TX_N 16
HDD_SATA_TX_P 16

HDD_UNLOAD 69





AC coupling caps near connector < 100 mils



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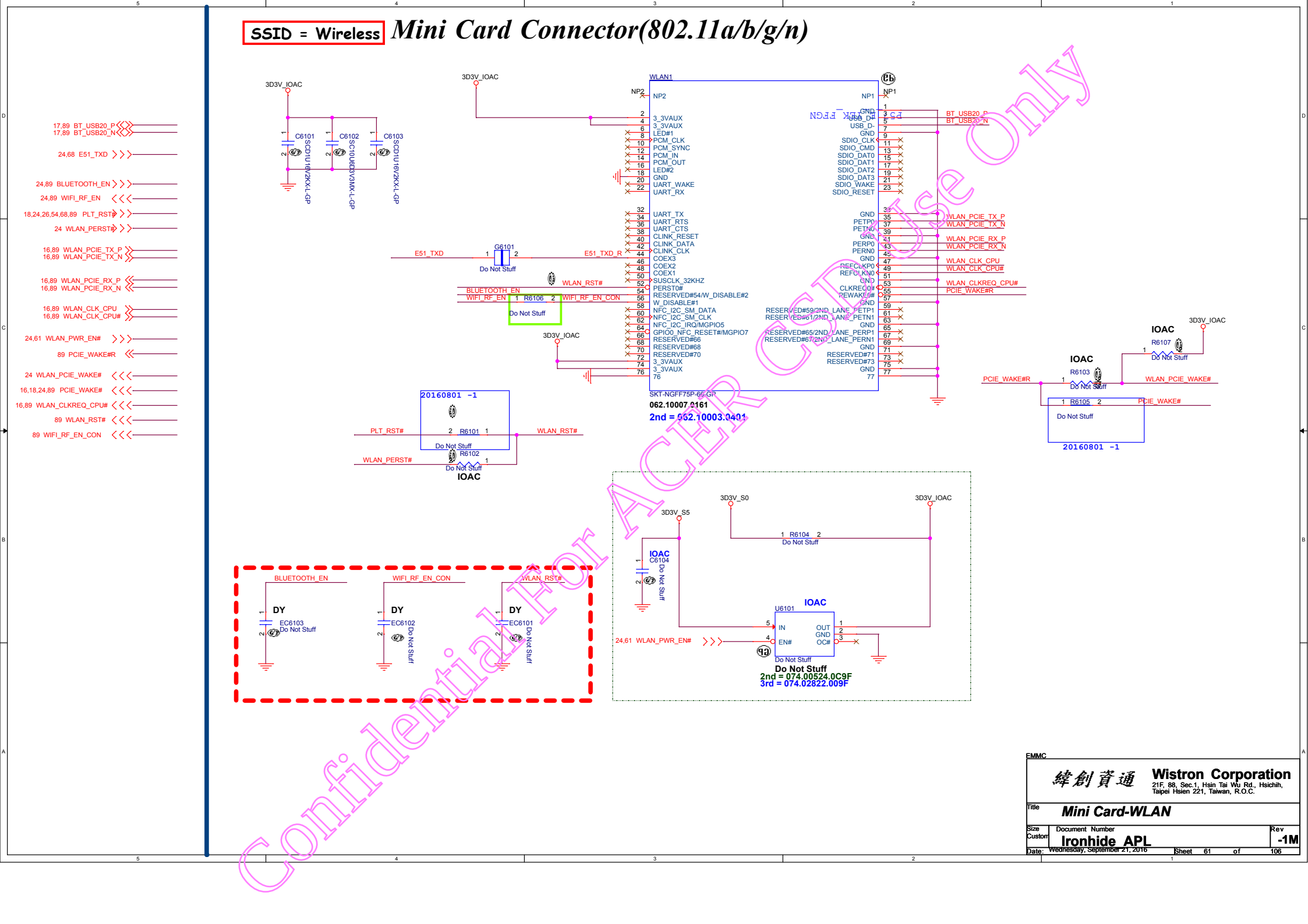
Title: HDD/SSD

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



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Title: Mini Card-WLAN

Size: Custom | Document Number: Ironhide_APL | Rev: -1M

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Title: *Audio Jack*

Size	Document Number	Rev
A	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 62 of 106

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Title: SSD

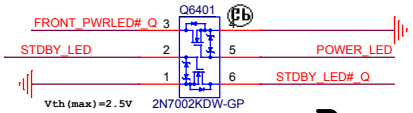
Size: A3 | Document Number: Ironhide_APL | Rev: -1M

Date: Wednesday, September 21, 2016 | Sheet 63 of 106

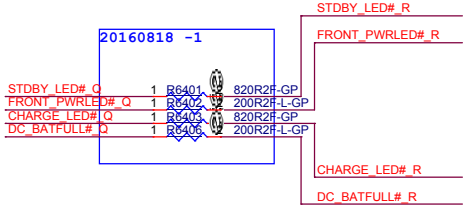
SSID = User.Interface

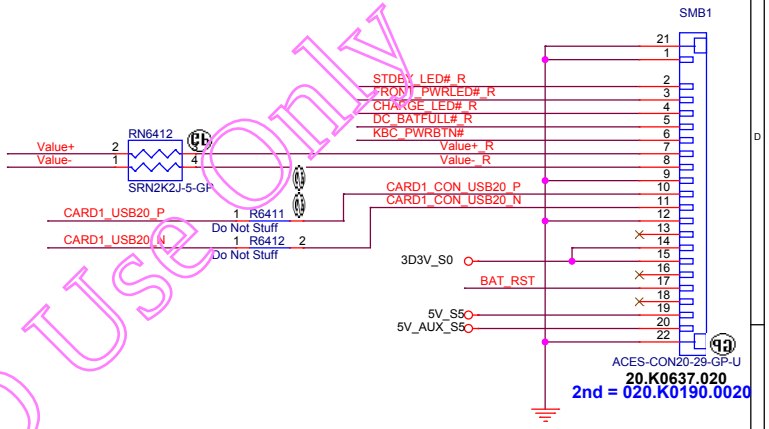
17 CARD1_USB20_P
17 CARD1_USB20_N
24 STDBY_LED
24 POWER_LED
24 CHARGE_LED
24 DC_BATFULL
24,89 LID_CLOSE#
24,89 LID_CLOSE2#
89 STDBY_LED#_R
89 FRONT_PWRLED#_R
89 CHARGE_LED#_R
89 DC_BATFULL#_R
18,24,89 KBC_PWRBTN#
24 Value+
24 Value-
89 Value+_R
89 Value-_R
89 CARD1_CON_USB20_P
89 CARD1_CON_USB20_N
43 BAT_RST

Power button LED

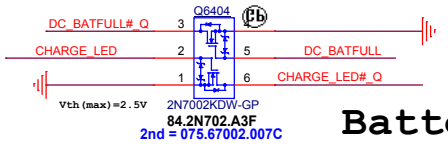


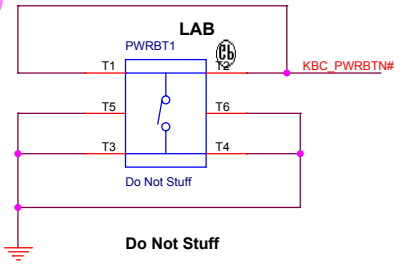
Power STDBY_LED



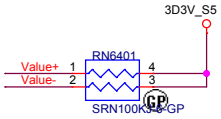


Battery LED2(DC_BATFULL)

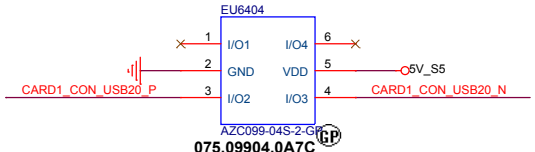


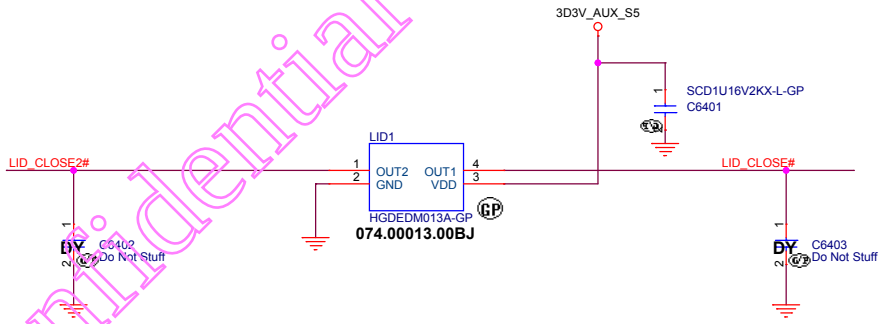


Do Not Stuff



Battery LED1(CHARGE)





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Title	LED Bard/Power Button	
Size A3	Document Number Ironhide_APL	Rev -1M
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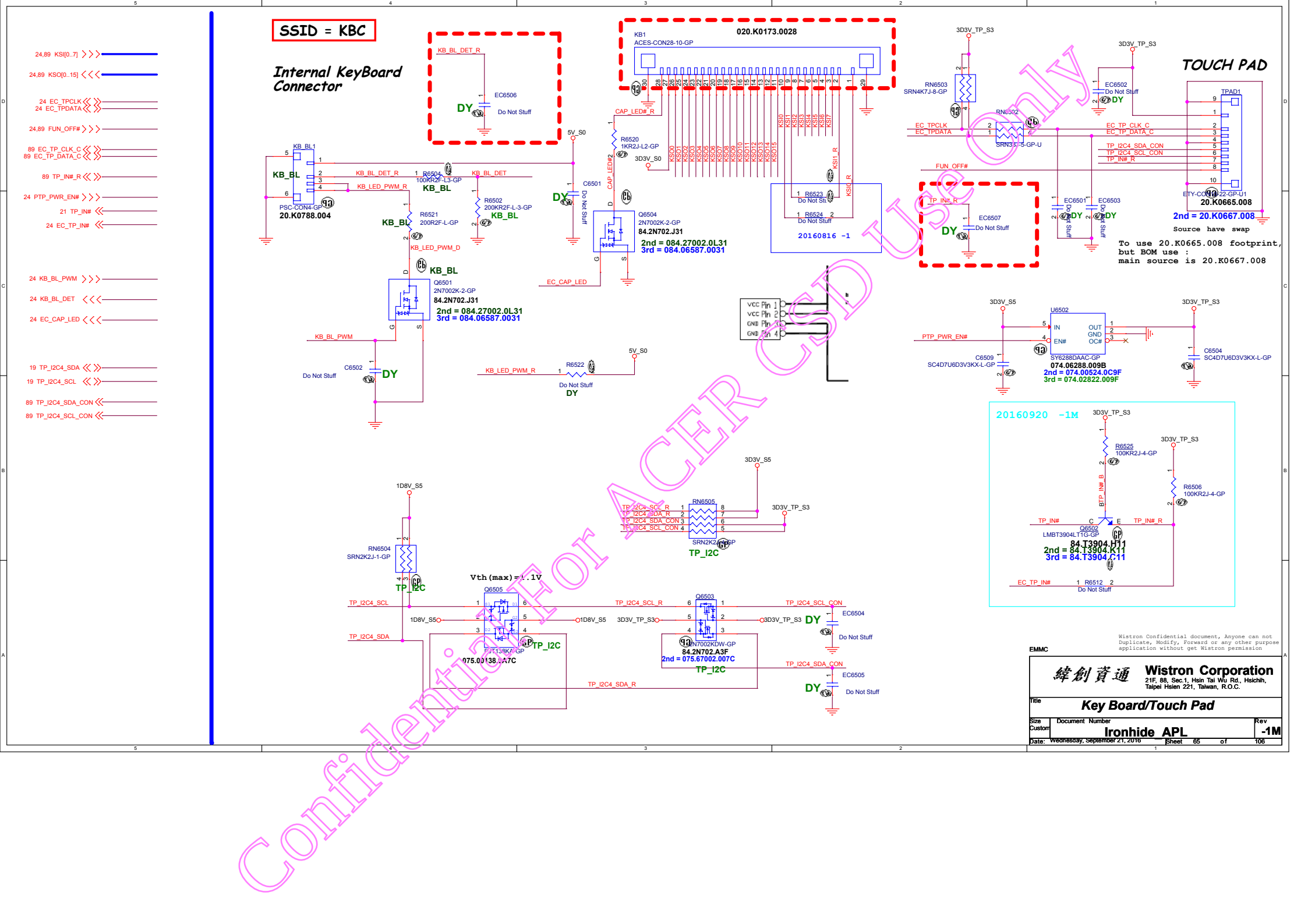
SSID = KBC
Internal KeyBoard Connector
020.K0173.0028
TOUCH PAD
20.K0788.004
20.K0665.008
2nd = 20.K0667.008
Source have swap
To use 20.K0665.008 footprint, but BOM use : main source is 20.K0667.008
20160816 -1
20160920 -1M
Vth(max)=1.1V
Confidential for ACER CSD Use Only
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Key Board/Touch Pad
Ironhide_APL
-1M
Wednesday, September 21, 2016
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Title	IO/POWER BOARD CONN	
Size A	Document Number Ironhide_APL	Rev -1M
Date: Wednesday, September 21, 2016	Sheet 66 of 106	

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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```
SDO="H";   address="3Ah"
*SDO="L";  address="38h"
```

```
*CS="H";   mode="I2C"
CS="L";    mode="SPI"
```


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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G Sensor***

Size	Document Number	Rev
A	Ironhide_APL	-1M

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19,24 INT_SERIRQ
19,90 LPC_CLK_DBG

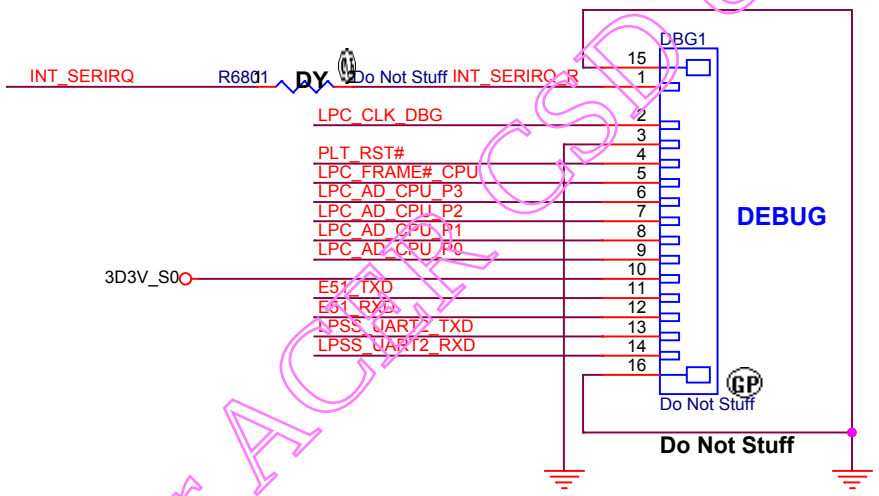
18,24,26,54,61,89 PLT_RST#
19,24 LPC_FRAME#_CPU

19,24 LPC_AD_CPU_P3
19,24 LPC_AD_CPU_P2

19,24 LPC_AD_CPU_P1
19,24 LPC_AD_CPU_P0

24,61 E51_TXD
24 E51_RXD

21 LPSS_UART2_TXD
21 LPSS_UART2_RXD



EMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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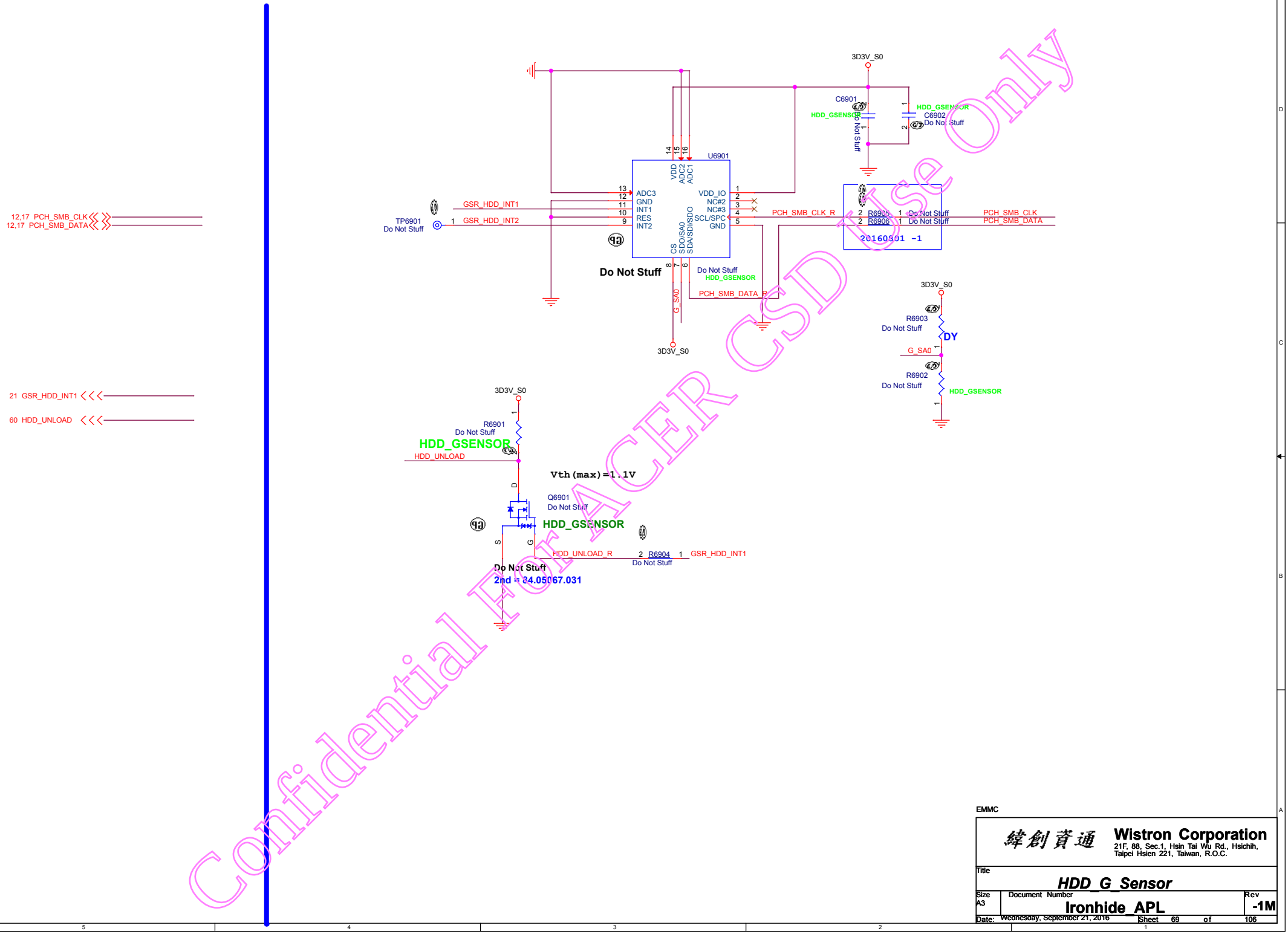

EMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD_G_Sensor***

Size	Document Number	Rev
A3	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 69 of 106

SSID = User.Interface

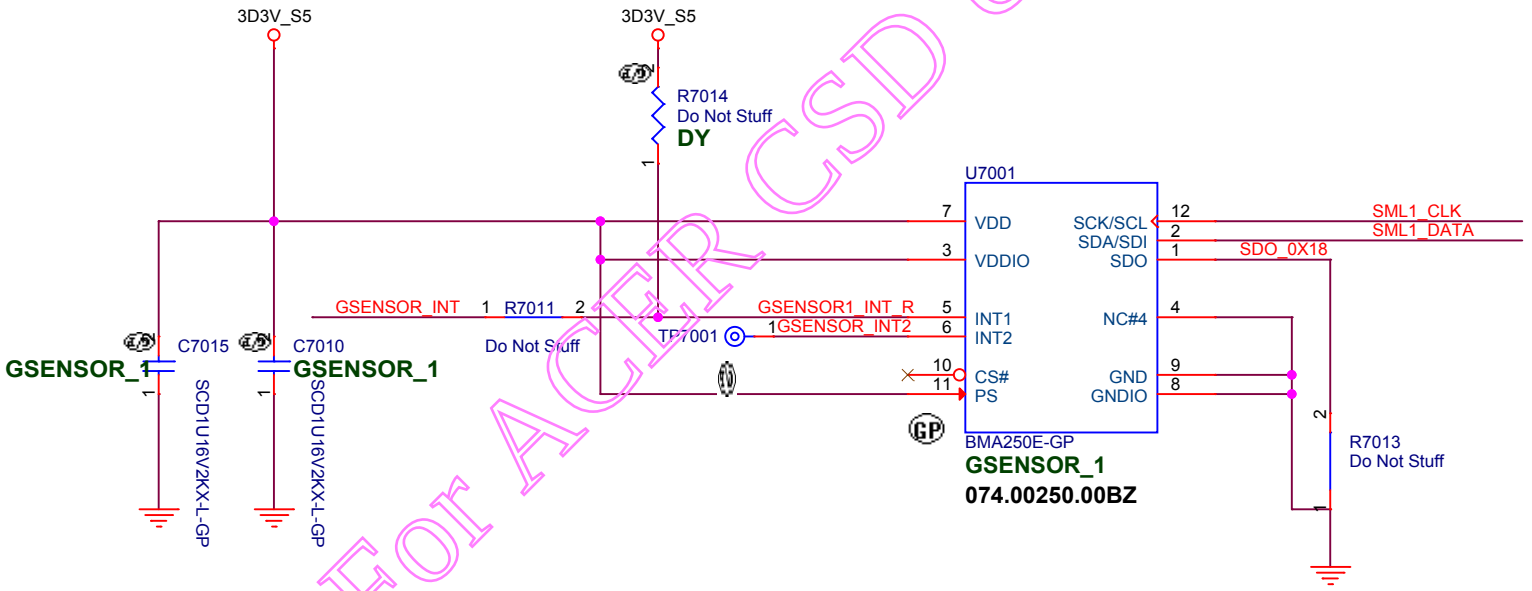
G Sensor

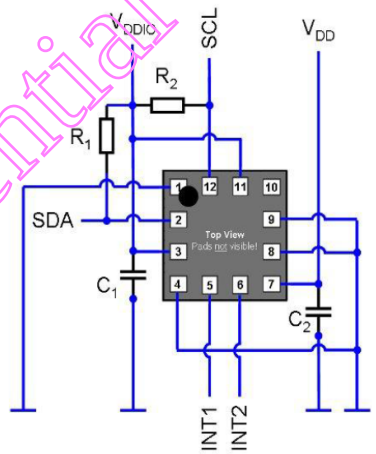
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.

24,55 GSENSOR_INT

18,24,55 SML1_CLK
18,24,55 SML1_DATA





EMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **G SENSOR**

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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Title

H_Sensor

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (5/5)*

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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Title: GPU(PEG)

Size	Document Number	Rev
A2	Ironhide_APL	-1M

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EMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (DIGITALOUT)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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EMMC

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21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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EMMC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (GPIO/STRAP)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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EMMC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (POWER/GND)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

Date: Wednesday, September 21, 2016 Sheet 79 of 106

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RT8812A_VGA_CORE

Size	Document Number	Rev
A4	Ironhide_APL	-1M
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EMMC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A2	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Switchable GFX LCD(2/2)

Size	Document Number	Rev
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Date: Wednesday, September 21, 2016 Sheet 85 of 106

SSID = Finger Print

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	Ironhide_APL	-1M

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EMMC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **Ironhide_APL**	Rev **-1M**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio Jack

Size	Document Number	Rev
A	Ironhide_APL	-1M

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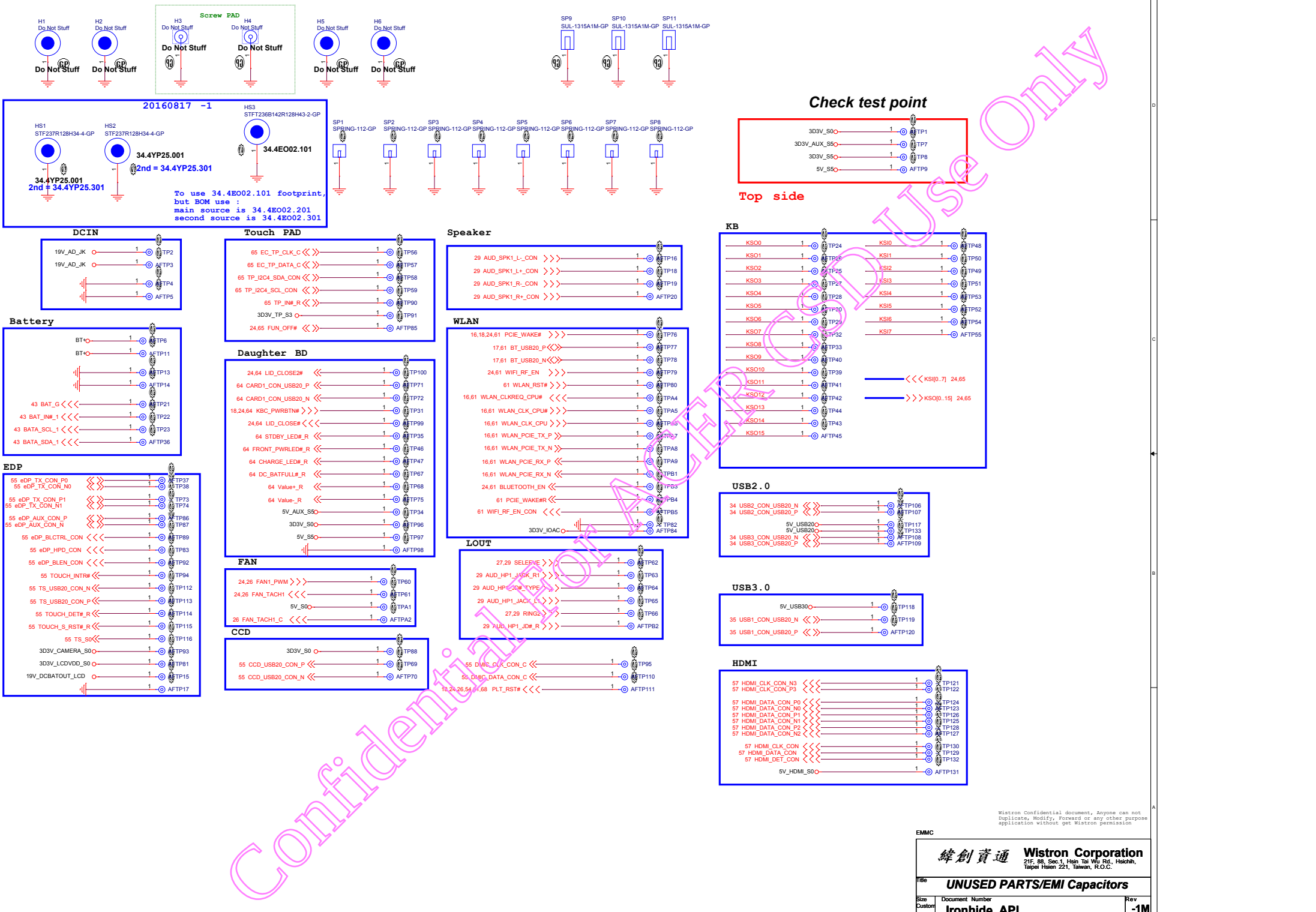

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Title: ***UNUSED PARTS/EMI Capacitors***

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let the cap close to PR4417

BT+ — EC9001 1 — Do Not Stuff

let the cap close to PU4504

PWR_DCBATOUT_5V — EC9003 1 — Do Not Stuff; EC9004 1 — Do Not Stuff

let the cap close to PU4502

PWR_DCBATOUT_3D3V — EC9007 1 — Do Not Stuff; EC9008 1 — Do Not Stuff

let the cap close to PU4403

19V_DCBATOUT — EC9023 1 — Do Not Stuff; EC9024 1 — Do Not Stuff

let the cap close to PU5101

PWR_DCBATOUT_VDDQ — EC9019 1 — Do Not Stuff; EC9020 1 — Do Not Stuff

let the cap close to PU4601.

19V_DCBATOUT — EC9011 1 — Do Not Stuff; EC9012 1 — Do Not Stuff

let the cap close to PU4702.

19V_DCBATOUT — EC9015 1 — Do Not Stuff; EC9016 1 — Do Not Stuff

let the cap close to PU5003

PWR_DCBATOUT_VNN — EC9071 1 — Do Not Stuff; EC9072 1 — Do Not Stuff

let the cap close to EDP1

19V_DCBATOUT_LCD — EC9053 1 — Do Not Stuff; EC9054 1 — Do Not Stuff

let the cap close to U2401

19,24,90 LPC_CLK_KBC — EC9041 1 — Do Not Stuff

let the cap close to U2701

21,27 HDA_BITCLK_CODEC — EC9042 1 — Do Not Stuff

let the cap close to CPU.

21,27 HDA_SDOUT_CODEC — EC9059 1 — Do Not Stuff

let the cap close to CPU.

19 HDA_RST#_CPU — EC9060 1 — Do Not Stuff

19V_DCBATOUT — EC9073 1 — SCD1U25V2KX-L-GP; EC9074 1 — SCD1U25V2KX-L-GP; EC9075 1 — SCD1U25V2KX-L-GP; EC9076 1 — SCD1U25V2KX-L-GP; EC9077 1 — SCD1U25V2KX-L-GP; EC9078 1 — SCD1U25V2KX-L-GP; EC9079 1 — SCD1U25V2KX-L-GP

19V_DCBATOUT — EC9080 1 — Do Not Stuff — DY

For Acoustic Noise

let the cap close to PU4403

19V_DCBATOUT — FC9001 1 — Do Not Stuff; FC9002 1 — Do Not Stuff

let the cap close to PR4417

BT+ — FC9003 1 — Do Not Stuff; FC9004 1 — Do Not Stuff

let the cap close to PU4504

PWR_DCBATOUT_5V — FC9005 1 — Do Not Stuff; FC9006 1 — Do Not Stuff

let the cap close to PL4502

PWR_5V — FC9007 1 — Do Not Stuff; FC9008 1 — Do Not Stuff

let the cap close to PU4502

PWR_DCBATOUT_3D3V — FC909 1 — Do Not Stuff; FC9010 1 — Do Not Stuff

let the cap close to PL4501

PWR_3D3V — FC9011 1 — Do Not Stuff; FC9012 1 — Do Not Stuff

let the cap close to PU4601

19V_DCBATOUT — FC9013 1 — Do Not Stuff; FC9014 1 — Do Not Stuff

let the cap close to PL4603

1D8V_S5 — FC9015 1 — Do Not Stuff; FC9016 1 — Do Not Stuff

let the cap close to PL4601

1D24V_S5 — FC9017 1 — Do Not Stuff; FC9018 1 — Do Not Stuff

let the cap close to PL4602

1D05V_S0 — FC9019 1 — Do Not Stuff; FC9020 1 — Do Not Stuff

let the cap close to PU4701

0D675V_VREF_S0 — FC9021 1 — Do Not Stuff; FC9022 1 — Do Not Stuff

let the cap close to PU4601

PWR_VDDQ — FC9023 1 — Do Not Stuff; FC9024 1 — Do Not Stuff

let the cap close to U4001

5V_S5 — FC9025 1 — Do Not Stuff; FC9026 1 — Do Not Stuff

let the cap close to U4001

3D3V_S5 — FC9027 1 — Do Not Stuff; FC9028 1 — Do Not Stuff

let the cap close to U4001

5V_SYS_OUT — FC9029 1 — Do Not Stuff; FC9030 1 — Do Not Stuff

let the cap close to U4001

3V_SYS_OUT — FC9031 1 — Do Not Stuff; FC9032 1 — Do Not Stuff

let the cap close to U4002

1D8V_S5 — FC9034 1 — Do Not Stuff; FC9033 1 — Do Not Stuff

let the cap close to U4002

1D8V_S0 — FC9035 1 — Do Not Stuff; FC9036 1 — Do Not Stuff

let the cap close to U5301

3D3V_S5 — FC9037 1 — Do Not Stuff; FC9038 1 — Do Not Stuff

let the cap close to U5302

1D5V_S0 — FC9039 1 — Do Not Stuff; FC9040 1 — Do Not Stuff

let the cap close to PU4701

5V_S5 — FC9041 1 — Do Not Stuff; FC9042 1 — Do Not Stuff

let the cap close to PU4702

19V_DCBATOUT — FC9043 1 — Do Not Stuff; FC9044 1 — Do Not Stuff

let the cap close to PL4701

1V_CPU_VCGI — FC9045 1 — Do Not Stuff; FC9046 1 — Do Not Stuff

let the cap close to CPU1

1D35V_S3 — FC9047 1 — Do Not Stuff; FC9048 1 — 2 SCD1U16V2KX-L-GP; FC9095 1 — 2 Do Not Stuff; FC9096 1 — 2 SC2D2U16V2KX-GP

let the cap close to CPU1

1D05V_S0 — FC9049 1 — 2 SCD1U16V2KX-L-GP; FC9050 1 — 2 SC2D2U16V2KX-GP; FC9097 1 — Do Not Stuff; FC9098 1 — 2 SCD1U16V2KX-L-GP

let the cap close to CPU1

1D8V_S5 — FC9051 1 — 2 SCD1U16V2KX-L-GP; FC9052 1 — 2 SC2D2U16V2KX-GP; FC9099 1 — Do Not Stuff; FC9100 1 — Do Not Stuff

let the cap close to CPU1

1V_CPU_VCGI — FC9053 1 — 2 SCD1U16V2KX-L-GP; FC9054 1 — 2 SC2D2U16V2KX-GP; FC9102 1 — Do Not Stuff; FC9101 1 — Do Not Stuff

let the cap close to PU5002

5V_S5 — FC9056 1 — Do Not Stuff; FC9055 1 — Do Not Stuff

let the cap close to PU5003

PWR_DCBATOUT_VNN — FC9058 1 — Do Not Stuff; FC9057 1 — Do Not Stuff

let the cap close to PL5001

1V_CPU_VNN — FC9060 1 — Do Not Stuff; FC9059 1 — Do Not Stuff

let the cap close to PU5103

5V_S5 — FC9062 1 — Do Not Stuff; FC9061 1 — Do Not Stuff

let the cap close to PU5101

PWR_DCBATOUT_VDDQ — FC9064 1 — Do Not Stuff; FC9063 1 — Do Not Stuff

let the cap close to PL5101

PWR_VDDQ — FC9066 1 — Do Not Stuff; FC9065 1 — Do Not Stuff

let the cap close to RN1207

1D35V_S3 — FC9068 1 — 2 Do Not Stuff; FC9067 1 — 2 SC2D2U16V2KX-GP

let the cap close to DM1

3D3V_S0 — FC9070 1 — 2 SC2D2U16V2KX-GP; FC9069 1 — 2 SCD1U16V2KX-L-GP

let the cap close to DM1

1D35V_S3 — FC9071 1 — 2 SC2D2U16V2KX-GP; FC9072 1 — 2 SCD1U16V2KX-L-GP; FC9104 1 — 2 SCD1U16V2KX-L-GP; FC9103 1 — 2 SCD1U16V2KX-L-GP; FC9105 1 — 2 Do Not Stuff; FC9106 1 — 2 Do Not Stuff

let the cap close to WLAN1

3D3V_IOAC — FC9073 1 — Do Not Stuff

let the cap close to EDP1

3D3V_S0 — FC9075 1 — Do Not Stuff

let the cap close to EDP1

3D3V_S5 — FC9077 1 — Do Not Stuff

let the cap close to EDP1

3D3V_LCDVDD_S0 — FC9079 1 — Do Not Stuff

let the cap close to EDP1

19V_DCBATOUT_LCD — FC9081 1 — Do Not Stuff

let the cap close to HDMI1

5V_HDMI_S0 — FC9083 1 — Do Not Stuff

let the cap close to HDD1

5V_S0 — FC9085 1 — EC4D7U10V3KX-GP — HDD 20160803 -1

let the cap close to SSDBD

3D3V_S0 — FC9087 1 — Do Not Stuff; FC9088 1 — Do Not Stuff

let the cap close to U7001

3D3V_S5 — FC9089 1 — Do Not Stuff

let the cap close to R1905

19,24,90 LPC_CLK_KBC — FC9091 1 — Do Not Stuff

let the cap close to R1904

19,68 LPC_CLK_DBG — FC9092 1 — Do Not Stuff

let the cap close to CPU1

19,24,25 SPI_CLK_ROM — FC9093 1 — Do Not Stuff

let the cap close to CPU1

21,27 HDA_SDIN0_CPU — FC9094 1 — Do Not Stuff

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SSID = Docking

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SSID = Intel LAN

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	O	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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PCH_XDP

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Title: ***Audio Jack***

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Main Func = Debug

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Title: *table of content*

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Change History

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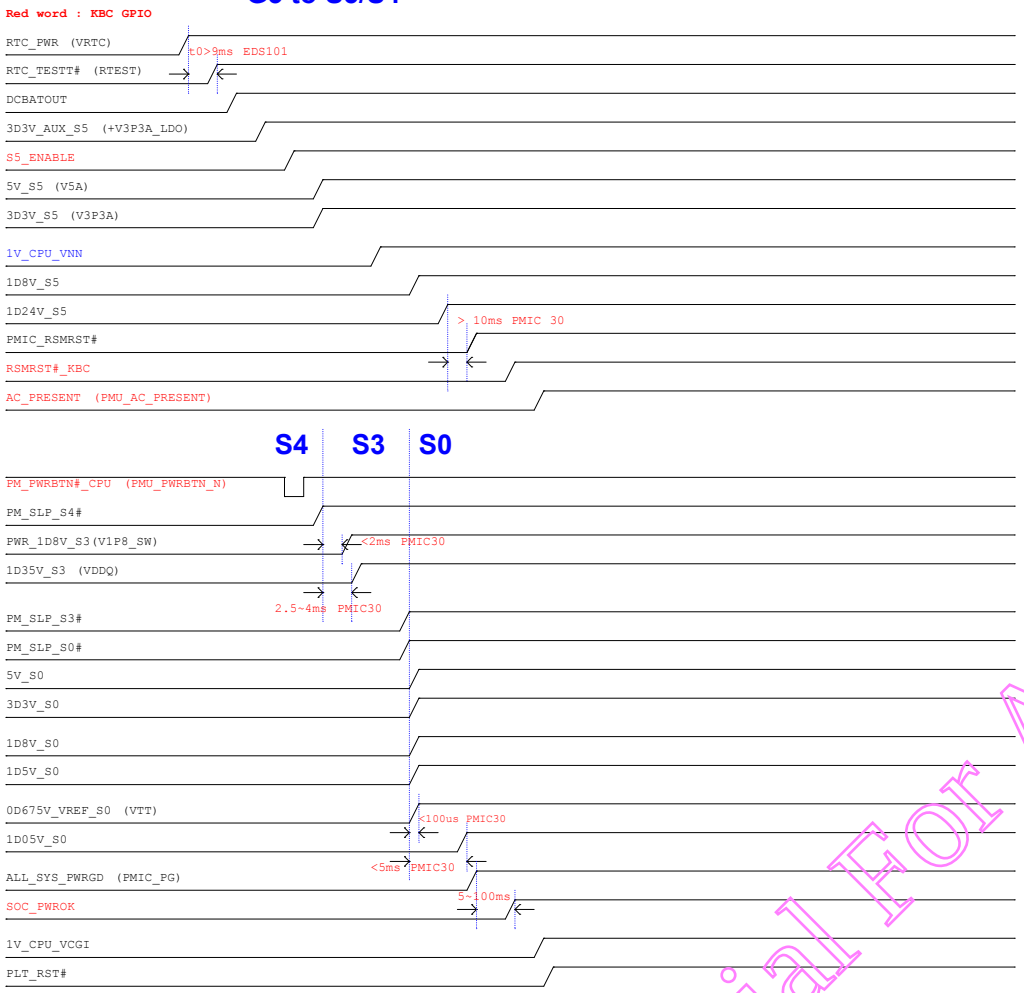
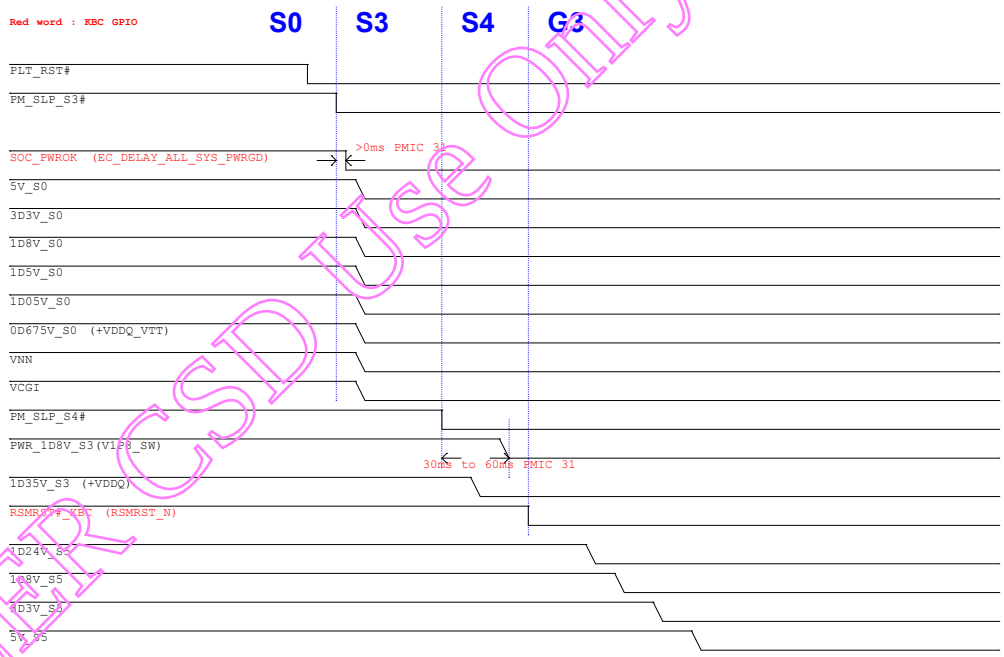
Intel-Power Up Sequence

G3 to S5/S4



Intel-Power Down Sequence



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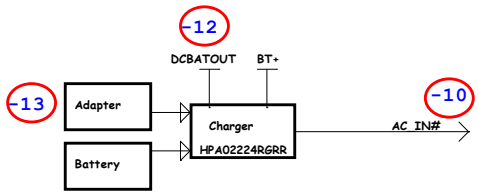
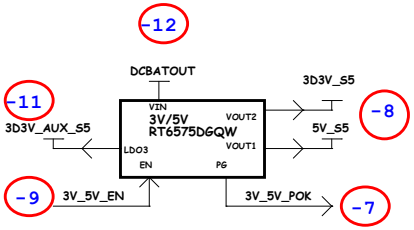
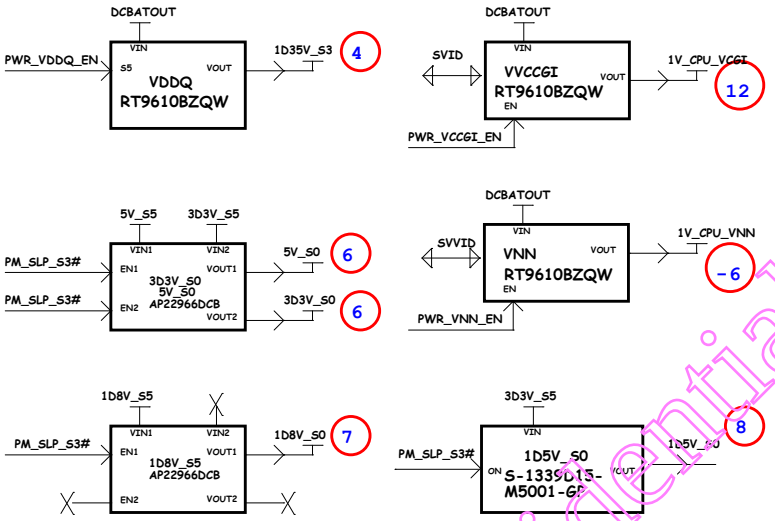
APOLLO LAKE SEQUENCE & BLOCK DIAGRAM

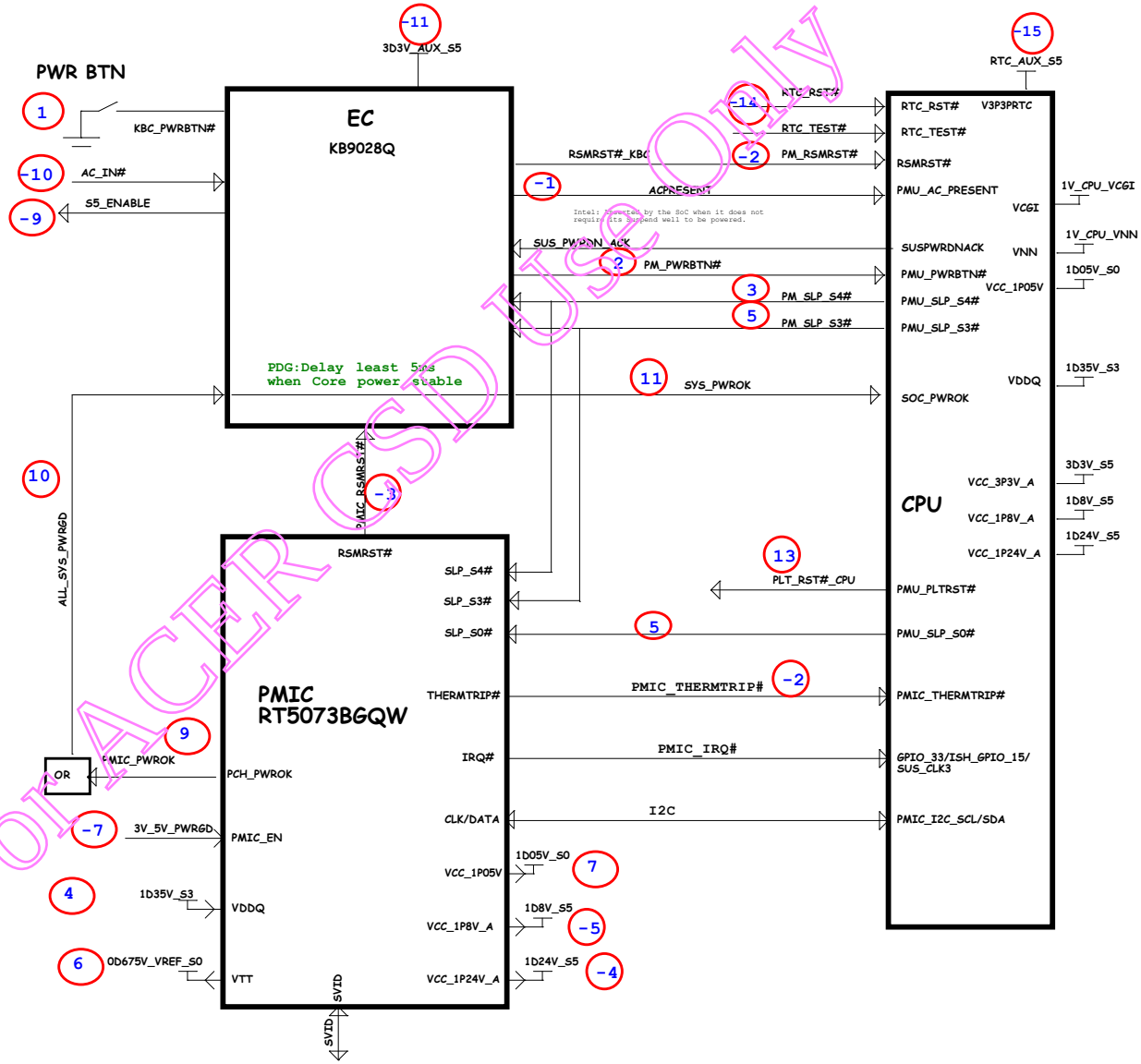


S5 PWR



S3-S0 PWR





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Title: **Power Block Diagram**

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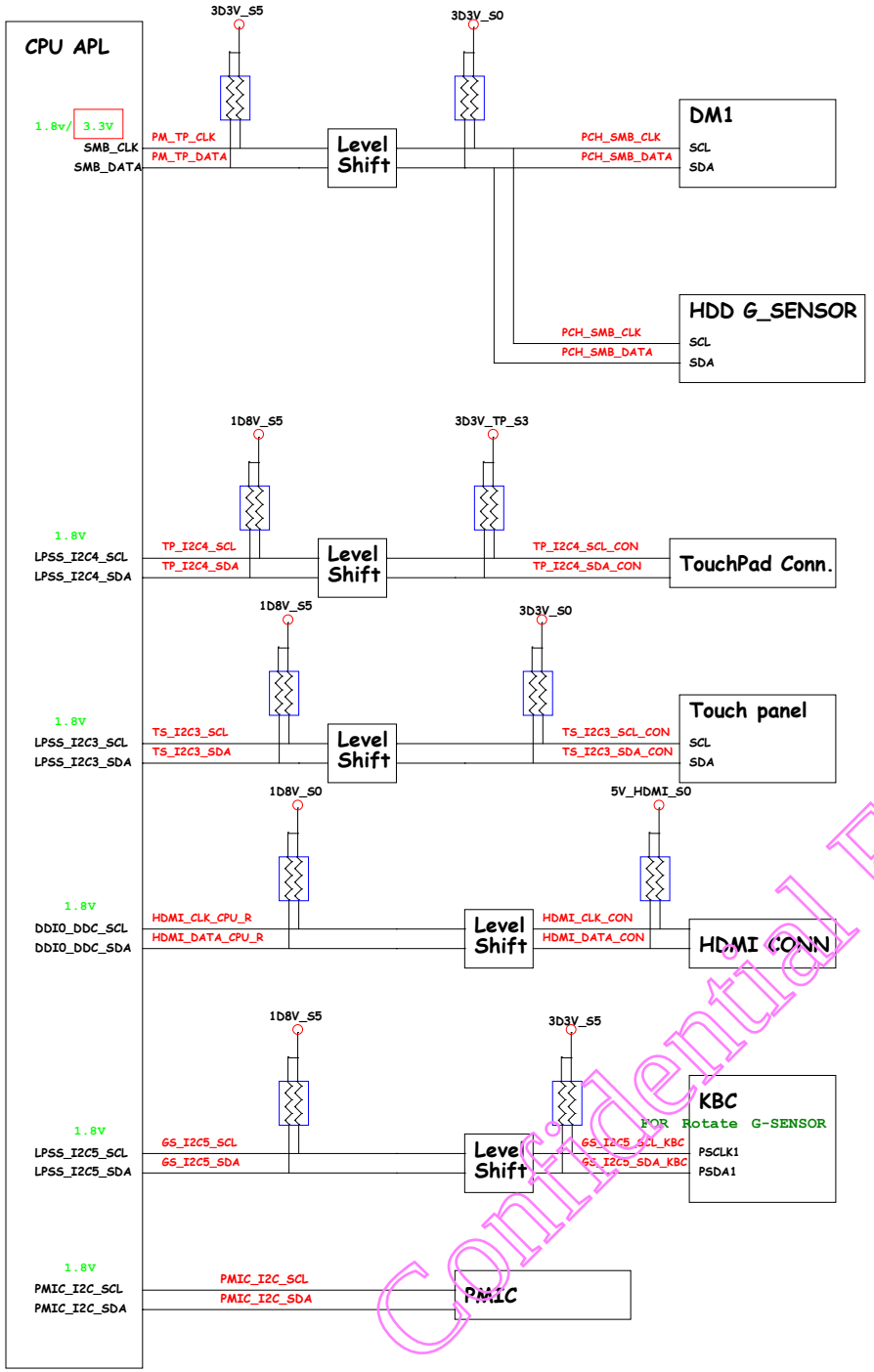
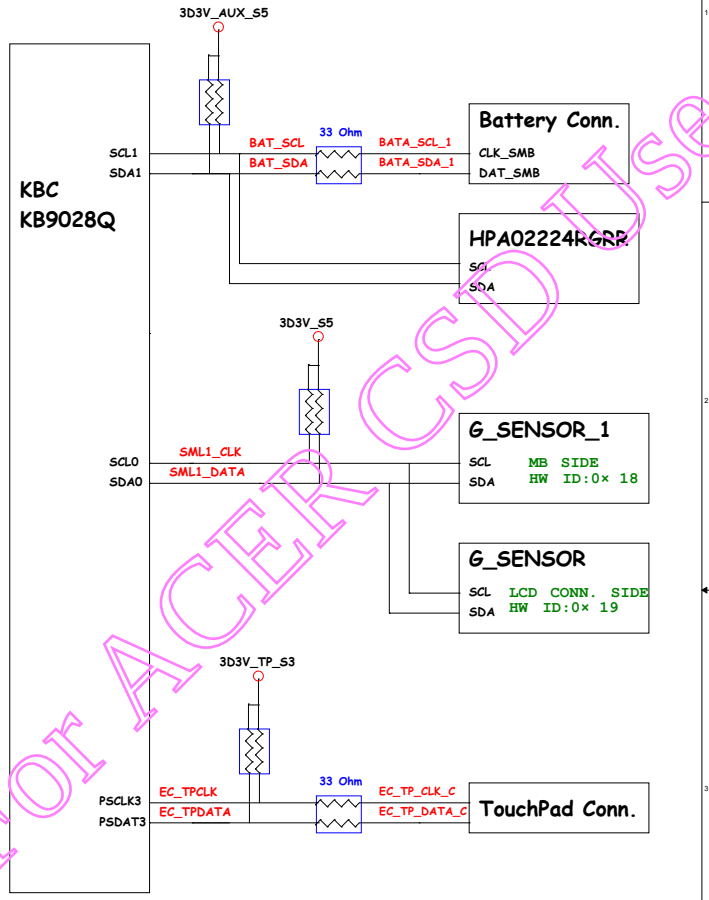
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

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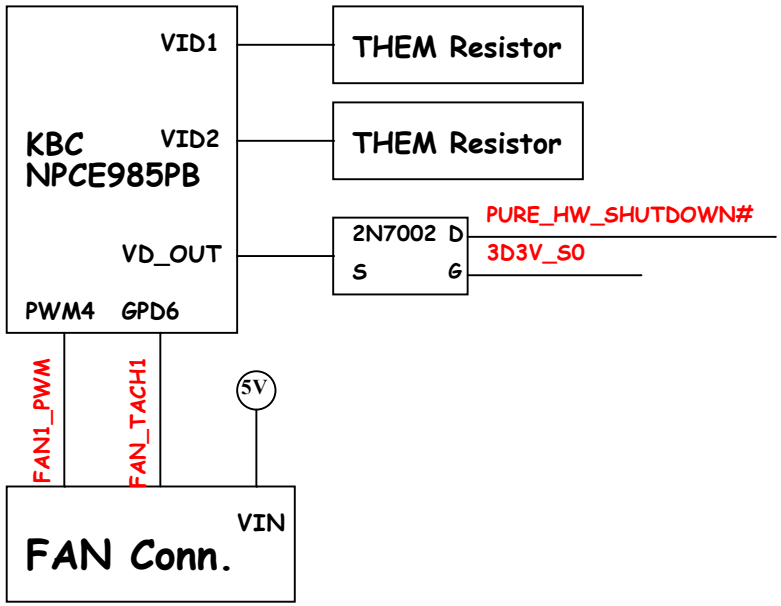
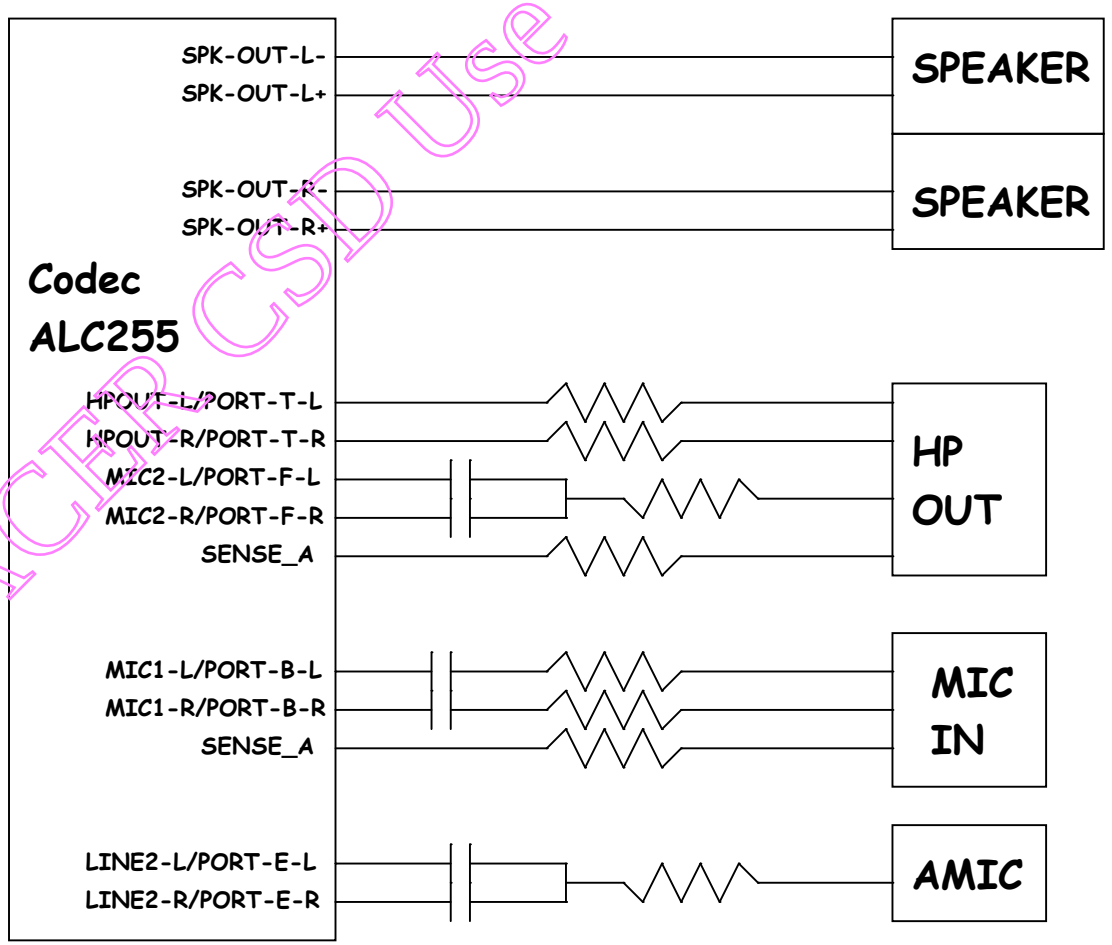
Thermal Block Diagram



Audio Block Diagram



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LAN Switch

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