IPPLP-RH

Revision: B00

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55	FRONT PANEL
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58	HDMI OUT
59	G-SENSOR
60	DP REDRIVER
61	DP CONN
62	TPM
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67	3P3_LAN,12V,1P5V_PCH,3P3V_BG

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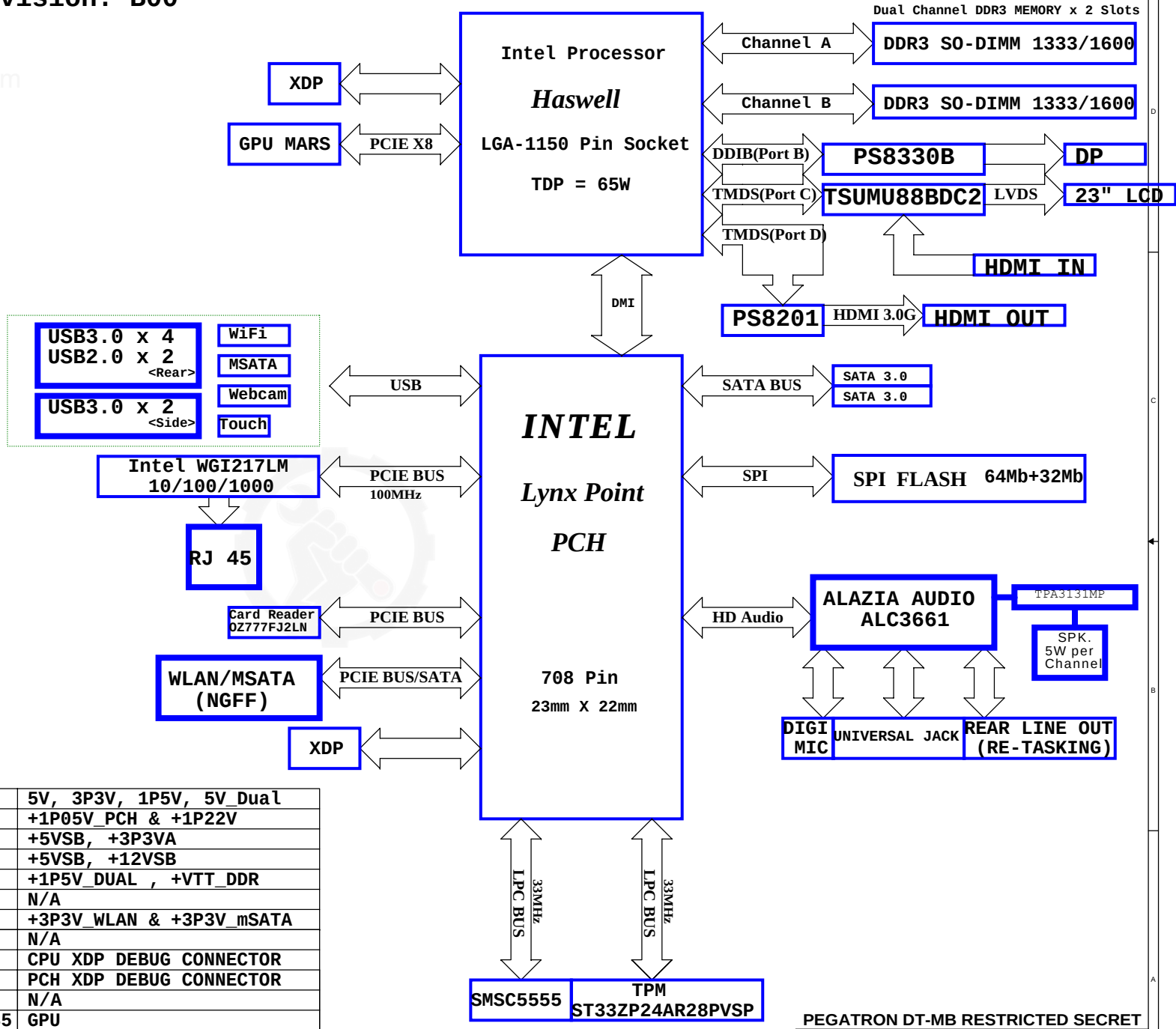
69	+1P05V_PCH & +1P22V
70	+5VSB, +3P3VA
71	+5VSB, +12VSB
72	+1P5V_DUAL , +VTT_DDR
73	N/A
74	+3P3V_WLAN & +3P3V_mSATA
75	N/A
76	CPU XDP DEBUG CONNECTOR
77	PCH XDP DEBUG CONNECTOR
78	N/A
79~85	GPU
86~89	VRAM
90	+1P8V
91	3P3V_GPU&+0P95V
92	+1P35V_GPU & +1P05V_ME

93~94	VDDC CONTROLLER
95	SIDE KEY
96	CONVERTER BOARD
95	TP



PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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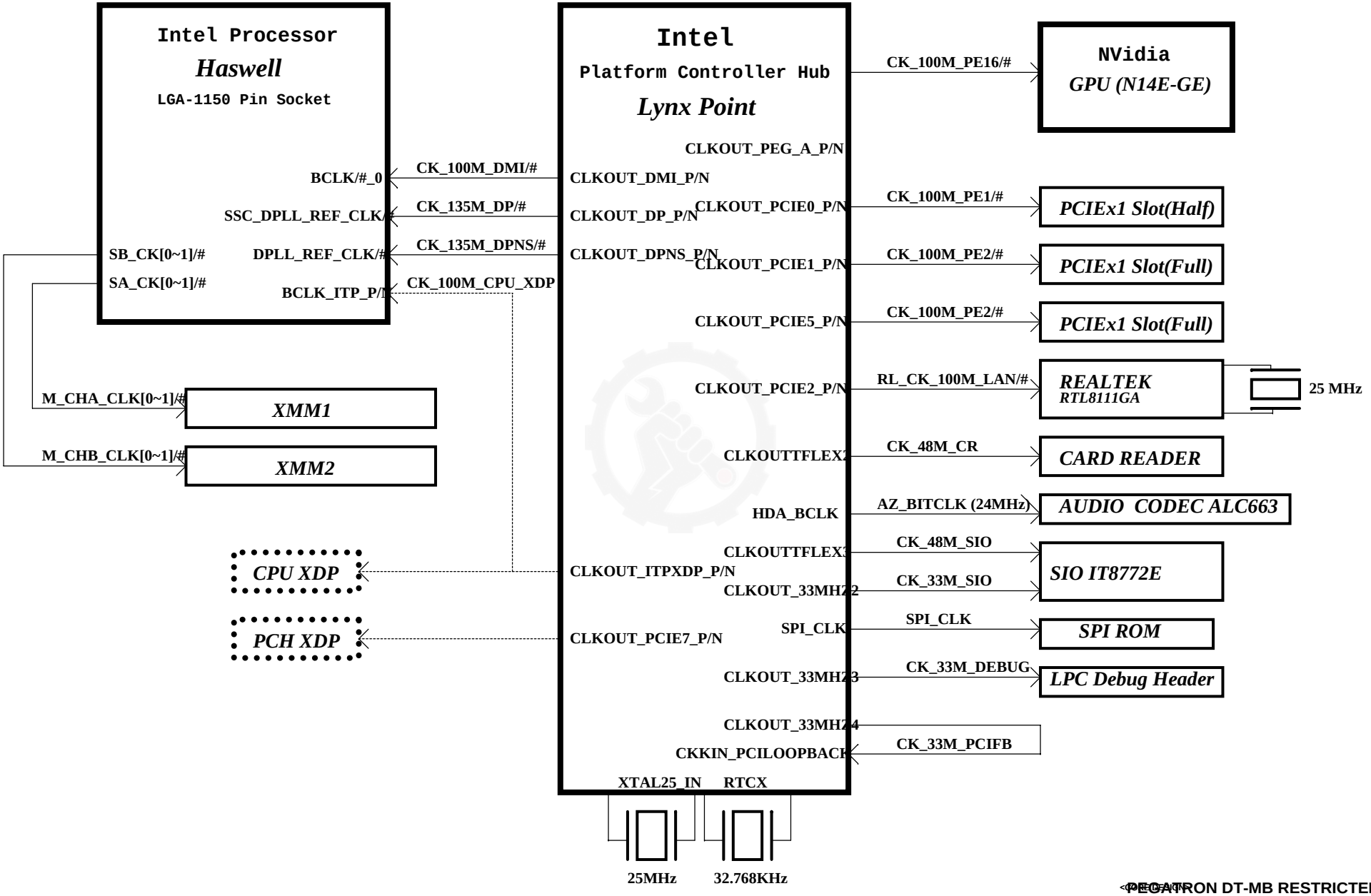

PEGATRON	Title : CLCOK DISTRIBUTION	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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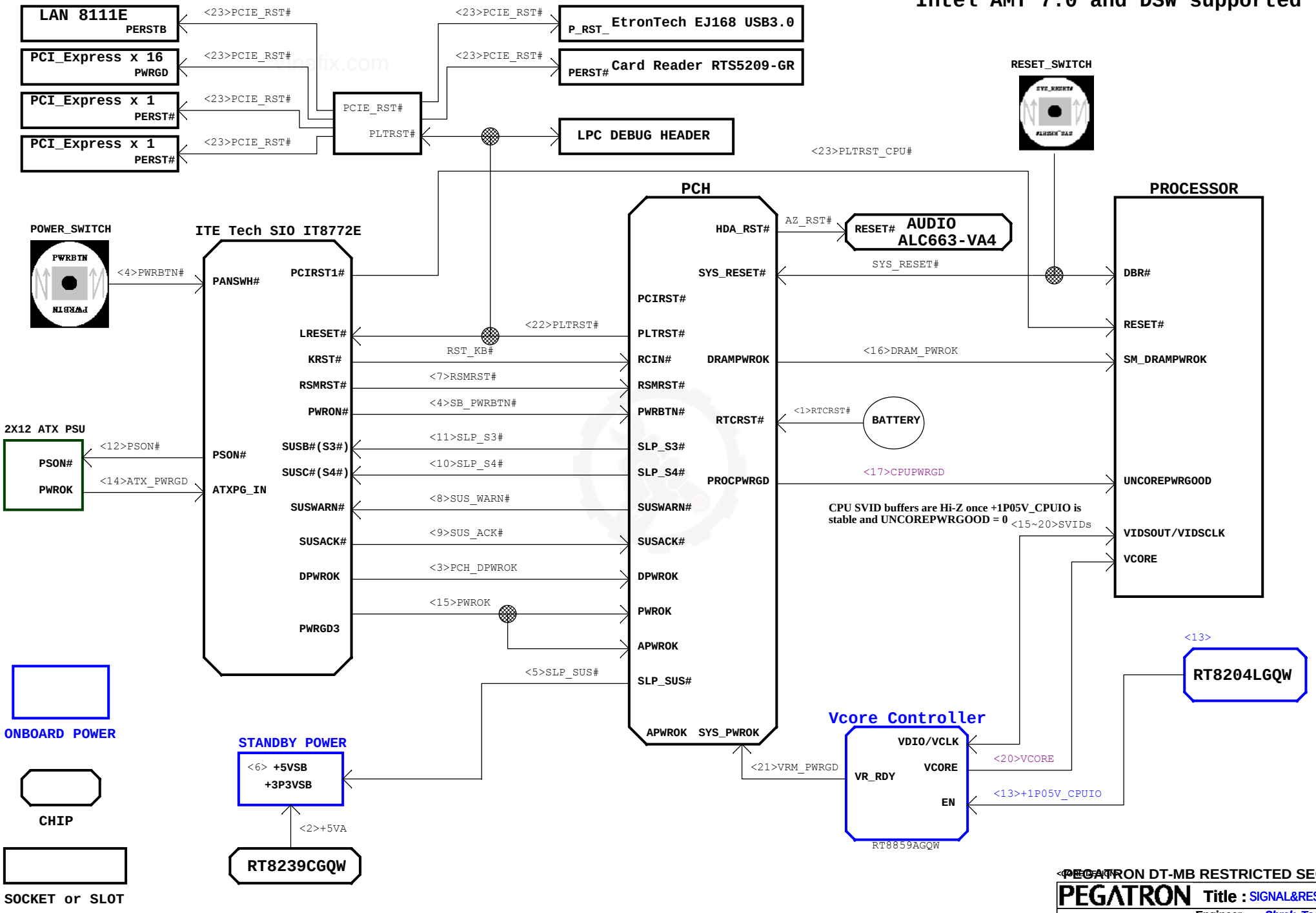
Intel AMT 7.0 and DSW supported



PEGATRON	Title : SIGNAL&RESET MAP	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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Schematics Change History

Version	Date	Comments
	2012/11/19	PCIEX16 RVS(20121119_2100)

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.
Property: BOM
I = Installed Part. PROTO = PROTO Phase Only.
NI = Not Installed Part. VP = Virtual Part.

PEGATRON Title : CHANGE HISTORY

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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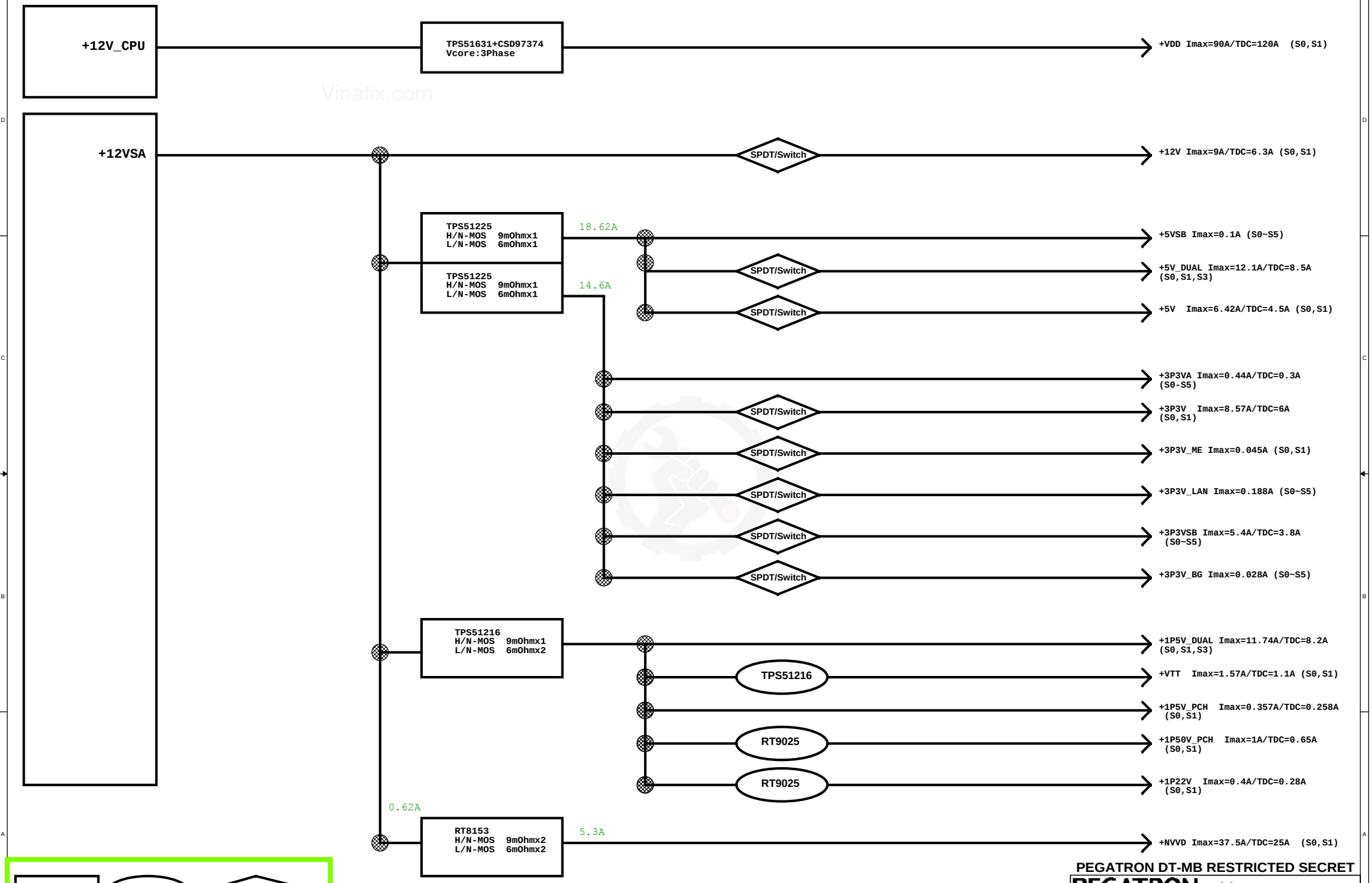

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER FLOW

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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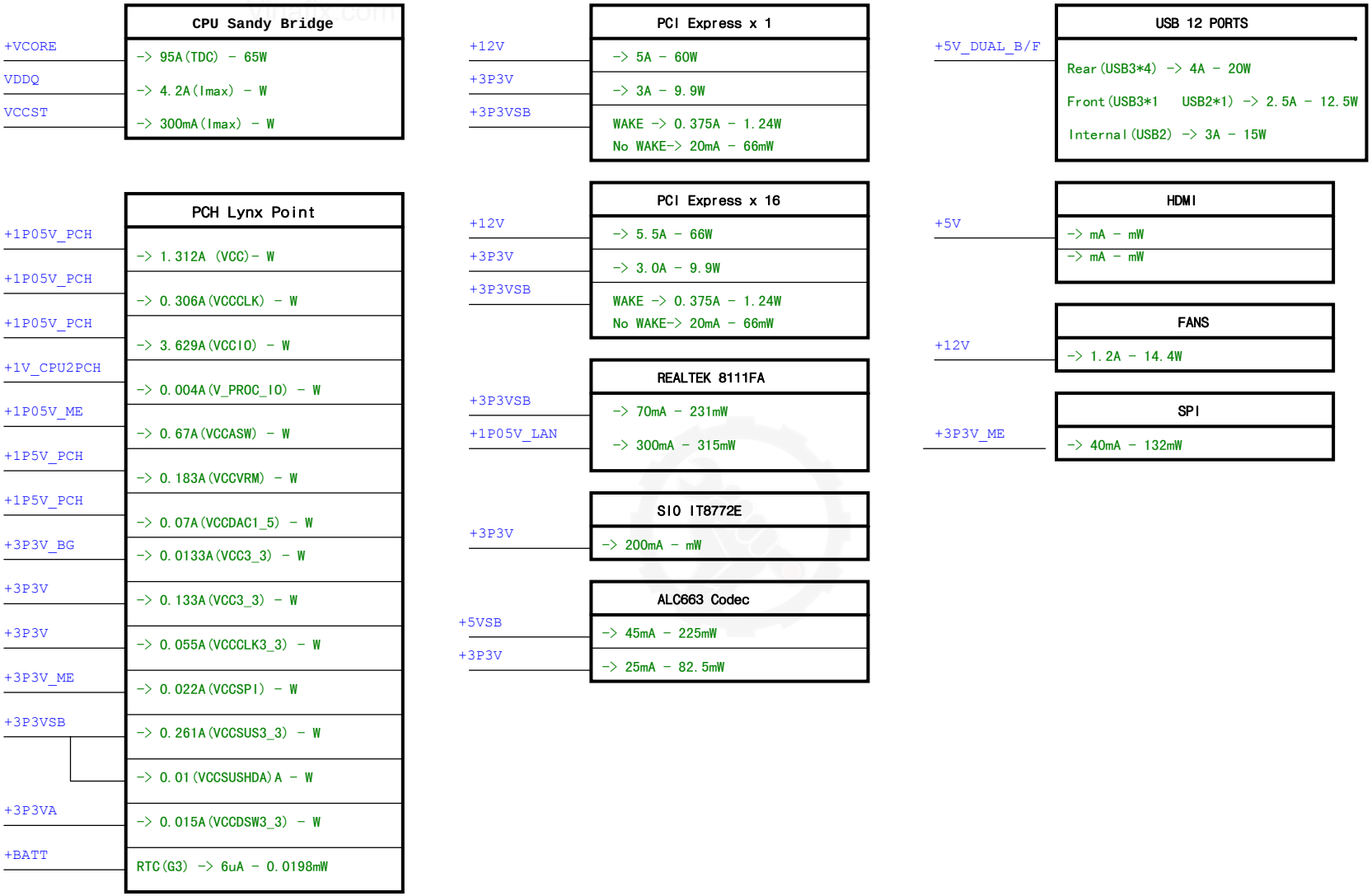

PEGATRON	Title : POWER DISTRIBUTION	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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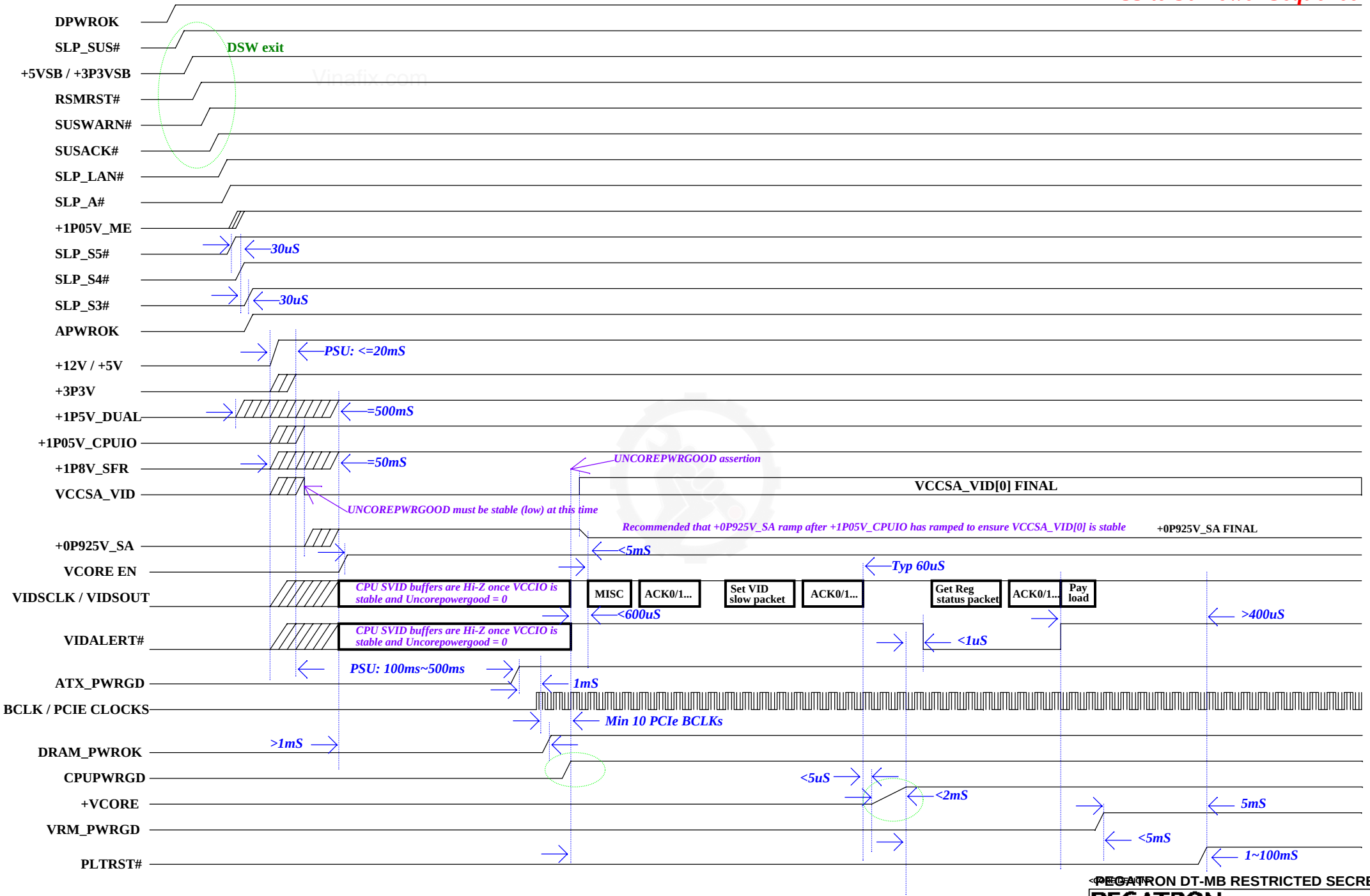
S5 to S0 Power Sequence



PEGATRON	Title : POWER SEQUENCE	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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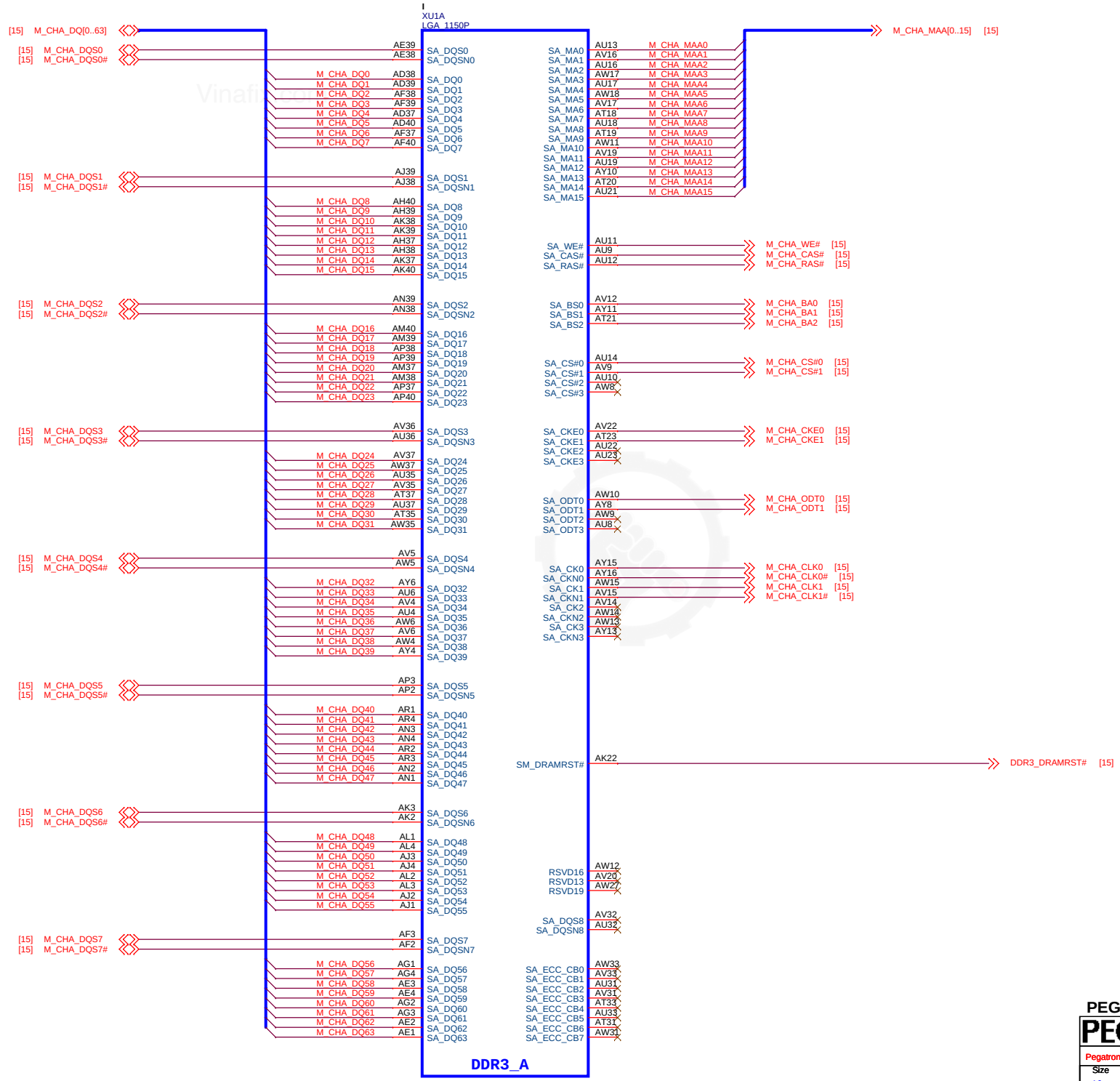

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3_A 1-6	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size A3	Project Name IPPLP-TH	Rev A00
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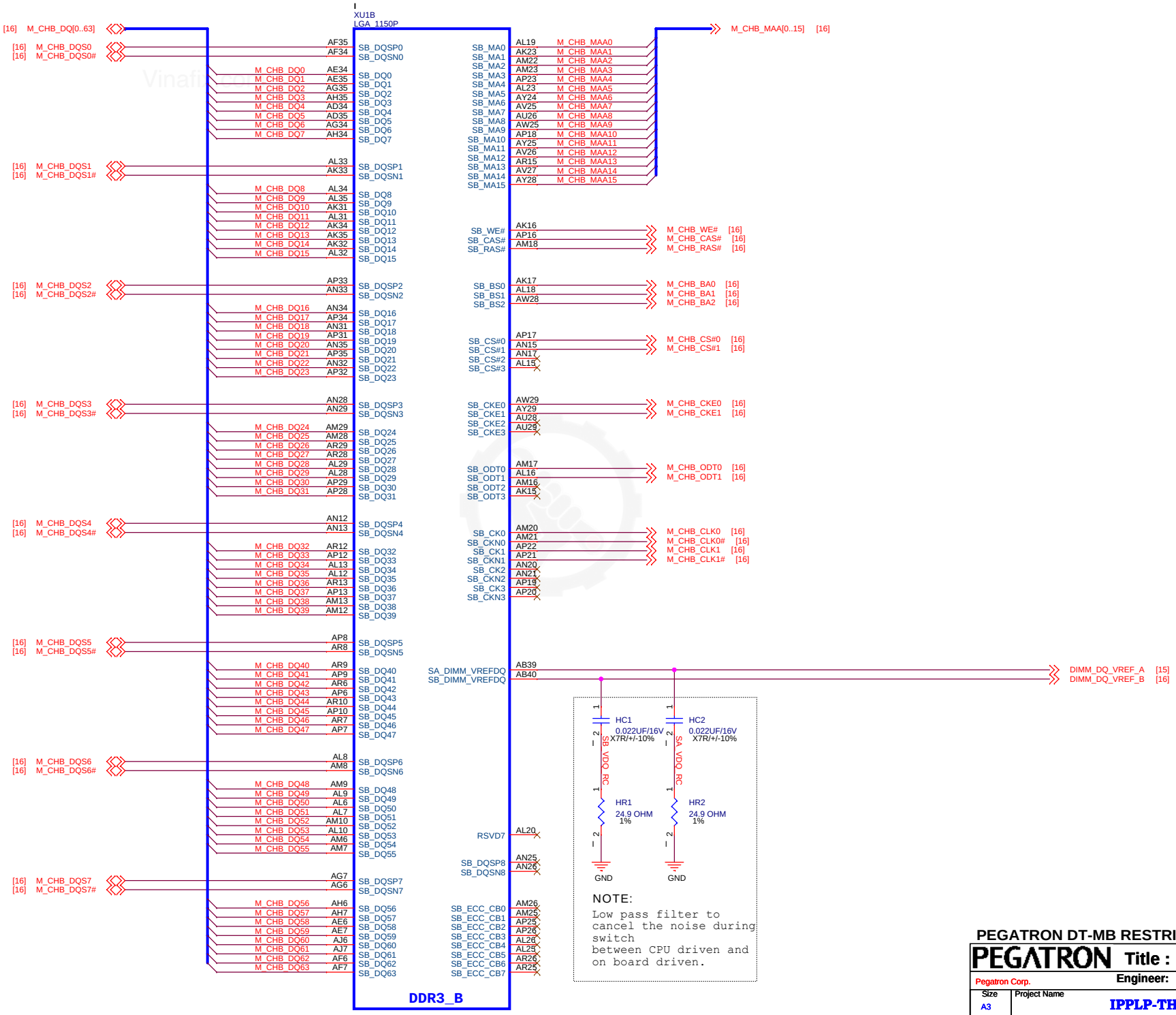

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3_B 2-6		
Pegatron Corp.	Engineer: Shrek_Tseng		
Size: A3	Project Name: IPPLP-TH		Rev: A00
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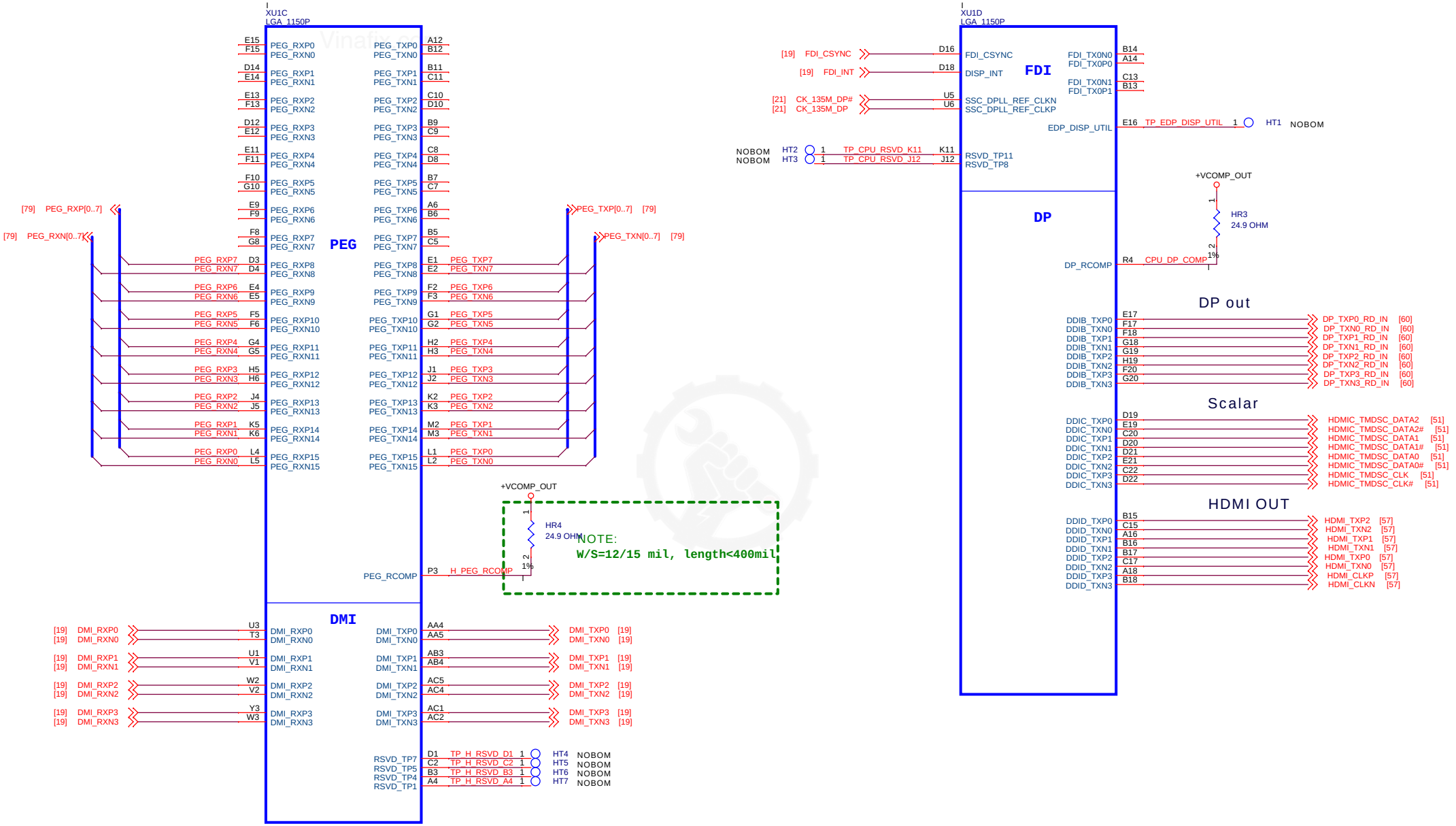

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	PCIE/DMI/DP 3-6
Pegatron Corp.	Engineer:	Shrek_Tseng
Size: A3	Project Name: IPPLP-TH	Rev: A00
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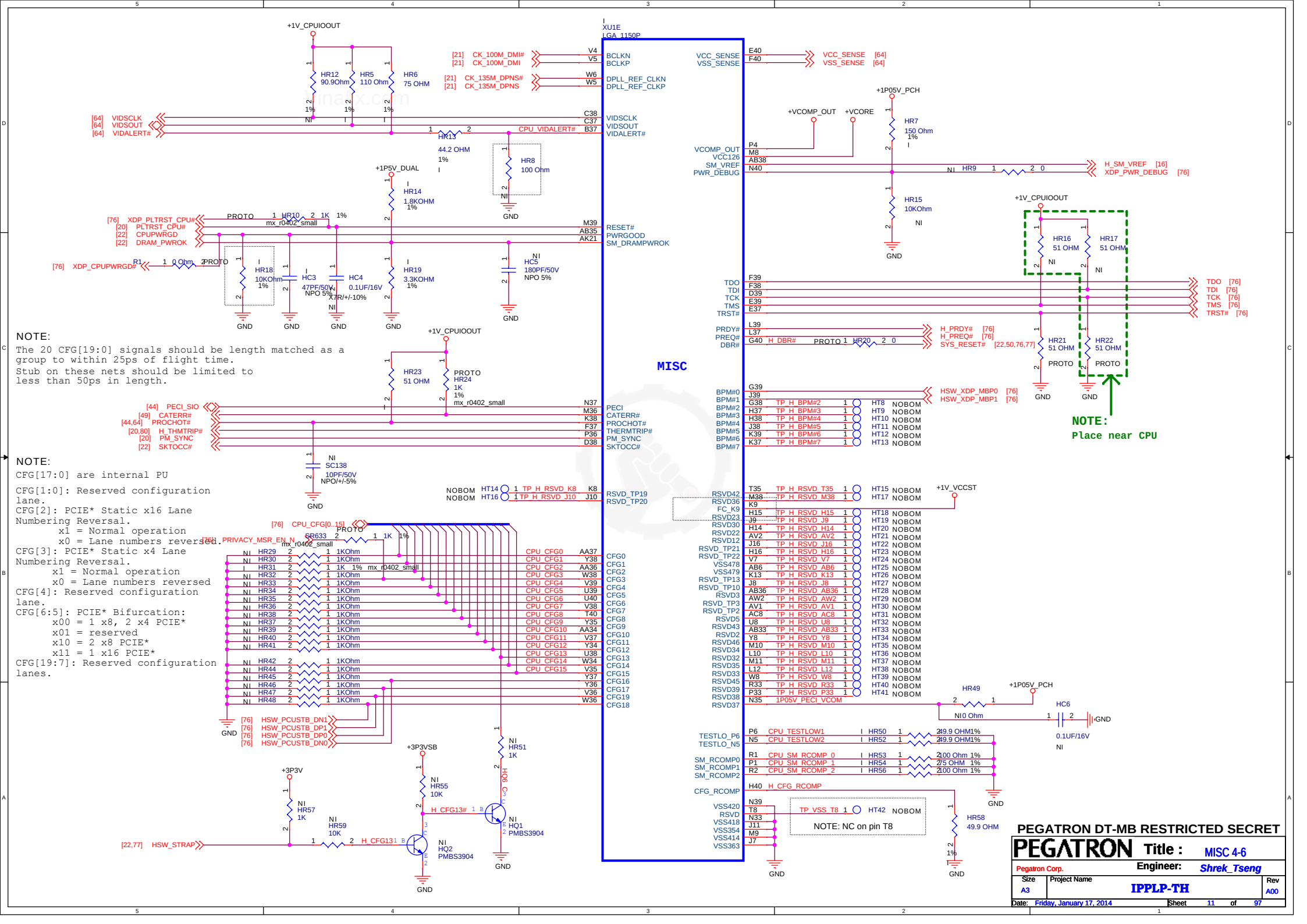
XU1E
LGA_1150P
MISC
+1V_CPUIOOUT
+1P05V_PCH
+1P5V_DUAL
+3P3V
+3P3VSB
+1V_VCCST
GND
NOTE:
The 20 CFG[19:0] signals should be length matched as a group to within 25ps of flight time.
Stub on these nets should be limited to less than 50ps in length.
NOTE:
CFG[17:0] are internal PU
CFG[1:0]: Reserved configuration lane.
CFG[2]: PCIE* Static x16 Lane Numbering Reversal.
x1 = Normal operation
x0 = Lane numbers reversed.
CFG[3]: PCIE* Static x4 Lane Numbering Reversal.
x1 = Normal operation
x0 = Lane numbers reversed
CFG[4]: Reserved configuration lane.
CFG[6:5]: PCIE* Bifurcation:
x00 = 1 x8, 2 x4 PCIE*
x01 = reserved
x10 = 2 x8 PCIE*
x11 = 1 x16 PCIE*
CFG[19:7]: Reserved configuration lanes.
NOTE:
Place near CPU
NOTE: NC on pin T8
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : MISC 4-6
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev A00
Date: Friday, January 17, 2014
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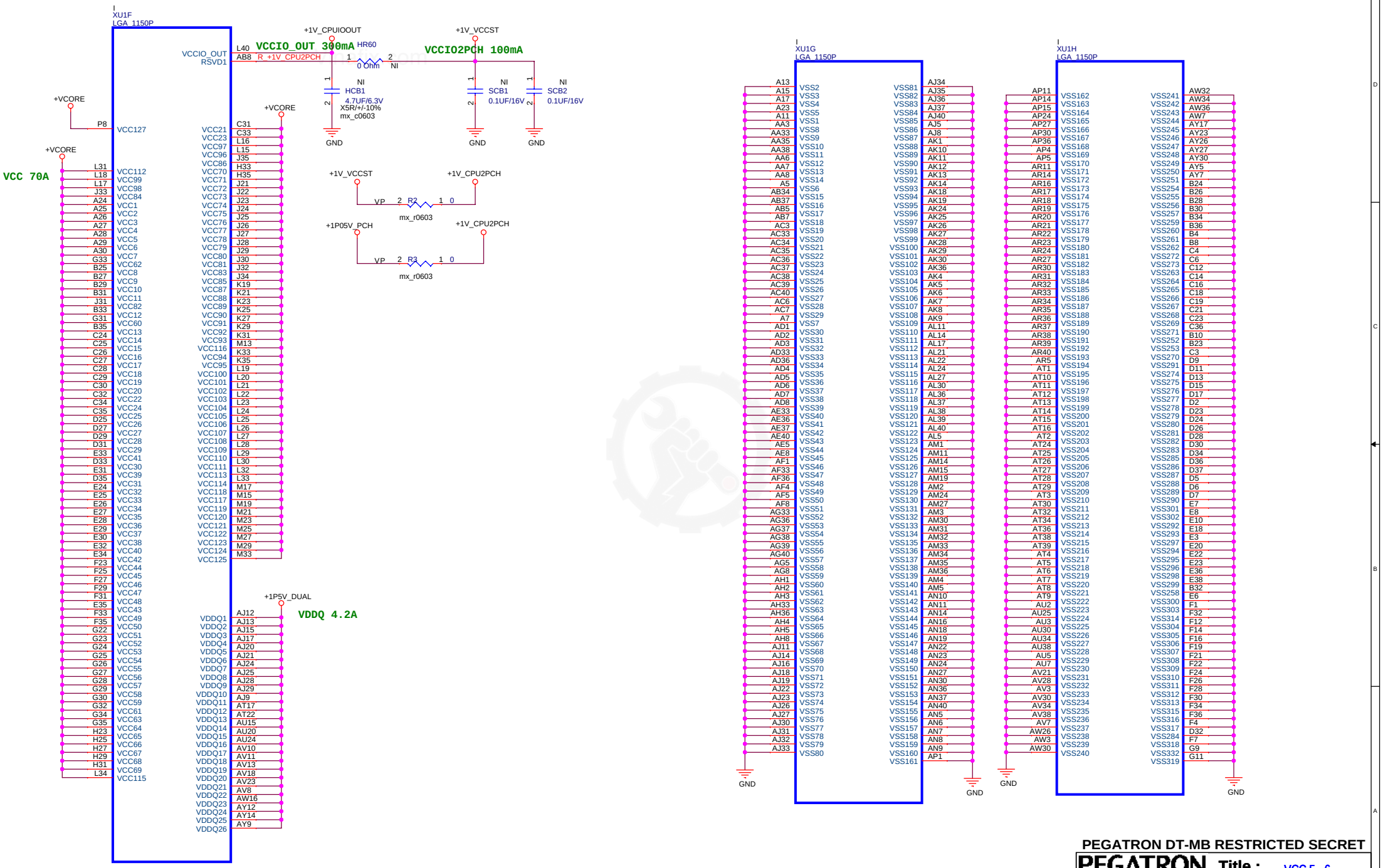

PEGATRON Title : VCC 5 - 6

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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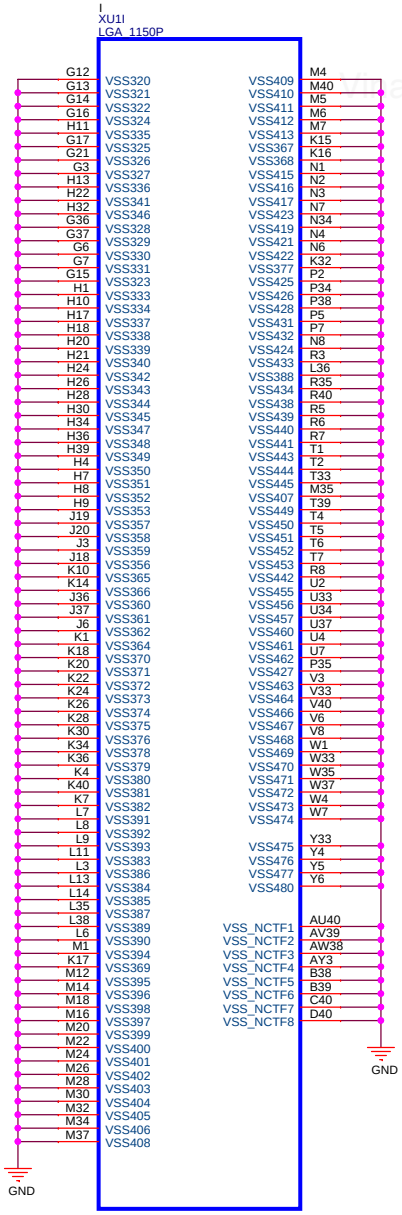
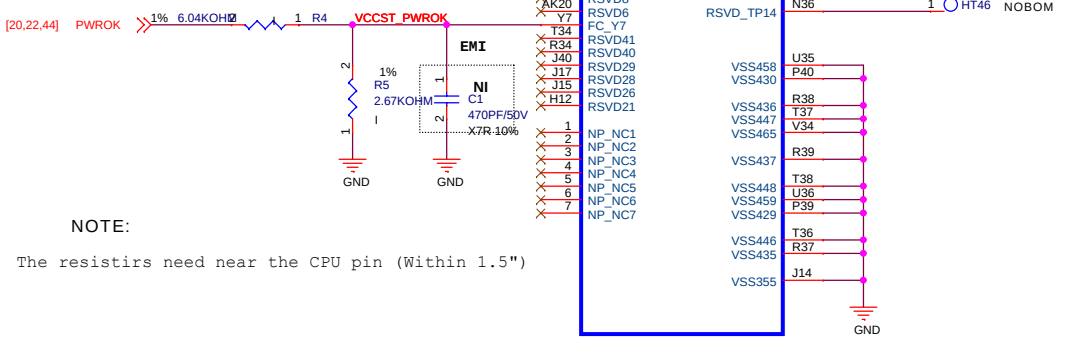
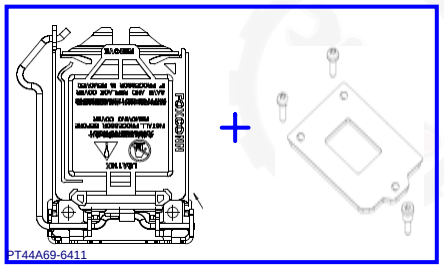
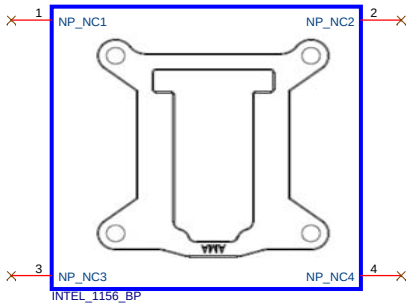




NOTE:

The resistirs need near the CPU pin (Within 1.5")





NOTE: (CPU)

	Standard
Part	PE115027_4041_01F_INTEL
Symbol	mx_socket_1150p (with 4 screws)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 6 - 6

Pegatron Corp. Engineer: Shrek_Tseng

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A3	IPPLP-TH	A00

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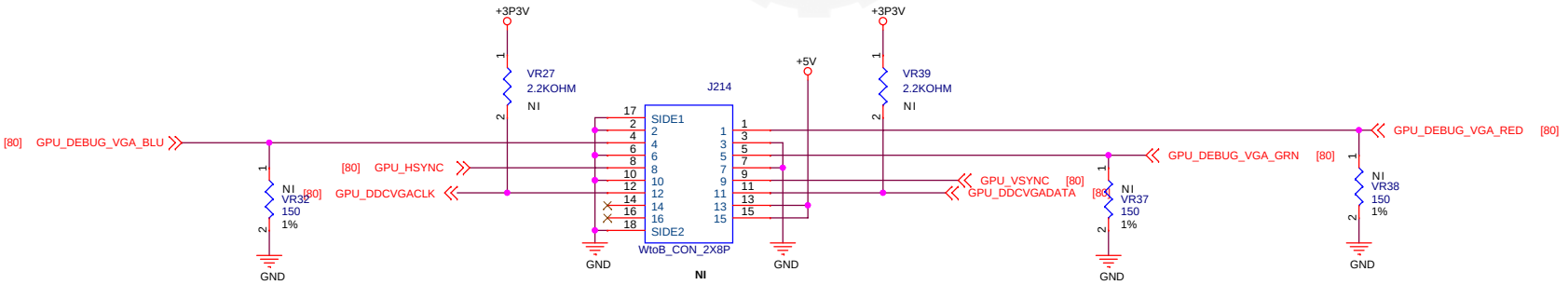

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VGA DEBUG	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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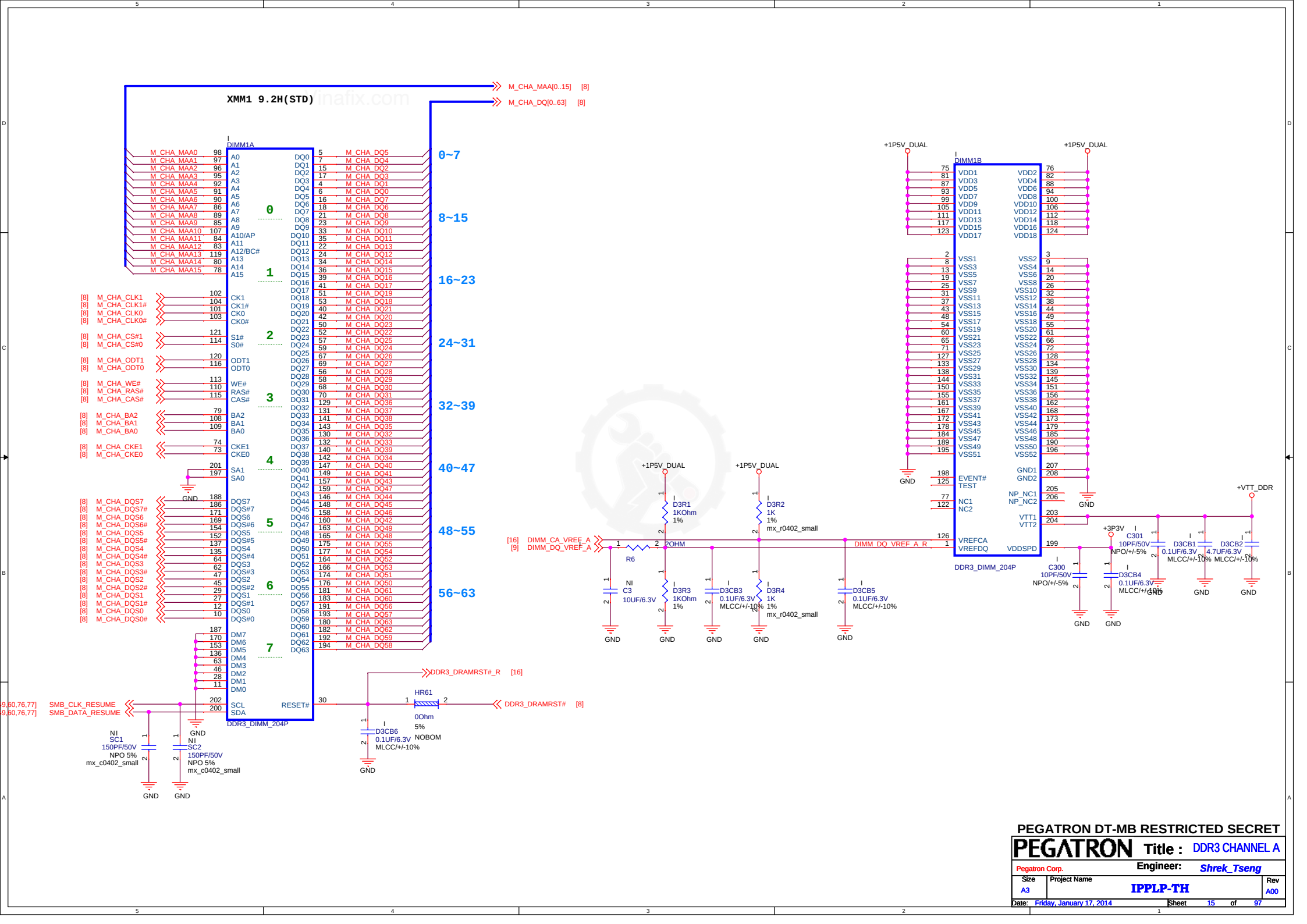

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 CHANNEL A

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
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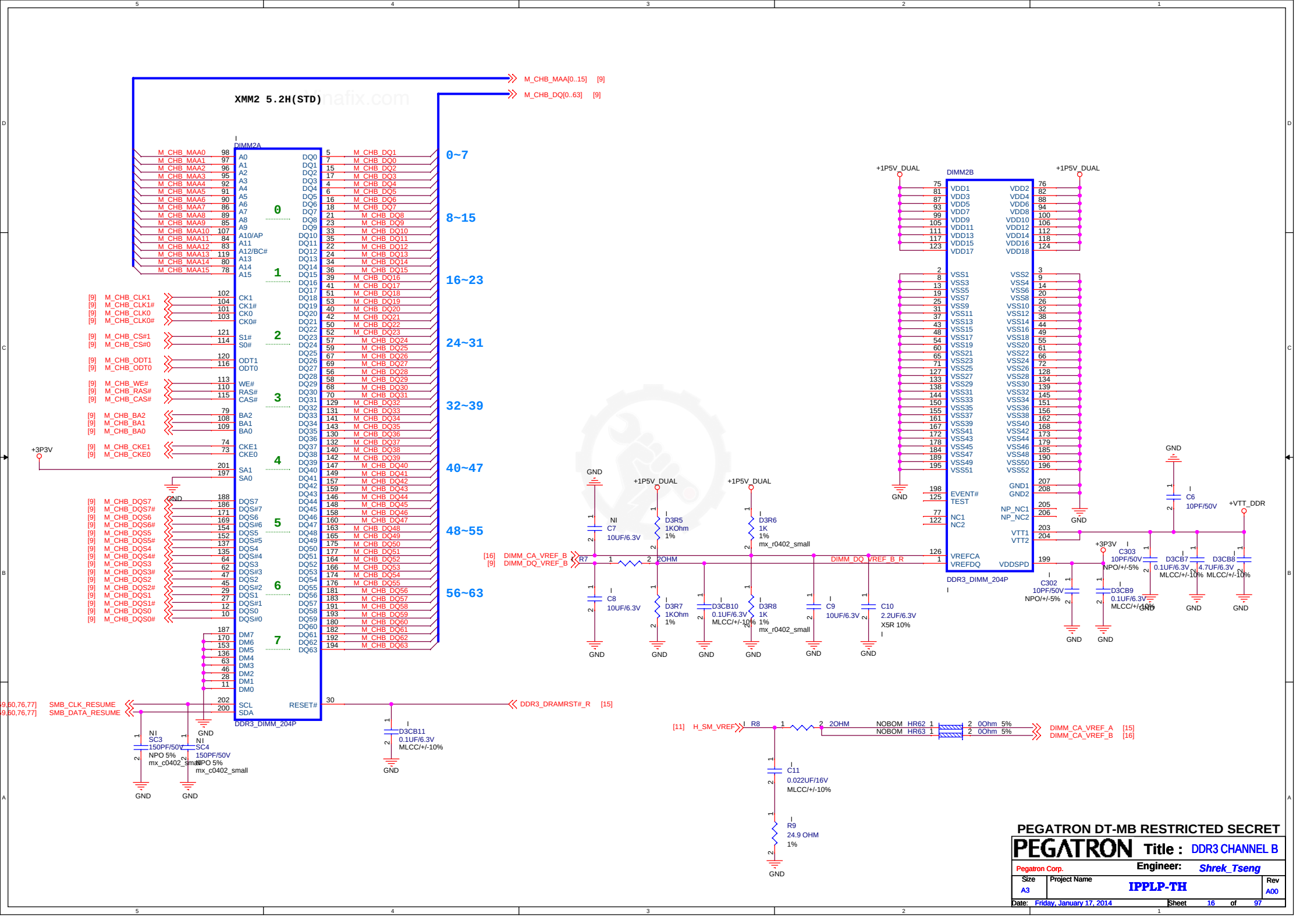
XMM2 5.2H(STD)
M_CHB_MAA[0..15] [9]
M_CHB_DQ[0..63] [9]
DIMM2A
DDR3_DIMM_204P
0~7
8~15
16~23
24~31
32~39
40~47
48~55
56~63
DIMM2B
DDR3_DIMM_204P
+3P3V
+1P5V_DUAL
GND
+VTT_DDR
SMB_CLK_RESUME
SMB_DATA_RESUME
RESET#
DDR3_DRAMRST#_R [15]
H_SM_VREF
DIMM_CA_VREF_A [15]
DIMM_CA_VREF_B [16]
DIMM_CA_VREF_B [16]
DIMM_DQ_VREF_B [9]
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : DDR3 CHANNEL B
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev A00
Date: Friday, January 17, 2014
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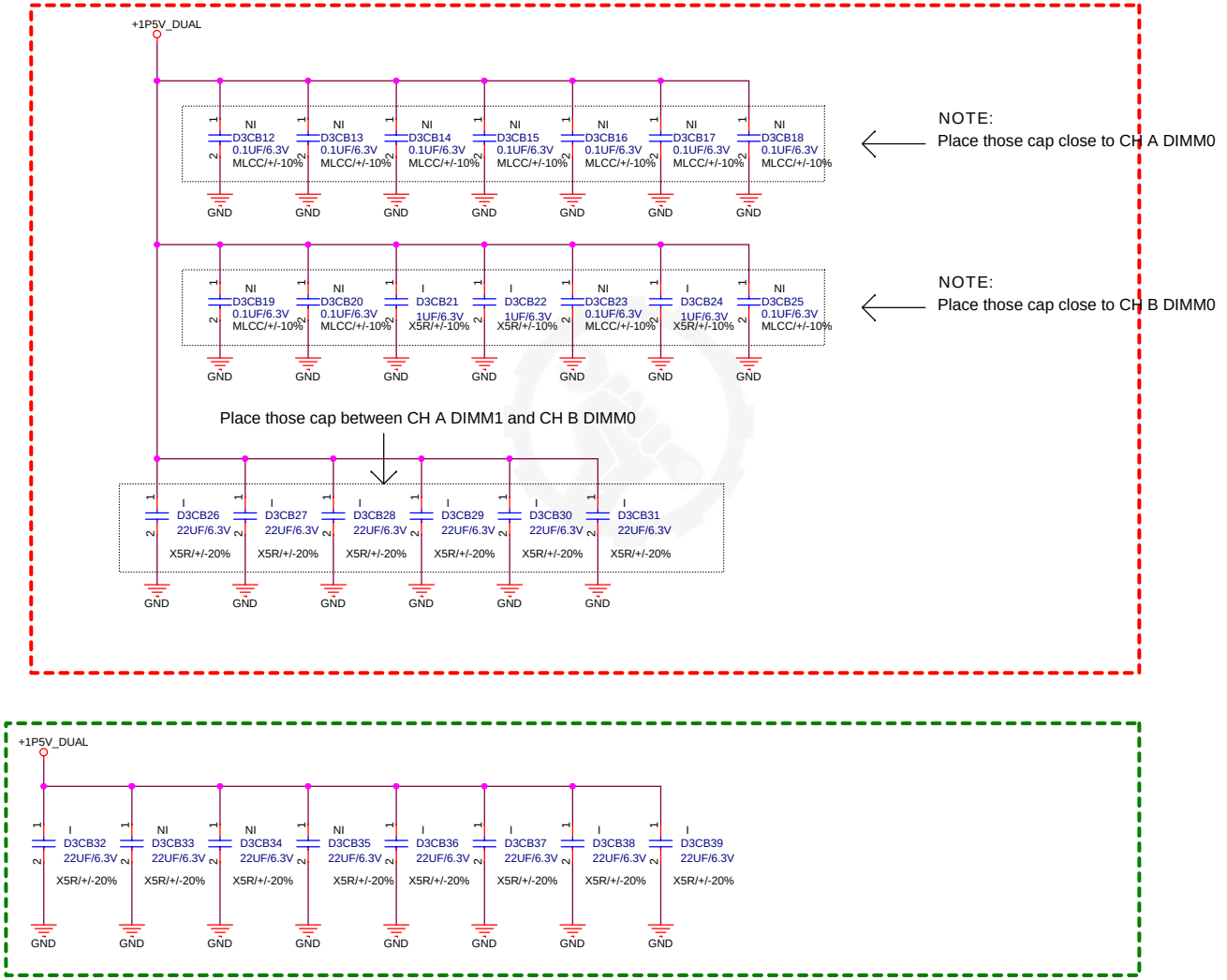

Place those cap inside CPU SOCKET cavity

PEGATRON Title : DDR3 TERMINATION

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : XXXXXX	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
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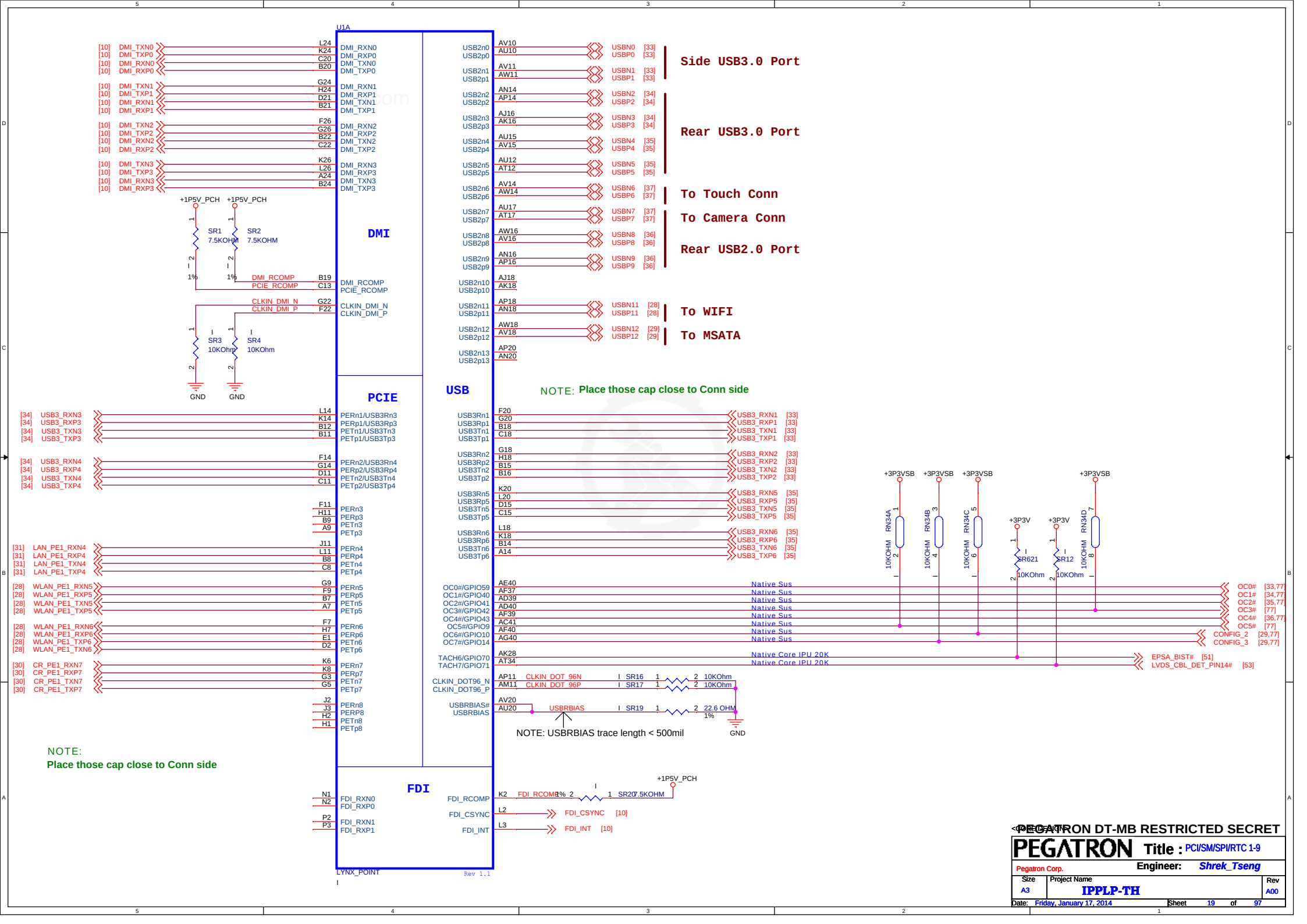
U1A
DMI
PCIE
USB
FDI
LYNX_POINT
Rev 1.1
Side USB3.0 Port
Rear USB3.0 Port
To Touch Conn
To Camera Conn
Rear USB2.0 Port
To WIFI
To MSATA
NOTE: Place those cap close to Conn side
NOTE: USBRBIAS trace length < 500mil
NOTE:
Place those cap close to Conn side
GND
+1P5V_PCH
+3P3VSB
+3P3V
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCI/SM/SPI/RTC 1-9
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev A00
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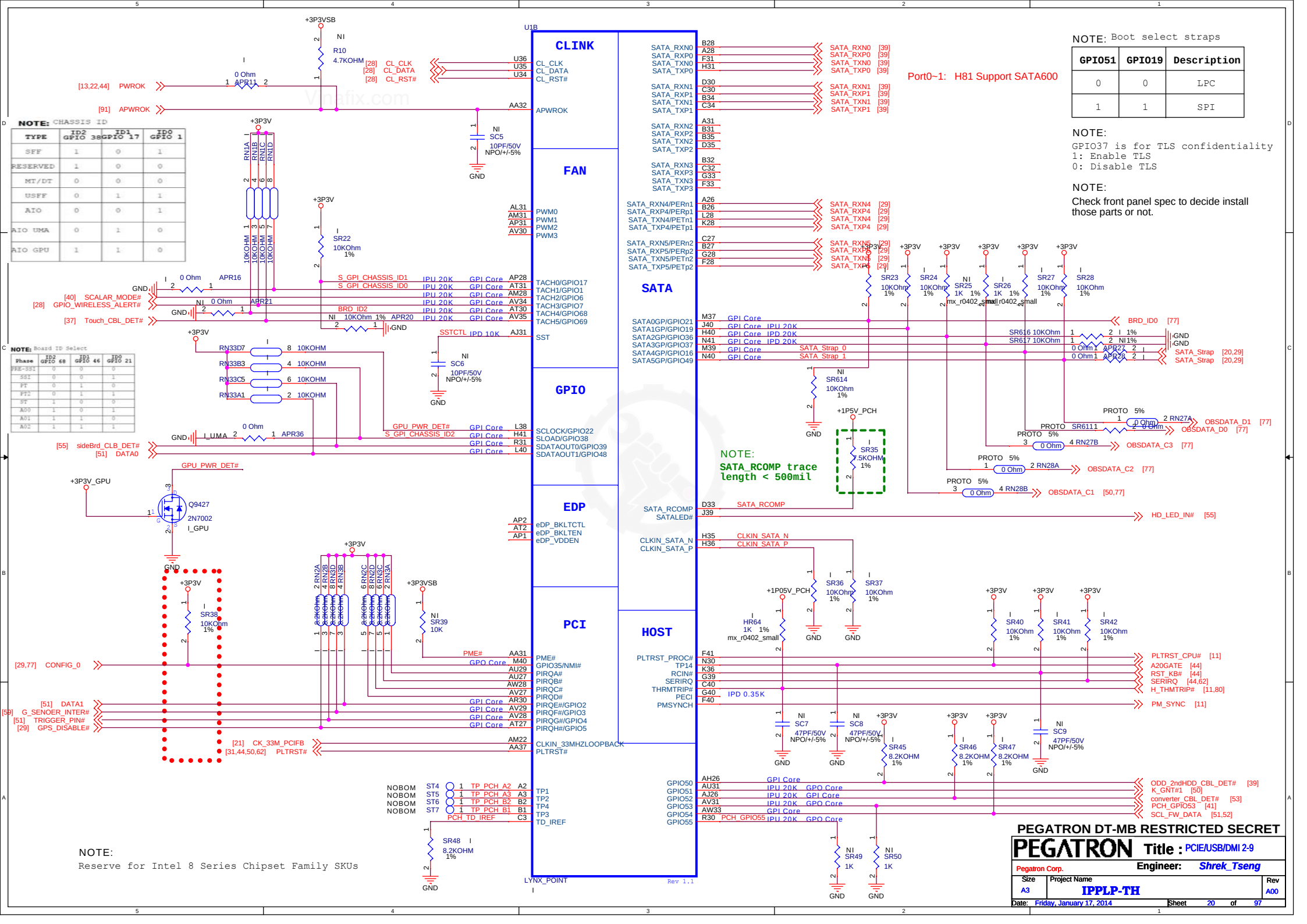

NOTE: CHASSIS ID

TYPE	ID2 GPIO 38	ID1 GPIO 17	ID0 GPIO 1
SFF	1	0	1
RESERVED	1	0	0
MT/DT	0	0	0
USFF	0	1	1
AIO	0	0	1
AIO UMA	0	1	0
AIO GPU	1	1	0

NOTE: Board ID Select

Phase	ID2 GPIO 68	ID1 GPIO 46	ID0 GPIO 21
PRE-SSI	0	0	0
SSI	0	0	1
PT	0	1	0
PT2	0	1	1
ST	1	0	0
A00	1	0	1
A01	1	1	0
A02	1	1	1

NOTE: Boot select straps

GPIO51	GPIO19	Description
0	0	LPC
1	1	SPI

NOTE:
GPIO37 is for TLS confidentiality
1: Enable TLS
0: Disable TLS

NOTE:
Check front panel spec to decide install those parts or not.

NOTE:
Reserve for Intel 8 Series Chipset Family SKUs

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/USB/DMI 2-9

Pegatron Corp. Engineer: Shrek_Tseng

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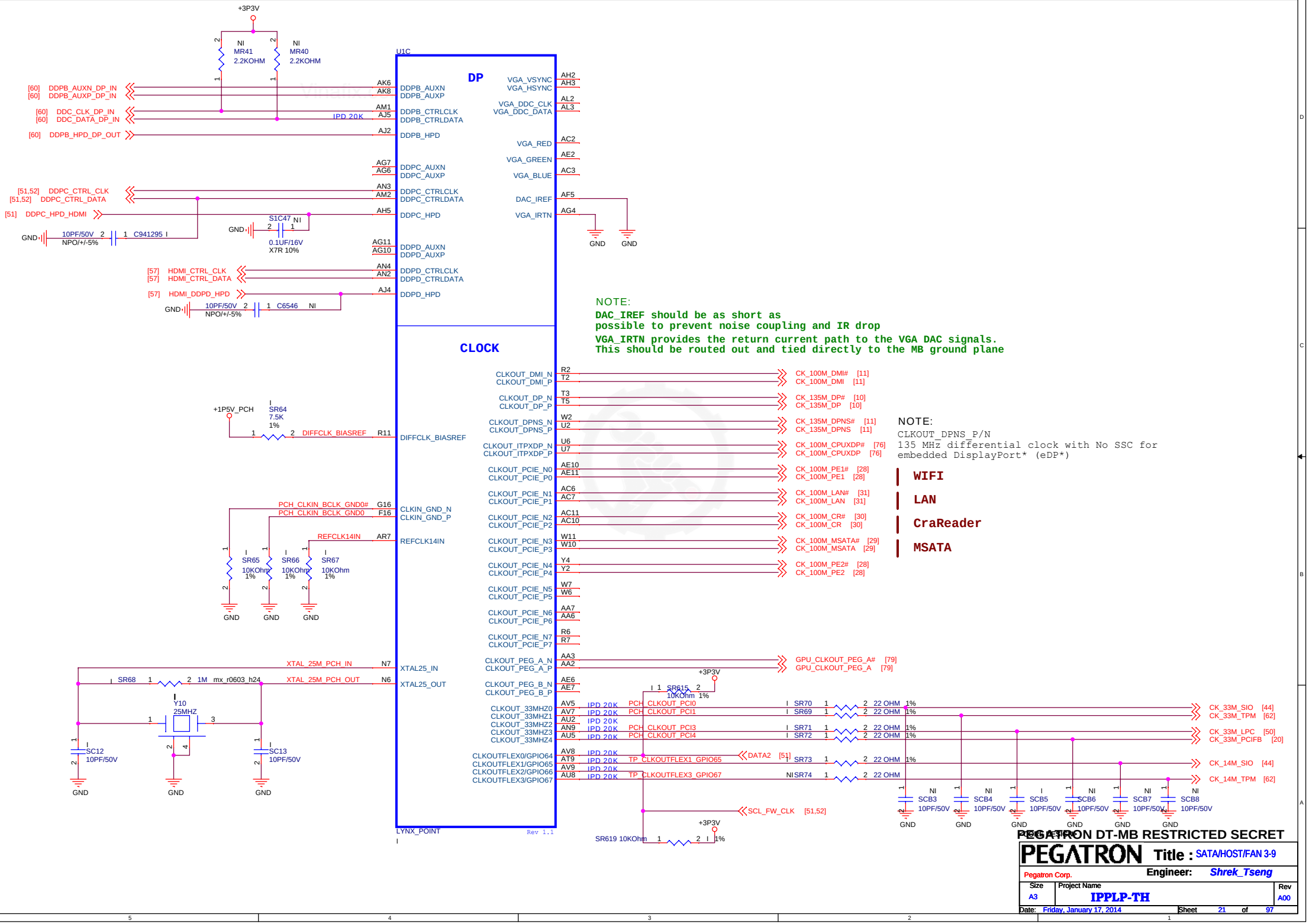
U1C
DP
CLOCK
LYNX_POINT
Rev 1.1
+3P3V
NI MR41 2.2KOHM
NI MR40 2.2KOHM
[60] DDPB_AUXN_DP_IN
[60] DDPB_AUXP_DP_IN
[60] DDC_CLK_DP_IN
[60] DDC_DATA_DP_IN
[60] DDPB_HPD_DP_OUT
IPD 20K
DDPB_AUXN
DDPB_AUXP
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPB_HPD
[51,52] DDPC_CTRL_CLK
[51,52] DDPC_CTRL_DATA
[51] DDPC_HPD_HDMI
10PF/50V NPO/+/-5% C941295
S1C47 NI 0.1UF/16V X7R 10%
DDPC_AUXN
DDPC_AUXP
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_HPD
[57] HDMI_CTRL_CLK
[57] HDMI_CTRL_DATA
[57] HDMI_DDPD_HPD
10PF/50V NPO/+/-5% C6546 NI
DDPD_AUXN
DDPD_AUXP
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_HPD
VGA_VSYNC
VGA_HSYNC
VGA_DDC_CLK
VGA_DDC_DATA
VGA_RED
VGA_GREEN
VGA_BLUE
DAC_IREF
VGA_IRTN
GND
NOTE:
DAC_IREF should be as short as possible to prevent noise coupling and IR drop
VGA_IRTN provides the return current path to the VGA DAC signals. This should be routed out and tied directly to the MB ground plane
+1P5V_PCH
SR64 7.5K 1%
DIFFCLK_BIASREF
PCH_CLKIN_BCLK_GND0#
PCH_CLKIN_BCLK_GND0
CLKIN_GND_N
CLKIN_GND_P
REFCLK14IN
SR65 10KOhm 1%
SR66 10KOhm 1%
SR67 10KOhm 1%
XTAL_25M_PCH_IN
XTAL_25M_PCH_OUT
SR68 1M mx r0603 h24
Y10 25MHZ
SC12 10PF/50V
SC13 10PF/50V
XTAL25_IN
XTAL25_OUT
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CK_100M_DMI# [11]
CK_100M_DMI [11]
CK_135M_DP# [10]
CK_135M_DP [10]
CK_135M_DPNS# [11]
CK_135M_DPNS [11]
CK_100M_CPUXDP# [76]
CK_100M_CPUXDP [76]
CK_100M_PE1# [28]
CK_100M_PE1 [28]
CK_100M_LAN# [31]
CK_100M_LAN [31]
CK_100M_CR# [30]
CK_100M_CR [30]
CK_100M_MSATA# [29]
CK_100M_MSATA [29]
CK_100M_PE2# [28]
CK_100M_PE2 [28]
NOTE:
CLKOUT_DPNS_P/N
135 MHz differential clock with No SSC for embedded DisplayPort* (eDP*)
WIFI
LAN
CraReader
MSATA
GPU_CLKOUT_PEG_A# [79]
GPU_CLKOUT_PEG_A [79]
PCH_CLKOUT_PCI0
PCH_CLKOUT_PCI1
PCH_CLKOUT_PCI3
PCH_CLKOUT_PCI4
SR70 22 OHM 1%
SR69 22 OHM 1%
SR71 22 OHM 1%
SR72 22 OHM 1%
CK_33M_SIO [44]
CK_33M_TPM [62]
CK_33M_LPC [50]
CK_33M_PCIFB [20]
DATA2 [51]
TP_CLKOUTFLEX1_GPIO65
SR73 22 OHM 1%
TP_CLKOUTFLEX3_GPIO67
SR74 22 OHM 1%
CK_14M_SIO [44]
CK_14M_TPM [62]
SCB3 10PF/50V
SCB4 10PF/50V
SCB5 10PF/50V
SCB6 10PF/50V
SCB7 10PF/50V
SCB8 10PF/50V
SR615 10KOhm 1%
SCL_FW_CLK [51,52]
SR619 10KOhm 1%
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : SATA/HOST/FAN 3-9
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
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Date: Friday, January 17, 2014
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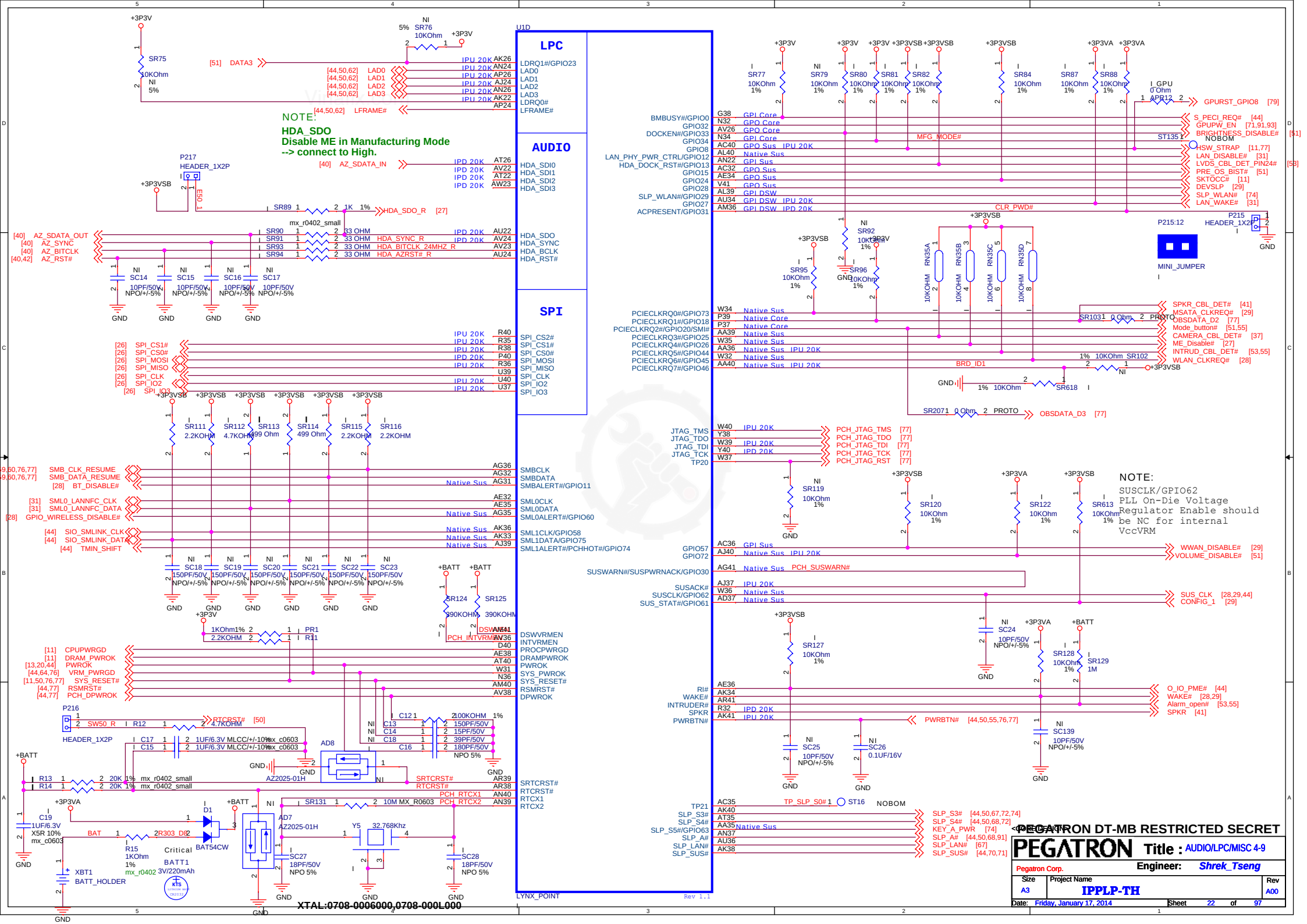
U1D
LPC
AUDIO
SPI
LYNX_POINT
Rev 1.1
NOTE:
HDA_SDO
Disable ME in Manufacturing Mode
--> connect to High.
XTAL:0708-0006000,0708-000L000
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : AUDIO/LPC/MISC 4-9
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev A00
Date: Friday, January 17, 2014
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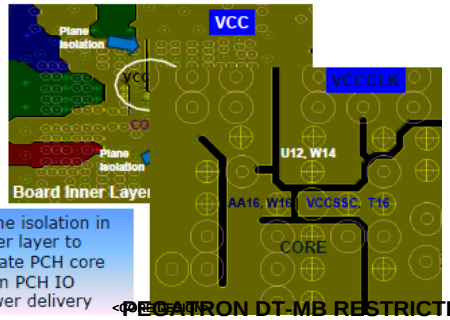
NOTE:
Backup 09X241023060 1UH/300mA(0805)
and install 10uF for External VRM

NOTE:
Backup 09X241031260 10UH/125mA(0805)
and install 10uF/1Ω for External VRM

NOTE:
Pin AF19, AF20, AF22, AF23 are connected to on bottom layer only. Not connected on VCC layer to avoid noise coupling.

NOTE:
Caps can be removed on DcpSus (pin AE30, P19 and AJ22) if Internal VRM is used.

NOTE:
PCH power plane isolation



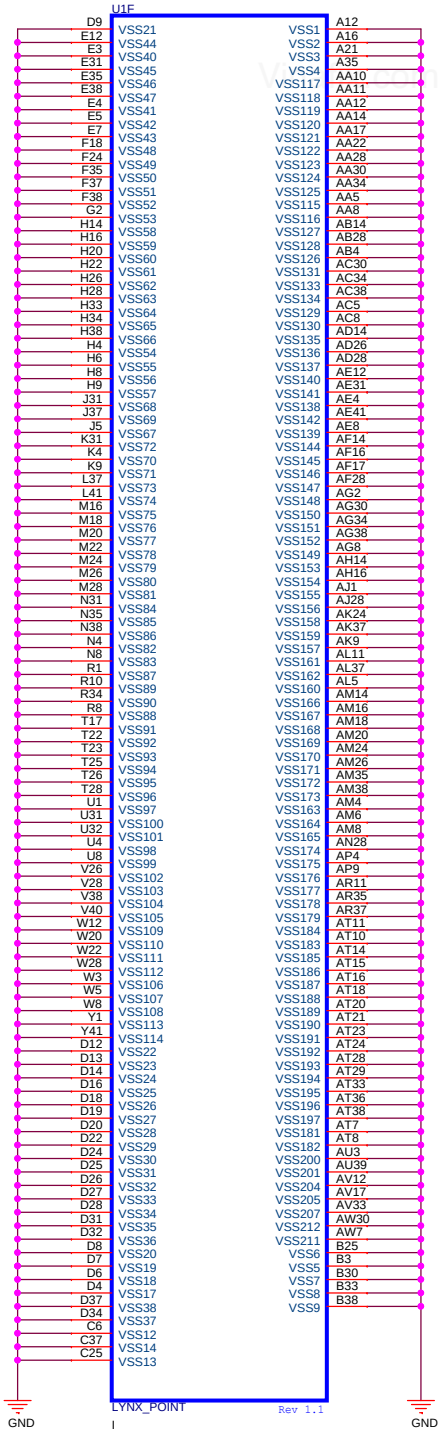
Plane isolation in inner layer to isolate PCH core from PCH IO power delivery

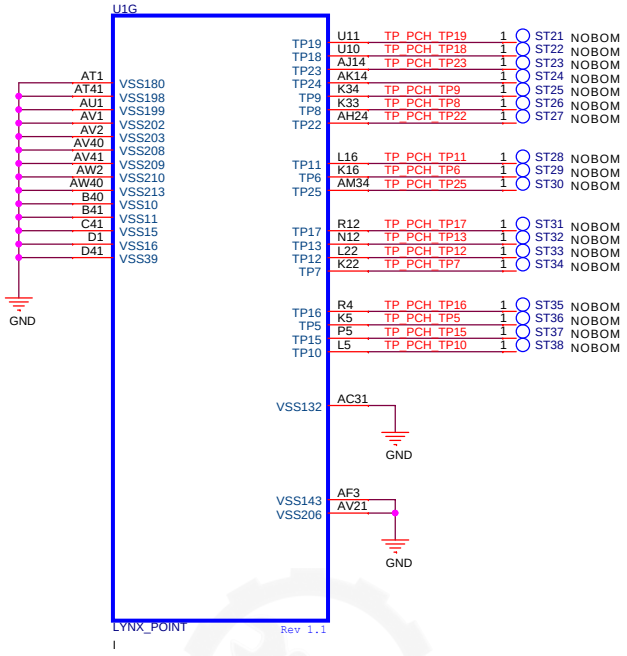
PEGATRON Title : VGA/DP/HDMI 5-9

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

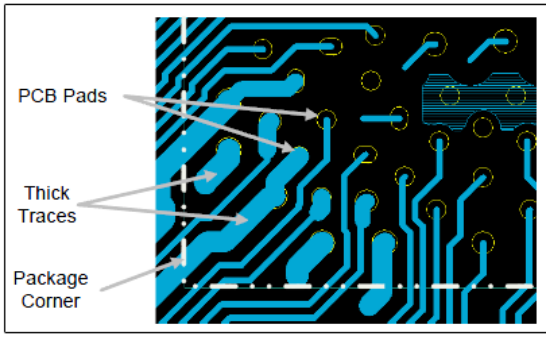
Date: Friday, January 17, 2014 Sheet 23 of 97





Remove Heatsink

NOTE: Solder Pad Recommendation



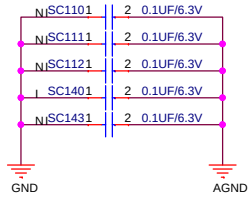
PEGATRON DT-MB RESTRICTED SECRET

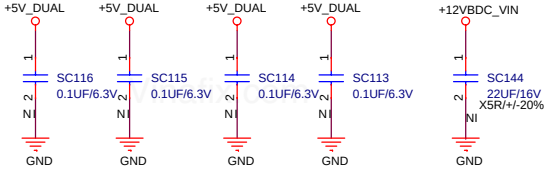
PEGATRON Title : CLK/NVRAM/FDI 6-9

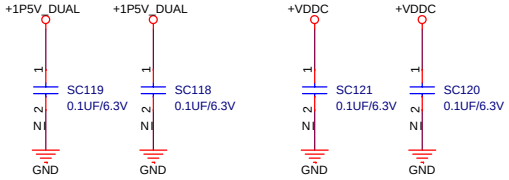
Pegatron Corp. Engineer: Shrek_Tseng

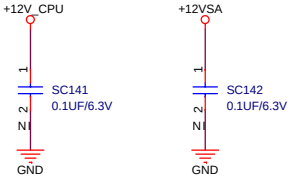
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 24 of 97







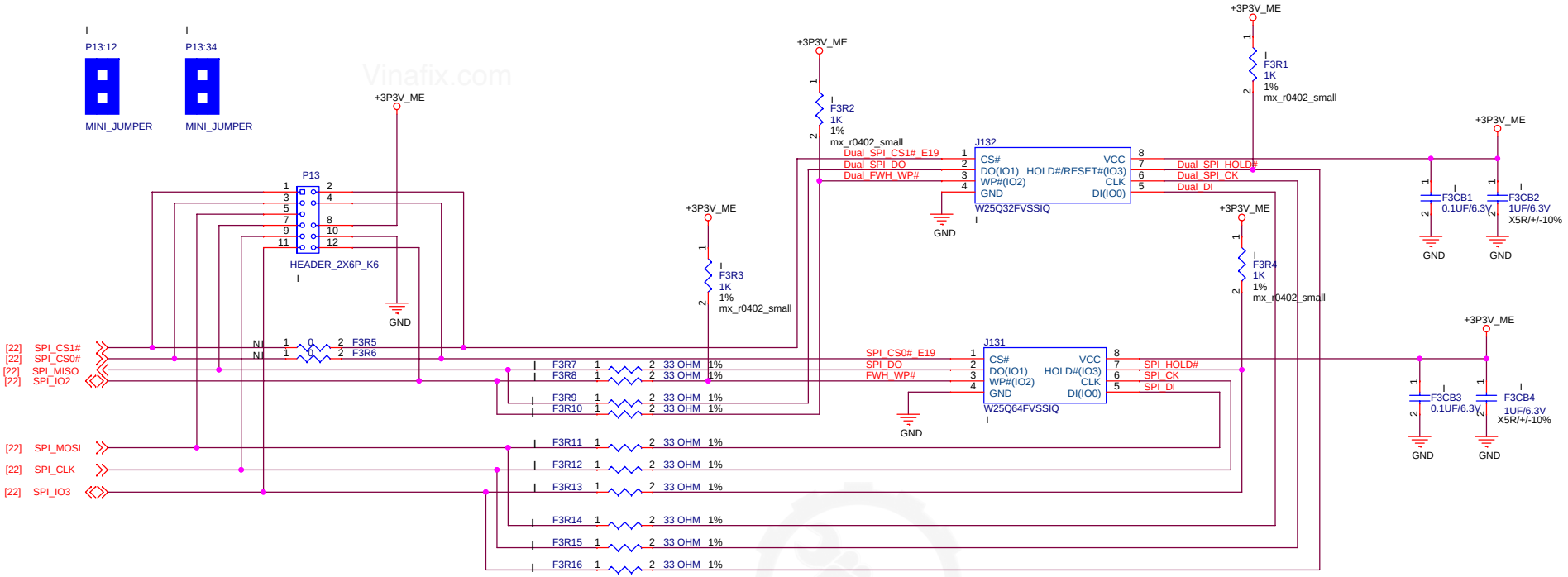


PEGATRON Title : PCH_DPWROK & SLP_SUS

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

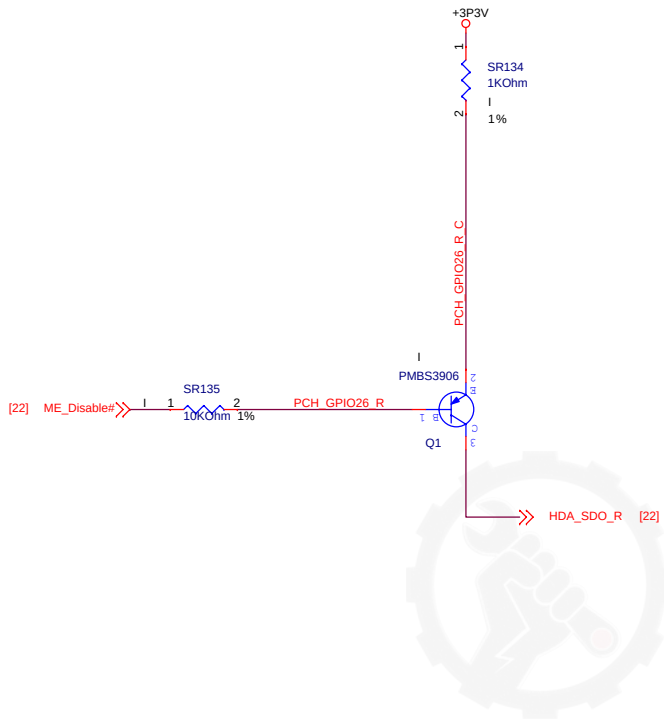
Date: Friday, January 17, 2014 Sheet 25 of 97



PEGATRON DT-MB RESTRICTED SECRET

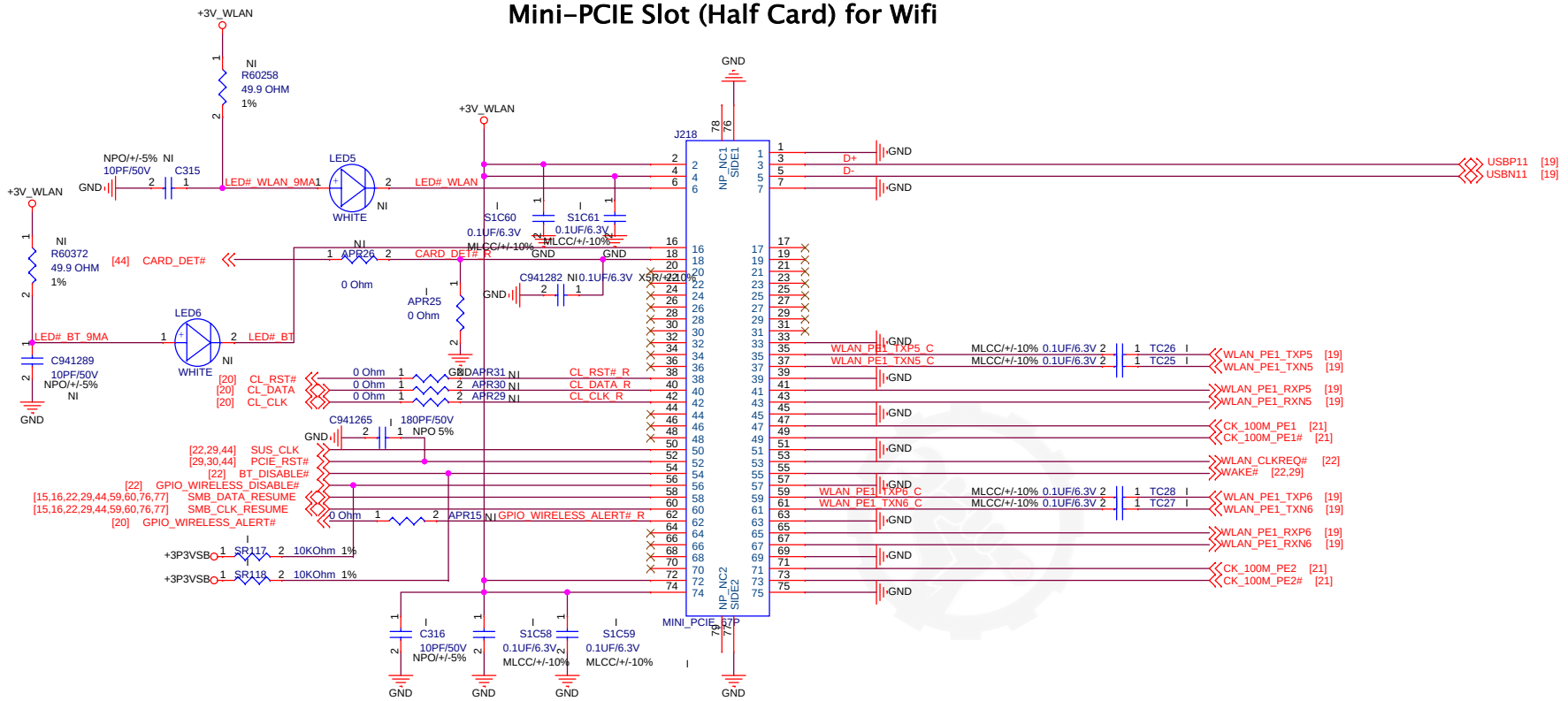
PEGATRON	Title :	SM BUS & SPI ROM
Pegatron Corp.	Engineer:	Shrek_Tseng
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 26 of 93	

ME Disable

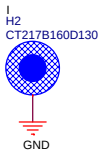


PEGATRON	Title : ME DISABLE	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 27 of 97	

Mini-PCIE Slot (Half Card) for Wifi



H=4mm



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : NGFF KEY A(WLAN)

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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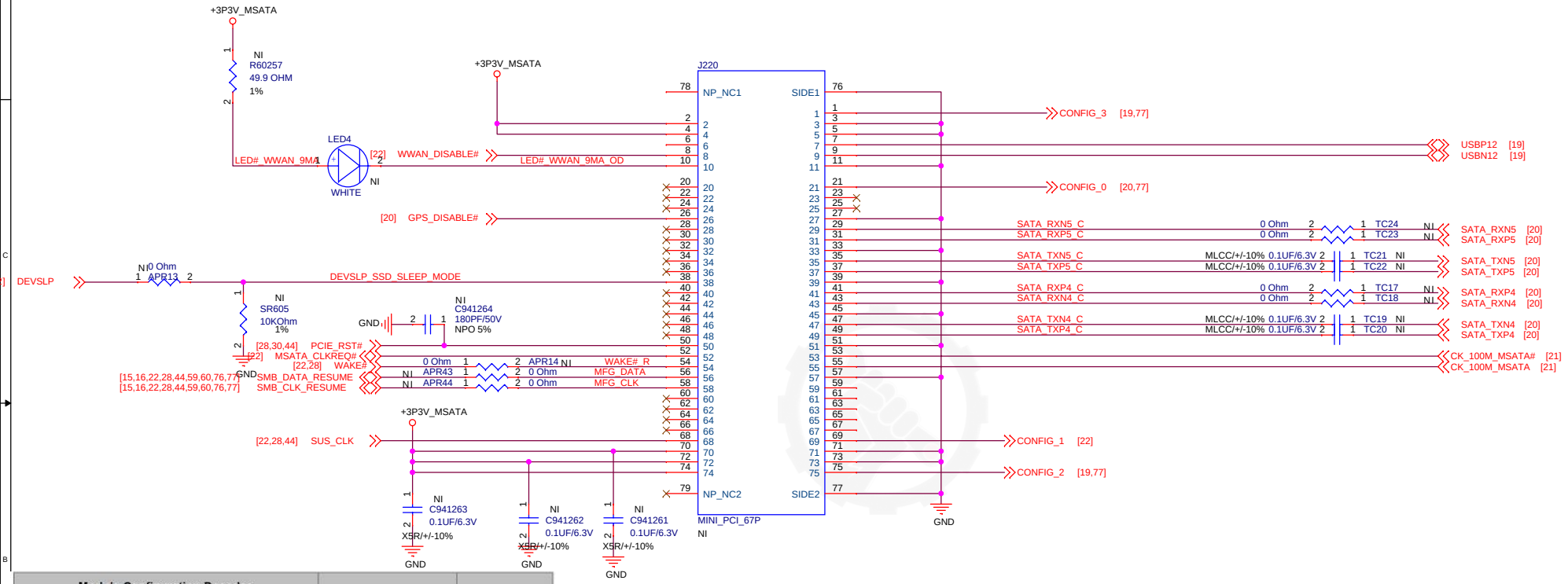

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
GND	GND	GND	GND	SSD – SATA	N/A
GND	~~NC~~	GND	GND	SSD – PCIe	N/A
GND	GND	~~NC~~	GND	WWAN – PCIe	0
GND	~~NC~~	~~NC~~	GND	WWAN – PCIe	1
GND	GND	GND	~~NC~~	WWAN – USB 3.0	0
GND	~~NC~~	GND	~~NC~~	WWAN – USB 3.0	1
GND	GND	~~NC~~	~~NC~~	WWAN – USB 3.0	2
GND	~~NC~~	~~NC~~	~~NC~~	WWAN – USB 3.0	3
~~NC~~	GND	GND	GND	WWAN – SSIC	0
~~NC~~	~~NC~~	GND	GND	WWAN – SSIC	1
~~NC~~	GND	~~NC~~	GND	WWAN – SSIC	2
~~NC~~	~~NC~~	~~NC~~	GND	WWAN – SSIC	3
~~NC~~	GND	GND	~~NC~~	WWAN – PCIe	2
~~NC~~	~~NC~~	GND	~~NC~~	WWAN – PCIe	3
~~NC~~	GND	~~NC~~	~~NC~~	RFU	N/A
~~NC~~	~~NC~~	~~NC~~	~~NC~~	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)

[2] Applicable to WWAN only

H=4mm

NI
H1
CT217B160D130
GND

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : NGFF KEY B(MSATA)

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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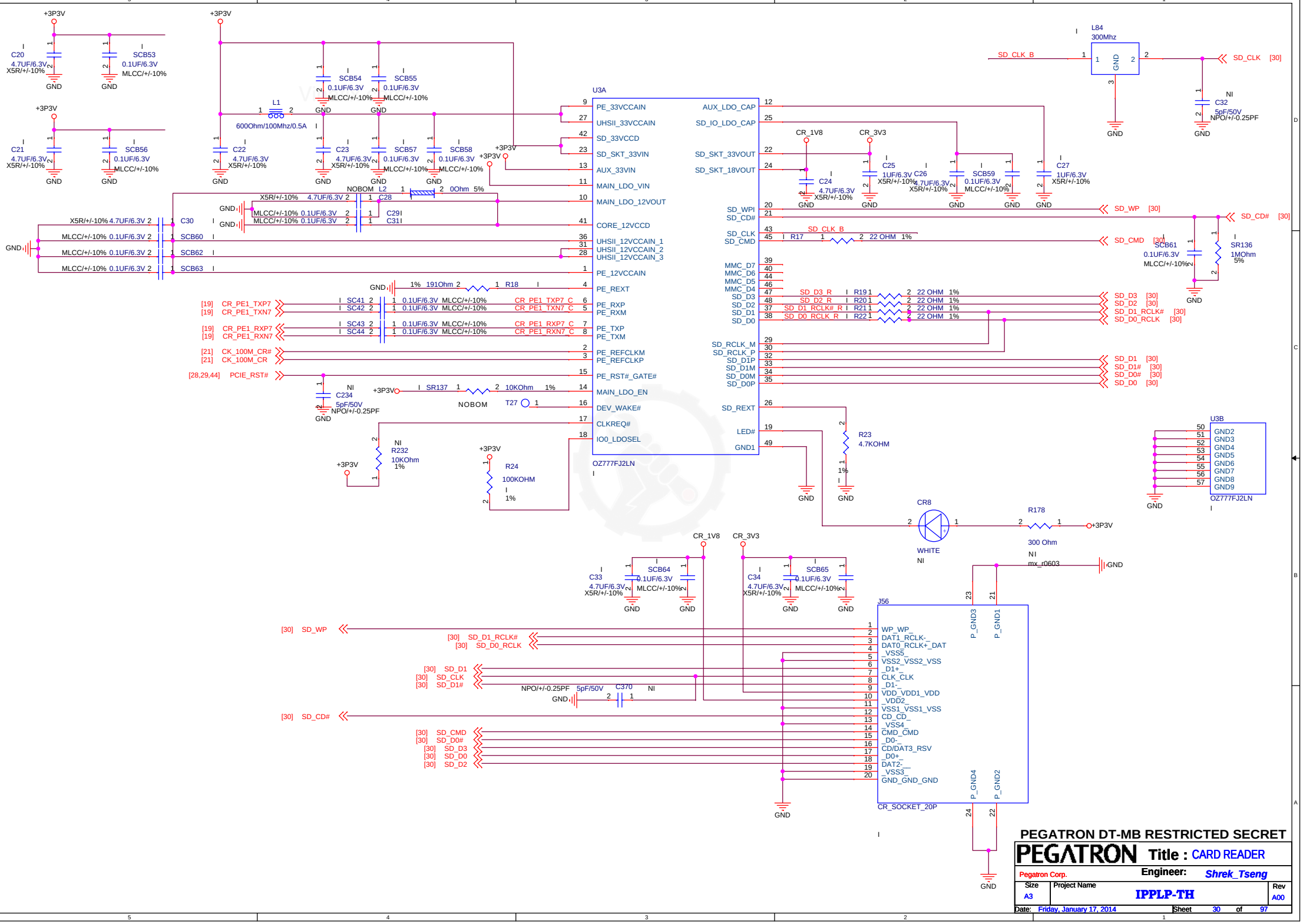

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CARD READER

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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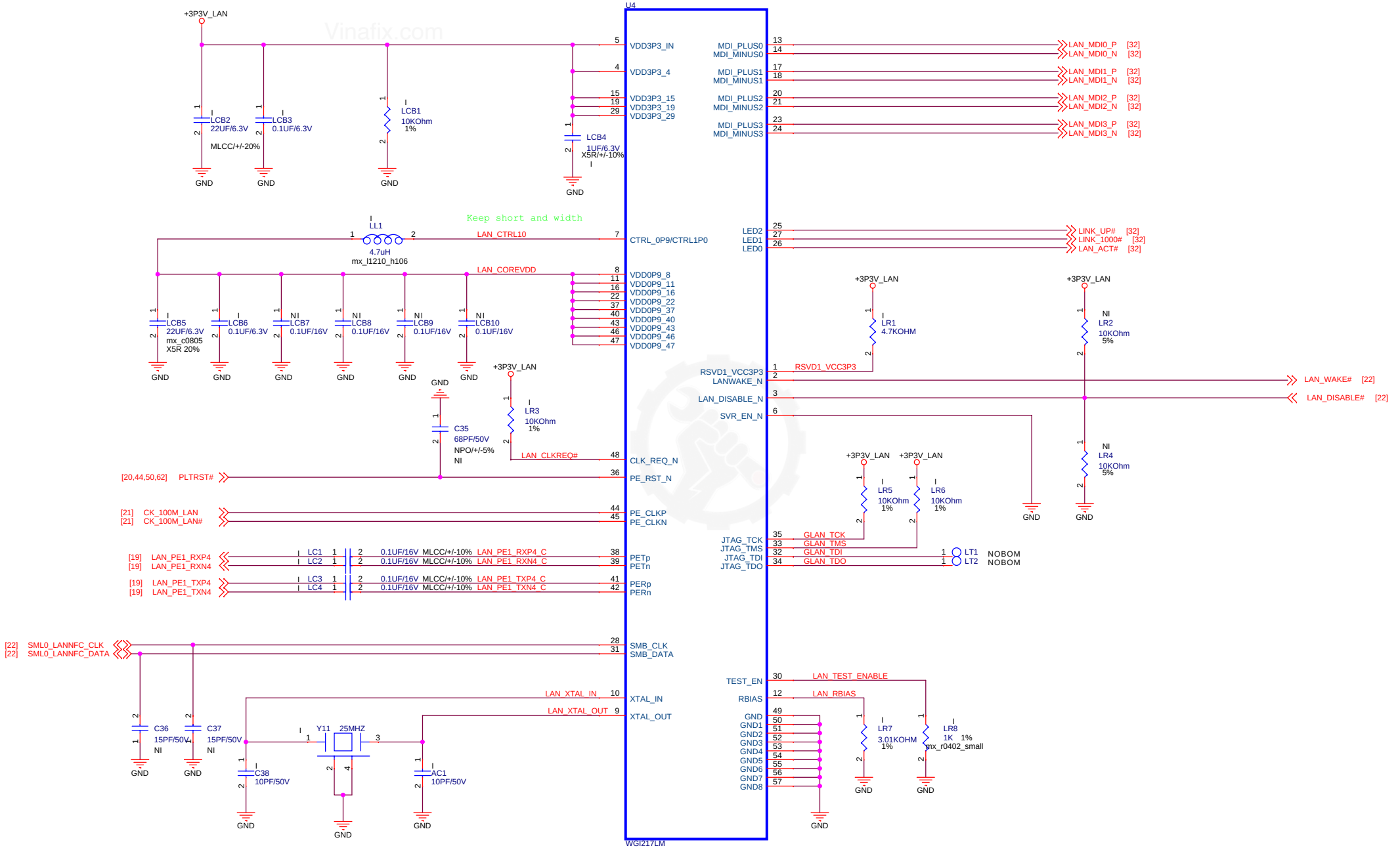
正式料號:0200-00SC0DE



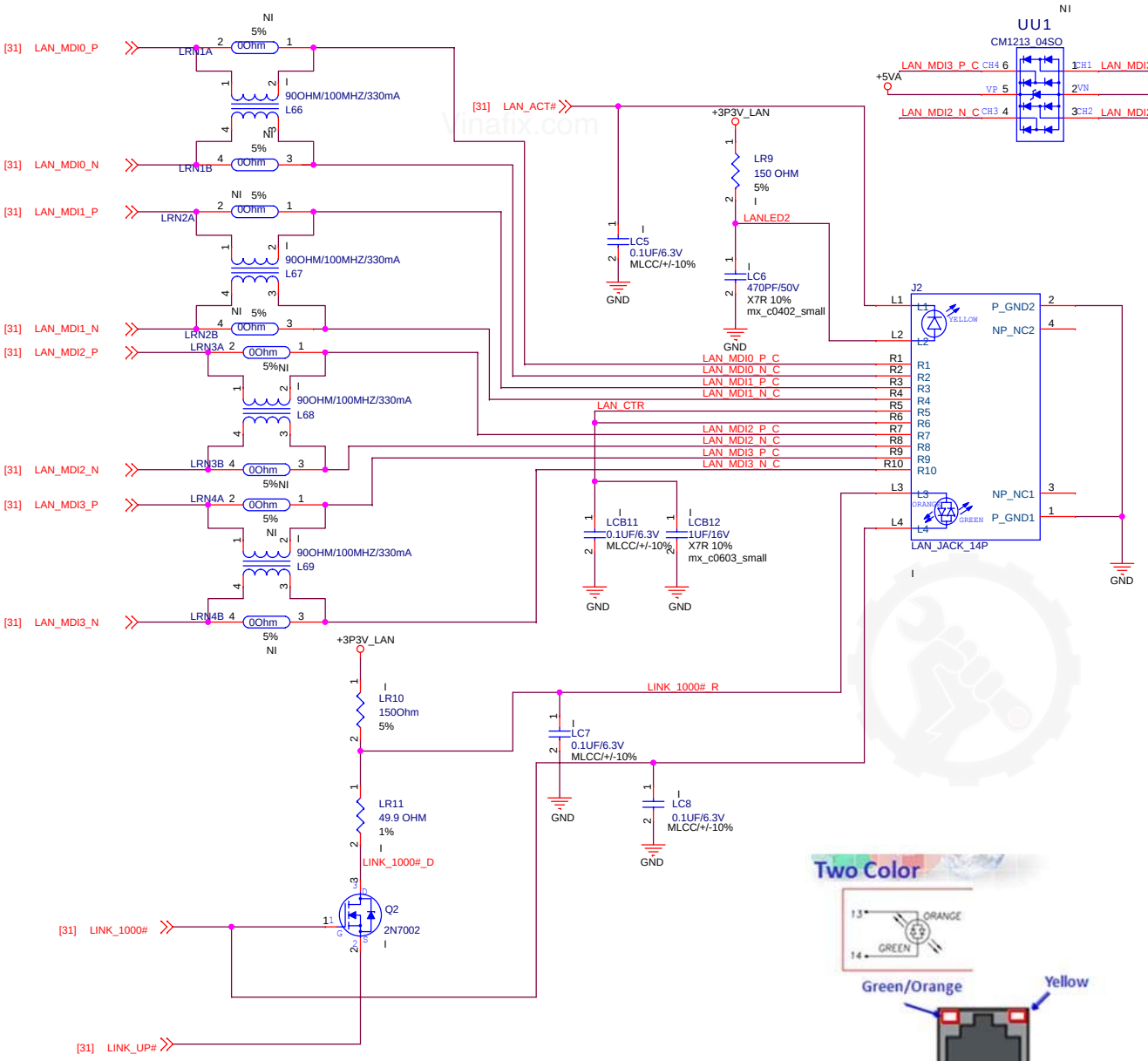
PEGATRON DT-MB RESTRICTED SECRET

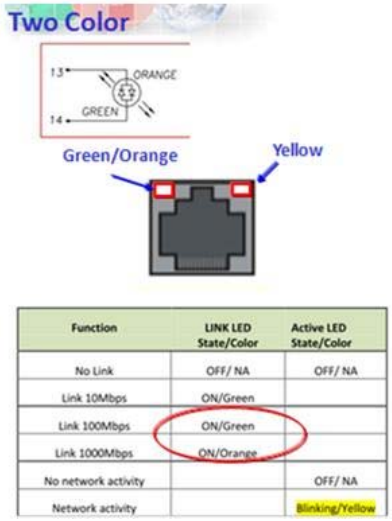
PEGATRON Title : INTEL CLARKVILLE

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 31 of 97





Function	LINK LED State/Color	Active LED State/Color
No Link	OFF/ NA	OFF/ NA
Link 10Mbps	ON/Green	
Link 100Mbps	ON/Green	
Link 1000Mbps	ON/Orange	
No network activity		OFF/ NA
Network activity		Blinking/Yellow

LED Modes Table

Mode	Selected Mode	Source Indication
000	Link 10/1000	Asserted when either 10 or 1000Mbps link is established and maintained
001	Link 100/1000	Asserted when either 100 or 1000Mbps link is established and maintained
010	Link Up	Asserted when any speed link is established and maintained.
011	Activity	Asserted when link is established and packets are being transmitted or received
100	Link/Activity	Asserted when link is established AND when there is NO transmit or receive activity
101	Link 10	Asserted when a 10Mbps link is established and maintained.
110	Link 100	Asserted when a 100Mbps link is established and maintained
111	Link 1000	Asserted when a 1000Mbps link is established and maintained

LED Configuration PHY Address 01, Page 0, Register 30

Name	Default	Bits	Description	Type
Blink rate	0b	15	Specifies the blink mode of the LEDs. 0b = Blinks at 200 ms on and 200 ms off. 1b = Blinks at 83 ms on and 83 ms off.	RW
LED2 Blink	0b	14	LED2_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED2 Invert	0b	13	LED2_IVRT Field 0b = Active low output. 1b = Active high output.	RW

LED Configuration PHY Address 01, Page 0, Register 30

Name	Default	Bits	Description	Type
LED2 Mode	110b	12:10	Mode specifying what event/state/pattern is displayed on LED2.	RW
LED1 Blink	0b	9	LED1_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED1 Invert	0b	8	LED1_IVRT Field 0b = Active low output. 1b = Active high output.	RW
LED1 Mode	111b	7:5	Mode specifying what event/state/pattern is displayed on LED1.	RW
LED0 Blink	1b	4	LED0_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED0 Invert	0b	3	LED0_IVRT Field 0b = Active low output. 1b = Active high output.	RW
LED0 Mode	100b	2:0	Mode specifying what event/state/pattern is displayed on LED0.	RW

PEGATRON Title : LAN JACK

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

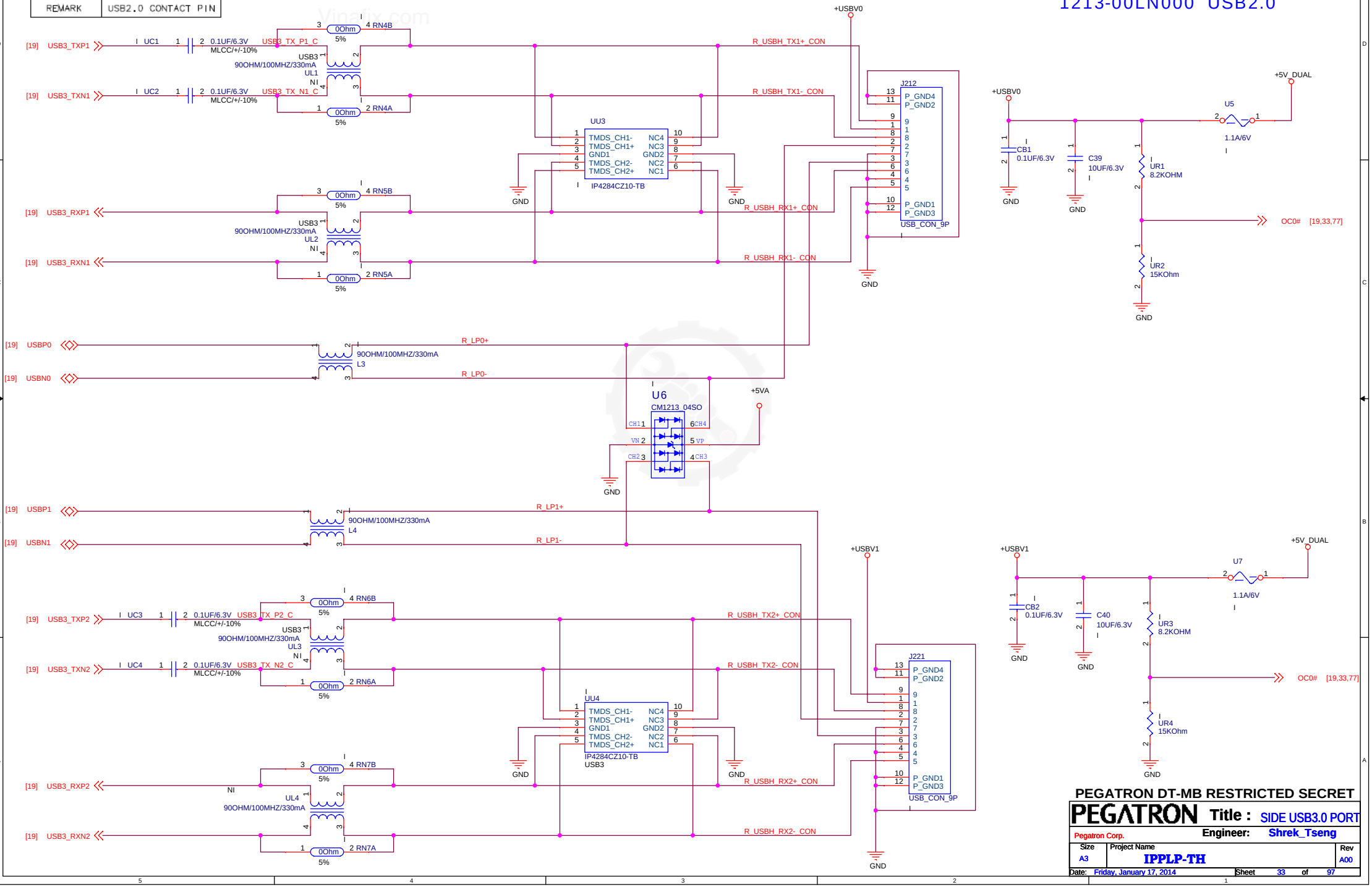
Date: Friday, January 17, 2014 Sheet 32 of 97

1213-00LN000 USB2.0

PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	PGND
REMARK	USB2.0 CONTACT PIN			

NOTE:
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

Gold flash only
Co-lay USB connecter
1213-00LH000 USB3.0
1213-00LN000 USB2.0



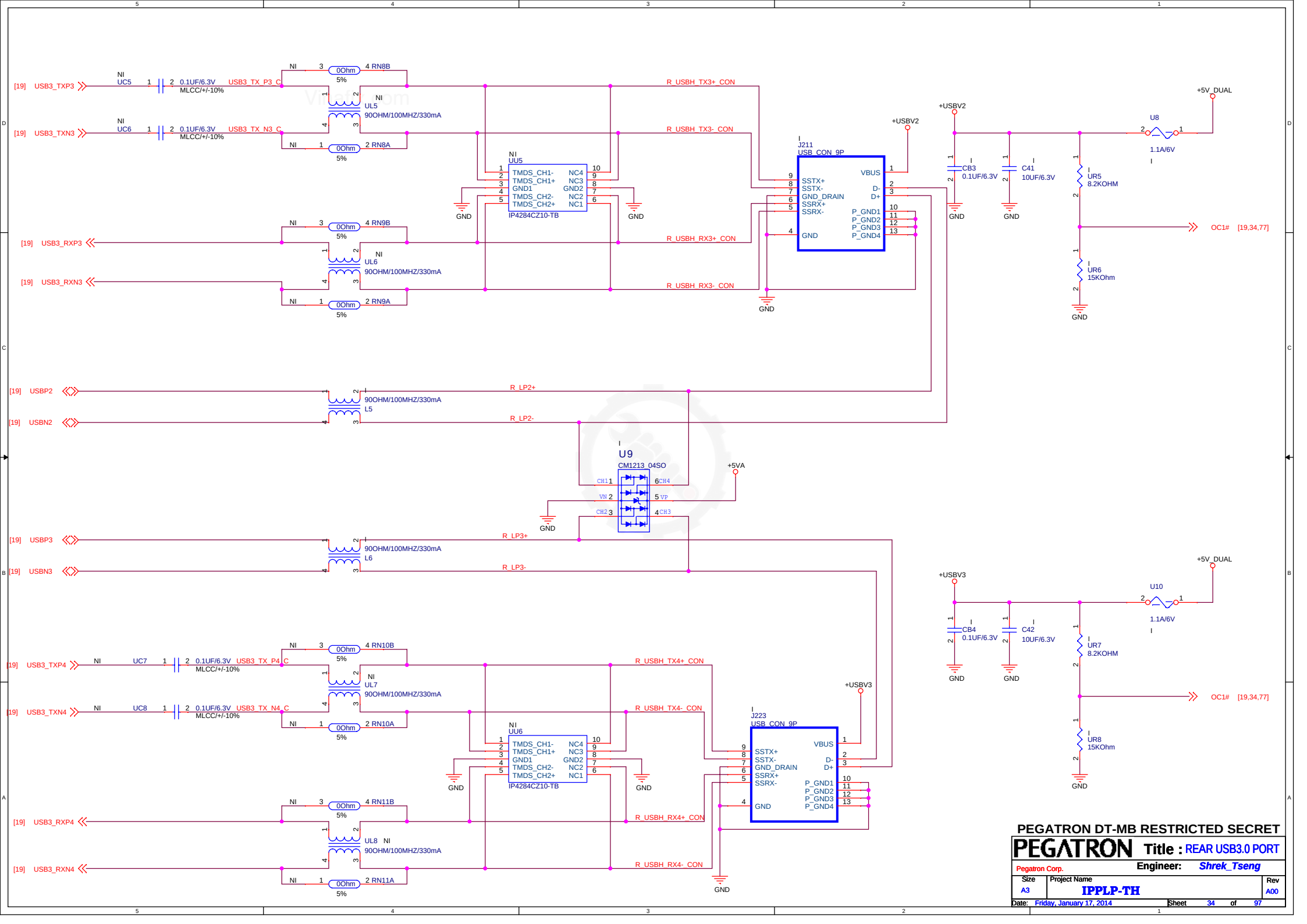
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIDE USB3.0 PORT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 33 of 97



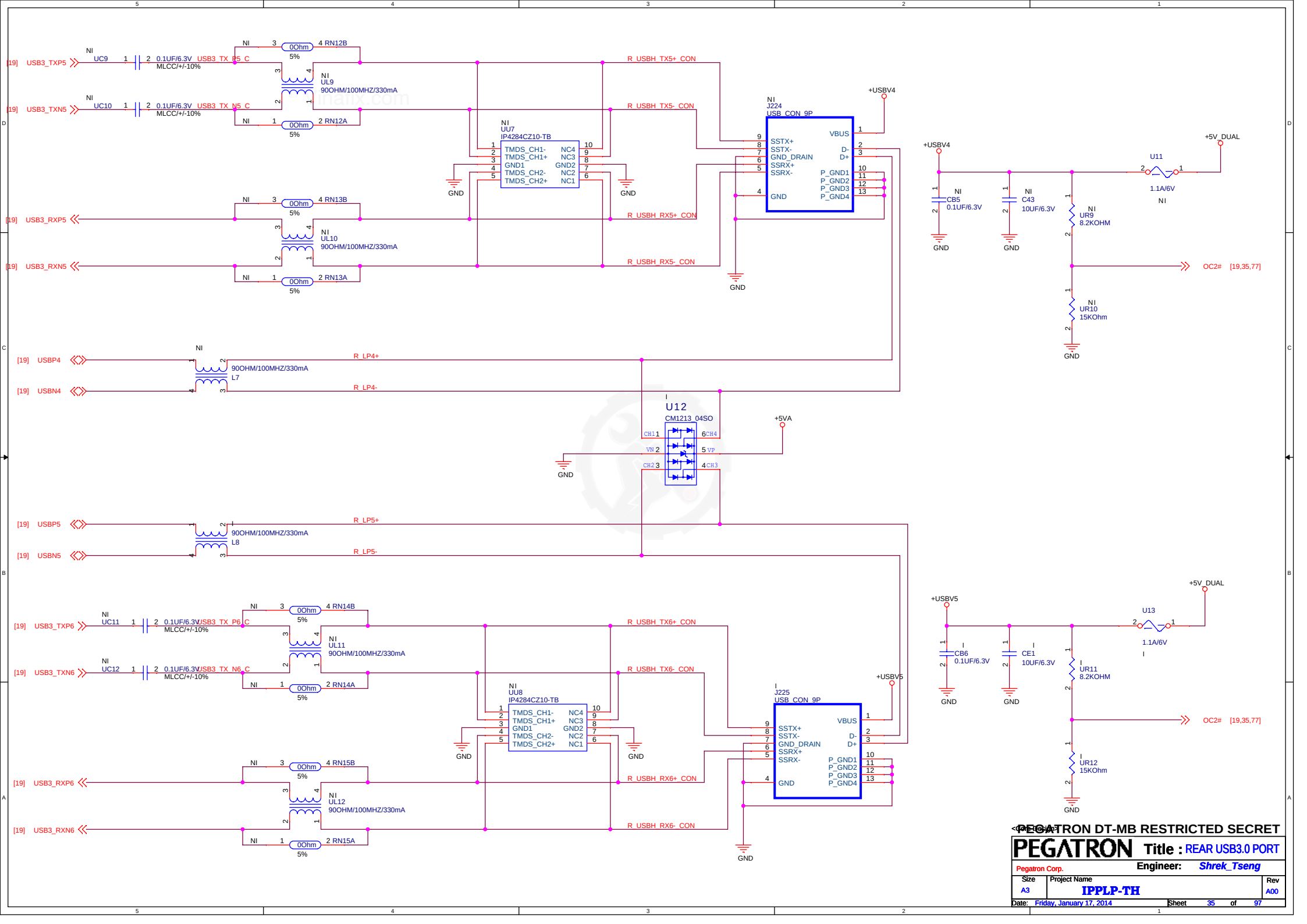
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : REAR USB3.0 PORT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 34 of 97

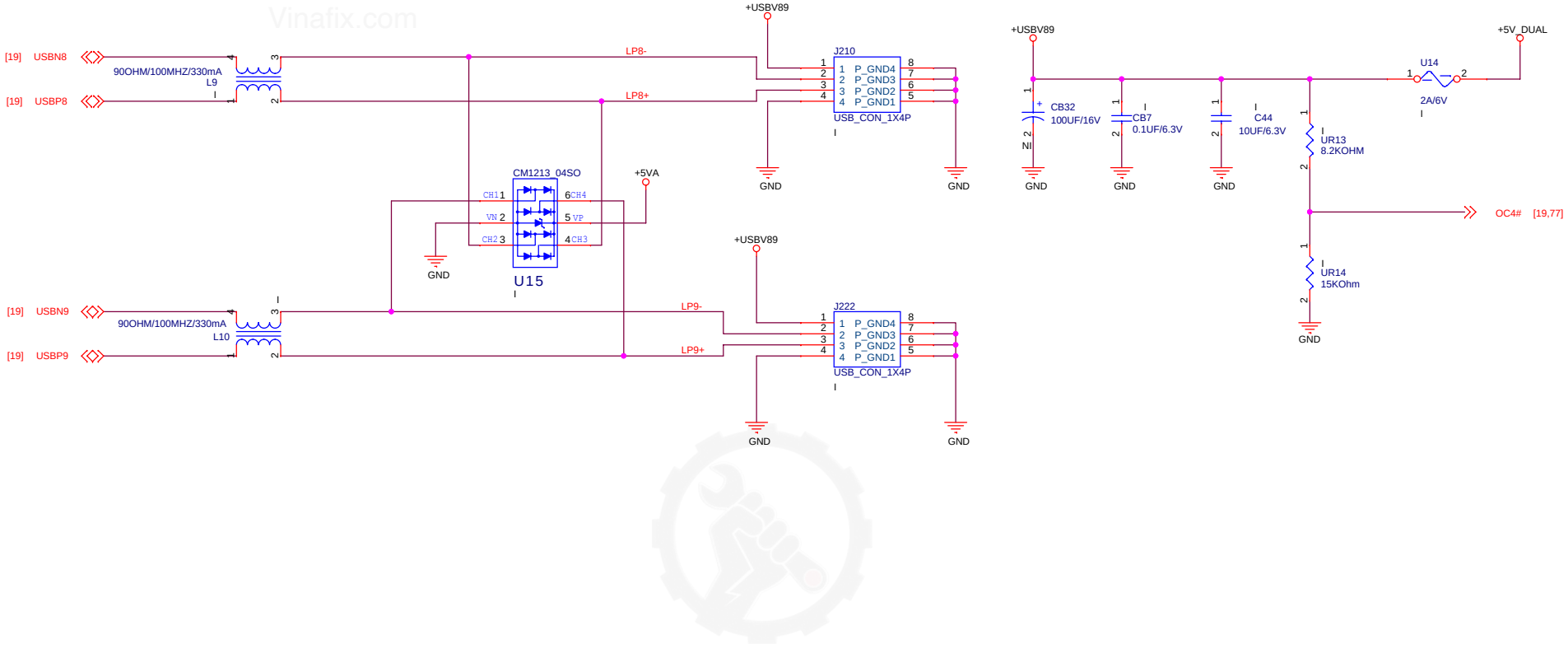


PEGATRON Title : REAR USB3.0 PORT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 35 of 97



PEGATRON Title : REAR USB2.0 PORT

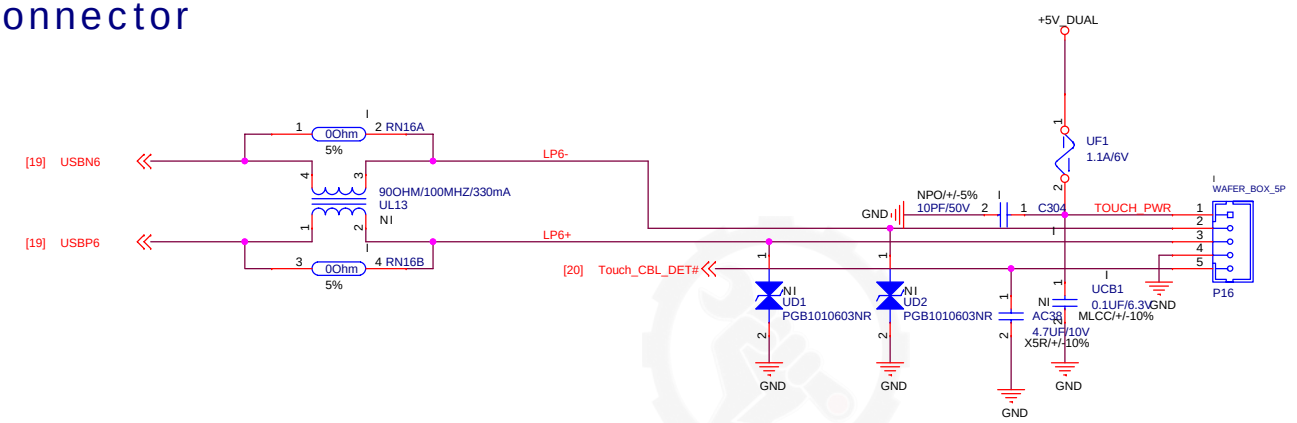
Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 36 of 97

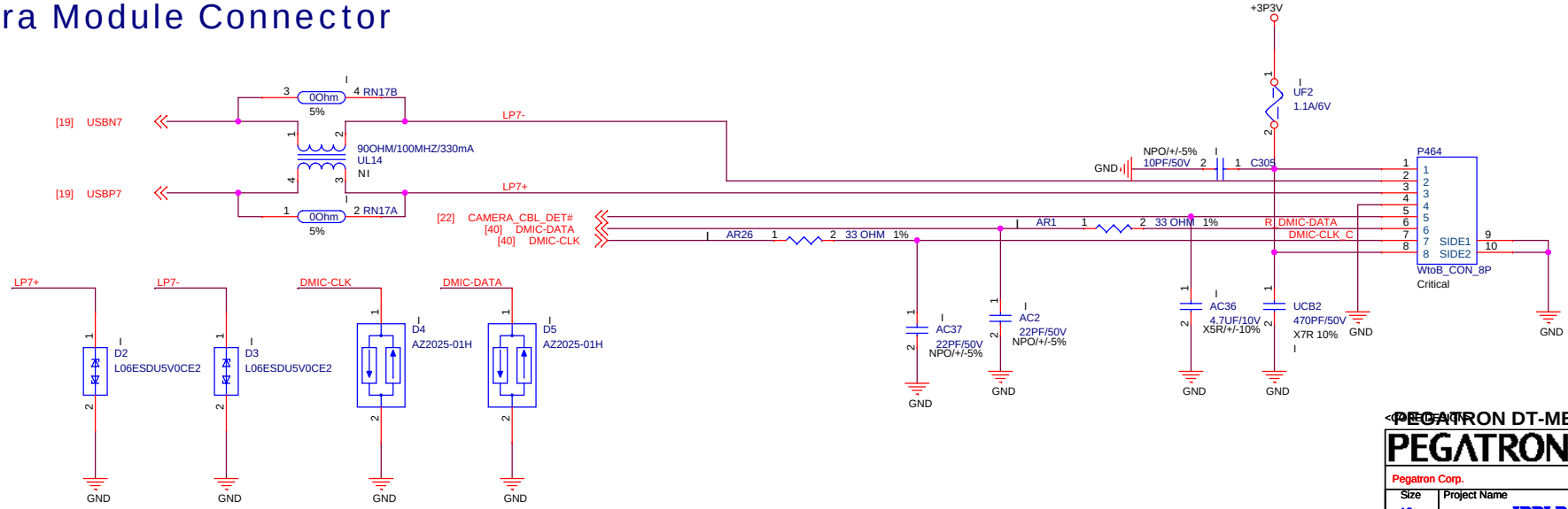
Touch Power Connector

Touch Panel Connector



Install MLCC 1UF/10V(0402) X5R 10%
1AX200271000
1A20-00A6600
1A20-00A7C00
1A20-00A5D00
1A20-00WTA00

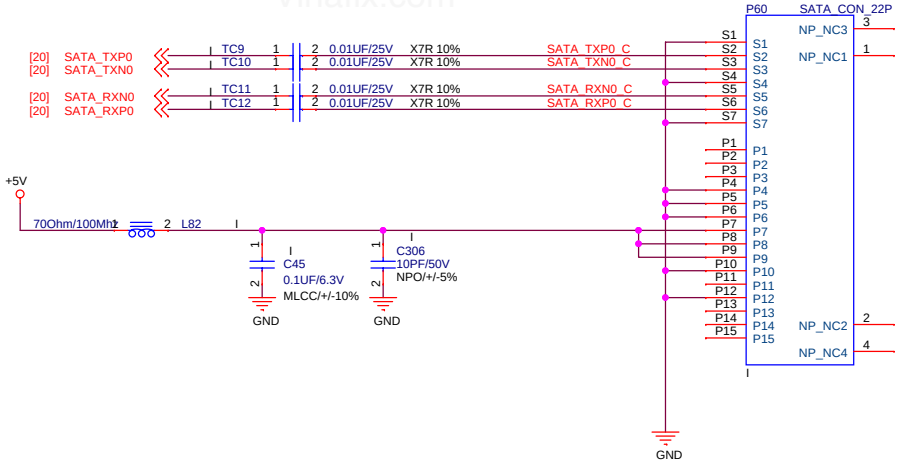
Camera Module Connector

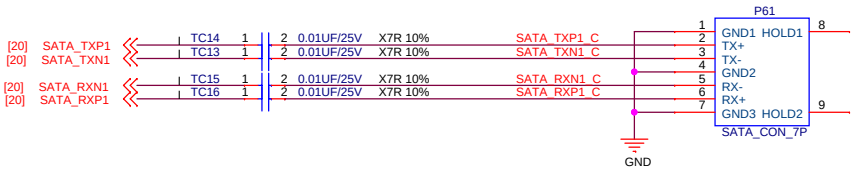


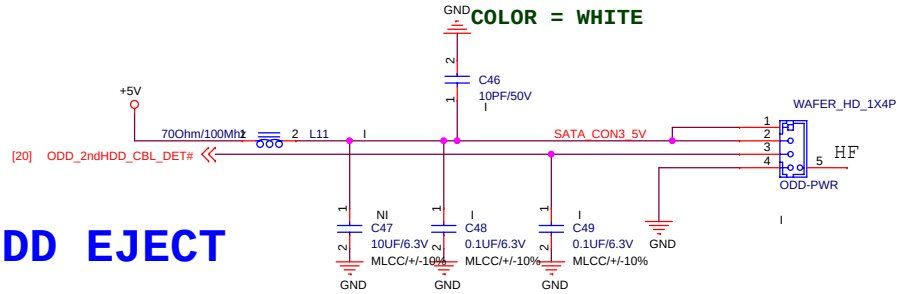
PEGATRON	Title : TOUCH & WEBCAM	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 37 of 97	

SATA CONNECTOR

NOTE:
Place those Cap close to Conn sode
To Conn distance are less then 500mils







ODD EJECT

PEGATRON DT-MB RESTRICTED SECRET

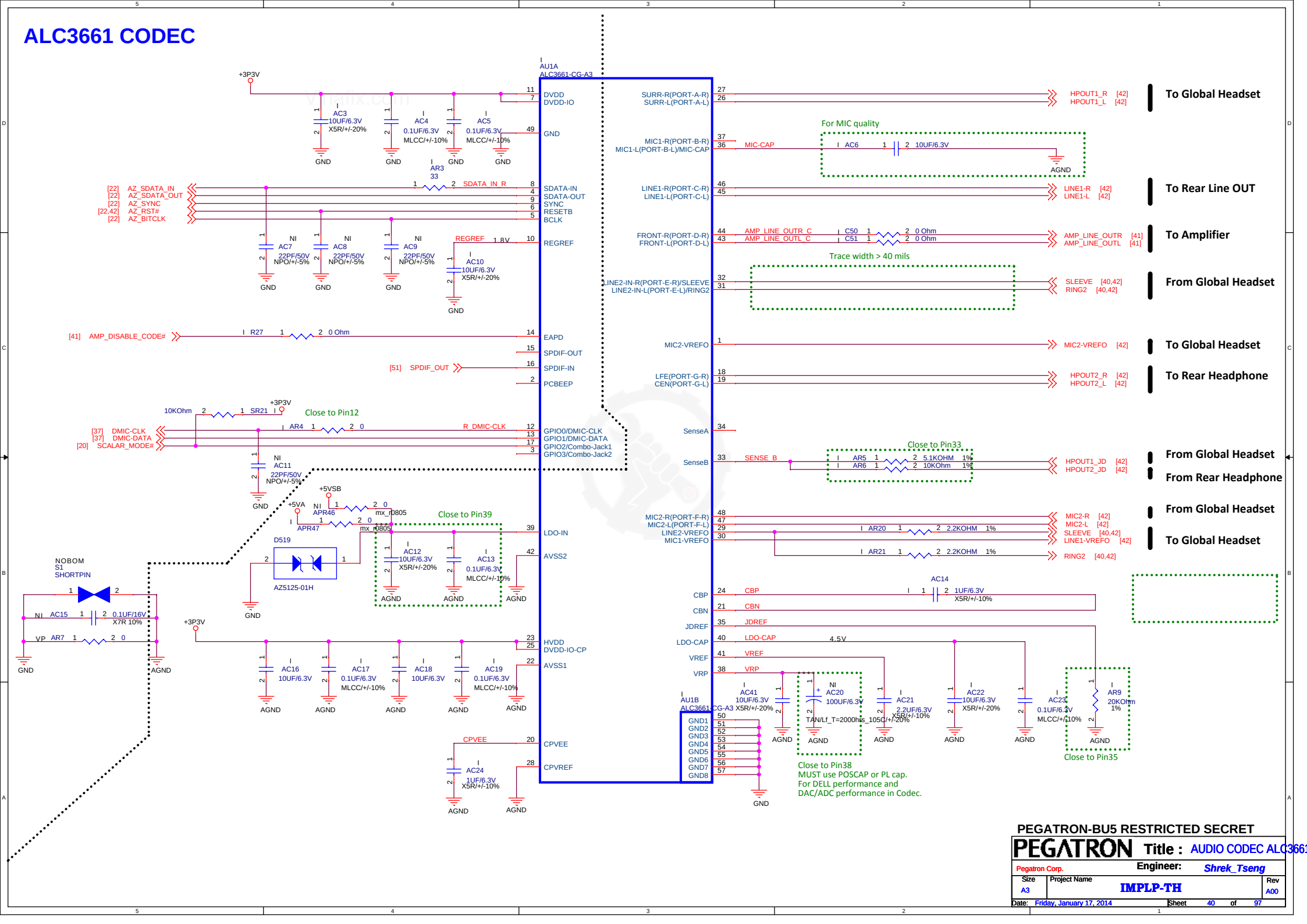
PEGATRON Title : SATA CONN

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

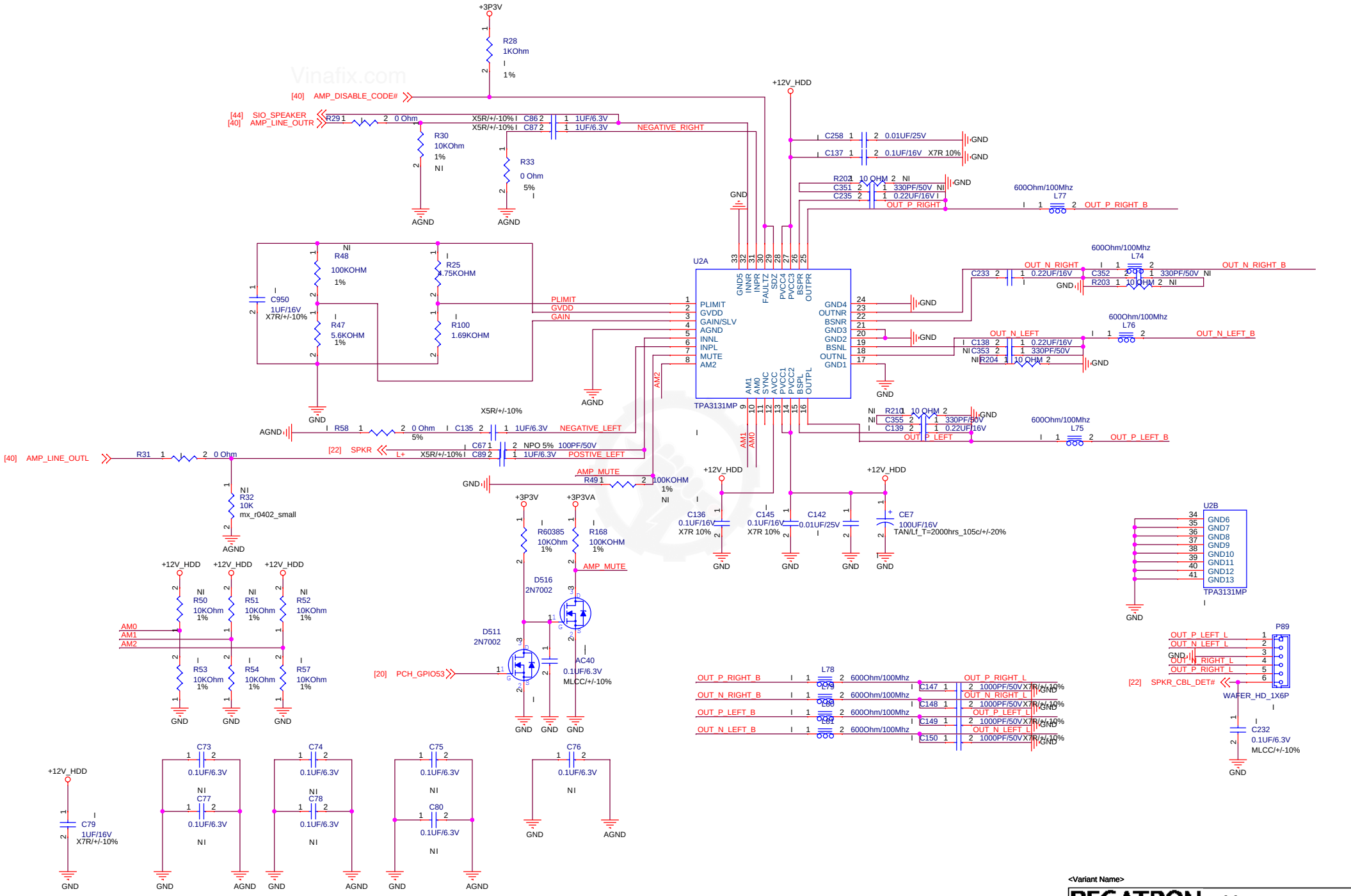
Date: Friday, January 17, 2014 Sheet 39 of 97

ALC3661 CODEC



PEGATRON-BU5 RESTRICTED SECRET

PEGATRON	Title : AUDIO CODEC ALC3661	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IMPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 40 of 97	



<Variant Name>

PEGATRON Title : AMP

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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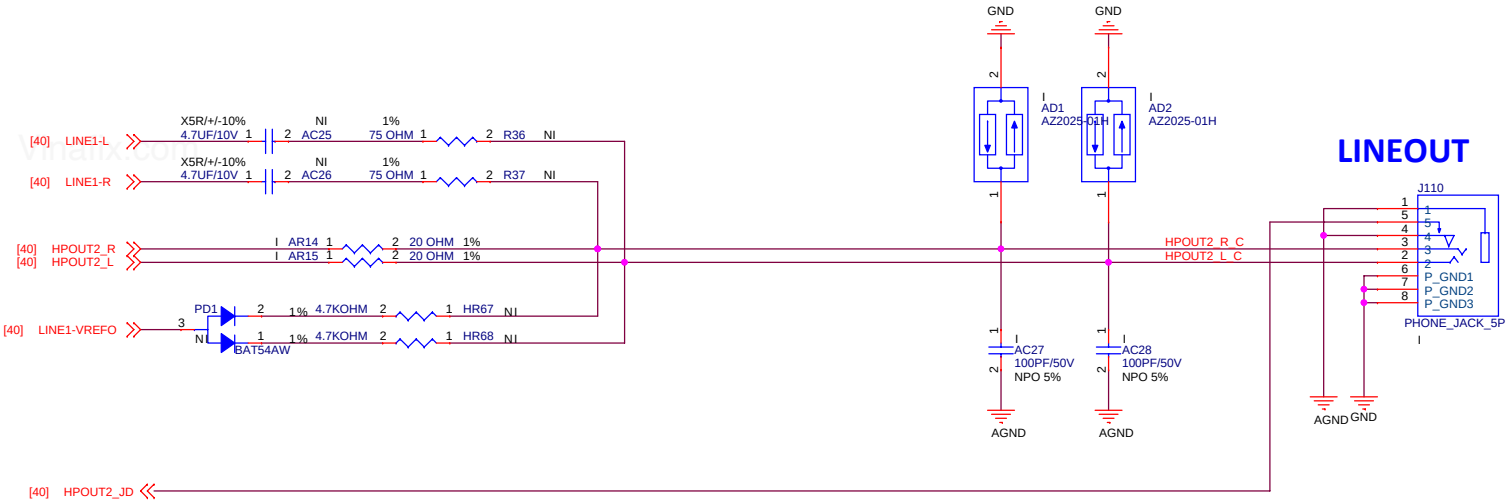
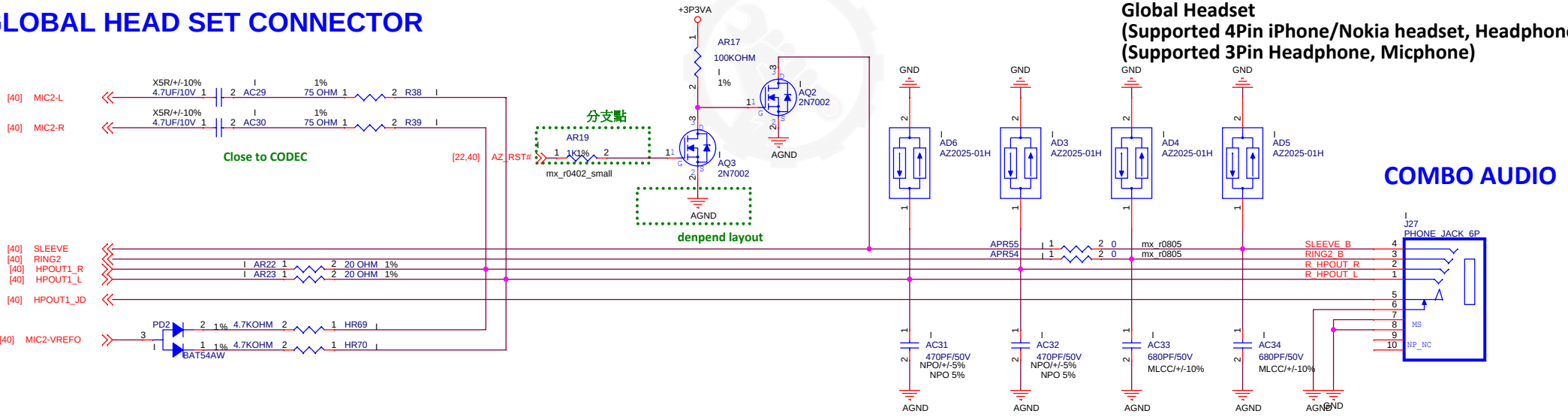
REAR LINE-OUT

Support Re-Tasking Function



GLOBAL HEAD SET CONNECTOR

Global Headset
(Supported 4Pin iPhone/Nokia headset, Headphone)
(Supported 3Pin Headphone, Micphone)

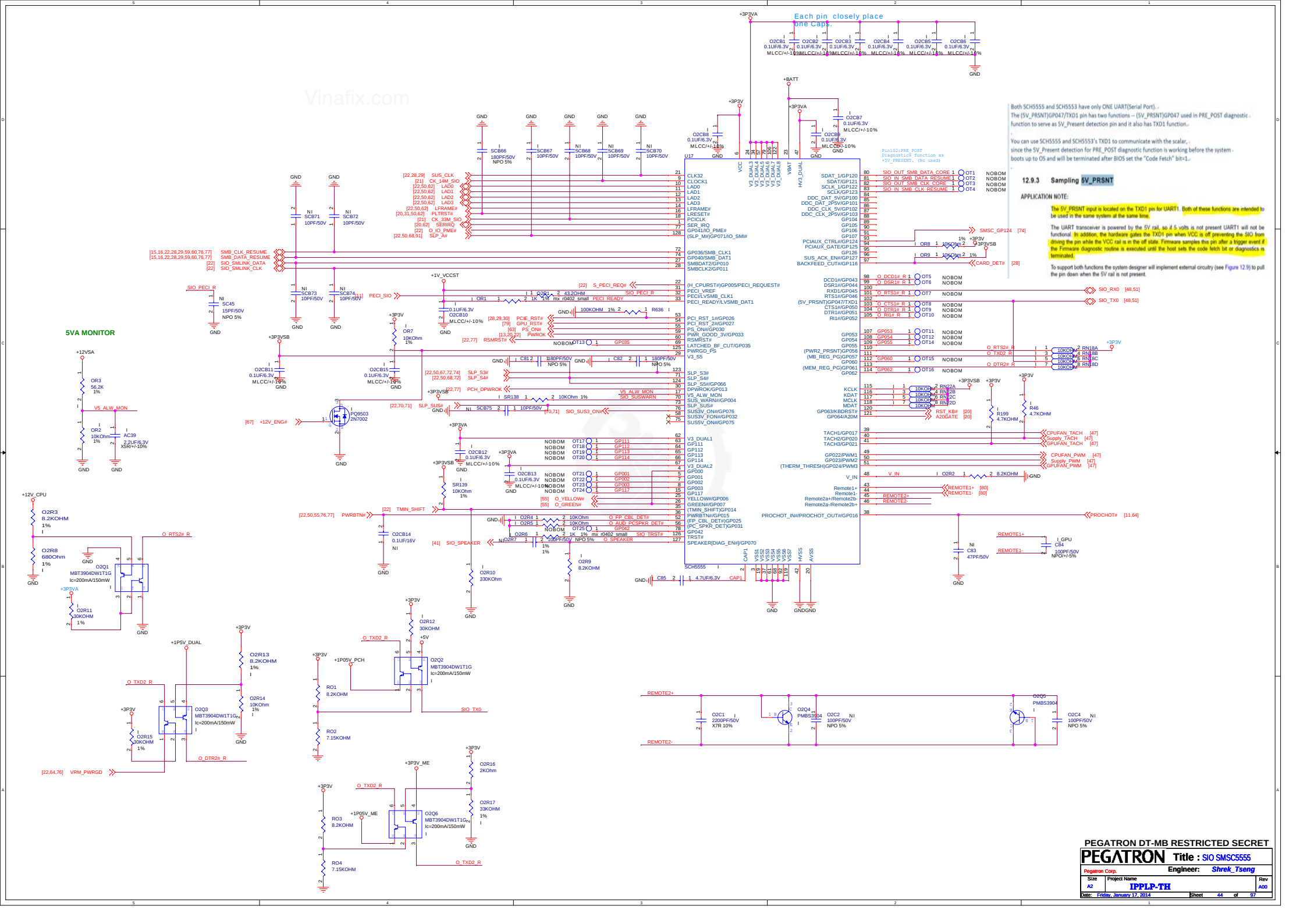


COMBO AUDIO

GHS JACK
12X141608000 -->12X141940000

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : REAR LINE OUT& GHS CONN	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 42 of 97	


Each pin closely place one Caps.
5VA MONITOR
U17
SCH5555
Pin102:PRE_POST DiagnosticS function as +5V_PRESENT. (No used)
Both SCH5555 and SCH5553 have only ONE UART(Serial Port).
The (5V_PRSNT)GP047/TXD1 pin has two functions -- (5V_PRSNT)GP047 used in PRE_POST diagnostic function to serve as 5V_Present detection pin and it also has TXD1 function.
You can use SCH5555 and SCH5553's TXD1 to communicate with the scalar, since the 5V_Present detection for PRE_POST diagnostic function is working before the system boots up to OS and will be terminated after BIOS set the "Code Fetch" bit=1.
12.9.3 Sampling 5V_PRSNT
APPLICATION NOTE:
The 5V_PRSNT input is located on the TXD1 pin for UART1. Both of these functions are intended to be used in the same system at the same time.
The UART transceiver is powered by the 5V rail, so if 5 volts is not present UART1 will not be functional. In addition, the hardware gates the TXD1 pin when VCC is off preventing the SIO from driving the pin while the VCC rail is in the off state. Firmware samples this pin after a trigger event if the Firmware diagnostic routine is executed until the host sets the code fetch bit or diagnostics is terminated.
To support both functions the system designer will implement external circuitry (see Figure 12.9) to pull the pin down when the 5V rail is not present.
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : SIO SMSC5555
Pegatron Corp.
Engineer: Shrek_Tseng
Size A2
Project Name IPPLP-TH
Rev A00
Date: Friday, January 17, 2014
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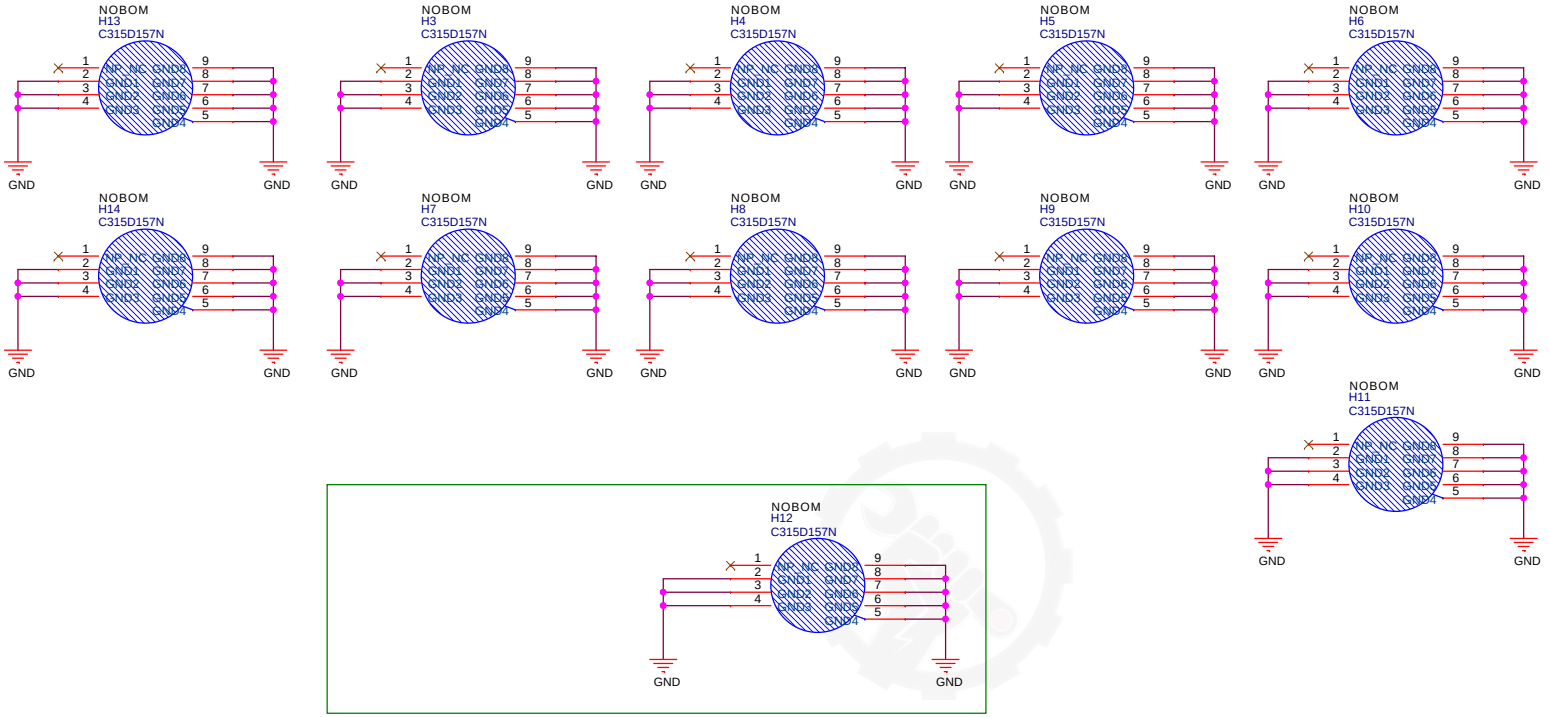

GPU SHOLE

H24	C126D126N	NOBOM
H25	C126D126N	NOBOM
H26	C126D126N	NOBOM
H27	C126D126N	NOBOM
H28	C224D224N	NOBOM
H29	C224D224N	NOBOM
H30	C252D252N	
H31	C224D224N	NOBOM

PEGATRON Title : SCREW HOLE

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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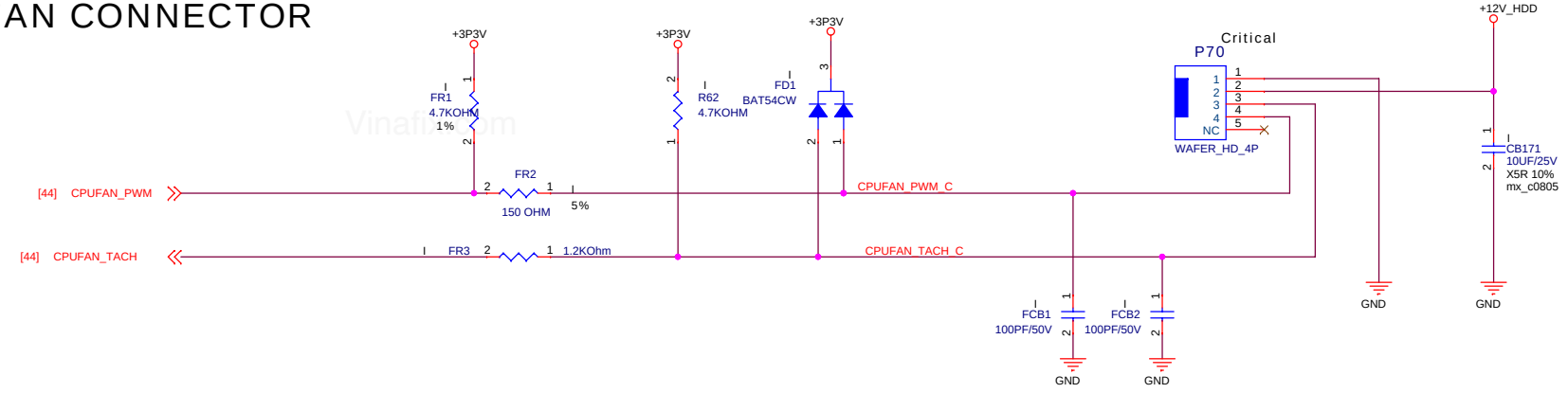
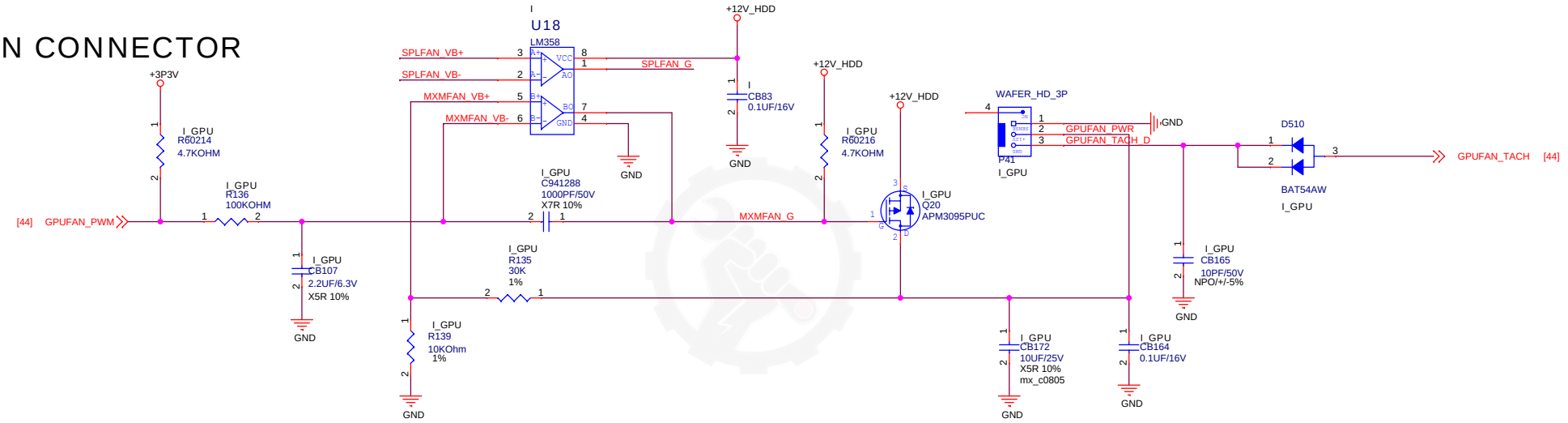
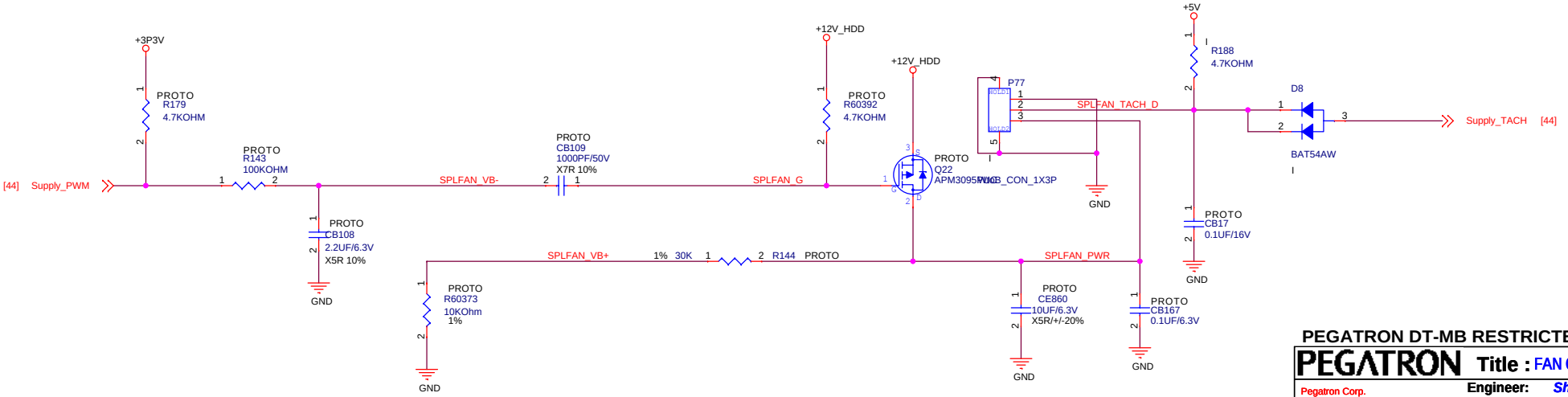
CPU FAN CONNECTOR



GPU FAN CONNECTOR





POWER SUPPLY FAN CONNECTOR

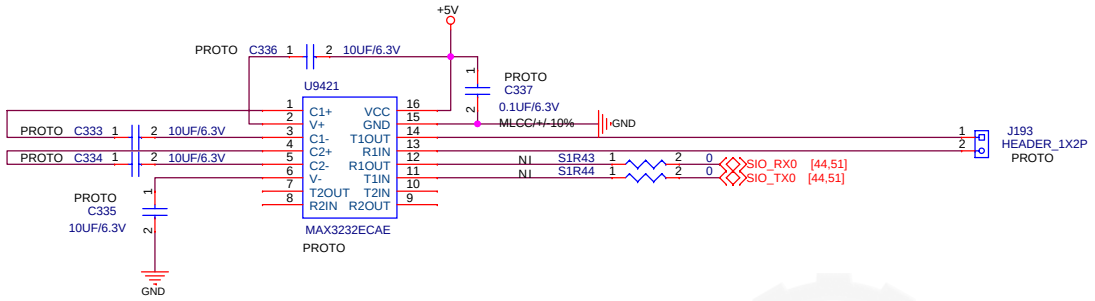
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FAN CIRCUIT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

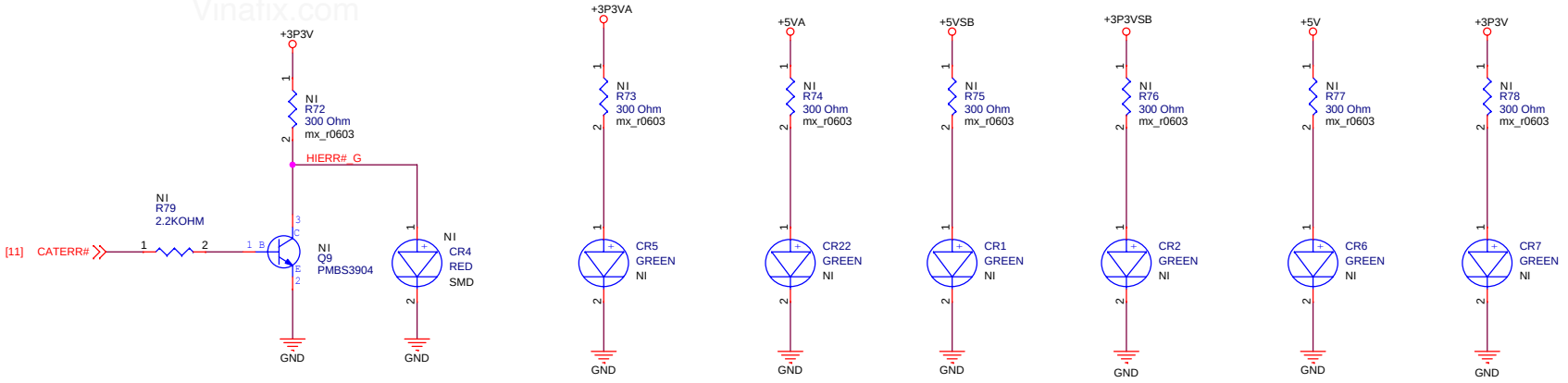
Date: Friday, January 17, 2014 Sheet 47 of 97



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	COM PORT
Pegatron Corp.	Engineer:	Shrek_Tseng
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 48 of 97	

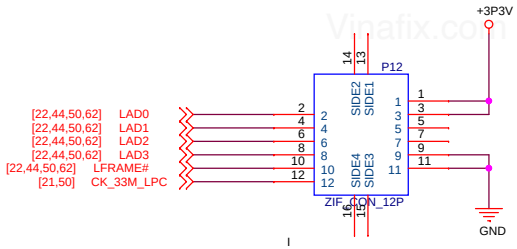
+5VA : GREEN
+5VSB : GREEN

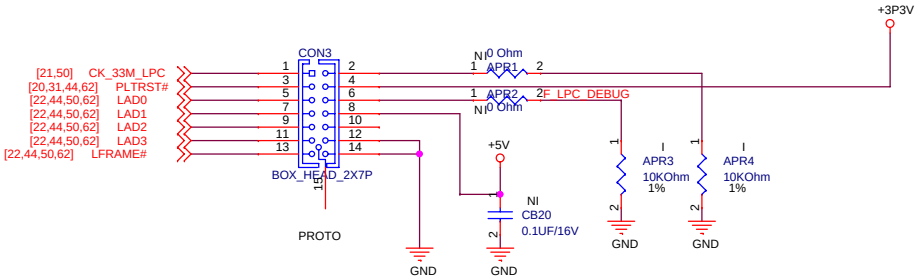


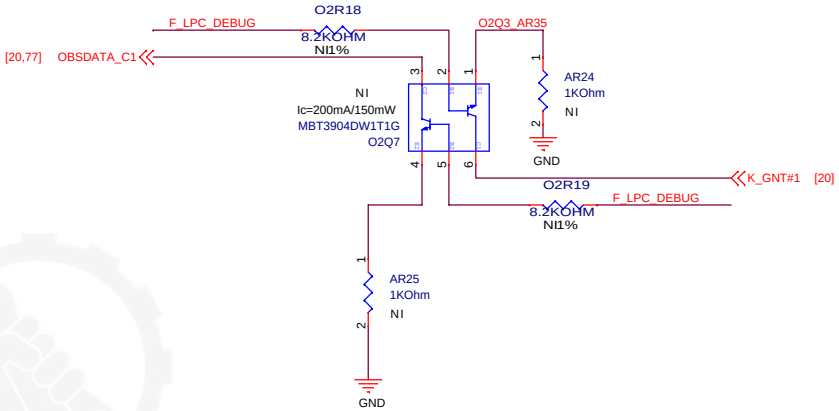
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DEBUG LED	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size A3	Project Name IPPLP-TH	Rev A00
Date: Friday, January 17, 2014	Sheet 49 of 97	

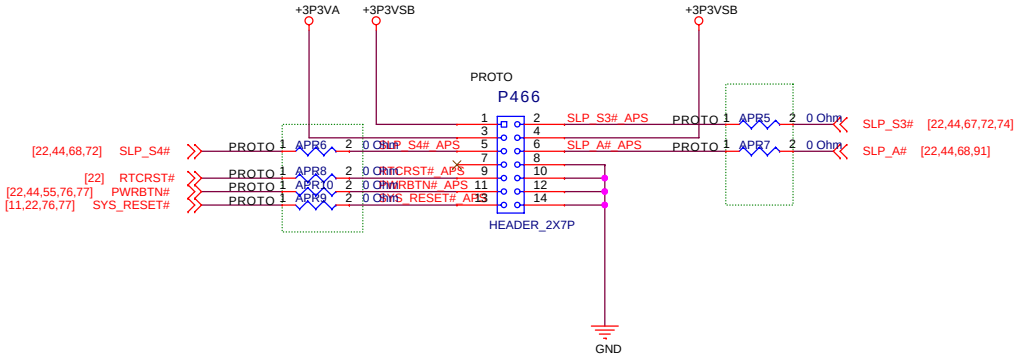
Debug Card CON







APS



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : APS/LPC DEBUG

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 50 of 97

*ALL RESISTOR ARE MX_R0402_SMALL FOOTPRINT

S1C35 can NI if power noise test pass

From External HDMI In

From PCH

From Internal CPU HDMI In

To PCH

To LVDS & Dual CONN.

To SIO

To Scalar Debug

To Scalar EEPROM

To Scalar SPI ROM

To LVDS CONN.

	ID_0_A	ID_1_A
LG	1	1
SAM	1	0

000	Brightness up	
001	Brightness Down	
010	Volume up	
011	Volume Down	
100	PC mode	
101	AV Mode	
110	Screen Off Enable	
111	Screen Off Disable	

PEGATRON DT-MB RESTRICTED SECRET

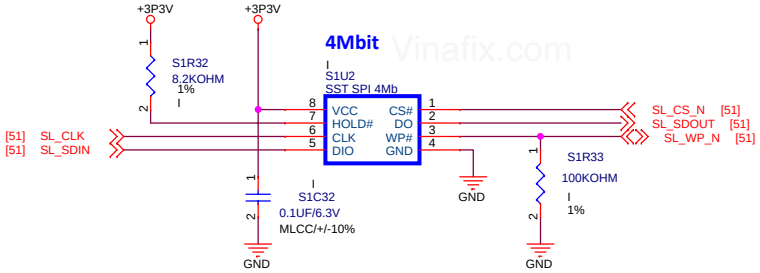
PEGATRON Title : SCALAR_TSUMU88BDC2-1

Pegatron Corp. Engineer: Shrek_Tseng

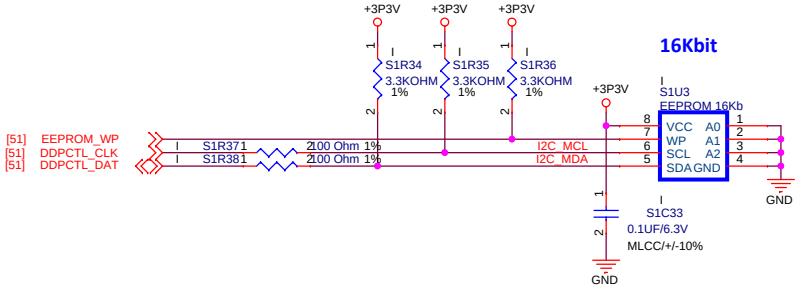
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 51 of 97

SCALAR SPI ROM

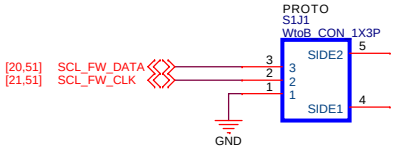


SCALAR EEPROM



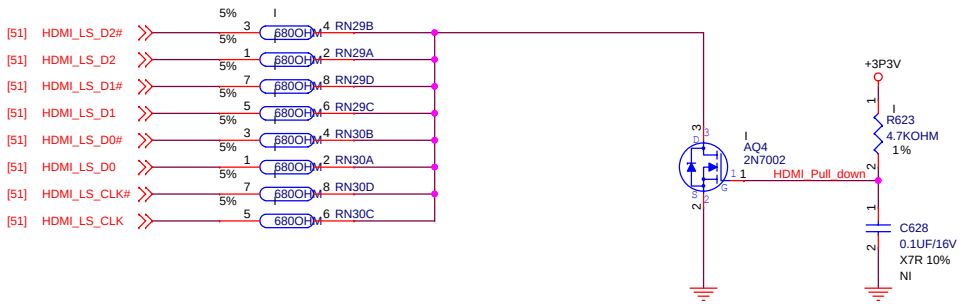
OSD Power Button wake up from Screen off

SCALAR DEBUG PORT

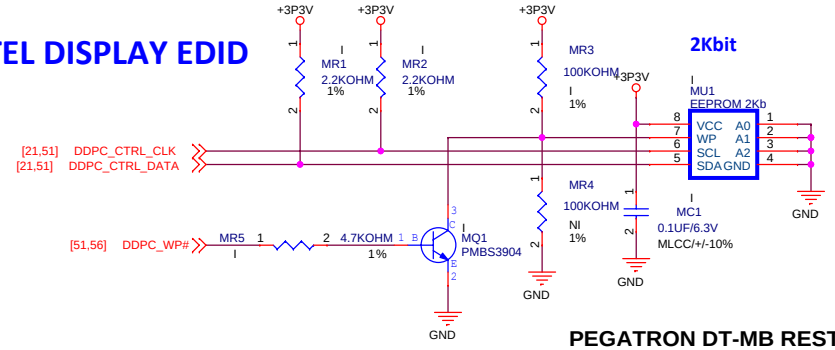


SCALAR HDMI LEVEL SHIFT (Cost Reduce)

Cost Reduced Level Shifter Motherboard Topology for max data rate of 1.65 Gb/s
Active Level Shifter Motherboard Topology for max data rate of 2.97 Gb/s

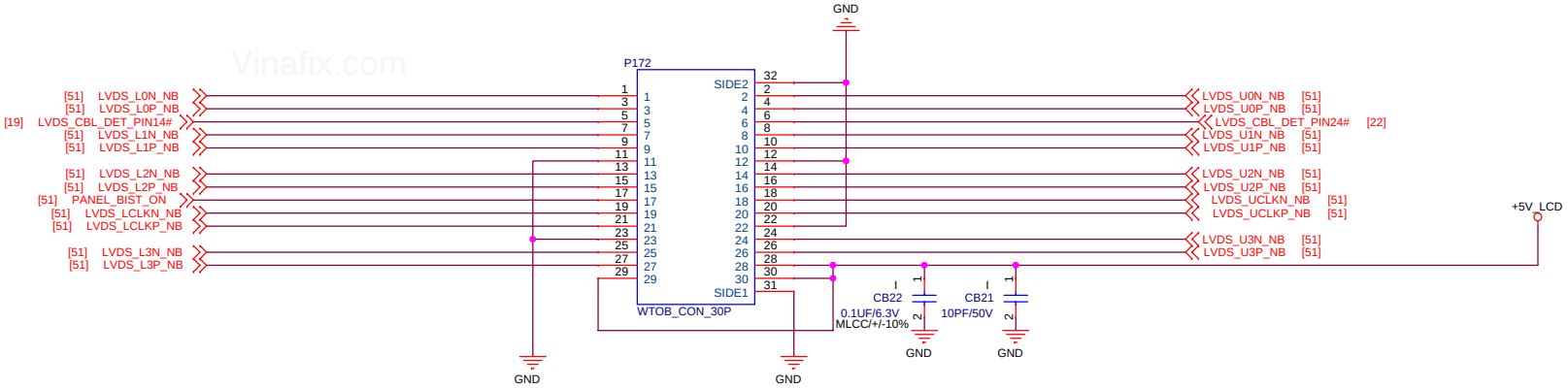


INTEL DISPLAY EDID



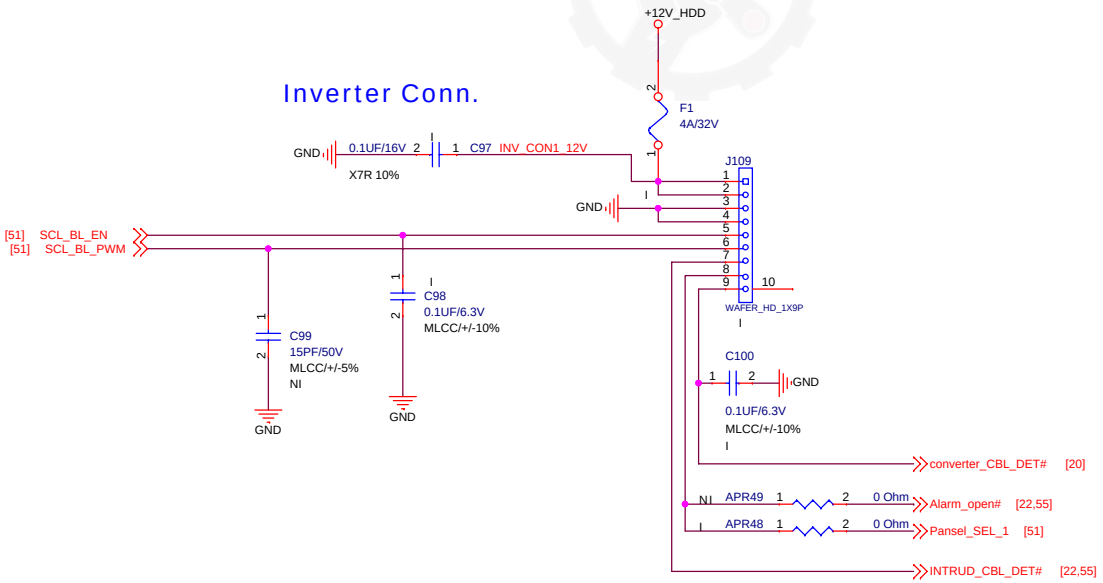
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SCALAR_TSUMU88BDC2-2	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 52 of 97	



CONVERTER CONN.

Inverter Conn.



PEGATRON DT-MB RESTRICTED SECRET

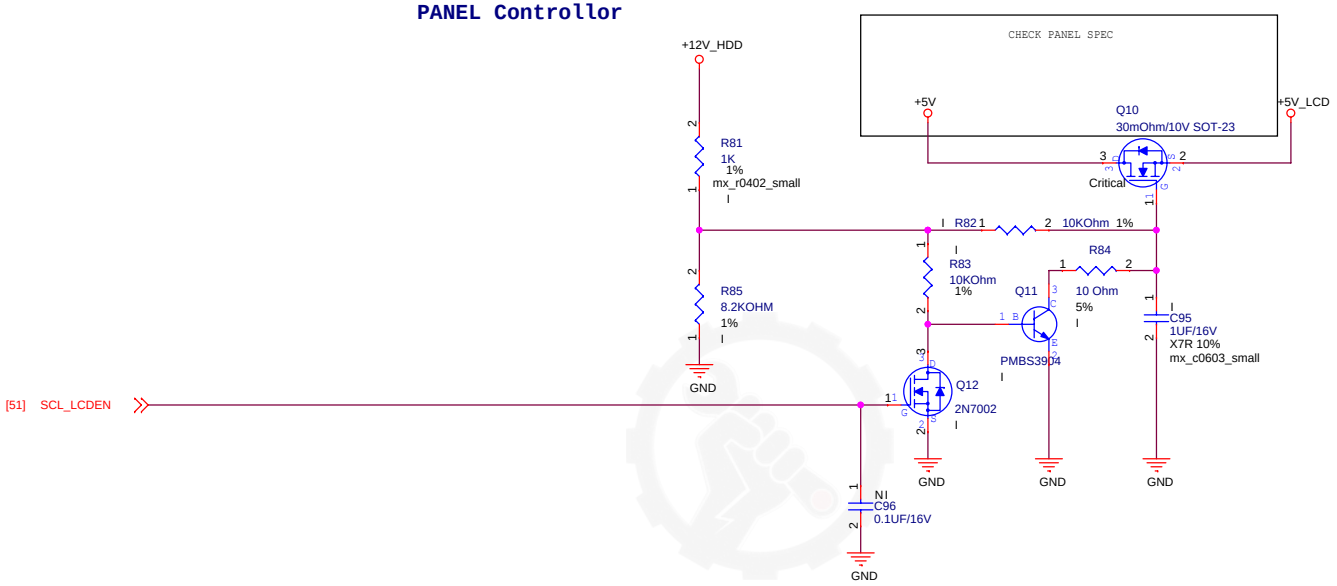
PEGATRON Title : LVDS & CONVERTER CO

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

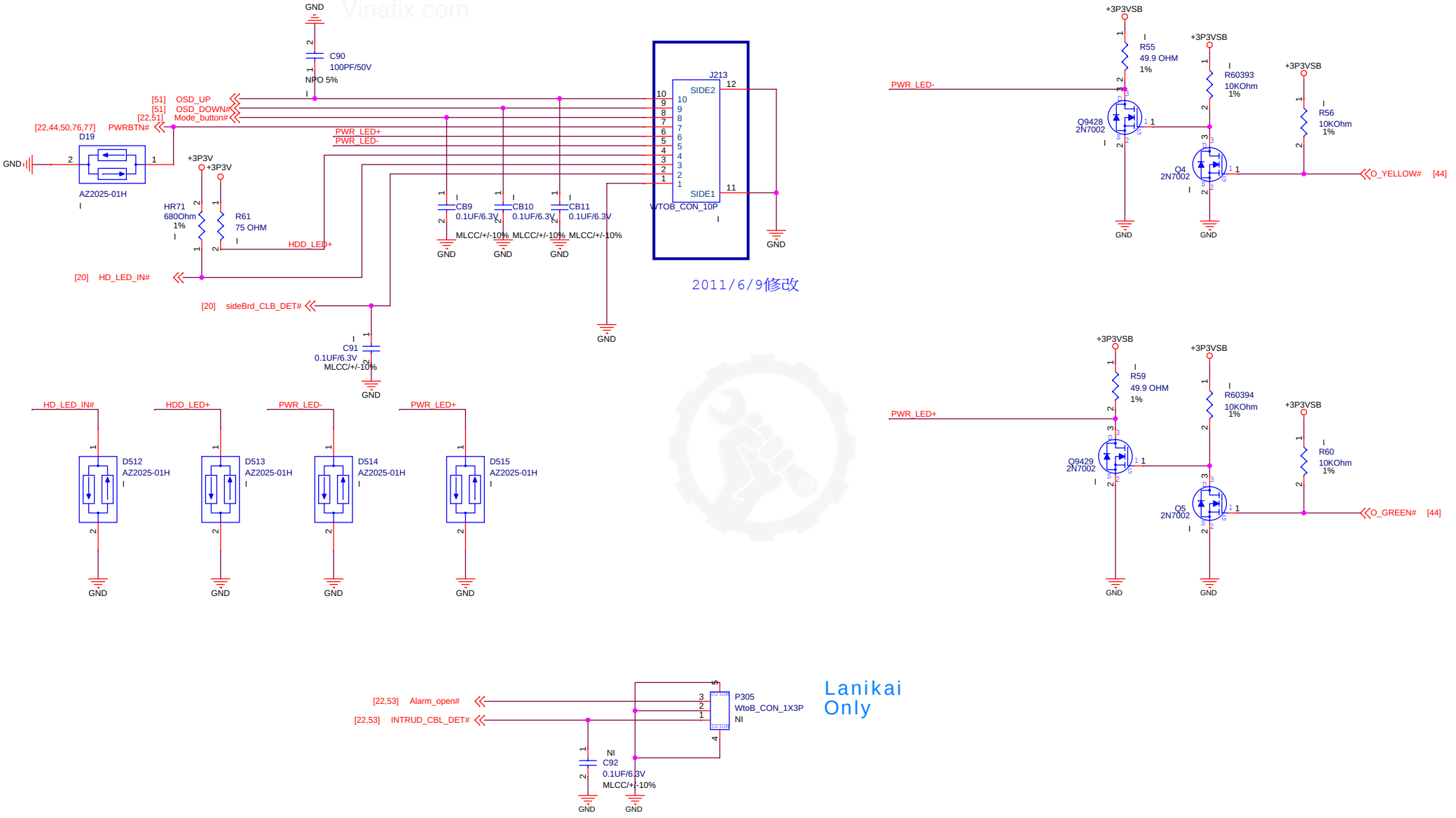
Date: Friday, January 17, 2014 Sheet 53 of 97

PANEL Controllor



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Corp.	Title : SCALAR LCD ENABLE	
	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 54 of 97	



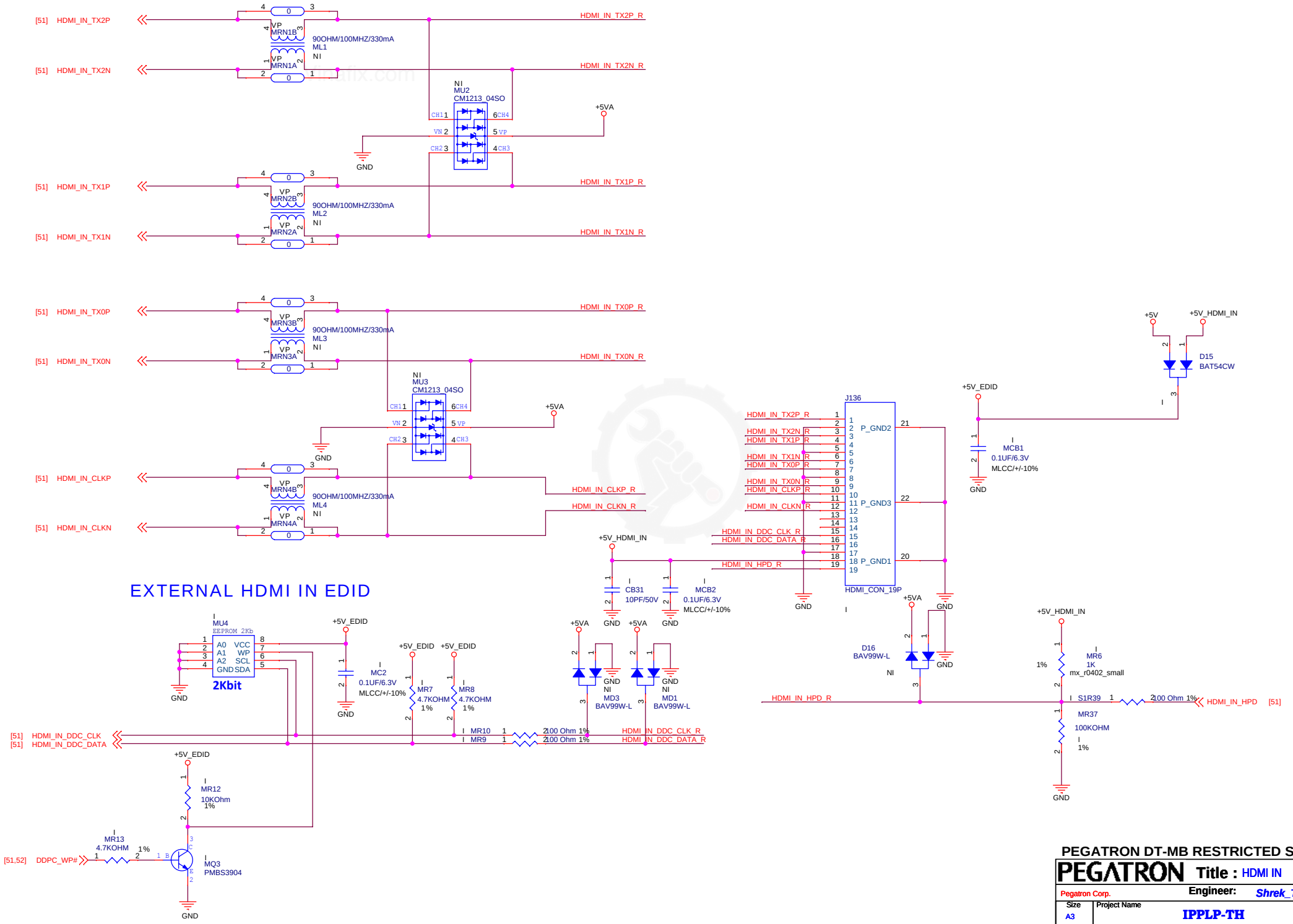
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FRONT PANEL

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 55 of 97



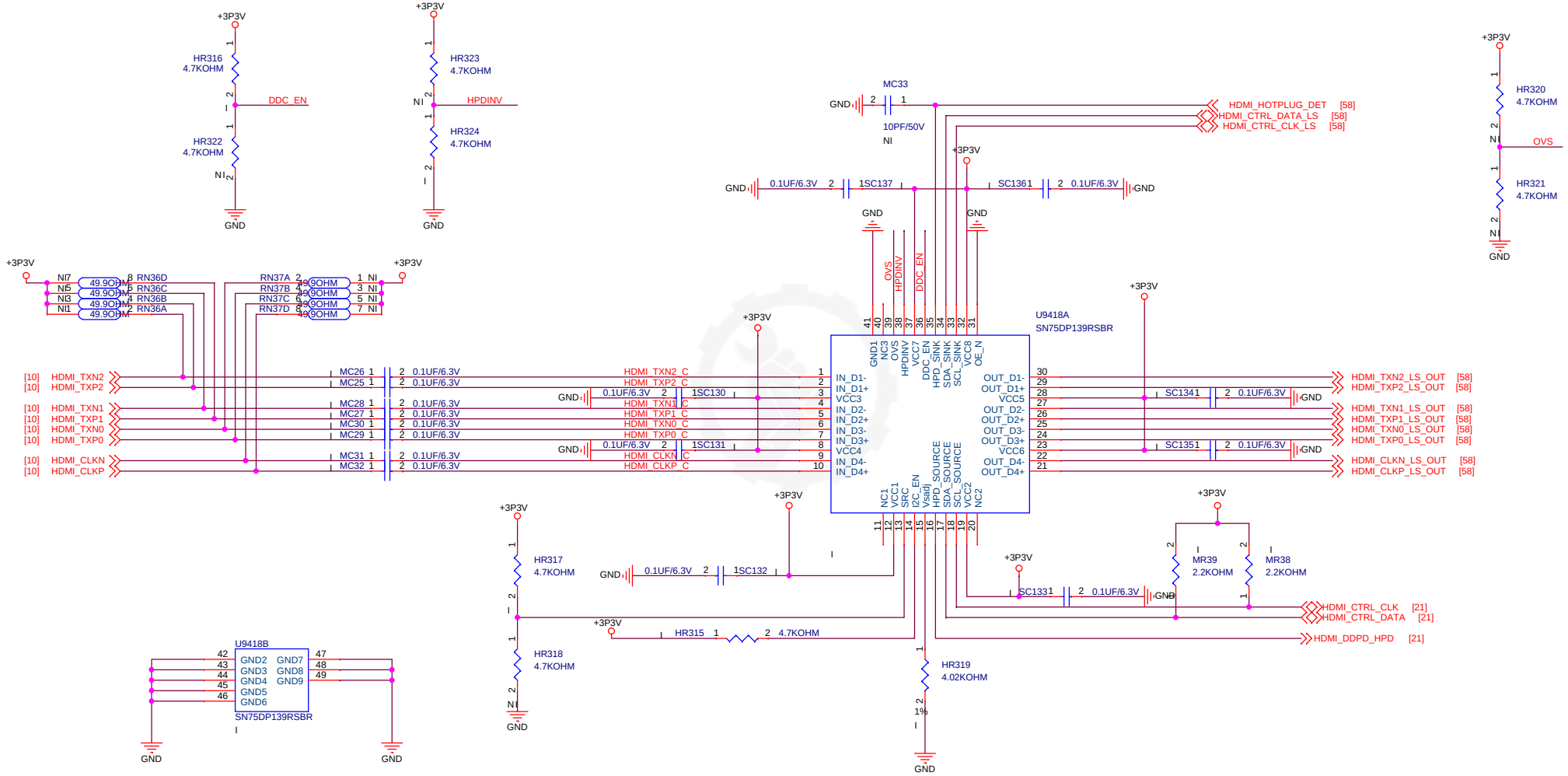
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HDMI IN

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 56 of 97

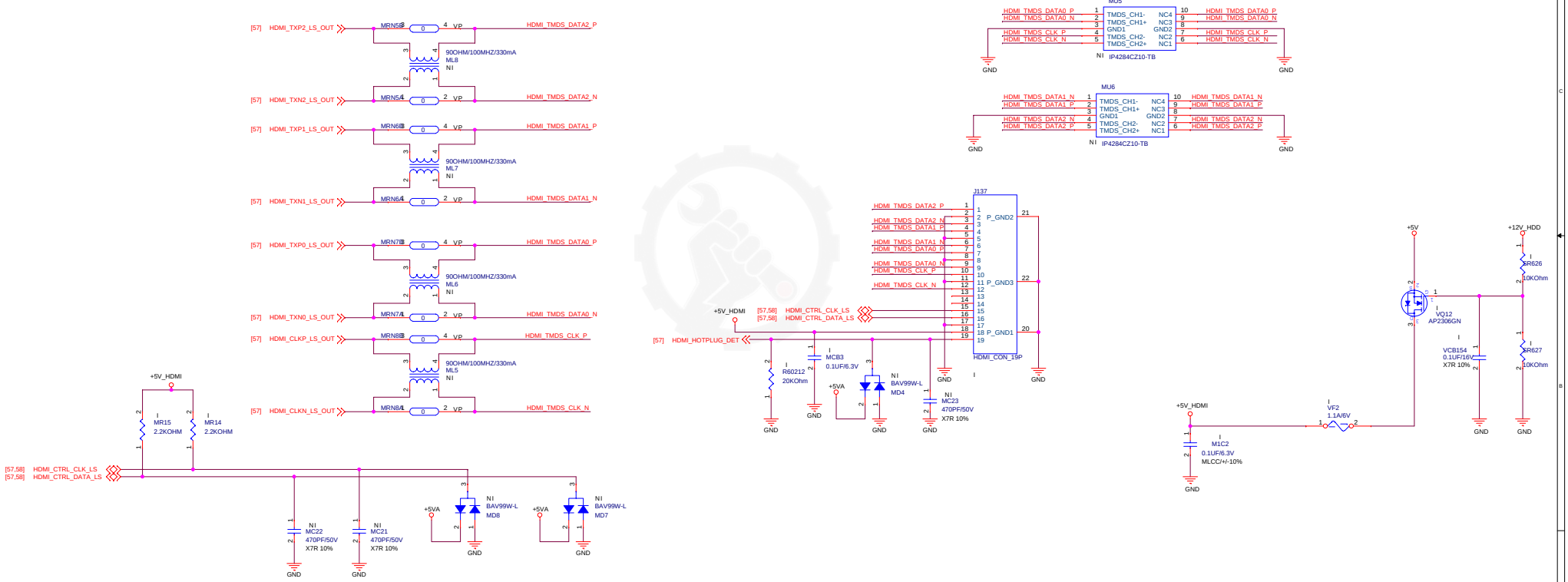


PEGATRON Title : HDMI LEVEL SHIFT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 57 of 97



PEGATRON DT-MB RESTRICTED SECRET

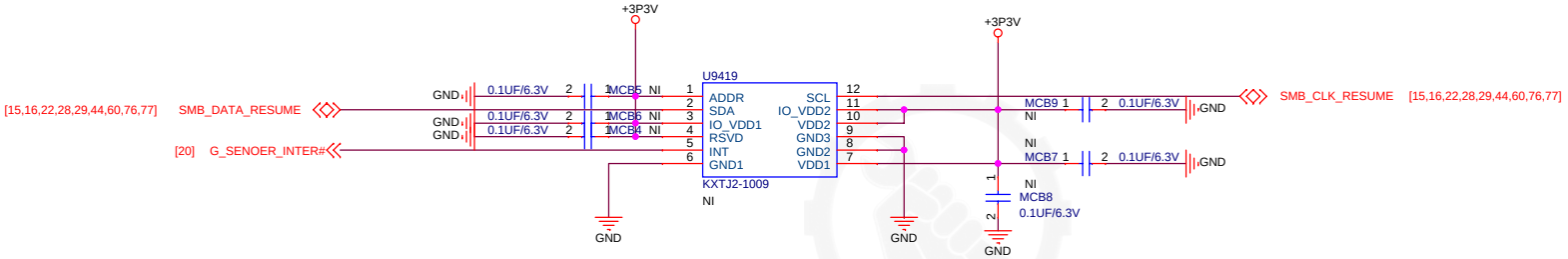
<Core Design>

PEGATRON Title : HDMI OUT

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A2	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 58 of 97



PEGATRON DT-MB RESTRICTED SECRET

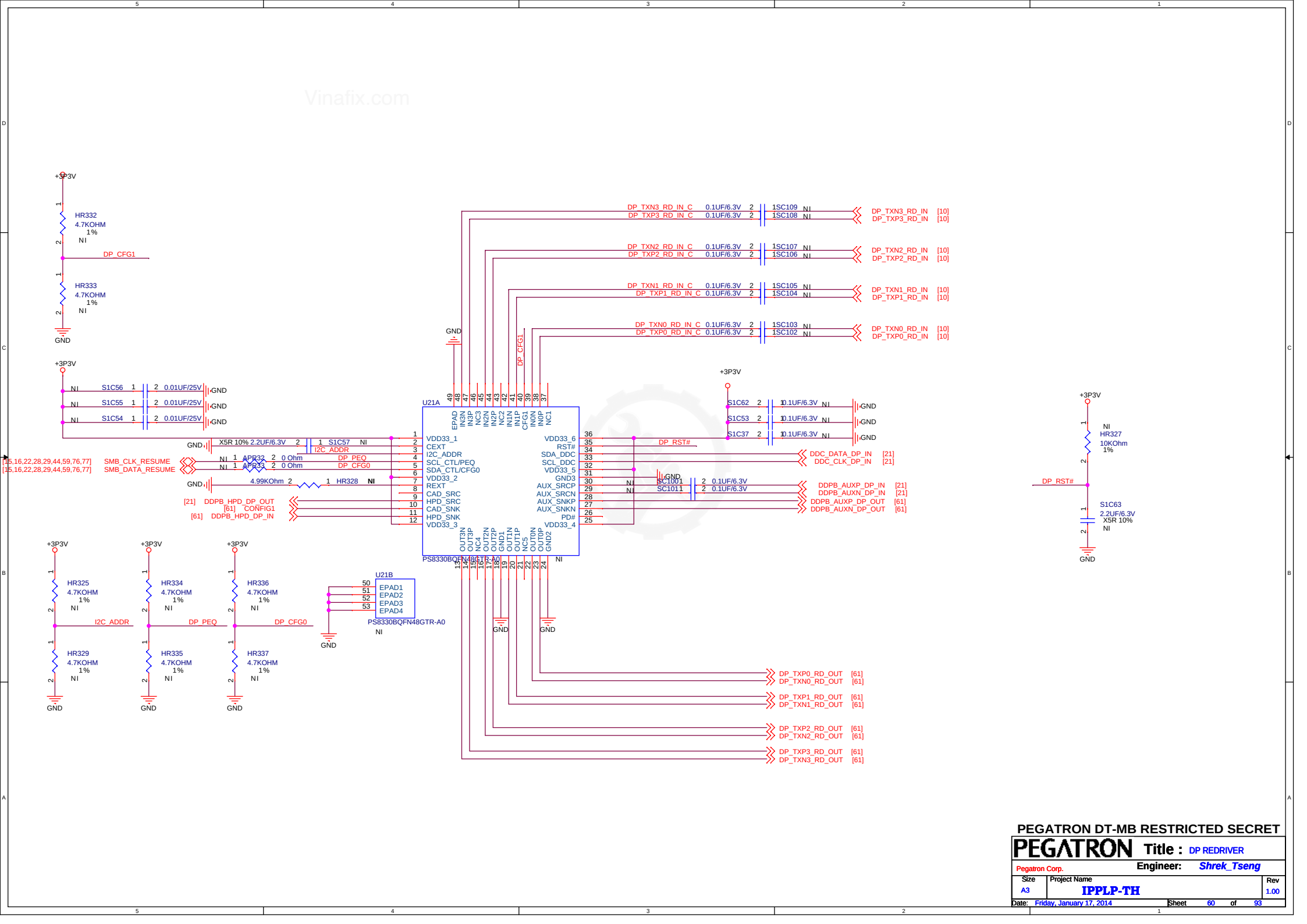
<Core Design>

PEGATRON Title : G-SENSOR

Pegatron Corp. Engineer: Shrek_Tseng

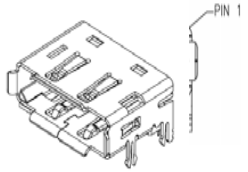
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 59 of 97



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DP REDRIVER	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: 1.00
Date: Friday, January 17, 2014	Sheet 60 of 93	



NOTE:
Install M1Q6 and M1R7
on Intel Ibex Peak platform

Pass gate to prevent back-drive
when sink device is on and
PCH is powered down

[60] DP_TXP0_RD_OUT
[60] DP_TXN0_RD_OUT
[60] DP_TXP1_RD_OUT
[60] DP_TXN1_RD_OUT
[60] DP_TXP2_RD_OUT
[60] DP_TXN2_RD_OUT
[60] DP_TXP3_RD_OUT
[60] DDPB_AUXP_DP_OUT
[60] DDPB_AUXN_DP_OUT
[60] CONFIG1

NI SC64 1 2 0.1UF/6.3V
NI SC65 1 2 0.1UF/6.3V
NI SC66 1 2 0.1UF/6.3V
NI SC67 1 2 0.1UF/6.3V
NI SC68 1 2 0.1UF/6.3V
NI SC69 1 2 0.1UF/6.3V
NI SC70 1 2 0.1UF/6.3V
NI SC71 1 2 0.1UF/6.3V

ML_LANE_0P
ML_LANE_0N
ML_LANE_1P
ML_LANE_1N
ML_LANE_2P
ML_LANE_2N
ML_LANE_3P
ML_LANE_3N

NI
M1U1
CM1213_04SO
DP

NI
M1U2
CM1213_04SO
DP

+5VA
GND

J125
DISPLAY_CON_20P
NI

ML_LANE_0P
ML_LANE_0N
ML_LANE_1P
ML_LANE_1N
ML_LANE_2P
ML_LANE_2N
ML_LANE_3P
ML_LANE_3N
DP_PWR
RETURN
HOT_PLUG_DETECT
AUX_CH_P
AUX_CH_N
CONFIG1
CONFIG2
GND_0
GND_1
GND_2
GND_3
GND_4
P_GND1
P_GND2
P_GND3

+3P3V_DP
NI M1F1 1.1A/6V
DP_3P3V_PWR_FUSE
NI M1C1 0.1UF/6.3V MLCC/+/-10%

+3P3V
NI AP2306GN MQ4
NI VCB155 0.1UF/16V X7R 10%

+12V_HDD
NI SR628 10KOhm
NI SR629 10KOhm

SR142 100KOHM 1% NI
SR143 100KOHM 1% NI
NI SR141 1MOhm 5%
NI SR144 1% 4.99Mohm

DDPB_HPD_DP_IN [60]

PEGATRON Title : DP CONN

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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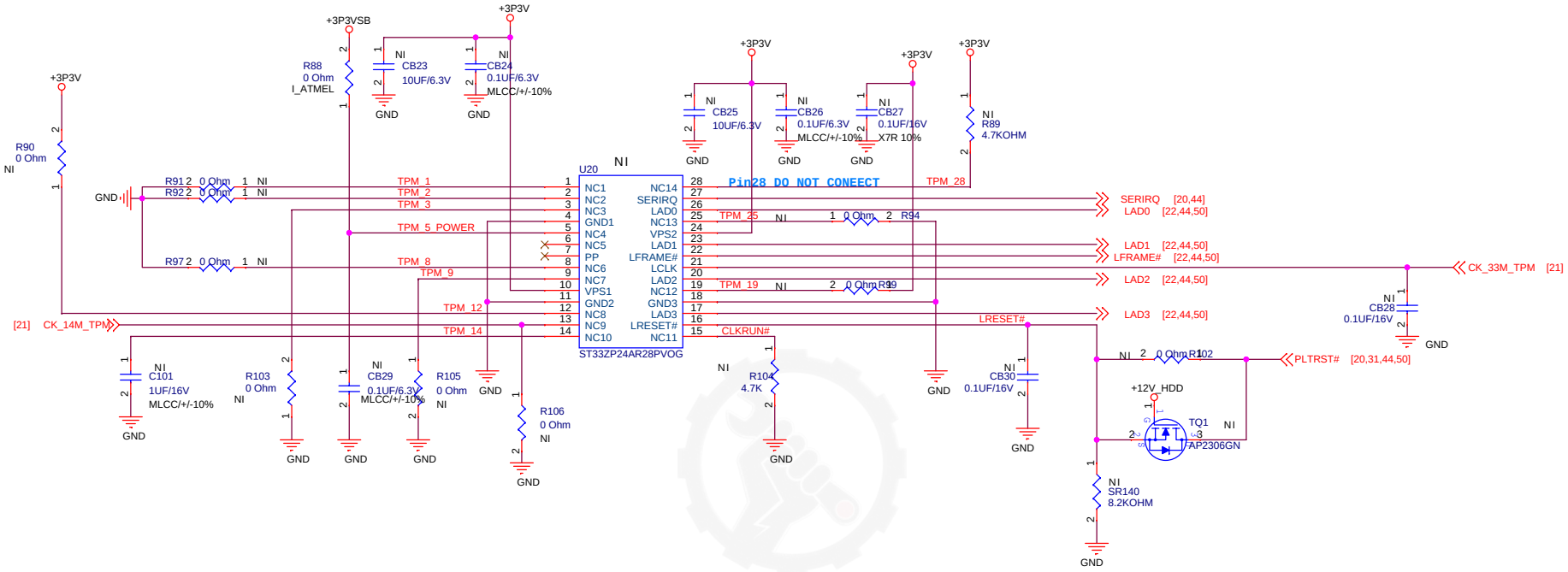


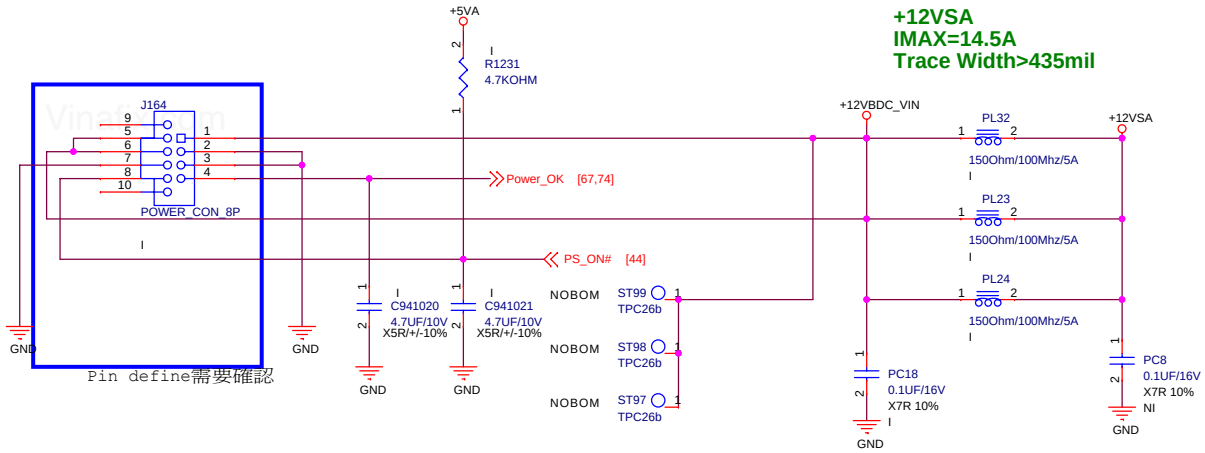
PEGATRON DT-MB RESTRICTED SECRET

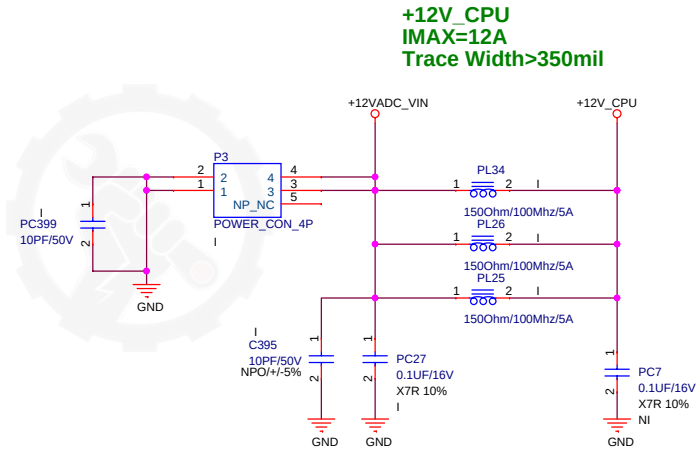
PEGATRON Title : TPM

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	1.00

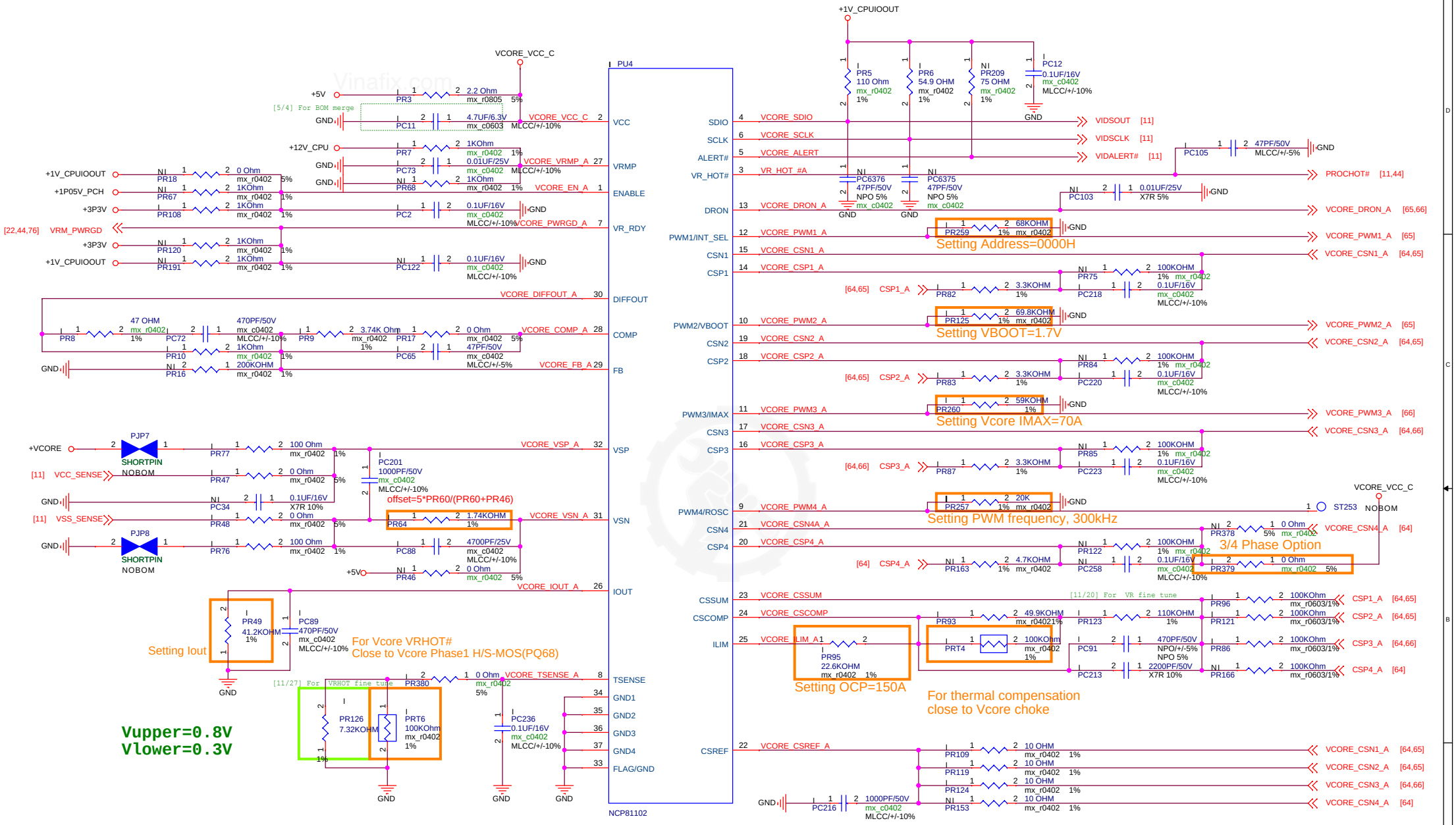
Date: Friday, January 17, 2014 Sheet 62 of 97





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DC IN	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 63 of 97	



<Variant Name>

PEGATRON Title : VCORE CONTROLLER

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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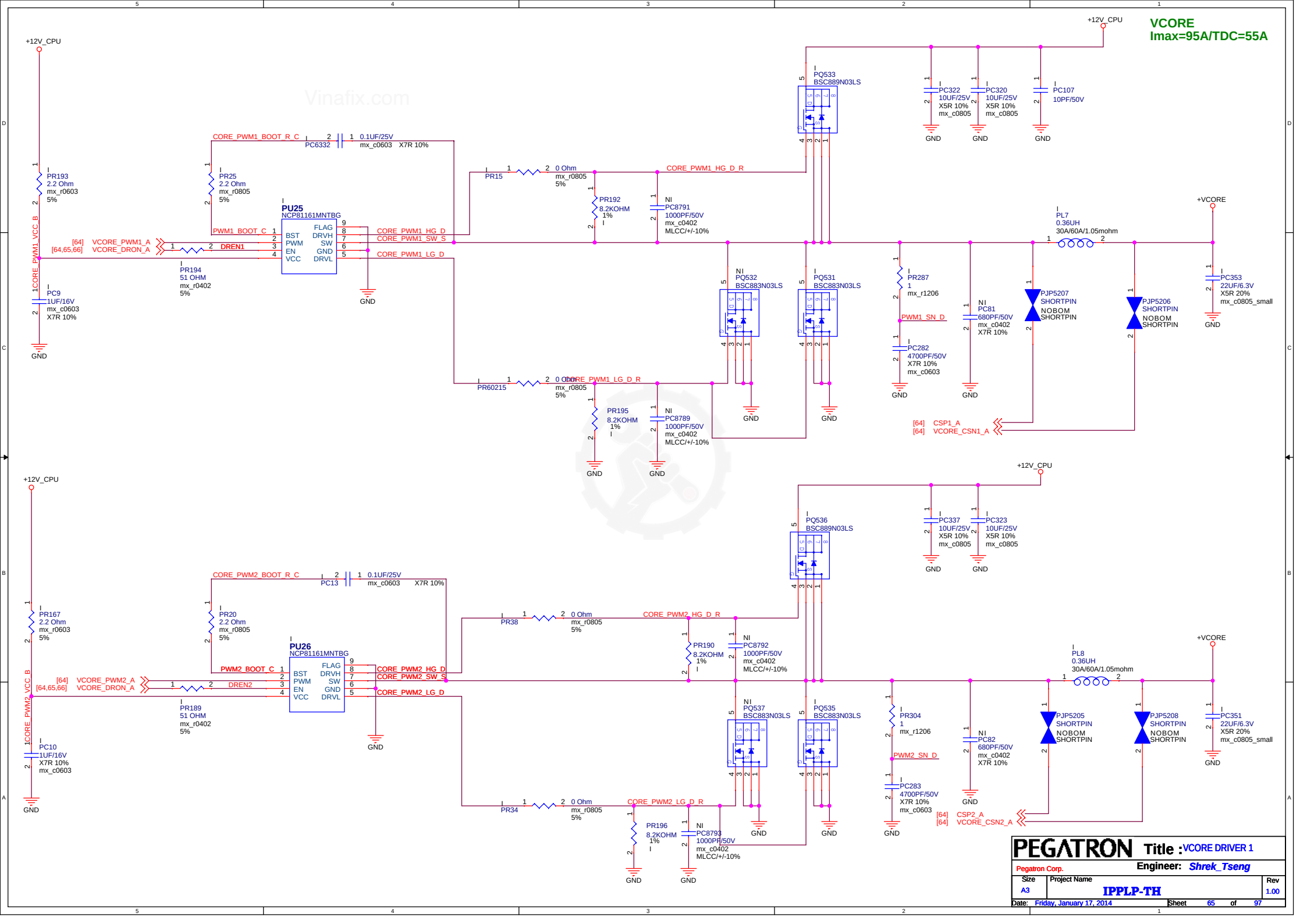

VCORE
Imax=95A/TDC=55A
+12V_CPU
PU25
NCP81161MNTBG
BST
PWM
EN
VCC
FLAG
DRVH
SW
GND
DRVL
CORE_PWM1_BOOT_R_C
PWM1_BOOT_C
CORE_PWM1_HG_D
CORE_PWM1_SW_S
CORE_PWM1_LG_D
DREN1
[64] VCORE_PWM1_A
[64,65,66] VCORE_DRON_A
CORE_PWM1_HG_D_R
CORE_PWM1_LG_D_R
PWM1_SN_D
[64] CSP1_A
[64] VCORE_CSN1_A
+VCORE
PU26
NCP81161MNTBG
CORE_PWM2_BOOT_R_C
PWM2_BOOT_C
CORE_PWM2_HG_D
CORE_PWM2_SW_S
CORE_PWM2_LG_D
DREN2
[64] VCORE_PWM2_A
[64,65,66] VCORE_DRON_A
CORE_PWM2_HG_D_R
CORE_PWM2_LG_D_R
PWM2_SN_D
[64] CSP2_A
[64] VCORE_CSN2_A
PEGATRON
Title : VCORE DRIVER 1
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev 1.00
Date: Friday, January 17, 2014
Sheet 65 of 97

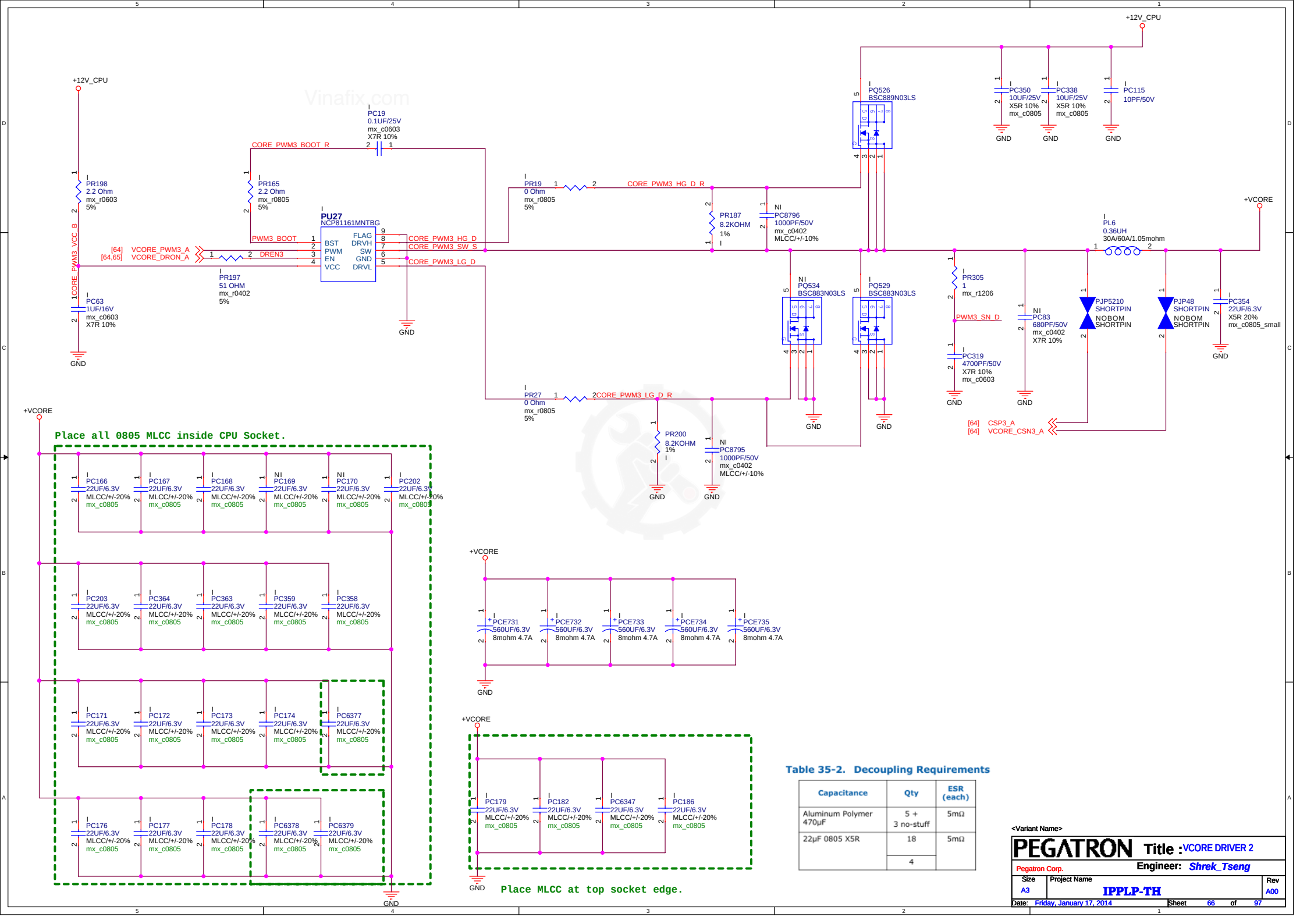


Table 35-2. Decoupling Requirements

Capacitance	Qty	ESR (each)
Aluminum Polymer 470µF	5 + 3 no-stuff	5mΩ
22µF 0805 X5R	18	5mΩ
	4	

<Variant Name>

PEGATRON Title : VCORE DRIVER 2

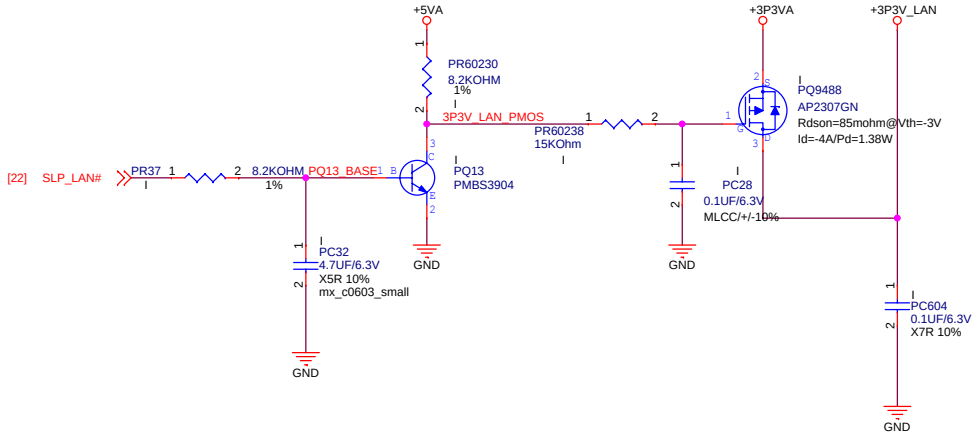
Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 66 of 97

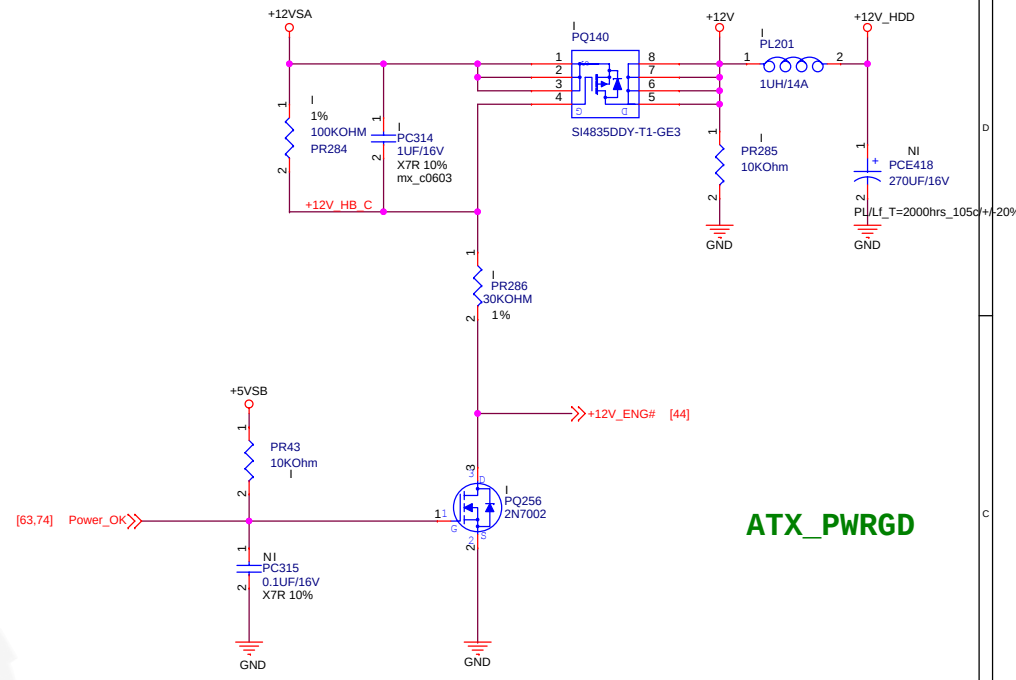
+3.3V_LAN
Imax=0.188A

Vdroop: 0.188A*218mohm=40mV



+12V/Imax:10A/TDC:7A

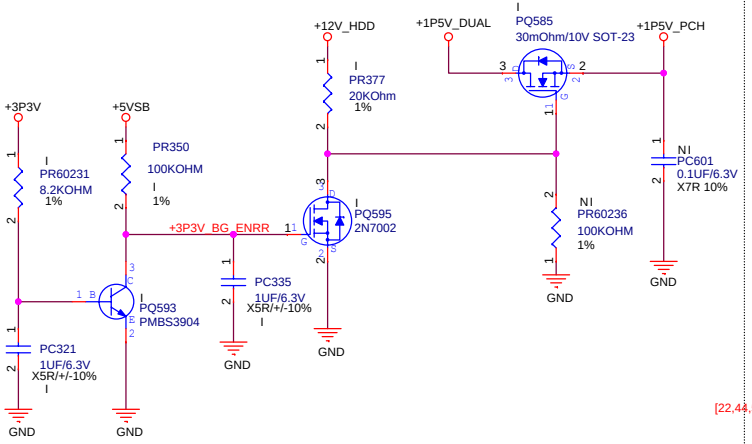
Vdroop: 7A*18mohm=126mV



ATX_PWRGD

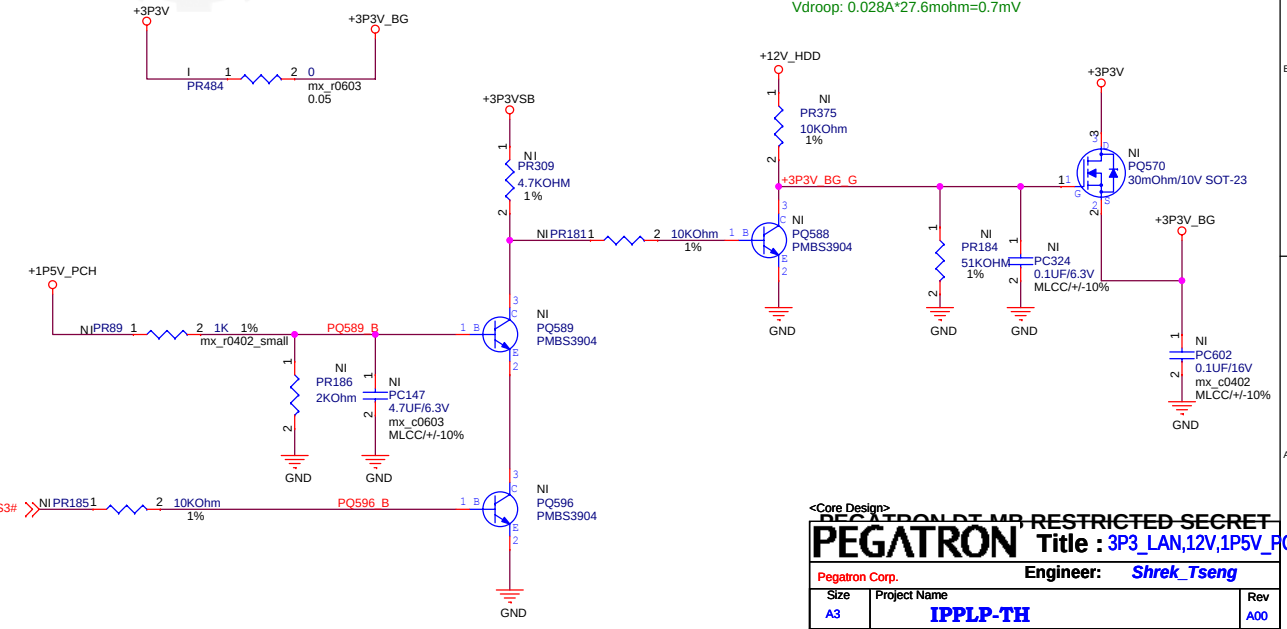
+1P5V_PCH/Imax:0.36A

Vdroop: 0.36A*27.6mohm=19mV



+3P3V_BG/Imax:0.028A

Vdroop: 0.028A*27.6mohm=0.7mV



<Core Design>

PEGATRON RESTRICTED SECRET

PEGATRON Title : 3P3_LAN,12V,1P5V_PCH,3

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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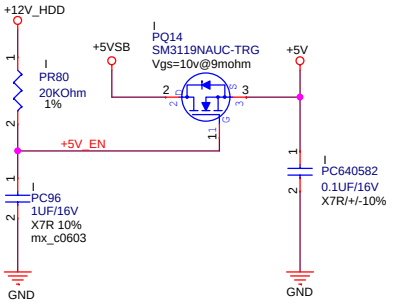
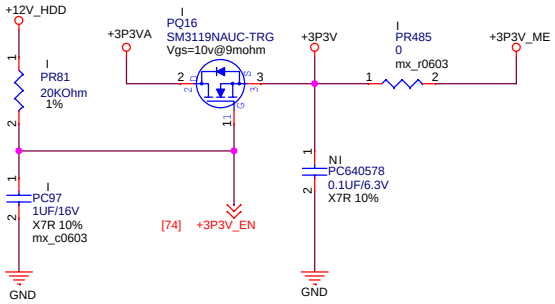
+5V/Imax:6.42A/TDC:4.5A

Vdroop: 4.5A*9mohm=40.5mV



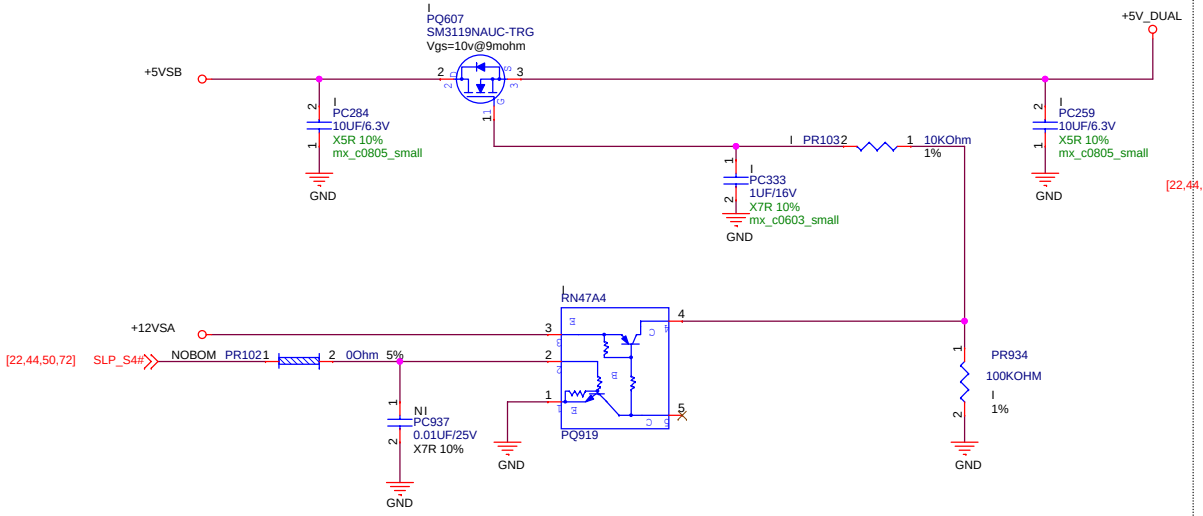
+3P3V/Imax:8.57A/TDC:6A

Vdroop: 6A*9mohm=54mV



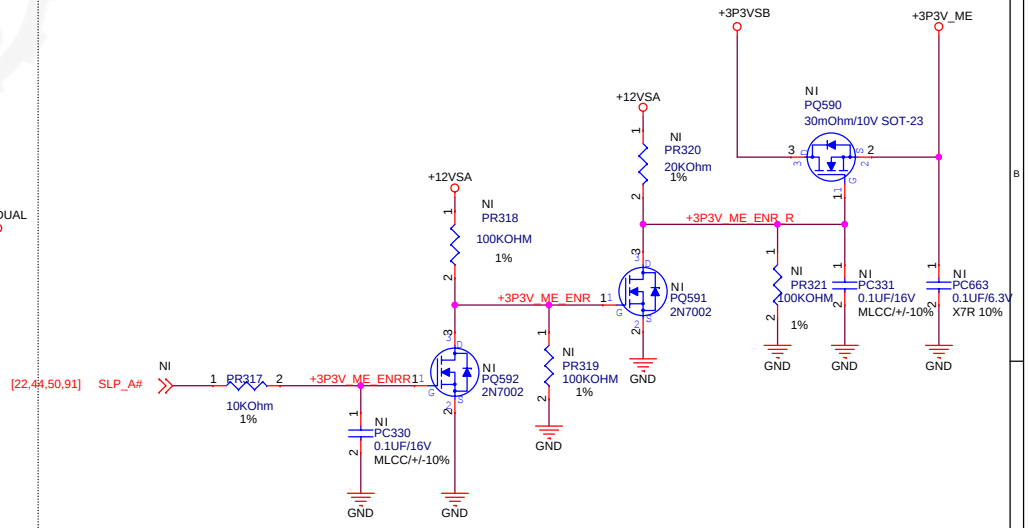
+5V_DUAL / TDC:8.5A

Vdroop = 8.5A*13.8m = 117mV



+3P3V_ME/Imax:0.03A

Vdroop: 0.03A*27.6mohm=1mV



PEGATRON Title : 5V, 3P3V, 1P5V, 5V_Dual

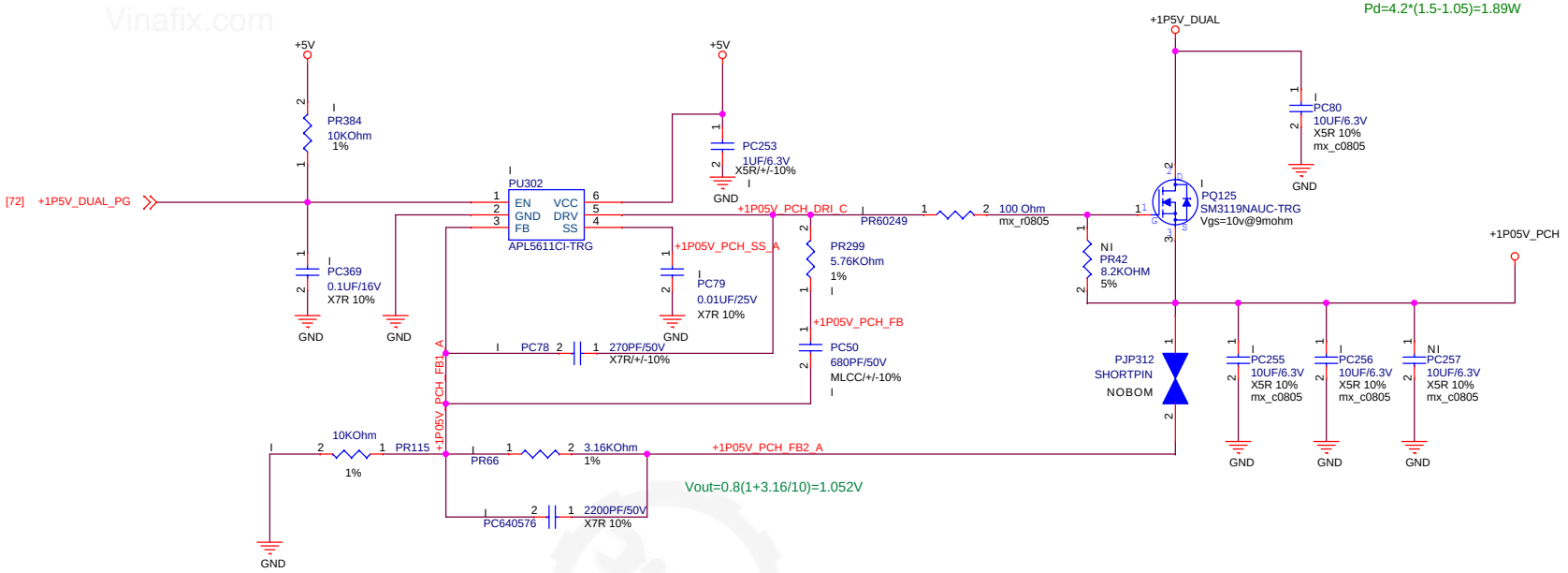
Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 68 of 97

+1P05V_PCH Imax=6A

Pd=4.2*(1.5-1.05)=1.89W

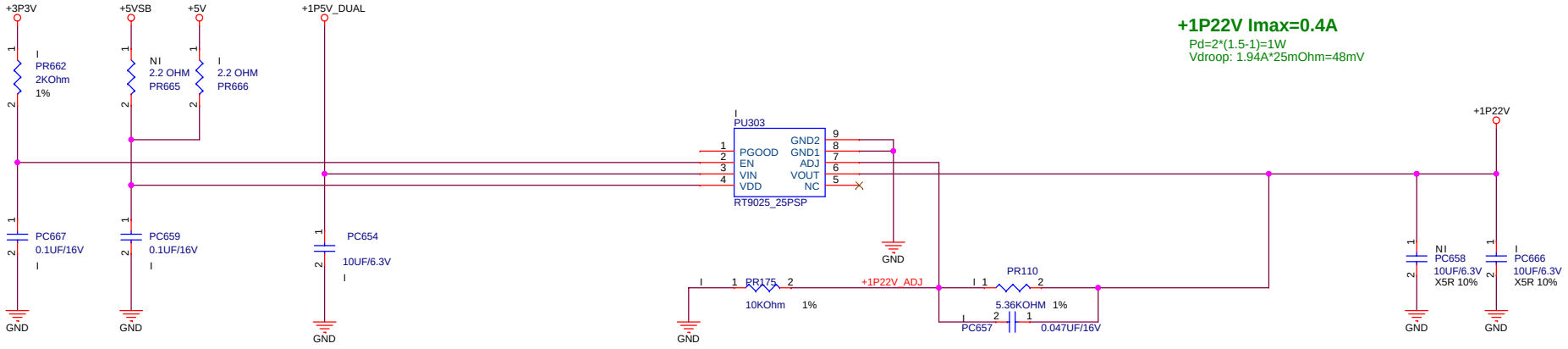


Vout=0.8(1+3.16/10)=1.052V

+1P22V Imax=0.4A

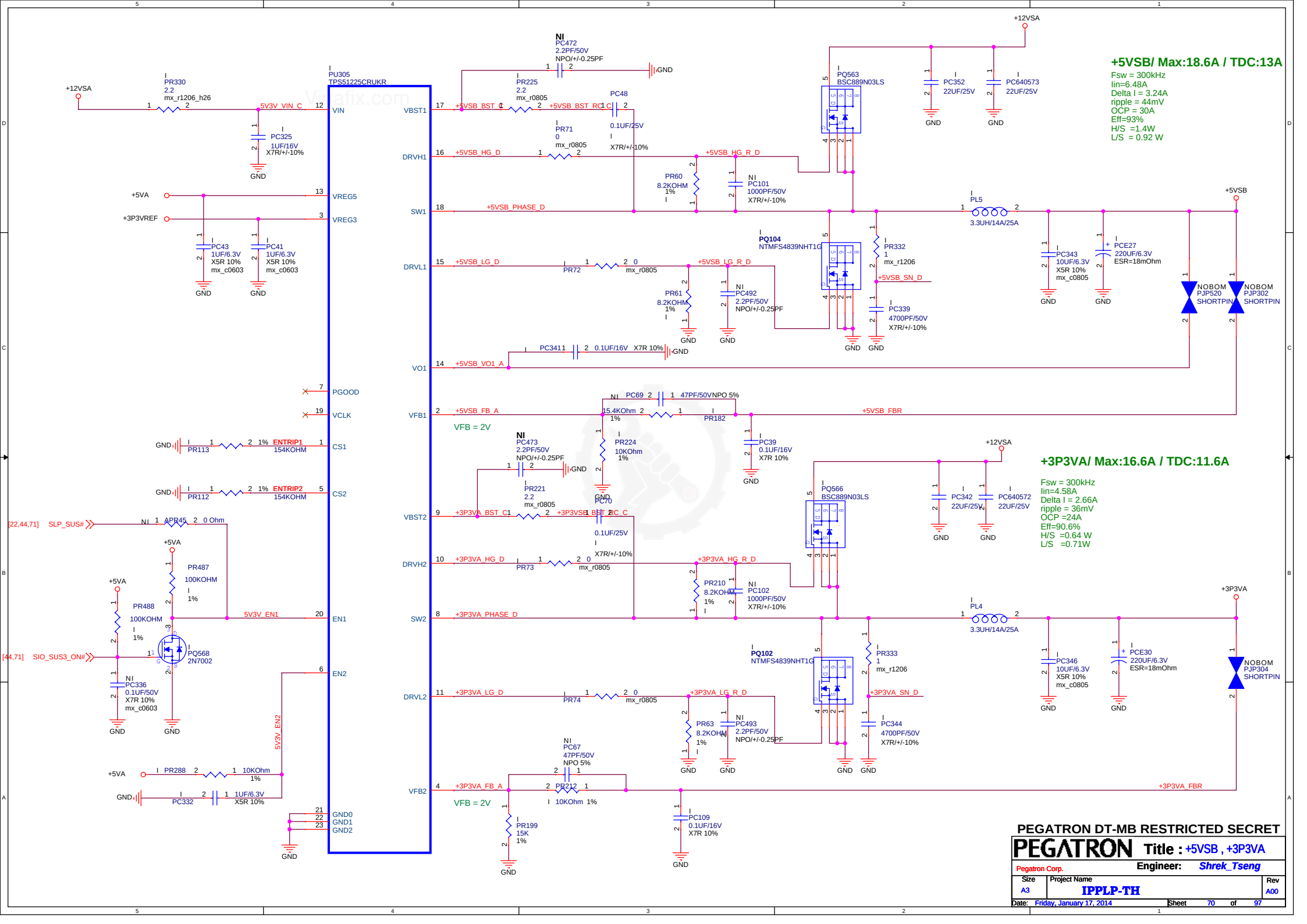
Pd=2*(1.5-1)=1W

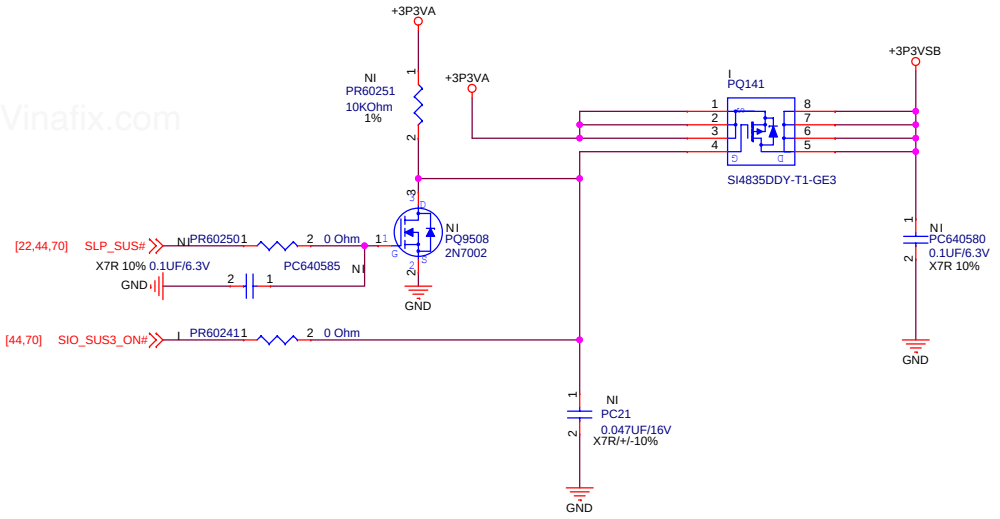
Vdroop: 1.94A*25mOhm=48mV



Vout=((6.34K/10K)+1)*0.75V=1.22V

PEGATRON	Title :	+1P05V_PCH & +1P22	
Pegatron Corp.	Engineer:	Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH		Rev: A00
Date: Friday, January 17, 2014	Sheet 69 of 97		

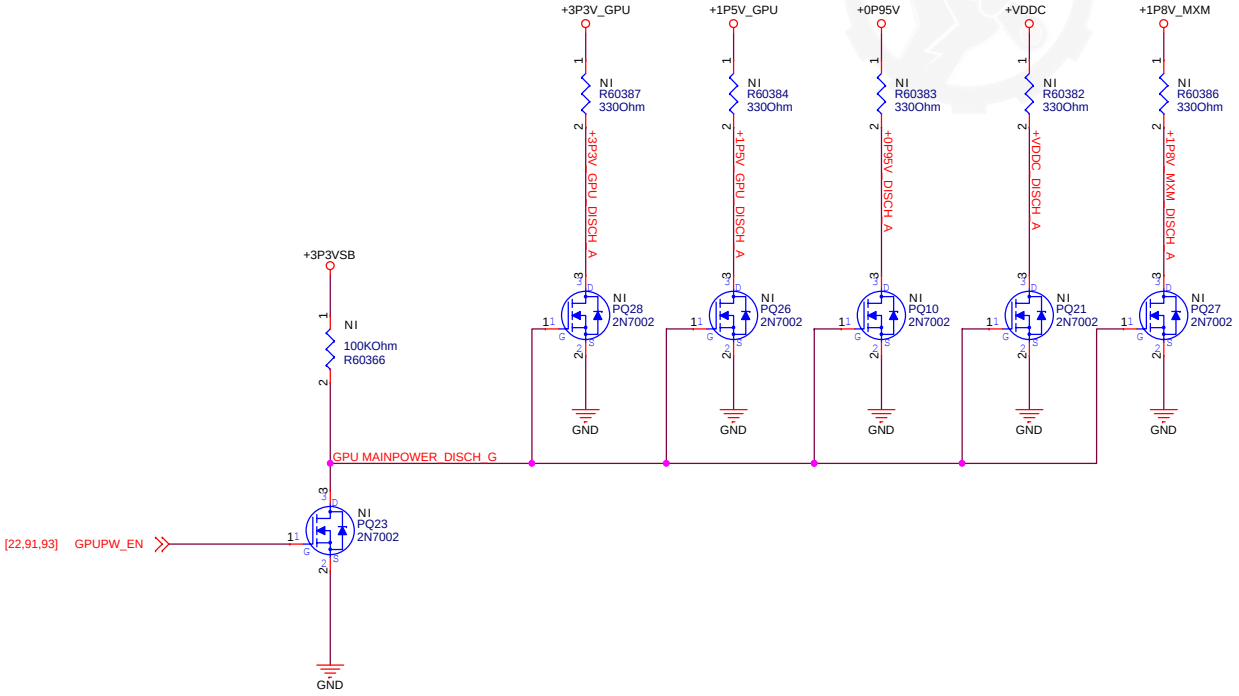

+5VSB/ Max:18.6A / TDC:13A
Fsw = 300kHz
Iin=6.48A
Delta I = 3.24A
ripple = 44mV
OCP = 30A
Eff=93%
H/S =1.4W
L/S = 0.92 W
+3P3VA/ Max:16.6A / TDC:11.6A
Fsw = 300kHz
Iin=4.58A
Delta I = 2.66A
ripple = 36mV
OCP =24A
Eff=90.6%
H/S =0.64 W
L/S =0.71W
PU305
TPS51225CRUKR
VFB = 2V
VFB = 2V
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : +5VSB , +3P3VA
Pegatron Corp.
Engineer: Shrek_Tseng
Size A3
Project Name IPPLP-TH
Rev A00
Date: Friday, January 17, 2014
Sheet 70 of 97



+3P3VSB/TDC:3.8A

Vdroop =3.8A*35mohm = 133mV

GPU POWER DISCHARGE



<Variant Name>

PEGATRON	Title :	+3P3VSB & GPU DISCHAR
Pegatron Corp.	Engineer:	Shrek_Tseng
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 71 of 97	

+1P5V_DUAL / Max:28A / TDC:19.6A

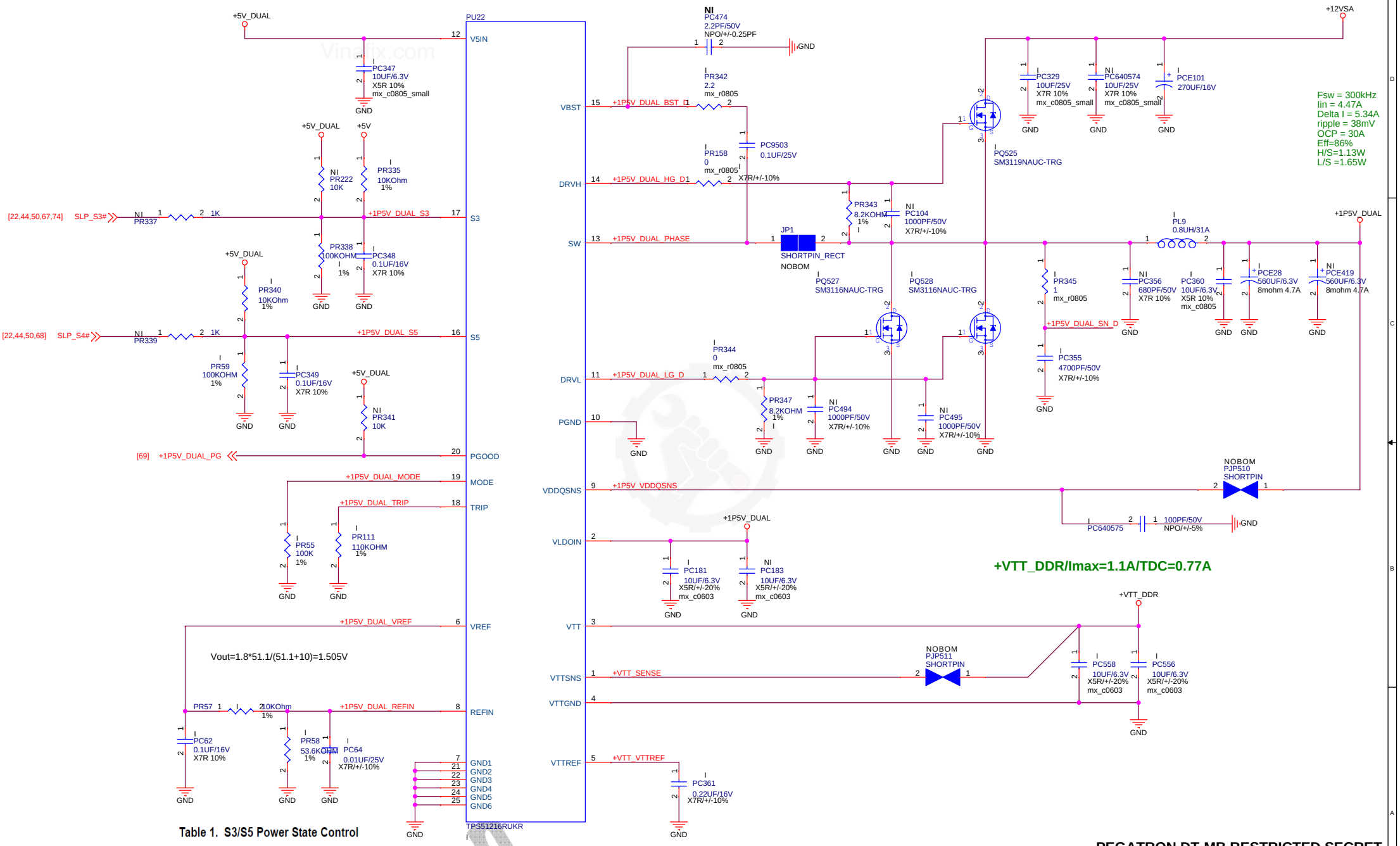


Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P5V_DUAL & +VTT_DDR

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 72 of 97

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : XXXXXX

Pegatron Corp. Engineer: Shrek_Tseng

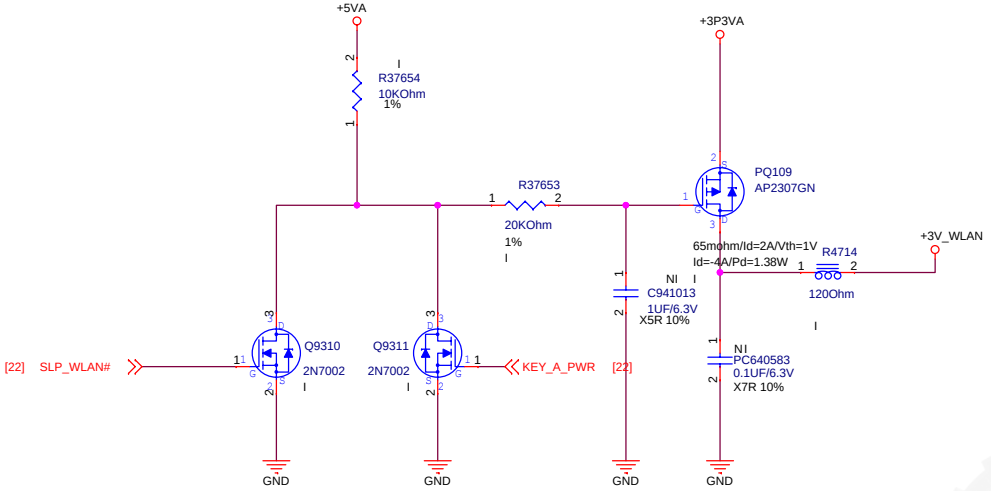
Size	Project Name	Rev
A3	IPPLP-TH	A00

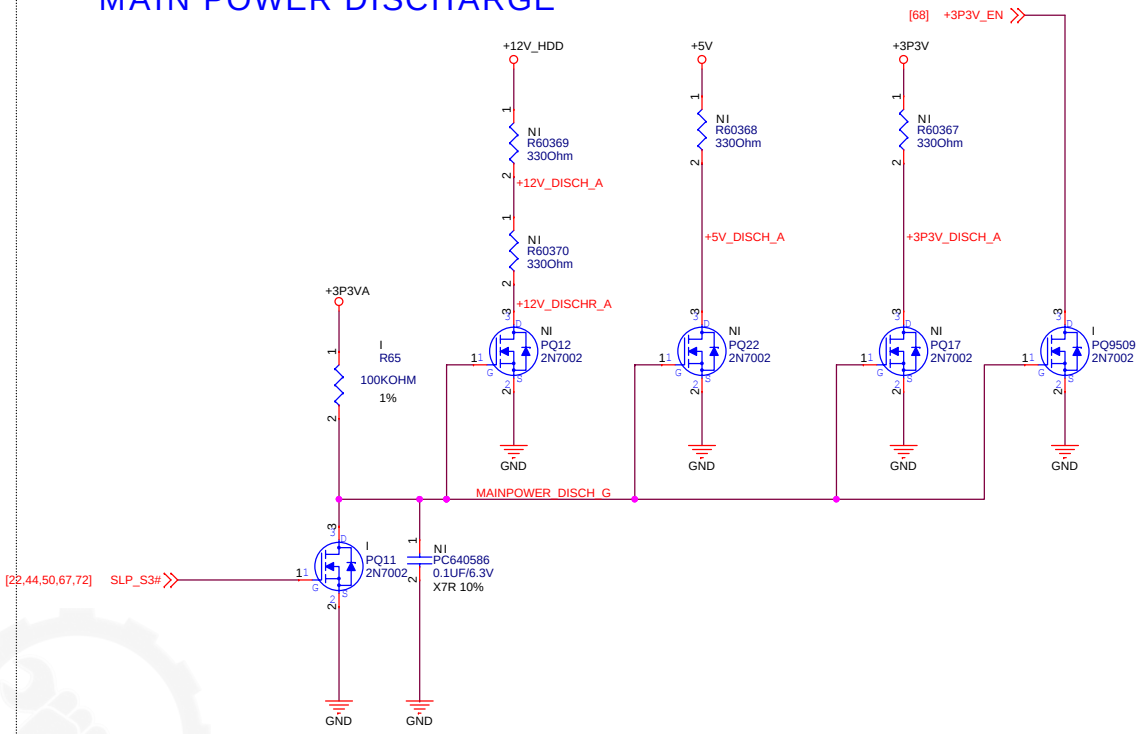
Date: Friday, January 17, 2014 Sheet 73 of 97

MAIN POWER DISCHARGE

+3P3V_WLAN
Imax=2A /TDC=1.4A

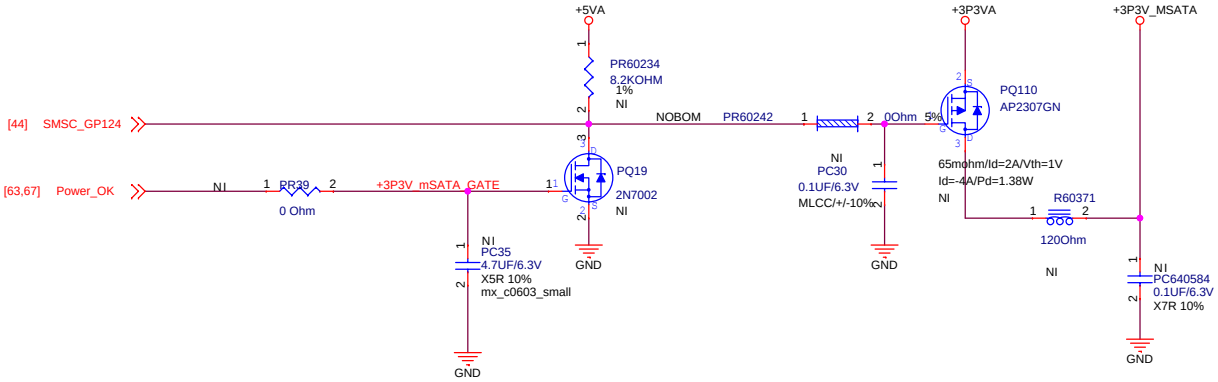
Vdroop: 1.4A*65mohm=91mV >3.3*0.95





+3P3V_mSATA
Imax=2.5A/TDC=1.75A

Vdroop: 1.75A*65mohm=113mV



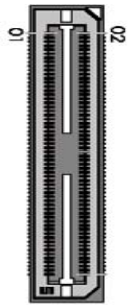
PEGATRON Title : +3P3V_WLAN & +3P3V_MS

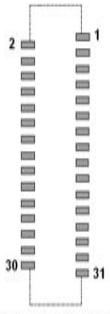
Pegatron Corp. Engineer: Shrek_Tseng

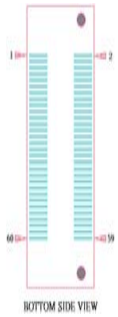
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 74 of 97

INTEL CPU XDP DEBUG PORT







NOTE:
Place near XDP connector

XDP1

+1V_CPUIOOUT
NI HCB2 0.1UF/16V
GND

+1P05V_PCH
PROTO HR91 51
NI HR92 820 1%
GND

[11] CPU_CFG[0..15]

CPU_CFG0
CPU_CFG1
CPU_CFG2
CPU_CFG3
CPU_CFG4
CPU_CFG5
CPU_CFG6
CPU_CFG7
CPU_CFG8
CPU_CFG9
CPU_CFG10
CPU_CFG11
CPU_CFG12
CPU_CFG13
CPU_CFG14
CPU_CFG15

[11] H_PREQ#
[11] H_PRDY#
[11] HSW_XDP_MBP0
[11] HSW_XDP_MBP1
[11] HSW_PCUSTB_DP0
[11] HSW_PCUSTB_DN0
[11] HSW_PCUSTB_DP1
[11] HSW_PCUSTB_DN1

[21] CK_100M_CPUXDP
[21] CK_100M_CPUXDP#
NI HR95 1 2 0 CPU_ITPCLK_HOOK4
NI HR97 1 2 0 CPU_ITPCLK#_HOOK5

NOTE:
Please close to each other to reduse stub.

[15,16,22,28,29,44,59,60,77] SMB_DATA_RESUME
[15,16,22,28,29,44,59,60,77] SMB_CLK_RESUME

43	VCC_OBS_AB	TCK1	55
44	VCC_OBS_CD	TCK0	57
		TDO	52
		TRSTn	54
		TDI	56
		TMS	58
3	OBSFN_A0	HOOK0	39
5	OBSFN_A1		
9	OBSDATA_A0		
11	OBSDATA_A1		
15	OBSDATA_A2		
17	OBSDATA_A3		
21	OBSFN_B0		
23	OBSFN_B1		
27	OBSDATA_B0		
29	OBSDATA_B1		
33	OBSDATA_B2		
35	OBSDATA_B3		
40	ITPCLK/HOOK4	HOOK1	41
42	ITPCLK#/HOOK5	HOOK2	45
		HOOK3	47
		HOOK6/RESET#	46
		HOOK7/DBR#	48
51	SDA		
53	SCL		
4	OBSFN_C0		
6	OBSFN_C1		
10	OBSDATA_C0		
12	OBSDATA_C1		
16	OBSDATA_C2		
18	OBSDATA_C3		
22	OBSFN_D0		
24	OBSFN_D1		
28	OBSDATA_D0		
30	OBSDATA_D1		
34	OBSDATA_D2		
36	OBSDATA_D3		

GND1 1
GND2 2
GND3 7
GND4 8
GND5 13
GND6 14
GND7 19
GND8 20
GND9 25
GND10 26
GND11 31
GND12 32
GND13 37
GND14 38
GND15 49
GND16 50
GND17 59
GND18 60
NP_NC1 61
NP_NC2 62
GND

BtoB_CON_60P
PROTO

TCK [11]
TDO [11]
TRST# [11]
TDI [11]
TMS [11]

XDP_CPUPWRGD# R
PROTO HR93 1% 1K mx_r0402_small
XDP_CPUPWRGD# [11]

NOTE:
TBD. PDG and DPDG is 1KΩ
Follow PDG 0.9 is 1KΩ

NI HR94 1K
GND

CPUXDP_HOOK1
CPUXDP_HOOK3
PLTRST_CPU#_HOOK6

PROTO HR96 2 1 3.3KOHM 1%
PROTO HR98 1 2 0

PWRBTN# [22,44,50,55,77]
XDP_PWR_DEBUG [11]
VRM_PWRGD [22,44,64]
XDP_PLTRST_CPU# [11]
SYS_RESET# [11,22,50,77]

NI HC8 470PF/50V
GND

PRIVACY_MSR_EN_N [11]

NOBOM PT156 1
NOBOM PT157 1
NOBOM PT158 1
NOBOM PT159 1
GND

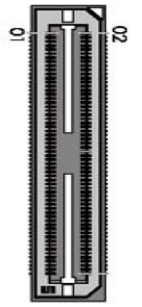
PEGATRON Title : CPU XDP DEBUG

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

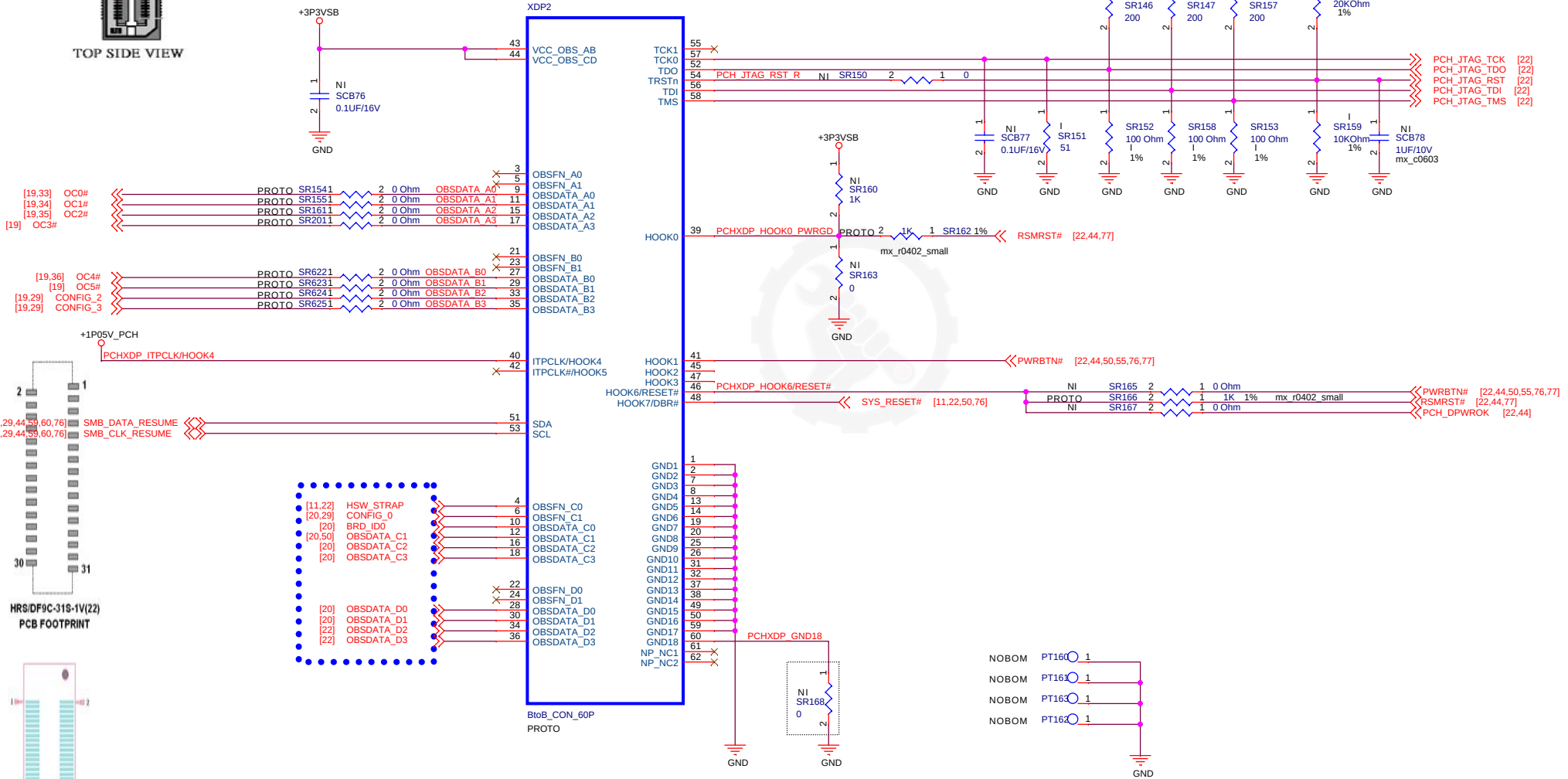
Date: Friday, January 17, 2014 Sheet 76 of 97

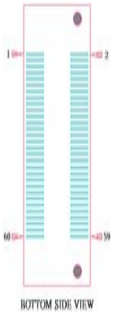
INTEL PCH XDP DEBUG PORT



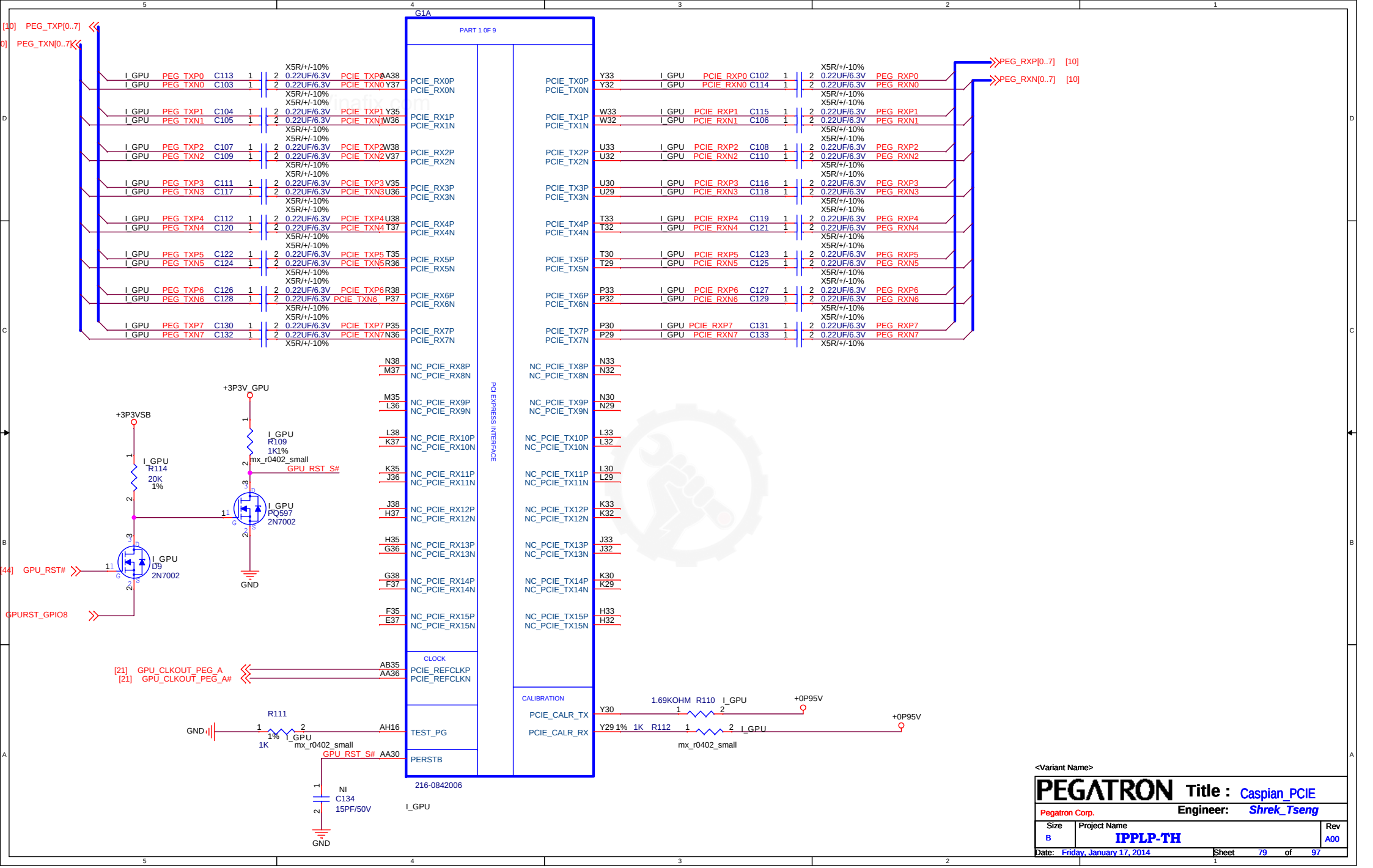
TOP SIDE VIEW

NOTE:
Place strap resistors of TDO near to XDP connector,
and TDI and TMS near to CPU.





PEGATRON	Title : PCH XDP DEBUG	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A3	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 77 of 97	



<Variant Name>

PEGATRON

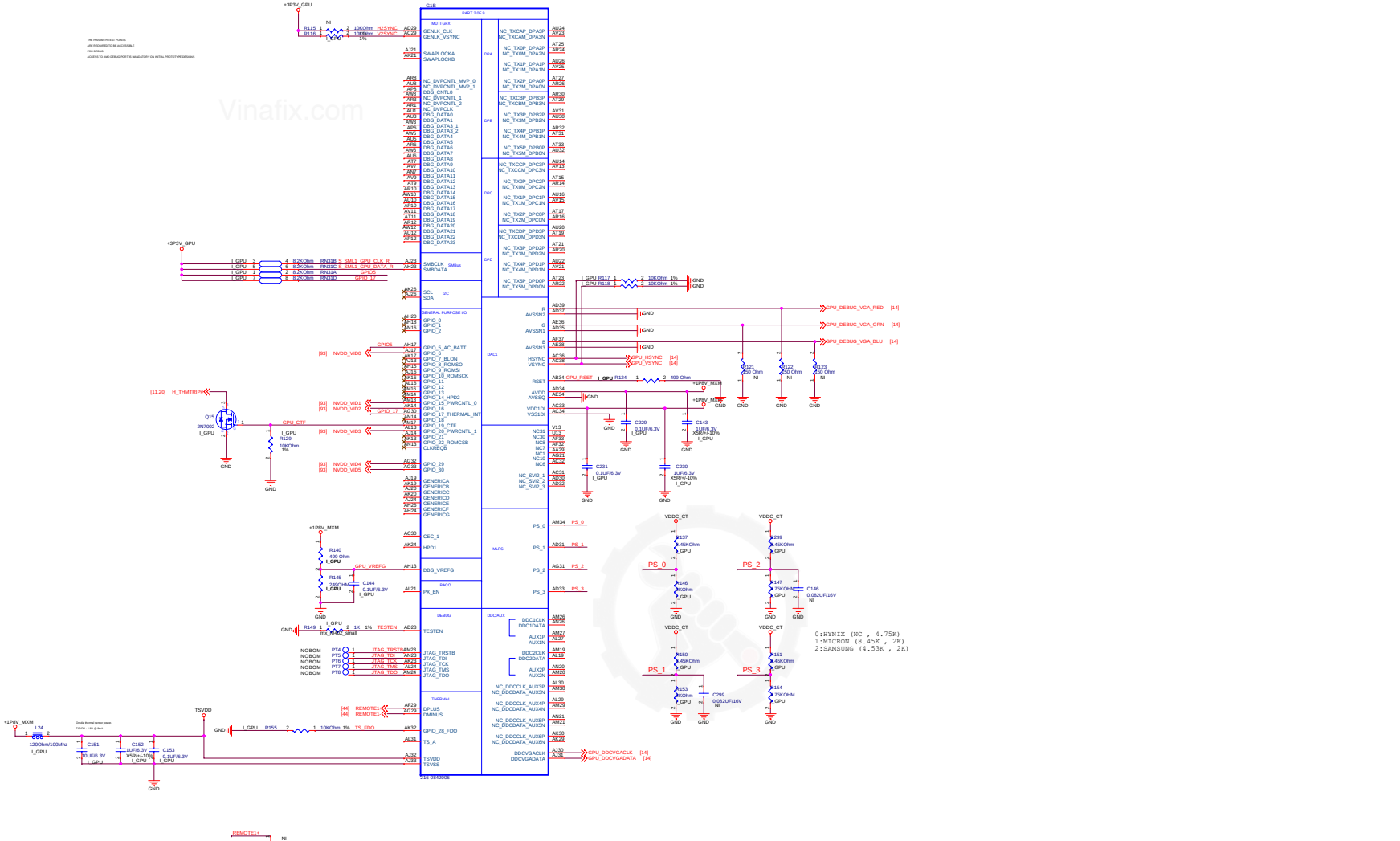
Title : Caspian_PCIE

Pegatron Corp.

Engineer: Shrek_Tseng

Size	Project Name	Rev
B	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 79 of 97


+3P3V_GPU
G1B
PART 2 OF 9
MUTI GFX
GENLK_CLK
GENLK_VSYNC
SWAPLOCKA
SWAPLOCKB
NC_DVPCNTL_MVP_0
NC_DVPCNTL_MVP_1
DBG_CNTL0
NC_DVPCNTL_1
NC_DVPCNTL_2
NC_DVPCLK
DBG_DATA0
DBG_DATA1
DBG_DATA3_1
DBG_DATA3_2
DBG_DATA4
DBG_DATA5
DBG_DATA6
DBG_DATA7
DBG_DATA8
DBG_DATA9
DBG_DATA10
DBG_DATA11
DBG_DATA12
DBG_DATA13
DBG_DATA14
DBG_DATA15
DBG_DATA16
DBG_DATA17
DBG_DATA18
DBG_DATA19
DBG_DATA20
DBG_DATA21
DBG_DATA22
DBG_DATA23
SMBCLK
SMBDATA
SCL
SDA
GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16
GPIO_17_THERMAL_INT
GPIO_18
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21
GPIO_22_ROMCSB
CLKREQB
GPIO_29
GPIO_30
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE
GENERICF
GENERICG
CEC_1
HPD1
DBG_VREFG
PX_EN
DEBUG
TESTEN
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
THERMAL
DPLUS
DMINUS
GPIO_28_FDO
TS_A
TSVDD
TSVSS
DPA
DPB
DPC
DPD
DAC1
MLPS
BACO
DDC/AUX
PS_0
PS_1
PS_2
PS_3
DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCVGACLK
DDCVGADATA
216-0842008
R115
R116
10KOhm_H2SYNC
10KOhm_V2SYNC
NI
5%
THE PAD WITH TEST POINTS
ARE REQUIRED TO BE ACCESSIBLE
FOR DRMO.
ACCESS TO AMD DEBUG PORT IS MANDATORY ON INITIAL PROTOTYPE DESIGNS.
Vinafix.com
+3P3V_GPU
I_GPU_3
I_GPU_5
I_GPU_1
I_GPU_7
8.2KOhm
RN31B
RN31C
RN31A
RN31D
S_SML1_GPU_CLK_R
S_SML1_GPU_DATA_R
GPIO5
GPIO_17
[93] NVDD_VID0
[93] NVDD_VID1
[93] NVDD_VID2
[93] NVDD_VID3
[93] NVDD_VID4
[93] NVDD_VID5
[11,20] H_THMTRIPB
Q15
2N7002
I_GPU
R129
10KOhm
1%
GPU_CTF
GND
+1P8V_MXM
R140
499 Ohm
R145
249OHM
C144
0.1UF/6.3V
GPU_VREFG
R149
1K
TESTEN
NOBOM
PTS
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TSVDD
L24
120Ohm/100Mhz
C151
10UF/6.3V
C152
C153
0.1UF/6.3V
R155
10KOhm
TS_FDO
[44] REMOTE1+
[44] REMOTE1-
REMOTE1+
REMOTE1-
C154
100PF/25V
NI
NOTE:
The current numbers shown here are for reference only
For actual current, check with databook
I_GPU R117
I_GPU R118
10KOhm 1%
GND
AVSSN2
AVSSN1
AVSSN3
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD10
VSS10
GPU_HSYNC
GPU_VSYNC
GPU_DEBUG_VGA_RED
GPU_DEBUG_VGA_GRN
GPU_DEBUG_VGA_BLU
GPU_RSET
R124
499 Ohm
+1P8V_MXM
R121
R122
R123
150 Ohm
C229
C143
C231
C230
0.1UF/6.3V
1UF/6.3V
X5R/+-10%
I_GPU
NC1
NC30
NC8
NC7
NC5
NC6
NC_SVI2_1
NC_SVI2_2
NC_SVI2_3
VDDC_CT
R137
R146
R150
R153
R209
R147
R151
R154
45KOhm
75KOhm
C209
C146
0.082UF/16V
0:HYNIX (NC , 4.75K)
1:MICRON (8.45K , 2K)
2:SAMSUNG (4.53K , 2K)

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

For Thames/Whistler/Seymour

a dedicated BEAD is required

for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

For Thames/Whistler/Seymour

a dedicated BEAD is required

for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

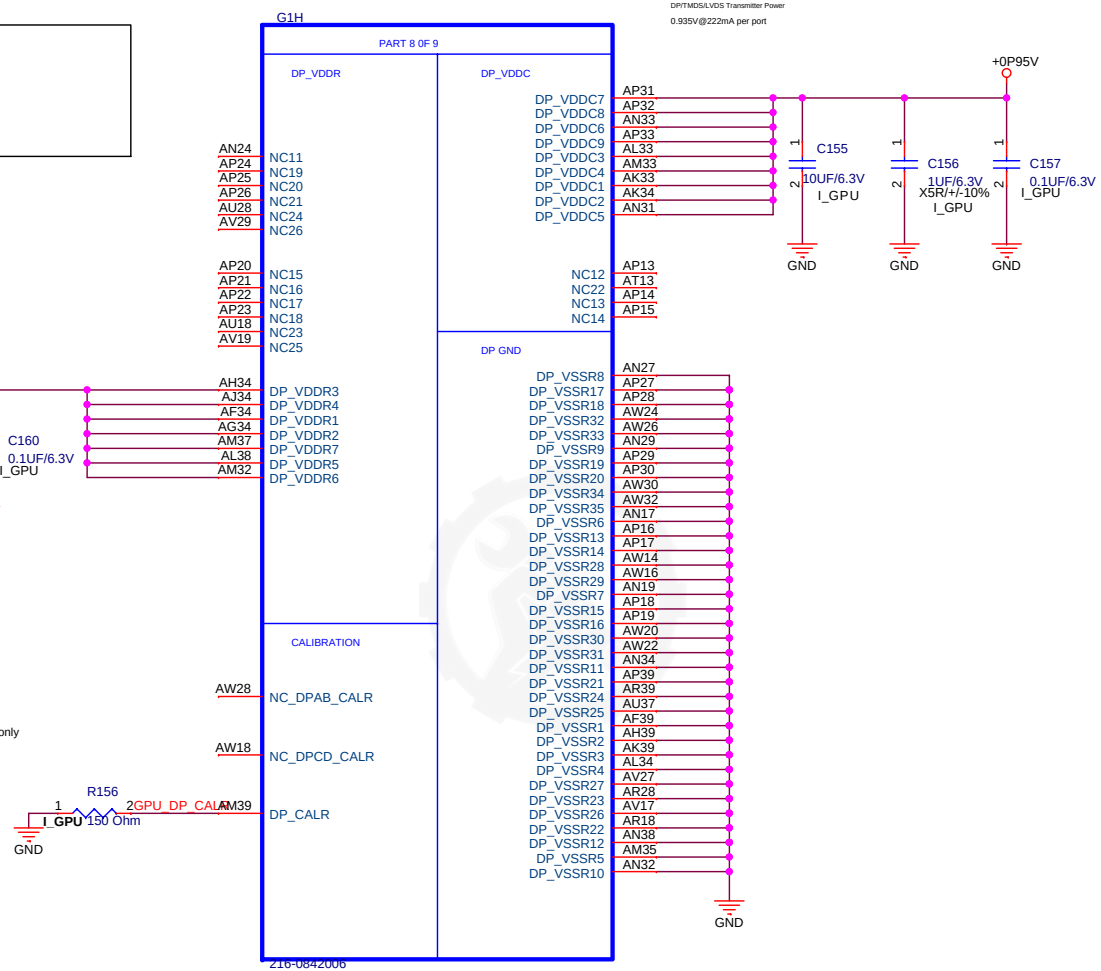
DP/TMDS/LVDS Transmitter Power

DP mode: 1.8V@188mA per port

HDMI mode: 1.8V@237mA per port

DP/TMDS/LVDS Transmitter Power

0.935V@222mA per port



NOTE:

The current numbers shown here are for reference only

For actual current, check with databook

<Variant Name>

PEGATRON Title : Caspian_DP A--D

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
B	IPPLP-TH	A00

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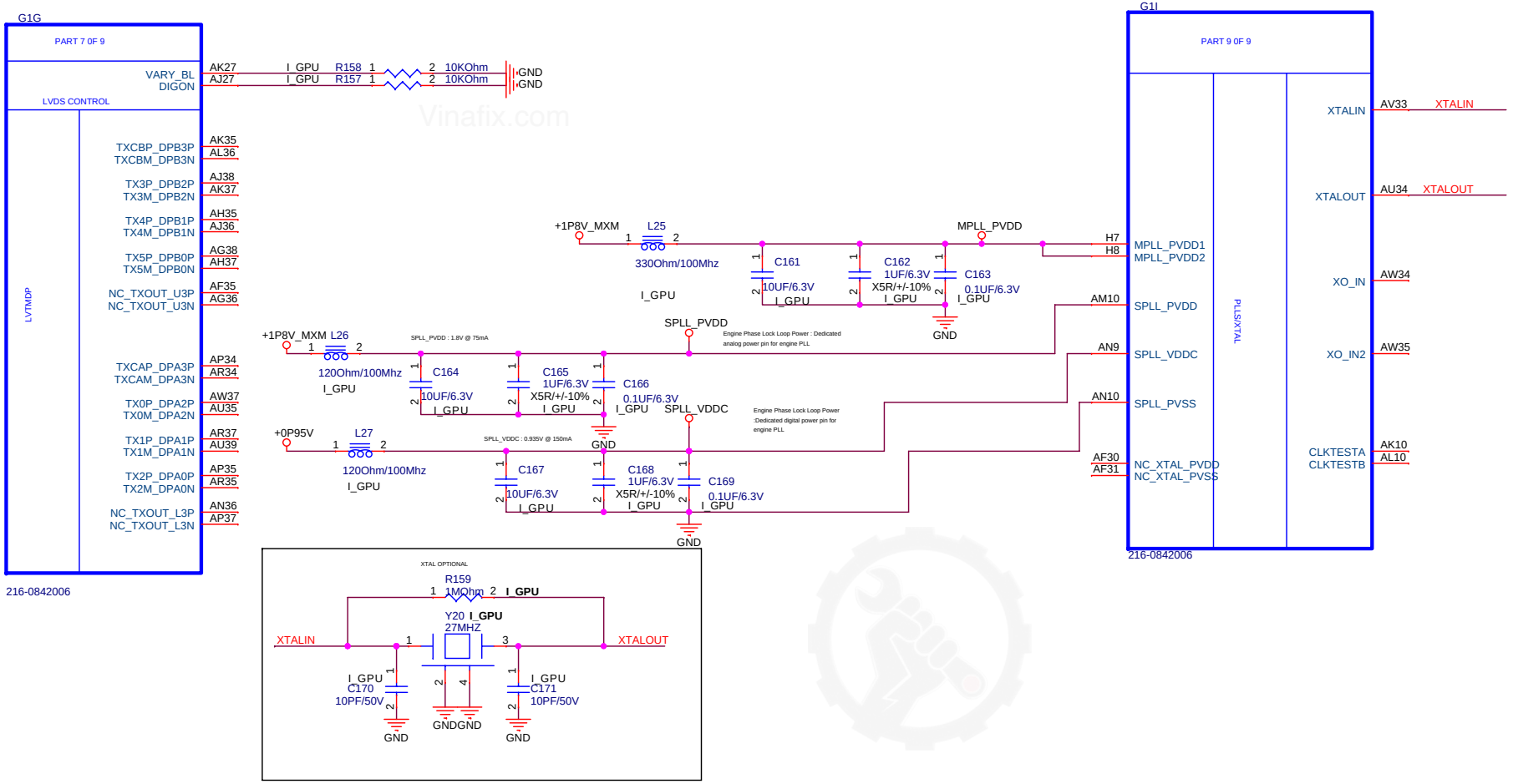


<Variant Name>

PEGATRON Title : Caspian_LVDS1

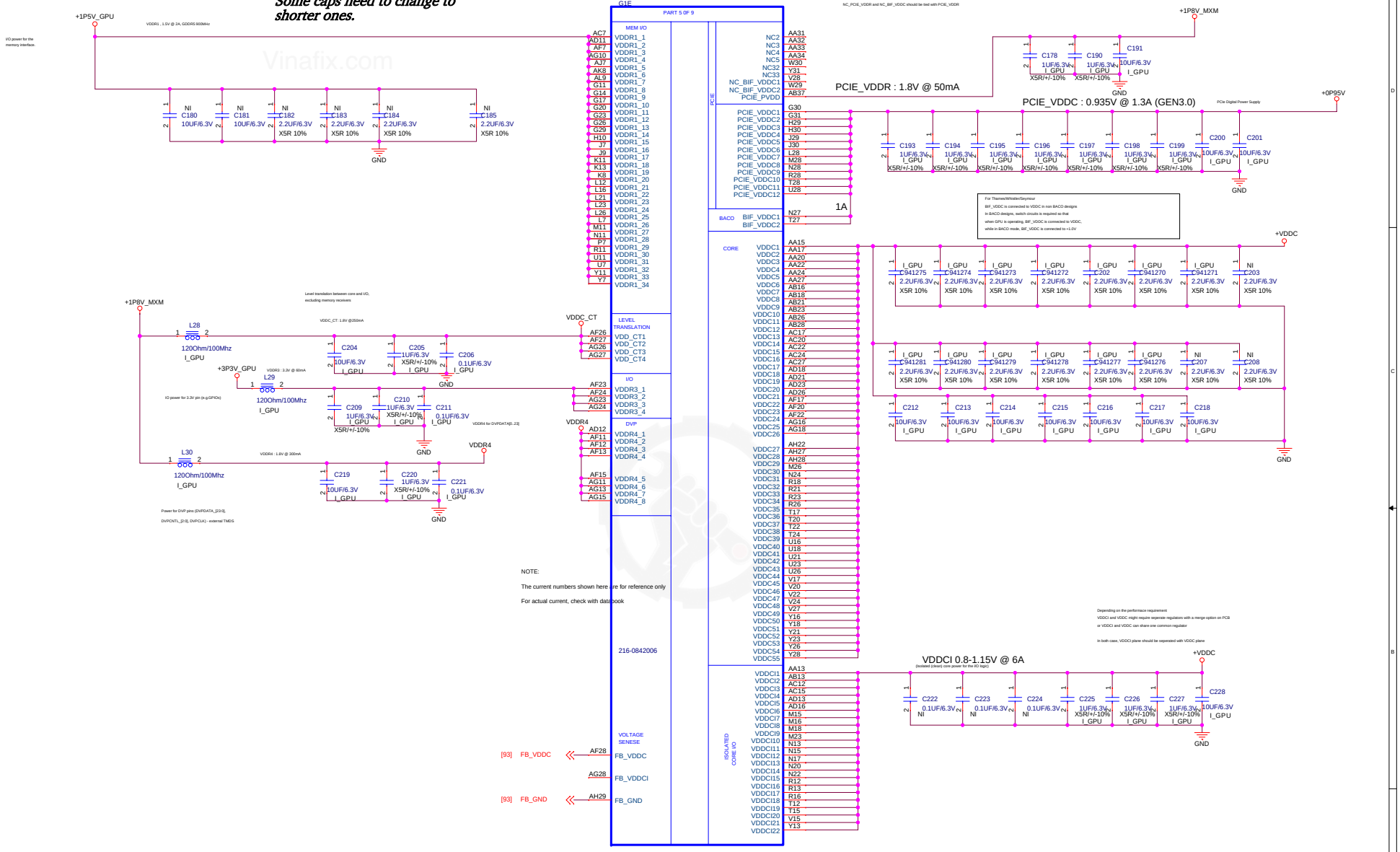
Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
B	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 82 of 97

COMPONENTS SHOWN ARE EXAMPLES ONLYAND NOT NECESSARILY QUALIFIED

Some caps need to change to shorter ones.



<Variant Name>

PEGATRON Corp.

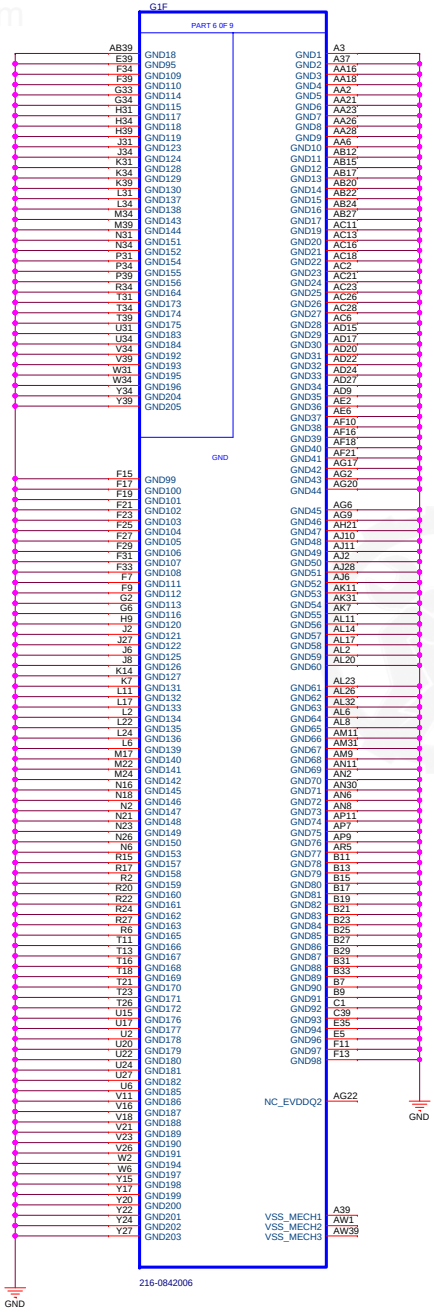
Title : Caspian_POWER

Engineer: Shrek_Tseng

Size	Project Name	Rev
C	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 83 of 97

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



<Variant Name>

PEGATRON Title : Caspian_GND

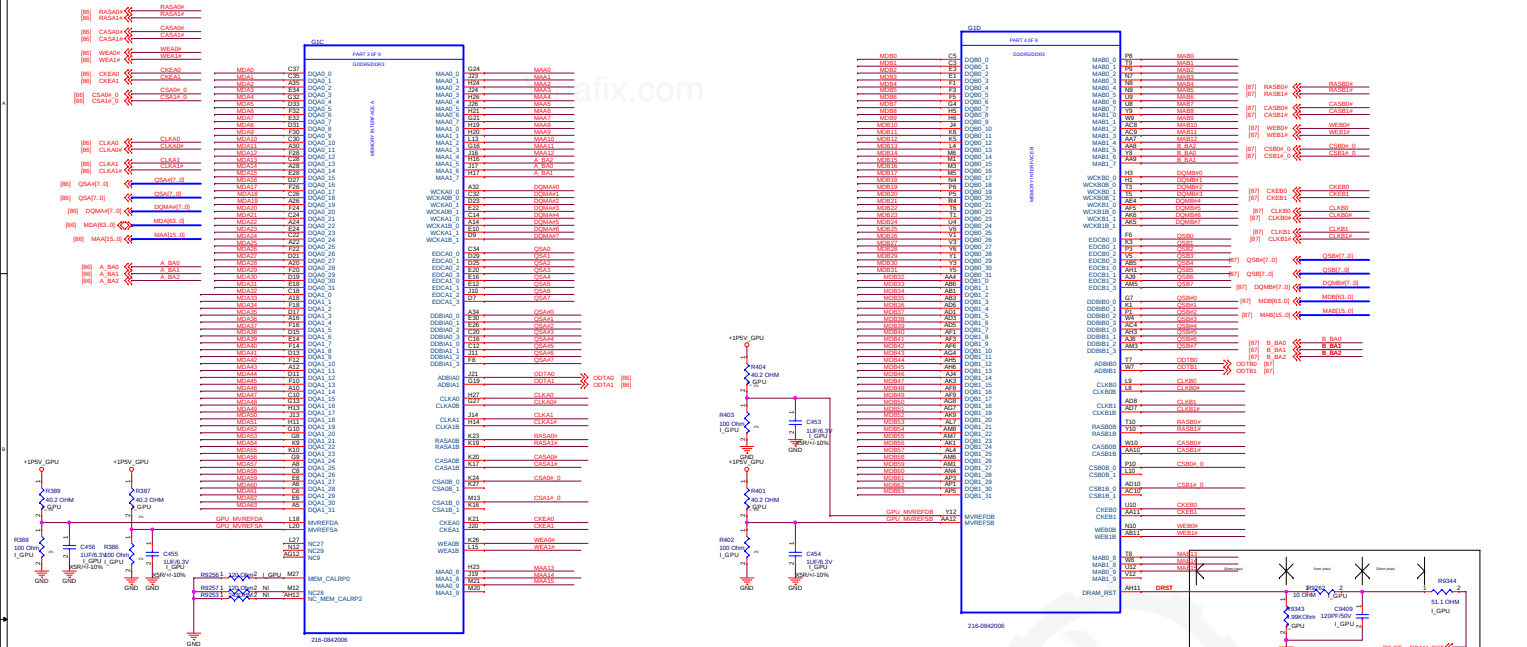
Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
C	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 84 of 97

COMPONENTS SHOWN ARE EXAMPLES ONLY

AND NOT NECESSARILY QUALIFIED



<Variant Name>

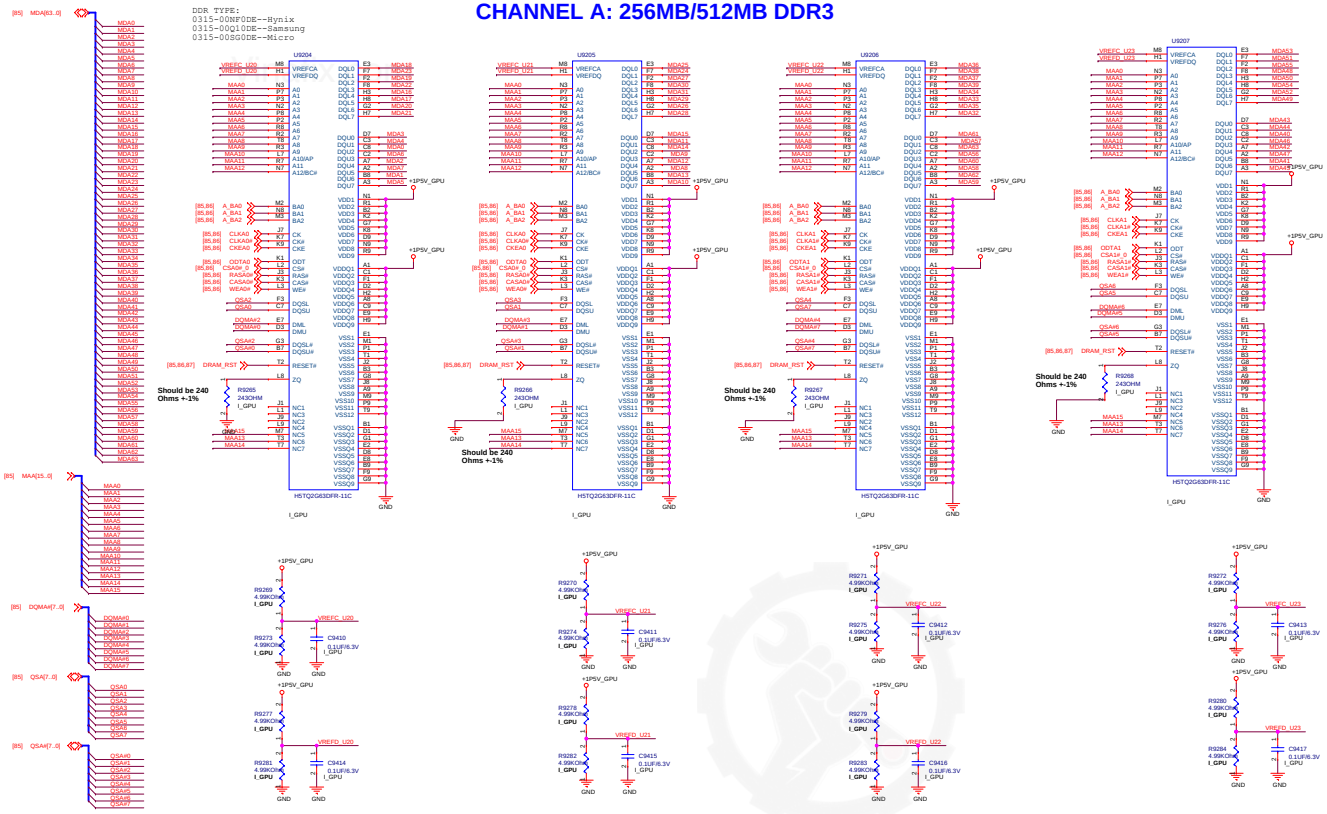
PEGATRON Title : Caspian_MEMORY

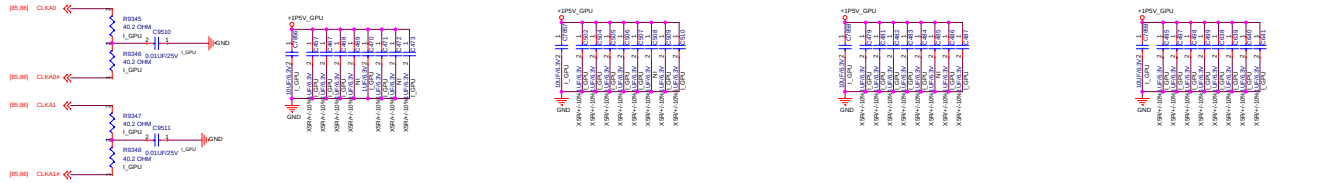
Pegatron Corp. Engineer: Shrek_Tseng

Size: D | Project Name: IPPLP-TH | Rev: A00

Date: Friday, January 17, 2014 | Sheet 85 of 97

CHANNEL A: 256MB/512MB DDR3





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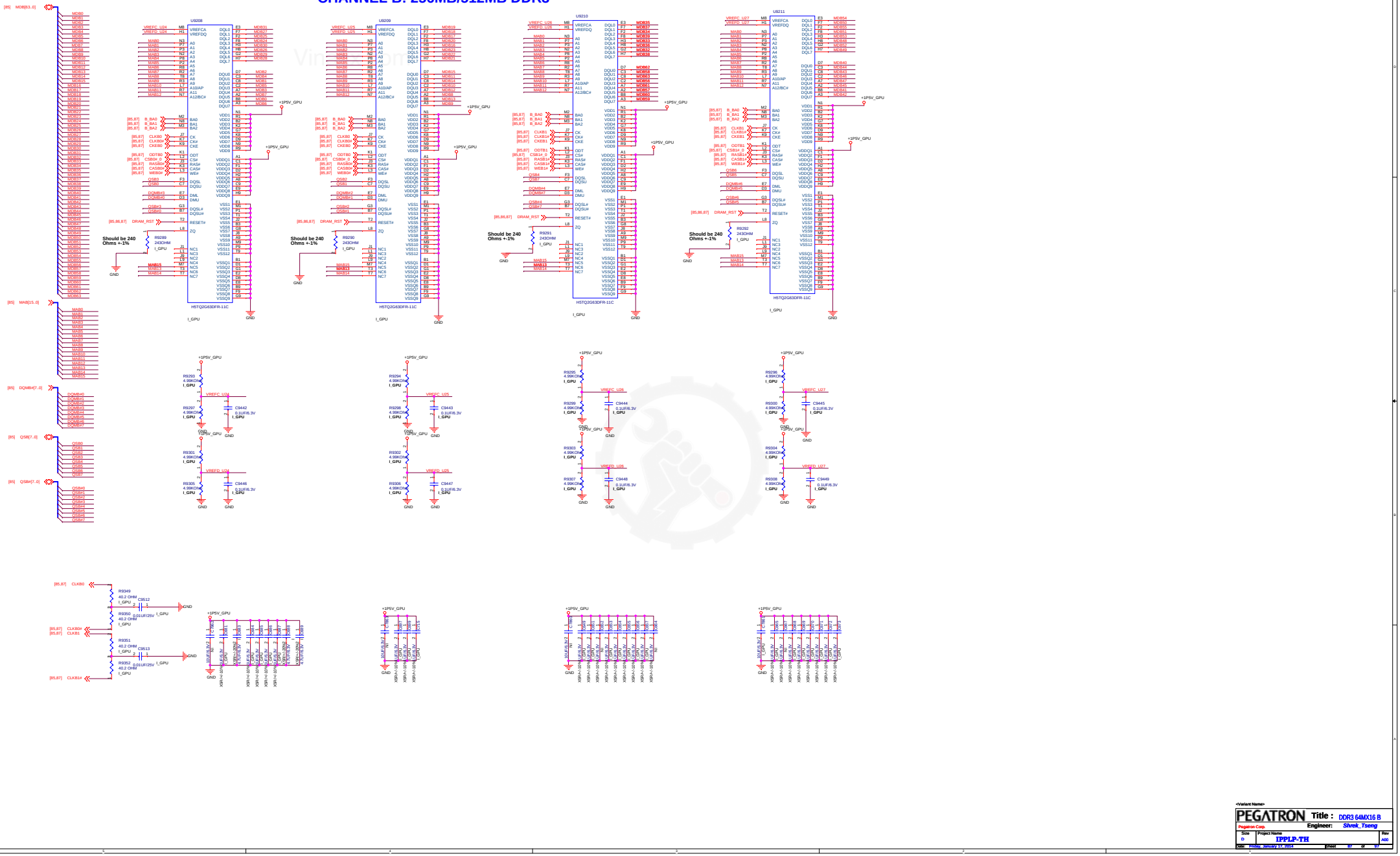
PEGATRON Title : DDR3 64MX16 A
Pegatron Corp. Engineer: Shrek_Tseng
Size: D | Project Name: IPPLP-AZ | Rev: A00
Date: Friday, January 17, 2014 | Sheet 86 of 97

CHANNEL B: 256MB/512MB DDR3



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PEGATRON

Title : DDR3 64MX16 B

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
D	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 87 of 97

<Variant Name>

PEGATRON Title : XXXXXX

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 88 of 97

<Variant Name>

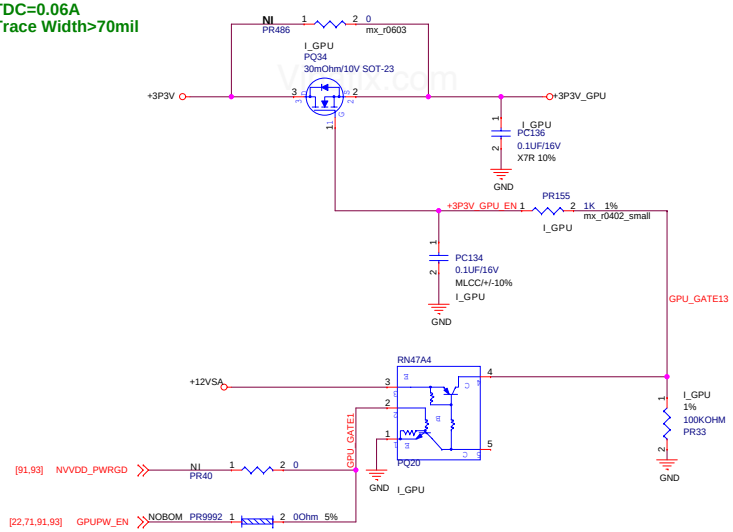
PEGATRON Title : XXXXXX

Pegatron Corp. Engineer: Shrek_Tseng

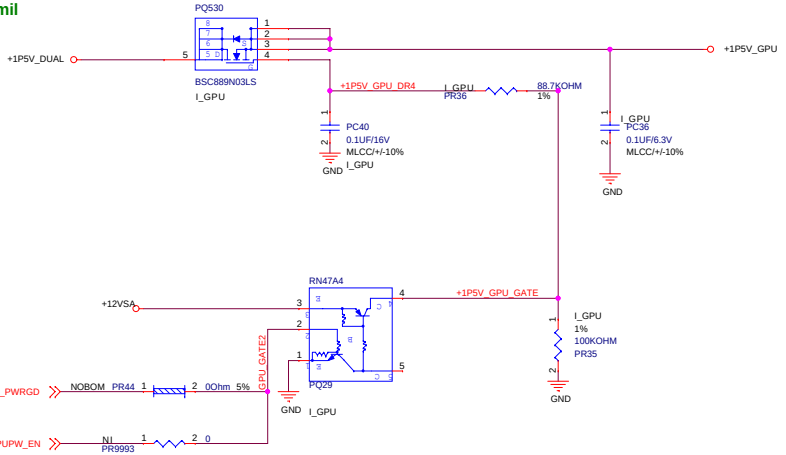
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 89 of 97

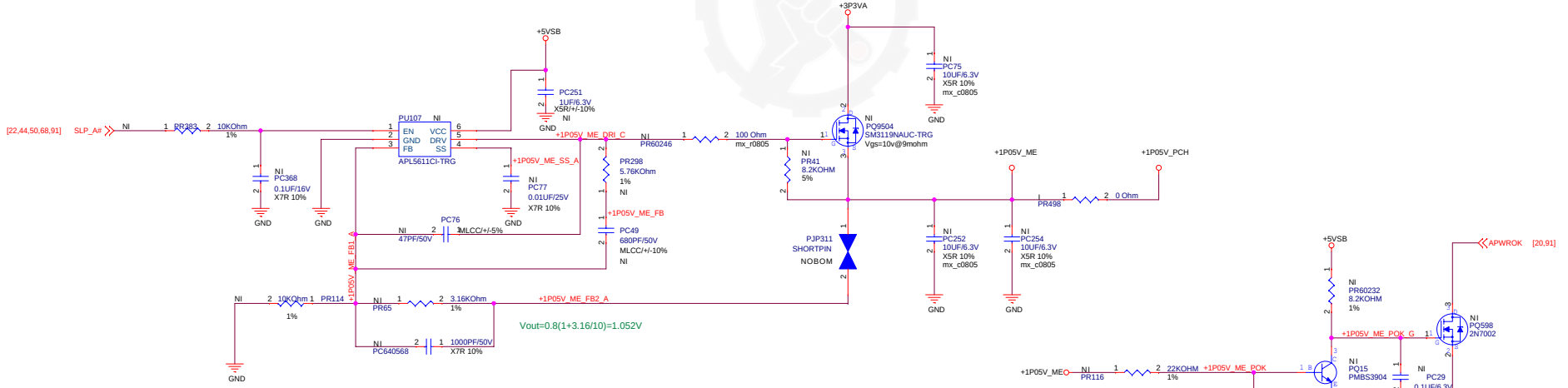
+3P3V_GPU
TDC=0.06A
Trace Width>70mil



+1P5V_GPU
IMAX=8A
Trace Width>240mil



+1P05V_ME/Imax:1A
Pd = 0.55*(3.3-1.05) = 1.2W



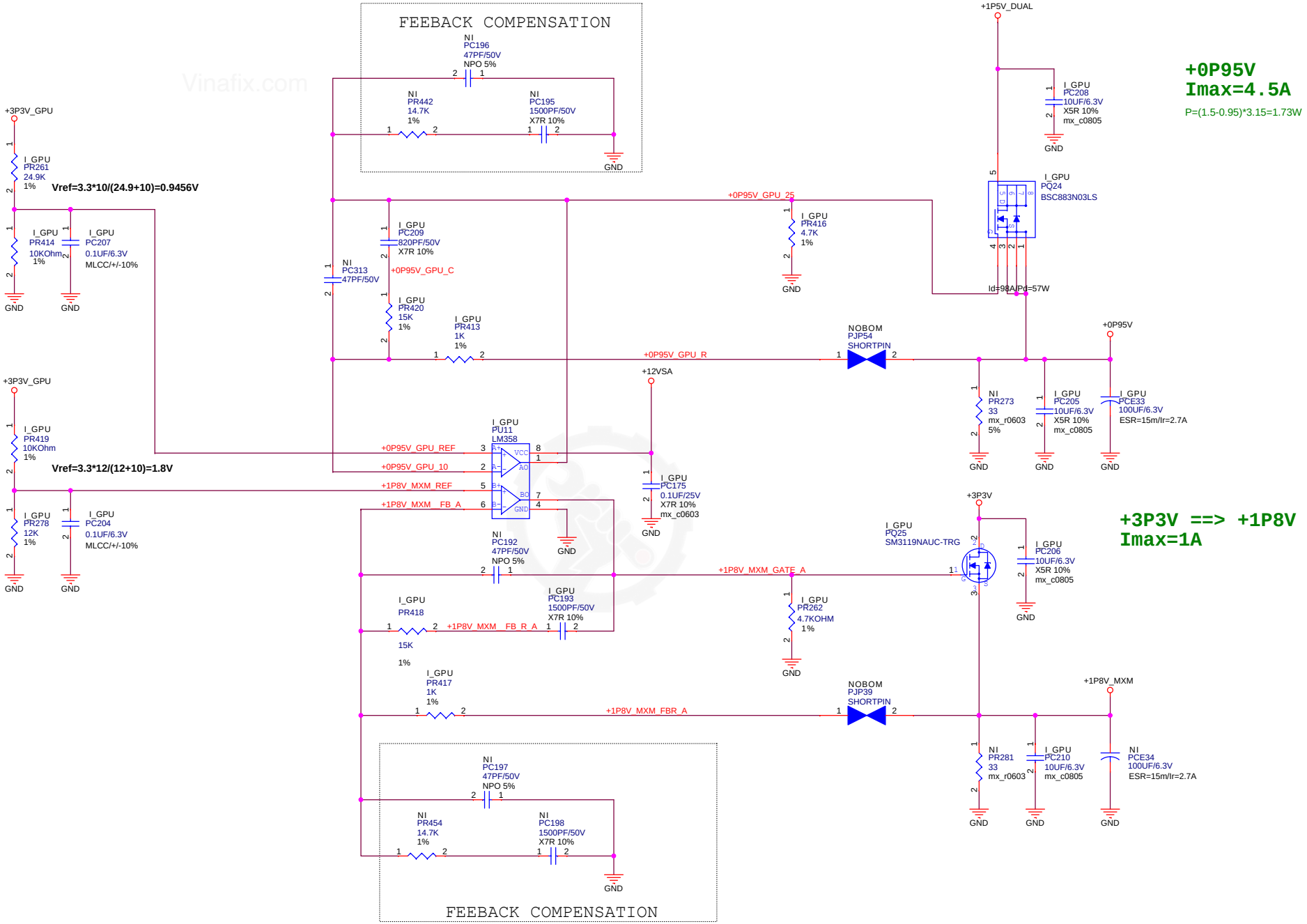
<Variant Name>

PEGATRON Title : 3P3V_GPU & +1P05V_ME

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
C	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 91 of 97



PEGATRON Title : +0P95V & +1P8V_MXM

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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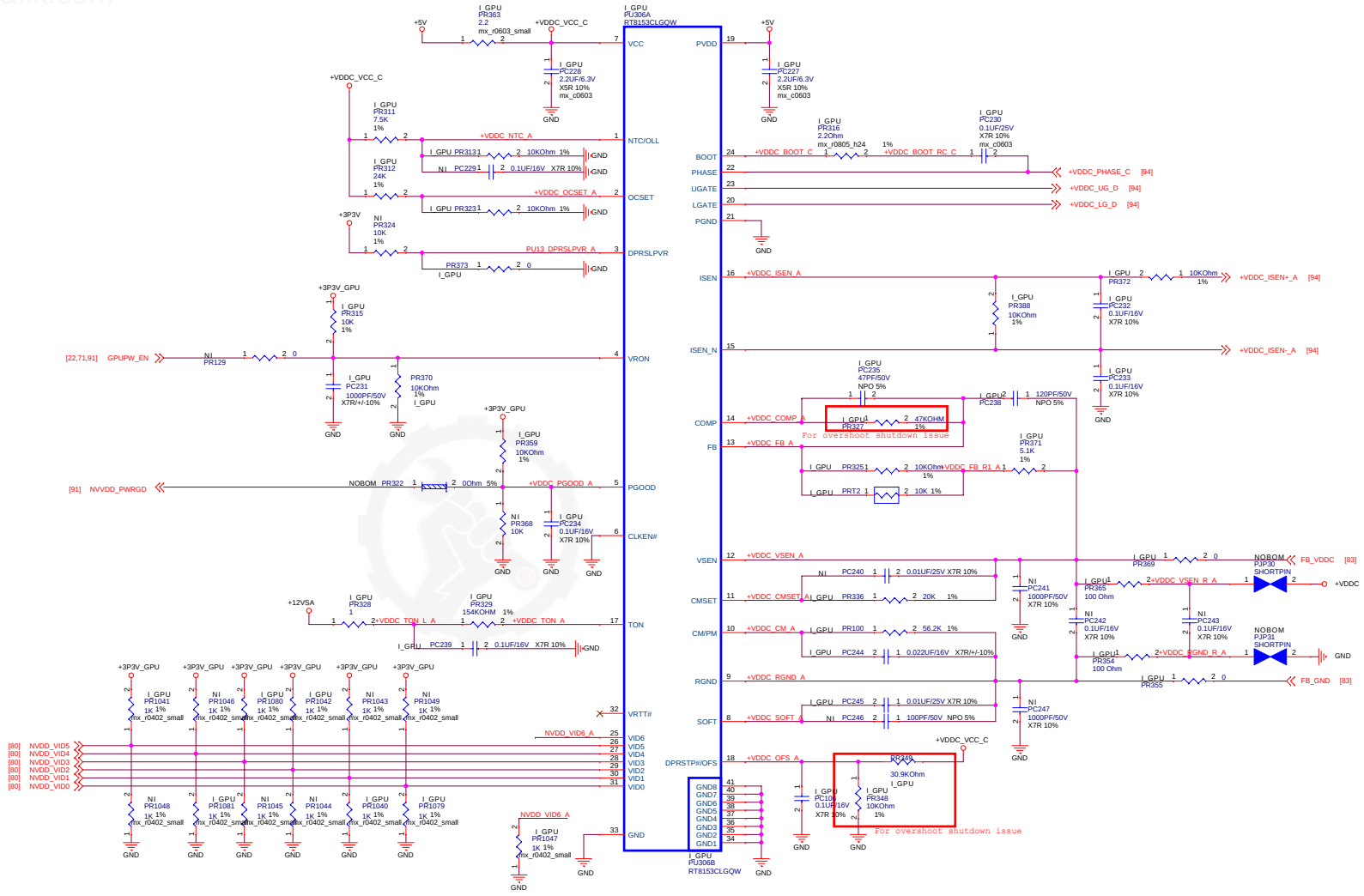
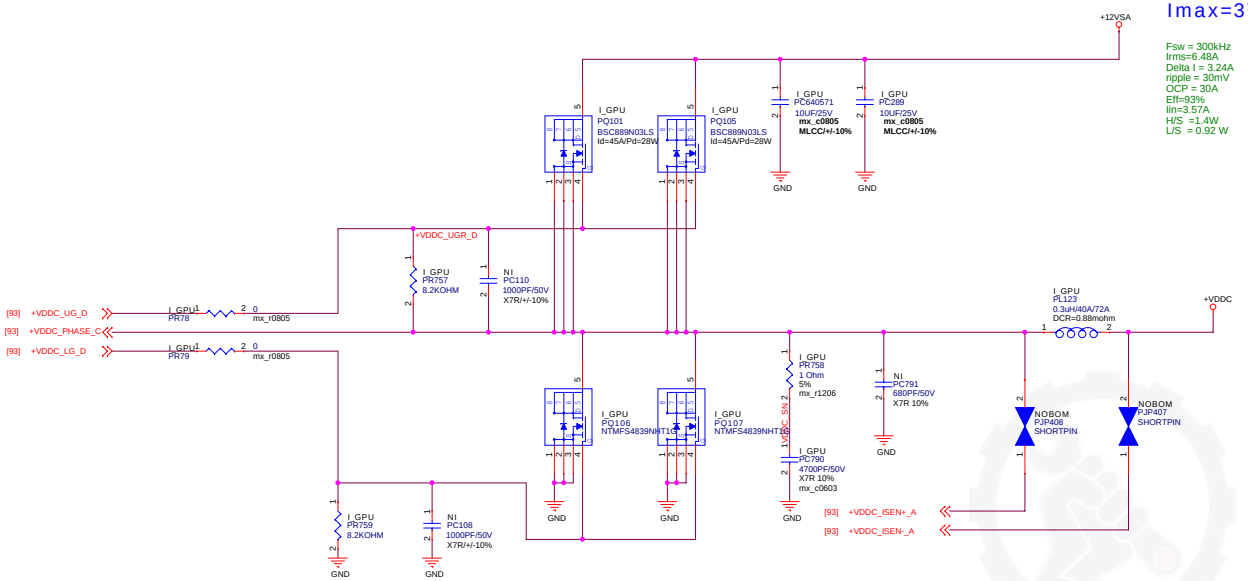


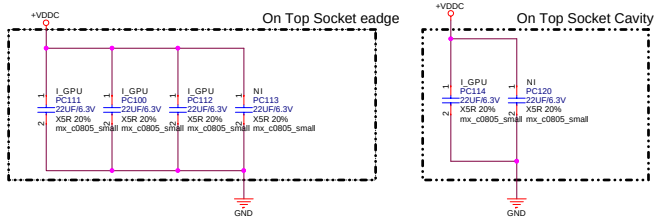
PEGATRON DT-MB RESTRICTED SECRET

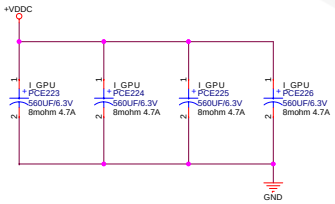
PEGATRON	Title : +VDDC CONTROLLER	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A2	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 93 of 97	

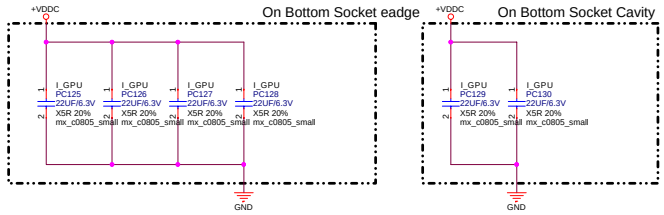
+VDDC
TDC=25A
Imax=37.5A

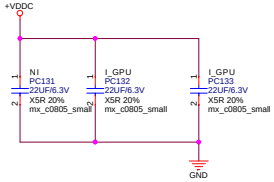
Fsw = 300kHz
Irms=6.48A
Delta I = 3.24A
ripple = 30mV
OCP = 30A
Eff=93%
Iin=3.57A
H/S =1.4W
L/S = 0.92 W







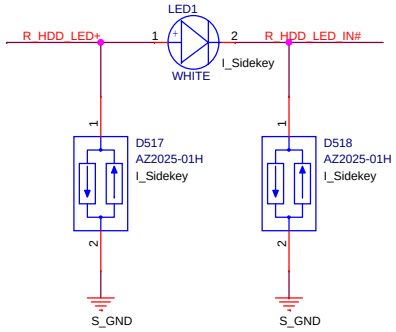




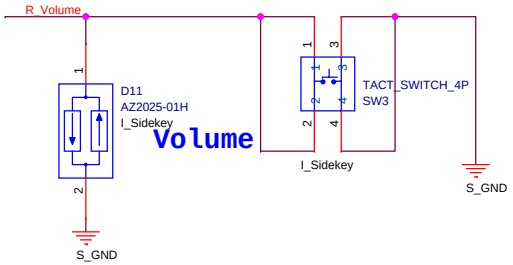
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +VDDC CAP	
Pegatron Corp.	Engineer: Shrek_Tseng	
Size: A2	Project Name: IPPLP-TH	Rev: A00
Date: Friday, January 17, 2014	Sheet 94 of 97	

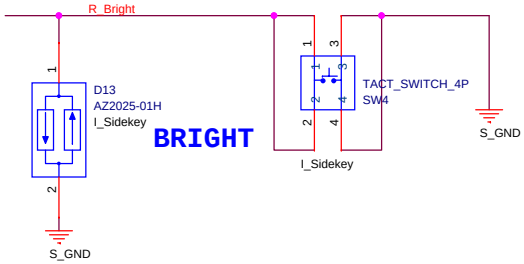
HDD LED



07XA030W0002



HF P/N: 12X902050B30
1209-008C000
1209-007V000



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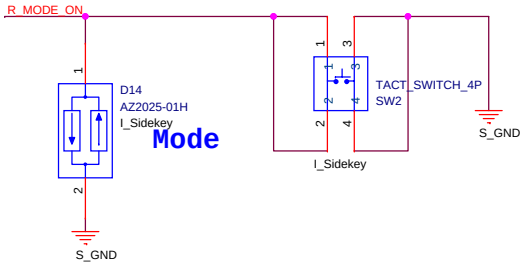
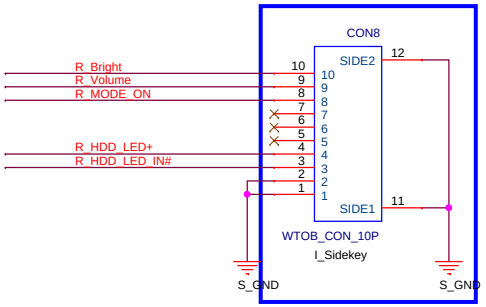


HF P/N: 12X902050B30
1209-008C000
1209-007V000

6/22修改成 R/A connector (機構要求)



PPID1

40X4_WHITE
I

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIDE KEY

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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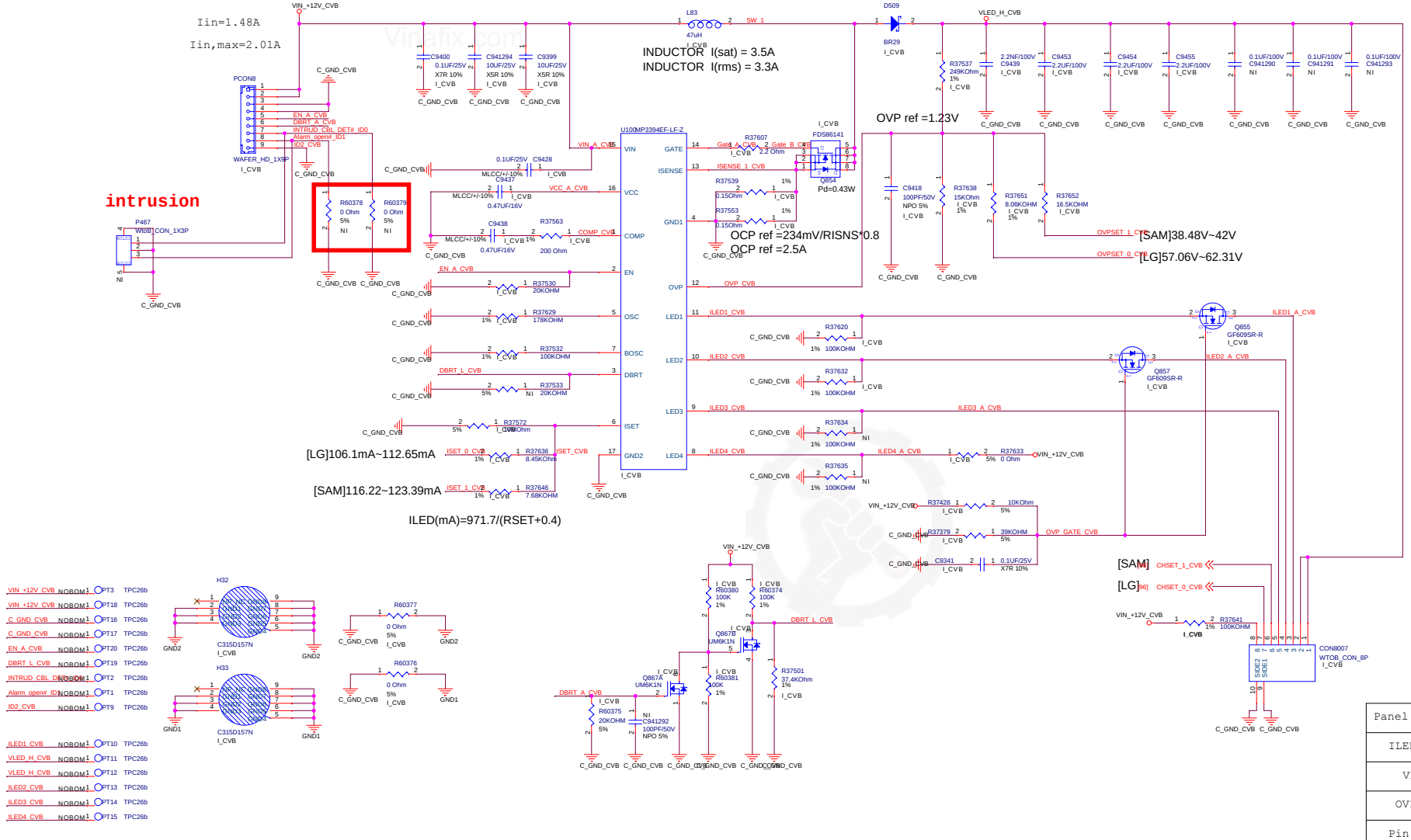

Panel(23")	LG	SAM
ILED.typ	110/120 mA	120/130 mA
VF	52.7/56.1V	34/37V
OVP	59.64V	40.21V
Pin NO.	4	4
ID	1 1	1 0
ID Level(V)	1.6	0

PEGATRON Title : CONVERTER BOARD

PEGATRON COMPUTER INC Engineer: Bell_Yang

Size	Project Name	Rev
A2	IPPLP-TH	A00

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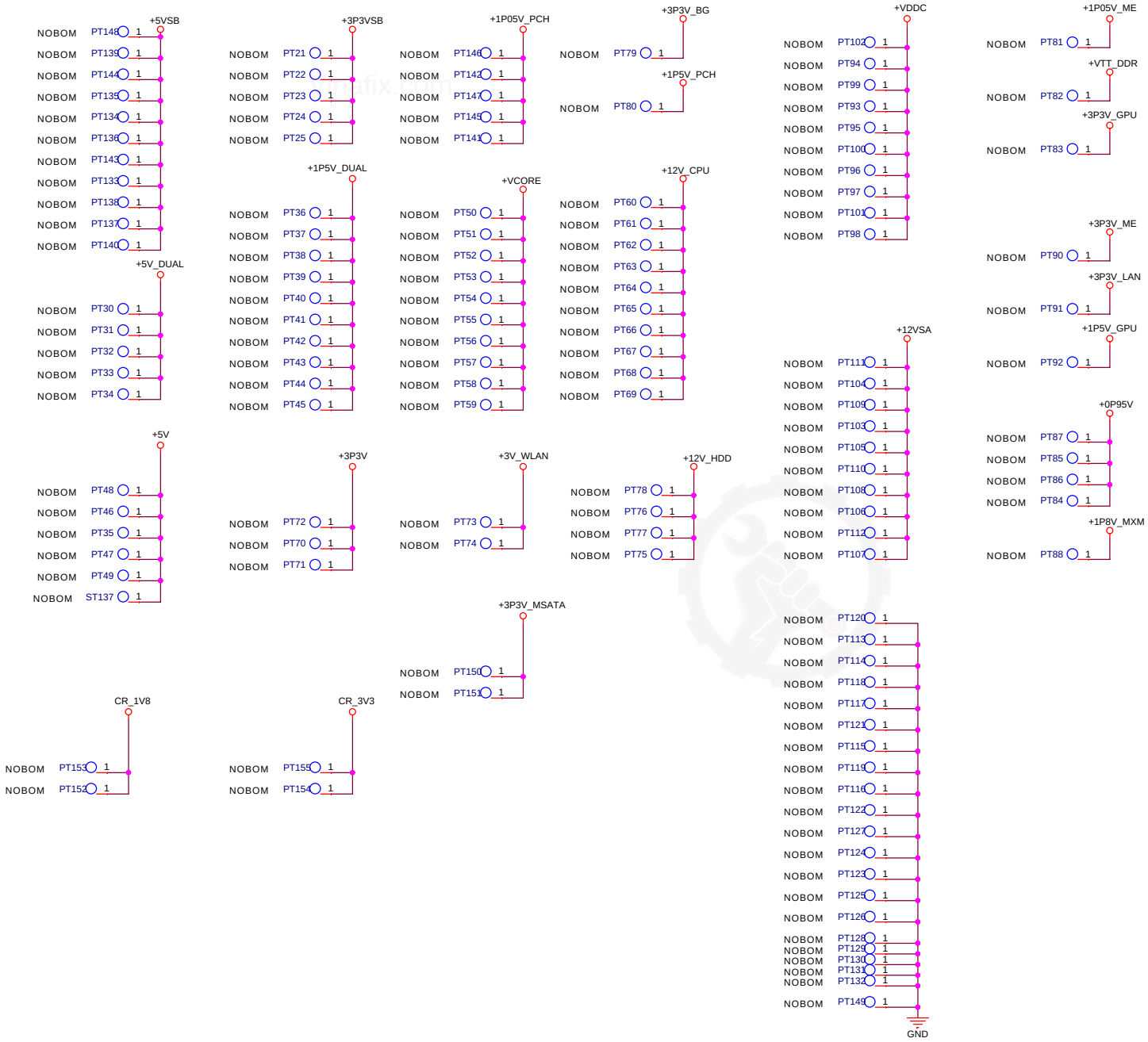

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TP

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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