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G 320 AST M/B Schematics Document

NM_B321 REV:0.2

AMD FT4 Stoney SOC with DDRIIII

AMD R17M-M1-70

2017-02-04

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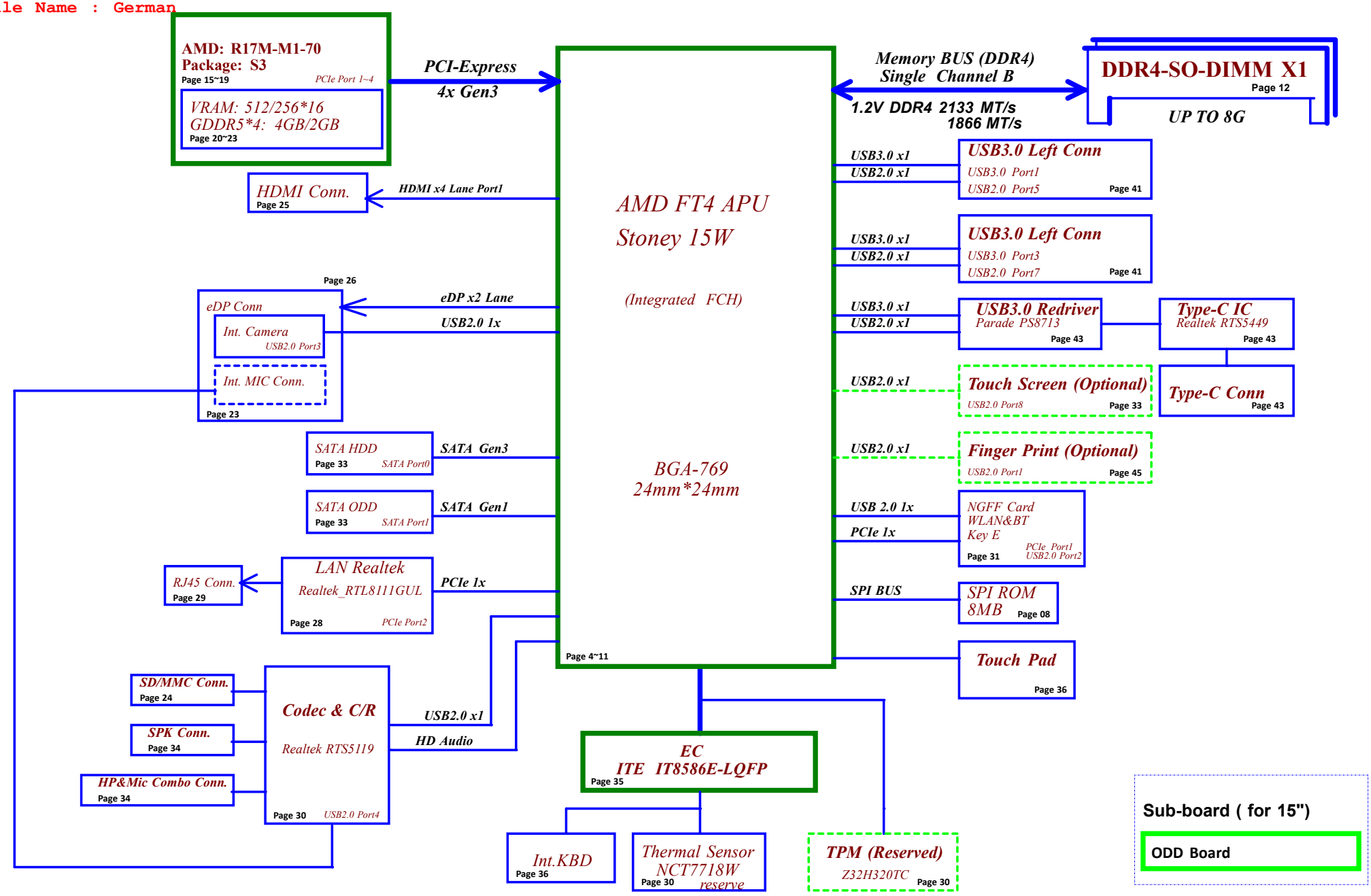
File Name : German



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+2.5V +1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID1	BOARD_ID2 reserve
	0: Dis	0: No KBL
	1: UMA	1: KBL

BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

USB Port Table for Stoney FT4

USB 2.0	USB 3.0	Port	Port device
EHCI		0	Finger print
		1	Blue Tooth
		2	Camera
		3	Card Reader
xHCI		4	LEFT USB (3.0)
		5	Type-C
	2	6	RighT USB (3.0) upper
		7	Touch screen

PCIE PORT LIST

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	DIS GPU
	1	
	2	
	3	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_CZ@	EMC Carrizo APU part
EMC_15@	EMC 15 part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
CZ@	Carrizo Part
CZL@	CarrizoL part
CZPX@	Carrizo Discrete Part
CZLPX@	CarrizoL Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
CZLUMA@	CarrizoL UMA Part
CZUMA@	Carrizo UMA Part
SIVCD@	SIV COST down material
HDMI@	HDMI Logo
STN@	Stoney part
KBL@	Key board backlight part

VRAM

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	X	V		X	X	X	X	V	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X		X	X	V	V APU_SIC APU_SID 1.8VS for ASF	X	X	X
APU_SMB_CLK APU_SMB_DATA	APU +3VS	X	X	X	V	V	X		X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VL_EC	X	X		X	X	X	X	X	V	X
TP_I2C0_SCL_R TP_I2C0_SDA_R	APU +1.8VS	X	X	X	X	X	X		X	X	V

EC SM Bus1 address

Device	Address
Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
PMIC	0X34

EC SM Bus3 address

Device	Address
Thermal Sensor	1001_100xb(reserve)
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

APU SM Bus1 address

Device	Address
Touch pad	0x15

APU SM Bus2

No use

APU SM Bus3 address

Device	Address
DDR DIMM	0xA0h
WLAN	RSVD

APU SM Bus4

No use

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Title: **Notes List**

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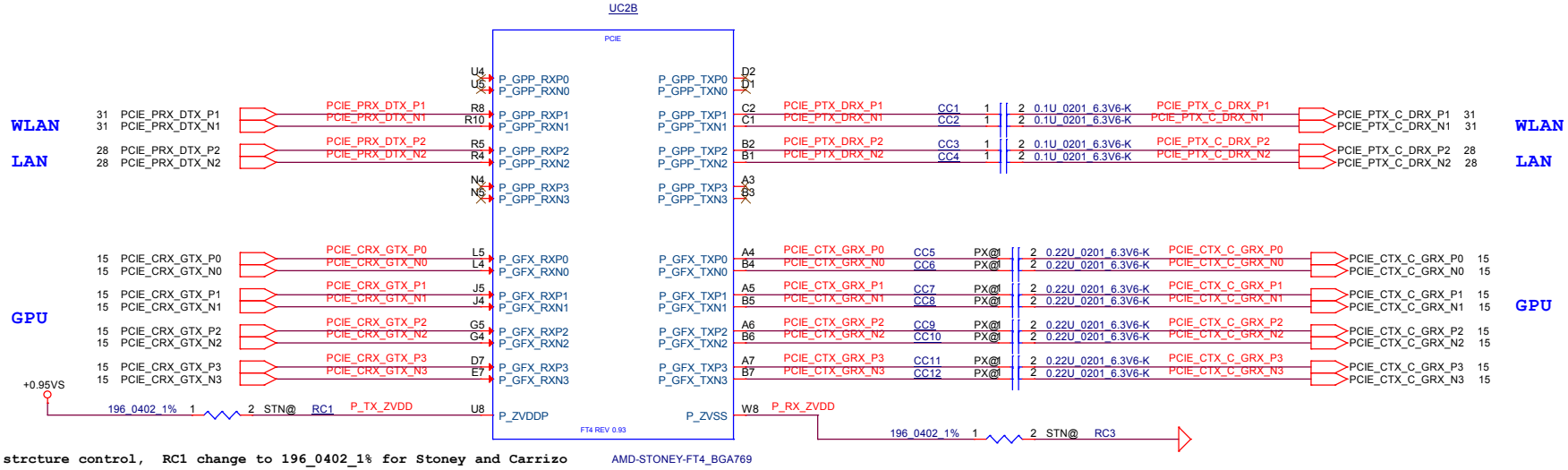

with BOM strcture control, RC1 change to 196_0402_1% for Stoney and Carrizo

@

CarrizoL not support GFX4-GFX7

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Title: FT4 (PCIE I/F)

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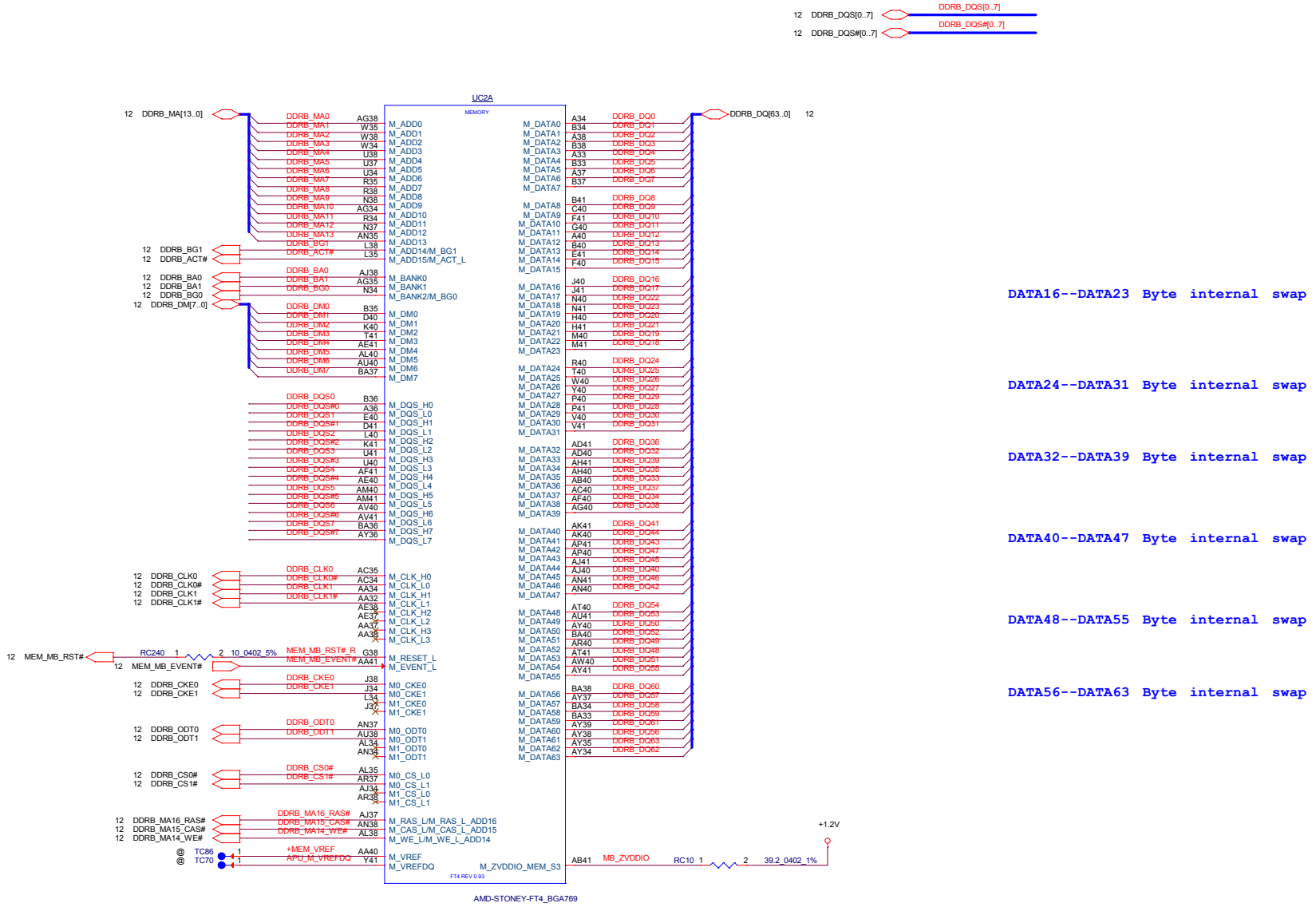

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Title: **FT4 (MEM)**

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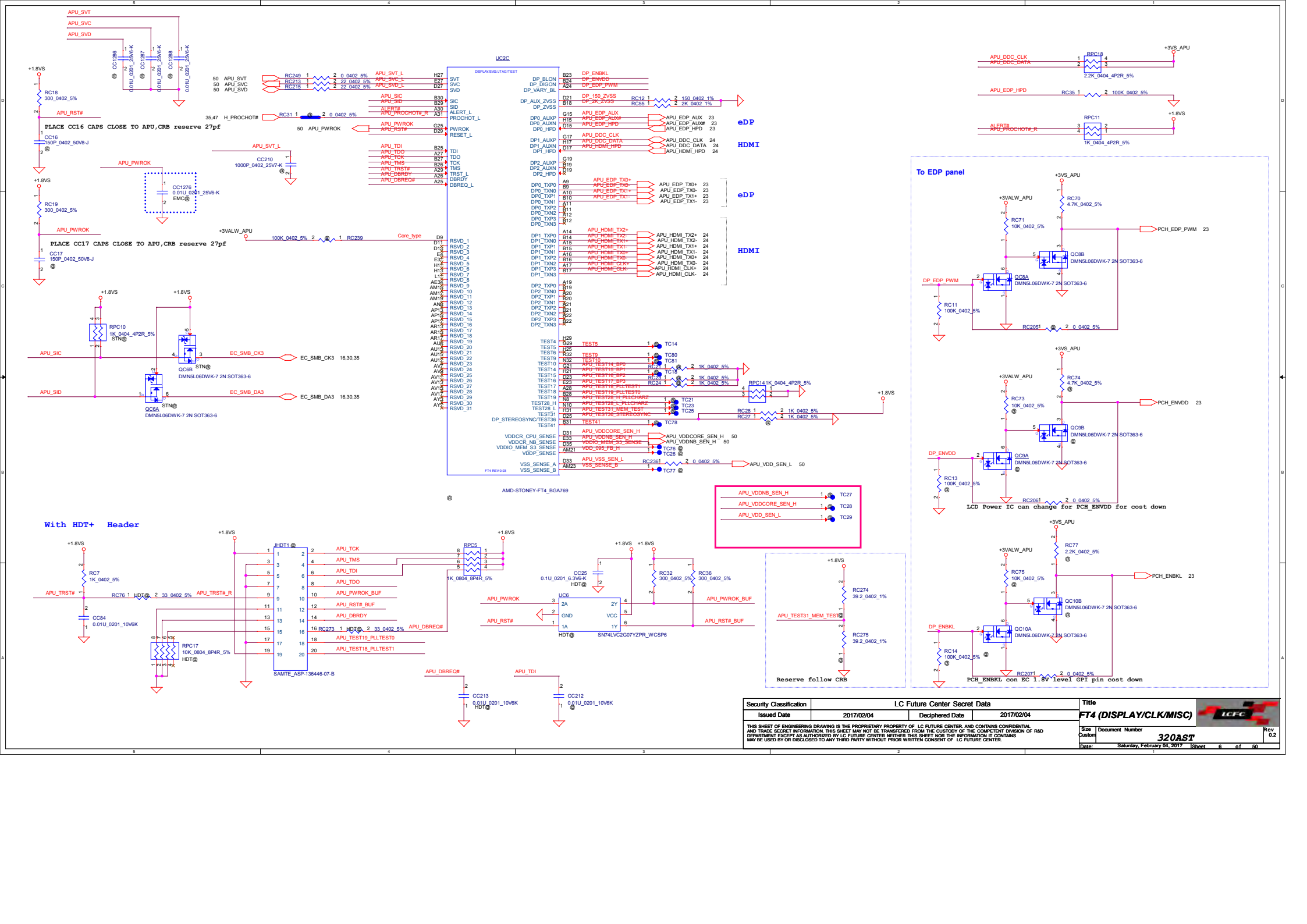

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Title: FT4 (DISPLAY/CLK/MISC)

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BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

Connected to 10-ms RC-delay circuit on VDD_18_S5 power rail.
(CRB PWR Dealy: 22K/0.1uF)

with QC16,QC17, EC must set EC_RSMRST# and EC_SYS_PWRGD reversed compare to DC1 and DC2

Connect TouchPad to I2C port0 following CRB 10/28

Max ESR < 65K ohm !!

delete APU_SHUTDOWN# signal for Stoney FT4

APU_S5_MUX_CTRL 100K pull high follow CRB
BLINK isn't strap pin, don't need pull high

CRB: CARRIZO NEED 10K PD ON UNUSED SDIN
DG: 10K PD

PXS_PWREN_R/PXS_RST#_R/VR_VGA_PWRGD internal pull up 40k

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Title: FT4 (GEVENT/GPIO/SD/AZ)

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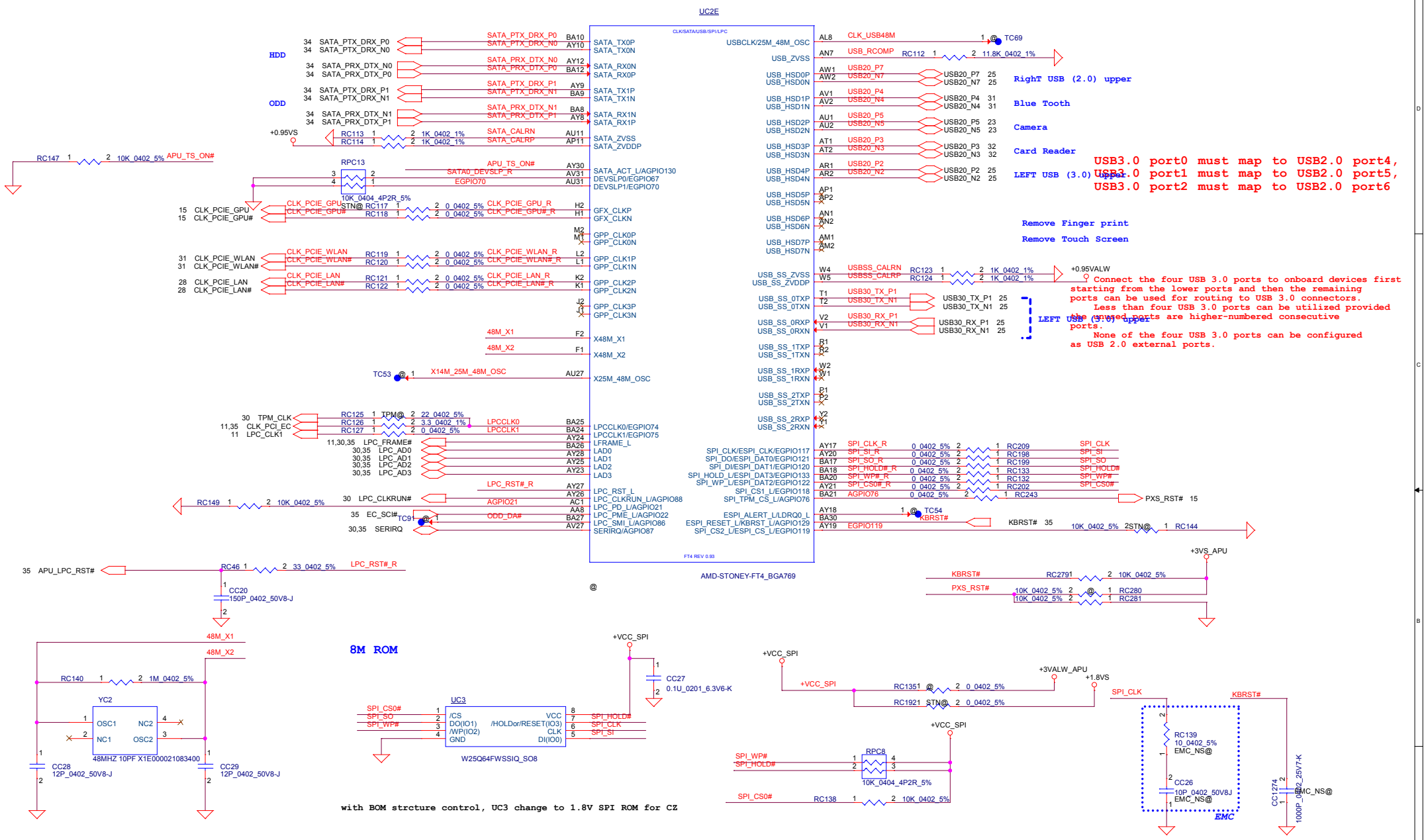

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Title: FT4 (SATA/USB/LPC/SPI)

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Custom	320AST	0.2

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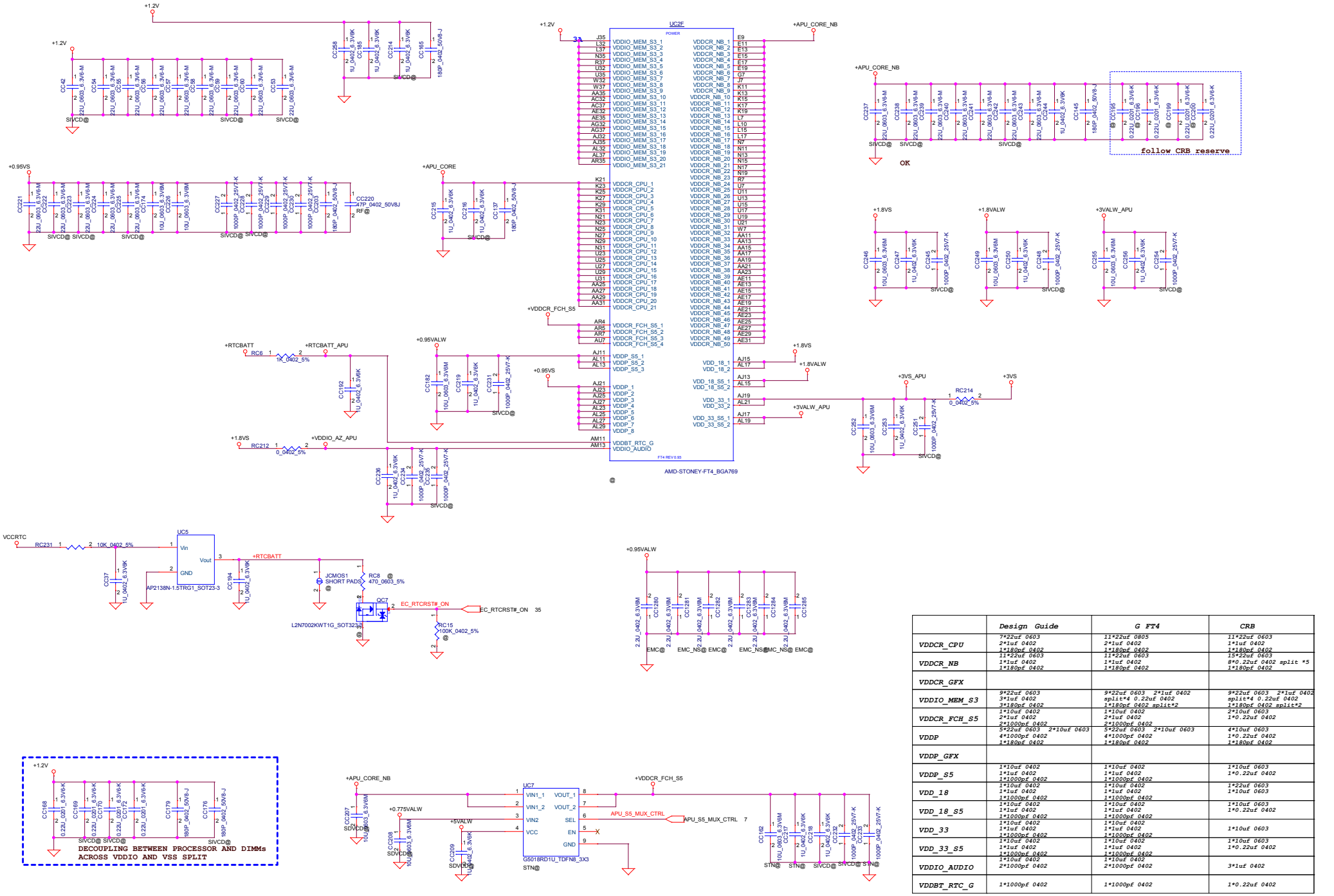

	Design Guide	G FT4	CRB
VDDCR_CPU	7*22uf 0603 2*1uf 0402 1*180pf 0402	11*22uf 0805 2*1uf 0402 1*180pf 0402	11*22uf 0603 1*1uf 0402 1*180pf 0402
VDDCR_NB	11*22uf 0603 1*1uf 0402 1*180pf 0402	11*22uf 0603 1*1uf 0402 1*180pf 0402	15*22uf 0603 8*0.22uf 0402 split *5 1*180pf 0402
VDDCR_GFX			
VDDIO_MEM_S3	9*22uf 0603 3*1uf 0402 3*180pf 0402	9*22uf 0603 2*1uf 0402 split*4 0.22uf 0402 1*180pf 0402 split*2	9*22uf 0603 2*1uf 0402 split*4 0.22uf 0402 1*180pf 0402 split*2
VDDCR_FCH_S5	1*10uf 0402 2*1uf 0402 2*1000pf 0402	1*10uf 0402 2*1uf 0402 2*1000pf 0402	2*10uf 0603 1*0.22uf 0402
VDDP	5*22uf 0603 2*10uf 0603 4*1000pf 0402 1*180pf 0402	5*22uf 0603 2*10uf 0603 4*1000pf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402
VDDP_GFX			
VDDP_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDD_18	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*22uf 0603 1*10uf 0603
VDD_18_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDD_33	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603
VDD_33_S5	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0402 1*1uf 0402 1*1000pf 0402	1*10uf 0603 1*0.22uf 0402
VDDIO_AUDIO	1*10uf 0402 2*1000pf 0402	1*10uf 0402 2*1000pf 0402	3*1uf 0402
VDDBT_RTC_G	1*1000pf 0402	1*1000pf 0402	1*0.22uf 0402

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Title: FT4 (POWER&DECOUPLING)

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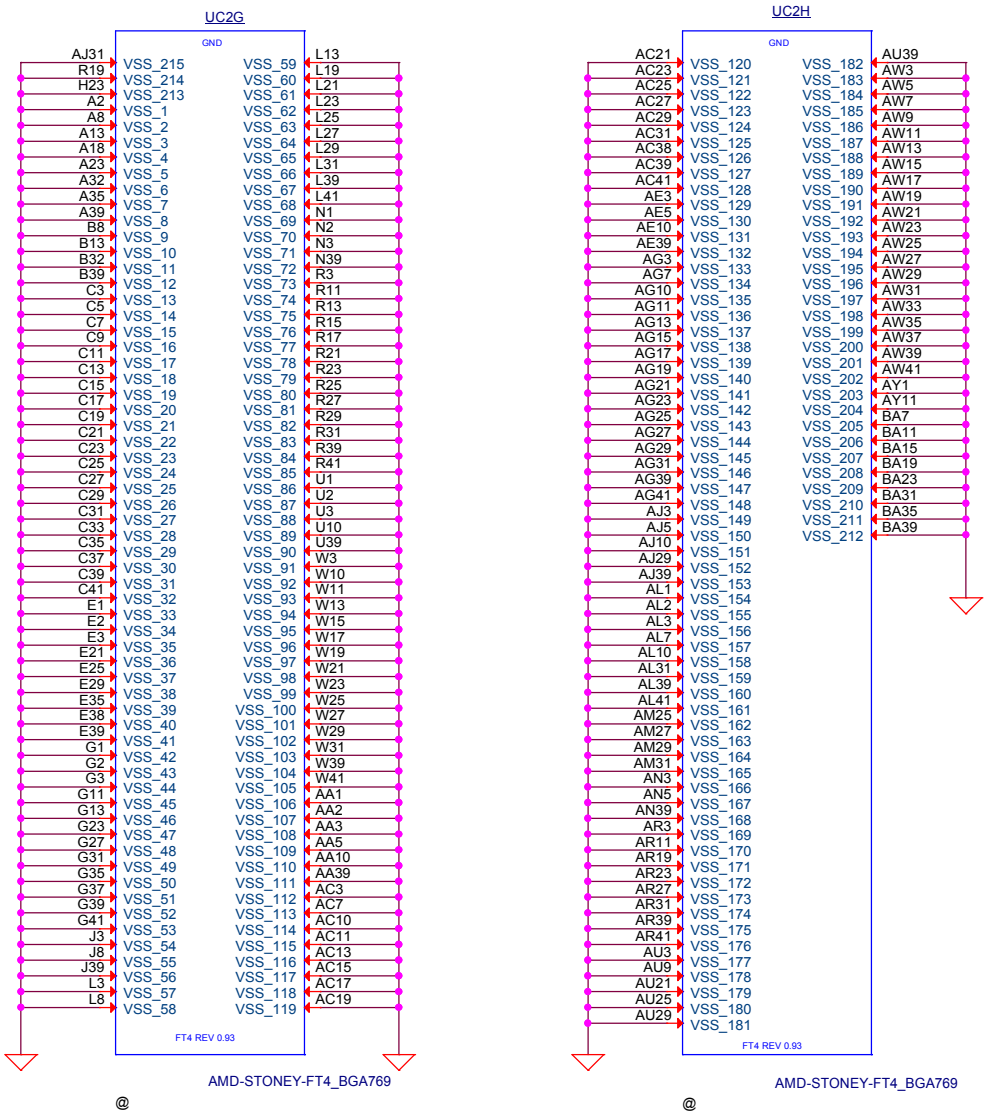

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Title: **FT4 (VSS)**

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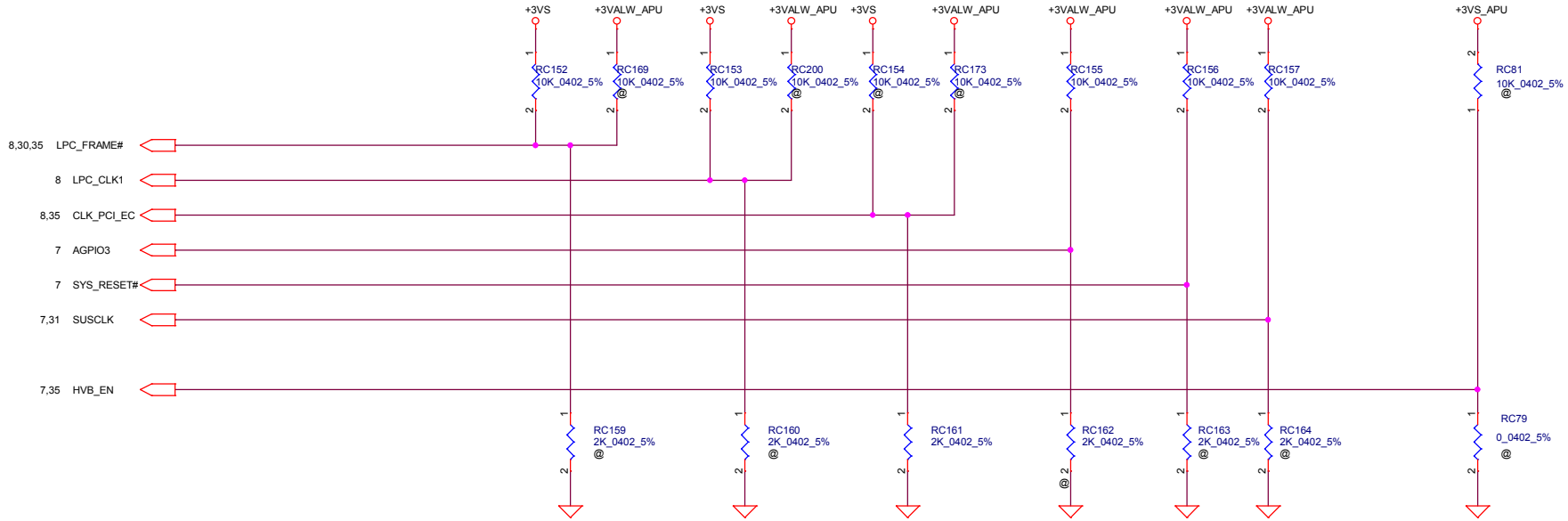

STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FT4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FT4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.
Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to ' 1' for ¢
AGPIO3

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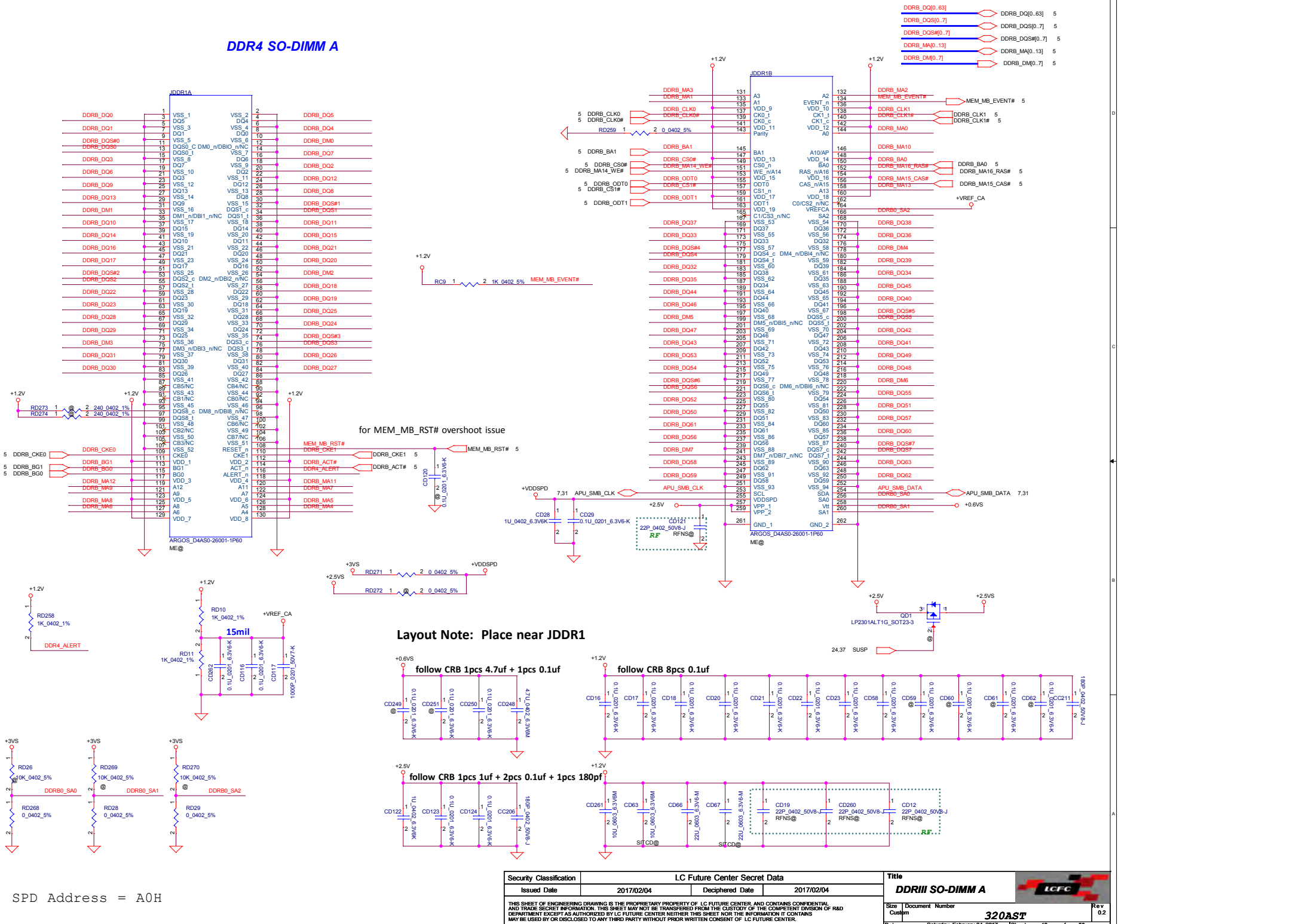
DDR4 SO-DIMM A



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Title: DDRIII SO-DIMM A

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Title

DDRIII SO-DIMM B

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

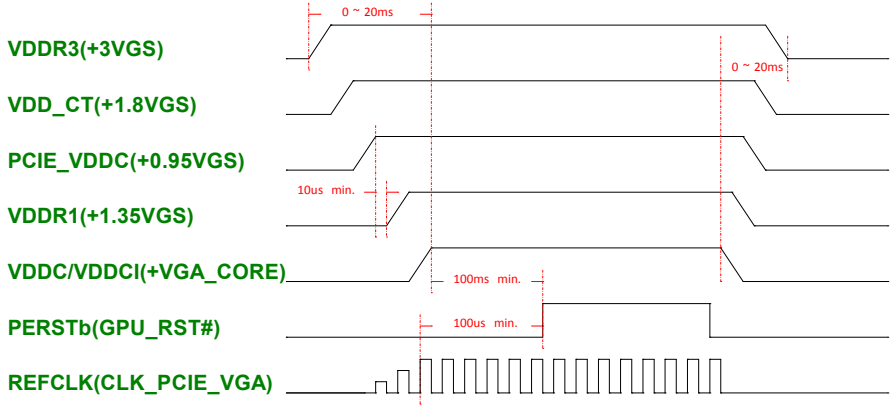
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

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Title: VGA Notes List

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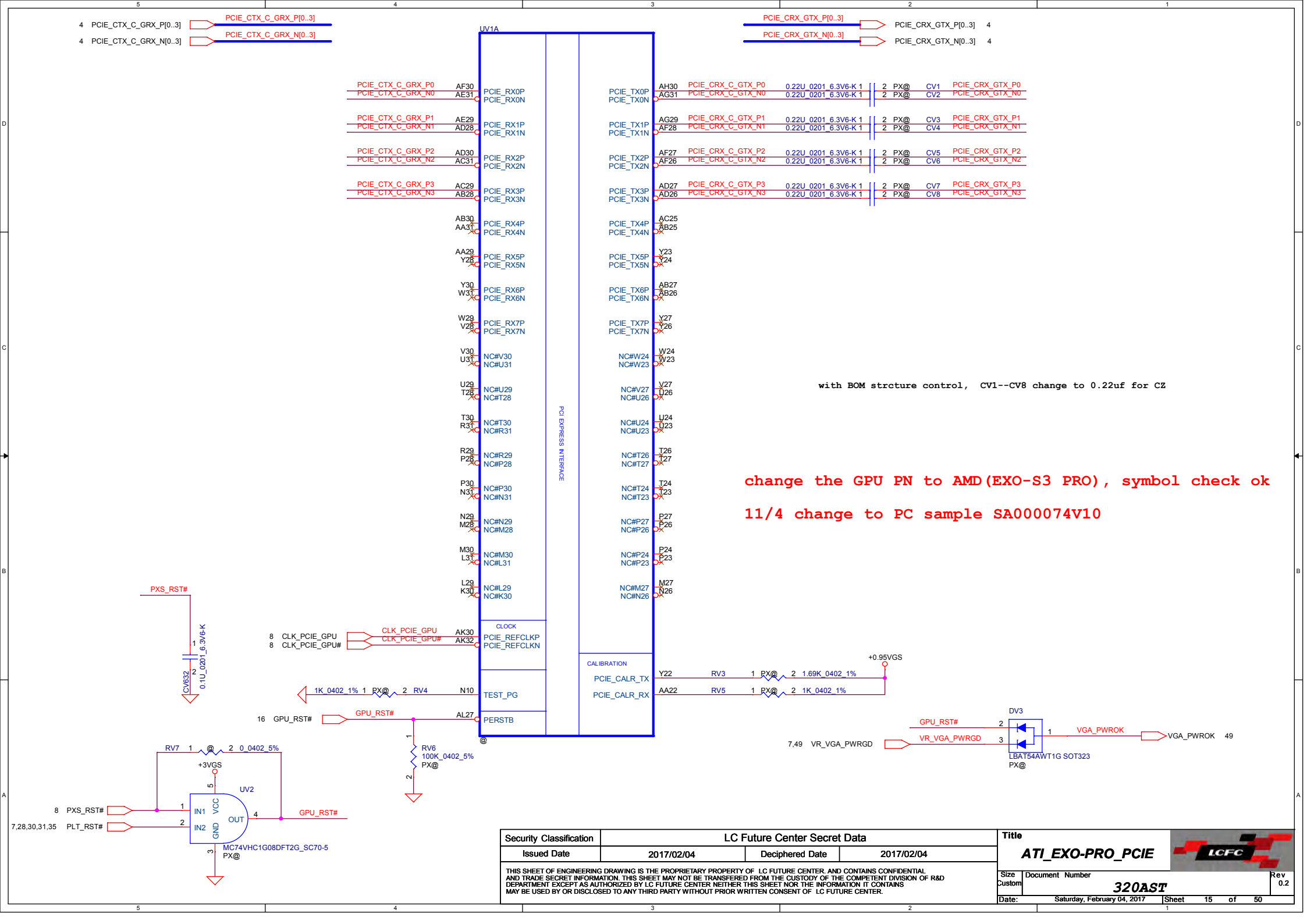

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Title: ATI_EXO-PRO_PCIE

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= GEN3 is supported	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 1G 000 = Hynix 2G 111 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

MLPS	Bit				BOM		
	5	4	3	2	1	R_pu ( )	R_pd ( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=8.45K	RV80=2K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=NC

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Connect GPIO_28 to 10K pull down to enable MLPS.

(1.8V@20mA TSVDD)

2016/09/02: Pull-down GPU_CLKREQ# at GPU side

Reserve for Topaz

Pull down for none OBFF design

For Topaz, RV23/RV24 stuff 100ohm
For EXO, RV23/RV24 stuff 0hm

no symbol for 8pf cap, PLM has PN,change the PN

Internal VGA Thermal Sensor

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Title: ATI_EXO-PRO_Main_MSIC

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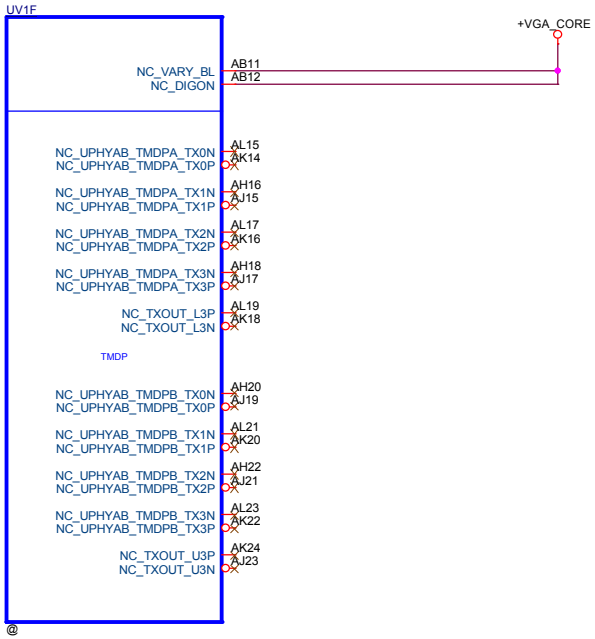

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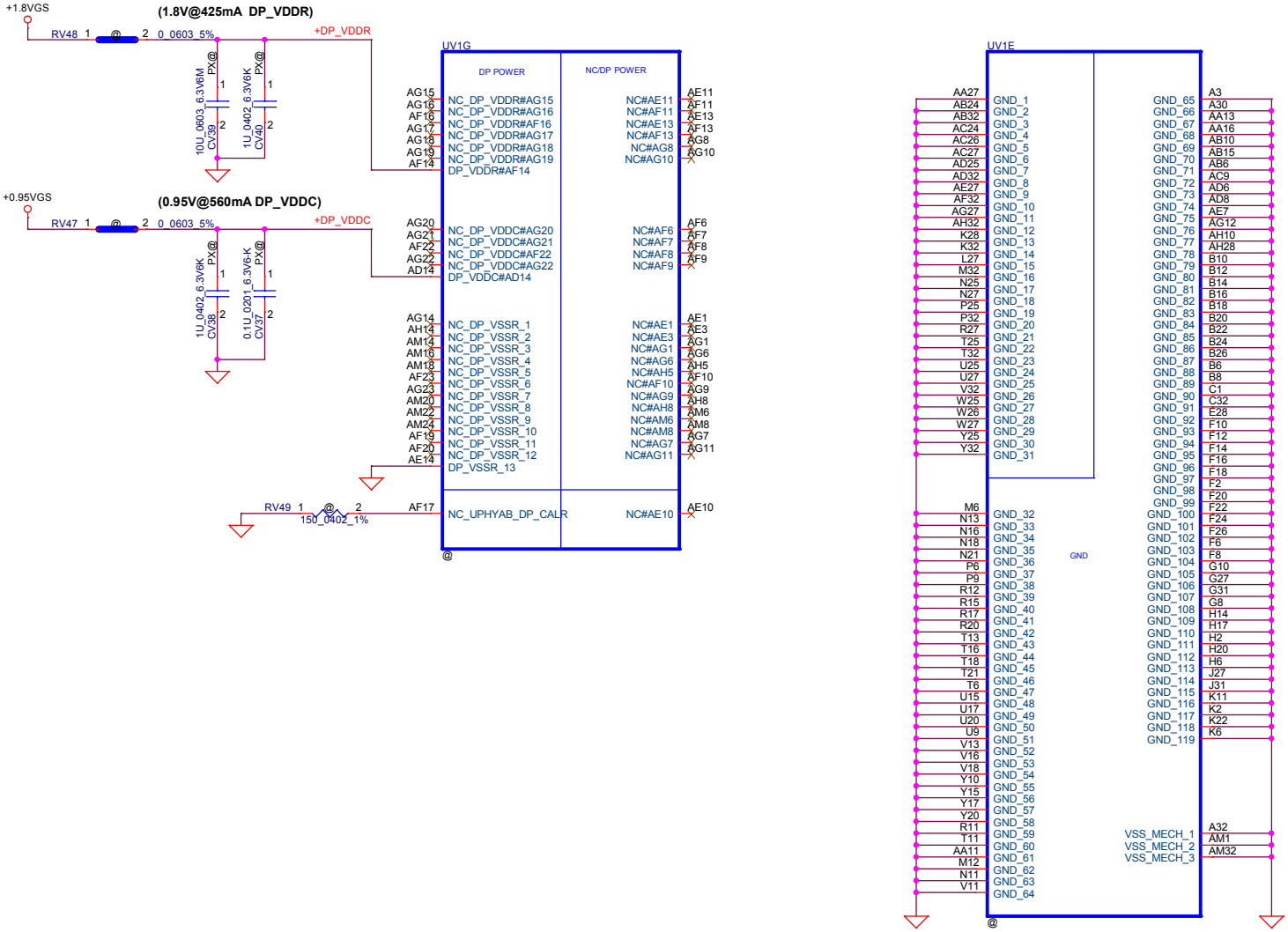
Title: ATI_EXO-PRO_TMDP

Size: Custom	Document Number: 320AST	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 17 of 50	



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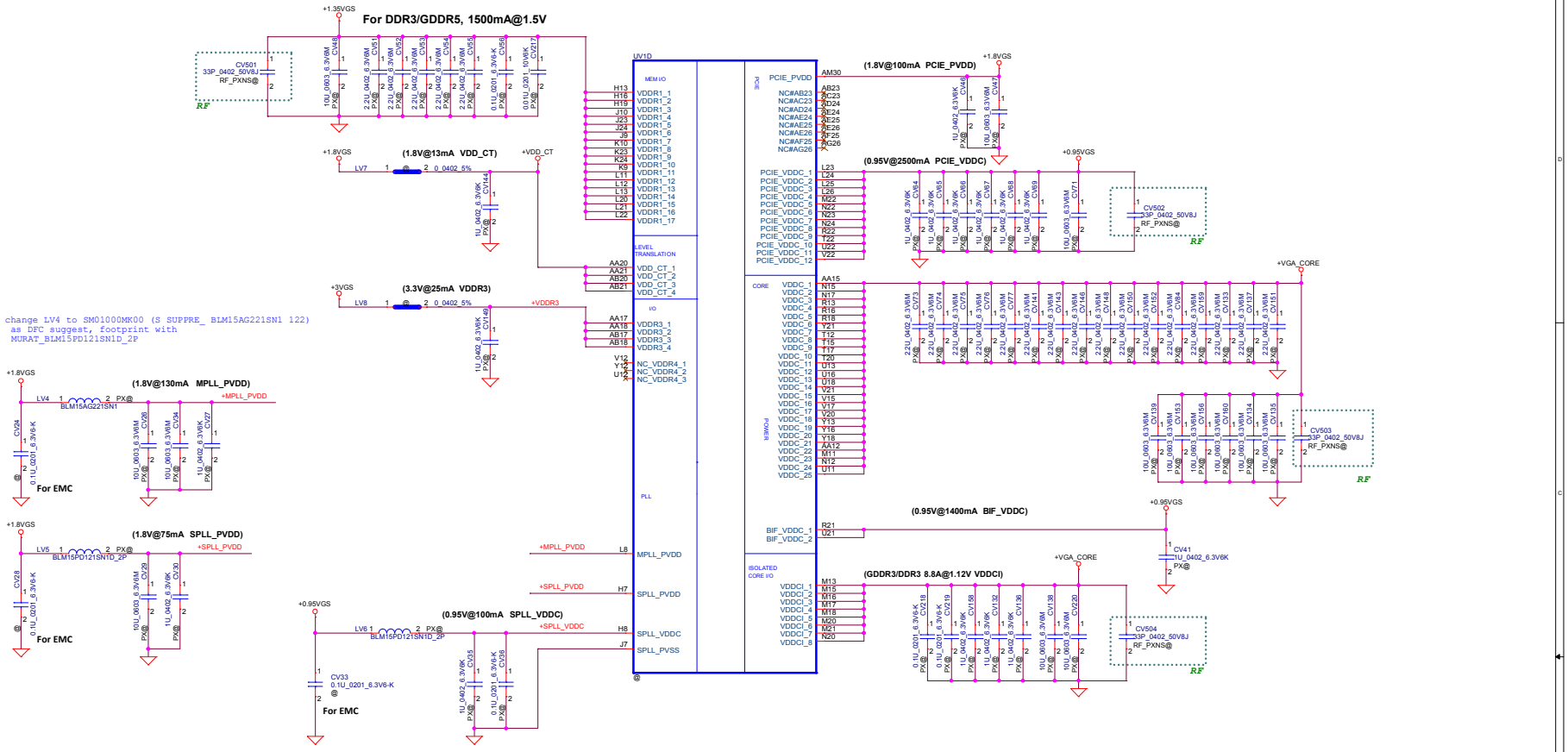
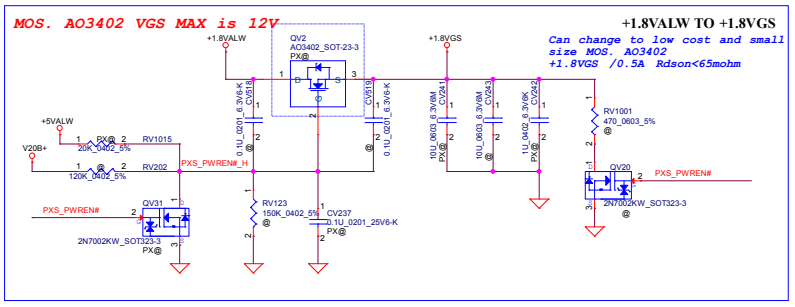
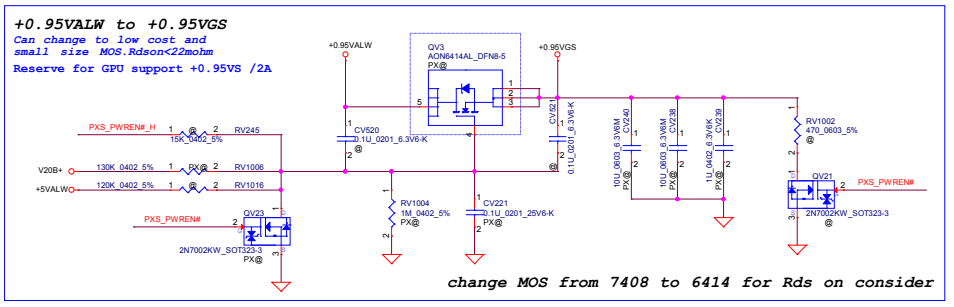
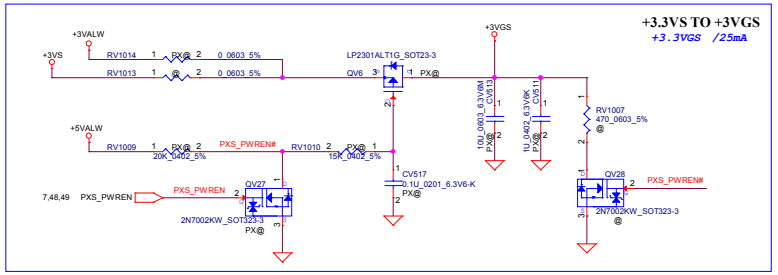
Title: ATI_EXO-PRO_DP Power

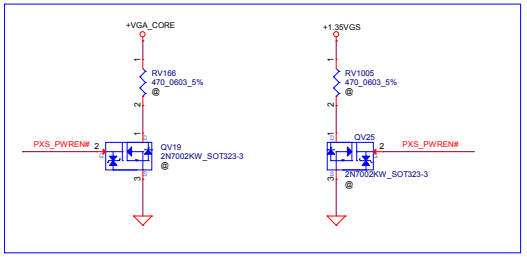
Size: Custom	Document Number: 320AST	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 18 of 50	











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Title	ATI_EXO-PRO_Power		
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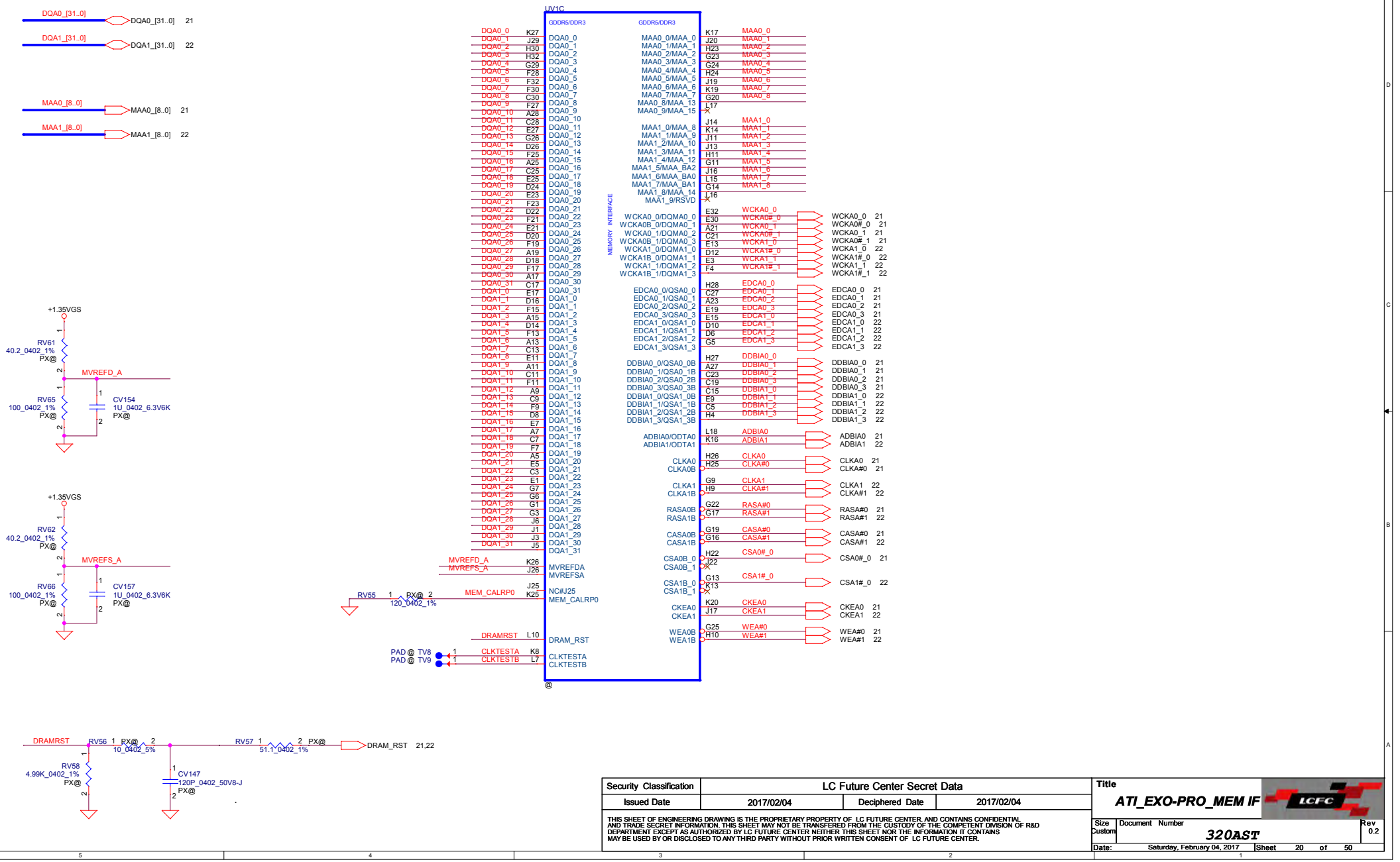
Date: Saturday, February 04, 2017	Sheet 19 of 50		



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Title: ATI_EXO-PRO_MEM IF

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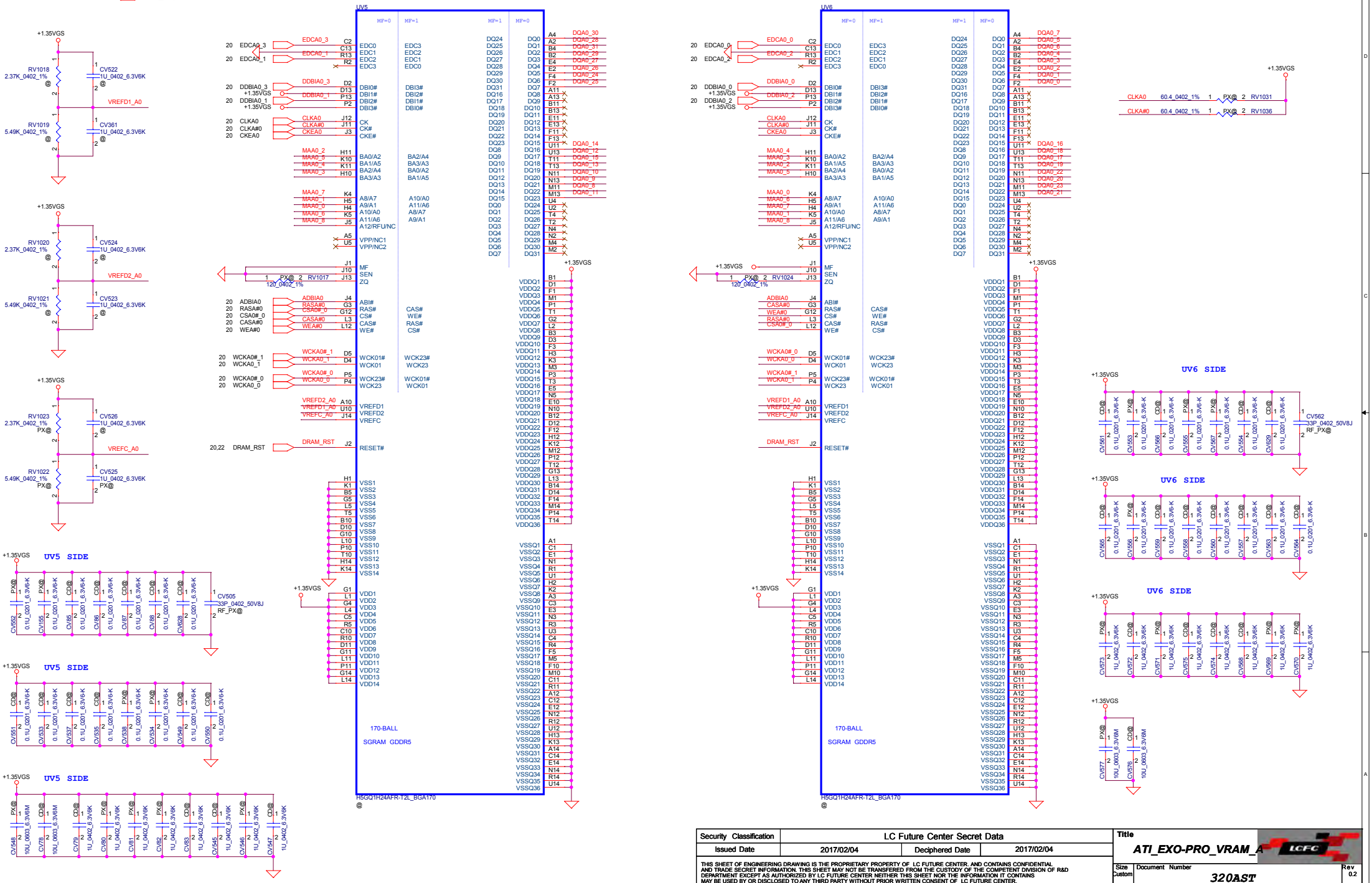
Lower 32 bits

DQA0_[31..0] 20

MAA0_[8..0] 20

MF=0 No Mirror

MF=1 Mirror



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Title: ATI_EXO-PRO_VRAM_A

Size: Custom | Document Number: 320AST | Rev: 0.2

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Upper 32 bits

DQA1_[31..0] 20

MAA1_[8..0] 20

MF=1 Mirror

MF=0 No Mirror

UV7

UV8

MF=0 MF=1 MF=1 MF=0

+1.35VGS

RV1025 2.37K_0402_1% @ CV528 1U_0402_6.3V6K @ VREFD2_A1

RV1026 5.49K_0402_1% @ CV527 1U_0402_6.3V6K @

RV1028 2.37K_0402_1% @ CV530 1U_0402_6.3V6K @ VREFD1_A1

RV1027 5.49K_0402_1% @ CV529 1U_0402_6.3V6K @

RV1029 2.37K_0402_1% PX@ CV532 1U_0402_6.3V6K @ VREFC_A1

RV1030 5.49K_0402_1% PX@ CV531 1U_0402_6.3V6K PX@

UV7 SIDE

CV596 33P_0402_50V8J RF_PX@

UV7 SIDE

UV7 SIDE

UV8 SIDE

UV8 SIDE

UV8 SIDE

CLKA1 60.4_0402_1% PX@ RV1037

CLKA#1 60.4_0402_1% PX@ RV1038

CV613 33P_0402_50V8J RF_PX@

170-BALL SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170 @

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Title: ATI_EXO-PRO_VRAM_B

Size: Custom | Document Number: 320AST | Rev: 0.2

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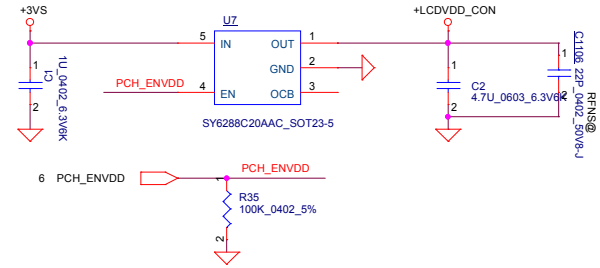
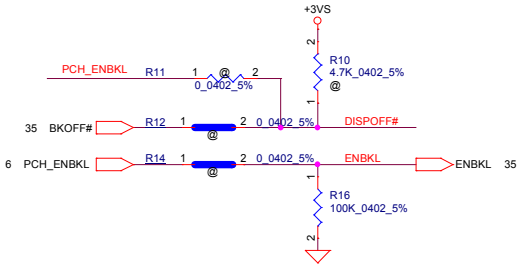
LCD POWER CIRCUIT

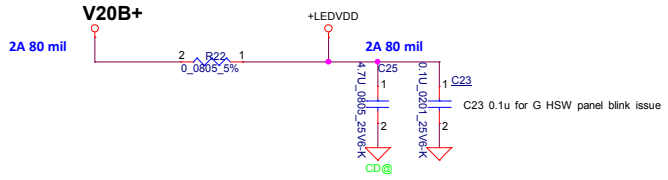


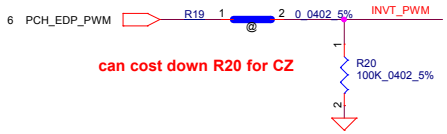
APU output enable Voh min is 1.8V-0.45V=1.35V



Touch Screen

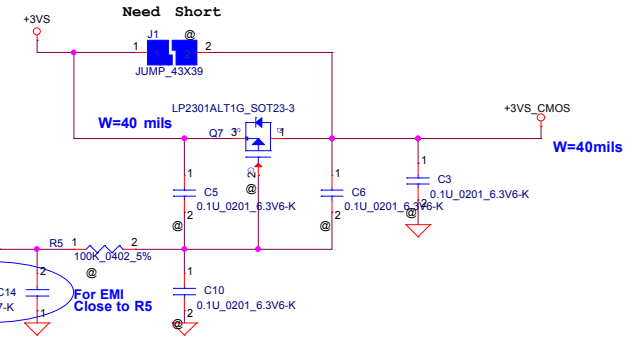
B+ to +LEDVDD POWER

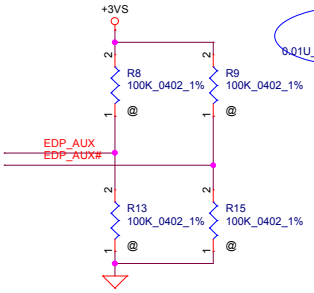


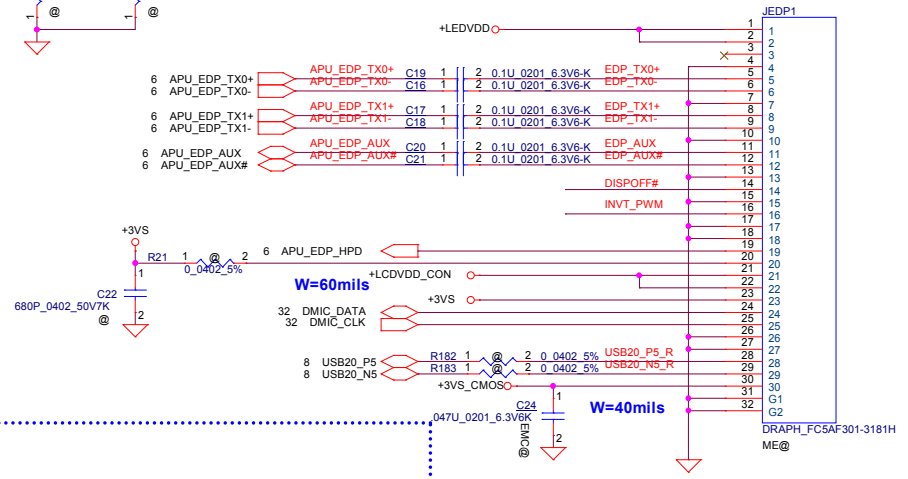


can cost down R20 for CZ

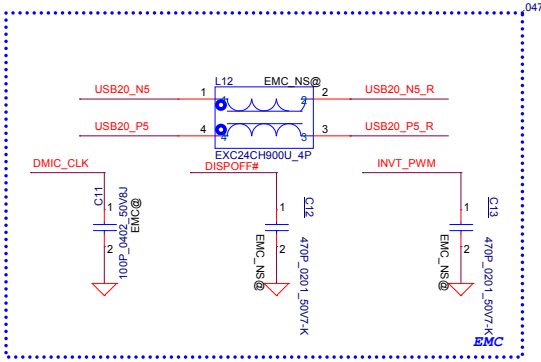
CMOS Camera







Remove Touch screen for 320 AST



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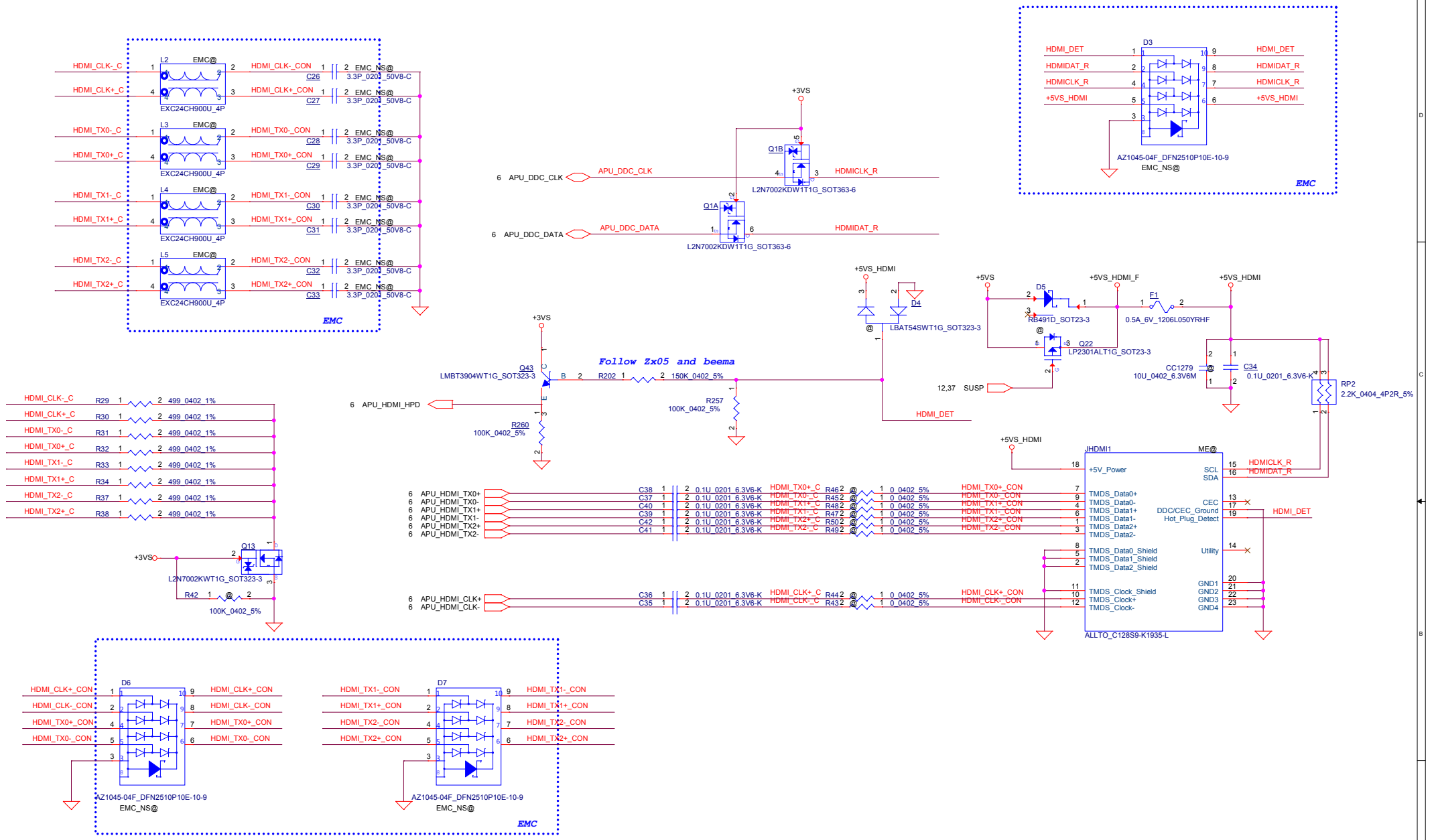
Title	eDP/CMOS/Touch screen		
Size: Custom	Document Number: 320AST		Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 23 of 50		



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Title: **HDMI_CONN**

Size	Document Number	Rev
Custom	320AST	0.2

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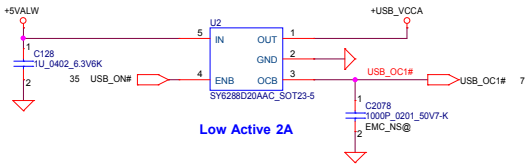
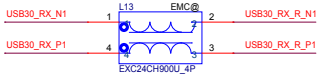
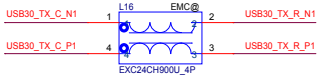
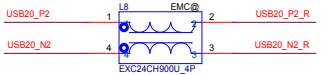
LEFT SIDE USB3.0 PORT x2



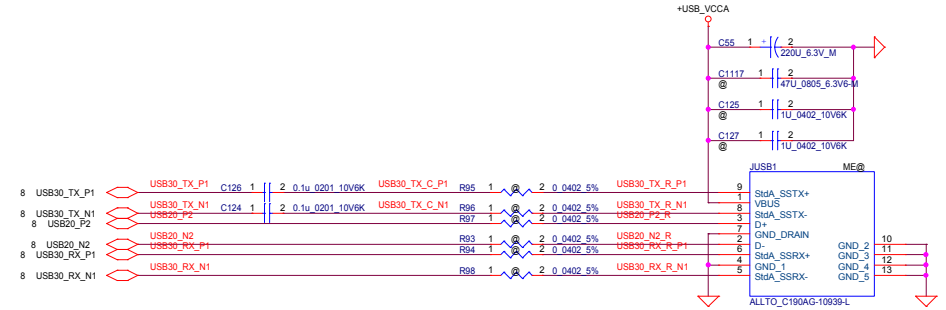
Low Active 2A



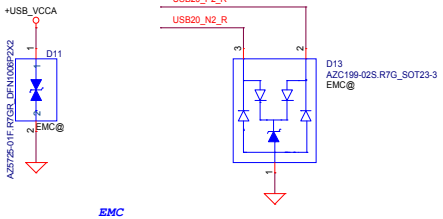




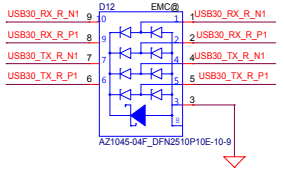
EMC

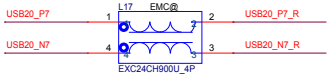


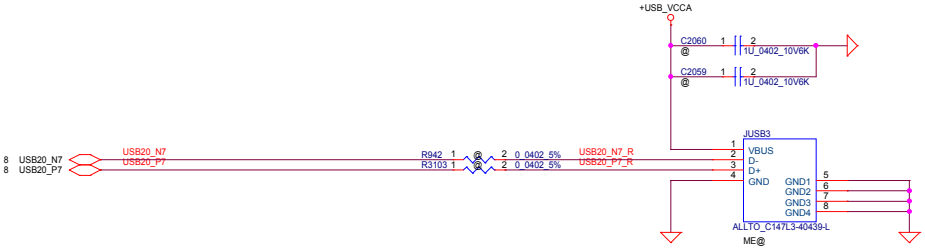
09/05 Update USBConn. P/N DC021609011 wei



EMC

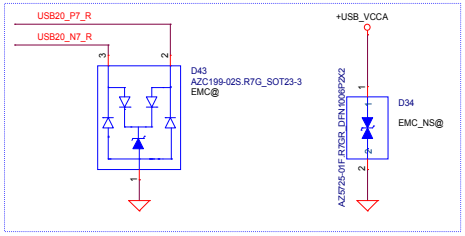






09/05 Update USBConn. P/N DC021609011 wei

FOR ESD Close to Connector



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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Title	USB3.0 PORT (LEFT)		
Size C	Document Number 320AST		Rev 0.2
Date: Saturday, February 04, 2017	Sheet 25 of 50		

Remove USB Type-C follow OD

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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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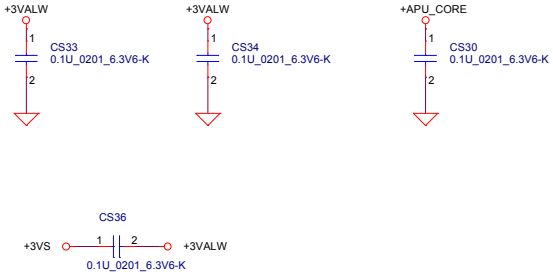
Title: *3D Camera*

Size: Custom	Document Number: *320AST*	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 26 of 50	



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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Title: ***DP to CRT Convert(IT6515FN)***

Size	Document Number	Rev
Custom	***320AST***	0.2

Date: Saturday, February 04, 2017 | Sheet 27 of 50

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%) 0.5ms<spec<10 0ms

Need short

width : 40 mils

JUMP_43X79

LP2301ALT1G_SOT23-3

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

APU CLKREQ all both 3VS power plane

CL10 close to Pin18
CL11 close to Pin17

RTL8106E-CG_QFN32_4X4

8106E@

follow G CarrizoL 10pf

For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuf f

Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

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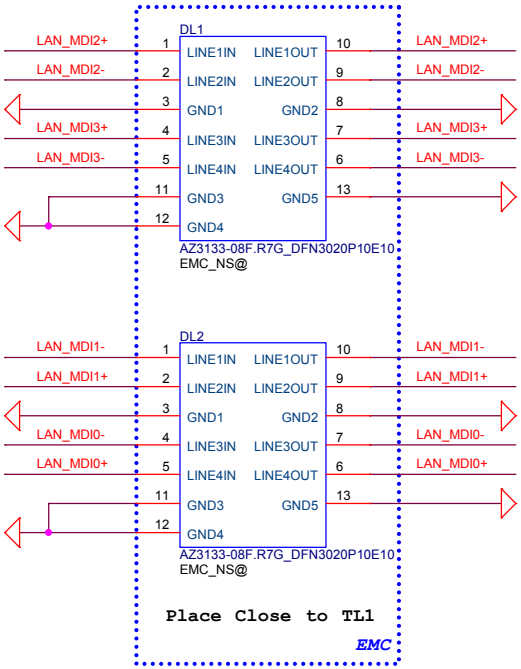
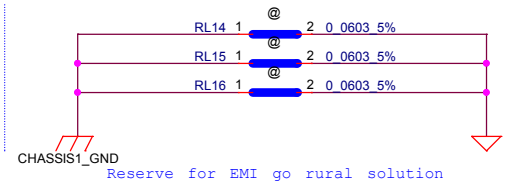
Title: LAN_RTL8111GUL

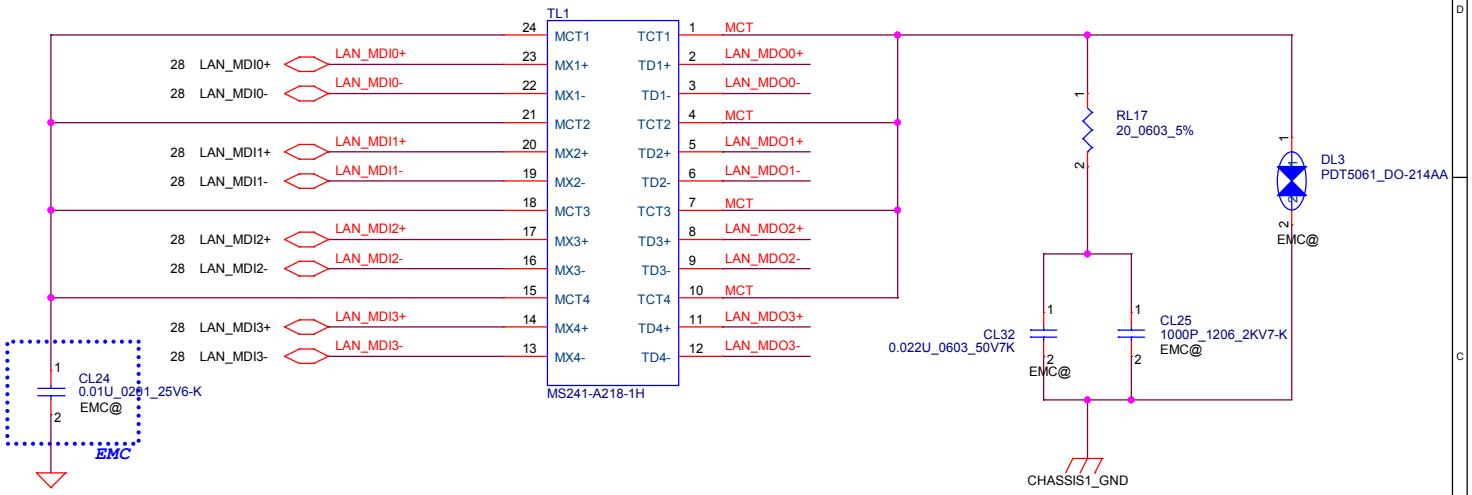
Size: Custom | Document Number: 320ABR | Rev: 0.2

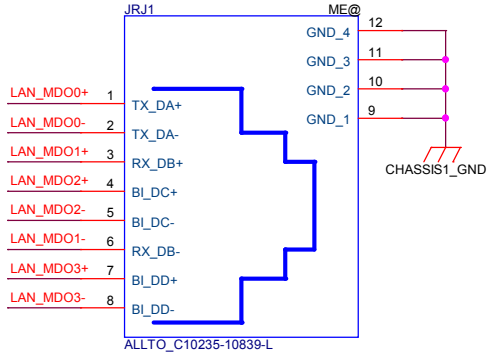
Date: Saturday, February 04, 2017 | Sheet 28 of 50

DL1/DL2
1'S PN:SC300003M00









Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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Title	LAN_Transformer		
Size B	Document Number 320ABR		Rev 0.2
Date: Saturday, February 04, 2017	Sheet 29 of 50		

Close to U1

C44 2200P_0402_50V7K

REMOTE+_R

REMOTE-_R

R175 R176 R177 R178 0_0402_5%

REMOTE1+ REMOTE2+ REMOTE2- REMOTE1-

REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Near GPU&VRAM

C45 100P_0402_50V8J

Q15 LMBT3904WT1G_SOT323-3

Near CPU core

C46 100P_0402_50V8J

Q16 LMBT3904WT1G_SOT323-3

SMSC thermal sensor
placed near DIMM

U1 NCT7718W_MSOP8

VDD D+ D- T_CRIT# SCL SDA ALERT# GND

EC_SMB_CK3 EC_SMB_DA3 6,16,35

C47 0.1U_0201_6.3V6-K

R51 10K_0402_5%

Address 1001_101xb

+3VALW

R17 13.7K_0402_1%

NTC_V1

R1 100K_0402_1%_TSM0B104F4251RZ PX@

R184 R185 0_0402_5% PX@

EC_AGND

Near CPU

R25 13.7K_0402_1%

NTC_V2

R3 100K_0402_1%_TSM0B104F4251RZ

R191 R192 0_0402_5%

HW thermal sensor

C4 0.1U_0201_6.3V6-K

U4 G718TM1U_SOT23-8

VCC TMSNS1 GND RHYST1 OT1 TMSNS2 OT2 RHYST2

TMSNS1 PHYST1 TMSNS2 PHYST2

R252 R253 21.5K_0402_1%

R196 R197 0_0402_5%

NTC_V1 35 NTC_V2 35

46 EC_ON_R

R6 R7 10K_0402_5%

over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

TPM

UTPM1 Z32H320TC-LPC-T28-LT1_TSSOP28

RTPM1 RTPM2 RTPM12 RTPM11 RTPM4 RTPM5 RTPM6 RTPM7 RTPM8 RTPM9 RTPM10 RTPM13

CTPM4 CTPM1 CTPM3

Reserve for Nationz TPM

Add for Nuvoton TPM

Reserve for Nuvoton TPM

SERIRQ LPC_AD0 LPC_AD1 LPC_FRAME# LPC_AD2 LPC_AD3 LPC_CLKRUN# TPM_CLK PLT_RST# 7,15,28,31,35

R52 C49 10U_0805_10V6K C50 0.1u_0201_10V6K

+5VS_FAN

EC_FAN_SPEED EC_FAN_PWM

JFAN1 ACES_85205-04001 ME@

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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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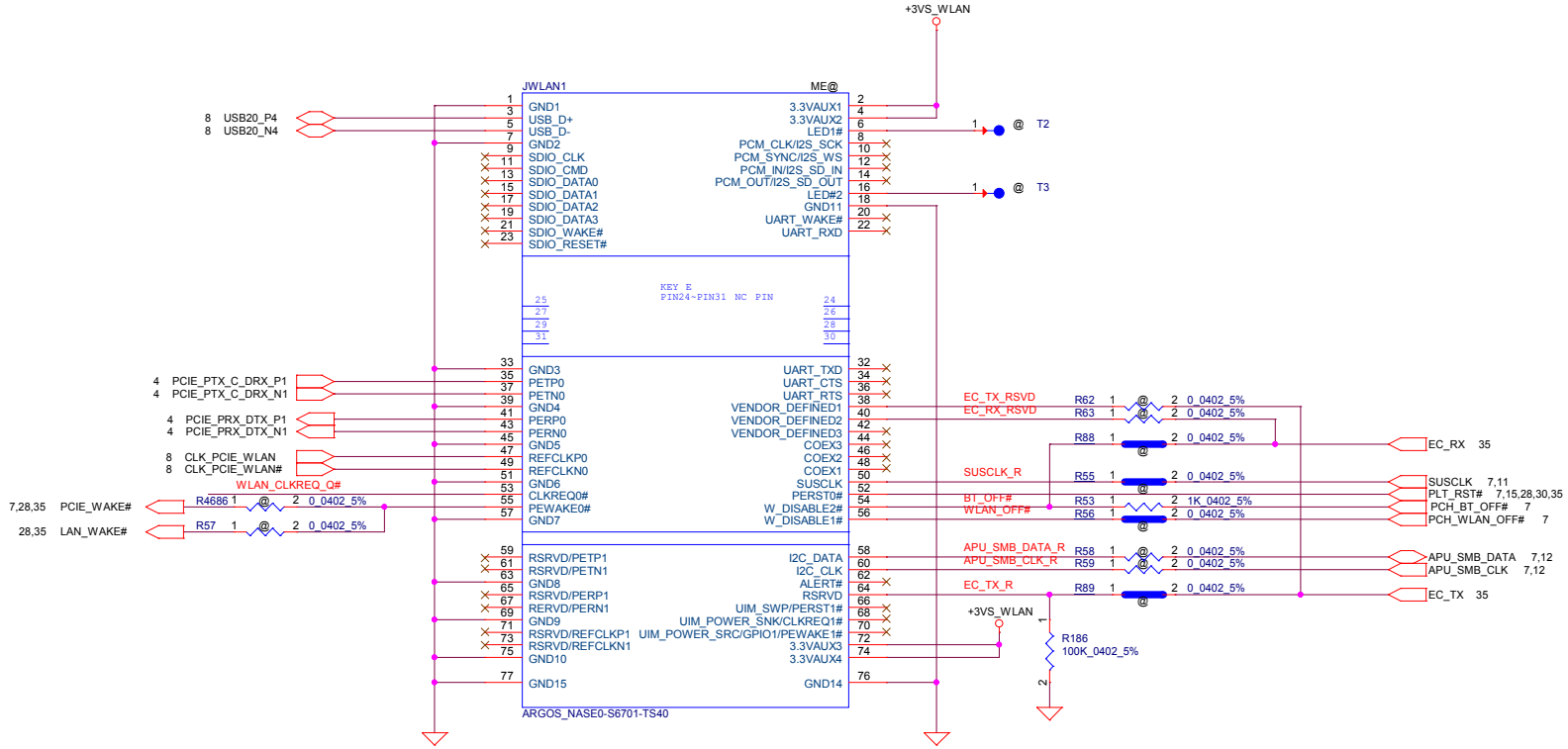
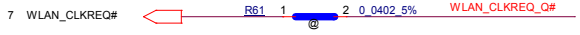
Title: Thermal sensor/FAN CONN/TPM

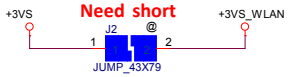
Size: Custom | Document Number: 320AST | Rev: 0.2

Date: Saturday, February 04, 2017 | Sheet 30 of 50

Mini-Express Card(WLAN/WiMAX)







If support AOAC, NC R61;
if not support AOAC, stuff R61.

Not support AOAC, delete AOAC power circuit 1015

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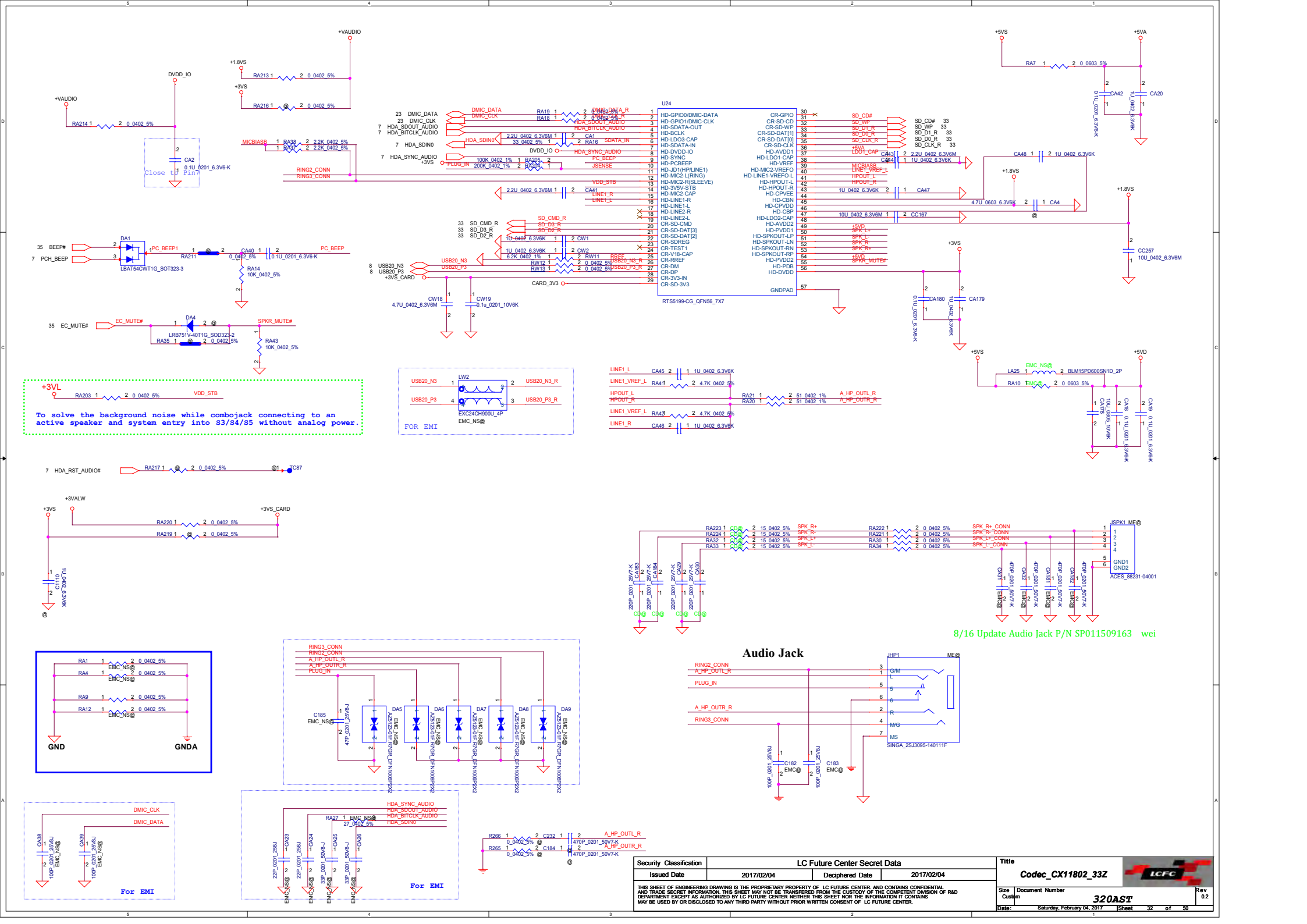
Title: NGFF WLAN

Size	Document Number	Rev
Custom	320AST	0.2

Date: Saturday, February 04, 2017 Sheet 31 of 50



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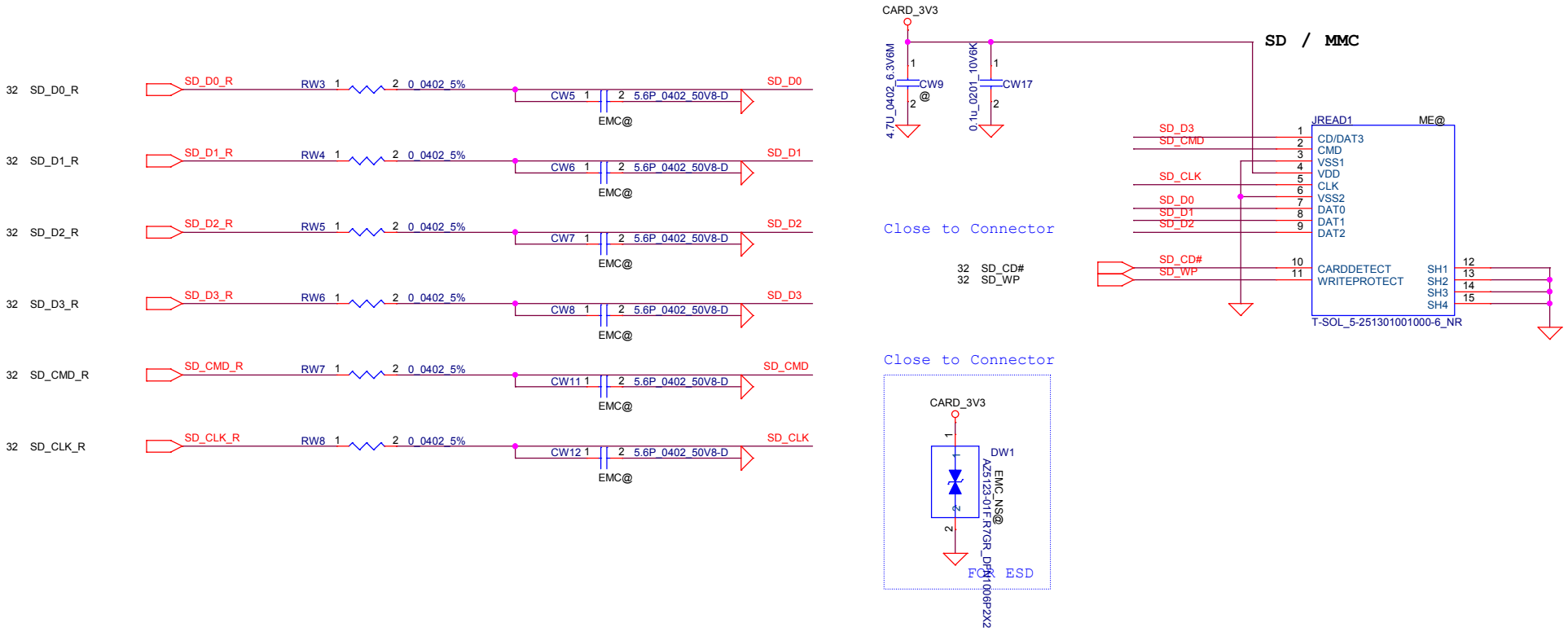
Title: Codec_CX11802_33Z

Size: Custom | Document Number: 320AST | Rev: 0.2

Date: Saturday, February 04, 2017 | Sheet 32 of 50



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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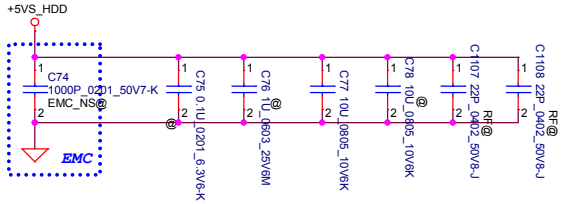
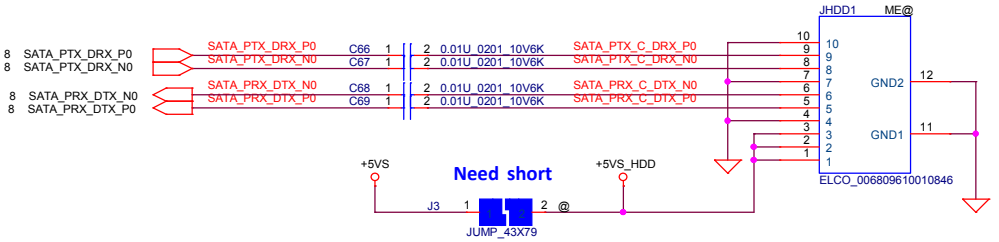
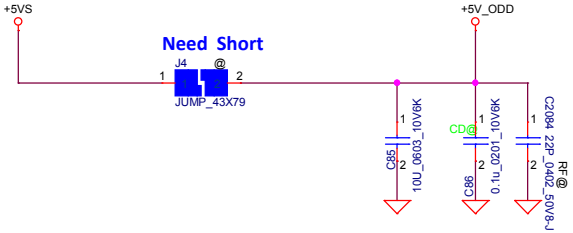
Title: **CardReader**

Size: B	Document Number: 320AST	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 33 of 50	



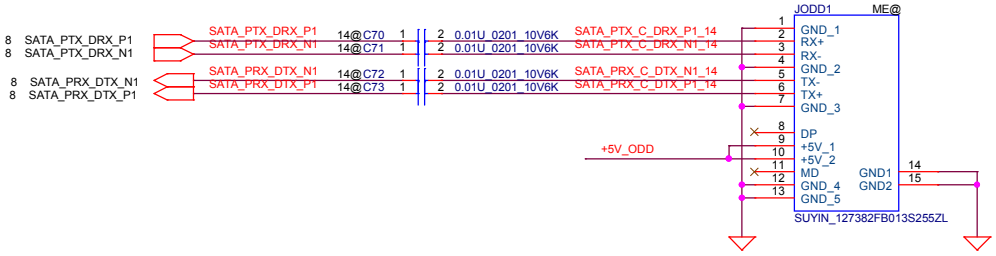
SATA HDD Conn.

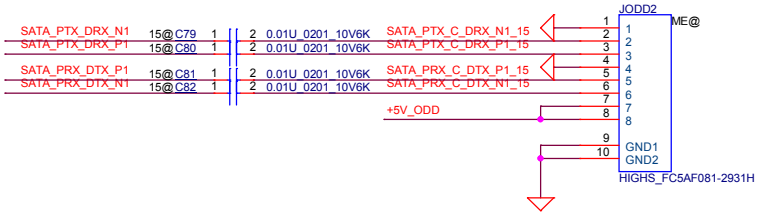




SATA 15 ODD P/N pin assgin is different from G SKL

FOR 14" SATA ODD Conn.





8/16 Update Conn. P/N SP01001YV00 wei

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Title	HDD/ODD CONN		
Size	Document Number		Rev
Custom	320AST		0.2
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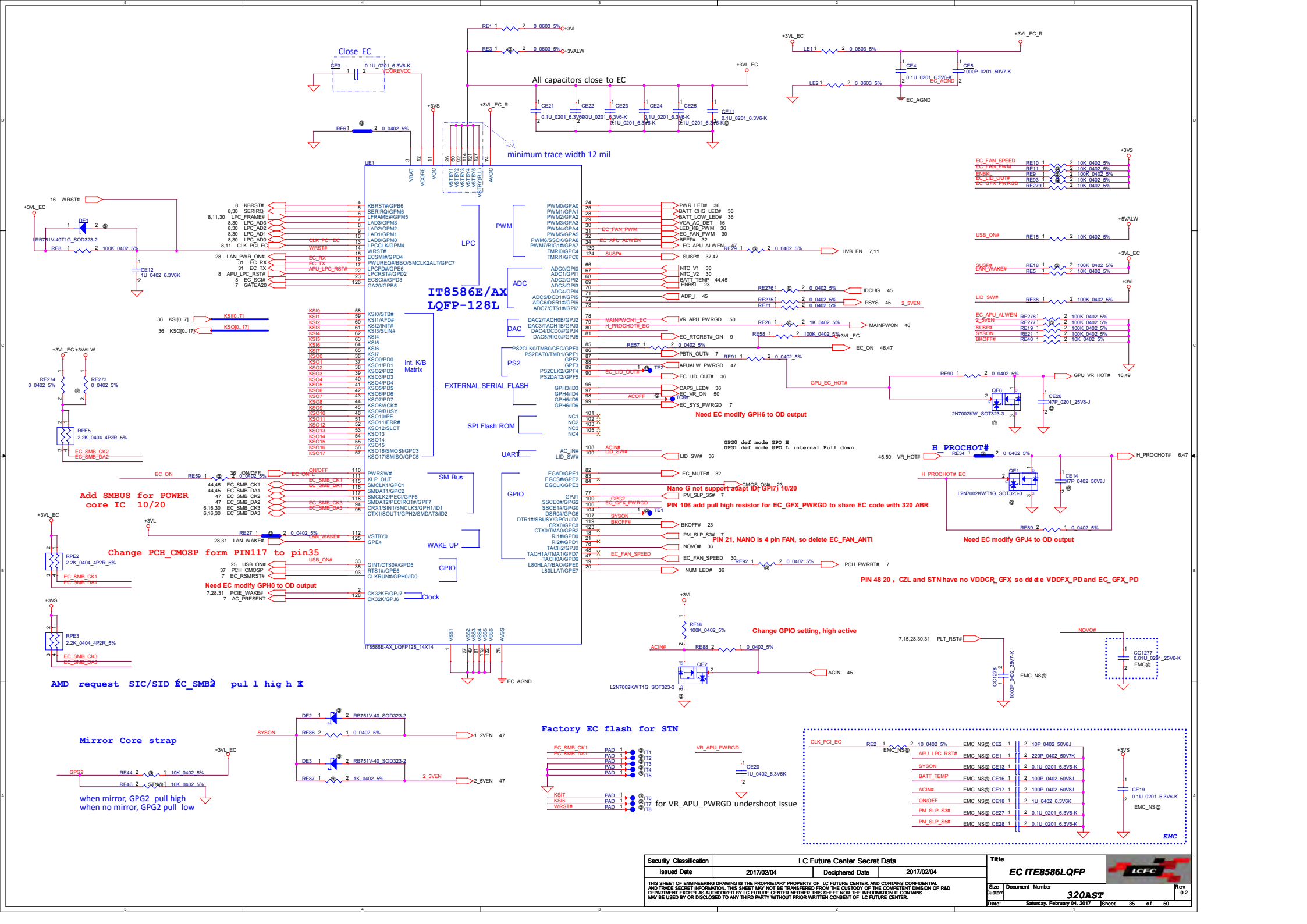

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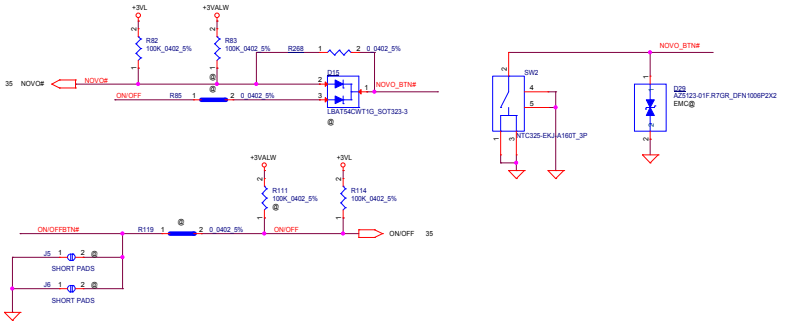
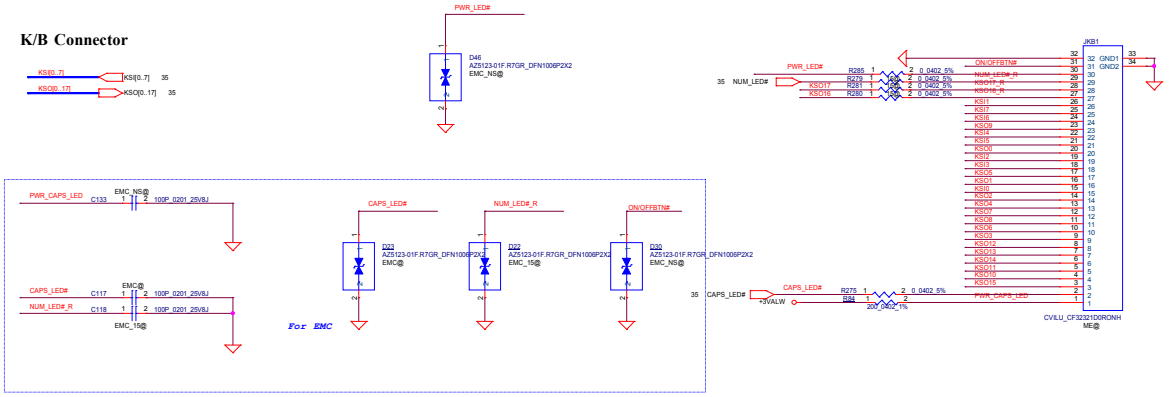
Title	EC ITE8586LQFP		
Size	Document Number		Rev
Custom	320AST		0.2
Date:	Saturday, February 04, 2017	Sheet	35 of 50

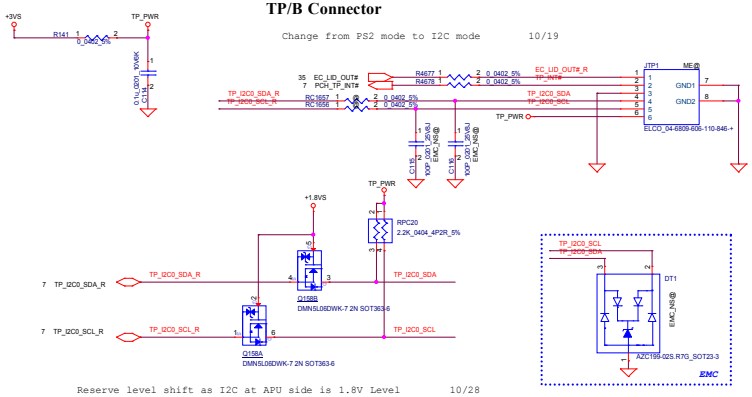
ON/OFF switch



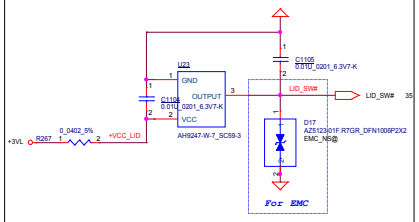
K/B Connector



TP/B Connector

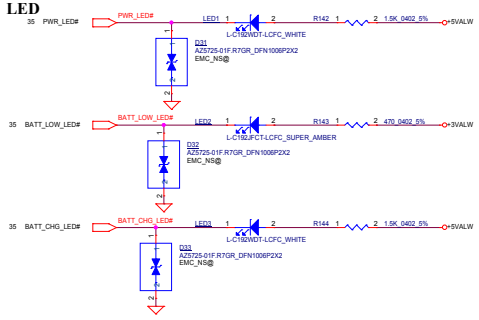


LID Connector

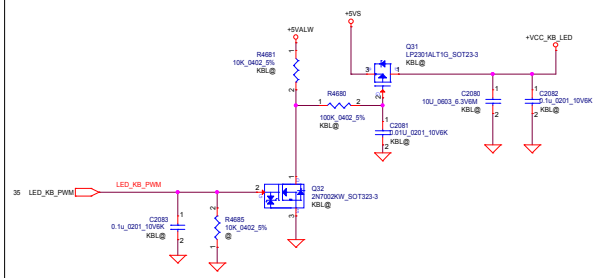


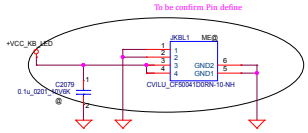
Finger Print Connector

LED



KB Backlight Connector





8/31 Update KBL Conn. P/N SP011608241 wei

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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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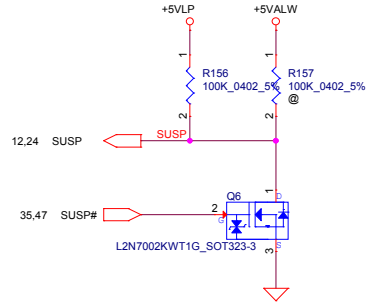
Title: KBD/PWR/IO/LED/TP Conn.

Size: Custom | Document Number: 320AST | Rev: 0.2

Date: Saturday, February 04, 2017 | Sheet 38 of 50



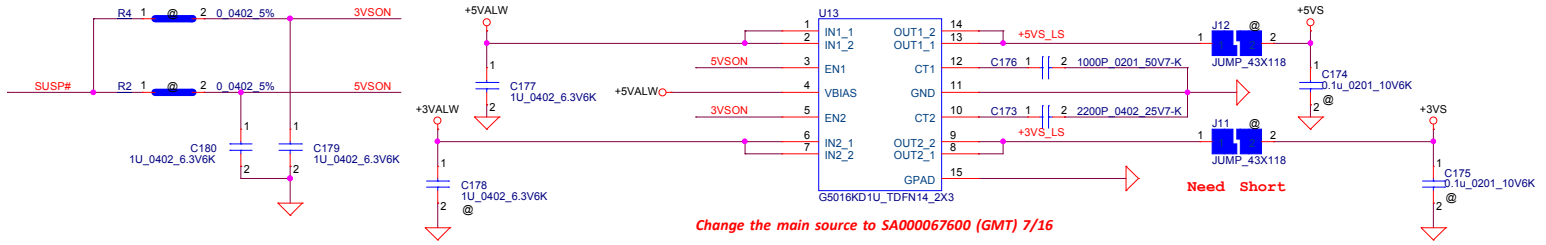
Load Switch

+5VALW To +5VS — **+3VS, C173 --> 2.74ms**

+3VALW To +3VS — **+5VS, C176 --> 2.03ms**

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short



Need Short

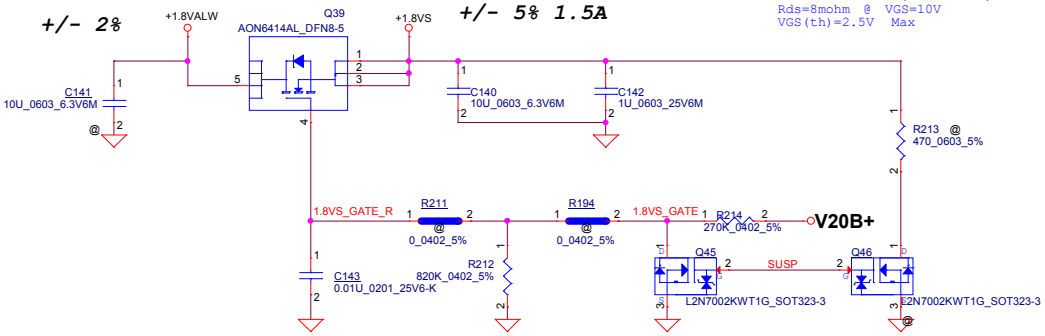
Change the main source to SA000067600 (GMT) 7/16

+1.8VALW to +1.8VS

+/- 2%

+/- 5% 1.5A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

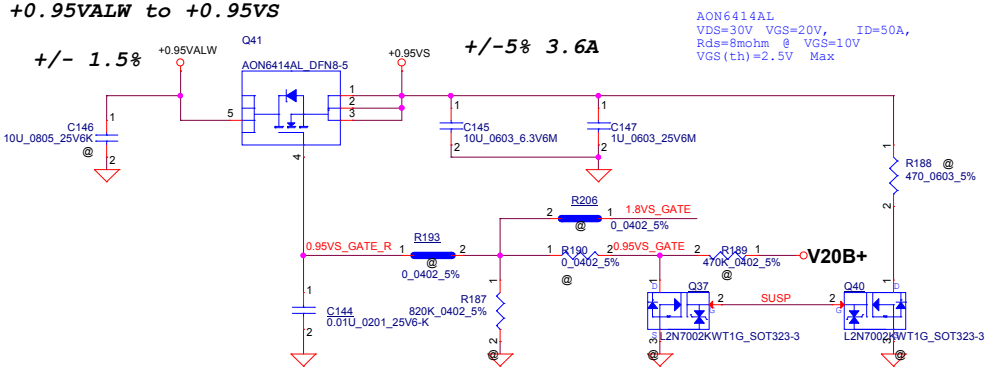


+0.95VALW to +0.95VS

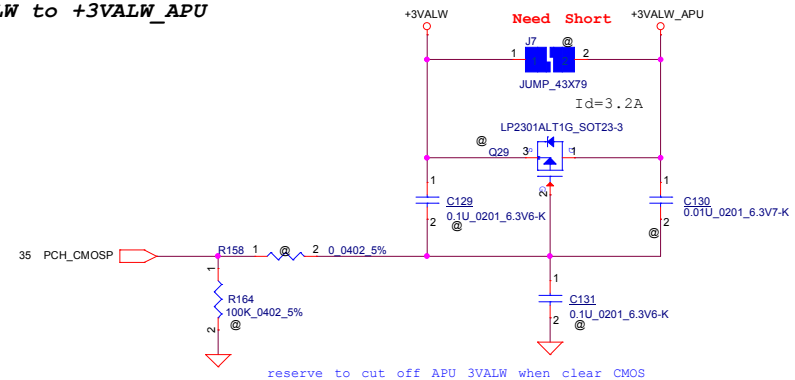
+/- 1.5%

+/-5% 3.6A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

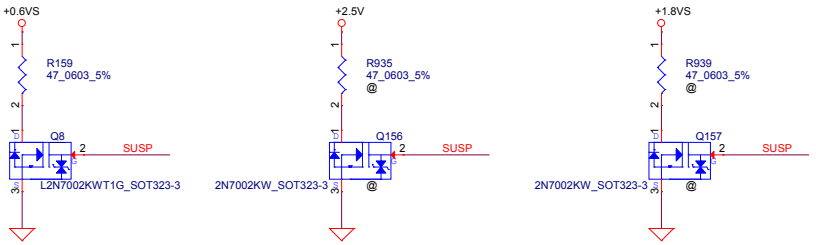


+3VALW to +3VALW_APU



reserve to cut off APU 3VALW when clear CMOS

For DisCharge



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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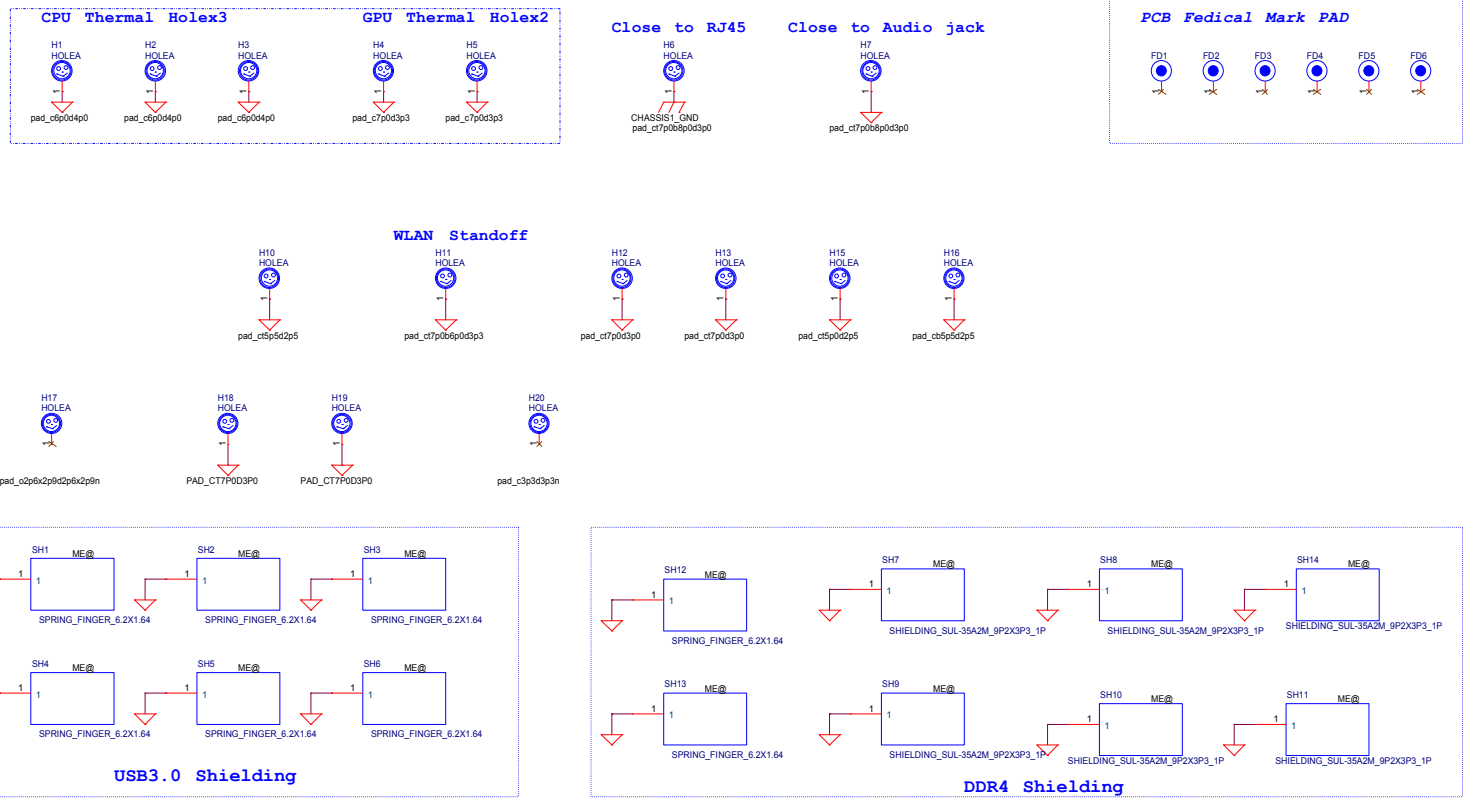
Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
Custom	320AST		0.2
Date:	Saturday, February 04, 2017	Sheet	37 of 50



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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Title: Hole

Size	Document Number	Rev
C	320AST	0.2

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ZZZ1

PCB PN
DA600013D00

PCB

HDMI@

ZZZ2

HDMI PN
RO00000040J

HDMI

UL1 8107E@

RTL8107E-CG
SA00007FR00

LAN Chip

UV1 PX@

R17M-M1-70 GPU
SA000086K00

GPU

UC2

AMD A6-9220 2.5G/2C/1M/FT4
A6@
SA00008A600

UC2

AMD E2-9000 1.8G/2C/1M/FT4
E2@
SA00007WW10

UC2

AMD A9-9420 3.0G/2C/1M/FT4
A9@
SA00008A500

UC2

AMD A4-9120 2.2G/2C/1M/FT4
A4@
SA00008A700

APU type

Board ID

BD14@

RC47

2K_0402_5%
SD02820018J

RC1659 BD14@

2K_0402_5%
SD02820018J

BD15@

RC47

2K_0402_5%
SD02820018J

RC1660 BD15@

10K_0402_5%
SD02810028J

BD17@

RC39

10K_0402_5%
SD02810028J

RC1659 BD17@

2K_0402_5%
SD02820018J

BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

ZZZ3 S4GX4@

Samsung
X7643P12001

ZZZ3 H4GX4@

Hynix
X7643Q12001

ZZZ3 M4GX4@

Micron
X7643T12001

VRAM X76 BOM

UV5 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV6 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV7 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV8 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

RV63 S4G_VR@

3.4K_0402_1%
SD03434018J

RV70 S4G_VR@

10K_0402_1%
SD03410028J

VRAM_Samsung 4GX4

UV5 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV6 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV7 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV8 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

RV63 H4G_VR@

4.53K_0402_1%
SD03445318J

RV70 H4G_VR@

4.99K_0402_1%
SD03449918J

VRAM_Hynix 4GX4

UV5 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV6 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV7 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV8 M4G_VR@

EDW4032BABG-70-F
SA000081800

RV63 M4G_VR@

4.75K_0402_1%
SD03447518J

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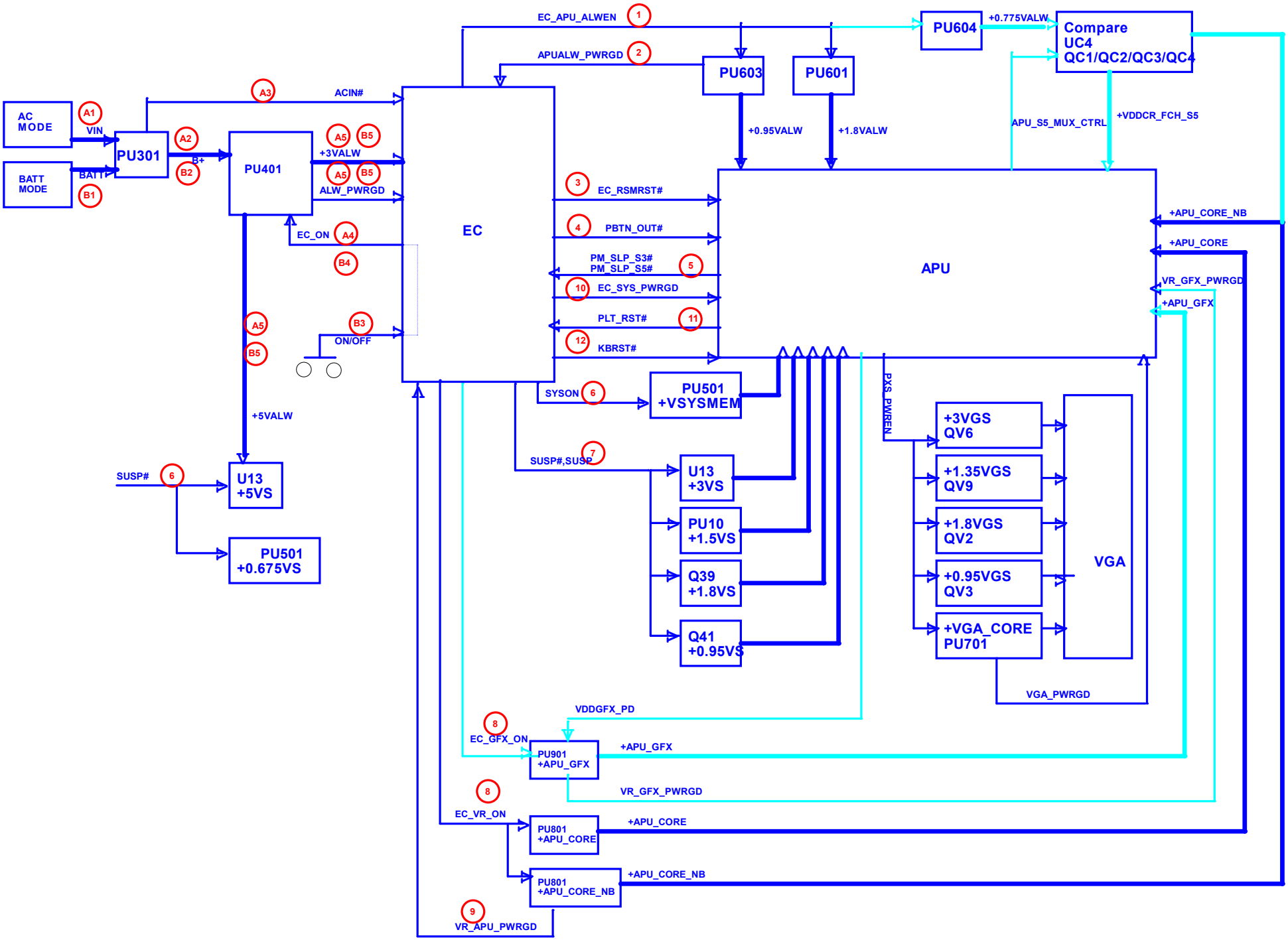
Title: *Virtual symbol*

LCFC

Size	Document Number	Rev
Custom	320AST	0.2

Date: Saturday, February 04, 2017 Sheet 39 of 50



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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Title: *Power sequence Block*

Size	Document Number	Rev
Custom	320AST	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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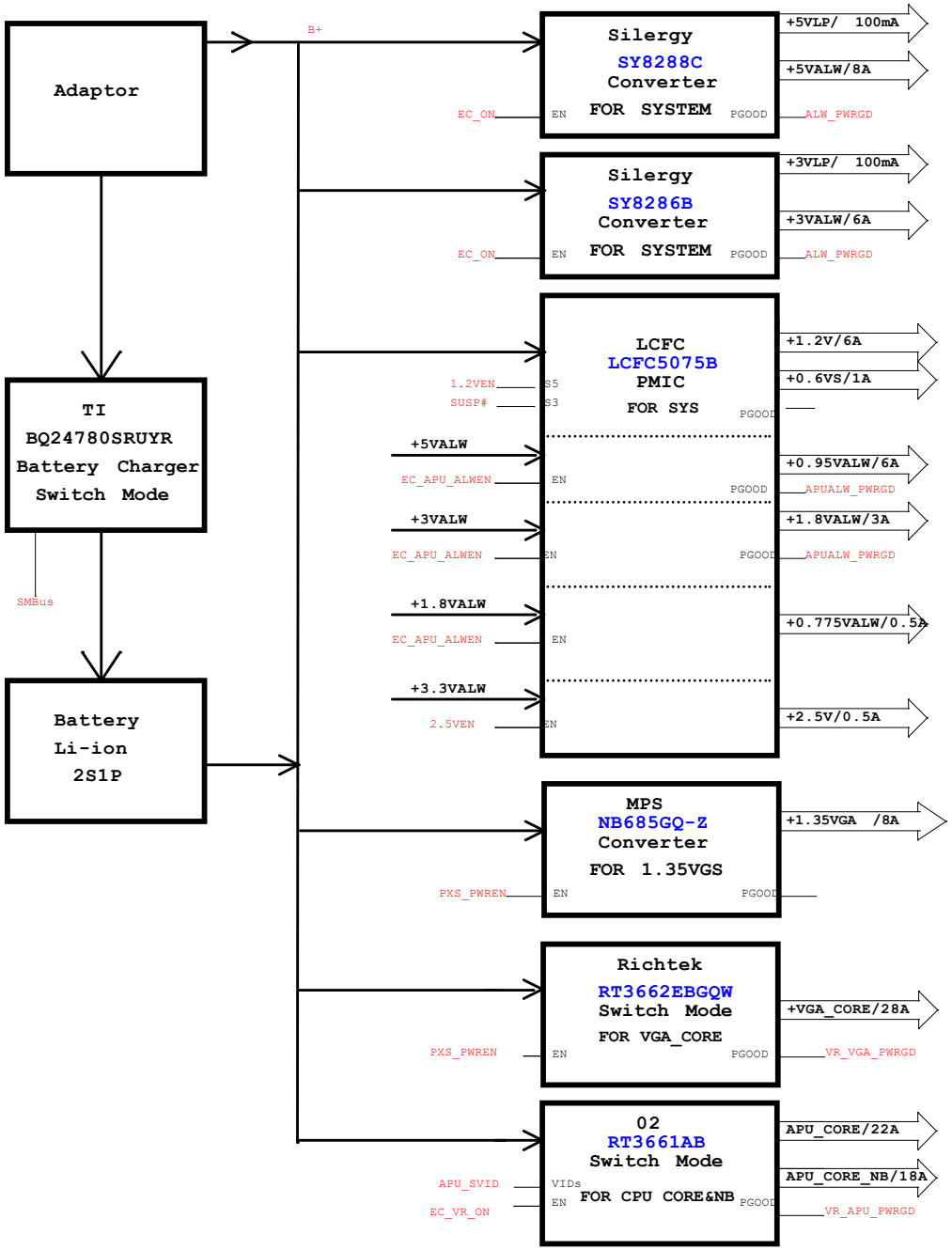
Title

DP to CRT Convert(IT6515FN)

Size: Custom	Document Number: 320AST	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 41 of 50	



Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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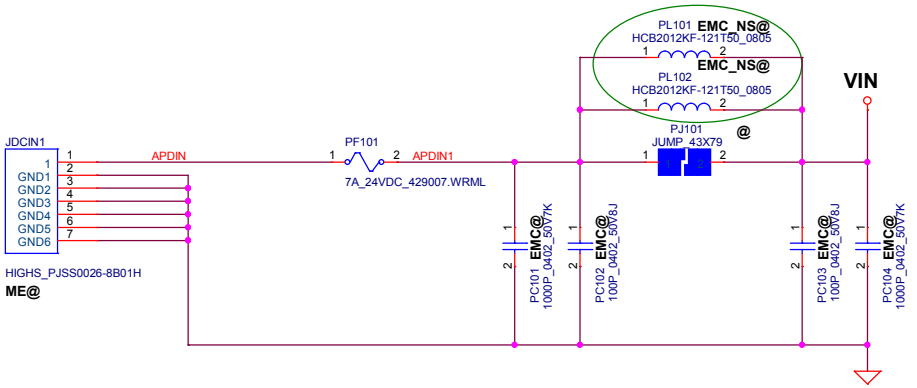
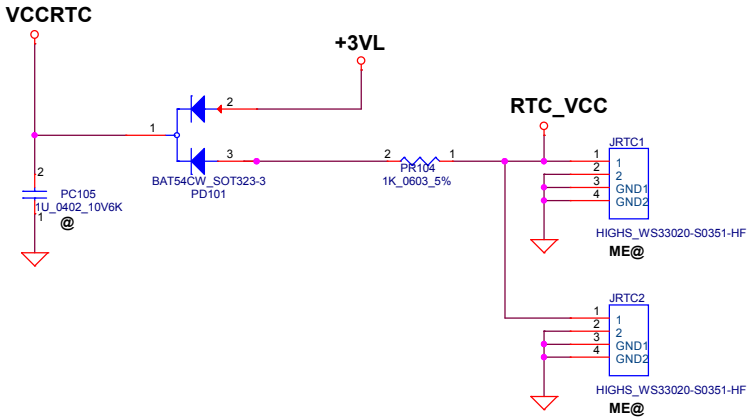
Title: **Power Diagram**

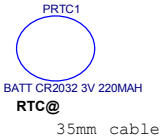
Size	Document Number	Rev
Custom	320AST	0.2

Date: Saturday, February 04, 2017 Sheet 42 of 50

Cost down PL101,PL102 if EMC test pass







35mm cable

RTC Battery for GCM BOM
(2nd source and quoted price)

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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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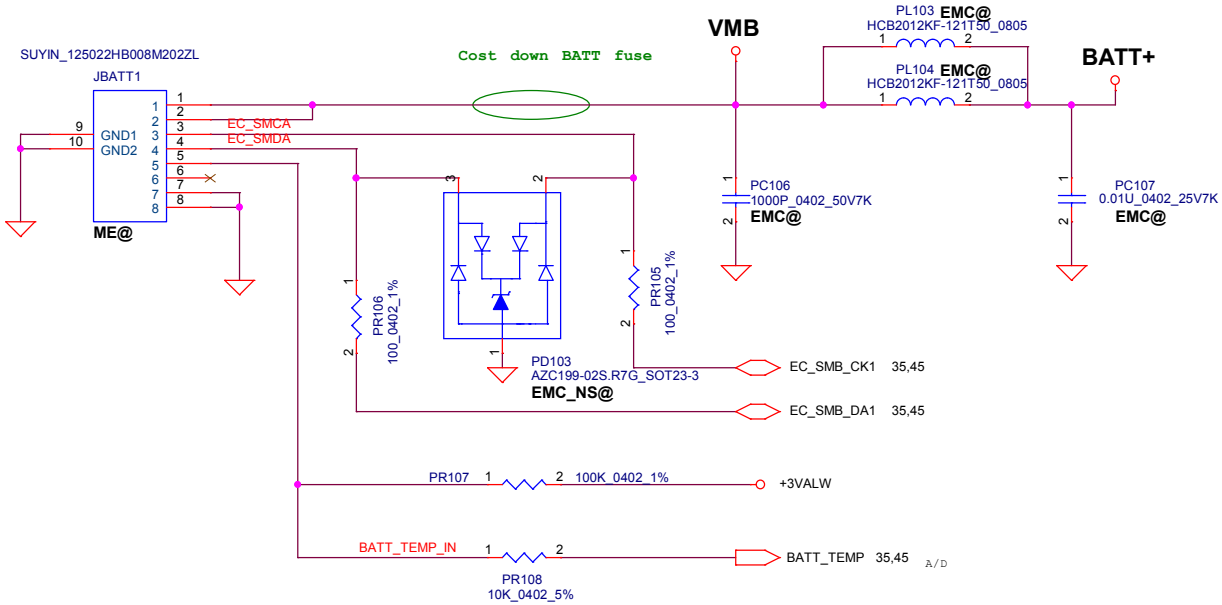
Title: DCIN / RTC

Size: Custom	Document Number: 320ABR	Rev: 0.2
Date: Saturday, February 04, 2017	Sheet 43 of 50	



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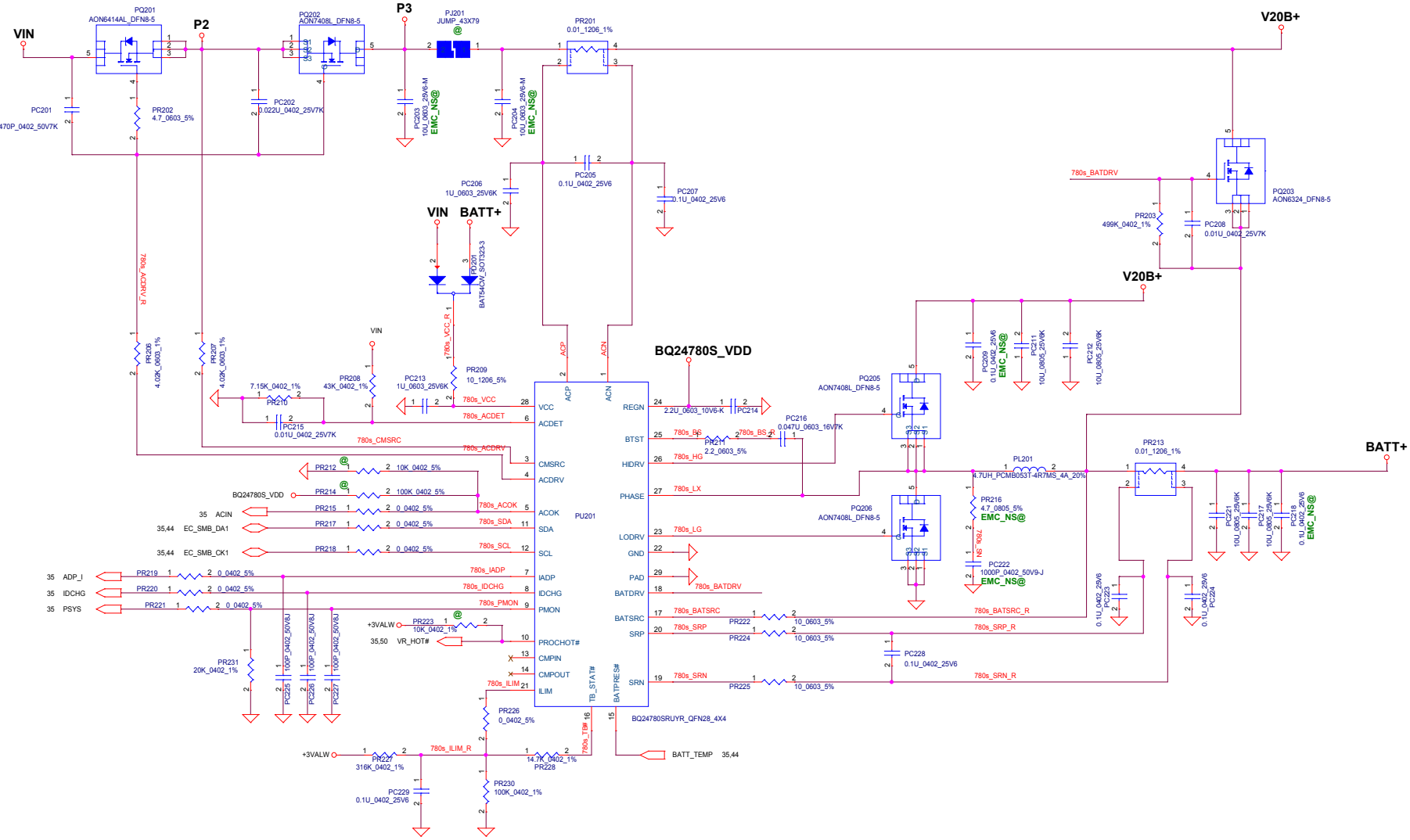
Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
B	320ABR	0.2

Date: Saturday, February 04, 2017 Sheet 44 of 50



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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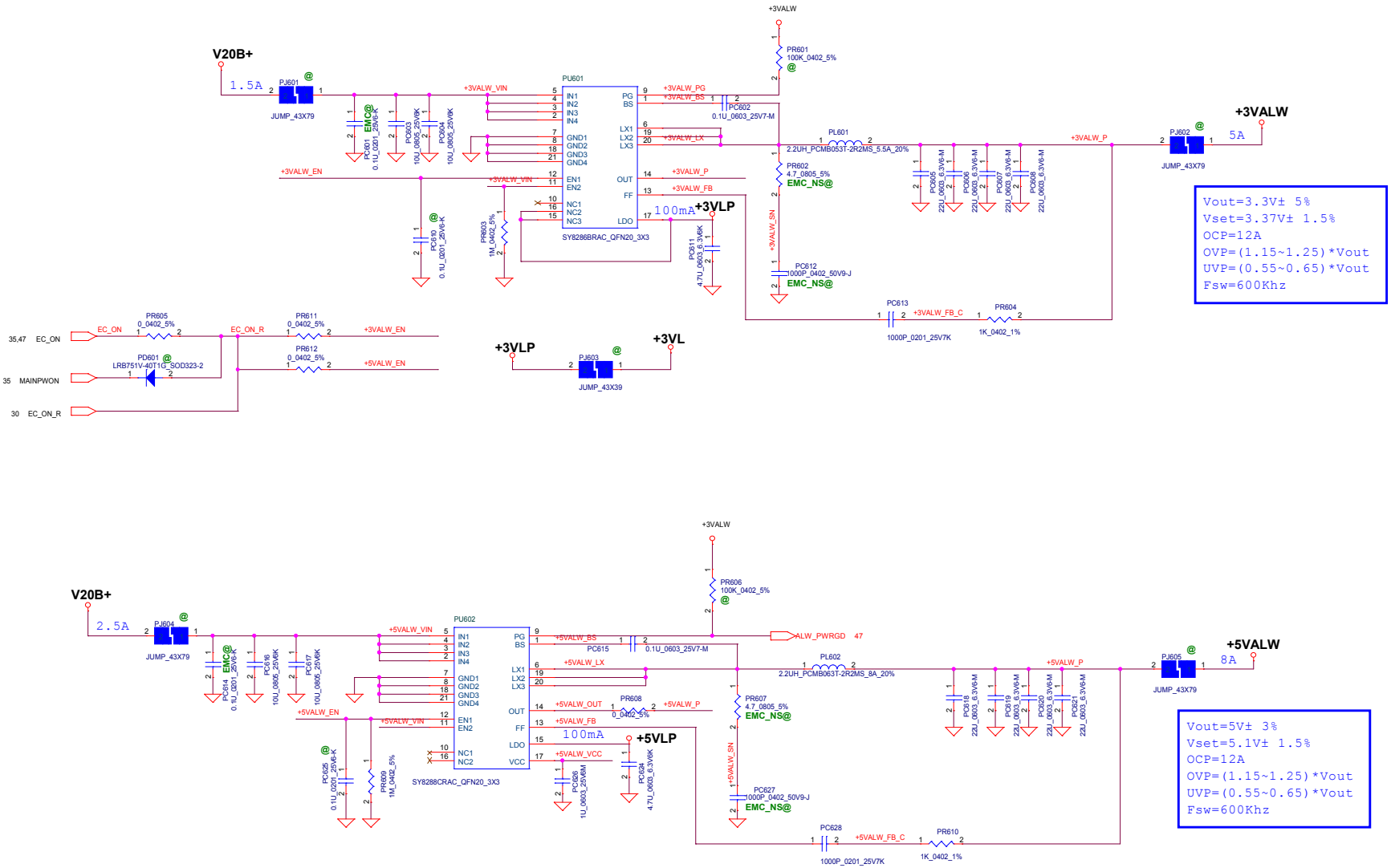
Title	CHARGER		
Size	Document Number		Rev
C	320ABR		0.2
Date:	Saturday, February 04, 2017	Sheet	45 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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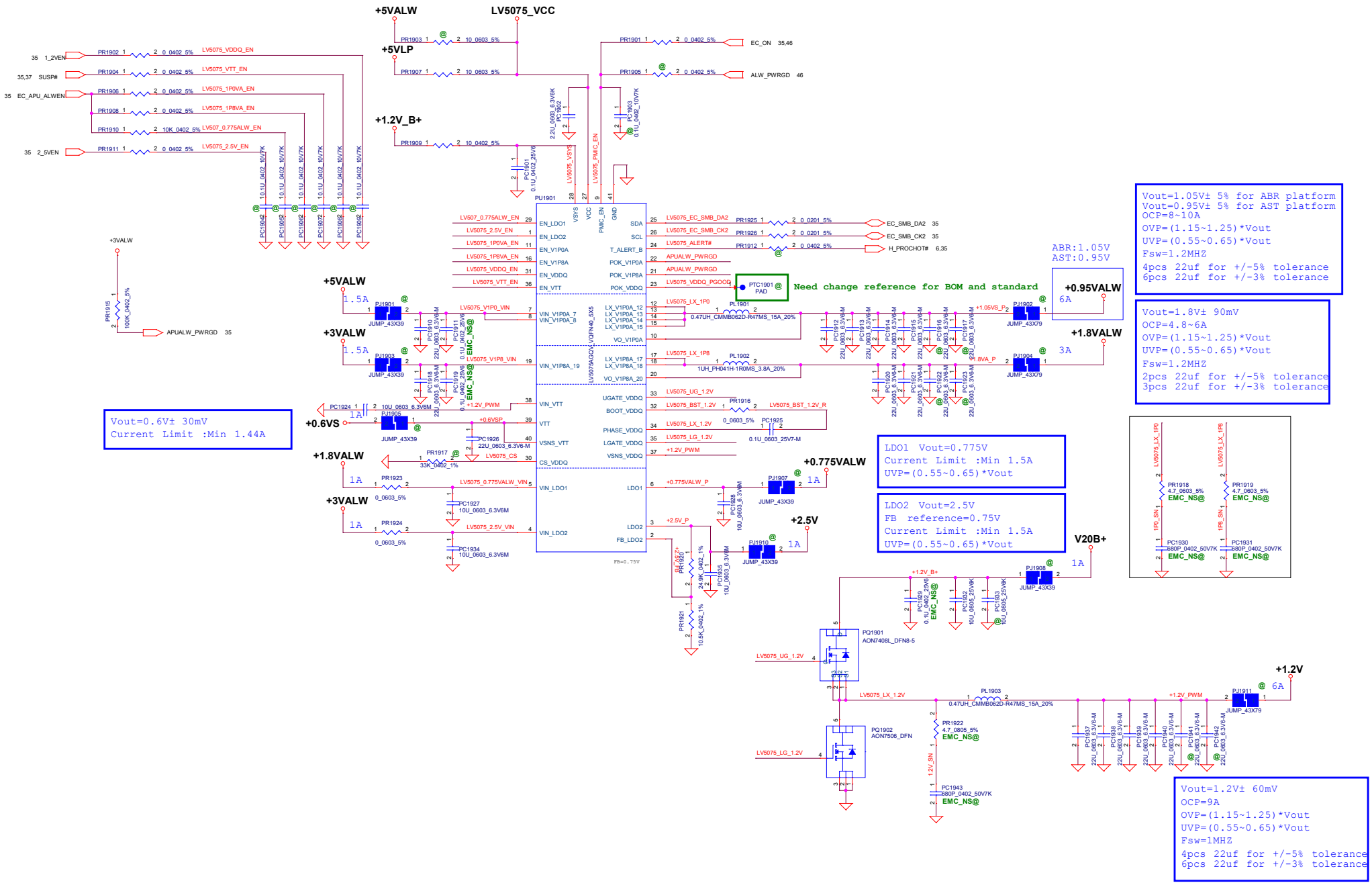
Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	320ABR		0.2
Date:	Saturday, February 04, 2017	Sheet	46 of 50



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Issued Date	2017/02/04	Deciphered Date	2017/02/04

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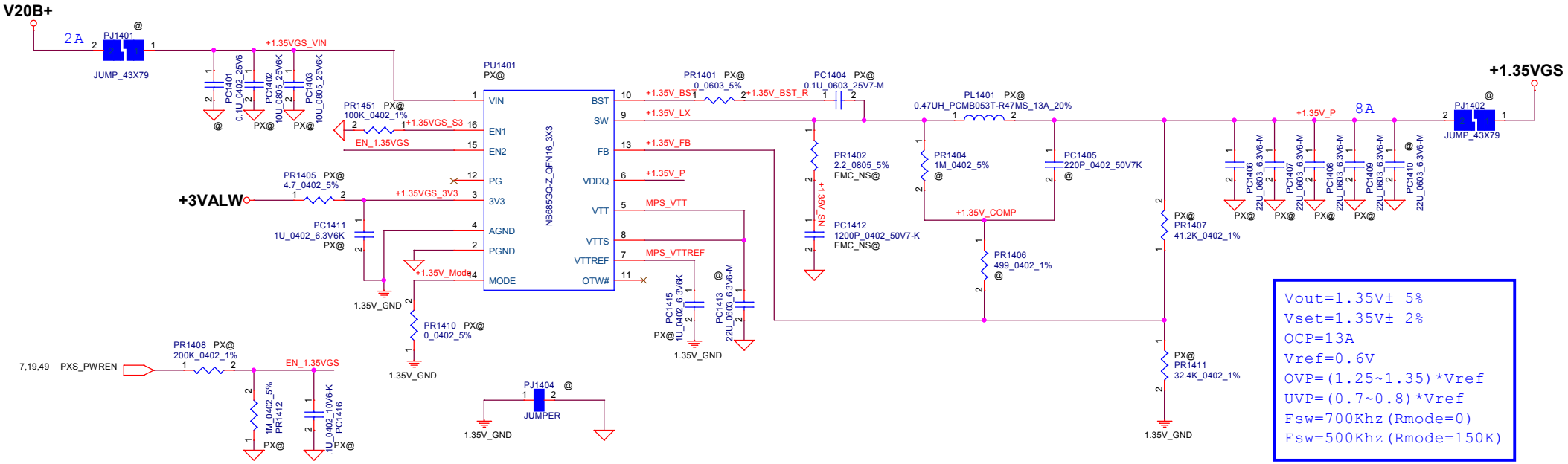
Title	System PMIC		
Size	Document Number		Rev
A2	320ABR		0.2
Date:	Saturday, February 04, 2017	Sheet	47 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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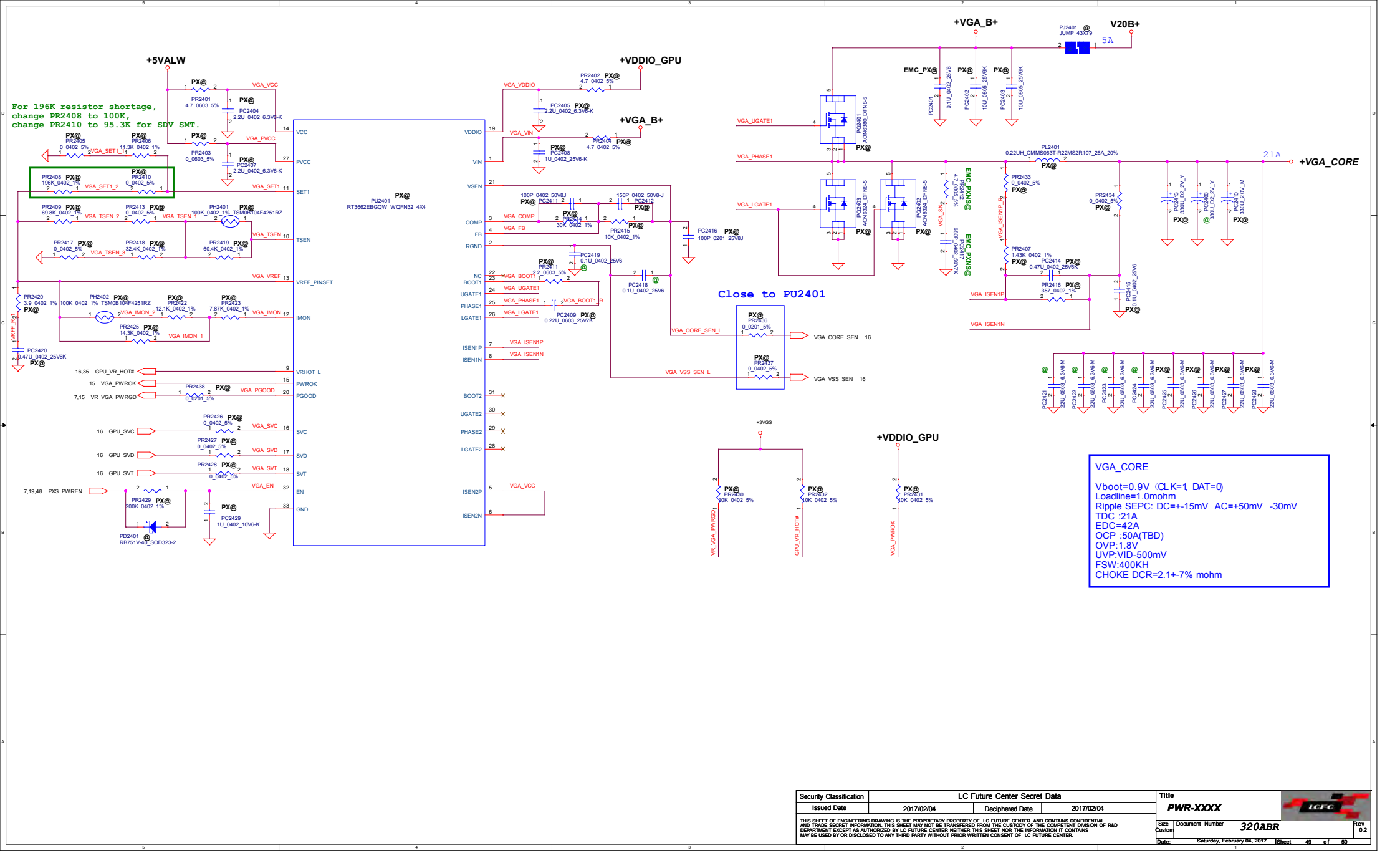
Title: *1.35VGS*

Size	Document Number	Rev
A3	*320ABR*	0.2

Date: Saturday, February 04, 2017 Sheet 48 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2017/02/04	Deciphered Date	2017/02/04

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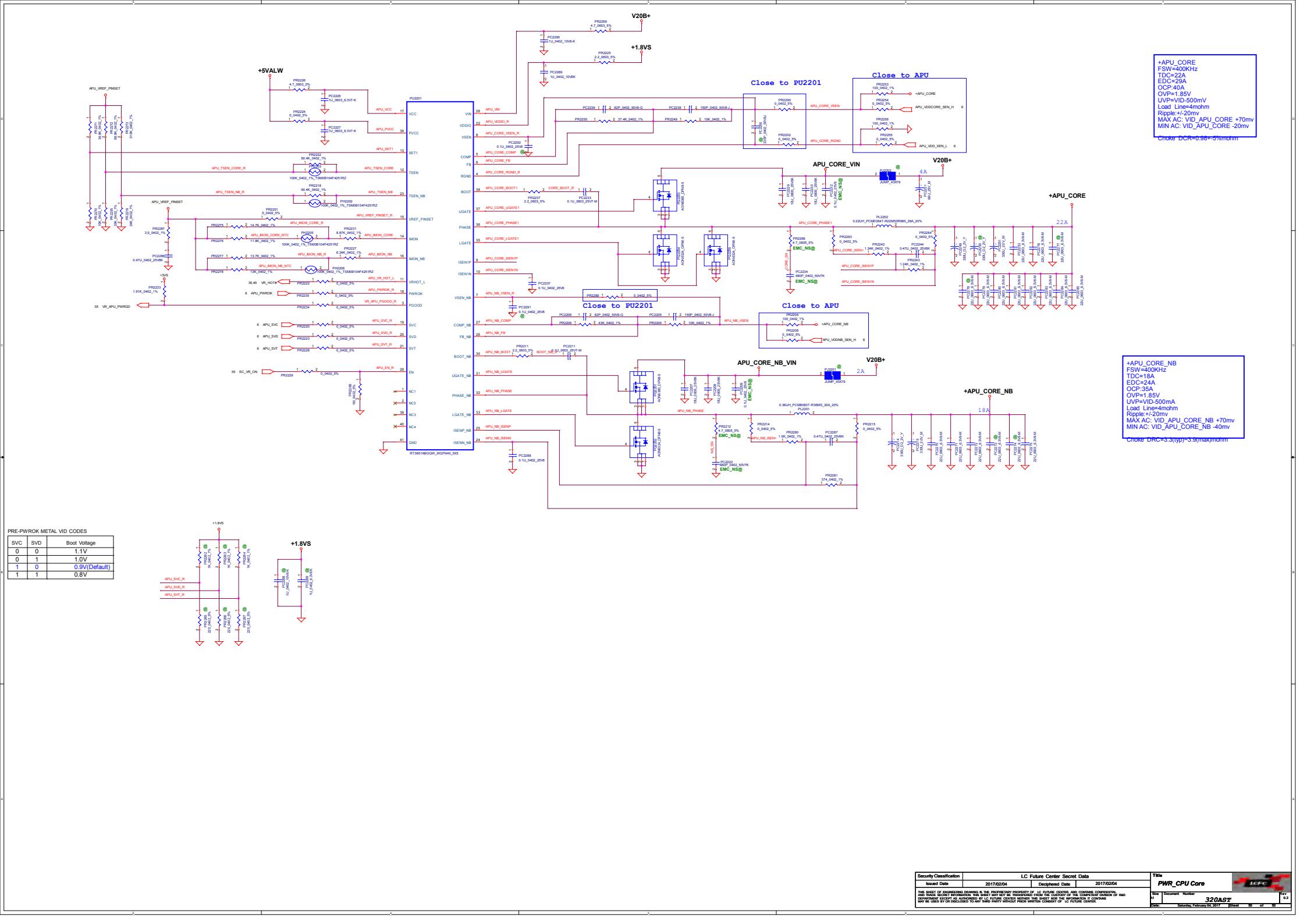
Title: PWR-XXXX

Size	Document Number	Rev
Custom	320ABR	0.2

Date: Saturday, February 04, 2017 Sheet 49 of 50


+APU_CORE
FSW=400KHz
TDC=22A
EDC=29A
OCP:40A
OVP=1.85V
UVP=VID-500mV
Load Line=4mohm
Ripple:+/-20mv
MAX AC: VID_APU_CORE +70mv
MIN AC: VID_APU_CORE -20mv
Choke DCR=0.98+-5%mohm
+APU_CORE_NB
FSW=400KHz
TDC=18A
EDC=24A
OCP:35A
OVP=1.85V
UVP=VID-500mA
Load Line=4mohm
Ripple:+/-20mv
MAX AC: VID_APU_CORE_NB +70mv
MIN AC: VID_APU_CORE_NB -40mv
Choke DRC=3.3(typ)~3.9(max)mohm
Close to PU2201
Close to APU
APU_CORE_VIN
APU_CORE_NB_VIN
+APU_CORE
+APU_CORE_NB
+5VALW
+1.8VS
V20B+
PU2201
RT3661ABGQW_WQFN40_5X5
PRE-PWROK METAL VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Security Classification
LC Future Center Secret Data
Issued Date 2017/02/04
Deciphered Date 2017/02/04
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Title
PWR_CPU Core
Size A1
Document Number
320AST
Rev 0.2
Date: Saturday, February 04, 2017
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