MS-1453(Switchable) & MS-1454(UMA) Ver : 0A

2009/07/07

Calpella Platform

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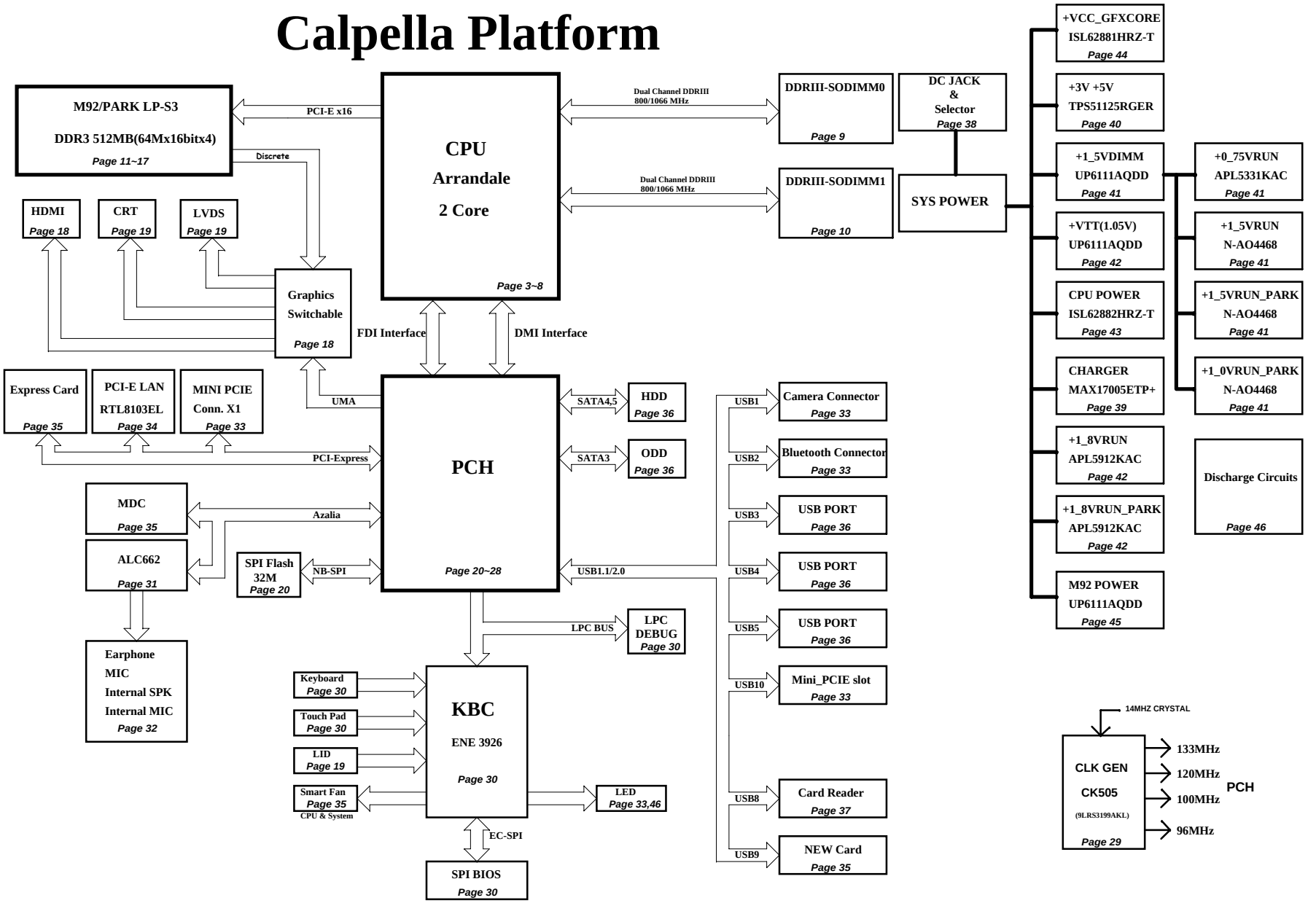

MICRO-STAR INT'L CO.,LTD.

BLOCK DIAGRAM

MS-145X

Rev 0A

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
		S0	
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

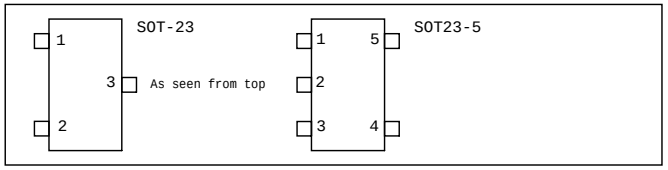
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

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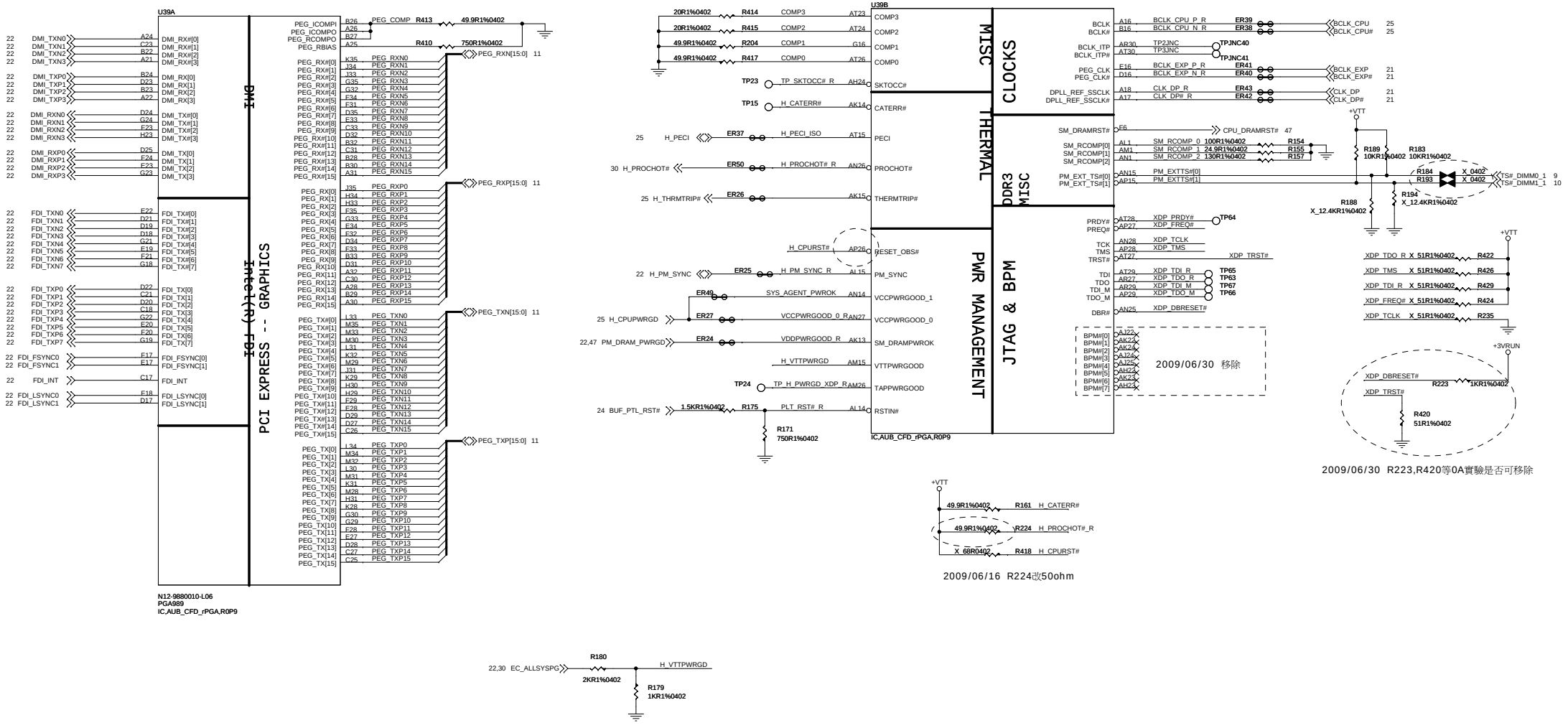
ARRANDALE PROCESSOR (CLK,MISC,JTAG)



MICRO-STAR INT'L CO.,LTD.	
Title	PROCESSOR
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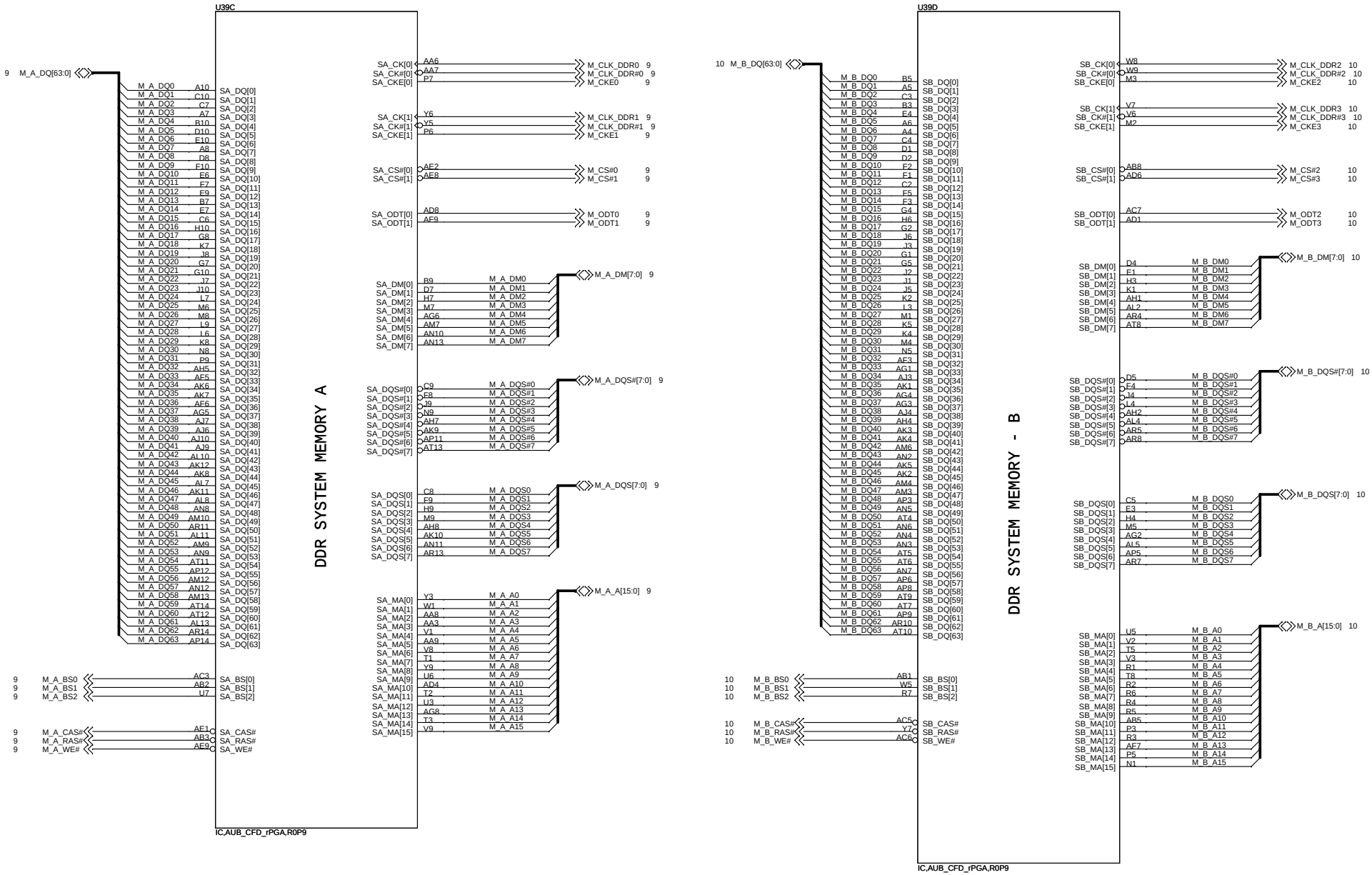
ARRANDALE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title: DDR3

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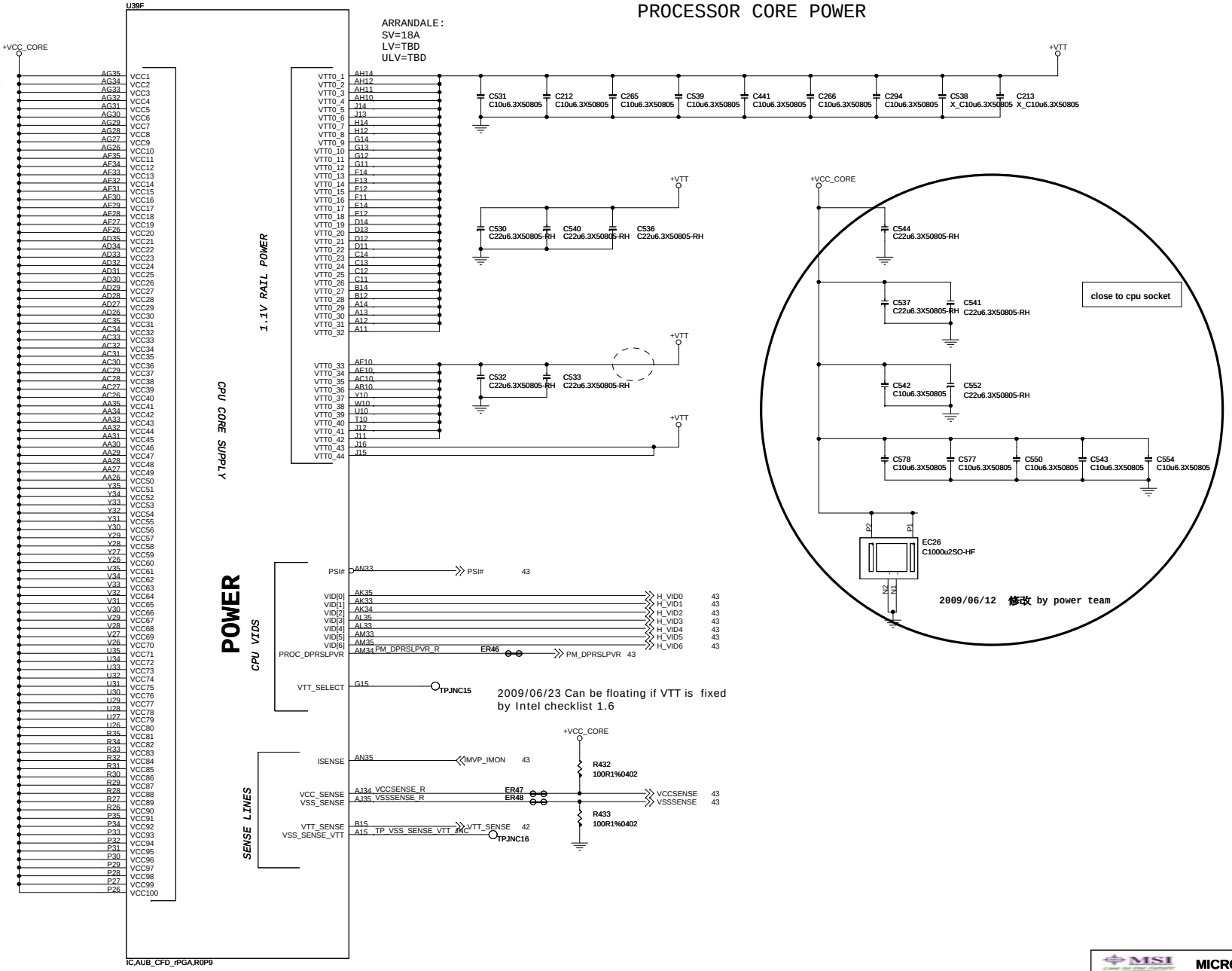
ARRANDALE PROCESSOR (POWER)

ARRANDALE:
SV=48A
LV=35A
ULV=27A

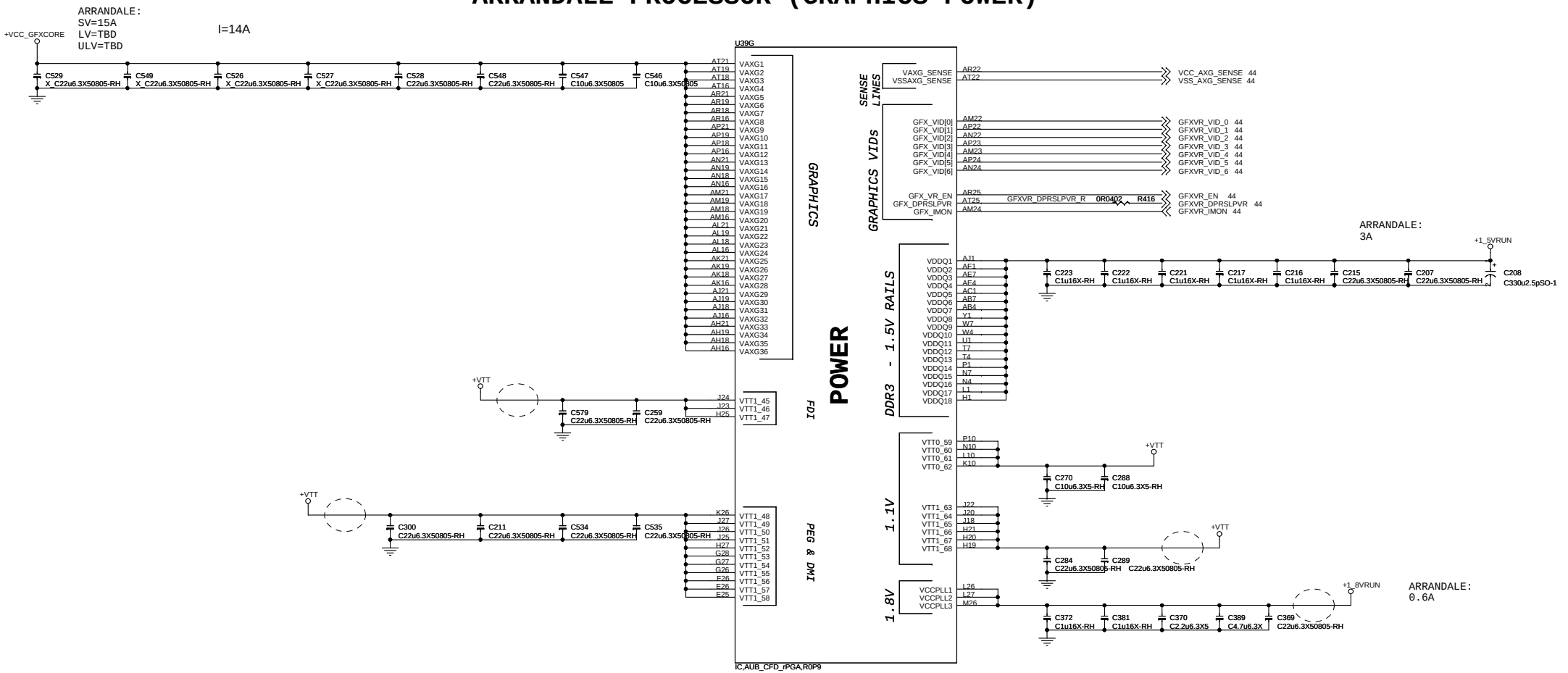
PROCESSOR CORE POWER

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER



ARRANDALE PROCESSOR (GRAPHICS POWER)



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	GRAPHICS POWER	
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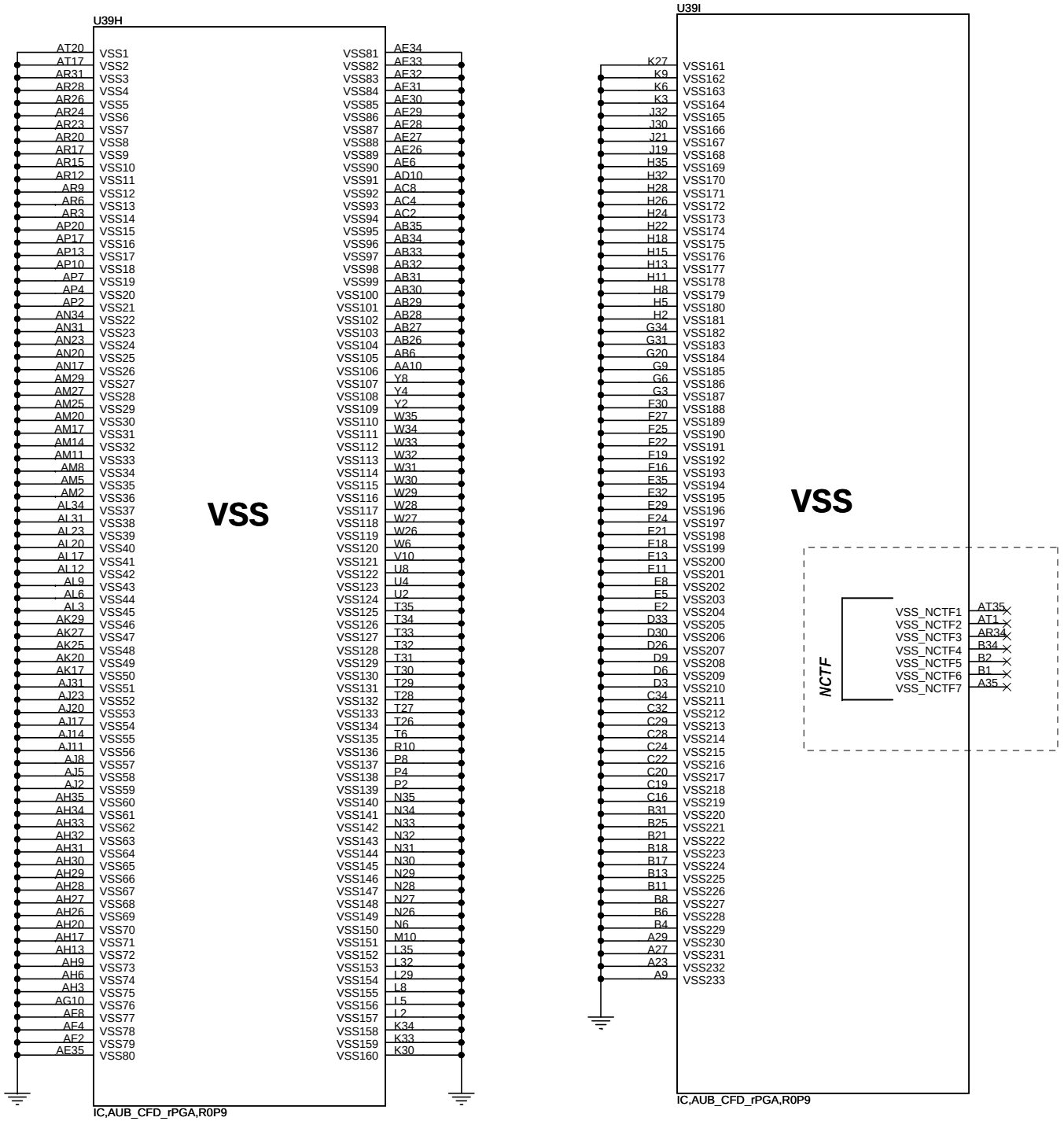
ARRANDALE PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR GND

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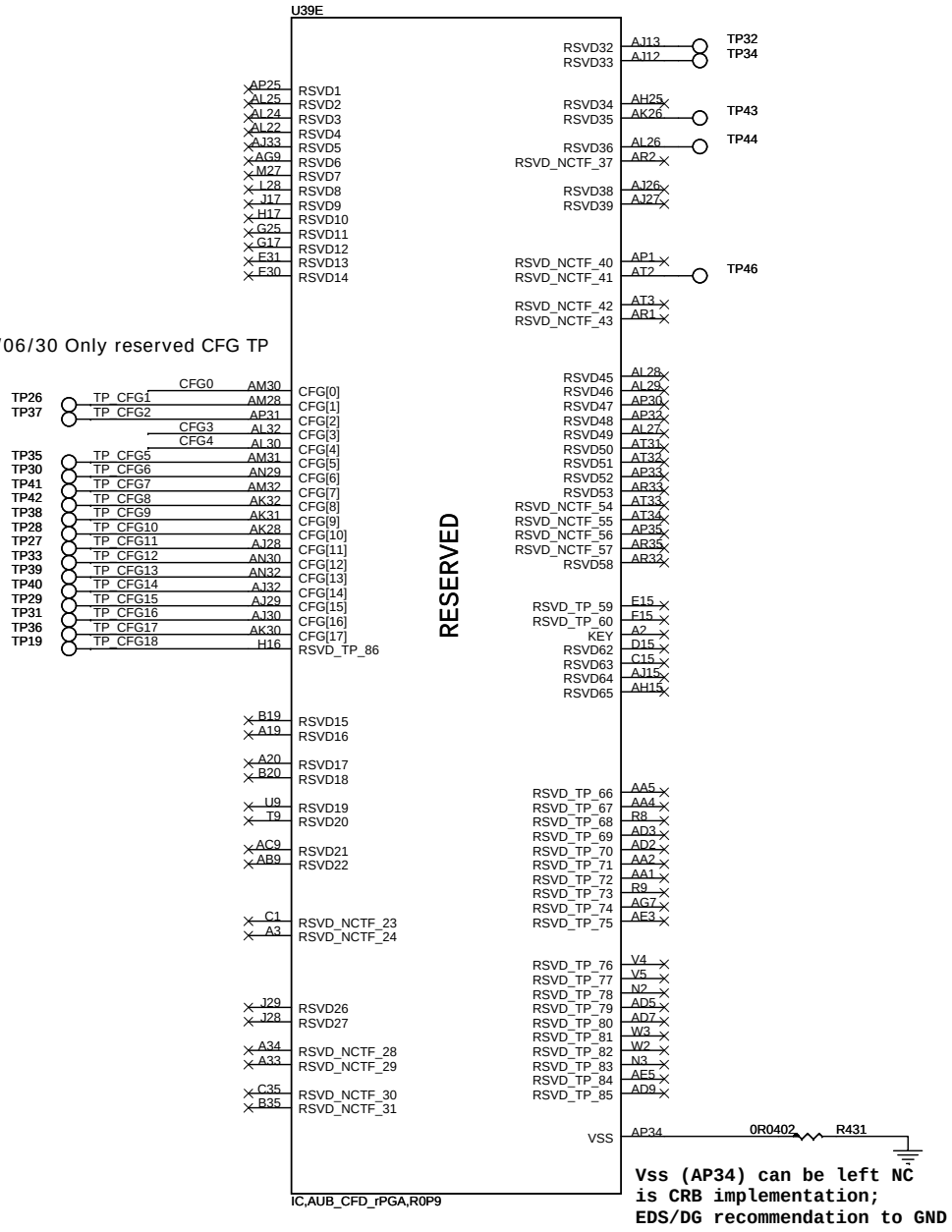
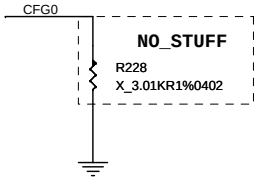
ARRANDALE PROCESSOR (RESERVED)

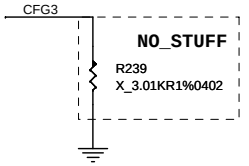


Vss (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

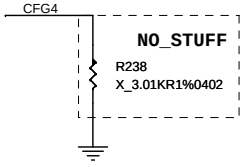
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR RESERVED

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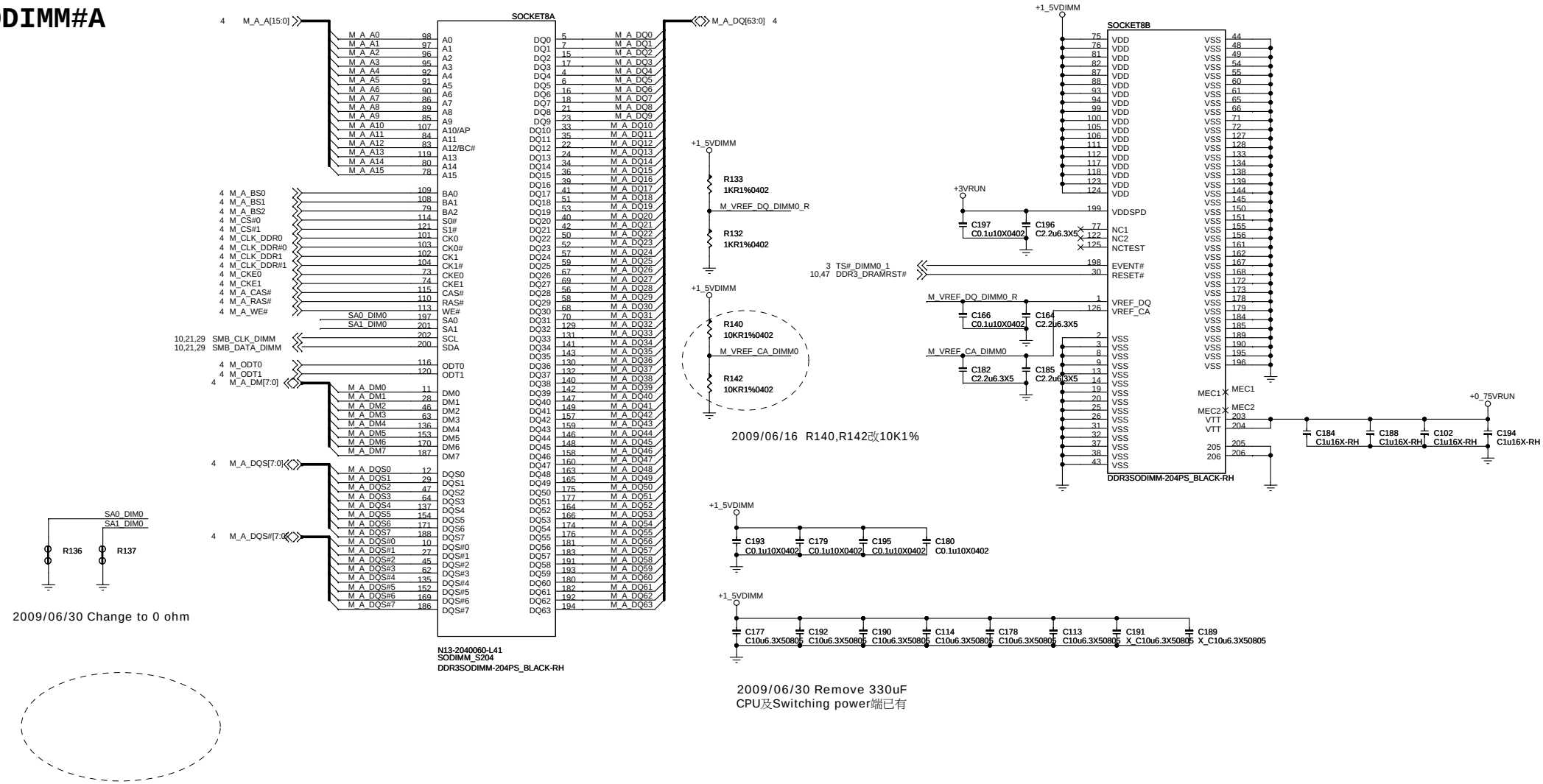
SODIMM#A



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Title	DDR3 SODIMM0	
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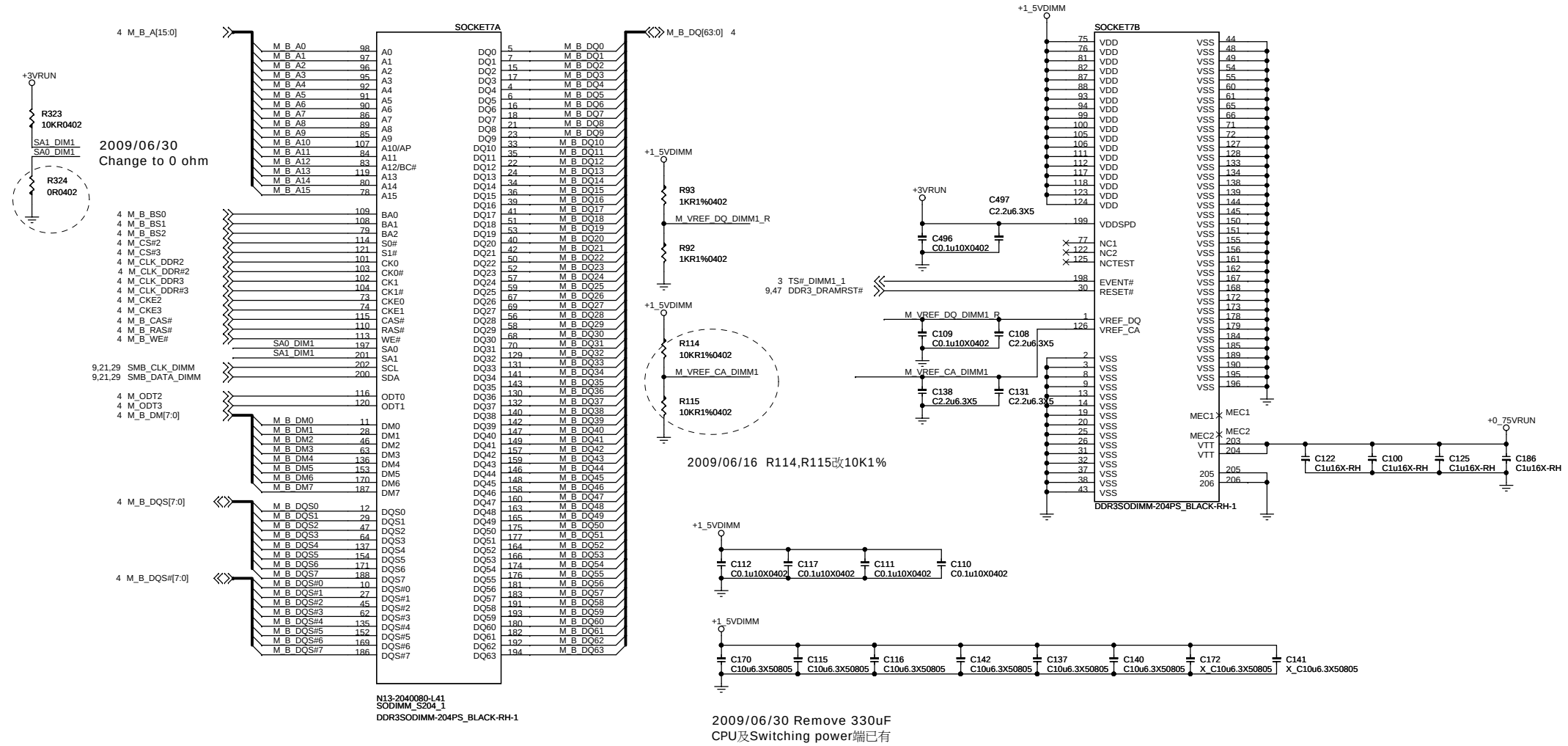
SODIMM#B



Title	DDR3 SODIMM1
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MICRO-STAR INT'L CO.,LTD.

2009/06/30 靠近CPU(TX)

CheckResetSequence

For Park-S3: PWRGOOD pin must need to pull low

For M92-S2/S3: PWRGOOD pin should be NC

	M92-S2	PARK-S3
R215	X	-

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (PCIE_Interface)

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	M92-S2	PARK-S3
R210	X	-
R195	X	-
R208	X	-
C659	X	-
C658	X	-
C512	X	-
C662	X	-
C661	X	-
C660	X	-
R197	X	-
R356	X	-
C665	X	-
C664	X	-
C663	X	-
R406	X	-
R404	X	-
R402	X	-

For Park-S3: Install All components in this Box INCLUDING Decoupling caps and Bead connecting to DPC_VDD18#

For M92-S2: DO NOT Install any Component in this Box.

For M92-S2: Use 0R to VDDR4
For Park-S3: DNI (NC)

	M92-S2	PARK-S3
R206	X	-

1.0 change P/N

Sequence

AVSSQ have to be away from noisy ground
A2VSSQ have to be away from noisy ground
it is for layout recommendation

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

ATI suggestion

2009/07/09 Default use clock GEN. 27MHz(SS)

Note:1
For M9x-S2/S3 XO_IN and XO_IN2 Pins are NC, can be gronded

For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.

OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

Check 1.8VRUN and VDDR3 Sequence
For Park-S3 : Stuff R443
For M92-S2 : Stuff R451

LVDS Interface

216-0728020-00-A12-RH

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (Main IO)

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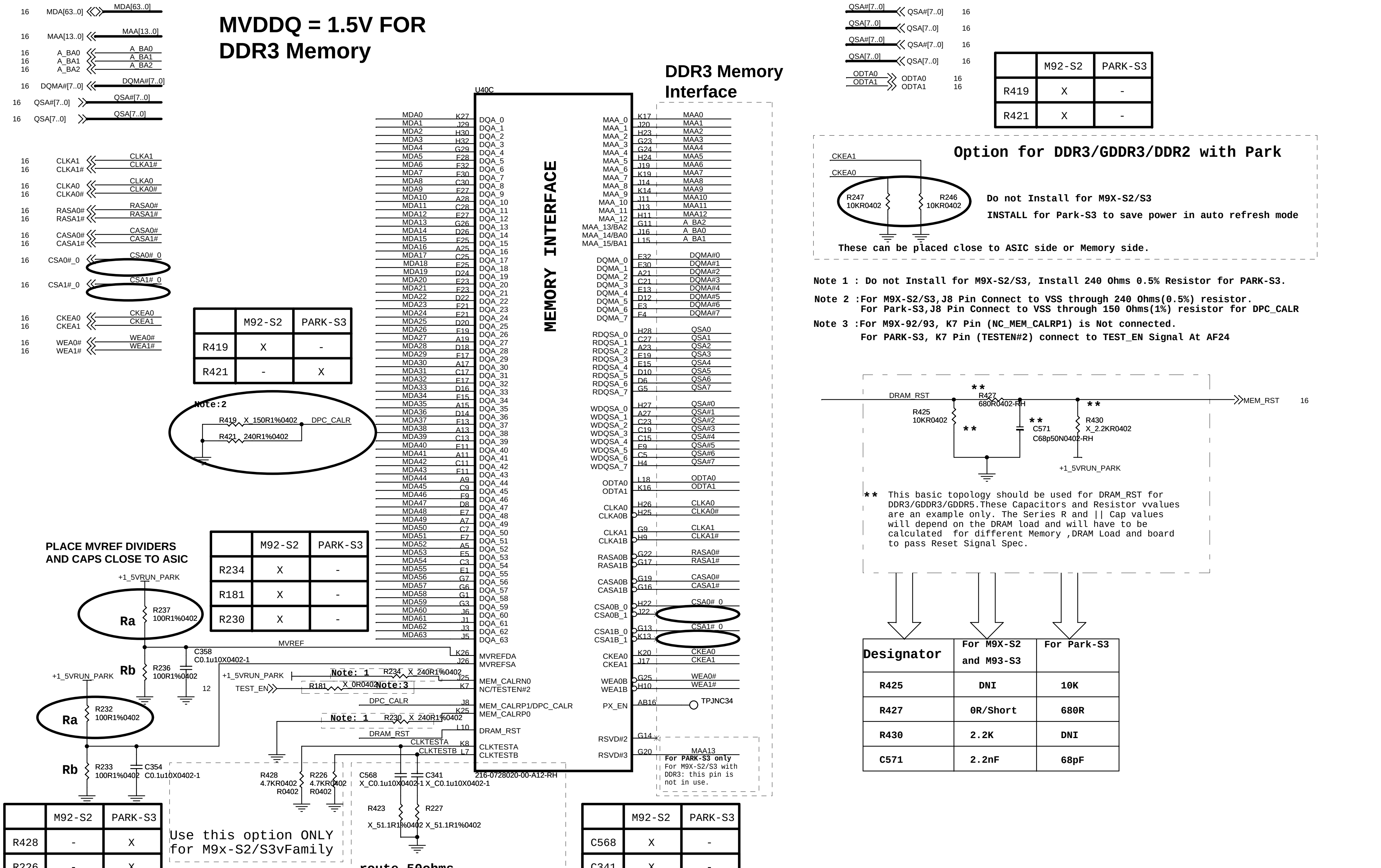
MVDDQ = 1.5V FOR DDR3 Memory

DDR3 Memory Interface



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

	M92-S2	PARK-S3
R419	X	-
R421	X	-

	M92-S2	PARK-S3
R419	X	-
R421	-	X

	M92-S2	PARK-S3
R234	X	-
R181	X	-
R230	X	-

	M92-S2	PARK-S3
R428	-	X
R226	-	X

Use this option ONLY for M9x-S2/S3vFamily

	M92-S2	PARK-S3
C568	X	-
C341	X	-
R423	X	-
R227	X	-

route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

DIVIDER RESISTORS	DDR3	GDDR3
MVREF TO 1.5V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

Option for DDR3/GDDR3/DDR2 with Park

Do not Install for M9X-S2/S3
INSTALL for Park-S3 to save power in auto refresh mode

These can be placed close to ASIC side or Memory side.

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR

Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For M9X-S2 and M93-S3	For Park-S3
R425	DNI	10K
R427	0R/Short	680R
R430	2.2K	DNI
C571	2.2nF	68pF

MICRO-STAR INT'L CO.,LTD.
Title: M92/Pak-Sx (MEM_Interface)
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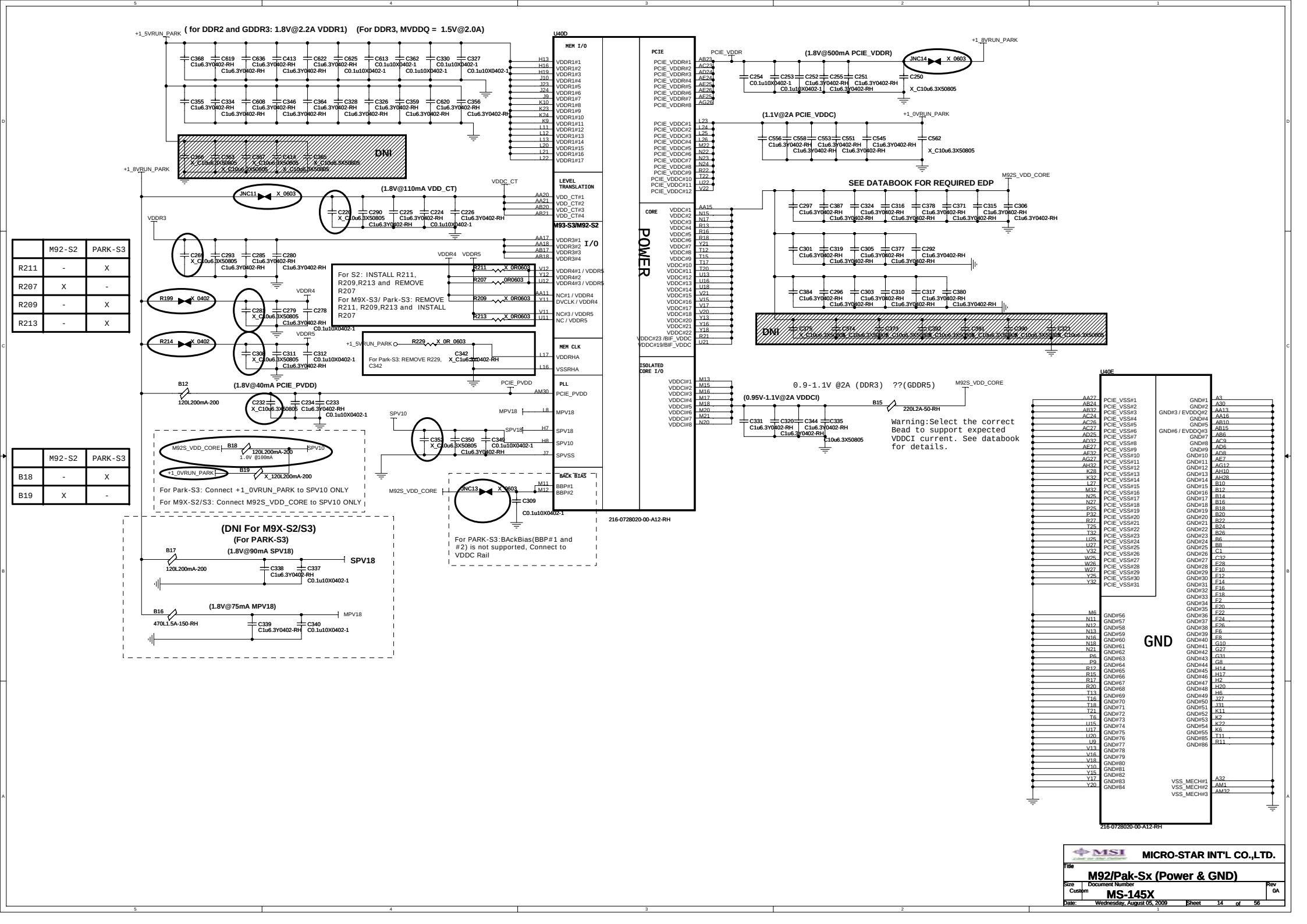
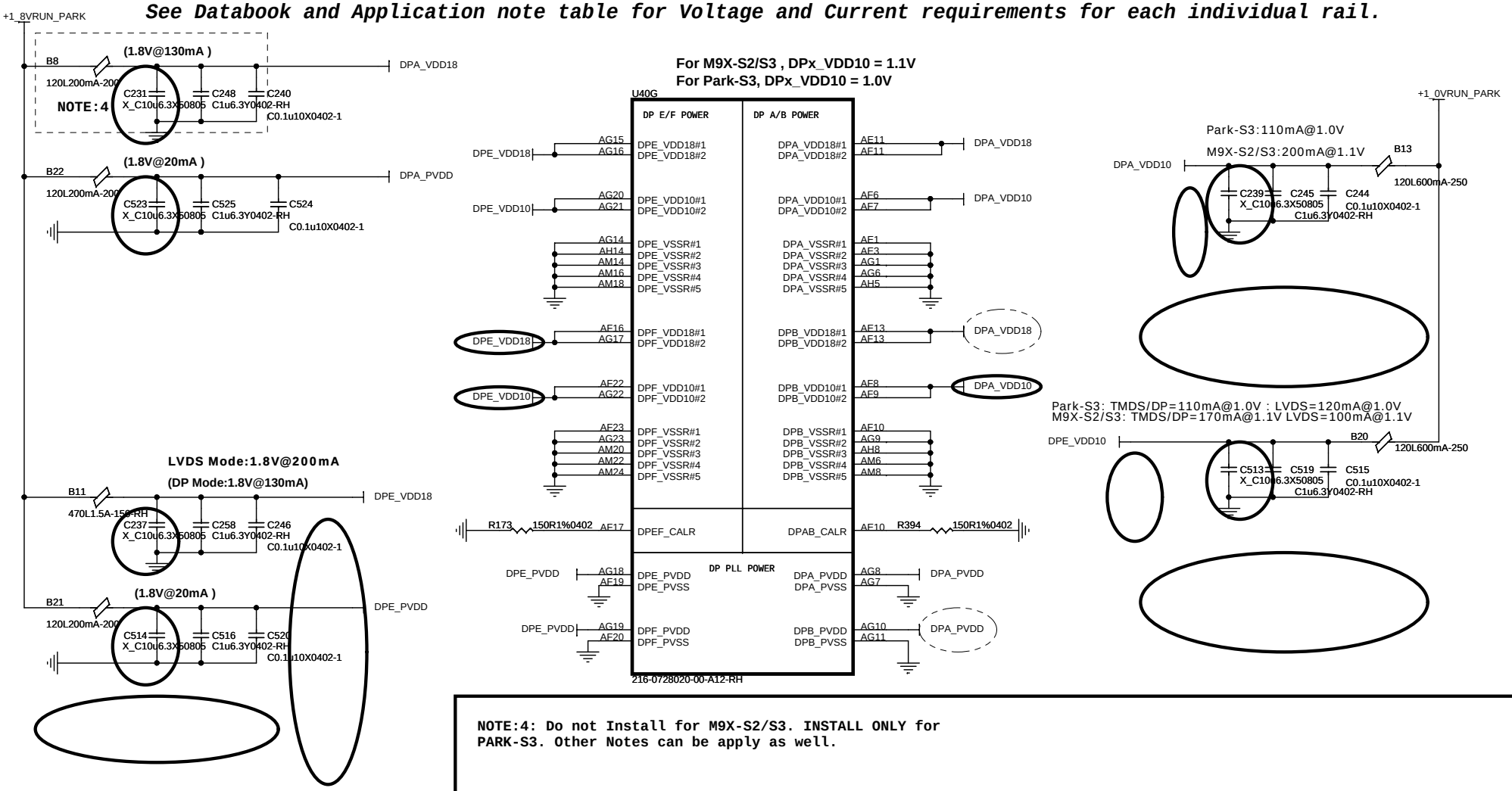


	M92-S2	PARK-S3
R211	-	X
R207	X	-
R209	-	X
R213	-	X

	M92-S2	PARK-S3
B18	-	X
B19	X	-

See Databook and Application note table for Voltage and Current requirements for each individual rail.



NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

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Title: M92/Pak-Sx (DP_Power)		
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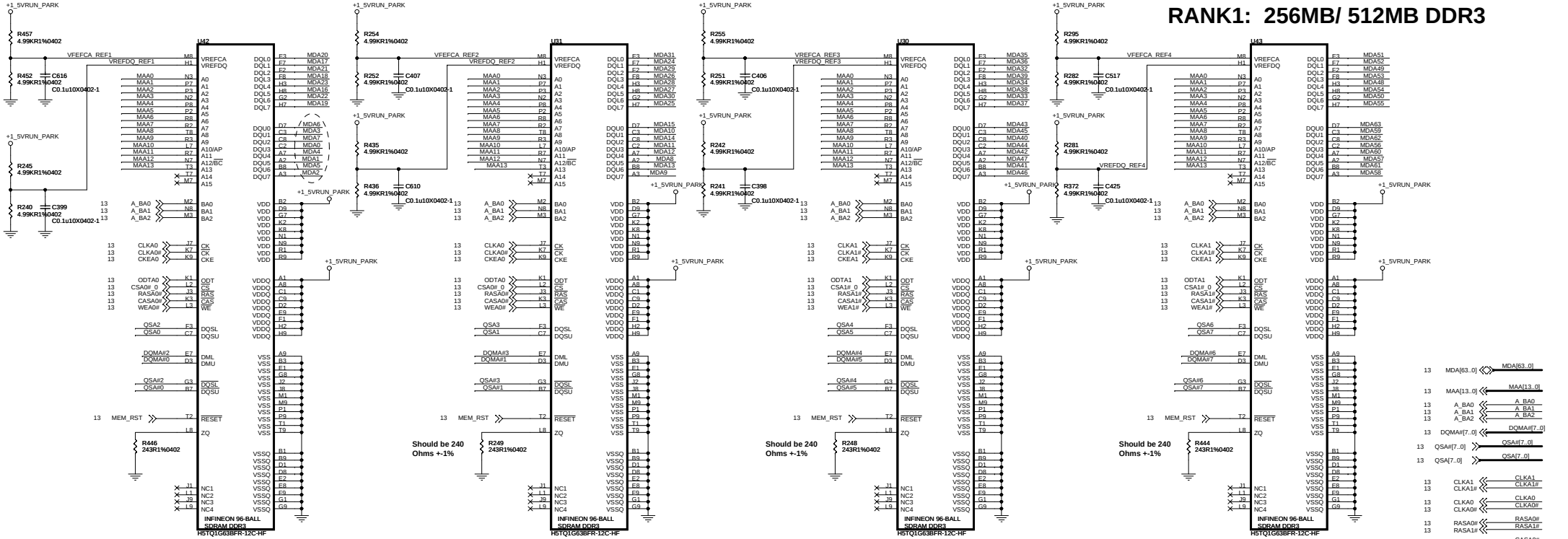
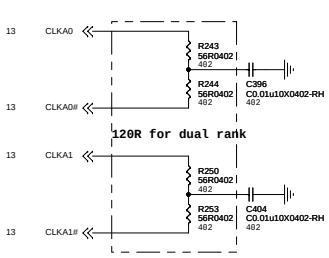
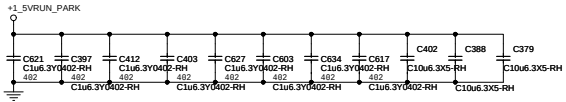
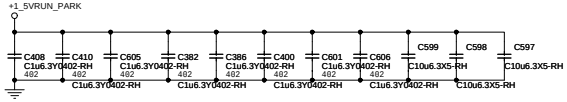
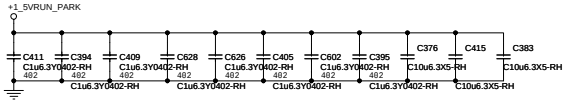
RANK1: 256MB/ 512MB DDR3

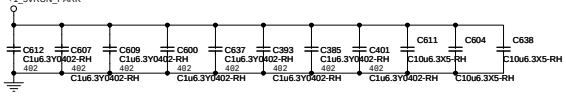


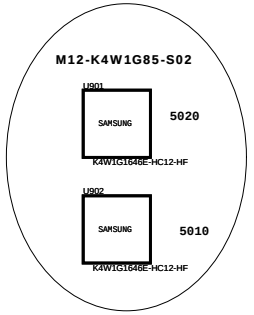












For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC

For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.

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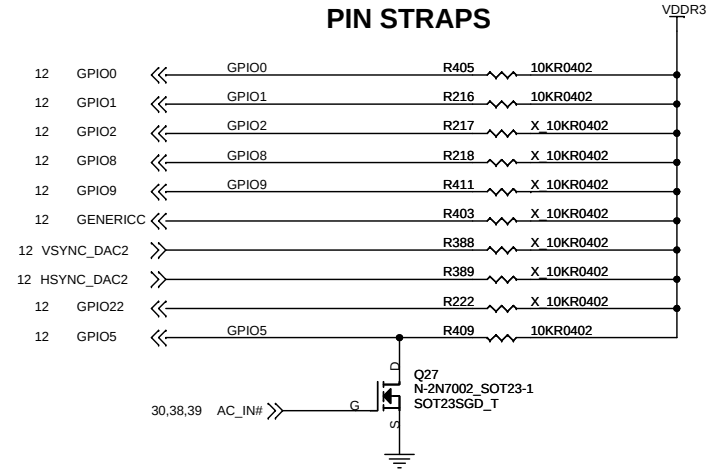
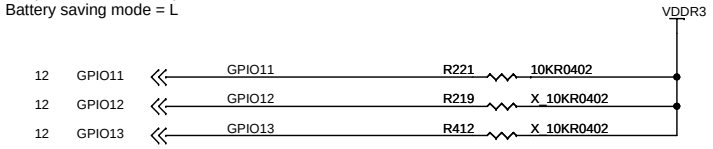
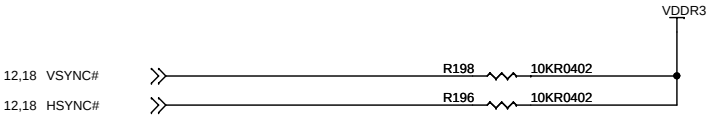
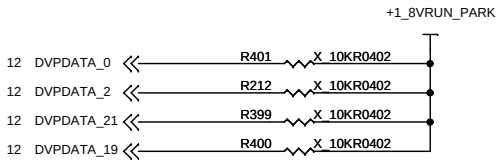
PIN STRAPS



GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L







CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIE device as 2.5 GT/S capable at power -on GPIO=1 Advertises the PCIE device as 5 GT/S capable at power -on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controler.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11			0 0 0=128 MB
	0 0 1		0 0 1=256 MB
			0 1 0=64 MB

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#			0 0=No audio function
			0 1=Audio for display port only
			1 0=Audio for display port and HDMI if dongle is detected
	1 1		1 1=Audio for both displayport and HDMI

DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	

MICRO-STAR INT'L CO.,LTD.

Title: **M92/Pak-Sx (Straps & Thermal)**

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CRT Switch

2009/07/14 Change RGB SW

Logic Input	Function
0	S2 PORT
1	S1 PORT

BR-ADJ

MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

UMA (MS-1454) USE ONLY

CRT_B_UMA	R14	X_0R0402	VGA_BLUE
CRT_G_UMA	R13	X_0R0402	VGA_GREEN
CRT_R_UMA	R11	X_0R0402	VGA_RED
CRT_HSYNC_UMA	R12	X_0R0402	VGA_HSYNC
CRT_VSYNC_UMA	R15	X_0R0402	VGA_VSYNC

X_PI3V512QE_QSOP24-RH

LVDS Switch

TS3DV520ERUAR_QFN42-RH

TS3DV520ERUAR

UMA (MS-1454) USE ONLY

LVDSA_CLK#	RN4	X_8P4R-0R0402	LVDSA_CLK_N1
LVDSA_CLK			LVDSA_CLK_P1
LVDSA_DATA0#			LVDSA_D_N0
LVDSA_DATA0			LVDSA_D_P0
LVDSA_DATA1#	RN5	X_8P4R-0R0402	LVDSA_D_N1
LVDSA_DATA1			LVDSA_D_P1
LVDSA_DATA2#			LVDSA_D_N2
LVDSA_DATA2			LVDSA_D_P2
LVDS_VDD_EN	R71	X_0R0402	LVDS_VDDEN
L_BKLT_EN	R359	X_0R0402	BLON

EDID Switch (CRT,LVDS)

NC7SB3157P6X_SOT323-6

LVDS EDID

UMA I2C Pull high to +3VRUN by 2.2K

MXM I2C Pull high to VDDR3 by 10K

RGB EDID

UMA I2C Pull high to +3VRUN by 2.2K

MXM I2C Pull high to VDDR3 by 10K

2009/07/14 DEL HDMI I2C SW (U26,U27)

R58 UMA (MS-1454) USE ONLY

Logic Input	Function
0	PORT 1
1	PORT 2

UMA (MS-1454) USE ONLY

LVDS_DDC_CLK	R84	X_0R0402	LVDS_CLK
LVDS_DDC_DATA	R82	X_0R0402	LVDS_DATA
CRT_DATA_UMA	R265	X_0R0402	RGB_DATA
CRT_CLK_UMA	R266	X_0R0402	RGB_CLK

2009/07/14 DEL HDMI I2C RES (R372,R374)

HDMI Switch

2009/07/14 Change HDMI SW

Logic Input	Function
0	B PORT
1	A PORT

2009/07/02 R167,R168 改爲49.9K ohm

2009/07/14 R167,R168,Q20,Q21 not stuff for MS-1454

R160,R169 stuff for MS-1454

2009/06/22 Modify HDMI conn PN by ME

2009/07/09 Add C657

X_PI3HDMI201ZFE_TQFN56-RH

I94-3H2010C-P23

CLOSE TO U2030

CLOSE TO CONNECTOR

Title	SWITCH&HDMI
Size	Custom
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Date:	Wednesday, August 05, 2009
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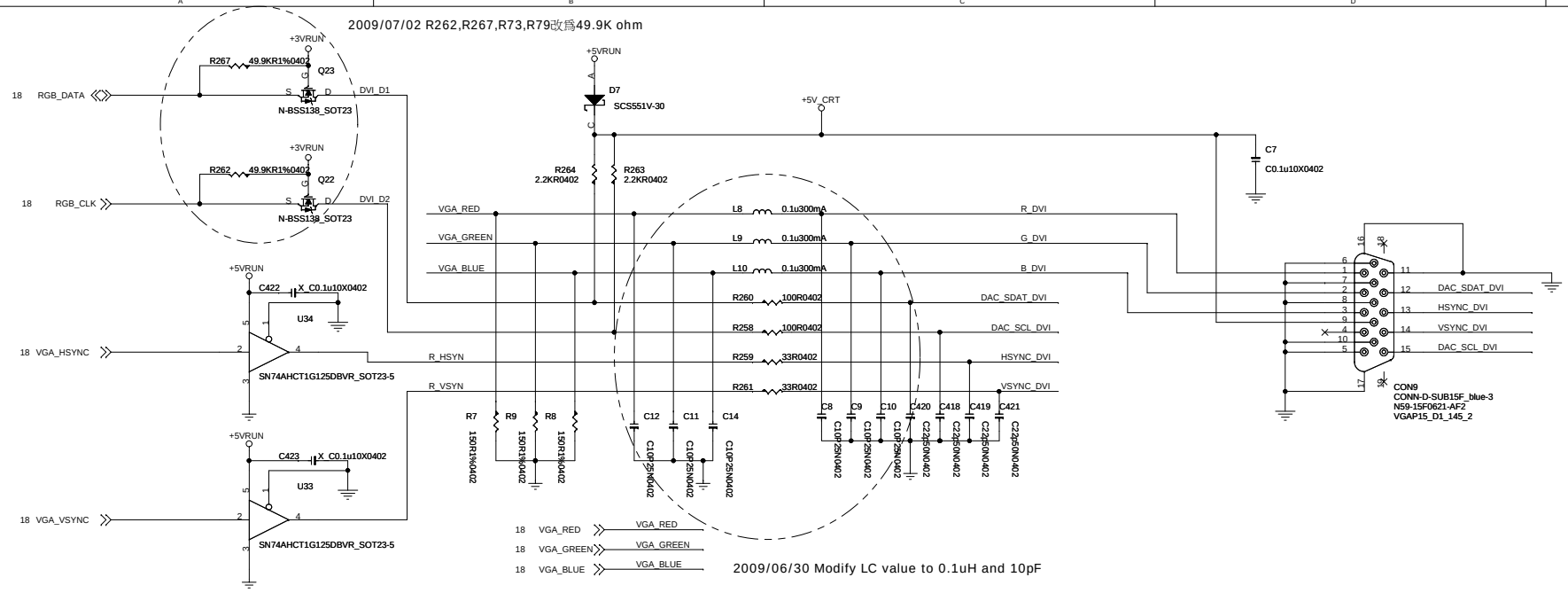
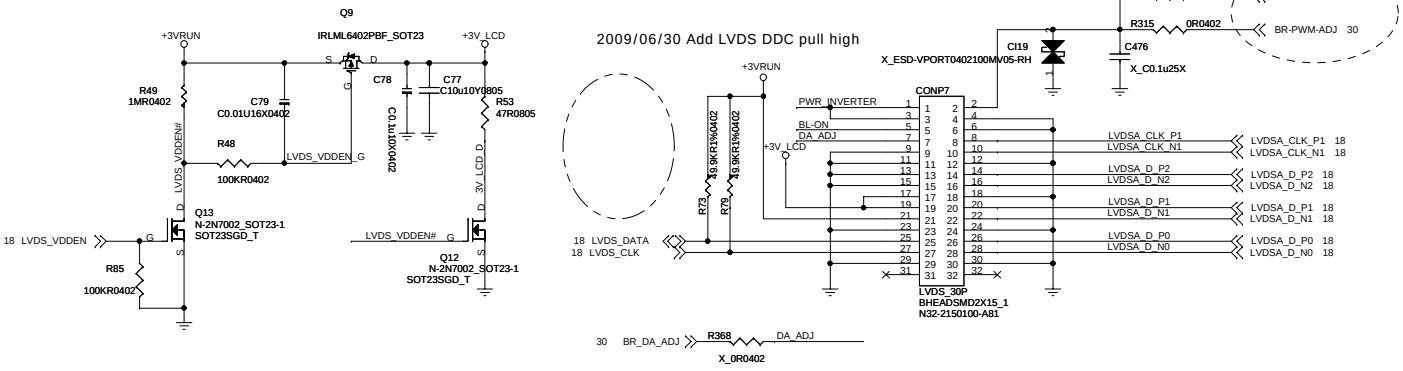
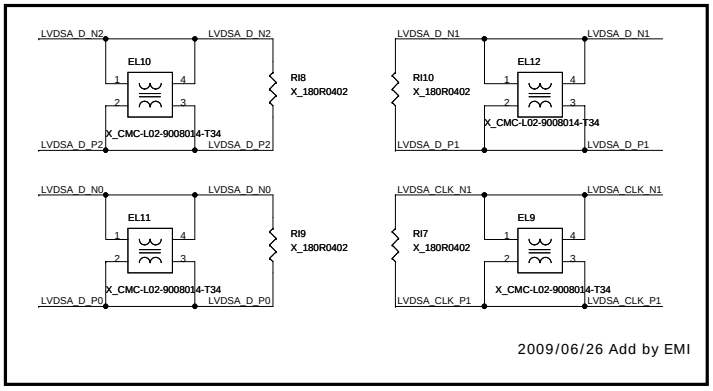
MICRO-STAR INT'L CO.,LTD.

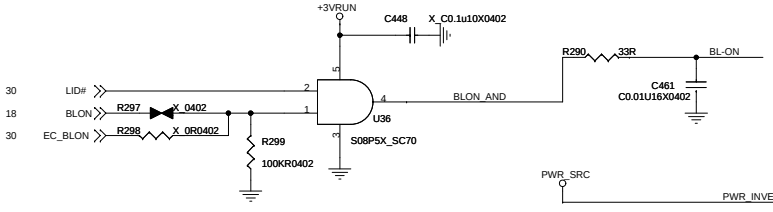
2009/07/02 R262,R267,R73,R79改爲49.9K ohm

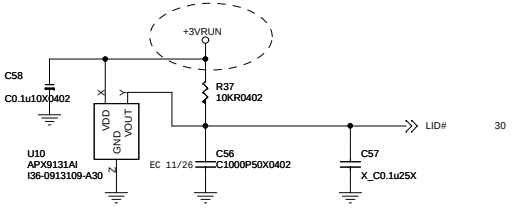


2009/07/07 Remove EMI diode for switch placement









MICRO-STAR INT'L CO.,LTD.			
Title: CRT & LVDS			
Size: Custom	Document Number: MS-145X		Rev: 0A
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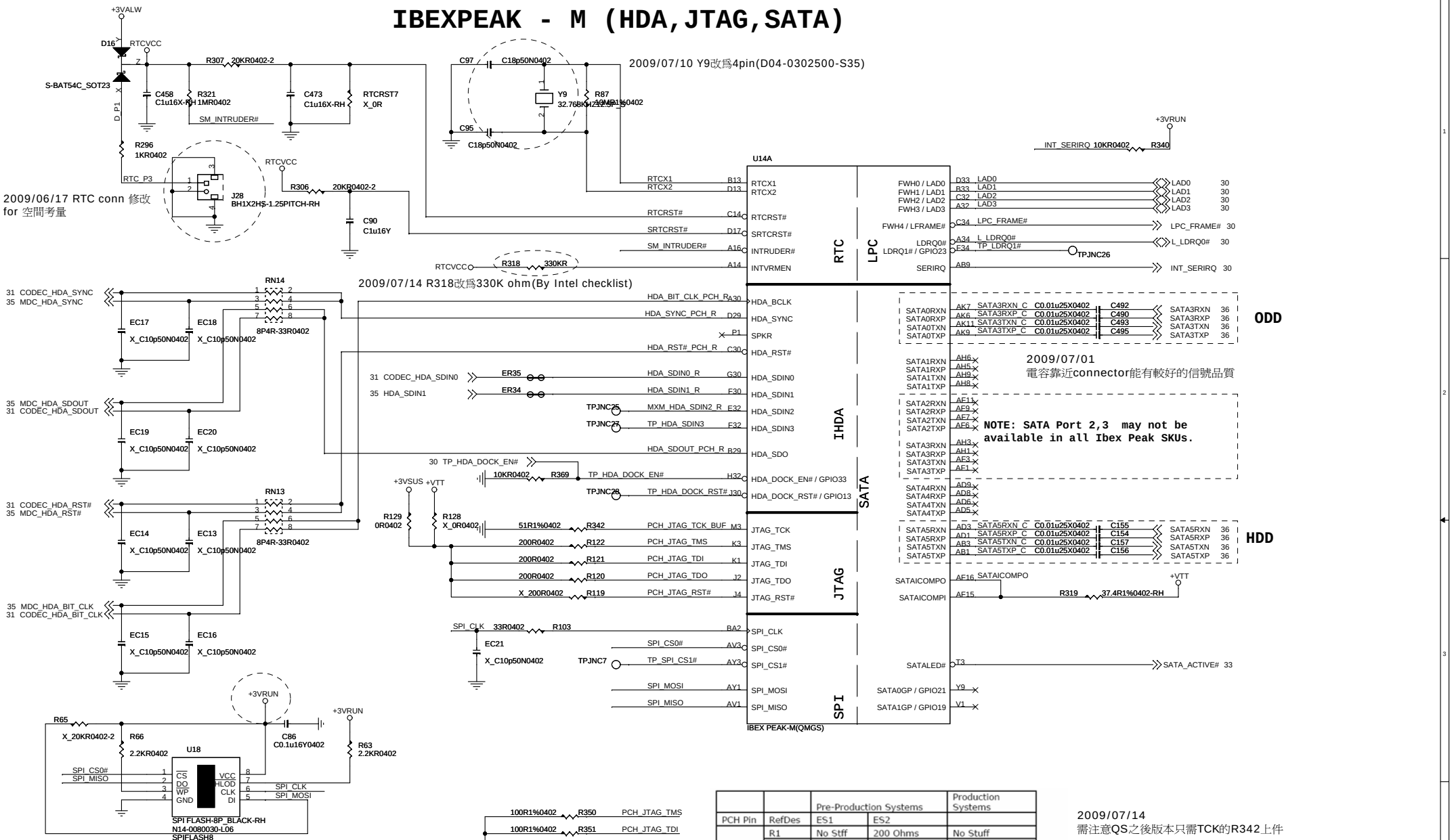
IBEXPEAK - M (HDA,JTAG,SATA)



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

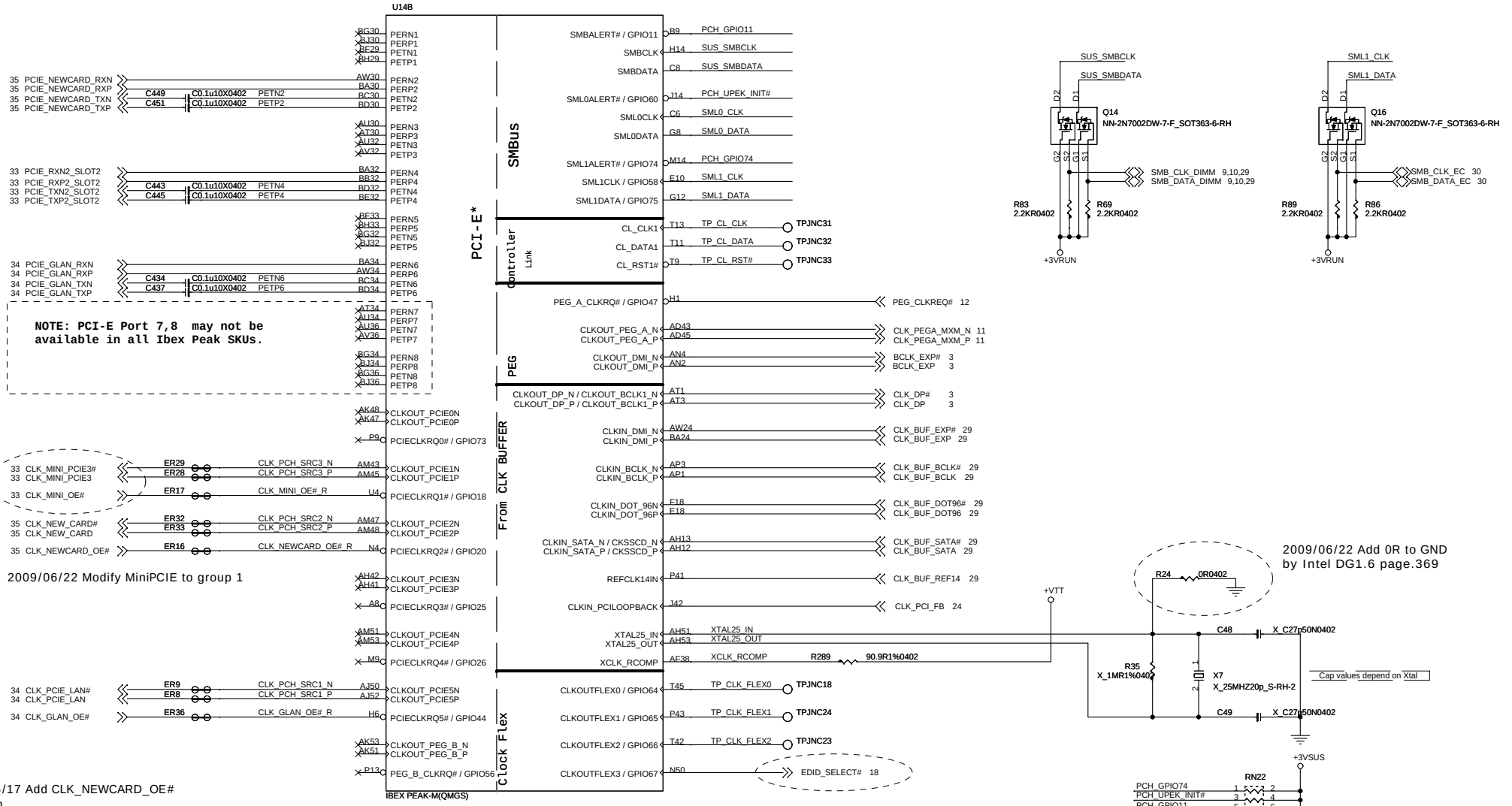
MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (HDA,JTAG,SATA)

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 20 of 56

IBEXPEAK - M (PCI-E,SMBUS,CLK)



Title	IBEXPEAK - M (PCI-E,SMBUS,CLK)
Size	Custom
Document Number	MS-145X
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Date:	Wednesday, August 05, 2009
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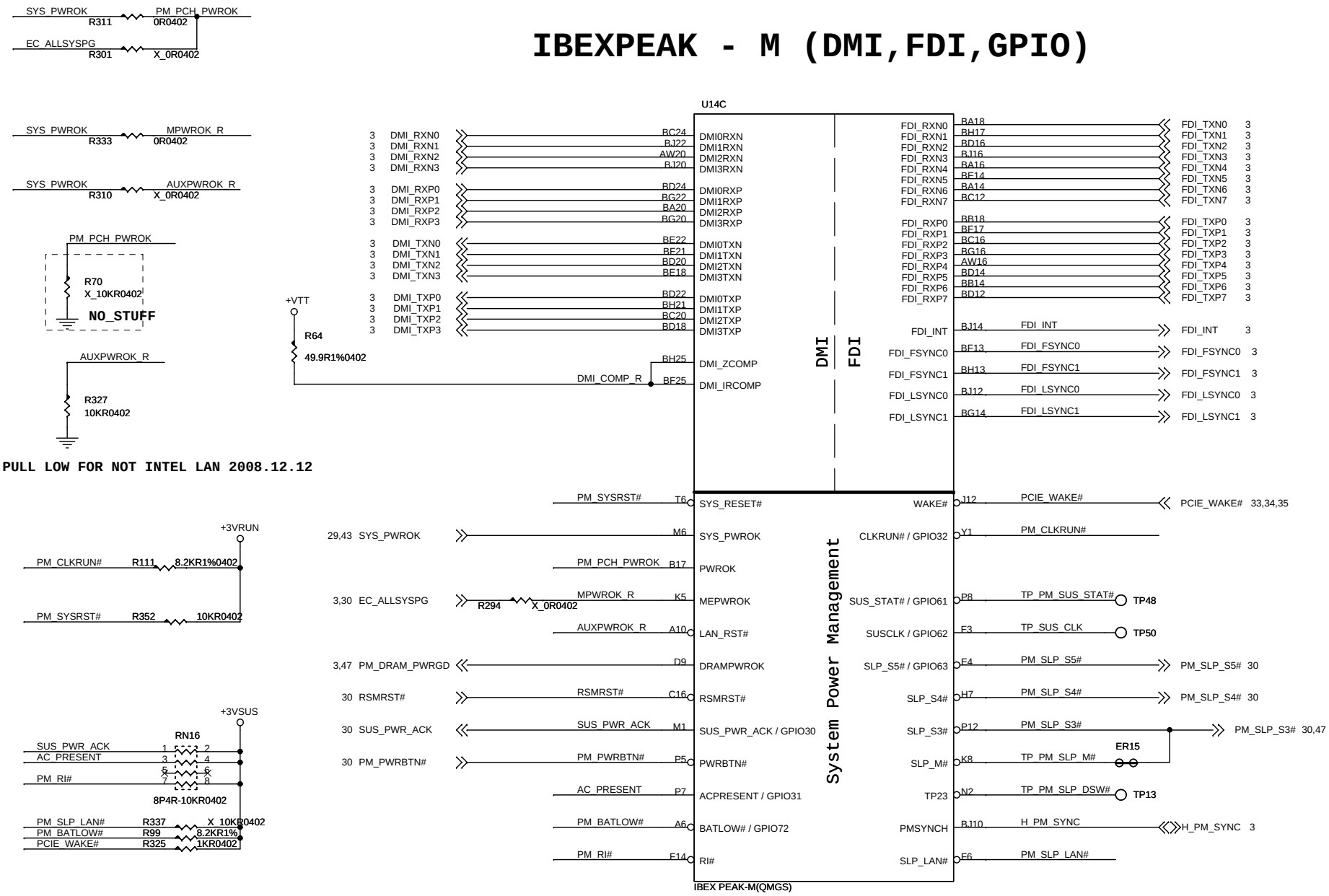
MICRO-STAR INT'L CO.,LTD.

IBEXPEAK - M (DMI,FDI,GPIO)



MICRO-STAR INT'L CO.,LTD.	
Title	IBEXPEAK - M (DMI,FDI,GPIO)
Size: Custom	Document Number: MS-145X
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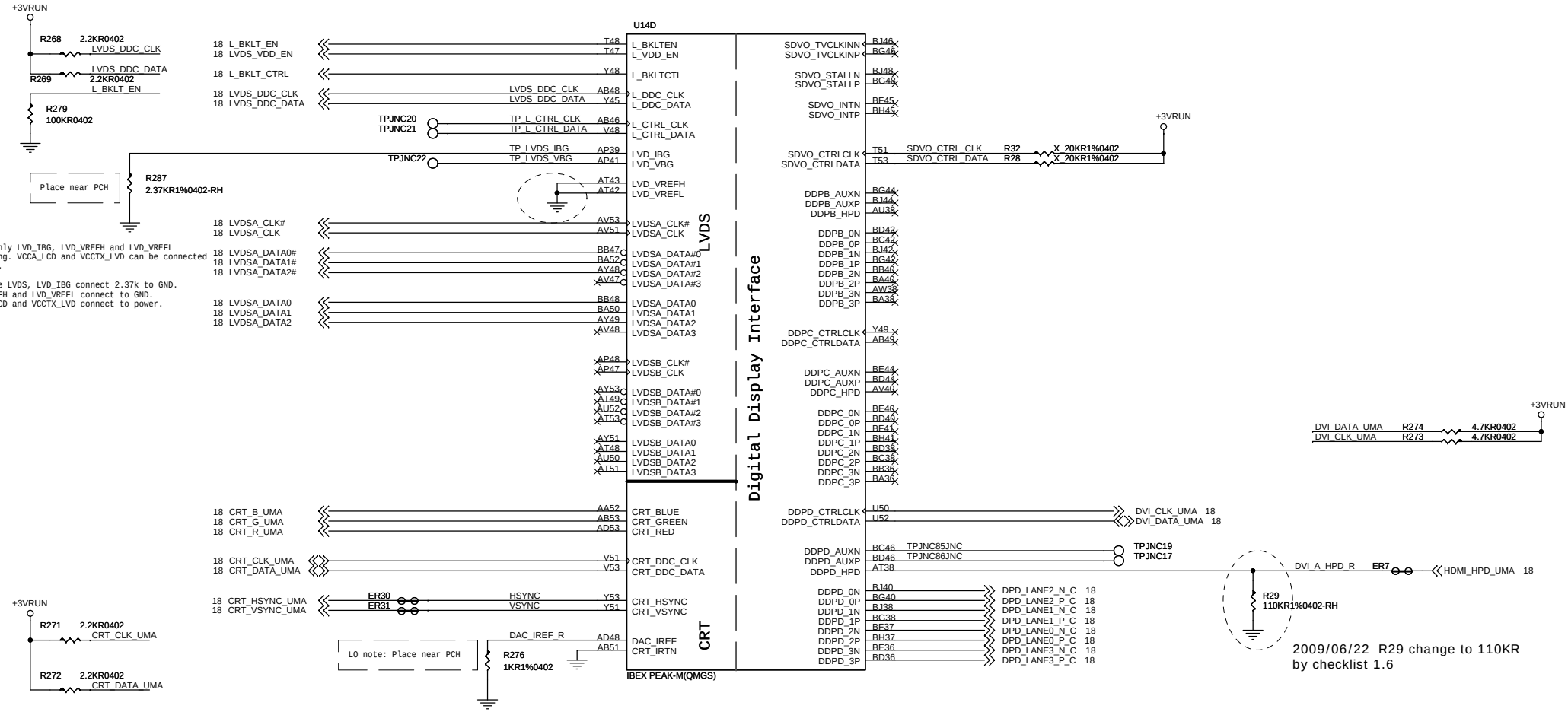
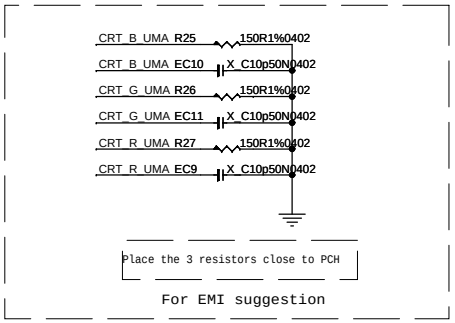
IBEXPEAK - M (LVDS,DDI)



2009/06/22 R29 change to 110KR by checklist 1.6



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (LVDS,DDI)

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IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

2009/06/26 For DGPU_SELECT# driving reserved
(No need for MS-1454)
R367 not stuff for MS-1454

PCI_GNT#0
PCI_GNT#1
R280 X_1KR0402
R277 X_1KR0402
PCI_GNT#3
DGPU_PWM_SELECT#
R275 X_1KR0402
R291 X_1KR0402
R367 0R0402
+3VRUN
R31 X_10KR0402
R36 X_10KR0402
18 DGPU_SELECT#
Q7 X_NN-2N7002DW-7-F_SOT363-6-RH
18 DGPU_PWM_SELECT#
TP51 TP_PCI_PME#
21 CLK_PCI_FB
30 CLK_PCI_KBC
30 CLK_PCIF_PORT80
EC8 X_C10p50N0402
EC27 X_C10p50N0402
EC7 X_C10p50N0402

U14E

PCI: AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#–REQ3# / GPIO50–GPIO54, GNT0#–GNT3# / GPIO51–GPIO55, PIRQE#–PIRQH# / GPIO2–GPIO5, PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

NVRAM: NV_CE#0–NV_CE#3, NV_DQS0, NV_DQS1, NV_DQ0 / NV_IO0 – NV_DQ15 / NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1

USB: USBP0N/P – USBP13N/P, USBRBIAS#, USBRBIAS, OC0# / GPIO59 – OC7# / GPIO14

IBEX PEAK-M(QMGS)

R107 X_32.4R1%0402-RH
R303 22.6R1%0402
R314 10KR0402

NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.

Not stuff for MS-1454
+3VSUS
C151 C0.1u10X0402
U21 S08P5X_SC70
25 DGPU_HOLD_RST#
PCIE_RST# 11
PLT_RST#
C128 C0.1u10X0402
U19 S08P5X_SC70
RN18 8P4R-33R0402
LAN_RST# 34
LPC_RST# 30
NEWCARD_RST# 35
WLAN_RST# 33
R98 X_0402
BUF_PTL_RST# 3

+3VRUN
RN10 8P4R-8.2KR0402-1
RN9 8P4R-8.2KR0402-1
RN12 8P4R-8.2KR0402-1
RN21 8P4R-8.2KR0402-1
RN11 8P4R-8.2KR0402-1
PCI_REQ#1, PCI_FRAME#, PCI_TRDY#, INT_PIRQH#, PCI_REQ#0, INT_PIRQB#, INT_PIRQF#, PCI_REQ#3, INT_PIRQG#, INT_PIRQC#, INT_PIRQE#, PCI_STOP#, PCI_LOCK#, PCI_PERR#, PCI_DEVSEL#, INT_PIRQA#, PCI_IRDY#, PCI_SERR#, INT_PIRQD#, PCI_REQ#2
DGPU_PWM_SELECT# R288 10KR0402

MSI	MICRO-STAR INT'L CO.,LTD.
Title	IBEXPEAK - M (PCI,USB,NVRAM)
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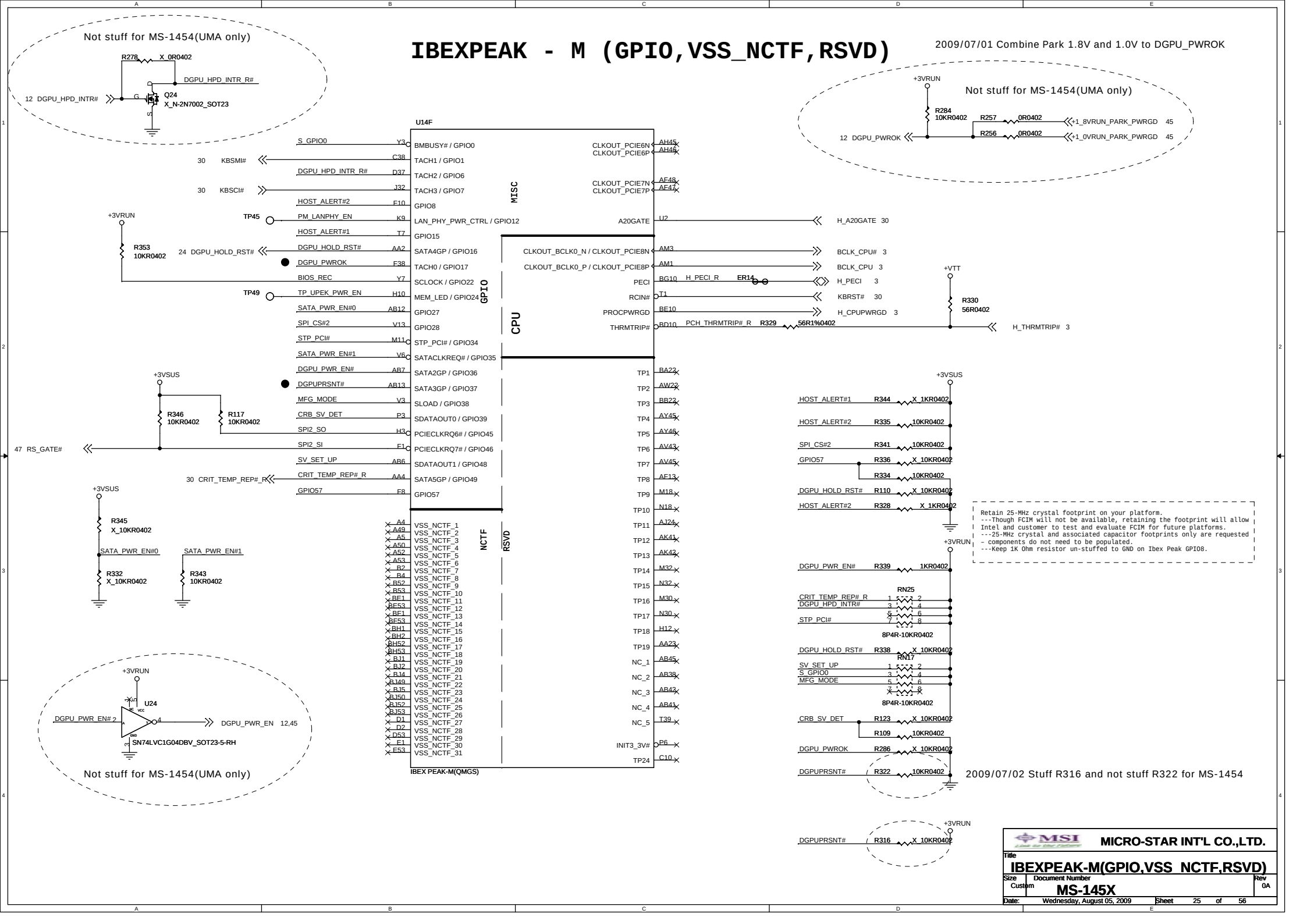
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

2009/07/01 Combine Park 1.8V and 1.0V to DGPU_PWROK



MICRO-STAR INT'L CO.,LTD.			
Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)			
Size: Custom	Document Number: MS-145X		Rev: 0A
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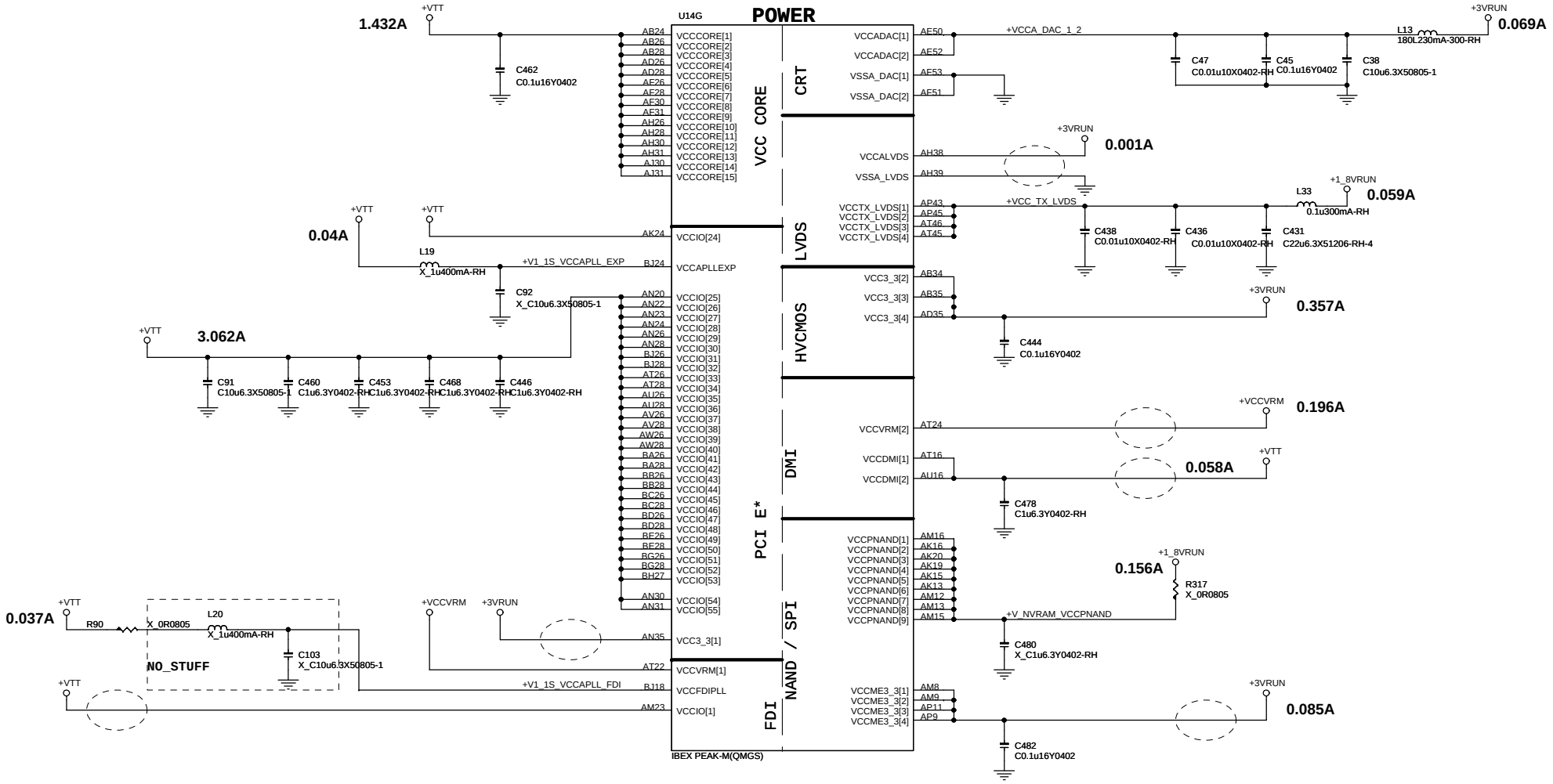
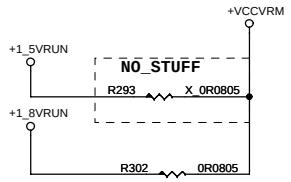
IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (POWER)	
Size: Custom	Document Number: MS-145X	Rev: 0A
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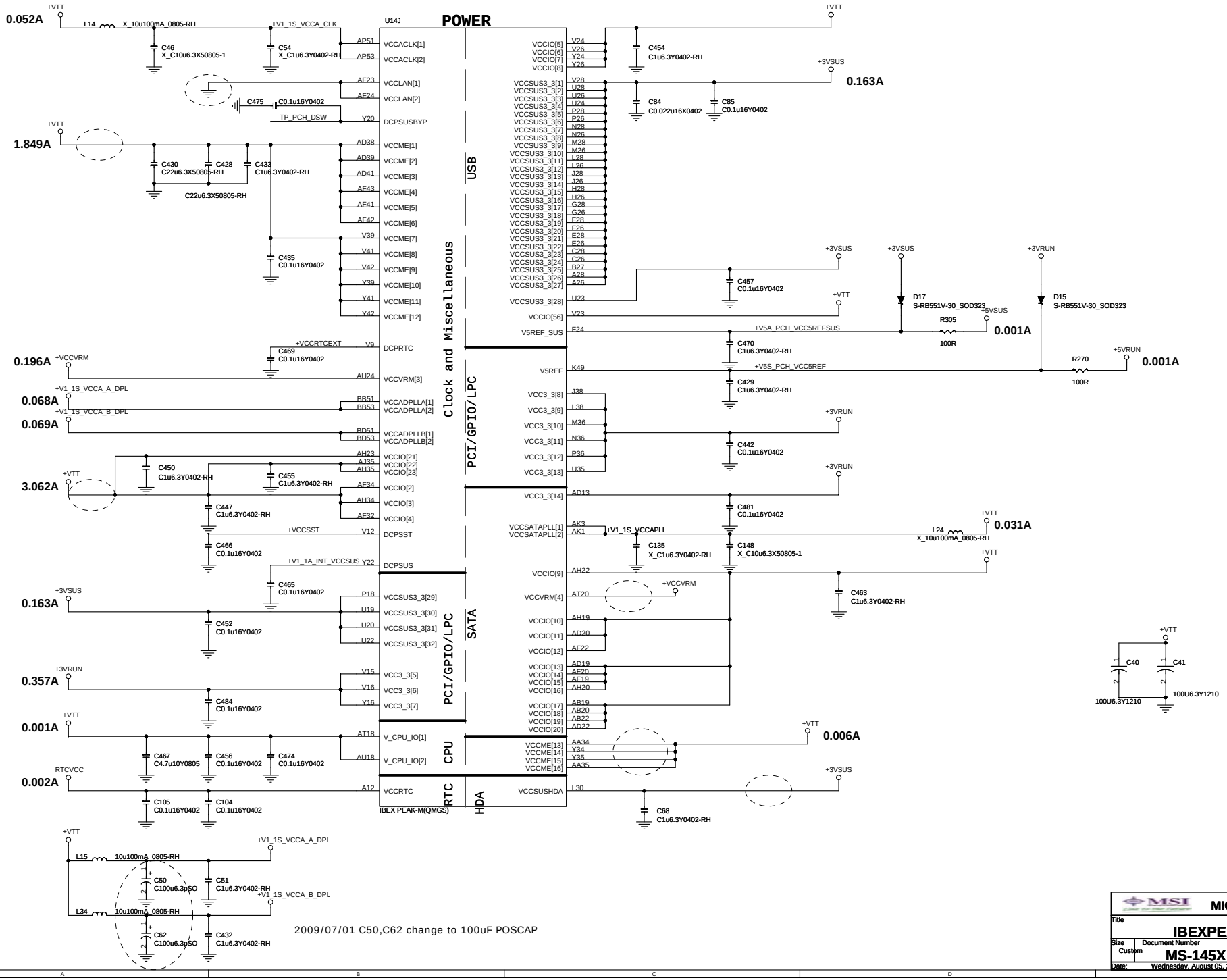
IBEXPEAK - M (POWER)



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (POWER)		
Size: Custom	Document Number: MS-145X		Rev: 0A
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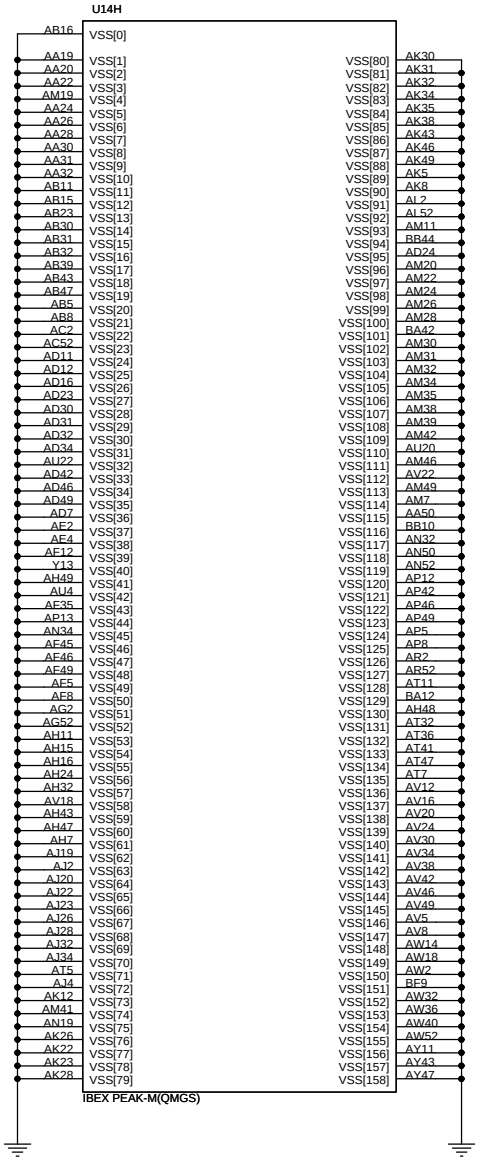
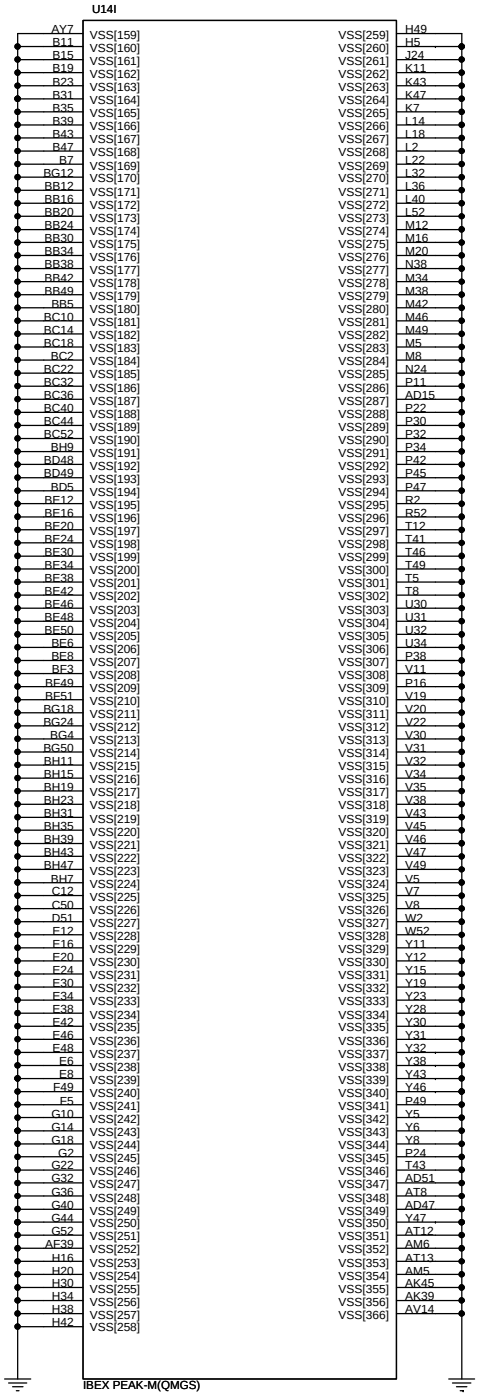
IBEXPEAK - M (GND)





MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (GND)

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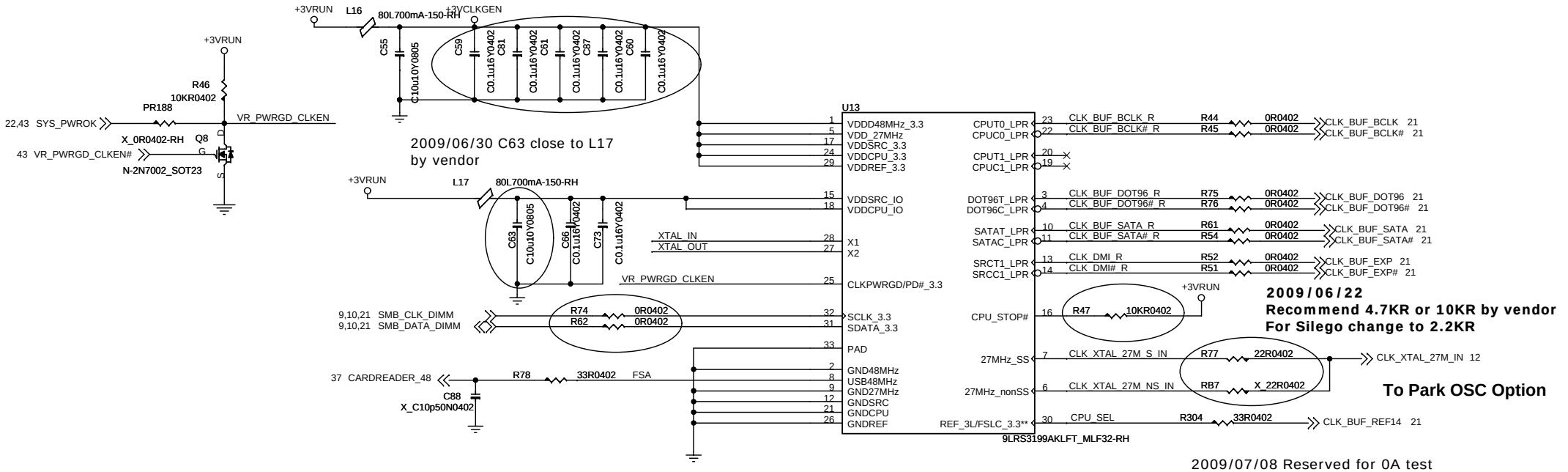
C59 Close to L16 ; C60,C61,C81,C87 Close to power pin

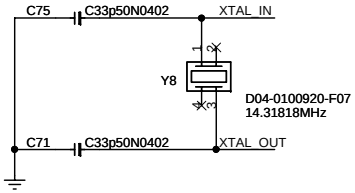


2009/06/22
Recommend 4.7KR or 10KR by vendor
For Silego change to 2.2KR

To Park OSC Option

2009/07/08 Reserved for 0A test
R3211 is for Spread clock(Default use)
RB8 is for non-Spread clock

2009/07/08
Y4換成49S type(cost down as MS-1122)

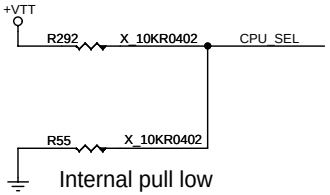


Capacity select

If Cload=20pf C71/C75=33pf

If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff



Internal pull low

For CPU frequency select (133MHz)

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Clock GEN. Vendor Table

	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff

MICRO-STAR INT'L CO.,LTD.

Title: **Clock Generator (9LRS3199AKLFT)**

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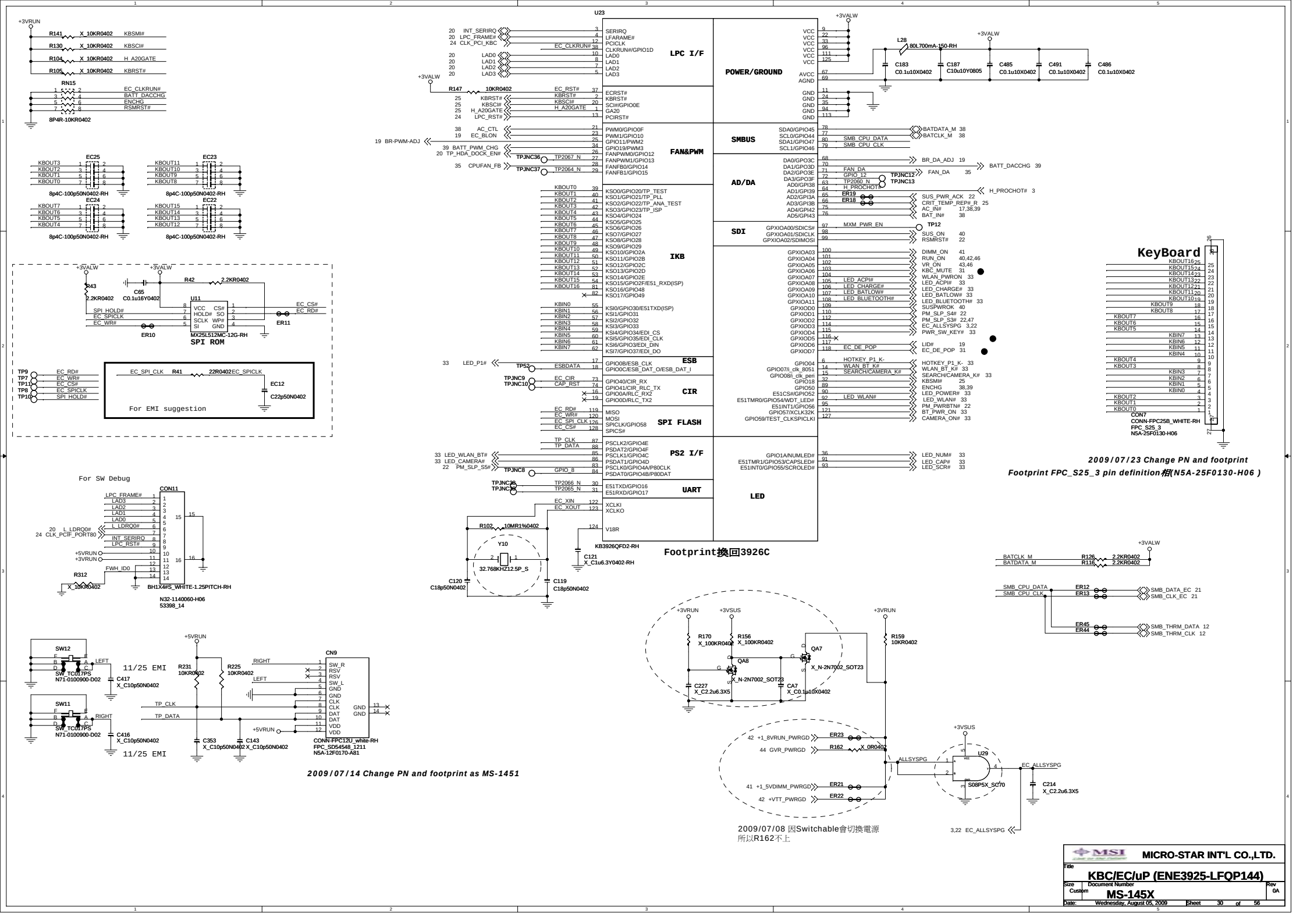
U23
LPC I/F
FAN&PWM
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
POWER/GROUND
SMBUS
AD/DA
SDI
LED
Footprint換回3926C
SPI ROM
MX25L512MC-12G-RH
KeyBoard
CONN-FPC25B_WHITE-RH
FPC_S25_3
N5A-25F0130-H06
2009/07/23 Change PN and footprint
Footprint FPC_S25_3 pin definition 按(N5A-25F0130-H06)
For SW Debug
For EMI suggestion
11/25 EMI
11/25 EMI
CONN-FPC12U_white-RH
FPC_SD54548_1211
N5A-12F0170-A81
2009/07/14 Change PN and footprint as MS-1451
2009/07/08 因Switchable會切換電源
所以R162不上
MICRO-STAR INT'L CO.,LTD.
KBC/EC/uP (ENE3925-LFQP144)
MS-145X
Wednesday, August 05, 2009
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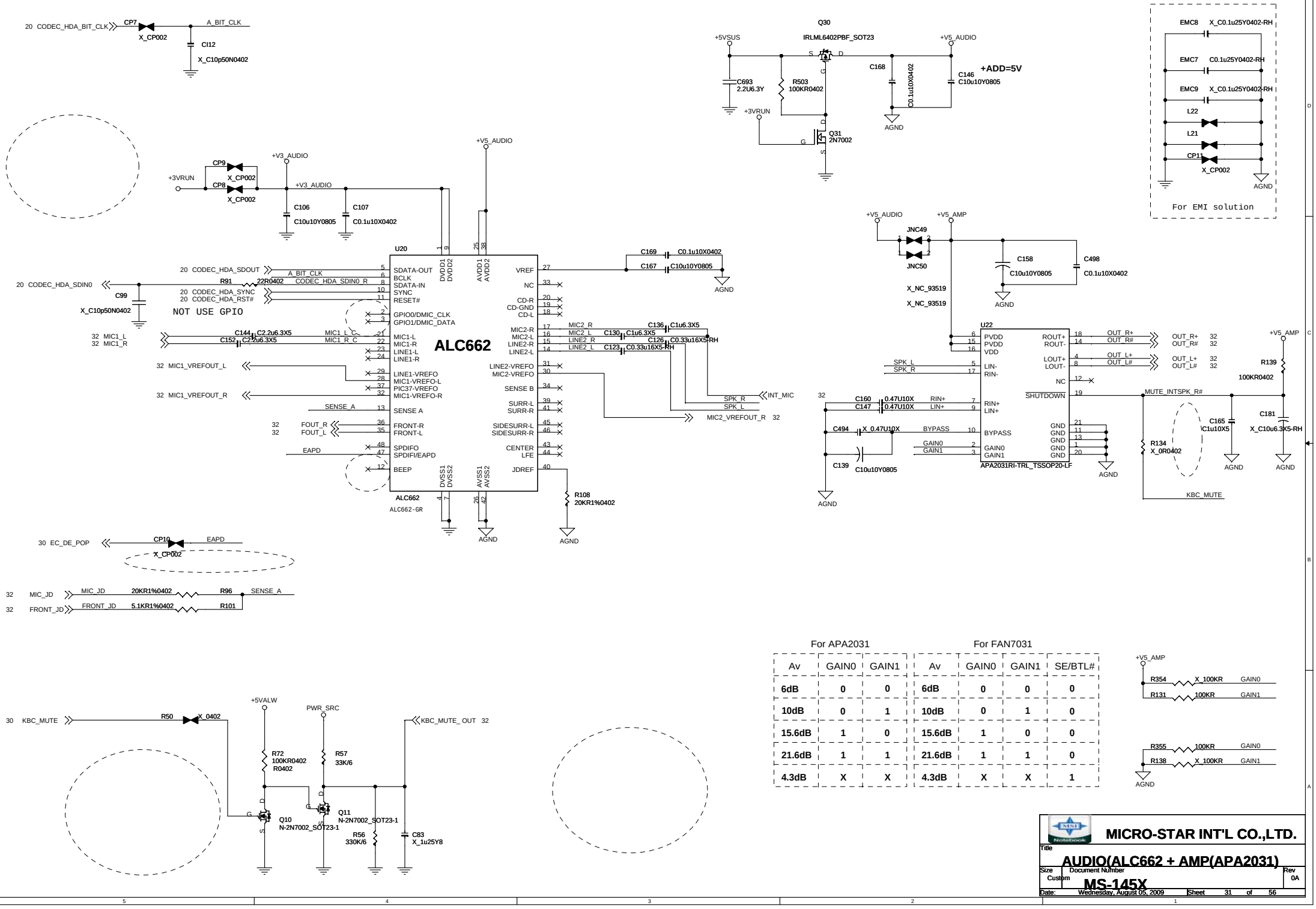
20 CODEC_HDA_BIT_CLK
CP7
X_CP002
A_BIT_CLK
CI12
X_C10p50N0402
Q30
IRLML6402PBF_SOT23
+5VSUS
+V5_AUDIO
C693
2.2U6.3Y
R503
100KR0402
C168
C0.1u10X0402
C146
C10u10Y0805
+ADD=5V
+3VRUN
Q31
2N7002
AGND
EMC8 X_C0.1u25Y0402-RH
EMC7 C0.1u25Y0402-RH
EMC9 X_C0.1u25Y0402-RH
L22
L21
CP11
X_CP002
For EMI solution
CP9
CP8
+V3_AUDIO
C106
C10u10Y0805
C107
C0.1u10X0402
U20
ALC662
ALC662-GR
20 CODEC_HDA_SDOUT
20 CODEC_HDA_SDIN0
R91
22R0402
CODEC_HDA_SDIN0_R
20 CODEC_HDA_SYNC
20 CODEC_HDA_RST#
C99
X_C10p50N0402
NOT USE GPIO
SDATA-OUT
BCLK
SDATA-IN
SYNC
RESET#
GPIO0/DMIC_CLK
GPIO1/DMIC_DATA
MIC1-L
MIC1-R
LINE1-L
LINE1-R
LINE1-VREFO
MIC1-VREFO-L
PIC37-VREFO
MIC1-VREFO-R
SENSE A
FRONT-R
FRONT-L
SPDIFO
SPDIFI/EAPD
BEEP
VREF
NC
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
LINE2-VREFO
MIC2-VREFO
SENSE B
SURR-L
SURR-R
SIDESURR-L
SIDESURR-R
CENTER
LFE
JDREF
C169
C0.1u10X0402
C167
C10u10Y0805
C144
C2.2u6.3X5
C152
C2.2u6.3X5
C136
C1u6.3X5
C130
C1u6.3X5
C126
C0.33u16X5-RH
C123
C0.33u16X5-RH
32 MIC1_L
32 MIC1_R
32 MIC1_VREFOUT_L
32 MIC1_VREFOUT_R
32 FOUT_R
32 FOUT_L
EAPD
SPK_R
SPK_L
INT_MIC
MIC2_VREFOUT_R 32
R108
20KR1%0402
30 EC_DE_POP
CP10
X_CP002
32 MIC_JD
32 FRONT_JD
MIC_JD
FRONT_JD
20KR1%0402
5.1KR1%0402
R96
R101
SENSE_A
+V5_AUDIO
+V5_AMP
JNC49
JNC50
X_NC_93519
X_NC_93519
C158
C10u10Y0805
C498
C0.1u10X0402
U22
APA2031RI-TRL_TSSOP20-LF
PVDD
VDD
LIN-
RIN-
ROUT+
ROUT-
LOUT+
LOUT-
SHUTDOWN
BYPASS
GAIN0
GAIN1
GND
SPK_L
SPK_R
OUT_R+
OUT_R#
OUT_L+
OUT_L#
MUTE_INTSPK_R#
C160
0.47U10X
C147
0.47U10X
C494
X_0.47U10X
C139
C10u10Y0805
R139
100KR0402
C165
C1u10X5
C181
X_C10u6.3X5-RH
R134
X_0R0402
KBC_MUTE
30 KBC_MUTE
R50
X_0402
+5VALW
PWR_SRC
KBC_MUTE_OUT 32
R72
100KR0402
R0402
R57
33K/6
Q10
N-2N7002_SOT23-1
Q11
N-2N7002_SOT23-1
R56
330K/6
C83
X_1u25Y8
For APA2031
For FAN7031
Av
GAIN0
GAIN1
SE/BTL#
6dB 0 0
10dB 0 1
15.6dB 1 0
21.6dB 1 1
4.3dB X X
6dB 0 0 0
10dB 0 1 0
15.6dB 1 0 0
21.6dB 1 1 0
4.3dB X X 1
R354 X_100KR GAIN0
R131 100KR GAIN1
R355 100KR GAIN0
R138 X_100KR GAIN1
MICRO-STAR INT'L CO.,LTD.
Title
AUDIO(ALC662 + AMP(APA2031)
Size Custom
Document Number MS-145X
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Date: Wednesday, August 05, 2009
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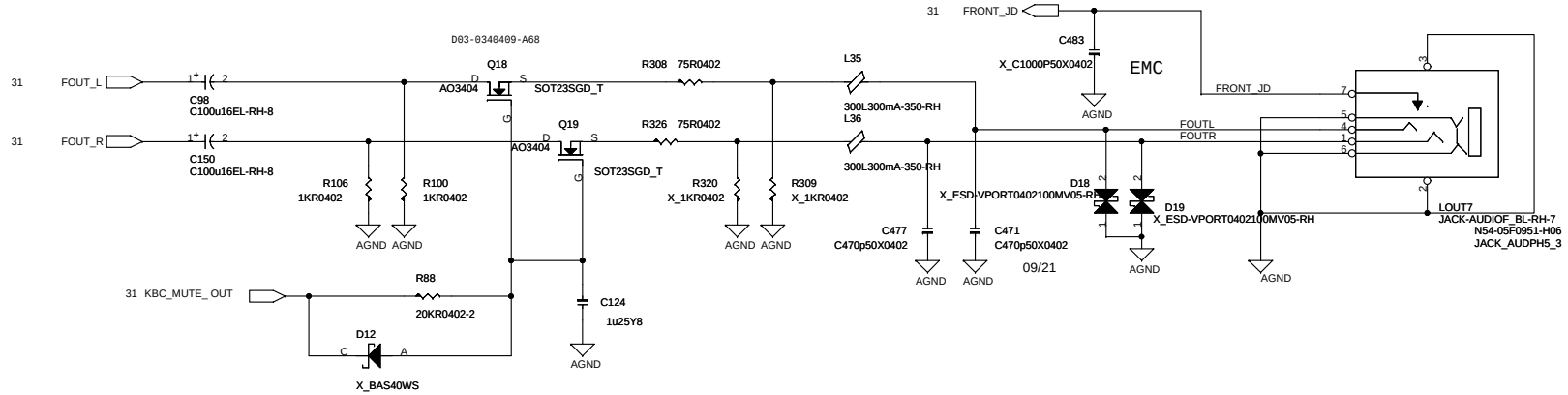
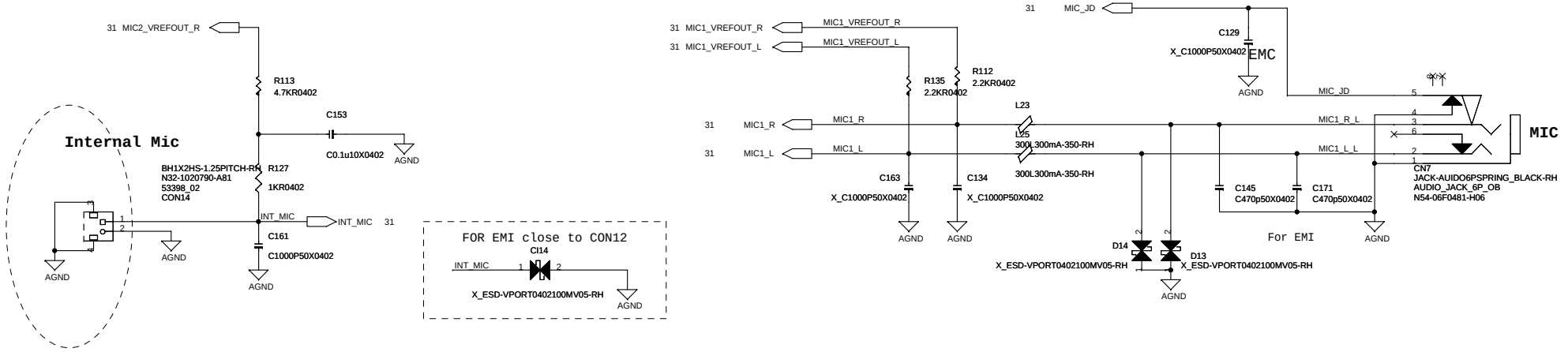
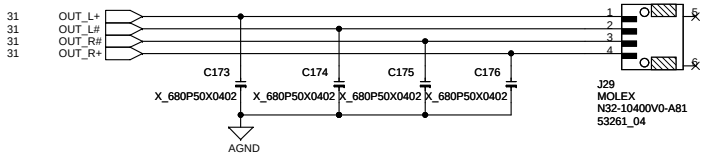




2009/06/29 Modify internal MIC PN to N32-1020790-A81



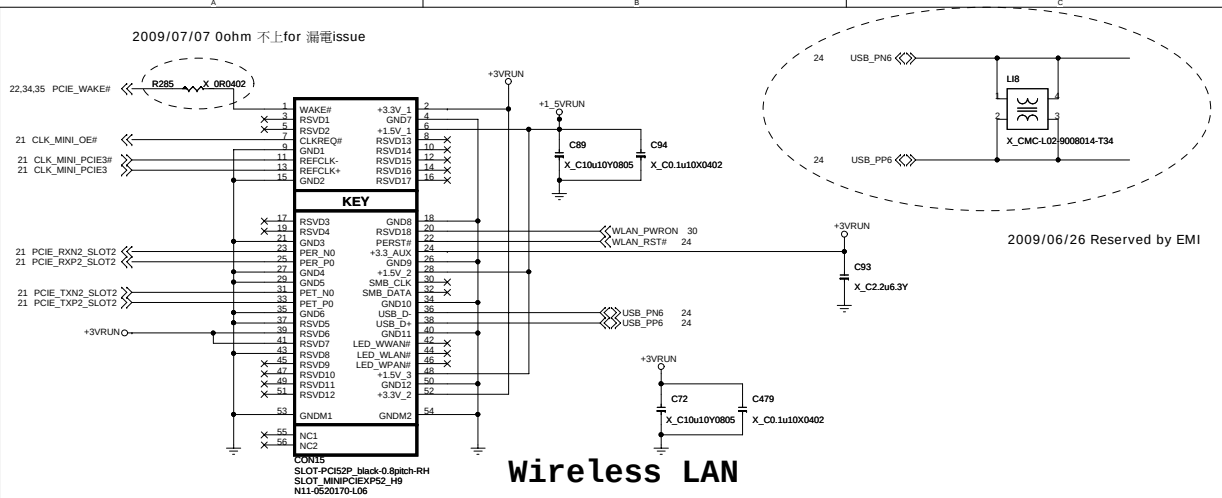
MICRO-STAR INT'L CO.,LTD.

Title: SPK / HP / MIC

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 32 of 56

2009/07/07 0ohm 不上for 漏電issue

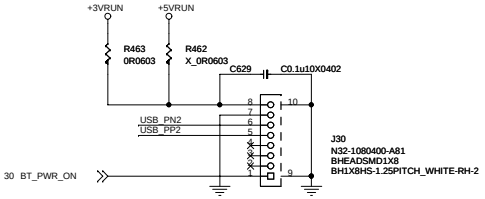


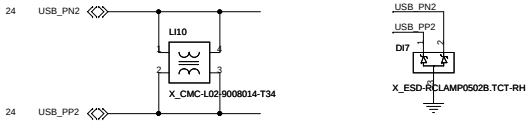
2009/06/26 Reserved by EMI

Wireless LAN

BLUETOOTH

2009/05/11 修改 for new MS-3801

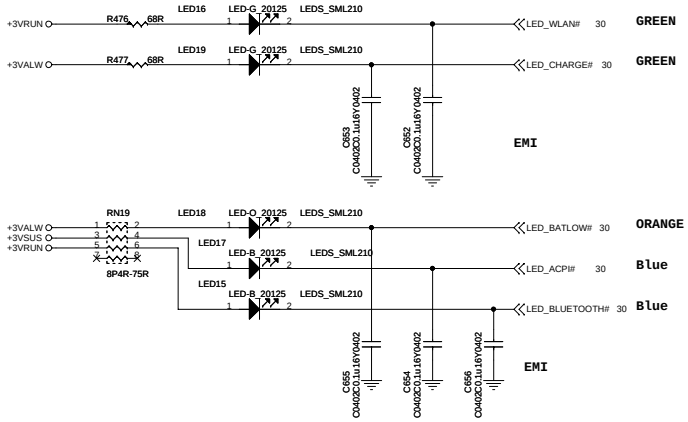




Reserved for EMI

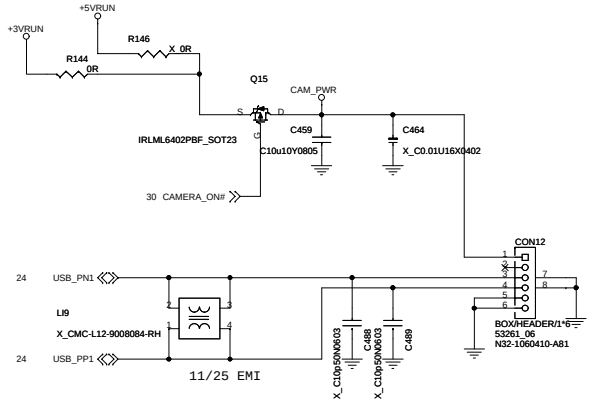
LED light

del CN8 0716



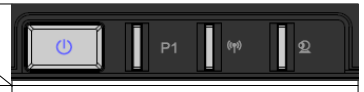
CAMERA

2009/06/29 Reserved 0 ohm pad by EMI



11/25 EMI

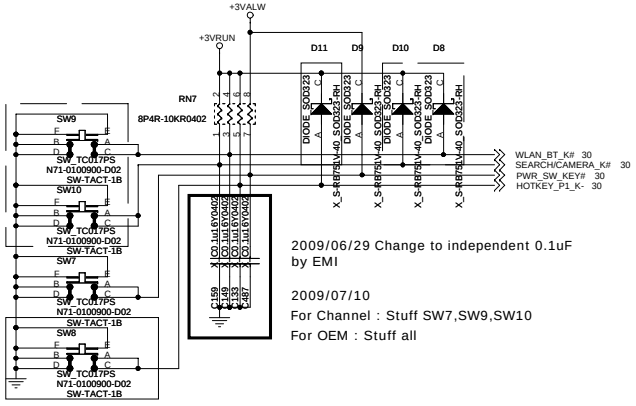
	LED7	LED8	LED9	LED10
	SW7	SW8	SW9	SW10



1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

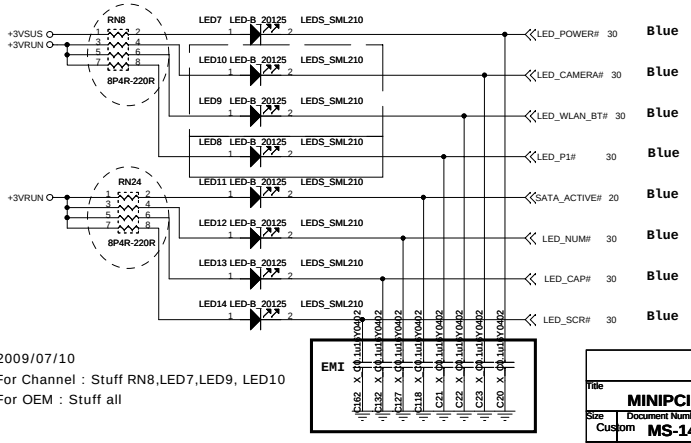
Stuff for CHANNEL ——— ———

Stuff for OEM ———



2009/06/29 Change to independent 0.1uF by EMI

2009/07/10
For Channel : Stuff SW7,SW9,SW10
For OEM : Stuff all



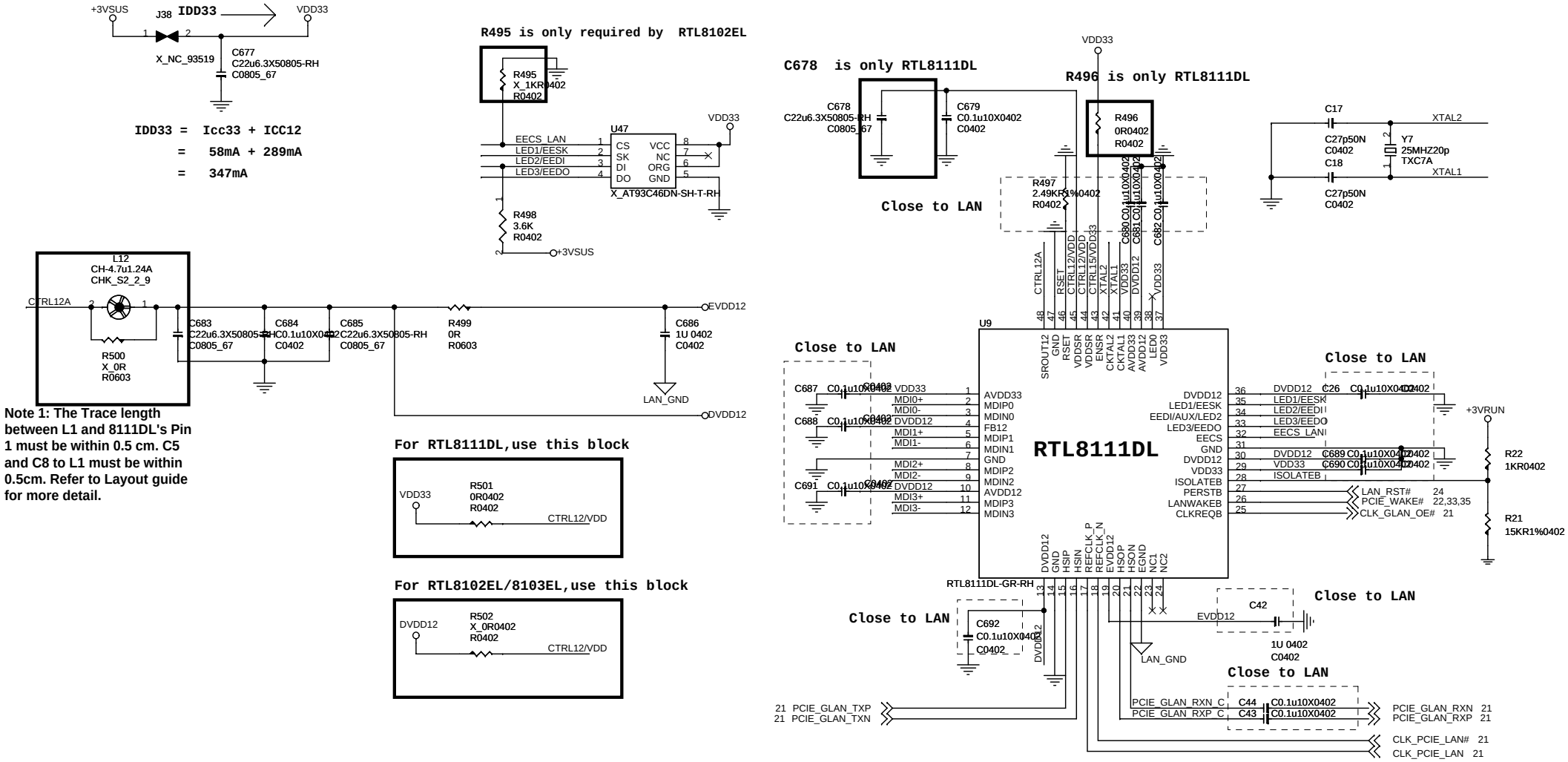
2009/07/10
For Channel : Stuff RN8,LED7,LED9, LED10
For OEM : Stuff all

MSI CORPORATION

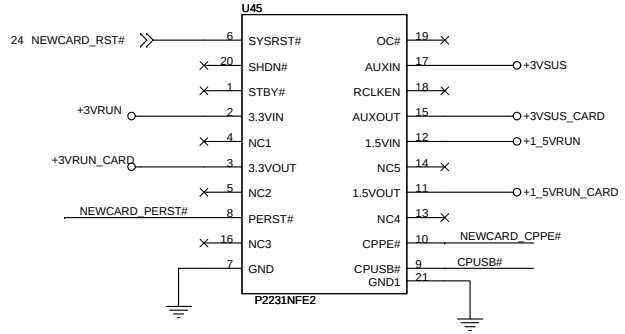
Title: MINIPCIE,CAMERA,BLUETOOTH,SW

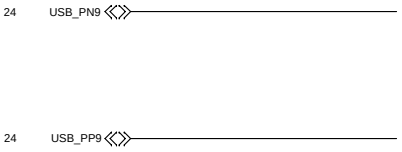
Size: Custom | Document Number: MS-145X | Rev: 0A

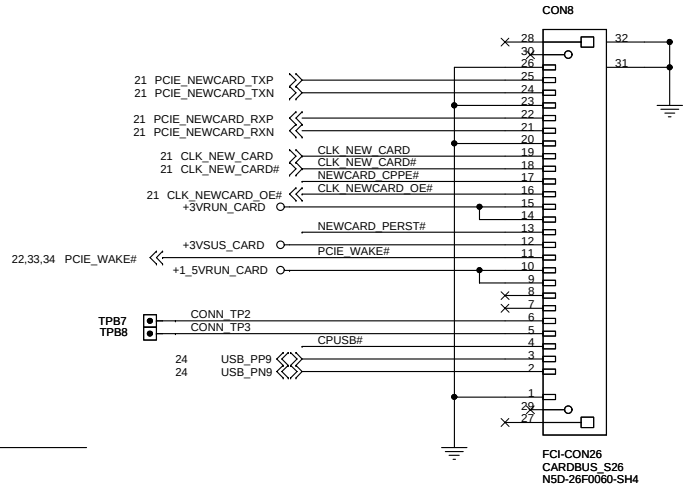
Date: Wednesday, August 05, 2009 | Sheet 33 of 56


+3VSUS
J38 IDD33
VDD33
X_NC_93519
C677
C22u6.3X50805-RH
C0805_67
IDD33 = Icc33 + ICC12
= 58mA + 289mA
= 347mA
R495 is only required by RTL8102EL
R495
X_1KR0402
R0402
U47
EECS_LAN
LED1/EESK
LED2/EEDI
LED3/EEDO
CS
SK
DI
DO
VCC
NC
ORG
GND
X_AT93C46DN-SH-T-RH
R498
3.6K
R0402
+3VSUS
C678 is only RTL8111DL
C678
C22u6.3X50805-RH
C0805_67
C679
C0.1u10X0402
C0402
R496 is only RTL8111DL
R496
0R0402
R0402
Close to LAN
R497
2.49KR1%0402
R0402
C17
C27p50N
C0402
C18
C27p50N
C0402
Y7
25MHZ20p
TXC7A
XTAL2
XTAL1
L12
CH-4.7u1.24A
CHK_S2_2_9
CTRL12A
R500
X_0R
R0603
C683
C22u6.3X50805-RH
C0805_67
C684
C0.1u10X0402
C0402
C685
C22u6.3X50805-RH
C0805_67
R499
0R
R0603
C686
1U 0402
C0402
LAN_GND
EVDD12
DVDD12
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.
For RTL8111DL,use this block
VDD33
R501
0R0402
R0402
CTRL12/VDD
For RTL8102EL/8103EL,use this block
DVDD12
R502
X_0R0402
R0402
CTRL12/VDD
U9
RTL8111DL
RTL8111DL-GR-RH
Close to LAN
C687 C0.1u10X0402
C688 C0.1u10X0402
C691 C0.1u10X0402
C692
C0.1u10X0402
C0402
C42
1U 0402
C0402
LAN_GND
R22
1KR0402
R21
15KR1%0402
+3VRUN
LAN_RST# 24
PCIE_WAKE# 22,33,35
CLK_GLAN_OE# 21
21 PCIE_GLAN_TXP
21 PCIE_GLAN_TXN
PCIE_GLAN_RXN_C
PCIE_GLAN_RXP_C
C44 C0.1u10X0402
C43 C0.1u10X0402
PCIE_GLAN_RXN 21
PCIE_GLAN_RXP 21
CLK_PCIE_LAN# 21
CLK_PCIE_LAN 21
MDC CONN
CN12
L11
TS
CN_TS
1000L400m_450_0805
L7
RING
CN_RING
1000L400m_450_0805
BH1X2S_white-1.25pitch
N32-1020650-H06
SD_53780_0210
CN11
RJ11
RJ45
CN_TS
CN_RING
TRD3-
TRD3+
TRD1-
TRD1+
TRD2-
TRD2+
TRD0-
TRD0+
LTK_RJ4511ROS_RJ4511
N55-12F0110-AF2
RJ45_RJ11_SMT_14P
LAN MAGNETICS
Close to Transfomer
T7
C674 C0.1u10X
C675 C0.1u10X
C676 C0.1u10X
C673 C0.1u10X
V_DAC
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
TCT4
TD4+
TD4-
MCT1
MX1+
MX1-
MCT2
MX2+
MX2-
MCT3
MX3+
MX3-
MCT4
MX4+
MX4-
MCT4
TRD3-
TRD3+
MCT3
TRD2-
TRD2+
MCT2
TRD1-
TRD1+
MCT1
TRD0-
TRD0+
GST5009 LF-RH
R20
X_NC_93519
LAN_GND
RN20
MCT1
MCT2
MCT3
MCT4
8P4R-75R
RN0402_MSI
EC2
C1000p50N
C0805_67
2009/06/24 Modify as 1451
MICRO-STAR INT'L CO.,LTD.
Title
PCIE 1G LAN (RTL8111DL)
Size
Custom
Document Number
MS-145X
Rev
0A
Date:
Sheet 34 of 56

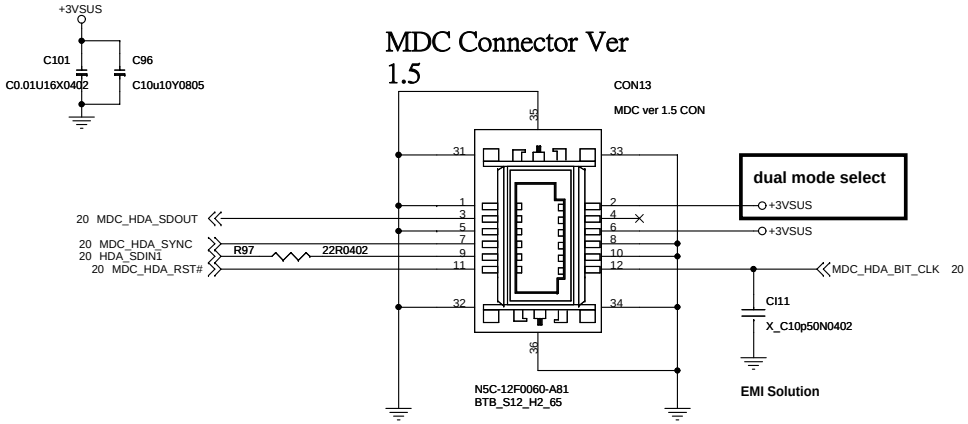
NEW CARD





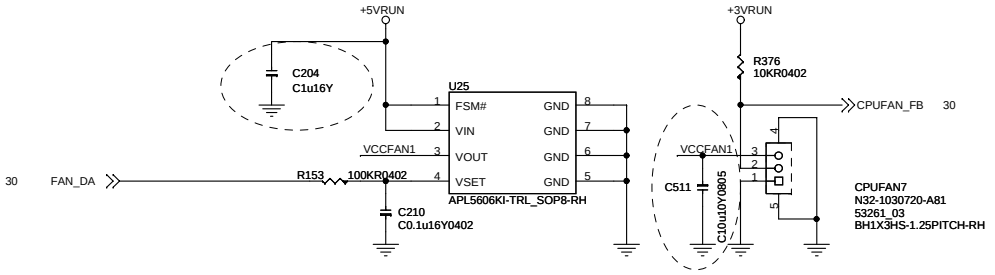


MDC Connector



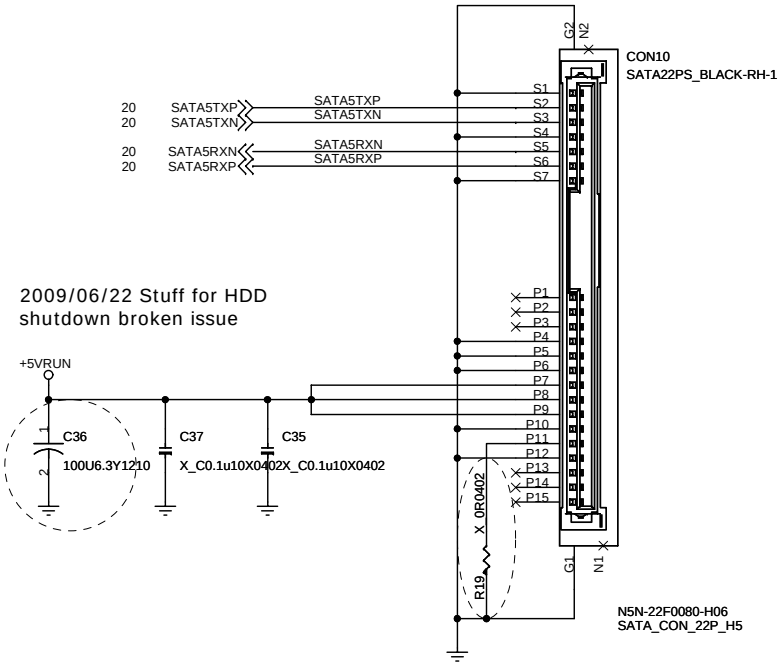
2009/07/14 因限高問題,改回1451用料N5C-12F0060-A81

CPU FAN



MSI	MICRO-STAR INT'L CO.,LTD.
Title	NEWCARD,FAN
Size: Custom	Document Number: MS-145X
Rev	0A
Date:	Sheet 35 of 56

SATA HDD

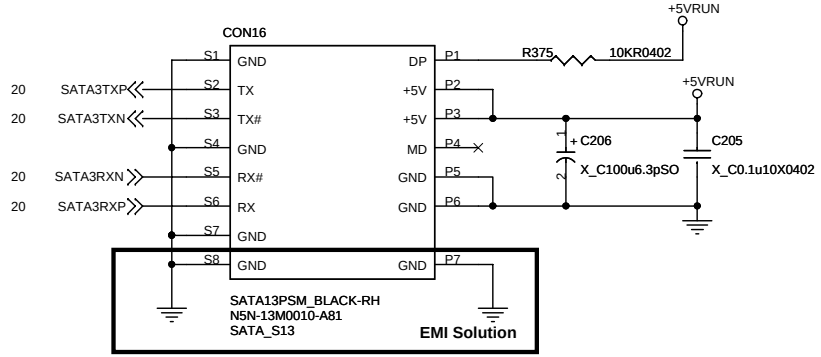


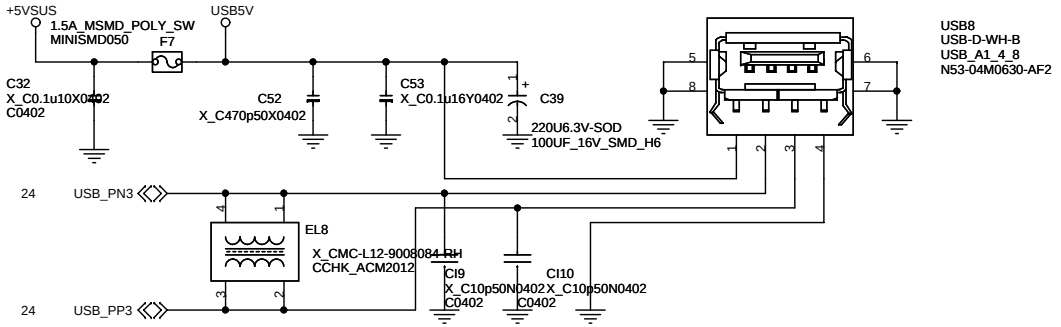
2009/06/22 SATA HDD P11 is Staggered Spinup function

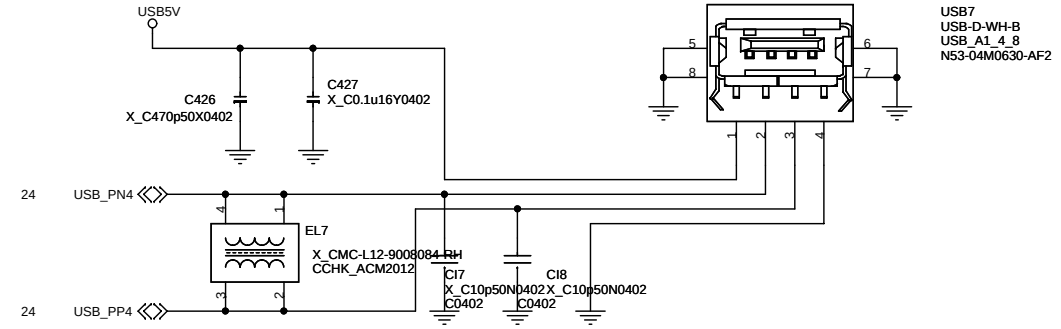
Staggered Spinup :

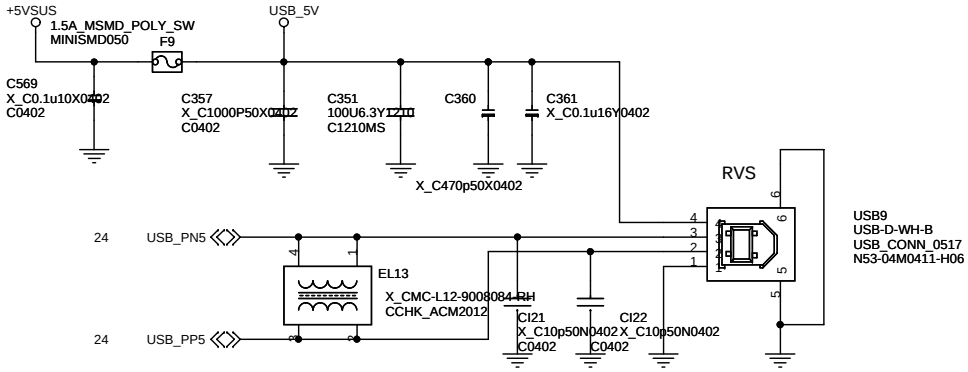
如果system 支援這個功能,開機時 HDD 的馬達是不轉的,
BIOS 必須下command 把 HDD wake up,才能做偵測HDD的動作
如果不支援Staggered Spinup 這個function 這隻腳必須接地

SATA ODD









2009/07/07 USB common choke先不上

MSI MICRO-STAR INT'L CO.,LTD.

Title: HDD,CDROM,USB

Size: Custom | Document Number: MS-145X | Rev: 0A

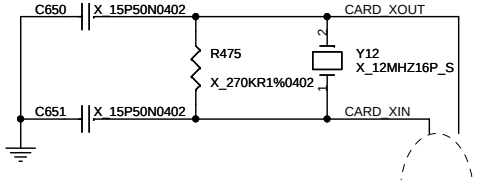
Date: Wednesday, August 05, 2009 | Sheet 36 of 56

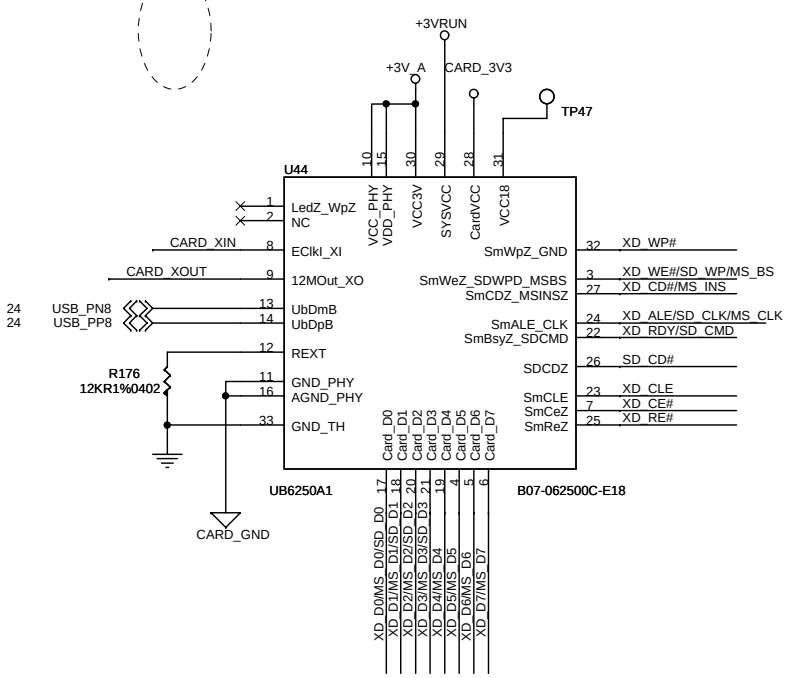
ENE UB6250 USB20 Flash Card Reader Controller
Pins for SD, MMC, MS, and xD memory cards

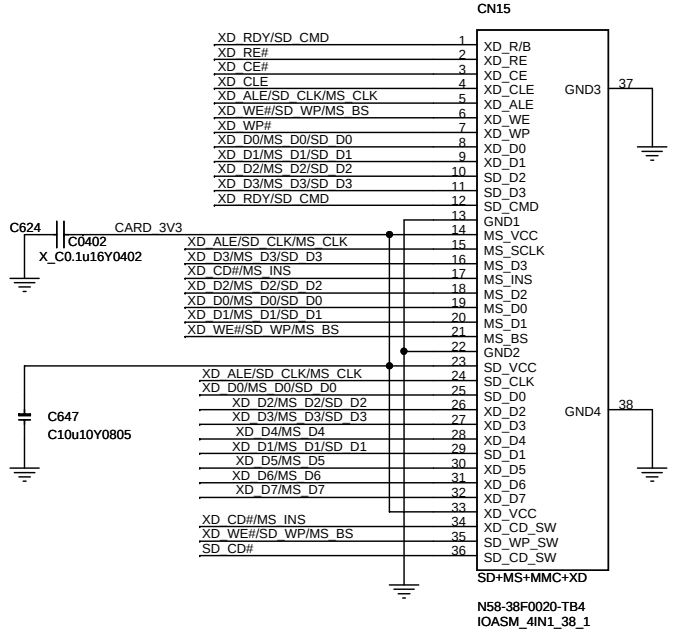
Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD

29 CARDREADER_48 — 0R0402 — R473 — CARD_XIN

2009/07/01 48MHz from Clock GEN.



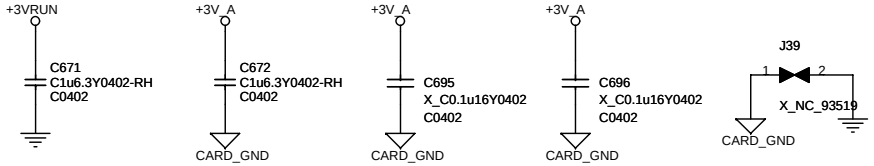




CLOCK frequency can vary
lie on strap pin config(pin7&pin25)

Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClkin pin
xDReZ	xDCeZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz



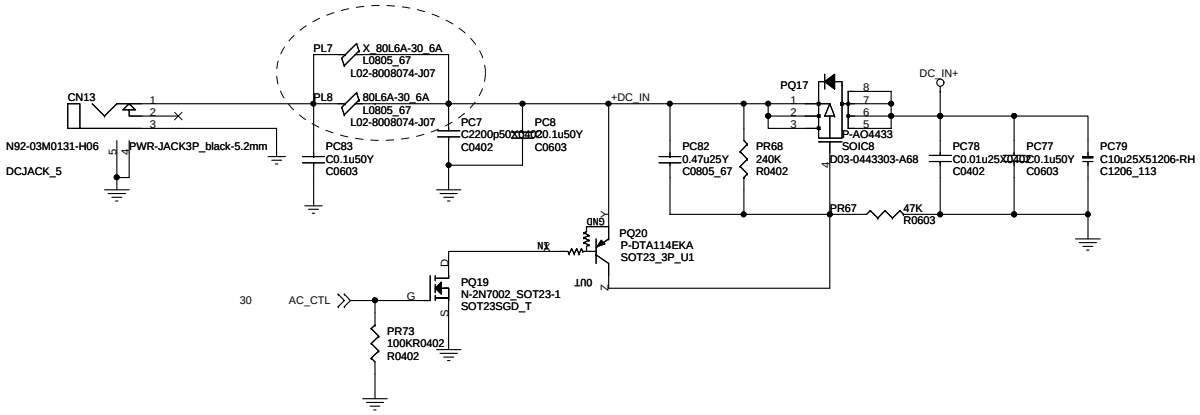
MICRO-STAR INT'L CO.,LTD.

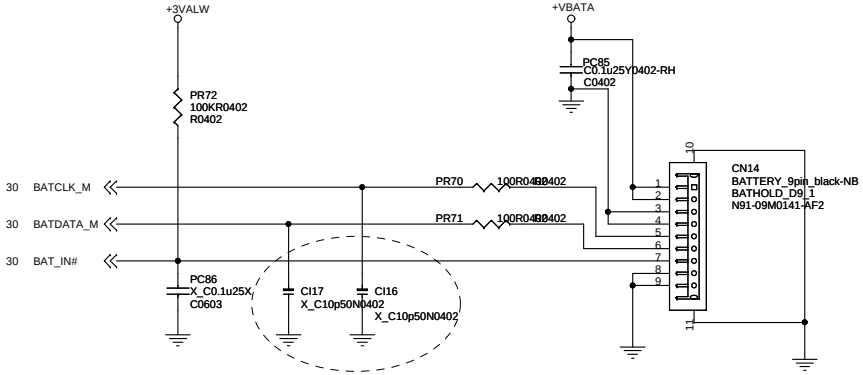
Title: CARD_READER (RTS5159)

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 37 of 56

2009/07/10 65W adaptor只需要上一個BEAD

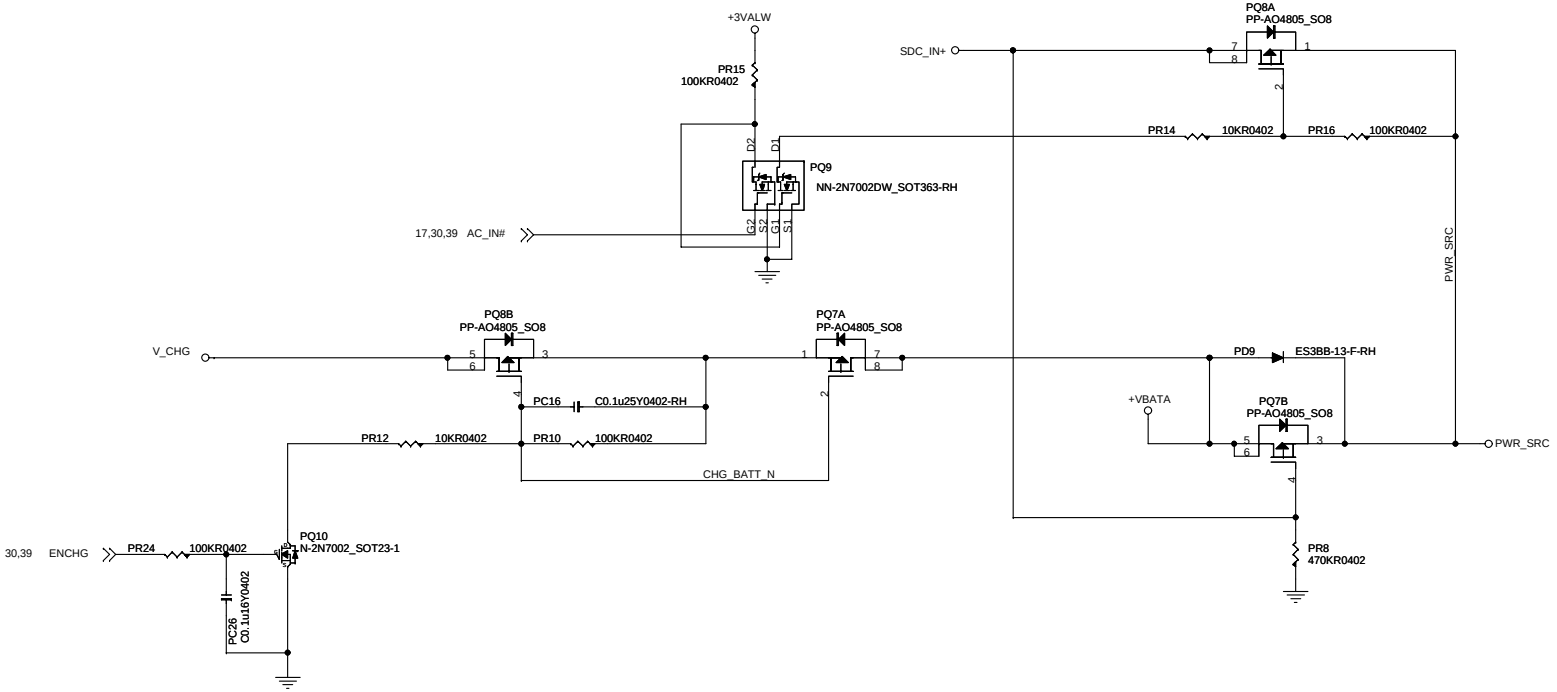




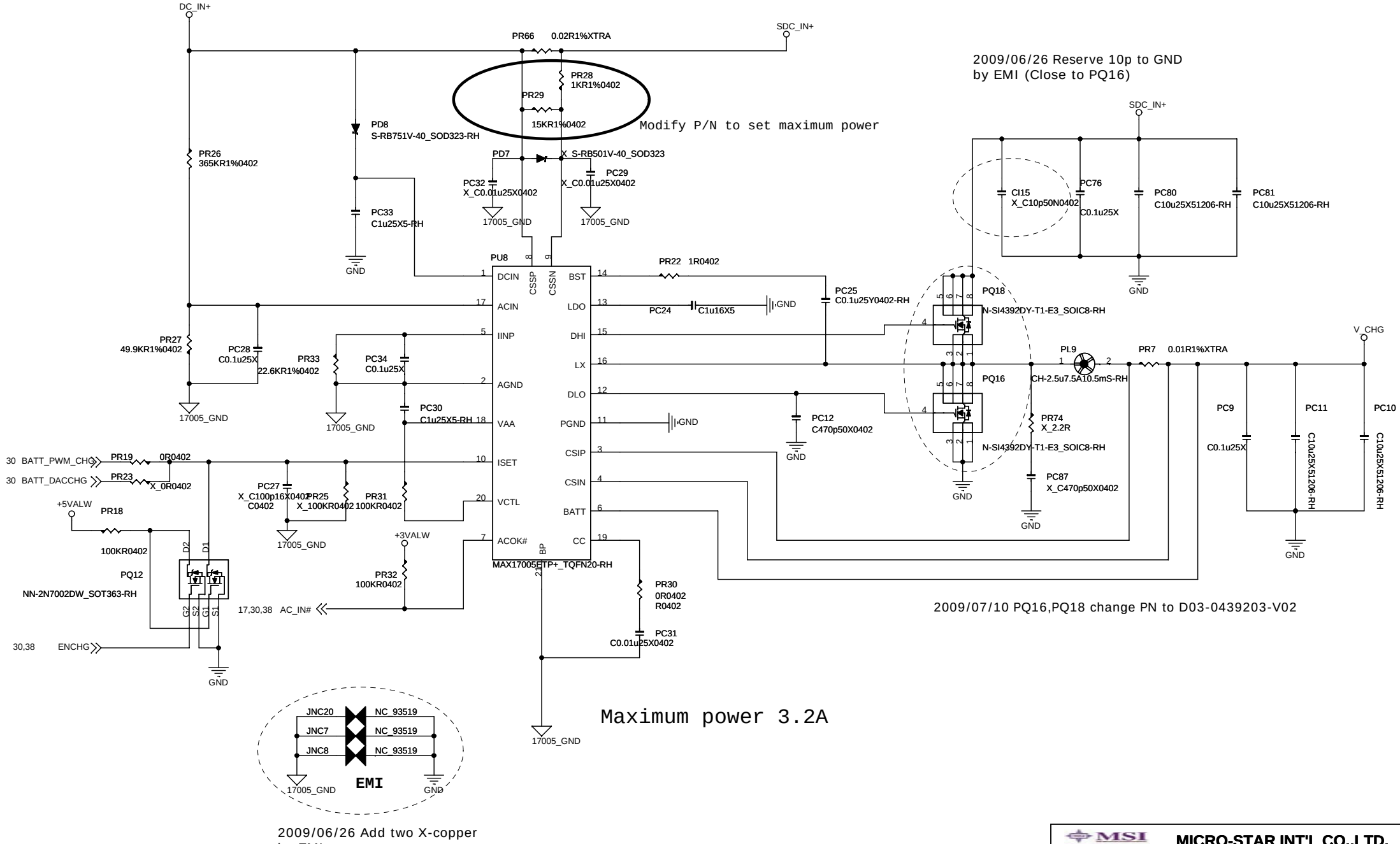
2009/06/26 Reserve 10p to GND
by EMI

JBAT1 Pin Definition

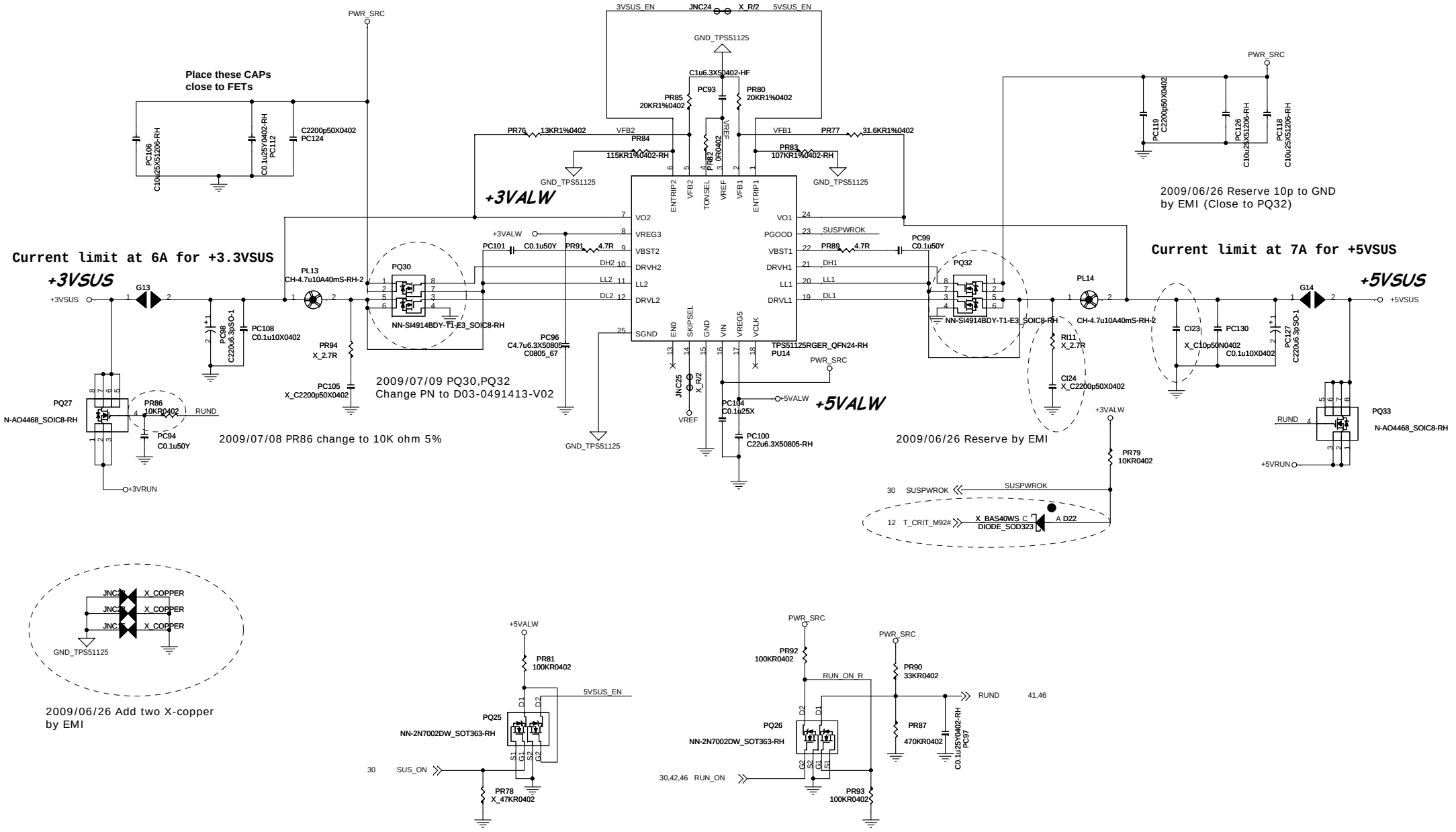
1: VBATA+
2: VBATA+
3: NC
4: NC
5: SMBCLK
6: SMBDATA
7: BAT_IN#
8: GND
9: GND



MSI MICRO-STAR INT'L CO.,LTD.			
Title: Battery Select			
Size: Custom	Document Number: MS-145X		Rev: 0A
Date: Wednesday, August 05, 2009		Sheet 38 of 56	



MSI Link to the Future	MICRO-STAR INT'L CO.,LTD.	
Title: Battery Charger		
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 39 of 56	



MICRO-STAR INT'L CO.,LTD.

Title: System power

Size: Custom | Document Number: MS-145X | Rev: 0A

Date: Wednesday, August 05, 2009 | Sheet 40 of 56

2009/06/26 Reserve 10p to GND
by EMI (Close to PQ21)

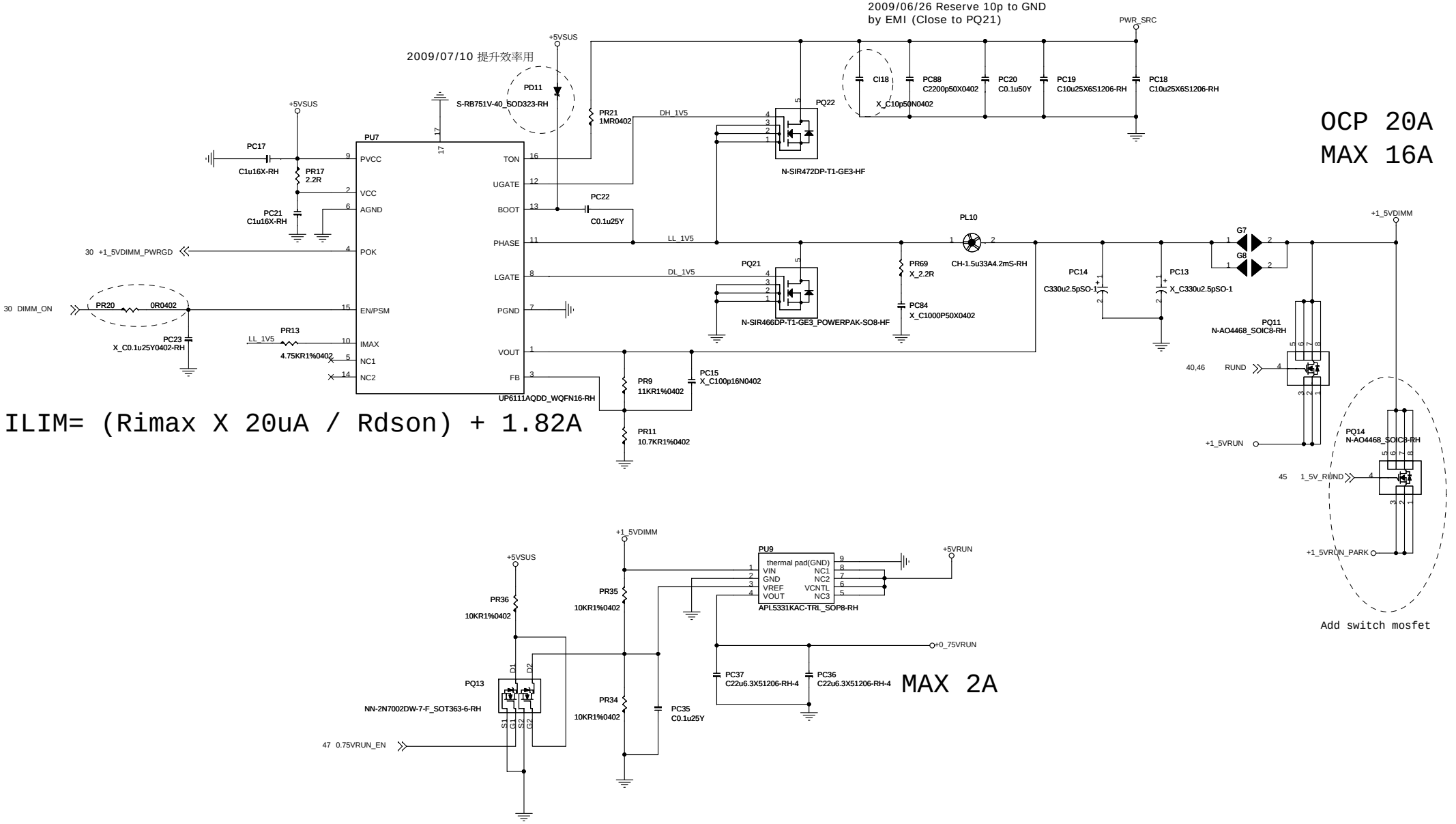
2009/07/10 提升效率用

OCP 20A
MAX 16A

ILIM= (Rimax X 20uA / Rdson) + 1.82A

MAX 2A

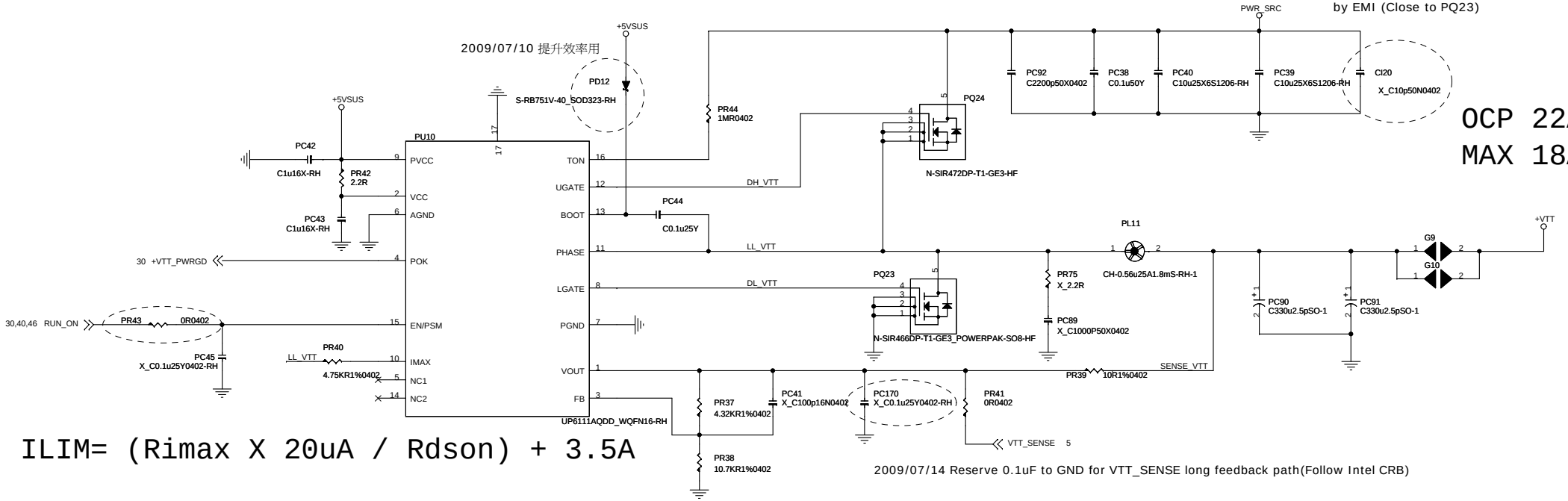
Add switch mosfet



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	SMDDR_VTERM /1_5VRUN	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 41 of 56	

2009/06/26 Reserve 10p to GND
by EMI (Close to PQ23)

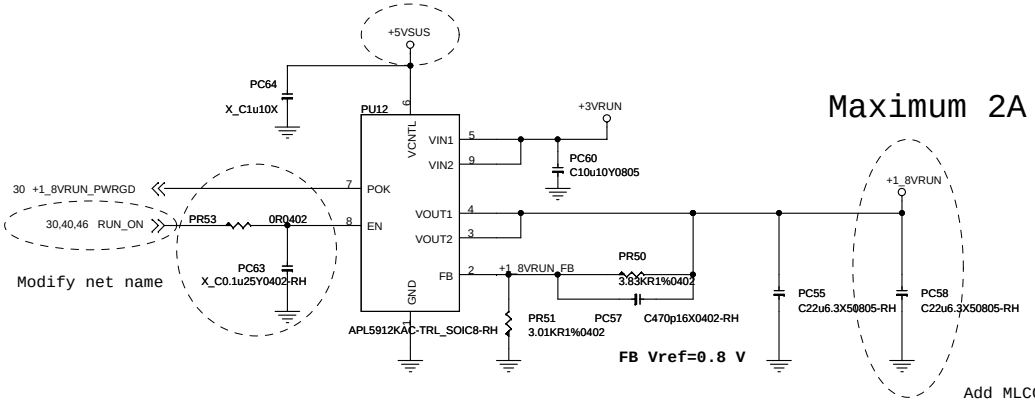
2009/07/10 提升效率用



OCP 22A
MAX 18A

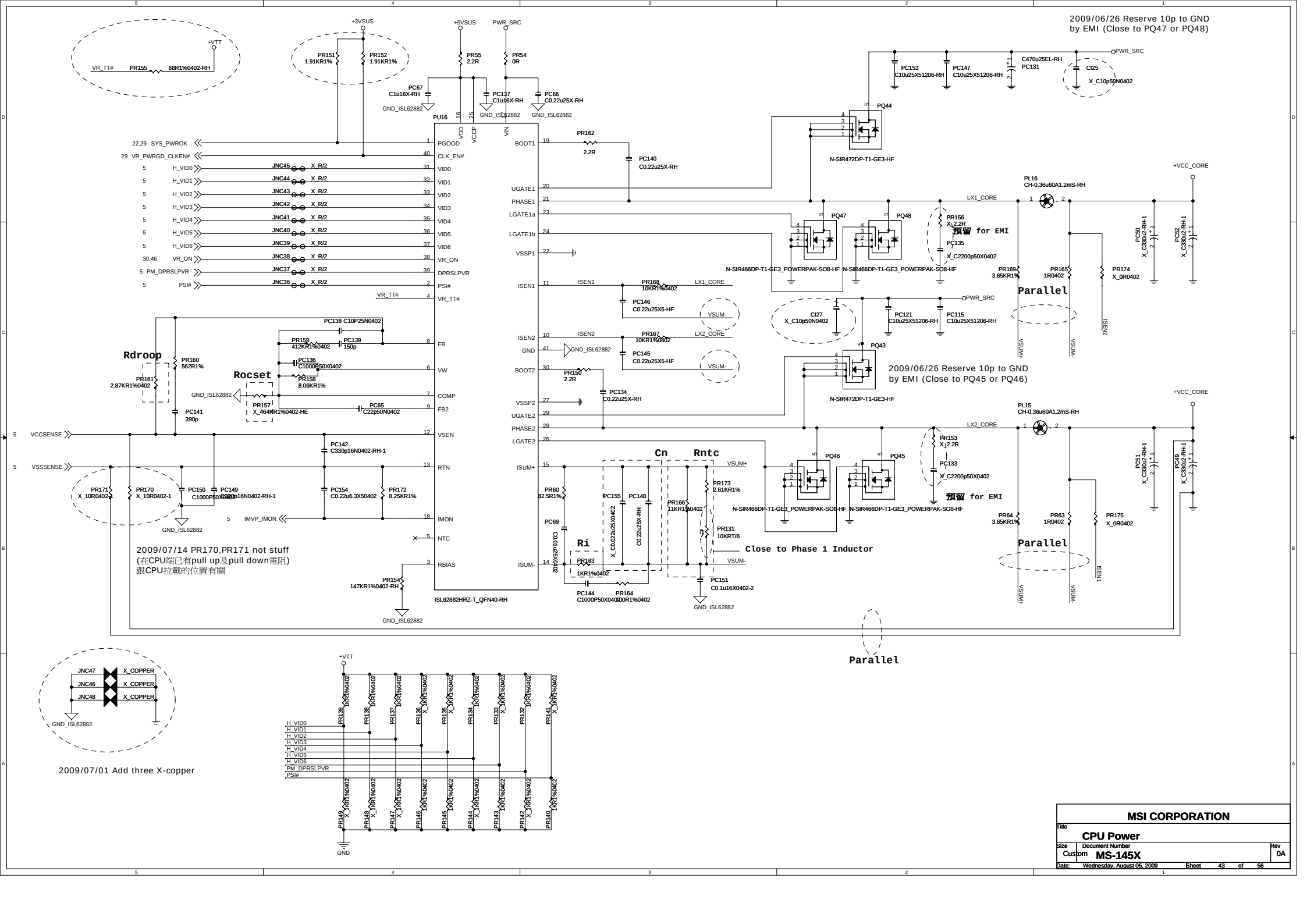
ILIM= (Rimax X 20uA / Rdson) + 3.5A

2009/07/14 Reserve 0.1uF to GND for VTT_SENSE long feedback path(Follow Intel CRB)



Maximum 2A

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	VTT Power,+1.8VRUN	
Size: Custom	Document Number: MS-145X	Rev: 0A
Date: Wednesday, August 05, 2009	Sheet 42 of 56	


2009/06/26 Reserve 10p to GND
by EMI (Close to PQ47 or PQ48)
2009/06/26 Reserve 10p to GND
by EMI (Close to PQ45 or PQ46)
2009/07/14 PR170,PR171 not stuff
(在CPU端已有pull up及pull down電阻)
跟CPU拉載的位置有關
2009/07/01 Add three X-copper
Close to Phase 1 Inductor
Parallel
Parallel
ISL62882HRZ-T_QFN40-RH
N-SIR472DP-T1-GE3-HF
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
Rdroop
Rocset
Cn
Rntc
Ri
MSI CORPORATION
CPU Power
MS-145X
Custom
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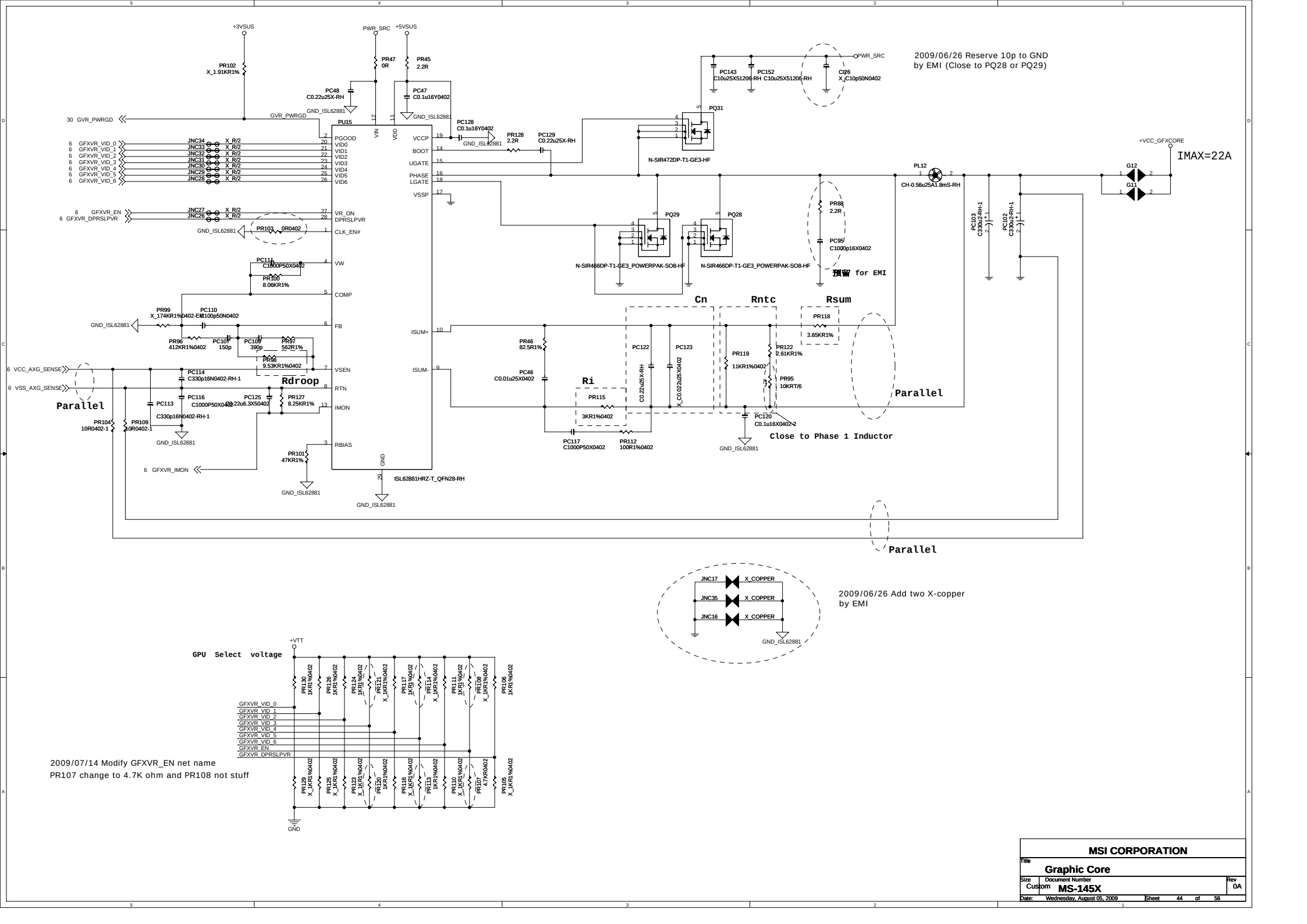

MSI CORPORATION	
Title	Graphic Core
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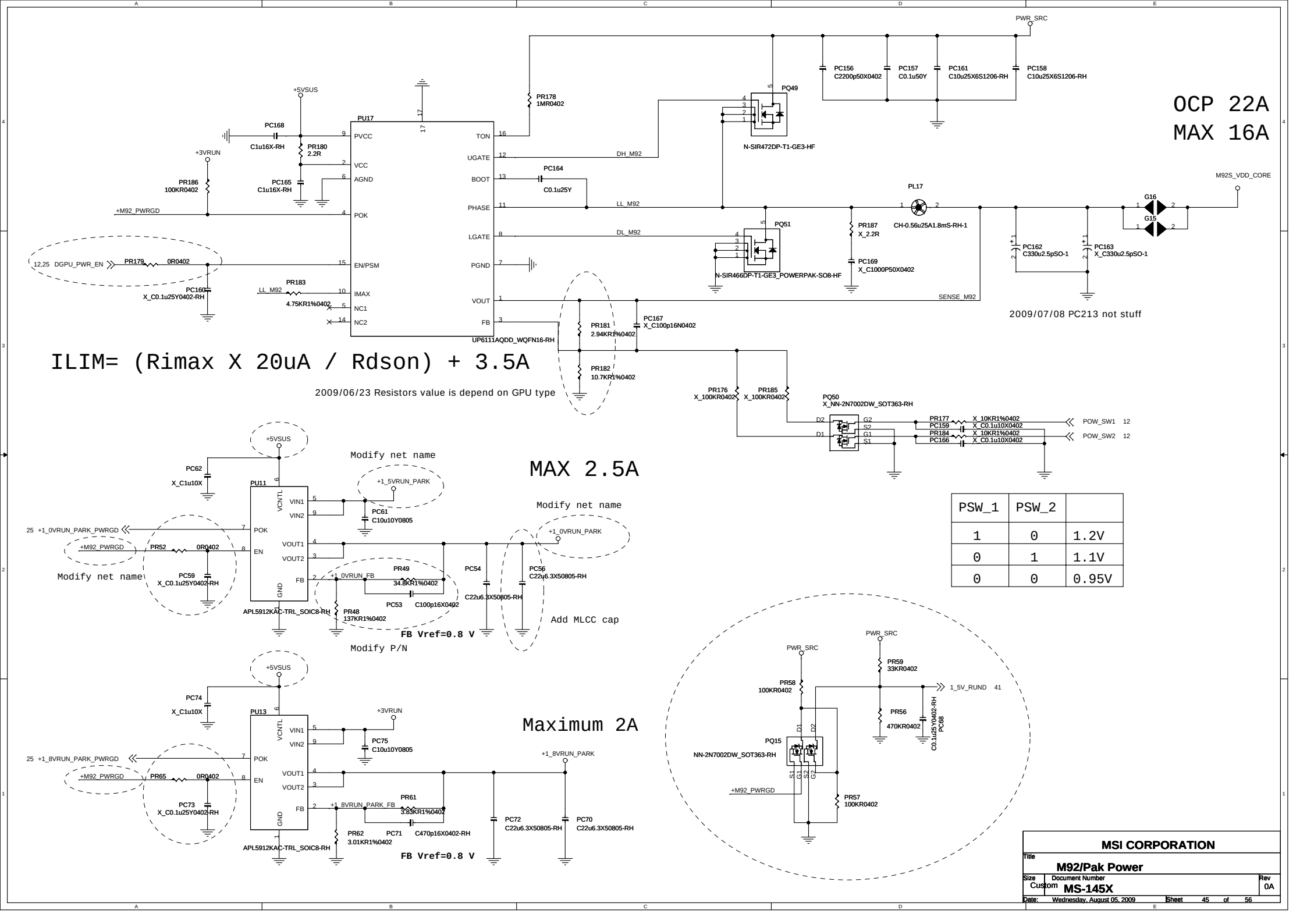

PSW_1	PSW_2	
1	0	1.2V
0	1	1.1V
0	0	0.95V

MSI CORPORATION		
Title: M92/Pak Power		
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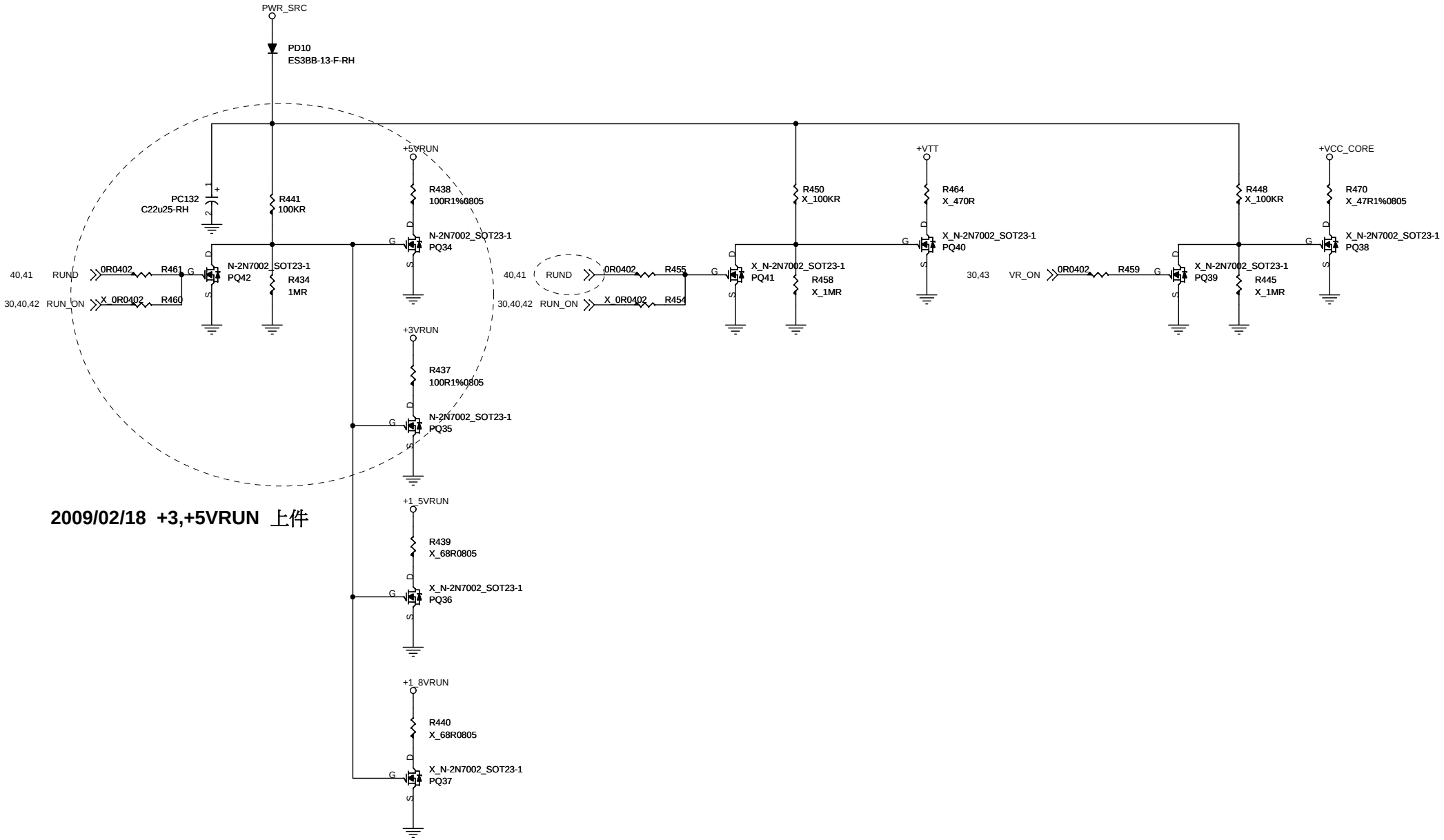

2009/02/18 +3,+5VRUN 上件

MICRO-STAR INT'L CO.,LTD.			
Title: Discharge Circuits			
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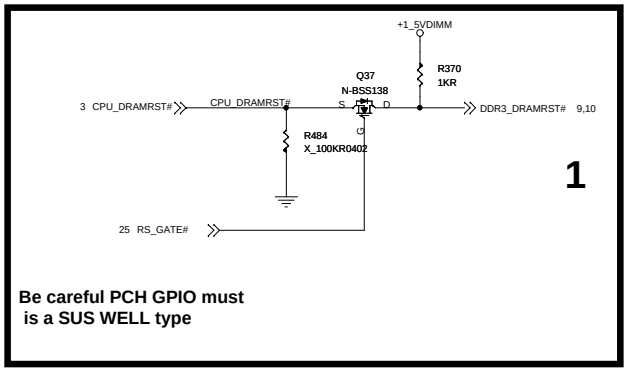

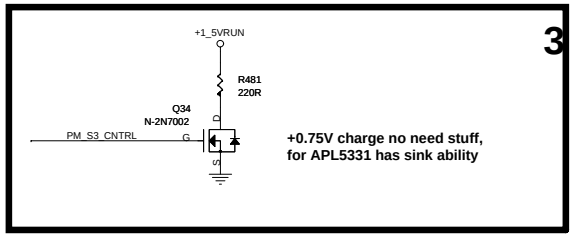

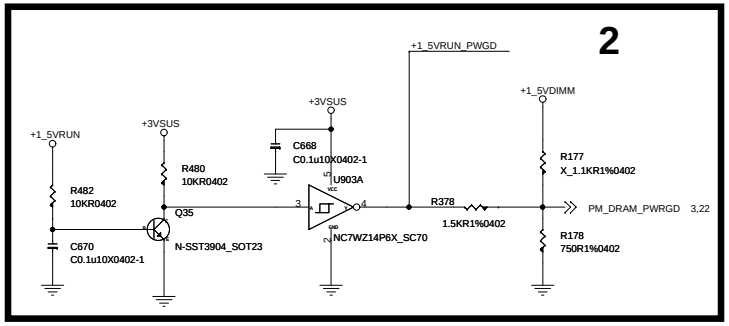

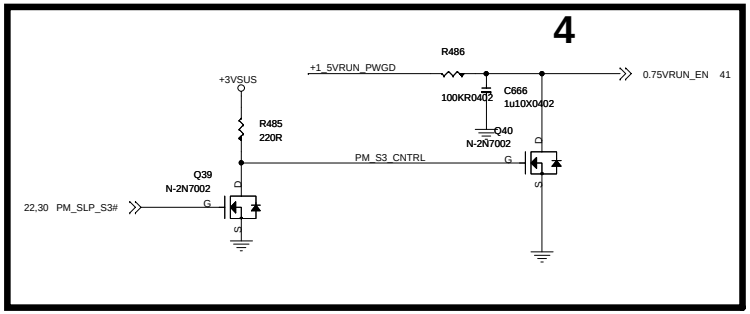

MICRO-STAR INT'L CO.,LTD.

Title: INTEL S3 POWER

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C-case & D-case

MH17 HOLES_8X8_D3MM_VIA8
MH14 HOLES_8X8_D3MM_VIA5
MH18 HOLES_8X8_D3MM_VIA8
MH19 HOLES_8X8_D3MM_VIA8
MH15 HOLES_8X8_D3MM_VIA8
MH10 HOLES_8X8_D3MM_VIA8
MH8 HOLES_8X8_D3MM_VIA8
MH7 HOLES_8X8_D3MM_VIA8
MH13 HOLES_8X8_D3MM_VIA5
MH12 HOLES_8X8_D3MM_VIA5
MH9 HOLES_8X8_D3MM_VIA8
MH11 HOLES_8X8_D3MM_VIA5

12/1 EMI

UME8
HOLES_R177D91
E2B-1634020-L63

MDC Stand off

CN10
FRAME_62_55X44_7
New Card Socket
E2M-4410111-SH4
SCREW5
SCREW6
E43-1204004-H29
E43-1204004-H29

ExpressCard

UME1
HDMI LABEL
HDMI_LABEL

PCB PN

PCB4
PCB
P30-1451111-H73

MH16
HOLES_8X8_D3MM_VIA5

阻抗測試線確認

J19 L3_DIFF_8/5/8_70_Ohm+ / X_H1X2_black-RH	J24 L4_DIFF_8/5/8_70_Ohm+ / X_H1X2_black-RH	J17 L1_5mil_55_Ohm / X_H1X2_black-RH	J13 L6_5mil_55_Ohm / X_H1X2_black-RH
J10 L3_DIFF_8/5/8_70_Ohm- / X_H1X2_black-RH	J18 L4_DIFF_8/5/8_70_Ohm- / X_H1X2_black-RH	J12 L3_4.5mil_55_ohm / X_H1X2_black-RH	J25 L4_4.5mil_55_ohm / X_H1X2_black-RH
J11 L4_DIFF_4.5/5.5/4.5_90_Ohm+ / X_H1X2_black-RH	J20 L6_DIFF_4.5/5.5/4.5_90_Ohm+ / X_H1X2_black-RH	J16 L4_5.5mil_50_Ohm / X_H1X2_black-RH	
J22 L4_DIFF_4.5/5.5/4.5_90_Ohm- / X_H1X2_black-RH	J23 L6_DIFF_4.5/5.5/4.5_90_Ohm- / X_H1X2_black-RH		
J27 L1_DIFF_4/7/4_100_Ohm+ / X_H1X2_black-RH	J7 L3_DIFF_4/7/4_100_Ohm+ / X_H1X2_black-RH	J9 L4_DIFF_4/7/4_100_Ohm+ / X_H1X2_black-RH	J8 L6_DIFF_4/7/4_100_Ohm+ / X_H1X2_black-RH
J26 L1_DIFF_4/7/4_100_Ohm- / X_H1X2_black-RH	J15 L3_DIFF_4/7/4_100_Ohm- / X_H1X2_black-RH	J14 L4_DIFF_4/7/4_100_Ohm- / X_H1X2_black-RH	J21 L6_DIFF_4/7/4_100_Ohm- / X_H1X2_black-RH

PCH

Holes_R276D185P_PT H7 HOLES_R268D142
Holes_R276D185P_PT H8 HOLES_R268D142

CPU

Holes_R276D185P_PT H10 E2B-1676010-RH
Holes_R276D185P_PT H9 E2B-1676010-RH
Holes_R276D185P_PT H11 E2B-1676010-RH

GPU

HOLES_R177D91 H12 E2B-1022010-RH

Thermal_Module_Stand-off 螺絲孔

PAD12 E23-1029010-RH
PAD10 X_E23-1029050-RH
PAD7 X_E23-1029050-RH
PAD11 X_E23-1029050-RH
PAD9 E23-1029050-RH

GND PAD in TOP side

FM1 F_PAD_X
FM2 F_PAD_X
FM3 F_PAD_X
FM4 F_PAD_X
FM5 F_PAD_X
FM6 F_PAD_X
FM7 F_PAD_X
FM8 F_PAD_X
FM9 F_PAD_X
FM10 F_PAD_X
FM11 F_PAD_X
FM12 F_PAD_X
FM13 F_PAD_X
FM14 F_PAD_X
FM15 F_PAD_X
FM16 F_PAD_X
FM17 F_PAD_X
FM18 F_PAD_X
FM19 F_PAD_X
FM20 F_PAD_X

+1_5VDIMM
+0_75VRUN
+VTT
+VCC_CORE
+5VSUS
+3VSUS
+1_8VRUN
+VCC_GFXCORE
+5VRUN
+3VRUN
+3VALW
PWR_SRC
SDC_IN+

PAD18 10X6.7X3.1
PAD19 10X6.7X3.1
PAD20 X_MS-55101-RH
PAD21 X_MS-55101-RH
PAD22 X_MS-55101-RH

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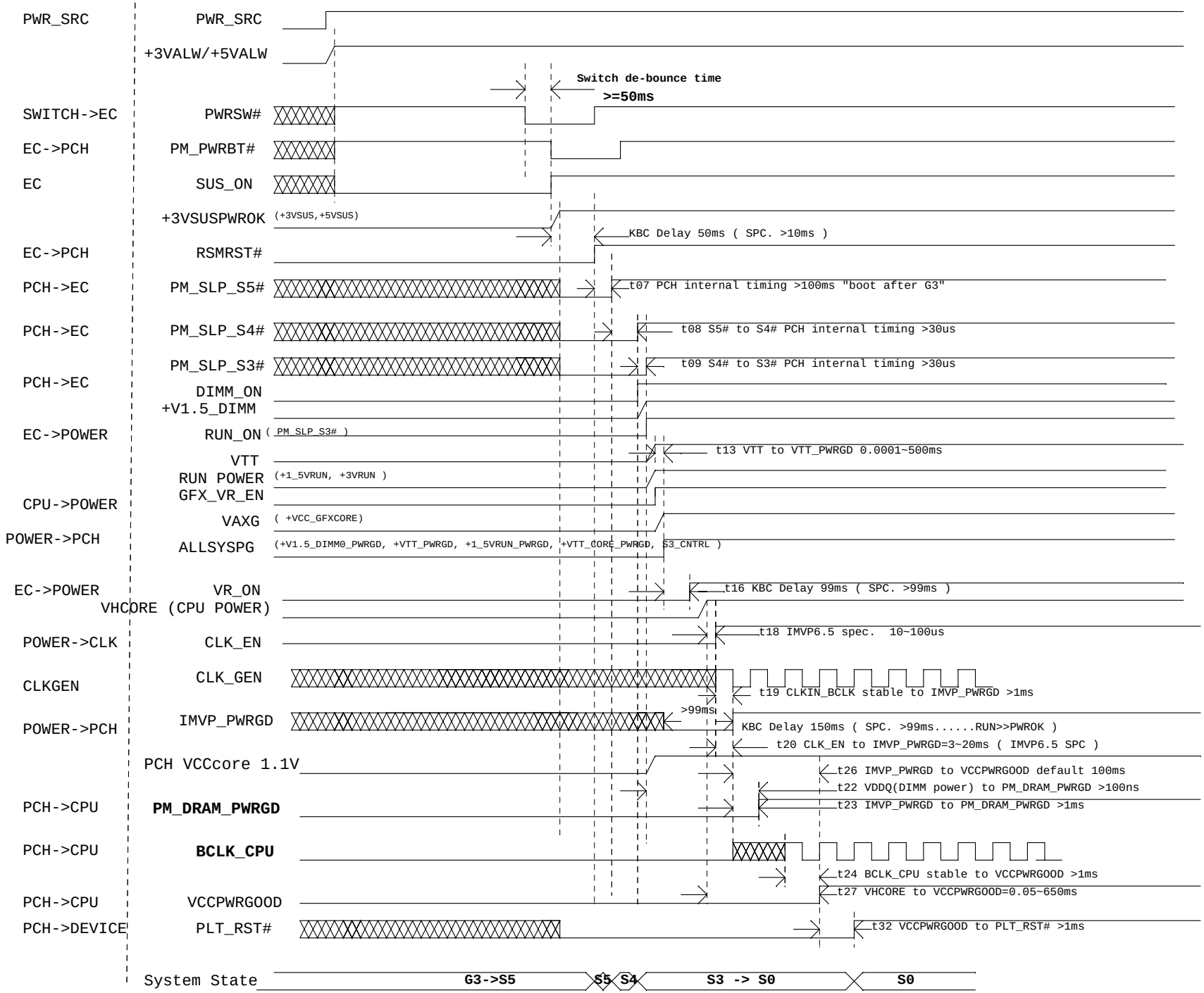
Calpella System Power on Sequence DC mode



MSI	MICRO-STAR INT'L CO.,LTD.
Title	Power on Sequency
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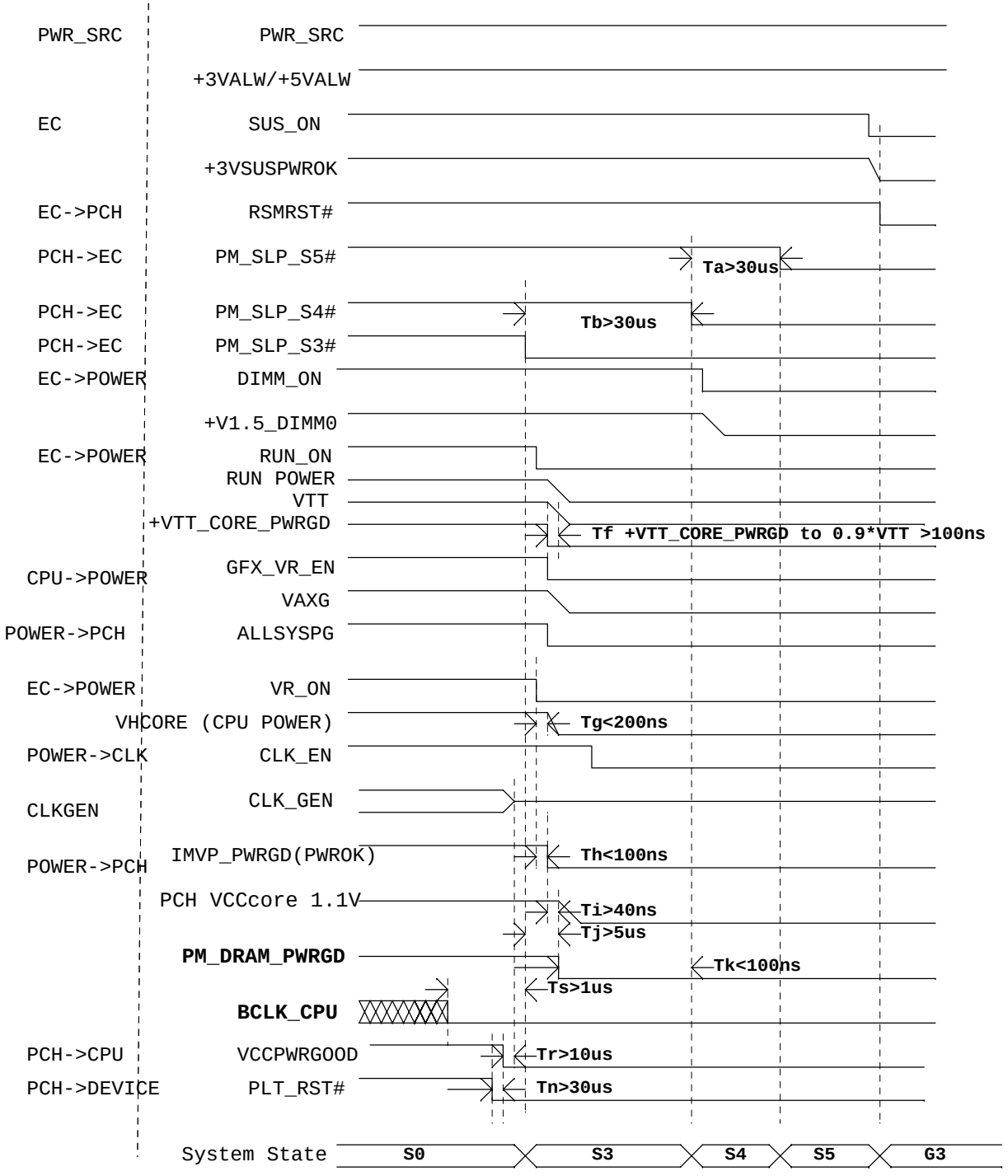
Power down Sequence DC mode S0 to G3



MICRO-STAR INT'L CO.,LTD.			
Title: Power on Sequency			
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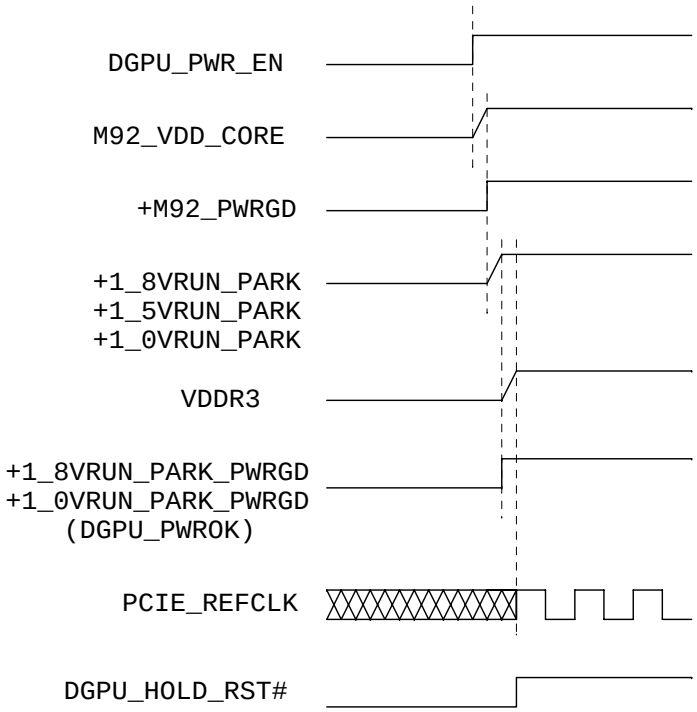
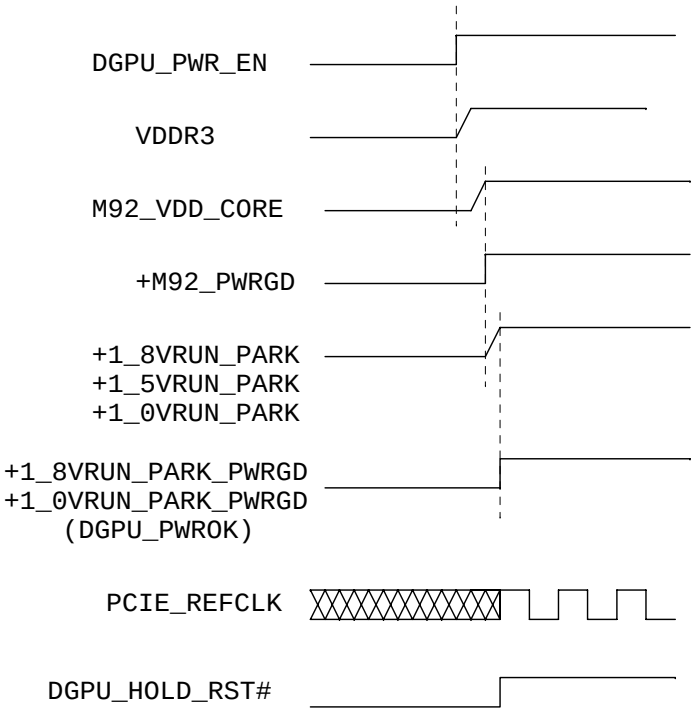
M92 Power on Sequence



PARK Power on Sequence



MICRO-STAR INT'L CO.,LTD.

Title: M92/PARK Power on Sequence

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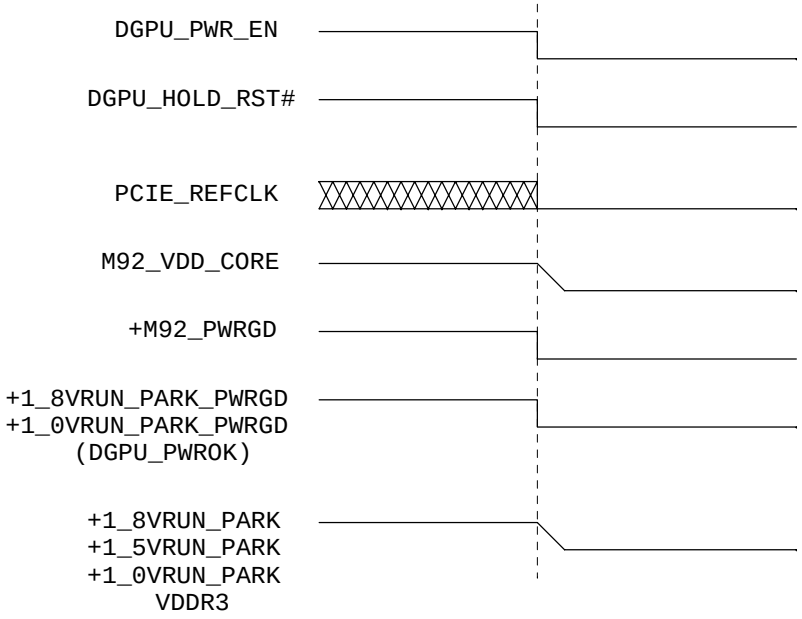
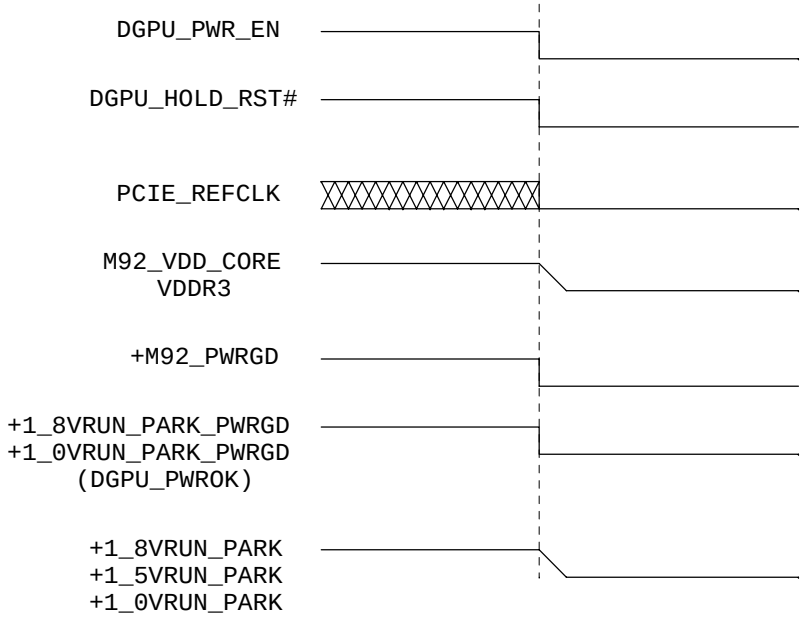
M92 Power down Sequence



PARK Power down Sequence



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Title: M92/PARK Power down Sequence

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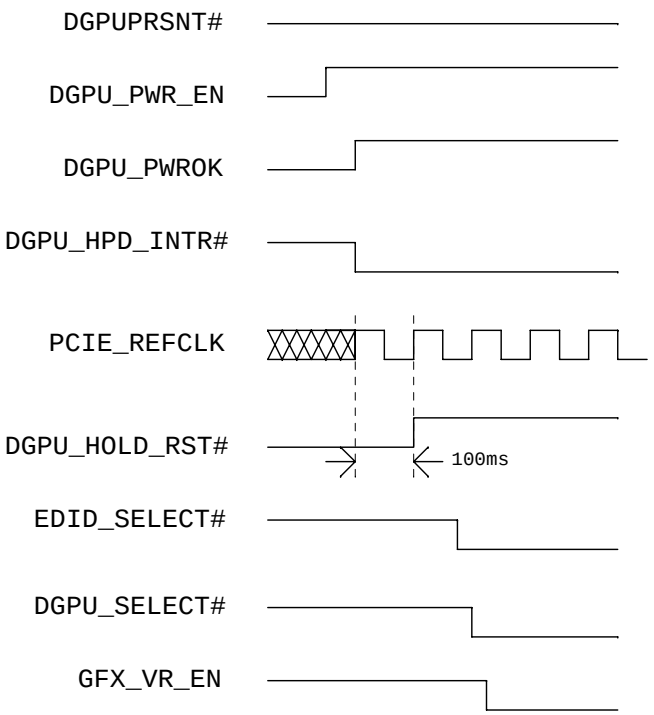
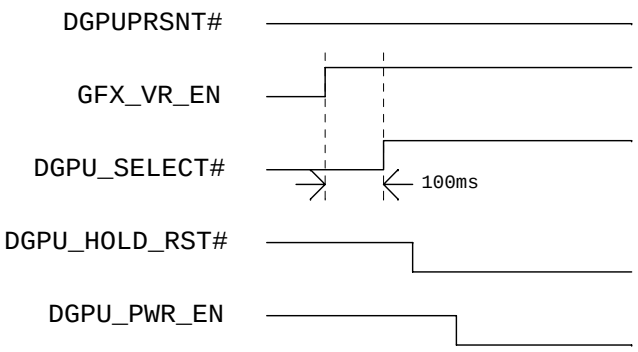
Switchable DGPU Power on Sequence
Discrete Mode



Switchable DGPU Power off Sequence
UMA Mode



MICRO-STAR INT'L CO.,LTD.		
Title: Switchable Power Sequence		
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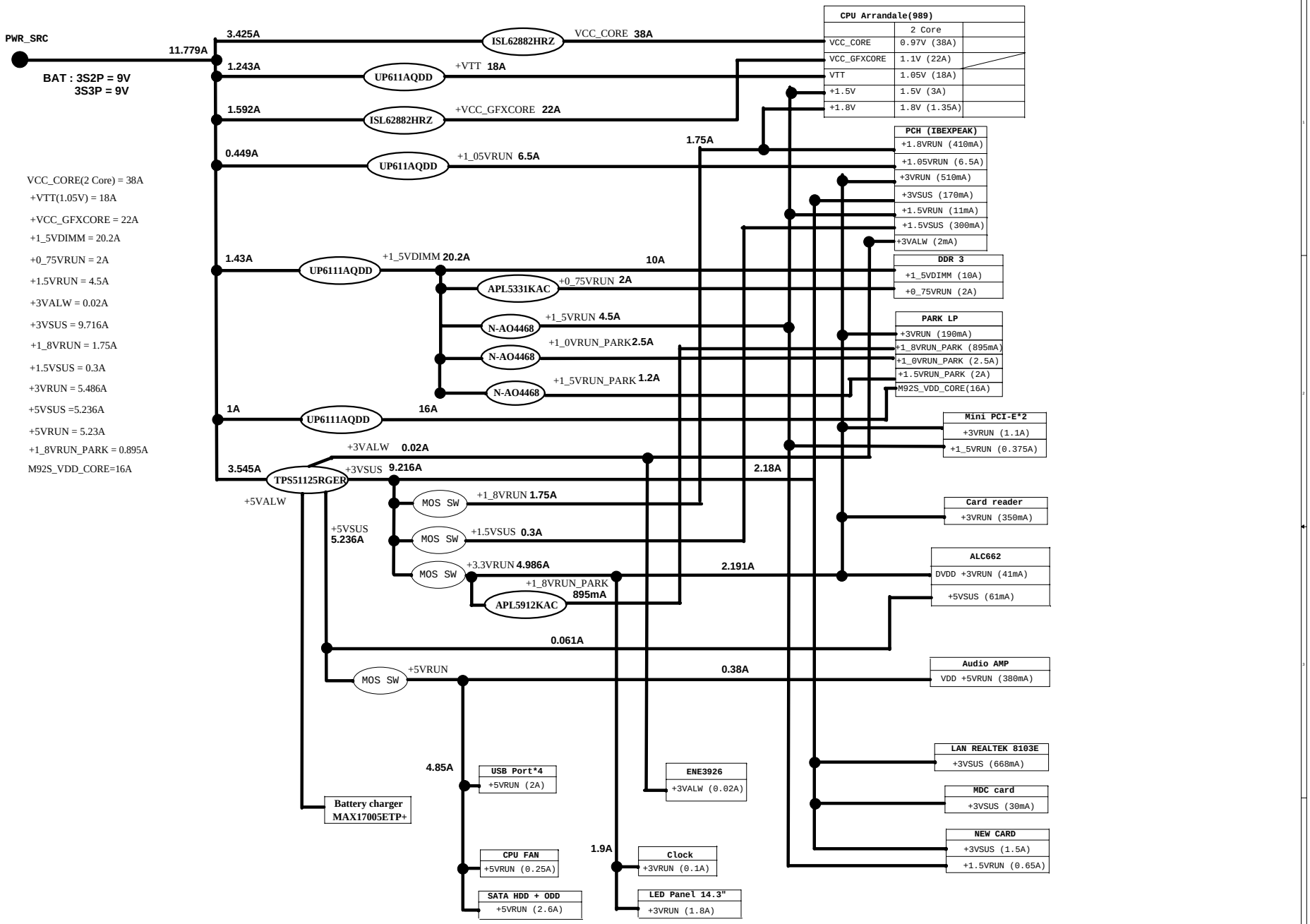

VCC_CORE(2 Core) = 38A
+VTT(1.05V) = 18A
+VCC_GFXCORE = 22A
+1_5VDIMM = 20.2A
+0_75VRUN = 2A
+1.5VRUN = 4.5A
+3VALW = 0.02A
+3VSUS = 9.716A
+1_8VRUN = 1.75A
+1.5VSUS = 0.3A
+3VRUN = 5.486A
+5VSUS =5.236A
+5VRUN = 5.23A
+1_8VRUN_PARK = 0.895A
M92S_VDD_CORE=16A

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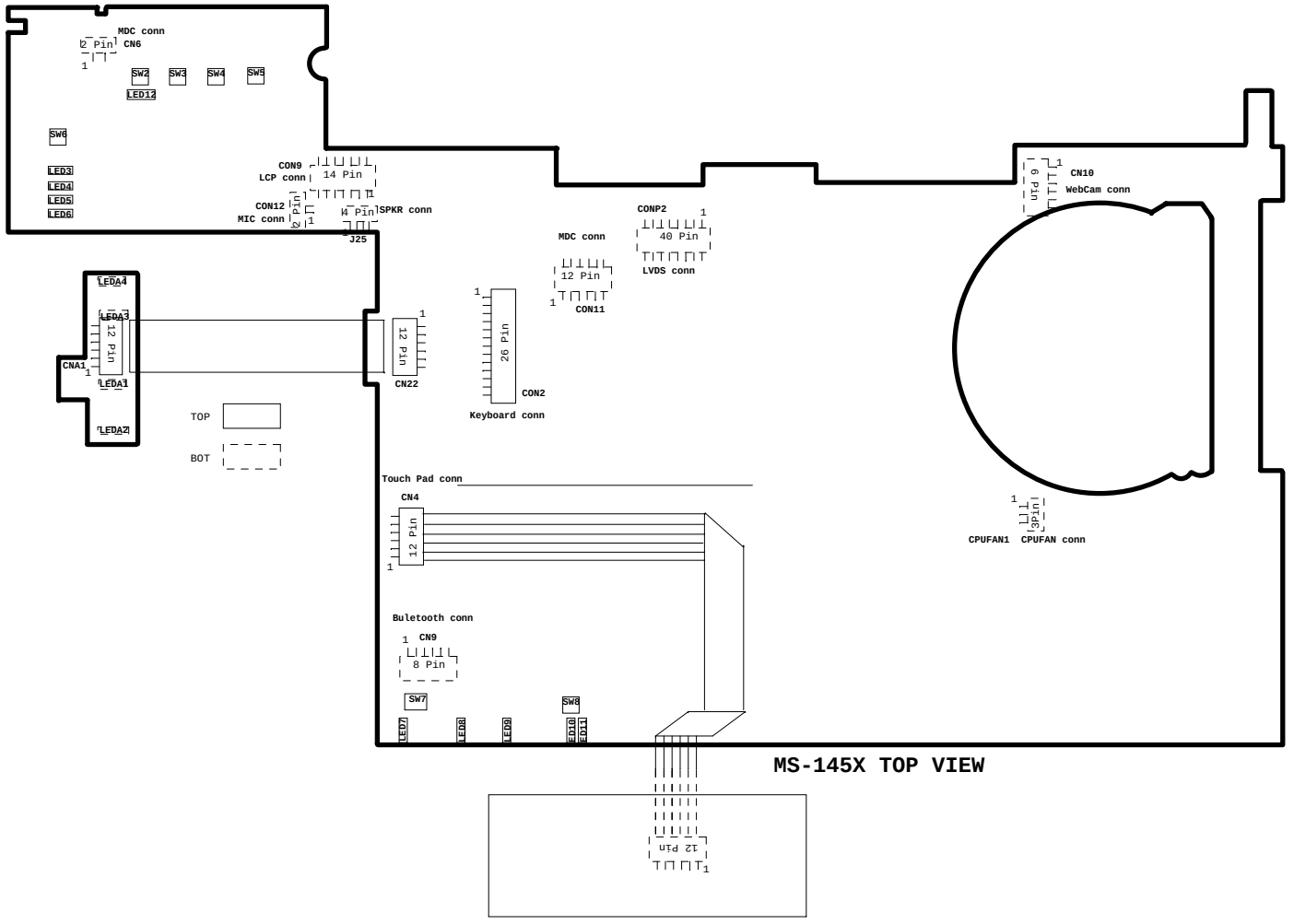
MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyP1_button(FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD LED(FOR OEM)
LED4	NUM_LED(FOR OEM)
LED5	CAP_LED(FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED(FOR OEM)
LEDA2	HDD_LED(FOR OEM)
LEDA3	CAP_LED(FOR OEM)
LEDA4	SCR_LED (FOR OEM)

MS-145X : Main Board
MS-145XA : LED board



MS-145X TOP VIEW

MICRO-STAR INT'L CO.,LTD.

Title: Topology

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2009/06/25 [Page33] Add LED and switch function for OEM reserved

[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix

[Page41/42] Modify APL5912 VCNTL to +5VSUS

[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable

[Page19] Add LVDS common choke by EMI

[Page12] Reserve RGB 10p to GND

[Page38] Reserve BAT CLK and DATA 10p to GND

[Page39] Reserve 10p SDC_IN+ to GND and close to PQ57

Add two X-Copper

[Page40] Reserve 10p +5VSUS to GND and close to PQ60

Reserve 2.2R+2200p

[Page41] Reserve 10p PWR_SRC to GND and close to PQ68

[Page42] Reserve 10p PWR_SRC to GND and close to PQ72

[Page43] Reserve 10p PWR_SRC to GND and close to PQ75 or PQ76

Reserve 10p PWR_SRC to GND and close to PQ78 or PQ79

[Page43] Reserve 10p PWR_SRC to GND and close to PQ81 or PQ82

Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)

Modify PARK circuit

Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature

Modify Audio jack PN to N54-05F0951-H06

Modify internal MIC PN to N32-1020790-A81

Modify power sequence map

2009/07/01 [Page3] R234,R412等0A實驗結果再決定是否移除

BPM#[0~7] remove

BCLK只保留from PCH,移除from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS_NCTF1~7 remove

[Page8] 只保留CFG的測點,其餘移除

[Page9] SA0_DIM0及SA1_DIM0改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page10] SA0_DIM1改爲0 ohm對地

移除330uF,因在CPU以及switching power端已有

[Page12] 補上HPD線路

[Page16] MDA0~MDA7 swap

[Page18] CRT及LVDS的預留電阻(for MS-1454)均改爲單顆的0 ohm

EDID switch的電源pin加上0.1uF

R3238,R3239改爲10K ohm

移除BR-AD-ADJ,BR-PWM-ADJ名稱改爲PWM-ADJ,HDMI DDC名稱改爲HDM_SDA及HDM_SCL

[Page19] 兀型濾波LC值改爲0.1uH+10pF

新增LVDS DDC pull high,backlight adj預留net PWM-ADJ

[Page25] DGPUPRSNT#改接pull down

[Page30] 修改+1_8VRUN_PARK_PWRGD及+1_0VRUN_PARK_PWRGD結合爲DGPU_PWROK

[Page34] C47,C49改爲0.1uF

[Page43] Add three X-copper

MICRO-STAR INT'L CO.,LTD.

Title: History

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