1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J95 MLB SKL

LAST_MODIFICATION=Thu Feb 26 18:38:23 2015

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0003859507	ENGINEERING RELEASED	2015-02-26

DRAWING

TITLE=J95_skl_am
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 26 18:38:23 2015

J95,SCHEM,MLB_SKL_AM

DRAWING TITLE: SCHEM,MLB SKL,J95

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D
REVISION: 4.0.0
BRANCH: proto1b
PAGE: 1 OF 120
SHEET: 1 OF 96

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00041	PCBA,DEV,MLB_SKL,J95	DEVELOPMENT,J95_DEVEL
685-00059	PCBA,MLB_SKL,COMMON PARTS,J95	J95_COMMON
639-00847	PCBA,MLB SKL,AMETHYST PROA,VRAM_HYNIX,2GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_PROA,FB:2G_HYNIX,EEEE:G99J
639-00846	PCBA,MLB SKL,AMETHYST PROA,VRAM_ELPIDA,2GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_PROA,FB:2G_ELPIDA,EEEE:GCP9
639-00849	PCBA,MLB SKL,AMETHYST XTA,VRAM_HYNIX,4GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_XTA,FB:4G_HYNIX,EEEE:GCR6
639-00848	PCBA,MLB SKL,AMETHYST XTA,VRAM_ELPIDA,4GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_XTA,FB:4G_ELPIDA,EEEE:GCR7
639-01033	PCBA,MLB SKL,CTO,AMETHYST PROA,VRAM_HYNIX,2GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_PROA,FB:2G_HYNIX,EEEE:G99J
639-01032	PCBA,MLB SKL,CTO,AMETHYST PROA,VRAM_ELPIDA,2GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_PROA,FB:2G_ELPIDA,EEEE:GCP9
639-01035	PCBA,MLB SKL,CTO,AMETHYST XTA,VRAM_HYNIX,4GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_XTA,FB:4G_HYNIX,EEEE:GCR6
639-01034	PCBA,MLB SKL,CTO,AMETHYST XTA,VRAM_ELPIDA,4GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_XTA,FB:4G_ELPIDA,EEEE:GCR7

BOM Groups

BOM GROUP	BOM OPTIONS
J95_COMMON	COMMON,ALTERNATE,J95_PROGPARTS,GPU_AM_EM,XDP,SPEAKERID,FBVDDQ_OFLT:1V5,SMCREG:SUP,VR_BULKCAP:CURRENT,GPU:AME_NEP
J95_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG
J95_DEVEL	XDP_CONN,T112,DEVEL_AUDIO

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00122	1	CPU,SKL,QHQF,ES2,Q0,2.6,95W,LGA1151	CPU	CRITICAL	CPU:CTO
337S00114	1	CPU,SKL,QH8E,ES,P0,4/2,2.2,95W,LGA1151	CPU	CRITICAL	CPU:ULT
337S00121	1	CPU,SKL,QHQG,ES2,Q0,2.2,65W,LGA1151	CPU	CRITICAL	CPU:BEST

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S00002	1	SOCKET.MOLEX,LGA1151,H4	U0500	CRITICAL	

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00124	1	IC,PCH-H,SKL,SUPRSKU,C0,QHPT,ES2,BGA1151	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00058	1	IC,EFI,V0174,J78	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S00236	1	IC,SMC-B1,EXTERNAL,VXXXX,POC-S,J78AM	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/50DMIPS,MCU,157BGA	U5000	CRITICAL	SMC:BLANK
341S00152	1	IC,T29,EPROM,FR,VTBD,POC,J95	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET ROM,NUMONYX,V1.15,J16/J16G/J17	U3990	CRITICAL	CIVROM:PROG
335S0854	1	1-MBIT,SPI FLASH ROM SOIC, HF	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA FLASH,V7230,J16/J17	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_G99J	CRITICAL	EEEE:G99J
825-7896	1	LABEL,MLB,2D	EEEE_GCP9	CRITICAL	EEEE:GCP9
825-7896	1	LABEL,MLB,2D	EEEE_GCR6	CRITICAL	EEEE:GCR6
825-7896	1	LABEL,MLB,2D	EEEE_GCR7	CRITICAL	EEEE:GCR7

J95 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-00321	1	SCH,MLB SKL,J95	SCH1	CRITICAL	J95
820-00134	1	PCBF,MLB SKL,J95	PCB1	CRITICAL	J95
685-00059	1	PCBA,MLB SKL COMMON PARTS,J95	CMNPTS	CRITICAL	MLB_CMNPTS

J95 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diode Array
197S0481	197S0480		ALL	25MHX PCH XTAL
197S0479	197S0478		ALL	12MHZ CAM/NXP XTAL
372S0186	372S0185		ALL	Alternate Temp Diode
107S00030	107S00029		ALL	Alt 5mOhm sense
107S0255	107S0240		ALL	Alt 1mOhm sense
341S00016	341S3912		U3990	IC,ENETROM,ADESTO,V1,15,J78
138S0681	138S0638		ALL	10uF Caps
138S0860	138S0775		ALL	Single-source 1uF 402
128S0398	128S0220		ALL	3.3V INPUT CAP
378S0391	378S0390		ALL	DEGUG LEDS
311S00008	311S0271		ALL	AND GATE
155S0830	155S0316		ALL	FERR BD,600 OHM,25,0.5A
376S00016	376S0644		ALL	MOSFET,P-CH,20V,1A
376S00001	376S0659		ALL	MOSFET,P-CH,20V
376S00015	376S0610		ALL	XSTR,FET,DL NCH,60V
138S1103	138S0719		ALL	4.7uF 0402
311S00004	311S0370		ALL	Config. Logic Gate
311S00075	311S0377		ALL	AND GATE
132S0447	132S0448		ALL	0.1uF 0201
138S0855	138S0750		ALL	4.7uF 0402
353S00095	353S3328		ALL	2:4 Diff MUX
311S00072	311S0657		ALL	Dual 2 INP AND GATE

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00081	1	IC,GPU,AMD,PS,AMST,XTA,ES,256B,BGA1737	U8700	CRITICAL	GPU:AM_XTA
337S00082	1	IC,GPU,AMD,PS,AMST,PROA,ES,256B,BGA1737	U8700	CRITICAL	GPU:AM_PROA
333S00027	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300,U9350	CRITICAL	FB:4G_HYNIX
333S00027	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500,U9550	CRITICAL	FB:4G_HYNIX
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300,U9350	CRITICAL	FB:4G_ELPIDA
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500,U9550	CRITICAL	FB:4G_ELPIDA
333S0734	4	IC,GDDR5,2GBIT,64MX32,6GBPS,29NM	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_HYNIX
333S0734	4	IC,GDDR5,2GBIT,64MX32,6GBPS,29NM	U9400,U9450,U9500,U9550	CRITICAL	FB:2G_HYNIX
333S0701	4	IC,GDDR5,2GBIT,64MX32,6GBPS,38NM	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_ELPIDA
333S0701	4	IC,GDDR5,2GBIT,64MX32,6GBPS,38NM	U9400,U9450,U9500,U9550	CRITICAL	FB:2G_ELPIDA

SYNC_MASTER=J17_DINI SYNC_DATE=03/15/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

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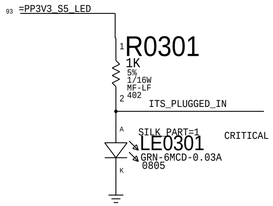
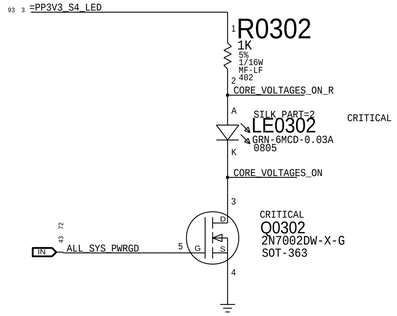
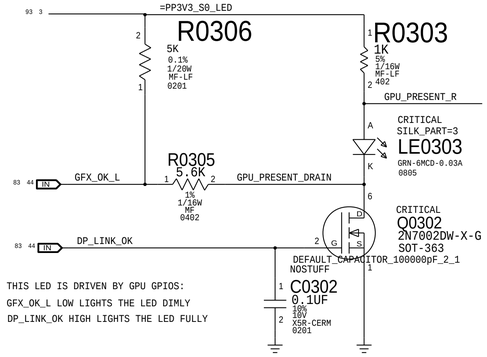
S5 Led



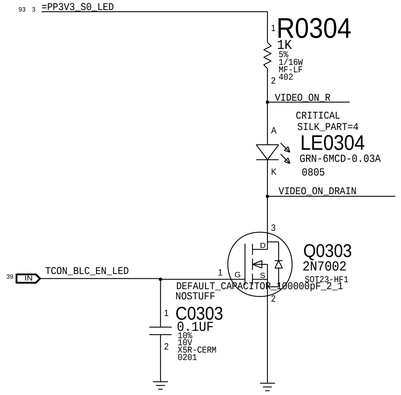
ALL_SYS_PWRGD Led



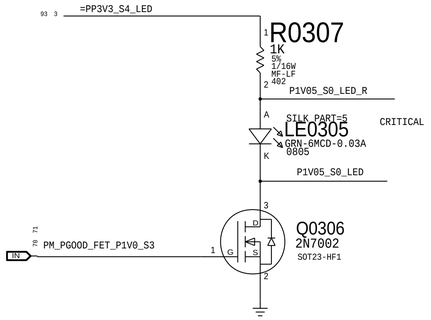
GPU GOOD Led



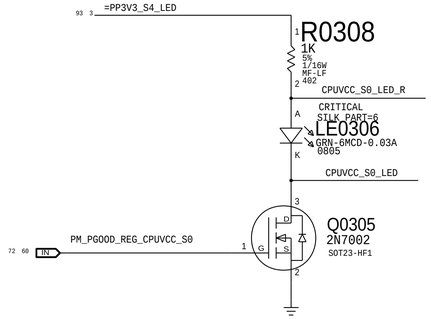
VIDEO ON Led



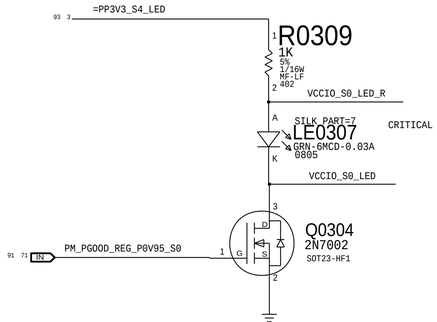
P1V0_S3_PWRGD Led



CPUVCC_S0_PWRGD Led



VCCIO_S0_PWRGD Led



SYNC_MASTER=J17_MAX SYNC_DATE=02/11/2013

PAGE TITLE

DEBUG: LEDs

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

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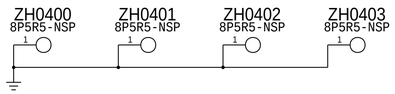
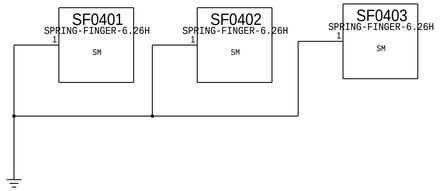
CPU Heatsink

4MM PLATED HOLES (998-4158)



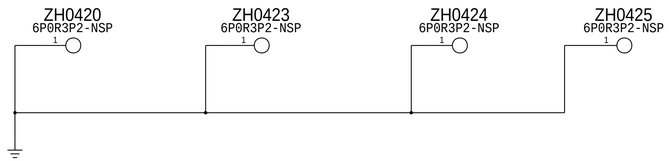
Display EMI Springs

APN: 870-00886



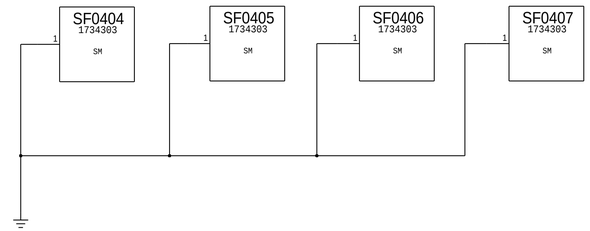
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



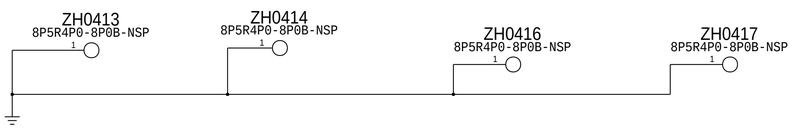
VRAM EMI Springs

APN: 870-00907



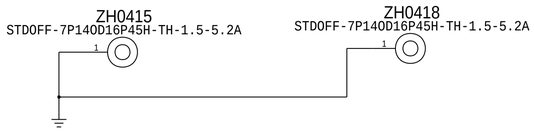
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



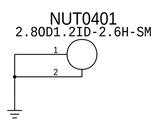
Rear Cover

860-5674 (PCB STANDOFF)



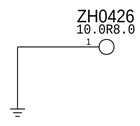
T29 BUMPER

APN: 860-00201



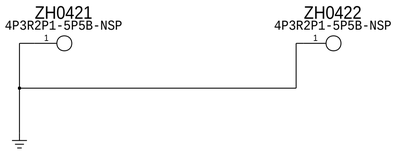
HEATPIPE MTG HOLES

998-5527 (PLATED HOLES, 8MM DIA, 10MM PAD)



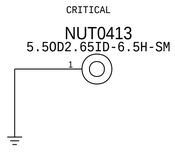
X238D WIRELESS CARD MTG HOLES

998-01489 (PLATED HOLES, 2.1MM INNER DIAMETER, 5.5MM PAD)



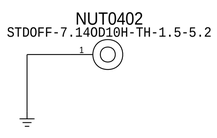
SSD STANDOFF

APN: 860-00198



LOL Boss

860-5675 (PLATED HOLE, 8.41mm pad Top, 8mm pad Bot)



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PAGE TITLE
MECHANICAL: Holes/PD parts

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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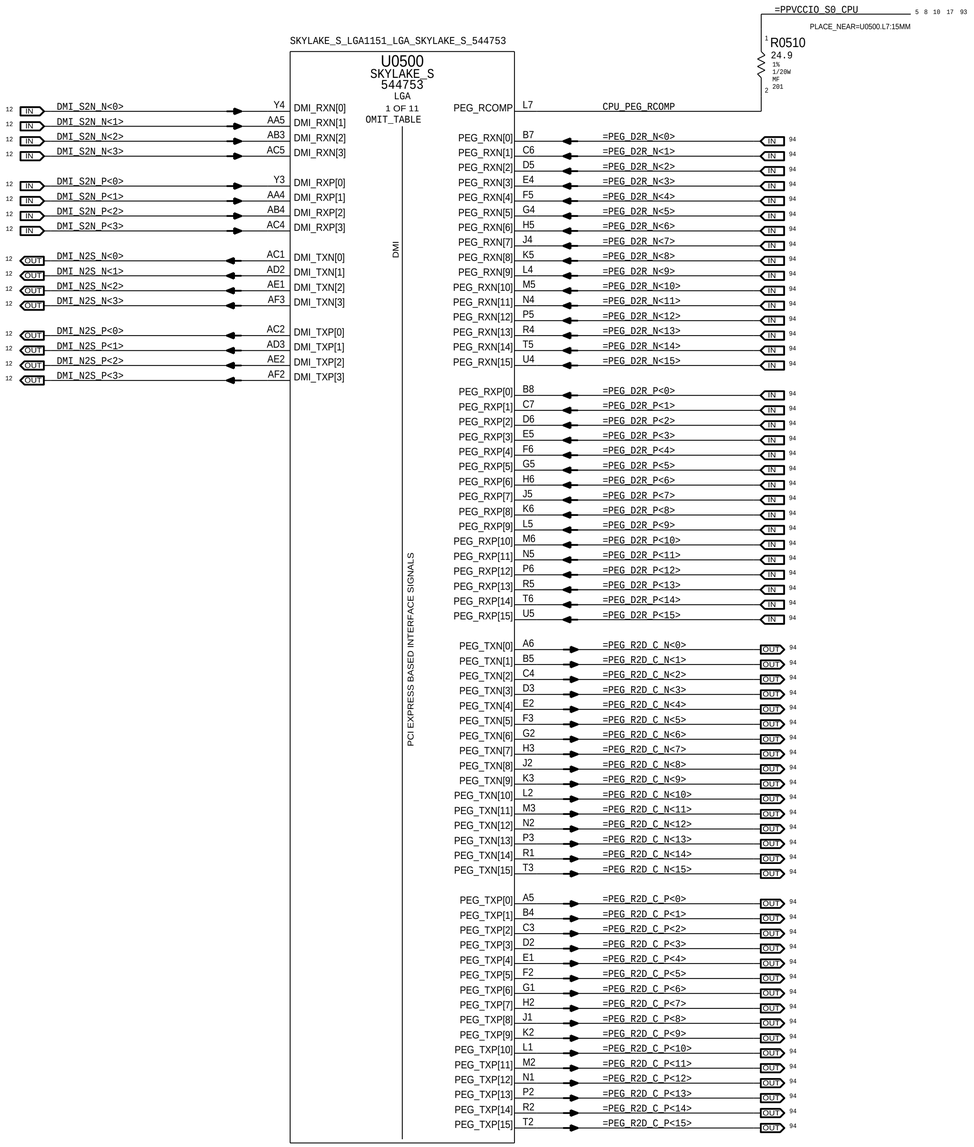

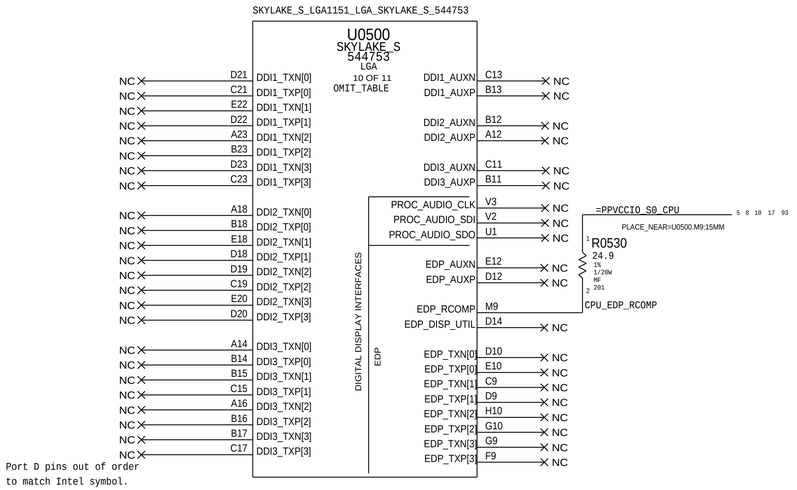

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Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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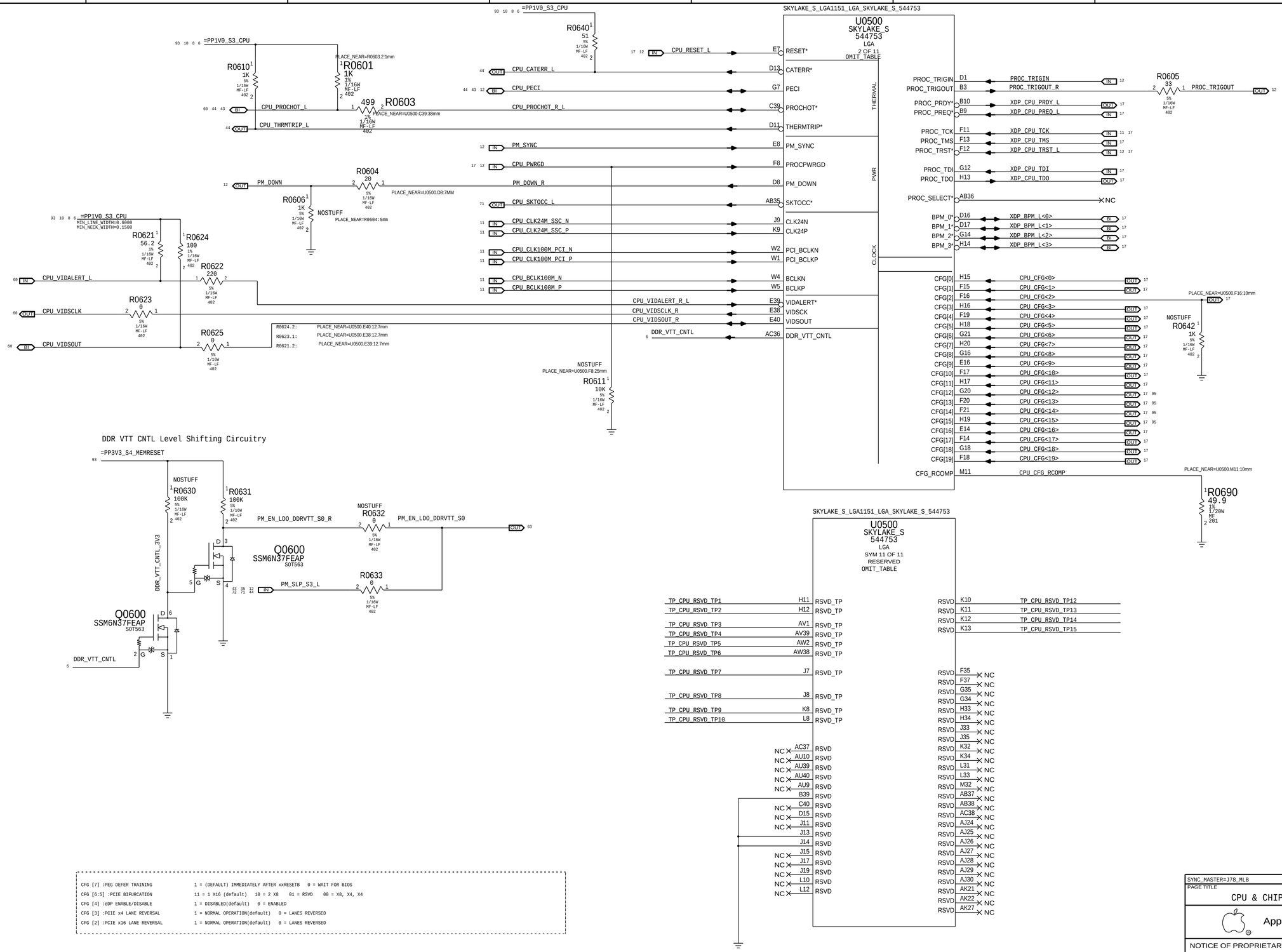
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R0610 1K
R0601 1K
R0603 499
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PLACE_NEAR=U0500.C39:38mm
CPU_PROCHOT_L
CPU_THRMTRIP_L
CPU_PROCHOT_R_L
CPU_RESET_L
CPU_CATERR_L
CPU_PECI
PM_SYNC
CPU_PWRGD
PM_DOWN
PM_DOWN_R
CPU_SKTOCC_L
CPU_CLK24M_SSC_N
CPU_CLK24M_SSC_P
CPU_CLK100M_PCI_N
CPU_CLK100M_PCI_P
CPU_BCLK100M_N
CPU_BCLK100M_P
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R0606 1K
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PLACE_NEAR=U0500.D8:7MM
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R0624 100
R0622 220
R0623 0
R0625 0
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MIN_NECK_WIDTH=0.1500
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
R0624.2: PLACE_NEAR=U0500.E40:12.7mm
R0623.1: PLACE_NEAR=U0500.E38:12.7mm
R0621.2: PLACE_NEAR=U0500.E39:12.7mm
DDR_VTT_CNTL
R0611 10K
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SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753
U0500
SKYLAKE_S
544753
LGA
2 OF 11
OMIT_TABLE
THERMAL
PWR
CLOCK
RESET*
CATERR*
PECI
PROCHOT*
THERMTRIP*
PM_SYNC
PROCPWRGD
PM_DOWN
SKTOCC*
CLK24N
CLK24P
PCI_BCLKN
PCI_BCLKP
BCLKN
BCLKP
VIDALERT*
VIDSCK
VIDSOUT
DDR_VTT_CNTL
PROC_TRIGIN
PROC_TRIGOUT
PROC_PRDY*
PROC_PREQ*
PROC_TCK
PROC_TMS
PROC_TRST*
PROC_TDI
PROC_TDO
PROC_SELECT*
BPM_0*
BPM_1*
BPM_2*
BPM_3*
R0605 33
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XDP_CPU_PREQ_L
XDP_CPU_TCK
XDP_CPU_TMS
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TDO
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PLACE_NEAR=U0500.M11:10mm
R0690 49.9
DDR VTT CNTL Level Shifting Circuitry
=PP3V3_S4_MEMRESET
R0630 100K
R0631 100K
R0632 0
R0633 0
Q0600
SSM6N37FEAP
SOT563
DDR_VTT_CNTL_3V3
PM_EN_LDO_DDRVTT_S0_R
PM_EN_LDO_DDRVTT_S0
PM_SLP_S3_L
TP_CPU_RSVD_TP1
TP_CPU_RSVD_TP2
TP_CPU_RSVD_TP3
TP_CPU_RSVD_TP4
TP_CPU_RSVD_TP5
TP_CPU_RSVD_TP6
TP_CPU_RSVD_TP7
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TP_CPU_RSVD_TP10
TP_CPU_RSVD_TP12
TP_CPU_RSVD_TP13
TP_CPU_RSVD_TP14
TP_CPU_RSVD_TP15
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (default) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eOP ENABLE/DISABLE 1 = DISABLED(default) 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION(default) 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION(default) 0 = LANES REVERSED
SYNC_MASTER=J78_MLB
SYNC_DATE=06/30/2014
PAGE TITLE
CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 6 OF 120
SHEET 6 OF 96
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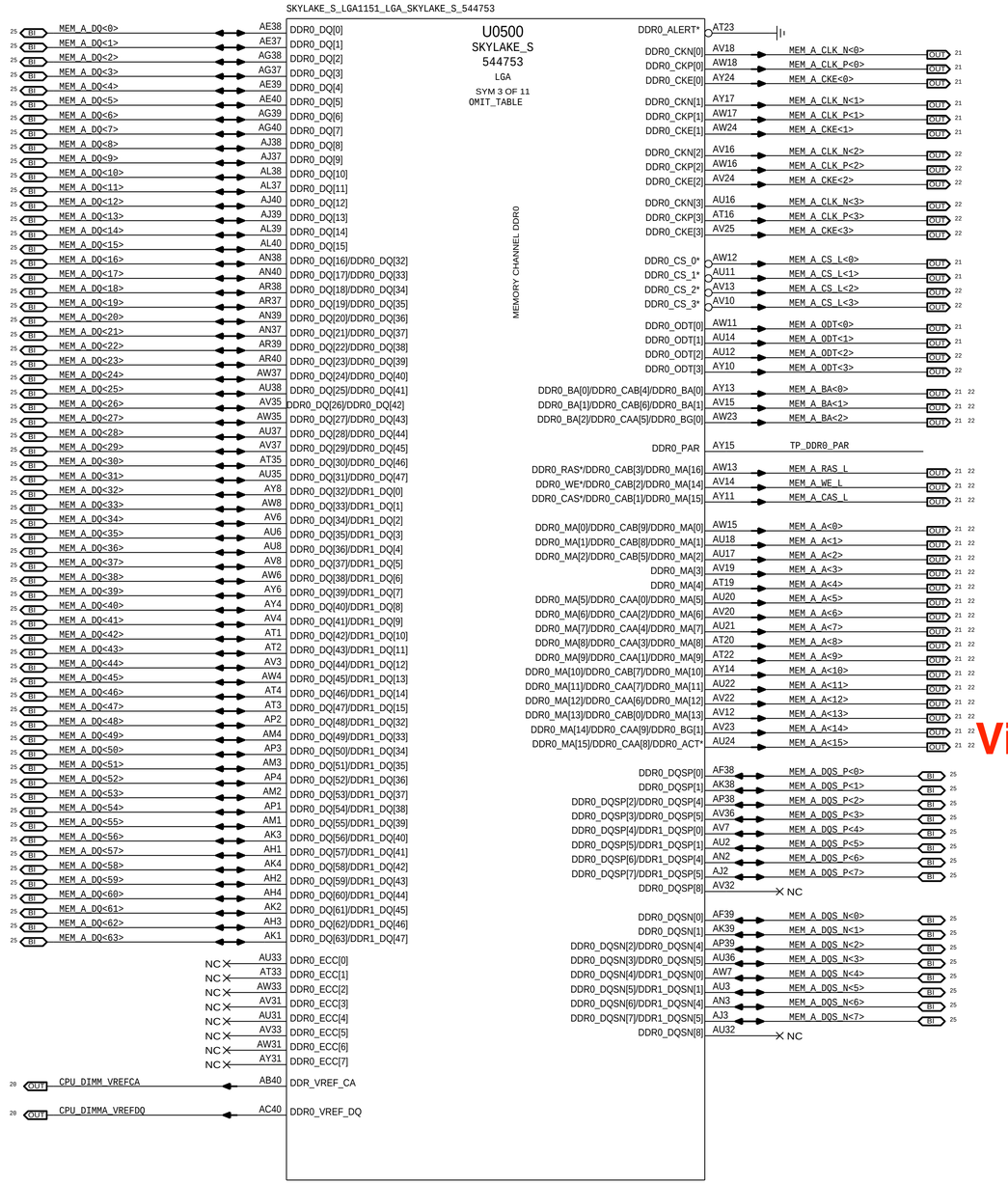

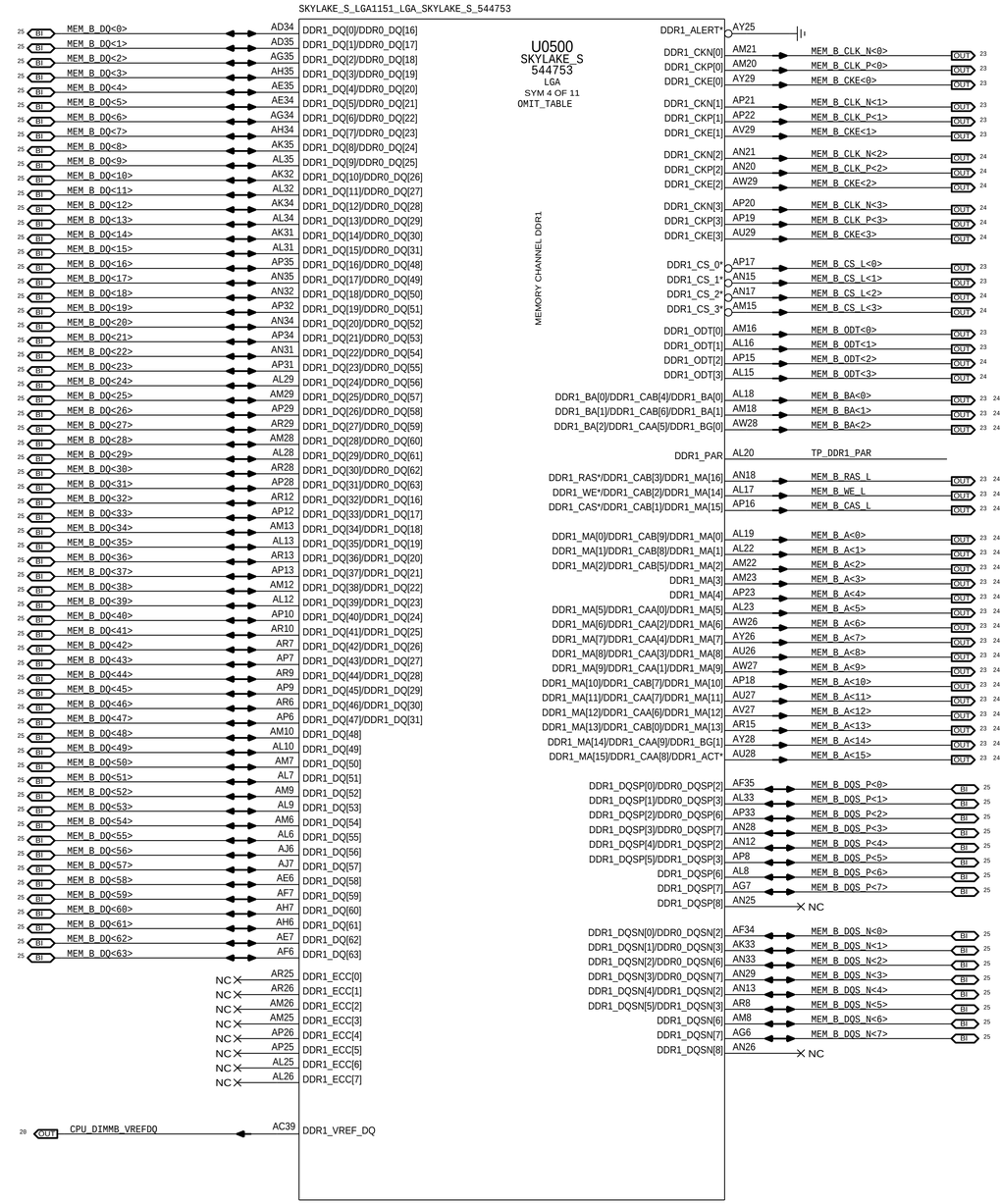

Vinafix

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: DDR3L Interfaces

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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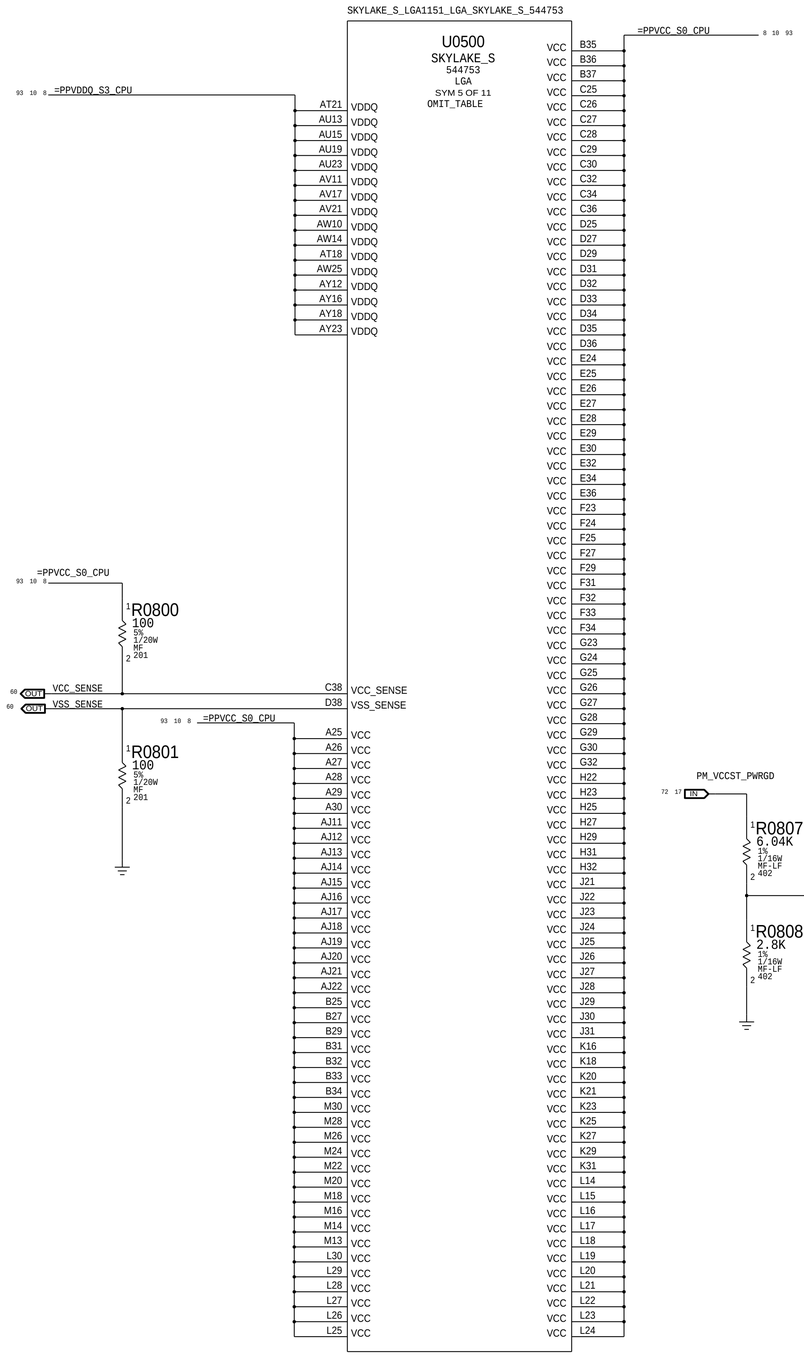
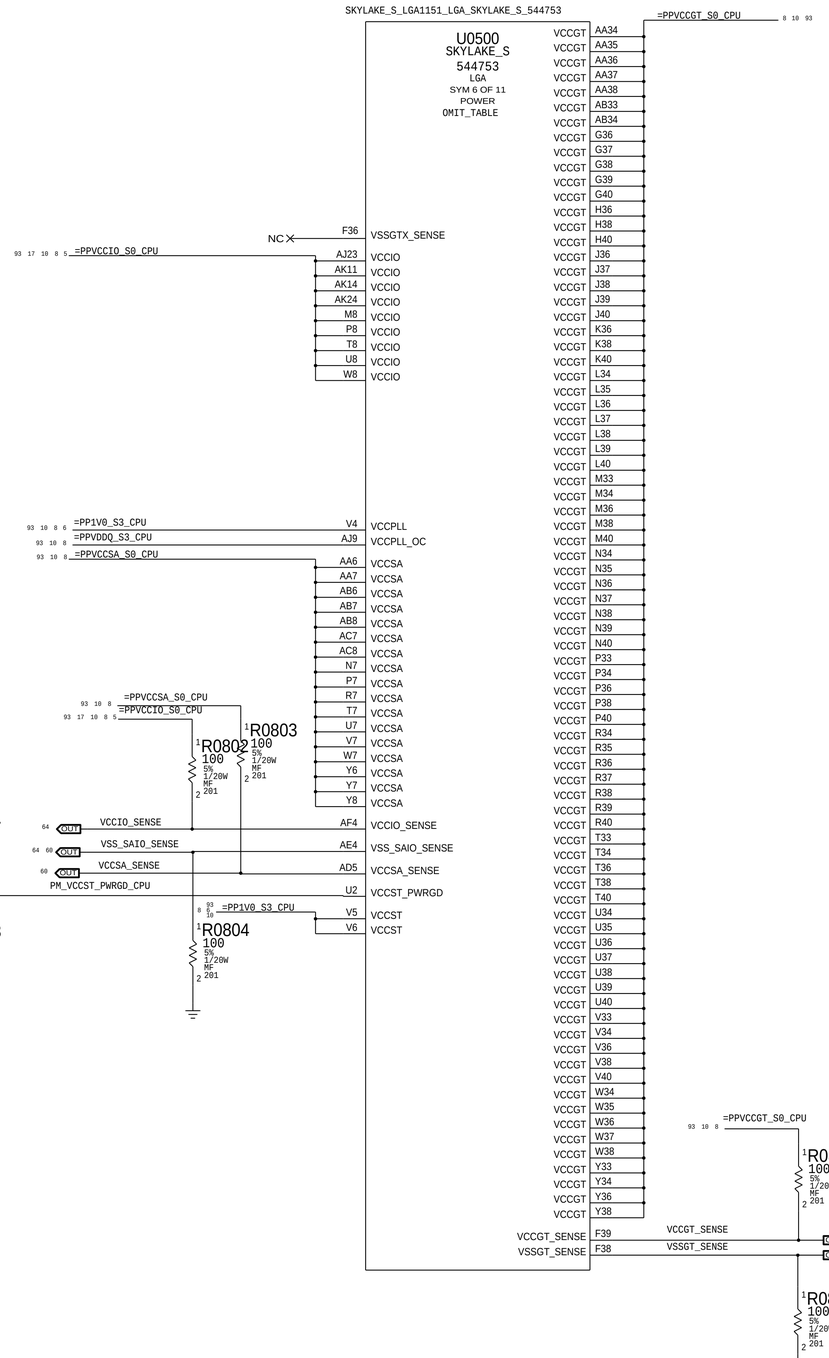
SHEET 7 OF 96





SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU Power

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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SHEET 8 OF 96

SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 7 OF 11
GROUND
OMIT_TABLE

A7	VSS	VSS	AJ35
A11	VSS	VSS	AJ36
A13	VSS	VSS	AK5
A15	VSS	VSS	AK6
A17	VSS	VSS	AK7
A24	VSS	VSS	AK8
AA3	VSS	VSS	AK9
AA8	VSS	VSS	AK10
AA33	VSS	VSS	AK12
AB5	VSS	VSS	AK13
AB39	VSS	VSS	AK15
AC3	VSS	VSS	AK16
AC6	VSS	VSS	AK17
AC33	VSS	VSS	AK18
AC34	VSS	VSS	AK19
AC35	VSS	VSS	AK20
AD1	VSS	VSS	AK23
AD4	VSS	VSS	AK25
AD6	VSS	VSS	AK26
AD7	VSS	VSS	AK28
AD8	VSS	VSS	AK29
AD33	VSS	VSS	AK30
AD36	VSS	VSS	AK36
AD37	VSS	VSS	AK37
AD38	VSS	VSS	AK40
AD39	VSS	VSS	AL1
AD40	VSS	VSS	AL2
AE3	VSS	VSS	AL3
AE5	VSS	VSS	AL4
AE8	VSS	VSS	AL5
AE33	VSS	VSS	AL11
AE36	VSS	VSS	AL14
AF1	VSS	VSS	AL21
AF5	VSS	VSS	AL24
AF8	VSS	VSS	AL27
AF33	VSS	VSS	AL30
AF36	VSS	VSS	AL36
AF37	VSS	VSS	AM5
AF40	VSS	VSS	AM11
AG1	VSS	VSS	AM14
AG2	VSS	VSS	AM17
AG3	VSS	VSS	AM19
AG4	VSS	VSS	AM24
AG5	VSS	VSS	AM27
AG8	VSS	VSS	AM30
AG33	VSS	VSS	AM31
AG36	VSS	VSS	AM32
AH5	VSS	VSS	AM33
AH8	VSS	VSS	AM34
AH33	VSS	VSS	AM35
AH36	VSS	VSS	AM36
AH37	VSS	VSS	AM37
AH38	VSS	VSS	AM38
AH39	VSS	VSS	AM39
AH40	VSS	VSS	AM40
AJ1	VSS	VSS	AN1
AJ4	VSS	VSS	AN4
AJ5	VSS	VSS	AN5
AJ8	VSS	VSS	AN6
AJ31	VSS	VSS	AN7
AJ32	VSS	VSS	AN8
AJ33	VSS	VSS	AN9
AJ34	VSS	VSS	AN10

SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 8 OF 11
GROUND
OMIT_TABLE

AN11	VSS	VSS	AT32
AN14	VSS	VSS	AT34
AN16	VSS	VSS	AT36
AN19	VSS	VSS	AT37
AN22	VSS	VSS	AT38
AN23	VSS	VSS	AT39
AN24	VSS	VSS	AT40
AN27	VSS	VSS	AU1
AN30	VSS	VSS	AU4
AN36	VSS	VSS	AU5
AP5	VSS	VSS	AU7
AP11	VSS	VSS	AU25
AP14	VSS	VSS	AU30
AP24	VSS	VSS	AU34
AP27	VSS	VSS	AV2
AP30	VSS	VSS	AV5
AP36	VSS	VSS	AV9
AP37	VSS	VSS	AV26
AP40	VSS	VSS	AV28
AR1	VSS	VSS	AV30
AR2	VSS	VSS	AV34
AR3	VSS	VSS	AV38
AR4	VSS	VSS	AW3
AR5	VSS	VSS	AW5
AR11	VSS	VSS	AW9
AR14	VSS	VSS	AW30
AR16	VSS	VSS	AW32
AR17	VSS	VSS	AW34
AR18	VSS	VSS	AW36
AR19	VSS	VSS	AY5
AR20	VSS	VSS	AY7
AR21	VSS	VSS	AY9
AR22	VSS	VSS	AY27
AR23	VSS	VSS	AY30
AR24	VSS	VSS	B6
AR27	VSS	VSS	B24
AR30	VSS	VSS	B26
AR31	VSS	VSS	B28
AR32	VSS	VSS	B30
AR33	VSS	VSS	C5
AR34	VSS	VSS	C8
AR35	VSS	VSS	C10
AR36	VSS	VSS	C12
AT5	VSS	VSS	C14
AT6	VSS	VSS	C16
AT7	VSS	VSS	C18
AT8	VSS	VSS	C20
AT9	VSS	VSS	C22
AT10	VSS	VSS	C24
AT11	VSS	VSS	C31
AT12	VSS	VSS	C33
AT13	VSS	VSS	C35
AT14	VSS	VSS	C37
AT15	VSS	VSS	D4
AT17	VSS	VSS	D7
AT24	VSS	VSS	D24
AT25	VSS	VSS	D26
AT26	VSS	VSS	D28
AT27	VSS	VSS	D30
AT28	VSS	VSS	D37
AT29	VSS	VSS	D39
AT30	VSS	VSS	E3
AT31	VSS	VSS	E6

SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 9 OF 11
GROUND
OMIT_TABLE

E9	VSS	VSS	K30
E11	VSS	VSS	K33
E13	VSS	VSS	K35
E15	VSS	VSS	K37
E17	VSS	VSS	K39
E19	VSS	VSS	L3
E21	VSS	VSS	L6
E23	VSS	VSS	L9
E31	VSS	VSS	L11
E33	VSS	VSS	L13
E35	VSS	VSS	L32
E37	VSS	VSS	M1
F1	VSS	VSS	M4
F4	VSS	VSS	M7
F7	VSS	VSS	M10
F10	VSS	VSS	M12
F22	VSS	VSS	M15
F26	VSS	VSS	M17
F28	VSS	VSS	M19
F30	VSS	VSS	M21
F40	VSS	VSS	M23
G3	VSS	VSS	M25
G6	VSS	VSS	M27
G11	VSS	VSS	M29
G13	VSS	VSS	M35
G15	VSS	VSS	M37
G17	VSS	VSS	M39
G19	VSS	VSS	N3
G22	VSS	VSS	N6
G31	VSS	VSS	N8
G33	VSS	VSS	N33
H1	VSS	VSS	P1
H4	VSS	VSS	P4
H7	VSS	VSS	P35
H9	VSS	VSS	P37
H21	VSS	VSS	P39
H24	VSS	VSS	R3
H26	VSS	VSS	R6
H28	VSS	VSS	R8
H30	VSS	VSS	R33
H35	VSS	VSS	T1
H37	VSS	VSS	T4
H39	VSS	VSS	T35
J3	VSS	VSS	T37
J6	VSS	VSS	T39
J10	VSS	VSS	U3
J12	VSS	VSS	U6
J16	VSS	VSS	U33
J18	VSS	VSS	V1
J20	VSS	VSS	V8
J32	VSS	VSS	V35
J34	VSS	VSS	V37
K1	VSS	VSS	V39
K4	VSS	VSS	W3
K7	VSS	VSS	W6
K14	VSS	VSS	W33
K15	VSS	VSS	Y5
K17	VSS	VSS	Y35
K19	VSS	VSS	Y37
K22	VSS	VSS	G8
K24	VSS	VSS	H8
K26	VSS	VSS	AY3
K28	VSS		
		VSS_NCTF	A4
		VSS_NCTF	B38
		VSS_NCTF	C2
		VSS_NCTF	D40

SYNC_MASTER=J78_MLB

SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU Ground

Apple Inc.

DRAWING NUMBER: 051-00321

SIZE: D

REVISION: 4.0.0

BRANCH: proto1b

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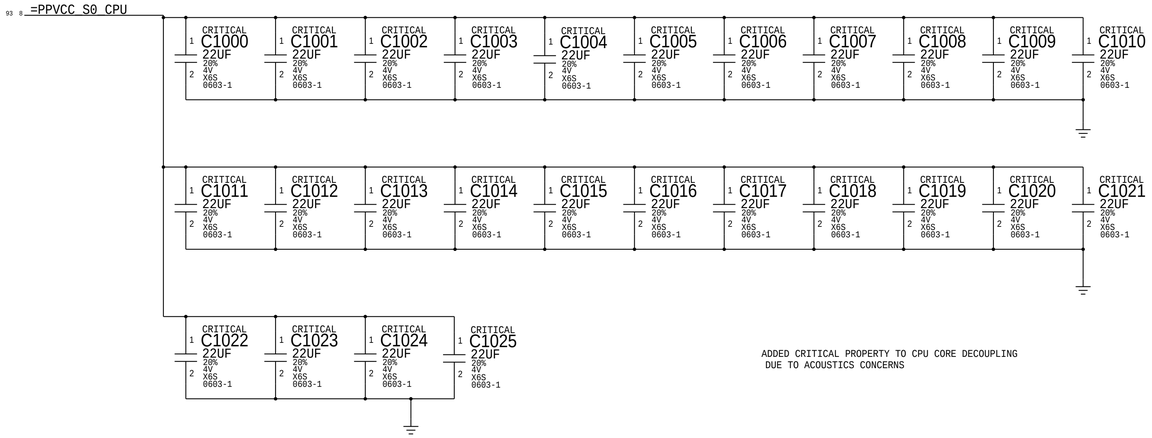
SHEET: 9 OF 96

CPU VCORE DECOUPLING

Intel Recommendation:12x 22UF 0805 (top side cavity)
6x 22UF 0603 (top side cavity)
5x 22UF 0805 (top side outside cavity)

Apple Implementation:26x 22UF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71



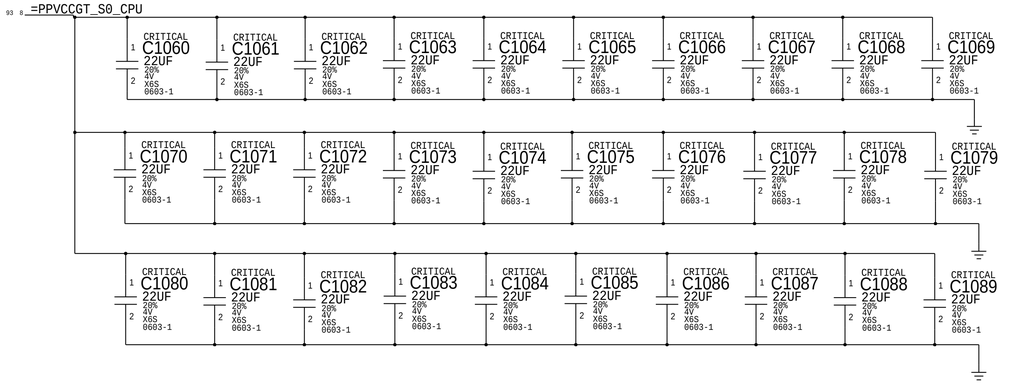
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

Intel Recommendation:9x 47UF 0805 (top side cavity)
4x 47UF 0805 (top side outside cavity)

Apple Implementation: 30x 22uF 0603

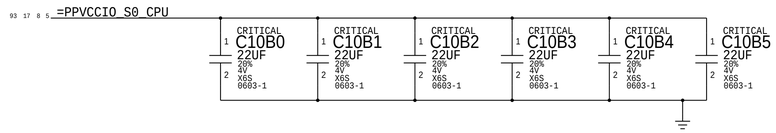
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:5x 22UF 0603 (top side cavity)
1x 22UF 0805 (top side cavity)

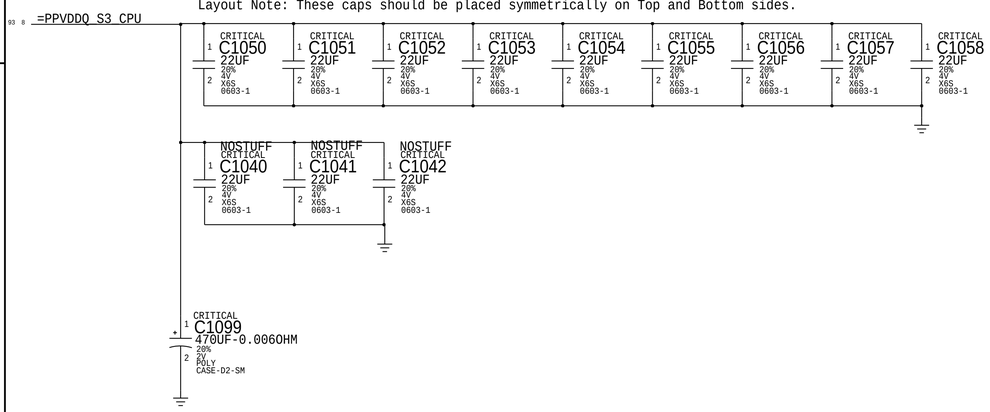
Apple Implementation:(following Intel recommendation w/ 0603)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:4x 22UF 0603 (top side outside cavity)

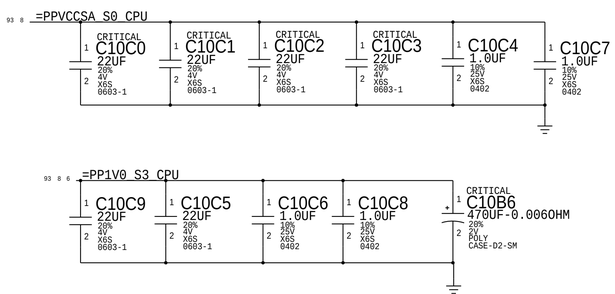
Apple Implementation:9x 22UF 0603 (J78 carry over)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCSA / VCCST+VCCPLL DECOUPLING

Intel Recommendation:2x 22UF 0603 near top side cavity

Apple Implementation: VCCST/VCCPLL: 1X 22UF 0603/2X 1UF 0402
Layout Note: These caps should be placed on top side cavity.



SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE
CPU & CHIPSET: CPU Decoupling

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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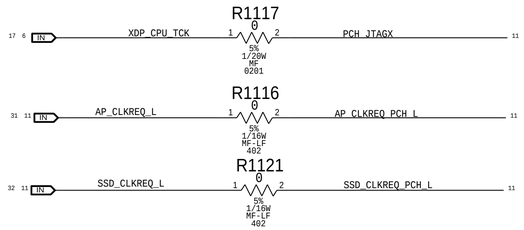
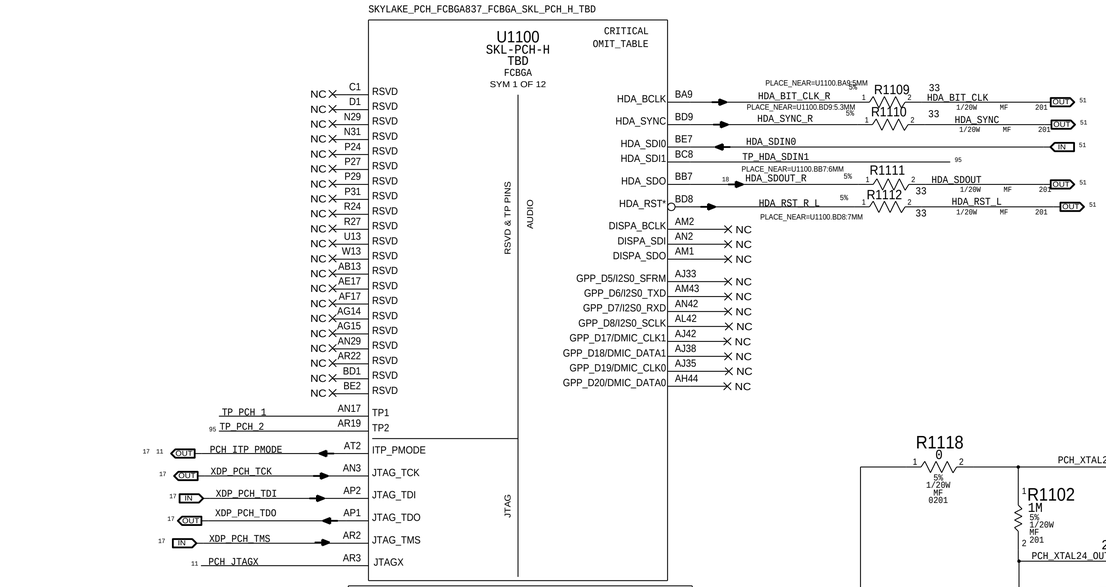
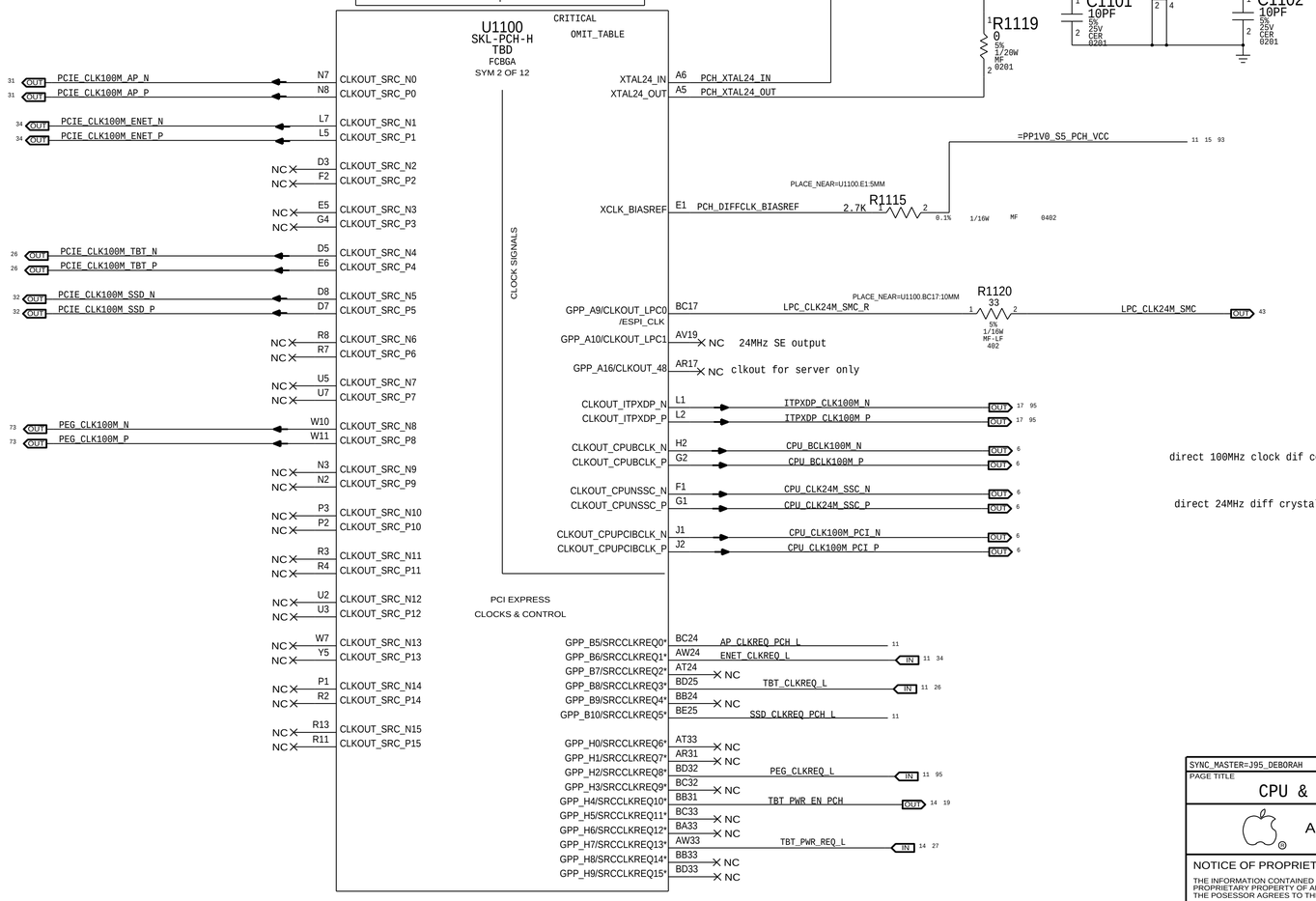
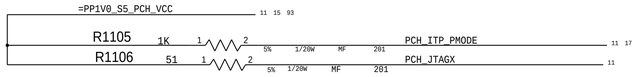


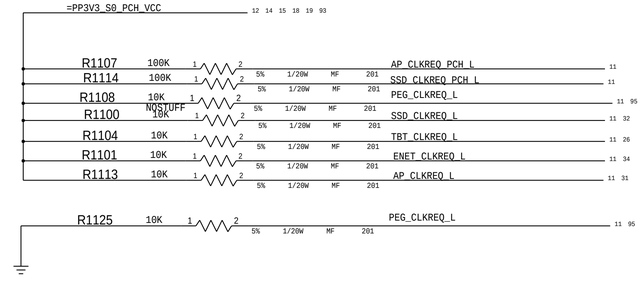




direct 100MHz clock dif core ref clock from PCH to processor

direct 24MHz diff crystal ref clock from PCH to processor





SYNC_MASTER=J95_DEBORAH	SYNC_DATE=10/20/2014
PAGE TITLE	CPU & CHIPSET: Clocks/HDA/JTAG
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

CRITICAL

U1100
SKL-PCH-H
TBD
FCBGA
SYM 3 OF 12

OMIT_TABLE

SPI

SPI_CLK_R	BC31	SPI0_CLK	
SPI_CS0_R_L	BD31	SPI0_CS0*	
NC	AW31	SPI0_CS1*	
NC	AT31	SPI0_CS2*	
SPI_MOSI_R	BB29	SPI0_MOSI	
SPI_MISO	BE30	SPI0_MISO	
SPI_IO_R<2>	BC29	SPI0_IO2	
SPI_IO_R<3>	BD30	SPI0_IO3	

GSPI

GPP_B15/GSPI0_CS*	AR24	NC
GPP_B16/GSPI0_CLK	AW27	NC
GPP_B17/GSPI0_MISO	BD27	NC
GPP_B18/GSPI0_MOSI	BD28	PCH_STRP_NOREBOOT
GPP_B19/GSPI1_CS*	BC27	NC
GPP_B20/GSPI1_CLK	AV29	NC
GPP_B21/GSPI1_MISO	AR29	NC
GPP_B22/GSPI1_MOSI	AT29	PCH_STRP_BOOT_LPC

C-LINK

CL_CLK	AV2	TP_CLINK_CLK
CL_DATA	AV3	TP_CLINK_DATA
CL_RST*	AW2	TP_CLINK_RESET_L

=PP3V3_G3_PCH_RTC

R1200 1M 5% 1/20W MF 201
R1201 20K 5% 1/20W MF 201
R1202 20K 5% 1/20W MF 201

PCH_SRTCRST_L
PCH_INTRUDER_L
RTC_RESET_L

C1200 1UF 10% 10V X5R 402
C1201 1UF 10% 10V X5R 402

=PP3V3_S0_PCH_VCC

R1230	10K	LPC_SERIRQ	
R1234	10K	PCH_RCIN_TERM	
R1204	10K	PCH_STRP_BOOT_LPC	
NOSTUFF			

=PP3V3_S5_PCH_VCC

R1203	1K	PCH_STRP_NOREBOOT
R1236	8.2K	LPC_CLKRUN_L
R1233	10K	PCH_PME_L
R1231	10K	PM_ACPRESENT
R1210	1K	PCIE_WAKE_L
R1211	3.0K	PM_PWRBTN_L
R1232	10K	PCH_BATLOW_L
R1235	10K	PCH_VRALERT_L
R1290	100K	TP_PCH_GPP_A12
NOSTUFF		

R1237	100K	PCH_STRP_GPP_B23	
R1206	1K	PCH_PECI	
R1212	100K	PM_SLP_S3_L	
R1213	100K	PM_SLP_S4_L	
R1214	100K	PM_SLP_S5_L	
R1215	100K	PM_SLP_SUS_L	
NOSTUFF			

R1286 0 5% 1/20W MF 0201

PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PLT_RESET_L
PM_RSMRST_PCH_L
PCH_SUSWARN_L
PM_PWRBTN_L
PM_ACPRESENT
PCH_BATLOW_L
BATLOW only in mobile package
TP_PCH_SLP_WLAN_L
PCH_PME_L
TP_PCH_GPP_A12

U1100
SKL-PCH-H
TBD
FCBGA
SYM 4 OF 12

CRITICAL

OMIT_TABLE

SYSTEM POWER MANAGEMENT

GPP_A15/SUSACK*	BB19	DRAM_RESET*	BC14
SYS_RESET*	AW1	DSW_PWROK	AV11
SYS_PWROK	AY1	WAKE*	BC13
PCH_PWROK	AW11	GPP_A8/CLKRUN*	AW22
		GPP_A14/SUS_STAT*/ESPI_RESET*	BC18
GPP_B13/PLTRST*	BB27	GPD8/SUSCLK	AN15
RSMRST*	BA11	GPD10/SLP_S5*	BA13
GPP_A13/SUSWARN*/SUSPWRDNACK	BD19	GPD5/SLP_S4*	BD15
GPD3/PWRBTN*	AT13	GPD4/SLP_S3*	AW15
GPD1/ACPRESENT	BB15	GPD6/SLP_A*	BC15
GPD0/BATLOW*	BD13	SLP_SUS*	BB13
GPP_B12/SLP_S0*	BC26	SLP_LAN*	AV15
GPD9/SLP_WLAN*	AV13	GPD2/LAN_WAKE*	BD11
GPP_A11/PME*	BD17	GPD11/LANPHYPC	AR15
GPP_A12/BMBUSY*/ISH_GP6/SX_EXIT_HOLDOFF*	BB17	GPP_B2/VRALERT*	BD23

RTC

RTCX1	BC9	PCH_CLK32K_RTCX1
RTCX2	BD10	PCH_CLK32K_RTCX2
INTRUDER*	BE11	PCH_INTRUDER_L
SRTCRST*	BB10	PCH_SRTCRST_L
RTCRST*	BC10	RTC_RESET_L

ESPI/LPC

GPP_A0/RCIN*/ESPI_ALERT1*	AT17	PCH_RCIN_TERM	
GPP_A1/LAD0/ESPI_IO0	AT22	LPC_AD_R<0>	R1221 33
GPP_A2/LAD1/ESPI_IO1	AV22	LPC_AD_R<1>	R1222 33
GPP_A3/LAD2/ESPI_IO2	AT19	LPC_AD_R<2>	R1223 33
GPP_A4/LAD3/ESPI_IO3	BD16	LPC_AD_R<3>	R1224 33
GPP_A5/LFRAME*/ESPI_CS0*	BE16	LPC_FRAME_R_L	R1225 33
GPP_A6/SERIRQ/ESPI_CS1*	BA17	LPC_SERIRQ	
GPP_A7/PIRQA*/ESPI_ALERT0*	AW17	SMC_RUNTIME_SCI_L	
GPD7/RSVD	BD14	NC	

=PPVDDQ_S3_MEMRESET

R1261 1K 5% 1/10W MF-LF 402
R1271 0 5% 1/20W MF 0201
MEM_RESET_L
C1261 0.1UF 10% 16V X7R-CERM 0402
R1220 100K 5% 1/20W MF 201

PCH_MEM_RESET_L
PM_RSMRST_PCH_L
PCIE_WAKE_L
LPC_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
TP_PCH_SLP_LAN_L
SMC_WAKE_SCI_L
PCH_VRALERT_L

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
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CRITICAL

OMIT_TABLE

DMI

CPU/MISC

DMI_S2N_N<0>	C27	DMI_TXN0
DMI_S2N_P<0>	B27	DMI_TXP0
DMI_S2N_N<1>	B28	DMI_TXN1
DMI_S2N_P<1>	A28	DMI_TXP1
DMI_S2N_N<2>	B29	DMI_TXN2
DMI_S2N_P<2>	C29	DMI_TXP2
DMI_S2N_N<3>	B30	DMI_TXN3
DMI_S2N_P<3>	A30	DMI_TXP3
DMI_N2S_N<0>	L27	DMI_RXN0
DMI_N2S_P<0>	N27	DMI_RXP0
DMI_N2S_N<1>	E24	DMI_RXN1
DMI_N2S_P<1>	G24	DMI_RXP1
DMI_N2S_N<2>	G27	DMI_RXN2
DMI_N2S_P<2>	E26	DMI_RXP2
DMI_N2S_N<3>	L29	DMI_RXN3
DMI_N2S_P<3>	K29	DMI_RXP3

PROCPWRGD	AM3	PCH_PROCPWRGD	R1216 33 CPU_PWRGD
THERMTRIP*	AJ3	PM_THRMTRIP_PCH_R_L	R1219 560 PM_THRMTRIP_L
PECI	AL3	PCH_PECI	R1217 13 NOSTUFF CPU_PECI
GPP_B3/CPU_GP2	BC23	NC	
GPP_B4/CPU_GP3	BD24	NC	
GPP_E3/CPU_GP0	AF41	XDP_PCH_OBSDATA_A2	
GPP_E7/CPU_GP1	AE44	XDP_PCH_OBSDATA_B2	
GPP_B23/SML1ALERT*/PCHHOT*	AT27	PCH_STRP_GPP_B23	
CPU_TRST*	AY5	PCH_TRST_L	R1226 0 XDP_CPU_TRST_L
PLTRST_PROC*	AK2	CPU_RESET_L	
PRDY*	AT4	PCH_PRDY_L	
PREQ*	AT3	PCH_PREQ_L	
PCH_TRIGIN	AK1	PROC_TRIGOUT	
PCH_TRIGOUT	AL2	PROC_TRIGIN_R	R1228 33 PROC_TRIGIN
PM_DOWN	AH2	PM_DOWN	
PM_SYNC	AJ4	PM_SYNC_R	R1229 33 PM_SYNC

=PP1V0_S3_VCCST

R1218 1K 5% 1/16W MF-LF 402

PLACE_NEAR=U1100.AM3:12.7MM
PLACE_NEAR=U1100.AL3:12.7MM
PLACE R1217 NEAR TRACE T-POINT
PLACE_NEAR=U1100.AL2:12.7MM
PLACE_NEAR=U1100.AJ4:5MM
PLACE_NEAR=R1219.2:3MM

SYNC_MASTER=J95_DEBORAH	SYNC_DATE=10/20/2014
PAGE TITLE	CPU & CHIPSET: PCH RTC/DMI/PM/CPU_Misc
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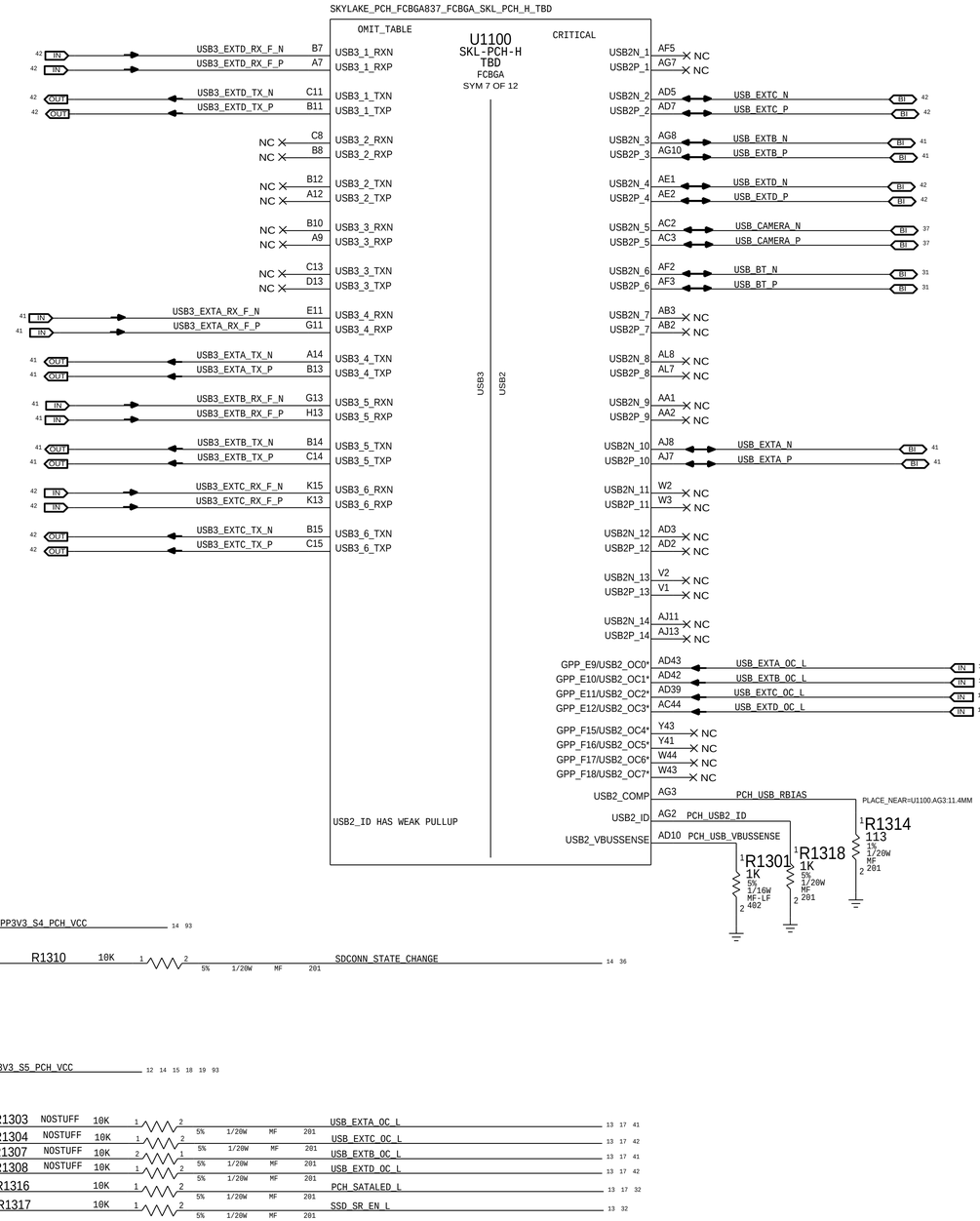

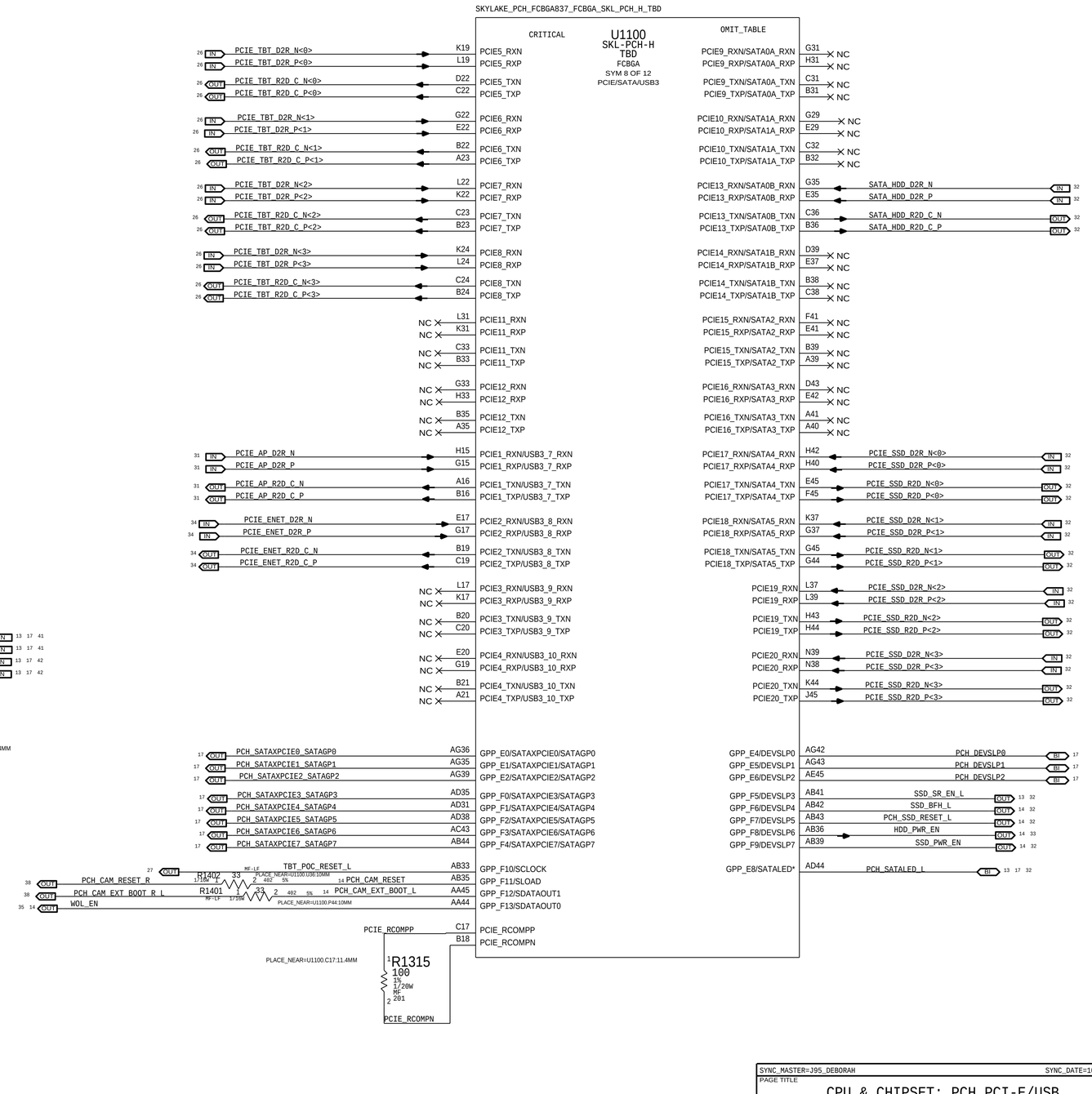

SYNC_MASTER=J95_DEBORAH	SYNC_DATE=10/20/2014
PAGE TITLE	CPU & CHIPSET: PCH PCI-E/USB
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=PP3V3_S5_PCH_VCC 12 13 14 15 18 19 93

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
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CRITICAL

OMIT_TABLE

NOSTUFF R1440 1K 5% 1/20W MF 201 — 1 2 — PCH_BOARD_ID<0>
NOSTUFF R1441 1K 5% 1/20W MF 201 — 1 2 — PCH_BOARD_ID<1>
NOSTUFF R1442 1K 5% 1/20W MF 201 — 1 2 — PCH_BOARD_ID<2>
NOSTUFF R1443 1K 5% 1/20W MF 201 — 1 2 — PCH_BOARD_ID<3>

GPP_A17/ISH_GP7 BC19 NC
GPP_A18/ISH_GP0 BB22 NC
GPP_A19/ISH_GP1 BD21 NC
GPP_A20/ISH_GP2 BD22 PCH_BOARD_ID<0>
GPP_A21/ISH_GP3 BE21 PCH_BOARD_ID<1>
GPP_A22/ISH_GP4 BD18 PCH_BOARD_ID<2>
GPP_A23/ISH_GP5 BC22 PCH_BOARD_ID<3>
GPPA/ INTEGRATED SENSOR

GPP_B0 AR27 NC
GPP_B1 AL27 NC
GPP_B11 AN24 NC
GPP_B14/SPKR BD26 PCH_STRP_TOPBLK_SWP_L (44 IN)
GPPB
GPPC/SMLINK/I2C/UART

GPP_D0 AL39 NC
GPP_D1 AN36 NC
GPP_D2 AN38 NC
GPP_D3 AN41 NC
GPP_D9 AL44 NC
GPP_D10 AL36 NC
GPP_D11 AL35 NC
GPP_D12 AJ39 NC
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA AK45 NC
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL AK44 NC
GPP_D15/ISH_UART0_RTS* AL43 NC
GPP_D16/ISH_UART0_CTS* AJ43 NC
GPP_D21 AG44 NC
GPP_D22 AH43 NC
GPP_D4/ISH_I2C2_SDA/I2C3_SDA AM44 NC
GPP_D23/ISH_I2C2_SCL/I2C3_SCL AJ44 NC
GPPD/INTEGRATED SENSOR/UART/I2C

GPP_C0/SMBCLK AW44 SMBUS_PCH_CLK (OUT 46)
GPP_C1/SMBDATA BB43 SMBUS_PCH_DATA (BI 46)
GPP_C2/SMBALERT* BB41 PCH_SMBALERT_L 14
GPP_C3/SML0CLK AY44 SML_PCH_0_CLK (OUT 46)
GPP_C4/SML0DATA BB39 SML_PCH_0_DATA (BI 46)
GPP_C5/SML0ALERT* BA40 PCH_STRP_LPC_L 14
GPP_C6/SML1CLK AW42 SML_PCH_1_CLK (IN 46)
GPP_C7/SML1DATA AW45 SML_PCH_1_DATA (BI 46)
GPP_C8/UART0_RXD BA41 GPU_NEPTUNE_EMERALD_ID (IN 95)
GPP_C9/UART0_TXD AV44 NC
GPP_C10/UART0_RTS* AV43 NC
GPP_C11/UART0_CTS* AU44 NC
GPP_C12/UART1_RXD/ISH_UART1_RXD AU43 NC
GPP_C13/UART1_TXD/ISH_UART1_TXD AT43 NC
GPP_C14/UART1_RTS*/ISH_UART1_RTS* AT44 NC
GPP_C15/UART1_CTS*/ISH_UART1_CTS* AU41 NC
GPP_C16/I2C0_SDA AT42 NC
GPP_C17/I2C0_SCL AR38 NC
GPP_C18/I2C1_SDA AR44 NC
GPP_C19/I2C1_SCL AR41 NC
GPP_C20/UART2_RXD AR45 NC
GPP_C21/UART2_TXD AR39 NC
GPP_C22/UART2_RTS* AN44 NC
GPP_C23/UART2_CTS* AN43 NC

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
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CRITICAL

OMIT_TABLE

19 14 (OUT) ENET_LOW_PWR_PCH — GPP_F14 Y44
NC — GPP_F19/EDP_VDDEN W42
NC — GPP_F20/EDP_BKLTEN W35
NC — GPP_F21/EDP_BKLTCTL W36
39 (OUT) TCON_RESET_L — R1405 33 1/16W MF-LF — GPP_F22 W39 — TCON_RESET_R_L 14
45 (BI) — SPIROM_USE_MLB — GPP_F23 V44
PLACE_NEAR=U1100.M45:10MM
GPPF/ BACKLIGHT

NC — GPP_I0/DDPB_HPD0 AW4
NC — GPP_I1/DDPC_HPD1 AY2
NC — GPP_I2/DDPD_HPD2 AV4
NC — GPP_I3/DDPE_HPD3 BA4
R1426 100K 5% 1/20W MF 201 — PCH_EDP_HPD_PD — GPP_I4/EDP_HPD BD7
GPPI IS ON VCC3V3_PRIM
NC — GPP_I5/DDPB_CTRLCLK BA5
NC — GPP_I6/DDPB_CTRLDATA BC4
NC — GPP_I7/DDPC_CTRLCLK BB3
NC — GPP_I8/DDPC_CTRLDATA BB6
NC — GPP_I9/DDPD_CTRLCLK BE5
NC — GPP_I10/DDPD_CTRLDATA BE6
GPP_H10/SML2CLK BD34
GPP_H11/SML2DATA AW35
GPP_H12/SML2ALERT* BD35
GPP_H13/SML3CLK BC35
GPP_H14/SML3DATA BA35
GPP_H15/SML3ALERT* BB36
GPP_H16/SML4CLK BD39
GPP_H17/SML4DATA BE34
GPP_H18/SML4ALERT* BC36
GPP_H19/ISH_I2C0_SDA BB38
GPP_H20/ISH_I2C0_SCL BC38
GPP_H21/ISH_I2C1_SDA BE39
GPP_H22/ISH_I2C1_SCL BD38
GPP_H23 BD36
GPP_I/O DISPLAY
GPPH/I2C/INTEGRATED SENSOR /SMLINK

GPP_G0/FAN_TACH_0 U43 NC
GPP_G1/FAN_TACH_1 U42 NC
GPP_G2/FAN_TACH_2 U41 NC
GPP_G3/FAN_TACH_3 M44 NC
GPP_G4/FAN_TACH_4 U36 NC
GPP_G5/FAN_TACH_5 P44 NC
GPP_G6/FAN_TACH_6 T45 NC
GPP_G7/FAN_TACH_7 T44 NC
GPP_G8/FAN_PWM_0 R44 NC
GPP_G9/FAN_PWM_1 R43 NC
GPP_G10/FAN_PWM_2 U39 NC
GPP_G11/FAN_PWM_3 N42 NC
GPP_G12/GSXDOUT B39 NC
GPP_G13/GSXSLOAD R36 NC
GPP_G14/GSXDIN R42 NC
GPP_G15/GSXSRESET* R41 NC
GPP_G16/GSXCLK P43 NC
GPP_G17/ADR_COMPLETE N44 NC
GPP_G18/NMI* N43 NC
GPP_G19/SMI* M45 NC
GPP_G20 R35 NC
GPP_G21 U35 AUD_IPHS_SWITCH_EN_PCH (OUT 14 19)
GPP_G22 L44 AUD_IP_PERIPHERAL_DET (IN 97)
GPP_G23 L43 AUD_I2C_INT_L (IN 95)
GPP_G/ GPPG

=PP3V3_S4_PCH_VCC 13 93

R1429 10K 5% 1/20W MF 201 — 1 2 — SSD_PWR_EN 13 32

=PP3V3_S5_PCH_VCC 12 13 14 15 18 19 93

R1412 10K 5% 1/20W MF 201 — 1 2 — SMC_WAKE_SCI_L 12 43
R1427 10K 5% 1/20W MF 201 — 1 2 — HDD_PWR_EN 13 33
NOSTUFF R1428 10K 5% 1/20W MF 201 — 1 2 — PCH_SSD_RESET_L 13 32
R1403 10K 5% 1/20W MF 201 — 2 1 — TBT_PWR_EN_PCH 11 19

=PP3V3_S0_PCH_VCC 11 12 15 18 19 93

R1490 100K 5% 1/20W MF 201 — 1 2 — AUD_IPHS_SWITCH_EN_PCH 14 19
R1450 10K 5% 1/20W MF 201 — 1 2 — TBT_PWR_REQ_L 11 27
R1404 100K 5% 1/20W MF 201 — 1 2 — PCH_SMBALERT_L 14
R1421 10K 5% 1/20W MF 201 — 1 2 — SDCONN_OC_L 14 36
R1406 10K 5% 1/20W MF 201 — 2 1 — SMC_RUNTIME_SCI_L 12 43
R1411 10K 5% 1/20W MF 201 — 2 1 — JTAG_TBT_TMS_PCH 14 19
R1415 10K 5% 1/20W MF 201 — 1 2 — JTAG_ISP_TDO 14 19
R1416 100K 5% 1/20W MF 201 — 1 2 — JTAG_ISP_TDI 14 19
R1425 10K 5% 1/20W MF 201 — 1 2 — TCON_RESET_R_L 14

NOSTUFF R1453 10K 5% 1/20W MF 201 — 1 2 — PCH_STRP_LPC_L 14
NOSTUFF R1489 10K 5% 1/20W MF 201 — 1 2 — SSD_BFH_L 13 32
R1407 10K 5% 1/20W MF 201 — 1 2 — WOL_EN 13 35
R1414 10K 5% 1/20W MF 201 — 2 1 — JTAG_ISP_TCK 14 19
R1417 10K 5% 1/20W MF 201 — 1 2 — ENET_LOW_PWR_PCH 14 19
R1451 10K 5% 1/20W MF 201 — 1 2 — ENET_MEDIA_SENSE 14 34
R1424 10K 5% 1/20W MF 201 — 1 2 — DP_TBT_SEL 14 40 57

JTAG_ISP_TDO (IN 19 14) — JTAG_ISP_TDI (OUT 19 14) — JTAG_ISP_TCK (OUT 19 14) — JTAG_TBT_TMS_PCH (OUT 19 14)
DP_TBT_SEL (OUT 57 40 14) — ENET_MEDIA_SENSE (IN 34 14) — BKLT_FAULT_INT_L (IN 68)
SDCONN_STATE_CHANGE (IN 36 13) — SDCONN_OC_L (IN 36 14)
TBT_CIO_PLUG_EVENT_R_L (IN 19)

PCH_CAM_EXT_BOOT_L 13
PCH_CAM_RESET 13

R1422 10K 5% 1/20W MF 201
R1423 10K 5% 1/20W MF 201

SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE
CPU & CHIPSET: PCH GPIO/Misc

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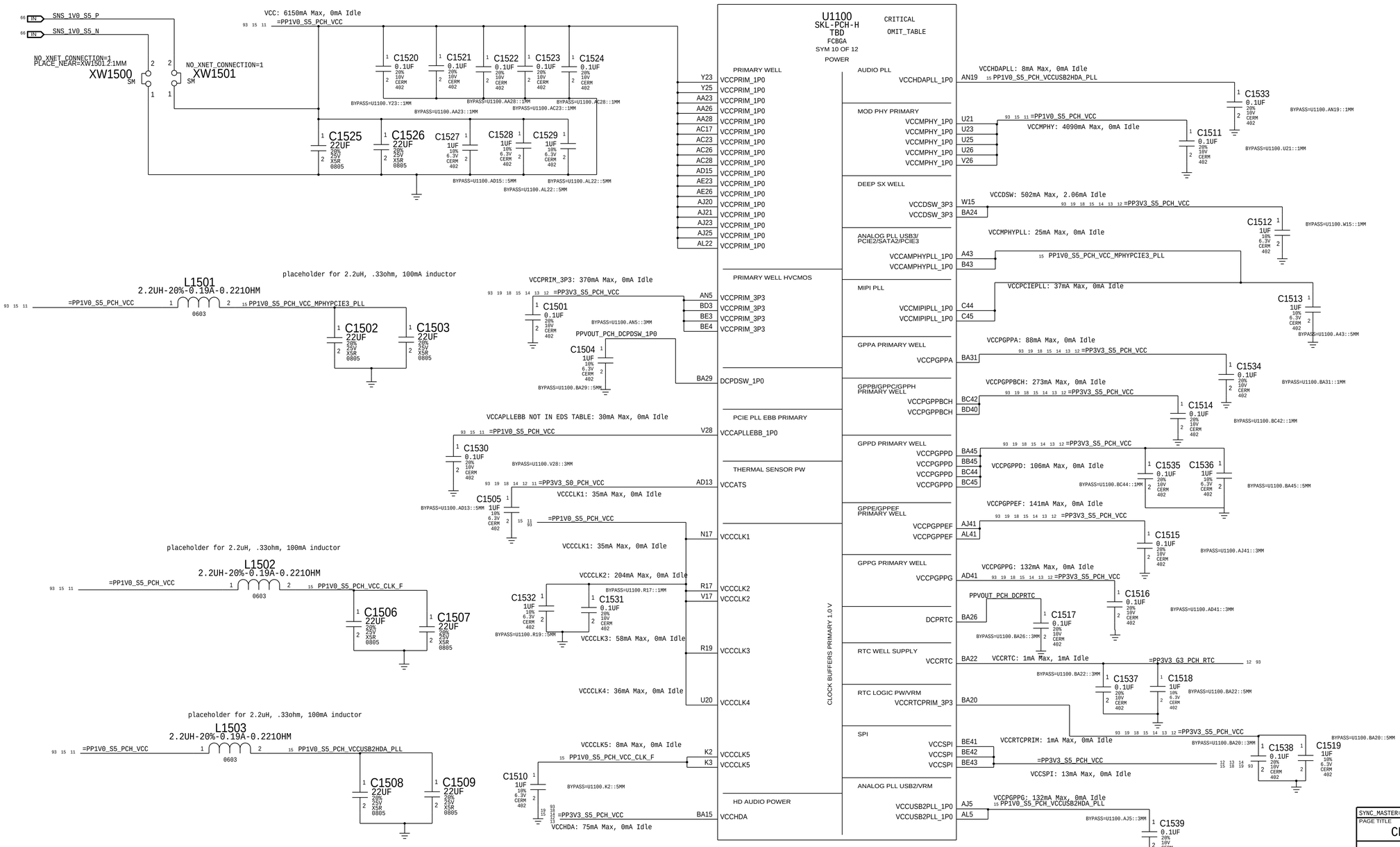
NEED TO ADD 47UF BULK CAPS TO 1.0V AND 3.3V RAIL



Current data from EDS (doc #546717, Rev 0.7).

SYNC_MASTER=J95_DDRESSLER	SYNC_DATE=02/24/2015
PAGE TITLE	CPU & CHIPSET: PCH Power/Decoupling
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
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SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
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CRITICAL

OMIT_TABLE

A2	VSS	VSS	M35
A3	VSS	VSS	M42
A4	VSS	VSS	N4
A18	VSS	VSS	N5
A25	VSS	VSS	N10
A32	VSS	VSS	N15
A37	VSS	VSS	N19
A42	VSS	VSS	N22
A44	VSS	VSS	N24
B1	VSS	VSS	N35
B2	VSS	VSS	N36
B3	VSS	VSS	N41
B6	VSS	VSS	P17
B25	VSS	VSS	P19
B37	VSS	VSS	P22
B40	VSS	VSS	P45
B44	VSS	VSS	R5
B45	VSS	VSS	R10
C2	VSS	VSS	R14
C4	VSS	VSS	R22
C10	VSS	VSS	R29
C28	VSS	VSS	R33
C37	VSS	VSS	R38
C42	VSS	VSS	T1
D10	VSS	VSS	T2
D12	VSS	VSS	T4
D15	VSS	VSS	T42
D16	VSS	VSS	U4
D17	VSS	VSS	U8
D19	VSS	VSS	U10
D21	VSS	VSS	U11
D24	VSS	VSS	U14
D25	VSS	VSS	U15
D27	VSS	VSS	U17
D29	VSS	VSS	U18
D30	VSS	VSS	U28
D31	VSS	VSS	U29
D33	VSS	VSS	U31
D35	VSS	VSS	U32
D36	VSS	VSS	U33
D45	VSS	VSS	U38
E13	VSS	VSS	V3
E15	VSS	VSS	V18
E31	VSS	VSS	V20
E33	VSS	VSS	V21
F8	VSS	VSS	V23
F44	VSS	VSS	V25
G9	VSS	VSS	V29
G42	VSS	VSS	V45
H3	VSS	VSS	W4
H17	VSS	VSS	W8
H19	VSS	VSS	W14
H22	VSS	VSS	W31
H24	VSS	VSS	W32
H27	VSS	VSS	W33
H29	VSS	VSS	W38
H35	VSS	VSS	Y17
J3	VSS	VSS	Y18
J5	VSS	VSS	Y20
J7	VSS	VSS	Y21
J10	VSS	VSS	Y26
J11	VSS	VSS	Y28
J39	VSS	VSS	Y29
K4	VSS	VSS	AA4
K10	VSS	VSS	AA17
K27	VSS	VSS	AA18
K33	VSS	VSS	AA20
K36	VSS	VSS	AA21
K42	VSS	VSS	AA25
K43	VSS	VSS	AA29
L4	VSS	VSS	AA42
L8	VSS	VSS	AB4
L12	VSS	VSS	AB5
L13	VSS	VSS	AB7
L15	VSS	VSS	AB8
L41	VSS	VSS	AB10

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
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CRITICAL

OMIT_TABLE

AB11	VSS	VSS	AL32
AB14	VSS	VSS	AL33
AB15	VSS	VSS	AL38
AB31	VSS	VSS	AM15
AB32	VSS	VSS	AM17
AB38	VSS	VSS	AM19
AC1	VSS	VSS	AM22
AC18	VSS	VSS	AM24
AC20	VSS	VSS	AM27
AC21	VSS	VSS	AM29
AC25	VSS	VSS	AM45
AC29	VSS	VSS	AN4
AC45	VSS	VSS	AN7
AD4	VSS	VSS	AN8
AD8	VSS	VSS	AN10
AD11	VSS	VSS	AN11
AD14	VSS	VSS	AN22
AD32	VSS	VSS	AN27
AD33	VSS	VSS	AN31
AD36	VSS	VSS	AN39
AE4	VSS	VSS	AP4
AE18	VSS	VSS	AP11
AE20	VSS	VSS	AR5
AE21	VSS	VSS	AR7
AE25	VSS	VSS	AR9
AE28	VSS	VSS	AR33
AE29	VSS	VSS	AR34
AE42	VSS	VSS	AR42
AF18	VSS	VSS	AT9
AF20	VSS	VSS	AT10
AF21	VSS	VSS	AT15
AF23	VSS	VSS	AT36
AF25	VSS	VSS	AU1
AF26	VSS	VSS	AU7
AF28	VSS	VSS	AU35
AF29	VSS	VSS	AU36
AG4	VSS	VSS	AU39
AG11	VSS	VSS	AU45
AG13	VSS	VSS	AV6
AG31	VSS	VSS	AV17
AG32	VSS	VSS	AV24
AG33	VSS	VSS	AV27
AG38	VSS	VSS	AV31
AH1	VSS	VSS	AV33
AH17	VSS	VSS	AW9
AH18	VSS	VSS	AW13
AH20	VSS	VSS	AW19
AH21	VSS	VSS	AW29
AH23	VSS	VSS	AW37
AH25	VSS	VSS	AY38
AH26	VSS	VSS	AY45
AH28	VSS	VSS	BA1
AH29	VSS	VSS	BB1
AH45	VSS	VSS	BB11
AJ10	VSS	VSS	BB16
AJ14	VSS	VSS	BB21
AJ15	VSS	VSS	BB25
AJ17	VSS	VSS	BB30
AJ18	VSS	VSS	BB34
AJ26	VSS	VSS	BC1
AJ28	VSS	VSS	BC2
AJ29	VSS	VSS	BD2
AJ31	VSS	VSS	BD43
AJ32	VSS	VSS	BD44
AJ36	VSS	VSS	BD45
AK4	VSS	VSS	BE9
AK42	VSS	VSS	BE14
AL4	VSS	VSS	BE18
AL10	VSS	VSS	BE23
AL11	VSS	VSS	BE28
AL13	VSS	VSS	BE32
AL17	VSS	VSS	BE37
AL19	VSS	VSS	BE40
AL24	VSS	VSS	BE44
AL29	VSS		

SYNC_MASTER=J95_DEBORAH SYNC_DATE=10/20/2014

PAGE TITLE

CPU & CHIPSET: PCH Grounds

Apple Inc.

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REVISION 4.0.0

BRANCH proto1b

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Primary Micro2-XDP

Extra BPM Testpoints

IN XDP_BPM_L<2> → TP TP-P6 TP1802
IN XDP_BPM_L<3> → TP TP-P6 TP1803

CRB has no-stuff S3 pull-up on PREQ_L
PDG allows any value from 51 to 3K

=PPVCCIO_S0_CPU → 150 MF 1% 1/20W 201 → XDP R1847

=PP1V0_S3_XDP → XDP R1831 1K 5% 1/16W MF-LF 402 (NOSTUFF R1898 1K 5% 1/10W MF-LF 402)
CPU_CFG_3_R → R1803 MF 1/20W 0201 5% (NOSTUFF)

XDP_CPU_PREQ_L ↔ XDP_CPU_PRDY_L → XDP R1839 1K 1/20W 5% MF 201

Connect Hook2 to CFG<0>
and pull-up to S0
(as in CRB)

=PP3V3_S5_ROM

PM_VCCST_PWRGD → R1891 NOSTUFF 1K
PM_RSMRST_PCH_L → R1806 XDP 1K
CPU_PWRGD → R1800 NOSTUFF 1K
PLACE_NEAR=U0500.AB35:16.5mm
R1801 NOSTUFF 2.2K 5% 1/20W MF 201

PM_PWRBTN_L → R1802 XDP 0 5% 1/20W MF 0201
PM_PCH_SYS_PWROK → R1804 NOSTUFF 220 5% 1/20W MF 201
SPI_MOSI_R → R1826 XDP 0 5% 1/20W MF 0201

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

XDP C1805 0.1UF 20% 10V CERM 402
NOSTUFF C1804 0.1UF 20% 10V CERM 402

XDP_PCH_TCK → XDP_PCH_TCK_R_2 → R1828 0 5% 1/20W MF 0201 → XDP_CPU_TCK
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP R1866 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AN3:28mm)
XDP R1823 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.F11:50.0mm)

XDP C1800 0.1UF 20% 10V CERM 402
XDP C1801 0.1UF 20% 10V CERM 402
XDP C1806 0.1UF 20% 10V CERM 402

XDP_CPU_PRESENT_L → R1825 0 5% 1/20W MF 0201 → SPI_IO_R<2>
R1899 NOSTUFF MF 1/20W 0201 5%

XDP_CPU_PREQ_L → R1848 0 5% 1/20W MF 0201 → XDP_PREQ_L_R
XDP_PCH_PREQ_L → R1850 0 5% 1/20W MF 0201 (PLACE_NEAR=U1100.AT3:150.0mm)
R1851 0 5% 1/20W MF 0201 NOSTUFF (PLACE_NEAR=R1850.1:10mm)

XDP_CPU_PRDY_L → R1849 0 5% 1/20W MF 0201 → XDP_PRDY_L_R
XDP_PCH_PRDY_L → R1852 0 5% 1/20W MF 0201 (PLACE_NEAR=U1100.AT4:150.0mm)
R1853 0 5% 1/20W MF 0201 NOSTUFF (PLACE_NEAR=R1852.1:10mm)

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM
998-2516

OBSFN_A0	OBSFN_A1	OBSFN_C0	CPU_CFG<17>
OBSDATA_A0	OBSDATA_A1	OBSFN_C1	CPU_CFG<16>
OBSDATA_A2	OBSDATA_A3	OBSDATA_C0	CPU_CFG<8>
OBSFN_B0	OBSFN_B1	OBSDATA_C1	CPU_CFG<9>
OBSDATA_B0	OBSDATA_B1	OBSDATA_C2	CPU_CFG<10>
OBSDATA_B2	OBSDATA_B3	OBSDATA_C3	CPU_CFG<11>
PWRGD/HOOK0	HOOK1	OBSFN_D0	CPU_CFG<19>
HOOK2	HOOK3	OBSFN_D1	CPU_CFG<18>
SDA	SCL	OBSDATA_D0	CPU_CFG<12>
TCK1	TCK0	OBSDATA_D1	CPU_CFG<13>
		OBSDATA_D2	CPU_CFG<14>
		OBSDATA_D3	CPU_CFG<15>
		ITPCLK/HOOK4	ITPXDP_CLK100M_P
		ITPCLK#/HOOK5	ITPXDP_CLK100M_N
		VCC_OBS_CD	
		RESET#/HOOK6	XDP_CPURST_L
		DBR#/HOOK7	XDP_DBRESET_L
		TDO	XDP_PCH_TDO
		TRSTn	XDP_CPU_TRST_L
		TDI	XDP_CPU_TDI
		TMS	XDP_CPU_TMS
		XDP_PRESENT#	

XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_HOOK2_R
XDP_VR_READY

NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

ICT CPU & PCH JTAG Test-Points:

TP1840 = TMS
TP1841 = TDI
TP1842 = TDO
TP1843 = TCK0
(TP1844 = TCK1)
TP1845 = DAISY
TP1846 = DAISY_L
TP1847 = TRST_L

=PP1V0_S3_XDP → XDP R1860 51 5% 1/20W MF 201 → XDP R1861 51 5% 1/20W MF 201 → XDP R1862 51 5% 1/20W MF 201
TP1842 TP TP-P6
XDP_PCH_TDO IN ← U1100.AP1:50.0mm
XDP_PCH_TDI OUT → U1100.AP2:4mm
U1100.AR2:3.5mm
XDP_PCH_TMS OUT
XDP_CPU_TMS → R1838 0 5% 1/20W MF 0201 (PLACE_NEAR=J1800.51:5MM)
TP1840 TP TP-P6
XDP C1898 0.1UF 20% 10V CERM 402
XDP_CPU_TDO → R1820 51 5% 1/20W MF 201 (PLACE_NEAR=J1800.51:5MM)
XDP_CPU_TRST_L → R1824 51 5% 1/20W NOSTUFF MF 201
TP1847 TP TP-P6
XDP C1899 0.1UF 20% 10V CERM 402

NOTE: TDI and TMS are terminated in CPU.

=PP1V0_S5_XDP → R1808 2.2K 5% 1/20W MF 201
R1807 0 5% 1/20W MF 0201 XDP PCH_ITP_PMODE IN
R1805 NOSTUFF 1K 5% 1/20W MF 201 CPU_RESET_L IN (PLACE_NEAR=R1808.2:5MM)

ICT CPU & PCH JTAG Daisy-Chain Support (S0):

To configure CPU and PCH JTAG in an ICT Daisy-Chain:
Drive ICT_JTAG_DAISY to 5V and
drive ICT_JTAG_DAISY_L to Ground.

TP1845 TP TP-P6 ICT_JTAG_DAISY
R1845 1K 5% 1/20W MF 201 (PLACE_NEAR=J1800.51:5.08mm)
Q1840 DMN5L06VK-7 SOT563 VER 5 (PLACE_NEAR=J1800.57:5.08MM)
XDP_PCH_TCK → TP1844 TP TP-P6
R1841 1M 5% 1/20W MF 201 (PLACE_NEAR=J1800.58:5.08MM)
Q1840 DMN5L06VK-7 SOT563 VER 5
XDP_CPU_TCK → TP1843 TP TP-P6 → XDP_CPU_PCH_TCK

Q1842 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3 (PLACE_NEAR=J1800.51:5.08mm)
Q1848 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3 (PLACE_NEAR=J1850.55:5.08mm)
XDP_CPU_TDO ↔ XDP_CPU_TDO_PCH_TDI ↔ XDP_PCH_TDI
R1842 1M 5% 1/20W MF 201

TP1846 TP TP-P6 ICT_JTAG_DAISY_L
=PP5V_S5_XDP → R1836 2.2K 5% 1/20W MF 201
Q1846 DMN5L06VK-7 SOT563 VER 5 (PLACE_NEAR=J1800.57:6MM)
R1840 1M 5% 1/20W MF 201
R1837 0 5% 1/20W MF 0201 NOSTUFF → XDP_PCH_TDO
Q1846 DMN5L06VK-7 SOT563 VER 5 (PLACE_NEAR=J1800.58:5.08MM)
XDP_CPU_PCH_TDO → XDP_CPU_TDO
R1829 0 5% 1/20W MF 0201 NOSTUFF

Q1844 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
Q1845 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
XDP_CPU_TDI → XDP_CPU_TDI_PCH_TDI → XDP_PCH_TDI
TP1841 TP TP-P6
R1843 0 5% 1/20W MF 0201 NOSTUFF
R1854 1M 5% 1/20W MF 201
R1844 0 5% 1/20W MF 0201 NOSTUFF

Secondary (PCH) Micro2-XDP

=PP1V0_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM
998-2516

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

XDP_PCH_PREQ_L_R	XDP_PCH_PRDY_L_R	OBSFN_C0	XDP_PCH_SATAXPCIE0_SATAGP0
OBSFN_A0	OBSFN_A1	OBSFN_C1	XDP_PCH_SATAXPCIE7_SATAGP7
XDP_PCH_SATAXPCIE1_SATAGP1	XDP_PCH_SATAXPCIE2_SATAGP2	OBSDATA_C0	XDP_PCH_USB2_0C0_L
OBSDATA_A0	OBSDATA_A1	OBSDATA_C1	XDP_PCH_USB2_0C1_L
XDP_PCH_CPU_GP0	XDP_PCH_DEVSLP0	OBSDATA_C2	XDP_PCH_USB2_0C2_L
OBSDATA_A2	OBSDATA_A3	OBSDATA_C3	XDP_PCH_USB2_0C3_L
OBSFN_B0	OBSFN_B1	OBSFN_D0	
		OBSFN_D1	
XDP_PCH_DEVSLP1	XDP_PCH_DEVSLP2	OBSDATA_D0	XDP_PCH_SATAXPCIE3_SATAGP3
OBSDATA_B0	OBSDATA_B1	OBSDATA_D1	XDP_PCH_SATAXPCIE4_SATAGP4
XDP_PCH_CPU_GP1	XDP_PCH_SATALED_L	OBSDATA_D2	XDP_PCH_SATAXPCIE5_SATAGP5
OBSDATA_B2	OBSDATA_B3	OBSDATA_D3	XDP_PCH_SATAXPCIE6_SATAGP6
XDP_PCH_RSMRST_L	PWRGD/HOOK0	ITPCLK/HOOK4	
HOOK1	VCC_OBS_AB	ITPCLK#/HOOK5	
HOOK2	HOOK3	VCC_OBS_CD	
		RESET#/HOOK6	XDP_PCH_ITP_PMODE
		DBR#/HOOK7	XDP_PM_SYSRST_L
=SMBUS_XDP_SDA	SDA		
=SMBUS_XDP_SCL	SCL		

XDP C1880 0.1UF 20% 10V CERM 402
XDP C1881 0.1UF 20% 10V CERM 402
XDP_PRESENT#

PCH SIGNALS / XDP SIGNALS

PCH_PREQ_L	OMIT	R1890	SHORT	XDP_PCH_PREQ_L
PCH_PRDY_L	OMIT	R1893	SHORT	XDP_PCH_PRDY_L
PCH_SATAXPCIE0_SATAGP0	OMIT	R1894	SHORT	XDP_PCH_SATAXPCIE0_SATAGP0
PCH_SATAXPCIE1_SATAGP1	OMIT	R1895	SHORT	XDP_PCH_SATAXPCIE1_SATAGP1
PCH_SATAXPCIE2_SATAGP2	OMIT	R1880	SHORT	XDP_PCH_SATAXPCIE2_SATAGP2
PCH_SATAXPCIE3_SATAGP3	OMIT	R1881	SHORT	XDP_PCH_SATAXPCIE3_SATAGP3
PCH_SATAXPCIE4_SATAGP4	OMIT	R1896	SHORT	XDP_PCH_SATAXPCIE4_SATAGP4
PCH_SATAXPCIE5_SATAGP5	OMIT	R1897	SHORT	XDP_PCH_SATAXPCIE5_SATAGP5
PCH_SATAXPCIE6_SATAGP6	OMIT	R1872	SHORT	XDP_PCH_SATAXPCIE6_SATAGP6
PCH_SATAXPCIE7_SATAGP7	OMIT	R1873	SHORT	XDP_PCH_SATAXPCIE7_SATAGP7
XDP_PCH_OBSDATA_A2	OMIT	R1874	SHORT	XDP_PCH_CPU_GP0
PCH_DEVSLP0	OMIT	R1875	SHORT	XDP_PCH_DEVSLP0
PCH_ITP_PMODE	OMIT	R1878	SHORT	XDP_PCH_ITP_PMODE
PCH_DEVSLP1	OMIT	R1879	SHORT	XDP_PCH_DEVSLP1
PCH_DEVSLP2	OMIT	R1882	SHORT	XDP_PCH_DEVSLP2
XDP_PCH_OBSDATA_B2	OMIT	R1883	SHORT	XDP_PCH_CPU_GP1
PCH_SATALED_L	OMIT	R1886	SHORT	XDP_PCH_SATALED_L
PM_RSMRST_PCH_L	OMIT	R1887	SHORT	XDP_PCH_RSMRST_L
PM_SYSRST_L	OMIT	R1884	SHORT	XDP_PM_SYSRST_L
USB_EXTA_OC_L	OMIT	R1833	SHORT	XDP_PCH_USB2_0C0_L
USB_EXTB_OC_L	OMIT	R1835	SHORT	XDP_PCH_USB2_0C1_L
USB_EXTC_OC_L	OMIT	R1832	SHORT	XDP_PCH_USB2_0C2_L
USB_EXTD_OC_L	OMIT	R1834	SHORT	XDP_PCH_USB2_0C3_L

PCH/XDP Signal Isolation Notes:

R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).

SYNC_MASTER=J95_ANDREW SYNC_DATE=01/24/2015

PAGE TITLE: CPU & CHIPSET: XDP

Apple Inc.

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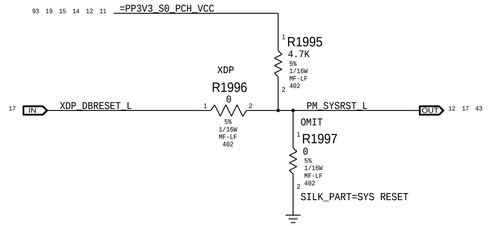
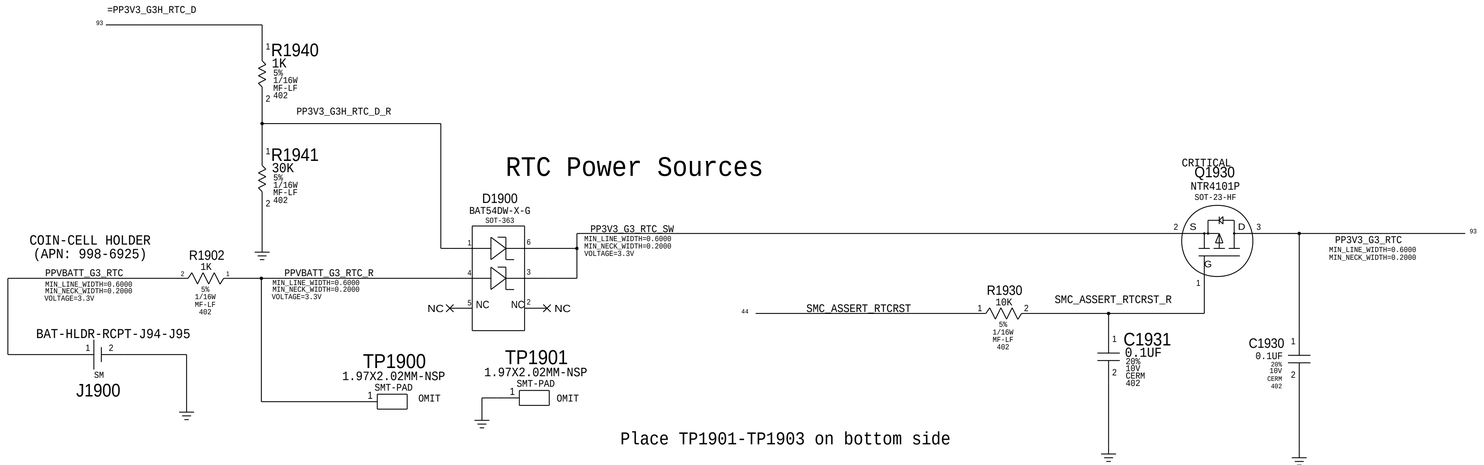
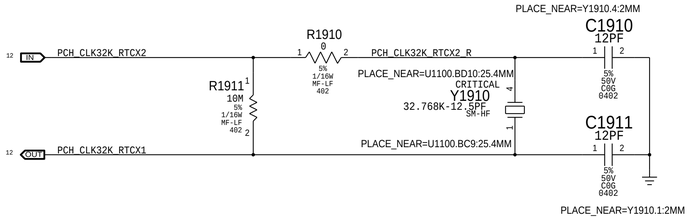
PCH Reset Button



RTC Power Sources

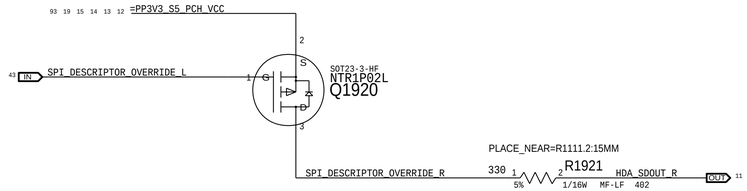


PCH RTC Crystal



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



SYNC_MASTER=BRANCH_SYEDKAR	SYNC_DATE=09/10/2014
PAGE TITLE	CPU & CHIPSET: Chipset Support
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
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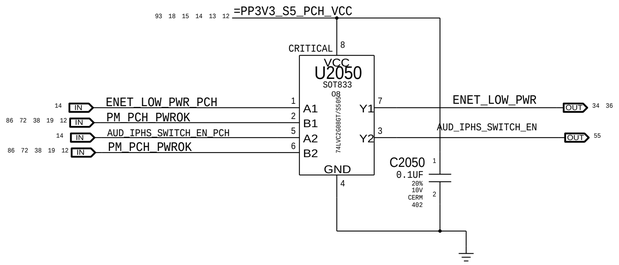
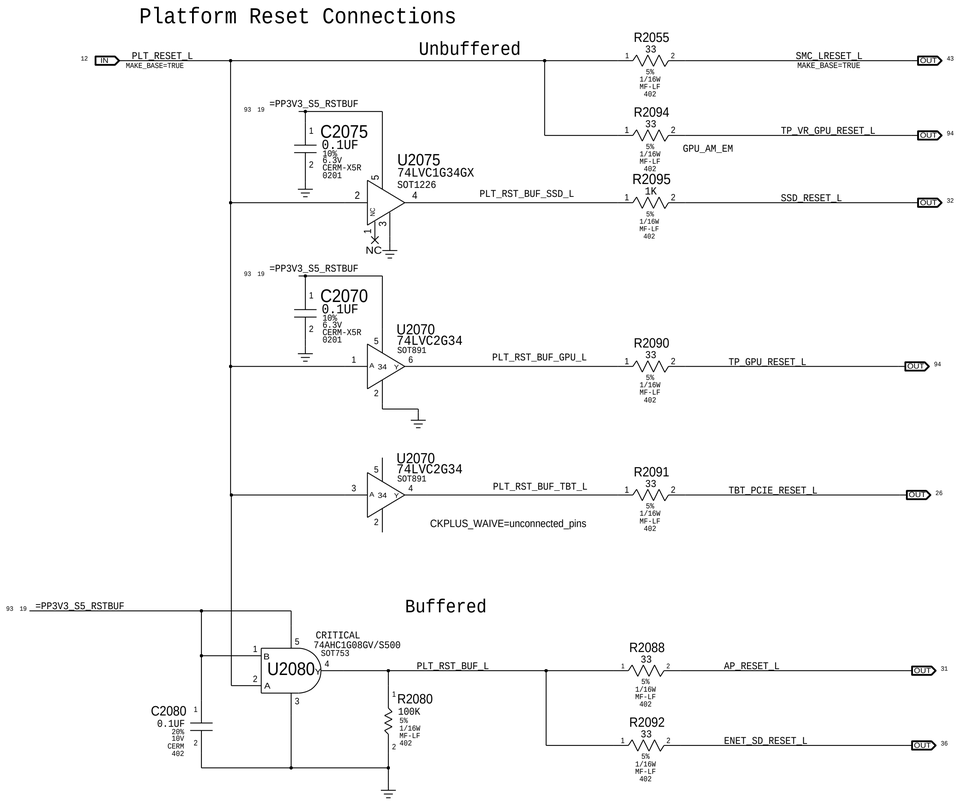
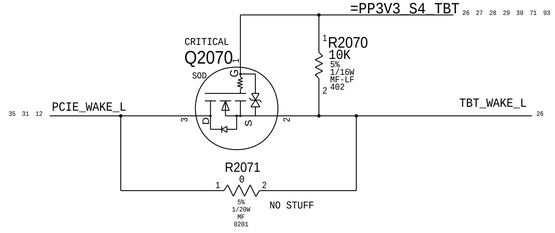
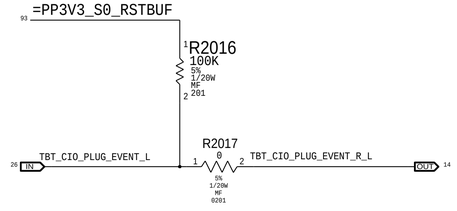
GPIO Glitch Prevention

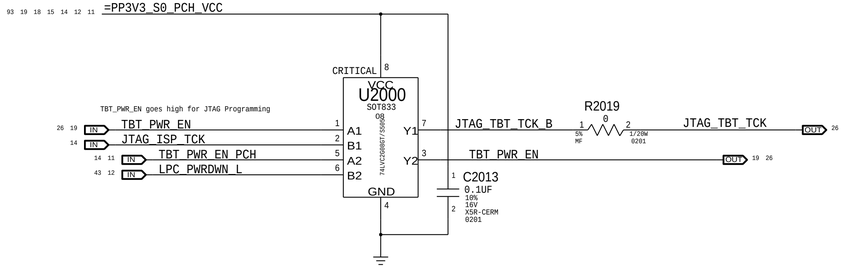


Platform Reset Connections

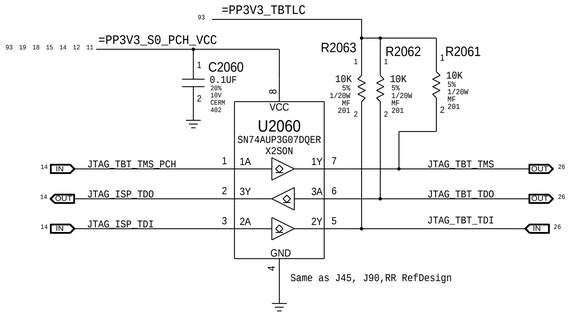








TBT_LC can be on when S0 is off and vice-versa.
Isolation ensure no leakage to FR or PCH
U2060 Supports I/Os powered when VCC = 0V



SYNC_MASTER=J16_IG	SYNC_DATE=04/29/2013
PAGE TITLE	CPU & CHIPSET: Project Chipset Support
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
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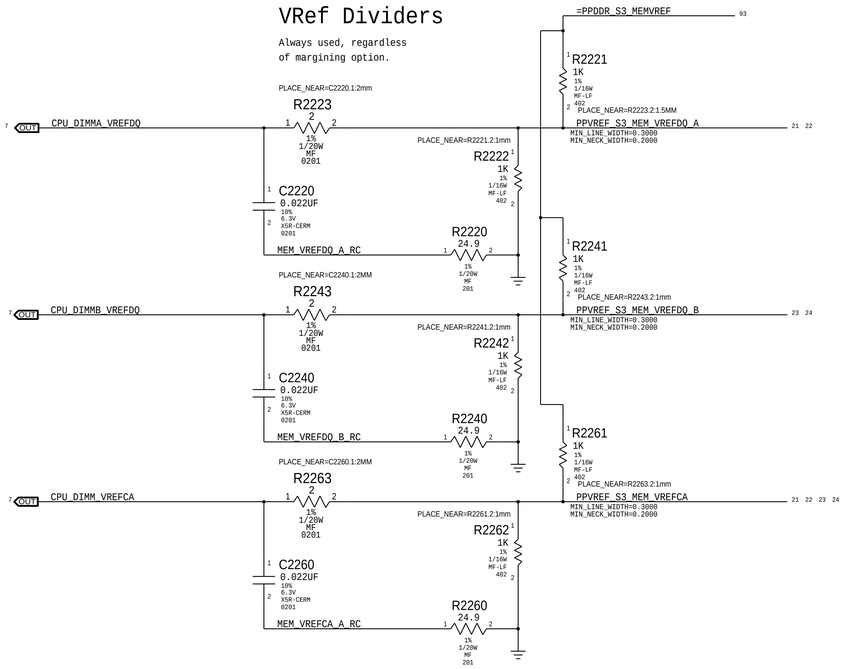
VRef Dividers

Always used, regardless
of margining option.



SYNC_MASTER=J78_DAVID SYNC_DATE=03/10/2014

PAGE TITLE

DRAM: VREF/VTT EN

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

J2300
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2
MTG HOLE
205
206
207
208
209

PPVREF_S3_MEM_VREFDQ_A

C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 16V CERM 402

J2300
CRITICAL
F-ANG-SM-1
SYM 1 OF 2
SODIMM-P0.60-D8

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

NC_0 = NC
NC_1 = NC
TEST = NC

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MEM_DIMM0_SA<1>

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MEM_RESET_L
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MEM_A_A<4>
MEM_A_A<2>
MEM_A_A<0>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>
MEM_A_BA<1>
MEM_A_RAS_L
MEM_A_CS_L<0>
MEM_A_ODT<0>
MEM_A_ODT<1>
=MEM_A_DQ<36>
=MEM_A_DQ<37>
=MEM_A_DQ<38>
=MEM_A_DQ<39>
=MEM_A_DQ<44>
=MEM_A_DQ<45>
=MEM_A_DQS_N<5>
=MEM_A_DQS_P<5>
=MEM_A_DQ<46>
=MEM_A_DQ<47>
=MEM_A_DQ<52>
=MEM_A_DQ<53>
=MEM_A_DQ<54>
=MEM_A_DQ<55>
=MEM_A_DQ<60>
=MEM_A_DQ<61>
=MEM_A_DQS_N<7>
=MEM_A_DQS_P<7>
=MEM_A_DQ<62>
=MEM_A_DQ<63>
MEM_EVENT_L
=I2C_SODIMMA_SDA
=I2C_SODIMMA_SCL

=PPVDDQ_S3_MEM_A

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

C2310 0.1UF 20% 16V X5R 402
C2311 0.1UF 20% 16V X5R 402
C2312 0.1UF 20% 16V X5R 402
C2313 0.1UF 20% 16V X5R 402
C2314 0.1UF 20% 16V X5R 402
C2315 0.1UF 20% 16V X5R 402
C2316 0.1UF 20% 16V X5R 402
C2317 0.1UF 20% 16V X5R 402
C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 16V X5R 402
C2319 0.1UF 20% 16V X5R 402
C2320 0.1UF 20% 16V X5R 402
C2321 0.1UF 20% 16V X5R 402
C2322 0.1UF 20% 16V X5R 402
C2323 0.1UF 20% 16V X5R 402

C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 16V CERM 402

C2350 1UF 10% 16V X5R 402
C2351 1UF 10% 16V X5R 402
C2352 1UF 10% 16V X5R 402
C2353 1UF 10% 16V X5R 402

=PPDDRVTT_S0_MEM_A

SYNC_MASTER=J78_NAT	SYNC_DATE=10/30/2013
PAGE TITLE	DRAM: SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-00321
	SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 23 OF 120
	SHEET 21 OF 96

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 1 OF 2
CRITICAL

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2

1	VREFDQ		2	VSS_0			
3	VSS_1		4	DQ4	=MEM_A_DQ<4>	BI	21 25
5	DQ0	=MEM_A_DQ<0>	6	DQ5	=MEM_A_DQ<5>	BI	21 25
7	DQ1	=MEM_A_DQ<1>	8	VSS_2			
9	VSS_3		10	DQS0*	=MEM_A_DQS_N<0>	BI	21 25
11	DM0		12	DQS0	=MEM_A_DQS_P<0>	BI	21 25
13	VSS_4		14	VSS_5			
15	DQ2	=MEM_A_DQ<2>	16	DQ6	=MEM_A_DQ<6>	BI	21 25
17	DQ3	=MEM_A_DQ<3>	18	DQ7	=MEM_A_DQ<7>	BI	21 25
19	VSS_6		20	VSS_7			
21	DQ8	=MEM_A_DQ<8>	22	DQ12	=MEM_A_DQ<12>	BI	21 25
23	DQ9	=MEM_A_DQ<9>	24	DQ13	=MEM_A_DQ<13>	BI	21 25
25	VSS_8		26	VSS_9			
27	DQS1*	=MEM_A_DQS_N<1>	28	DM1			
29	DQS1	=MEM_A_DQS_P<1>	30	RESET*	MEM_RESET_L	IN	12 21 23 24
31	VSS_10		32	VSS_11			
33	DQ10	=MEM_A_DQ<10>	34	DQ14	=MEM_A_DQ<14>	BI	21 25
35	DQ11	=MEM_A_DQ<11>	36	DQ15	=MEM_A_DQ<15>	BI	21 25
37	VSS_12		38	VSS_13			
39	DQ16	=MEM_A_DQ<16>	40	DQ20	=MEM_A_DQ<20>	BI	21 25
41	DQ17	=MEM_A_DQ<17>	42	DQ21	=MEM_A_DQ<21>	BI	21 25
43	VSS_14		44	VSS_15			
45	DQS2*	=MEM_A_DQS_N<2>	46	DM2			
47	DQS2	=MEM_A_DQS_P<2>	48	VSS_16			
49	VSS_17		50	DQ22	=MEM_A_DQ<22>	BI	21 25
51	DQ18	=MEM_A_DQ<18>	52	DQ23	=MEM_A_DQ<23>	BI	21 25
53	DQ19	=MEM_A_DQ<19>	54	VSS_18			
55	VSS_19		56	DQ28	=MEM_A_DQ<28>	BI	21 25
57	DQ24	=MEM_A_DQ<24>	58	DQ29	=MEM_A_DQ<29>	BI	21 25
59	DQ25	=MEM_A_DQ<25>	60	VSS_20			
61	VSS_21		62	DQS3*	=MEM_A_DQS_N<3>	BI	21 25
63	DM3		64	DQS3	=MEM_A_DQS_P<3>	BI	21 25
65	VSS_22		66	VSS_23			
67	DQ26	=MEM_A_DQ<26>	68	DQ30	=MEM_A_DQ<30>	BI	21 25
69	DQ27	=MEM_A_DQ<27>	70	DQ31	=MEM_A_DQ<31>	BI	21 25
71	VSS_24		72	VSS_25			
	KEY						
73	CKE0	MEM_A_CKE<2>	74	CKE1	MEM_A_CKE<3>	IN	7
75	VDD_0		76	VDD_1			
77	NC_0	NCX	78	A15	MEM_A_A<15>	IN	7 21
79	BA2	MEM_A_BA<2>	80	A14	MEM_A_A<14>	IN	7 21
81	VDD_2		82	VDD_3			
83	A12/BC*	MEM_A_A<12>	84	A11	MEM_A_A<11>	IN	7 21
85	A9	MEM_A_A<9>	86	A7	MEM_A_A<7>	IN	7 21
87	VDD_4		88	VDD_5			
89	A8	MEM_A_A<8>	90	A6	MEM_A_A<6>	IN	7 21
91	A5	MEM_A_A<5>	92	A4	MEM_A_A<4>	IN	7 21
93	VDD_6		94	VDD_7			
95	A3	MEM_A_A<3>	96	A2	MEM_A_A<2>	IN	7 21
97	A1	MEM_A_A<1>	98	A0	MEM_A_A<0>	IN	7 21
99	VDD_8		100	VDD_9			
101	CK0	MEM_A_CLK_P<2>	102	CK1	MEM_A_CLK_P<3>	IN	7
103	CK0*	MEM_A_CLK_N<2>	104	CK1*	MEM_A_CLK_N<3>	IN	7
105	VDD_10		106	VDD_11			
107	A10_AP	MEM_A_A<10>	108	BA1	MEM_A_BA<1>	IN	7 21
109	BA0	MEM_A_BA<0>	110	RAS*	MEM_A_RAS_L	IN	7 21
111	VDD_12		112	VDD_13			
113	WE*	MEM_A_WE_L	114	S0*	MEM_A_CS_L<2>	IN	7
115	CAS*	MEM_A_CAS_L	116	ODT0	MEM_A_ODT<2>	IN	7
117	VDD_14		118	VDD_15			
119	A13	MEM_A_A<13>	120	ODT1	MEM_A_ODT<3>	IN	7
121	S1*	MEM_A_CS_L<3>	122	NC_1	NCX		
123	VDD_16		124	VDD_17			
125	TEST	NCX	126	VREFCA	PPVREF_S3_MEM_VREFCA		20 21 23 24
127	VSS_26		128	VSS_27			
129	DQ32	=MEM_A_DQ<32>	130	DQ36	=MEM_A_DQ<36>	BI	21 25
131	DQ33	=MEM_A_DQ<33>	132	DQ37	=MEM_A_DQ<37>	BI	21 25
133	VSS_28		134	VSS_29			
135	DQS4*	=MEM_A_DQS_N<4>	136	DM4			
137	DQS4	=MEM_A_DQS_P<4>	138	VSS_30			
139	VSS_31		140	DQ38	=MEM_A_DQ<38>	BI	21 25
141	DQ34	=MEM_A_DQ<34>	142	DQ39	=MEM_A_DQ<39>	BI	21 25
143	DQ35	=MEM_A_DQ<35>	144	VSS_32			
145	VSS_33		146	DQ44	=MEM_A_DQ<44>	BI	21 25
147	DQ40	=MEM_A_DQ<40>	148	DQ45	=MEM_A_DQ<45>	BI	21 25
149	DQ41	=MEM_A_DQ<41>	150	VSS_34			
151	VSS_35		152	DQS5*	=MEM_A_DQS_N<5>	BI	21 25
153	DM5		154	DQS5	=MEM_A_DQS_P<5>	BI	21 25
155	VSS_36		156	VSS_37			
157	DQ42	=MEM_A_DQ<42>	158	DQ46	=MEM_A_DQ<46>	BI	21 25
159	DQ43	=MEM_A_DQ<43>	160	DQ47	=MEM_A_DQ<47>	BI	21 25
161	VSS_38		162	VSS_39			
163	DQ48	=MEM_A_DQ<48>	164	DQ52	=MEM_A_DQ<52>	BI	21 25
165	DQ49	=MEM_A_DQ<49>	166	DQ53	=MEM_A_DQ<53>	BI	21 25
167	VSS_40		168	VSS_41			
169	DQS6*	=MEM_A_DQS_N<6>	170	DM6			
171	DQS6	=MEM_A_DQS_P<6>	172	VSS_42			
173	VSS_43		174	DQ54	=MEM_A_DQ<54>	BI	21 25
175	DQ50	=MEM_A_DQ<50>	176	DQ55	=MEM_A_DQ<55>	BI	21 25
177	DQ51	=MEM_A_DQ<51>	178	VSS_44			
179	VSS_45		180	DQ60	=MEM_A_DQ<60>	BI	21 25
181	DQ56	=MEM_A_DQ<56>	182	DQ61	=MEM_A_DQ<61>	BI	21 25
183	DQ57	=MEM_A_DQ<57>	184	VSS_46			
185	VSS_47		186	DQS7*	=MEM_A_DQS_N<7>	BI	21 25
187	DM7		188	DQS7	=MEM_A_DQS_P<7>	BI	21 25
189	VSS_48		190	VSS_49			
191	DQ58	=MEM_A_DQ<58>	192	DQ62	=MEM_A_DQ<62>	BI	21 25
193	DQ59	=MEM_A_DQ<59>	194	DQ63	=MEM_A_DQ<63>	BI	21 25
195	VSS_50		196	VSS_51			
197	SA0	MEM_DIMM1_SA<0>	198	EVENT*	MEM_EVENT_L	OUT	21 23 24 43 44
199	VDDSPD	=PP3V3_S0_MEM_A_SPD	200	SDA	=I2C_SODIMMA_SDA	BI	21 46
201	SA1	MEM_DIMM1_SA<1>	202	SCL	=I2C_SODIMMA_SCL	IN	21 46
203	VTT_0		204	VTT_1			

205	MTG HOLE	
206		
207		
208		
209		

=PPVDDQ_S3_MEM_A (93 22 21) — C2410 0.1UF, C2411 0.1UF, C2412 0.1UF, C2413 0.1UF, C2414 0.1UF, C2415 0.1UF, C2416 0.1UF, C2417 0.1UF; C2400 10UF, C2401 10UF, C2418 0.1UF, C2419 0.1UF, C2420 0.1UF, C2421 0.1UF, C2422 0.1UF, C2423 0.1UF

=PP3V3_S0_MEM_A_SPD (93 22 21) — R2440 10K 5% 1/16W MF-LF 402 — MEM_DIMM1_SA<0> (22)

MEM_DIMM1_SA<1> (22) — =PP3V3_S0_MEM_A_SPD (93 22 21) — C2440 2.2UF 20% 6.3V CERM 402-LF — R2441 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A (93 22 21) — C2400 10UF 20% 6.3V X5R 603, C2401 10UF 20% 6.3V X5R 603, C2418 0.1UF 10% 16V CERM 402, C2419 0.1UF 10% 16V CERM 402, C2420 0.1UF 10% 16V CERM 402, C2421 0.1UF 10% 16V CERM 402, C2422 0.1UF 10% 16V CERM 402, C2423 0.1UF 10% 16V CERM 402

PPVREF_S3_MEM_VREFDQ (21 20) — C2430 2.2UF 20% 6.3V CERM 402-LF, C2431 0.1UF 10% 16V CERM 402

PPVREF_S3_MEM_VREFCA (20 21 23 24) — C2435 2.2UF 20% 6.3V CERM 402-LF, C2436 0.1UF 10% 16V CERM 402

=PPDDRVTT_S0_MEM_A (21 22 93) — C2450 1UF 10% 10V X5R 402, C2451 1UF 10% 10V X5R 402, C2452 1UF 10% 10V X5R 402, C2453 1UF 10% 10V X5R 402

=PPVDDQ_S3_MEM_A (21 22 93)

SYNC_MASTER=J78_NAT SYNC_DATE=10/30/2013

PAGE TITLE: DRAM: SO-DIMM Connector A Slot1

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D

REVISION: 4.0.0

BRANCH: proto1b

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SHEET: 22 OF 96

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

PPVREF_S3_MEM_VREFDQ_B
VOLTAGE=0.675V

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 0.1UF 20% 10V CERM 402

J2500 CRITICAL
F-ANG-SM-1
SODIMM-P0.60-D8
SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	2.2K NC	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

SODIMM-P0.60-D8
SYM 2 OF 2
MTG HOLE
205 206 207 208 209

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402
C2514 0.1UF 20% 10V CERM 402
C2515 0.1UF 20% 10V CERM 402
C2516 0.1UF 20% 10V CERM 402
C2517 0.1UF 20% 10V CERM 402
C2500 10UF 20% 6.3V X5R 603
C2501 10UF 20% 6.3V X5R 603
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402
C2520 0.1UF 20% 10V CERM 402
C2521 0.1UF 20% 10V CERM 402
C2522 0.1UF 20% 10V CERM 402
C2523 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD
R2541 10K 5% 1/16W MF-LF 402
MEM_DIMM2_SA<1>
MEM_DIMM2_SA<0>
=PP3V3_S0_MEM_B_SPD
C2540 2.2UF 20% 6.3V CERM 402-LF
R2540 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_B

C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 20% 10V CERM 402
C2550 1UF 10% 10V X5R 402
C2551 1UF 10% 10V X5R 402
C2552 1UF 10% 10V X5R 402
C2553 1UF 10% 10V X5R 402

SYNC_MASTER=J78_NAT	SYNC_DATE=10/30/2013
PAGE TITLE	DRAM: SO-DIMM CONNECTOR B SLOT0
Apple Inc.	DRAWING NUMBER 051-00321
	SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

=PPVREF_S3_MEM_VREFDQ_B
VOLTAGE=0.675V

C2630 2.2UF 20% 6.3V CERM 402-LF
C2631 0.1UF 20% 10V CERM 402

J2600 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 1 OF 2 CRITICAL

1	VREFDQ		2	VSS_0	
3	VSS_1		4	DQ4	=MEM_B_DQ<4>
5	DQ0	=MEM_B_DQ<0>	6	DQ5	=MEM_B_DQ<5>
7	DQ1	=MEM_B_DQ<1>	8	VSS_2	
9	VSS_3		10	DQS0*	=MEM_B_DQS_N<0>
11	DM0		12	DQS0	=MEM_B_DQS_P<0>
13	VSS_4		14	VSS_5	
15	DQ2	=MEM_B_DQ<2>	16	DQ6	=MEM_B_DQ<6>
17	DQ3	=MEM_B_DQ<3>	18	DQ7	=MEM_B_DQ<7>
19	VSS_6		20	VSS_7	
21	DQ8	=MEM_B_DQ<8>	22	DQ12	=MEM_B_DQ<12>
23	DQ9	=MEM_B_DQ<9>	24	DQ13	=MEM_B_DQ<13>
25	VSS_8		26	VSS_9	
27	DQS1*	=MEM_B_DQS_N<1>	28	DM1	
29	DQS1	=MEM_B_DQS_P<1>	30	RESET*	MEM_RESET_L
31	VSS_10		32	VSS_11	
33	DQ10	=MEM_B_DQ<10>	34	DQ14	=MEM_B_DQ<14>
35	DQ11	=MEM_B_DQ<11>	36	DQ15	=MEM_B_DQ<15>
37	VSS_12		38	VSS_13	
39	DQ16	=MEM_B_DQ<16>	40	DQ20	=MEM_B_DQ<20>
41	DQ17	=MEM_B_DQ<17>	42	DQ21	=MEM_B_DQ<21>
43	VSS_14		44	VSS_15	
45	DQS2*	=MEM_B_DQS_N<2>	46	DM2	
47	DQS2	=MEM_B_DQS_P<2>	48	VSS_16	
49	VSS_17		50	DQ22	=MEM_B_DQ<22>
51	DQ18	=MEM_B_DQ<18>	52	DQ23	=MEM_B_DQ<23>
53	DQ19	=MEM_B_DQ<19>	54	VSS_18	
55	VSS_19		56	DQ28	=MEM_B_DQ<28>
57	DQ24	=MEM_B_DQ<24>	58	DQ29	=MEM_B_DQ<29>
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61	VSS_21		62	DQS3*	=MEM_B_DQS_N<3>
63	DM3		64	DQS3	=MEM_B_DQS_P<3>
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77	NC_0	NC	78	A15	MEM_B_A<15>
79	BA2	MEM_B_BA<2>	80	A14	MEM_B_A<14>
81	VDD_2		82	VDD_3	
83	A12/BC*	MEM_B_A<12>	84	A11	MEM_B_A<11>
85	A9	MEM_B_A<9>	86	A7	MEM_B_A<7>
87	VDD_4		88	VDD_5	
89	A8	MEM_B_A<8>	90	A6	MEM_B_A<6>
91	A5	MEM_B_A<5>	92	A4	MEM_B_A<4>
93	VDD_6		94	VDD_7	
95	A3	MEM_B_A<3>	96	A2	MEM_B_A<2>
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99	VDD_8		100	VDD_9	
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103	CK0*	MEM_B_CLK_N<2>	104	CK1*	MEM_B_CLK_N<3>
105	VDD_10		106	VDD_11	
107	A10_AP	MEM_B_A<10>	108	BA1	MEM_B_BA<1>
109	BA0	MEM_B_BA<0>	110	RAS*	MEM_B_RAS_L
111	VDD_12		112	VDD_13	
113	WE*	MEM_B_WE_L	114	S0*	MEM_B_CS_L<2>
115	CAS*	MEM_B_CAS_L	116	ODT0	MEM_B_ODT<2>
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119	A13	MEM_B_A<13>	120	ODT1	MEM_B_ODT<3>
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123	VDD_16		124	VDD_17	
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127	VSS_26		128	VSS_27	
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137	DQS4	=MEM_B_DQS_P<4>	138	VSS_30	
139	VSS_31		140	DQ38	=MEM_B_DQ<38>
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201	SA1	MEM_DIMM3_SA<1>	202	SCL	=I2C_SODIMMB_SCL
203	VTT_0		204	VTT_1	

J2600 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2
205 206 207 208 209 MTG HOLE

=PPVDDQ_S3_MEM_B

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

C2610 C2611 C2612 C2613 C2614 C2615 C2616 C2617 0.1UF 20% 10V CERM 402
C2600 10UF 20% 6.3V X5R 603
C2601 10UF 20% 6.3V X5R 603
C2618 C2619 C2620 C2621 C2622 C2623 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD
R2641 10K 5% 1/16W MF-LF 402
R2640 10K 5% 1/16W MF-LF 402
MEM_DIMM3_SA<1>
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C2640 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B

C2635 2.2UF 20% 6.3V CERM 402-LF
C2636 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B
C2650 C2651 C2652 C2653 1UF 10% 10V X5R 402

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Apple Inc.	DRAWING NUMBER 051-00321
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	REVISION 4.0.0
	BRANCH proto1b
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	SHEET 24 OF 96

THERE ARE NO PIN SWAPS

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PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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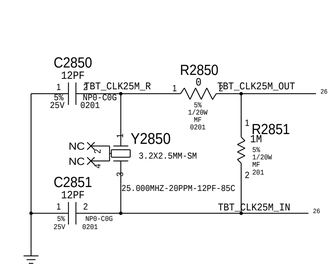
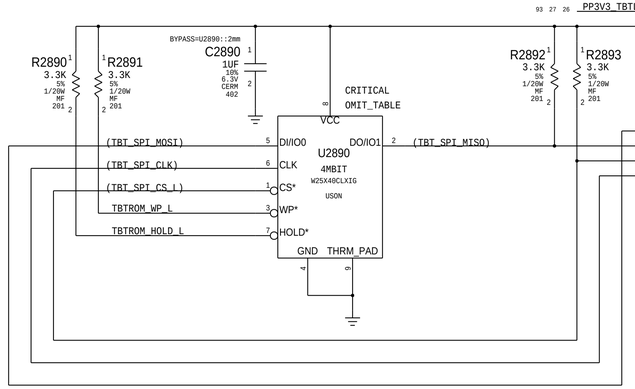
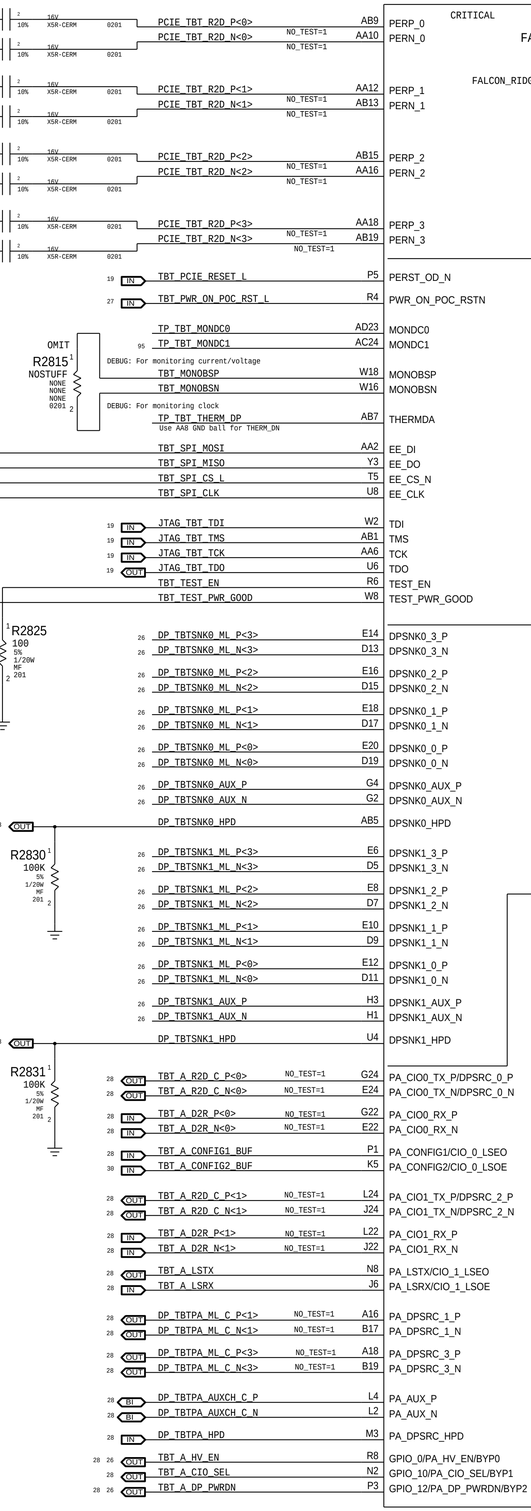
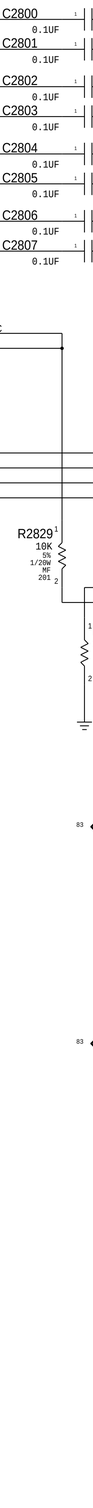
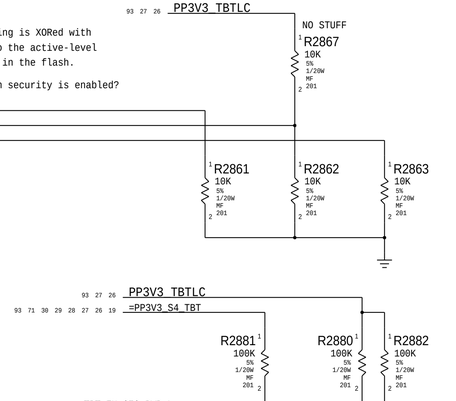


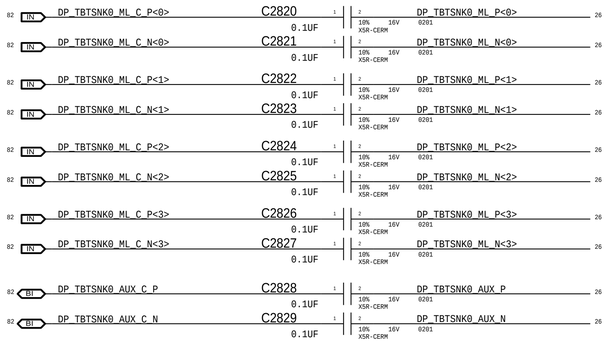




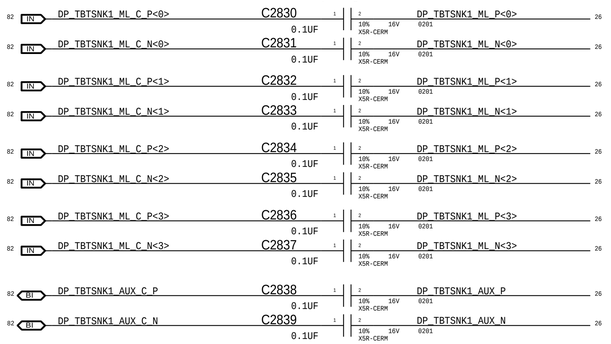




SNK0 AC Coupling



SNK1 AC Coupling



For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=11/06/2014

PAGE TITLE: TBT/DP: Host (1 of 2)

Apple Inc.

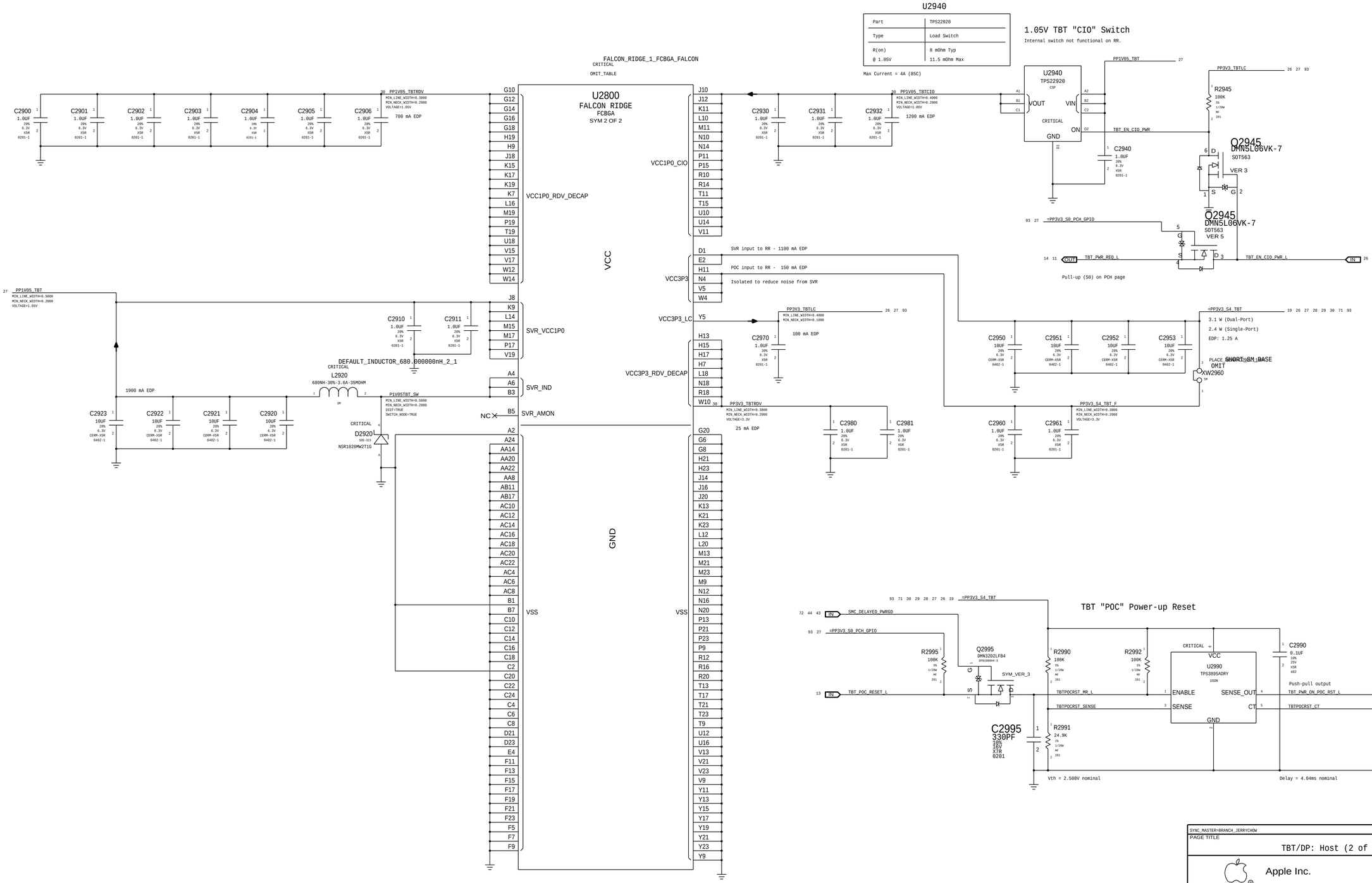
DRAWING NUMBER: 051-00321 SIZE: D

REVISION: 4.0.0

BRANCH: proto1b

PAGE: 28 OF 120

SHEET: 26 OF 96



SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE

TBT/DP: Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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SHEET 27 OF 96

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM CRITICAL
C3280 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL
C3281 0.1UF 20% 10V CERM 402

=PPHV_SW_TBTAPWRSW
18.9V Max
C3215 4.7UF 10% 25V 0603 X5R-CERM
C3210 0.1UF 10% 50V X7R 603-1

353S3931
U3210
CD3211A1RGP
QFN

19	V3P3	V3P3OUT	18
20			
		NC	12
6	VHV	OUT	14
7			
16	ENHVU	FAULTZ	4
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
	GND	THRM PAD	21

PP3V3RHV_S4_TBTAPWR
C3211 0.1UF 10% 50V X7R 603-1
C3200 0.01UF 10% 50V X7R-CERM 0402
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=15V

L3200
FERR-120-OHM-3A
0603 CRITICAL
PP3V3RHV_S4_TBTAPWR_F
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.3800
VOLTAGE=15V

=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

R3210 35.7K 1% 1/20W MF 201
R3211 35.7K 1% 1/20W MF 201
R3212 36.5K 1% 1/16W MF-LF 402

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

(Both C's)
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
C3274 0.47UF 20% 4V CERM-X5R-1 201
C3275 0.47UF 20% 4V CERM-X5R-1 201
GND_VOID=TRUE
NO_TEST=1

NOTE: Polarity Swapped for layout!

TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT Dir
DP Dir
TBT : RX_0
DEFAULT_RESISTOR_0.001OHM_2_1
R3291 0 5% 1/20W MF 201
TBT_A_HPD_R
TBT_A_HPD

C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
TBT: Terminated
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: UNUSED
R3294 1K 1% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
NO_XNET_CONNECTION=1
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT : RX_1
R3201 12 5% 1/20W MF 201
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V

TBT_A_CONFIG2_RC_R
DEFAULT_RESISTOR_0.001OHM_2_1
R3292 0 5% 1/20W MF 201
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201

R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_20_RC
C3201 0.01UF 10% 50V X7R-CERM 0402

DP Source must pull
down HPD input with
greater than or equal
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
to 100K (DPv1.1a).

CRITICAL
J3200
DUAL-MDP-D8
CON_F40ANG_250U_DUAL_TH_F_ANG_TH_DUAL_MDP_D8
SHLD
F-ANG-TH

2	HPD	GND0	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND2	GND1	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND4	GND3	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19
	PORT A SHLD		

TBTACONN_1_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V
C3206 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)

TBTACONN_7_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V
C3205 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)

TBT: TX_0
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)

TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
R3271 470K 5% 1/20W MF 201
R3270 470K 5% 1/20W MF 201

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3273 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201

(Both C's)
NOTE: Polarity Swapped for layout!

470k R's for ESD protection
on AC-coupled signals.

=PP3V3_S4_TBT
C3220 0.1UF 10% 6.3V 0201 CERM-X5R
C3221 0.1UF 10% 6.3V 0201 CERM-X5R
SIGNAL_MODEL=CBTL05024_HVQFN24_COMBO_CBTL05024_TBT

353S3812
U3220
CBTL05024
HVQFN24-COMBO
VDD
CRITICAL

TBT_A_D2R_N<1>		TB-	7
TBT_A_D2R_P<1> (Both C's)		TB+	8
DP_TBTPA_AUXCH_C_N		AUX-	1
DP_TBTPA_AUXCH_C_P		AUX+	2
DP_TBTP_A_DDC_DATA		DDC_DAT	4
DP_TBTP_A_DDC_CLK		DDC_CLK	5
TBT_A_CONFIG1_BUF		CA_DETOUT	16
DP_TBTPA_ML_P<1>		DP+	11
DP_TBTPA_ML_N<1>		DP-	10
		LSTX	14
TBT_A_LSRX		LSRX	13
DP_TBTPA_HPD		HPDOUT	12
		TB_ENA	15
		AUXIO_EN	24
		DP_PD	6
		AUXIO-	23
		AUXIO+	22
		CA_DET	18
		DPMLO+	19
		DPMLO-	20
		HPD	17
		GND THMPAD	9, 21, 25

TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD

Thunderbolt Connector A

514-0831

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE: TBT/DP: Connector A

Apple Inc.

DRAWING NUMBER	051-00321
SIZE	D
REVISION	4.0.0
BRANCH	proto1b
PAGE	32 OF 120
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM CRITICAL
C3380 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL
C3381 0.1UF 10% 10V CERM 402
353S3931
U3310 CD3211A1RGP QFN
V3P3OUT NC
V3P3 CRITICAL
OUT PP3V3RHV_S4_TBTBPWR
L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F
MIN_LINE_WIDTH=0.3800 MIN_NECK_WIDTH=0.2000 VOLTAGE=15V
C3311 0.1UF 10% 50V X7R 603-1
C3300 0.01UF 10% 50V X7R-CERM 0402
=PPHV_SW_TBTBPWRSW
18.9V Max
C3315 4.7UF 10% 25V 0603 X5R-CERM
C3310 0.1UF 10% 50V X7R 603-1
VHV
ENHVU
FAULTZ
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
EN
HV_EN
S0
ISET_V3P3 TBTBPWRSW_ISET_V3P3
ISET_S0 TBTBPWRSW_ISET_S0
ISET_S3 TBTBPWRSW_ISET_S3
GND
THRM PAD
R3310 35.7K 1% 1/20W MF 201
R3311 35.7K 1% 1/20W MF 201
R3312 36.5K 1% 1/10W MF-LF 402

BAUER3 ISET no can limit current to 3.1A if Rset is shorted to GND FOR SINGLE-FAULT PROTECTIO

	NORMINAL	MIN	MAX	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

=PP3V3_S4_TBT
C3320 0.1UF 10% 6.3V 0201 CERM-X5R
C3321 0.1UF 10% 6.3V 0201 CERM-X5R
353S3812
U3320 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=CBTL05024_HVQFN24_COMBO_CBTL05024_TBT
VDD
TB- TB+ AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX LSRX HPDOUT GND_THMPAD
TB_ENA AUXIO_EN DP_PD AUXIO- AUXIO+ CA_DET DPMLO+ DPMLO- HPD
TBT_B_CIO_SEL TBTDP_AUXIO_EN TBT_B_DP_PWRDN TBT_B_D2R1_AUXDDC_N TBT_B_D2R1_AUXDDC_P TBT_B_CONFIG1_RC TBT_B_LSX_ML_P<1> TBT_B_LSX_ML_N<1> TBT_B.HPD
TBT: RX_1
TBT: LSX_B_R2P/P2R (P/N)

TBT_B_D2R_N<1> TBT_B_D2R_P<1> (Both C's)
C3377 0.47UF
C3376 0.47UF
TBT_B_D2R_C_N<1> TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_C_N DP_TBTPB_AUXCH_C_P
C3330 0.1UF
C3331 0.1UF
DP_TBTPB_AUXCH_N DP_TBTPB_AUXCH_P
DP_TBTP_B_DDC_DATA DP_TBTP_B_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1> DP_TBTPB_ML_C_N<1>
C3332 0.22UF
C3333 0.22UF
DP_TBTPB_ML_P<1> DP_TBTPB_ML_N<1>
TBT_B_LSTX TBT_B_LSRX DP_TBTPB_HPD
TBT: TX_1
TBTBCONN_1_C
TBTBCONN_7_C
C3306 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
C3305 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
C3370 0.22UF
C3371 0.22UF
TBT_B_R2D_C_P<0> TBT_B_R2D_N<0> TBT_B_R2D_C_N<0> TBT_B_R2D_C_P<0>
(Both C's)
R3371 470K 5% 1/20W MF 201
R3370 470K 5% 1/20W MF 201
TBT: TX_0
C3372 0.22UF
C3373 0.22UF
TBT_B_R2D_P<1> TBT_B_R2D_N<1> TBT_B_R2D_C_N<1> TBT_B_R2D_C_P<1>
(Both C's)
R3373 470K 5% 1/20W MF 201
R3372 470K 5% 1/20W MF 201
470k R's for ESD protection
on AC-coupled signals.
NOTE: Polarity Swapped for layout!

NOTE: Polarity Swapped for layout!
TBT_B_HPD
R3391 0 5% 1/20W MF 201 TBT_B_HPD_R
DEFAULT_RESISTOR_0.001OHM_2_1
TBT : RX_0
TBT_B_D2R_N<0> TBT_B_D2R_P<0>
C3374 0.47UF
C3375 0.47UF
TBT_B_D2R_C_P<0> TBT_B_D2R_C_N<0>
TBT Dir DP Dir
TBT: UNUSED
DP_TBTPB_ML_C_P<3> DP_TBTPB_ML_C_N<3>
C3378 0.22UF
C3379 0.22UF
TBT: Terminated
R3394 1K 1/20W 5% MF 201
R3395 1K 1/20W 5% MF 201
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
NO_XNET_CONNECTION=1
TBT_B_D2R1_AUXDDC_P TBT_B_D2R1_AUXDDC_N
TBT : RX_1
R3301 12 1/20W 5% MF 201
TBTBCONN_20_RC
TBT_B_CONFIG2_RC_R
DEFAULT_RESISTOR_0.001OHM_2_1
R3392 0 5% 1/20W MF 201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 25V X5R-CERM 0201
C3301 0.01UF 10% 50V X7R-CERM 0402
TBT_B_CONFIG1_RC TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R 0201
C3395 330PF 10% 16V X7R 0201

DP Source must pull
down HPD input with
greater than or equal
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
to 100K (DPv1.1a).

THUNDERBOLT CONNECTOR B

514-0831

CRITICAL
J3200 DUAL-MDP-D8 F-ANG-TH
CON_F40ANG_25MT_MDP_DUAL_TH_F_ANG_TH_DUAL_MDP_D8
SHLD
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
GND0 ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT B

SYNC_MASTER=BRANCH_JERRYCHOW	SYNC_DATE=09/10/2014	
PAGE TITLE: TBT/DP: Connector B		
Apple Inc.	DRAWING NUMBER: 051-00321	SIZE: D
	REVISION: 4.0.0	
	BRANCH: proto1b	
	PAGE: 33 OF 120	
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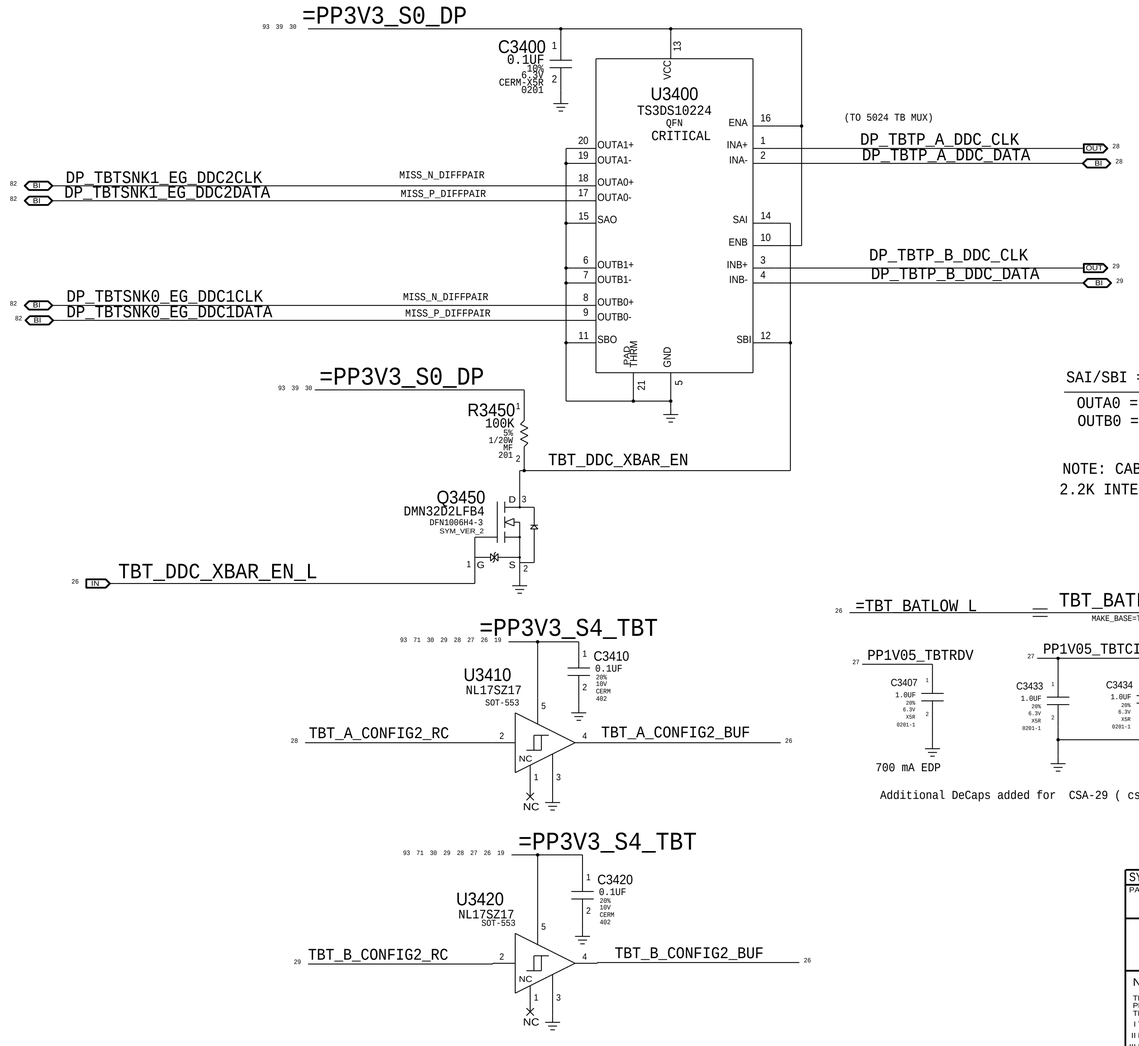
Dual-Port Host DDC Crossbar



SAI/SBI =	0	1
OUTA0 =	INB	INA
OUTB0 =	INA	INB

NOTE: CABLE ADAPTERS ARE REQUIRED TO HAVE 2.2K INTERNAL PULL-UPS.

Additional DeCaps added for CSA-29 (csa-29 is syncing from J44)

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=11/05/2014

PAGE TITLE

TBT/DP: DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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AIRPORT
BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

=PP3V3_S4_AP
U3510
TPS22924
CSP
A2 VIN
B2
C2 ON
A1 VOUT
B1
GND
CRITICAL
C1
AP_PWR_EN
PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
CRITICAL
L3502
FERR-220-OHM-2.5A
0603
PP3V3_S4_AP_FLT
C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V
514S0335
CRITICAL
J3500
SSD-K99
F-RT-SM1
AP_EVENT_L
PCIE_AP_R2D_C_N
C3505 0.1UF 10% 6.3V X5R-CERM 0201
PCIE_AP_R2D_C_P
C3506 0.1UF 10% 6.3V X5R-CERM 0201
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P
=PP3V3_G3H_BT
U3540
TPS22924B
CSP
SMC_BT_PWR_EN
PP3V3_G3H_BT_FET
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
CRITICAL
L3501
FERR-220-OHM-2.5A
0603
PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L
CRITICAL
Q3501
SOD
=PP3V3_G3H_BT
C3500 0.1UF 10% 10V X5R-CERM 0201
U3501
USB3740
DFN
CRITICAL
USB_BT_N
USB_BT_P
USB_BT_WAKEN
PM_SLP_S5_L
NC
DP_2
DM_2
DP_1
DM_1
OE*
S
DP
DM
GND
USB_BT_MUX_N
USB_BT_MUX_P
R3501 15K 1% 1/20W MF 201
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K 1% 1/10W MF-LF 402
R3531 232K 1% 1/10W MF-LF 402
CRITICAL
U3530
SLG4AP041V
TDFN
C3530 0.1uF 20% 10V CERM 402
P3V3AP_VMON
SENSE
VREF
DLY
AP_RESET_CONN_R_L
R3533 33 5% 1/20W MF 201
RESET*
MR*
EN
OUT
IN
THRM PAD
GND
AP_RESET_CONN_L
AP_CLKREQ_Q_L
AP_RESET_L
AP_PWR_EN
AP_CLKREQ
R3532 100K 1% 1/10W MF-LF 402

PP3V3_S4_AP_FLT
CRITICAL
Q3570
R3570 10K 5% 1/10W MF-LF 402
PCIE_WAKE_L
AP_WAKE_L

SYNC_MASTER=J16_IG	SYNC_DATE=04/29/2013
PAGE TITLE	WIRELESS: Airport/Bluetooth
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 35 OF 120
	SHEET 31 OF 96

PPVSSD S4 FET

93 65 32 =PP3V3_S5_SSD_PWRCTL
C3782 0.1UF 10% 6.3V CERM-X5R 0201
PM_EPO_L N-FET INVERTER ON CSA 76
65 IN PM_EPO
SN74LVC1G02 SOT553-5 U3782
IN PM_PGOOD_REG_P5V_S4
R3782 0 5% MF-LF 1/16W 402
PM_PGOOD_REG_P5V_S4_R
PM_EN_FET_P3V3_S4_SSD 32
NOSTUFF C3783 0.47UF 10% 6.3V CERM-X5R 402

CRITICAL 376S0981 Q3771 IRLHS6242TRPBF PQFN2X2
93 =PPVSSD_S5_FET_S4_SSD
PP3V3_S4_FET_SSD OUT 93
93 70 =PP12V_S5_FET_PWRCTL
R3791 10K 5% 1/16W MF-LF 402
R3793 0 5% MF-LF 1/16W 402
P3V3SSD_S4
PM_EN_SSD_L
R3792 100K 5% 1/16W MF-LF 402
C3792 0.01UF 10% 50V 0402 X7R-CERM
CRITICAL Q3772 2N7002DW-X-G SOT-363
32 PM_EN_FET_P3V3_S4_SSD
NOSTUFF R3795 100K 5% 1/16W MF-LF 402
CRITICAL Q3772 2N7002DW-X-G SOT-363
NC NC NC NC

HDD SIGNAL CONNECTOR

J3720
SILK_PART=HDD
CRITICAL
PSA127-0747-A01-1H
M-ST-SM
518S0893
GND_VOID=TRUE
SATA_HDD_R2D_P
SATA_HDD_R2D_N
SATA_HDD_D2R_C_N
SATA_HDD_D2R_C_P
C3721 0.01UF 10% 25V X7R 402 GND_VOID=TRUE
C3722 0.01UF 10% 25V X7R 402 GND_VOID=TRUE
C3723 0.01UF 10% 25V X7R 402 GND_VOID=TRUE
C3724 0.01UF 10% 25V X7R 402 GND_VOID=TRUE
SATA_HDD_R2D_C_P IN 13
SATA_HDD_R2D_C_N IN 13
SATA_HDD_D2R_N OUT 13
SATA_HDD_D2R_P OUT 13

SATA Activity LED

93 =PP3V3_S0_LED_SATA
DEVELOPMENT R3799 330 5% 1/10W MF-LF 603
SATALED_R_L
DEVELOPMENT DS3799 GRN-6MCD-0.03A 0805
17 13 PCH_SATALED_L
SILK_PART=SATA ACTIVE

93 65 32 =PP3V3_S5_SSD_PWRCTL
C3781 0.1UF 10% 6.3V CERM-X5R 0201
93 72 71 65 =PP3V3_S5_PWRCTL
U3781 TC7SZ08FEAPE SOT665
71 70 65 59 32 IN PM_EPO_L
SSD_ISOL_FET_GATE 32

152S1060
L3700 CRITICAL
PLACE_NEAR=J3700.1:10.1MM
0.22UH+/-20%-0.006OHM-9A
PIMB042T-SM
93 =PPVSSD_S4_CONN
SSD:Y
C3701 0.1UF 20% 10V CERM 402
C3700 0.1UF 20% 10V CERM 402
PP3V3_S4_SSD_FLT 32
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V

GS3 SSD

J3700
SSD:Y
SILK_PART=SSD
CRITICAL
SSD-J90
F-RT-SM

SSD_ISOL_FET_GATE 32
PP3V3_S4_SSD_FLT 32
R3772 10K 5% 1/16W MF-LF 402
SSD_SR_EN_L IN 13
LPSR_EN_L 32
NOSTUFF R3776 10K 5% 1/16W MF-LF 402
SOT563 DMN5L06VK-7 VER 1 Q3770
R3773 0 5% 1/20W MF 0201 NOSTUFF

SSD_ISOL_FET_GATE 32
PP3V3_S4_SSD_FLT 32
R3770 10K 5% 1/16W MF-LF 402
SSD_RESET_L IN 19
PCH_SSD_RESET_L IN 14 13
R3790 0 5% 1/20W MF 0201
STORAGE_RESET_L 32
SOT563 DMN5L06VK-7 VER 1 Q3770
R3771 0 5% 1/20W MF 0201 NOSTUFF

R3719 0 5% MF-LF 1/16W 402 SSD:Y
32 LPSR_EN_L LPSR_EN_R_L
R3775 0 5% MF-LF 1/16W 402 SSD:Y
32 STORAGE_RESET_L STORAGE_RESET_R_L
14 13 SSD_BFH_L R3720 0 5% MF-LF 1/16W 402 SSD_BFH_R_L

PCIE TX3 (POLARITY REVERSED)

PCIE_SSD_R2D_P<3> IN 13
PCIE_SSD_R2D_N<3> IN 13
C3717 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.11:5MM
C3716 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.12:5MM

PCIE TX2

PCIE_SSD_R2D_N<2> IN 13
PCIE_SSD_R2D_P<2> IN 13
C3715 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.14:5MM
C3714 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.15:5MM

PCIE TX1 (POLARITY REVERSED)

PCIE_SSD_R2D_P<1> IN 13
PCIE_SSD_R2D_N<1> IN 13
C3711 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.19:5MM
C3710 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.19:5MM

PCIE TX0

PCIE_SSD_R2D_N<0> IN 13
PCIE_SSD_R2D_P<0> IN 13
C3713 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.21:5MM
C3712 0.22UF 20% 6.3V X5R 0201 SSD:Y GND_VOID=TRUE PLACE_NEAR=J3700.22:5MM

11 SSD_CLKREQ_L

PCIE_SSD_R2D_C_P<3>
PCIE_SSD_R2D_C_N<3>
PCIE_SSD_R2D_C_N<2>
PCIE_SSD_R2D_C_P<2>
PCIE_SSD_R2D_C_P<1>
PCIE_SSD_R2D_C_N<1>
PCIE_SSD_R2D_C_N<0>
PCIE_SSD_R2D_C_P<0>
GND_VOID=TRUE

SMC_OOB2_R2D_L
SMC_OOB2_D2R_L
SSD_V_SEL
PM_EPO_L
SSD_PWR_EN
NC
IN 32 59 65 70 71
IN 13 14

PCIE_SSD_D2R_P<3>
PCIE_SSD_D2R_N<3>
PCIE_SSD_D2R_P<2>
PCIE_SSD_D2R_N<2>
PCIE_SSD_D2R_P<1>
PCIE_SSD_D2R_N<1>
PCIE_SSD_D2R_P<0>
PCIE_SSD_D2R_N<0>
GND_VOID=TRUE
OUT 13

PCIE_CLK100M_SSD_N IN 11
PCIE_CLK100M_SSD_P IN 11

POR:514S0457 (tall)

SSD V_SEL

93 44 =PP3V3_S5_SMC
R3713 100K 5% 1/16W MF-LF 402
IN 44
OUT 44
R3712 100K 5% 1/16W MF-LF 402
32 SSD_V_SEL
SSD:Y
R3715 100K 5% 1/16W MF-LF 402

TO SSD VR
H=2.7V,L=3.3V (SSD PULLS PIN LOW FOR 3.3V)

PD_L (S3X ONLY)

BP05 BP06 BP07 BP08 BP01 BP02 BP03 BP04
TP-BP-P19XP55SMP14X450

Current SSD Conn Pinout

PCIE Pinout on UBX:	PCIE Pinout for S3X
RXD0_N=22, TXD0_N=34	RXD0_P=22, TXD0_P=34
RXD0_P=21, TXD0_P=35	RXD0_N=21, TXD0_N=35
RXD1_N=19, TXD1_N=37	RXD1_P=37, TXD1_P=37
RXD1_P=18, TXD1_P=38	RXD1_N=18, TXD1_N=38
RXD2_N=15, TXD2_N=41	RXD2_P=15, TXD2_P=41
RXD2_P=14, TXD2_P=42	RXD2_N=14, TXD2_N=42
RXD3_N=12, TXD3_N=44	RXD3_P=12, TXD3_P=44
RXD3_P=11, TXD3_P=45	RXD3_N=11, TXD3_N=45

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013
PAGE TITLE: SDD/HDD:SATA/SSD Connectors
Apple Inc.
DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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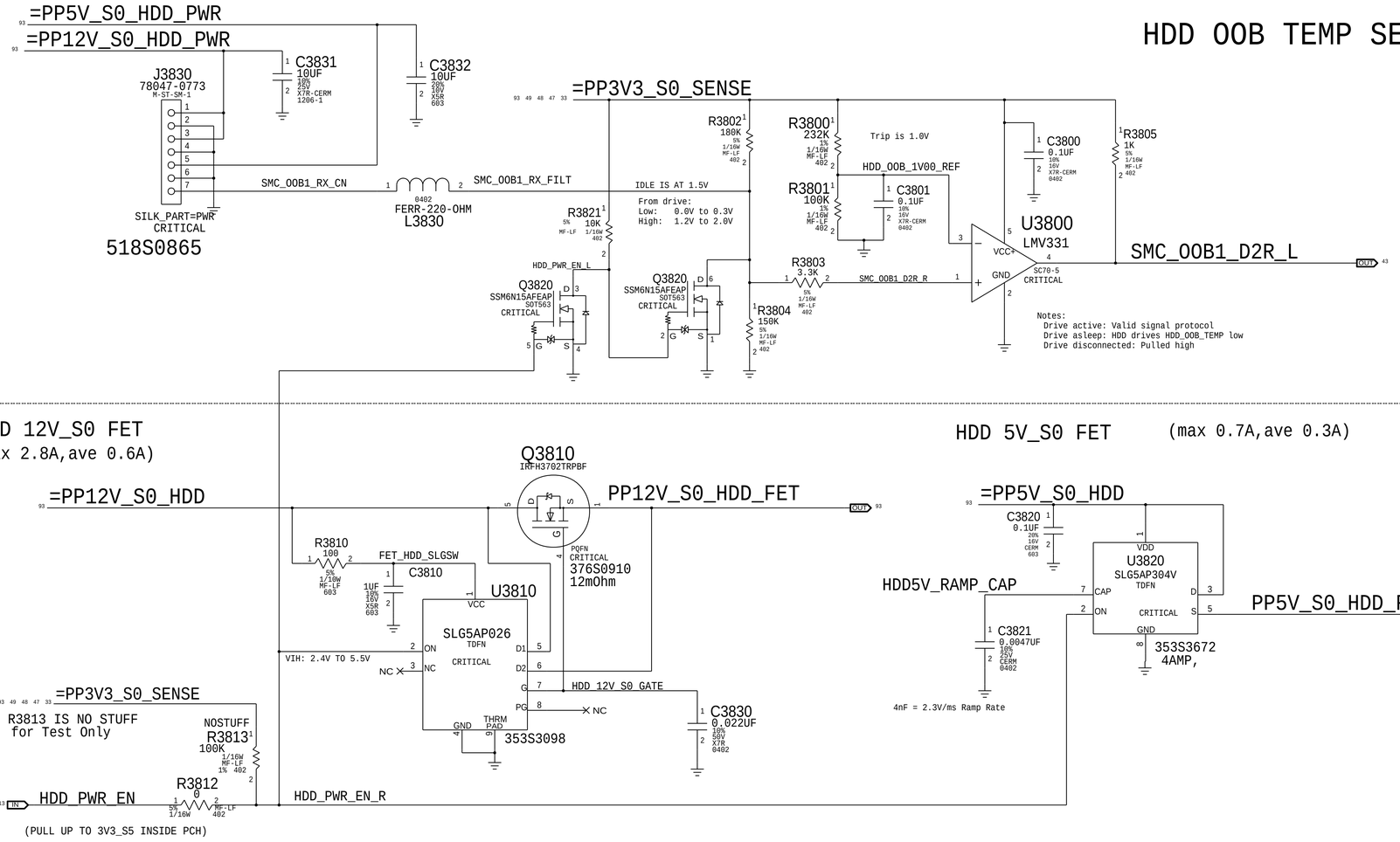
HDD POWER



HDD OOB TEMP SENSING

REMOVE R3813 AND SHORT R3812 AFTER HDD_PWR_EN WORKS

SYNC_MASTER=J78_KENNY SYNC_DATE=03/10/2014

PAGE TITLE
HDD: SSD Temp Sense

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.
=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)
VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO
ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.
=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)
CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM
ENET_XTALVDDH
C3900
0.1UF
L3905
PP3V3_ENET_PHY_BIASVDDH
C3905
L3910
PP3V3_ENET_PHY_AVDDH
R3910
4.7K
C3910
C3911
L3920
PP1V2_ENET_PHY_AVDDL
C3921
C3920
4.7UF
L3925
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926
C3925
L3930
PP1V2_ENET_PHY_GPHYPLL
C3931
C3930
C3936
C3935
10UF
R3940
R3941
C3915
C3916
=PP3V3_S0_ENET
R3942
1K
Current Limiting Resistor
C3950
PCIE_ENET_D2R_N
C3951
PCIE_ENET_D2R_P
C3955
PCIE_ENET_R2D_C_P
C3956
PCIE_ENET_R2D_C_N
=ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.
ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_TRAFFICLED_L
ENET_XTAL_IN
ENET_XTAL_OUT
ENET_RDAC
R3965
1.24K
OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8
VMAIN_PRSNT
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST*
CLKREQ*
WAKE*
LOW_PWR
SMB_CLK
SMB_DATA
SCLK_SPD1000LED*
SI/EEDATA
SO_LINKLED*
CS*/EECLK
SPD100LED*/SERIAL_DO
TRAFFICLED*/SERIAL_DI
XTALI
XTALO
RDAC
THRM_PAD
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
TRD0_P
TRD0_N
TRD1_P
TRD1_N
TRD2_P
TRD2_N
TRD3_P
TRD3_N
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
PP3V3R1V8_ENET_LR_OUT
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.
GPIO_0/CR_ACT_LED*
GPIO_1/LR_OUT
GPIO_2/MEDIA_SENSE
ENET_MEDIA_SENSE
SD_DETECT
ENET_SD_DETECT_L
CR_CMD
ENET_SD_CMD
R3961
SDCONN_CMD
CR_CLK
ENET_SD_CLK
R3979
SDCONN_CLK
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
ENET_CR_DATA<0>
ENET_CR_DATA<1>
ENET_CR_DATA<2>
ENET_CR_DATA<3>
R3971
R3972
R3973
R3974
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
MS_INS*
CR_LED*/CR_BUS_PWR
ENET_CR_PWREN
CR_WP*
SDCONN_WP
SR_DISABLE
ENET_SR_DISABLE
R3981
1K
(See note)
ENET 1.2V SR IS ENABLED IF FLOATING.
ENET supports both active-levels for WP.
ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.
ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)
=PP3V3_ENET_PHY
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
C3990
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF
R3990
R3997
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.
Ethernet 25MHz Crystal
C3945
20PF
ENET_XTAL_OUT_R
R3945
ENET_XTAL_OUT
NOSTUFF
R3946
1M
CRITICAL
Y3900
25.000MHZ-20PPM-12PF-85C
C3946
20PF
ENET_XTAL_IN
NOTE: 30 PPM crystal required
SYNC_MASTER=J16_IG
SYNC_DATE=04/29/2013
PAGE TITLE
ETHERNET: PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER
051-00321
SIZE
D
REVISION
4.0.0
BRANCH
proto1b
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34 OF 96
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CAESAR IV 1.2V INT.VR CMPTS

93 35 34 =PP3V3_ENET_PHY

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402

C4011 0.1UF 10% 16V X7R-CERM 0402

CRITICAL
L4010 4.7UH-0.8A PCAA031B-SM

34 ENET_SR_LX
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

C4012 10UF 20% 6.3V X5R 603

C4013 0.1UF 10% 16V X7R-CERM 0402

PP1V2_ENET_INTREG 35
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

Feedback loop

35 PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_ENET_PHY 34
=ENET_SR_VFB 34

ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

14 13 IN WOL_EN

72 71 44 43 12 6 IN PM_SLP_S3_L

CRITICAL
Q4021 2N7002DW-X-G SOT-363

CRITICAL
Q4021 2N7002DW-X-G SOT-363

3.3V ENET FET

93 =PP3V3_S4_FET_ENET

CRITICAL
Q4020 NTR4101P SOT-23-HF

PP3V3_ENET_FET 93

R4020 10K 5% 1/10W MF-LF 402

R4021 100K 5% 1/10W MF-LF 402

C4020 0.033UF 10% 16V X5R 402

C4021 0.01UF 10% 50V X7R-CERM 0402

PM_EN_ENET_L

P3V3ENET_SS

CAESAR IV ACTIVITY LED

93 35 34 =PP3V3_ENET_PHY

DEVELOPMENT
R4050 330 5% 1/10W MF-LF 402

ENET_ACT

DEFAULT_RESISTOR_0.001OHM_K_A
DEVELOPMENT
LED4050 GRN-OMCD-0.03A 0805

SILKSCREEN:ENET ACT

34 ENET_TRAFFICLED_L

CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY 34 35 93

CRITICAL
Q4070 SOD

R4070 10K 5% 1/16W MF-LF 402

31 19 12 PCIE_WAKE_L

ENET_WAKE_L
MAKE_BASE=TRUE

=ENET_WAKE_L 34

PP3V3R1V8_ENET_LR_OUT 34
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1500

=PP3V3R1V8_CR_VDDIO 34

C4030 4.7UF 20% 6.3V X5R-CERM1 402

C4031 0.1UF 10% 16V X5R-CERM 0201

C4032 0.1UF 10% 16V X5R-CERM 0201

157S0058
CRITICAL
T4000 SM

ENETCONN_MDI_N<1> 34 BI 1
ENETCONN_MDI_P<1> 34 BI 2
ENETCONN_MDI_T_N<1> 12 BI 35
ENETCONN_MDI_T_P<1> 11 BI 35
3 10 ENETCONN_MCT1
TX
LFE8904CF
4 9 ENETCONN_MCT3
ENETCONN_MDI_N<0> 34 BI 5
ENETCONN_MDI_P<0> 34 BI 6
ENETCONN_MDI_T_N<0> 8 BI 35
ENETCONN_MDI_T_P<0> 7 BI 35
RX

CRITICAL
T4010 SM

ENETCONN_MDI_N<2> 34 BI 1
ENETCONN_MDI_P<2> 34 BI 2
ENETCONN_MDI_T_N<2> 12 BI 35
ENETCONN_MDI_T_P<2> 11 BI 35
3 10 ENETCONN_MCT2
TX
LFE8904CF
4 9 ENETCONN_MCT0
ENETCONN_MDI_P<3> 34 BI 5
ENETCONN_MDI_N<3> 34 BI 6
ENETCONN_MDI_T_P<3> 8 BI 35
ENETCONN_MDI_T_N<3> 7 BI 35
RX

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402

C4002 0.1UF 20% 10V CERM 402

C4003 0.1UF 20% 10V CERM 402

C4004 0.1UF 20% 10V CERM 402

R4000 75 5% 1/16W MF-LF 402

R4001 75 5% 1/16W MF-LF 402

R4002 75 5% 1/16W MF-LF 402

R4003 75 5% 1/16W MF-LF 402

ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000

NOSTUFF
C4000 1000PF 10% 3KV CERM 1206

514-0822
CRITICAL
J4000 RCPT-RJ45-D8 F-ANG-TH

ENETCONN_MDI_T_N<3> 35 BI 8 ENET_MDI_TRAN3-
ENETCONN_MDI_T_P<3> 35 BI 7 ENET_MDI_TRAN3+
ENETCONN_MDI_T_N<1> 35 BI 6 ENET_MDI_TRAN1-
ENETCONN_MDI_T_N<2> 35 BI 5 ENET_MDI_TRAN2-
ENETCONN_MDI_T_P<2> 35 BI 4 ENET_MDI_TRAN2+
ENETCONN_MDI_T_P<1> 35 BI 3 ENET_MDI_TRAN1+
ENETCONN_MDI_T_N<0> 35 BI 2 ENET_MDI_TRAN0-
ENETCONN_MDI_T_P<0> 35 BI 1 ENET_MDI_TRAN0+
ENET_MDI
9 10 11 12 13 14 SHIELD PINS

SYNC_MASTER=J16_IG SYNC_DATE=12/07/2012

PAGE TITLE
ETHERNET: Support & Connector

Apple Inc.

DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
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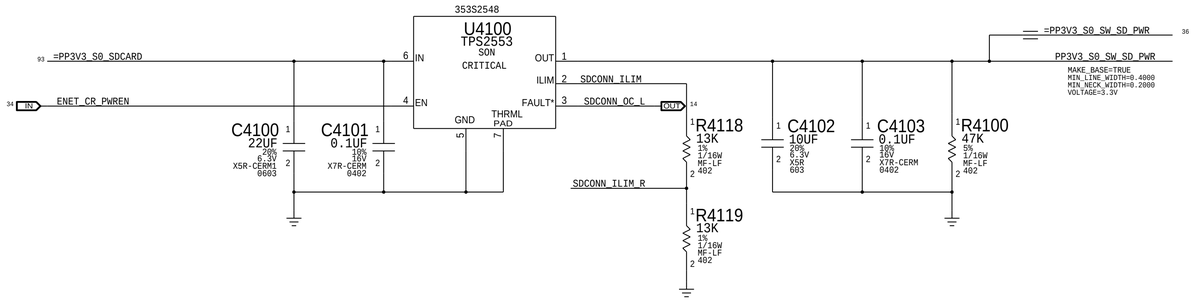
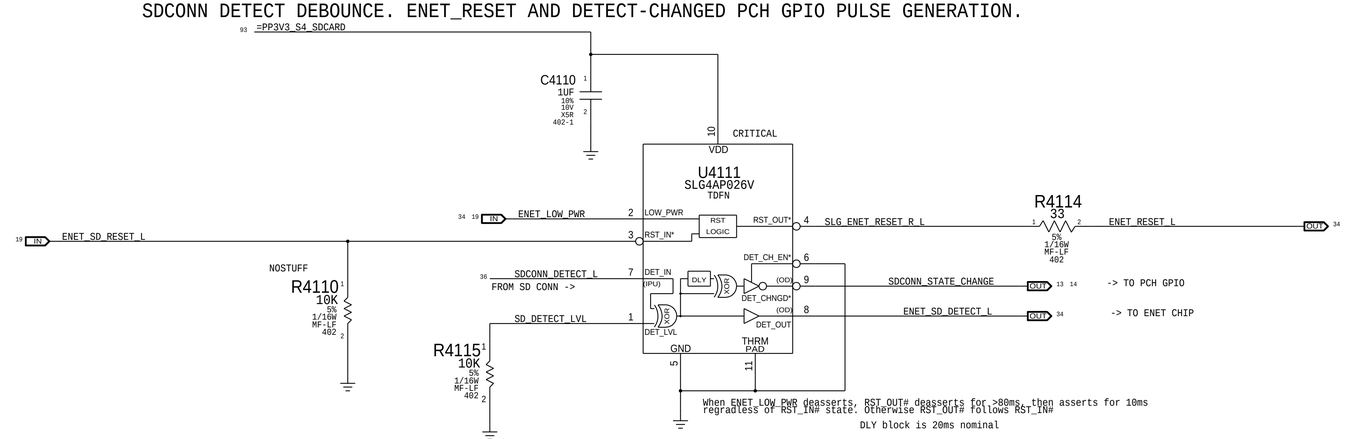
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

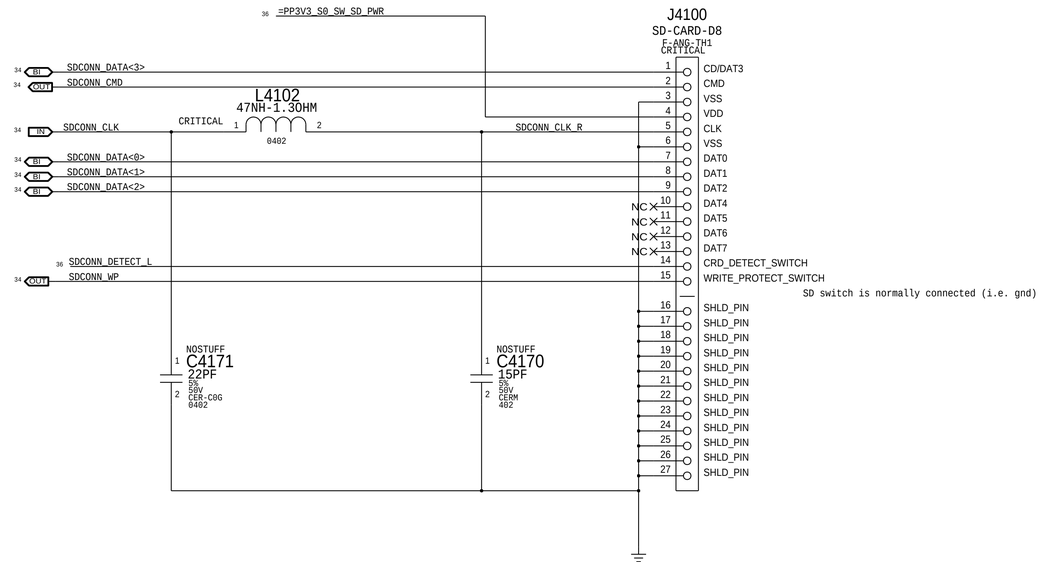


SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE

SD CARD: Connector

Apple Inc.

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REVISION 4.0.0

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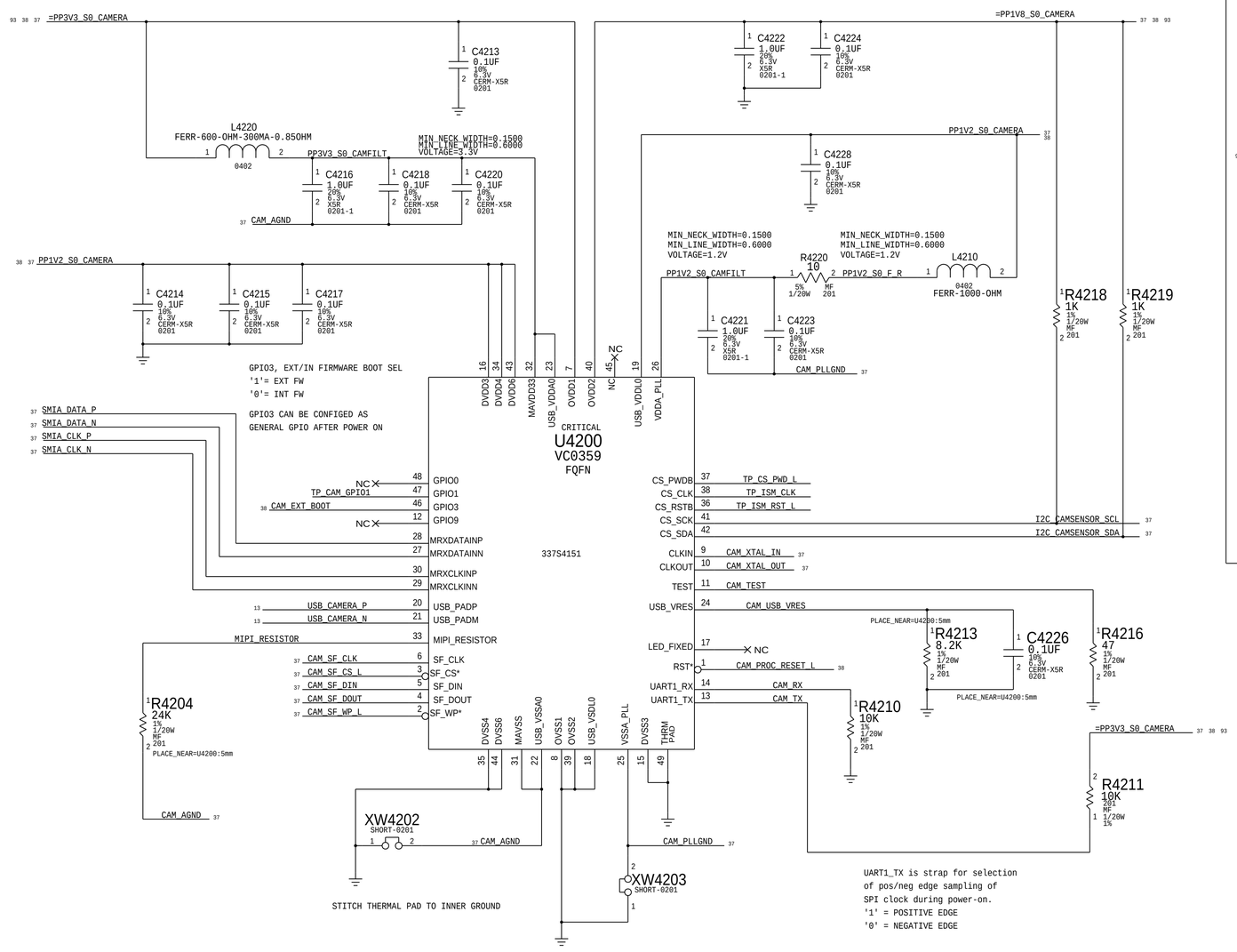
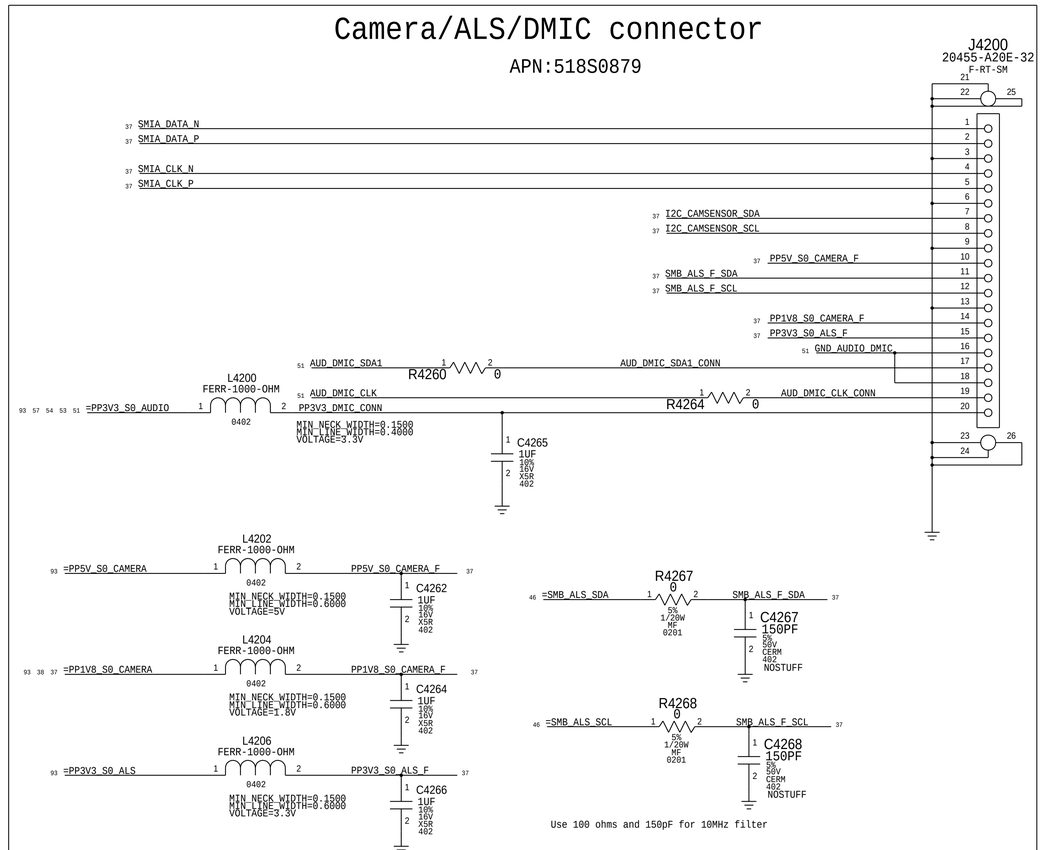
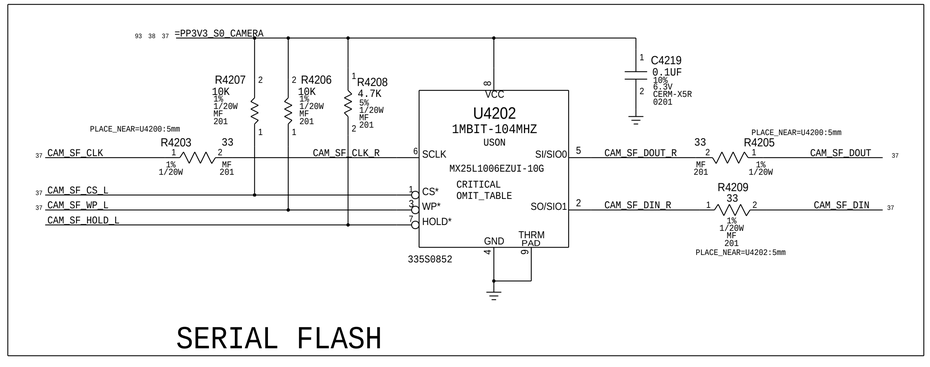
USB CAMERA CONTROLLER



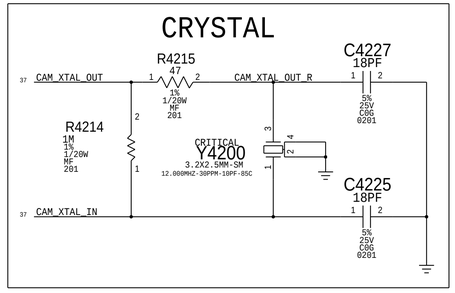
Camera/ALS/DMIC connector

APN:518S0879





SERIAL FLASH



SYNC_MASTER=J78_NAT	SYNC_DATE=11/05/2013
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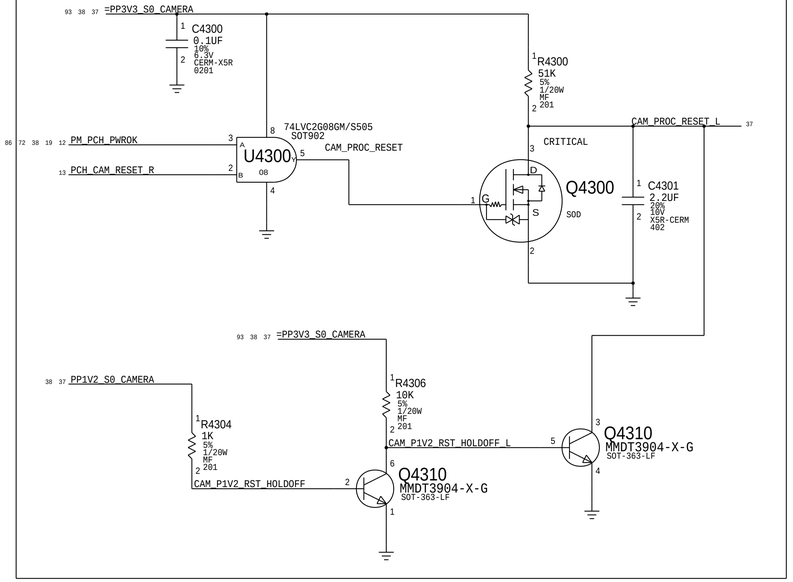
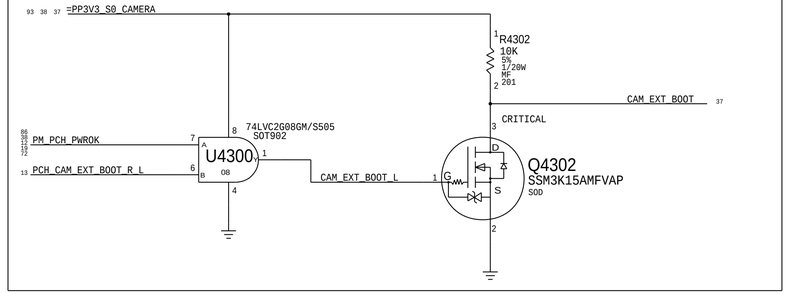
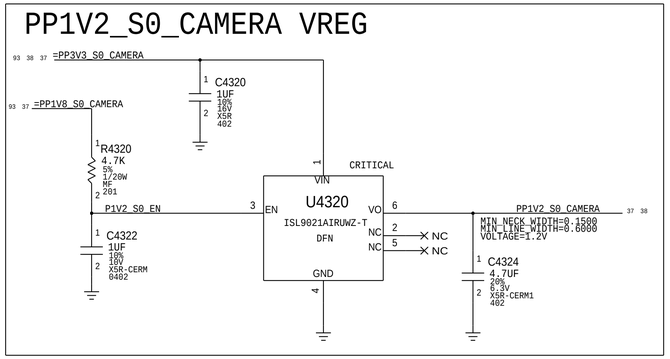
Camera Processor Reset



Camera Processor ExtBoot Cntl



PP1V2_S0_CAMERA VREG



SYNC_MASTER=J78_NAT SYNC_DATE=11/05/2013

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INTERNAL DP(STRAIGHT)

518S0886
CRITICAL
J4400
20525-160E-01
F-RT-SM

=PP12V_S0_LCD → F4400 2AMP-32V (0603) → PP12V_LCD_F (VOLTAGE=12V, MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.2000) → L4400 FERR-120-OHM-3A (0603, 155S0367) → PP12V_LCD (VOLTAGE=12V, MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.2000)

PP12V_LCD:
- C4420 10UF 10% 16V XSR-CERM 0805
- C4401 0.001UF 20% 50V CERM 0402
- C4421 0.1UF 10% 16V X7R-CERM 0402

NOSTUFF R4419 0 1/16W 402 5% → DP_INT_PIN_1

NOSTUFF R4418 0 1/16W 402 5% → DP_INT_PIN_9

DISPLAY TCON MASTER I2C (NOT USED FOR J95)

DISPLAY TCON SLAVE I2C (CONNECTS TO SMC)

- SMB_DP_TCON_SLA_SDA (BI)
- SMB_DP_TCON_SLA_SCL (BI)
- DP_INTPNL_ML_HPD (OUT)

DP_INT_EG_SL_HPD (OUT) → R4400 100K 5% 1/20W MF 201

DP_INT_EG_SL_P<0>	C4450 0.1UF	DP_INT_EG_SL_C_P<0>
DP_INT_EG_SL_N<0>	C4451 0.1UF	DP_INT_EG_SL_C_N<0>
DP_INT_EG_SL_P<1>	C4452 0.1UF	DP_INT_EG_SL_C_P<1>
DP_INT_EG_SL_N<1>	C4453 0.1UF	DP_INT_EG_SL_C_N<1>
DP_INT_EG_SL_P<2>	C4454 0.1UF	DP_INT_EG_SL_C_P<2>
DP_INT_EG_SL_N<2>	C4455 0.1UF	DP_INT_EG_SL_C_N<2>
DP_INT_EG_SL_P<3>	C4456 0.1UF	DP_INT_EG_SL_C_P<3>
DP_INT_EG_SL_N<3>	C4457 0.1UF	DP_INT_EG_SL_C_N<3>

All: 10% 6.3V CERM-XSR 0201

DP_INT_EG_SL_AUX_P (BI) → C4458 0.1UF
DP_INT_EG_SL_AUX_N (BI) → C4459 0.1UF
(10% 6.3V CERM-XSR 0201)

DISPLAYPORT SOURCE_DETECT PULL-DOWN → R4406 100K 5% 1/20W MF 201

R4407 100K 5% 1/20W MF 201 → =PP3V3_S0_INTDPMUX

DISPLAYPORT POWERED SOURCE_DETECT PULL-UP

NOSTUFF R4417 0 1/16W 402 5%
TCON_RESET_L (IN) → R4417 → DP_INT_PIN_54

- DP_INT_PIN_55 (OUT)
- DP_INT_SPDIF_AUDIO (OUT)
- DP_INT_PIN_57 (OUT)
- BLC_VSYNC (OUT)
- BLC_LSYNC (OUT)
- BLC_EN

TCON_BLC_EN (OUT) → R4415 0 1/16W 402 5%

=PP3V3_S0_DP → C4400 0.1UF 10% 6.3V CERM-XSR 0201

CRITICAL TC7SZ08FEAPE SOT665 → U4400
TCON_BLC_EN_LED (OUT)

NC
NC

DP_INT_EG_SL_AUX_C_P
DP_INT_EG_SL_AUX_C_N

- DP_INTPNL_ML_AUX_C_P (BI)
- DP_INTPNL_ML_AUX_C_N (BI)
- DP_INTPNL_ML_C_P<0> (IN)
- DP_INTPNL_ML_C_N<0> (IN)
- DP_INTPNL_ML_C_P<1> (IN)
- DP_INTPNL_ML_C_N<1> (IN)
- DP_INTPNL_ML_C_P<2> (IN)
- DP_INTPNL_ML_C_N<2> (IN)
- DP_INTPNL_ML_C_P<3> (IN)
- DP_INTPNL_ML_C_N<3> (IN)
- DP_INT_EG_SL_C_P<0>
- DP_INT_EG_SL_C_N<0>
- DP_INT_EG_SL_C_P<1>
- DP_INT_EG_SL_C_N<1>
- DP_INT_EG_SL_C_P<2>
- DP_INT_EG_SL_C_N<2>
- DP_INT_EG_SL_C_P<3>
- DP_INT_EG_SL_C_N<3>

SYNC_MASTER=J95_ANDREW SYNC_DATE=1/27/2015

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TP to DP aliases

26 IN TP_DP_TBTSRC_ML_CP<0> = DP_TBTSRC_ML_P<0> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CN<0> = DP_TBTSRC_ML_N<0> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CP<1> = DP_TBTSRC_ML_P<1> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CN<1> = DP_TBTSRC_ML_N<1> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CP<2> = DP_TBTSRC_ML_P<2> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CN<2> = DP_TBTSRC_ML_N<2> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CP<3> = DP_TBTSRC_ML_P<3> 40 (MAKE_BASE=TRUE)
26 IN TP_DP_TBTSRC_ML_CN<3> = DP_TBTSRC_ML_N<3> 40 (MAKE_BASE=TRUE)
26 BI TP_DP_TBTSRC_AUXCH_CP = DP_TBTSRC_AUXCH_P 40 (MAKE_BASE=TRUE)
26 BI TP_DP_TBTSRC_AUXCH_CN = DP_TBTSRC_AUXCH_N 40 (MAKE_BASE=TRUE)

93 40 =PP1V8_S0_DP

R4510 470K 5% 1/20W MF 201
R4511 470K 5% 1/20W MF 201

82 BI DP_INT_EG_ML_AUX_P — C4508 0.1UF — DP_INT_EG_ML_AUX_C_P
82 BI DP_INT_EG_ML_AUX_N — C4509 0.1UF — DP_INT_EG_ML_AUX_C_N

93 40 =PP1V8_S0_DP

R4512 470K 5% 1/20W MF 201
R4513 470K 5% 1/20W MF 201

40 DP_TBTSRC_AUXCH_P — C4510 0.1UF — DP_TBTSRC_AUX_C_P
40 DP_TBTSRC_AUXCH_N — C4511 0.1UF — DP_TBTSRC_AUX_C_N

83 OUT DP_INT_EG_ML_HPD
R4500 200K 1% 1/20W MF 201

93 40 39 =PP3V3_S0_INTDPMUX

R4504 10K 5% 1/20W MF 201

26 OUT DP_TBTSRC_HPD (PD is on the LR page)
57 14 IN DP_TBT_SEL
DP_GPU_MUX_EN

NOSTUFF
R4501 10K 5% 1/20W MF 201
U4500.A1:8MM

=PP3V3_S0_INTDPMUX 39 40 93

C4568 0.1UF 10% 6.3V CERM-X5R 0201
C4569 0.1UF 10% 6.3V CERM-X5R 0201

U4500
CBTL06142EEE
TFBGA
CRITICAL

82 IN	DP_INT_EG_ML_P<0>	B4	DIN1_0+
82 IN	DP_INT_EG_ML_N<0>	A4	DIN1_0-
82 IN	DP_INT_EG_ML_P<1>	B5	DIN1_1+
82 IN	DP_INT_EG_ML_N<1>	A5	DIN1_1-
82 IN	DP_INT_EG_ML_P<2>	B6	DIN1_2+
82 IN	DP_INT_EG_ML_N<2>	A6	DIN1_2-
82 IN	DP_INT_EG_ML_P<3>	A8	DIN1_3+
82 IN	DP_INT_EG_ML_N<3>	A9	DIN1_3-
		H9	DAUX1+
		J9	DAUX1-
	NC	H8	DDC_CLK1
	NC	J8	DDC_DAT1
		J2	HPD_1
40 IN	DP_TBTSRC_ML_C_P<0>	B8	DIN2_0+
40 IN	DP_TBTSRC_ML_C_N<0>	B9	DIN2_0-
40 IN	DP_TBTSRC_ML_C_P<1>	D8	DIN2_1+
40 IN	DP_TBTSRC_ML_C_N<1>	D9	DIN2_1-
40 IN	DP_TBTSRC_ML_C_P<2>	E8	DIN2_2+
40 IN	DP_TBTSRC_ML_C_N<2>	E9	DIN2_2-
40 IN	DP_TBTSRC_ML_C_P<3>	F8	DIN2_3+
40 IN	DP_TBTSRC_ML_C_N<3>	F9	DIN2_3-
		H6	DAUX2+
		J6	DAUX2-
	NC	H5	DDC_CLK2
	NC	J5	DDC_DAT2
		H3	HPD_2
		A1	GPU_SEL
		B7	XSD*

VDD A2, VDD J4
GND B3, GND C8, GND G8, GND H4, GND H7, GND G2
DDC_AUX_SEL C2

DOUT_0+	B2	DP_INTPNL_ML_P<0>	C4500 0.1UF — DP_INTPNL_ML_C_P<0> OUT 39
DOUT_0-	B1	DP_INTPNL_ML_N<0>	C4501 0.1UF — DP_INTPNL_ML_C_N<0> OUT 39
DOUT_1+	D2	DP_INTPNL_ML_P<1>	C4502 0.1UF — DP_INTPNL_ML_C_P<1> OUT 39
DOUT_1-	D1	DP_INTPNL_ML_N<1>	C4503 0.1UF — DP_INTPNL_ML_C_N<1> OUT 39
DOUT_2+	E2	DP_INTPNL_ML_P<2>	C4504 0.1UF — DP_INTPNL_ML_C_P<2> OUT 39
DOUT_2-	E1	DP_INTPNL_ML_N<2>	C4505 0.1UF — DP_INTPNL_ML_C_N<2> OUT 39
DOUT_3+	F2	DP_INTPNL_ML_P<3>	C4506 0.1UF — DP_INTPNL_ML_C_P<3> OUT 39
DOUT_3-	F1	DP_INTPNL_ML_N<3>	C4507 0.1UF — DP_INTPNL_ML_C_N<3> OUT 39

AUX+ H2 DP_INTPNL_ML_AUX_P — R4558 0 — DP_INTPNL_ML_AUX_C_P BI 39
AUX- H1 DP_INTPNL_ML_AUX_N — R4559 0 — DP_INTPNL_ML_AUX_C_N BI 39
HPDIN J1 DP_INTPNL_ML_HPD IN 39 68

R4502 100K 5% 1/20W MF 201
R4503 100K 5% 1/20W MF 201
=PP3V3_S0_INTDPMUX 39 40 93

40 IN DP_TBTSRC_ML_P<0> = DP_TBTSRC_ML_C_P<0> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_N<0> = DP_TBTSRC_ML_C_N<0> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_P<1> = DP_TBTSRC_ML_C_P<1> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_N<1> = DP_TBTSRC_ML_C_N<1> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_P<2> = DP_TBTSRC_ML_C_P<2> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_N<2> = DP_TBTSRC_ML_C_N<2> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_P<3> = DP_TBTSRC_ML_C_P<3> 40 (MAKE_BASE=TRUE)
40 IN DP_TBTSRC_ML_N<3> = DP_TBTSRC_ML_C_N<3> 40 (MAKE_BASE=TRUE)

SYNC_MASTER=J78_KENNY SYNC_DATE=10/09/2013
PAGE TITLE: DISPLAY: MUXing

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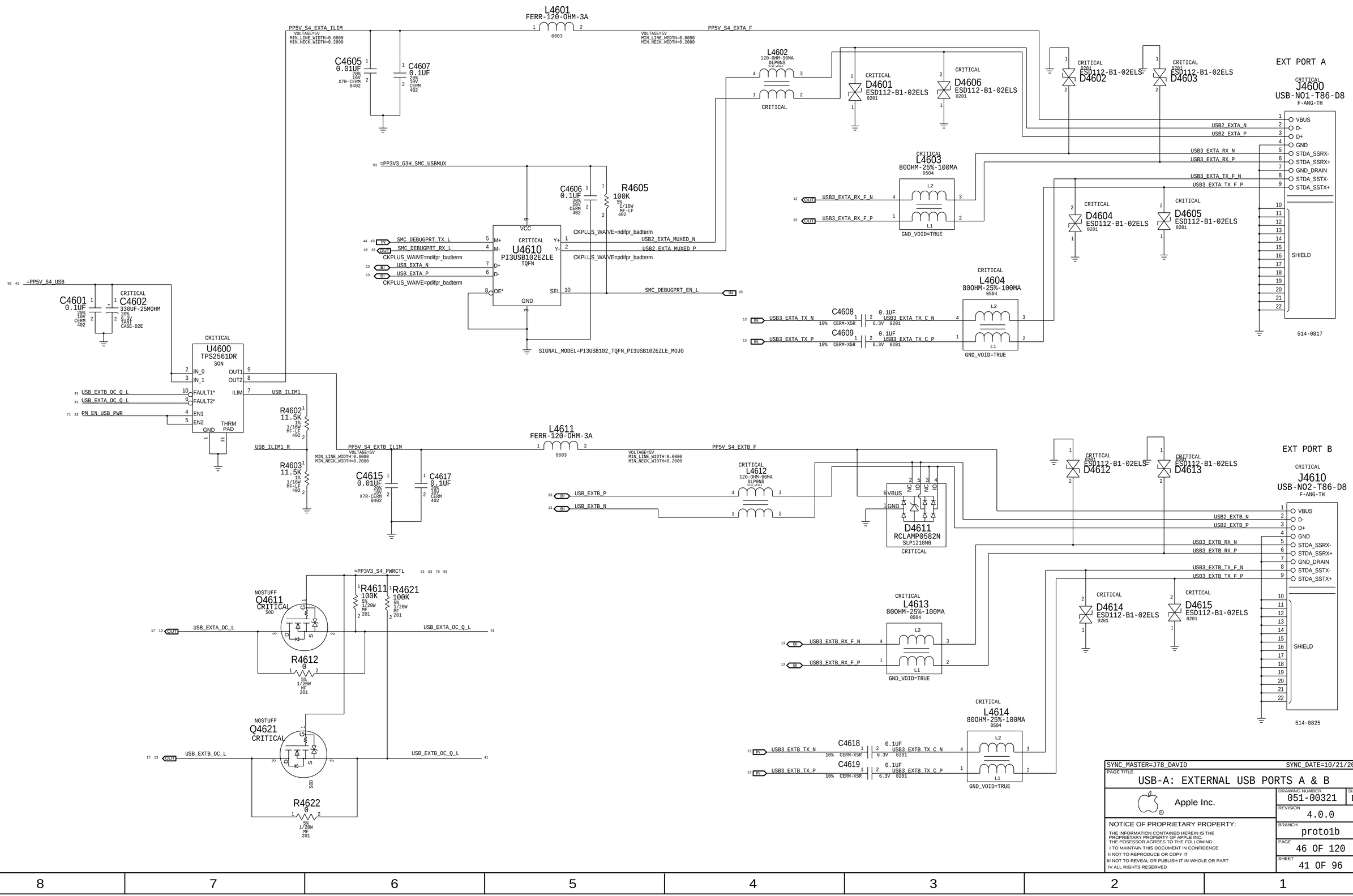

SYNC_MASTER=J78_DAVID SYNC_DATE=10/21/2013

PAGE TITLE

USB-A: EXTERNAL USB PORTS A & B

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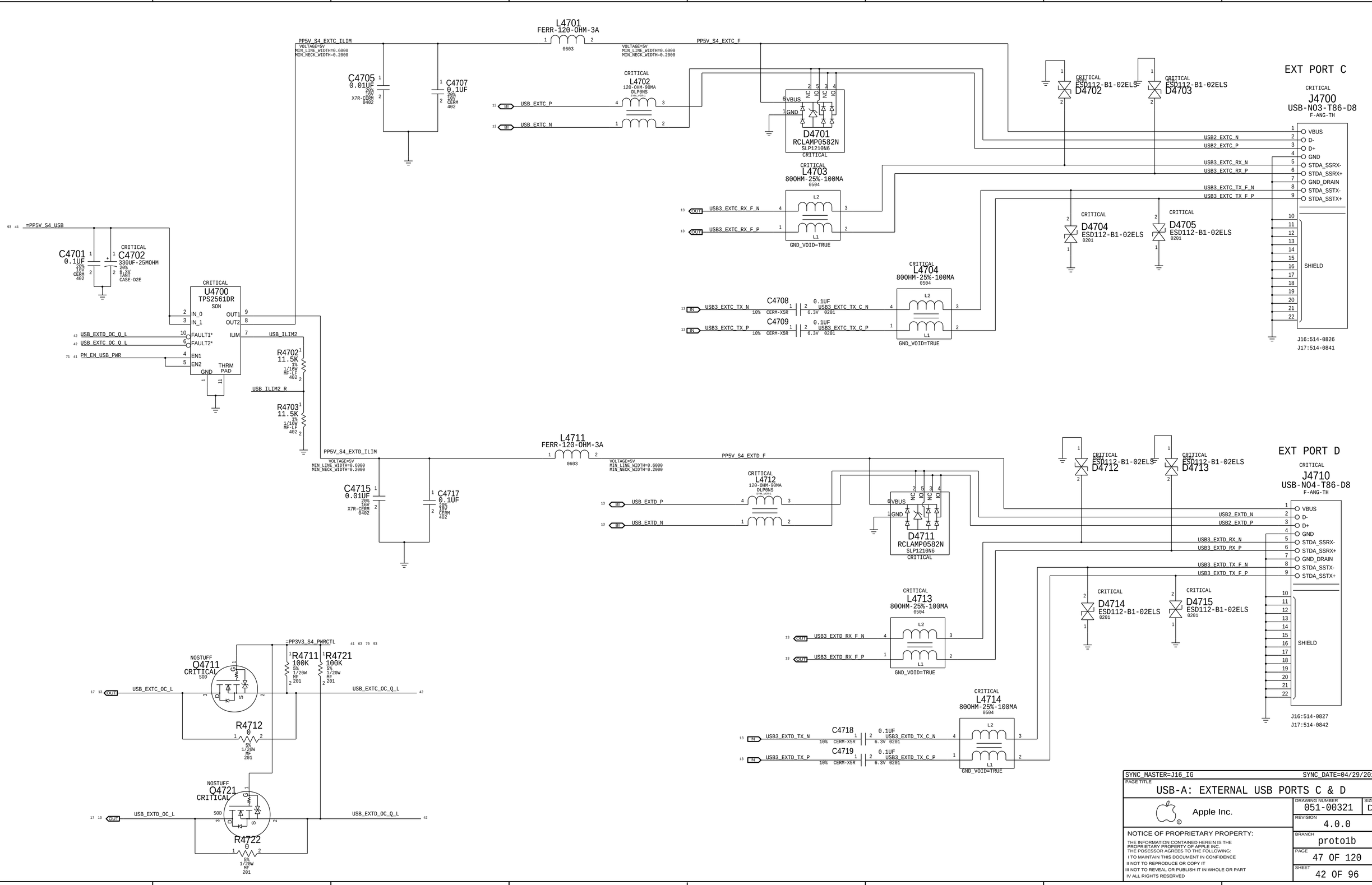

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE

USB-A: EXTERNAL USB PORTS C & D

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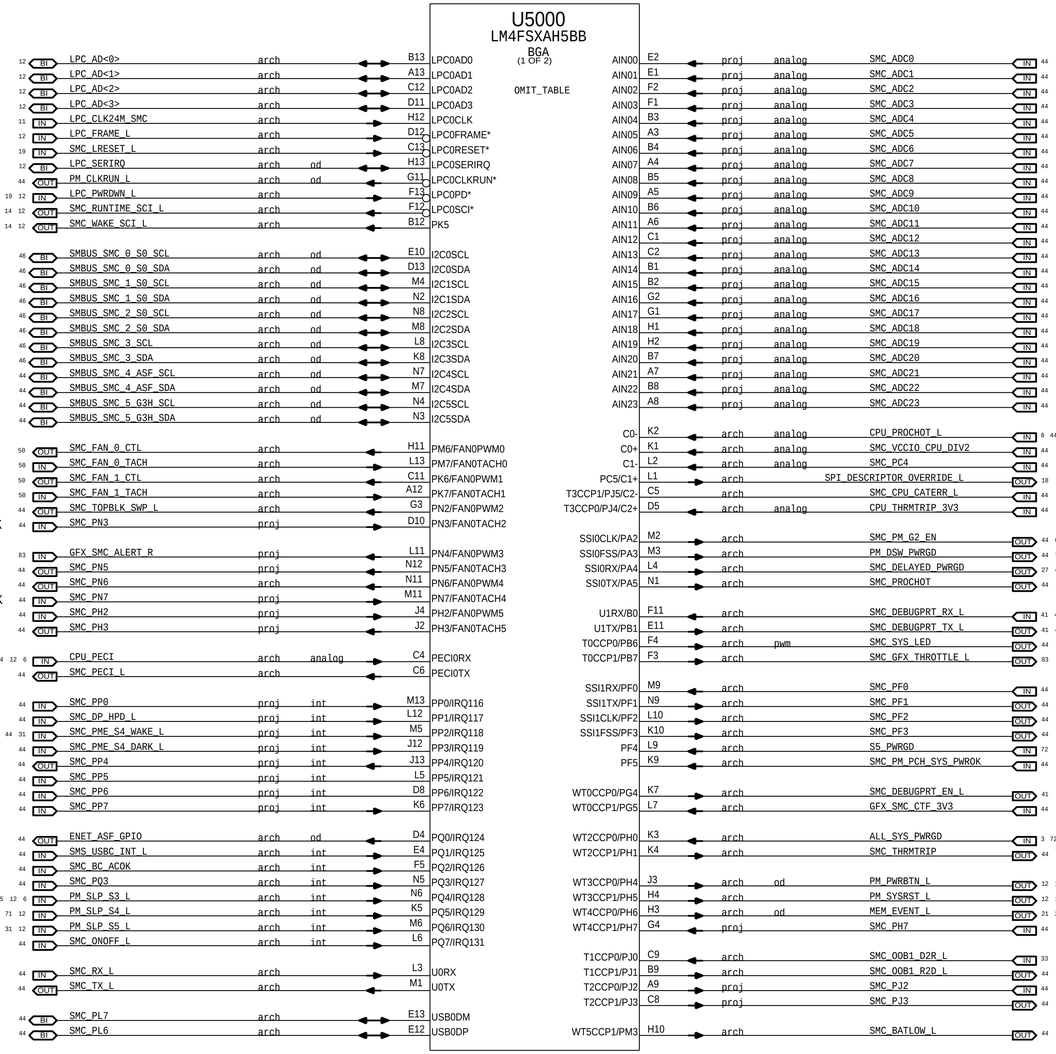
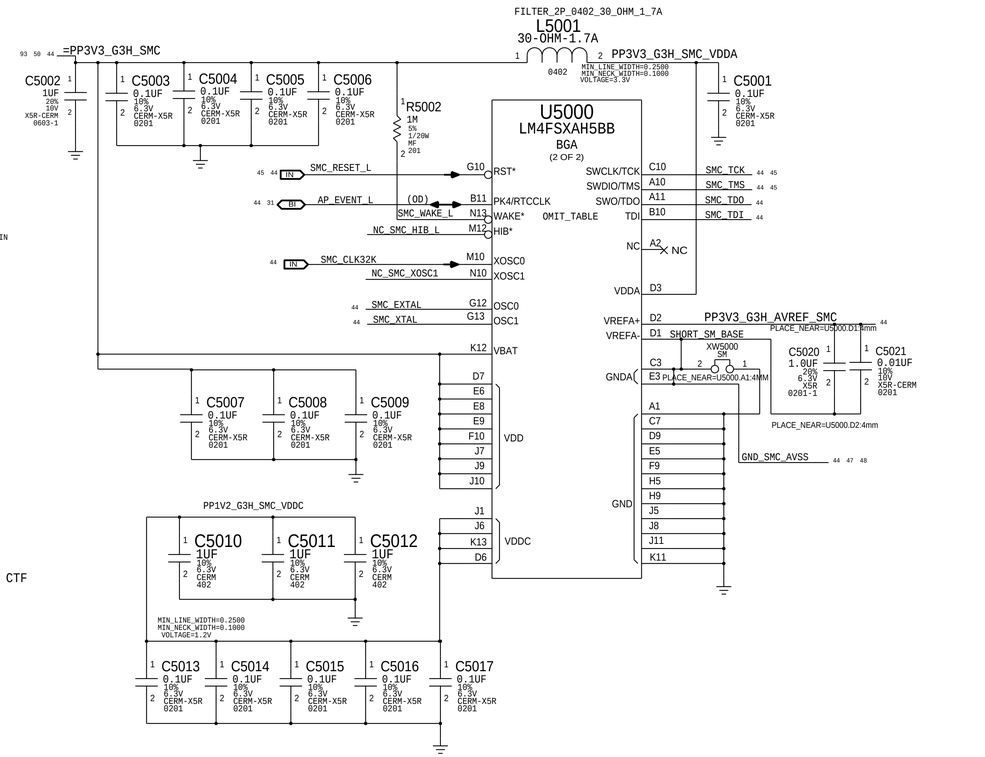
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





SYNC_MASTER=BRANCH_JERRYCHOW	SYNC_DATE=11/06/2014
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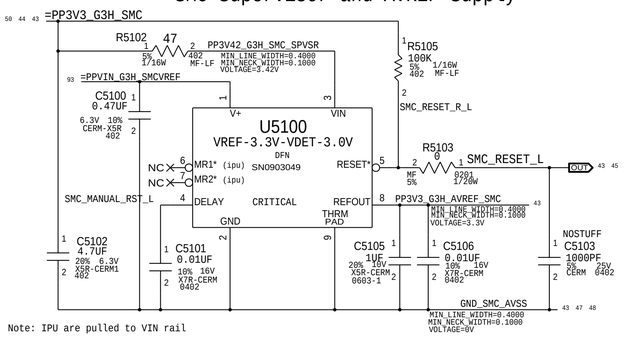
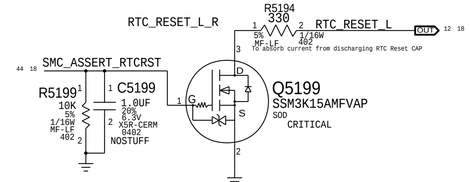
SMC Supervisor and AVREF Supply



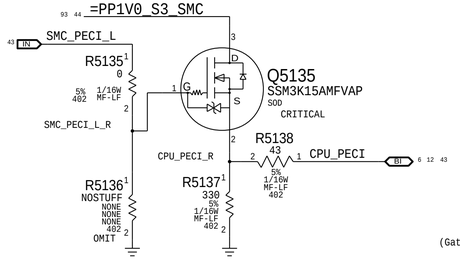
Note: IPU are pulled to VIN rail

SMC Controlled RTC Reset

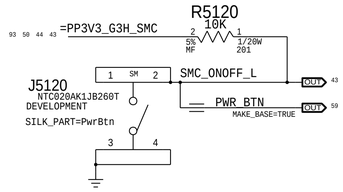


PECI Support

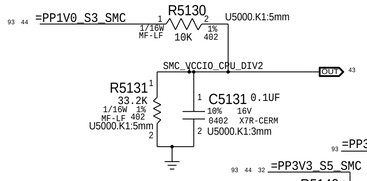
Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



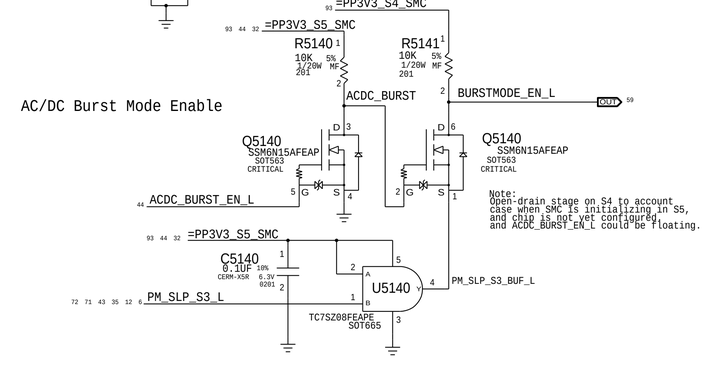
Power Button



Comparator VRef



AC/DC Burst Mode Enable



ADC Channel Aliases

43 SMC_ADC0	VSNS_P12VG3H 47	MAKE_BASE=TRUE	VD2R
43 SMC_ADC1	ISNS_P12VG3H 47	MAKE_BASE=TRUE	ID2R
43 SMC_ADC2	VSNS_P12VS0_CPUCORE 47	MAKE_BASE=TRUE	VD20
43 SMC_ADC3	ISNS_P12VS0_CPUCORE 47	MAKE_BASE=TRUE	ID20
43 SMC_ADC4	VSNS_CPUVCC 47	MAKE_BASE=TRUE	VC0C
43 SMC_ADC5	ISNS_CPUVCC 47	MAKE_BASE=TRUE	IC0C
43 SMC_ADC6	VSNS_CPUVCC_GT 47	MAKE_BASE=TRUE	VC0G
43 SMC_ADC7	ISNS_CPUVCC_GT 47	MAKE_BASE=TRUE	IC0G
43 SMC_ADC8	ISNS_CPUVCC_IO 47	MAKE_BASE=TRUE	IC0I
43 SMC_ADC9	ISNS_P1V35S0 48	MAKE_BASE=TRUE	IC0M
43 SMC_ADC10	ISNS_CPUVCC_SA 47	MAKE_BASE=TRUE	IC0S
43 SMC_ADC11	ISNS_P12VS0_FBVDDQ 47	MAKE_BASE=TRUE	IG1F
43 SMC_ADC12	VSNS_GPUCORE_ALT 47	MAKE_BASE=TRUE	VG0C
43 SMC_ADC13	ISNS_GPUCORE_ALT 47	MAKE_BASE=TRUE	IG0C
43 SMC_ADC14	VSNS_GPU_VDDCI 48	MAKE_BASE=TRUE	VG0I
43 SMC_ADC15	ISNS_GPU_VDDCI 48	MAKE_BASE=TRUE	IG0I
43 SMC_ADC16	ISNS_P12VS0_GPU_AUX 47	MAKE_BASE=TRUE	IG1A
43 SMC_ADC17	ISNS_P12VS0_GPUCORE 47	MAKE_BASE=TRUE	IG1C
43 SMC_ADC18	ISNS_P12VS0_HDD 48	MAKE_BASE=TRUE	IH02
43 SMC_ADC19	ISNS_HDDS0 48	MAKE_BASE=TRUE	IH05
43 SMC_ADC20	VSNS_SSD_S4 48	MAKE_BASE=TRUE	VH1R
43 SMC_ADC21	ISNS_SSD_S4 48	MAKE_BASE=TRUE	IH1R
43 SMC_ADC22	VSNS_VDDQS3_DDR 48	MAKE_BASE=TRUE	VM0R
43 SMC_ADC23	ISNS_VDDQS3_DDR 48	MAKE_BASE=TRUE	IM0R

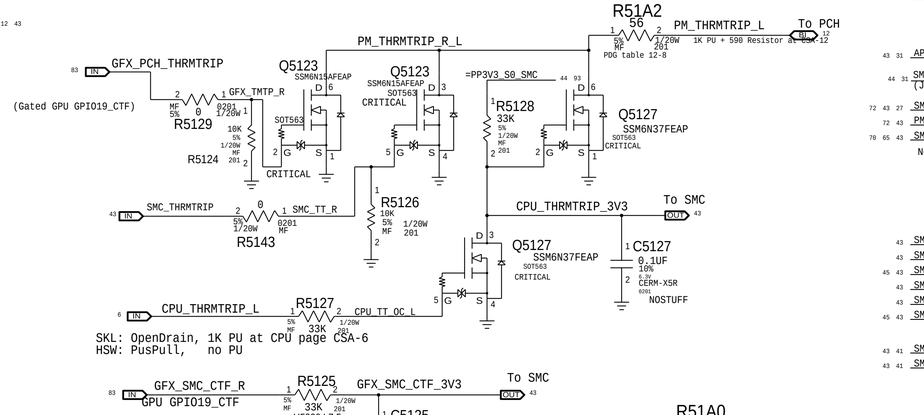
Project-specific Aliases

43 SMC_PN5	ACDC_BURST_EN_L 44	MAKE_BASE=TRUE	
43 SMC_PJ3	SMC_OOB2_R2D_L 32	MAKE_BASE=TRUE	
43 SMC_PJ2	SMC_OOB2_D2R_L 32	MAKE_BASE=TRUE	
43 SMC_PP0	SMC_ACDC_ID 59	MAKE_BASE=TRUE	
43 SMC_PH2	SMC_ASSERT_RTCRST 18 44	MAKE_BASE=TRUE	
43 SMC_PL6	SMC_WIFI_PWR_EN 44	MAKE_BASE=TRUE	
43 SMC_PN3	TCON_BLC_EN (LED-4) 39 60	MAKE_BASE=TRUE	(100K PD AT BLC)
43 SMC_PH7	GFX_OK_L (LED-3) 3 83	MAKE_BASE=TRUE	(5K PU AT MLB)
43 SMC_PN7	DP_LINK_OK (LED-3) 3 83	MAKE_BASE=TRUE	

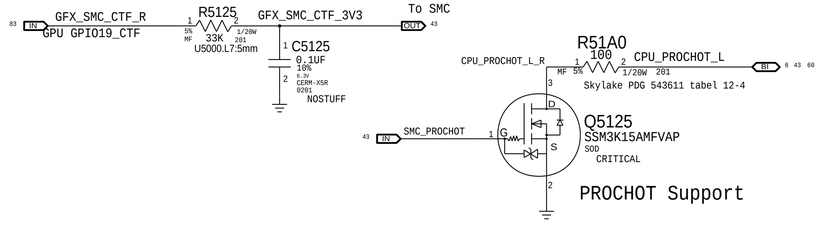
Unused Project-specific

43 SMC_PF0	NC_SMC_PF0	MAKE_BASE=TRUE	
43 SMC_PF1	NC_SMC_PF1	MAKE_BASE=TRUE	
43 SMC_PF2	NC_SMC_PF2	MAKE_BASE=TRUE	
43 SMC_PF3	NC_SMC_PF3	MAKE_BASE=TRUE	
43 SMC_PL7	SMC_BT_PWR_EN 31 44	MAKE_BASE=TRUE	(J95 new)
43 SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	
43 SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PC4	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PQ3	NC_G3_POWERON_L	MAKE_BASE=TRUE	
43 SMC_PN6	NC_SMC_G3_WAKESRC_EN	MAKE_BASE=TRUE	
43 SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	
43 SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=1	
43 SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=1	
43 SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_BATLOW_L	NC_SMC_SMC_BATLOW_L	MAKE_BASE=TRUE NO_TEST=1	
43 SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE NO_TEST=1	

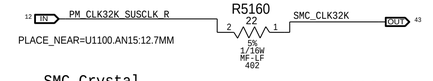
Platform Thermal Control



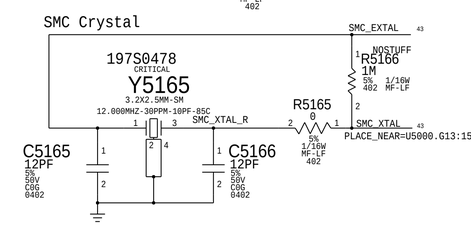
SKL: OpenDrain, 1K PU at CPU page CSA-6
HSW: PusPull, no PU

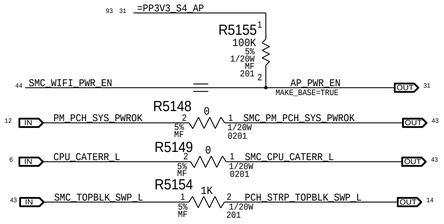


SMC 32KHz Clock

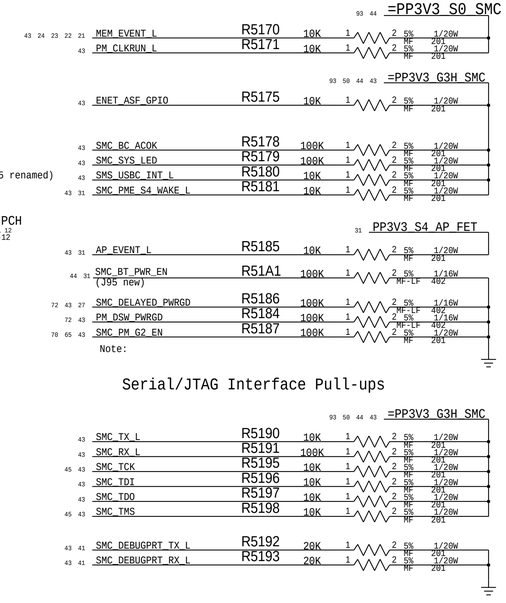


SMC Crystal





Arch Pull Up/Down



Serial/JTAG Interface Pull-ups

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=11/06/2014

PAGE TITLE

SMC: Controller Support

Apple Inc.

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BRANCH proto1b

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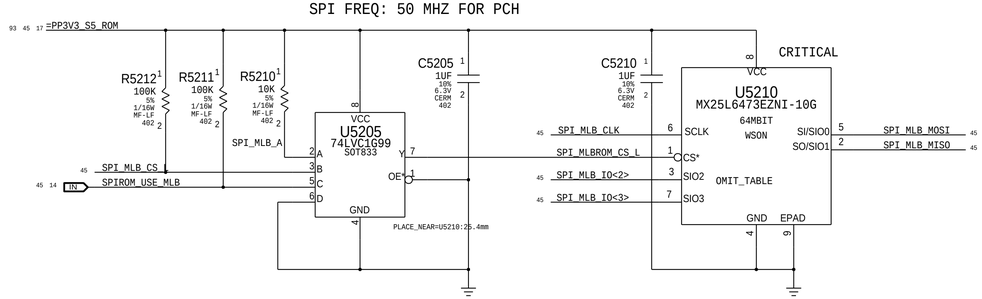
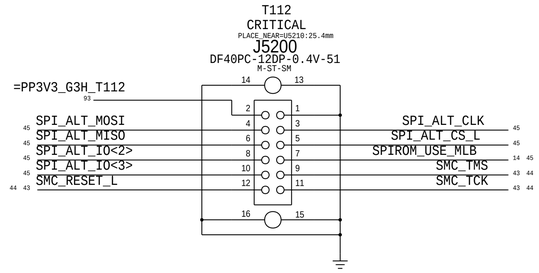
SPI BootROM

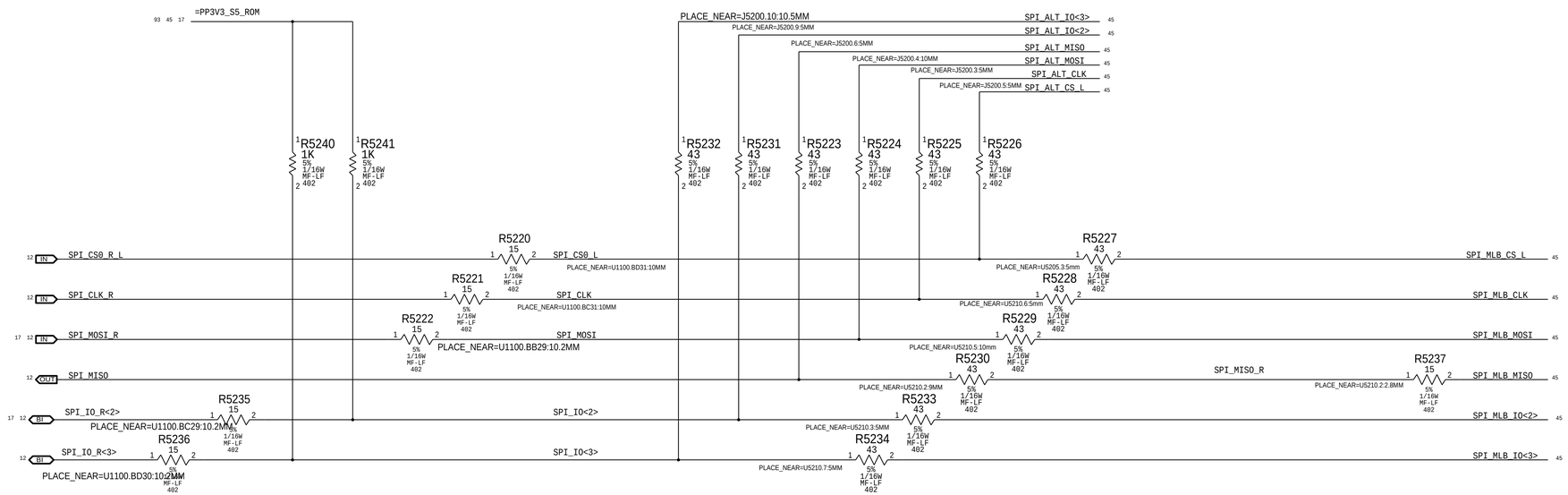
QUAD_IO MODE (MODE 0 & 3) SUPPORTED
SPI FREQ: 50 MHZ FOR PCH



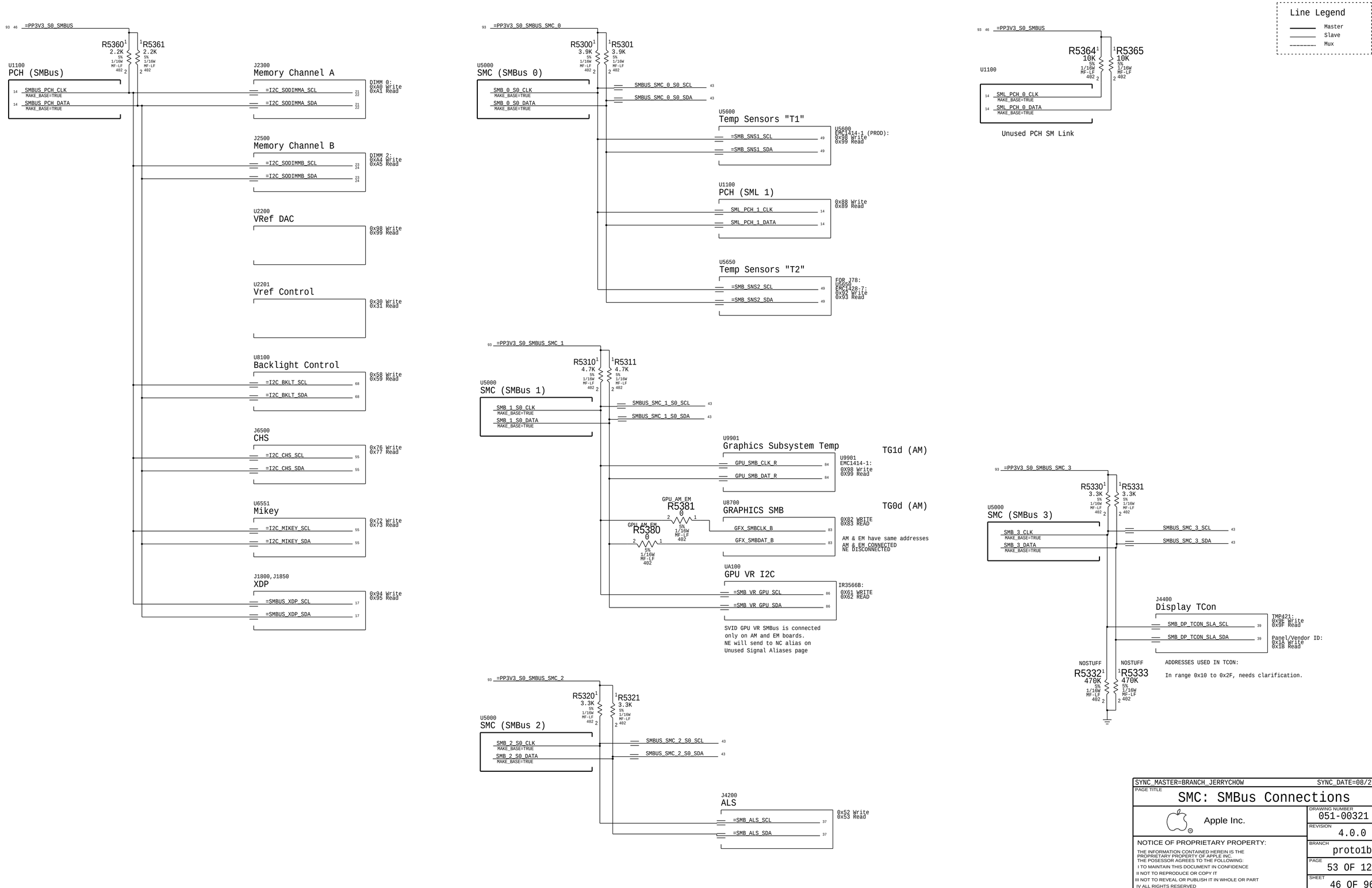
T112 Connector



SPI Series Termination



SYNC_MASTER=J17_TONY	SYNC_DATE=03/13/2013
PAGE TITLE: CPU & CHIPSET: SPI and Debug Connector	
Apple Inc.	DRAWING NUMBER: 051-00321
	SIZE: D
	REVISION: 4.0.0
	BRANCH: proto1b
	PAGE: 52 OF 120
	SHEET: 45 OF 96



SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=08/26/2014

PAGE TITLE

SMC: SMBus Connections

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

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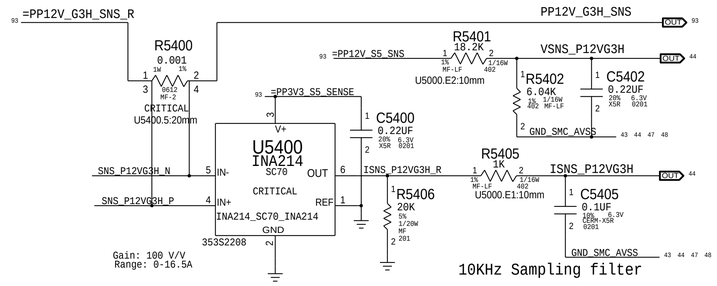
12V G3H (VD2R:ADC0/ID2R:ADC1)

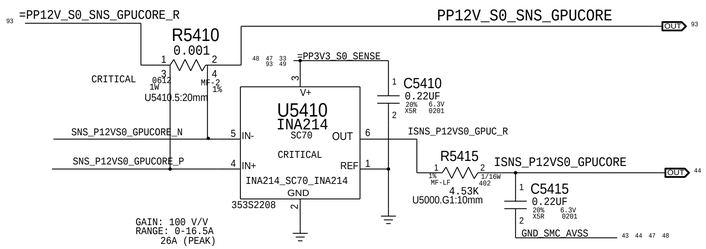
AC/DC lowside sense (System total)



NOTE:VSNS on S5 to avoid burning G3H Power

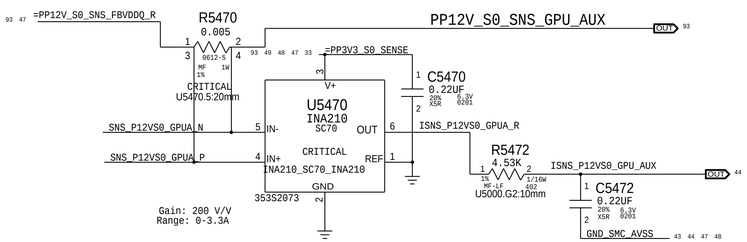
PP12V_S0_GPU (VG1C=VD20, IG1C:ADC17)

GPU highside sense for GPU Core Regulator



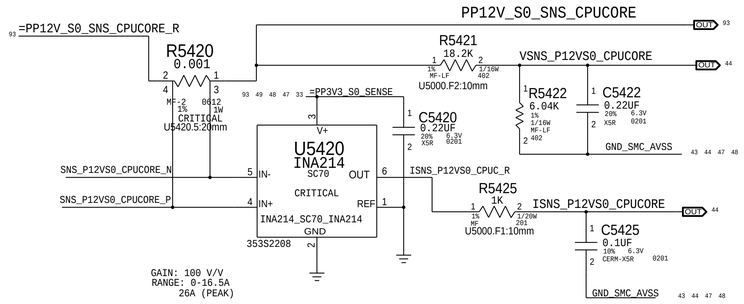
GPU AUX RAILS (VG1A=VD20, IG1A:ADC16)

GPU highside sense for GPU 0.9V & 1.8V VR



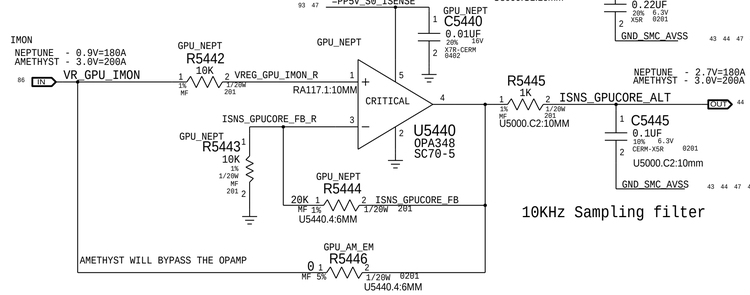
PP12V_S0_CPU (VD20:ADC2 /ID20:ADC3)

CPU highside sense for CPU Core Regulator



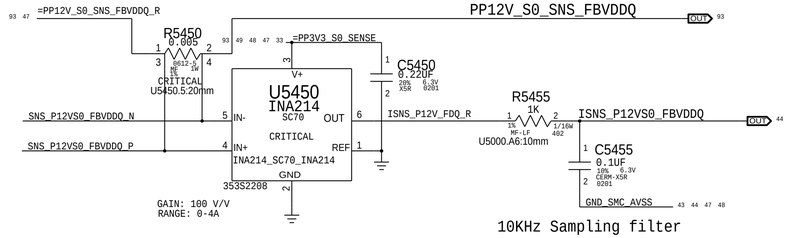
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp

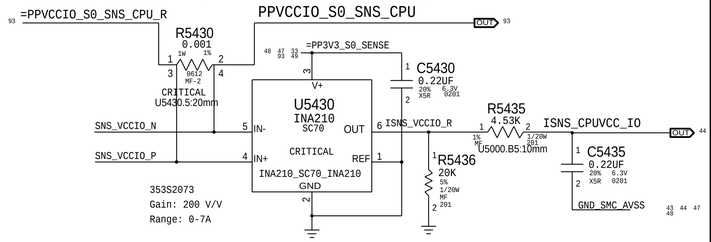


GPU FB (VG1F=VD20, IG1F:ADC11)

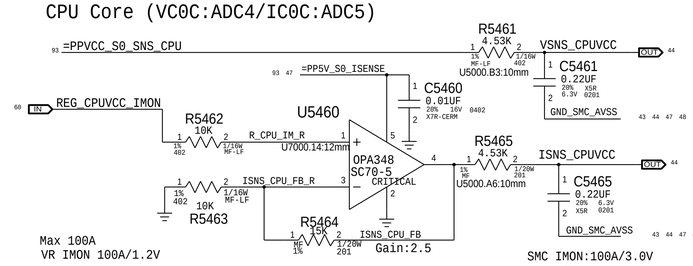
GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



CPU VCCIO (VC0I=tbd, IC0I:ADC8)

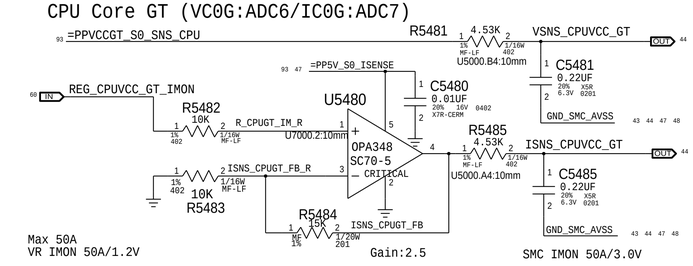


CPU Core (VC0C:ADC4/IC0C:ADC5)

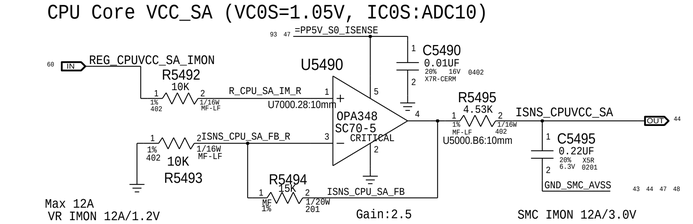


1KHz Sampling filter

CPU Core GT (VC0G:ADC6/IC0G:ADC7)



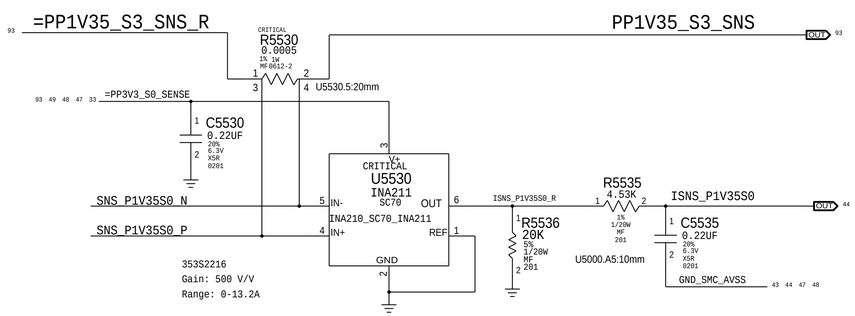
CPU Core VCC_SA (VC0S=1.05V, IC0S:ADC10)



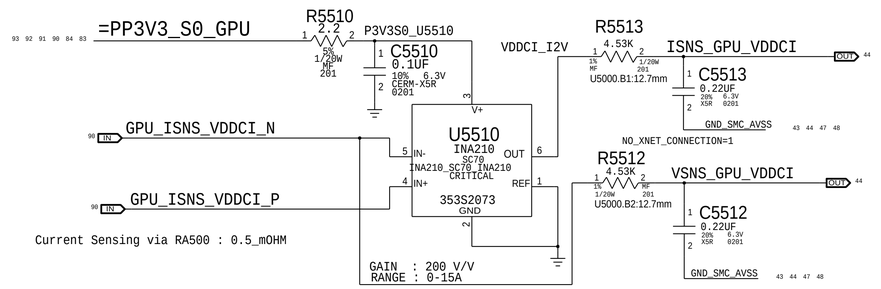
SYNC_MASTER=BRANCH_JERRYCHOW	SYNC_DATE=09/10/2014
PAGE TITLE	SENSORS: I and V Sense
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH proto1b · PAGE 54 OF 120 · SHEET 47 OF 96

VDDQ S3 (VC0M=VM0R, IC0M:ADC9)

VDDQ lowside sense for SO-DIMM modules



GPU_VDDCI S0 (VG0I:ADC14 /IG0I: ADC15)



VDDQ S3 (VM0R:ADC22/ IM0R:ADC23)

VDDQ lowside sense for SO-DIMM modules

HDD S0 (VH05=5V, IH05:ADC19)

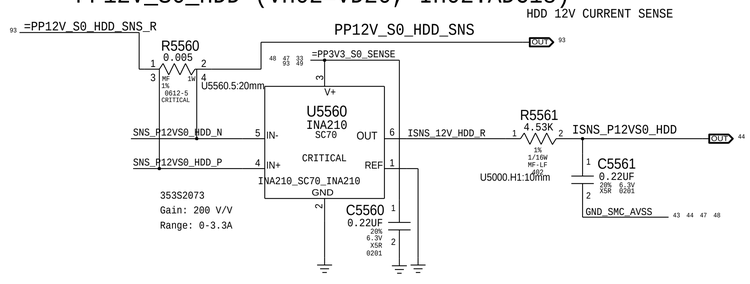
I/V-sense for HDD 5V

SSD S4 (VR1R:ADC20 / IH1R:ADC21)

I-SENSE FOR SSD / V-SENSE FOR PPSSD_S4)

PP12V_S0_HDD (VH02=VD20, IH02:ADC18)

HDD 12V CURRENT SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0201	2	RES,0 OHM,201	C5525,C5526	SSD:N

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE: SENSORS: I and V Sense(Continued)

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D

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BRANCH: proto1b

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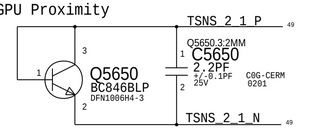
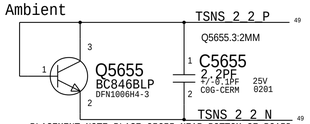
GPU Proximity



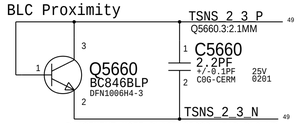
PLACEMENT_NOTE=PLACE Q5650 NEAR GPU AND GDDR5

Ambient



PLACEMENT_NOTE=PLACE Q5655 NEAR BOTTOM OF BOARD

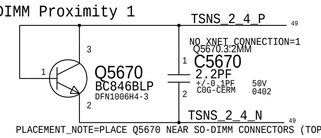
BLC Proximity



PLACEMENT_NOTE=PLACE Q5660 NEAR BLC VR

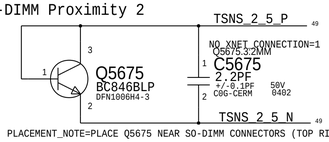
NEED TO FIND LOCATION

SO-DIMM Proximity 1



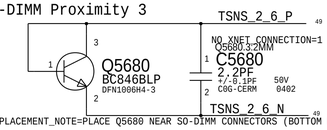
PLACEMENT_NOTE=PLACE Q5670 NEAR SO-DIMM CONNECTORS (TOP LEFT)

SO-DIMM Proximity 2



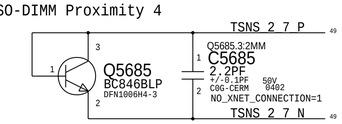
PLACEMENT_NOTE=PLACE Q5675 NEAR SO-DIMM CONNECTORS (TOP RIGHT)

SO-DIMM Proximity 3



PLACEMENT_NOTE=PLACE Q5680 NEAR SO-DIMM CONNECTORS (BOTTOM LEFT)

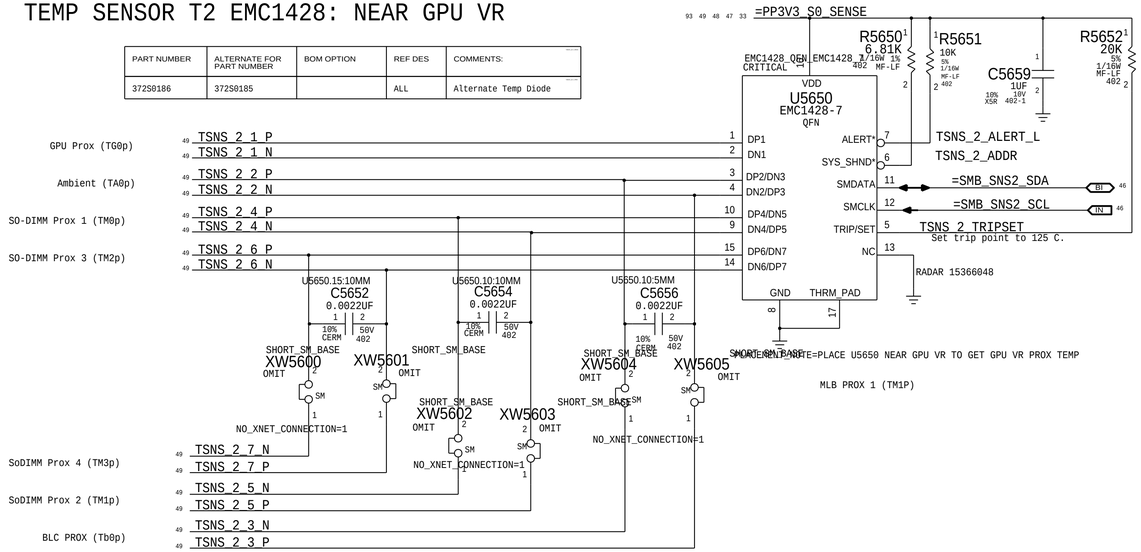
SO-DIMM Proximity 4



PLACEMENT_NOTE=PLACE Q5685 NEAR SO-DIMM CONNECTORS (BOTTOM RIGHT)

TEMP SENSOR T2 EMC1428: NEAR GPU VR

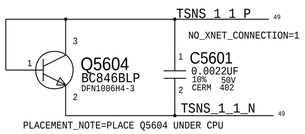
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

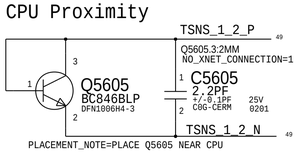
SNS T2: TEMP SENSOR IC

MLB Proximity



PLACEMENT_NOTE=PLACE Q5604 UNDER CPU

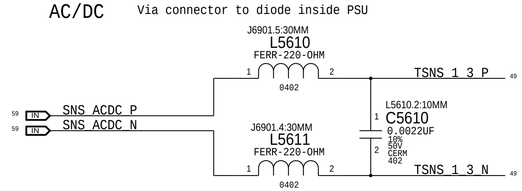
CPU Proximity



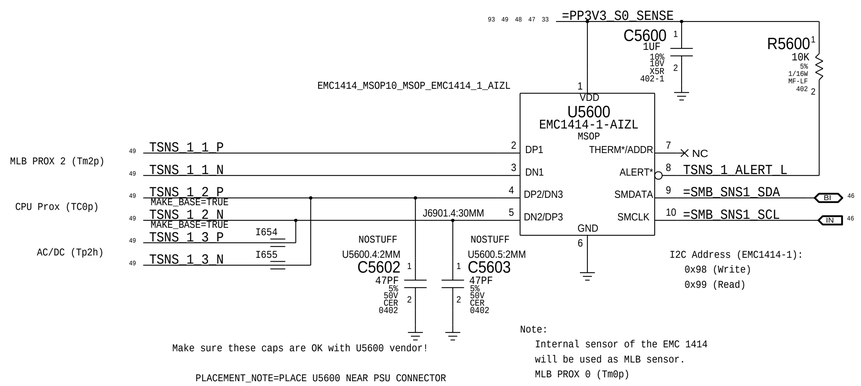
PLACEMENT_NOTE=PLACE Q5605 NEAR CPU

AC/DC

Via connector to diode inside PSU



Temperature Sensor T1 EMC1414: Near PSU Conn



Make sure these caps are OK with U5600 vendor!

PLACEMENT_NOTE=PLACE U5600 NEAR PSU CONNECTOR

I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB PROX 0 (Tm0p)

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE
SENSORS: Temperature Sensors

Apple Inc.

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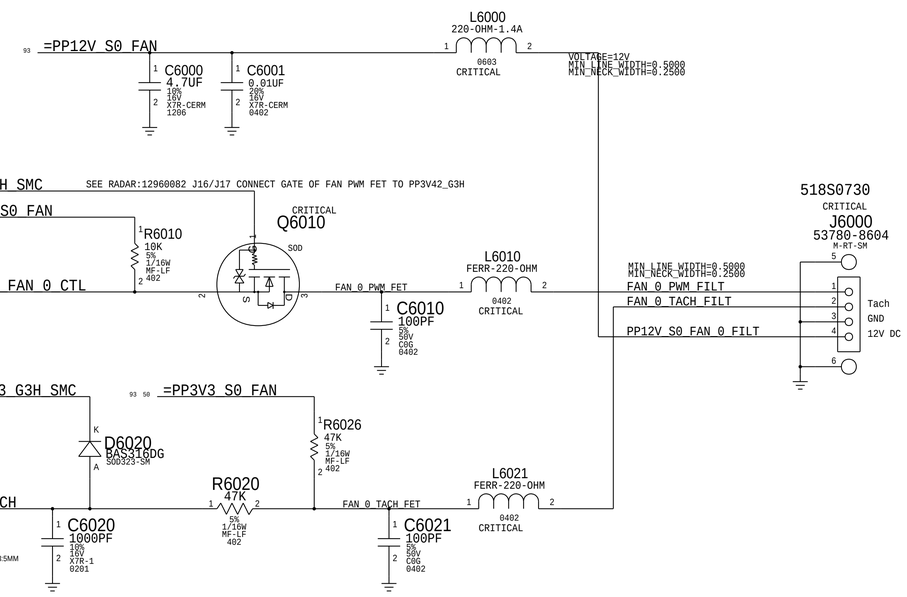
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
FAN: System Fan

Apple Inc.

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AUDIO CODEC
APPLE P/N 353S2592

PLACE C6100 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

PP1V5_S0_AUD_DIG
PLACE_NEAR=U6101.9:12.5mm

C6101 4.7UF 20% 4V X5R-1 402
C6100 0.47UF 10% 10V X5R 0402
C6108 10UF 20% POLY-TANT CASE-B2-SM
C6109 2.2UF 20% 6.3V CERM 402-LF
C6110 2.2UF 20% 6.3V CERM 402-LF
C6102 0.47UF 10% 10V X5R 0402
C6103 10UF 20% 16V POLY-TANT CASE-B2-SM
C6105 1UF 10% 10V X5R 402-1
C6104 0.47UF 10% 10V X5R 0402
C6106 0.47UF 10% 10V X5R 0402
C6107 CRITICAL 10UF 20% 10V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG
GND_AUDIO_CODEC

R6100 2.67K 1% 1/16W MF-LF 402
R6105 0 5% 1/16W MF-LF 402

VBIAS_DAC
CS4206_FP
CS4206_FN

U6101 CRITICAL
CS4206B
QFN

VD	9		
VA_REF	24		
VA_HP	46		
VA	25		
VBIAS_DAC	29		
VHP_FILT+	44		
VHP_FILT-	41		
HPOUT_L	38	MIN_LINE_WIDTH=0.1000	MIN_NECK_WIDTH=0.1000
HPOUT_R	40	MIN_LINE_WIDTH=0.1000	MIN_NECK_WIDTH=0.1000
HPREF	39	MIN_LINE_WIDTH=0.2000	MIN_NECK_WIDTH=0.1000
GPIO0/DMIC_SDA1	2		
GPIO1/DMIC_SDA2 /SPDIF_OUT2	12		
GPIO2	14		
GPIO3	15		
SENSE_A	13		
FLYP	45		
FLYC	43		
FLYN	42		
VL_HD	3		
VL_IF	1		
BITCLK	6		
SYNC	10		
SDI	8		
SDO	5		
RESET*	11		
SPDIF_IN	47		
SPDIF_OUT	48		
LINEOUT_L1+	35		
LINEOUT_L1-	34		
LINEOUT_R1+	36		
LINEOUT_R1-	37		
LINEOUT_L2+	31		
LINEOUT_L2-	30		
LINEOUT_R2+	32		
LINEOUT_R2-	33		
MICBIAS	16		
VCOM	28	CS4206_VCOM	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500
LINEIN_L+	21	NO_TEST=1	
LINEIN_C-	22		
LINEIN_R+	23		
MICIN_L+	18		
MICIN_L-	17		
MICIN_R+	19	NO_TEST=1	
MICIN_R-	20	NO_TEST=1	
VREF+_ADC	27	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500	
DMIC_SCL	4	CS4206_DMIC_SCL	
DGND	7		
THRM_PAD	49		
AGND	26		

TP_AUD_HP_L NC
TP_AUD_HP_R NC
CS4206_HPREF

AUD_LO1_L_P
AUD_LO1_L_N
AUD_LO1_R_P
AUD_LO1_R_N
AUD_LO2_L_P
AUD_LO2_L_N
AUD_LO2_R_P
AUD_LO2_R_N
AUD_CODEC_MICBIAS

AUD_LI_P_L NC
AUD_LI_COM NC
AUD_LI_P_R NC

AUD_MIC_INL_P
AUD_MIC_INL_N
AUD_MIC_INP_R NC
AUD_MIC_INN_R NC
CS4206_VREF_ADC NC

R6104 22 5% 1/16W MF-LF 402
AUD_DMIC_CLK

HP AMP/LINE OUT
TWEETERS

WOOFERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

Q6170 DMC2400UV SOT563 DEVEL_AUDIO CRITICAL
Q6170_P_S
Q6170_P_G
Q6170_N_G
Q6170_N_S
R6170 0 5% 1/16W MF-LF 402
R6171 0 5% 1/16W MF-LF 402

Q6171 DMC2400UV SOT563 DEVEL_AUDIO CRITICAL
Q6171_P_S
Q6171_P_G
Q6171_N_G
Q6171_N_S
R6172 0 5% 1/16W MF-LF 402
R6173 0 5% 1/16W MF-LF 402

DMICS 1 & 2
AUD_DMIC_SDA1
NC TP_AUD_GPIO_1
HP AMP CNTRL AUD_GPIO_2

MAC SPKR AMP CNTRL AUD_CODEC_MICBIAS
D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL AUD_GPIO_3
AUD_SENSE_A

R6106 100K 1% 1/16W MF-LF 402

C6111 2.2UF 20% 6.3V CERM 402-LF
C6112 2.2UF 20% 6.3V CERM 402-LF
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
DP_INT_SPDIF_AUDIO
AUD_SPDIF_OUT

R6101 22 5% 1/16W MF-LF 402
AUD_SDI_R

R6102 22 5% 1/16W MF-LF 402
AUD_SPDIF_CHIP

R6103 100K 1% 1/16W MF-LF 402

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0V

XW6100 SM

C6113 CRITICAL 1UF 10% 20V TANT CASE-P3-HF
C6114 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM
C6115 0.47UF 10% 10V X5R 0402

R6107 100K 1% 1/16W MF-LF 402
R6108 100K 1% 1/16W MF-LF 402
R6109 100K 1% 1/16W MF-LF 402
R6110 100K 1% 1/16W MF-LF 402
R6111 100K 1% 1/16W MF-LF 402

GND_AUDIO_CODEC

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402
=PP5V_S0_AUDIO

VR6101 TPS71745 SON CRITICAL
IN
OUT
EN
NR/FB
GND
NC
4V5_REG_IN
4V5_REG_EN
4V5_NR

PP4V5_AUDIO_ANALOG
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
VOLTAGE=4.5V

R6120 0 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO

C6122 1UF 10% 10V X5R 402-1
C6123 0.1UF 10% 16V X7R-CERM 0402
C6124 1UF 10% 10V X5R 402-1

XW6110 SM
XW6111 SM

MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V
GND_AUDIO_CODEC
GND_AUDIO_HPAMP

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

VR6102 TPS73115 SOT23-5
=PP1V8_S0_AUD_DIG
PLACE_NEAR=VR6102.1:12.5mm
PP1V5_S0_AUD_DIG
NC
GND
GND_AUDIO_CODEC

C6190 1UF 10% 10V X5R 402-1

SYNC_MASTER=J17_DIRK
SYNC_DATE=03/07/2013

PAGE TITLE
AUDIO: CODEC/REGULATORS

Apple Inc.

DRAWING NUMBER 051-00321
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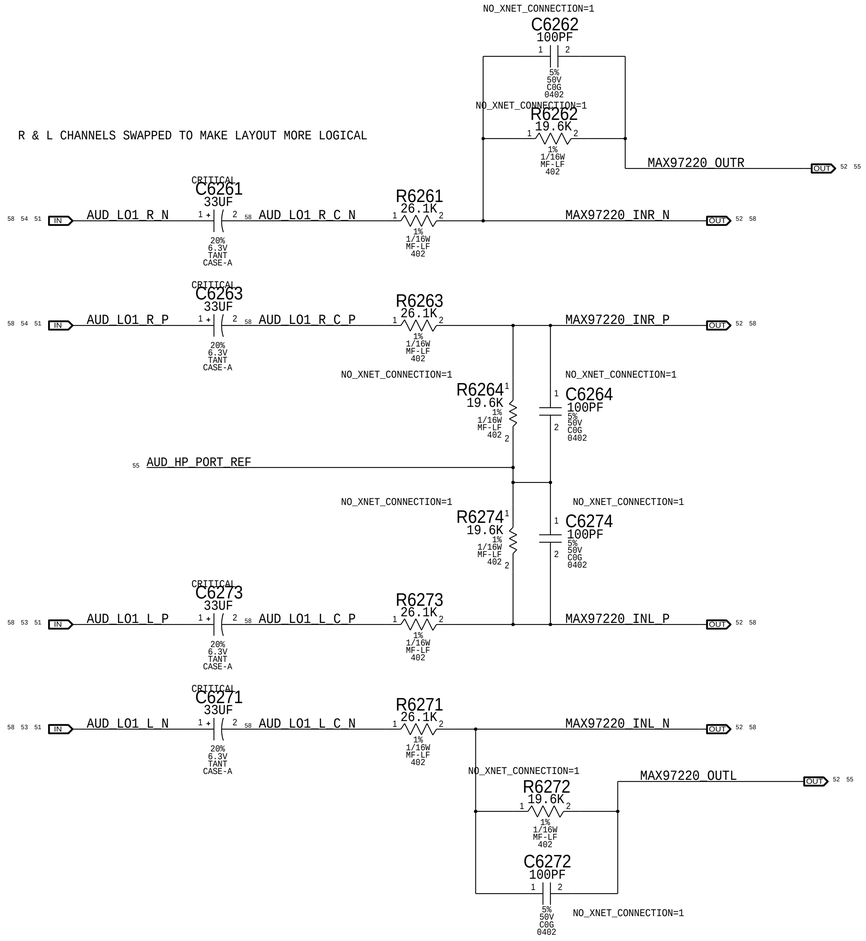
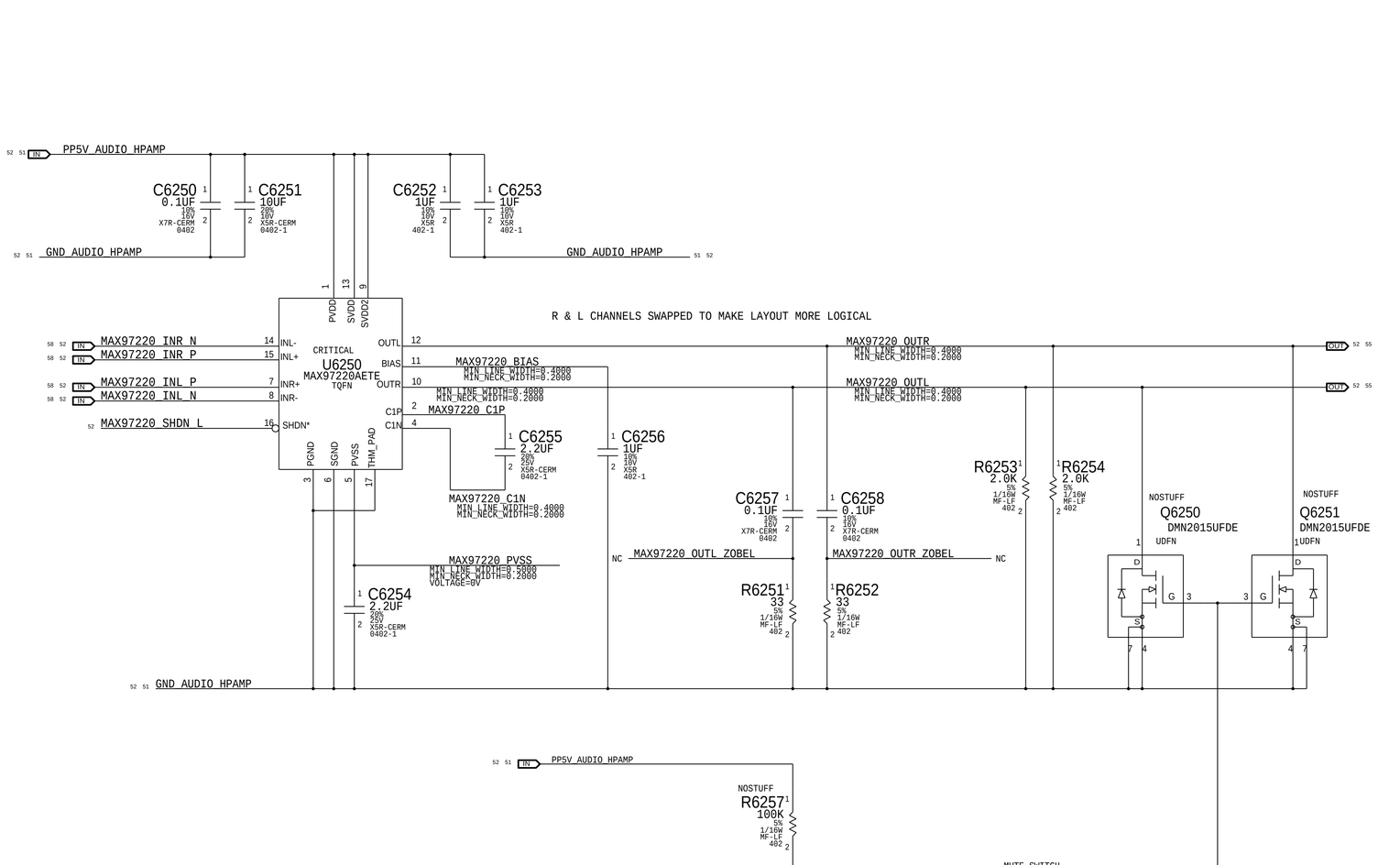
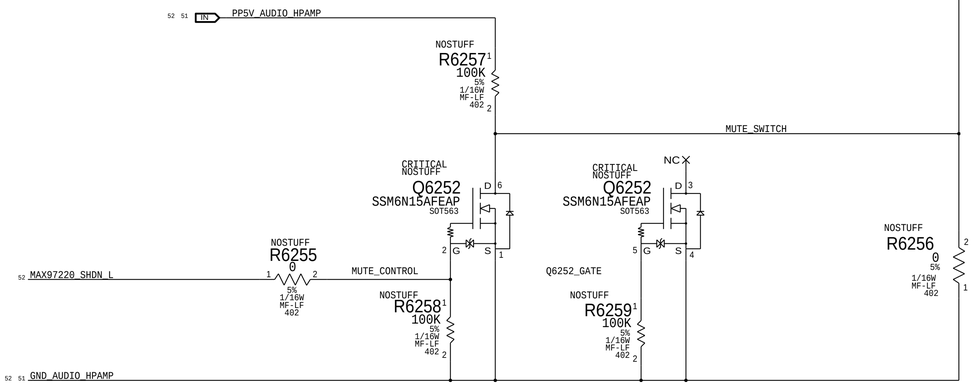
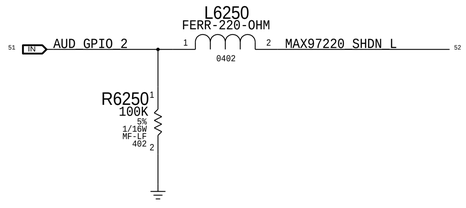
SHEET 51 OF 96









SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE

AUDIO: HEADPHONE AMP

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

93 54 IN =PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

58 54 IN AUD_LO2_L_N — L6300 FERR-1000-OHM 0402 — AUD_LAMP_RINC_P — C6308 1UF 10% 25V X5R 0402 — AUD_LAMP_RIN_P
58 51 IN AUD_LO2_L_P — L6301 FERR-1000-OHM 0402 — AUD_LAMP_RINC_N — C6309 1UF 10% 25V X5R 0402 — AUD_LAMP_RIN_N
58 52 53 IN AUD_LO1_L_P — L6302 FERR-1000-OHM 0402 — AUD_LAMP_LINC_P — C6310 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LIN_P
58 52 53 IN AUD_LO1_L_N — L6303 FERR-1000-OHM 0402 — AUD_LAMP_LINC_N — C6311 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LIN_N

34 35 36 37 PVDD

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	ONLY WOOFERS ON UNDER WINDOWS: 54 53 IN AUD_SPKRAMP_WIN_SHDN_L
16	MONO	53 AUD_LAMP_MONO
9	SDNL*	WOOFERS & TWEETERS ON UNDER MAC OS: 54 53 IN AUD_SPKRAMP_MAC_SHDN_L
11	INL+	
12	INL-	
21	GAIN	53 AUD_LAMP_GAIN
8	VREG/AVDD	53 AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500, VOLTAGE=5V)
23	REGEN	93 57 54 51 37 =PP3V3_S0_AUDIO
17	THERM	TP_AUD_LAMP_THERM — NC
30	BOOTR+	AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500) — C6313 0.22UF 20% 25V X5R 603
28	OUTR+	
29		
26	OUTR-	
27		
25	BOOTR-	AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500) — C6314 0.22UF 20% 25V X5R 603
10	EDGE	AUD_LAMP_EDGE 53
1	BOOTL+	AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500) — C6315 0.22UF 20% 25V X5R 603
2		
3	OUTL+	
4		
5	OUTL-	
6	BOOTL-	AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500) — C6316 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14		
15	TEST	
7 24 41	AGND	
	THERM_PAD	
31 32 33 38 39 40	PGND	

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2500) — 53 AUD_LAMP_OUTNR — L6305 110-OHM-3A DLY5ATN111SQ2 — NO_XNET_CONNECTION=1 — AUD_SPKR_LWFR_OUT_P — NO_XNET_CONNECTION=1 C6323 1000PF 5% 25V CERM 0402 — AUD_SPKR_LWFR_OUT_N
AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2500) — 53 AUD_LAMP_OUTPR
AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2500) — 53 AUD_LAMP_OUTNL — L6307 110-OHM-3A DLY5ATN111SQ2 — NO_XNET_CONNECTION=1 — AUD_SPKR_LTWT_OUT_P — NO_XNET_CONNECTION=1 C6324 1000PF 5% 25V CERM 0402 — AUD_SPKR_LTWT_OUT_N
AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2500) — 53 AUD_LAMP_OUTPL

AUD_SPKR_LWFR_OUT_P — OUT 56 58
AUD_SPKR_LWFR_OUT_N — OUT 56 58
AUD_SPKR_LTWT_OUT_P — OUT 56 58
AUD_SPKR_LTWT_OUT_N — OUT 56 58

NO_XNET_CONNECTION=1
CRITICAL C6320 1000PF 5% 25V CERM 0402
CRITICAL C6322 1000PF 5% 25V CERM 0402
CRITICAL C6319 1000PF 5% 25V CERM 0402
CRITICAL C6321 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=1

C6317 2.2UF 20% 6.3V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

L6308 FERR-1000-OHM 0402
51 IN AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L OUT 53 54
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V C0G 0402

R6308 0 5% 1/16W MF-LF 402
51 IN AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L OUT 53 54
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V C0G 0402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

53 AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE 53
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO 53
NOSTUFF R6306 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN 53
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013
PAGE TITLE: AUDIO: LEFT SPKR AMP
Apple Inc.
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

93 53 IN =PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

58 54 IN AUD_LO2_R_N — L6400 FERR-1000-OHM 0402 — 58 AUD_RAMP_RINC_P — C6408 1UF 10% 25V X5R 0402 — 58 AUD_RAMP_RIN_P
58 54 IN AUD_LO2_R_P — L6401 FERR-1000-OHM 0402 — 58 AUD_RAMP_RINC_N — C6409 1UF 10% 25V X5R 0402 — 58 AUD_RAMP_RIN_N
58 52 51 IN AUD_LO1_R_P — L6402 FERR-1000-OHM 0402 — 58 AUD_RAMP_LINC_P — C6410 4700PF 5% 50V NPO-C0G-CERM 0805 — 58 AUD_RAMP_LIN_P
58 52 51 IN AUD_LO1_R_N — L6403 FERR-1000-OHM 0402 — 58 AUD_RAMP_LINC_N — C6411 4700PF 5% 50V NPO-C0G-CERM 0805 — 58 AUD_RAMP_LIN_N

93 57 53 51 37 =PP3V3_S0_AUDIO

34 35 36 37 PVDD

CRITICAL U6400 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	53 IN AUD_SPKRAMP_WIN_SHDN_L (ONLY WOOFERS ON UNDER WINDOWS)
16	MONO	54 AUD_RAMP_MONO
9	SDNL*	53 IN AUD_SPKRAMP_MAC_SHDN_L (WOOFERS & TWEETERS ON UNDER MAC OS)
11	INL+	
12	INL-	
21	GAIN	54 AUD_RAMP_GAIN
8	VREG/AVDD	54 AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500 VOLTAGE=5V)
23	REGEN	
17	THERM	TP_AUD_RAMP_THERM — NC
30	BOOTR+	AUD_RAMP_BOOTRP (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500) — C6413 0.22UF 20% 25V X5R 603
28 29	OUTR+	
26 27	OUTR-	
25	BOOTR-	AUD_RAMP_BOOTRN (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500) — C6414 0.22UF 20% 25V X5R 603
10	EDGE	54 AUD_RAMP_EDGE
1	BOOTL+	AUD_RAMP_BOOTLP (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500) — C6415 0.22UF 20% 25V X5R 603
2 3	OUTL+	
4 5	OUTL-	
6	BOOTL-	AUD_RAMP_BOOTLN (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500) — C6416 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14	TEST	
15	TEST	
7 24 41	AGND	THRM_PAD
31 32 33 38 39 40	PGND	

C6417 2.2UF 20% 25V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_RAMP_OUTPR (MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2500) — NO_XNET_CONNECTION=1 CRITICAL L6405 110-OHM-3A DLYSATN111SQ2 — AUD_SPKR_RWFR_OUT_P — NO_XNET_CONNECTION=1 CRITICAL C6423 1000PF 5% 25V CERM 0402 — AUD_SPKR_RWFR_OUT_N
AUD_RAMP_OUTNR (MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2500)

AUD_RAMP_OUTPL (MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2500) — NO_XNET_CONNECTION=1 CRITICAL L6407 110-OHM-3A DLYSATN111SQ2 — AUD_SPKR_RTWT_OUT_P — NO_XNET_CONNECTION=1 CRITICAL C6424 1000PF 5% 25V CERM 0402 — AUD_SPKR_RTWT_OUT_N
AUD_RAMP_OUTNL (MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2500)

NO_XNET_CONNECTION=1 CRITICAL C6420 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=1 CRITICAL C6422 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=1 CRITICAL C6419 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=1 CRITICAL C6421 1000PF 5% 25V CERM 0402

EDGE_RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

54 AUD_RAMP_AVDD
R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE 54
NOSTUFF R6405 0 5% 1/16W MF-LF 402
AUD_RAMP_MONO 54 — R6403 0 5% 1/16W MF-LF 402
NOSTUFF R6406 0 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN 54
R6407 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE: AUDIO: RIGHT SPKR AMP

Apple Inc.

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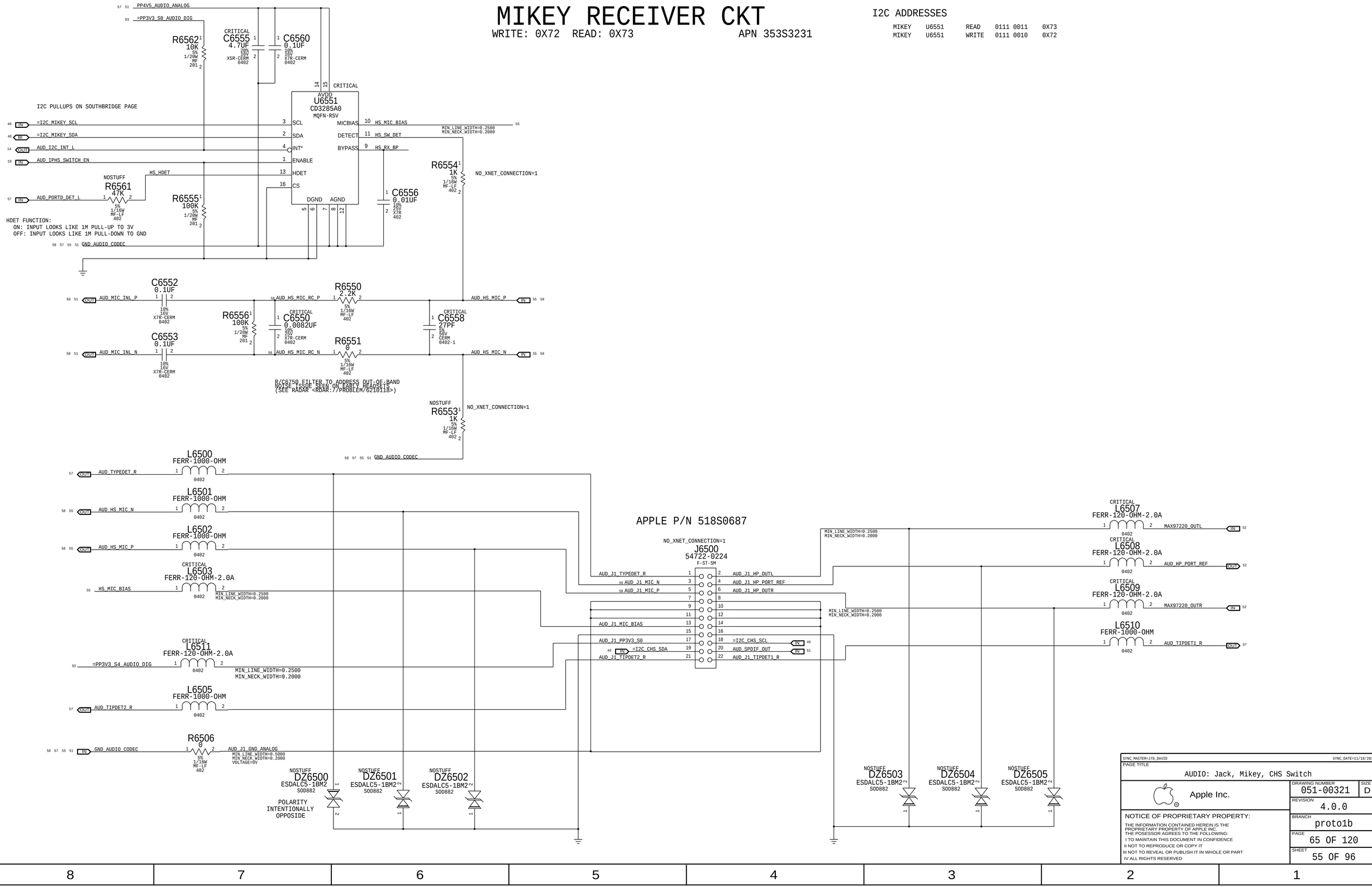
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE

AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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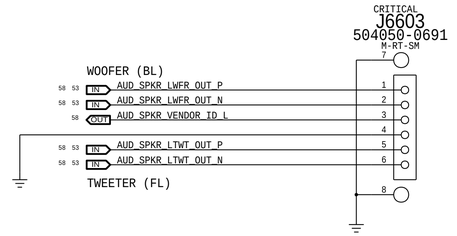
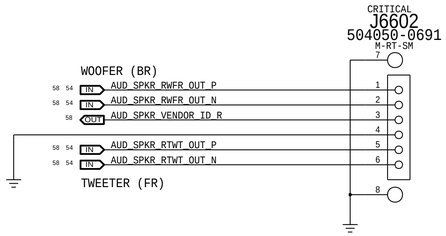
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862





SYNC_MASTER=J17_DIRK SYNC_DATE=03/07/2013

PAGE TITLE

AUDIO: Spkr/Mic Conn.

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

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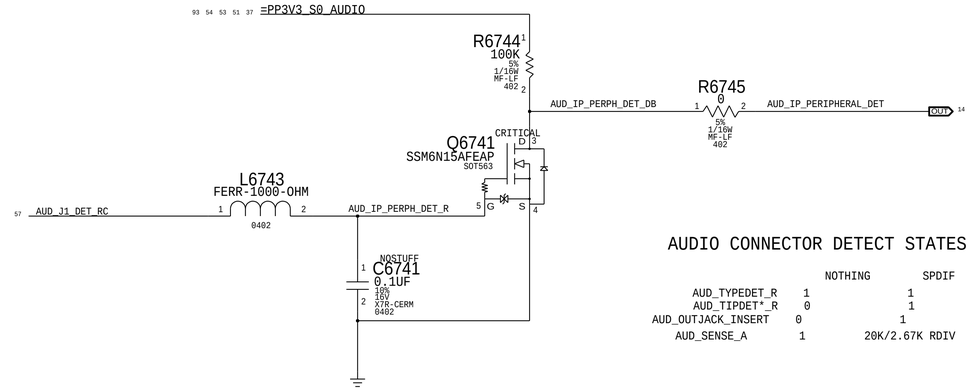
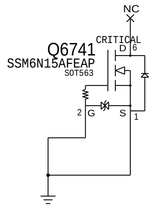
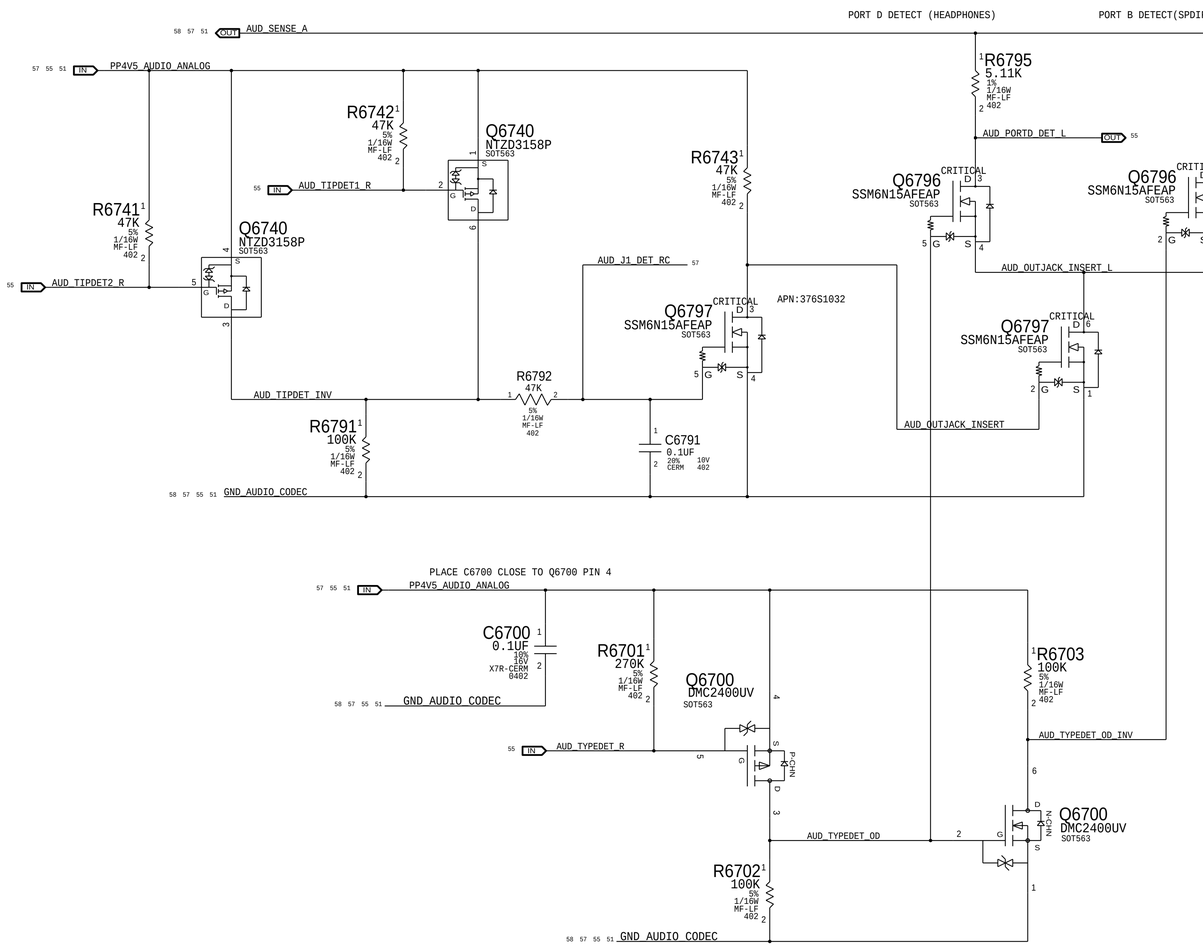
IPHS HS Detect Debounce CKT



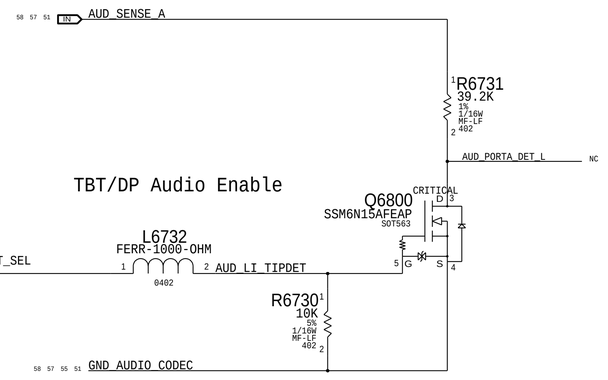
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





Target Display Mode Detect



SYNC_MASTER=J17_DIRK SYNC_DATE=03/07/2013

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

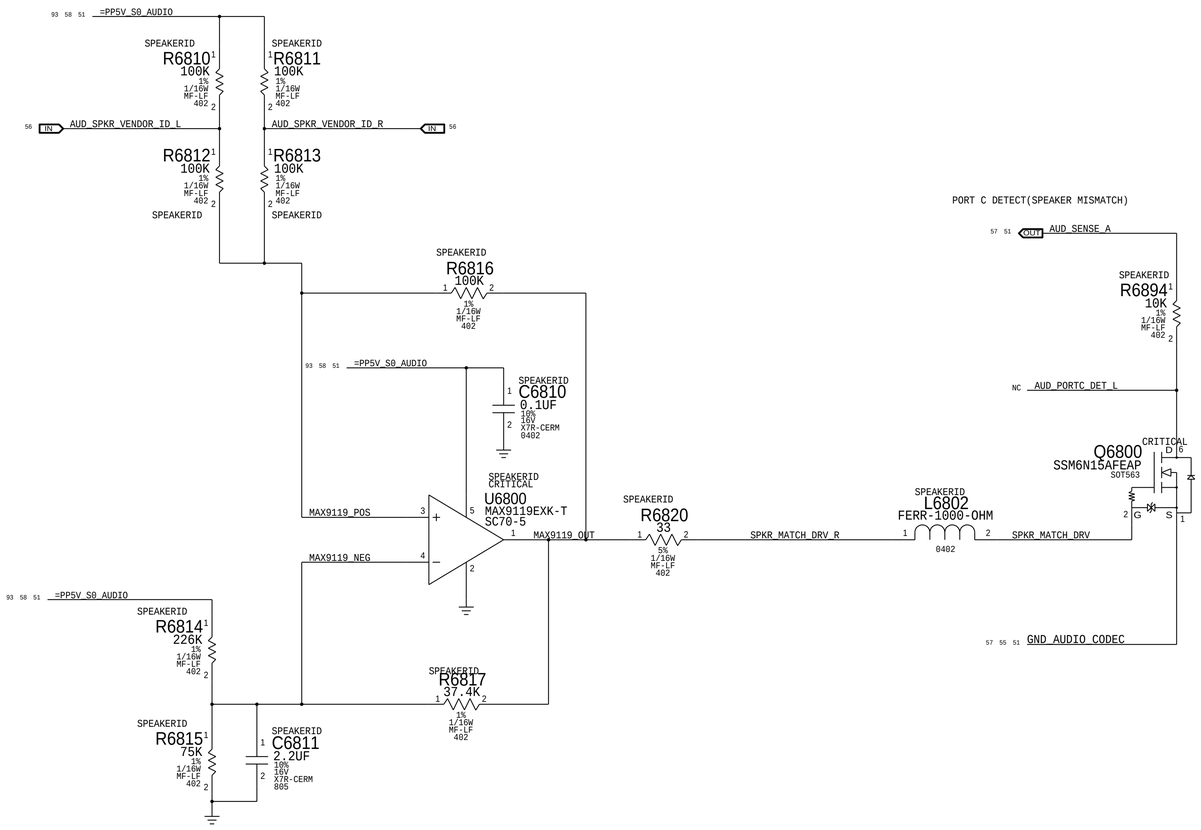
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



PORT C DETECT(SPEAKER MISMATCH)

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
P215 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 52 53
P216 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 52 53
P217 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	52
P218 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	52
P211 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 52 54
P212 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 52 54
P219 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	52
P220 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	52
P209 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
P208 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
P207 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 54
P206 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 54
P205 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	54
P203 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	54
P229 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	54
P230 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	54
P227 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	54
P225 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	54
P224 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	54
P226 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	54
P228 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	53
P235 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	53
P237 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	53
P238 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	53
P240 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	53
P239 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	53
P234 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	53
P233 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	53
P236 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	52
P238 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	52
P237 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	52
P239 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	52
P241 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	54 56
P242 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	54 56
P243 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	54 56
P244 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	54 56
P245 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	53 56
P246 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	53 56
P247 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	53 56
P248 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	53 56
P231 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 55
P232 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 55
P221 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	55
P222 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	55
P214 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	55
P213 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	55
P210 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	55
P204 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	55

SYNC_MASTER=J78_DAVID SYNC_DATE=11/21/2013

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D

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BRANCH: proto1b

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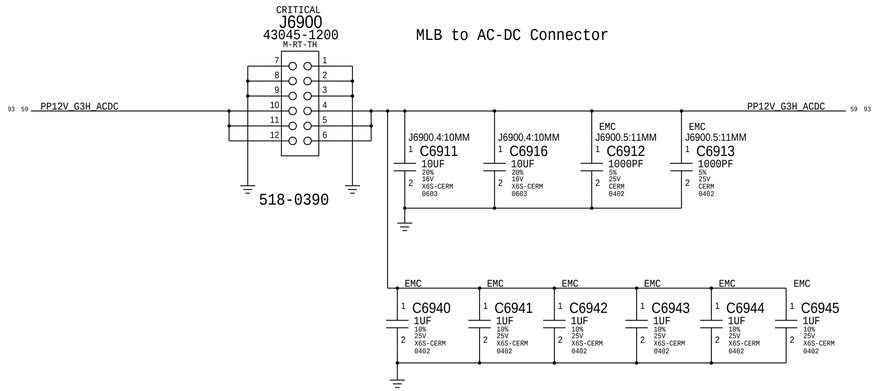
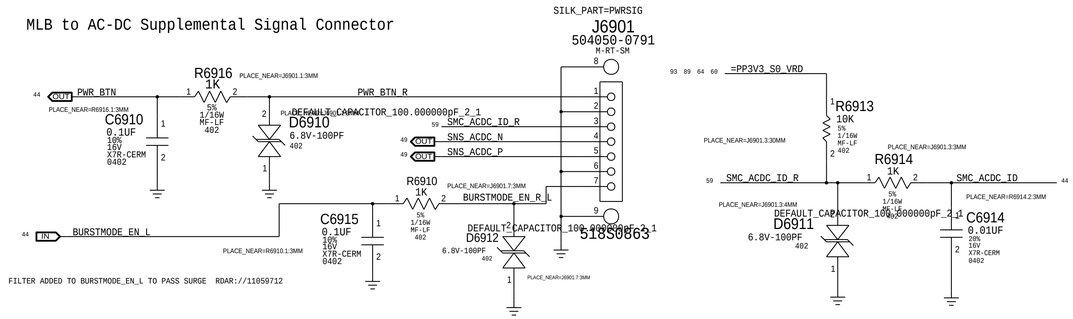
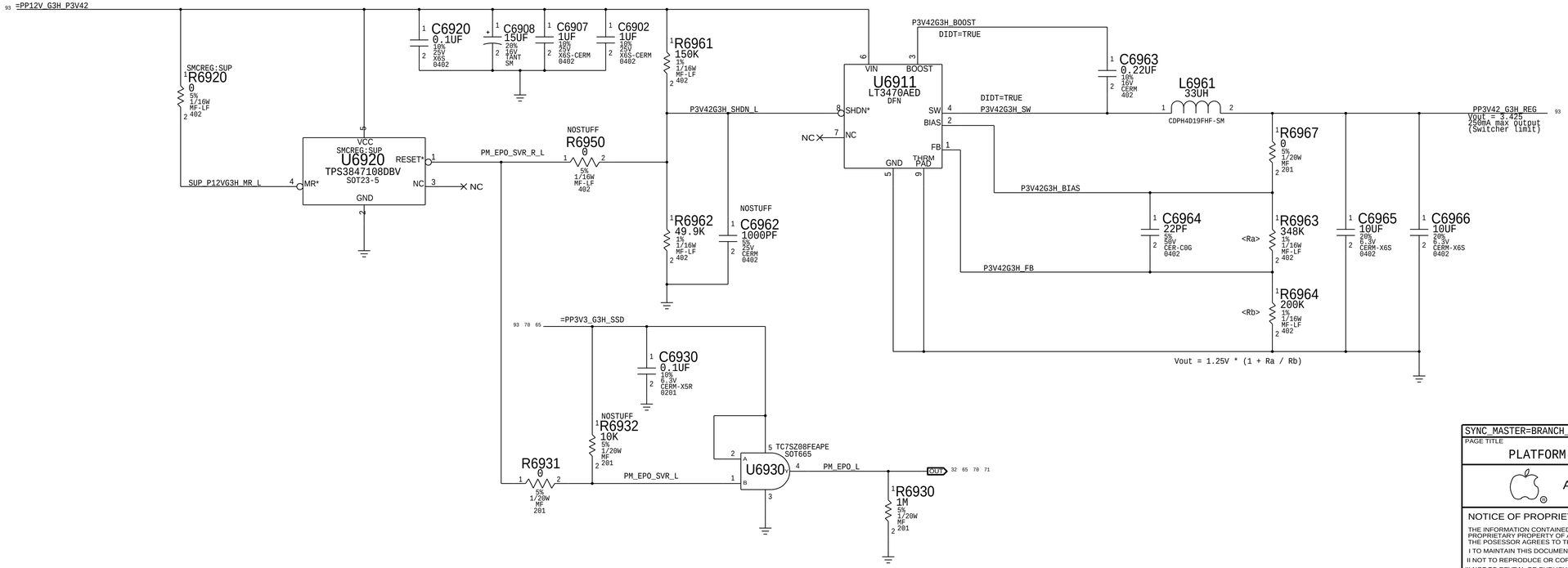




3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)



SYNC_MASTER=BRANCH_HCHENG	SYNC_DATE=10/29/2014
PAGE TITLE	PLATFORM POWER: Connectors / VReg G3Hot
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
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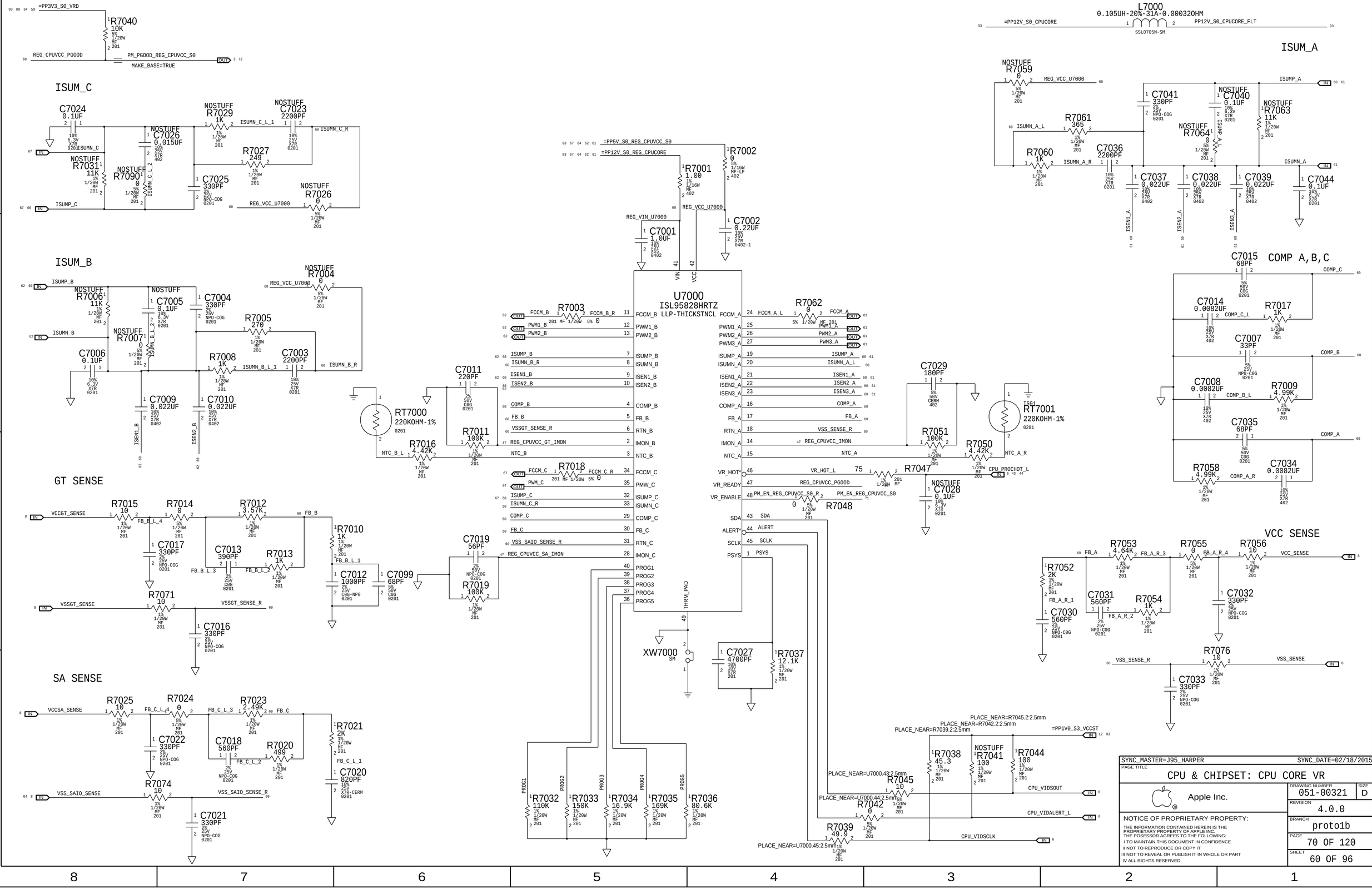

SYNC_MASTER=J95_HARPER SYNC_DATE=02/18/2015

PAGE TITLE

CPU & CHIPSET: CPU CORE VR

Apple Inc.

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CPU VCC Regulator
EDC = 100A
TDC = 70A

CPU VCORE Phase 1

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A1
BOOST_A_1_RC
BOOST_A_1
PHASE_A_1
SW_A_1
FCCM_A
DSBL_A_1
PWM1_A
THWN_A_1
REG_SNUBBER_CPUVCC_1
REG_CPUVCC_ISNS_1_P
REG_CPUVCC_ISNS_1_N
ISEN1_A
ISUMP_A
PPVCC_S0_CPU_REG

Q7110 SIC625CD MLP-THICKSTNCL

CPU VCORE Phase 2

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A2
BOOST_A_2_RC
BOOST_A_2
PHASE_A_2
SW_A_2
FCCM_A
DSBL_A_2
PWM2_A
THWN_A_2
REG_SNUBBER_CPUVCC_2
REG_CPUVCC_ISNS_2_P
REG_CPUVCC_ISNS_2_N
ISEN2_A
ISUMP_A

Q7130 SIC625CD MLP-THICKSTNCL

CPU Phase 3

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A3
BOOST_A_3_RC
BOOST_A_3
PHASE_A_3
SW_A_3
FCCM_A
DSBL_A_3
PWM3_A
THWN_A_3
REG_SNUBBER_CPUVCC_3
REG_CPUVCC_ISNS_3_P
REG_CPUVCC_ISNS_3_N
ISEN3_A
ISUMP_A

Q7150 SIC625CD MLP-THICKSTNCL

CPU VCORE OUTPUT DECOUPLING

PPVCC_S0_CPU_REG

DRAWING	LAST_MODIFIED=Thu Feb 26 18:42:55 2015
	SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCC)
	Apple Inc.
DRAWING NUMBER	051-00321
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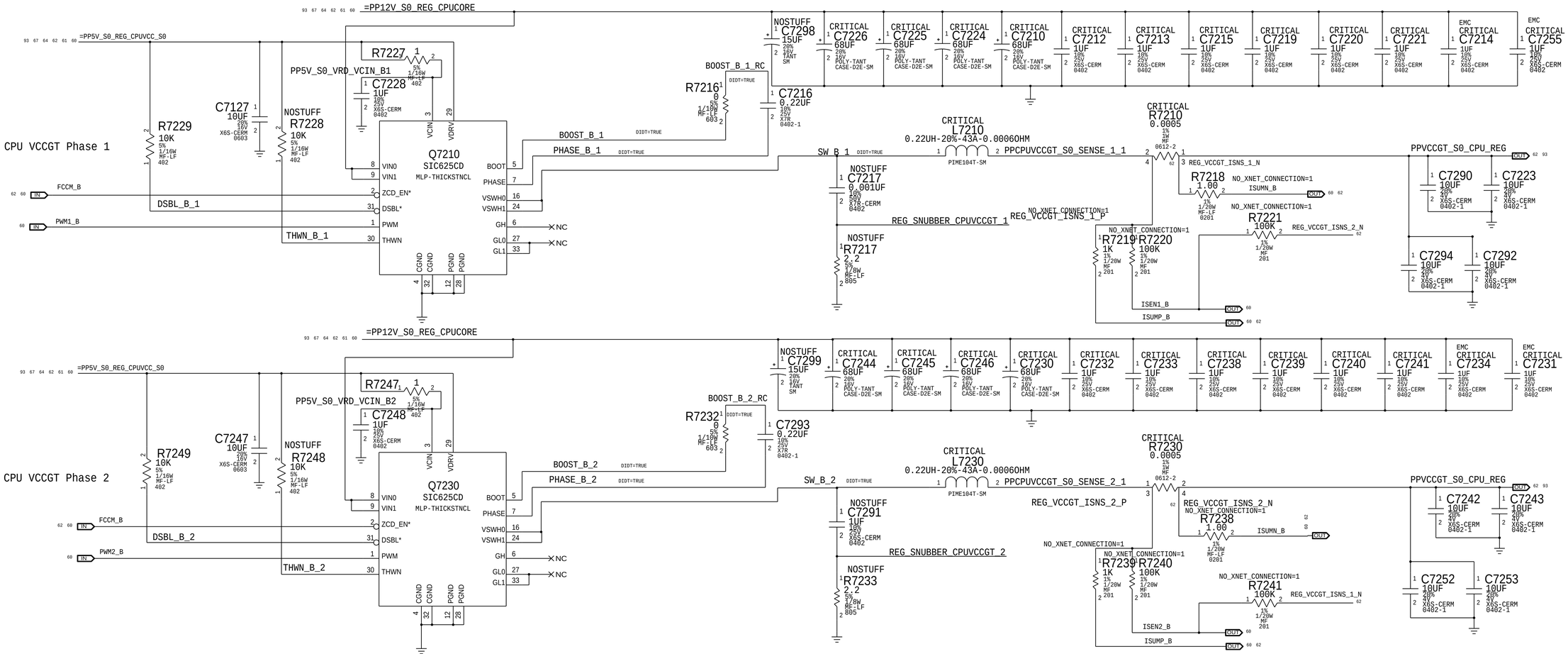
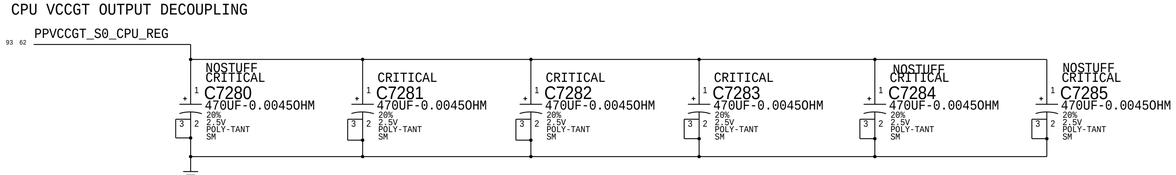
CPU VCCGT Regulator

EDC = 51A

TDC = 37A



CPU VCCGT OUTPUT DECOUPLING



DRAWING	LAST_MODIFIED=Thu Feb 26 18:42:55 2015
SYNC_MASTER=J95_HCHENG	SYNC_DATE=02/24/2015
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
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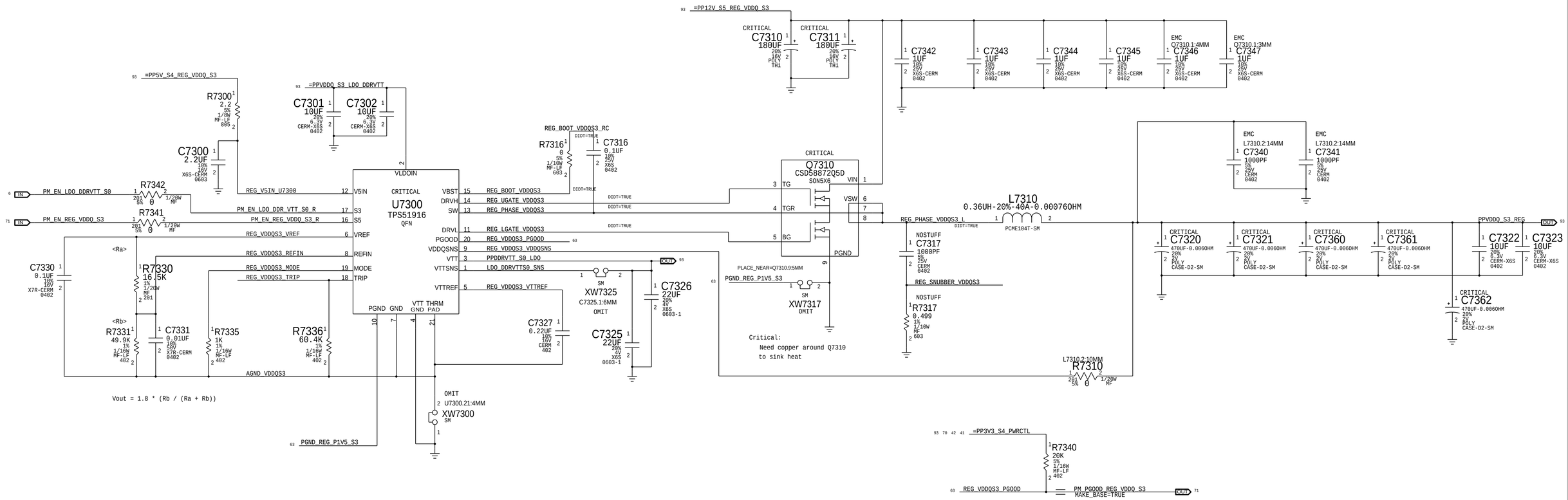
VDDQ (1.35V) S3 REGULATOR

EDC = 20A

TDC = 14A



SYNC_MASTER=BRANCH_HCHENG SYNC_DATE=10/29/2014

PAGE TITLE

CPU & CHIPSET: CPU VDDQ VR

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

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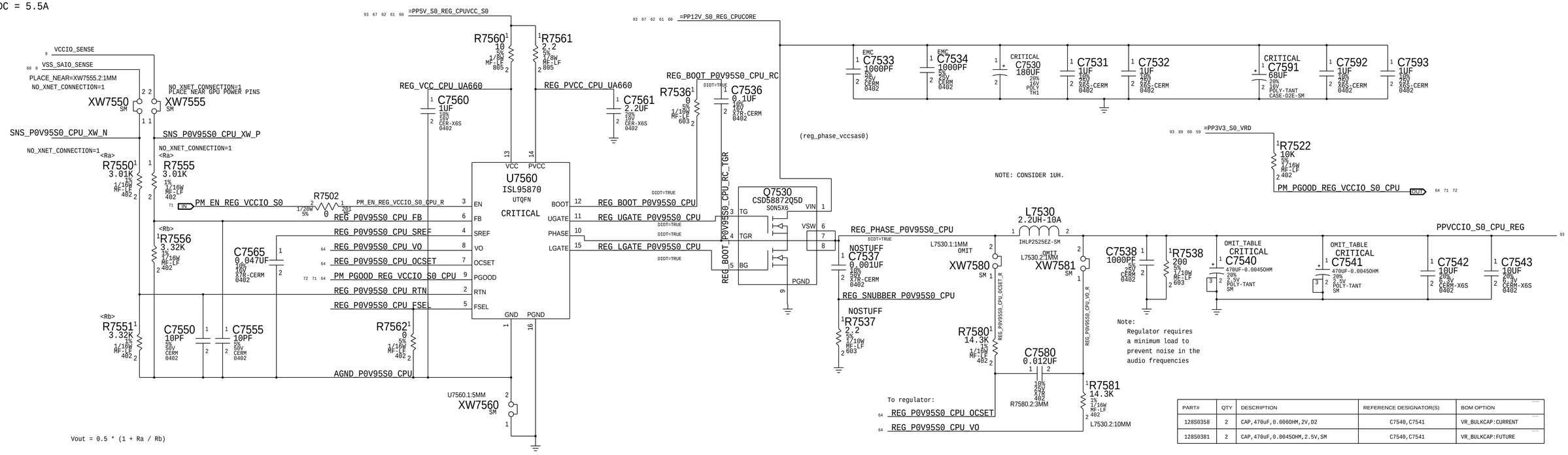
VCCIO (0.95V) S0 REGULATOR

EDC = 5.5A

TDC = 5.5A



Vout = 0.5 * (1 + Ra / Rb)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C7540,C7541	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.0045OHM,2.5V,SM	C7540,C7541	VR_BULKCAP:FUTURE

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:55 2015

SYNC_MASTER=J95_HARPER SYNC_DATE=02/13/2015

PAGE TITLE: CPU & CHIPSET: CPU VCCIO VR

Apple Inc.

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3.3V S5 Regulator

EDC = 12.46A

TDC = 9.4A

5V S4 Regulator

EDC = 6.5A

TDC = 5.9A

3V3 S5 FET NON SSD

Vout = 0.6 * (1 + Ra / Rb)

DCR(L7610) = 11.2 MOHM (TYP) / 12.5 MOHM (MAX)

DCR(L7650) = 6.2 MOHM (TYP) / 6.9 MOHM (MAX)

Input: 2.4V to 5.5V

SYNC_MASTER=J95_HCHENG	SYNC_DATE=02/24/2015
PAGE TITLE	PLATFORM POWER: 3.3V S5/5V S4 VR
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
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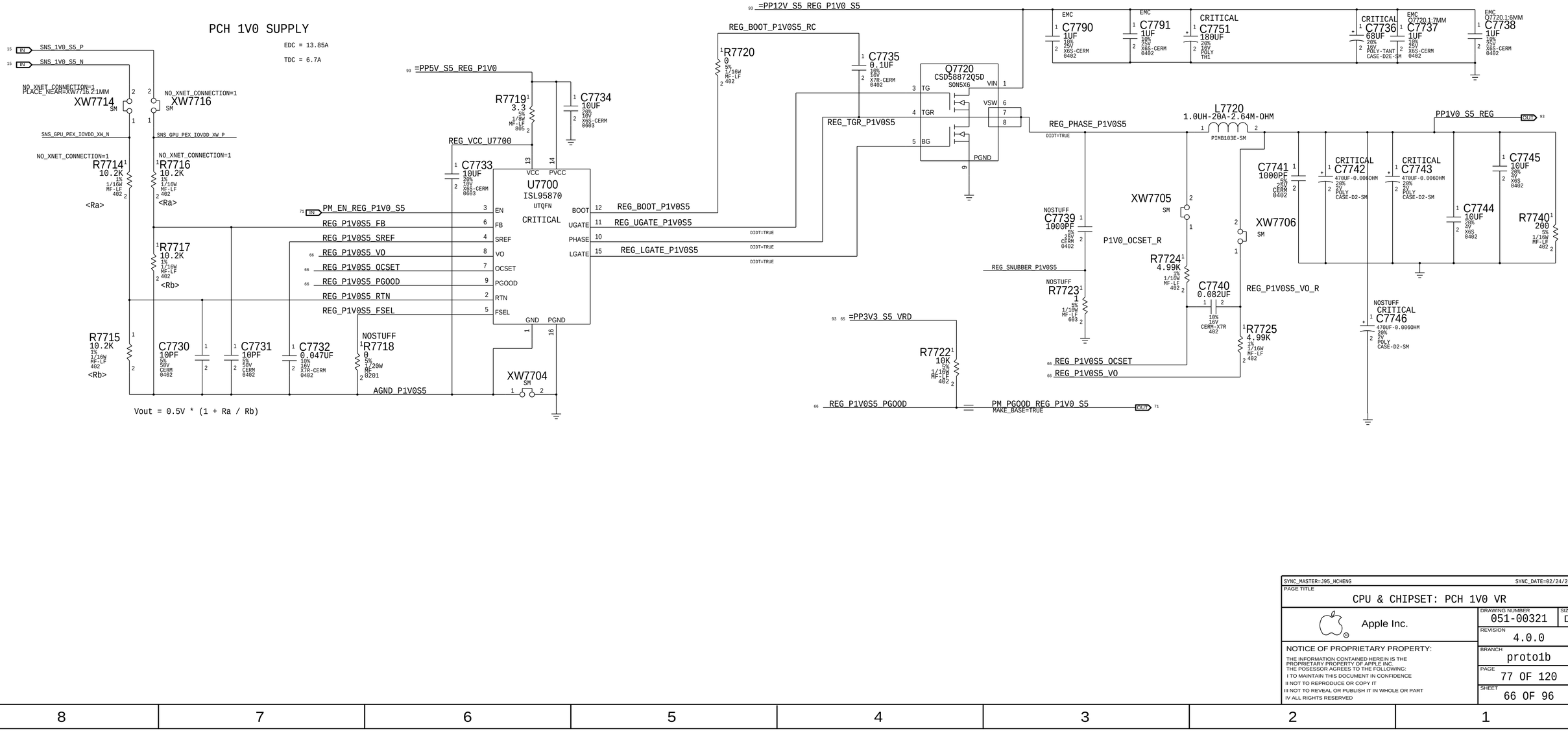
PCH 1V0 SUPPLY

EDC = 13.85A

TDC = 6.7A



SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015

PAGE TITLE

CPU & CHIPSET: PCH 1V0 VR

Apple Inc.

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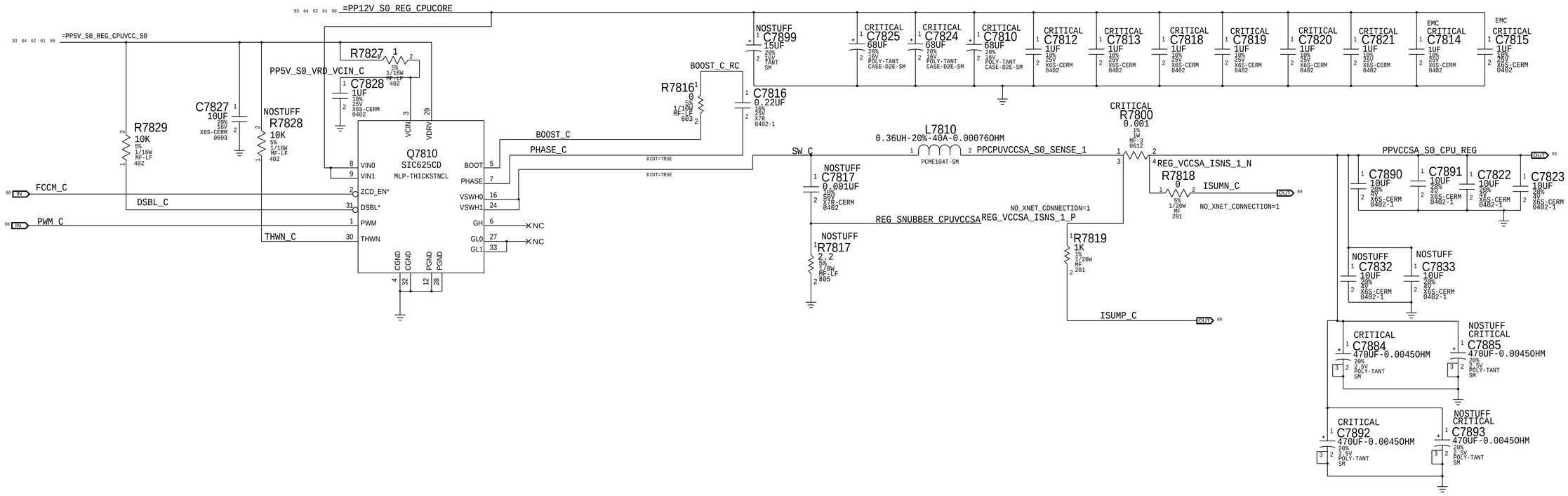
CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A



DRAWING	LAST_MODIFIED=Thu Feb 26 18:42:56 2015
SYNC_MASTER=J95_HCHENG	SYNC_DATE=02/24/2015
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCSA)
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OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

PP12V_S0_BKLT_PWR
D8103 SOD-323 SBR130S3
C8140 1000PF 5% 25V CERM 0402
C8141 1000PF 5% 25V CERM 0402
C8102 10UF 10% 25V X7R-CERM 1206-1 CRITICAL
C8103 10UF 10% 25V X7R-CERM 1206-1 CRITICAL
C8114 100UF 20% 35V ELEC 6.3X11-TH CRITICAL
PLACE C8114 NEAR HIGHER FREQUENCY CAPS
GND

OMIT_TABLE
L8100 33UH-20%-10A-0.03510HM
IHLP6767GZ-IHLP4040DZ11-SM
BKLT_PHASE
D8101 VS-8TQ100SPBF TO263
NOSTUFF R8123 4.7 5% 1/10W MF-LF 603
BKLT_SNUBBER
NOSTUFF C8113 100PF 5% 100V C0G-CERM 0603
GND

OMIT_TABLE OMIT_TABLE
C8119 100PF 5% 100V C0G-CERM 0603
C8106 2.2UF 10% 100V X7S-CERM 1206
C8108 2.2UF 10% 100V X7S-CERM 1206
C8109 15UF 20% 100V ELEC TH-COMBO CRITICAL
C8118 15UF 20% 100V ELEC TH-COMBO CRITICAL
C8120 100PF 5% 100V C0G-CERM 0603
GND
BKLT_BOOST

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1078	138S0810		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0782	371S0783		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211 TO Q8219	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR

PP3V3_S0_BKLT_VDDIO
PP5V_S0_BKLT_VDDD
PP5V_S0_BKLT_VDDA
PP12V_S0_BKLT_FILT
OMIT_TABLE
BKLT_GATE_R
R8119 0 5% 1/8W MF-LF 805
BKLT_SNSP_R
Q8120 IRF6643TRPBF DIRECTFET-MZ
R8114 20 5% 1/8W MF-LF 805
R8102 0.03 1% 2W MF 2512-LF
BKLT_SNSN_R
R8113 887K 1% 1/16W MF-LF 402
R8112 330K 1% 1/8W MF 0402
XW8109 SHORT-1206
C8110 1000PF 10% 100V X7R-CERM 0603
R8104 887K 1% 1/16W MF-LF 402
R8103 330K 1% 1/8W MF 0402
C8111 1000PF 10% 100V X7R-CERM 0603
BKLT_PHASE
Q8121 IRF6645PBF DIRECTFET-SJ
BKLT_GATE_R
BKLT_SNSP_R

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
353S00079	1	IC,PLP8565A13,LED BCKLGHT CTRL,7X7 QFN56	U8100	CRITICAL	
126-0190	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	

U8100 LP8565A13RWC WQFN

BKLT_SHUTDOWN	39	SD	
	40	UVLO_OVP	
=I2C_BKLT_SDA	9	SDA	
=I2C_BKLT_SCL	8	SCL	
DP_INTPNL_ML_HPD_R	2	HPD	
TCON_BLC_EN	3	BL_EN	
BKLT_FAULT_INT_R_L	12	INT	
BLC_VSYNC_R	10	BRT_SYNC	
BKLT_PWM_IN	7	PWM	
BLC_LSYNC_R	11	SYNC	
BKLT_PLL_FILT	43	FILTER	
BKLT_ANG_TEST	32	ANALOG_TEST	
BKLT_DIG_TEST	1	DIGITAL_TEST	
PP12V_S0_BKLT_PWR_R	38	VING	
BKLT_GD_RAIL	37	BST_GD_RAIL	
BKLT_NC_TEST	13	NC	
BST_GD	36	BKLT_GATE	
BST_ISENSE_P	34	BKLT_SNSP	
BST_ISENSE_N	33	BKLT_SNSN	
BST_FB	31	BKLT_BST_FB	
BST_SHORT_FB	30	BKLT_BST_SHORT_FB	
LED1_HDR	14	BKLT_VSEN1	IN
LED1_GD	15	BKLT_GD1	OUT
LED1_R	16	BKLT_ISEN1_Q	IN
LED2_HDR	17	BKLT_VSEN2	IN
LED2_GD	18	BKLT_GD2	OUT
LED2_R	19	BKLT_ISEN2_Q	IN
LED3_HDR	20	BKLT_VSEN3	IN
LED3_GD	21	BKLT_GD3	OUT
LED3_R	22	BKLT_ISEN3_Q	IN
LED4_HDR	24	BKLT_VSEN4	IN
LED4_GD	25	BKLT_GD4	OUT
LED4_R	26	BKLT_ISEN4_Q	IN
LED5_HDR	29	BKLT_VSEN5	IN
LED5_GD	27	BKLT_GD5	OUT
LED5_R	28	BKLT_ISEN5_Q	IN
LED6_HDR	44	BKLT_VSEN6	IN
LED6_GD	45	BKLT_GD6	OUT
LED6_R	46	BKLT_ISEN6_Q	IN
LED7_HDR	47	BKLT_VSEN7	IN
LED7_GD	48	BKLT_GD7	OUT
LED7_R	49	BKLT_ISEN7_Q	IN
LED8_HDR	51	BKLT_VSEN8	IN
LED8_GD	52	BKLT_GD8	OUT
LED8_R	53	BKLT_ISEN8_Q	IN
LED9_HDR	54	BKLT_VSEN9	IN
LED9_GD	55	BKLT_GD9	OUT
LED9_R	56	BKLT_ISEN9_Q	IN

GNDA	41
GNDD	6
LED_GND1	23
LED_GND2	50
GND_BST_GD	35
THRM PAD	57
VDDIO	4
VDDD	5
VDDA	42

BKLT_PLL_FILT
R8111 270K 5% 1/16W MF-LF 402
D8102 SOD-523 BAT54XV2T1 NOSTUFF
C8115 330PF 5% 25V C0G 402
BKLT_PLL_FILT_R
C8116 4700PF 10% 50V X7R-CERM 0402
BKLT_GNDA

BKLT_GD_RAIL
C8145 0.1UF 10% 25V X6S 0402 NOSTUFF
C8117 0.1UF 10% 25V X6S 0402
BKLT_GND_BST_GD

R8140 0 MF-LF 1/16W 5% 402 NOSTUFF BKLT_GD_RAIL
R8138 1 5% 1/16W MF-LF 402 PP12V_S0_BKLT_PWR
PP12V_S0_BKLT_PWR_R
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
C8142 1UF 10% 25V X7R 0603
C8143 0.01UF 10% 16V X7R-CERM 0402
C8144 0.1UF 10% 16V X7R-CERM 0402
BKLT_GND_BST_GD

XW8105 SMD BKLT_GNDA
XW8106 SMD BKLT_GNDD
XW8108 SMD BKLT_GND_BST_GD

R8137 1 5% 1/16W MF-LF 402 =PP5V_S0_BKLT
PP5V_S0_BKLT_VDDA
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
C8137 22UF 20% 10V X5R-CERM 0603
C8138 0.01UF 10% 16V X7R-CERM 0402
C8139 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDA

R8131 1 5% 1/16W MF-LF 402 =PP5V_S0_BKLT
PP5V_S0_BKLT_VDDD
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
C8131 22UF 20% 10V X5R-CERM 0603
C8132 0.01UF 10% 16V X7R-CERM 0402
C8133 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

R8134 1 5% 1/16W MF-LF 402 =PP3V3_S0_BKLT
PP3V3_S0_BKLT_VDDIO
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
C8134 1UF 10% 25V X7R 0603
C8135 0.01UF 10% 16V X7R-CERM 0402
C8136 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

=PP3V3_S0_BKLT
R8124 4.7K MF 1/20W 5%
BKLT_FAULT_INT_L
R8172 0 5% 1/16W MF-LF 402 BKLT_FAULT_INT_R_L

R8106	200K	1%	DP_INTPNL_HPD_R
R8105	100K	1%	TCON_BLC_EN
R8107	10K	5%	BKLT_PWM_IN
R8121	10K	5% NOSTUFF	BLC_VSYNC_R
R8120	10K	5% NOSTUFF	BLC_LSYNC_R

R8173 0 MF-LF 1/16W 5% 402 DP_INTPNL_HPD
R8170 0 MF-LF 1/16W 5% 402 BLC_VSYNC
R8139 0 NOSTUFF MF-LF 1/16W 5% 402
R8171 0 MF-LF 1/16W 5% 402 BLC_LSYNC

R8180	10K	BKLT_ANG_TEST
R8181	10K	BKLT_DIG_TEST
R8182	10K	BKLT_NC_TEST

BKLT_GNDA

BKLT_SNSP R8125 0 5% 1/10W MF-LF 402 BKLT_SNSP_R
C8130 1000PF 10% 100V X7R 603 NOSTUFF
BKLT_SNSN R8191 0 5% 1/10W MF-LF 402 BKLT_SNSN_R

LED_RETURN_1_FB
LED_RETURN_2_FB
LED_RETURN_3_FB
LED_RETURN_4_FB
LED_RETURN_5_FB
LED_RETURN_6_FB
LED_RETURN_7_FB
LED_RETURN_8_FB
LED_RETURN_9_FB

BKLT_BOOST
C8122 470PF 5% 100V CER-C0G 0603
C8124 470PF 5% 100V CER-C0G 0603
C8126 470PF 5% 100V CER-C0G 0603
C8128 470PF 5% 100V CER-C0G 0603
C8121 470PF 5% 100V CER-C0G 0603
C8123 470PF 5% 100V CER-C0G 0603
C8125 470PF 5% 100V CER-C0G 0603
C8127 470PF 5% 100V CER-C0G 0603
C8129 470PF 5% 100V CER-C0G 0603

=PP12V_S0_BKLT
F8100 6AMP-32V 0603-1
PP12V_BKLT_SNS
R8132 0.005 1% 1/4W MF 1206-1 CRITICAL
PP12V_BKLT_FUSED
FB8108 160-OHM-6A 1206 CRITICAL
PP12V_S0_BKLT_FILT
Q8119 FDMS6681Z POWER56
PP12V_S0_BKLT_PWR
C8171 0.1UF 10% 25V X6S 0402 NOSTUFF
R8101 330K 1% 1/8W MF 0402 NOSTUFF
C8101 0.01UF 10% 16V X7R-CERM 0402
BKLT_EN_DIV
R8133 147K 1% 1/16W MF-LF 402 NOSTUFF
BKLT_EN_L
R8122 0 5% 1/16W MF-LF 402
TCON_BLC_EN
Q8101 SSM3K15AMFVAP SOD CRITICAL
BKLT_SHUTDOWN
GND

SYNC_MASTER=MLB_CTO SYNC_DATE=05/14/2014
PAGE TITLE
DISPLAY: LCD Backlight Driver (LP8565)

Apple Inc.

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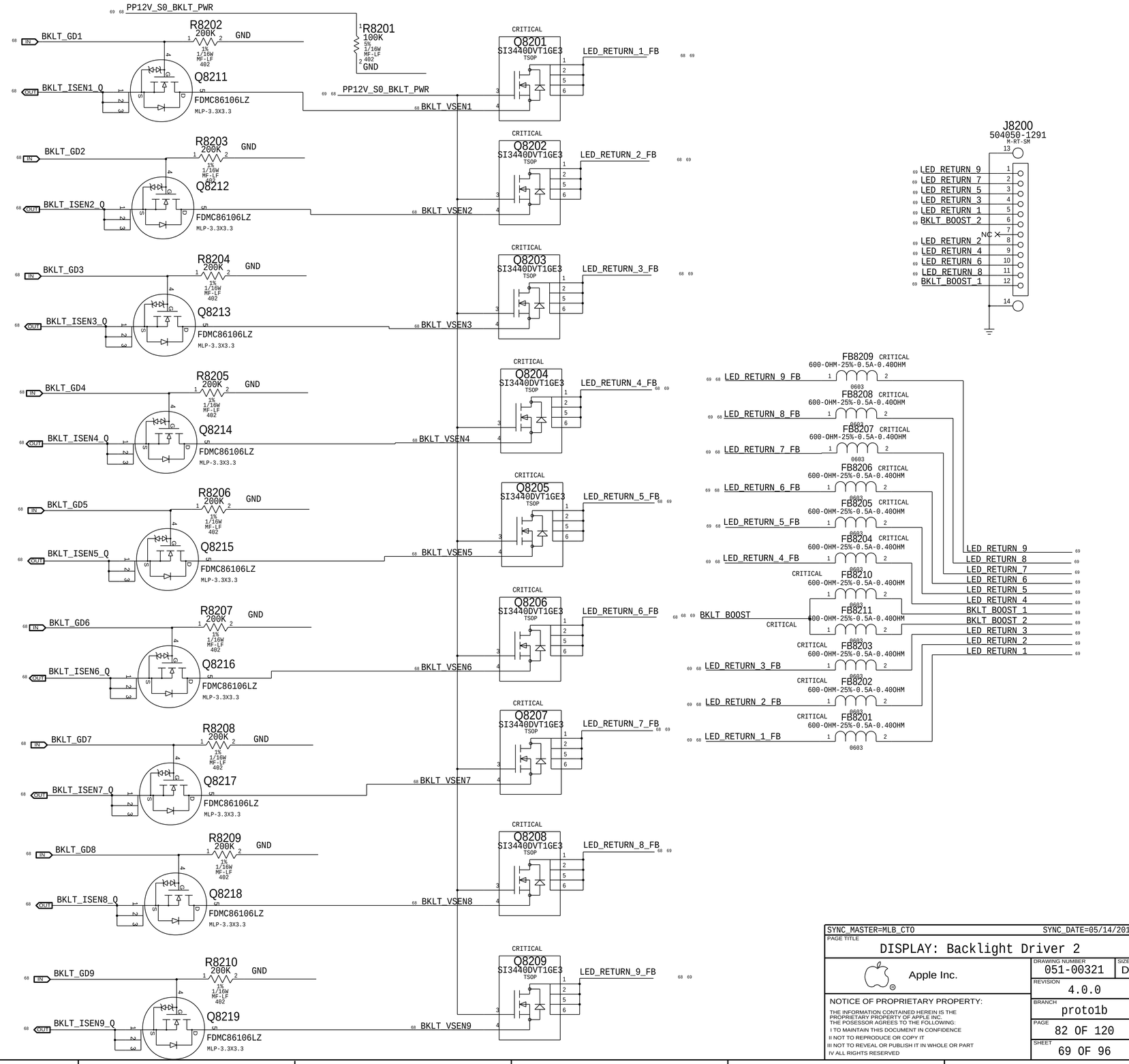
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



SYNC_MASTER=MLB_CTO SYNC_DATE=05/14/2014

PAGE TITLE

DISPLAY: Backlight Driver 2

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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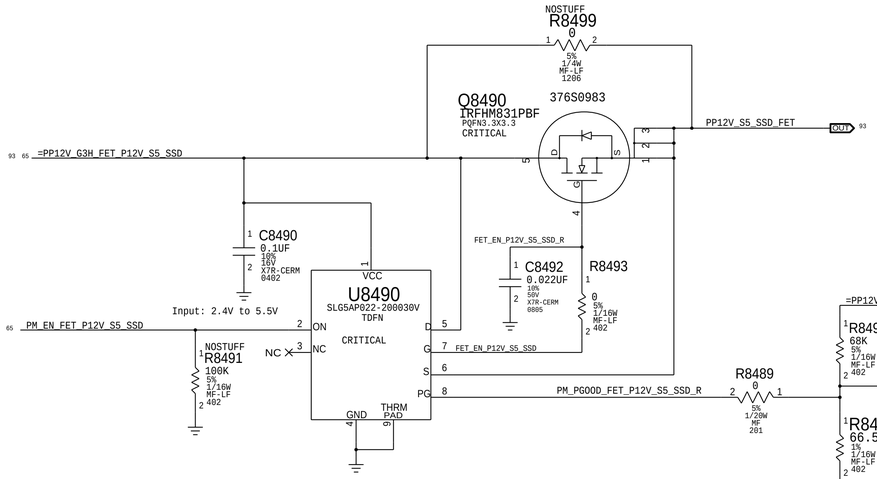
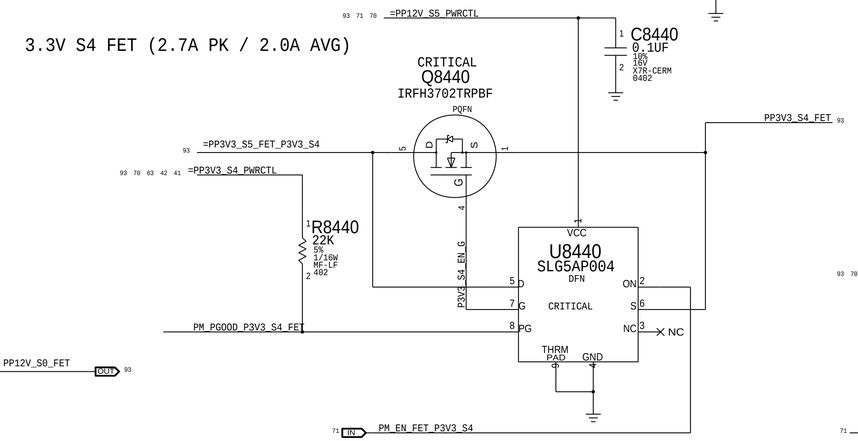
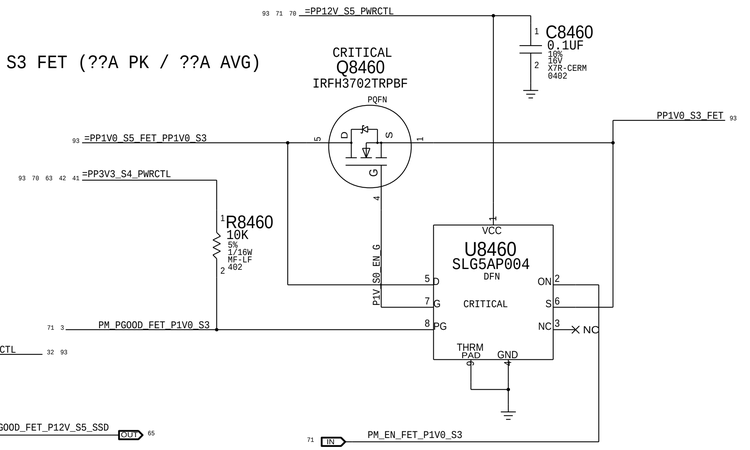
12V G3H ->S5 12V SSD FET



3.3V S4 FET (2.7A PK / 2.0A AVG)

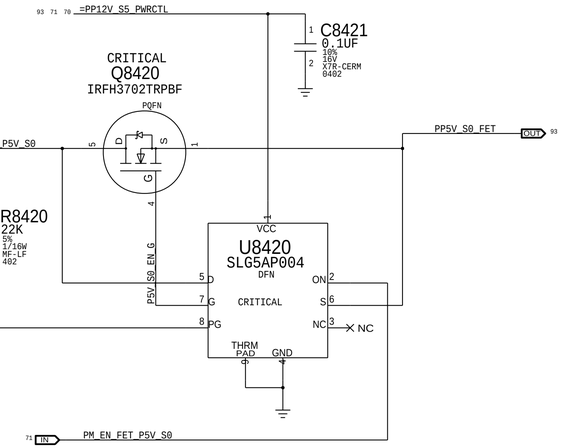


1.0V S3 FET (??A PK / ??A AVG)

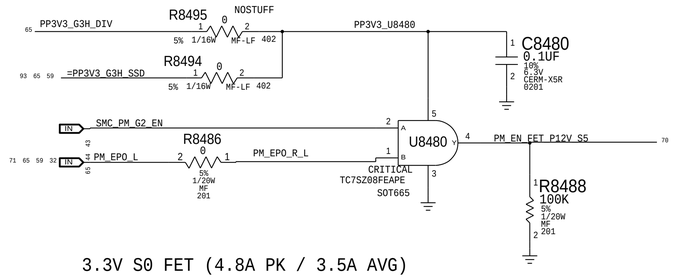


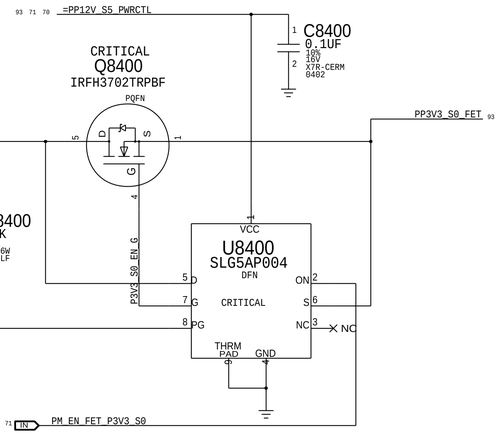
5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)



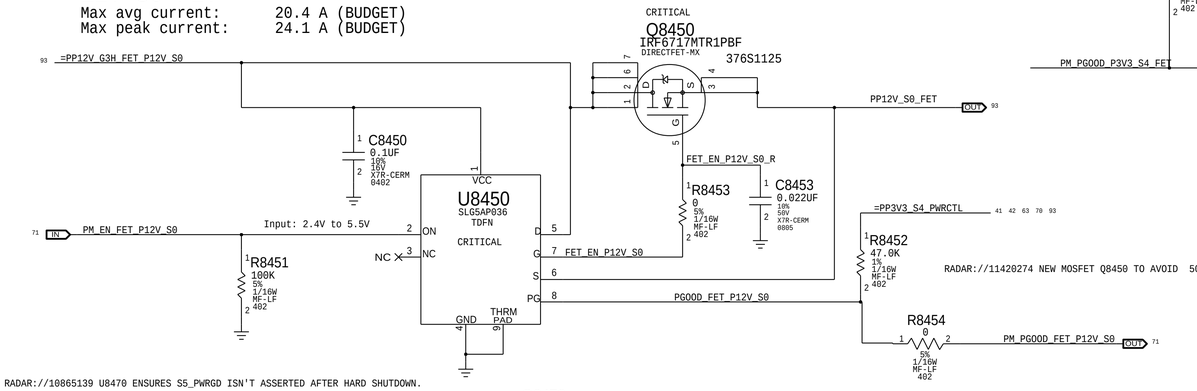
3.3V S0 FET (4.8A PK / 3.5A AVG)





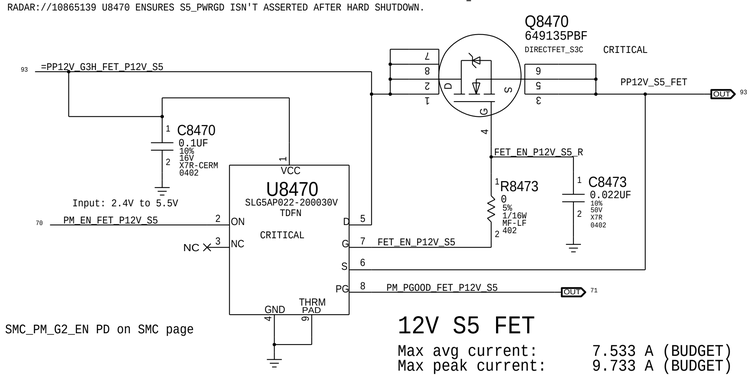
12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



RADAR://11420274 NEW MOSFET Q8450 TO AVOID 50A 100US PULSE ON 12V S0.

RADAR://10865139 U8470 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.



SMC_PM_G2_EN PD on SMC page

12V S5 FET

Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)

SYNC_MASTER=J17_MAX	SYNC_DATE=02/11/2013
PAGE TITLE: PLATFORM POWER: FET-Controlled S0 and S4	
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
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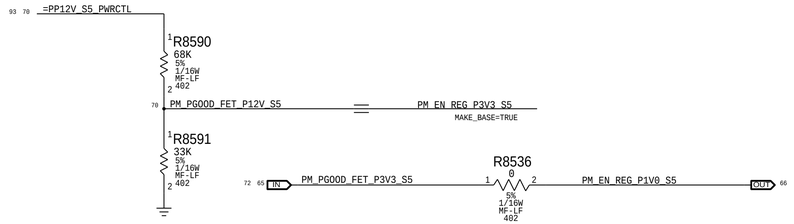
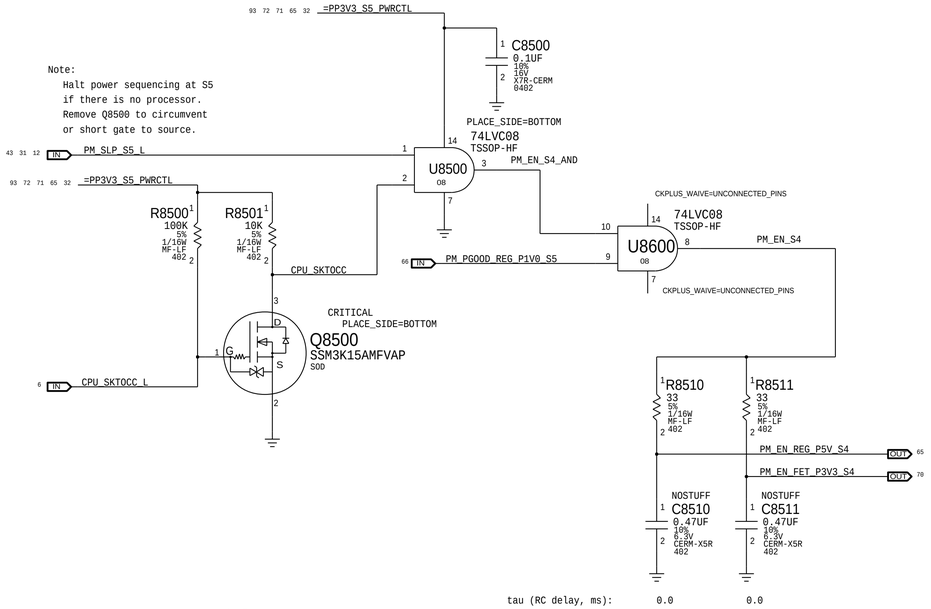
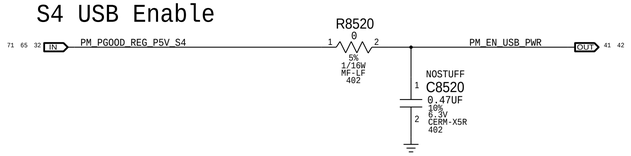
S5 Enable



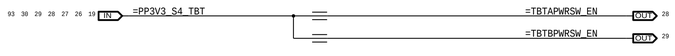
S4 Enables



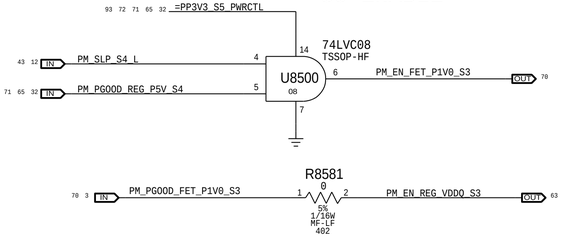
S4 USB Enable



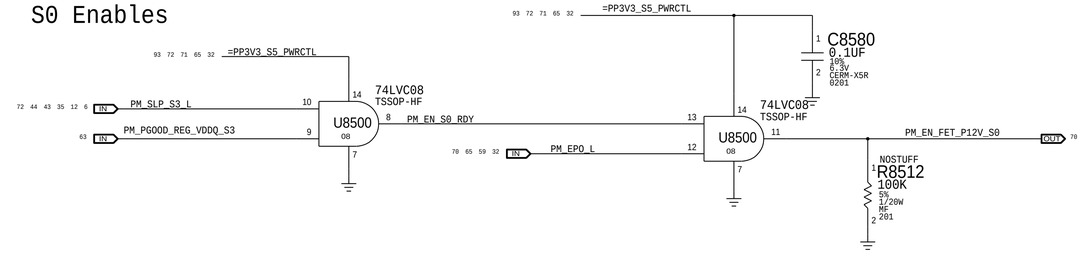
S4 TBT S4 Port Enable

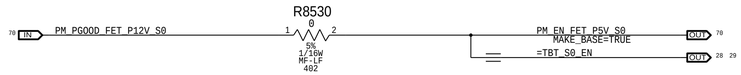


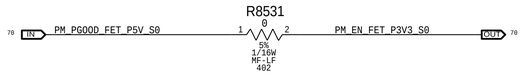
S3 ENABLE



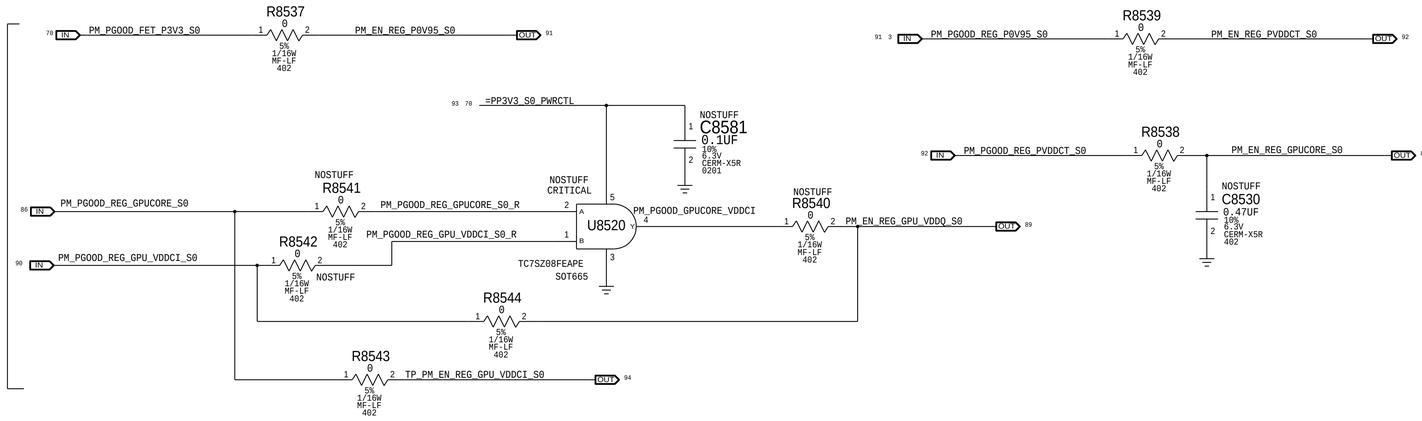
S0 Enables



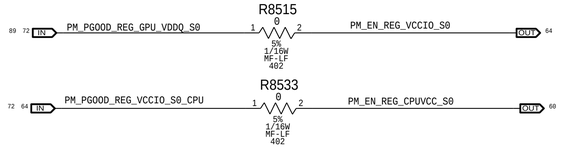




S0 GPU SEQUENCING



S0 CPU Sequencing



Power Sequencing requirements

System:

1. 12V_ACDC -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3

Intel CPU:

2. 1V0_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU Rails -> VCCIO_S0-> VCC_CPU_S0 (VCCGT & VCCSA)

AMD GPU:

3. 3V3_S0 -> 0V95 -> 1V8 (VDD_CT) -> GPUCORE (VDDC) -> VDDCI -> FBVDDQ

SYNC_MASTER=J78_KENNY SYNC_DATE=12/18/2013

PAGE TITLE

PLATFORM POWER: Regulator Enables

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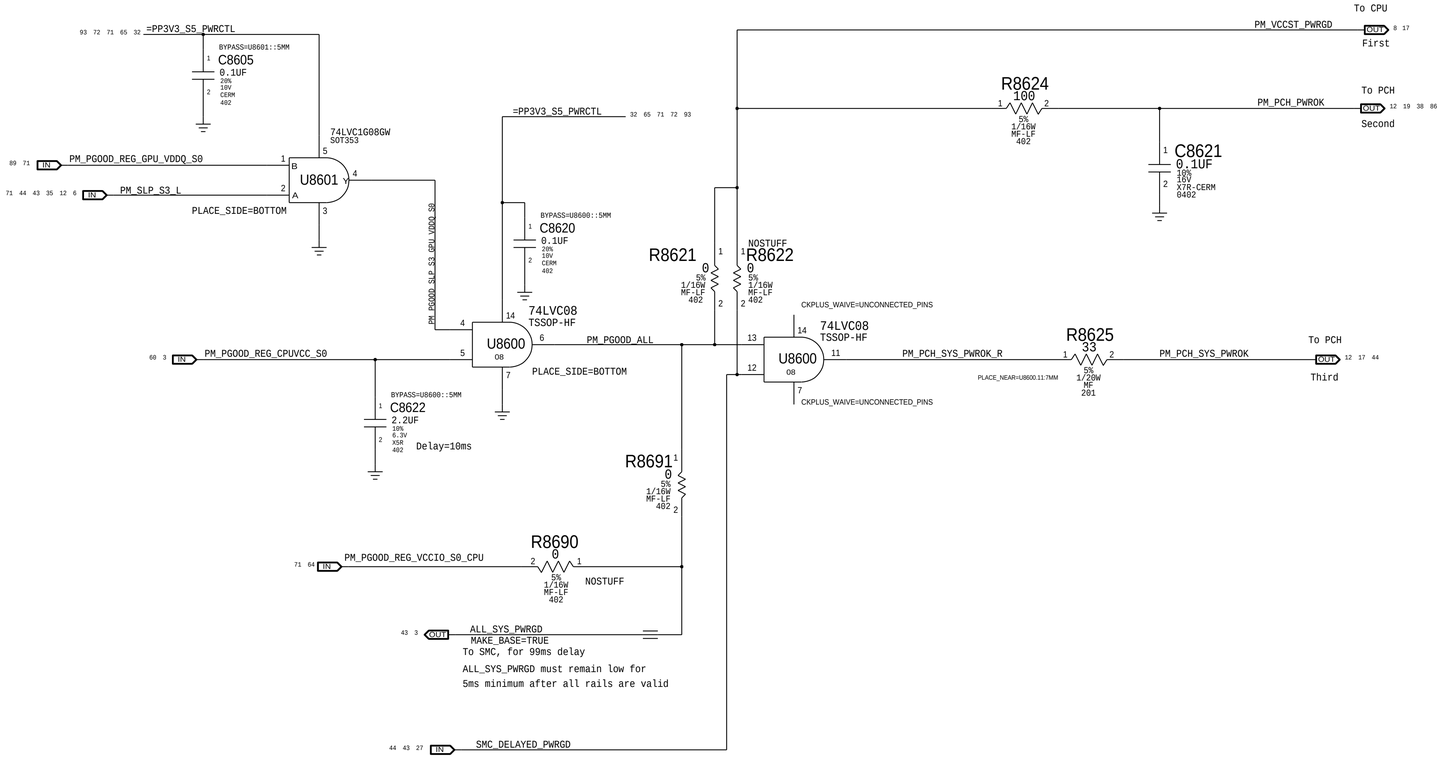
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

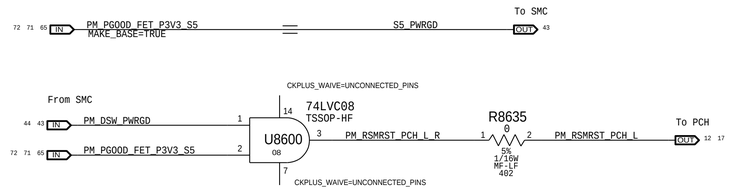
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
THE IMAC J78 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=J78_KENNY SYNC_DATE=10/09/2013

PAGE TITLE
PLATFORM POWER: PM Power Good

Apple Inc.

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POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 102

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NOTE:
TONGA DOES NOT GENERATE PCIE CLKREQ.

AMETHYST_BGA1737_HCBGA_AMETHYST_XT

U8700
AMETHYST_XT
HCBGA
SYM 2 OF 15
PCIEXPRESS
OMIT_TABLE

73	PEG_R2D_P<0>	AR50	PCIE_RX0P	PCIE_TX0P	AN47	PEG_D2R_C_P<0>	73
73	PEG_R2D_N<0>	AP49	PCIE_RX0N	PCIE_TX0N	AN46	PEG_D2R_C_N<0>	73
73	PEG_R2D_P<1>	AP51	PCIE_RX1P	PCIE_TX1P	AM44	PEG_D2R_C_P<1>	73
73	PEG_R2D_N<1>	AN52	PCIE_RX1N	PCIE_TX1N	AM43	PEG_D2R_C_N<1>	73
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73	PEG_R2D_N<2>	AM49	PCIE_RX2N	PCIE_TX2N	AM46	PEG_D2R_C_N<2>	73
73	PEG_R2D_P<3>	AM51	PCIE_RX3P	PCIE_TX3P	AL44	PEG_D2R_C_P<3>	73
73	PEG_R2D_N<3>	AL52	PCIE_RX3N	PCIE_TX3N	AL43	PEG_D2R_C_N<3>	73
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73	PEG_R2D_P<8>	AG50	PCIE_RX8P	PCIE_TX8P	AH47	PEG_D2R_C_P<8>	73
73	PEG_R2D_N<8>	AF49	PCIE_RX8N	PCIE_TX8N	AH46	PEG_D2R_C_N<8>	73
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73	PEG_R2D_P<15>	Y51	PCIE_RX15P	PCIE_TX15P	AB47	PEG_D2R_C_P<15>	73
73	PEG_R2D_N<15>	W52	PCIE_RX15N	PCIE_TX15N	AB46	PEG_D2R_C_N<15>	73

11	IN	PEG_CLK100M_P	AR47	PCIE_REFCLKP	PCIE_CALR_RX	AR43	GPU_PCIE_CALR_RX	73
11	IN	PEG_CLK100M_N	AR46	PCIE_REFCLKN	PCIE_CALR_TX	AR44	GPU_PCIE_CALR_TX	73

93 =PP1V8_S0_GPU_PEX_IO

C8700 10UF 20% 4V X6S 0402
C8732 1UF 10% 6.3V X7R 0402
C8731 1UF 10% 6.3V X7R 0402
C8730 1UF 10% 6.3V X7R 0402

AT45	PCIE_PVDD_1	
AT46	PCIE_PVDD_2	
AG40	BIF_VDDC	
AH41	BIF_VDDC	
AK40	BIF_VDDC	
AL41	BIF_VDDC	
AB43	PCIE_VDDC	
AB44	PCIE_VDDC	
AB45	PCIE_VDDC	
AD42	PCIE_VDDC	
AF42	PCIE_VDDC	
AG42	PCIE_VDDC	
Y53	VSS	
Y48	VSS	
W6	VSS	

PERST*	AU48	GPU_RESET_L	IN 83 94
CLKREQ*	AA43	NC	
WAKE*	BN48	GPU_WAKE_R_L	

PCIE_VDDC	AH42
PCIE_VDDC	AK42
PCIE_VDDC	AL42
PCIE_VDDC	AM42
PCIE_VDDC	AN42
PCIE_VDDC	AR42

R8786 4.7K 5% 1/20W MF 201

93 =PP0V95_S0_GPU_PCIEVDDC

C8729 1UF 10% 6.3V X7R 0402
C8728 1UF 10% 6.3V X7R 0402
C8718 1UF 10% 6.3V X7R 0402
C8717 1UF 10% 6.3V X7R 0402
C8716 1UF 10% 6.3V X7R 0402
C8709 1UF 10% 6.3V X7R 0402
C8710 1UF 10% 6.3V X7R 0402
C8711 1UF 10% 6.3V X7R 0402
C8712 1UF 10% 6.3V X7R 0402
C8713 1UF 10% 6.3V X7R 0402
C8714 1UF 10% 6.3V X7R 0402
C8715 1UF 10% 6.3V X7R 0402
C8705 10UF 20% 4V X6S 0402
C8704 10UF 20% 4V X6S 0402

93 91 83 82 =PP0V95_S0_GPU_VDDC

R8701 1K 1% 1/20W MF 201
R8702 1.69K 1% 1/20W MF 201

73 GPU_PCIE_CALR_RX
73 GPU_PCIE_CALR_TX

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:57 2015
SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015
PAGE TITLE
GRAPHICS: AMETHYST PCIE

Apple Inc.

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GPU VDDC/VDDCI DECOUPLING

PLACE ALL CAPS UNDER GPU

PLACE ALL CAPS UNDER GPU

=PPGPUCORE_S0

=PPVDDCI_S0_GPU

AMETHYST_BGA1737_HCBGA_AMETHYST_XT

OMIT_TABLE

U8700
AMETHYST_XT
HCBGA

SYM 9 OF 15

POWER1

C8991 C8992 C8993 C8994 C8995 — 1UF 20% 4V CERM-X6S 0201

C8996 C8997 C8998 C8999 C89A0 — 1UF 20% 4V CERM-X6S 0201

C89D3 C89D4 C89D5 C89D6 C89D7 — 15UF 20% 2V X6S 0402

C89D8 C89D9 C89E0 C89E1 C89E2 — 15UF 20% 2V X6S 0402

C89E3 C89E4 — 15UF 20% 2V X6S 0402

C8961 C8962 C8963 C8964 C8965 C8966 C8967 C8968 C8969 C8970 — 1UF 20% 4V CERM-X6S 0201

C8971 C8972 C8973 C8974 C8975 C8976 C8977 C8978 C8979 C8980 — 1UF 20% 4V CERM-X6S 0201

C8981 C8982 C8983 C8984 C8985 C8986 C8987 C8988 C8989 C8990 — 1UF 20% 4V CERM-X6S 0201

C89B3 C89B4 C89B5 C89B6 C89B7 C89B8 C89B9 C89C0 C89C1 C89C2 — 15UF 20% 2V X6S 0402

C89C3 C89C4 C89C5 C89C6 C89C7 C89C8 C89C9 C89D0 C89D1 C89D2 — 15UF 20% 2V X6S 0402

AL38	VDDC	VDDCI	AA16
AM37	VDDC	VDDCI	AA18
AM40	VDDC	VDDCI	AA36
AN36	VDDC	VDDCI	AA38
AN38	VDDC	VDDCI	AA41
AN41	VDDC	VDDCI	AB14
AR35	VDDC	VDDCI	AB17
AR37	VDDC	VDDCI	AB37
AR40	VDDC	VDDCI	AB40
AT33	VDDC	VDDCI	AB42
AT36	VDDC	VDDCI	AC16
AT38	VDDC	VDDCI	AC38
AT41	VDDC	VDDCI	AC41
AU32	VDDC	VDDCI	AD14
AU35	VDDC	VDDCI	AF13
AU37	VDDC	VDDCI	AG12
AU40	VDDC	VDDCI	AG14
AV33	VDDC	VDDCI	AH13
AV36	VDDC	VDDCI	AK14
AV38	VDDC	VDDCI	AL16
AV41	VDDC	VDDCI	AM14
AY32	VDDC	VDDCI	AM17
AY35	VDDC	VDDCI	AN16
AY37	VDDC	VDDCI	AR17
AY40	VDDC	VDDCI	AT16
BA33	VDDC	VDDCI	AT18
BA36	VDDC	VDDCI	AU17
BA38	VDDC	VDDCI	AU19
		VDDCI	AV18
		VDDCI	AY19
		VDDCI	M27
		VDDCI	N26
		VDDCI	N28
		VDDCI	P22
		VDDCI	P24
		VDDCI	P27
		VDDCI	P30
		VDDCI	P32
		VDDCI	P35
		VDDCI	T21
		VDDCI	T23
		VDDCI	T31
		VDDCI	T33
		VDDCI	T36
		VDDCI	U19
		VDDCI	U22
		VDDCI	U32
		VDDCI	U35
		VDDCI	U37
		VDDCI	V18
V21	VDDCI		
V33	VDDCI		
V36	VDDCI		
V38	VDDCI		
W17	VDDCI		
W19	VDDCI		
W35	VDDCI		
W37	VDDCI		
W40	VDDCI		

NC BB22 FB_VDDC

NC BB23 FB_VSSC

FB_VDDC AF41

FB_VSSC AG41

NOSTUFF R8803 0 5% 1/20W MF 201

NOSTUFF R8804 0 5% 1/20W MF 201

SNS_GPU_VDDCI_P — OUT 90

SNS_GPU_VDDCI_N — OUT 90

DRAWING — LAST_MODIFIED=Thu Feb 26 18:42:57 2015

SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013

PAGE TITLE

GRAPHICS: VDDC/VDDCI DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

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GPU MVDD/VDDGFX DECOUPLING

LAST_MODIFIED=Thu Feb 26 18:42:58 2015

DRAWING

SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013

PAGE TITLE

GRAPHICS: MVDD/VDDGFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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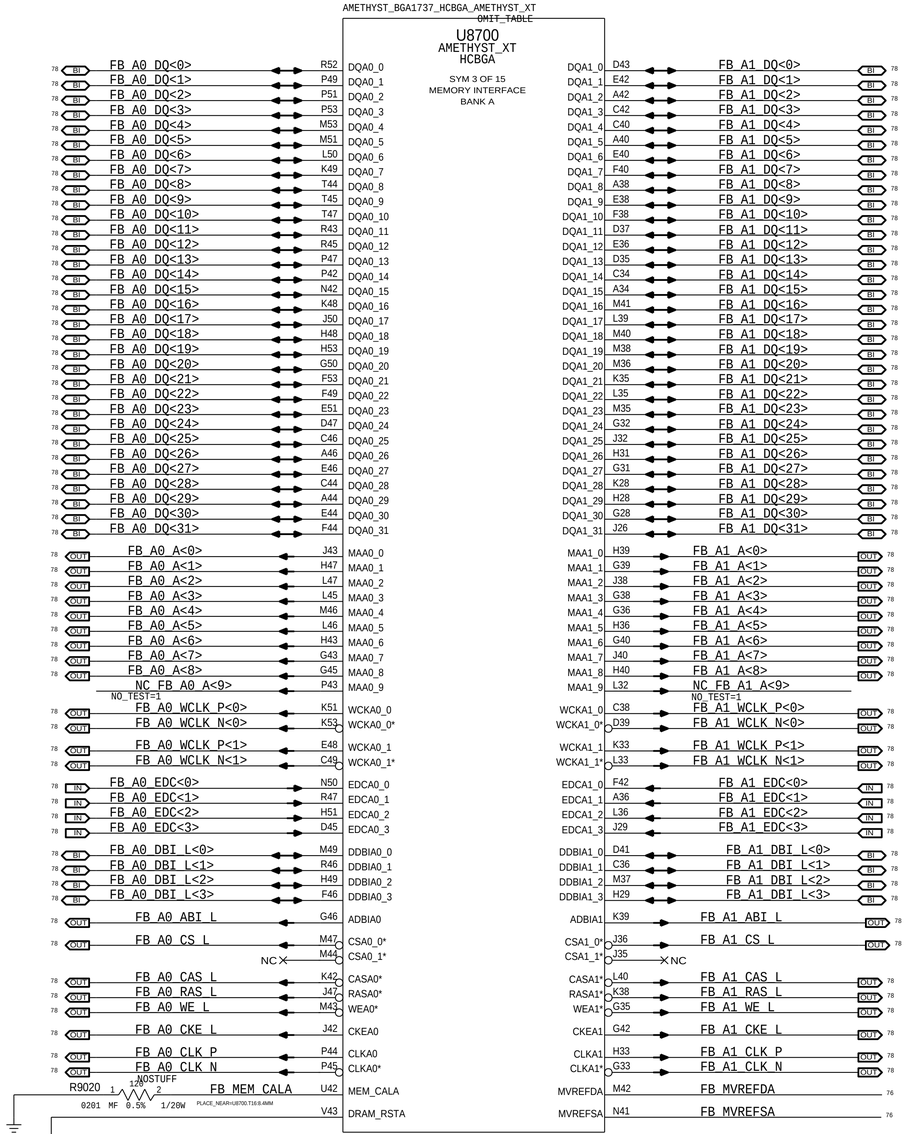

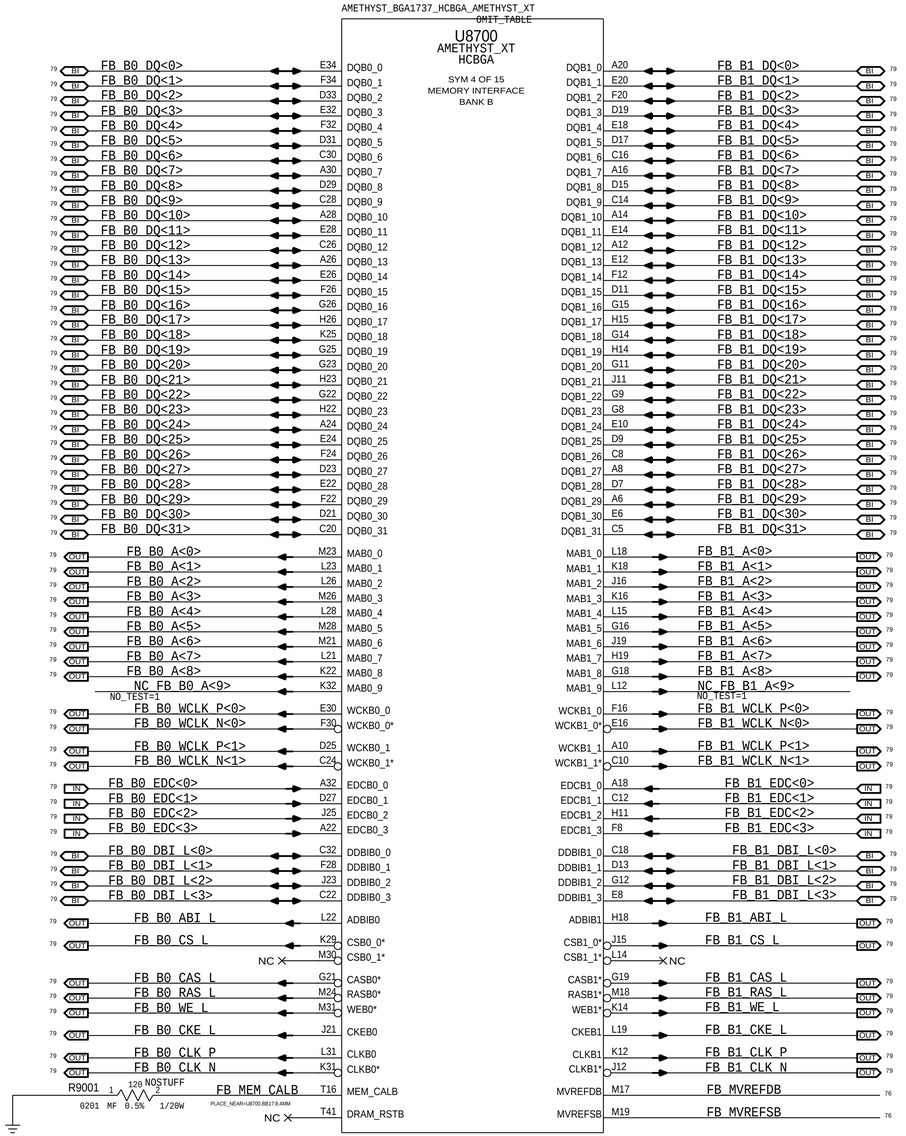

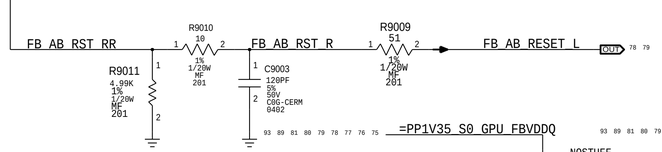

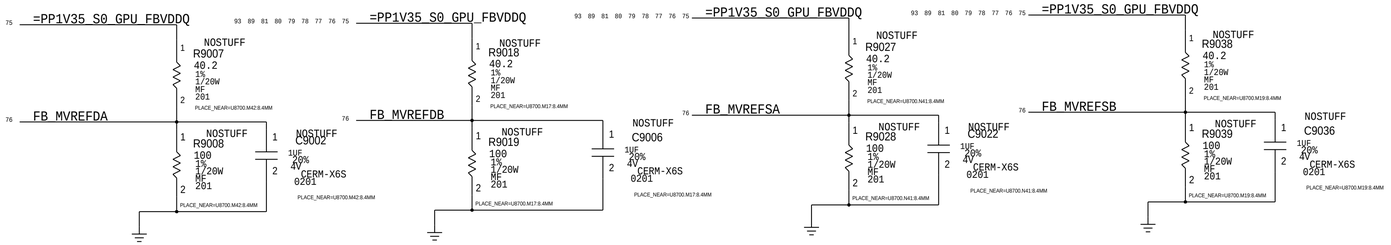

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SYNC_MASTER=J78_PETER
SYNC_DATE=12/04/2013
PAGE TITLE
GRAPHICS: FRAME BUFFER A/B
Apple Inc.
DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
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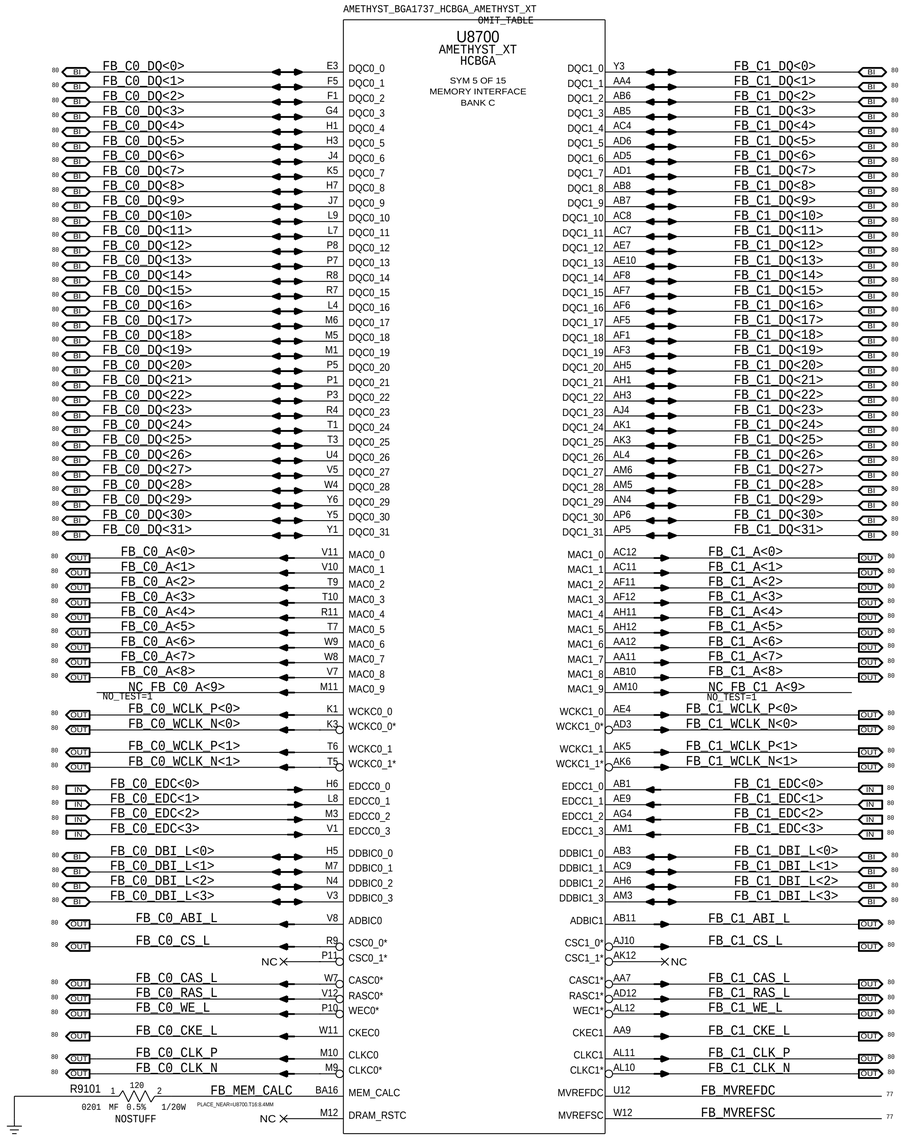

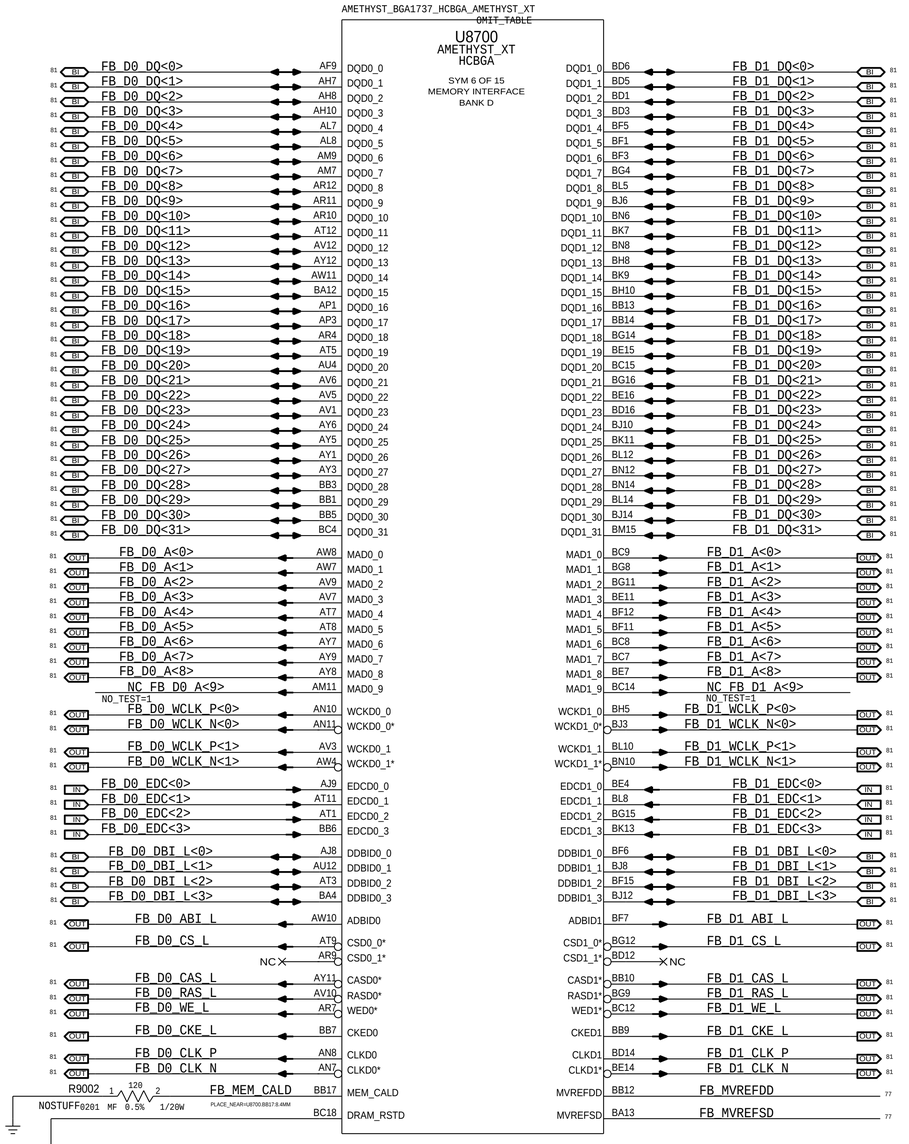

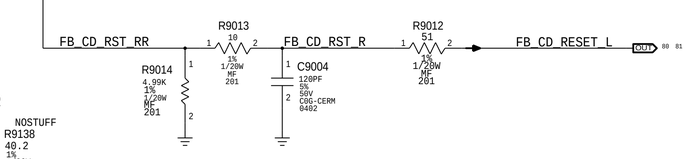

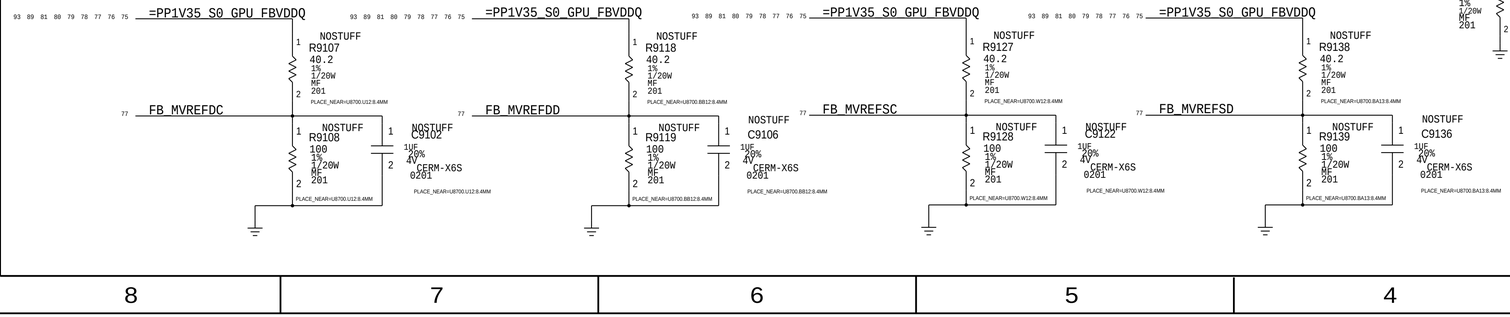

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SYNC_MASTER=J78_PETER SYNC_DATE=12/04/2013

PAGE TITLE

GRAPHICS: FRAME BUFFER C/D

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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Page Notes

Power aliases required by this page:

- +PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

NORMAL

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

SYNC_MASTER=J78_MLB	SYNC_DATE=08/02/2014
PAGE TITLE	GRAPHICS: GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

SYNC_MASTER=J78_MLB	SYNC_DATE=08/02/2014
PAGE TITLE	GRAPHICS: GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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	SHEET 79 OF 96

Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

U9400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

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R9402 60.4 1% 1/20W MF 201

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FB_C0_A<5>	K10	BA1/A5
FB_C0_A<4>	K11	BA2/A4
FB_C0_A<3>	H10	BA3/A3
FB_C0_A<7>	K4	A8/A7
FB_C0_A<1>	H5	A9/A1
FB_C0_A<0>	H4	A10/A0
FB_C0_A<6>	K5	A11/A6
FB_C0_CKE_L	J3	CKE*
FB_C0_CLK_P	J12	CK
FB_C0_CLK_N	J11	CK*
FB_C0_CS_L	G12	CS*
FB_C0_WE_L	L12	WE*
FB_C0_CAS_L	L3	CAS*
FB_C0_RAS_L	G3	RAS*
FB_C0_ZQ	J13	ZQ
FB_C0_MF	J1	MF (MF=0)
FB_C0_SEN	J10	SEN
FB_C0_RESET_L	J2	RESET*
FB_C0_ABI_L	J4	ABI*
FB_C0_EDC<3>	C2	EDC0
FB_C0_EDC<2>	C13	EDC1
FB_C0_EDC<0>	R13	EDC2
FB_C0_EDC<1>	R2	EDC3
FB_C0_WCLK_P<1>	D4	WCK01
FB_C0_WCLK_N<1>	D5	WCK01*
FB_C0_WCLK_P<0>	P4	WCK23
FB_C0_WCLK_N<0>	P5	WCK23*

R9400 120 1% 1/20W MF 201
R9404 1K 1% 1/20W MF 201
R9403 1K 1% 1/20W MF 201

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FB_C0_DBI_L<2>	D13	DBI1*
FB_C0_DBI_L<0>	P13	DBI2*
FB_C0_DBI_L<1>	P2	DBI3*
FB_C0_DQ<28>	A4	DQ0
FB_C0_DQ<30>	A2	DQ1
FB_C0_DQ<29>	B4	DQ2
FB_C0_DQ<31>	B2	DQ3
FB_C0_DQ<26>	E4	DQ4
FB_C0_DQ<24>	E2	DQ5
FB_C0_DQ<27>	F4	DQ6
FB_C0_DQ<25>	F2	DQ7
FB_C0_DQ<22>	A11	DQ8
FB_C0_DQ<17>	A13	DQ9
FB_C0_DQ<23>	B11	DQ10
FB_C0_DQ<16>	B13	DQ11
FB_C0_DQ<20>	E11	DQ12
FB_C0_DQ<19>	E13	DQ13
FB_C0_DQ<21>	F11	DQ14
FB_C0_DQ<18>	F13	DQ15
FB_C0_DQ<5>	U11	DQ16
FB_C0_DQ<0>	U13	DQ17
FB_C0_DQ<4>	T11	DQ18
FB_C0_DQ<1>	T13	DQ19
FB_C0_DQ<6>	N11	DQ20
FB_C0_DQ<3>	N13	DQ21
FB_C0_DQ<7>	M11	DQ22
FB_C0_DQ<2>	M13	DQ23
FB_C0_DQ<8>	U4	DQ24
FB_C0_DQ<10>	U2	DQ25
FB_C0_DQ<9>	T4	DQ26
FB_C0_DQ<11>	T2	DQ27
FB_C0_DQ<12>	N4	DQ28
FB_C0_DQ<13>	N2	DQ29
FB_C0_DQ<14>	M4	DQ30
FB_C0_DQ<15>	M2	DQ31
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FB_C0_A<8>	J5	A12/RFU/NC
	U5	NC

MIRRORED

U9450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

R9451 60.4 1% 1/20W MF 201
R9452 60.4 1% 1/20W MF 201

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FB_C1_A<4>	H11	BA2/A4
FB_C1_A<3>	K10	BA3/A3
FB_C1_A<7>	H4	A8/A7
FB_C1_A<1>	K5	A9/A1
FB_C1_A<0>	K4	A10/A0
FB_C1_A<6>	H5	A11/A6
FB_C1_CKE_L	J3	CKE*
FB_C1_CLK_P	J12	CK
FB_C1_CLK_N	J11	CK*
FB_C1_CS_L	L12	CS*
FB_C1_WE_L	G12	WE*
FB_C1_CAS_L	G3	CAS*
FB_C1_RAS_L	L3	RAS*
FB_C1_ZQ	J13	ZQ
FB_C1_MF	J1	MF (MF=1)
FB_C1_SEN	J10	SEN
FB_C0_RESET_L	J2	RESET*
FB_C1_ABI_L	J4	ABI*
FB_C1_EDC<2>	R2	EDC0
FB_C1_EDC<3>	R13	EDC1
FB_C1_EDC<1>	C13	EDC2
FB_C1_EDC<0>	C2	EDC3
FB_C1_WCLK_P<1>	P4	WCK01
FB_C1_WCLK_N<1>	P5	WCK01*
FB_C1_WCLK_P<0>	D4	WCK23
FB_C1_WCLK_N<0>	D5	WCK23*

R9450 120 1% 1/20W MF 201
R9454 1K 1% 1/20W MF 201
R9453 1K 1% 1/20W MF 201

FB_C1_DBI_L<3>	P13	DBI0*
FB_C1_DBI_L<1>	D13	DBI1*
FB_C1_DBI_L<2>	P2	DBI2*
FB_C1_DBI_L<0>	D2	DBI3*
FB_C1_DQ<21>	U4	DQ0
FB_C1_DQ<16>	U2	DQ1
FB_C1_DQ<22>	T4	DQ2
FB_C1_DQ<19>	T2	DQ3
FB_C1_DQ<23>	N4	DQ4
FB_C1_DQ<18>	N2	DQ5
FB_C1_DQ<20>	M4	DQ6
FB_C1_DQ<17>	M2	DQ7
FB_C1_DQ<29>	U11	DQ8
FB_C1_DQ<30>	U13	DQ9
FB_C1_DQ<28>	T11	DQ10
FB_C1_DQ<31>	T13	DQ11
FB_C1_DQ<25>	N11	DQ12
FB_C1_DQ<27>	N13	DQ13
FB_C1_DQ<26>	M11	DQ14
FB_C1_DQ<24>	M13	DQ15
FB_C1_DQ<9>	A11	DQ16
FB_C1_DQ<11>	A13	DQ17
FB_C1_DQ<8>	B11	DQ18
FB_C1_DQ<10>	B13	DQ19
FB_C1_DQ<14>	E11	DQ20
FB_C1_DQ<12>	E13	DQ21
FB_C1_DQ<15>	F11	DQ22
FB_C1_DQ<13>	F13	DQ23
FB_C1_DQ<6>	A4	DQ24
FB_C1_DQ<5>	A2	DQ25
FB_C1_DQ<0>	B4	DQ26
FB_C1_DQ<3>	B2	DQ27
FB_C1_DQ<4>	E4	DQ28
FB_C1_DQ<2>	E2	DQ29
FB_C1_DQ<7>	F4	DQ30
FB_C1_DQ<1>	F2	DQ31
	A5	NC
FB_C1_A<8>	J5	A12/RFU/NC
	U5	NC

VDD

U9400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

C9400 10UF 20% 6.3V CERM-X6S 0402
C9401 10UF 20% 6.3V CERM-X6S 0402
C9403 4.7UF 20% 6.3V X6S 0402
C9404 4.7UF 20% 6.3V X6S 0402
C9406 1.0UF 20% 4V X6S 0201
C9407 1.0UF 20% 4V X6S 0201
C9408 1.0UF 20% 4V X6S 0201
C9409 1.0UF 20% 4V X6S 0201
C9410 1.0UF 20% 4V X6S 0201
C9411 1.0UF 20% 4V X6S 0201
C9412 1.0UF 20% 4V X6S 0201
C9413 1.0UF 20% 4V X6S 0201
C9414 1.0UF 20% 4V X6S 0201
C9415 1.0UF 20% 4V X6S 0201
C9416 0.1UF 10% 4V CERM-X6S 0201
C9417 0.1UF 10% 4V CERM-X6S 0201
C9418 0.1UF 10% 4V CERM-X6S 0201
C9419 0.1UF 10% 4V CERM-X6S 0201
C9420 0.1UF 10% 4V CERM-X6S 0201
C9421 0.1UF 10% 4V CERM-X6S 0201
C9422 0.1UF 10% 4V CERM-X6S 0201
C9423 0.1UF 10% 4V CERM-X6S 0201
C9424 0.1UF 10% 4V CERM-X6S 0201
C9425 0.1UF 10% 4V CERM-X6S 0201

	C5	VDD
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	L11	
	L14	
	P11	
	R5	
	R10	
	B1	VDDQ
	B3	
	B12	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	K12	
	L2	
	L13	
	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B5	VSS
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
	A1	VSSQ
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	T12	
	U1	
	U3	
	U12	
	U14	

FB_C0_VREFC	J14	VREFC
FB_C0_VREFD0	A10	
FB_C0_VREFD1	U10	VREFD

=PP1V35_S0_GPU_FBVDDQ

R9430 2.37K 1% 1/20W MF 201
C9431 1.0UF 20% 4V X6S 0201
R9431 5.49K 1% 1/20W MF 201
FB_C0_VREFC
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

=PP1V35_S0_GPU_FBVDDQ

R9432 2.37K 1% 1/20W MF 201 NOSTUFF
C9433 1.0UF 20% 4V X6S 0201 NOSTUFF
R9433 5.49K 1% 1/20W MF 201 NOSTUFF
FB_C0_VREFD0
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

=PP1V35_S0_GPU_FBVDDQ

R9434 2.37K 1% 1/20W MF 201 NOSTUFF
C9440 1.0UF 20% 4V X6S 0201 NOSTUFF
R9435 5.49K 1% 1/20W MF 201 NOSTUFF
FB_C0_VREFD1
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

VDDQ

U9450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

C9450 10UF 20% 6.3V CERM-X6S 0402
C9451 10UF 20% 6.3V CERM-X6S 0402
C9453 4.7UF 20% 6.3V X6S 0402
C9454 4.7UF 20% 6.3V X6S 0402
C9456 1.0UF 20% 4V X6S 0201
C9457 1.0UF 20% 4V X6S 0201
C9458 1.0UF 20% 4V X6S 0201
C9459 1.0UF 20% 4V X6S 0201
C9460 1.0UF 20% 4V X6S 0201
C9461 1.0UF 20% 4V X6S 0201
C9462 1.0UF 20% 4V X6S 0201
C9463 1.0UF 20% 4V X6S 0201
C9464 1.0UF 20% 4V X6S 0201
C9465 1.0UF 20% 4V X6S 0201
C9466 0.1UF 10% 4V CERM-X6S 0201
C9467 0.1UF 10% 4V CERM-X6S 0201
C9468 0.1UF 10% 4V CERM-X6S 0201
C9469 0.1UF 10% 4V CERM-X6S 0201
C9470 0.1UF 10% 4V CERM-X6S 0201
C9471 0.1UF 10% 4V CERM-X6S 0201
C9472 0.1UF 10% 4V CERM-X6S 0201
C9473 0.1UF 10% 4V CERM-X6S 0201
C9474 0.1UF 10% 4V CERM-X6S 0201
C9475 0.1UF 10% 4V CERM-X6S 0201

	C5	VDD
	L11	
	L14	
	P11	
	R5	
	R10	
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	B1	VDDQ
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	B3	
	K12	
	L2	
	L13	
	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	B12	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
	B5	VSS
	L5	
	L10	
	P10	
	T5	
	T10	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	A1	VSSQ
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	A3	
	K13	
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	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

FB_C1_VREFC	J14	VREFC
FB_C1_VREFD0	A10	
FB_C1_VREFD1	U10	VREFD

=PP1V35_S0_GPU_FBVDDQ

R9436 2.37K 1% 1/20W MF 201
C2681 1.0UF 20% 4V X6S 0201
R2637 5.49K 1% 1/20W MF 201
FB_C1_VREFC
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

=PP1V35_S0_GPU_FBVDDQ

R9439 2.37K 1% 1/20W MF 201 NOSTUFF
C9483 1.0UF 20% 4V X6S 0201 NOSTUFF
R9440 5.49K 1% 1/20W MF 201 NOSTUFF
FB_C1_VREFD0
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

R9438 2.37K 1% 1/20W MF 201 NOSTUFF
C9441 1.0UF 20% 4V X6S 0201 NOSTUFF
R9441 5.49K 1% 1/20W MF 201 NOSTUFF
FB_C1_VREFD1
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1000

SYNC_MASTER=J78_MLB	SYNC_DATE=08/02/2014
PAGE TITLE	GRAPHICS: GDDR5 FRAME BUFFER C
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 94 OF 120
	SHEET 80 OF 96

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Page Notes

Power aliases required by this page:

- +PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

U9500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

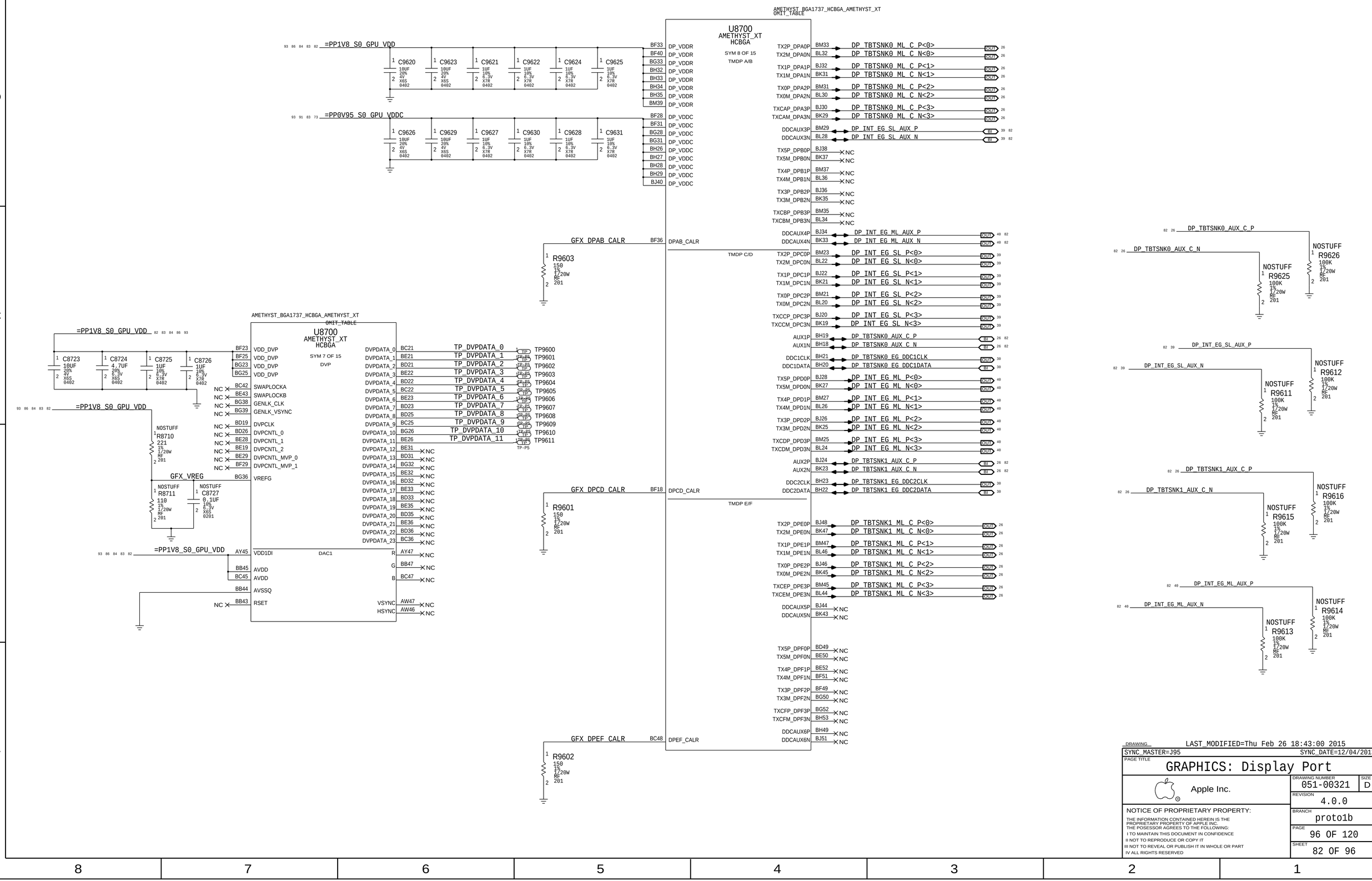
U9500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

U9550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

SYNC_MASTER=J78_MLB	SYNC_DATE=08/02/2014
PAGE TITLE	GRAPHICS: GDDR5 FRAME BUFFER D
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH proto1b
	PAGE 95 OF 120
	SHEET 81 OF 96



DRAWING	LAST_MODIFIED=Thu Feb 26 18:43:00 2015
SYNC_MASTER=J95	SYNC_DATE=12/04/2013
PAGE TITLE	GRAPHICS: Display Port
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
	BRANCH proto1b
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GPU overtemp masking

DRAWING
LAST_MODIFIED=Thu Feb 26 18:43:01 2015

SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE
GRAPHICS: GPU GPIOS/PLLS/STRAPS

Apple Inc.

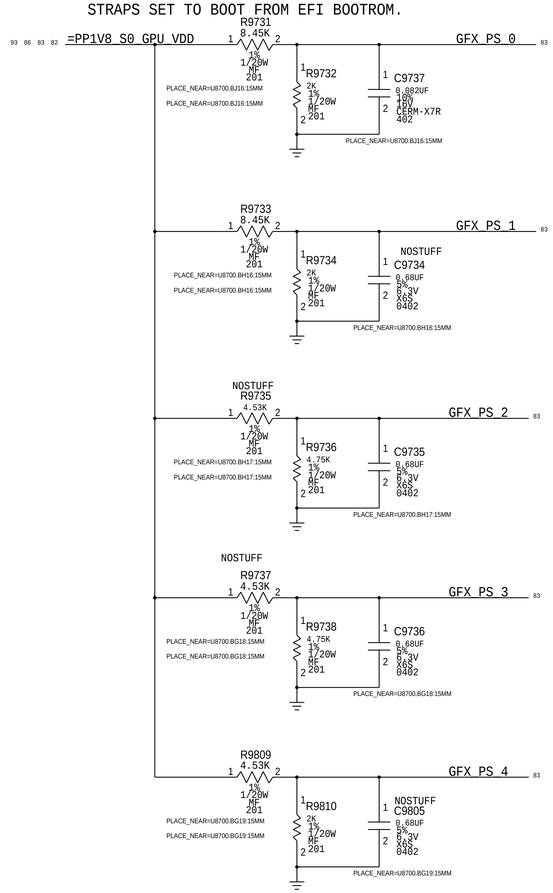
DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

CONFIG STRAPS - MLS

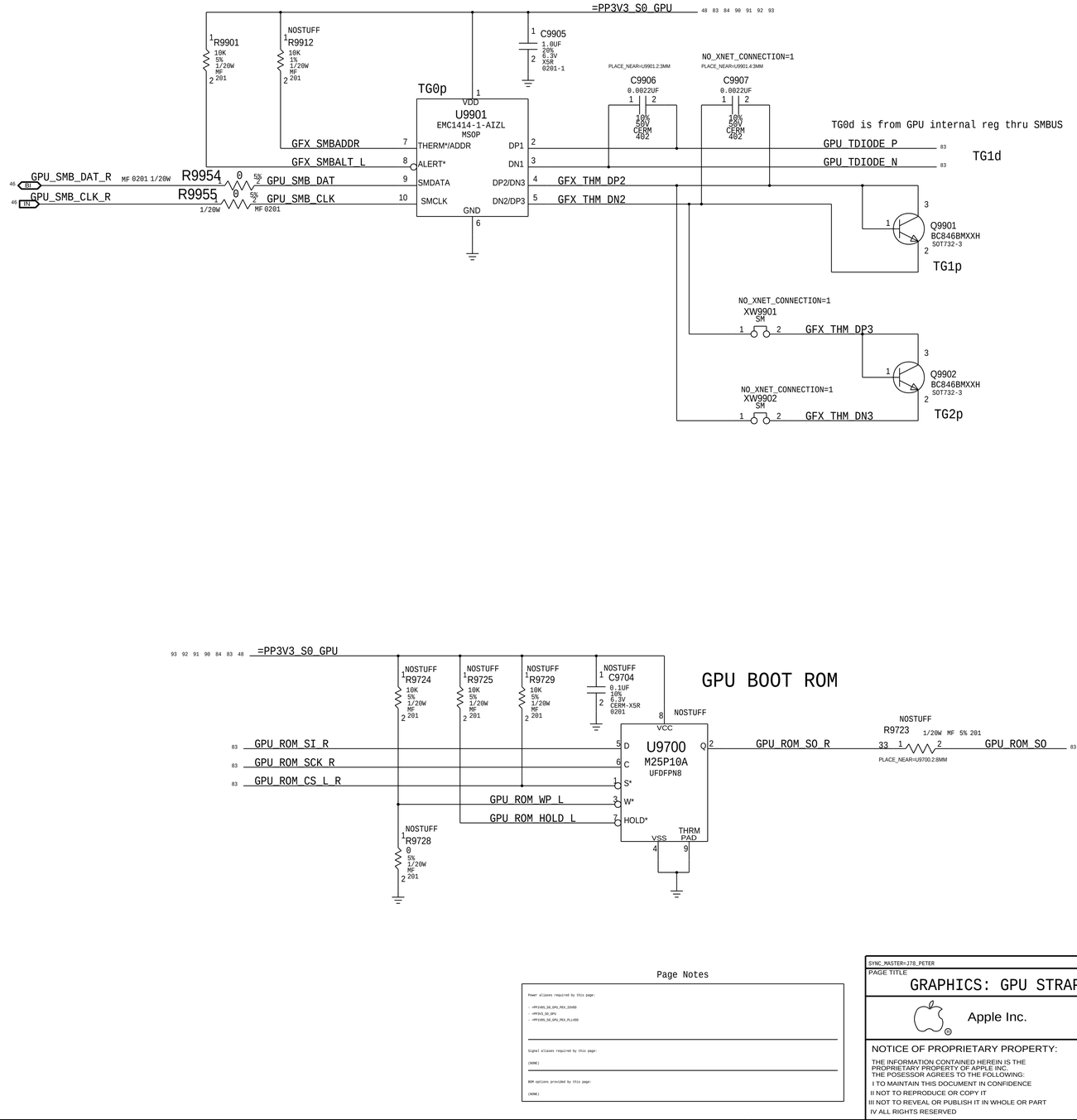
STRAPS SET TO BOOT FROM EFI BOOTROM.



SMC KEY

GFXA

GPU Prox Temp	TG0p
GPU VRAM Prox Temp	TG1p
GPU VR Prox Temp	TG2p
GPU TDiode Temp	TG1d



Page Notes

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- +PP1V05_S0_GPU_PEX_1DVDD
- +PP3V3_S0_GPU
- +PP1V05_S0_GPU_PEX_PLL45D

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

SYNC_MASTER=J78_PETER SYNC_DATE=11/13/2013

PAGE TITLE

GRAPHICS: GPU STRAPS,SENSORS,ROM

Apple Inc.

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REVISION 4.0.0

BRANCH proto1b

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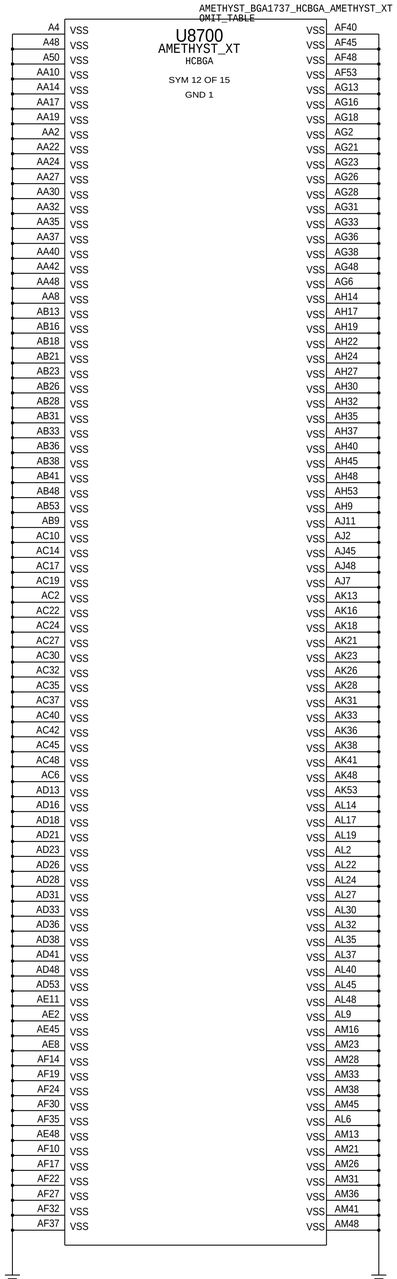

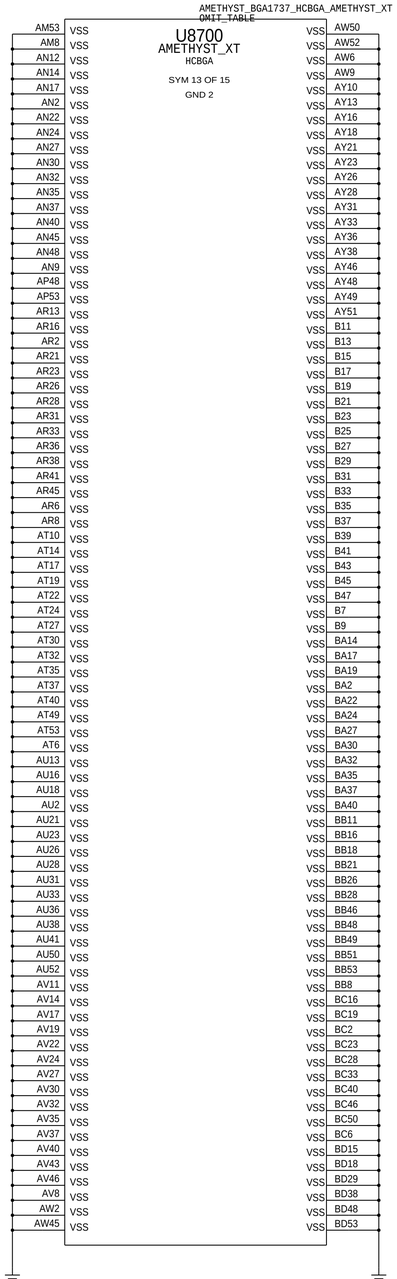

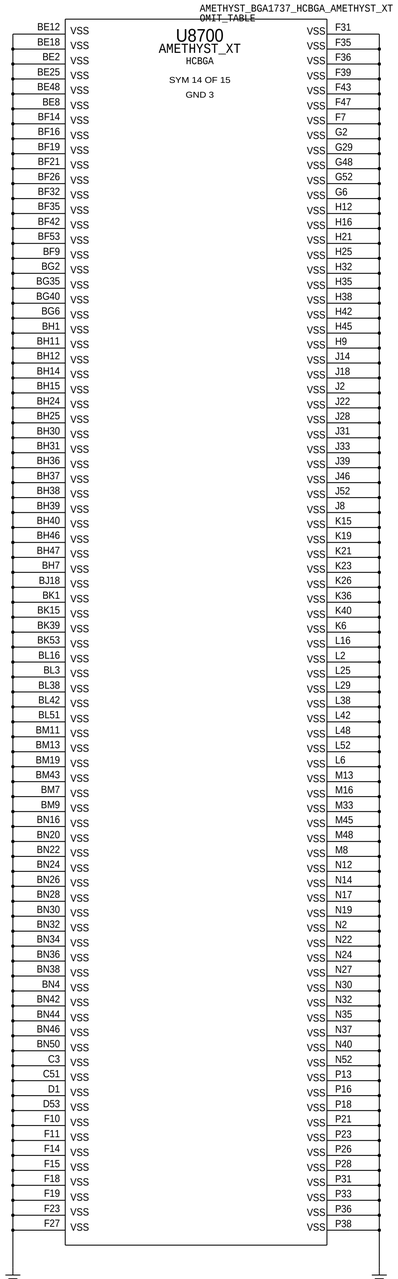

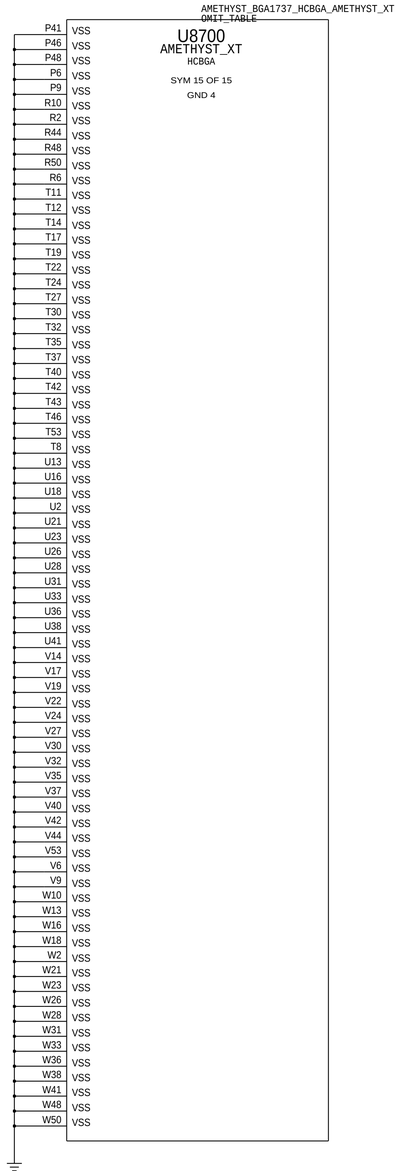

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LAST_MODIFIED=Thu Feb 26 18:43:01 2015

SYNC_MASTER=J78_PETER

SYNC_DATE=11/13/2013

PAGE TITLE

GRAPHICS: GPU GNDS & UNUSED

Apple Inc.

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BRANCH proto1b

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O/P= PPGPUCORE_S0_REG

GPUCORE
VOUT = VCORE
PEAK = 195A
AVG = 154A

DEFAULT->

SVC	SVD	GPUCORE
0	0	1.1 V
0	1	1.0 V
1	0	0.9 V
1	1	0.8 V

DRAWING
LAST_MODIFIED=Thu Feb 26 18:43:01 2015
SYNC_MASTER=J78_NAT
SYNC_DATE=02/06/2014
PAGE TITLE
GRAPHICS: GPU CORE VR
DRAWING NUMBER 051-00321
SIZE D
Apple Inc.
REVISION 4.0.0
BRANCH proto1b
PAGE 101 OF 120
SHEET 86 OF 96

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0315	1	CAP,39uF,20%,16V,POLY,D2	CA224	GPU:AME_NEP
	1	NO STUFF	CA224	GPU:EMERALD
138S0775	5	CAP,1uF,10%,25V,X6S,0402	CA254,CA220,CA255,CA239,CA261	GPU:AME_NEP
	5	NO STUFF	CA254,CA220,CA255,CA239,CA261	GPU:EMERALD

DRAWING LAST_MODIFIED=Thu Feb 26 18:43:02 2015

SYNC_MASTER=J95_HARPER SYNC_DATE=02/12/2015

PAGE TITLE

GRAPHICS: GPU CORE VR (PHASES 1-3)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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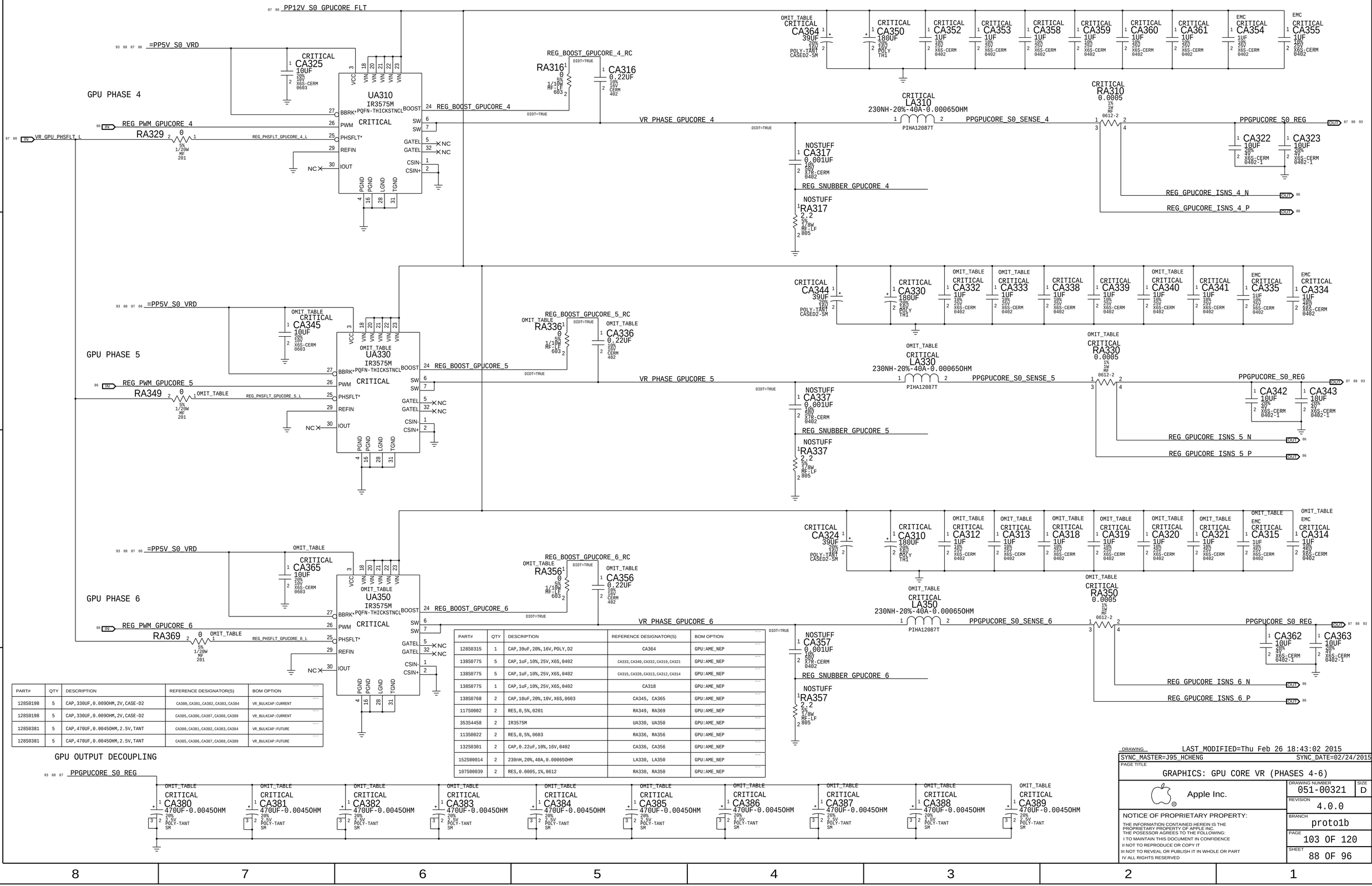
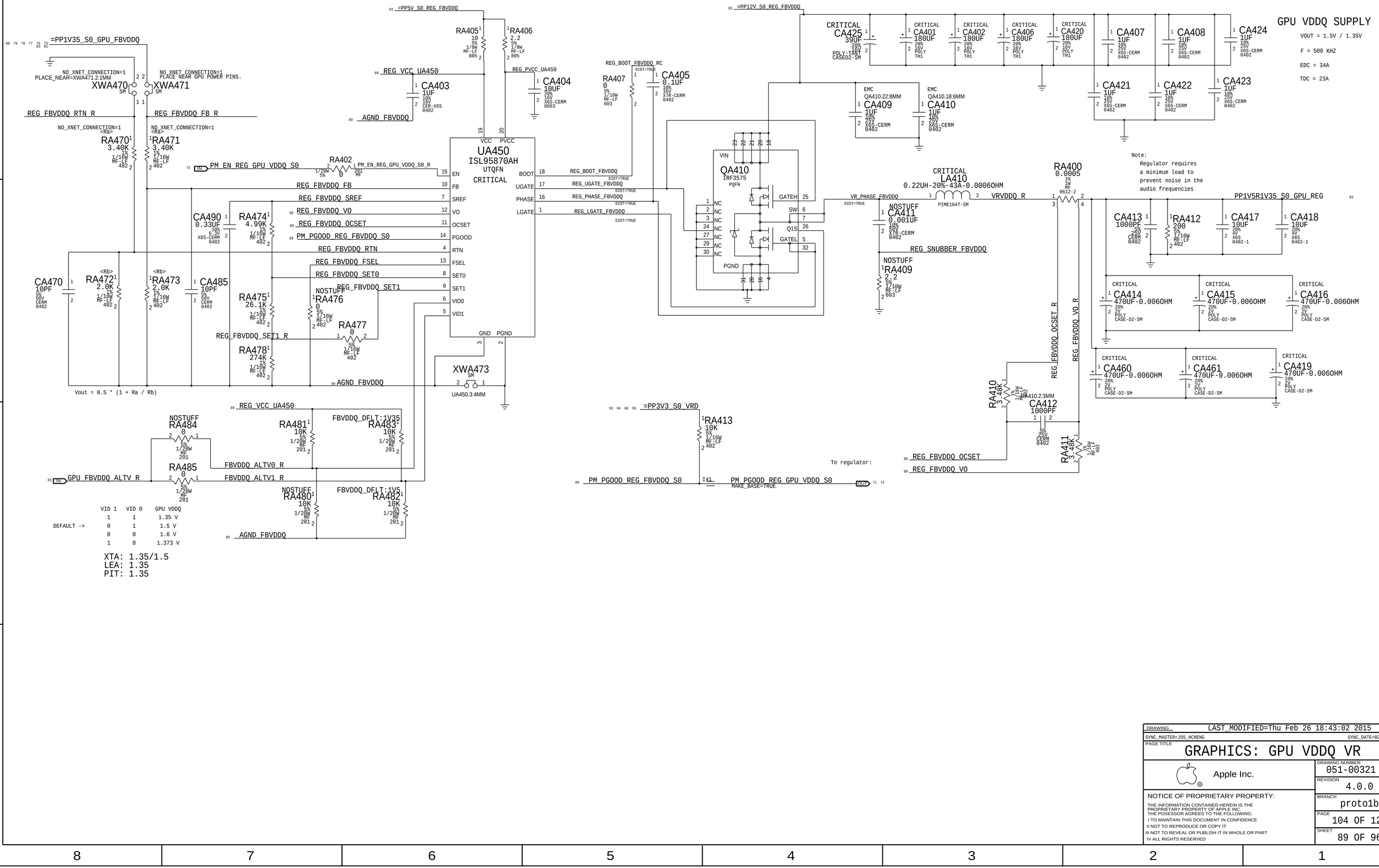


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0198	5	CAP,330UF,0.0090HM,2V,CASE-D2	CA380,CA381,CA382,CA383,CA384	VR_BULKCAP:CURRENT
128S0198	5	CAP,330UF,0.0090HM,2V,CASE-D2	CA385,CA386,CA387,CA388,CA389	VR_BULKCAP:CURRENT
128S0381	5	CAP,470UF,0.00450HM,2.5V,TANT	CA380,CA381,CA382,CA383,CA384	VR_BULKCAP:FUTURE
128S0381	5	CAP,470UF,0.00450HM,2.5V,TANT	CA385,CA386,CA387,CA388,CA389	VR_BULKCAP:FUTURE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0315	1	CAP,39UF,20%,16V,POLY,D2	CA364	GPU:AME_NEP
138S0775	5	CAP,1UF,10%,25V,X6S,0402	CA333,CA340,CA332,CA319,CA321	GPU:AME_NEP
138S0775	5	CAP,1UF,10%,25V,X6S,0402	CA315,CA320,CA313,CA312,CA314	GPU:AME_NEP
138S0775	1	CAP,1UF,10%,25V,X6S,0402	CA318	GPU:AME_NEP
138S0768	2	CAP,10UF,20%,10V,X6S,0603	CA345, CA365	GPU:AME_NEP
117S0002	2	RES,0,5%,0201	RA349, RA369	GPU:AME_NEP
353S4458	2	IR3575M	UA330, UA350	GPU:AME_NEP
113S0022	2	RES,0,5%,0603	RA336, RA356	GPU:AME_NEP
132S0301	2	CAP,0.22UF,10%,16V,0402	CA336, CA356	GPU:AME_NEP
152S00014	2	230nH,20%,40A,0.000650HM	LA330, LA350	GPU:AME_NEP
107S00039	2	RES,0.0005,1%,0612	RA330, RA350	GPU:AME_NEP

DRAWING: LAST_MODIFIED=Thu Feb 26 18:43:02 2015
SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015
PAGE TITLE: GRAPHICS: GPU CORE VR (PHASES 4-6)
Apple Inc.
DRAWING NUMBER: 051-00321 SIZE: D
REVISION: 4.0.0
BRANCH: proto1b
PAGE: 103 OF 120
SHEET: 88 OF 96



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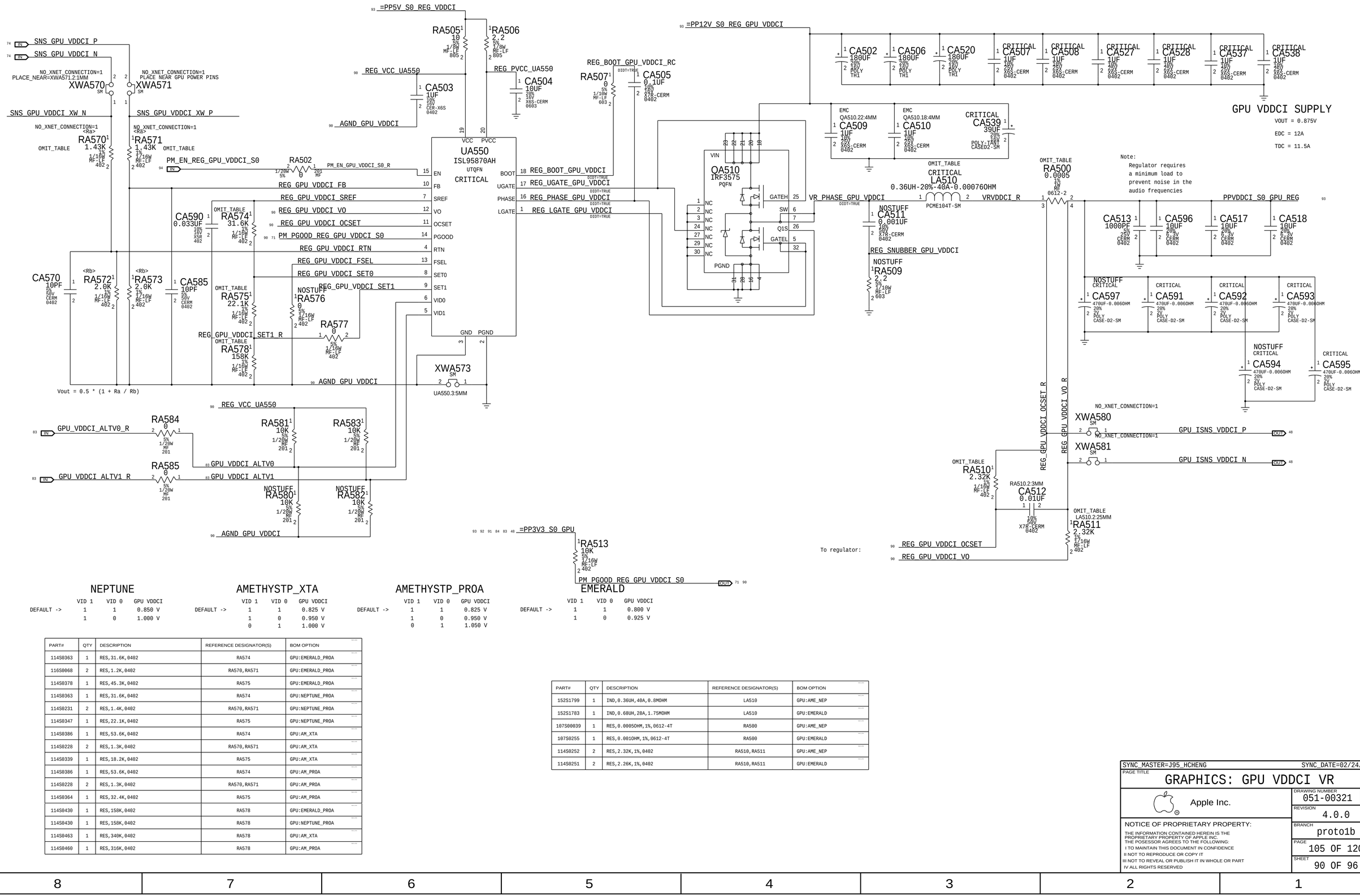
SYNC_MASTER=J95_HCHENG	SYNC_DATE=02/24/2015	
PAGE TITLE: GRAPHICS: GPU VDDQ VR		
Apple Inc.	DRAWING NUMBER: 051-00321	SIZE: D
	REVISION: 4.0.0	
	BRANCH: proto1b	
	PAGE: 104 OF 120	
	SHEET: 89 OF 96	



VID 1	VID 0	GPU VDDCI
DEFAULT -> 1	1	0.850 V
1	0	1.000 V

VID 1	VID 0	GPU VDDCI
DEFAULT -> 1	1	0.825 V
1	0	0.950 V
0	1	1.000 V

VID 1	VID 0	GPU VDDCI
DEFAULT -> 1	1	0.825 V
1	0	0.950 V
0	1	1.050 V

VID 1	VID 0	GPU VDDCI
DEFAULT -> 1	1	0.800 V
1	0	0.925 V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0363	1	RES,31.6K,0402	RA574	GPU:EMERALD_PROA
116S0068	2	RES,1.2K,0402	RA570,RA571	GPU:EMERALD_PROA
114S0378	1	RES,45.3K,0402	RA575	GPU:EMERALD_PROA
114S0363	1	RES,31.6K,0402	RA574	GPU:NEPTUNE_PROA
114S0231	2	RES,1.4K,0402	RA570,RA571	GPU:NEPTUNE_PROA
114S0347	1	RES,22.1K,0402	RA575	GPU:NEPTUNE_PROA
114S0386	1	RES,53.6K,0402	RA574	GPU:AM_XTA
114S0228	2	RES,1.3K,0402	RA570,RA571	GPU:AM_XTA
114S0339	1	RES,18.2K,0402	RA575	GPU:AM_XTA
114S0386	1	RES,53.6K,0402	RA574	GPU:AM_PROA
114S0228	2	RES,1.3K,0402	RA570,RA571	GPU:AM_PROA
114S0364	1	RES,32.4K,0402	RA575	GPU:AM_PROA
114S0430	1	RES,158K,0402	RA578	GPU:EMERALD_PROA
114S0430	1	RES,158K,0402	RA578	GPU:NEPTUNE_PROA
114S0463	1	RES,340K,0402	RA578	GPU:AM_XTA
114S0460	1	RES,316K,0402	RA578	GPU:AM_PROA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S1799	1	IND,0.36UH,40A,0.8MOHM	LA510	GPU:AME_NEP
152S1783	1	IND,0.68UH,28A,1.75MOHM	LA510	GPU:EMERALD
107S00039	1	RES,0.0005OHM,1%,0612-4T	RA500	GPU:AME_NEP
107S0255	1	RES,0.001OHM,1%,0612-4T	RA500	GPU:EMERALD
114S0252	2	RES,2.32K,1%,0402	RA510,RA511	GPU:AME_NEP
114S0251	2	RES,2.26K,1%,0402	RA510,RA511	GPU:EMERALD

SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015

PAGE TITLE

GRAPHICS: GPU VDDCI VR

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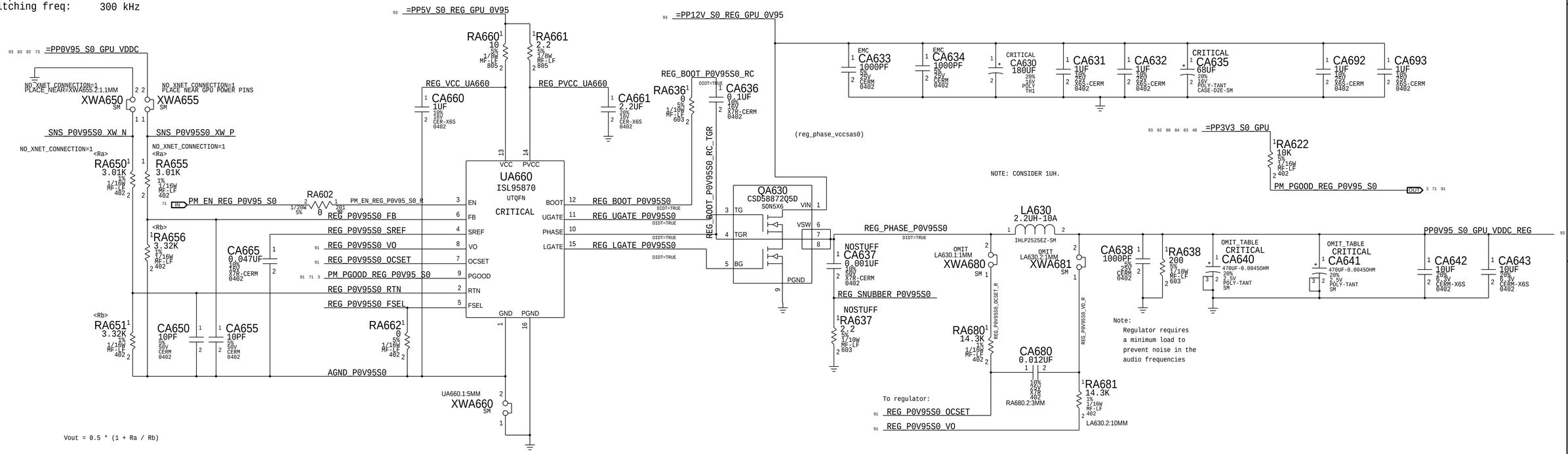
GPU VDDC (0.95V) S0 REGULATOR

Max avg current: 4.3 A
Max peak current: 4.5 A
Switching freq: 300 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.006OHM,2V,D2	CA640,CA641	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	CA640,CA641	VR_BULKCAP:FUTURE

DRAWING
LAST_MODIFIED=Thu Feb 26 18:43:02 2015
SYNC_MASTER=J78_MLB
SYNC_DATE=08/02/2014
PAGE TITLE
GRAPHICS: GPU 0V95 VR

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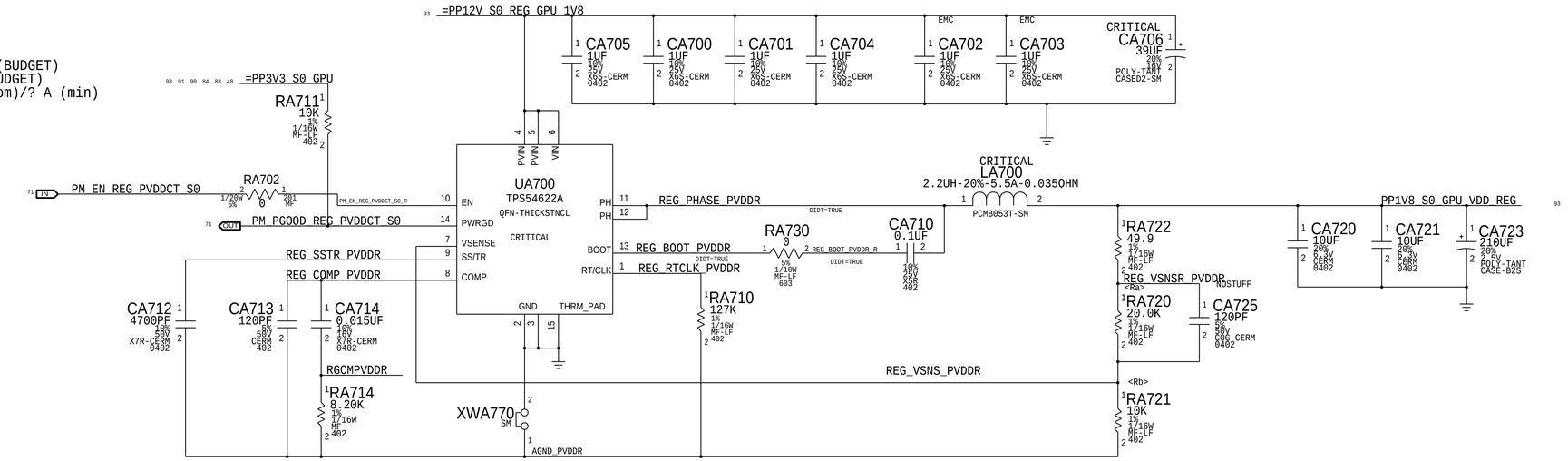
1.8V S0 Regulator

Max avg current: 2.4 A (BUDGET)
Max peak current: 3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



VOUT = 0.6 * (1 + RA / RB)

DRAWING	LAST_MODIFIED=Thu Feb 26 18:43:02 2015
SYNC_MASTER=J95_HARPER	SYNC_DATE=02/11/2015
PAGE TITLE	GRAPHICS: GPU 1V8 VR
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G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 18
- =PP3V3_G3_PCH_RTC — 12 15

G3H Rails

On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 59
- =PP12V_G3H_SNS_R — 47

PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 47
- =PP12V_G3H_P3V42 — 59
- =PP12V_G3H_FET_P12V_S0 — 70
- =PP12V_G3H_FET_P12V_S5 — 70
- =PP12V_G3H_FET_P12V_S5_SSD — 65 70

PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG — 59
- =PP3V3_G3H_BT — 31
- =PP3V3_G3H_RTC_D — 18
- =PP3V3_G3H_SMC — 43 44 50
- =PP3V3_G3H_SMC_USBMUX — 41
- =PPVIN_G3H_SMCVREF — 44
- =PP3V3_G3H_T112 — 45
- =PP3V3_G3H_SSD — 59 65 70

Ground/Common

GND (MAKE_BASE=TRUE)

S5 Rails

On when in S5

PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 70
- =PP12V_S5_REG_VDDQ_S3 — 63
- =PP12V_S5_PWRCTL — 70 71
- =PPHV_SW_TBTAPWRSW — 28
- =PPHV_SW_TBTBPWRSW — 29
- =PP12V_S5_SNS — 47
- =PP12V_S5_REG_P1V0_S5 — 66

PP12V_S5_SSD (MAKE_BASE=TRUE)
- PP12V_S5_SSD_FET — 70
- =PP12V_S5_FET_P3V3_S5_P5V_S4 — 65
- =PP12V_S5_FET_PWRCTL — 32 70
- =PP12V_S5_FET_P12V_S5_NON_SSD — 65

PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 65
- =PP5V_S5_REG_P1V0 — 66
- =PP5V_S5_XDP — 17

PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_FET_NON_SSD — 65
- =PP3V3_S5_FET_P3V3_S0 — 70
- =PP3V3_S5_FET_P3V3_S4 — 70
- =PP3V3_S5_SMC — 32 44
- =PP3V3_S5_LED — 3
- =PP3V3_S5_PCH_VCC — 12 13 14 15 18 19
- =PP3V3_S5_PWRCTL — 32 65 71 72
- =PP3V3_S5_ROM — 17 45
- =PP3V3_S5_VRD — 65 66
- =PP3V3_S5_SENSE — 47
- =PP3V3_S5_RSTBUF — 19

PP3V3_S5_SSD (MAKE_BASE=TRUE)
- PP3V3_S5_REG_SSD — 65
- =PPVSSD_S5_FET_S4_SSD — 32
- =PP3V3_S5_SSD_PWRCTL — 32 65
- =PP3V3_S5_NON_SSD — 65

PP1V0_S5 (MAKE_BASE=TRUE)
- PP1V0_S5_REG — 66
- =PP1V0_S5_PCH_VCC — 11 15
- =PP1V0_S5_XDP — 17
- =PP1V0_S5_FET_PP1V0_S3 — 70

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG — 65
- =PP5V_S4_REG_VDDQ_S3 — 63
- =PP5V_S4_FET_P5V_S0 — 70
- =PP5V_S4_USB — 41 42

PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 70
- =PP3V3_S4_FET_ENET — 35
- =PP3V3_S4_PWRCTL — 41 42 63 70
- =PP3V3_S4_LED — 3
- =PP3V3_S4_MEMRESET — 6
- =PP3V3_S4_PCH_VCC — 13 14
- =PP3V3_S4_SDCARD — 36
- =PP3V3_S4_SMC — 44
- =PP3V3_S4_TBT — 19 26 27 28 29 30 71
- =PP3V3_S4_AUDIO_DIG — 55
- =PP3V3_S4_TBTAPWRSW — 28
- =PP3V3_S4_TBTBPWRSW — 29
- =PP3V3_S4_AP — 31 44

PP3V3_S4_SSD_FET (MAKE_BASE=TRUE)
- PP3V3_S4_FET_SSD — 32
- =PPVSSD_S4_REG_SNS_R — 48

PP3V3_S4_SSD (MAKE_BASE=TRUE)
- PPVSSD_S4_REG_SNS — 48
- =PPVSSD_S4_CONN — 32

S3 Rails

Enabled when system is in run or sleep

PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 35
- =PP3V3_ENET_PHY — 34 35

PPVDDQ_S3 (MAKE_BASE=TRUE)
- PPVDDQ_S3_REG — 63
- =PPVDDQ_S3_SNS_DDR_R — 48
- =PP1V35_S3_SNS_R — 48

THIS IS 1.35V RAIL

PPVDDQ_S3_DDR (MAKE_BASE=TRUE)
- PPVDDQ_S3_SNS_DDR — 48
- =PPDDR_S3_MEMVREF — 20
- =PPVDDQ_S3_MEM_A — 21 22
- =PPVDDQ_S3_MEM_B — 23 24
- =PPVDDQ_S3_MEMRESET — 12
- =PPVDDQ_S3_LDO_DDRVTT — 63

THIS IS 1.35V RAIL

PP1V35_S3_CPU (MAKE_BASE=TRUE)
- PP1V35_S3_SNS — 48
- =PPVDDQ_S3_CPU — 8 10

PP1V0_S3_CPU_VCCST (MAKE_BASE=TRUE)
- PP1V0_S3_FET — 70
- =PP1V0_S3_VCCST — 12 60
- =PP1V0_S3_SMC — 44
- =PP1V0_S3_XDP — 17
- =PP1V0_S3_CPU — 6 8 10

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 70
- =PP12V_S0_AUDIO_SPKRAMP — 53 54
- =PP12V_S0_FAN — 50
- =PP12V_S0_SNS_GPUCORE_R — 47
- =PP12V_S0_LCD — 39
- =PP12V_S0_CPUCORE — 60
- =PP12V_S0_SNS_FBVDDQ_R — 47
- =PP12V_S0_HDD — 33
- =PP12V_S0_BKLT — 68

PP12V_S0_GPU_AUX (MAKE_BASE=TRUE)
- PP12V_S0_SNS_GPU_AUX — 47
- =PP12V_S0_REG_GPU_0V95 — 91
- =PP12V_S0_REG_GPU_1V8 — 92

PP12V_S0_GPUCORE (MAKE_BASE=TRUE)
- PP12V_S0_SNS_GPUCORE — 47
- =PP12V_S0_REG_GPUCORE — 86
- =PP12V_S0_REG_GPU_VDDCI — 90

93 60 PP12V_S0_CPUCORE_FLT (MAKE_BASE=TRUE)
- PP12V_S0_CPUCORE_FLT — 60 93
- =PP12V_S0_SNS_CPUCORE_R — 47

PP12V_S0_CPUCORE (MAKE_BASE=TRUE)
- PP12V_S0_SNS_CPUCORE — 47
- =PP12V_S0_REG_CPUCORE — 60 61 62 64 67

PPHDD12_S0 (MAKE_BASE=TRUE)
- PP12V_S0_HDD_FET — 33
- =PP12V_S0_HDD_SNS_R — 48

PP12V_S0_HDD (MAKE_BASE=TRUE)
- PP12V_S0_HDD_SNS — 48
- =PP12V_S0_HDD_PWR — 33

PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)
- PP12V_S0_SNS_FBVDDQ — 47
- =PP12V_S0_REG_FBVDDQ — 89

PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 70
- =PP5V_S0_AUDIO — 51 58
- =PP5V_S0_BKLT — 68
- =PP5V_S0_ISENSE — 47
- =PP5V_S0_REG_CPUVCC_S0 — 60 61 62 64 67
- =PP5V_S0_REG_FBVDDQ — 89
- =PP5V_S0_HDD — 33
- =PP5V_S0_VRD — 86 87 88
- =PP5V_S0_REG_VDDCI — 90
- =PP5V_S0_REG_GPU_0V95 — 91
- =PP5V_S0_CAMERA — 37
- =PP5V_S0_REG_GPUCORE — 86

PPHDD_S0 (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 33
- =PPHDD_S0_SNS_R — 48

PP5V_S0_HDD (MAKE_BASE=TRUE)
- PPHDD_S0_SNS — 48
- =PP5V_S0_HDD_PWR — 33

PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 70
- =PP3V3_S0_AUDIO — 37 51 53 54 57
- =PP3V3_S0_AUDIO_DIG — 55
- =PP3V3_S0_BKLT — 68
- =PP3V3_S0_DP — 30 39
- =PP3V3_S0_ENET — 34
- =PP3V3_S0_FAN — 50
- =PP3V3_S0_GPU — 48 83 84 90 91 92
- =PP3V3_S0_INTDPMUX — 39 40
- =PP3V3_S0_LED — 3
- =PP3V3_S0_LED_SATA — 32
- =PP3V3_S0_MEM_A_SPD — 21 22
- =PP3V3_S0_MEM_B_SPD — 23 24
- =PP3V3_S0_PCH_VCC — 11 12 14 15 18 19
- =PP3V3_S0_PWRCTL — 70 71
- =PP3V3_S0_RSTBUF — 19
- =PP3V3_S0_SDCARD — 36
- =PP3V3_S0_SENSE — 33 47 48 49
- =PP3V3_S0_SMBUS — 46
- =PP3V3_S0_SMBUS_SMC_0 — 46
- =PP3V3_S0_SMBUS_SMC_1 — 46
- =PP3V3_S0_SMBUS_SMC_3 — 46
- =PP3V3_S0_SMC — 44
- =PP3V3_S0_VRD — 59 60 64 89
- =PP3V3_S0_PCH_GPIO — 27
- =PP3V3_S0_CAMERA — 37 38
- =PP3V3_S0_ALS — 37
- =PP3V3_S0_SMBUS_SMC_2 — 46
- =PP3V3_S0_REG_GPUCORE — 86

PPDDRVTT_S0 (MAKE_BASE=TRUE)
- PPDDRVTT_S0_LDO — 63
- =PPDDRVTT_S0_MEM_A — 21 22
- =PPDDRVTT_S0_MEM_B — 23 24

GPU Rails (S0)

Enabled when system is in run

PPGPUCORE_S0 (MAKE_BASE=TRUE)
- PPGPUCORE_S0_REG — 87 88
- =PPGPUCORE_S0 — 74 75
- =PPGPUCORE_S0_SNS — 47

FBVDDQ IS 1.5V

PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)
- PP1V5R1V35_S0_GPU_REG — 89
- =PP1V35_S0_GPU_FBVDDQ — 75 76 77 78 79 80 81 89

PPVDDCI_S0_GPU (MAKE_BASE=TRUE)
- PPVDDCI_S0_GPU_REG — 90
- =PPVDDCI_S0_GPU — 74

PP0V95_S0_GPU_VDDC (MAKE_BASE=TRUE)
- PP0V95_S0_GPU_VDDC_REG — 91
- =PP0V95_S0_GPU_VDDC — 73 82 83 91
- =PP0V95_S0_GPU_PCIEVDDC — 73

PP1V8_S0_MISC (MAKE_BASE=TRUE)
- PP1V8_S0_GPU_VDD_REG — 92
- =PP1V8_S0_GPU_VDD — 82 83 84 86
- =PP1V8_S0_CAMERA — 37 38
- =PP1V8_S0_GPU_PEX_IO — 73
- =PP1V8_S0_AUD_DIG — 51
- =PP1V8_S0_DP — 40

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

27 26 PP3V3_TBTLC (MAKE_BASE=TRUE)
- =PP3V3_TBTLC — 19

CPU/PCH Rails (S0)

Enabled when system is in run

PPVCC_S0_CPU (MAKE_BASE=TRUE)
- PPVCC_S0_CPU_REG — 61
- =PPVCC_S0_CPU — 8 10
- =PPVCC_S0_SNS_CPU — 47

PPVCCGT_S0_CPU (MAKE_BASE=TRUE)
- PPVCCGT_S0_CPU_REG — 62
- =PPVCCGT_S0_CPU — 8 10
- =PPVCCGT_S0_SNS_CPU — 47

PPVCCSA_S0_CPU (MAKE_BASE=TRUE)
- PPVCCSA_S0_CPU_REG — 67
- =PPVCCSA_S0_CPU — 8 10

PPVCCIO_S0 (MAKE_BASE=TRUE)
- PPVCCIO_S0_CPU_REG — 64
- =PPVCCIO_S0_SNS_CPU_R — 47

PPVCCIO_S0_CPU (MAKE_BASE=TRUE)
- PPVCCIO_S0_SNS_CPU — 47
- =PPVCCIO_S0_CPU — 5 8 10 17

SYNC_MASTER=J78_MLB SYNC_DATE=11/20/2013

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Power Connectors/Aliases

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PEG aliases

73 PEG_D2R_N<0..15> ⟹ =PEG_D2R_N<15..0> 5
MAKE_BASE=TRUE

73 PEG_D2R_P<0..15> ⟹ =PEG_D2R_P<15..0> 5
MAKE_BASE=TRUE

73 PEG_R2D_C_N<0..15> ⟹ =PEG_R2D_C_N<15..0> 5
MAKE_BASE=TRUE

73 PEG_R2D_C_P<0..15> ⟹ =PEG_R2D_C_P<15..0> 5
MAKE_BASE=TRUE

GPU ALIASES

83 73 GPU_RESET_L ⟹ TP_GPU_RESET_L 19
MAKE_BASE=TRUE

86 VR_GPU_RESET_L ⟹ TP_VR_GPU_RESET_L 19
MAKE_BASE=TRUE

GPU VDDCI PGOOD

73 TP_PM_EN_REG_GPU_VDDCI_S0 ⟹ PM_EN_REG_GPU_VDDCI_S0 90
MAKE_BASE=TRUE

SYNC_MASTER=J78_MLB SYNC_DATE=12/05/2013

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Signal Aliases

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CPU Reserved

17 6 CPU_CFG<15..12> —— TP_CPU_CFG<15..12>
MAKE_BASE=TRUE

39 DP_INT_PIN_57 —— NC_DP_INT_PIN_57
MAKE_BASE=TRUE
39 DP_INT_PIN_55 —— NC_DP_INT_PIN_55
MAKE_BASE=TRUE

12 TP_CLINK_DATA —— CLINK_DATA
MAKE_BASE=TRUE NO_TEST=1
12 TP_CLINK_CLK —— CLINK_CLK
MAKE_BASE=TRUE NO_TEST=1
12 TP_CLINK_RESET_L —— CLINK_RESAT_L
MAKE_BASE=TRUE NO_TEST=1
83 TP_GPU_CB_REFCKN_OUT1 —— GPU_CB_REFCKN_OUT1
MAKE_BASE=TRUE
83 TP_GPU_CB_REFCKP_OUT1 —— GPU_CB_REFCKP_OUT1
MAKE_BASE=TRUE
83 TP_GPU_PLL_ANALOG_IN —— GPU_PLL_ANALOG_IN
MAKE_BASE=TRUE
12 TP_PCH_SLP_LAN_L —— PCH_SLP_LAN_L
MAKE_BASE=TRUE NO_TEST=1
11 TP_PCH_2 —— PCH_2
MAKE_BASE=TRUE NO_TEST=1
12 TP_PM_SLP_A_L —— PM_SLP_A_L
MAKE_BASE=TRUE NO_TEST=1
26 TP_TBT_MONDC1 —— TBT_MONDC1
MAKE_BASE=TRUE
26 TP_TBT_PCIE_RESET0_L —— TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=1

PCH Clocks

TP_ITPXDP_CLK100MP —— ITPXDP_CLK100M_P 11 17
MAKE_BASE=TRUE NO_TEST=1
TP_ITPXDP_CLK100MN —— ITPXDP_CLK100M_N 11 17
MAKE_BASE=TRUE NO_TEST=1

PCH Miscellaneous

11 TP_HDA_SDIN1 —— NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=1

11 PEG_CLKREQ_L —— NC_PEG_CLKREQ_L
MAKE_BASE=TRUE
14 GPU_NEPTUNE_EMERALD_ID —— NC_GPU_IS_AMETHYST
MAKE_BASE=TRUE NO_TEST=1

SYNC_MASTER=J78_MLB SYNC_DATE=12/05/2013

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Unused Signal Aliases

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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT,BGA_VRAM	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	0.070 MM	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

_____	Top	Signal	0.5 oz (Cu plated)
_____		Prepreg	0.071 MM
_____	2	Plane	1 oz
_____		Core	0.101 MM
_____	3	Signal	0.5 oz
_____		Prepreg	0.115 MM
_____	4	Plane	1 oz
_____		Core	0.076 MM
_____	5	Signal	0.5 oz
_____		Prepreg	0.380 MM
_____	6	Plane	1 oz
_____		Core	0.076 MM
_____	7	Plane	1 oz
_____		Prepreg	0.380 MM
_____	8	Signal	0.5 oz
_____		Core	0.076 MM
_____	9	Plane	1 oz
_____		Prepreg	0.115 MM
_____	10	Signal	0.5 oz
_____		Core	0.101 MM
_____	11	Plane	1 oz
_____		Prepreg	0.071 MM
_____	Btm	Signal	0.5 oz (Cu plated)

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

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Apple Inc.

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