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16	Calpella (RESERVE)
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18	PCH (PCI-e,SMBUS,CLK)
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20	PCH (LVDS,DDI)
21	PCH (PCI,USB,NVRAM)
22	PCH (GPIO,VSS_NCTF,RSVD)
23	PCH (POWER) 1
24	PCH (POWER) 2
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27	DDR3 (SO-DIMM_1)
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29	M92_S2 (STRAP) 2/6
30	M92_S2 (IO) 3/6
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32	M92_S2 (DP) 5/6
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34	GDDR (DDR3) 1/3
35	GDDR (DDR3) 2/3
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38	EC FLASH ROM/SPI
39	AUDIO ALC662
40	AUDIO SPK+AMP

PAGE	TITLE
41	AUDIO (MUTE)
42	AUDIO (JACK+AMP)
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44	RJ11
45	USB POWER I/O
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47	CARD READER
48	Mini_PCIe (WLAN) 1
49	Mini_PCIe (WLAN) 2
50	SATA HDD/ODD
51	VGA
52	LVDS
53	HDMI
54	Discrete GPU option
55	CAMERA
56	BlueTooth
57	FAN/THERMAL SENSOR
58	POWER Button Board/LED
59	PWR_DCIN/Battery
60	PWR_CHARGER
61	5VA/3.3VA
62	CPU_Vcore
63	1.1V VTT
64	1_05VS
65	1.8VS
66	DDR3 1.5V_VTT-DDR 0.75V
67	VPCIe
68	PWR_others power plane
69	CPU VREG/Decoupling
70	Graphic VDD_CORE
71	BLANK

C02

2010-05-05

Phase: MP
BOM:

PCB Fab Note

PCB1
Printed Circuit Board
PCB_CALPELLA_REV:X1
Critical

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Title: COVER		
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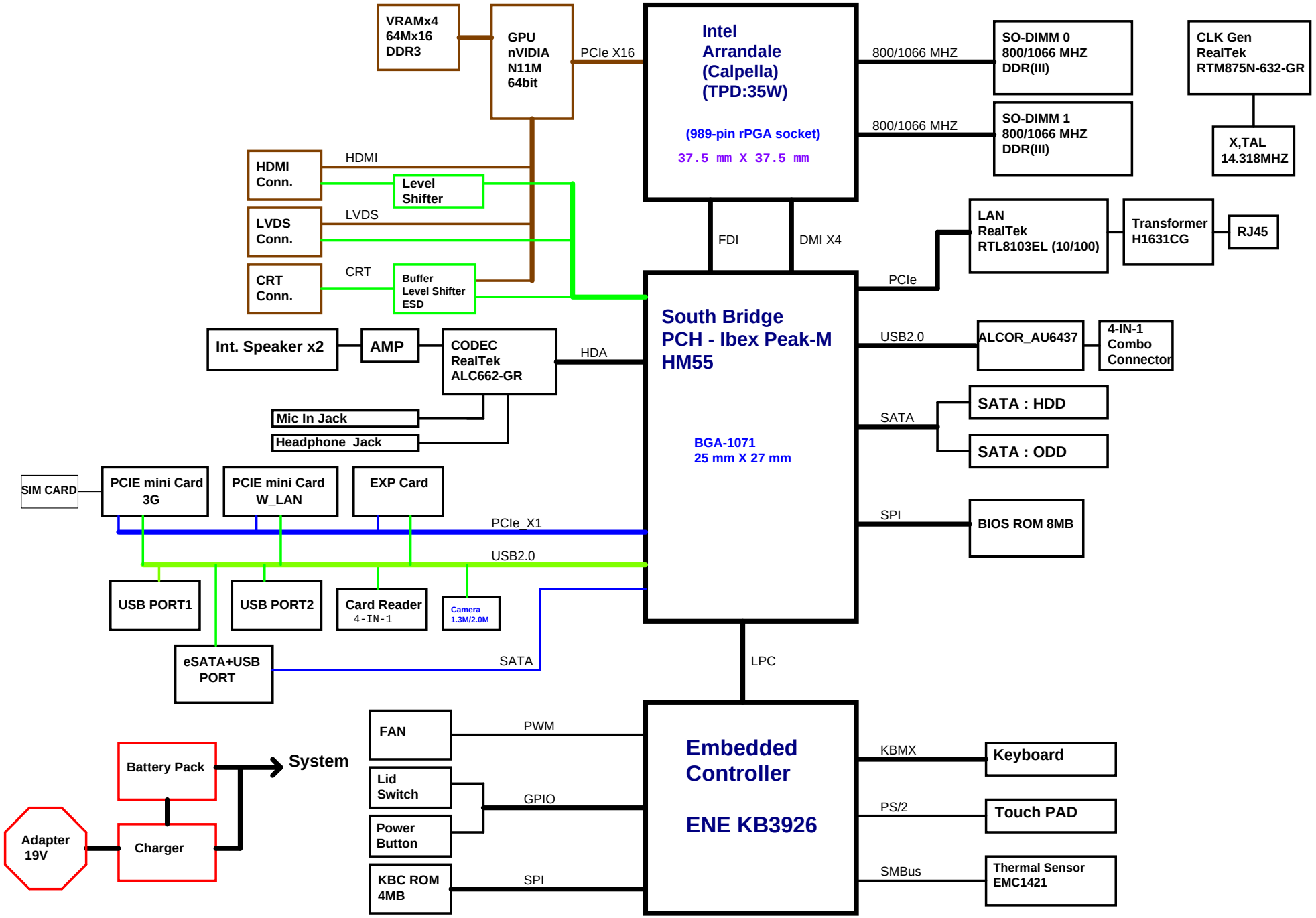

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Title: SYSTEM BLOCK DIAGRAM		
Size: Custom	Document Number: C02	Rev: A
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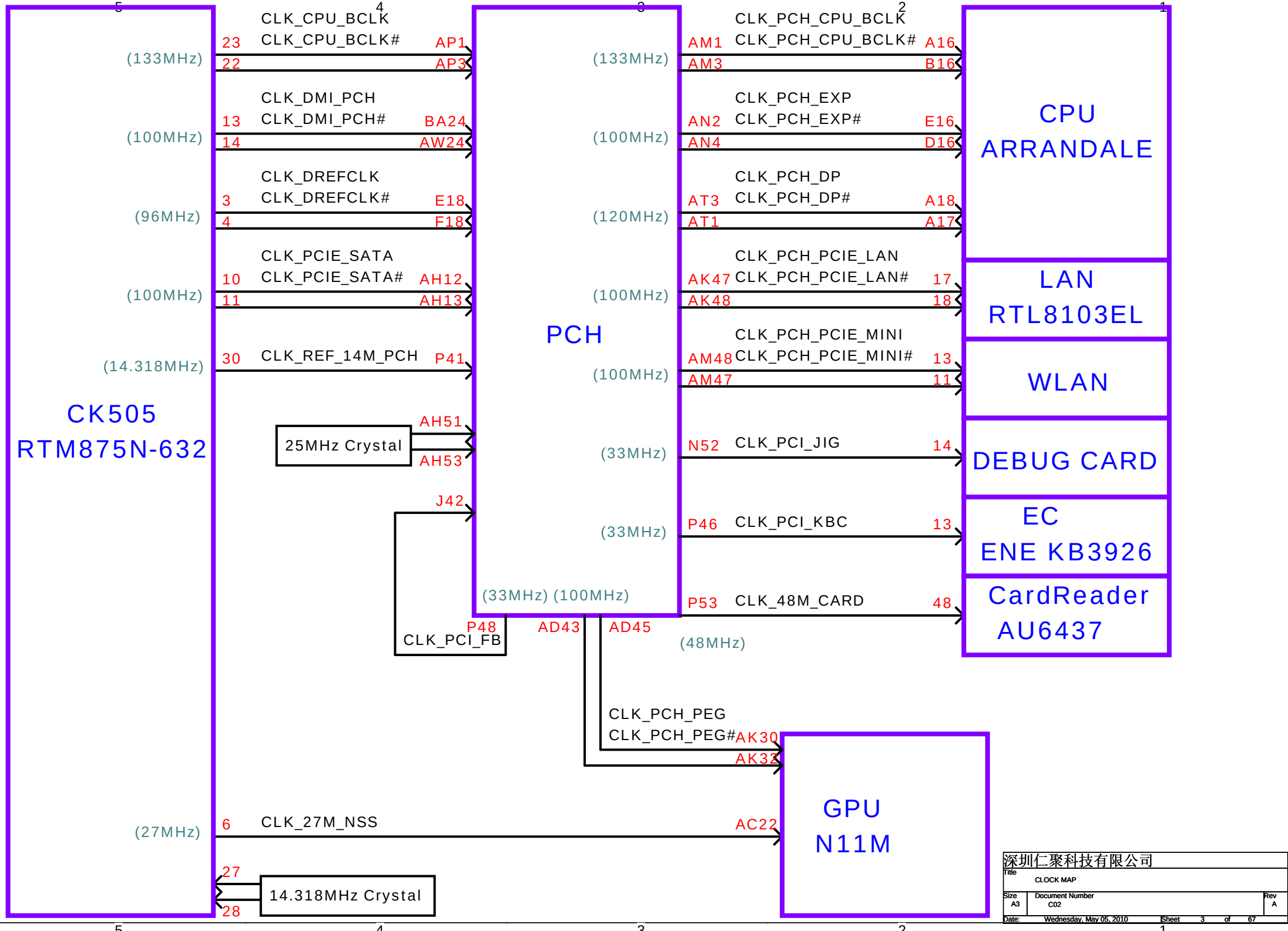
CK505
RTM875N-632
PCH
CPU
ARRANDALE
LAN
RTL8103EL
WLAN
DEBUG CARD
EC
ENE KB3926
CardReader
AU6437
GPU
N11M
25MHz Crystal
14.318MHz Crystal
CLK_CPU_BCLK
CLK_CPU_BCLK#
(133MHz)
23
22
AP1
AP3
AM1
AM3
A16
B16
CLK_DMI_PCH
CLK_DMI_PCH#
(100MHz)
13
14
BA24
AW24
CLK_PCH_EXP
CLK_PCH_EXP#
AN2
AN4
E16
D16
CLK_DREFCLK
CLK_DREFCLK#
(96MHz)
3
4
E18
F18
CLK_PCH_DP
CLK_PCH_DP#
(120MHz)
AT3
AT1
A18
A17
CLK_PCIE_SATA
CLK_PCIE_SATA#
(100MHz)
10
11
AH12
AH13
CLK_PCH_PCIE_LAN
CLK_PCH_PCIE_LAN#
AK47
AK48
17
18
CLK_REF_14M_PCH
(14.318MHz)
30
P41
CLK_PCH_PCIE_MINI
CLK_PCH_PCIE_MINI#
AM48
AM47
13
11
AH51
AH53
CLK_PCI_JIG
(33MHz)
N52
14
J42
CLK_PCI_KBC
(33MHz)
P46
13
(33MHz) (100MHz)
P48
CLK_PCI_FB
AD43
AD45
CLK_48M_CARD
P53
48
(48MHz)
CLK_PCH_PEG
CLK_PCH_PEG#
AK30
AK32
CLK_27M_NSS
(27MHz)
6
AC22
27
28
深圳仁聚科技有限公司
Title
CLOCK MAP
Size
A3
Document Number
C02
Rev
A
Date:
Wednesday, May 05, 2010
Sheet
3
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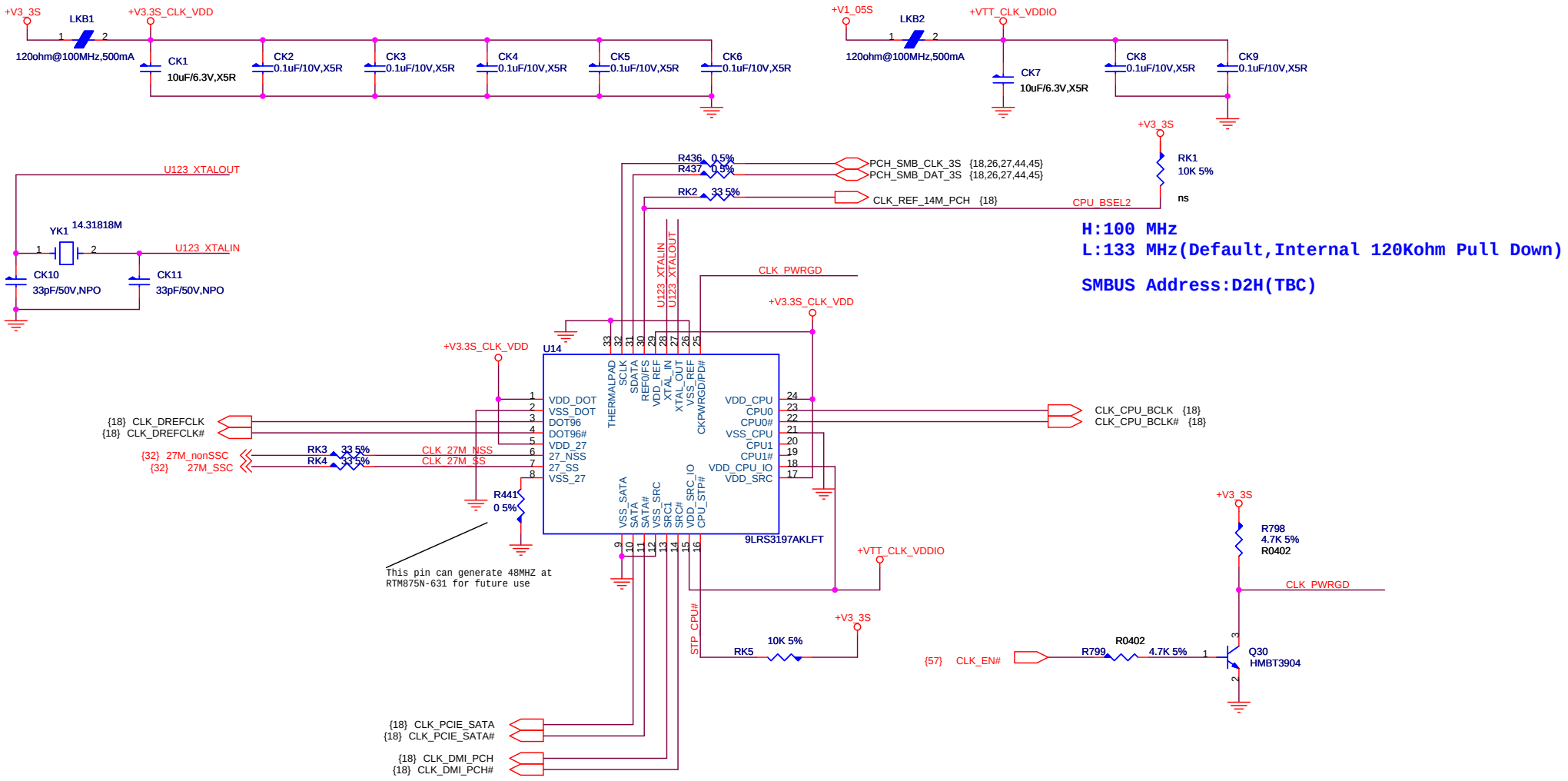
67



FSP Table

FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

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Title: CLOCK GEN

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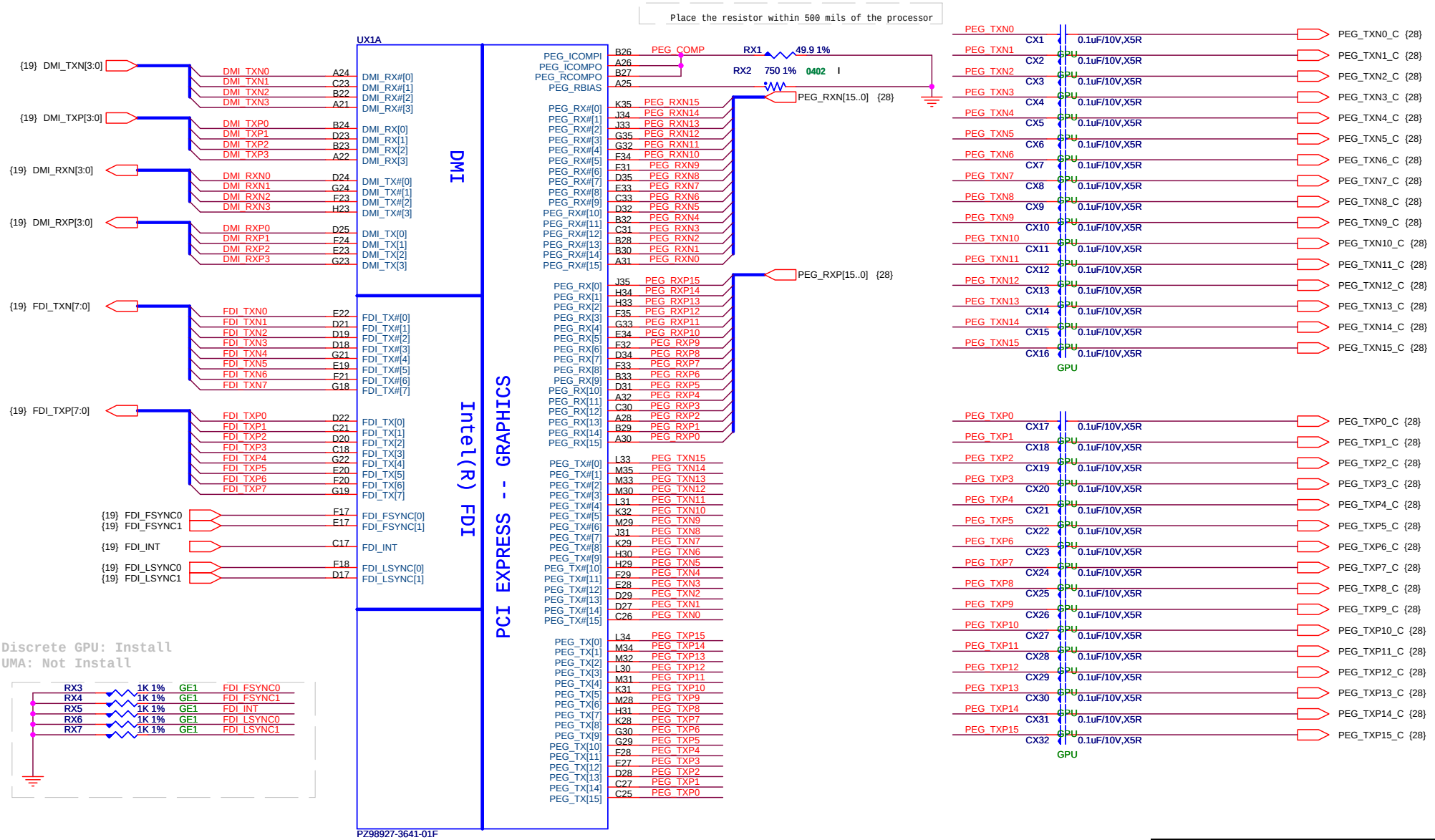

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Title: Calpella (DMI,PEG,FDI)		
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Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace
length shorter then 0.5". Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace
length shorter then 0.5". Width=5mil(MS)

Place close to chip

UX1B

MISC
CLOCKS
THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT

COMP3 AT23
COMP2 AT24
COMP1 G16
COMP0 AT26
SKTOCC# AH24
CATERR# AK14
PECI AT15
PROCHOT# AN26
THERMTRIP# AK15
RESET_OBS# AP26
PM_SYNC AL15
VCCPWRGOOD_1 AN14
VCCPWRGOOD_0 AN27
SM_DRAMPWROK AK13
VTTPWRGOOD AM15
TAPPWRGOOD AM26
RSTIN# AL14

BCLK A16
BCLK# B16
BCLK_ITP AR30
BCLK_ITP# AT30
PEG_CLK E16
PEG_CLK# D16
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17
SM_DRAMRST# F6
SM_RCOMP[0] AL1
SM_RCOMP[1] AM1
SM_RCOMP[2] AN1
PM_EXT_TS#[0] AN15
PM_EXT_TS#[1] AP15
PRDY# AT28
PREQ# AP27
TCK AN28
TMS AP28
TRST# AT27
TDI AT29
TDO AR27
TDI_M AR29
TDO_M AP29
DBR# AN25
BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23

PZ98927-3641-01F

Layout Check-thermal, power manager

Pins Unused by Clarksfield(TBC)

RX8 20 1% 0402 COMP3
RX9 20 1% 0402 COMP2
RX10 49.9 1% COMP1
RX12 49.9 1% COMP0
RX11 49.9 1%
+V1_05S
H_CATERR#
{22} H_PECI RX54 0 5% R0402 CPU_PECI
VR_PROCHOT#
{22,66} PM_THRMTRIP# RX39 0 5% H_THRMTRIP#
{19} H_PM_SYNC
RX26 0 5% CPUPWRGD1
{22} H_CPUPWRGD RX28 0 5% CPUPWRGD0
{19} PM_DRAM_PWRGD RX29 0 5% DRAM_PWRGD
VTTPWRGOOD
{21,28} PLT_RST# RX31 1.5K 1% RSTIN#
RX32 698 1% 0402

Clarksfield: 1.1V(RX30=1.5K 1%; RX31=750 1%)
Arrandale : 1.05V(RX30=1.5K 1% ; RX31=698 1%)

BCLK CLK_PCH_CPU_CLK {22}
BCLK# CLK_PCH_CPU_CLK# {22}
(133MHz)

TP380, TP379 ICT_TP

Discrete :RX14,RX17 Not Install and RX15,RX16 0 ohm
UMA: RX14,RX17 0 ohm and RX15,RX16 Not Install

BCLK_ITP CLK_PCH_EXP_R RX13 0 5%
BCLK_ITP# CLK_PCH_EXP# R RX14 0 5%
CLK_PCH_EXP {18}
CLK_PCH_EXP# {18}
(100MHz)

CLK_PCH_DP_R RX16 0 5% GE1
CLK_PCH_DP# R RX17 0 5% GE1
RX15 0 5% IGP_OP1 CLK_PCH_DP {18}
(120MHz)
RX18 0 5% IGP_OP1 CLK_PCH_DP# {18}

+V1_05S
DDR3_DRAMRST# {26,27}
SM_RCOMP0 RX20 100 1%
SM_RCOMP1 RX21 24.9 1%
SM_RCOMP2 RX23 130 1%
RX24 10K 5%
RX22 10K 5%
PM_EXTTS#0
PM_EXTTS#1 R
RX53 0 5% PM_EXTTS#1 {26,27}
RX25 12.4K 1% 0402 NI ns

XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
XDP_TDI_M
XDP_TDO_M
CPU_DBR# RX27 0 5% ns DBR_RESET# {19}

+V1_05S
R52 1K 5%
RX63 0 5% ns EC_PROCHOT2# {37}
R0402
VR_PROCHOT# {57}
{37} EC_PROCHOT# RX30 1K 5% R0402
QX2 2N7002PT SOT23
C338 1000pF/50V,X7R ns
C0402

Check with Intel CRB

TCK 50 PD
TMS 2k~5k PU
TRST 2k~5k PU
TDI 50 PU
TDO unconnect
TDI_M 50 PU
TDO_M unconnect

+V1_05S
XDP_TDO RX33 51 5% ns
XDP_TMS RX34 51 5% ns
XDP_TDI RX35 51 5% ns
XDP_PREQ# RX36 51 5% ns
XDP_TCLK RX37 51 5% ns
XDP_TRST#
RX38 51 5%

XDP_TDO_M
RX44 0 5%
ns
XDP_TDI_M

+V1_5SM
RX40 1.1K 1%
DRAM_PWRGD
RX45 2.61K 1% 0402

Clarksfield: 1.1V(RX38=1.1K 1%; RX43=3.01K 1%)
Arrandale : 1.05V(RX38=1.1K 1% ; Rx43=2.61K 1%)

ux2,ux3 co-layout

+V3_3S
UX3
V1_05S_PWROK
VCC
GND
VTTPWRGOOD_R
SN74AHC1G08DBV
SOT23_5

+V3_3S
CX33 0.1uF/10V,X5R
VTTPWRGOOD_R
{37,64} V1_05S_PWROK
UX2
RX42 2K 1%
VTTPWRGOOD
RX43 931 1% 0402
ns
74LVC1G17GW

Clarksfield: 1.1V(RX41=2K 1%; RX44=1K 1%)
Arrandale : 1.05V(RX41=2K 1% ; R44=931ohm 1%)

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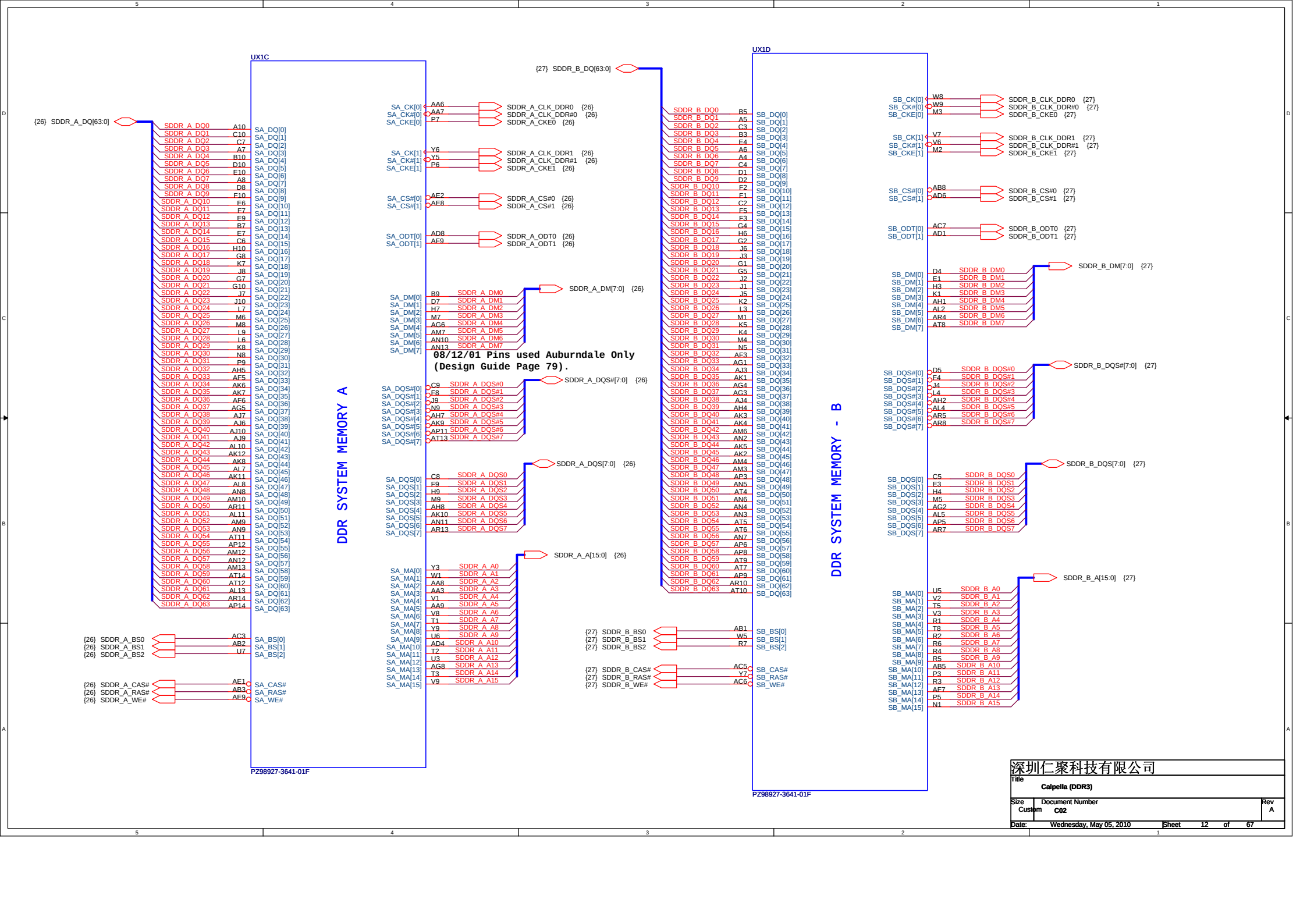
Title	Calpella (CLK,MISC,JTAG)	
Size: Custom	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 11 of 67	


UX1C
DDR SYSTEM MEMORY A
PZ98927-3641-01F
{26} SDDR_A_DQ[63:0]
SDDR_A_DQ0 A10
SDDR_A_DQ1 C10
SDDR_A_DQ2 C7
SDDR_A_DQ3 A7
SDDR_A_DQ4 B10
SDDR_A_DQ5 D10
SDDR_A_DQ6 E10
SDDR_A_DQ7 A8
SDDR_A_DQ8 D8
SDDR_A_DQ9 F10
SDDR_A_DQ10 F6
SDDR_A_DQ11 E7
SDDR_A_DQ12 E9
SDDR_A_DQ13 B7
SDDR_A_DQ14 E7
SDDR_A_DQ15 C6
SDDR_A_DQ16 H10
SDDR_A_DQ17 G8
SDDR_A_DQ18 K7
SDDR_A_DQ19 J8
SDDR_A_DQ20 G7
SDDR_A_DQ21 G10
SDDR_A_DQ22 J7
SDDR_A_DQ23 J10
SDDR_A_DQ24 L7
SDDR_A_DQ25 M6
SDDR_A_DQ26 M8
SDDR_A_DQ27 L9
SDDR_A_DQ28 L6
SDDR_A_DQ29 K8
SDDR_A_DQ30 N8
SDDR_A_DQ31 P9
SDDR_A_DQ32 AH5
SDDR_A_DQ33 AF5
SDDR_A_DQ34 AK6
SDDR_A_DQ35 AK7
SDDR_A_DQ36 AF6
SDDR_A_DQ37 AG5
SDDR_A_DQ38 AJ7
SDDR_A_DQ39 AJ6
SDDR_A_DQ40 AJ10
SDDR_A_DQ41 AJ9
SDDR_A_DQ42 AL10
SDDR_A_DQ43 AK12
SDDR_A_DQ44 AK8
SDDR_A_DQ45 AL7
SDDR_A_DQ46 AK11
SDDR_A_DQ47 AL8
SDDR_A_DQ48 AN8
SDDR_A_DQ49 AM10
SDDR_A_DQ50 AR11
SDDR_A_DQ51 AL11
SDDR_A_DQ52 AM9
SDDR_A_DQ53 AN9
SDDR_A_DQ54 AT11
SDDR_A_DQ55 AP12
SDDR_A_DQ56 AM12
SDDR_A_DQ57 AN12
SDDR_A_DQ58 AM13
SDDR_A_DQ59 AT14
SDDR_A_DQ60 AT12
SDDR_A_DQ61 AL13
SDDR_A_DQ62 AR14
SDDR_A_DQ63 AP14
SA_DQ[0]
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SA_DQ[57]
SA_DQ[58]
SA_DQ[59]
SA_DQ[60]
SA_DQ[61]
SA_DQ[62]
SA_DQ[63]
{26} SDDR_A_BS0
{26} SDDR_A_BS1
{26} SDDR_A_BS2
AC3
AB2
U7
SA_BS[0]
SA_BS[1]
SA_BS[2]
{26} SDDR_A_CAS#
{26} SDDR_A_RAS#
{26} SDDR_A_WE#
AE1
AB3
AE9
SA_CAS#
SA_RAS#
SA_WE#
SA_CK[0]
SA_CK#[0]
SA_CKE[0]
AA6
AA7
P7
SDDR_A_CLK_DDR0 {26}
SDDR_A_CLK_DDR#0 {26}
SDDR_A_CKE0 {26}
SA_CK[1]
SA_CK#[1]
SA_CKE[1]
Y6
Y5
P6
SDDR_A_CLK_DDR1 {26}
SDDR_A_CLK_DDR#1 {26}
SDDR_A_CKE1 {26}
SA_CS#[0]
SA_CS#[1]
AE2
AE8
SDDR_A_CS#0 {26}
SDDR_A_CS#1 {26}
SA_ODT[0]
SA_ODT[1]
AD8
AF9
SDDR_A_ODT0 {26}
SDDR_A_ODT1 {26}
SA_DM[0]
SA_DM[1]
SA_DM[2]
SA_DM[3]
SA_DM[4]
SA_DM[5]
SA_DM[6]
SA_DM[7]
B9 SDDR_A_DM0
D7 SDDR_A_DM1
H7 SDDR_A_DM2
M7 SDDR_A_DM3
AG6 SDDR_A_DM4
AM7 SDDR_A_DM5
AN10 SDDR_A_DM6
AN13 SDDR_A_DM7
SDDR_A_DM[7:0] {26}
08/12/01 Pins used Auburndale Only
(Design Guide Page 79).
SA_DQS[0]
SA_DQS[1]
SA_DQS[2]
SA_DQS[3]
SA_DQS[4]
SA_DQS[5]
SA_DQS[6]
SA_DQS[7]
C9 SDDR_A_DQS#0
E8 SDDR_A_DQS#1
J9 SDDR_A_DQS#2
N9 SDDR_A_DQS#3
AH7 SDDR_A_DQS#4
AK9 SDDR_A_DQS#5
AP11 SDDR_A_DQS#6
AT13 SDDR_A_DQS#7
SDDR_A_DQS#[7:0] {26}
SA_DQS[0]
SA_DQS[1]
SA_DQS[2]
SA_DQS[3]
SA_DQS[4]
SA_DQS[5]
SA_DQS[6]
SA_DQS[7]
C8 SDDR_A_DQS0
F9 SDDR_A_DQS1
H9 SDDR_A_DQS2
M9 SDDR_A_DQS3
AH8 SDDR_A_DQS4
AK10 SDDR_A_DQS5
AN11 SDDR_A_DQS6
AR13 SDDR_A_DQS7
SDDR_A_DQS[7:0] {26}
SA_MA[0]
SA_MA[1]
SA_MA[2]
SA_MA[3]
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SA_MA[7]
SA_MA[8]
SA_MA[9]
SA_MA[10]
SA_MA[11]
SA_MA[12]
SA_MA[13]
SA_MA[14]
SA_MA[15]
Y3 SDDR_A_A0
W1 SDDR_A_A1
AA8 SDDR_A_A2
AA3 SDDR_A_A3
V1 SDDR_A_A4
AA9 SDDR_A_A5
V8 SDDR_A_A6
T1 SDDR_A_A7
Y9 SDDR_A_A8
U6 SDDR_A_A9
AD4 SDDR_A_A10
T2 SDDR_A_A11
U3 SDDR_A_A12
AG8 SDDR_A_A13
T3 SDDR_A_A14
V9 SDDR_A_A15
SDDR_A_A[15:0] {26}
UX1D
DDR SYSTEM MEMORY - B
PZ98927-3641-01F
{27} SDDR_B_DQ[63:0]
SDDR_B_DQ0 B5
SDDR_B_DQ1 A5
SDDR_B_DQ2 C3
SDDR_B_DQ3 B3
SDDR_B_DQ4 E4
SDDR_B_DQ5 A6
SDDR_B_DQ6 A4
SDDR_B_DQ7 C4
SDDR_B_DQ8 D1
SDDR_B_DQ9 D2
SDDR_B_DQ10 F2
SDDR_B_DQ11 F1
SDDR_B_DQ12 C2
SDDR_B_DQ13 F5
SDDR_B_DQ14 F3
SDDR_B_DQ15 G4
SDDR_B_DQ16 H6
SDDR_B_DQ17 G2
SDDR_B_DQ18 J6
SDDR_B_DQ19 J3
SDDR_B_DQ20 G1
SDDR_B_DQ21 G5
SDDR_B_DQ22 J2
SDDR_B_DQ23 J1
SDDR_B_DQ24 J5
SDDR_B_DQ25 K2
SDDR_B_DQ26 L3
SDDR_B_DQ27 M1
SDDR_B_DQ28 K5
SDDR_B_DQ29 K4
SDDR_B_DQ30 M4
SDDR_B_DQ31 N5
SDDR_B_DQ32 AF3
SDDR_B_DQ33 AG1
SDDR_B_DQ34 AJ3
SDDR_B_DQ35 AK1
SDDR_B_DQ36 AG4
SDDR_B_DQ37 AG3
SDDR_B_DQ38 AJ4
SDDR_B_DQ39 AH4
SDDR_B_DQ40 AK3
SDDR_B_DQ41 AK4
SDDR_B_DQ42 AM6
SDDR_B_DQ43 AN2
SDDR_B_DQ44 AK5
SDDR_B_DQ45 AK2
SDDR_B_DQ46 AM4
SDDR_B_DQ47 AM3
SDDR_B_DQ48 AP3
SDDR_B_DQ49 AN5
SDDR_B_DQ50 AT4
SDDR_B_DQ51 AN6
SDDR_B_DQ52 AN4
SDDR_B_DQ53 AN3
SDDR_B_DQ54 AT5
SDDR_B_DQ55 AT6
SDDR_B_DQ56 AN7
SDDR_B_DQ57 AP6
SDDR_B_DQ58 AP8
SDDR_B_DQ59 AT9
SDDR_B_DQ60 AT7
SDDR_B_DQ61 AP9
SDDR_B_DQ62 AR10
SDDR_B_DQ63 AT10
SB_DQ[0]
SB_DQ[1]
SB_DQ[2]
SB_DQ[3]
SB_DQ[4]
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SB_DQ[8]
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SB_DQ[10]
SB_DQ[11]
SB_DQ[12]
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SB_DQ[48]
SB_DQ[49]
SB_DQ[50]
SB_DQ[51]
SB_DQ[52]
SB_DQ[53]
SB_DQ[54]
SB_DQ[55]
SB_DQ[56]
SB_DQ[57]
SB_DQ[58]
SB_DQ[59]
SB_DQ[60]
SB_DQ[61]
SB_DQ[62]
SB_DQ[63]
{27} SDDR_B_BS0
{27} SDDR_B_BS1
{27} SDDR_B_BS2
AB1
W5
R7
SB_BS[0]
SB_BS[1]
SB_BS[2]
{27} SDDR_B_CAS#
{27} SDDR_B_RAS#
{27} SDDR_B_WE#
AC5
Y7
AC6
SB_CAS#
SB_RAS#
SB_WE#
SB_CK[0]
SB_CK#[0]
SB_CKE[0]
W8
W9
M3
SDDR_B_CLK_DDR0 {27}
SDDR_B_CLK_DDR#0 {27}
SDDR_B_CKE0 {27}
SB_CK[1]
SB_CK#[1]
SB_CKE[1]
V7
V6
M2
SDDR_B_CLK_DDR1 {27}
SDDR_B_CLK_DDR#1 {27}
SDDR_B_CKE1 {27}
SB_CS#[0]
SB_CS#[1]
AB8
AD6
SDDR_B_CS#0 {27}
SDDR_B_CS#1 {27}
SB_ODT[0]
SB_ODT[1]
AC7
AD1
SDDR_B_ODT0 {27}
SDDR_B_ODT1 {27}
SB_DM[0]
SB_DM[1]
SB_DM[2]
SB_DM[3]
SB_DM[4]
SB_DM[5]
SB_DM[6]
SB_DM[7]
D4 SDDR_B_DM0
E1 SDDR_B_DM1
H3 SDDR_B_DM2
K1 SDDR_B_DM3
AH1 SDDR_B_DM4
AL2 SDDR_B_DM5
AR4 SDDR_B_DM6
AT8 SDDR_B_DM7
SDDR_B_DM[7:0] {27}
SB_DQS#[0]
SB_DQS#[1]
SB_DQS#[2]
SB_DQS#[3]
SB_DQS#[4]
SB_DQS#[5]
SB_DQS#[6]
SB_DQS#[7]
D5 SDDR_B_DQS#0
F4 SDDR_B_DQS#1
J4 SDDR_B_DQS#2
L4 SDDR_B_DQS#3
AH2 SDDR_B_DQS#4
AL4 SDDR_B_DQS#5
AR5 SDDR_B_DQS#6
AR8 SDDR_B_DQS#7
SDDR_B_DQS#[7:0] {27}
SB_DQS[0]
SB_DQS[1]
SB_DQS[2]
SB_DQS[3]
SB_DQS[4]
SB_DQS[5]
SB_DQS[6]
SB_DQS[7]
C5 SDDR_B_DQS0
E3 SDDR_B_DQS1
H4 SDDR_B_DQS2
M5 SDDR_B_DQS3
AG2 SDDR_B_DQS4
AL5 SDDR_B_DQS5
AP5 SDDR_B_DQS6
AR7 SDDR_B_DQS7
SDDR_B_DQS[7:0] {27}
SB_MA[0]
SB_MA[1]
SB_MA[2]
SB_MA[3]
SB_MA[4]
SB_MA[5]
SB_MA[6]
SB_MA[7]
SB_MA[8]
SB_MA[9]
SB_MA[10]
SB_MA[11]
SB_MA[12]
SB_MA[13]
SB_MA[14]
SB_MA[15]
U5 SDDR_B_A0
V2 SDDR_B_A1
T5 SDDR_B_A2
V3 SDDR_B_A3
R1 SDDR_B_A4
T8 SDDR_B_A5
R2 SDDR_B_A6
R6 SDDR_B_A7
R4 SDDR_B_A8
R5 SDDR_B_A9
AB5 SDDR_B_A10
P3 SDDR_B_A11
R3 SDDR_B_A12
AF7 SDDR_B_A13
P5 SDDR_B_A14
N1 SDDR_B_A15
SDDR_B_A[15:0] {27}
深圳仁聚科技有限公司
Title
Calpella (DDR3)
Size Custom
Document Number C02
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Date: Wednesday, May 05, 2010
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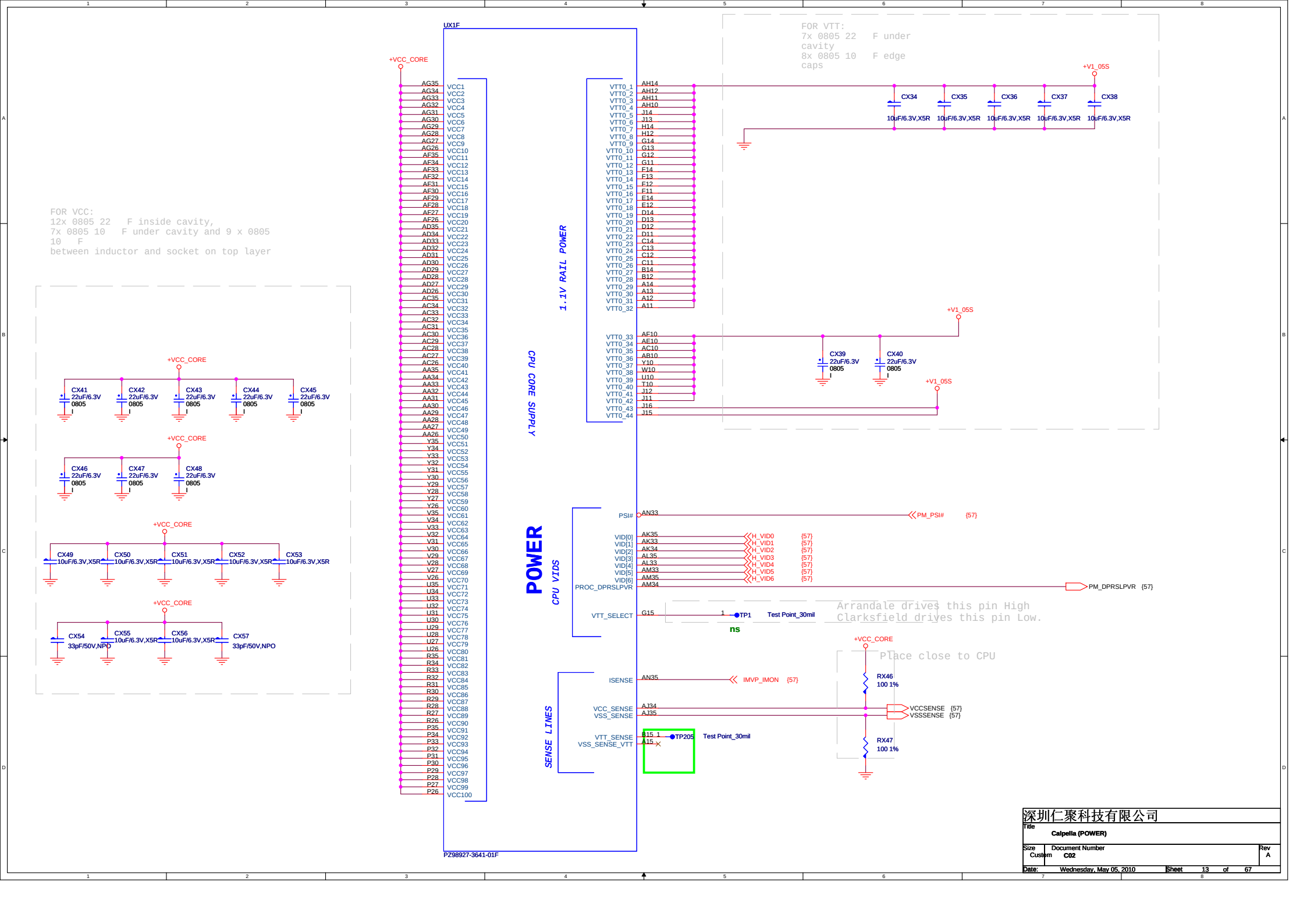

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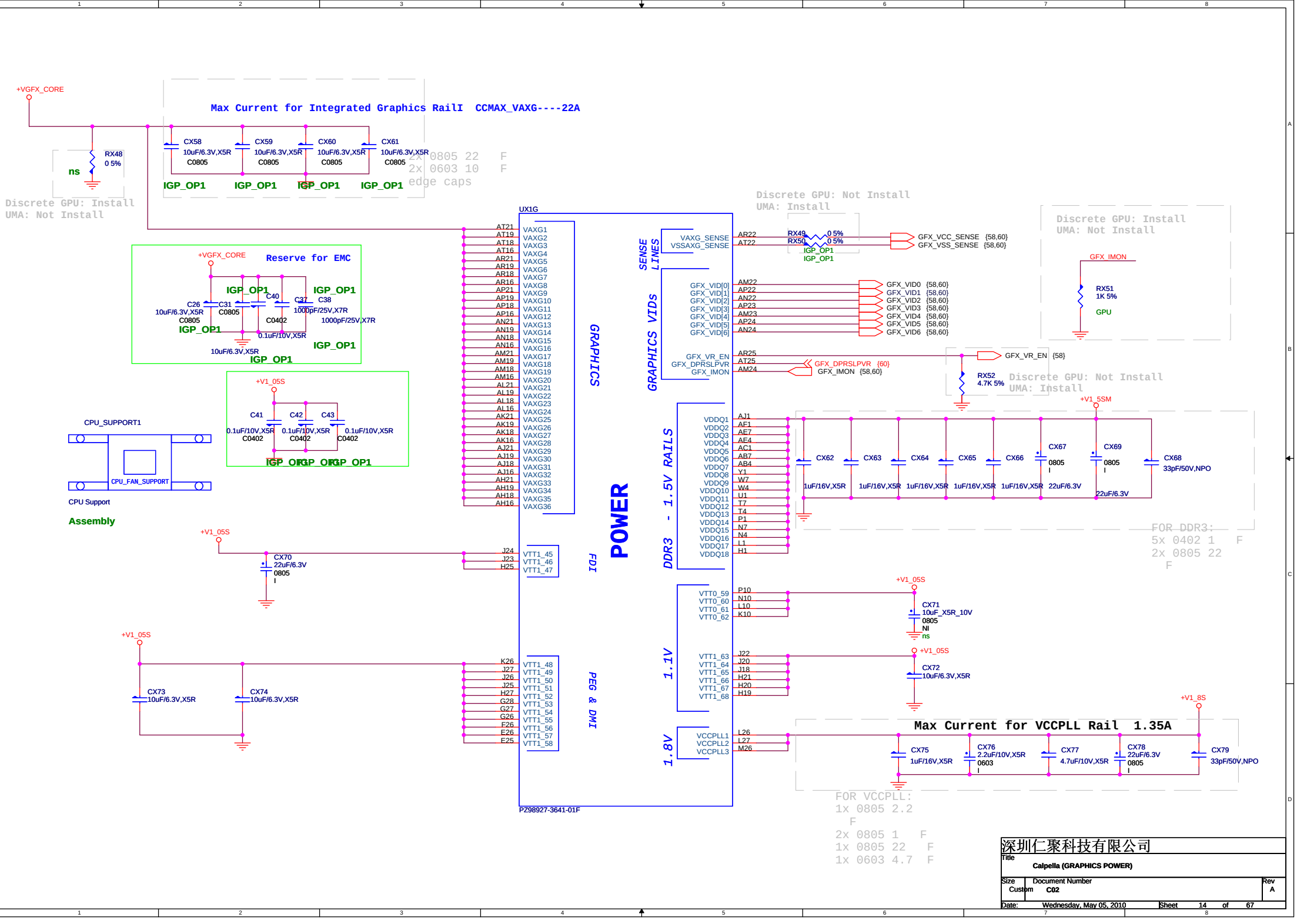
Title	Calpella (POWER)	
Size: Custom	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 13 of 67	


Max Current for Integrated Graphics RailI CCMAX_VAXG----22A
+VGFX_CORE
RX48 0 5%
ns
CX58 10uF/6.3V,X5R C0805
CX59 10uF/6.3V,X5R C0805
CX60 10uF/6.3V,X5R C0805
CX61 10uF/6.3V,X5R C0805
IGP_OP1
2x 0805 22 F
2x 0603 10 F
edge caps
Discrete GPU: Install
UMA: Not Install
Reserve for EMC
C26 10uF/6.3V,X5R C0805
C31 C0805
C40 C0402
C37 1000pF/25V,X7R
C38 1000pF/25V,X7R
0.1uF/10V,X5R
10uF/6.3V,X5R
C41 C42 C43 0.1uF/10V,X5R C0402
CPU_SUPPORT1
CPU_FAN_SUPPORT
CPU Support
Assembly
UX1G
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36
GRAPHICS
POWER
FDI
PEG & DMI
DDR3 - 1.5V RAILS
1.1V
1.8V
SENSE LINES
GRAPHICS VIDS
VAXG_SENSE VSSAXG_SENSE
GFX_VCC_SENSE {58,60}
GFX_VSS_SENSE {58,60}
GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6]
GFX_VR_EN
GFX_DPRSLPVR {60}
GFX_IMON {58,60}
Discrete GPU: Not Install
UMA: Install
GFX_IMON
RX51 1K 5%
GPU
RX52 4.7K 5%
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18
CX62 CX63 CX64 CX65 CX66 CX67 CX69 CX68
1uF/16V,X5R
22uF/6.3V
33pF/50V,NPO
FOR DDR3:
5x 0402 1 F
2x 0805 22 F
VTT0_59 VTT0_60 VTT0_61 VTT0_62
CX71 10uF_X5R_10V 0805 NI ns
VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68
CX72 10uF/6.3V,X5R
Max Current for VCCPLL Rail 1.35A
VCCPLL1 VCCPLL2 VCCPLL3
CX75 1uF/16V,X5R
CX76 2.2uF/10V,X5R 0603
CX77 4.7uF/10V,X5R
CX78 22uF/6.3V 0805
CX79 33pF/50V,NPO
FOR VCCPLL:
1x 0805 2.2 F
2x 0805 1 F
1x 0805 22 F
1x 0603 4.7 F
CX70 22uF/6.3V 0805
CX73 10uF/6.3V,X5R
CX74 10uF/6.3V,X5R
VTT1_45 VTT1_46 VTT1_47
VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58
PZ98927-3641-01F
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Title
Calpella (GRAPHICS POWER)
Size Custom
Document Number C02
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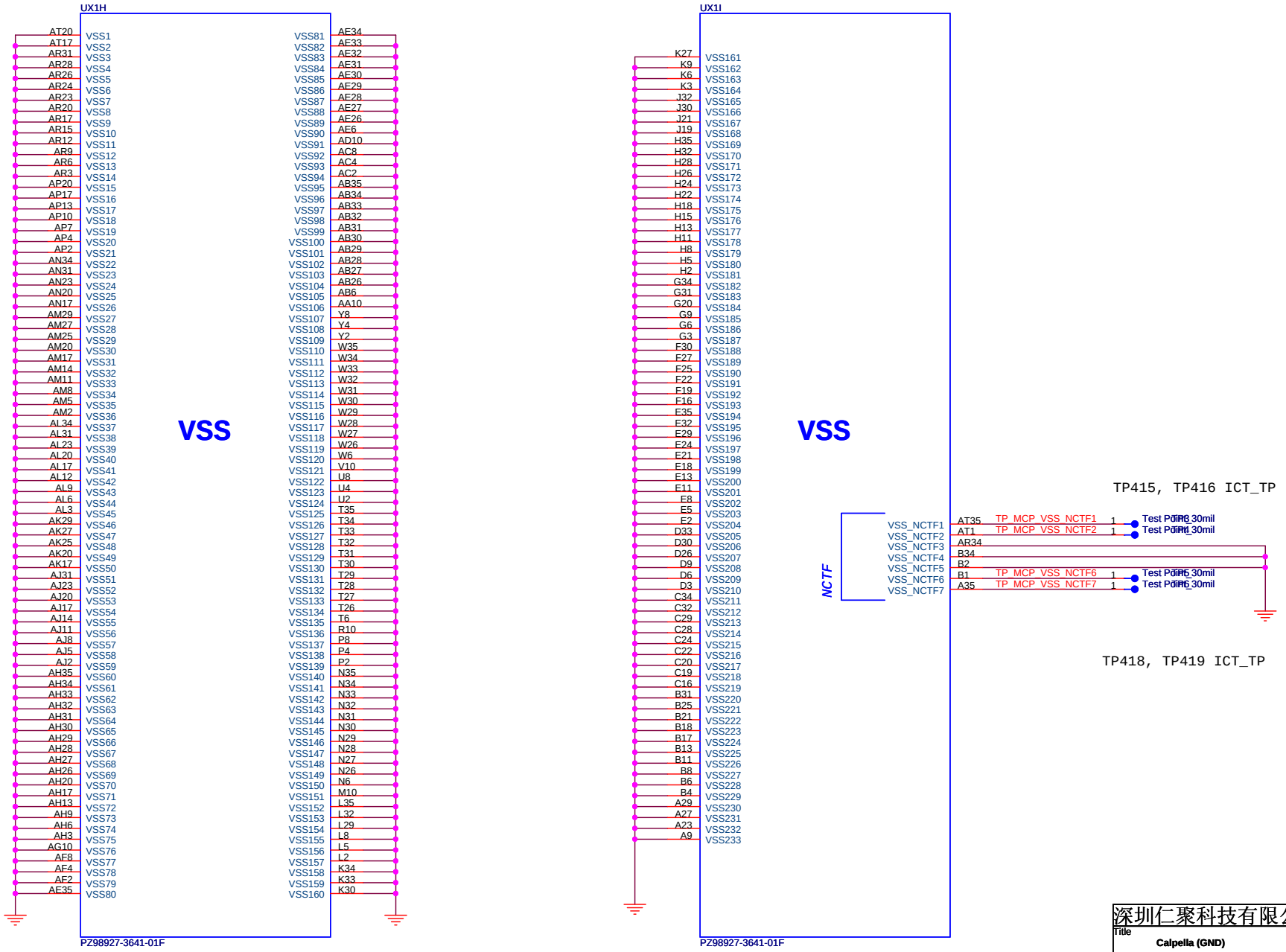

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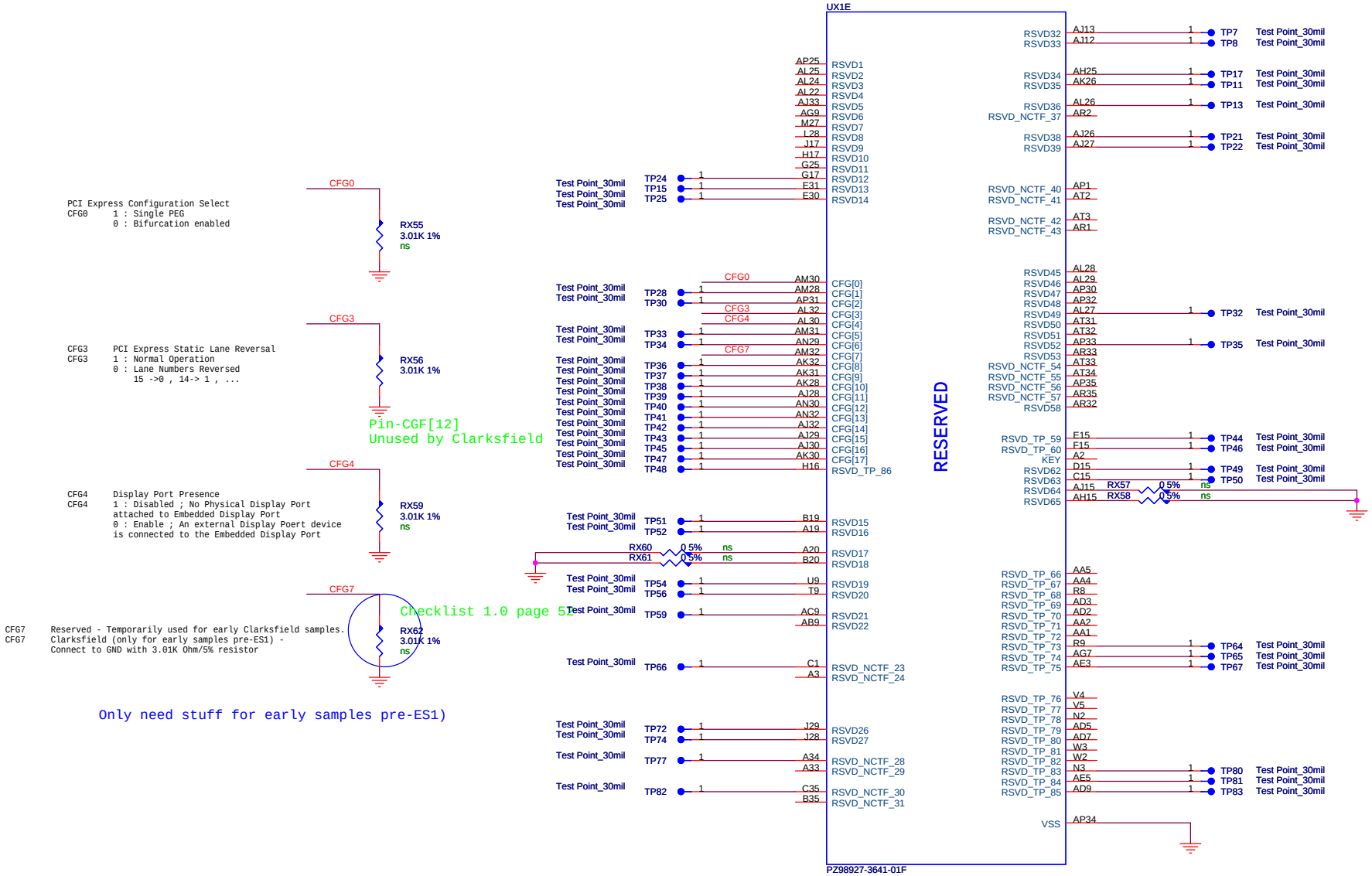
Title: Calpella (GND)		
Size: B	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 15 of 67	



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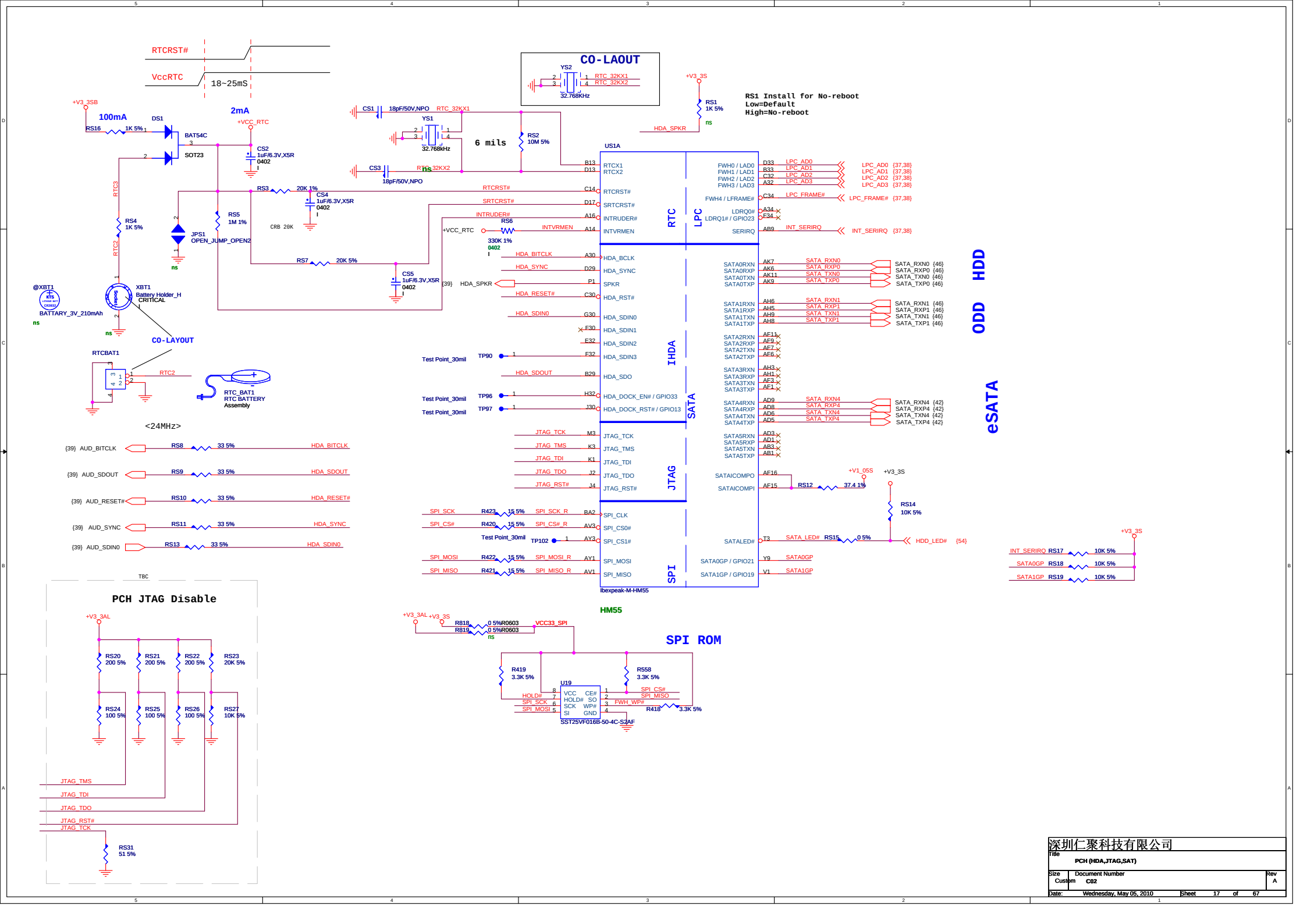
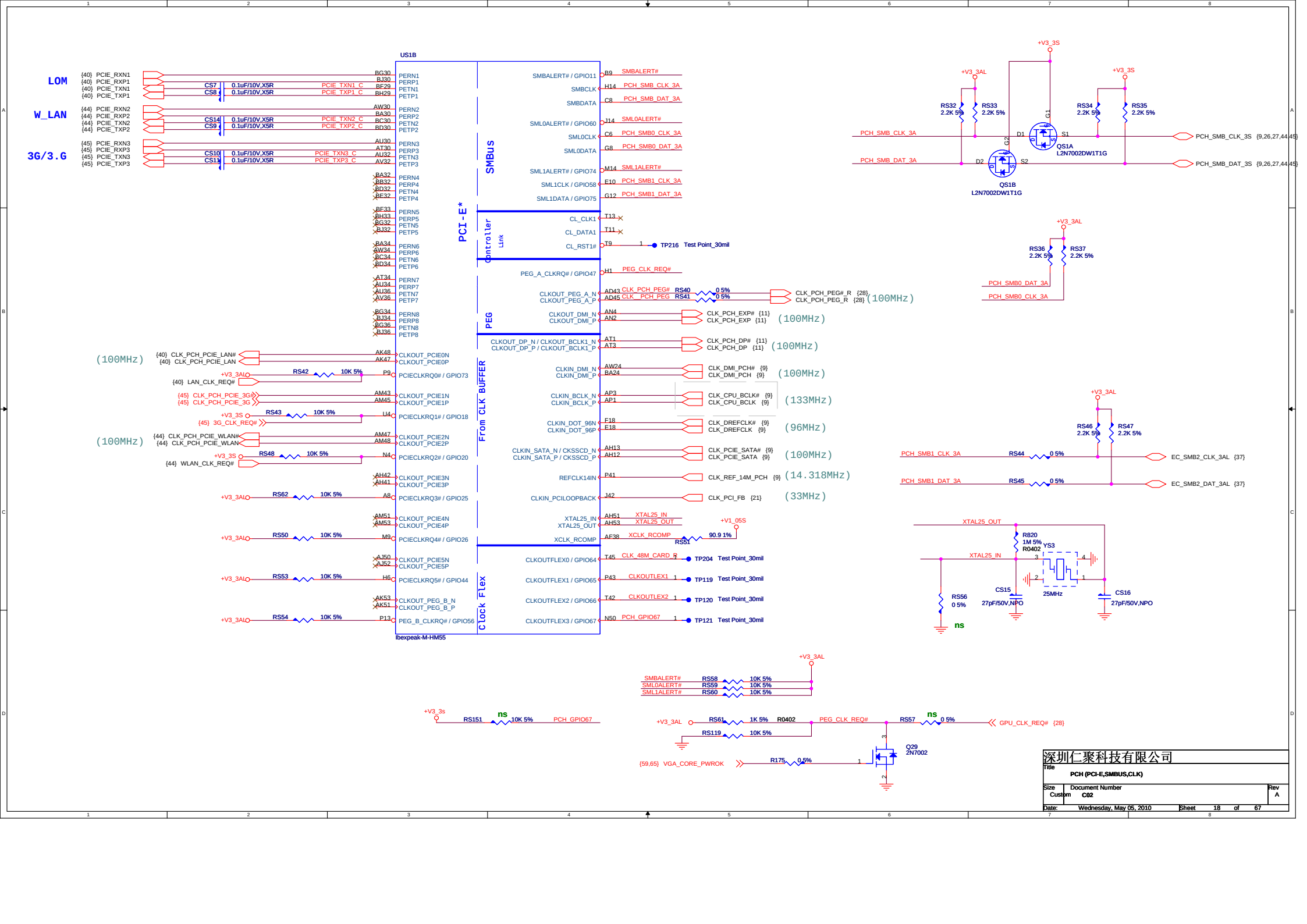
Title: Calpella (RESERVED)			
Size: Custom	Document Number: C02		Rev: A
Date: Wednesday, May 05, 2010	Sheet 16 of 67		



深圳仁聚科技有限公司			
Title: PCH (HDA,JTAG,SAT)			
Size: Custom	Document Number: C02		Rev: A
Date: Wednesday, May 05, 2010	Sheet 17 of 67		


US1B
LOM
{40} PCIE_RXN1
{40} PCIE_RXP1
{40} PCIE_TXN1
{40} PCIE_TXP1
CS7 0.1uF/10V,X5R PCIE_TXN1_C
CS8 0.1uF/10V,X5R PCIE_TXP1_C
W_LAN
{44} PCIE_RXN2
{44} PCIE_RXP2
{44} PCIE_TXN2
{44} PCIE_TXP2
CS14 0.1uF/10V,X5R PCIE_TXN2_C
CS9 0.1uF/10V,X5R PCIE_TXP2_C
3G/3.G
{45} PCIE_RXN3
{45} PCIE_RXP3
{45} PCIE_TXN3
{45} PCIE_TXP3
CS10 0.1uF/10V,X5R PCIE_TXN3_C
CS11 0.1uF/10V,X5R PCIE_TXP3_C
PCI-E*
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8
SMBus
SMBALERT# / GPIO11 B9 SMBALERT#
SMBCLK H14 PCH_SMB_CLK_3A
SMBDATA C8 PCH_SMB_DAT_3A
SML0ALERT# / GPIO60 J14 SML0ALERT#
SML0CLK C6 PCH_SMB0_CLK_3A
SML0DATA G8 PCH_SMB0_DAT_3A
SML1ALERT# / GPIO74 M14 SML1ALERT#
SML1CLK / GPIO58 E10 PCH_SMB1_CLK_3A
SML1DATA / GPIO75 G12 PCH_SMB1_DAT_3A
Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9 TP216 Test Point_30mil
PEG
PEG_A_CLKRQ# / GPIO47 H1 PEG_CLK_REQ#
CLKOUT_PEG_A_N AD43 CLK_PCH_PEG# RS40 0 5% CLK_PCH_PEG#_R {28}
CLKOUT_PEG_A_P AD45 CLK_PCH_PEG RS41 0 5% CLK_PCH_PEG_R {28} (100MHz)
CLKOUT_DMI_N AN4 CLK_PCH_EXP# {11}
CLKOUT_DMI_P AN2 CLK_PCH_EXP {11} (100MHz)
CLKOUT_DP_N / CLKOUT_BCLK1_N AT1 CLK_PCH_DP# {11}
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3 CLK_PCH_DP {11} (100MHz)
From CLK BUFFER
CLKIN_DMI_N AW24 CLK_DMI_PCH# {9}
CLKIN_DMI_P BA24 CLK_DMI_PCH {9} (100MHz)
CLKIN_BCLK_N AP3 CLK_CPU_BCLK# {9}
CLKIN_BCLK_P AP1 CLK_CPU_BCLK {9} (133MHz)
CLKIN_DOT_96N F18 CLK_DREFCLK# {9}
CLKIN_DOT_96P E18 CLK_DREFCLK {9} (96MHz)
CLKIN_SATA_N / CKSSCD_N AH13 CLK_PCIE_SATA# {9}
CLKIN_SATA_P / CKSSCD_P AH12 CLK_PCIE_SATA {9} (100MHz)
REFCLK14IN P41 CLK_REF_14M_PCH {9} (14.318MHz)
CLKIN_PCILOOPBACK J42 CLK_PCI_FB {21} (33MHz)
XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
+V1_05S
XCLK_RCOMP AF38 XCLK_RCOMP 90.9 1% RS51
Clock Flex
CLKOUTFLEX0 / GPIO64 T45 CLK_48M_CARD_R TP204 Test Point_30mil
CLKOUTFLEX1 / GPIO65 P43 CLKOUTLEX1 TP119 Test Point_30mil
CLKOUTFLEX2 / GPIO66 T42 CLKOUTLEX2 TP120 Test Point_30mil
CLKOUTFLEX3 / GPIO67 N50 PCH_GPIO67 TP121 Test Point_30mil
CLKOUT_PCIE0N AK48
CLKOUT_PCIE0P AK47
PCIECLKRQ0# / GPIO73 P9
CLKOUT_PCIE1N AM43
CLKOUT_PCIE1P AM45
PCIECLKRQ1# / GPIO18 U4
CLKOUT_PCIE2N AM47
CLKOUT_PCIE2P AM48
PCIECLKRQ2# / GPIO20 N4
CLKOUT_PCIE3N AH42
CLKOUT_PCIE3P AH41
PCIECLKRQ3# / GPIO25 A8
CLKOUT_PCIE4N AM51
CLKOUT_PCIE4P AM53
PCIECLKRQ4# / GPIO26 M9
CLKOUT_PCIE5N AJ50
CLKOUT_PCIE5P AJ52
PCIECLKRQ5# / GPIO44 H6
CLKOUT_PEG_B_N AK53
CLKOUT_PEG_B_P AK51
PEG_B_CLKRQ# / GPIO56 P13
(100MHz) {40} CLK_PCH_PCIE_LAN# {40} CLK_PCH_PCIE_LAN
+V3_3AL RS42 10K 5% {40} LAN_CLK_REQ#
{45} CLK_PCH_PCIE_3G# {45} CLK_PCH_PCIE_3G
+V3_3S RS43 10K 5% {45} 3G_CLK_REQ#
(100MHz) {44} CLK_PCH_PCIE_WLAN# {44} CLK_PCH_PCIE_WLAN
+V3_3S RS48 10K 5% {44} WLAN_CLK_REQ#
+V3_3AL RS62 10K 5%
+V3_3AL RS50 10K 5%
+V3_3AL RS53 10K 5%
+V3_3AL RS54 10K 5%
Ibexpeak-M-HM55
+V3_3S
+V3_3AL
RS32 2.2K 5%
RS33 2.2K 5%
RS34 2.2K 5%
RS35 2.2K 5%
PCH_SMB_CLK_3A
PCH_SMB_DAT_3A
QS1A L2N7002DW1T1G
QS1B L2N7002DW1T1G
PCH_SMB_CLK_3S {9,26,27,44,45}
PCH_SMB_DAT_3S {9,26,27,44,45}
RS36 2.2K 5%
RS37 2.2K 5%
PCH_SMB0_DAT_3A
PCH_SMB0_CLK_3A
RS46 2.2K 5%
RS47 2.2K 5%
PCH_SMB1_CLK_3A
PCH_SMB1_DAT_3A
RS44 0 5%
RS45 0 5%
EC_SMB2_CLK_3AL {37}
EC_SMB2_DAT_3AL {37}
XTAL25_OUT
R820 1M 5% R0402
YS3
XTAL25_IN
25MHz
CS15 27pF/50V,NPO
CS16 27pF/50V,NPO
RS56 0 5%
ns
SMBALERT# RS58 10K 5%
SML0ALERT# RS59 10K 5%
SML1ALERT# RS60 10K 5%
+V3_3s
RS151 ns 10K 5% PCH_GPIO67
+V3_3AL RS61 1K 5% R0402
RS119 10K 5%
PEG_CLK_REQ#
RS57 ns 0 5% GPU_CLK_REQ# {28}
{59,65} VGA_CORE_PWROK
R175 0.5%
Q29 2N7002
深圳仁聚科技有限公司
Title PCH (PCI-E,SMBUS,CLK)
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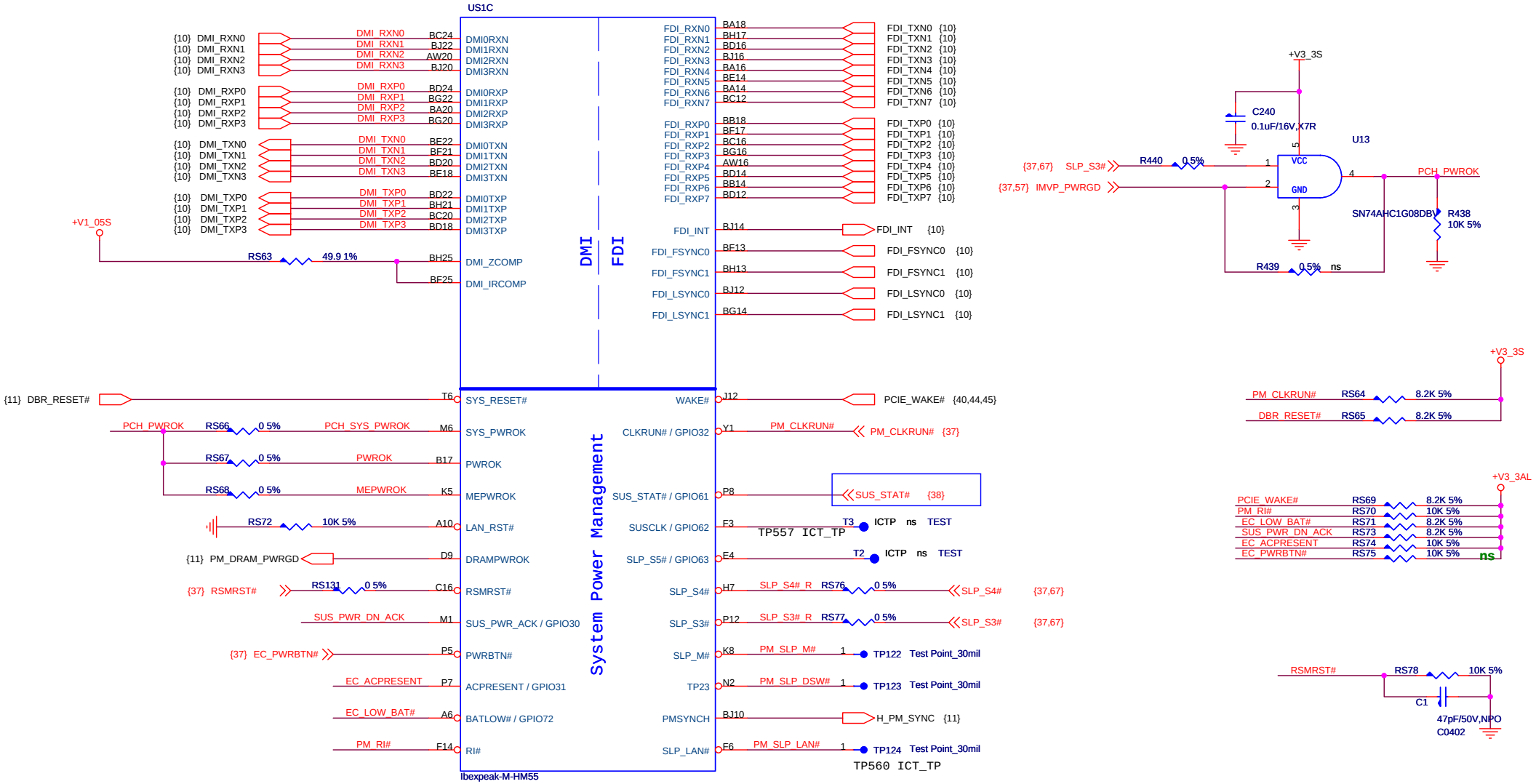

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Title: PCH (DMI,FDI,GPIO)		
Size: B	Document Number: C02	Rev: A
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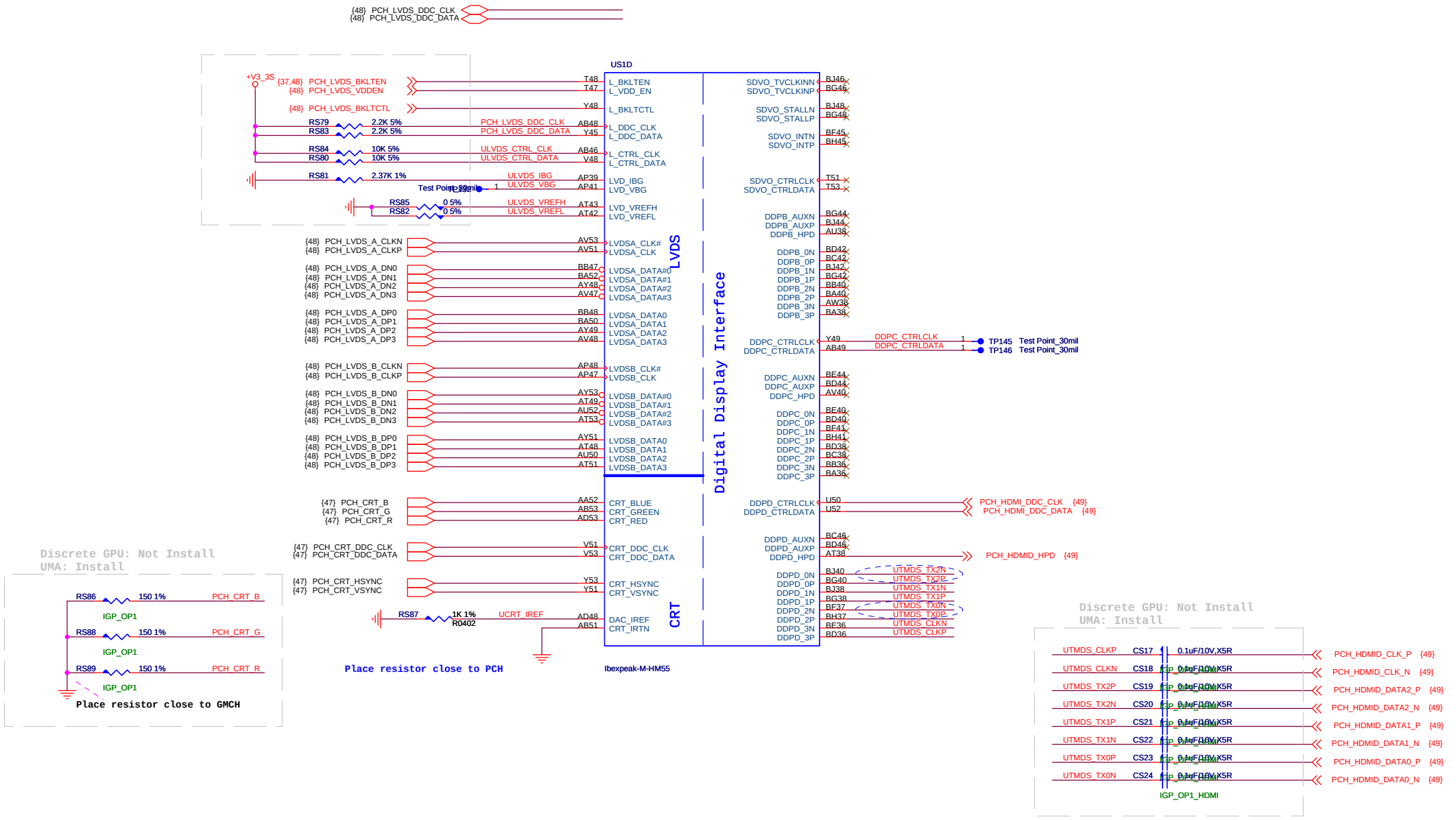

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Title	PCH (LVDS,DDI)	
Size: Custom	Document Number: C02	Rev: A
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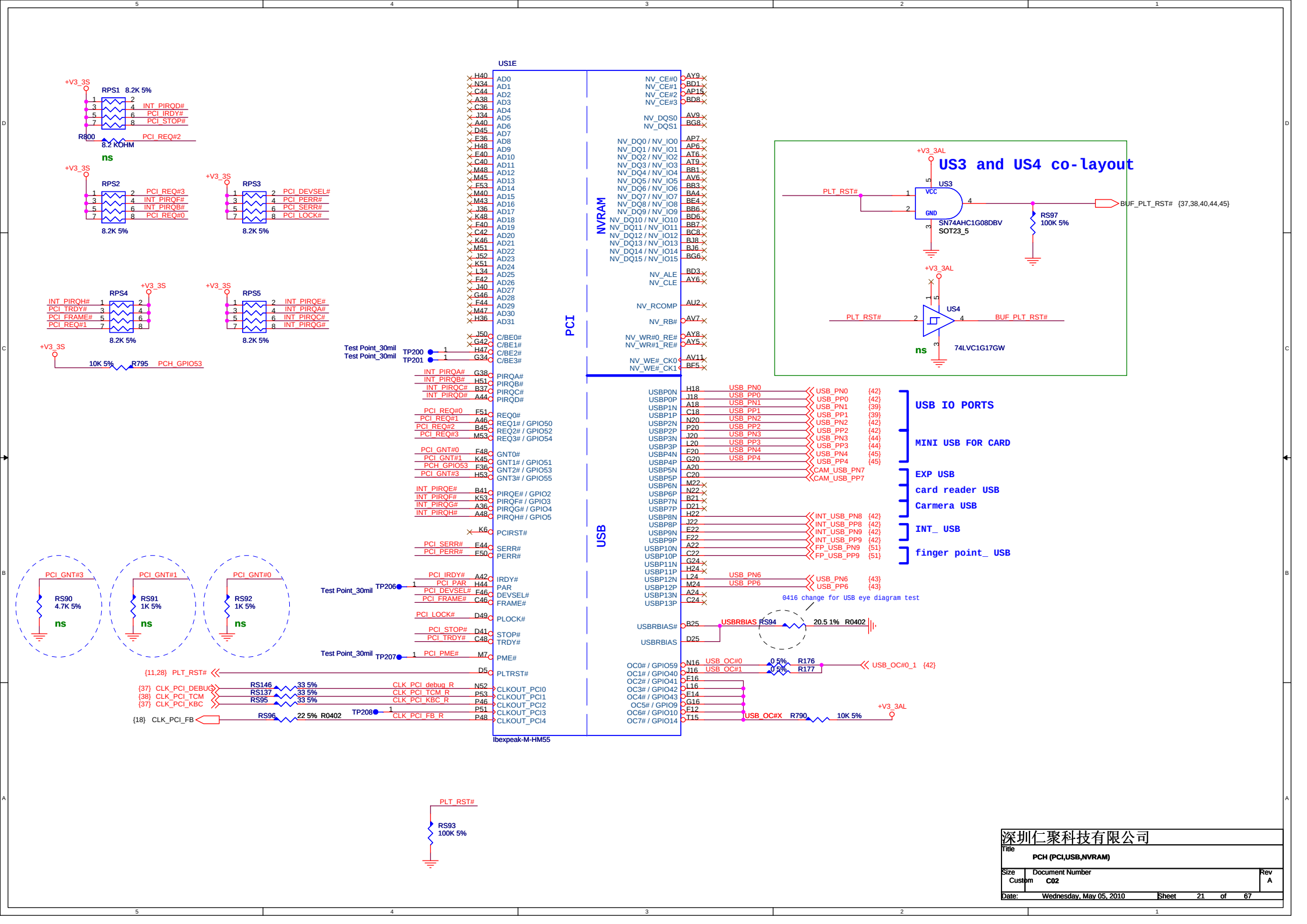
US1E
PCI
NVRAM
USB
Ibexpeak-M-HM55
RPS1 8.2K 5%
INT_PIRQD#
PCI_IRDY#
PCI_STOP#
PCI_REQ#2
R800
8.2 KOHM
ns
RPS2
PCI_REQ#3
INT_PIRQF#
INT_PIRQB#
PCI_REQ#0
8.2K 5%
RPS3
PCI_DEVSEL#
PCI_PERR#
PCI_SERR#
PCI_LOCK#
RPS4
INT_PIRQH#
PCI_TRDY#
PCI_FRAME#
PCI_REQ#1
RPS5
INT_PIRQE#
INT_PIRQA#
INT_PIRQC#
INT_PIRQG#
10K 5%
R795
PCH_GPIO53
Test Point_30mil
TP200
TP201
C/BE0#
C/BE1#
C/BE2#
C/BE3#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
REQ0#
REQ1# / GPIO50
REQ2# / GPIO52
REQ3# / GPIO54
GNT0#
GNT1# / GPIO51
GNT2# / GPIO53
GNT3# / GPIO55
PIRQE# / GPIO2
PIRQF# / GPIO3
PIRQG# / GPIO4
PIRQH# / GPIO5
PCIRST#
SERR#
PERR#
IRDY#
PAR
DEVSEL#
FRAME#
PLOCK#
STOP#
TRDY#
PME#
PLTRST#
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
TP206
TP207
TP208
PCI_GNT#3
PCI_GNT#1
PCI_GNT#0
RS90 4.7K 5%
RS91 1K 5%
RS92 1K 5%
{11,28} PLT_RST#
{37} CLK_PCI_DEBUG
{38} CLK_PCI_TCM
{37} CLK_PCI_KBC
{18} CLK_PCI_FB
RS146
RS137
RS95
RS96
33 5%
22 5%
R0402
CLK_PCI_debug_R
CLK_PCI_TCM_R
CLK_PCI_KBC_R
CLK_PCI_FB_R
NV_CE#0
NV_CE#1
NV_CE#2
NV_CE#3
NV_DQS0
NV_DQS1
NV_DQ0 / NV_IO0
NV_DQ1 / NV_IO1
NV_DQ2 / NV_IO2
NV_DQ3 / NV_IO3
NV_DQ4 / NV_IO4
NV_DQ5 / NV_IO5
NV_DQ6 / NV_IO6
NV_DQ7 / NV_IO7
NV_DQ8 / NV_IO8
NV_DQ9 / NV_IO9
NV_DQ10 / NV_IO10
NV_DQ11 / NV_IO11
NV_DQ12 / NV_IO12
NV_DQ13 / NV_IO13
NV_DQ14 / NV_IO14
NV_DQ15 / NV_IO15
NV_ALE
NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE#
NV_WR#1_RE#
NV_WE#_CK0
NV_WE#_CK1
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
USBRBIAS#
USBRBIAS
USB_PN0
USB_PP0
USB_PN1
USB_PP1
USB_PN2
USB_PP2
USB_PN3
USB_PP3
USB_PN4
USB_PP4
CAM_USB_PN7
CAM_USB_PP7
INT_USB_PN8
INT_USB_PP8
INT_USB_PN9
INT_USB_PP9
FP_USB_PN9
FP_USB_PP9
USB_PN6
USB_PP6
USBRBIAS RS94
20.5 1% R0402
0416 change for USB eye diagram test
OC0# / GPIO59
OC1# / GPIO40
OC2# / GPIO41
OC3# / GPIO42
OC4# / GPIO43
OC5# / GPIO9
OC6# / GPIO10
OC7# / GPIO14
USB_OC#0
USB_OC#1
R176
R177
USB_OC#0_1 {42}
USB_OC#X
R790
10K 5%
+V3_3AL
US3 and US4 co-layout
US3
SN74AHC1G08DBV
SOT23_5
RS97 100K 5%
BUF_PLT_RST# {37,38,40,44,45}
US4
74LVC1G17GW
USB IO PORTS
MINI USB FOR CARD
EXP USB
card reader USB
Carmera USB
INT_ USB
finger point_ USB
RS93 100K 5%
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PCH (PCI,USB,NVRAM)
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+V3_3AL

RS98 1K 5% ns PCH_GPIO15

RS99 10K 5% EXT_SMI#
RS100 10K 5% GPIO12
RS101 10K 5% GPIO24
RS102 10K 5% PCIECLKRQ6#
RS103 10K 5% PCIECLKRQ7#
RS104 10K 5% GPIO57
RS105 10K 5% PCH_GPIO28

GPIO check with EC(pull low/high/ voltage)

DVT Ask EC if we need to change GPIO pin.
GPIO8 can't be low.

+V3_3S

RS106 10K 5% GPIO0
RS107 10K 5% GPIO1
RS108 10K 5% ID_LPC_PCI#
RS109 10K 5% STP_PCI#
RS110 10K 5% GPIO17
RS111 10K 5% GPIO22
RS112 10K 5% GPIO37
RS113 10K 5% GPIO16
RS114 10K 5% GPIO36

RS116 10K 5% GPIO35

RS118 1K 5% ns GPIO27

{59} PCH_dGPU_PWR_ON R19 0.5% OP1 GPIO36

{28} PCH_PEX_RST# R20 0.5% GPIO16
{40} DSMCTRL R21 0.5% GPIO37
ns

+V3_3S

RS120 10K 5% PCH_GPIO38
RS121 10K 5% PCH_GPIO39
RS150 10K 5% PCH_GPIO48
RS122 10K 5% GPIO49

US1F

GPIO0 Y3 BMBUSY# / GPIO0
GPIO1 C38 TACH1 / GPIO1
ID_LPC_PCI# D37 TACH2 / GPIO6
{37} RUN_SCI# J32 TACH3 / GPIO7
{37} EXT_SMI# F10 GPIO8
GPIO12 K9 LAN_PHY_PWR_CTRL / GPIO12
PCH_GPIO15 T7 GPIO15
GPIO16 AA2 SATA4GP / GPIO16
GPIO17 F38 TACH0 / GPIO17
GPIO22 Y7 SCLOCK / GPIO22
GPIO24 H10 MEM_LED / GPIO24
GPIO27 AB12 GPIO27
PCH_GPIO28 V13 GPIO28
STP_PCI# M11 STP_PCI# / GPIO34
GPIO35 V6 SATACLKREQ# / GPIO35
GPIO36 AB7 SATA2GP / GPIO36
GPIO37 AB13 SATA3GP / GPIO37
PCH_GPIO38 V3 SLOAD / GPIO38
PCH_GPIO39 P3 SDATAOUT0 / GPIO39
PCIECLKRQ6# H3 PCIECLKRQ6# / GPIO45
PCIECLKRQ7# F1 PCIECLKRQ7# / GPIO46
PCH_GPIO48 AB6 SDATAOUT1 / GPIO48
GPIO49 AA4 SATA5GP / GPIO49
GPIO57 F8 GPIO57

MISC GPIO

A4 A49 A5 A50 A52 A53 B2 B4 B52 B53 BE1 BE53 BF1 BF53 BH1 BH2 BH52 BH53 BJ1 BJ2 BJ4 BJ49 BJ5 BJ50 BJ52 BJ53 D1 D2 D53 E1 E53
VSS_NCTF_1 VSS_NCTF_2 VSS_NCTF_3 VSS_NCTF_4 VSS_NCTF_5 VSS_NCTF_6 VSS_NCTF_7 VSS_NCTF_8 VSS_NCTF_9 VSS_NCTF_10 VSS_NCTF_11 VSS_NCTF_12 VSS_NCTF_13 VSS_NCTF_14 VSS_NCTF_15 VSS_NCTF_16 VSS_NCTF_17 VSS_NCTF_18 VSS_NCTF_19 VSS_NCTF_20 VSS_NCTF_21 VSS_NCTF_22 VSS_NCTF_23 VSS_NCTF_24 VSS_NCTF_25 VSS_NCTF_26 VSS_NCTF_27 VSS_NCTF_28 VSS_NCTF_29 VSS_NCTF_30 VSS_NCTF_31

NCTF RSVD

lbexpeak-M-HM55

CLKOUT_PCIE6N AH45 1 TP209 Test Point_30mil
CLKOUT_PCIE6P AH46 1 TP210 Test Point_30mil
CLKOUT_PCIE7N AF48 1 TP211 Test Point_30mil
CLKOUT_PCIE7P AF47 1 TP212 Test Point_30mil
A20GATE U2 H_A20GATE {37}
CLKOUT_BCLK0_N / CLKOUT_PCIE8N AM3 CLK_PCH_CPU_CLK# {11}
CLKOUT_BCLK0_P / CLKOUT_PCIE8P AM1 CLK_PCH_CPU_CLK {11}
PECI BG10 H_PECI {11}
RCIN# T1 KBRST# {37}
PROCPWRGD BE10 H_CPUPWRGD {11}
THRMTRIP# BD10 PCH_THRMTRIP# RS117 56 5%

+V1_05S
RS115 56 5% thermal/ procesor hot
PM_THRMTRIP# {11,66}

CPU

TP1 BA22 TP213 Test Point_30mil
TP2 AW22 TP214 Test Point_30mil
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32_1 TP221 Test Point_30mil
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41 TP237 Test Point_30mil
NC_5 T39_1 TP238 Test Point_30mil
INIT3_3V# P6_1 TP239 Test Point_30mil
TP24 C10

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Title	PCH (GPIO,VSS_NCTF,RSVD)	
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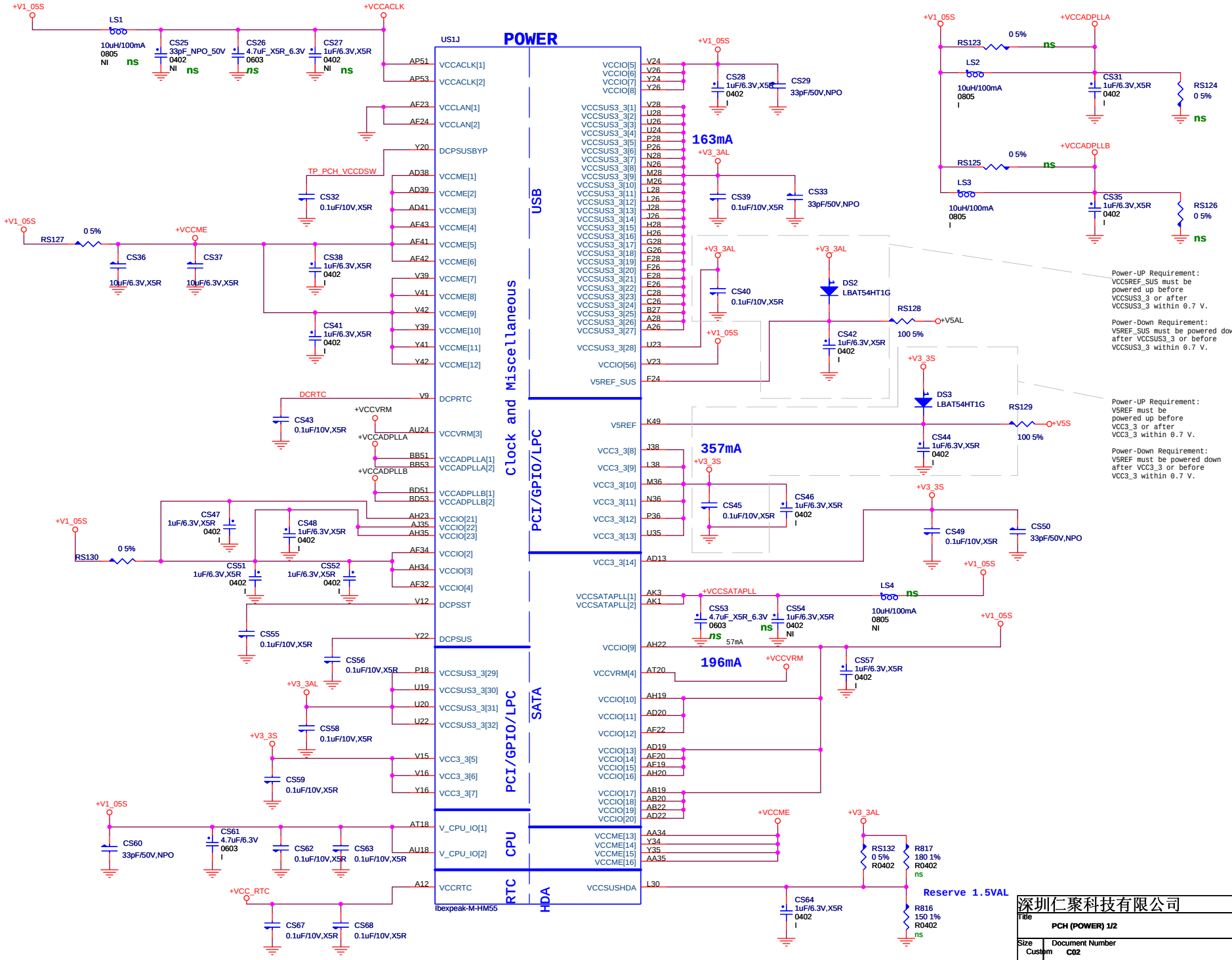
POWER
US1J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
PCI/GPIO/LPC
CPU
RTC
HDA
Ibexpeak-M-HM55
163mA
357mA
196mA
Reserve 1.5VAL
Power-UP Requirement:
VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V.
Power-Down Requirement:
V5REF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
Power-UP Requirement:
V5REF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.
Power-Down Requirement:
V5REF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.
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Title
PCH (POWER) 1/2
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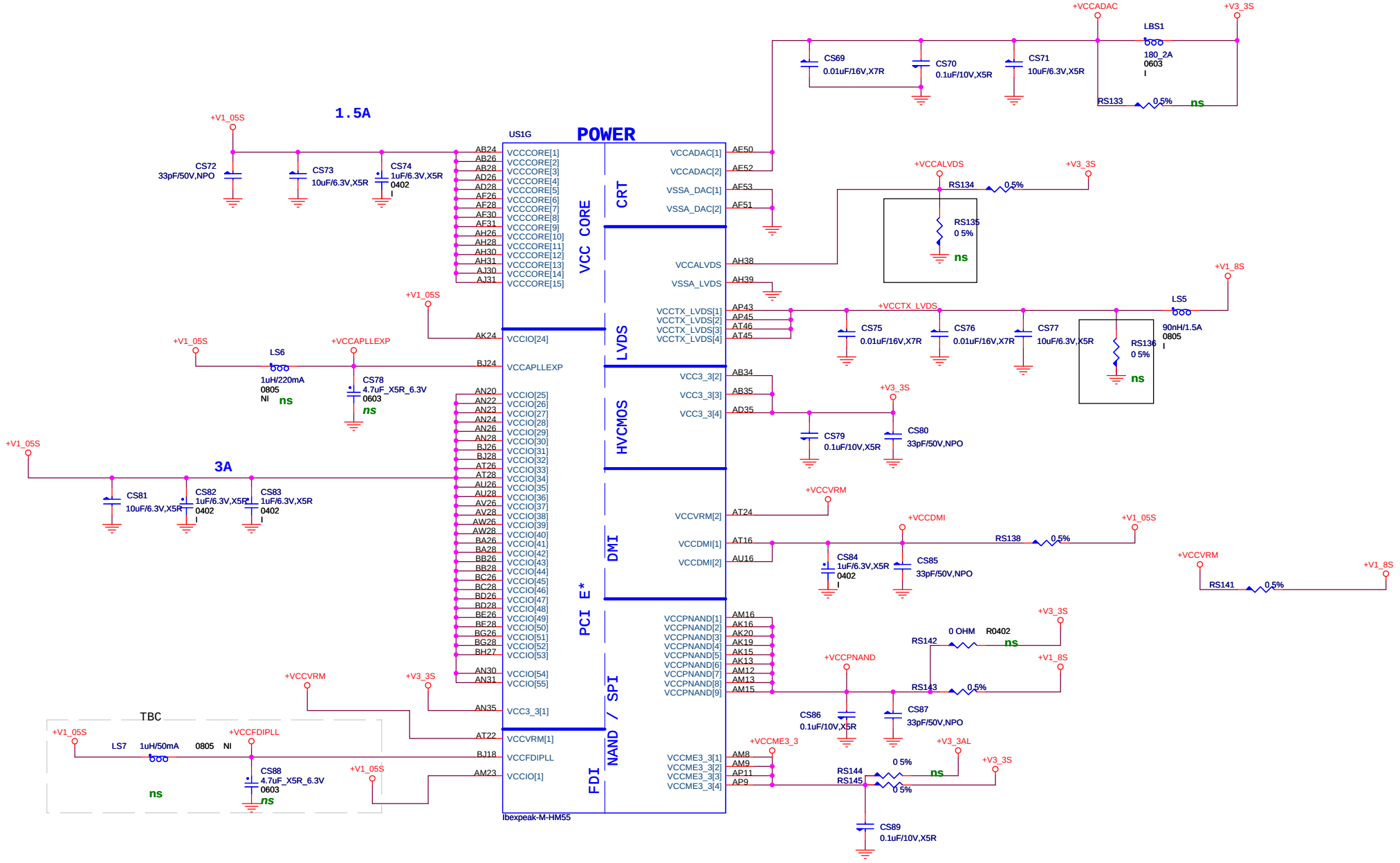

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Title: PCH (POWER) 2/2		
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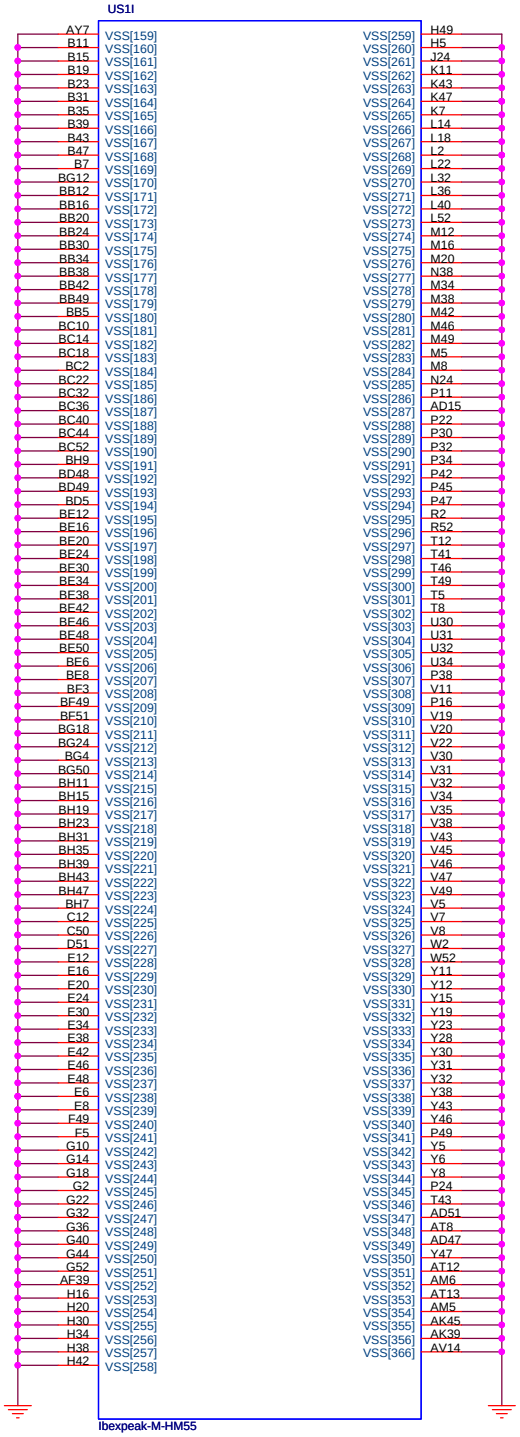

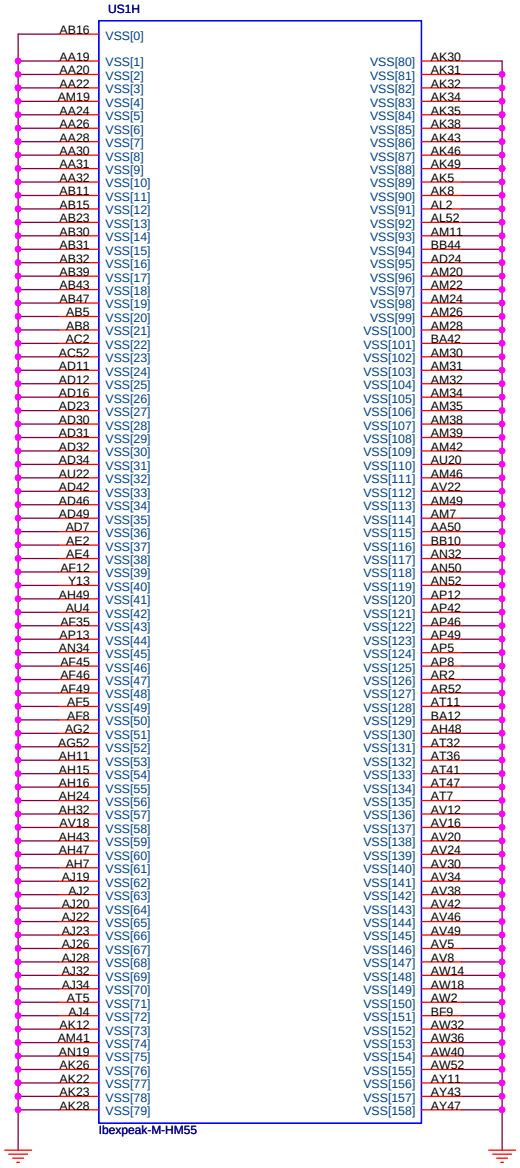

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Title	PCH (VSS)		
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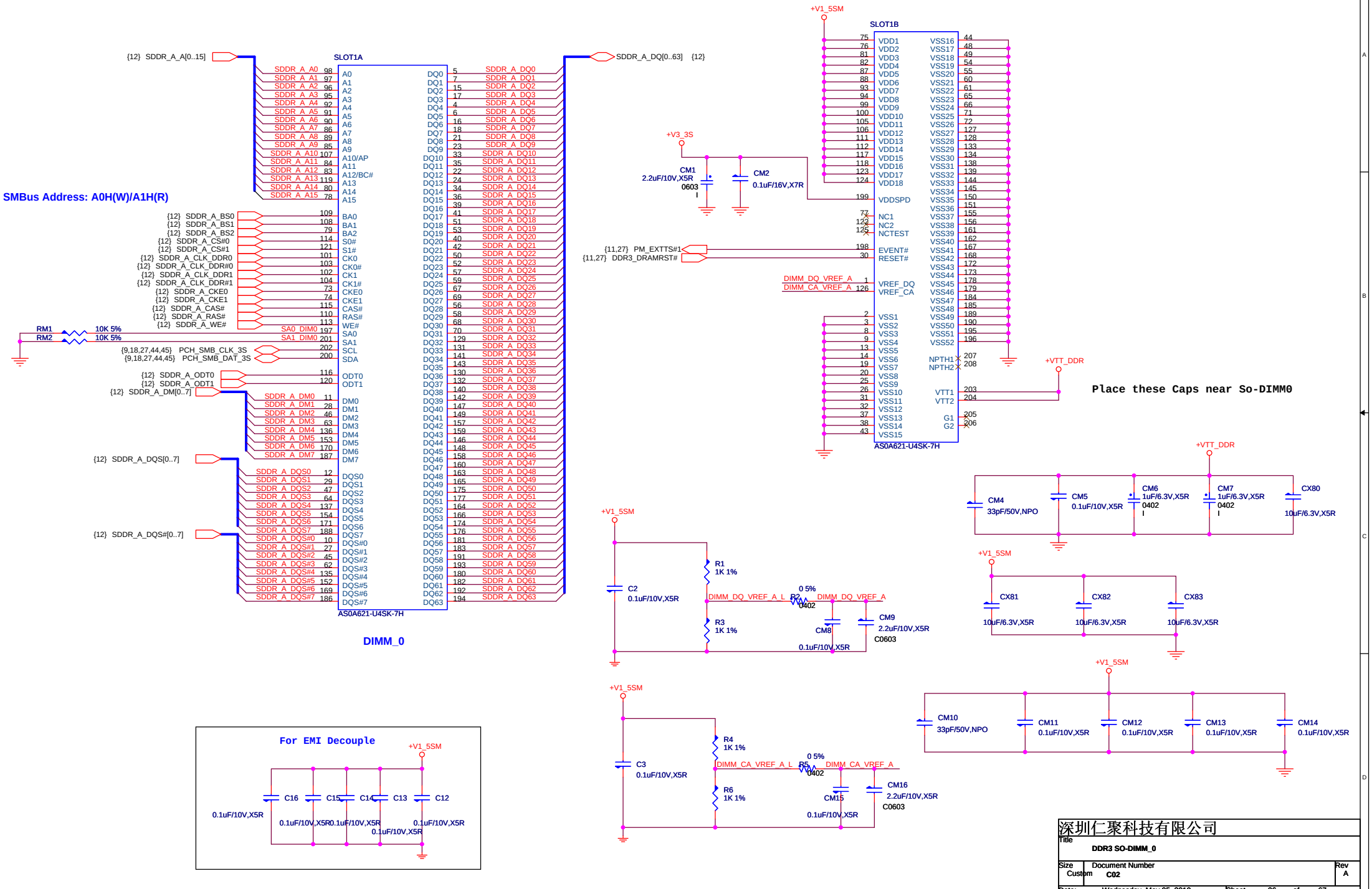

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Title	DDR3 SO-DIMM_0	
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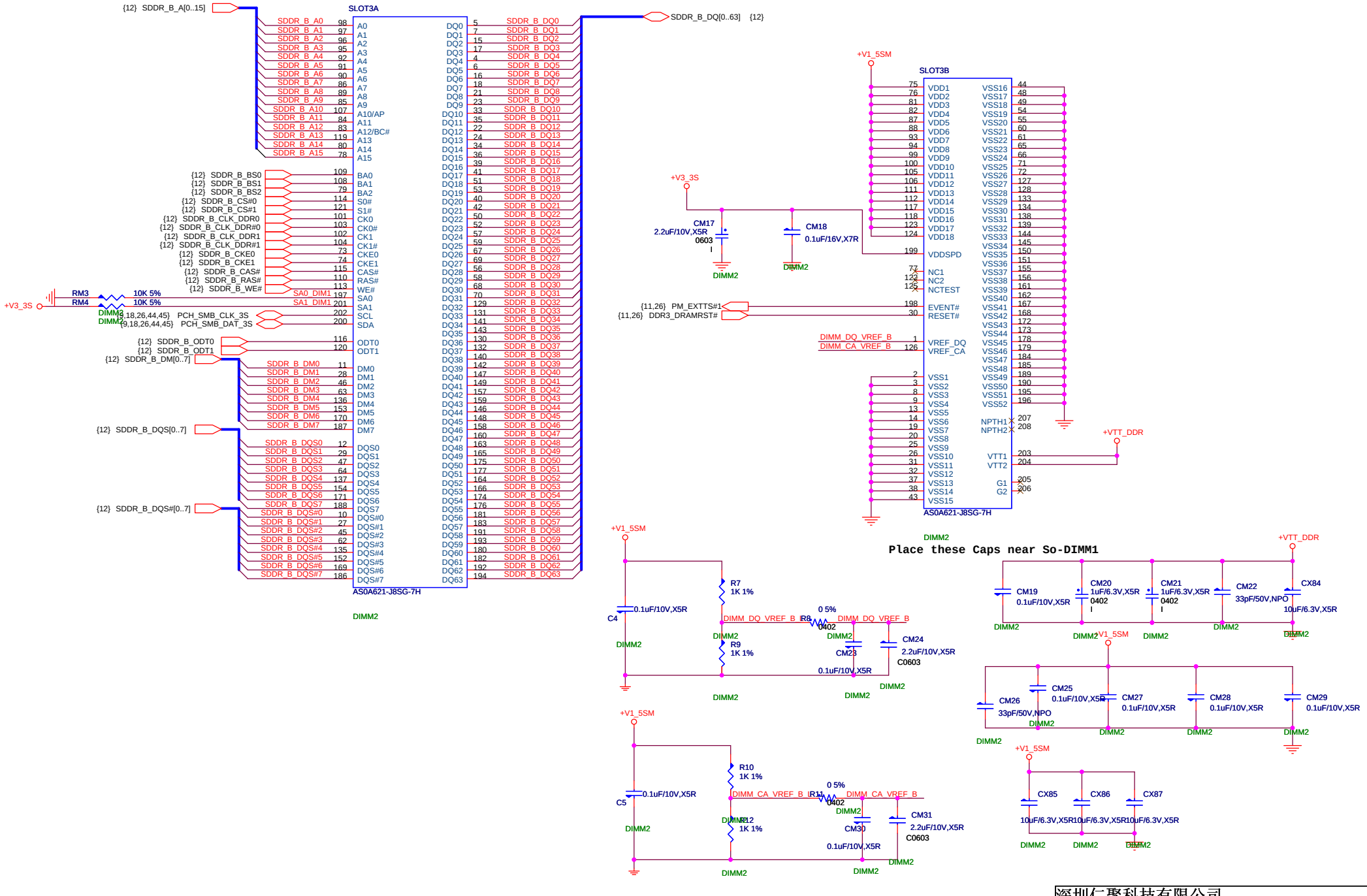

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Title	DDR3 SO-DIMM_2	
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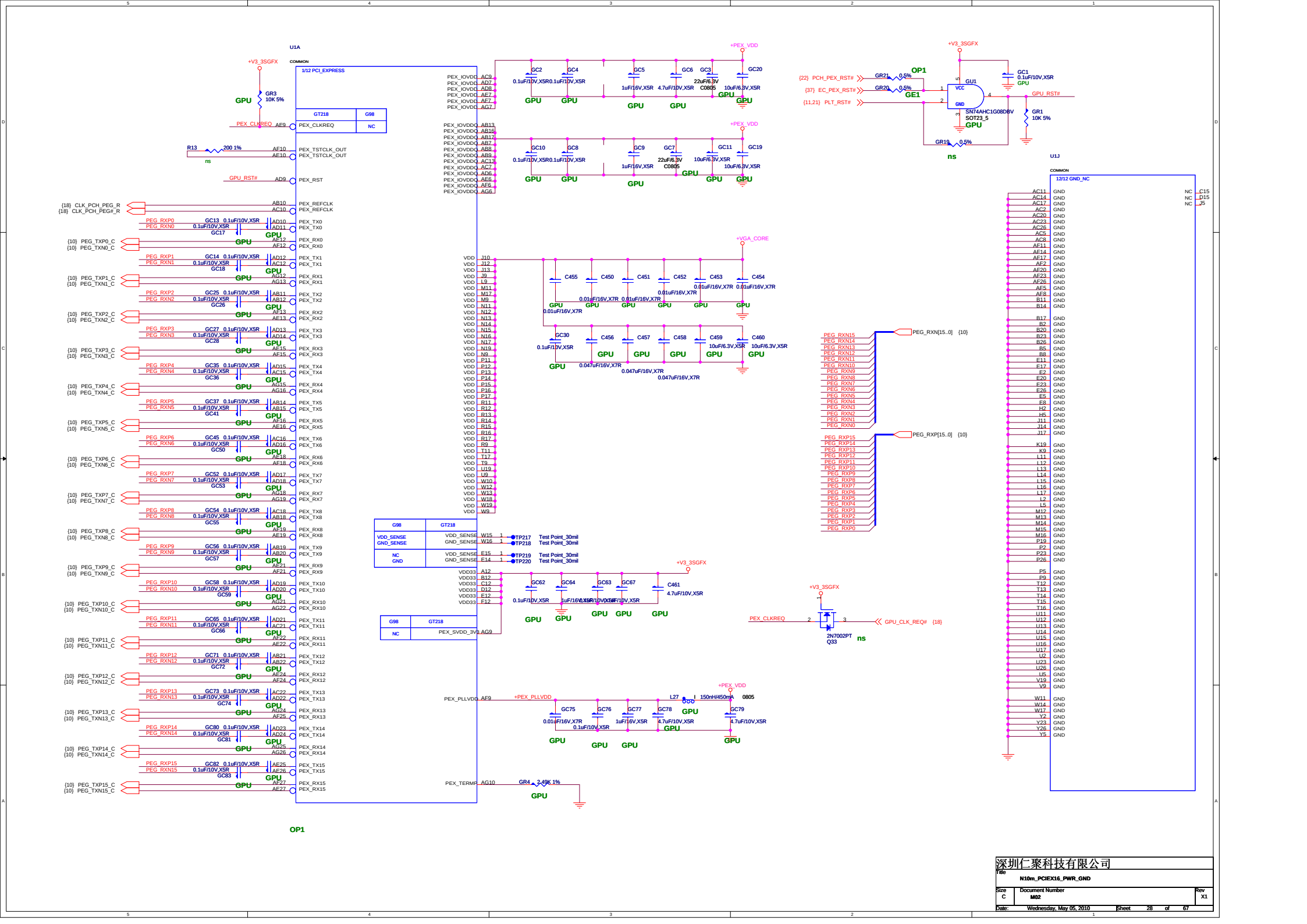
U1A
COMMON
1/12 PCI_EXPRESS
+V3_3SGFX
GPU
GR3
10K 5%
PEX_CLKREQ AE9
GT218 G98
PEX_CLKREQ NC
R13 200 1%
ns
AF10 PEX_TSTCLK_OUT
AE10 PEX_TSTCLK_OUT
GPU_RST# AD9 PEX_RST
{18} CLK_PCH_PEG_R
{18} CLK_PCH_PEG#_R
AB10 PEX_REFCLK
AC10 PEX_REFCLK
PEG_RXP0
PEG_RXN0
GC13 0.1uF/10V,X5R
GC17
{10} PEG_TXP0_C
{10} PEG_TXN0_C
AD10 PEX_TX0
AD11 PEX_TX0
AE12 PEX_RX0
AF12 PEX_RX0
PEG_RXP1
PEG_RXN1
GC14 0.1uF/10V,X5R
GC18
{10} PEG_TXP1_C
{10} PEG_TXN1_C
AD12 PEX_TX1
AC12 PEX_TX1
AG12 PEX_RX1
AG13 PEX_RX1
PEG_RXP2
PEG_RXN2
GC25 0.1uF/10V,X5R
GC26
{10} PEG_TXP2_C
{10} PEG_TXN2_C
AB11 PEX_TX2
AB12 PEX_TX2
AF13 PEX_RX2
AE13 PEX_RX2
PEG_RXP3
PEG_RXN3
GC27 0.1uF/10V,X5R
GC28
{10} PEG_TXP3_C
{10} PEG_TXN3_C
AD13 PEX_TX3
AD14 PEX_TX3
AF15 PEX_RX3
AF15 PEX_RX3
PEG_RXP4
PEG_RXN4
GC35 0.1uF/10V,X5R
GC36
{10} PEG_TXP4_C
{10} PEG_TXN4_C
AD15 PEX_TX4
AC15 PEX_TX4
AG15 PEX_RX4
AG16 PEX_RX4
PEG_RXP5
PEG_RXN5
GC37 0.1uF/10V,X5R
GC41
{10} PEG_TXP5_C
{10} PEG_TXN5_C
AB14 PEX_TX5
AB15 PEX_TX5
AF16 PEX_RX5
AE16 PEX_RX5
PEG_RXP6
PEG_RXN6
GC45 0.1uF/10V,X5R
GC50
{10} PEG_TXP6_C
{10} PEG_TXN6_C
AC16 PEX_TX6
AD16 PEX_TX6
AF18 PEX_RX6
AF18 PEX_RX6
PEG_RXP7
PEG_RXN7
GC52 0.1uF/10V,X5R
GC53
{10} PEG_TXP7_C
{10} PEG_TXN7_C
AD17 PEX_TX7
AD18 PEX_TX7
AG18 PEX_RX7
AG19 PEX_RX7
PEG_RXP8
PEG_RXN8
GC54 0.1uF/10V,X5R
GC55
{10} PEG_TXP8_C
{10} PEG_TXN8_C
AC18 PEX_TX8
AB18 PEX_TX8
AF19 PEX_RX8
AF19 PEX_RX8
PEG_RXP9
PEG_RXN9
GC56 0.1uF/10V,X5R
GC57
{10} PEG_TXP9_C
{10} PEG_TXN9_C
AB19 PEX_TX9
AB20 PEX_TX9
AF21 PEX_RX9
AF21 PEX_RX9
PEG_RXP10
PEG_RXN10
GC58 0.1uF/10V,X5R
GC59
{10} PEG_TXP10_C
{10} PEG_TXN10_C
AD19 PEX_TX10
AD20 PEX_TX10
AG21 PEX_RX10
AG22 PEX_RX10
PEG_RXP11
PEG_RXN11
GC65 0.1uF/10V,X5R
GC66
{10} PEG_TXP11_C
{10} PEG_TXN11_C
AB21 PEX_TX11
AC21 PEX_TX11
AF22 PEX_RX11
AF22 PEX_RX11
PEG_RXP12
PEG_RXN12
GC71 0.1uF/10V,X5R
GC72
{10} PEG_TXP12_C
{10} PEG_TXN12_C
AB21 PEX_TX12
AB22 PEX_TX12
AF24 PEX_RX12
AF24 PEX_RX12
PEG_RXP13
PEG_RXN13
GC73 0.1uF/10V,X5R
GC74
{10} PEG_TXP13_C
{10} PEG_TXN13_C
AC22 PEX_TX13
AD22 PEX_TX13
AG24 PEX_RX13
AF25 PEX_RX13
PEG_RXP14
PEG_RXN14
GC80 0.1uF/10V,X5R
GC81
{10} PEG_TXP14_C
{10} PEG_TXN14_C
AD23 PEX_TX14
AD24 PEX_TX14
AG25 PEX_RX14
AG26 PEX_RX14
PEG_RXP15
PEG_RXN15
GC82 0.1uF/10V,X5R
GC83
{10} PEG_TXP15_C
{10} PEG_TXN15_C
AE25 PEX_TX15
AE26 PEX_TX15
AF27 PEX_RX15
AE27 PEX_RX15
OP1
+PEX_VDD
PEX_IOVDDQ AC9
PEX_IOVDDQ AD7
PEX_IOVDDQ AD8
PEX_IOVDDQ AE7
PEX_IOVDDQ AF7
PEX_IOVDDQ AG7
GC2 0.1uF/10V,X5R
GC4 0.1uF/10V,X5R
GC5 1uF/16V,X5R
GC6 4.7uF/10V,X5R
GC3 22uF/6.3V C0805
GC20 10uF/6.3V,X5R
PEX_IOVDDQ AB13
PEX_IOVDDQ AB16
PEX_IOVDDQ AB17
PEX_IOVDDQ AB7
PEX_IOVDDQ AB8
PEX_IOVDDQ AB9
PEX_IOVDDQ AC13
PEX_IOVDDQ AC7
PEX_IOVDDQ AD6
PEX_IOVDDQ AE6
PEX_IOVDDQ AF6
PEX_IOVDDQ AG6
GC10 0.1uF/10V,X5R
GC8 0.1uF/10V,X5R
GC9 1uF/16V,X5R
GC7 22uF/6.3V C0805
GC11 10uF/6.3V,X5R
GC19 10uF/6.3V,X5R
+VGA_CORE
VDD J10
VDD J12
VDD J13
VDD J9
VDD L9
VDD M11
VDD M17
VDD M9
VDD N11
VDD N12
VDD N13
VDD N14
VDD N15
VDD N16
VDD N17
VDD N19
VDD N9
VDD P11
VDD P12
VDD P13
VDD P14
VDD P15
VDD P16
VDD P17
VDD R11
VDD R12
VDD R13
VDD R14
VDD R15
VDD R16
VDD R17
VDD R9
VDD T11
VDD T17
VDD T9
VDD U19
VDD U9
VDD W10
VDD W12
VDD W13
VDD W18
VDD W19
VDD W9
C455 0.01uF/16V,X7R
C450 0.01uF/16V,X7R
C451 0.01uF/16V,X7R
C452 0.01uF/16V,X7R
C453 0.01uF/16V,X7R
C454 0.01uF/16V,X7R
GC30 0.1uF/10V,X5R
C456 0.047uF/16V,X7R
C457 0.047uF/16V,X7R
C458 0.047uF/16V,X7R
C459 10uF/6.3V,X5R
C460 10uF/6.3V,X5R
G98 GT218
VDD_SENSE GND_SENSE
NC GND
VDD_SENSE W15
GND_SENSE W16
TP217 Test Point_30mil
TP218 Test Point_30mil
VDD_SENSE E15
GND_SENSE E14
TP219 Test Point_30mil
TP220 Test Point_30mil
G98 GT218
NC PEX_SVDD_3V3 AG9
+V3_3SGFX
VDD33 A12
VDD33 B12
VDD33 C12
VDD33 D12
VDD33 E12
VDD33 F12
GC62 0.1uF/10V,X5R
GC64 1uF/16V,X5R
GC63 0.1uF/10V,X5R
GC67 4.7uF/10V,X5R
C461 4.7uF/10V,X5R
PEX_PLLVDD AF9
+PEX_PLLVDD
L27 150nH/450mA 0805
GC75 0.01uF/16V,X7R
GC76 0.1uF/10V,X5R
GC77 1uF/16V,X5R
GC78 4.7uF/10V,X5R
GC79 4.7uF/10V,X5R
PEX_TERMP AG10
GR4 2.49K 1%
{22} PCH_PEX_RST#
{37} EC_PEX_RST#
{11,21} PLT_RST#
GR21 0.5%
GR20 0.5%
OP1
GE1
GU1
VCC
GND
SN74AHC1G08DBV
SOT23_5
GR19 0.5%
GC1 0.1uF/10V,X5R
GPU_RST#
GR1 10K 5%
U1J
COMMON
12/12 GND_NC
NC C15
NC D15
NC J5
PEG_RXN[15..0] {10}
PEG_RXP[15..0] {10}
PEX_CLKREQ
GPU_CLK_REQ# {18}
2N7002PT
Q33
深圳仁聚科技有限公司
N10m_PCIEX16_PWR_GND
Size C
Document Number M02
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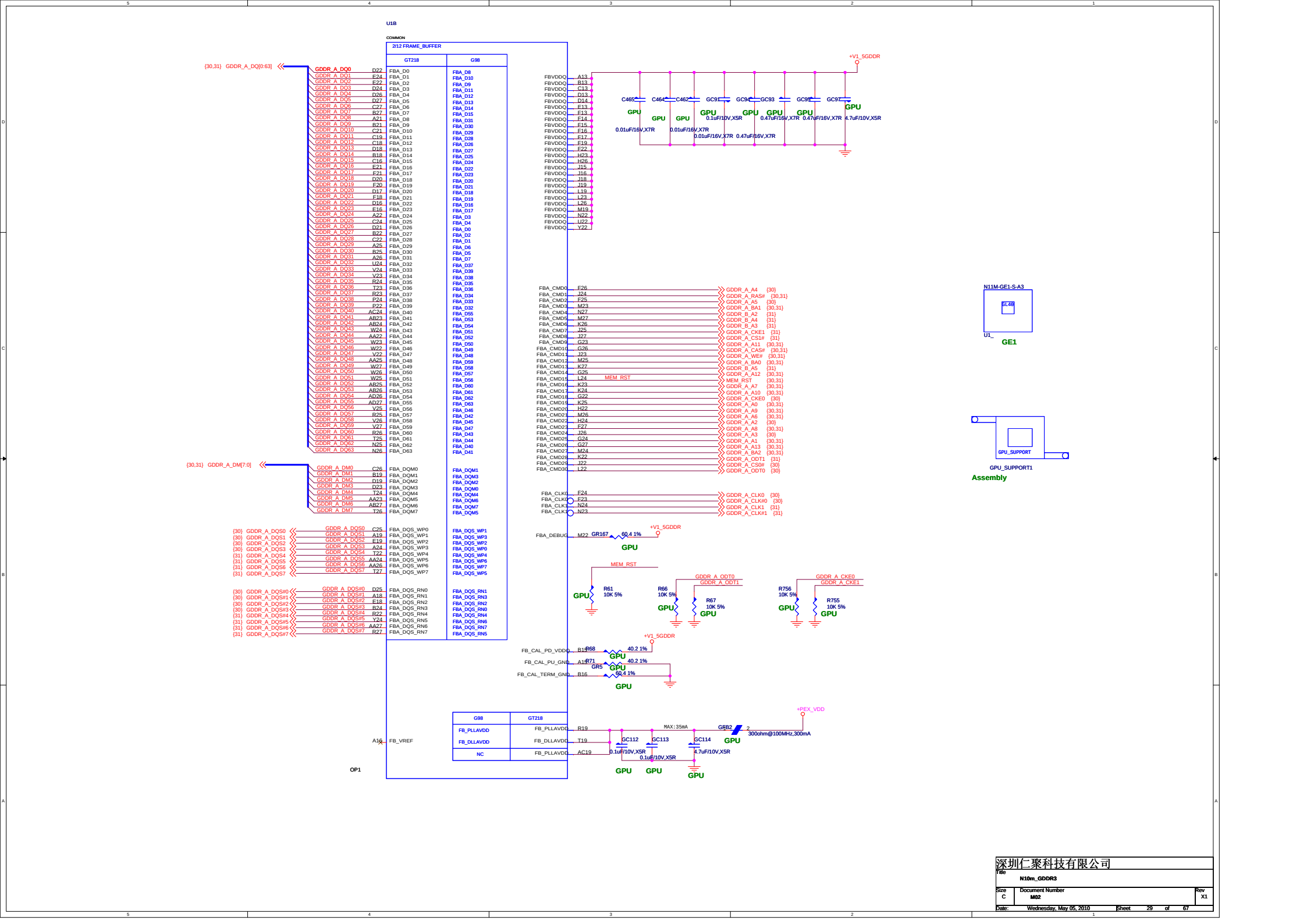
U1B
COMMON
2/12 FRAME_BUFFER
GT218
G98
{30,31} GDDR_A_DQ[0:63]
GDDR_A_DQ0 D22 FBA_D0 FBA_D8
GDDR_A_DQ1 E24 FBA_D1 FBA_D10
GDDR_A_DQ2 E22 FBA_D2 FBA_D9
GDDR_A_DQ3 D24 FBA_D3 FBA_D11
GDDR_A_DQ4 D26 FBA_D4 FBA_D12
GDDR_A_DQ5 D27 FBA_D5 FBA_D13
GDDR_A_DQ6 C27 FBA_D6 FBA_D14
GDDR_A_DQ7 B27 FBA_D7 FBA_D15
GDDR_A_DQ8 A21 FBA_D8 FBA_D31
GDDR_A_DQ9 B21 FBA_D9 FBA_D30
GDDR_A_DQ10 C21 FBA_D10 FBA_D29
GDDR_A_DQ11 C19 FBA_D11 FBA_D28
GDDR_A_DQ12 C18 FBA_D12 FBA_D26
GDDR_A_DQ13 D18 FBA_D13 FBA_D27
GDDR_A_DQ14 B18 FBA_D14 FBA_D25
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GDDR_A_DQ16 E21 FBA_D16 FBA_D22
GDDR_A_DQ17 F21 FBA_D17 FBA_D23
GDDR_A_DQ18 D20 FBA_D18 FBA_D20
GDDR_A_DQ19 F20 FBA_D19 FBA_D21
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GDDR_A_DQ21 F18 FBA_D21 FBA_D19
GDDR_A_DQ22 D16 FBA_D22 FBA_D16
GDDR_A_DQ23 E16 FBA_D23 FBA_D17
GDDR_A_DQ24 A22 FBA_D24 FBA_D3
GDDR_A_DQ25 C24 FBA_D25 FBA_D4
GDDR_A_DQ26 D21 FBA_D26 FBA_D0
GDDR_A_DQ27 B22 FBA_D27 FBA_D2
GDDR_A_DQ28 C22 FBA_D28 FBA_D1
GDDR_A_DQ29 A25 FBA_D29 FBA_D6
GDDR_A_DQ30 B25 FBA_D30 FBA_D5
GDDR_A_DQ31 A26 FBA_D31 FBA_D7
GDDR_A_DQ32 U24 FBA_D32 FBA_D37
GDDR_A_DQ33 V24 FBA_D33 FBA_D39
GDDR_A_DQ34 V23 FBA_D34 FBA_D38
GDDR_A_DQ35 R24 FBA_D35 FBA_D35
GDDR_A_DQ36 T23 FBA_D36 FBA_D36
GDDR_A_DQ37 R23 FBA_D37 FBA_D34
GDDR_A_DQ38 P24 FBA_D38 FBA_D33
GDDR_A_DQ39 P22 FBA_D39 FBA_D32
GDDR_A_DQ40 AC24 FBA_D40 FBA_D55
GDDR_A_DQ41 AB23 FBA_D41 FBA_D53
GDDR_A_DQ42 AB24 FBA_D42 FBA_D54
GDDR_A_DQ43 W24 FBA_D43 FBA_D51
GDDR_A_DQ44 AA22 FBA_D44 FBA_D52
GDDR_A_DQ45 W23 FBA_D45 FBA_D50
GDDR_A_DQ46 W22 FBA_D46 FBA_D49
GDDR_A_DQ47 V22 FBA_D47 FBA_D48
GDDR_A_DQ48 AA25 FBA_D48 FBA_D59
GDDR_A_DQ49 W27 FBA_D49 FBA_D58
GDDR_A_DQ50 W26 FBA_D50 FBA_D57
GDDR_A_DQ51 W25 FBA_D51 FBA_D56
GDDR_A_DQ52 AB25 FBA_D52 FBA_D60
GDDR_A_DQ53 AB26 FBA_D53 FBA_D61
GDDR_A_DQ54 AD26 FBA_D54 FBA_D62
GDDR_A_DQ55 AD27 FBA_D55 FBA_D63
GDDR_A_DQ56 V25 FBA_D56 FBA_D46
GDDR_A_DQ57 R25 FBA_D57 FBA_D42
GDDR_A_DQ58 V26 FBA_D58 FBA_D45
GDDR_A_DQ59 V27 FBA_D59 FBA_D47
GDDR_A_DQ60 R26 FBA_D60 FBA_D43
GDDR_A_DQ61 T25 FBA_D61 FBA_D44
GDDR_A_DQ62 N25 FBA_D62 FBA_D40
GDDR_A_DQ63 N26 FBA_D63 FBA_D41
{30,31} GDDR_A_DM[7:0]
GDDR_A_DM0 C26 FBA_DQM0 FBA_DQM1
GDDR_A_DM1 B19 FBA_DQM1 FBA_DQM3
GDDR_A_DM2 D19 FBA_DQM2 FBA_DQM2
GDDR_A_DM3 D23 FBA_DQM3 FBA_DQM0
GDDR_A_DM4 T24 FBA_DQM4 FBA_DQM4
GDDR_A_DM5 AA23 FBA_DQM5 FBA_DQM6
GDDR_A_DM6 AB27 FBA_DQM6 FBA_DQM7
GDDR_A_DM7 T26 FBA_DQM7 FBA_DQM5
{30} GDDR_A_DQS0 GDDR_A_DQS0 C25 FBA_DQS_WP0 FBA_DQS_WP1
{30} GDDR_A_DQS1 GDDR_A_DQS1 A19 FBA_DQS_WP1 FBA_DQS_WP3
{30} GDDR_A_DQS2 GDDR_A_DQS2 E19 FBA_DQS_WP2 FBA_DQS_WP2
{30} GDDR_A_DQS3 GDDR_A_DQS3 A24 FBA_DQS_WP3 FBA_DQS_WP0
{31} GDDR_A_DQS4 GDDR_A_DQS4 T22 FBA_DQS_WP4 FBA_DQS_WP4
{31} GDDR_A_DQS5 GDDR_A_DQS5 AA24 FBA_DQS_WP5 FBA_DQS_WP6
{31} GDDR_A_DQS6 GDDR_A_DQS6 AA26 FBA_DQS_WP6 FBA_DQS_WP7
{31} GDDR_A_DQS7 GDDR_A_DQS7 T27 FBA_DQS_WP7 FBA_DQS_WP5
{30} GDDR_A_DQS#0 GDDR_A_DQS#0 D25 FBA_DQS_RN0 FBA_DQS_RN1
{30} GDDR_A_DQS#1 GDDR_A_DQS#1 A18 FBA_DQS_RN1 FBA_DQS_RN3
{30} GDDR_A_DQS#2 GDDR_A_DQS#2 E18 FBA_DQS_RN2 FBA_DQS_RN2
{30} GDDR_A_DQS#3 GDDR_A_DQS#3 B24 FBA_DQS_RN3 FBA_DQS_RN0
{31} GDDR_A_DQS#4 GDDR_A_DQS#4 R22 FBA_DQS_RN4 FBA_DQS_RN4
{31} GDDR_A_DQS#5 GDDR_A_DQS#5 Y24 FBA_DQS_RN5 FBA_DQS_RN6
{31} GDDR_A_DQS#6 GDDR_A_DQS#6 AA27 FBA_DQS_RN6 FBA_DQS_RN7
{31} GDDR_A_DQS#7 GDDR_A_DQS#7 R27 FBA_DQS_RN7 FBA_DQS_RN5
A16 FBA_VREF
OP1
G98 GT218
FB_PLLAVDD FB_PLLAVDD R19
FB_DLLAVDD FB_DLLAVDD T19
NC FB_PLLAVDD AC19
FBVDDQ A13 B13 C13 D13 D14 E13 F13 F14 E15 F15 E16 F16 E17 F19 F22 H23 H26 J15 J16 J18 J19 L19 L23 L26 M19 N22 U22 Y22
+V1_5GDDR
C465 C464 C462 GC91 GC94 GC93 GC95 GC97
0.01uF/16V,X7R 0.01uF/16V,X7R 0.01uF/16V,X7R 0.1uF/10V,X5R 0.47uF/16V,X7R 0.47uF/16V,X7R 0.47uF/16V,X7R 4.7uF/10V,X5R
GPU
FBA_CMD0 F26 GDDR_A_A4 {30}
FBA_CMD1 J24 GDDR_A_RAS# {30,31}
FBA_CMD2 F25 GDDR_A_A5 {30}
FBA_CMD3 M23 GDDR_A_BA1 {30,31}
FBA_CMD4 N27 GDDR_B_A2 {31}
FBA_CMD5 M27 GDDR_B_A4 {31}
FBA_CMD6 K26 GDDR_B_A3 {31}
FBA_CMD7 J25 GDDR_A_CKE1 {31}
FBA_CMD8 J27 GDDR_A_CS1# {31}
FBA_CMD9 G23 GDDR_A_A11 {30,31}
FBA_CMD10 G26 GDDR_A_CAS# {30,31}
FBA_CMD11 J23 GDDR_A_WE# {30,31}
FBA_CMD12 M25 GDDR_A_BA0 {30,31}
FBA_CMD13 K27 GDDR_B_A5 {31}
FBA_CMD14 G25 GDDR_A_A12 {30,31}
FBA_CMD15 L24 MEM_RST MEM_RST {30,31}
FBA_CMD16 K23 GDDR_A_A7 {30,31}
FBA_CMD17 K24 GDDR_A_A10 {30,31}
FBA_CMD18 G22 GDDR_A_CKE0 {30}
FBA_CMD19 K25 GDDR_A_A0 {30,31}
FBA_CMD20 H22 GDDR_A_A9 {30,31}
FBA_CMD21 M26 GDDR_A_A6 {30,31}
FBA_CMD22 H24 GDDR_A_A2 {30}
FBA_CMD23 F27 GDDR_A_A8 {30,31}
FBA_CMD24 J26 GDDR_A_A3 {30}
FBA_CMD25 G24 GDDR_A_A1 {30,31}
FBA_CMD26 G27 GDDR_A_A13 {30,31}
FBA_CMD27 M24 GDDR_A_BA2 {30,31}
FBA_CMD28 K22 GDDR_A_ODT1 {31}
FBA_CMD29 J22 GDDR_A_CS0# {30}
FBA_CMD30 L22 GDDR_A_ODT0 {30}
FBA_CLK0 F24 GDDR_A_CLK0 {30}
FBA_CLK0 F23 GDDR_A_CLK#0 {30}
FBA_CLK1 N24 GDDR_A_CLK1 {31}
FBA_CLK1 N23 GDDR_A_CLK#1 {31}
FBA_DEBUG M22 GR167 60.4 1%
+V1_5GDDR
GPU
MEM_RST
R61 10K 5%
GDDR_A_ODT0 GDDR_A_ODT1
R66 10K 5% R67 10K 5%
GDDR_A_CKE0 GDDR_A_CKE1
R756 10K 5% R755 10K 5%
FB_CAL_PD_VDDQ B18 R68 40.2 1%
FB_CAL_PU_GND A18 R71 40.2 1%
FB_CAL_TERM_GND B16 GR5 60.4 1%
+V1_5GDDR
+PEX_VDD
MAX:35mA
GRB2 2 300ohm@100MHz,300mA
GC112 GC113 GC114
0.1uF/10V,X5R 0.1uF/10V,X5R 4.7uF/10V,X5R
N11M-GE1-S-A3
SLAB
U1_
GE1
GPU_SUPPORT
GPU_SUPPORT1
Assembly
深圳仁聚科技有限公司
Title
N10m_GDDR3
Size C
Document Number M02
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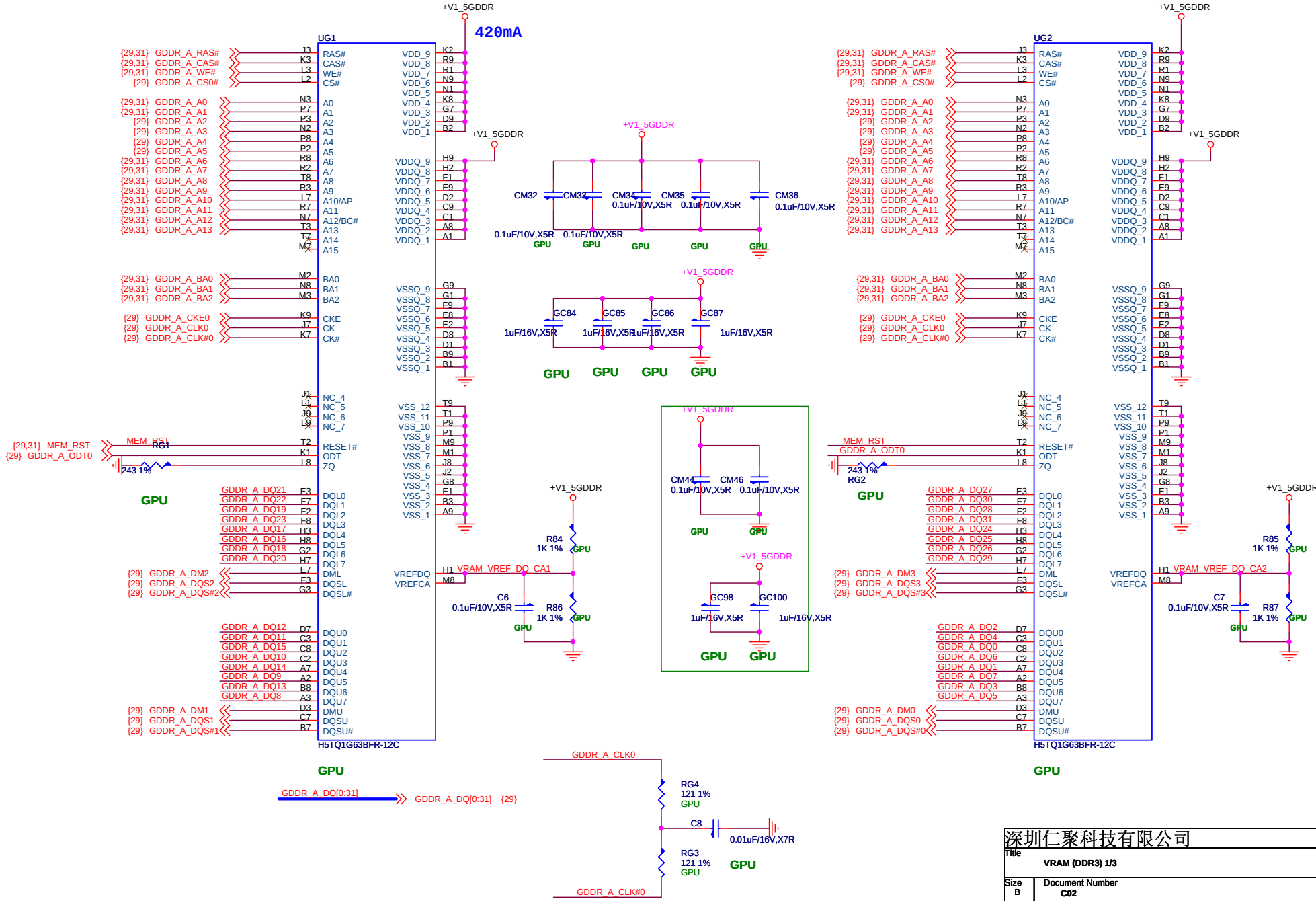

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Title	VRAM (DDR3) 1/3	
Size B	Document Number C02	Rev A
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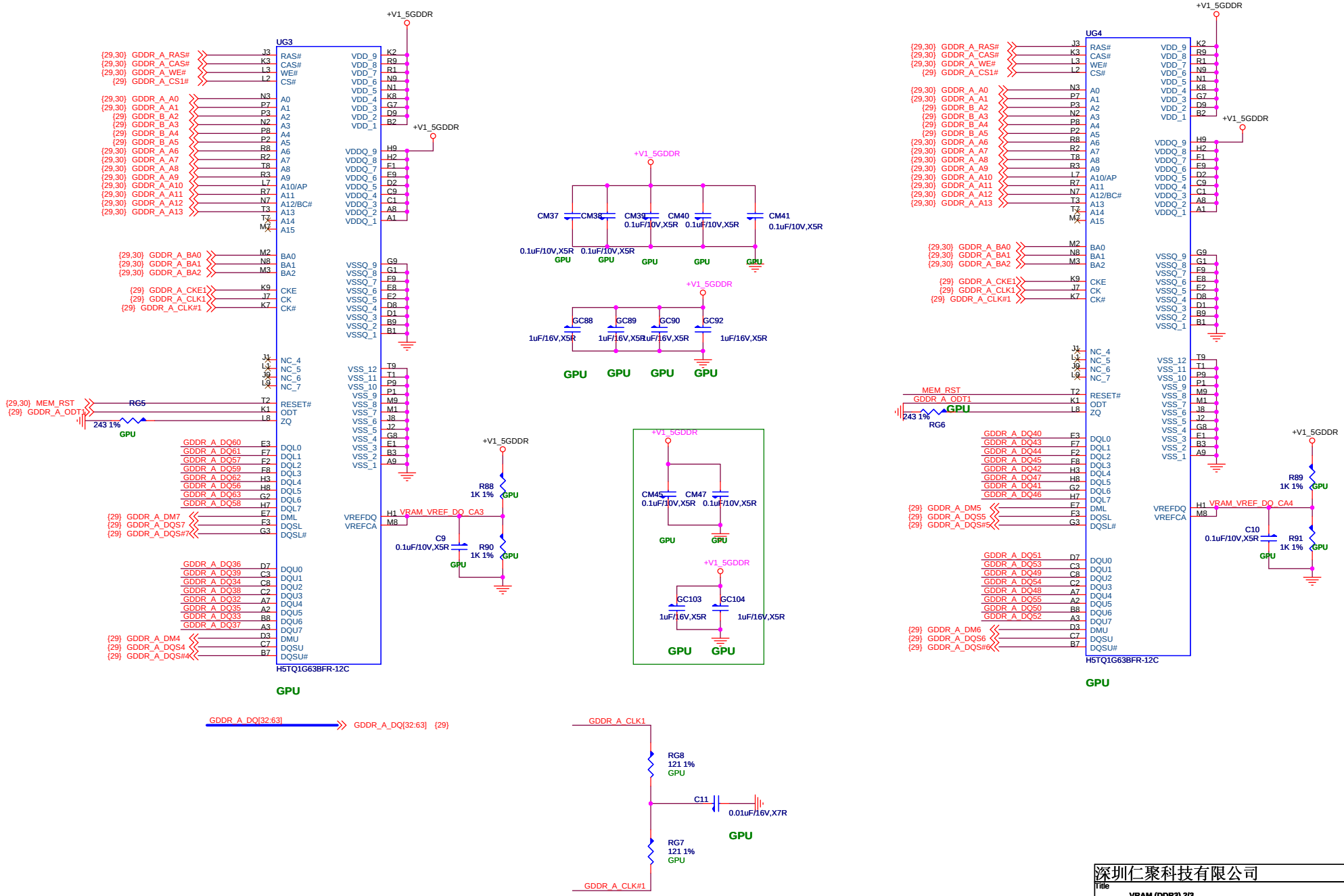

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Title	VRAM (DDR3) 2/3	
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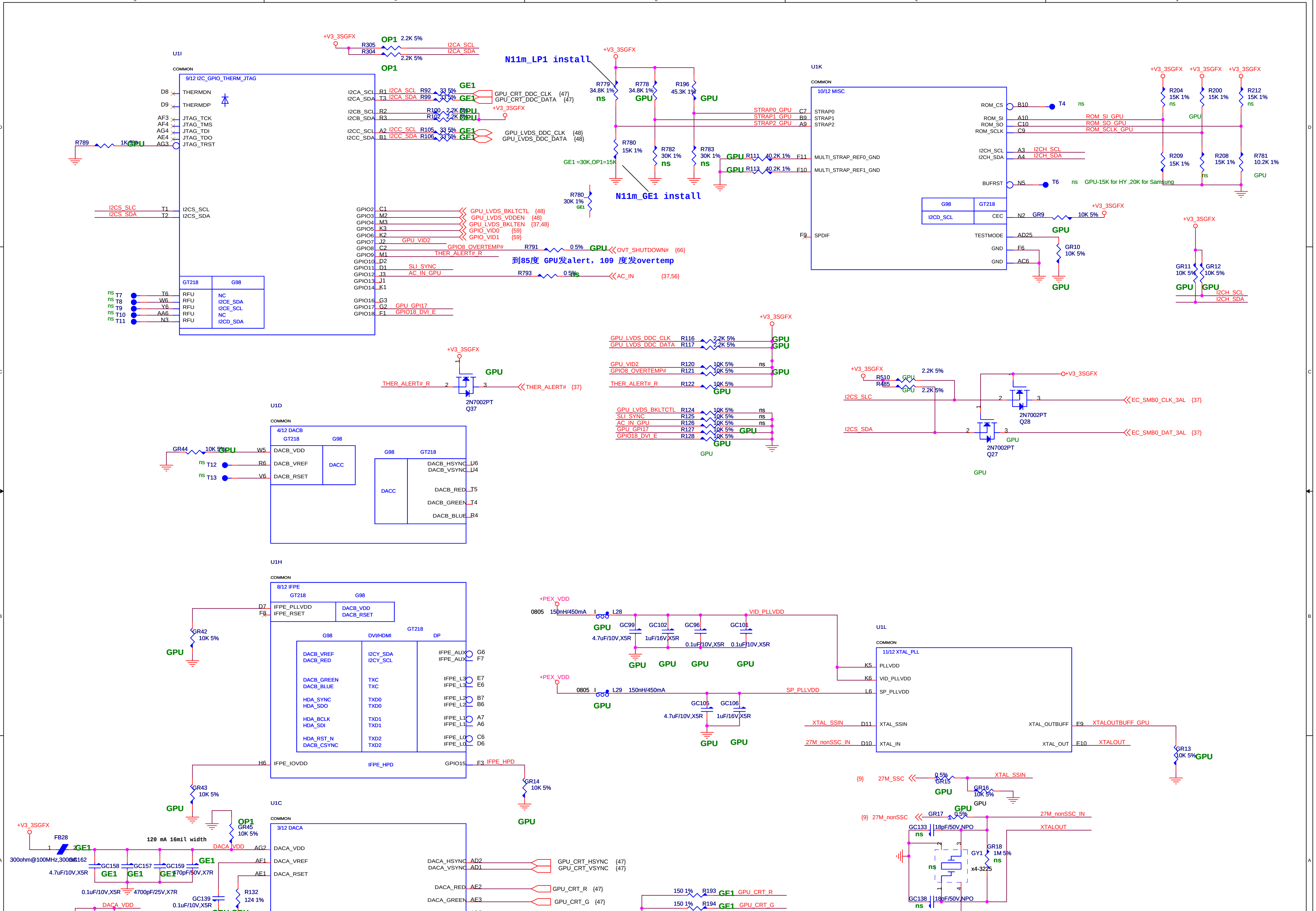

N11m_LP1 install
N11m_GE1 install
U1I
9/12 I2C_GPIO_THERM_JTAG
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA
GPU_CRT_DDC_CLK {47}
GPU_CRT_DDC_DATA {47}
GPU_LVDS_DDC_CLK {48}
GPU_LVDS_DDC_DATA {48}
GPU_LVDS_BKLTCTL {48}
GPU_LVDS_VDDEN {48}
GPU_LVDS_BKLTEN {37,48}
GPU_VID0 {59}
GPU_VID1 {59}
GPU_VID2
GPIO8_OVERTEMP#
THER_ALERT#_R
SLI_SYNC
AC_IN_GPU
GPU_GPI17
GPIO18_DVI_E
OVT_SHUTDOWN# {66}
AC_IN {37,56}
到85度 GPU发alert，109 度发overtemp
GE1 =30K,OP1=15K
U1K
10/12 MISC
STRAP0
STRAP1
STRAP2
MULTI_STRAP_REF0_GND
MULTI_STRAP_REF1_GND
SPDIF
ROM_CS
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST
CEC
TESTMODE
GND
ROM_SI_GPU
ROM_SO_GPU
ROM_SCLK_GPU
GPU-15K for HY ,20K for Samsung
+V3_3SGFX
2N7002PT
Q37
Q28
Q27
EC_SMB0_CLK_3AL {37}
EC_SMB0_DAT_3AL {37}
THER_ALERT# {37}
U1D
4/12 DACB
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
U1H
8/12 IFPE
IFPE_PLLVDD
IFPE_RSET
IFPE_IOVDD
IFPE_HPD
+PEX_VDD
VID_PLLVDD
SP_PLLVDD
U1L
11/12 XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
XTALOUTBUFF_GPU
XTALOUT
27M_SSC
27M_nonSSC
27M_nonSSC_IN
U1C
3/12 DACA
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
GPU_CRT_HSYNC {47}
GPU_CRT_VSYNC {47}
GPU_CRT_R {47}
GPU_CRT_G {47}
GPU_CRT_B {47}
120 mA 16mil width
300ohm@100MHz,3000mA

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Title	N10m_CRT_I2C_STRAP		
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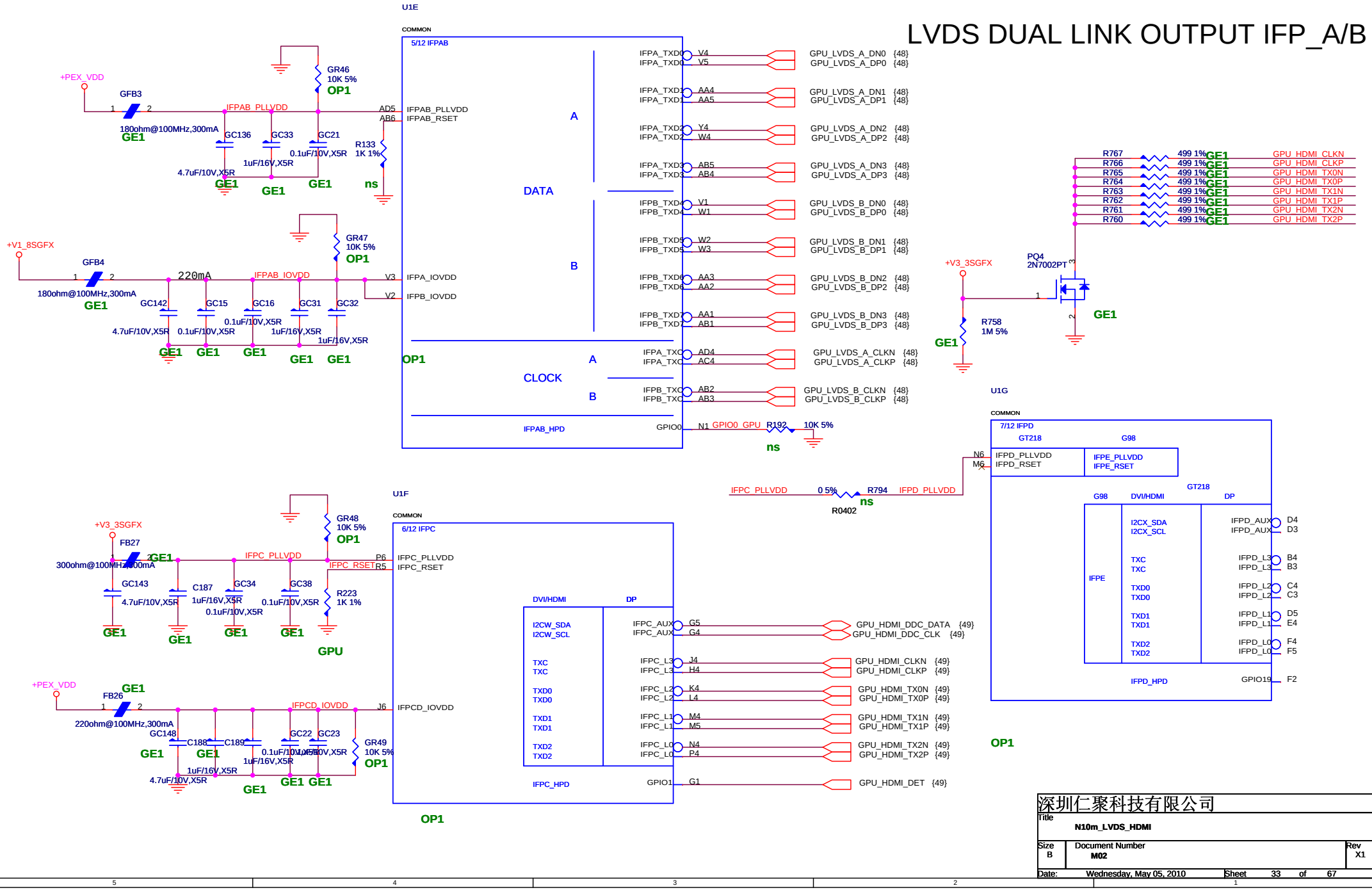
LVDS DUAL LINK OUTPUT IFP_A/B



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Title: N10m_LVDS_HDMI		
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Title: blank		
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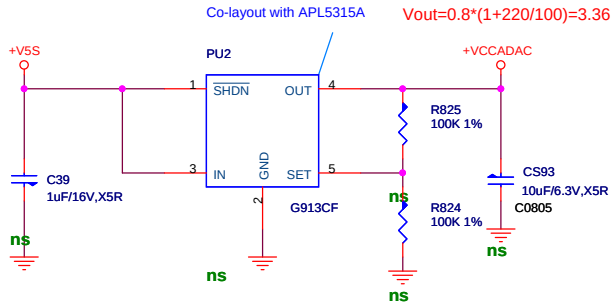
Title: BLANK		
Size: Custom	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 35 of 67	



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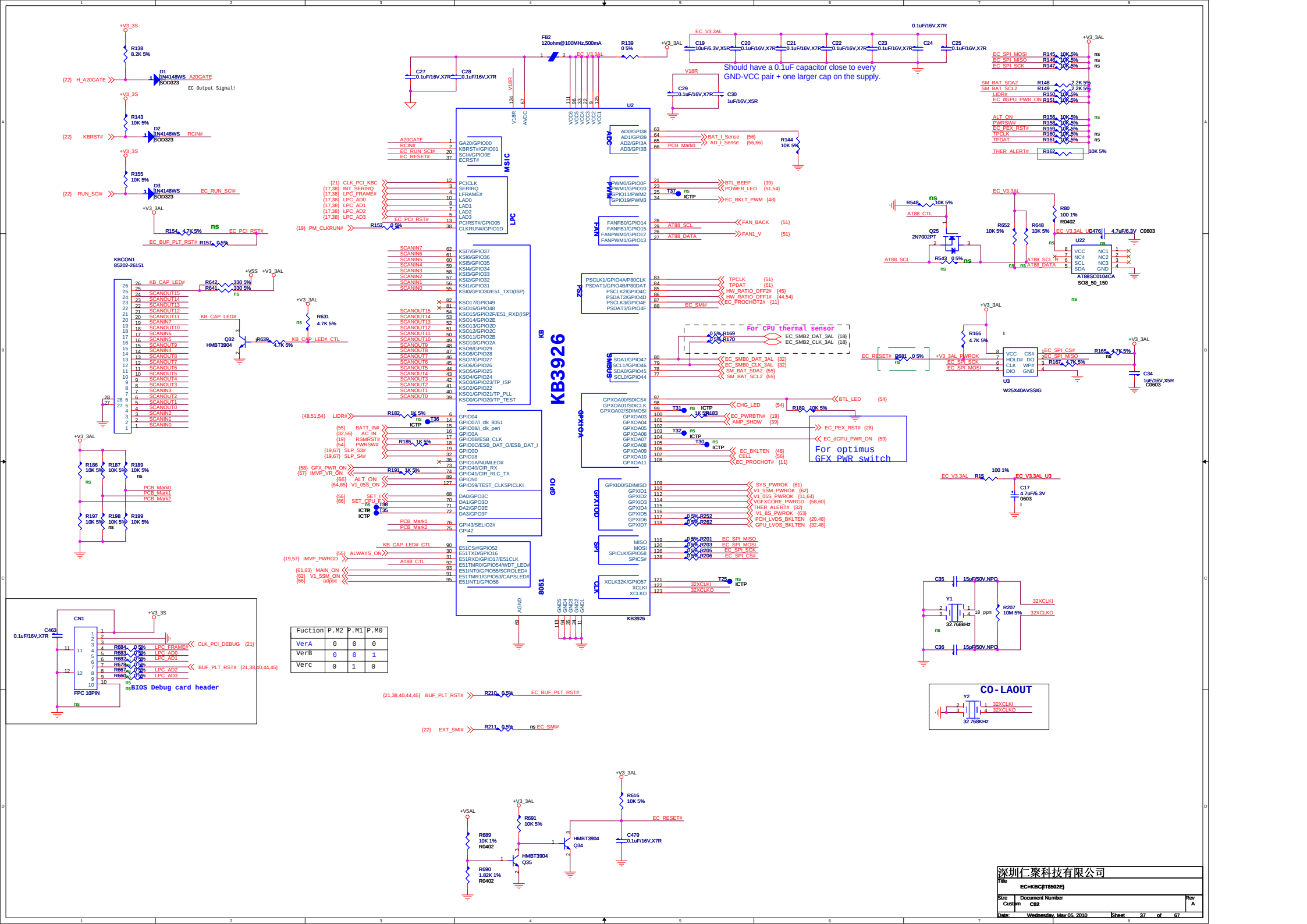
Title: BLANK		
Size: Custom	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 36 of 67	


KB3926
U2
KBCON1
85202-26151
CN1
FPC 10PIN
BIOS Debug card header
Should have a 0.1uF capacitor close to every
GND-VCC pair + one larger cap on the supply.
For CPU thermal sensor
For optimus
GFX PWR switch
CO-LAOUT
Fuction | P.M2 | P.M1 | P.M0
VerA | 0 | 0 | 0
VerB | 0 | 0 | 1
Verc | 0 | 1 | 0
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EC+KBC(IT8502E)
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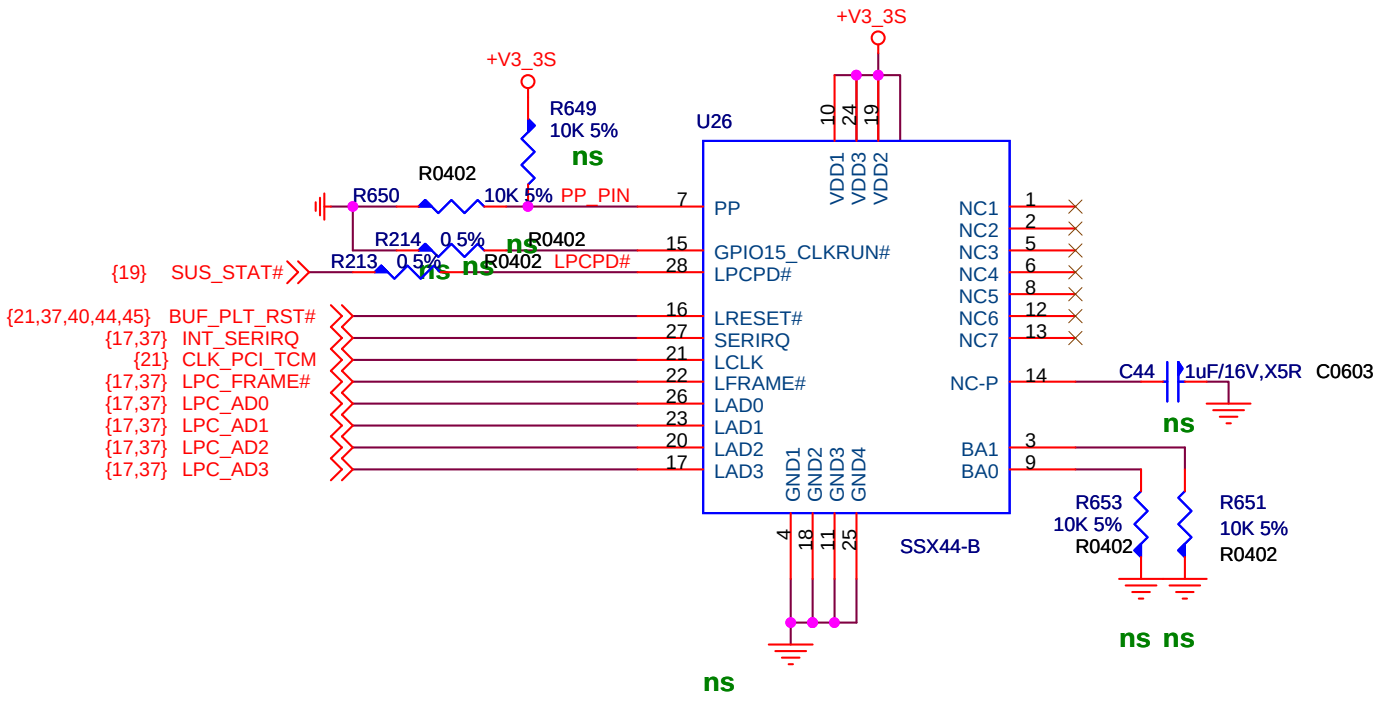

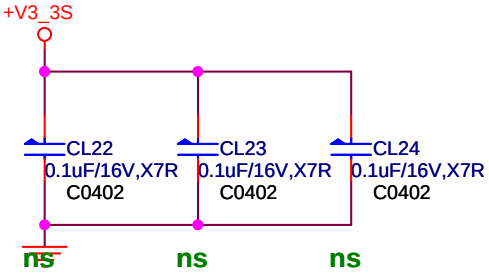

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Title: Flash ROM/SPI		
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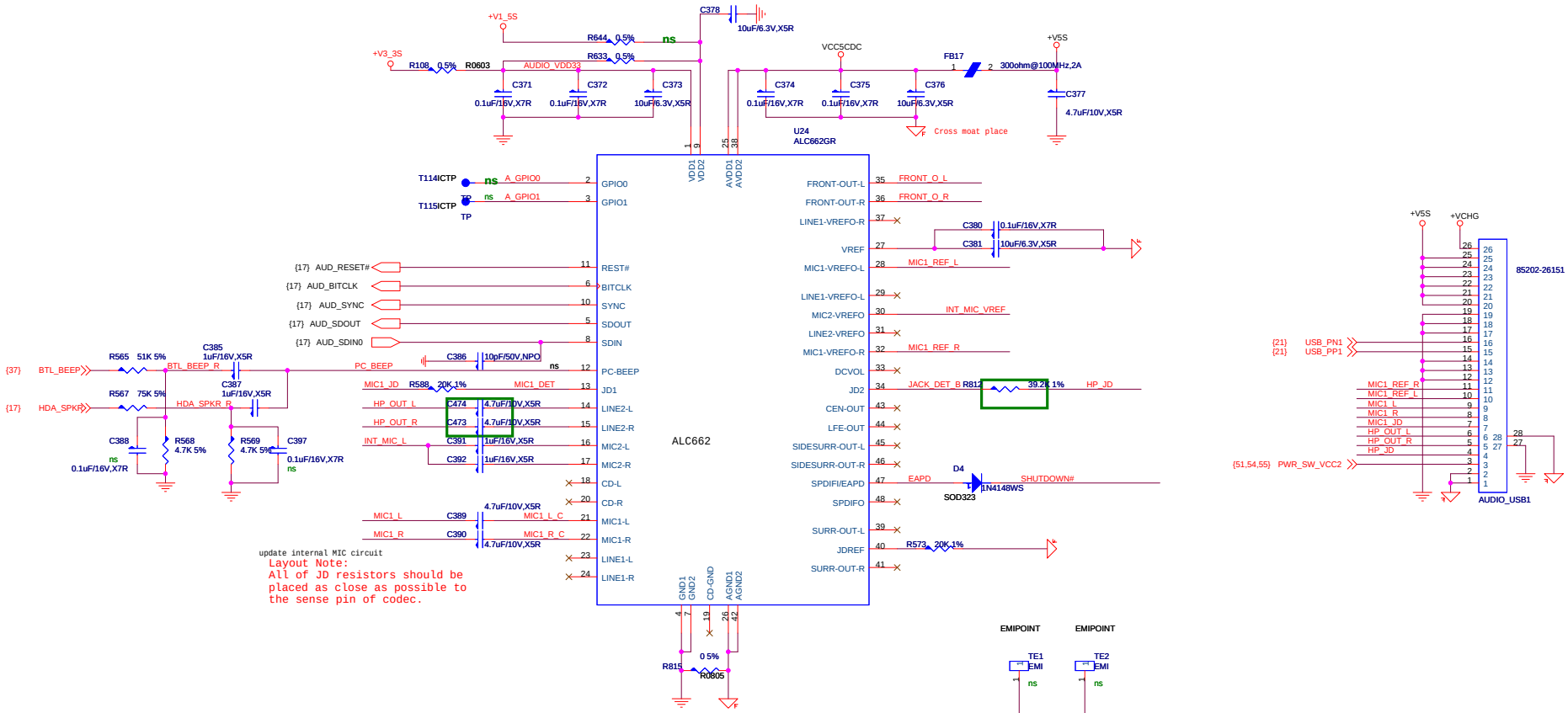
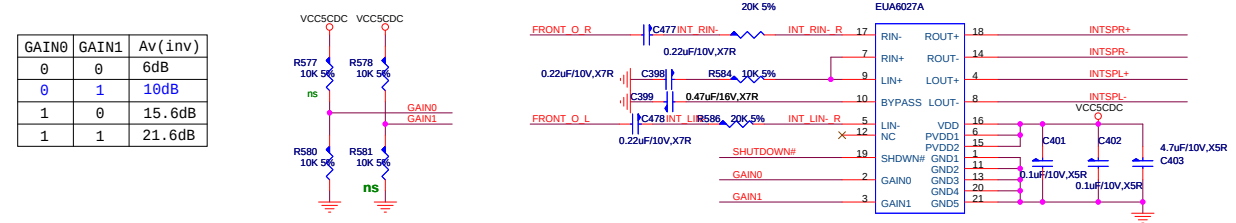
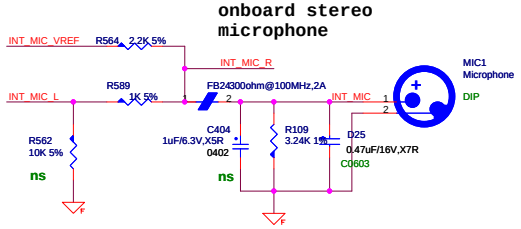
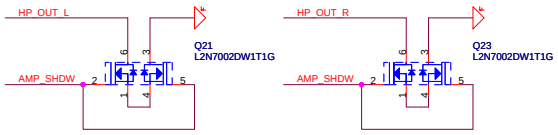
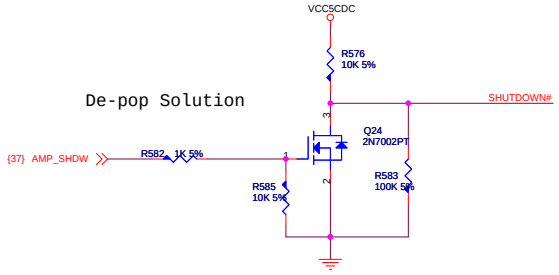


GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB









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Title: ALC662 Audio CODEC	
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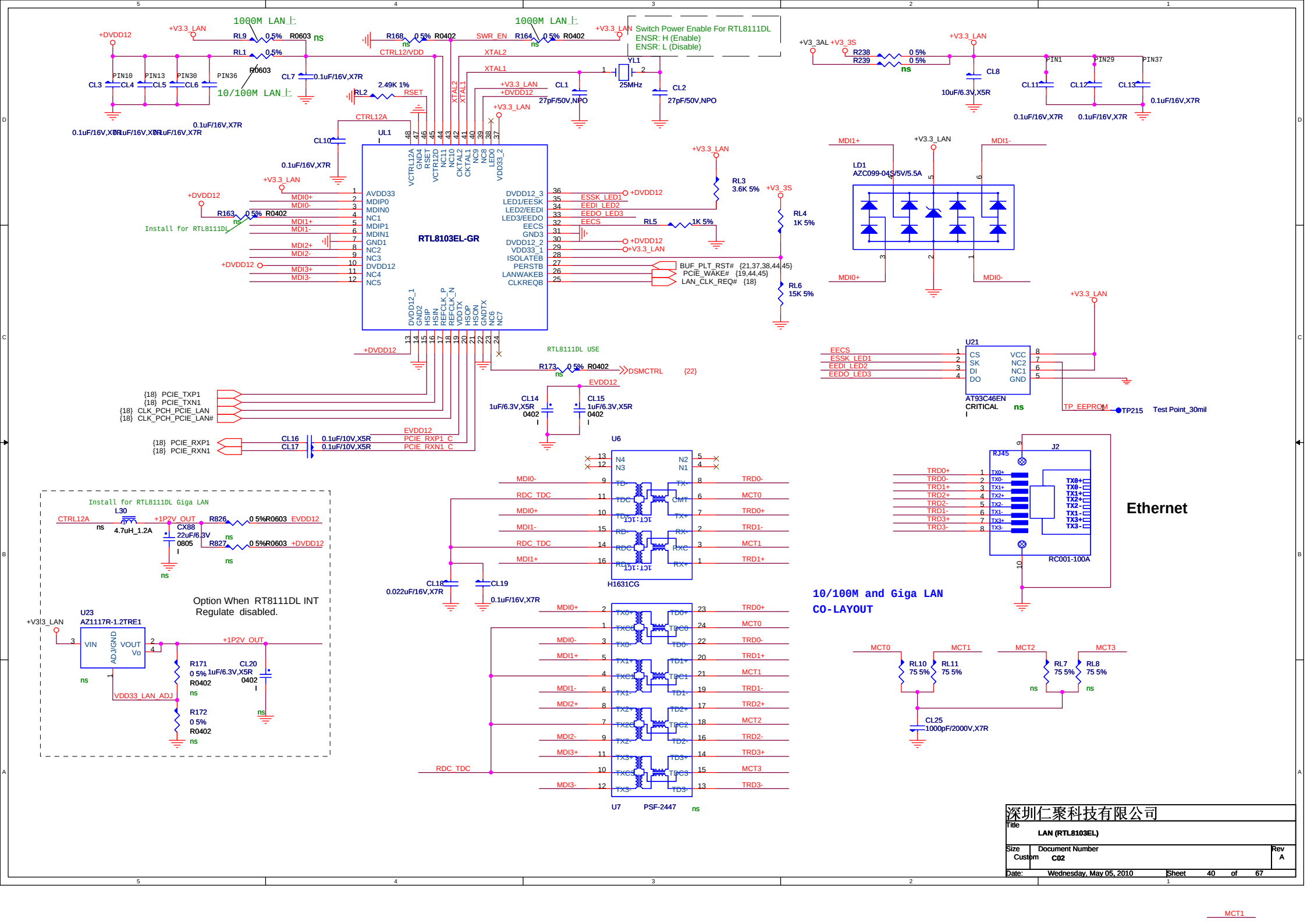
1000M LAN
10/100M LAN
Switch Power Enable For RTL8111DL
ENSR: H (Enable)
ENSR: L (Disable)
RTL8103EL-GR
RTL8111DL USE
Install for RTL8111DL
Install for RTL8111DL Giga LAN
Option When RT8111DL INT Regulate disabled.
Ethernet
10/100M and Giga LAN
CO-LAYOUT
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LAN (RTL8103EL)
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Title: RJ11		
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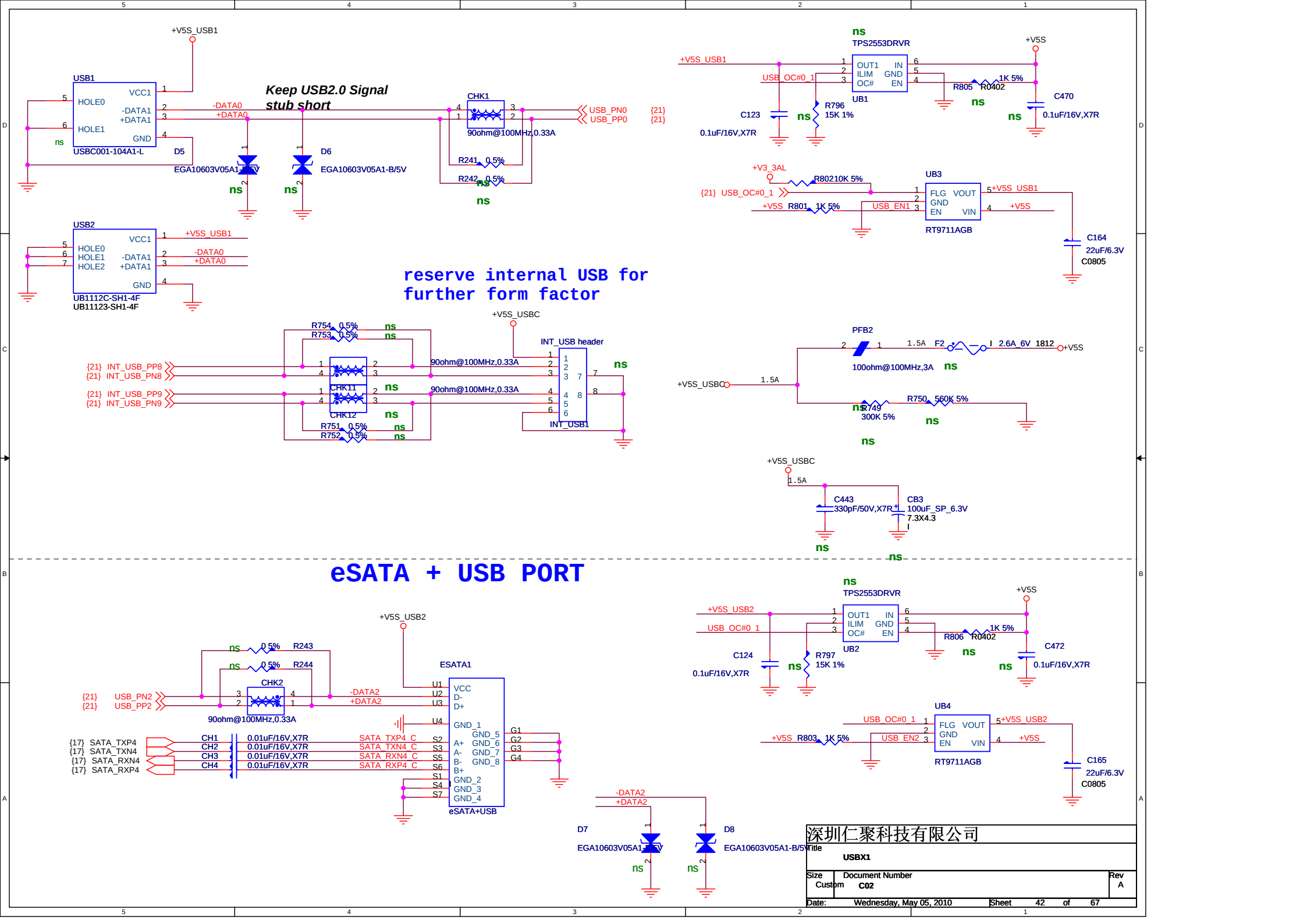
Keep USB2.0 Signal stub short
reserve internal USB for further form factor
eSATA + USB PORT
USB1
USBC001-104A1-L
USB2
UB1112C-SH1-4F
UB11123-SH1-4F
CHK1
90ohm@100MHz,0.33A
D5
D6
EGA10603V05A1-B/5V
TPS2553DRVR
UB1
UB3
RT9711AGB
INT_USB header
INT_USB1
CHK11
CHK12
PFB2
100ohm@100MHz,3A
ESATA1
eSATA+USB
CHK2
UB2
UB4
D7
D8
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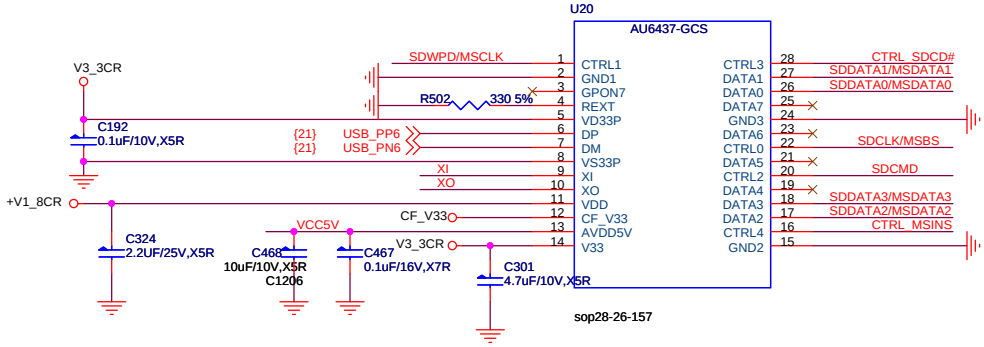
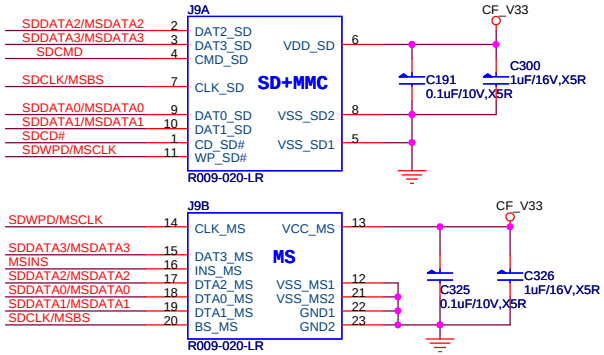
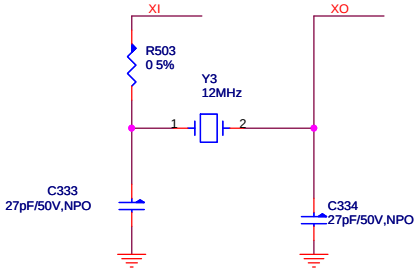
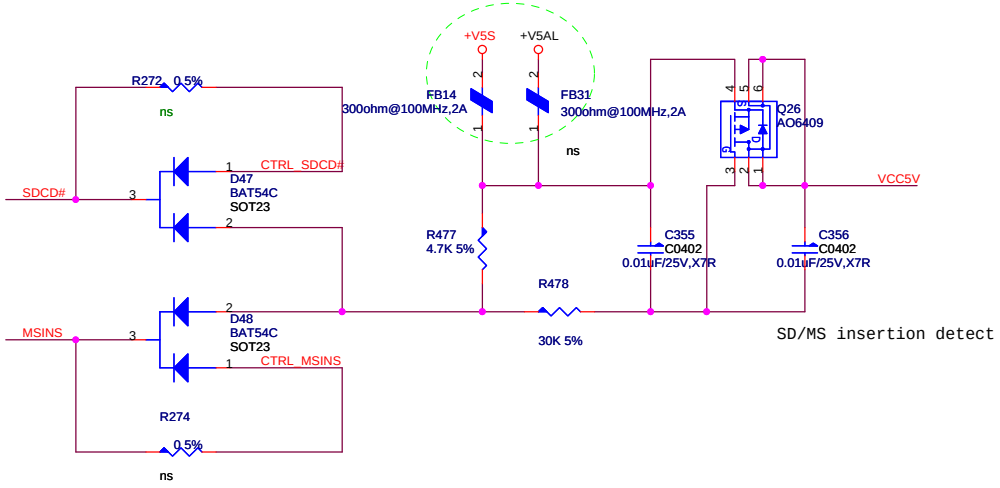
OLD 4IN1 CONN.









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Title: Card Reader		
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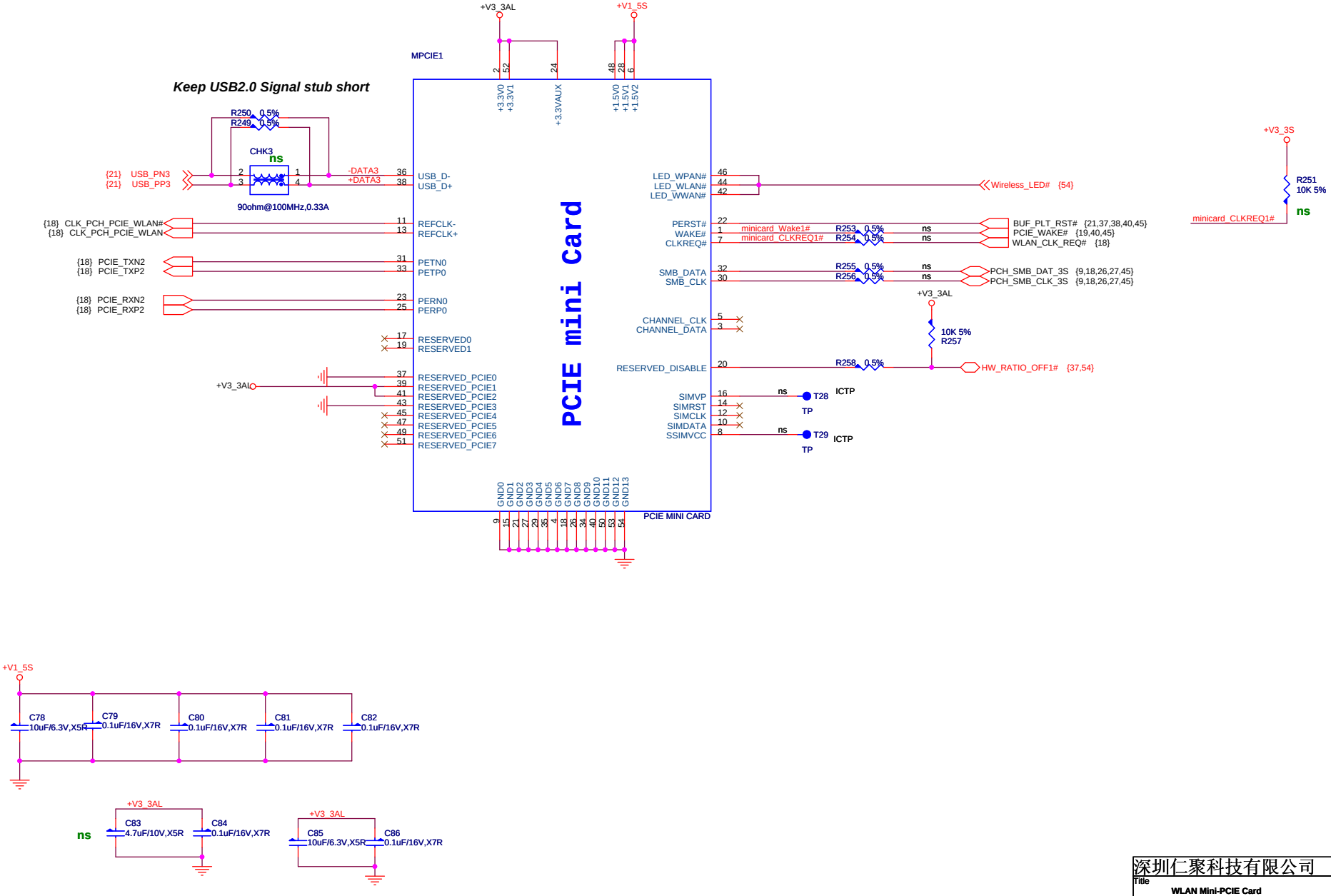

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Title: WLAN Mini-PCIE Card		
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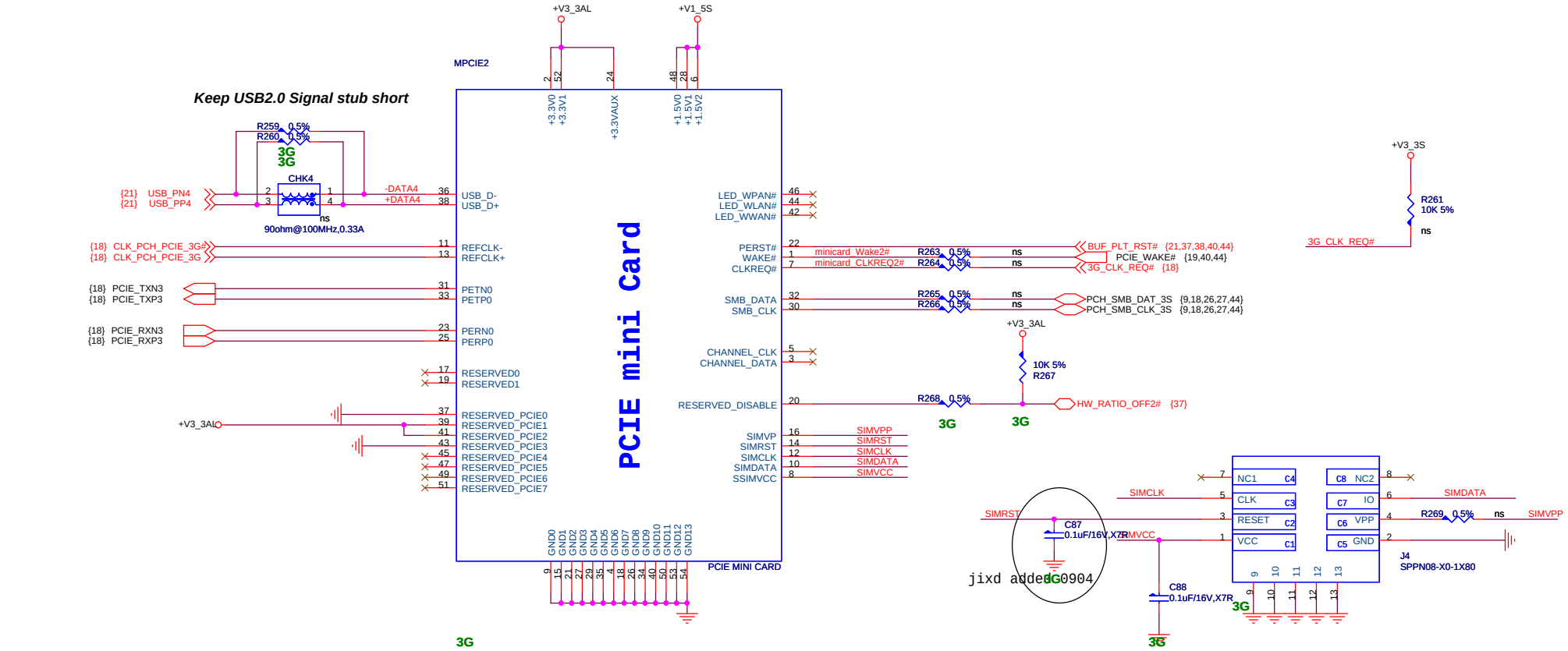
Date: Wednesday, May 05, 2010	Sheet 44 of 67	



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Title: Mini-PCIe(WWAN)		
Size: A3	Document Number: C02	Rev: A
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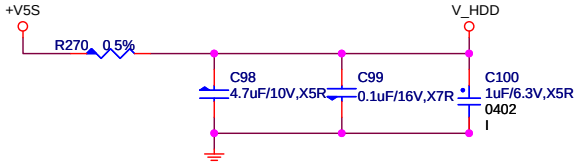
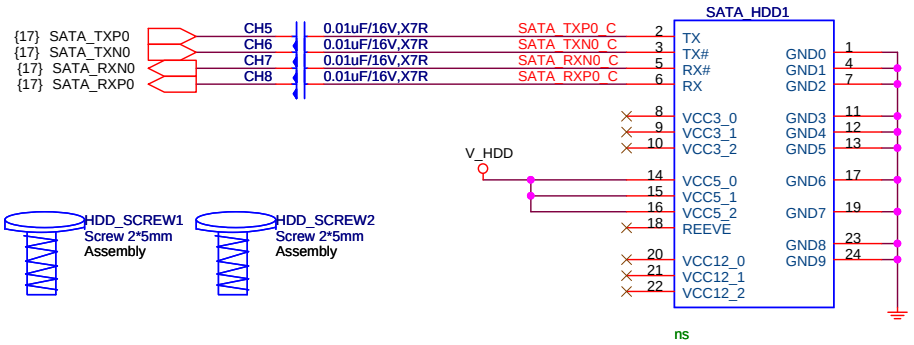
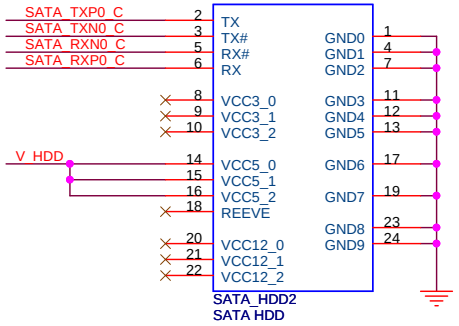
SATA HDD CONN

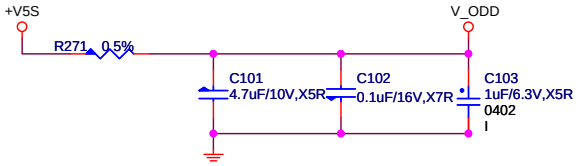


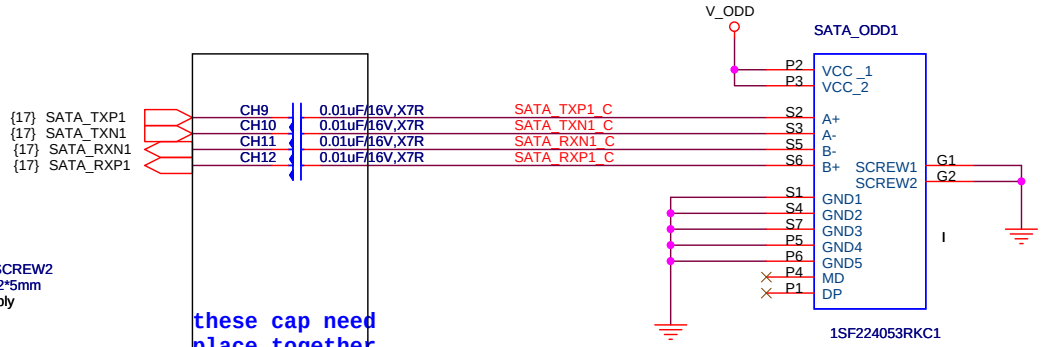


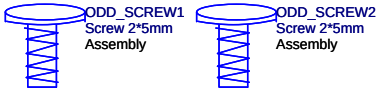
SATA_HDD1和SATA_HDD2 Co-Layout



SATA ODD CONN

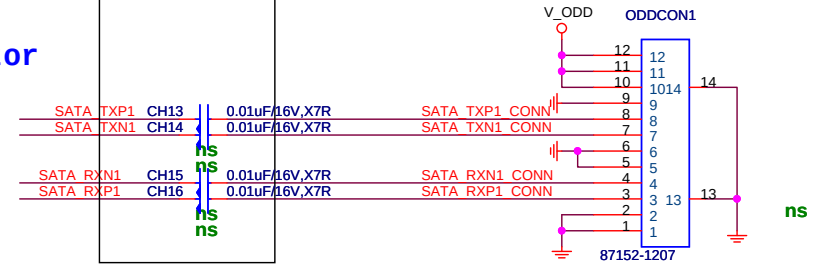






these cap need
place together

Reserve for more form factor



Power pin current
max. 1300 mA (less 2ms)

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Title: SATA HDD/ODD		
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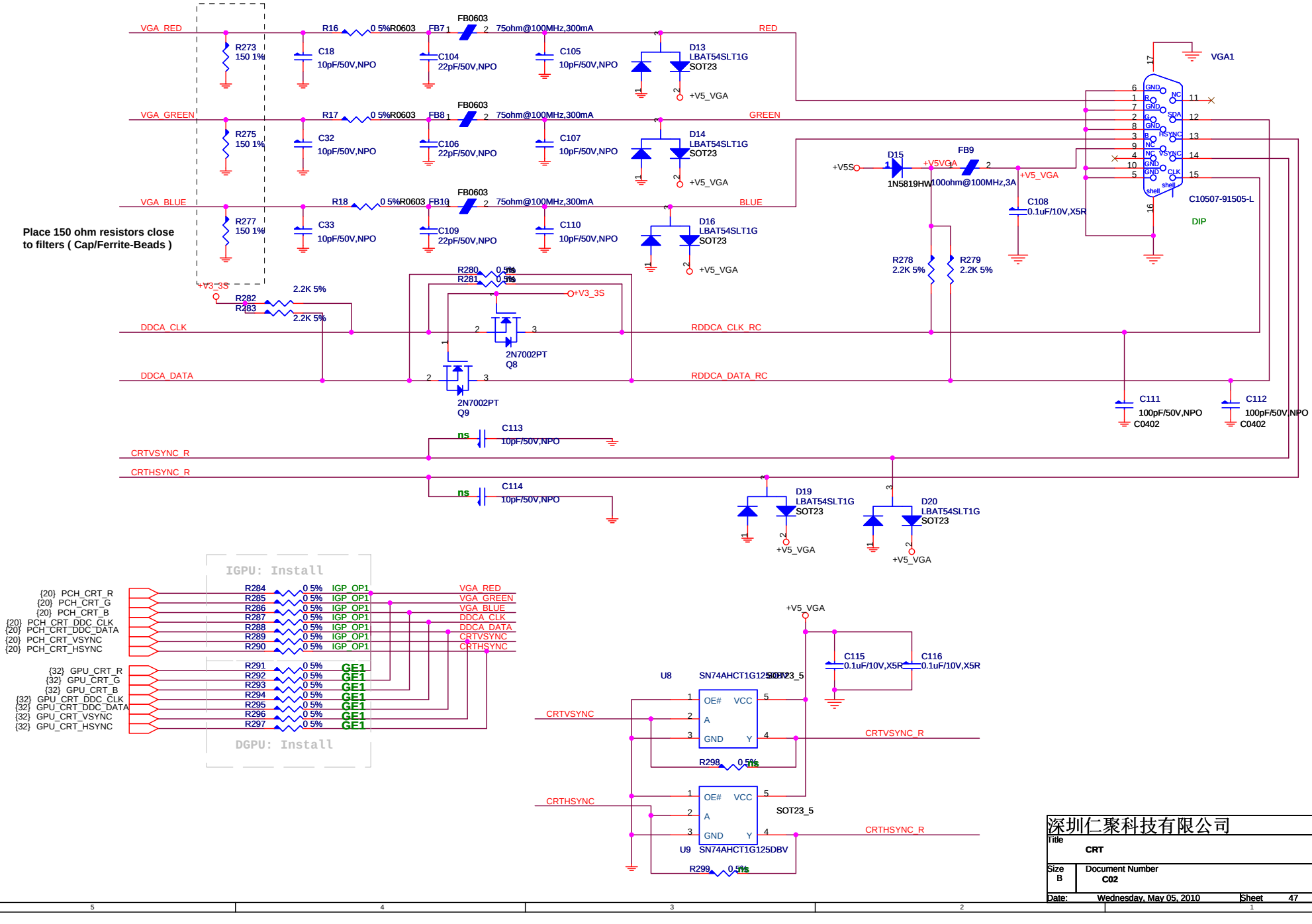

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Title: CRT		
Size: B	Document Number: C02	Rev: A
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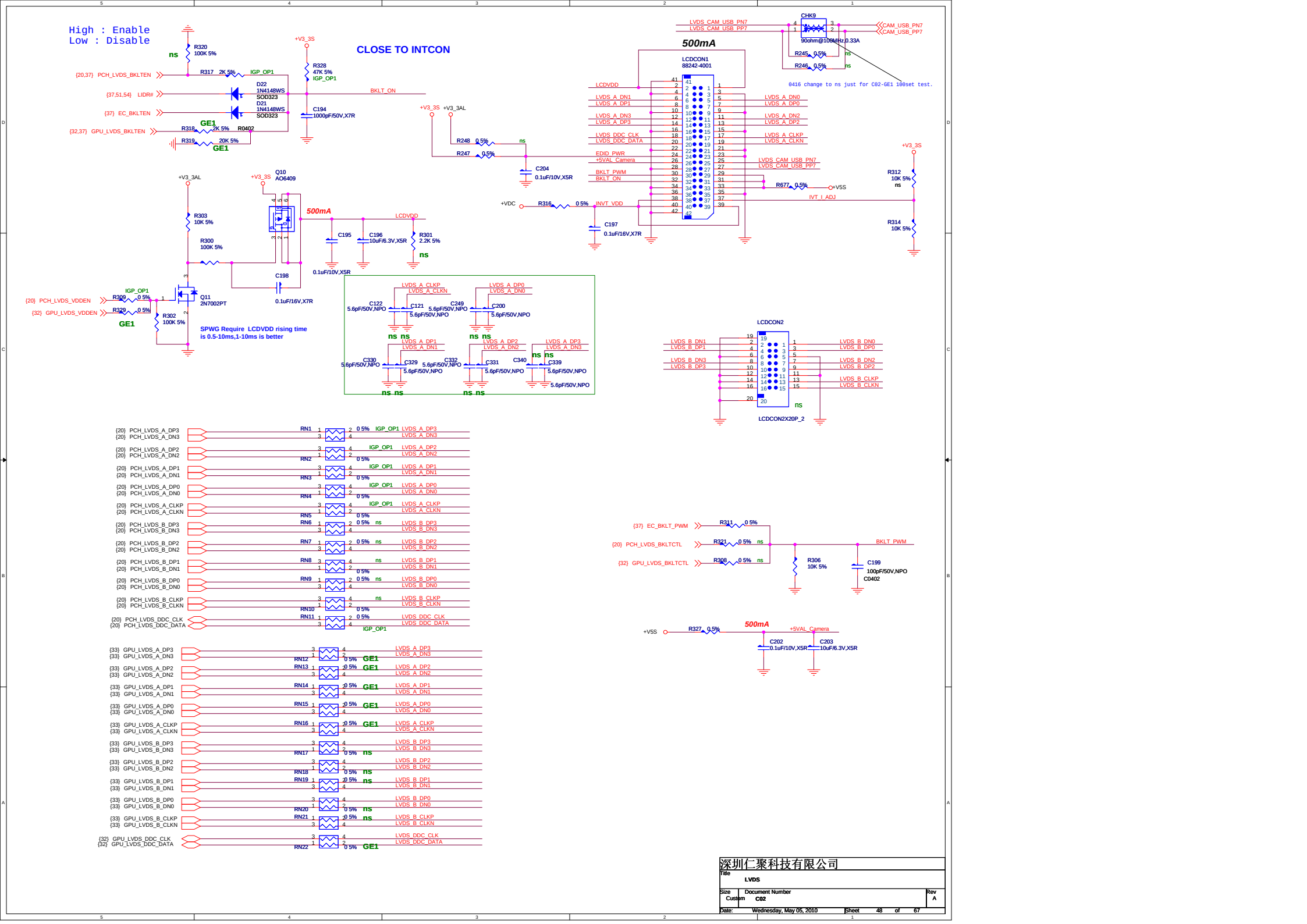
High : Enable
Low : Disable
CLOSE TO INTCON
500mA
0416 change to ns just for C02-GE1 100set test.
SPWG Require LCDVDD rising time is 0.5-10ms,1-10ms is better
LCDCON1 88242-4001
LCDCON2
LCDCON2X20P_2
CHK9
90ohm@100MHz,0.33A
深圳仁聚科技有限公司
Title LVDS
Size Custom
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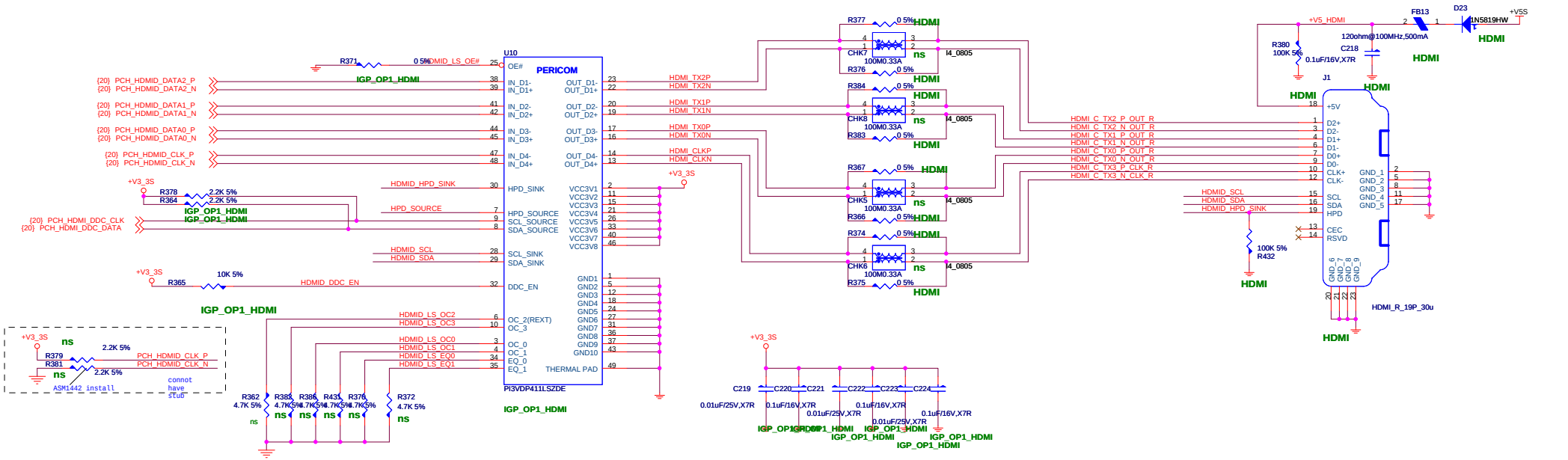

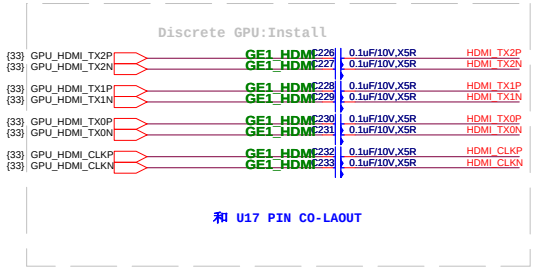

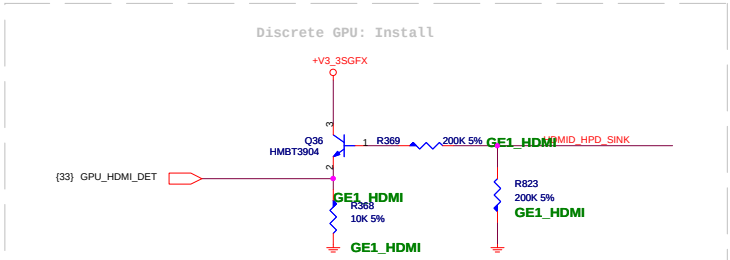

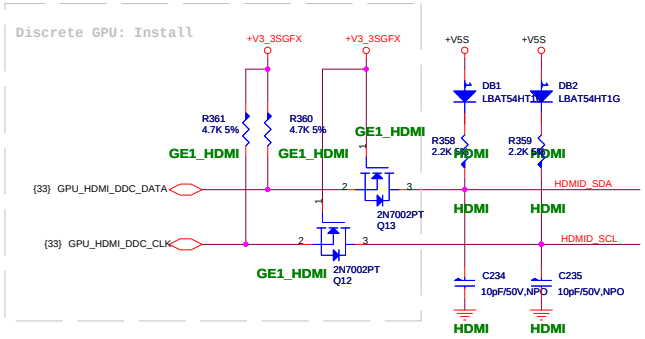

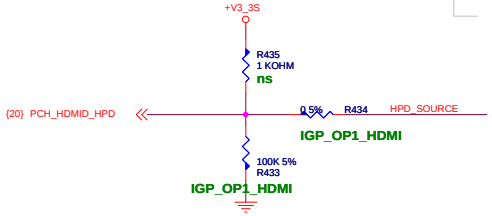

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Title	HDMI	
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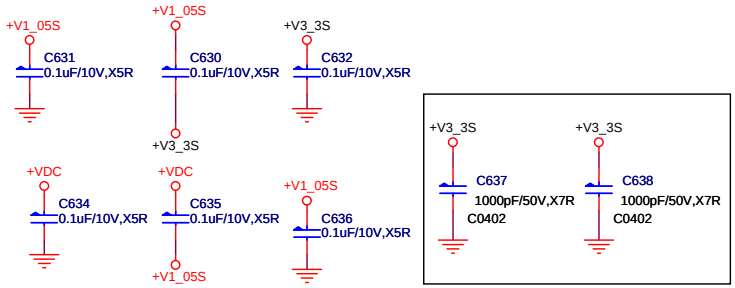

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Title: GPU Option		
Size: B	Document Number: C02	Rev: A
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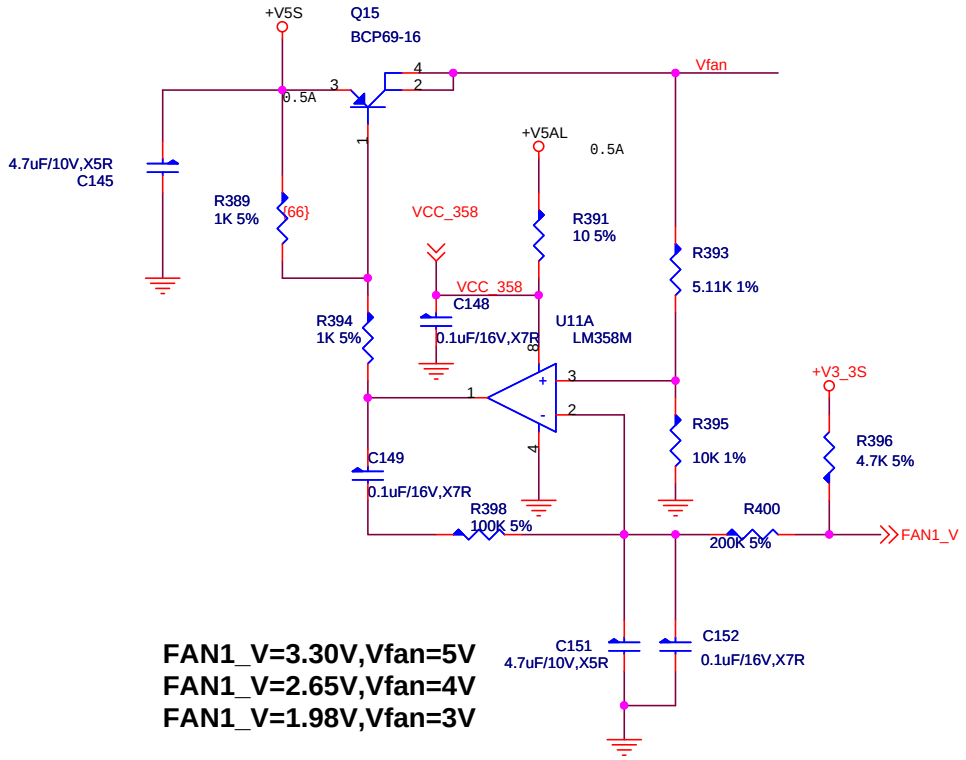

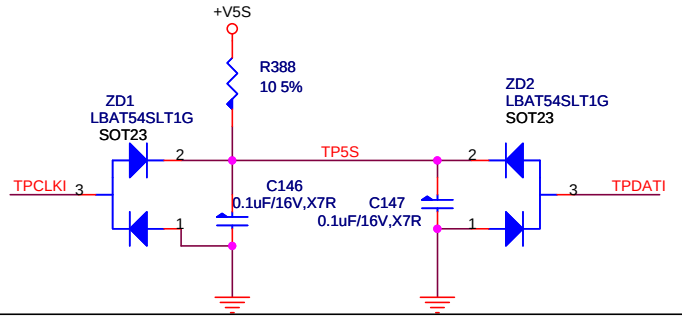

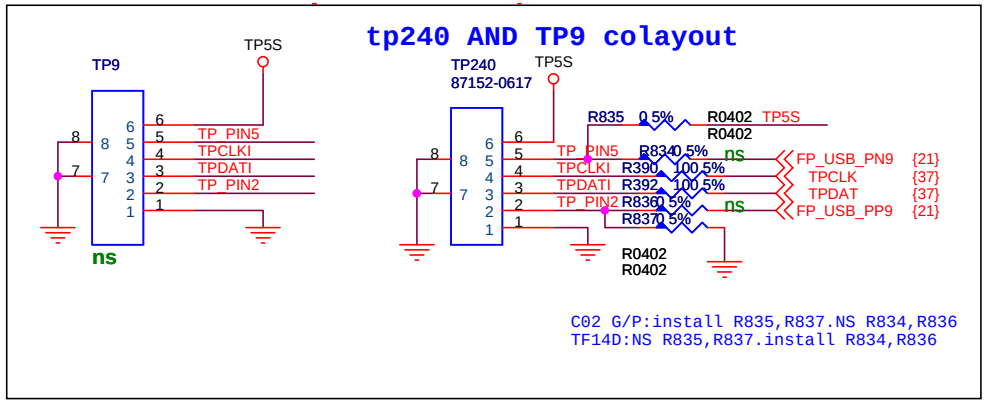

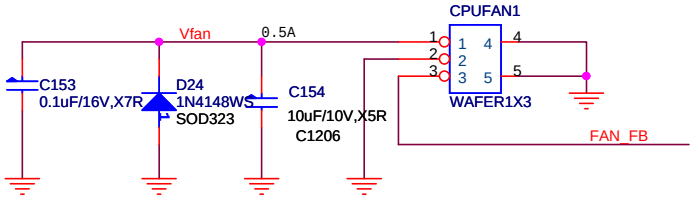

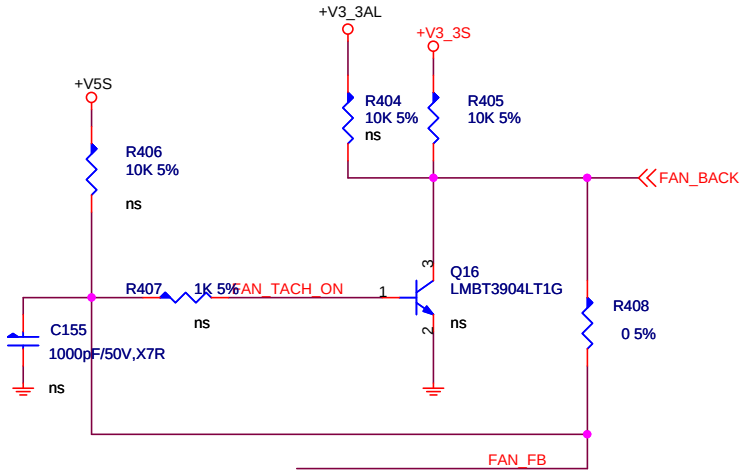

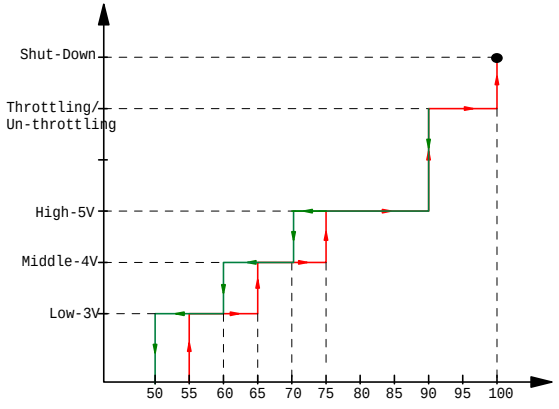

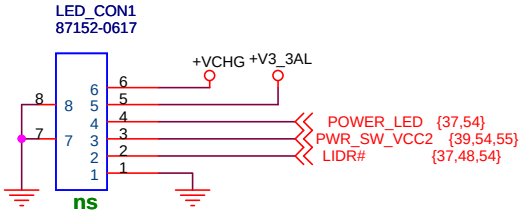

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Title: FAN		
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Title
EXPRESS CARD

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Title: FAN/Thermal Sensor		
Size: Custom	Document Number: C02	Rev: A
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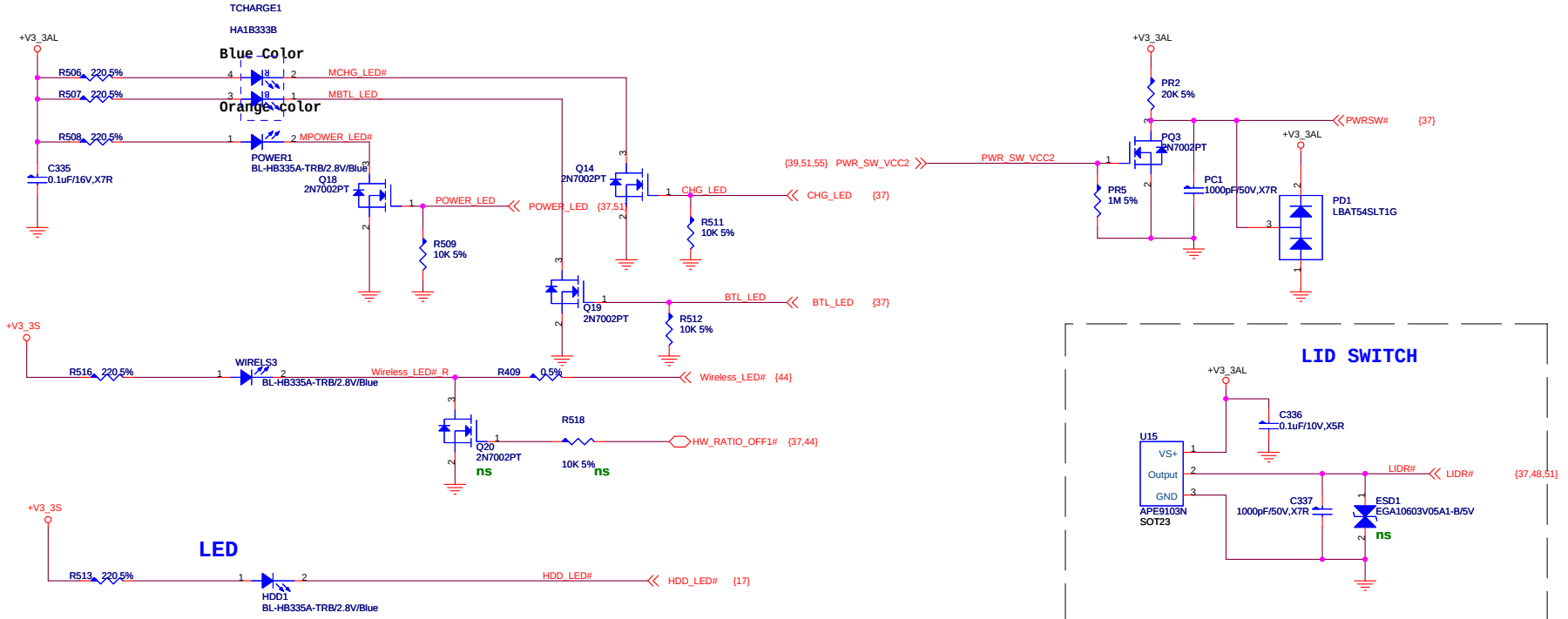

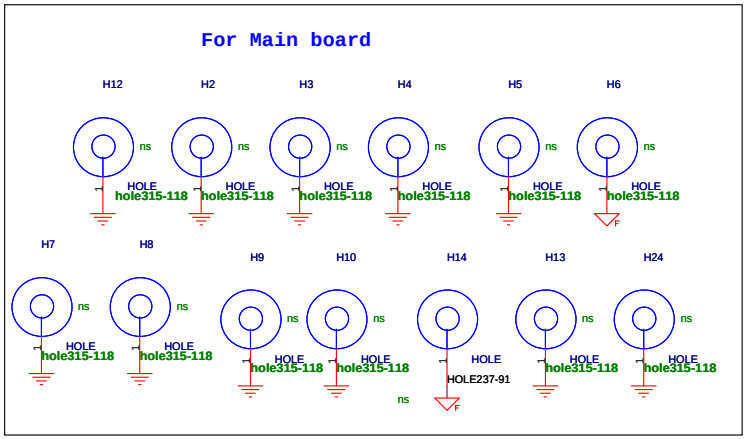

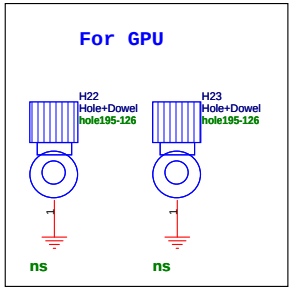

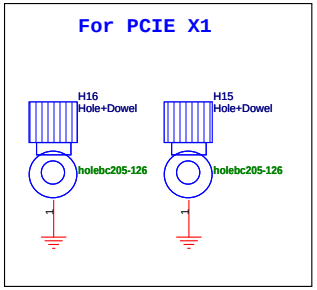

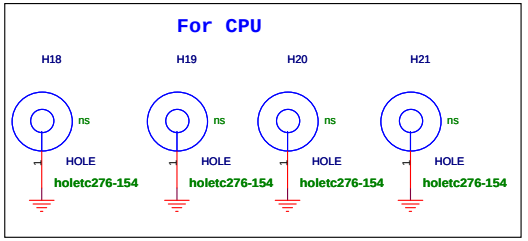

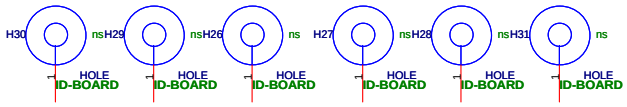

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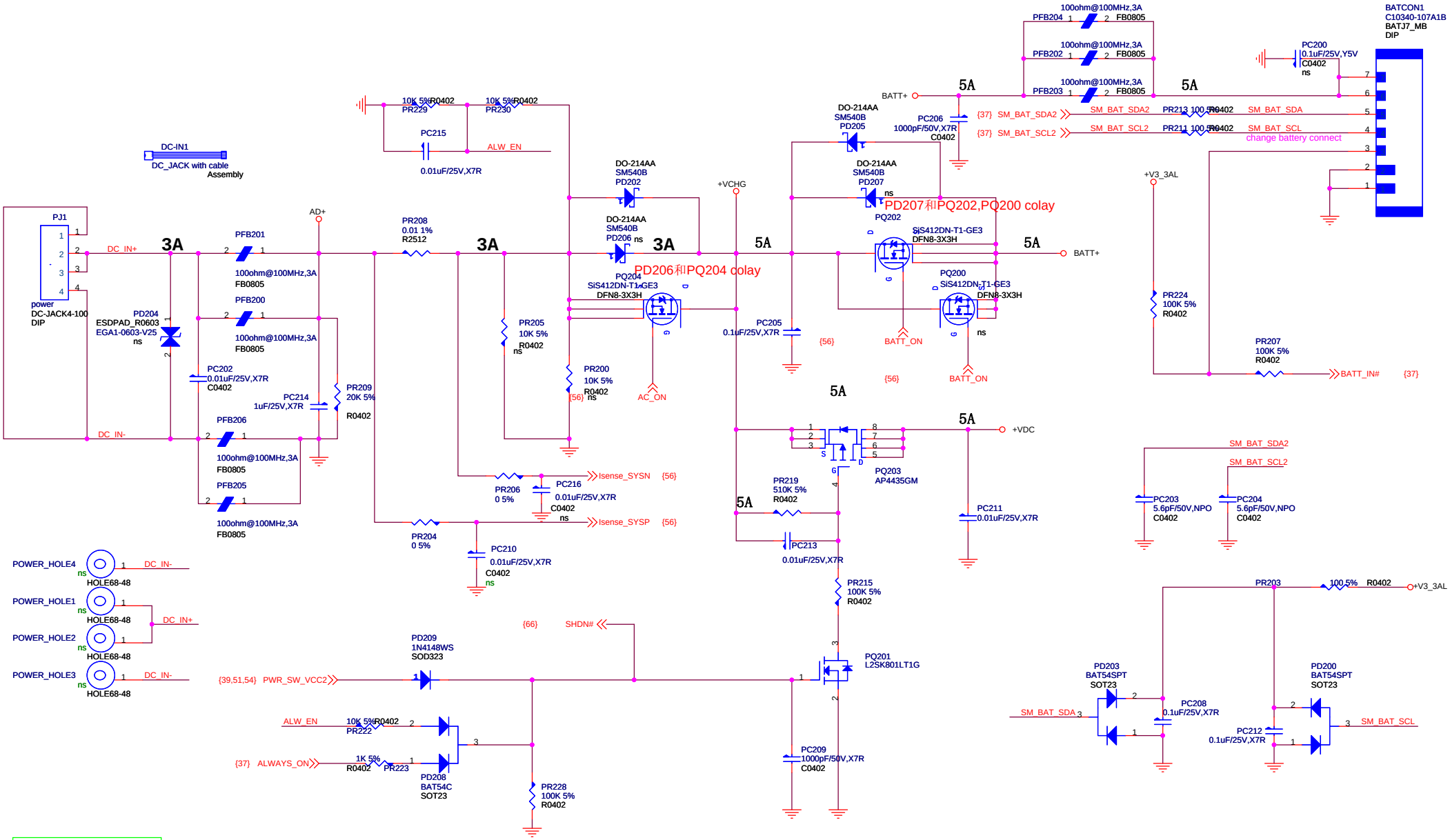
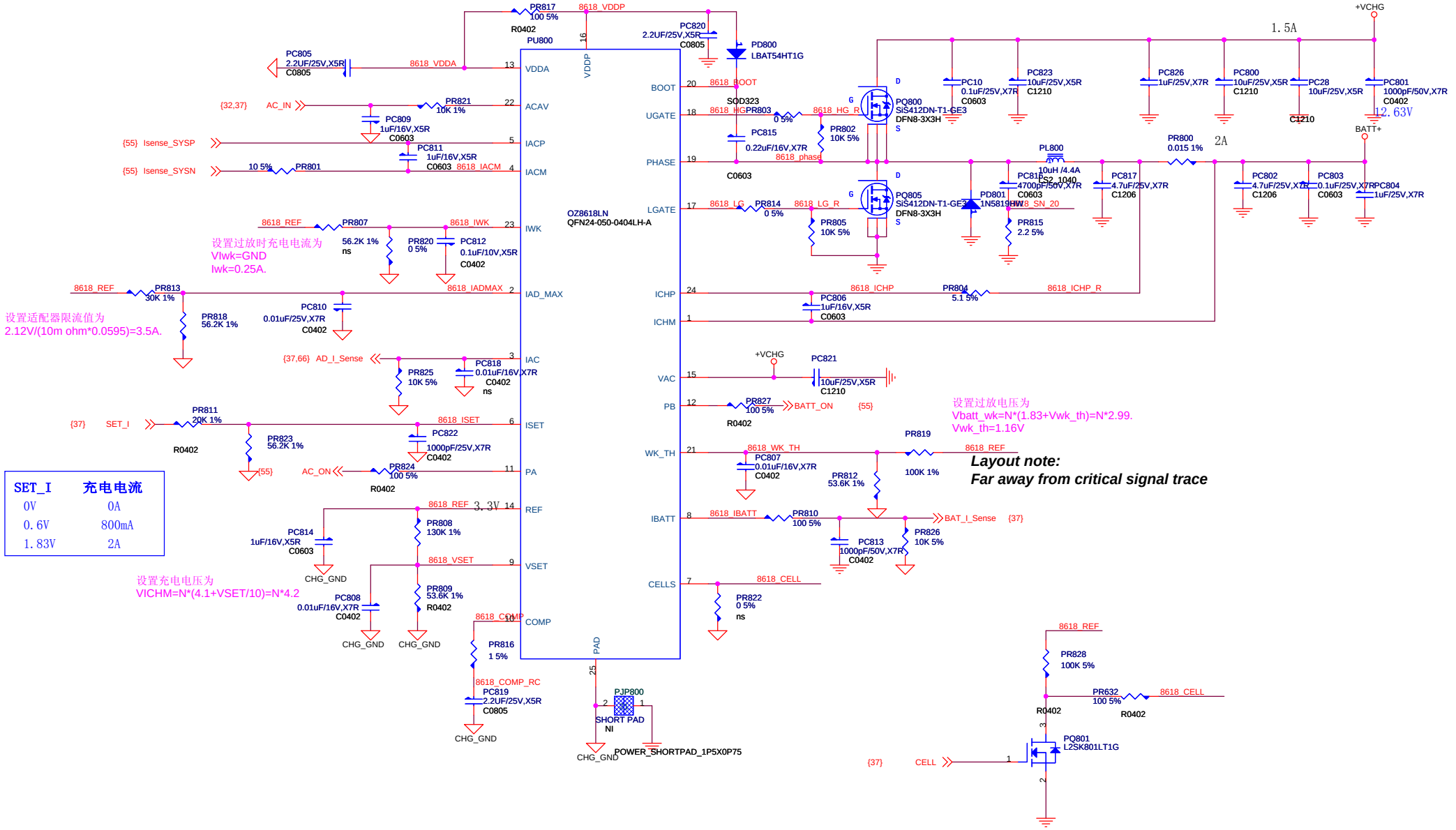
Title: Power Button Board/LED		
Size: Custom	Document Number: C02	Rev: A
Date: Wednesday, May 05, 2010	Sheet 54 of 67	



Title	AC IN& Battery	
Size A3	Document Number C02	Rev A
Date: Wednesday, May 05, 2010	Sheet 55 of 67	



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Title	CHARGER OZ8618
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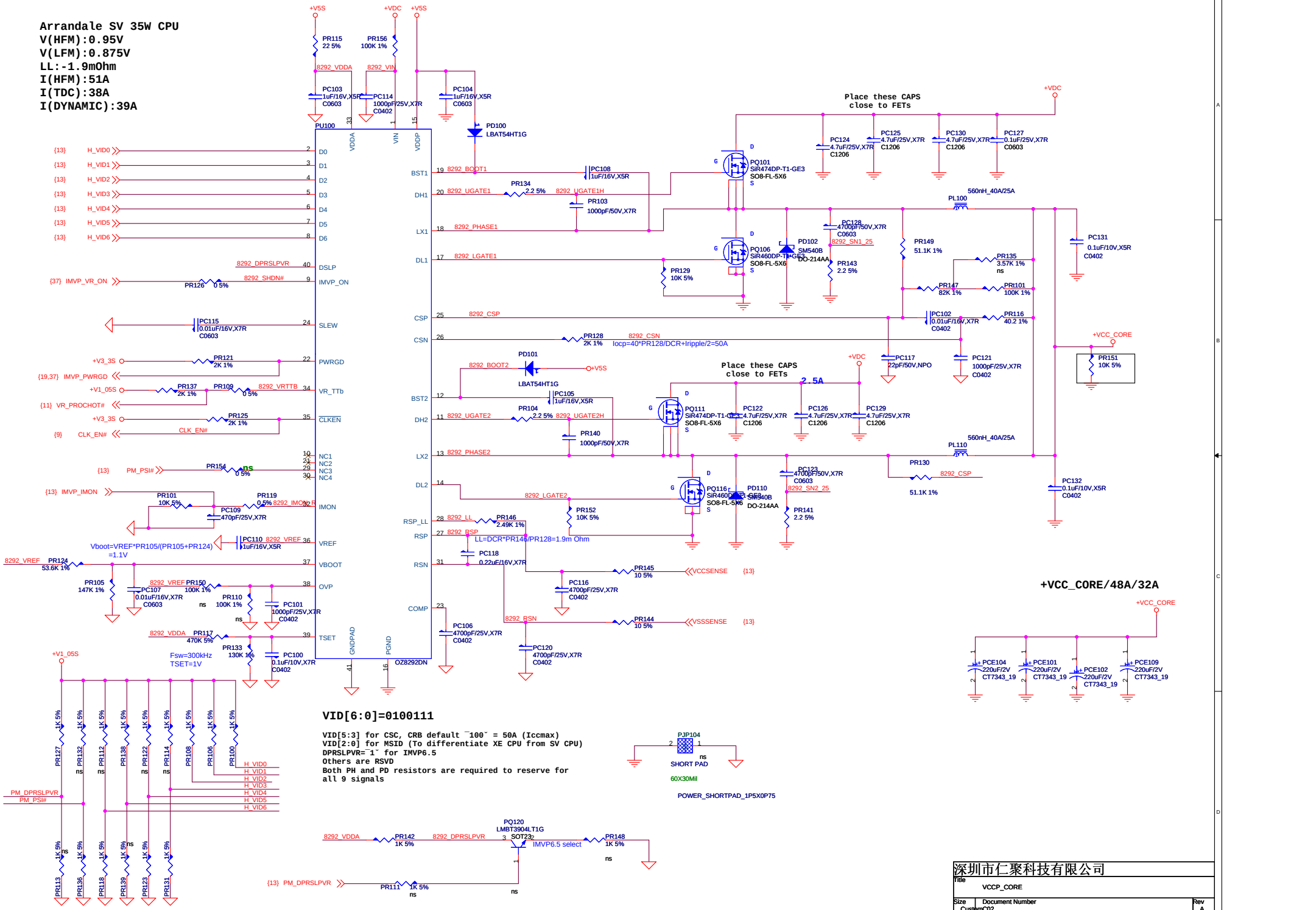
Arrandale SV 35W CPU
V(HFM):0.95V
V(LFM):0.875V
LL:-1.9mOhm
I(HFM):51A
I(TDC):38A
I(DYNAMIC):39A



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Title	VCCP_CORE	
Size: Custom	Document Number: C02	Rev: A
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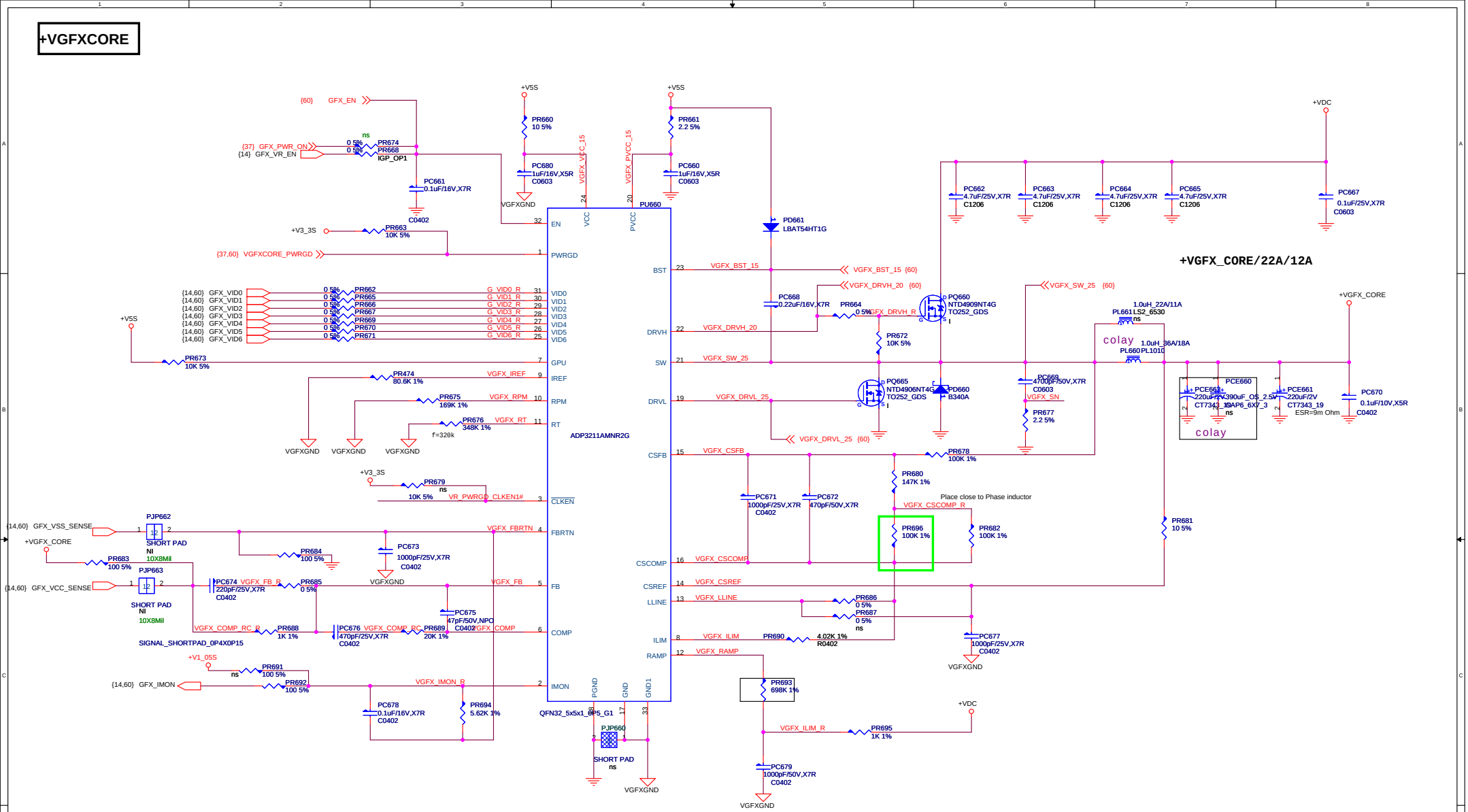
+VGFXCORE



深圳市仁聚科技有限公司

Title	CPU GFX_CORE	
Size: Custom	Document Number: C02	Rev: A
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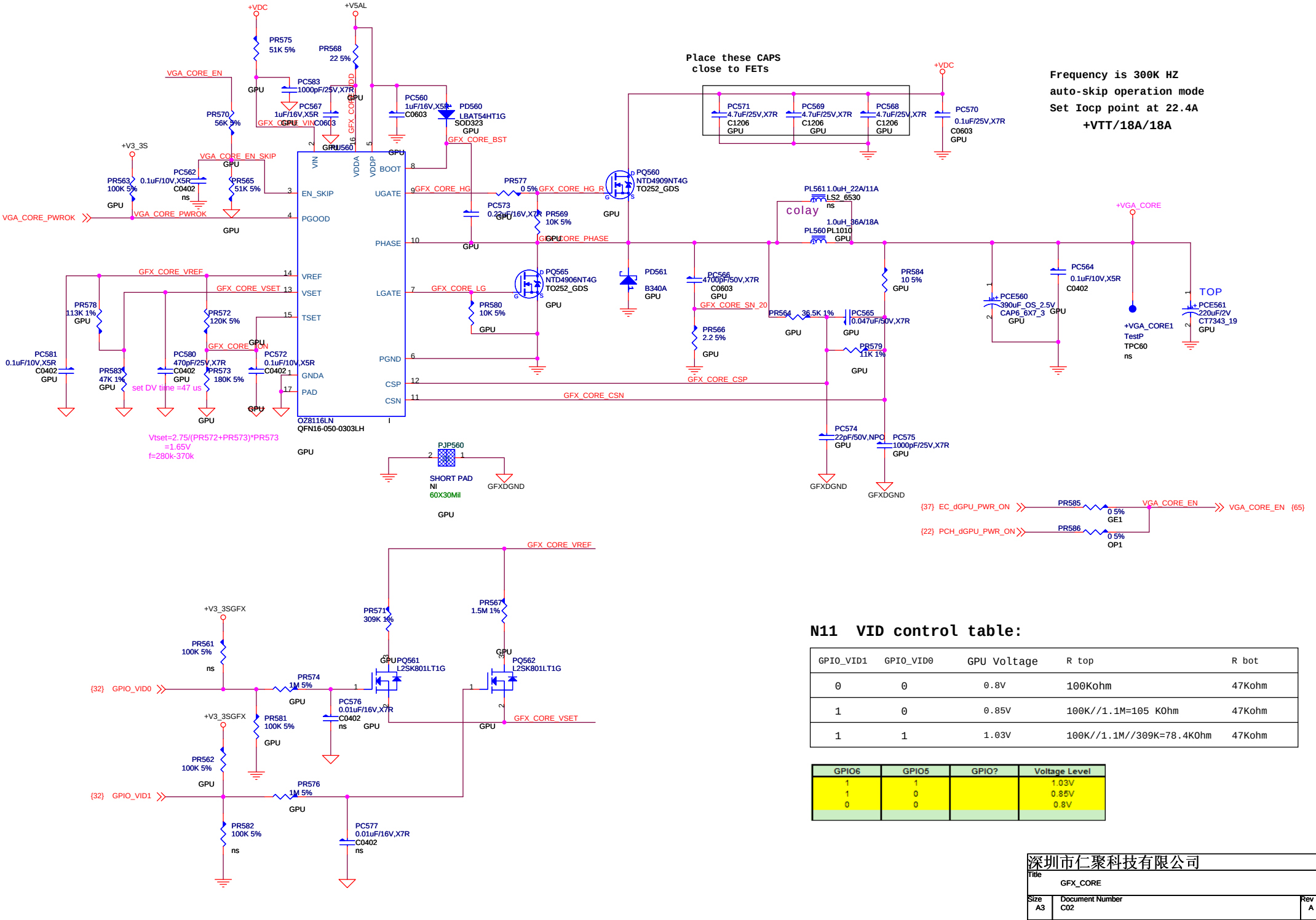

N11 VID control table:

GPIO_VID1	GPIO_VID0	GPU Voltage	R top	R bot
0	0	0.8V	100Kohm	47Kohm
1	0	0.85V	100K//1.1M=105 KOhm	47Kohm
1	1	1.03V	100K//1.1M//309K=78.4KOhm	47Kohm

GPIO6	GPIO5	GPIO?	Voltage Level
1	1		1.03V
1	0		0.85V
0	0		0.8V

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Title: GFX_CORE		
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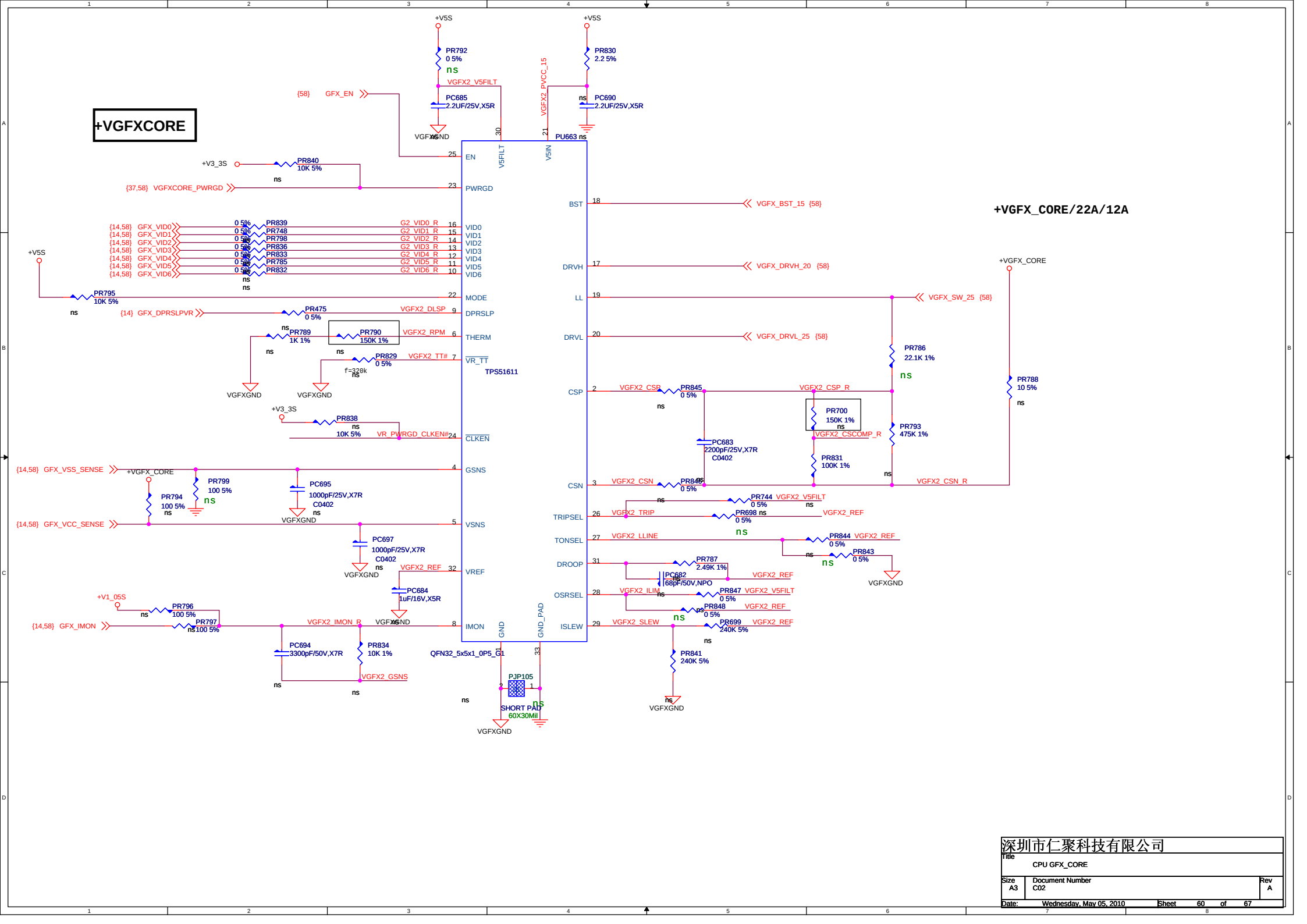

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Title	CPU GFX_CORE	
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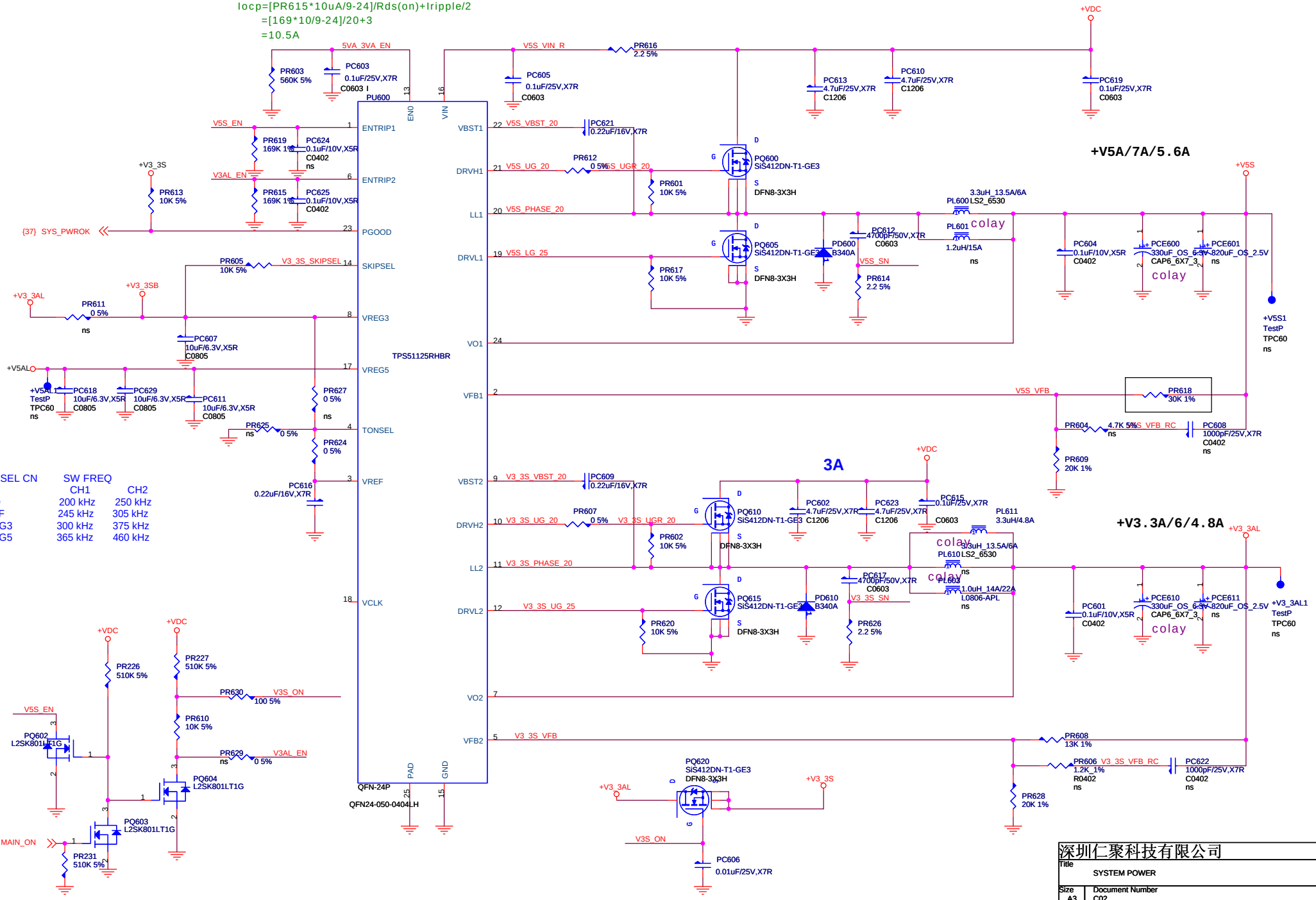
Iocp=[PR619*10uA/9-24]/Rds(on)+Iripple/2
=[169*10/9-24]/20+3
=10.5A

Iocp=[PR615*10uA/9-24]/Rds(on)+Iripple/2
=[169*10/9-24]/20+3
=10.5A



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Title: SYSTEM POWER		
Size: A3	Document Number: C02	Rev: A
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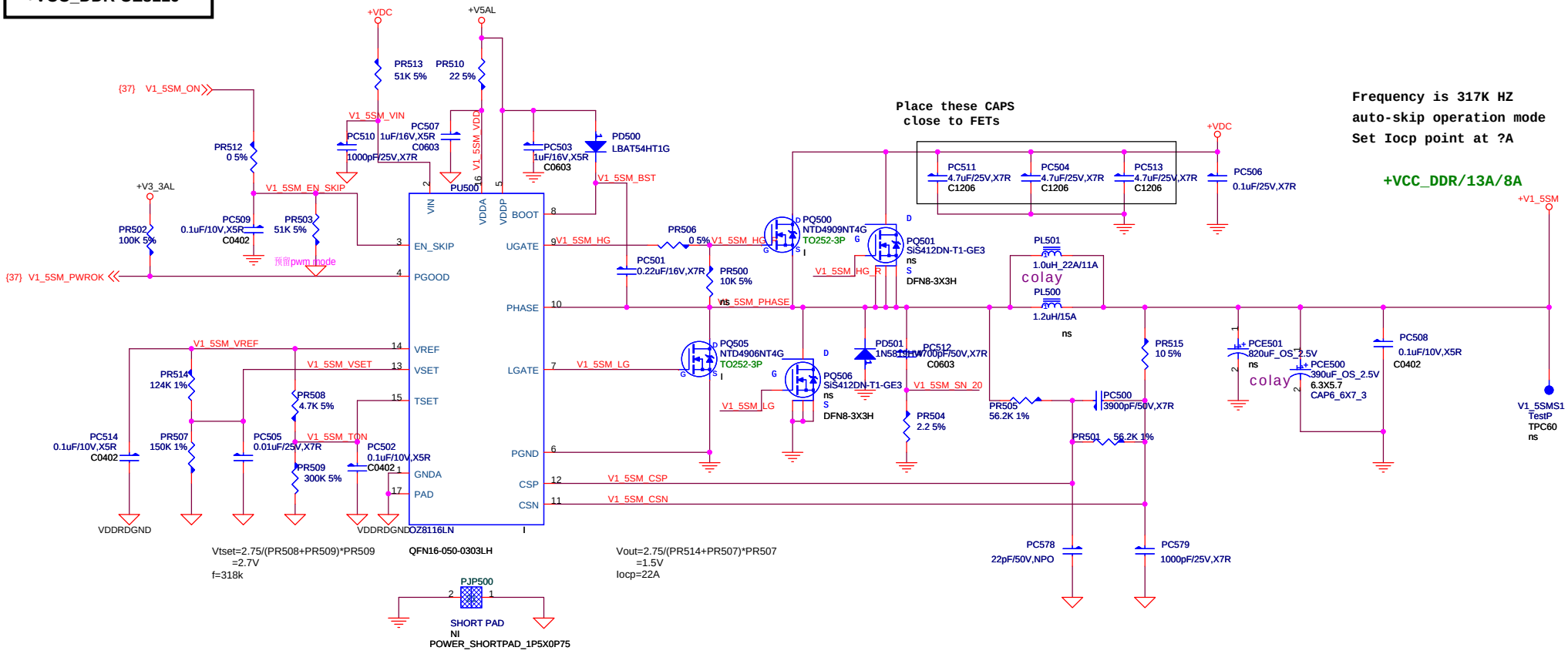
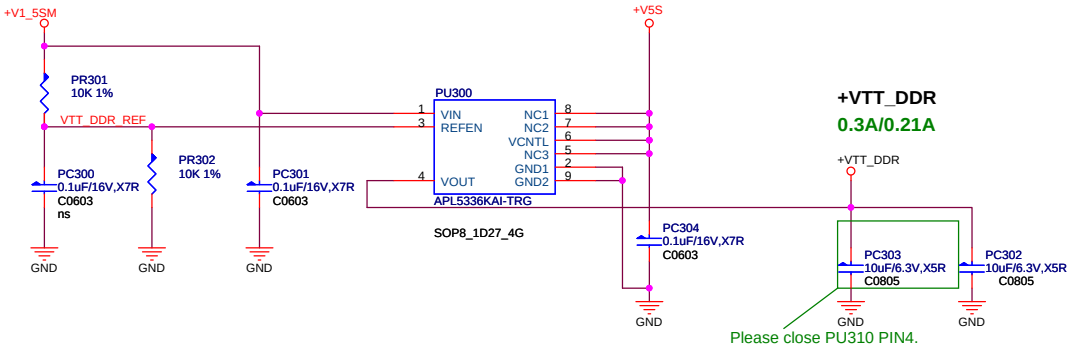
+VCC_DDR OZ8116





深圳仁聚科技有限公司		
Title: +VCC_DDR&+VTT_DDR		
Size: A3	Document Number: C02	Rev: A
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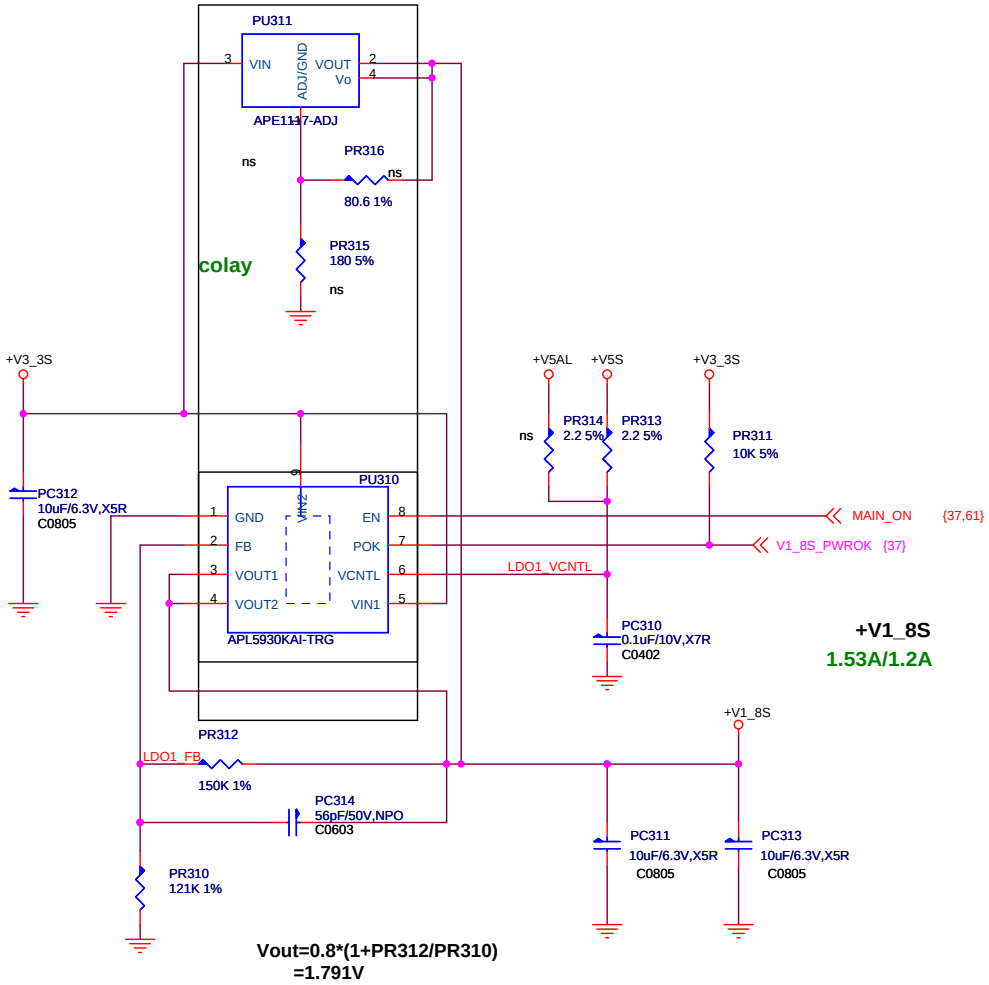
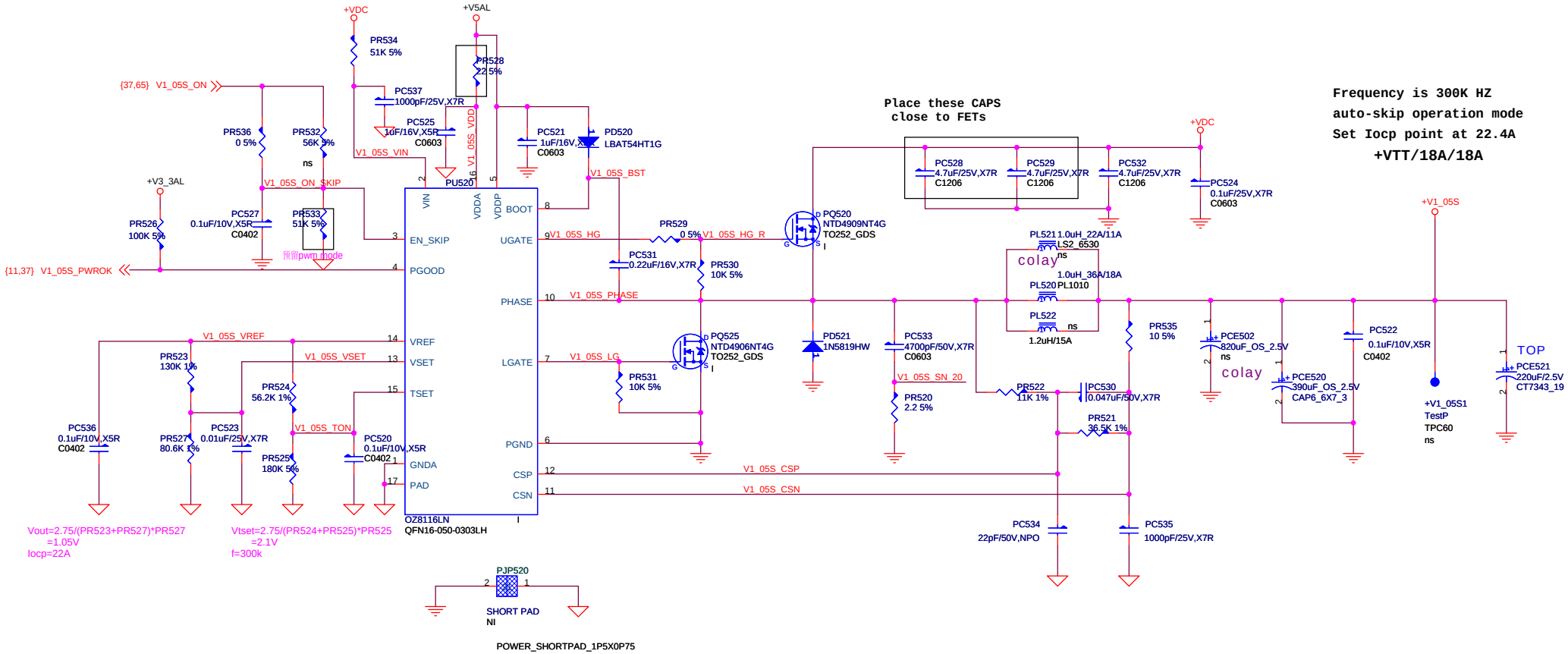


Title	V1_8S	
Size B	Document Number C02	Rev A
Date: Wednesday, May 05, 2010	Sheet 63 of 67	



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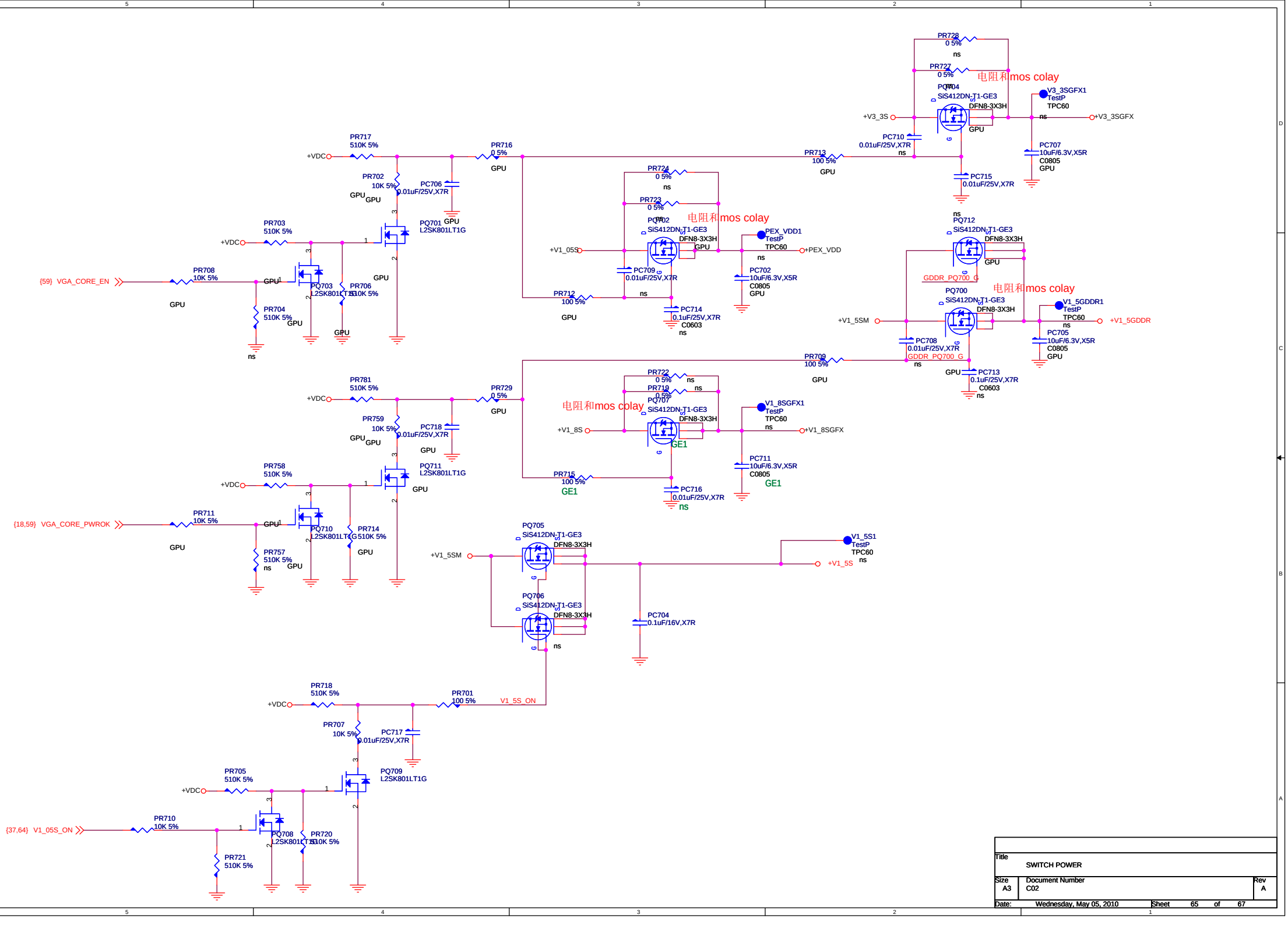
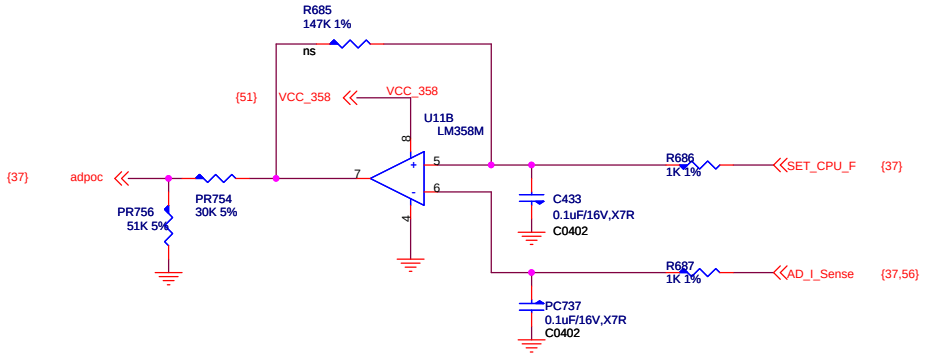
Title	1.05V VTT	
Size A3	Document Number C02	Rev A
Date: Wednesday, May 05, 2010	Sheet 64 of 67	



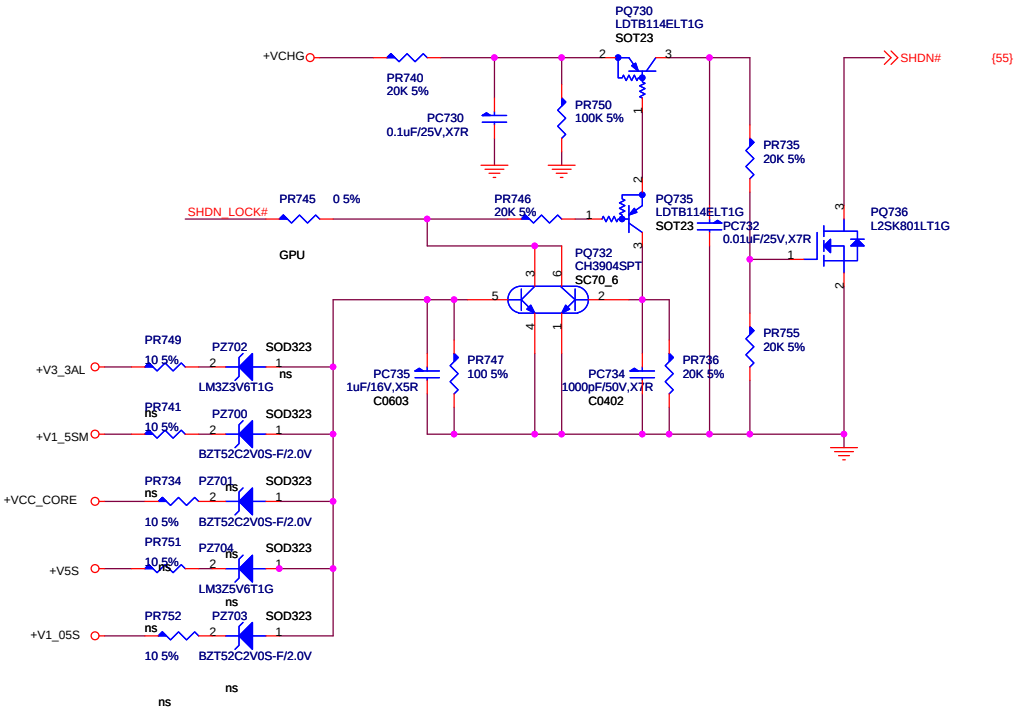
Title	SWITCH POWER	
Size A3	Document Number C02	Rev A
Date: Wednesday, May 05, 2010	Sheet 65 of 67	

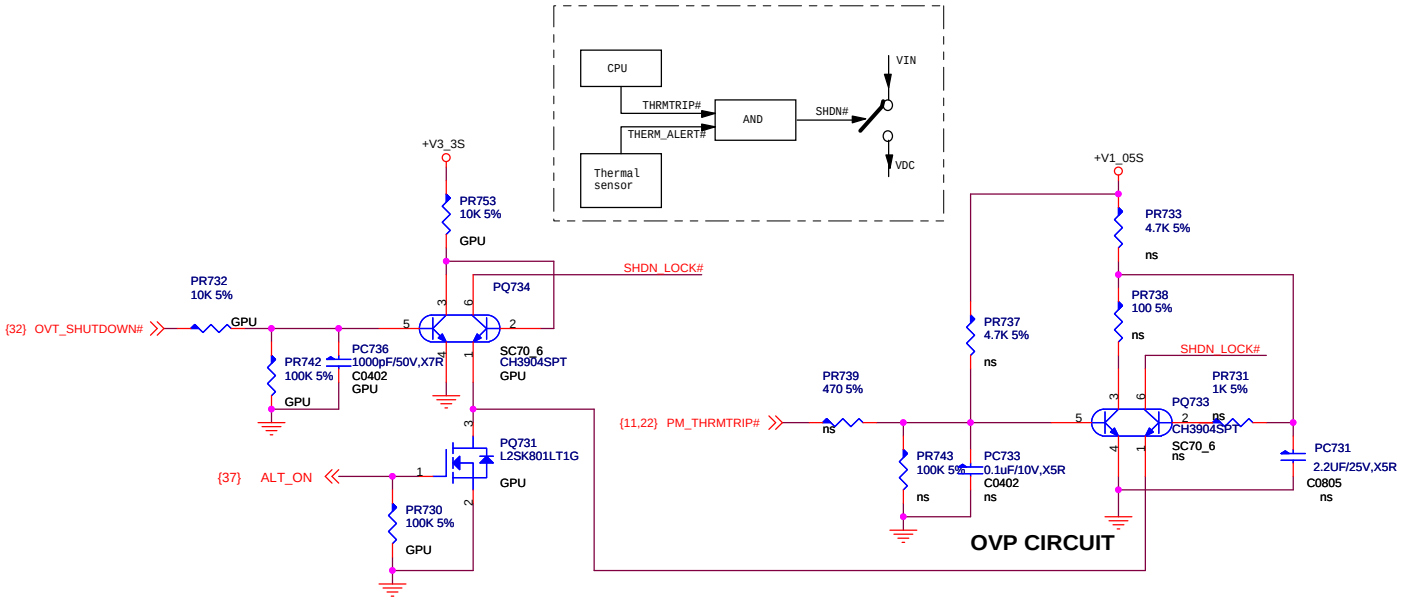


frequency adj for 65W adaptor

SET_CPU_F	AD_I_Sense	adpoc
2V	>2V(3.33A)	low(0V)
1.65V	<1.65V(2.75A)	high(3V)

OVP CIRCUIT





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Title	OVP&OTP	
Size A3	Document Number C02	Rev A
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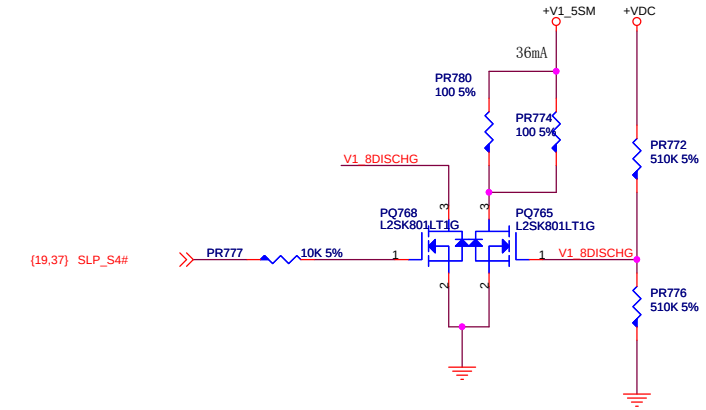
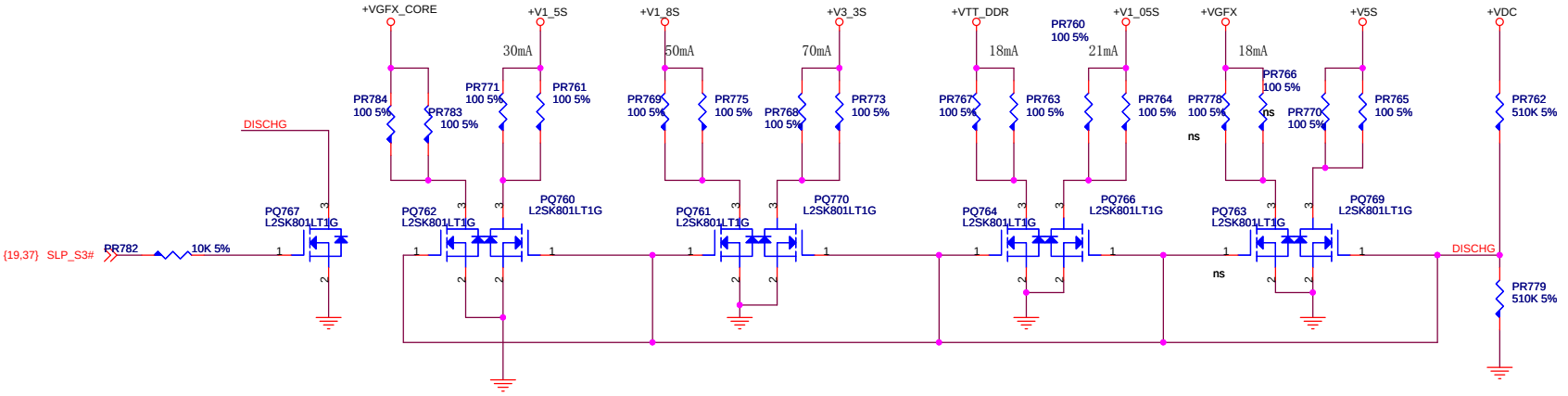


LZJ0819vb: Add +V5S
discharge circuit.



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Title: SYSTEM DISCHARGE		
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