PCB Number : (4 Layer)

Project Name: Bolton195i_BSW
Project Code: 3PD042010001

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Title	Cover Page	
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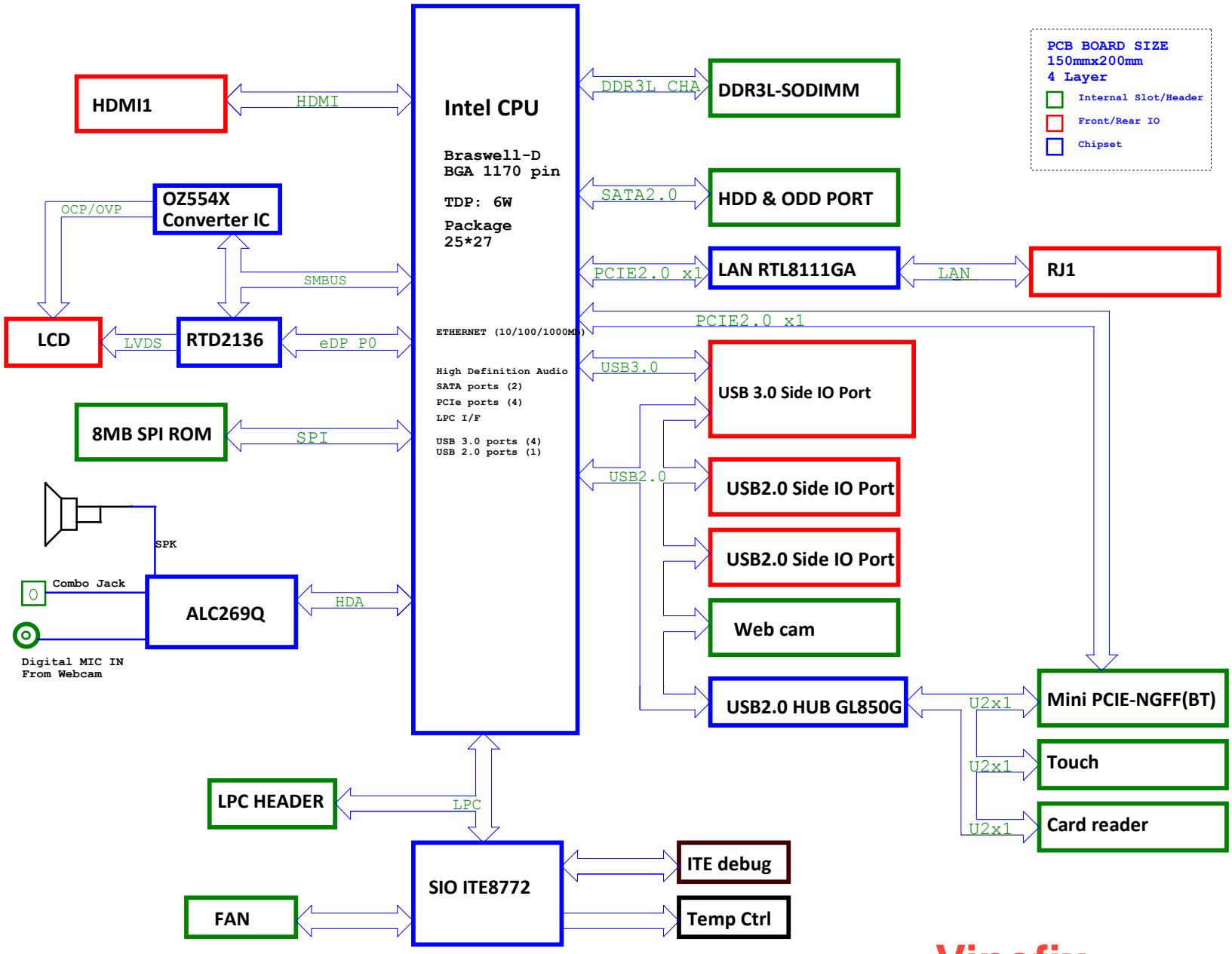
Date: Thursday, August 27, 2015	Sheet 1 of 108	

Project Name:Bolton195i_2
Project Code: 3PD042010001
PCB Number : 15047-1



Vinafix

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Title: Block Diagram
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Date: Wednesday, September 02, 2015 | Sheet 2 of 108

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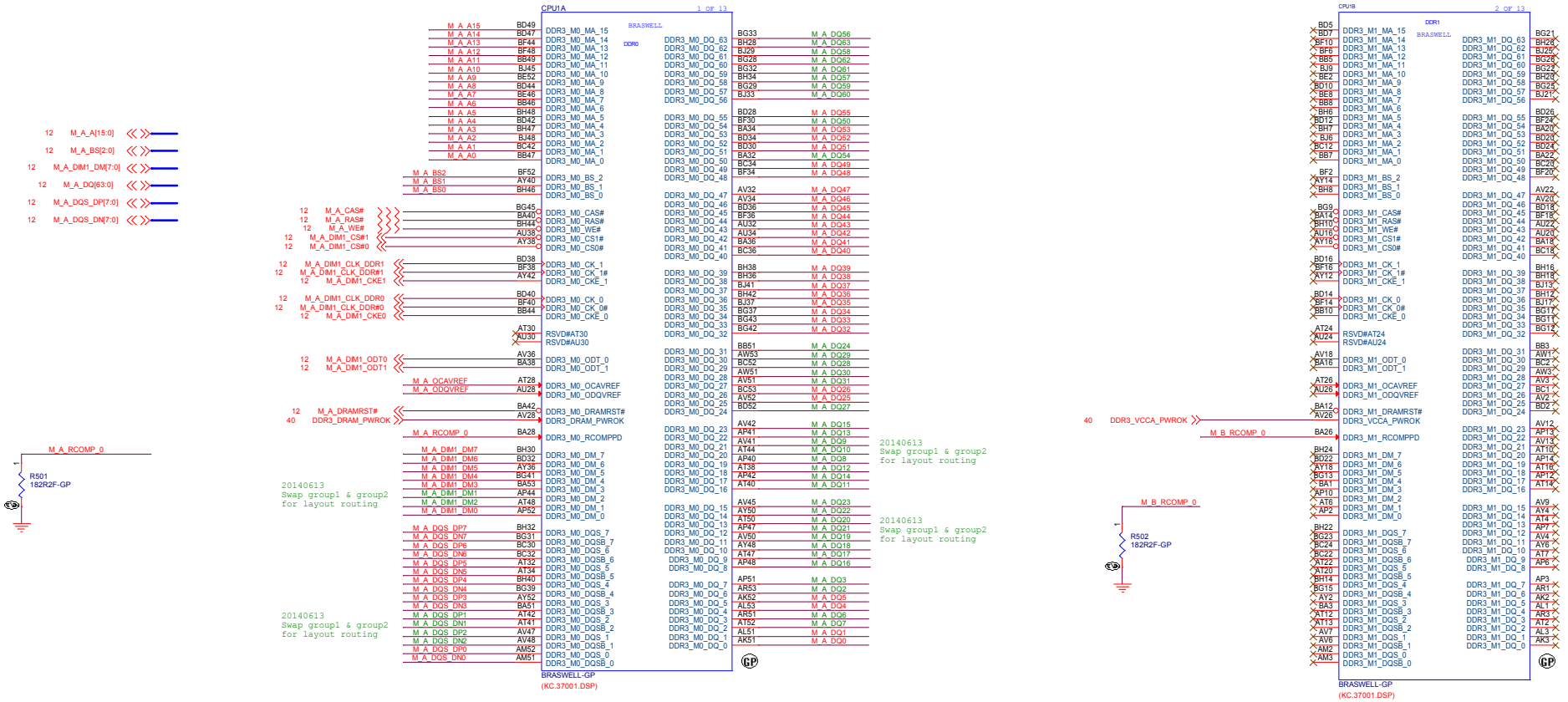
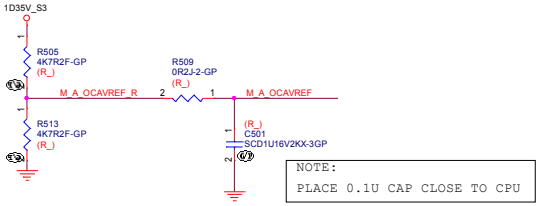
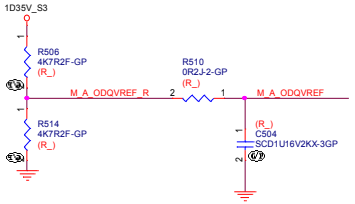


SOC VREF signals are not used for DDR3L designs
and can be left NC,DRAM VREF signals need to have resistor network



NOTE:
PLACE 0.1U CAP CLOSE TO CPU



NOTE:
PLACE 0.1U CAP CLOSE TO CPU

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

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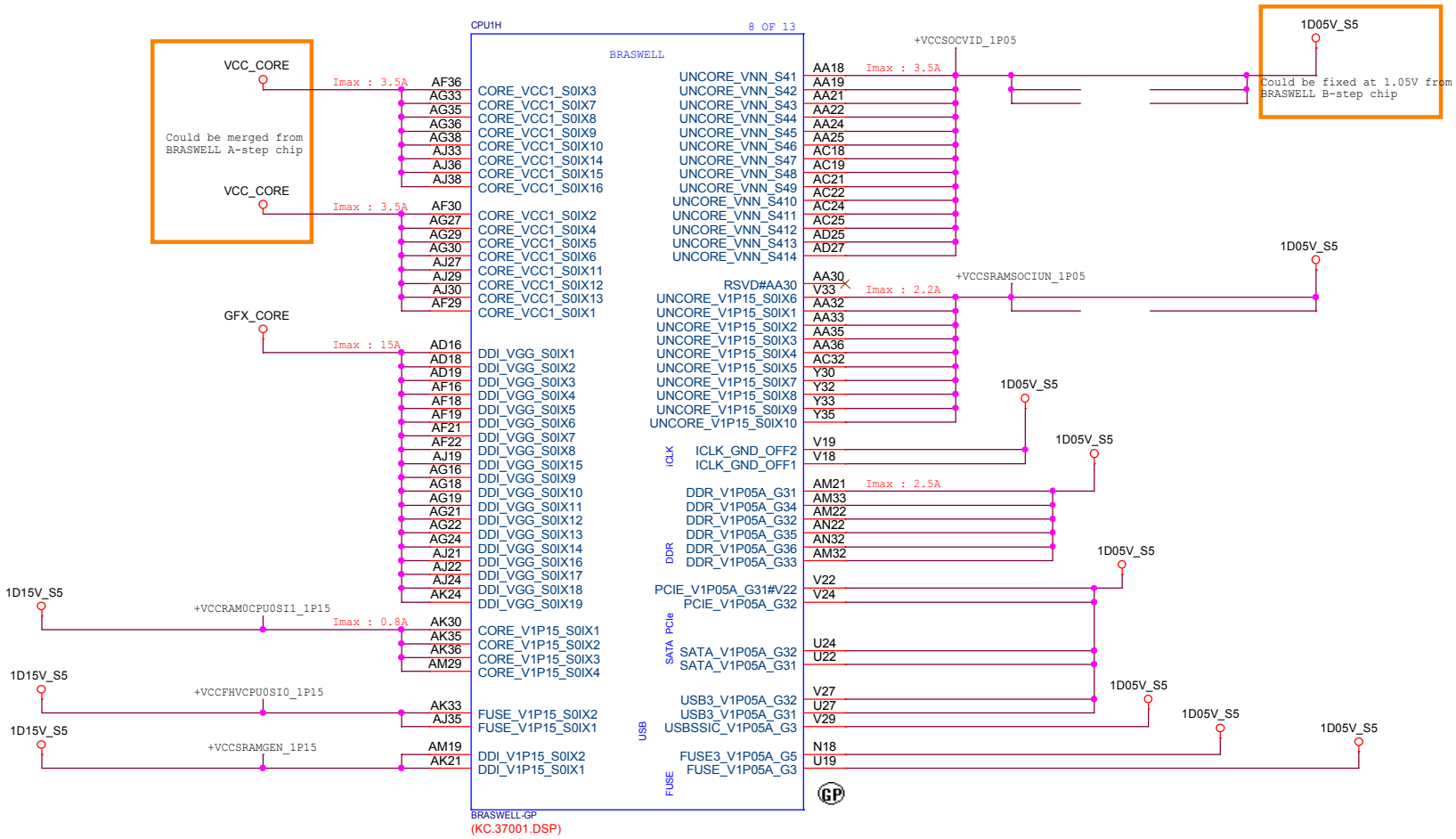

COMPRESSED IMAGE

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Braswell-M/D Platform
Display Configuration

	Default	1	2	3	4	5	6	7
DDI-0	DP	DP	DP	DP	HDMI	HDMI	HDMI	HDMI
DDI-1	eDP	eDP	DP	HDMI (retp)	eDP	eDP	DP	HDMI (retp)
DDI-2	HDMI	DP	HDMI	HDMI	HDMI	DP	HDMI	HDMI
PCU UART	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No

Table 139. DDI Disable Guidelines

Signal	Recommendation
DDIx_TXP[3:0] DDIx_TXN[3:0]	NC
DDIx_AUXP DDIx_AUXN	NC
DDIx_HPD DDIx_DDCCLK DDIx_DDCDATA	GND
DDIx_VDDEN DDIx_BKLTEN DDIx_BKLCTL	NC
DDI_RCOMP	NC

10.8 Unused Interface Termination

Table 53. MIPI*-CSI-2 Pins

Signal Name	Action
MCSI_[3:1]_CLKN MCSI_[3:1]_CLKP	No connect
MCSI_1_DN[0:3] MCSI_1_DP[0:3] MCSI_2_DN[0:1] MCSI_2_DP[0:1]	No connect
MCSI_RCOMP	No connect

NOTE: If a x1 or x2 or x3 Camera is used on MCSI_X4 port, causing some lines to be unconnected, these unused signals can be no connect.

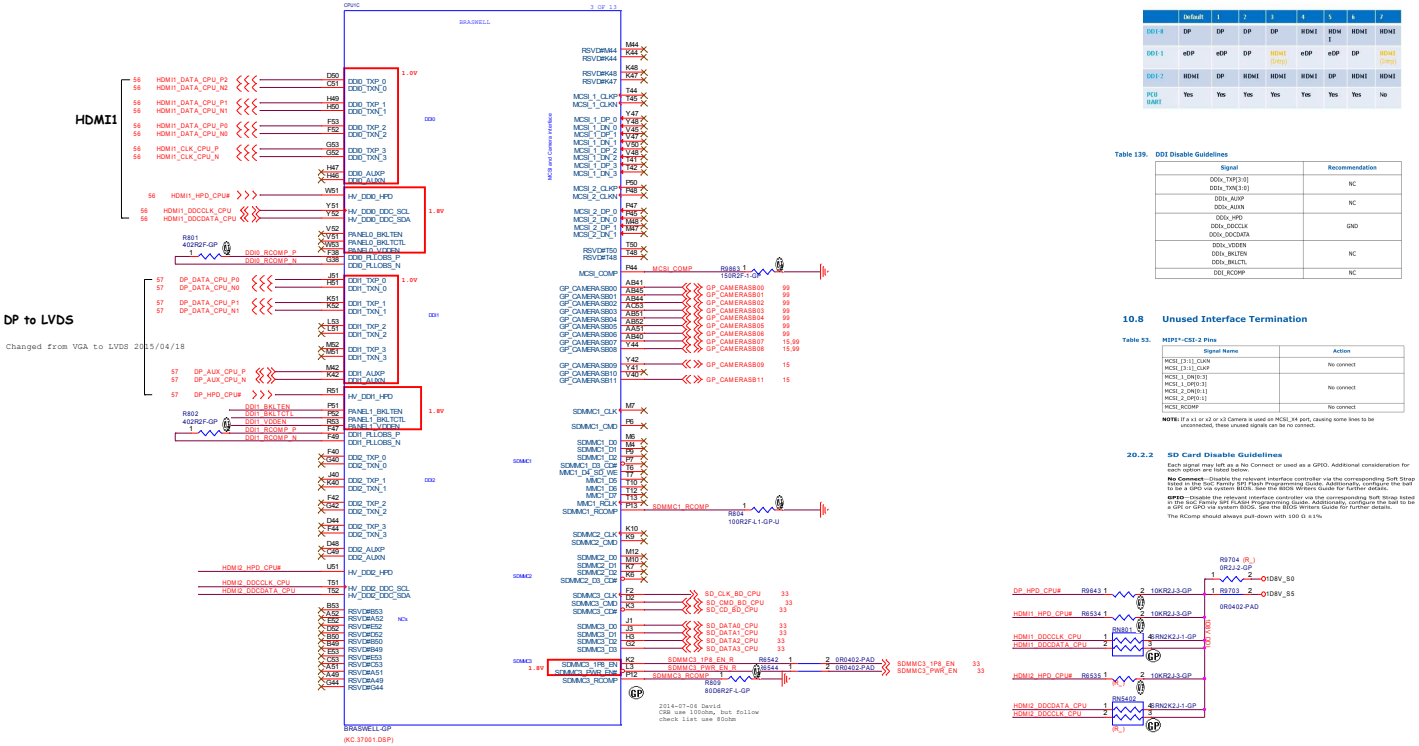
20.2.2 SD Card Disable Guidelines

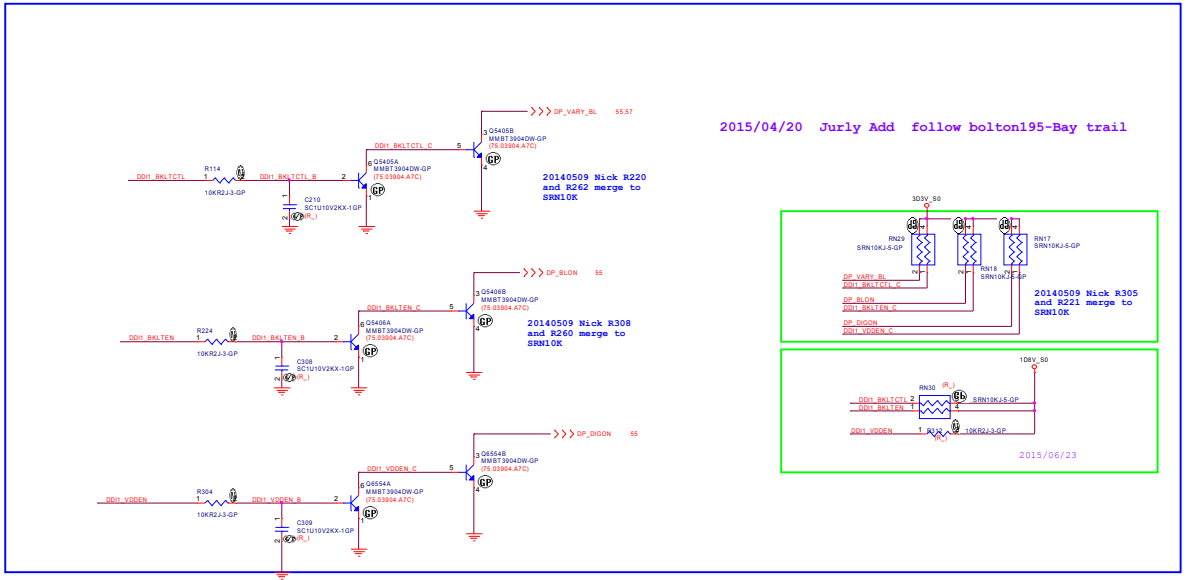
Each signal may left as a No Connect or used as a GPIO. Additional consideration for **No Connect** is listed below:

No Connect – Disable the relevant interface controller via the corresponding Soft Strap listed in the SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPO via system BIOS. See the BIOS Writers Guide for further details.

GPIO – Disable the relevant interface controller via the corresponding Soft Strap listed in the SoC Family SPI FLASH Programming Guide. Additionally, configure the ball to be a GPI or GPO via system BIOS. See the BIOS Writers Guide for further details.

The RComp should always pull-down with 100 Ω ±1%





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Title: CPU (DDI/EDP)			
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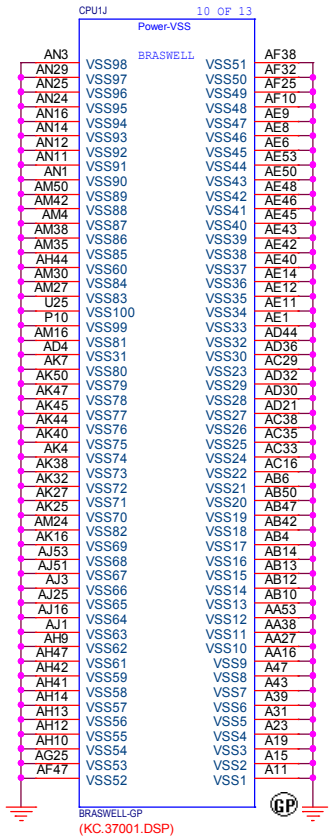

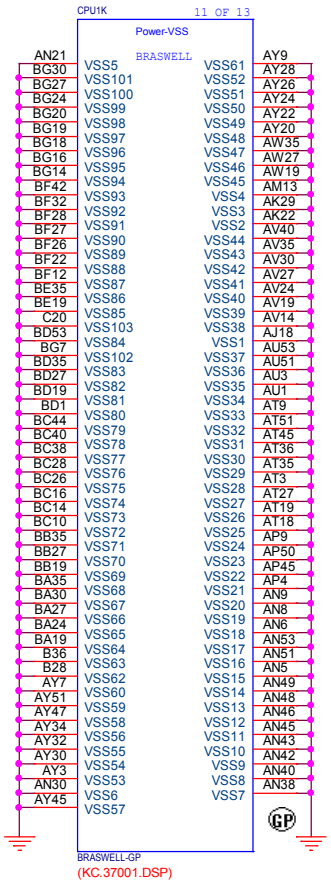

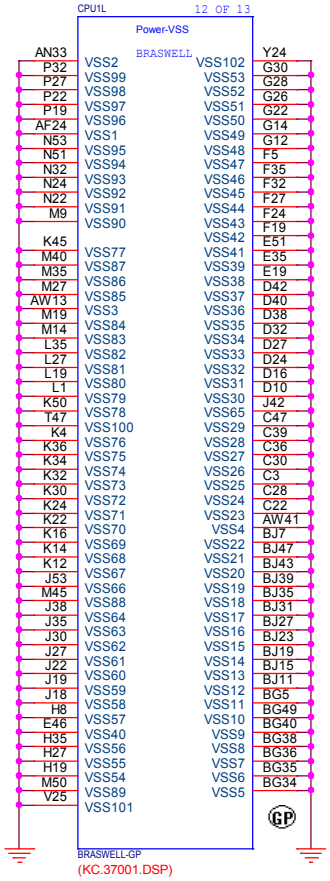

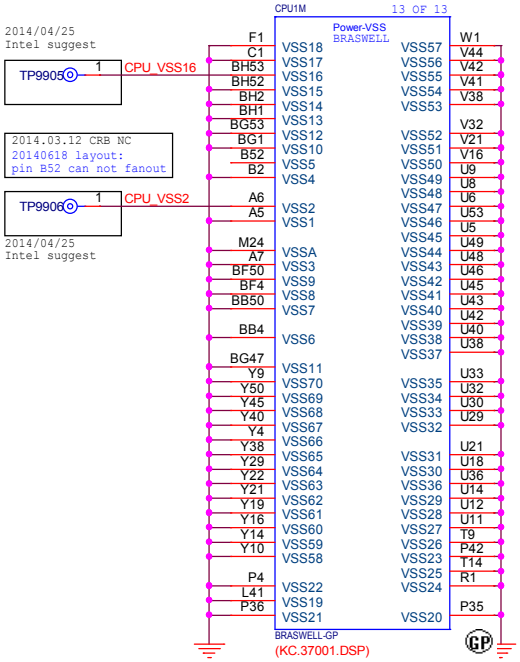

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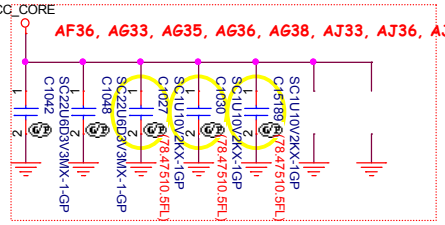
PLACE ALL THE CAPS
UNDER THE PKG SHADOW

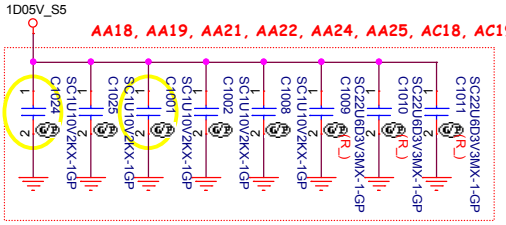
VCC_CORE

AF36, AG33, AG35, AG36, AG38, AJ33, AJ36, AJ38



1D05V_S5

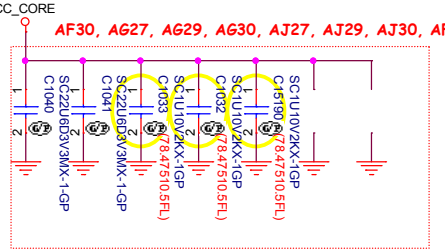
AA18, AA19, AA21, AA22, AA24, AA25, AC18, AC19, AC21, AC22, AC24, AC25, AD25, AD27



PLACE ALL THE CAPS
UNDER THE PKG SHADOW

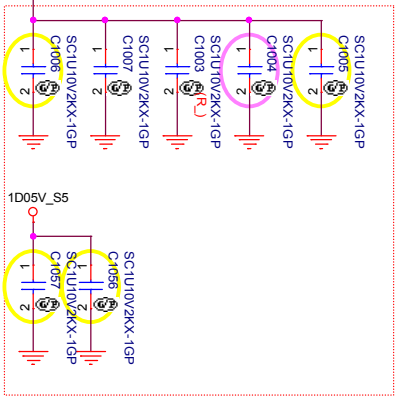
VCC_CORE

AF30, AG27, AG29, AG30, AJ27, AJ29, AJ30, AF29

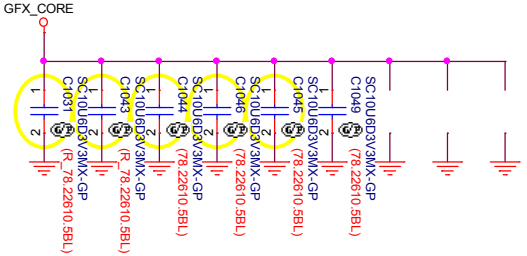


1D05V_S5

V33, AA32, AA33, AA35, AA36, AC32, Y30, Y32, Y33, Y35

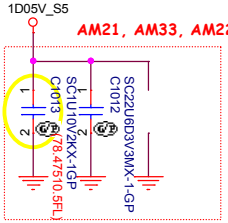


GFX_CORE



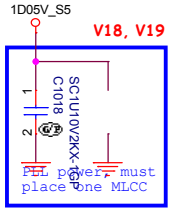
1D05V_S5

AM21, AM33, AM22, AN22, AN32, AM32



1D05V_S5

V18, V19



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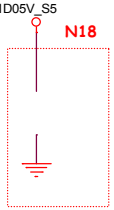
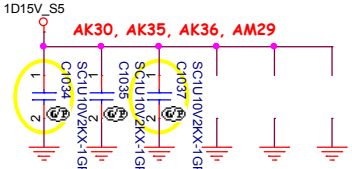
N18



1D15V_S5

AK30, AK35, AK36, AM29



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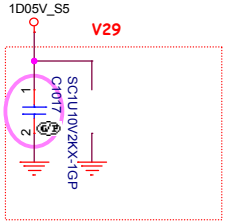
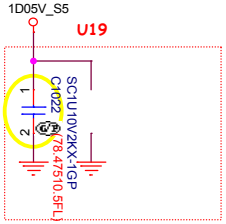
V29



1D05V_S5

U19



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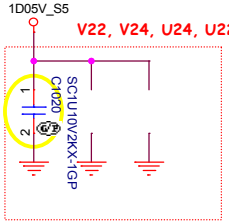
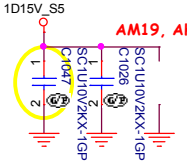
V22, V24, U24, U22, V27, U27



1D15V_S5

AM19, AK21



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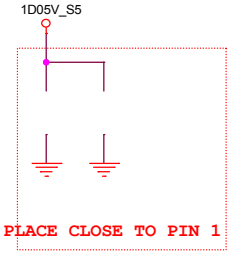
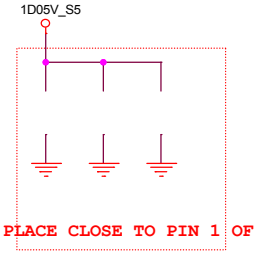


PLACE CLOSE TO PIN 1 OF RA

1D05V_S5



PLACE CLOSE TO PIN 1 OF RB

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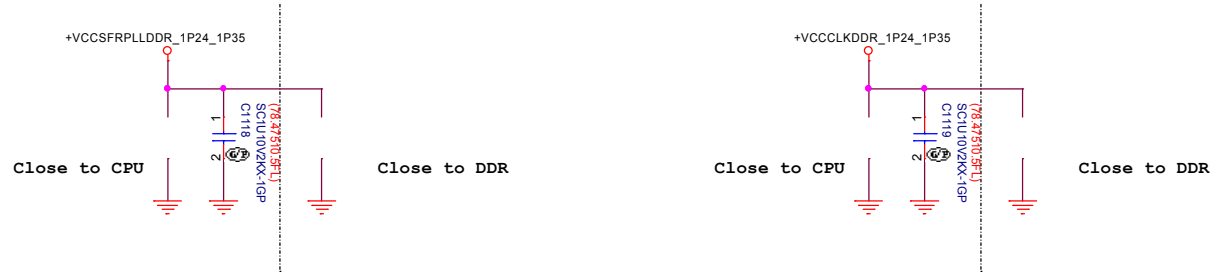

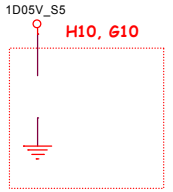

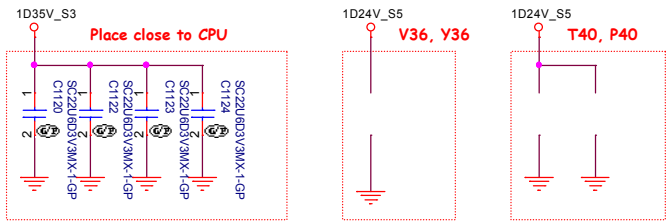

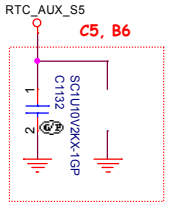

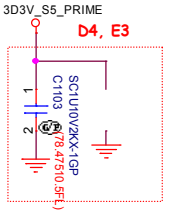

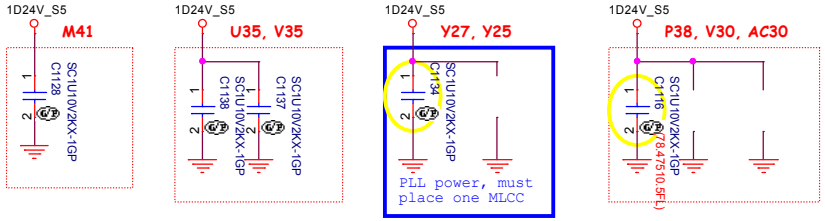

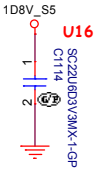

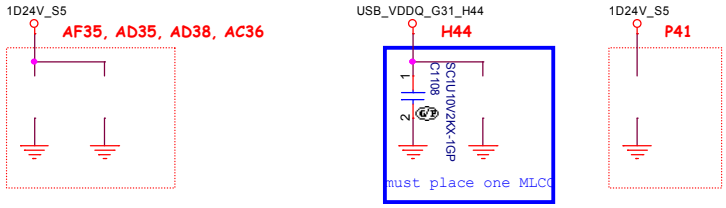

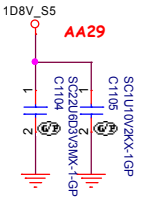

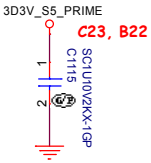

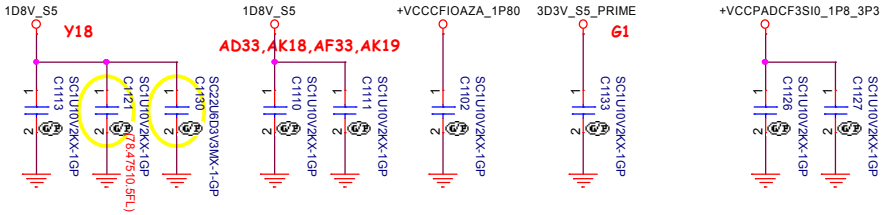

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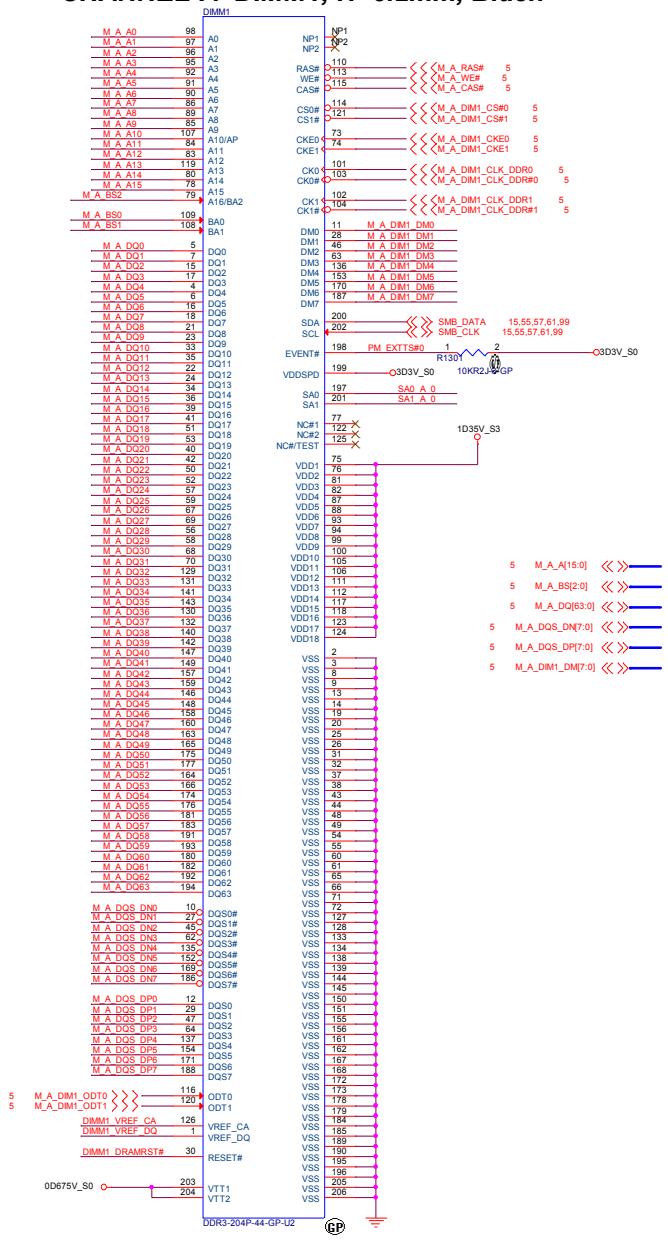
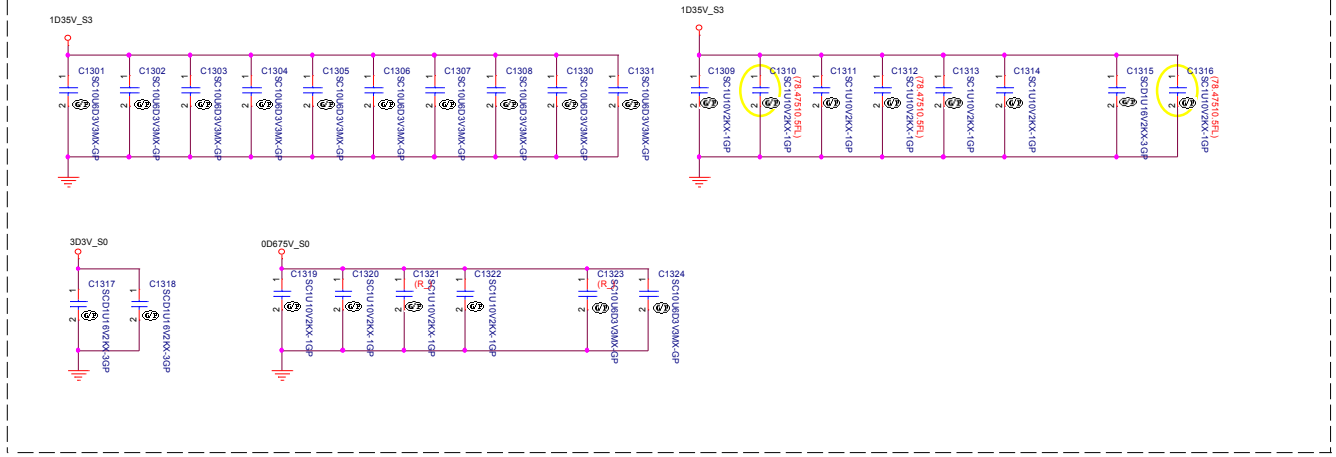
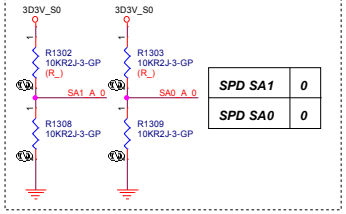
CHANNEL-A DIMM1, H=5.2mm, Black

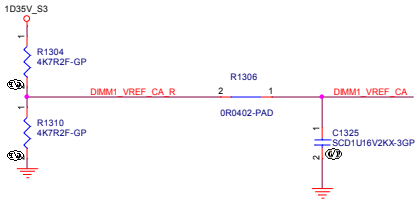


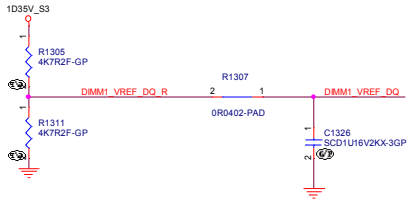
Place these Caps near DIMM1



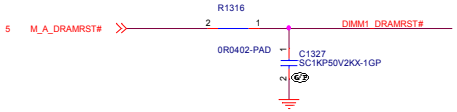
SPD Address of DIMM1







DIMM1 Reset



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DDR3L-SODIMM2(Reserved)

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

1-2:
Enable TXE
2-3:
Disable TXE
Could be override

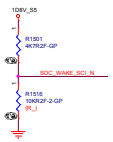
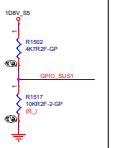
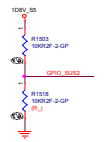
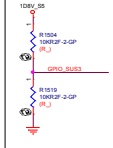
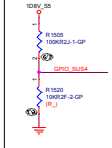
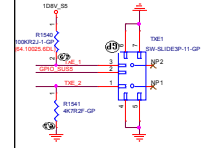
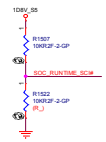
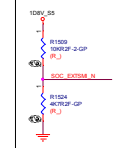
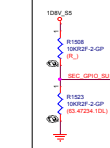
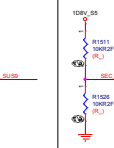
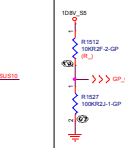
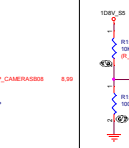
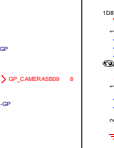
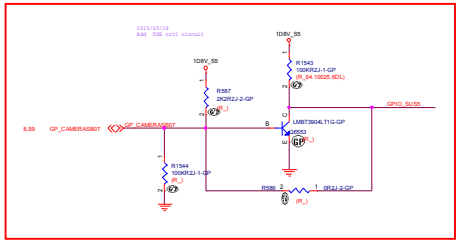
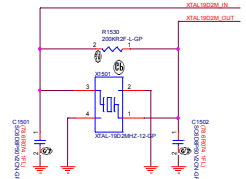
Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0 (Weak internal pull-down)	GPIO_SUS1 (Weak internal pull-down)	GPIO_SUS2 (Weak internal pull-up)	GPIO_SUS3 (Weak internal pull-down)	GPIO_SUS4 (Weak internal pull-up)	GPIO_SUS5 (Weak internal pull-up)	GPIO_SUS6 (Weak internal pull-up)	GPIO_SUS7 (Weak internal pull-up)	SEC_GPIO_SUS8 (Weak internal pull-up)	SEC_GPIO_SUS9 (Weak internal pull-down)	SEC_GPIO_SU10 (Weak internal pull-down)	GP_CAMERASB08 (Weak internal pull-down)	GP_CAMERASB09 (Weak internal pull-down)	GP_CAMERASB11 (Weak internal pull-down)
Schematic														
High	DDI0 Detect (V)	DDI1 Detect (V)	Normal Operation(V)	DSI Detect	Boot from SPI (V)	Normal Operation	Normal (V) (Follow CRB)	Normal (V) (Follow CRB)	1.35V	Bypass with 1.05V (V)	PMC	Bypass	Bypass	Bypass
Low	Not Detect	Not Detect	Change Boot Loader address(A16 Override)	Not Detect (V) (Follow CRB)	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V (V)	No bypass SPEC not match with CRB	Fuse controller (V) Check Function	No Bypass (V)	No Bypass (V)	No Bypass (V)

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation





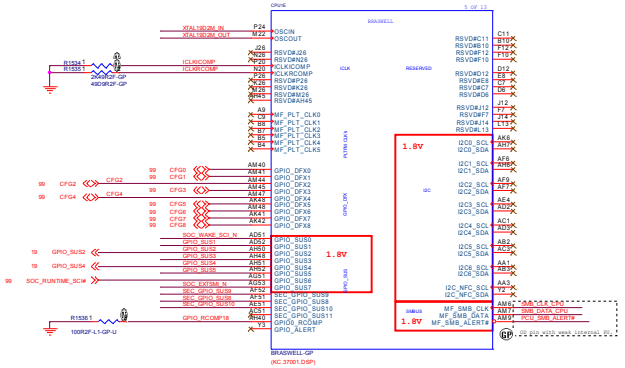
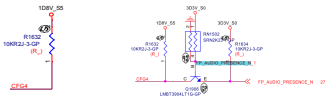
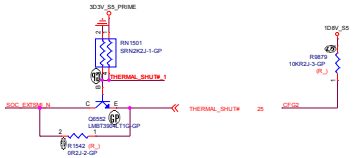


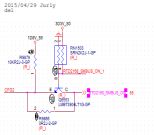
Table 29. Straps (Sheet 2 of 2)

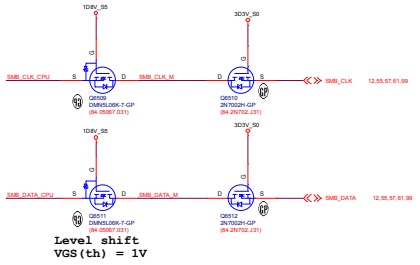
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

2014/04/17
Bolton195i delete FP_AUDIO_PRESENCE_N

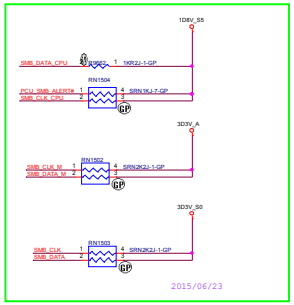








Level shift
VGS(th) = 1V



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Title: CPU (SMBUS/GPIO/STRAP)

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Custom	Bolton195i	-1A

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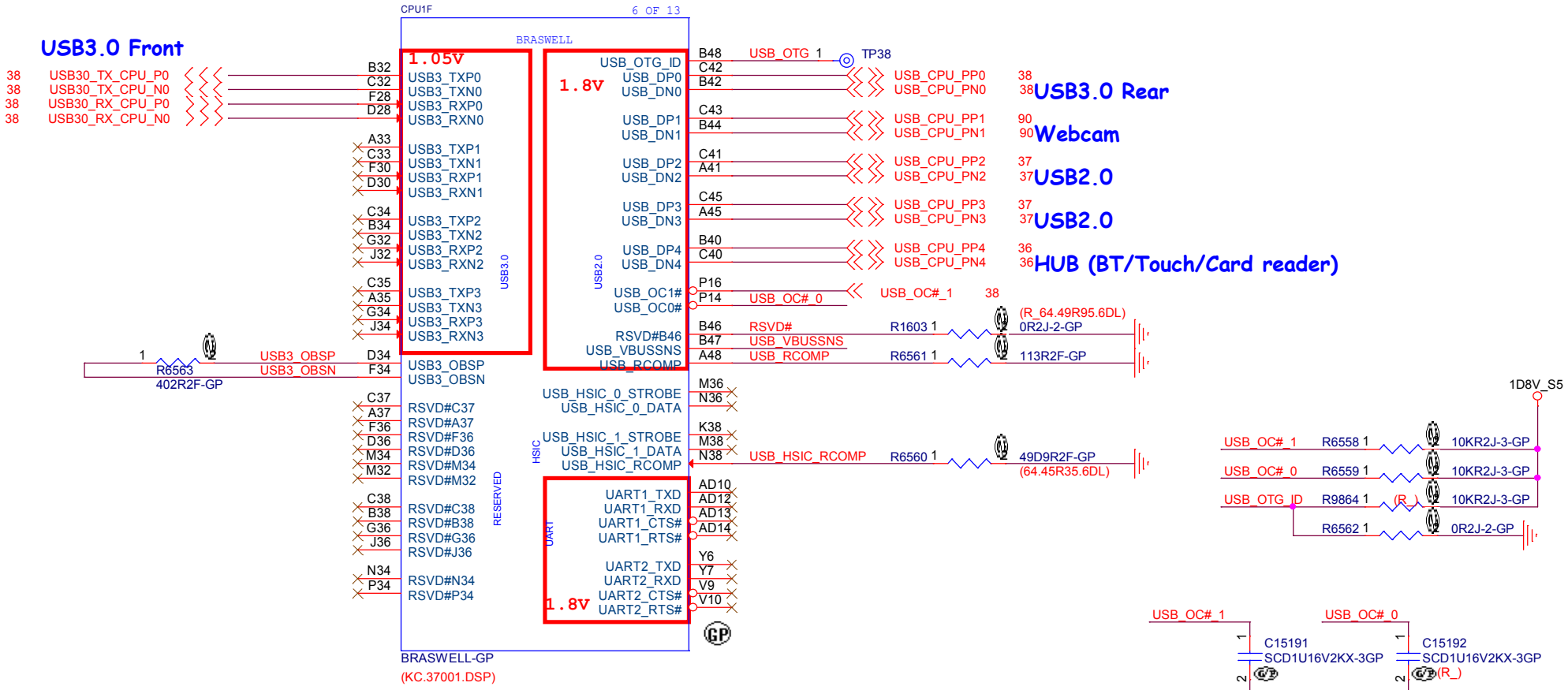

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	Hsichih, Taipei Hsien	
Title: CPU (USB)		
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Title: CPU (DMI/FDI) (Reserved)

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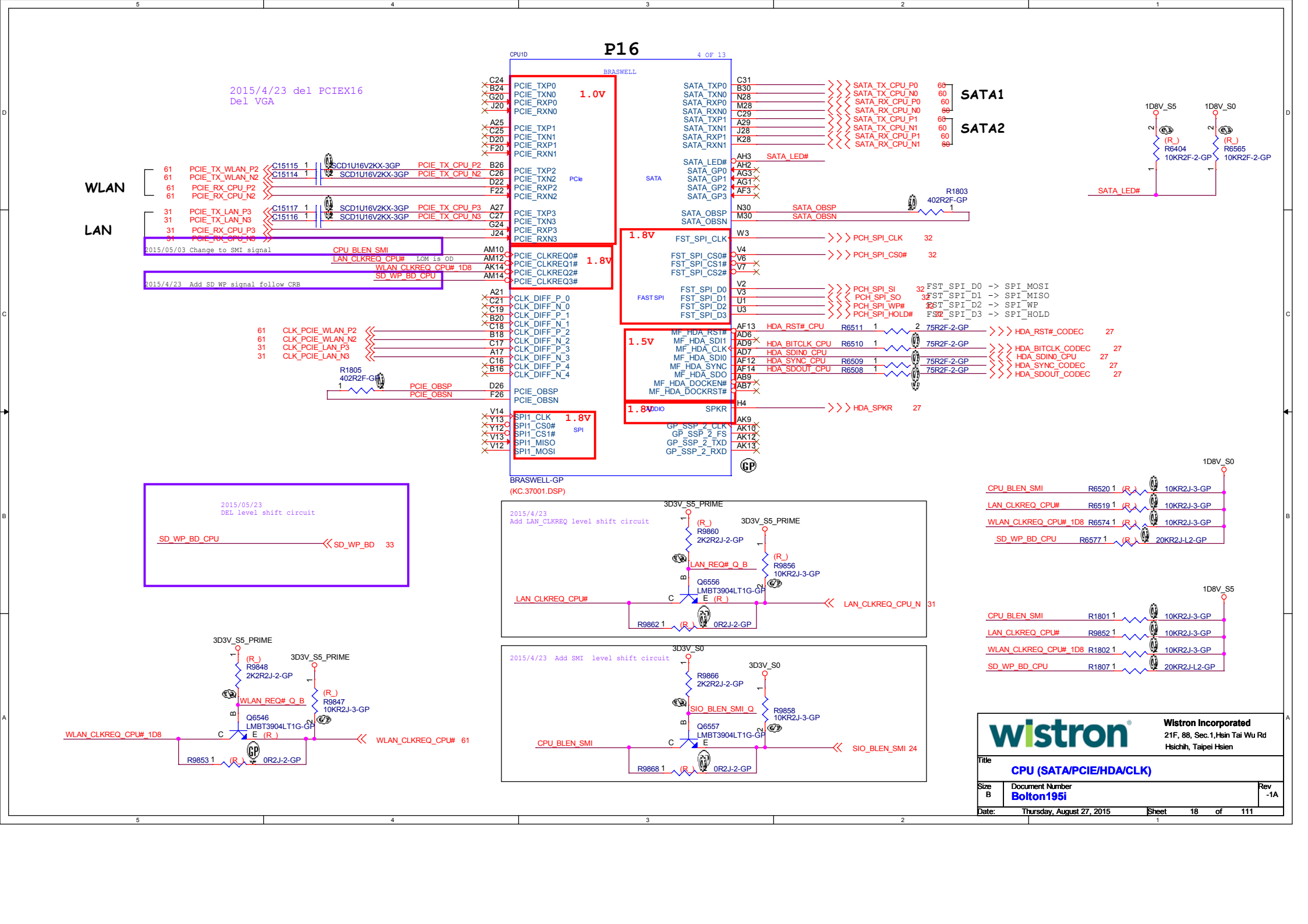
P16
2015/4/23 del PCIEX16
Del VGA
WLAN
LAN
SATA1
SATA2
BRASWELL-GP
(KC.37001.DSP)
2015/05/03 Change to SMI signal
2015/4/23 Add SD_WP signal follow CRB
2015/05/23
DEL level shift circuit
2015/4/23
Add LAN_CLKREQ level shift circuit
2015/4/23 Add SMI level shift circuit
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Hsichih, Taipei Hsien
CPU (SATA/PCIE/HDA/CLK)
Bolton195i
Thursday, August 27, 2015
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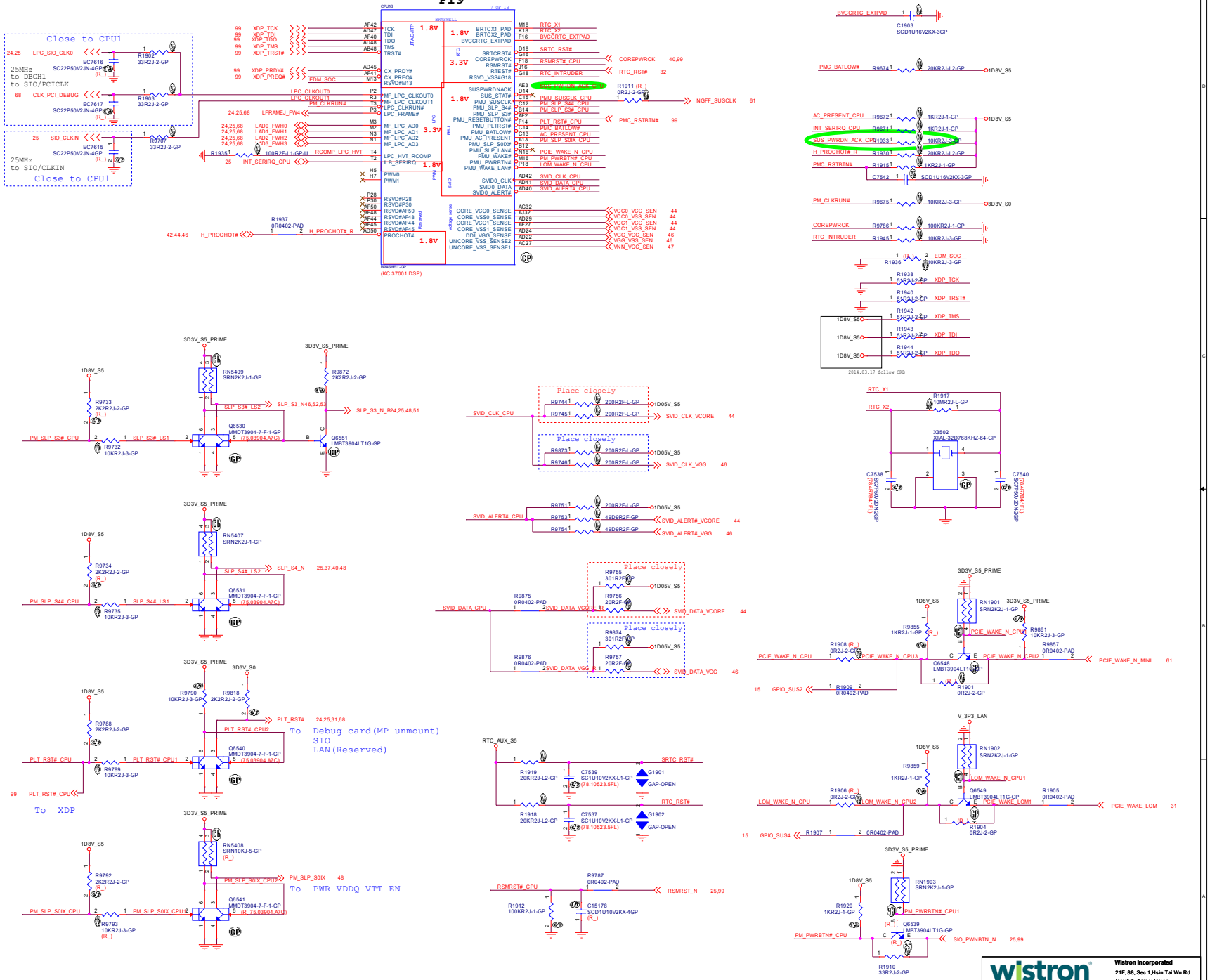
P19


Close to CPU1
25MHz
to DBGH1
to SIO/PCICLK
25MHz
to SIO/CLKIN
Close to CPU1
CPUIG
(KC.37001.DSP)
Place closely
To Debug card(MP unmount)
SIO
LAN(Reserved)
To XDP
To PWR_VDDQ_VTT_EN
wistron
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Hsichih, Taipei Hsien
CPU (RTC/LPC/JTAG)
Bolton19SI
Wednesday, September 02, 2015
111

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Title: CPU (GPIO/CPU) (Reserved)

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2014.03.21 change page

+VCCSFRPLLDDR_1P24_1P35 — R6529 0R0402-PAD — 1D35V_S3

+VCCCLKDDR_1P24_1P35 — R6528 0R0402-PAD — 1D35V_S3

redwood connect to 3.3V_S0,check with Intel

3D3V_S5_PRIME — R6527 0R2J-2-GP — +VCCPADCF3SI0_1P8_3P3

1D8V_S5

VSDIO — R6530 0R0402-PAD

SD3 IO SUPPLY

2015/05/20 Jurly del R6533

2015/04/24
Modify SD power to VSDIO

AUDIO IO SUPPLY

1D5V_S0 / 1D8V_S0 — R6526 0R2J-2-GP — +VCCCFIOAZA_1P80

1D8V_S5 — R9845 0R0402-PAD

2015/05/20 Jurly del R6532

2015/12/21 David
change to 1D8V_S5 to save 1D5V LDO

LPC IO SUPPLY

3D3V_S5_PRIME — +VCCPADCF1SI0_1P8_3P3

+VCCPADCF3SI0_1P8_3P3

+VCCCFIOAZA_1P80

1D8V_S5 — +VCCPADCF2SI0_E_1P80

1D8V_S5

+VCCCLKDDR_1P24_1P35 — +VCCSFRPLLDDR_1P24_1P35 — 1D35V_S3

CPU1I — BRASWELL — 9 OF 13

DDR:
AN27 DDRSFR_VDDQ_G_S4
AM25 DDR_VDDQ_G_S42
BE1 DDR_VDDQ_G_S416
BE53 DDR_VDDQ_G_S419
BJ2 DDR_VDDQ_G_S426
BJ3 DDR_VDDQ_G_S427
BJ49 DDR_VDDQ_G_S428
BJ5 DDR_VDDQ_G_S429
BH50 DDR_VDDQ_G_S425
BH5 DDR_VDDQ_G_S424
BH49 DDR_VDDQ_G_S423
BH4 DDR_VDDQ_G_S422
BE3 DDR_VDDQ_G_S417
BC51 DDR_VDDQ_G_S421
BC3 DDR_VDDQ_G_S420
BJ51 DDR_VDDQ_G_S430
BJ52 DDR_VDDQ_G_S431
AY10 DDR_VDDQ_G_S414
AY44 DDR_VDDQ_G_S415
AV44 DDR_VDDQ_G_S413
AV10 DDR_VDDQ_G_S410
BE51 DDR_VDDQ_G_S418
AV38 DDR_VDDQ_G_S412
AV16 DDR_VDDQ_G_S411
AU36 DDR_VDDQ_G_S49
AU18 DDR_VDDQ_G_S48
AN36 DDR_VDDQ_G_S47
AN35 DDR_VDDQ_G_S46
AN19 DDR_VDDQ_G_S45
AN18 DDR_VDDQ_G_S44
AM36 DDR_VDDQ_G_S43
AM18 DDR_VDDQ_G_S41

SDIO:
E1 SDIO_V3P3A_V1P8A_G31
E2 SDIO_V3P3A_V1P8A_G32
C1 SDIO_V3P3A_V1P8A_G33

UNCORE:
AH4 UNCORE_V1P8A_G32
AF4 UNCORE_V1P8A_G31

GPIO:
Y18 GPIO_V1P8A_G35
AD33 GPIO_V1P8A_G31
AK18 GPIO_V1P8A_G33
AF33 GPIO_V1P8A_G32
AK19 GPIO_V1P8A_G34

DDI:
V36 DDI_VDDQ_G31 — 1D24V_S5
Y36 DDI_VDDQ_G32 — 1D24V_S5

MIPI:
T40 MIPI_V1P2A_G32 — 1D24V_S5
P40 MIPI_V1P2A_G31 — 1D24V_S5

ICLK:
Y27 ICLK_VSFR_G32 — 1D24V_S5
Y25 ICLK_VSFR_G31 — 1D24V_S5

CORE:
P38 CORE_VSFR_G35 — 1D24V_S5
V30 CORE_VSFR_G36 — 1D24V_S5
AC30 PCIE_V1P05A_G31#AC30 — 1D24V_S5
AF35 CORE_VSFR_G34 — 1D24V_S5
AD35 CORE_VSFR_G32 — 1D24V_S5
AD38 CORE_VSFR_G33 — 1D24V_S5
AC36 CORE_VSFR_G31 — 1D24V_S5

USB:
M41 USBHSIC_V1P2A_G3 — 1D24V_S5
U35 USB_VDDQ_G32 — 1D24V_S5
V35 USB_VDDQ_G33 — USB_VDDQ_G31_H44 — 1D24V_S5
H44 USB_VDDQ_G31 — 1D24V_S5
P41 USBSSIC_V1P2A_G3 — +VCCUSB2_1P8 — 1D8V_S5
AA29 USB_V1P8A_G3 — 3D3V_S5_PRIME
C23 USB_V3P3A_G32 — RTC_AUX_S5
B22 USB_V3P3A_G31 — 3D3V_S5_PRIME

USB_VDDQ_G31_H44 — R2130 0R0402-PAD — 1D24V_S5

RTC:
C5 RTC_V3P3RTC_G52 — RTC_AUX_S5
B6 RTC_V3P3RTC_G51 — 3D3V_S5_PRIME
D4 RTC_V3P3A_G51
E3 RTC_V3P3A_G52 — 1D8V_S5
U16 FUSE_V1P8A_G3 — 1D05V_S5

FUSE:
H10 FUSE1_V1P05A_G4
G10 FUSE0_V1P05A_G3
A3 RSVD_VSS#A3
K20 RSVD#K20
M20 RSVD#M20

BRASWELL-GP
(KC.37001.DSP)

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Title: CPU (VSS) (Reserved)

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Colay to ITE8732

FAN
25 CPU_FANTACH1
25 CPU_FANCTL1

LPC
19,25,68 LFRAMEJ_FW4
19,25,68 LAD0_FWH0
19,25,68 LAD1_FWH1
19,25,68 LAD2_FWH2
19,25,68 LAD3_FWH3

CLOCK
19,25 LPC_SIO_CLK0
25 CLK_48M_SIO

19,25,48,51 SLP_S3_N_B
25 SLP_S4_N_R
19,25,31,68 PLT_RST#
25 SERIRQ_N

25 PB_IN_N_1
25,54 SIO_PSON_N
25 SW_ON_N_SIO
25,64 SUSLED_R_N

HW Monitor
25 HM_VCCP_R
25 SIO_VIN1
25 SIO_VIN2
25 SIO_VIN4
25 SIO_VIN5
25 SIO_VREF
25 REMOTE1+
25 DIMM_TMPIN2
25 SIO_AGND

KB/MS
25 MCLK
25 MDAT
25 KBCLK
25 KDAT

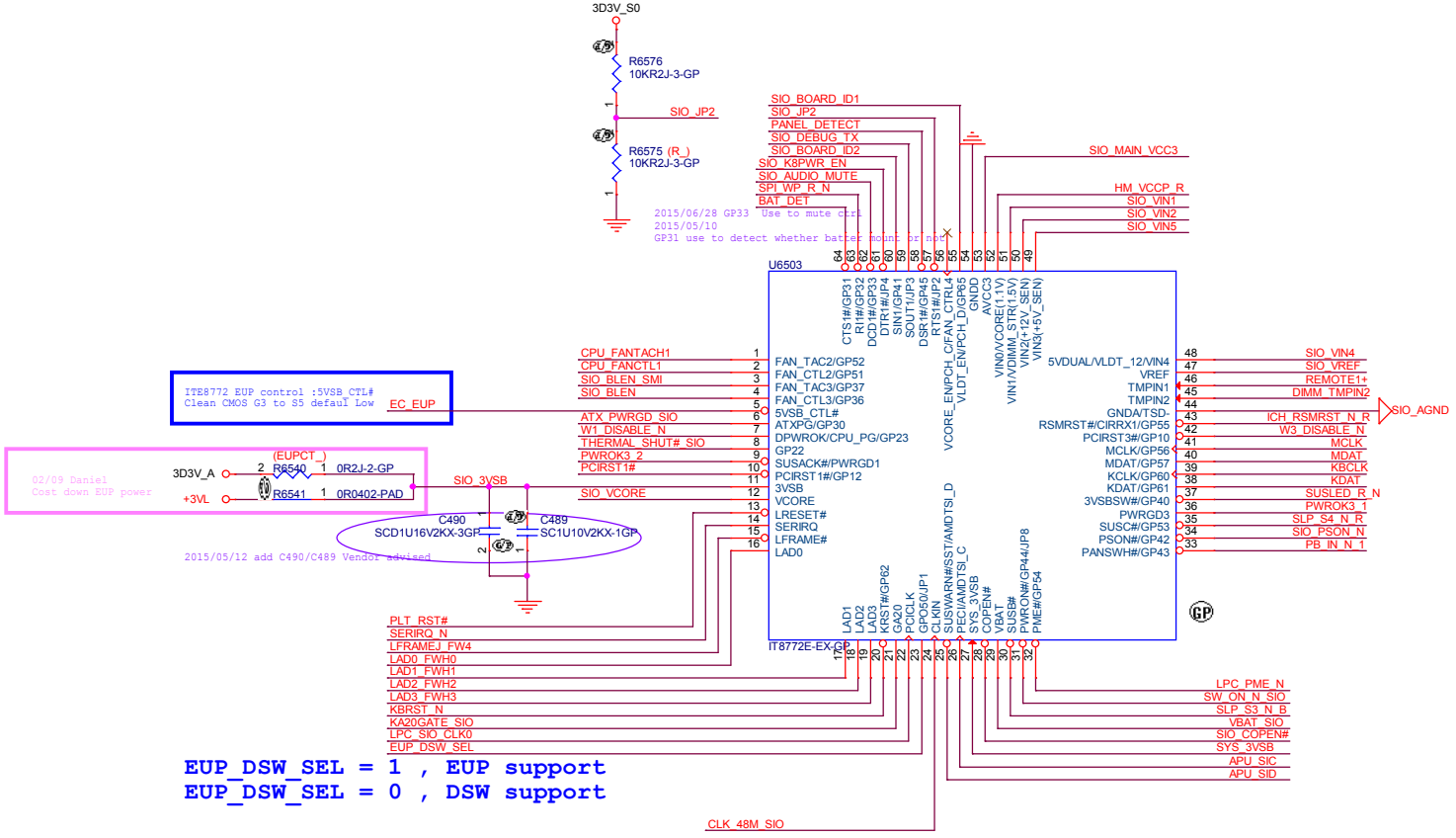
Power Manager
25 EUP_DSW_SEL
25 EC_EUP
25,51 ATX_PWRGD_SIO
25 PWROK3_2
25 PWROK3_1
43,49 EC_EUP_EN#

25 APU_SIC
25 APU_SID

OTHERS
25 SIO_DEBUG_TX
25 SIO_K8PWR_EN
25 ICH_RSMRST_N_R
25 SIO_BOARD_ID2
25 SIO_BOARD_ID1
25 THERMAL_SHUT#_SIO
25 SIO_COPEN#
25,61 W1_DISABLE_N
25,61 W3_DISABLE_N
55 SIO_BLEN
25,32 BAT_DET
25 SIO_MAIN_VCC3
25 SIO_VCORE
25 VBAT_SIO
25 SYS_3VSB
43,49 SIO_AUDIO_MUTE
25 KBRST_N
25 KA20GATE_SIO
25 LPC_PME_N
25 PCIRST1#
18 SIO_BLEN_SMI
18 SPI_WP_R_N
43,49 PANEL_DETECT

IT8732 PIN92: VCC3 detect , 去 detect VCC3 是否有 in ,IC 內部有電路去做偵測 , 需接 1K 電阻
IT8772 PIN53: VCC3 電源 input , 實際 VCC3 in , 外部不用接 1K 電阻

IC	P/N	Location
ITE8772	63.R0034.1DL	R537 (0R)
ITE8732	63.10234.1DL	R537(1k)



EUP_DSW_SEL = 1 , EUP support
EUP_DSW_SEL = 0 , DSW support

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Title	SIO (IT8772E-EX)	
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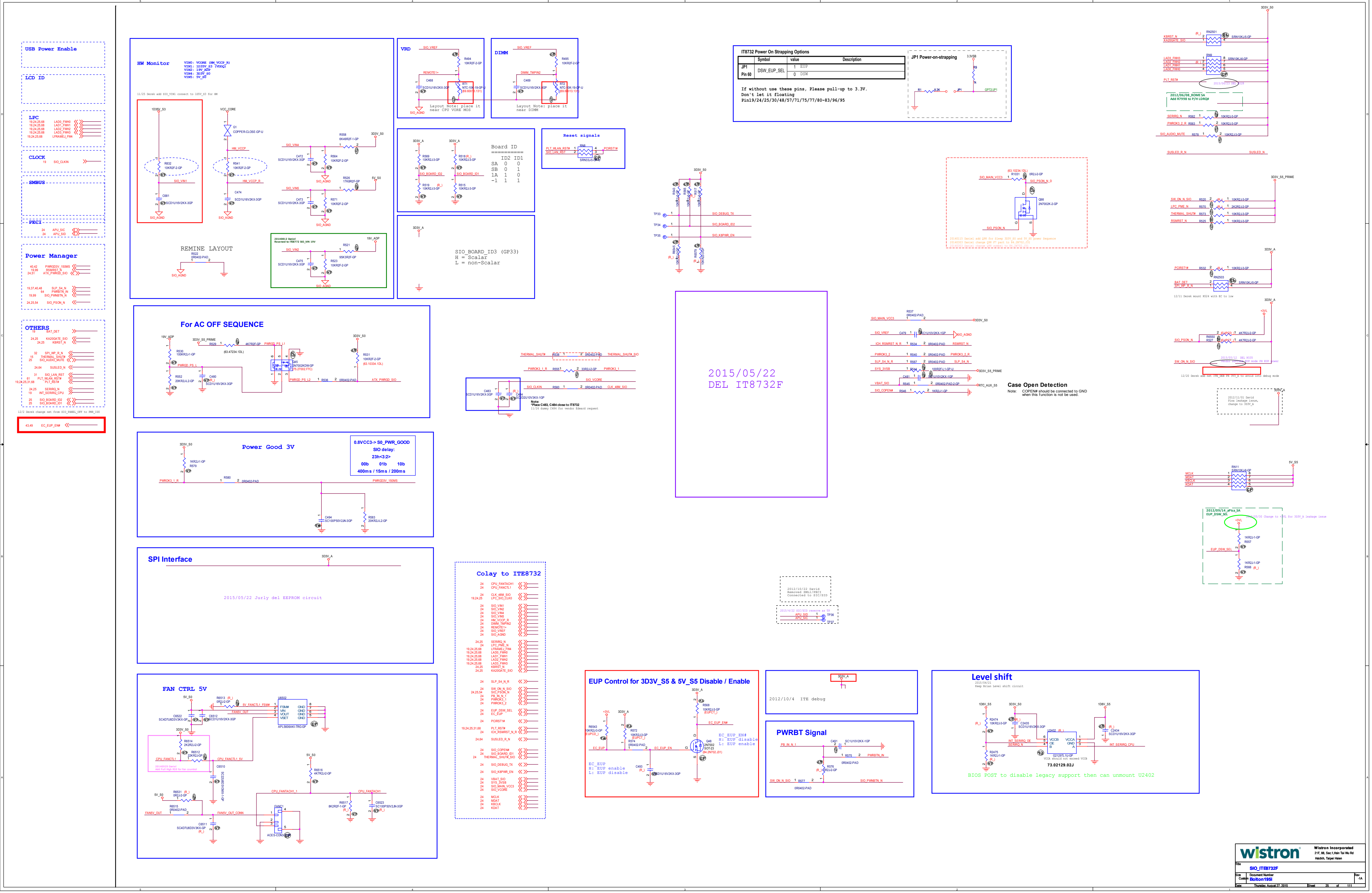

USB Power Enable
LCD ID
LPC
CLOCK
SMBUS
PECI
Power Manager
OTHERS
HW Monitor
VRD
DIMM
Layout Note: place it near CPU VORE MOS
Layout Note: place it near DIMM
Board ID
ID2 ID1
SA 0 0
SB 0 1
1A 1 0
-1 1 1
Reset signals
REMINE LAYOUT
SIO_BOARD_ID3 (GP33)
H = Scalar
L = non-Scalar
IT8732 Power On Strapping Options
JP1 Power-on-strapping
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80~83/96/95
For AC OFF SEQUENCE
2015/05/22
DEL IT8732F
Case Open Detection
Note: COPEN# should be connected to GND when this function is not be used.
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
SPI Interface
2015/05/22 Jurly del EEPROM circuit
Colay to ITE8732
FAN CTRL 5V
EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable
EC_EUP_EN#
H: EUP disable
L: EUP enable
2012/10/4 ITE debug
PWRBT Signal
Level shift
BIOS POST to disable legacy support then can unmount U2402
wistron
Wistron Incorporated
SIO_ITE8732F
Bolton19SI

wistron

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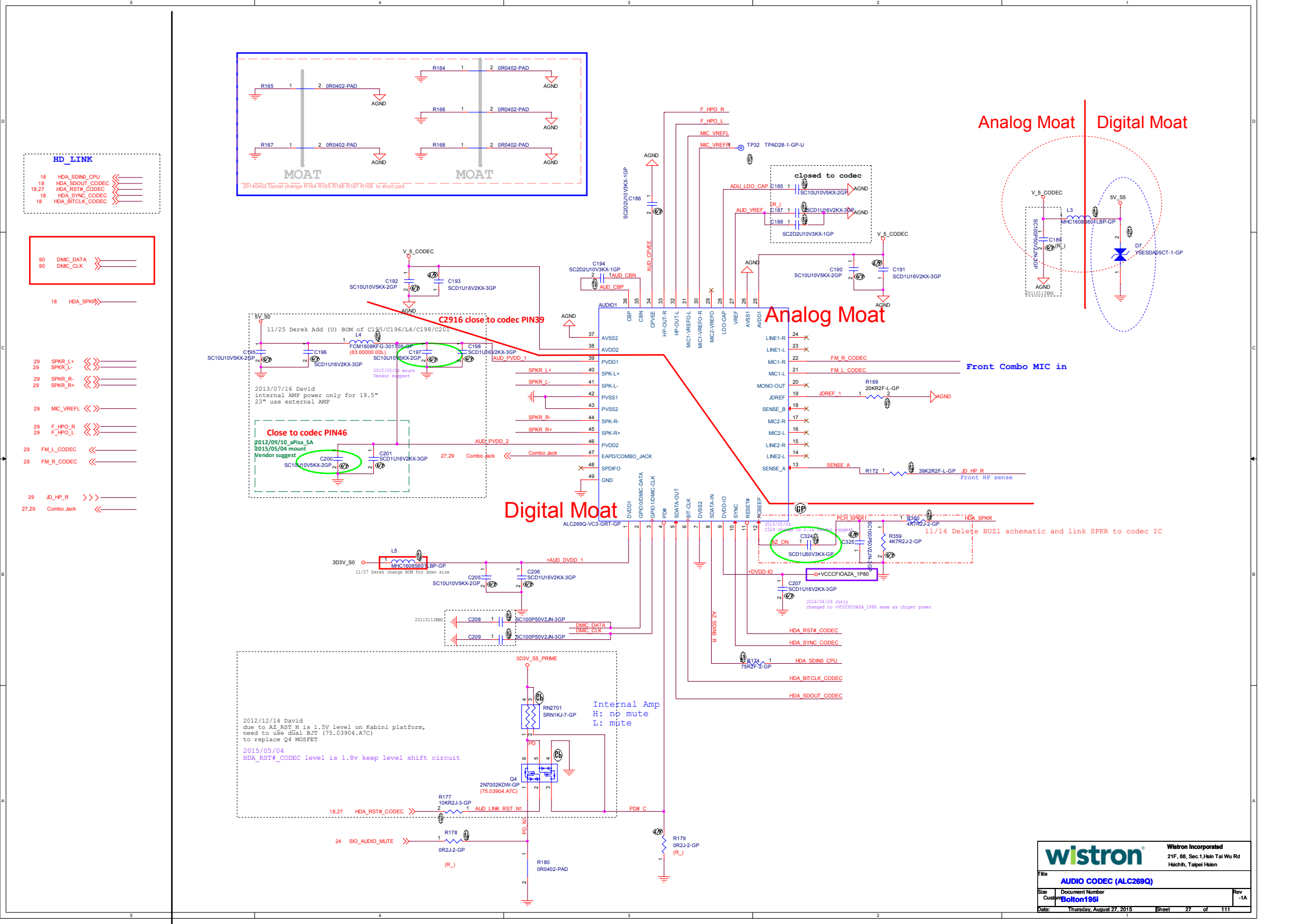
Hsichih, Taipei Hsien

Title
Thermal/FAN

Size	Document Number	Rev
A	**Bolton195i**	-1A

Date: Thursday, August 27, 2015 Sheet 26 of 111


HD_LINK
18 HDA_SDIN0_CPU
18 HDA_SDOUT_CODEC
18,27 HDA_RST#_CODEC
18 HDA_SYNC_CODEC
18 HDA_BITCLK_CODEC
90 DMIC_DATA
90 DMIC_CLK
18 HDA_SPKR
29 SPKR_L+
29 SPKR_L-
29 SPKR_R-
29 SPKR_R+
29 MIC_VREFL
29 F_HPO_R
29 F_HPO_L
29 FM_L_CODEC
29 FM_R_CODEC
29 JD_HP_R
27,29 Combo Jack
MOAT
MOAT
20140402 Daniel change R164 R165 R166 R167 R168 to short pad
Analog Moat
Digital Moat
closed to codec
C2916 close to codec PIN39
Analog Moat
Front Combo MIC in
Digital Moat
ALC269Q-VC3-GRT-GP
11/25 Derek Add (U) BOM of C195/C196/L4/C198/C201
2013/07/16 David
internal AMP power only for 19.5"
23" use external AMP
Close to codec PIN46
2012/09/10_aPisa_SA
2015/05/04 mount
Vendor suggest
11/14 Delete BUZ1 schematic and link SPKR to codec IC
Internal Amp
H: no mute
L: mute
2012/12/14 David
due to AZ_RST_N is 1.5V level on Kabini platform,
need to use dial BJT (75.03904.A7C)
to replace Q4 MOSFET
2015/05/04
HDA_RST#_CODEC level is 1.8v keep level shift circuit
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
AUDIO CODEC (ALC269Q)
Bolton195i
Thursday, August 27, 2015
27
111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
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Title
AMP (Reserved)

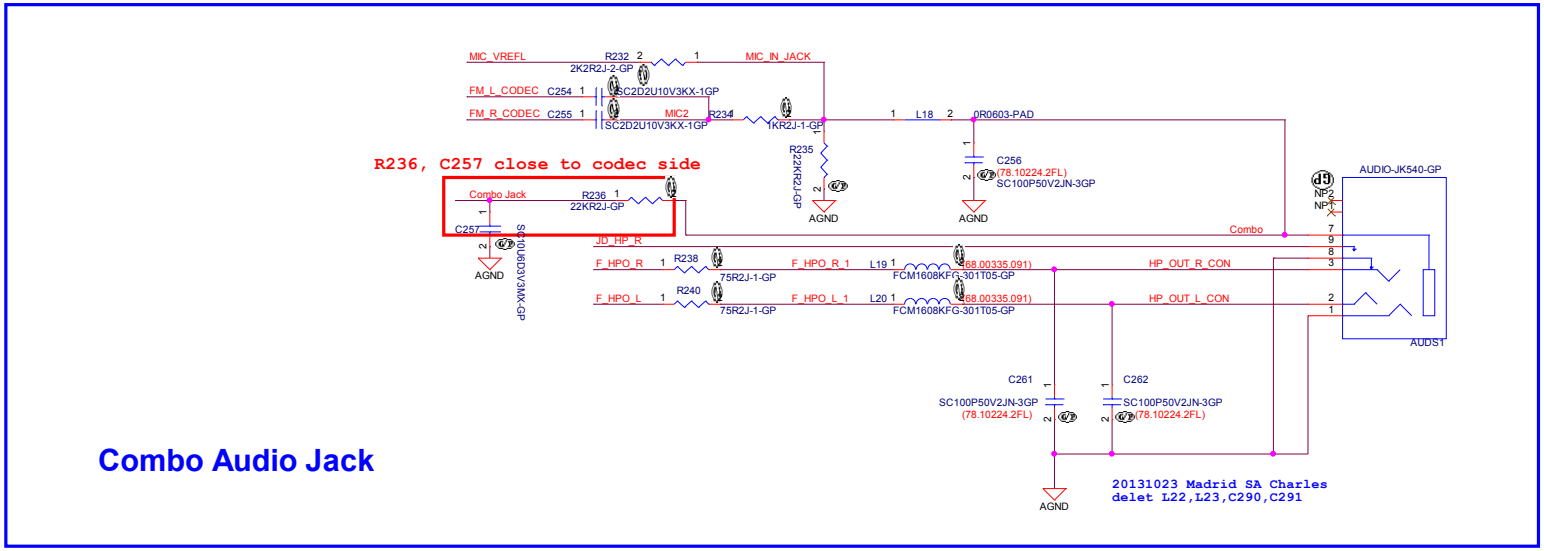
Size A | Document Number Bolton195i | Rev -1A

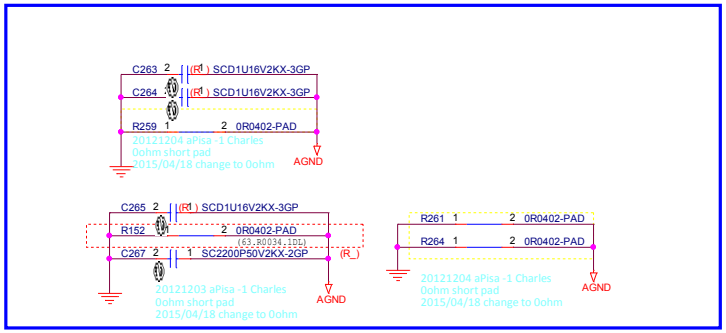
Date: Thursday, August 27, 2015 | Sheet 28 of 111

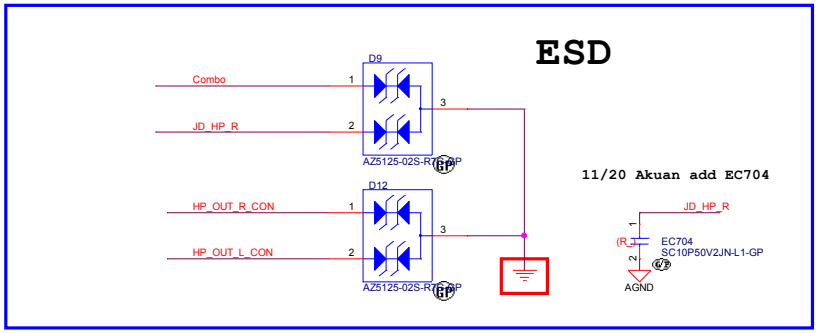
Control

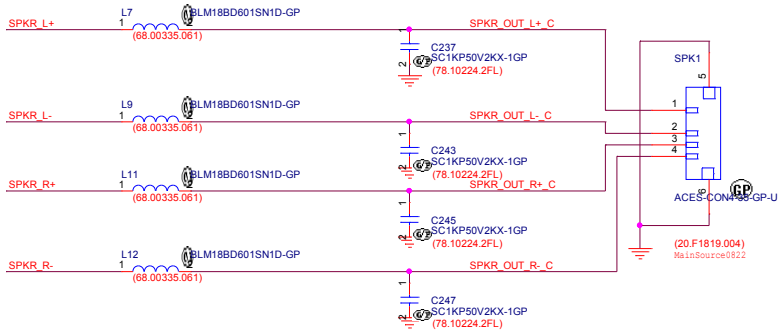
27 JD_HP_R
27 FM_L_CODEC
27 FM_R_CODEC
27 MIC_VREFL
27 F_HPO_R
27 F_HPO_L
27 SPKR_L+
27 SPKR_L-
27 SPKR_R-
27 SPKR_R+
27 Combo Jack

2012/08/28_aPisa_SA









wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
Title: MIC/SPKR/AUDIO JACK			
Size: Custom	Document Number: Bolton195i		Rev: -1A
Date: Thursday, August 27, 2015	Sheet 29 of 111		

BUZZER
Del 2015/04/18

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Hsichih, Taipei Hsien

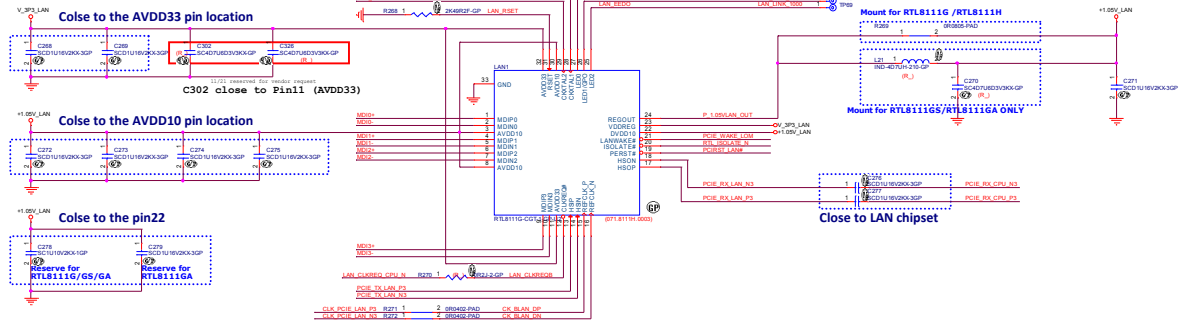
Title **BUZZER**

Size	Document Number	Rev
A	**Bolton195i**	-1A

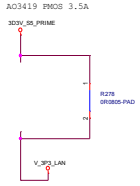
Date: Thursday, August 27, 2015 Sheet 30 of 111

Giga LAN

Bogis 20121222
Change solution to RTL8111GA



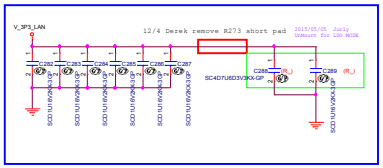
Lan Power



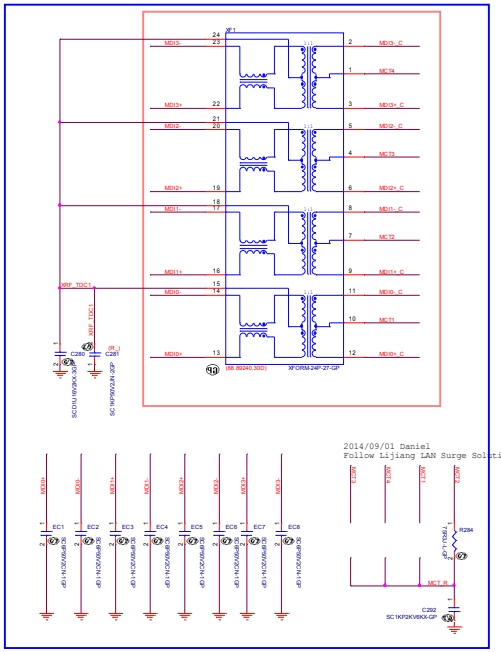
The V_3P3_LAN rise time must be controlled between 0.5ms and 100ms
Bolton195 test can 0R Pass

IC	P/N	L21	R269	C270
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R
RTL8111H	071.8111H.0003	R	M	R

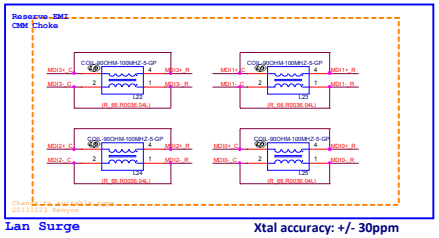
M:Mount
R:Reserved

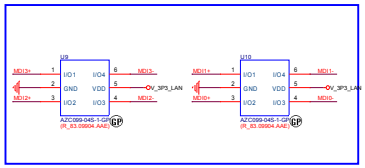


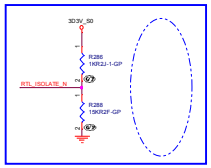
11/18 Akuan dummy



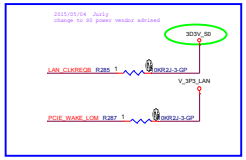
2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down



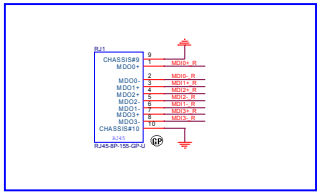




Bogis 20121222
Remove LAN_ENSWREG
Del R292 R300

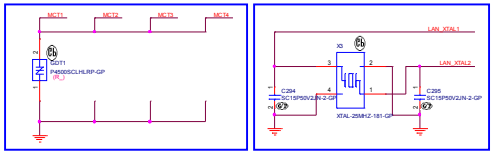


Bogis 20121222
no EECS EEDI
Del R301 R302

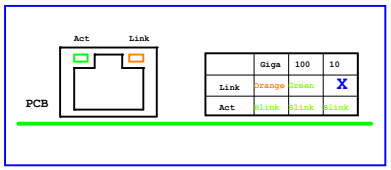


Lan Surge

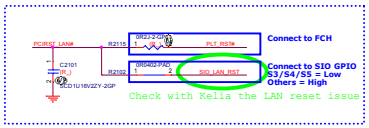
Xtal accuracy: +/- 30ppm



2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down



	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink



Layout close to CPU/FCH/PCH

@. Check PU power well

wistron
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Hsichih, Taipei Hsien

Title: LAN (RTL8111GA)
Size: D
Document Number: Bolton195
Rev: -1A
Date: Thursday, August 27, 2015
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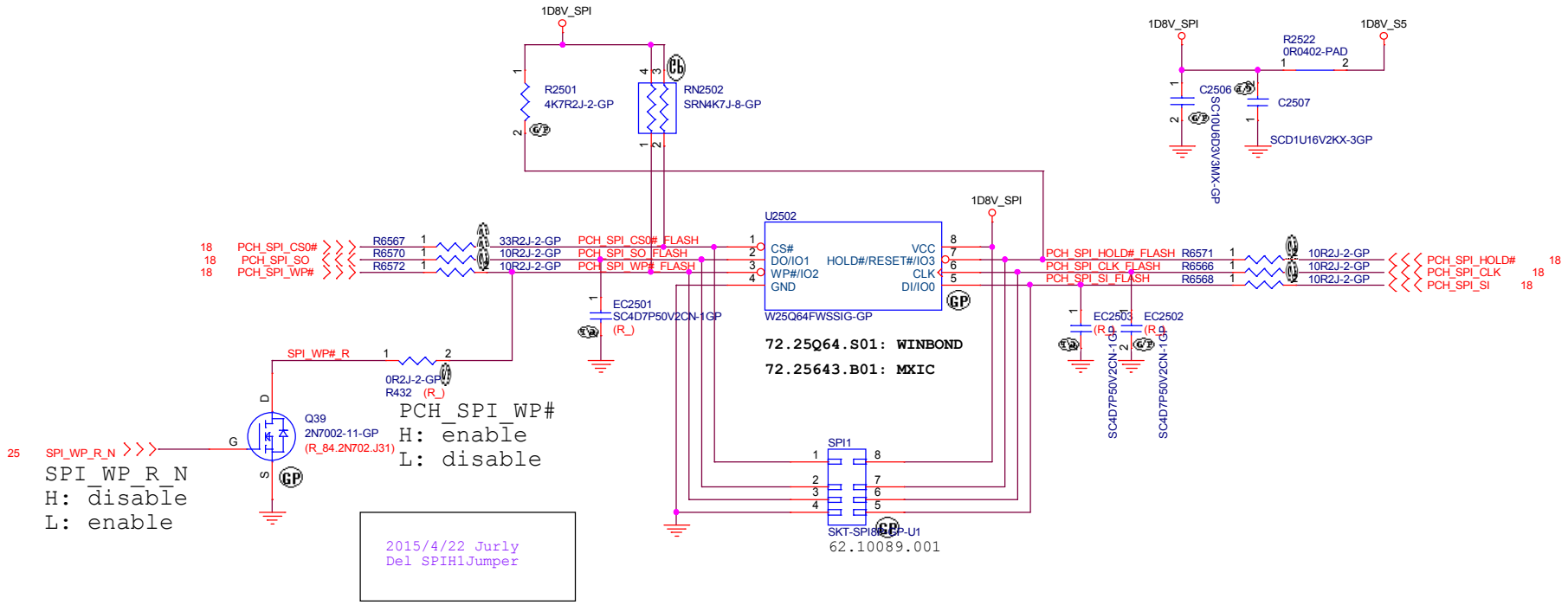
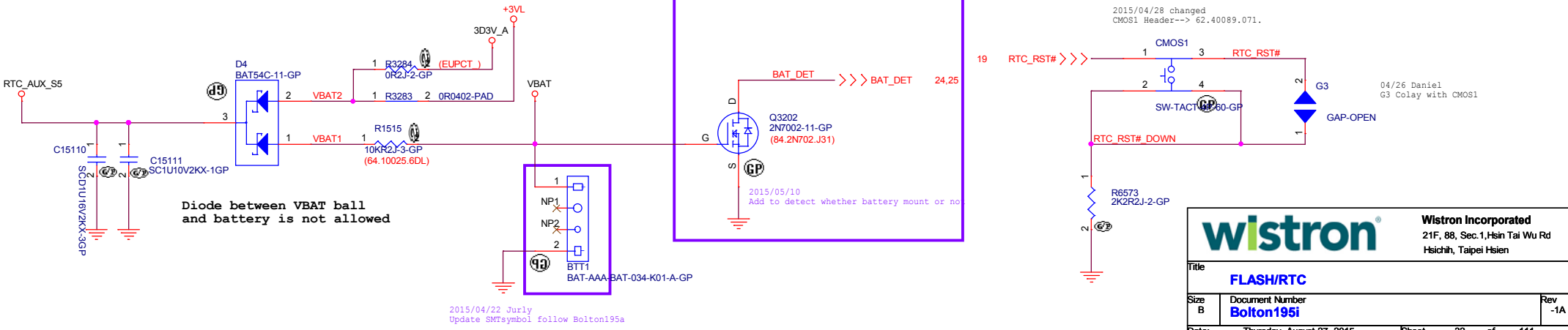
SPI FLASH ROM (8M Byte) for PCH



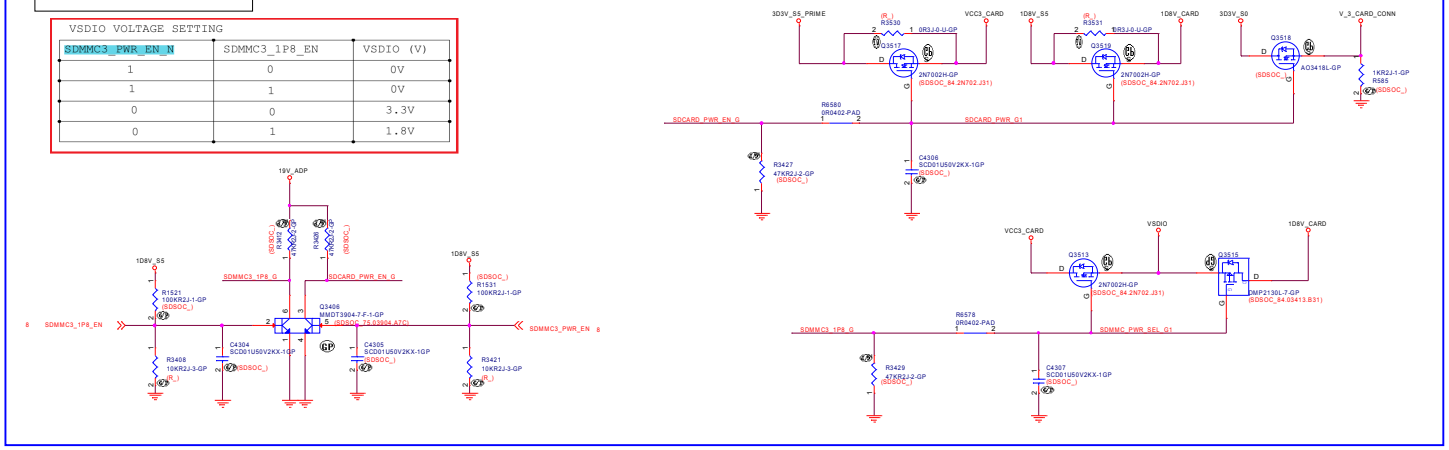


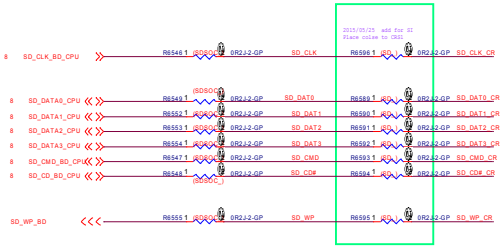
wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	FLASH/RTC	
Size B	Document Number Bolton195i	Rev -1A
Date: Thursday, August 27, 2015	Sheet 32 of 111	

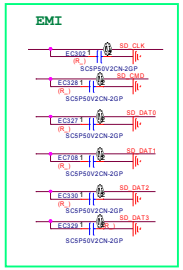
VSDIO POWER

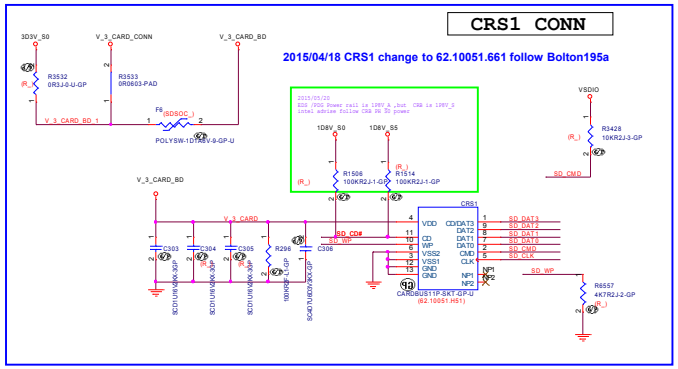
VSDIO VOLTAGE SETTING

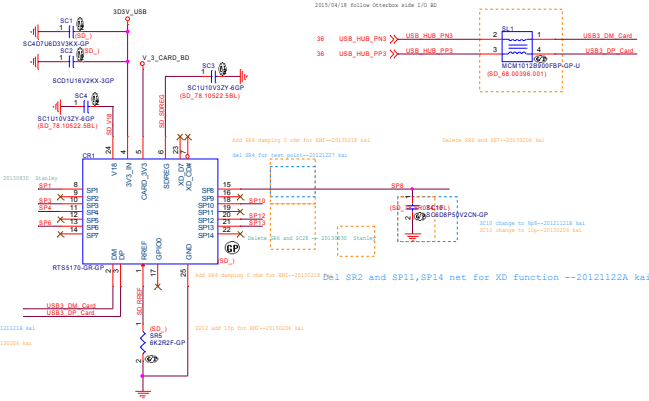
SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO (V)
1	0	0V
1	1	0V
0	0	3.3V
0	1	1.8V



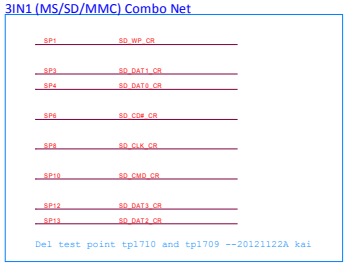








3IN1 (MS/SD/MMC) Combo Net



wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Card Reader IC		
Size: Custom	Document Number: Bolton195i	Rev: -1A
Date: Thursday, August 27, 2015	Sheet 33 of 111	

Reserve

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
034_USB Charger

Size
A

Document Number
Bolton195i

Rev
-1A

Date: Thursday, August 27, 2015

Reserve

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB redriver (Reserved)

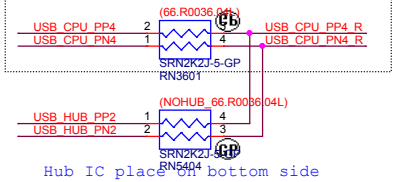
Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 35 of 111

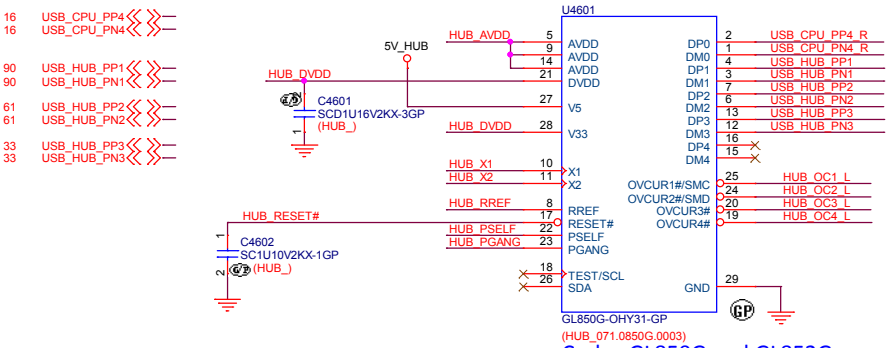
GL850G
Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
Set USB port to be internal (non-removable): set OC pin is floating
Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

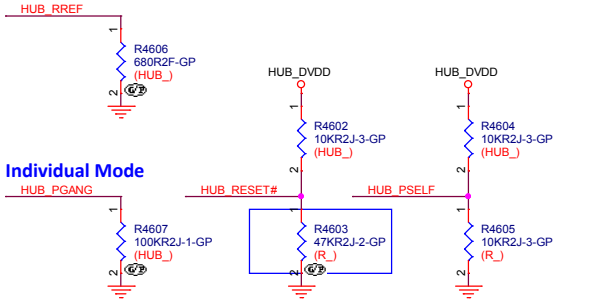
GL852G
Enable/Disable USB output port: setting by EEPROM
Set USB port to be internal (non-removable) or external (removable): setting by EEPROM

20140717 David
vendor suggest add series resister
between CPU & HUB for debug purpose



Hub IC place on bottom side
RN5404 place on top side

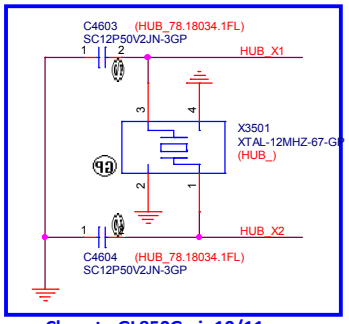




HUB_PSELF = 1 if self-powered
HUB_PSELF = 0 if bus-powered

Co-lay GL850G and GL852G
GL850G: 71.0850G.003 (USB2.0 STT 1 to 4)
GL852G: 71.00852.A03 (USB2.0 MTT 1 to 4)

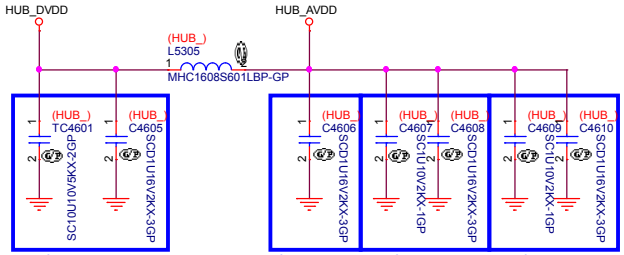
Xtal accuracy: +/- 30ppm



Close to GL850G pin10/11

Internal Power

(Hub Internal VR output from pin 28 V33 = HUB_DVDD)

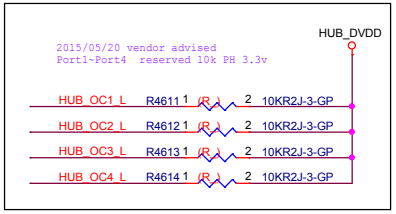


close to PIN28 | Close to pin 5 | Close to pin 9 | Close to pin 14

Over Current

	R divider Removable	Floating Non-Removable
OVCUR1#		V
OVCUR2#		V
OVCUR3#		V
OVCUR4#	NA	NA

external internal

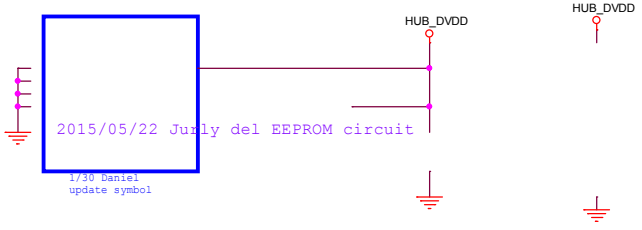


Bogis 20131014
Change X3501 to 82.30006.641

2nd source: 82.30006.501

EEPROM

EEPROM is used for customized VID, PID, String, Configuration
The purpose is to set 4 USB ports to be internal/external
Default settings: 4 ports are external ports



USB Table

Pair	Device	
1	Internal USB2.0 for TOUCH	internal
2	Internal USB2.0 for BT	internal
3	Internal USB2.0 for Card reader	internal
4	NA	

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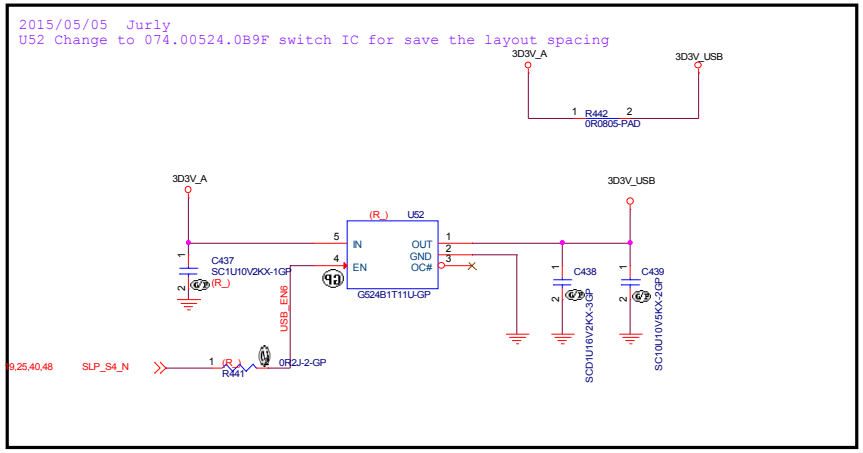
Hsichih, Taipei Hsien

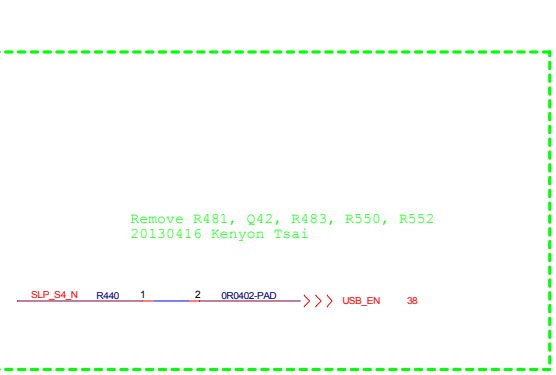
Title: USB2.0 HUB
Size: Custom | Document Number: Bolton195i | Rev: -1A
Date: Thursday, August 27, 2015 | Sheet 36 of 111

SSID = USB

2015/05/05 Jurly
U52 Change to 074.00524.0B9F switch IC for save the layout spacing



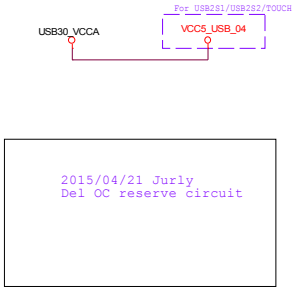
Remove R481, Q42, R483, R550, R552
20130416 Kenyon Tsai

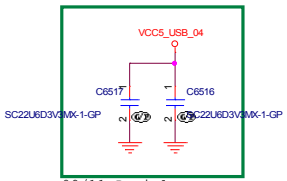


USB2.0 Port -> REAR I/O

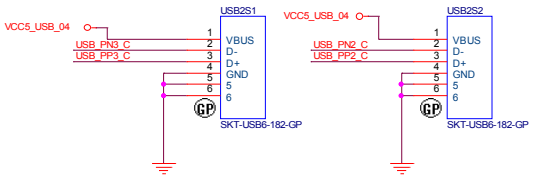
2015/04/28 changed
USB2.0 CONN 22.10254.211--> 22.10218.H01

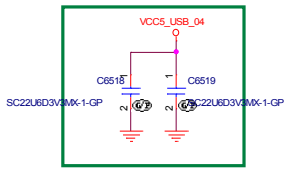
12/11 Derek add EUP power for other USB30





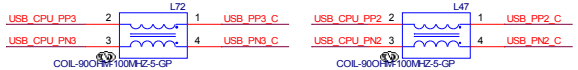
09/11 Daniel
Add MLCC Close to USB2S1

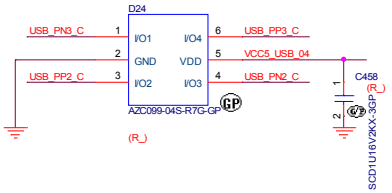




09/11 Daniel
Add MLCC Close to USB2S1

11/27 Derek mount CMC





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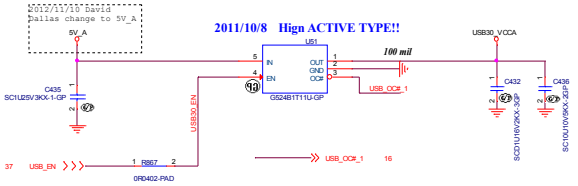
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB2.0 conn

Size: Custom | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 37 of 111

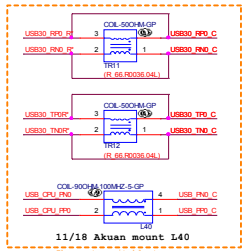
Modified to meet Dallas SPEC on 20121002 Kenyon.

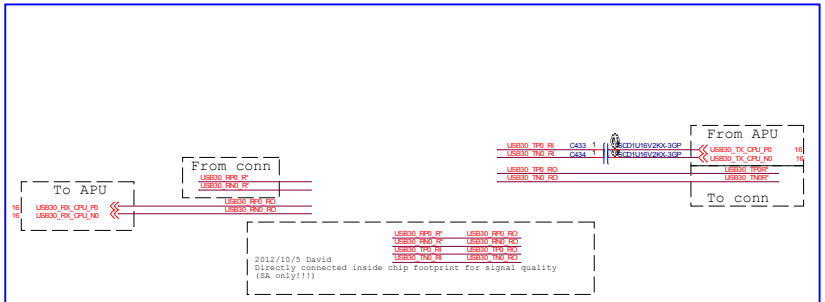


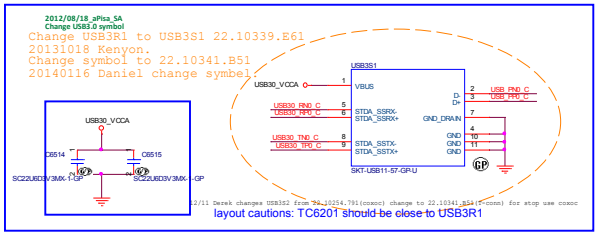
2011/10/12

EMI

Modified to meet Dallas SPEC on 20121002 Kenyon.

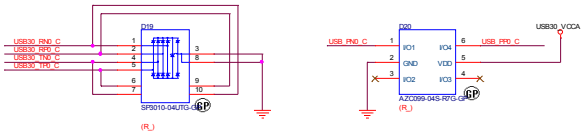




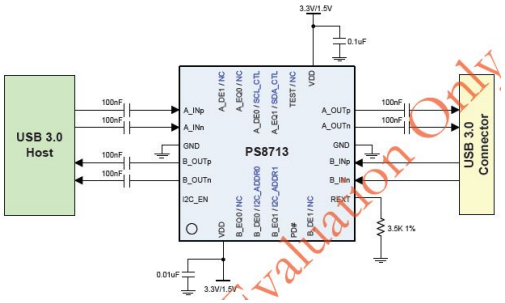


USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

Modified to meet Dallas SPEC on 20121002 Kenyon.



ESD



Modified to meet Dallas SPEC on 20121002 Kenyon.

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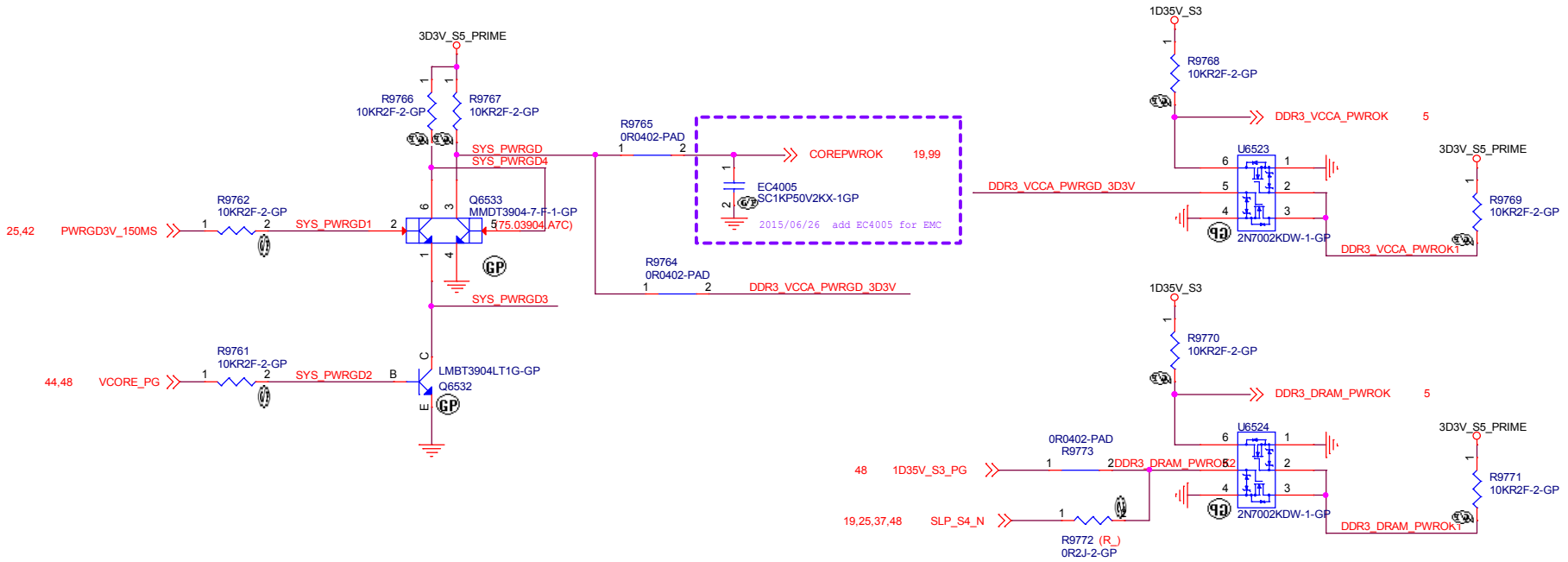
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB3.0 conn

Size: Custom | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 38 of 111

Wistron Incorporated	21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	USB3.0 conn
Size: B	Document Number: Bolton195i
Rev: -1A	
Date: Thursday, August 27, 2015	Sheet 39 of 111



For AC OFF SEQUENCE

2015/05/04 del

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Power Plane EN Sequence		
Size: B	Document Number: Bolton195i	Rev: -1A
Date: Thursday, August 27, 2015	Sheet 40 of 111	

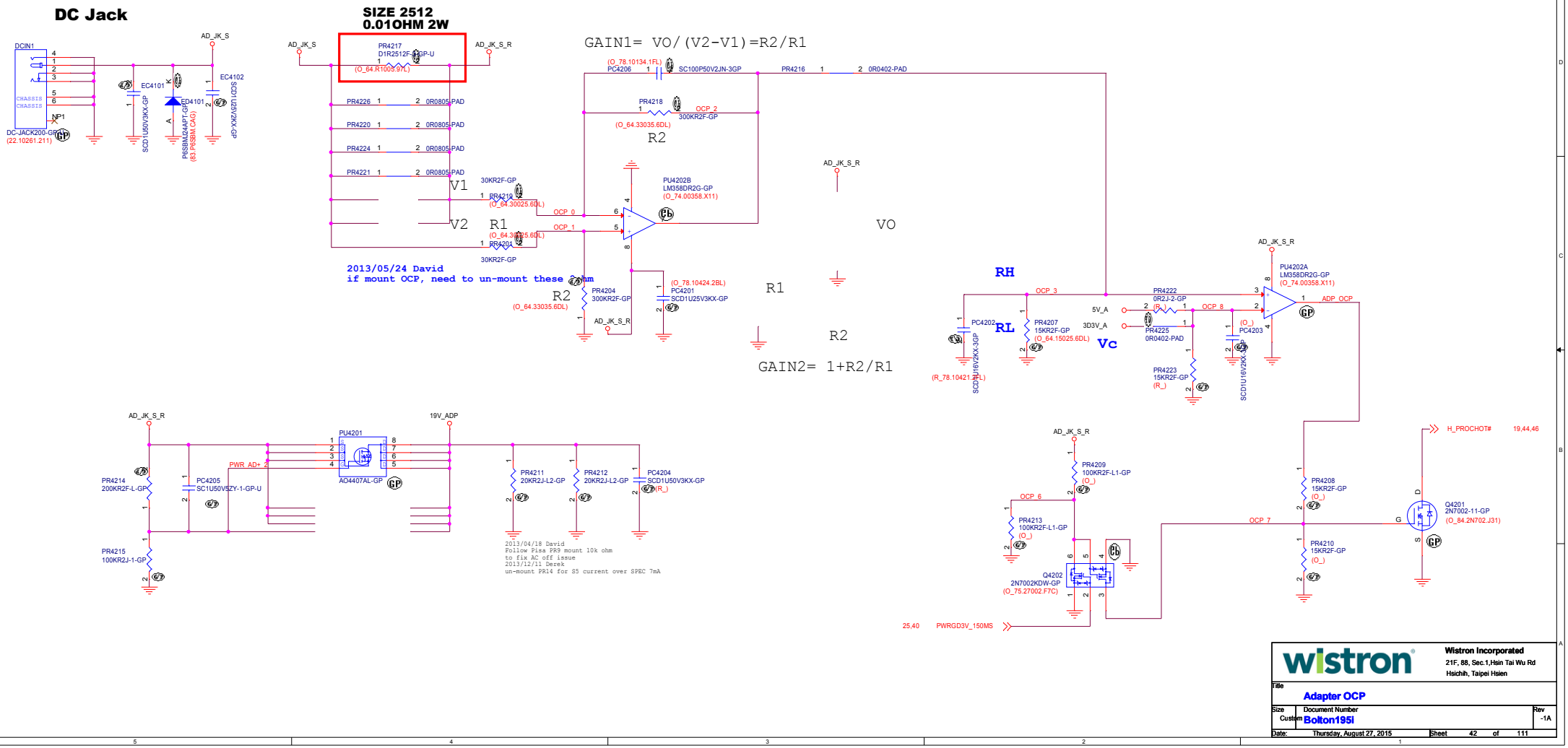
Reserve

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: ATX/DCIN

Size: A | Document Number: Bolton195i | Rev: -1A

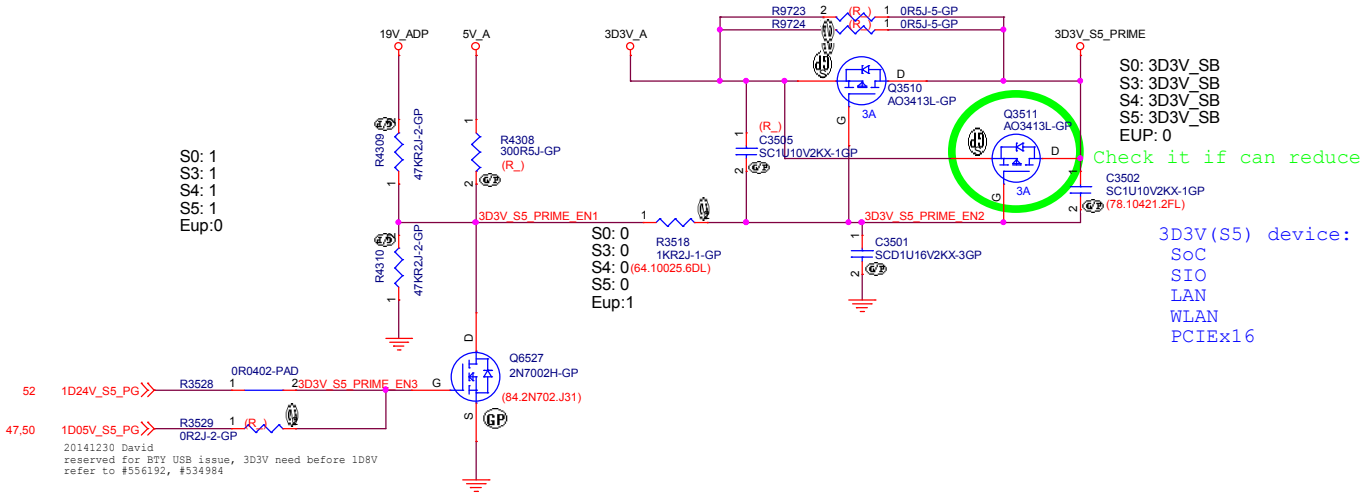
Date: Thursday, August 27, 2015 | Sheet 41 of 111


DC Jack
SIZE 2512
0.01OHM 2W
GAIN1= VO/(V2-V1)=R2/R1
GAIN2= 1+R2/R1
2013/05/24 David
if mount OCP, need to un-mount these 2 ohm
2013/04/18 David
Follow Pisa PR9 mount 10k ohm
to fix AC off issue
2013/12/11 Derek
un-mount PR14 for S5 current over SPEC 7mA
RH
RL
Vc
V1
V2
R1
R2
VO
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Adapter OCP
Bolton195I
Thursday, August 27, 2015
Sheet 42 of 111

PSU Eup Power Control

2014/04/29 Jurly
Del 5V_AUX circuit

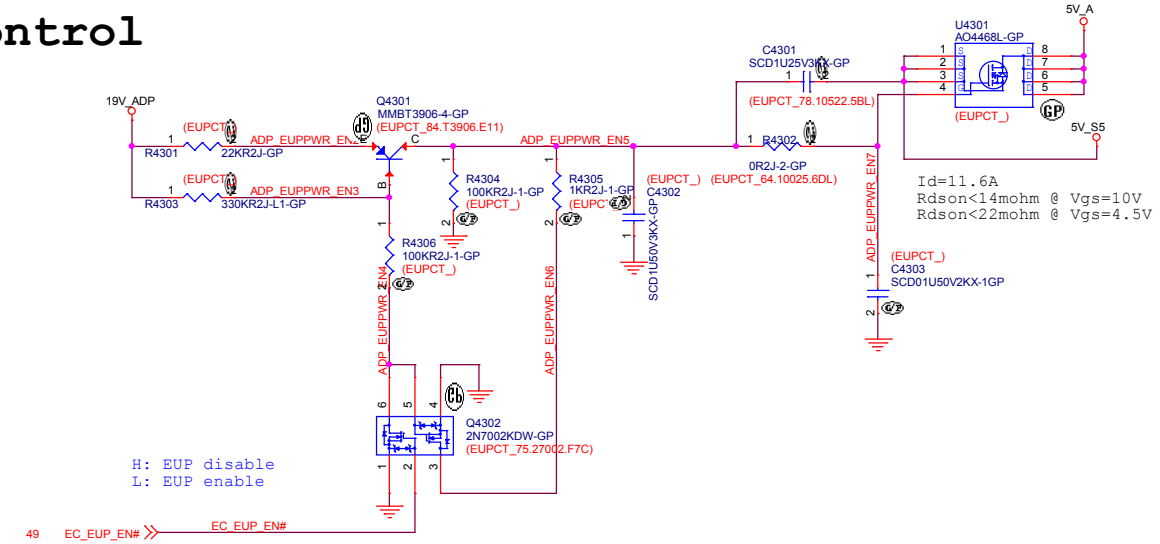
3D3V_S5_PRIME



3D3V(S5) device:
SoC
SIO
LAN
WLAN
PCIEx16

	SIO_EUP_EN	SLP_S3_N	5V_DUAL
S0	0	1	5V_S0
S3	0	0	5V_SB
S4	0	0	5V_SB
S5	0 (EUP disable)	0	5V_SB
S5	1 (EUP enable)	0	0

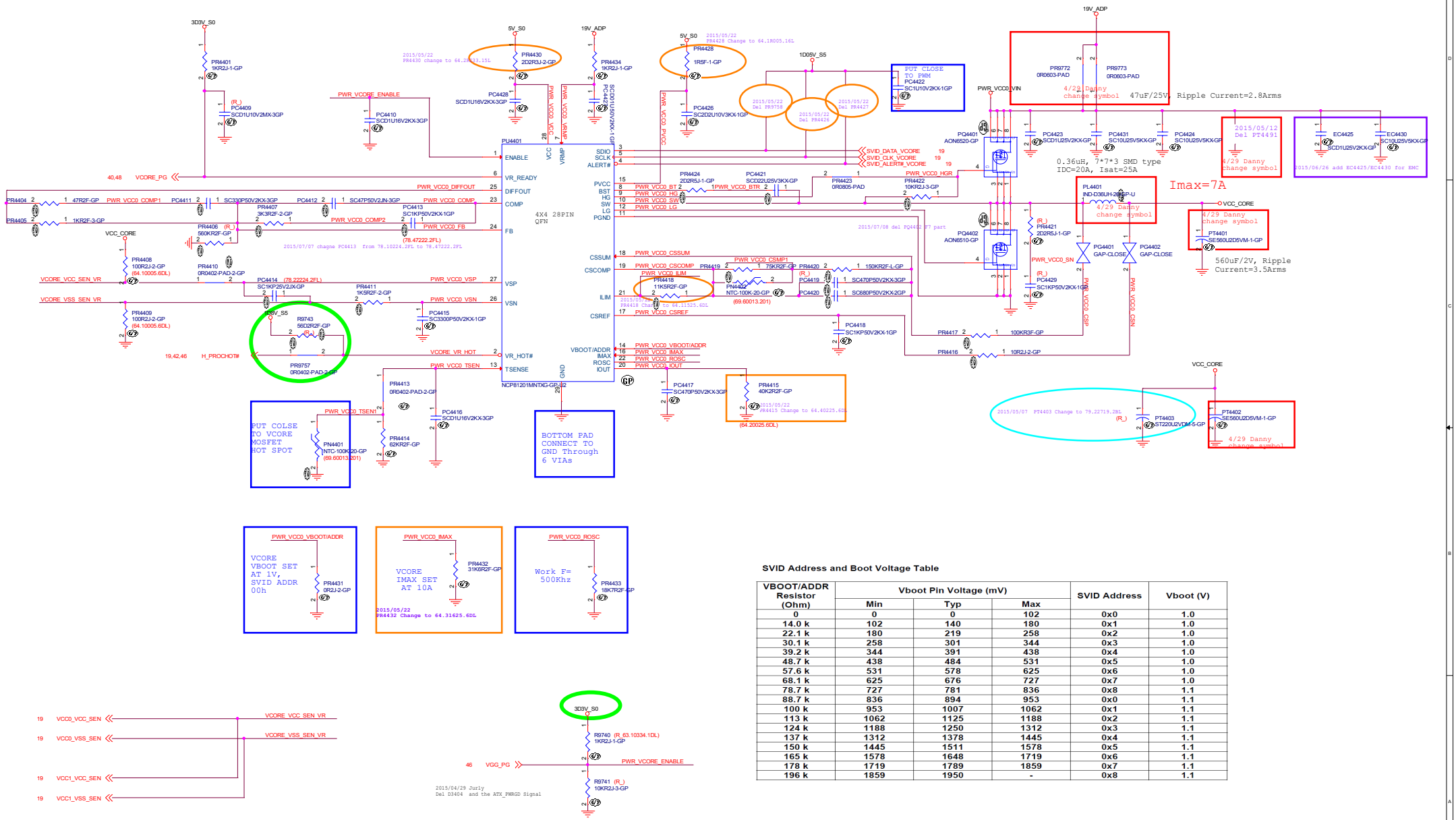
ADP Eup Power Control



Wistron Incorporated	21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	DS3/Eup power
Size: Custom	Document Number: Bolton195i
Rev	-1A
Date: Thursday, August 27, 2015	Sheet 43 of 111

12V_S0 -> VCC_CORE

VR12.1 POWER CKT - 1 phase 12Vin



SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

<Variant Name>

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU Core1 (NCP81201)

Size: Custom | Document Number: Bolton195i | Rev: -1A

Date: Friday, August 28, 2015 | Sheet 44 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

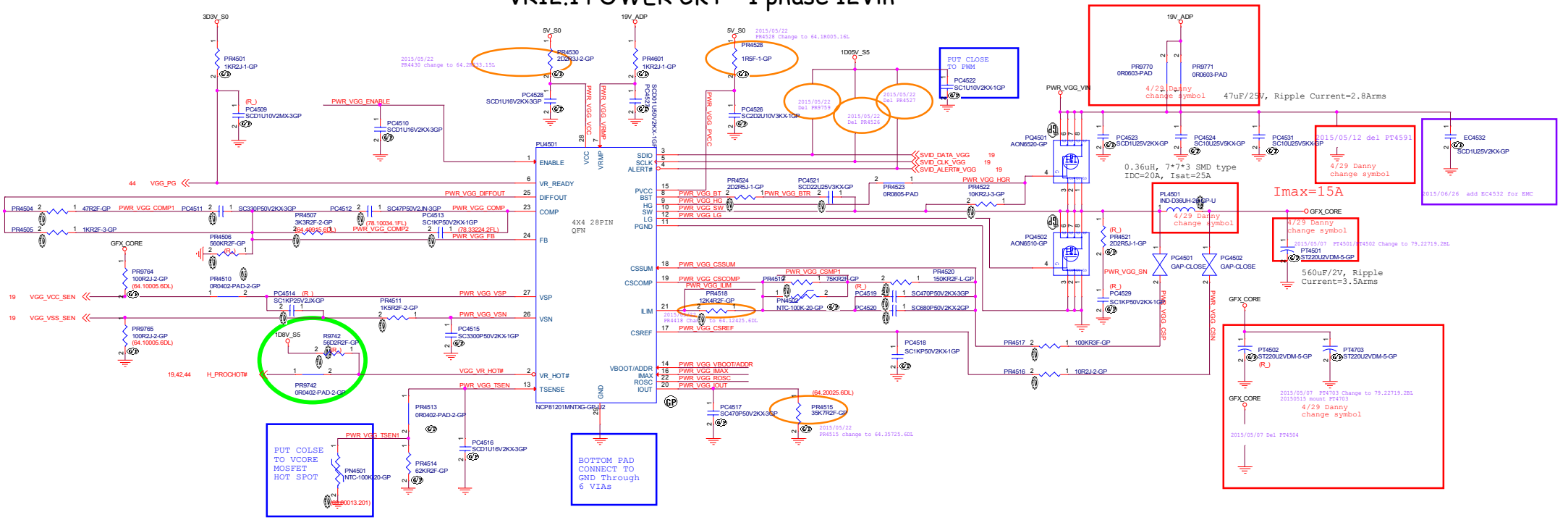
Title
CPU Core2 (Reserved)

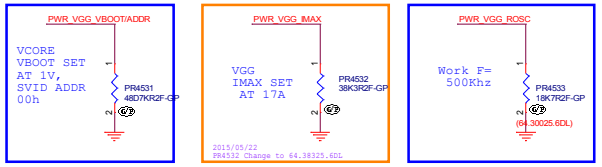
Size A | Document Number Bolton195i | Rev -1A

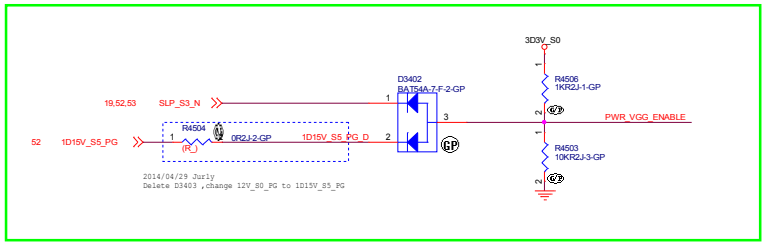
Date: Thursday, August 27, 2015 | Sheet 45 of 111

12V_S0 -> GFX_CORE

VR12.1 POWER CKT - 1 phase 12Vin







SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

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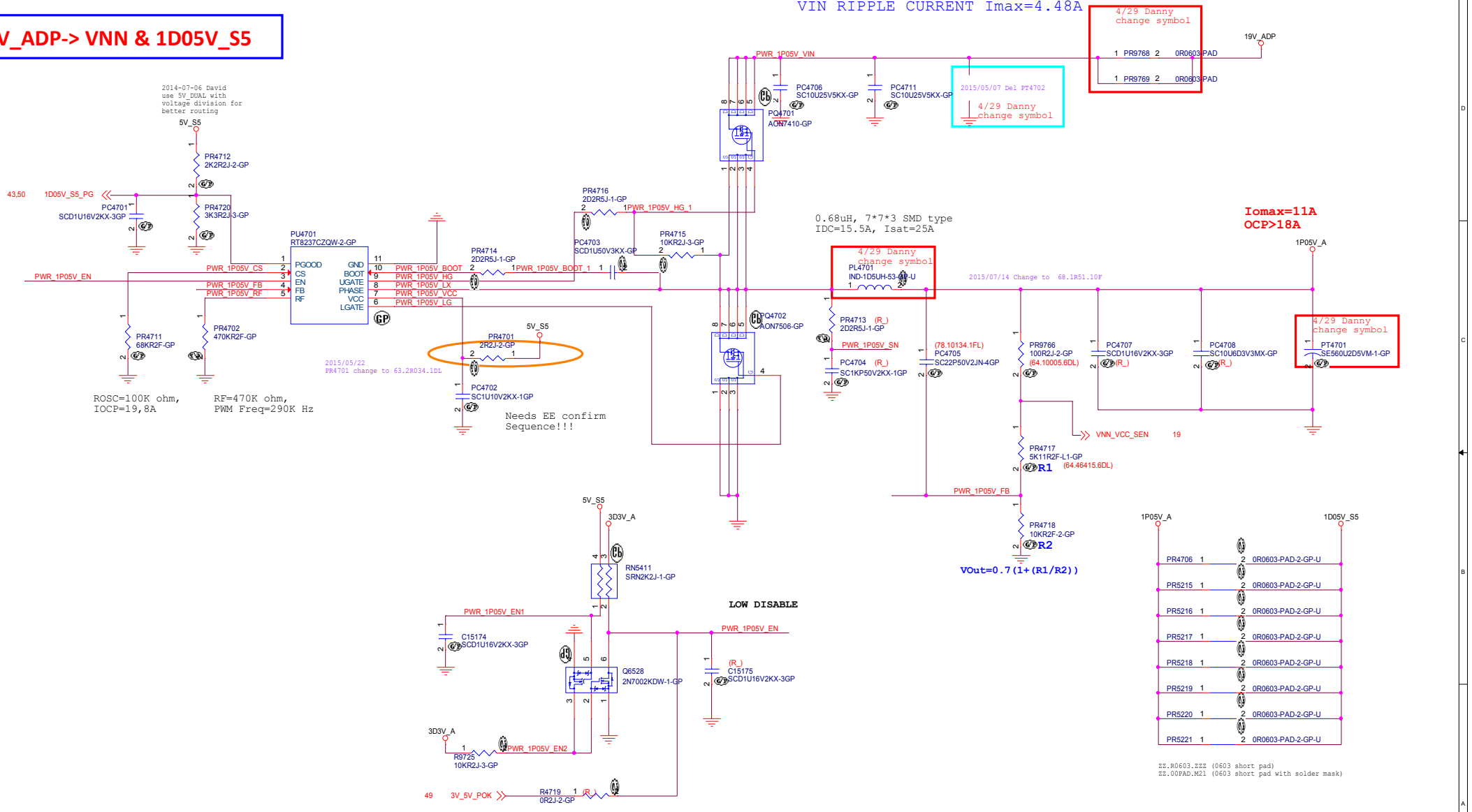
Hsichih, Taipei Hsien
Title: CPU AXG/GFX (NCP81201)
Size: Custom | Document Number: Bolton195I | Rev: -1A
Date: Friday, August 28, 2015 | Sheet 46 of 111

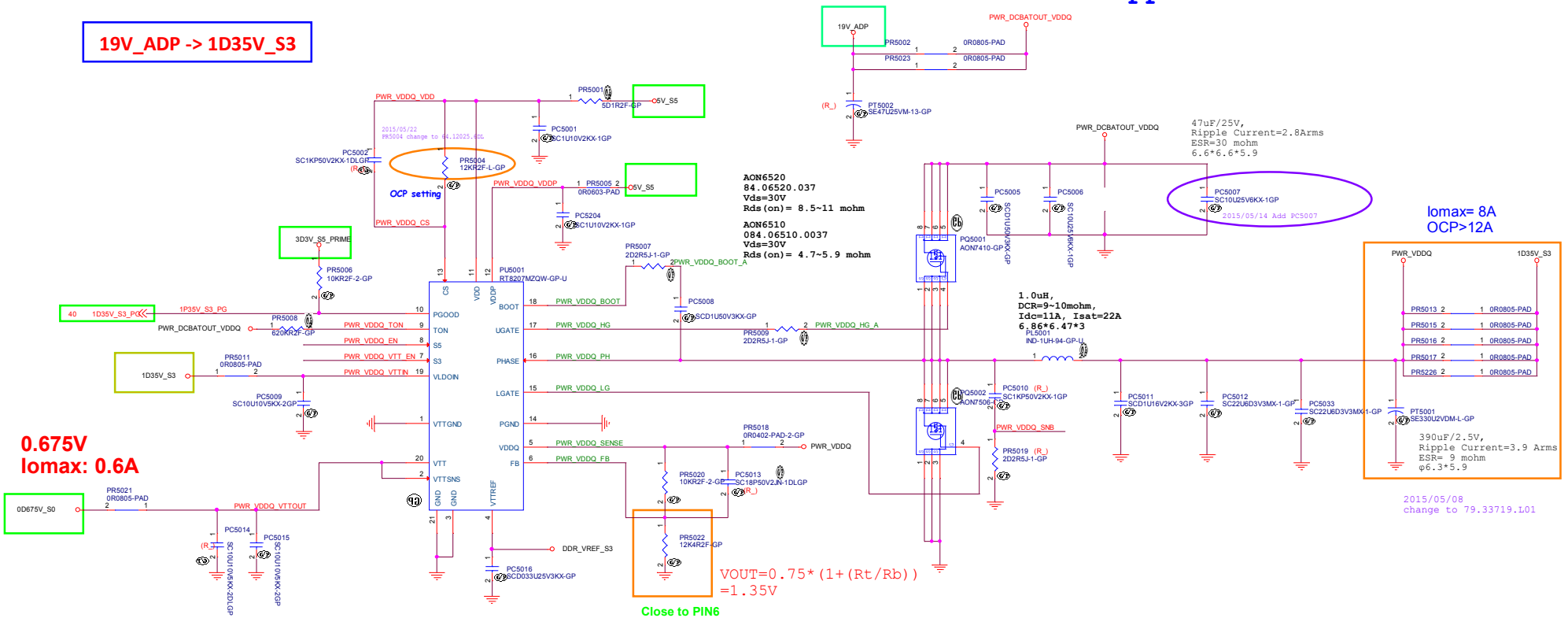
19V_ADP-> VNN & 1D05V_S5



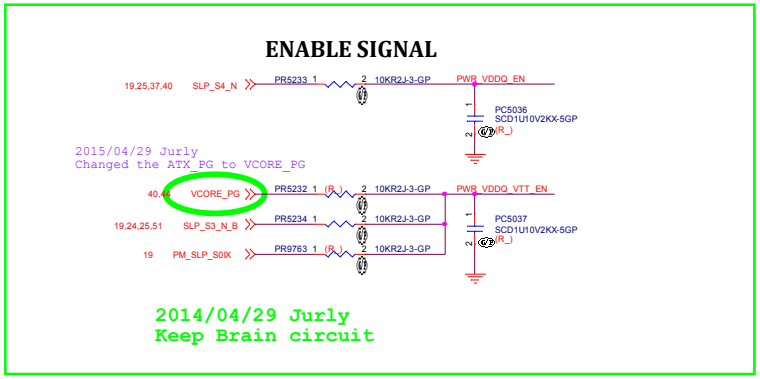
Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
Title: CPU VCCSA/VNN (RT8237C)		
Size: Custom	Document Number: Bolton195i	Rev: -1A
Date: Thursday, August 27, 2015	Sheet 47 of 111	

Vin ripple=2.05A

19V_ADP -> 1D35V_S3



ENABLE SIGNAL



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DCDC-1D35V (RT8207M)

Size: Custom | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 48 of 111

19V_A -> 3D3V_A/5V_A

power team

EE

V_3P3_A

84.07410.A37 AON7410
Vgs @ 4.5V,
Id = 8A,
Rds(on) = 16~29mohm,
Qg = 3.6~5.5nC

84.07506.037 AON4703
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 13~15.8mohm,
Qg = 4.3~5.8nC

Iomax=4.47A
OCP>6.705A

3.3uH, DCR=28~30mohm,
Idc=6A, Isat=13.5A 7*7

220uF/6.3V,
ESR=15mohm
Ripple Current =3110mA

Vout = 2*(1+R1/R2)
= 2*(1+6.65/10)
= 3.33V

OCP setting

EC_EUP_EN#
H: EUP disable
L: EUP enable

V_5P0_A

84.07410.A37 AON7410
Vgs @ 4.5V,
Id = 8A,
Rds(on) = 16~29mohm,
Qg = 3.6~5.5nC

84.07506.037 AON4703
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 13~15.8mohm,
Qg = 4.3~5.8nC

Iomax=5.32A
OCP>10A

3.3uH, DCR=28~30mohm,
Idc=6A, Isat=13.5A 7*7

220uF/6.3V,
ESR=15mohm
Ripple Current =3110mA

Vout = 2*(1+R1/R2)
= 2*(1+15/10)
= 5.0V

Table 2. Power Up Sequencing(RT8243A/B)

ENLDO (V)	SECFB	ENTRIP1	ENTRIP2	LDO5 (V)	LDO3 (V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On	On	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	Off

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Hsichih, Taipei Hsien

Title: DCDC-3D3V/5V

Size: Custom | Document Number: Bolton19SI | Rev: -1A

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19V_ADP -> 1D8V_S5

PWR_1D8V

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Vin ripple=0.88A

47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9

Need EE to check

2014/04/29 Jurly
add change the PR to 3D3V_SB

3D3V_A
PR5104 10KR2J-3-GP
52 1D8V_S5_PG
PC5106 SCD1U10V2KX4-GP (78.10421.2FL)

PU5101 RT8237CZQW-2-GP
PWR_1V8_PG
PWR_1V8_CS
PWR_1V8_EN
PWR_1V8_FB
PWR_1V8_RF
PGOOD
CS
EN
FB
RF
GND
BOOT
UGATE
PHASE
VCC
LGATE
PWR_1V8_BOOT
PWR_1V8_HG
PWR_1V8_PH
PWR_1V8_VCC
PWR_1V8_LG

PWR_1V8_BOOT_A
PR5106 2D2R5J-1-GP
PC5105 SCD1U25V3KX-GP (78.10424.2BL)

PR5107 2D2R5J-1-GP
PWR_1V8_HG_A

PR5112 30KR2F-GP
2015/05/22
PR5112 change to 64.30025.6DL
OCP setting

PR5111 470KR2F-GP

5V_S5
PR5113 2D2R5J-1-GP
PC5109 SC1U6D3V2KX-GP (78.10523.5FL)

PWR_DCBATOUT_1D8V
PC5102 SCD1U25V2KX-2-GP (78.10422.5FL)
PC5103 SC10U25V6KX-1GP
2015/05/13 Del PT5101
PC5107 SC10U25V6KX-1GP
EC5110 SCD1U25V2KX-GP
2015/06/26 add EC5110 for EMC

PQ5101 AON7410-GP
PQ5102 AON7410-GP
PR5119 (R_) 2D2R5F-2-GP
PWR_1V8_SNB
PC5108 (R_) SC1KP50V2KX-1GP

PL5101 IND-1D5UH-53-GP-U
1.5uH,
DCR=14~15mohm,
Idc=9A, Isat=18A
7*7*3

PG5101 GAP-CLOSE-PWR-3-GP
PWR_1V8_FB_A
PR5120 34K8R2F-1-GP
R1
(R_) PC5112 SC22P50V2JN-4-LL-GP
PR5118 22KR2F-GP
R2

Vout=0.704*(1+R1/R2)
=0.704*(1+10/22)
=1.8176

Iomax= 3A
OCP>4.5A

PWR_1D8V
PC5101 SC10U6D3V3MX-GP
PT5107 SE390U2D5VM-11-GP

390uF/2.5V,
Ripple Current=3.9 Arms
ESR= 9 mohm
φ6.3*5.9

19V_ADP
PR5102 0R0805-PAD
PR5103 0R0805-PAD

PWR_1D8V
1D8V_S5
PR5114 0R0805-PAD
PR5101 0R0805-PAD
PR5115 0R0805-PAD
PR5116 0R0805-PAD

2015/04/29 Jurly
add Enable signals follow Brain

LOW DISABLE

43,47 1D05V_S5_PG
R9728 0R0402-PAD
PWR_1V8_EN
3D3V_S5_PRIME
R5004 0R2J-2-GP
PC5219 SCD1U16V2KX-3GP

20141230 David
reserved for RTY USB issue, 3D3V need before 1D8V
refer to #556192, #534984

19V_A -> 12V_S0

2015/04/28 Jurly
del 12V_S0 power

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

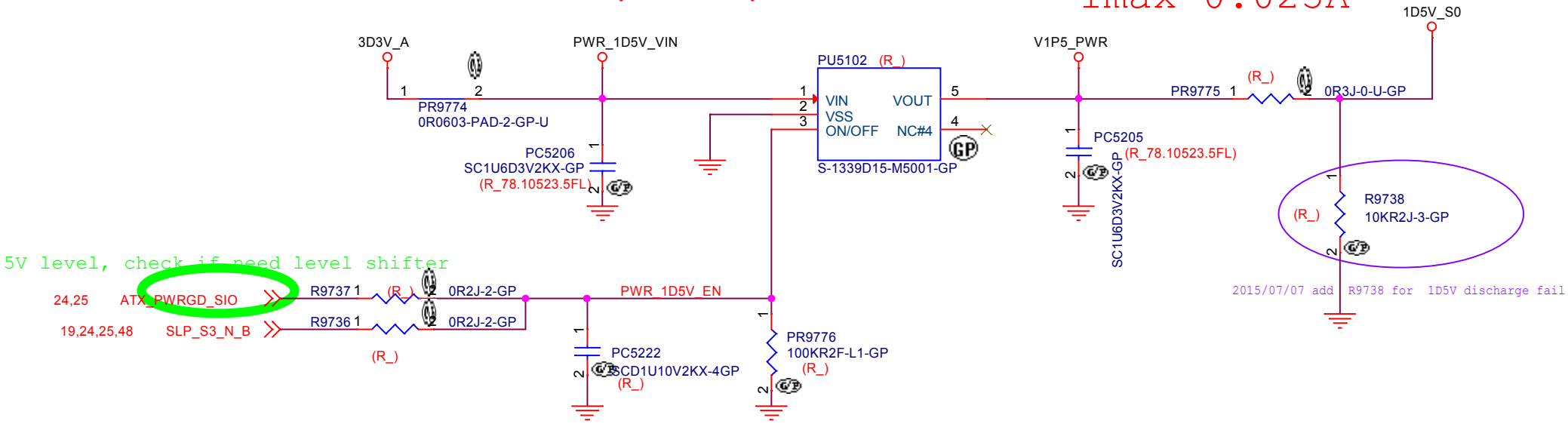
Title: DCDC-1D15V (RT8237C)
Size: Custom
Document Number: Bolton1951
Rev: -1A
Date: Thursday, August 27, 2015
Sheet 50 of 111

3D3V_SB -> 1D5V_S0

Iomax=0.42A

PD=(Vin-Vout)*Iomax
=(3.3-1.5)*0.025A=0.045W

Imax=0.025A



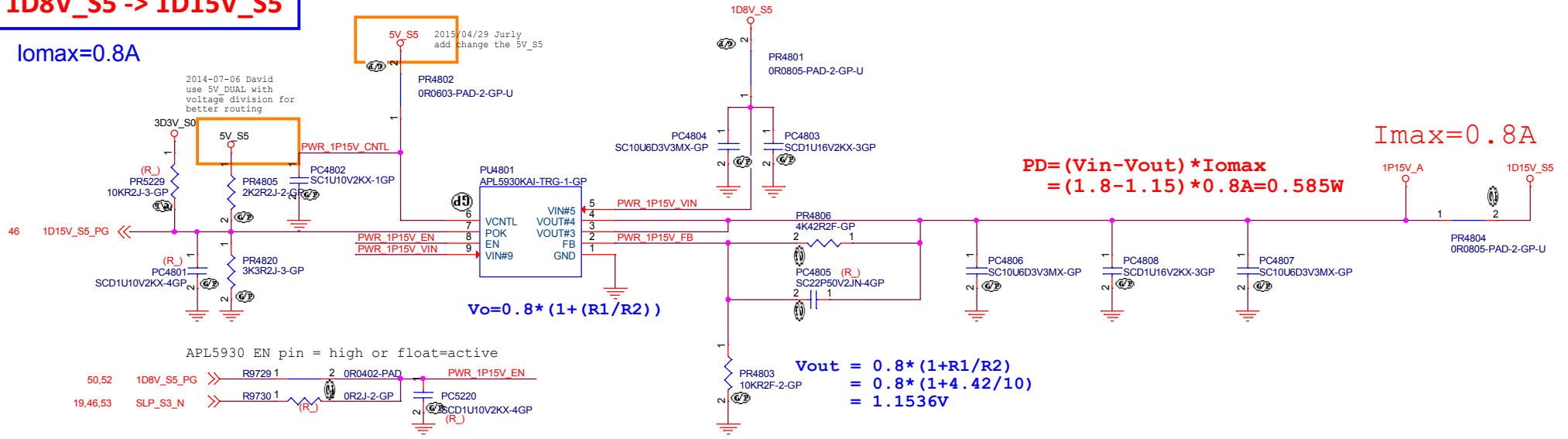
5V_SB -> 3D3V_SB

2015/4/26 del

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: LDO-1D5V (APL5930)		
Size: Custom	Document Number: Bolton195i	Rev: -1A
Date: Thursday, August 27, 2015	Sheet 51 of 111	

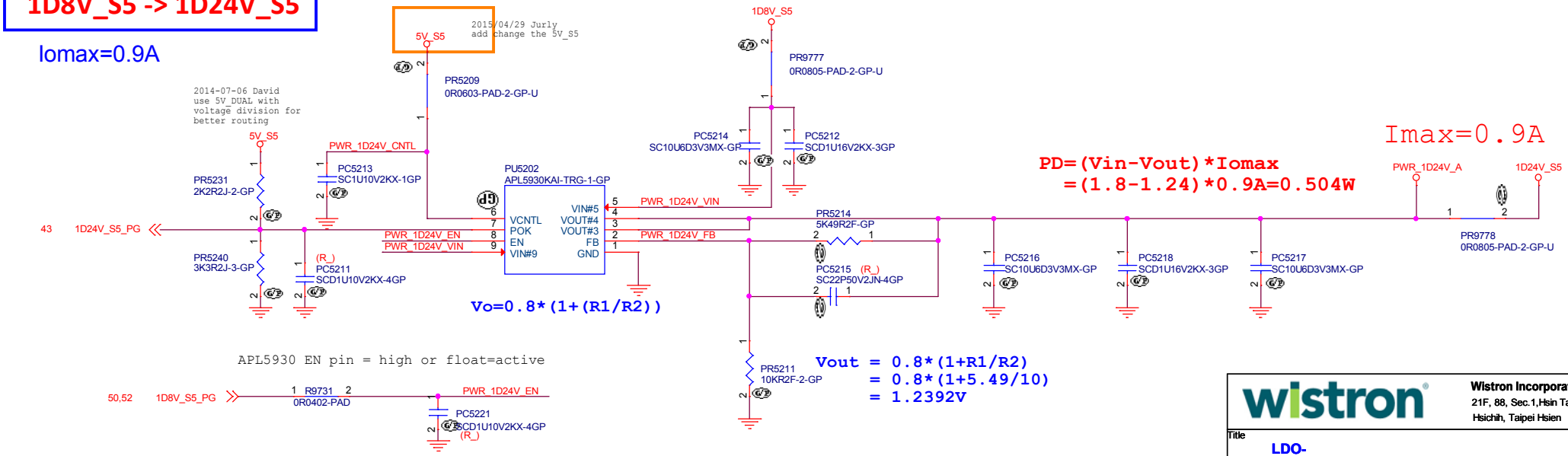
1D8V_S5 -> 1D15V_S5

Iomax=0.8A



1D8V_S5 -> 1D24V_S5

Iomax=0.9A



wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LDO-

Size	Document Number	Rev
B	Bolton195i	-1A

Date: Thursday, August 27, 2015 Sheet 52 of 111

(Reserved)

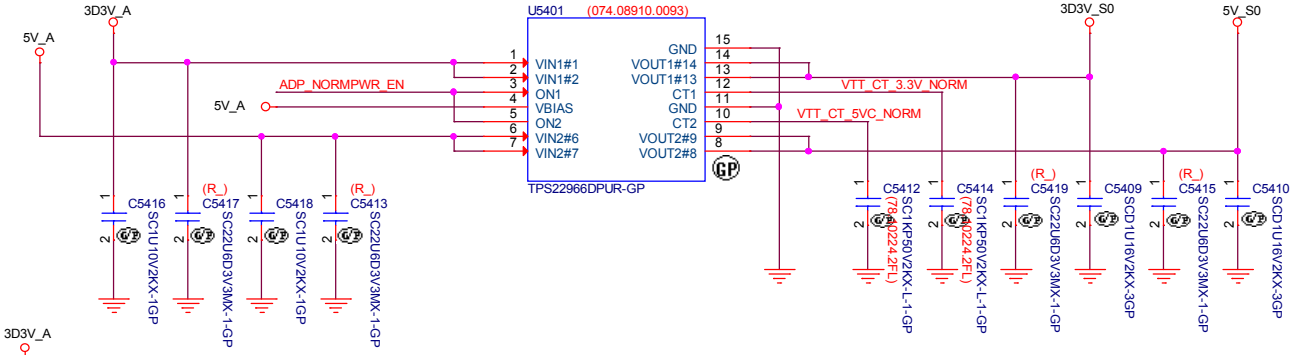
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

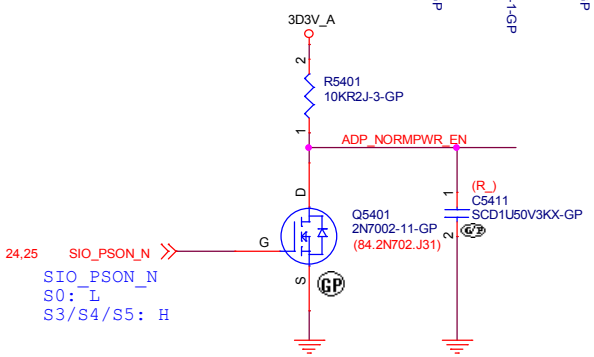
Title: Switch power- (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 53 of 111

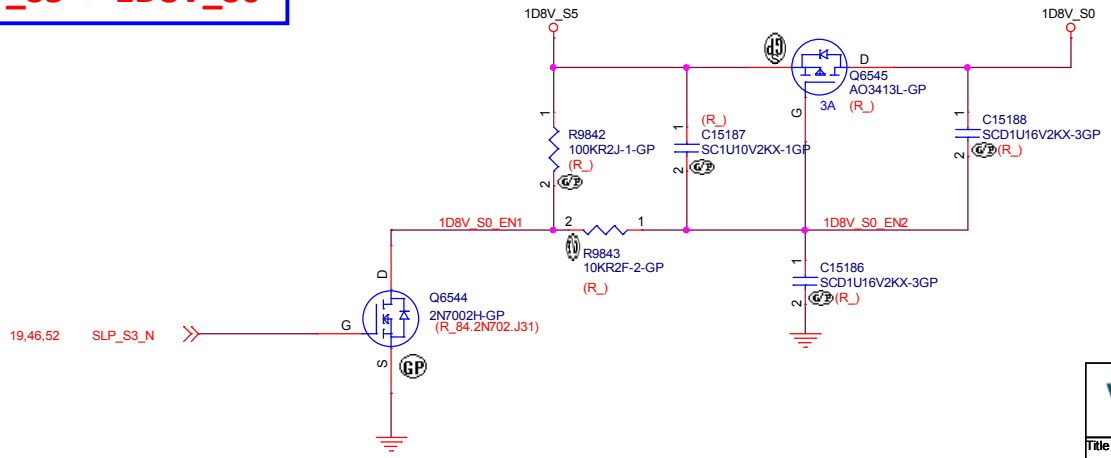
3D3V_A -> 3D3V_S0
5V_A -> 5V_S0





2014/12/17 Gary
PSU mount C5409,C5410
Customer request MB Main Power Rail Design & Quality

1D8V_S5 -> 1D8V_S0



wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
Title	Switch power-1D24V (RT8068A		
Size: Custom	Document Number: Bolton195i		Rev: SA
Date: Thursday, August 27, 2015	Sheet 54 of 111		

SSID = VIDEO

LCD ID

CONVERTOR SMB

12,15,57,61,99 SMB_DATA
12,15,57,61,99 SMB_CLK

LVDS For Scalar

55,57 EDP_LVDS_L0_N
55,57 EDP_LVDS_L0_P
55,57 EDP_LVDS_L1_N
55,57 EDP_LVDS_L1_P
55,57 EDP_LVDS_L2_N
55,57 EDP_LVDS_L2_P
55,57 EDP_LVDS_L3_N
55,57 EDP_LVDS_L3_P
55,57 EDP_LVDS_LC_N
55,57 EDP_LVDS_LC_P

55,57 EDP_LVDS_U0_N
55,57 EDP_LVDS_U0_P
55,57 EDP_LVDS_U1_N
55,57 EDP_LVDS_U1_P
55,57 EDP_LVDS_U2_N
55,57 EDP_LVDS_U2_P
55,57 EDP_LVDS_U3_N
55,57 EDP_LVDS_U3_P
55,57 EDP_LVDS_UC_N
55,57 EDP_LVDS_UC_P

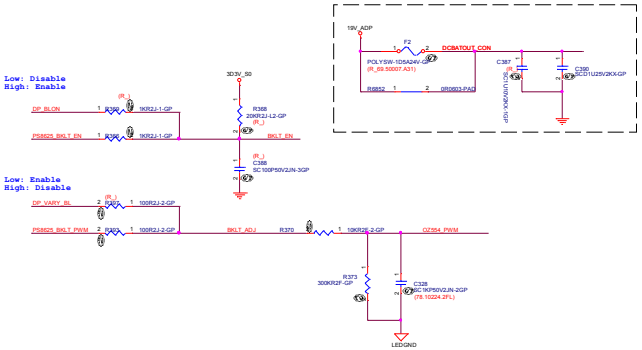
8 DP_BLON
8,57 DP_VARY_BL

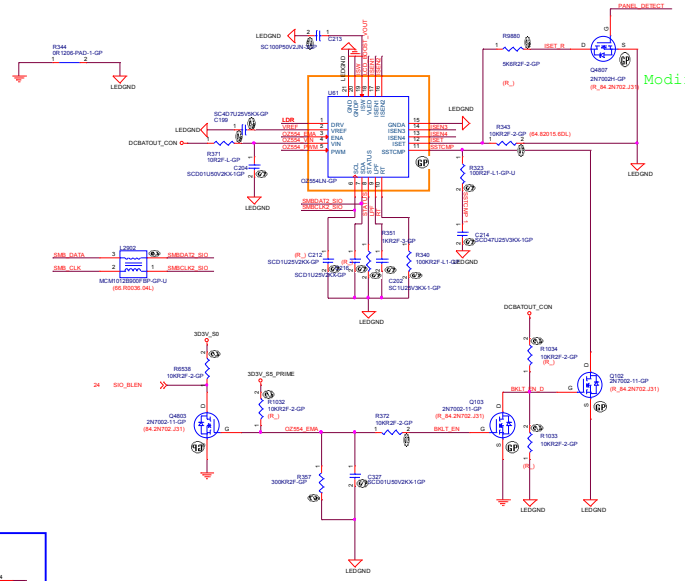
LVDS For eDP translator

55,57 EDP_LVDS_L0_N
55,57 EDP_LVDS_L0_P
55,57 EDP_LVDS_L1_N
55,57 EDP_LVDS_L1_P
55,57 EDP_LVDS_L2_N
55,57 EDP_LVDS_L2_P
55,57 EDP_LVDS_L3_N
55,57 EDP_LVDS_L3_P
55,57 EDP_LVDS_LC_N
55,57 EDP_LVDS_LC_P

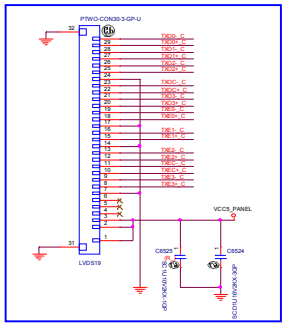
55,57 EDP_LVDS_U0_N
55,57 EDP_LVDS_U0_P
55,57 EDP_LVDS_U1_N
55,57 EDP_LVDS_U1_P
55,57 EDP_LVDS_U2_N
55,57 EDP_LVDS_U2_P
55,57 EDP_LVDS_U3_N
55,57 EDP_LVDS_U3_P
55,57 EDP_LVDS_UC_N
55,57 EDP_LVDS_UC_P

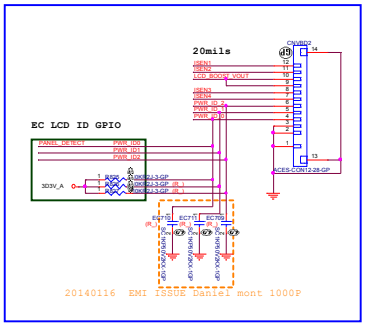
57 PS8625_BKLT_PWM
8 DP_DIGON
57 PS8625_BKLT_EN
57 PS8625_LCD_PW_EN
43,49 PANEL_DETECT



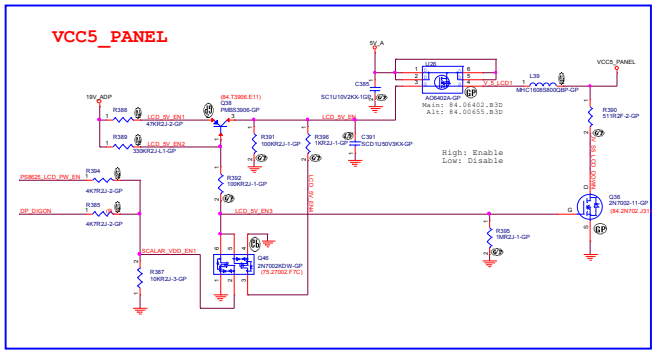


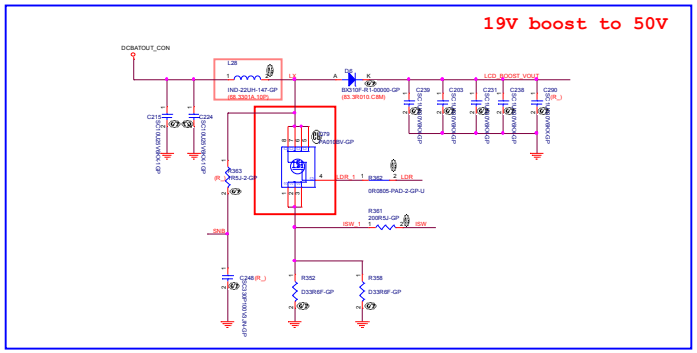
Modified by Kenyon. Use CMC to choose signal source. 2012/11/07





Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF5-TLF1	0	0	1	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF3-SLL1	0	1	0	3,4 Vout 1,6 RTN 2,5 N.C
CMI M195FGE-L23 C1	1	0	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C3	1	1	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C1	1	1	1	1,2,5,6 Vout 3,4 RTN





wistron Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LVDS/Converter
Size: Custom
Document Number: Bolton18SI
Rev: -1A
Date: Thursday, August 27, 2015
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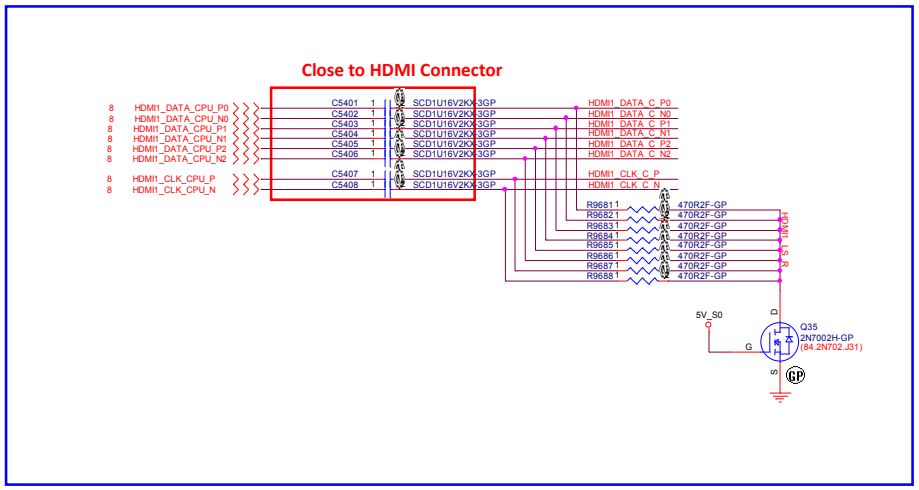

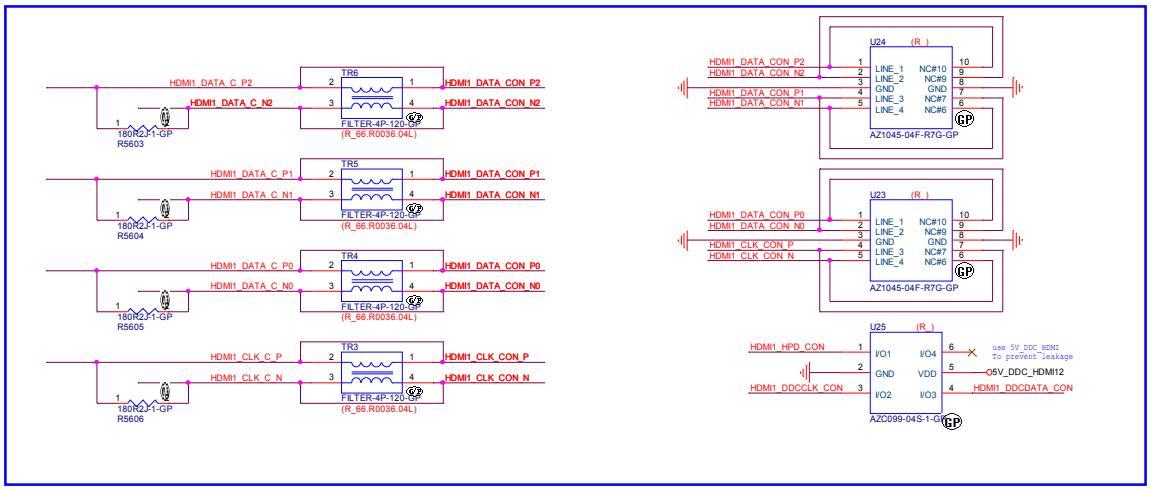

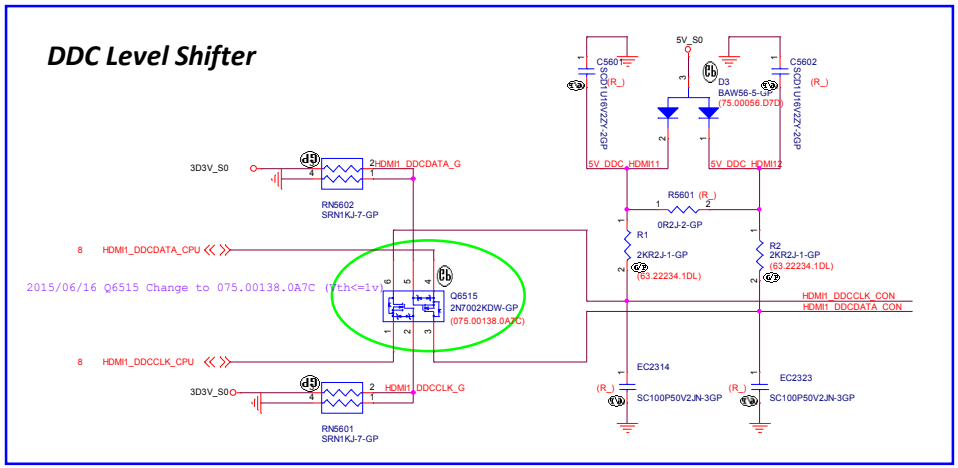

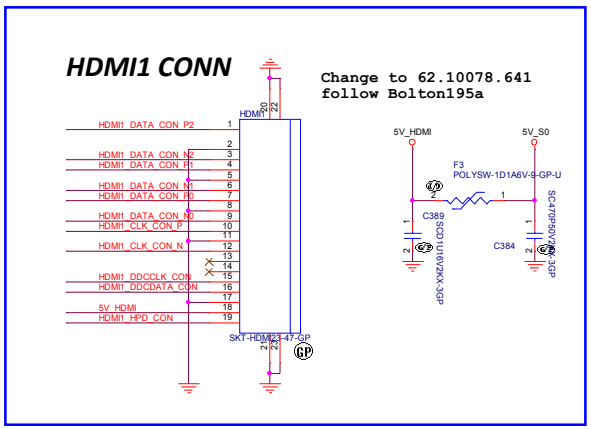

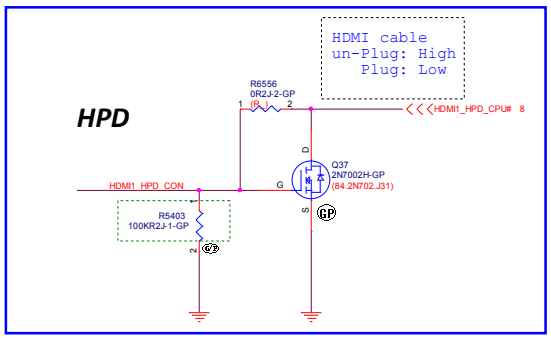

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI conn/Level Shifter

Size	Document Number	Rev
Custom	Bolton195i	-1A

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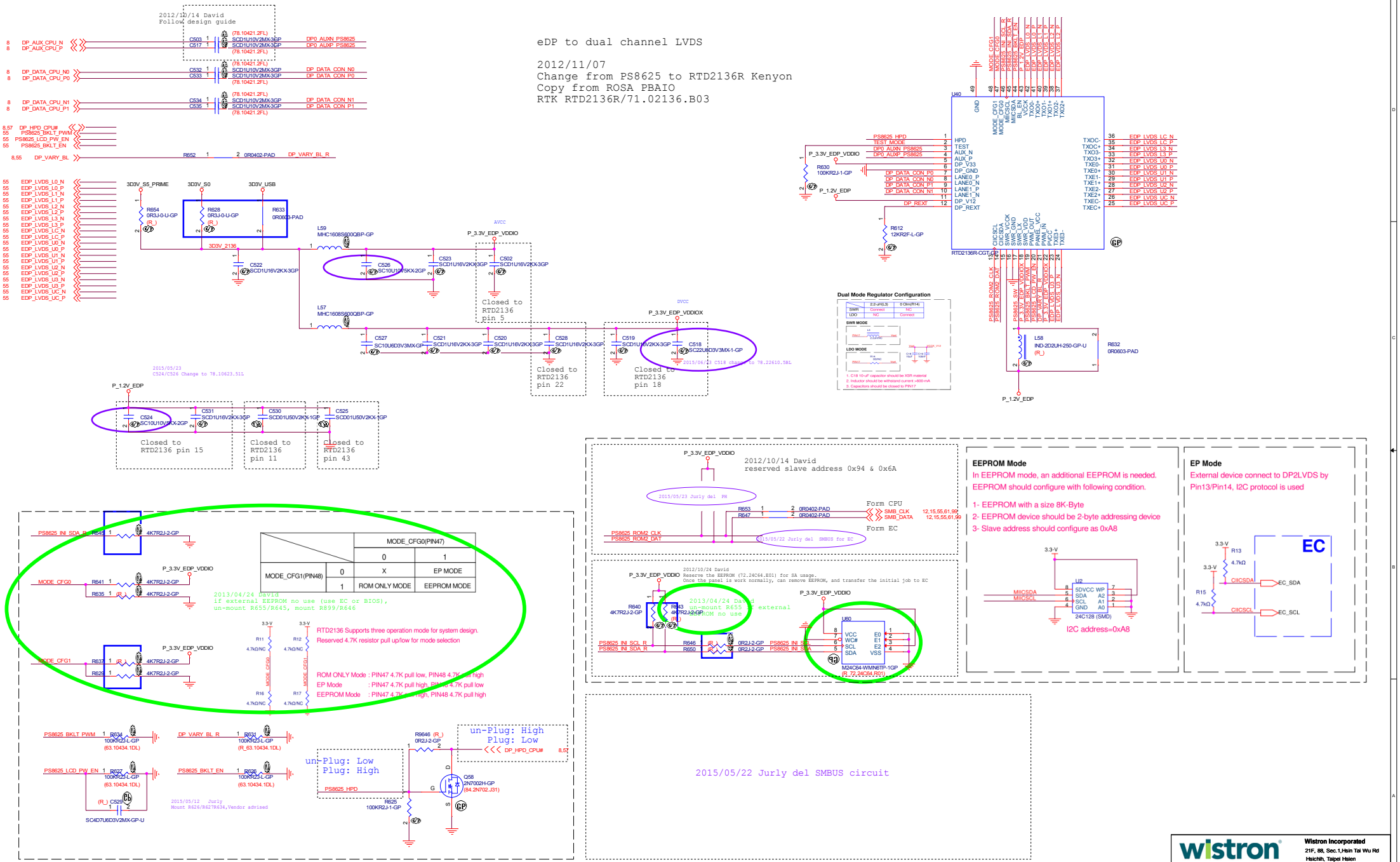
eDP to dual channel LVDS

2012/11/07
Change from PS8625 to RTD2136R Kenyon
Copy from ROSA PBAIO
RTK RTD2136R/71.02136.B03



Wistron Incorporated	
21F, 88, Sec.1,Hsin Tai Wu Rd	
Hsichih, Taipei Hsien	
Title	RTD2136 eDP to LVDS
Size: Custom	Document Number: Bolton1951
Rev	-1A
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2015/4/22
Del VGA

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
DVI/VGA conn(Reserve)

Size	Document Number	Rev
A	**Bolton195i**	-1A

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
Display switch

Size	Document Number	Rev
A	**Bolton195i**	-1A

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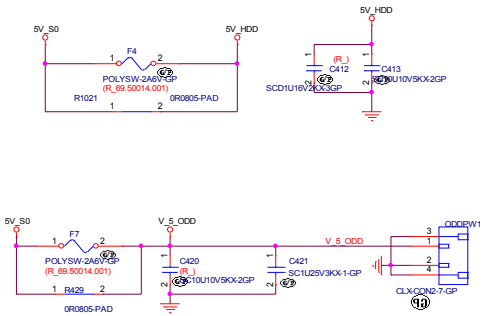
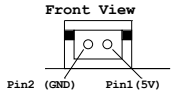
SSID = SATA

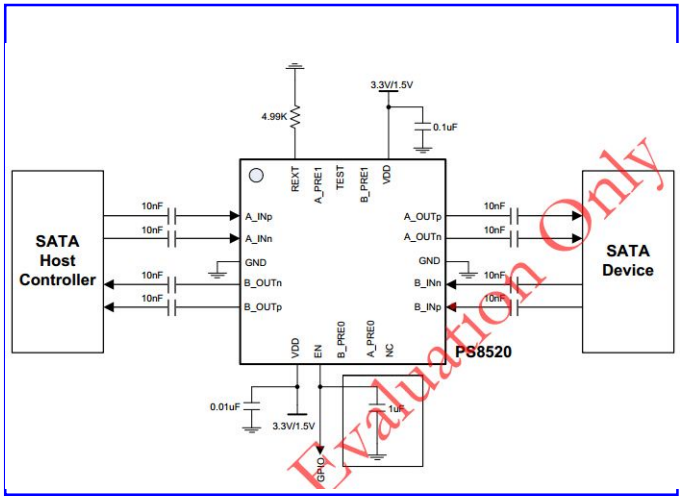
SATA HDD Connector

Layout: Put them together

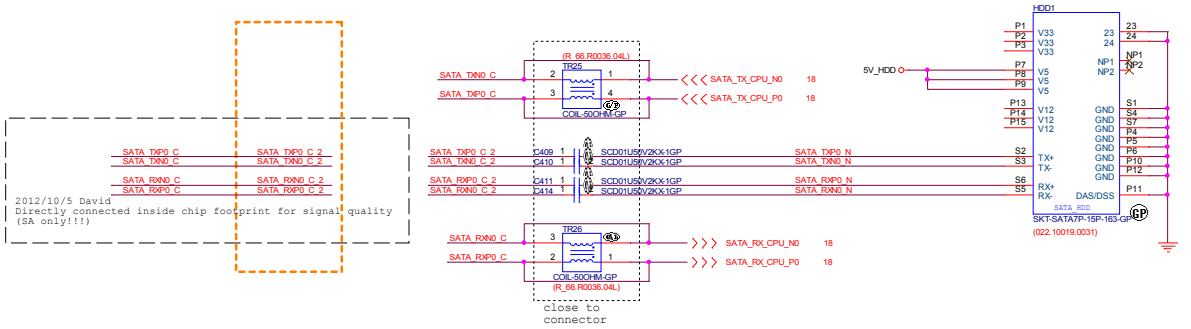


Front View

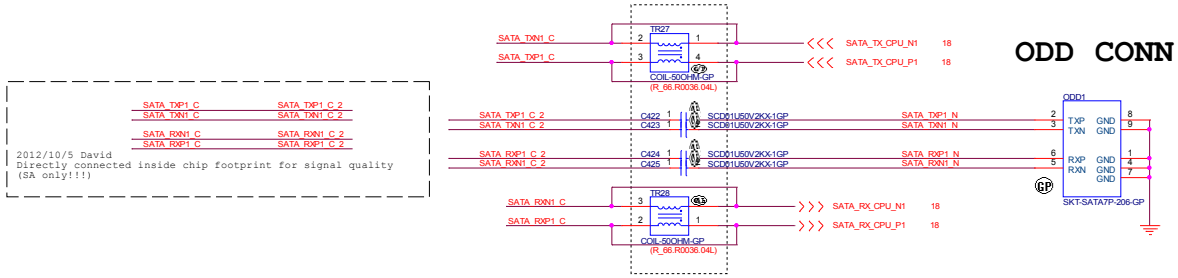


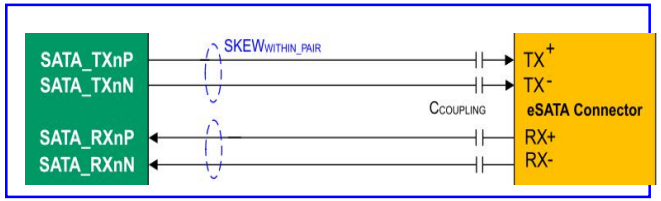


HDD CONN



ODD CONN





wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDD/ODD

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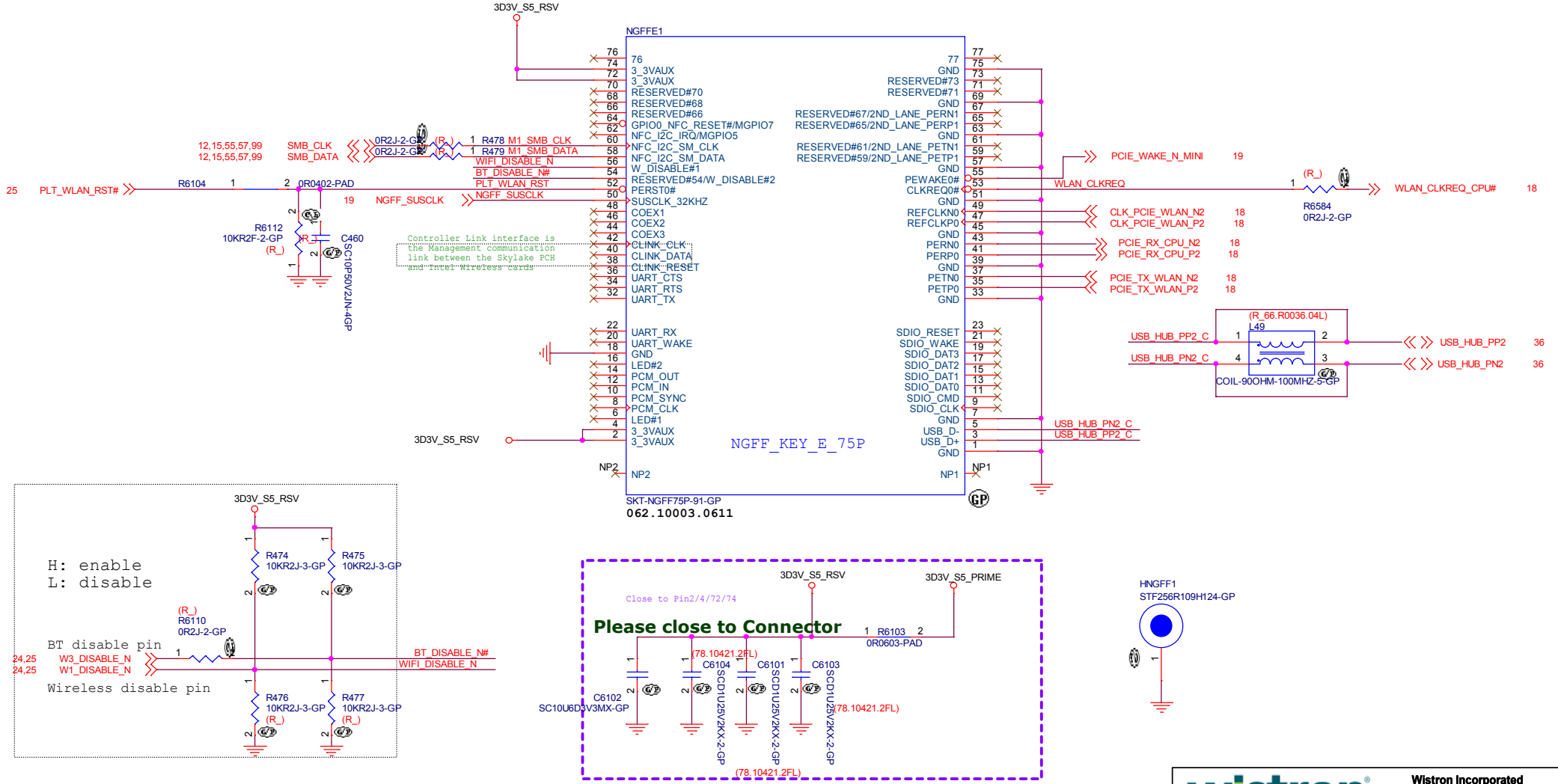
M.2 2230 / 1630 Key E Type
(Wireless LAN+BT)



Wistron Incorporated		
21F, 88, Sec.1,Hsin Tai Wu Rd		
Hsichih, Taipei Hsien		
Title: Mini card-WLAN		
Size: B	Document Number: Bolton195i	Rev: -1A
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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Mini card-SSD/TV (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Mini card-NGFF (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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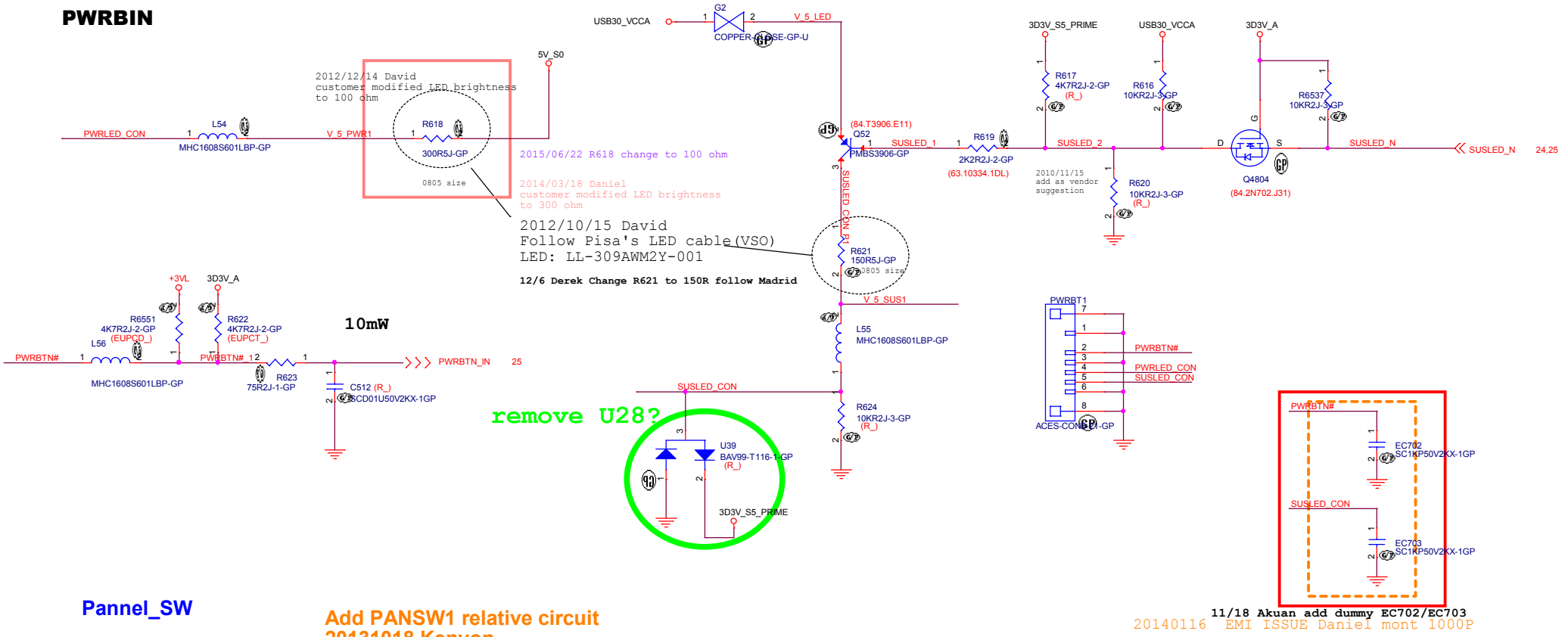
PWRBIN



Pannel_SW

Add PANSW1 relative circuit
20131018 Kenyon

11/18 Akuan add dummy EC702/EC703

20140116 EMI ISSUE Daniel mont 1000P

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	PWRBIN/Side Key/LED	
Size: Custom	Document Number: Bolton195i	Rev: -1A
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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: IO Board (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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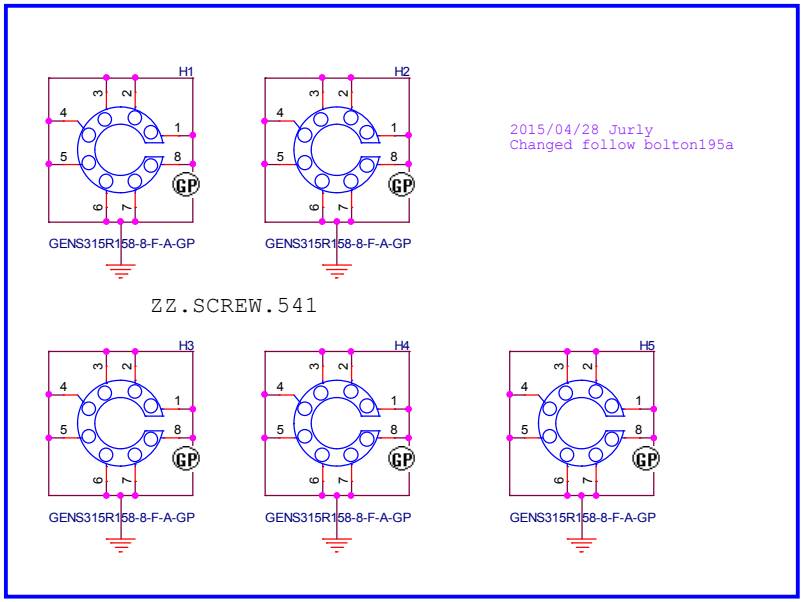
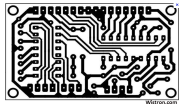


PCB No.: 15047
PCB Version: -1A

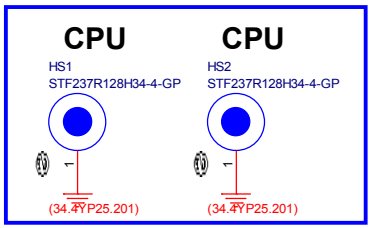
Part Number	Vendor (Gerber Out)
----------	----------

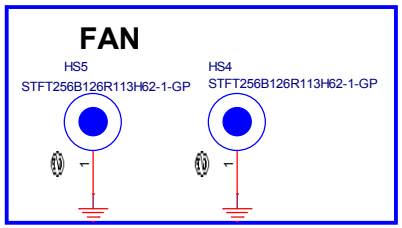
PCB Symbol



PCB1
PCB
(R_348.02203.001A)

2015/04/28 Jurly
Stand-off add follow bolton195a





LABEL

LBL1
LABEL
(40.3KP03.011)

45.41107.011 (一般的紙，70x8mm過完高溫reflow之後會變的偏黃)
45.41101.001
(一般的紙，35x15mm，過完高溫reflow之後會變的偏黃)
40.3KP03.001
(高溫貼紙，35x15mm，過完高溫reflow之後紙還是很白)
45.41115.001 (34 x 13.5mm for aDallas)

LBL2
LABEL
(R_45.41101.011)

2015/02/02 WZS's request
35x15 (40.3KP03.011)
30x15 (40.3BZ24.011)

LBL3
LABEL
(R_45.41107.021)

70x8 (45.41107.021)

(R_40.3KP03.001)

HeatSink Symbol

2014/04/28 Jurly
Removed HeatSink

Brian 10W P/N:	Vendor P/N:
360.02201.0001	60.3ET05.001
360.02201.0011	60.3ET05.011
360.02201.0021	60.3ET05.021

Battery Symbol

BAT1
BATTERY CR2032
(23.20068.001)

23.20068.001 KTS BBBCR2032BX
23.20023.311 MITSUBISHI CR2032 MITSUBISHI
23.22063.001 JHT CR2032 JHT

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Screw Hole

Size	Document Number	Rev
Custom	Bolton195i	-1A

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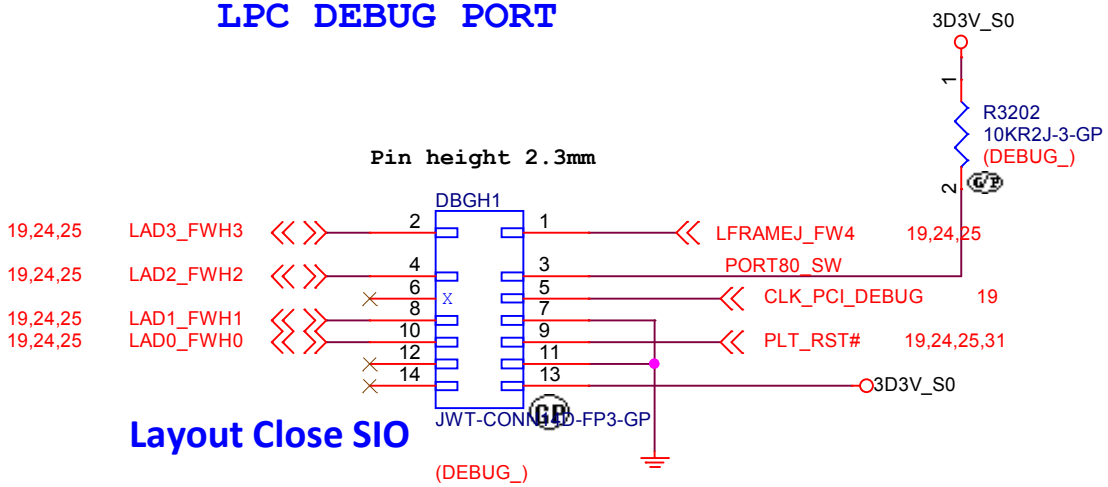
LPC DEBUG PORT



Layout Close SIO

2015/04/21 Jurly
Del the FAN circ uit

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: Debug		
Size: A	Document Number: Bolton195i	Rev: -1A
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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: G Sensor (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 70 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 71 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 72 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 73 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

Date: Thursday, August 27, 2015 | Sheet 74 of 111

(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
GPU (Reserved)

Size	Document Number	Rev
A	Bolton195i	-1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 1/2 (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 3/4 (Reserved)

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 5/6 (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 7/8 (Reserved)

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU CORE (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU power (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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(Reserved)

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
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Title: GPU Switch (Reserved)

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Title
GPU Switch (Reserved)

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A	Bolton195i	-1A

Date: Thursday, August 27, 2015 Sheet 88 of 111

(Reserved)

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Title: GPU others (Reserved)

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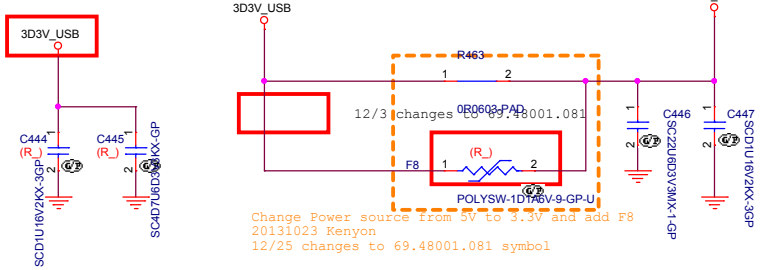
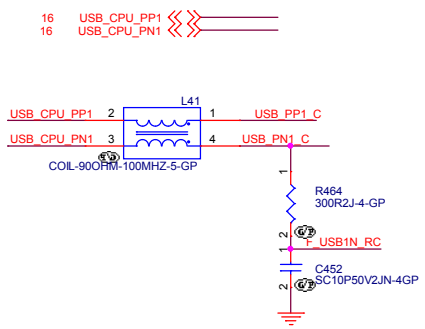
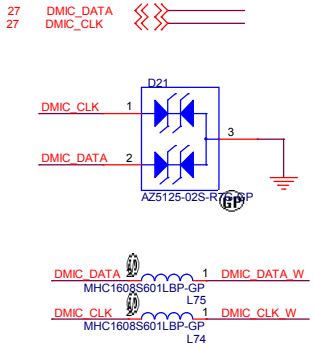
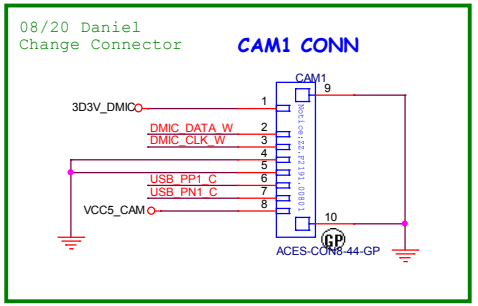
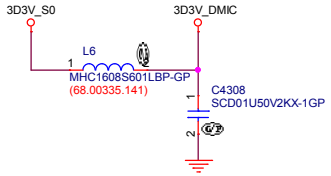
USB Port1 -> WEB CAM



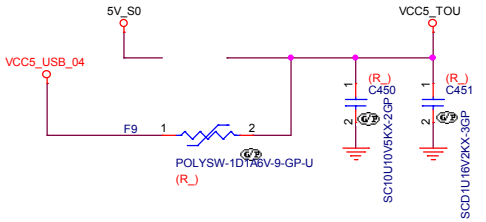


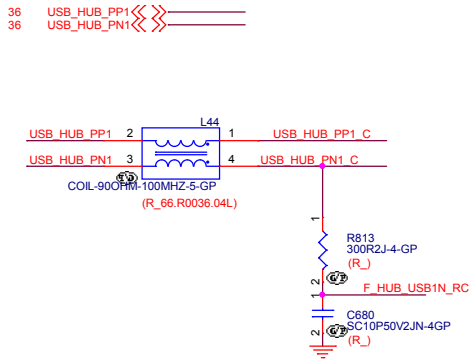


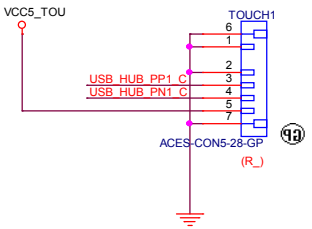




USB HUB PORT1 -> TOUCH







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Title: Camera/Touch/DMIC (Reserved

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Title: TPM/Serial (Reserved)

Size: A | Document Number: Bolton195i | Rev: -1A

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Title: PS2/Parallel

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PCIEx16 Power Estimation for 75W Card
12V_S0 @ 5.5A
3D3V_S0 @ 3A
3D3V_S5 @ 0.375A

2015/4/22 Jurly
Del PCIEX16

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Title: Express Card(Reserve)

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Title: Smart Card (Reserved)

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(Reserved)

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Title: Scalar (Reserved)		
Size: A	Document Number: Bolton195i	Rev: -1A
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(Reserved)

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Title: MCU (Reserved)

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(Reserved)

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Title: Intel LAN (Reserved)

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Title: LAN Switch (Reserved)

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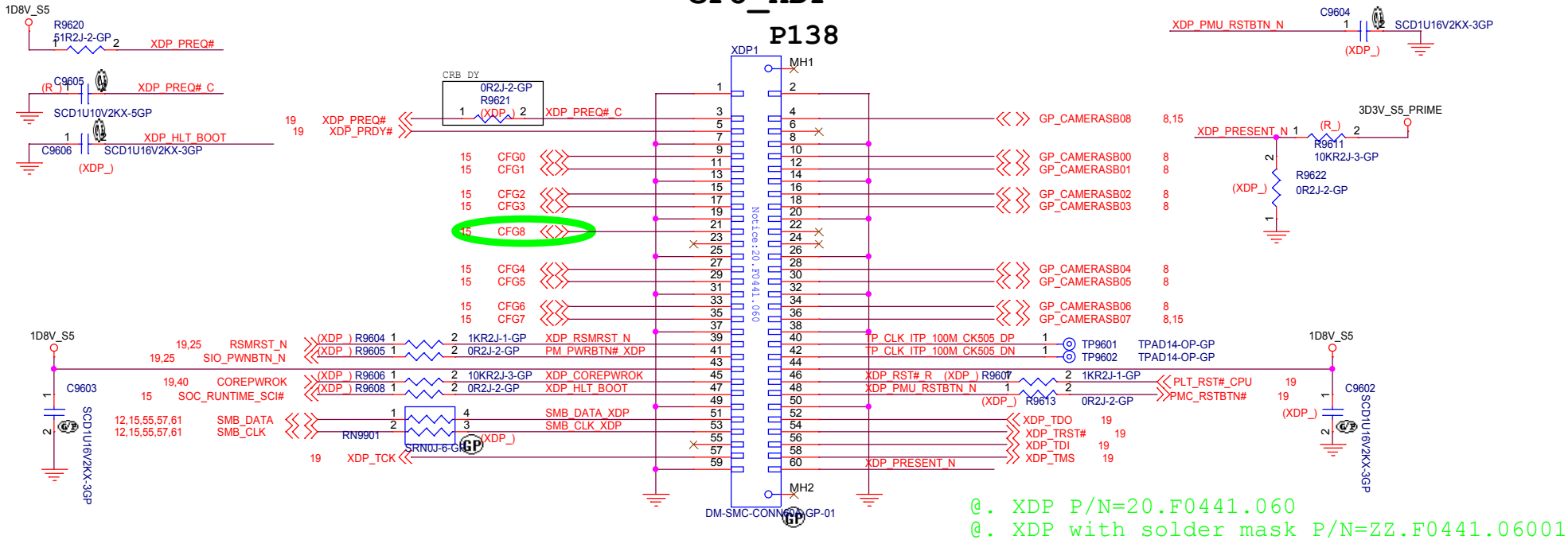
SSID = CPU_XDP

CPU_XDP

P138



@. XDP P/N=20.F0441.060
@. XDP with solder mask P/N=ZZ.F0441.06001

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Title: XDP/ITP		
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Project Name: Bolton195i (4 Layer)
Project Code: 3PD01Z010001
PCB Number : 15047-SA

CPU

SA:
KC.30501.DSC
KC.31501.DSC
KC.37001.DSP

On Board Header/CONN

CONN	Default	DESCRIPTION
CMOS1		CMOS CLEAR BUTTON
TXE1	1-2	TXE header 1*3 PIN
AUDS1		Audio Combo Jack
FANC1		CPU FAN CONN 4 pin
XDP1		XDP CONN (CPU Debug)
USB2S1		Front USB 2.0
USB2S2		Front USB 2.0
USB3S1		Front USB 3.0
DBGH1		Debug Port 2x7
SPK1		CONN 1*4PIN
DCIN1		ADP POWER
BTT1		Battery Holder
PWRBT1		CONN 1*6PIN

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1501	CPU	19.2M	+/-10ppm CL:7P	C1501=4.7pF C1502=4.7pF
X3502	CPU	32.768K	+/-20ppm CL:7P	C7538=4.7pF C7540=4.7pF
X3	LAN	25M	+/-20ppm CL:12P	C2116=18pF C2117=18pF
X3501	HUB	12M	+/-30ppm CL:12P	C4603=18pF C4604=18pF
OSC1	SIO	48M		

BOM Configuration

R - unmount
XDP - XDP function
HUB - USB2.0 hub
NOHUB - no hub and colay to BT
O - adapter OCP
NOOCP - no OCP
SIO - ITE8772
EUPCT - EUP Control
EUPCD - EUP cost down
SDSOC - SD form SOC directiy
SD - SD from USB down-stream
DEBUG - debug

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Title: Table of Content/BOM config
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IC Pin Name	Power Well	Default	Default State	Usage	BIOS Programming				
					S0	S1	S3	S4	S5
GENINT1_L/GPIO32	VDD_33	General Input	Input, 8.2K PU	ID0	GPI	GPI	GPI	GPI	GPI
GENINT2_L/GPIO33	VDD_33	General Input	Input, 8.2K PU	ID1	GPI	GPI	GPI	GPI	GPI
SCL0/GPIO43	VDD_33	null	Input,Tristate	SMB0_CLK	Native	Native	Native	Native	Native
SD_LED/GPIO45	VDD_33	null	Output HIGH	no use	N/A	N/A	N/A	N/A	N/A
SDA0/GPIO47	VDD_33	null	Input, Tri-State	SMB0_DAT A	Native	Native	Native	Native	Native
SERIRQ/GPIO48	VDD_33	null	Input, 8.2K PU	SERIRQ_N	Native	Native	Native	Native	Native
GPIO49	VDD_33	null	Input, 8.2K PU	R1SER_ID_0	GPI	GPI	GPI	GPI	GPI
GPIO50	VDD_33	null	Input, 8.2K PU	R1SER_ID_1	GPI	GPI	GPI	GPI	GPI
GPIO51	VDD_33	null	Input, 8.2K PU	~~FCH_APU_SIC_L~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A
FANOUT0/GPIO52	VDD_33	null	Input, 8.2K PU	SIO_GP41	GPO	~~GPI~~ GPO	~~GPI~~ GPO	~~GPI~~ GPO	~~GPI~~ GPO
DEVSLP[0]/GPIO55	VDD_33	null	Input, 8.2K PU	~~FCH_APU_SID_L~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A	~~GPO~~ N/A
FANIN0/GPIO56	VDD_33	null	Input, 8.2K PU	SIO_GP45	GPO	GPO	GPO	GPO	GPO
GPIO57	VDD_33	null	Input, 8.2K PU	X16_PRSNT	GPO	GPO	GPO	GPO	GPO
GPIO58	VDD_33	null	Input, 8.2K PU	PCIEX16_DET0	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI
DEVSLP[1]/GPIO59	VDD_33	null	Input, 8.2K PU	PCIEX16_DET1	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI	~~GPO~~ GPI
CLK_REQ0_L/ SATA_IS0_L/ SATA_ZP0_L/GPIO60	VDD_33	null	Input, 8.2K PU	BLANCLK_REQ_N_1	Native	Native	Native	Native	Native
CLK_REQ1_L/GPIO61	VDD_33	null	Input, 8.2K PU	IO_SMI_N	GPO	GPO	GPO	GPO	GPO
CLK_REQ2_L/GPIO62	VDD_33	null	Input, 8.2K PU	Test Point	N/A	N/A	N/A	N/A	N/A
CLK_REQ3_L/ SATA_IS1_L/ SATA_ZP1_L/GPIO63	VDD_33	null	Input, 8.2K PU	ILIM_SEL	~~GPI~~ GPO	~~GPI~~ GPO	~~GPI~~ GPO	~~GPI~~ GPO	~~GPI~~ GPO
GPIO64	VDD_33	null	Input, 8.2K PU	FP_AUDIO_PRESENCE_N	GPI	GPI	GPI	GPI	GPI
CLK_REQG_L/GPIO65/ OSCIN	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SPKR/GPIO66	VDD_33	null	Input,PU	SPKR	Native	Native	Native	Native	Native
SATA_ACT_L/GPIO67	VDD_33	null	Input, 8.2K PU	FCH_SATA_LED_N	Native	Native	Native	Native	Native
GPIO68	VDD_33	null	Input, 8.2K PU	AUD_DET	GPO	GPO	GPO	GPO	GPO
GPIO69	VDD_33	null	Input, 8.2K PU	~~FP_AUDIO_PRESENCE_N~~	~~GPI~~	~~GPI~~	~~GPI~~	~~GPI~~	~~GPI~~
GPIO70	VDD_33	null	Tri-State	no use	N/A	N/A	N/A	N/A	N/A
GPIO71	VDD_33	null	Tri-State	APU_PROCHOT#_R	GPO	GPO	GPO	GPO	GPO
SD_CLK/SCLK_2/ GPIO73	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CMD/GPIO74	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CD/GPIO75	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_WP/GPIO76	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA0/ SDATI_2/ GPIO77	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA1/ SDATO_2/ GPIO78	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA2/GPIO79	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA3/GPIO80	VDD_33	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SPI_WP_L/GPIO161	VDD_33_ALW	null or SPI (strap dependent)	Input,PU	~~no use~~ ROM_RST#	~~GPO~~ Native	~~GPO~~ Native	~~GPO~~ Native	~~GPO~~ Native	~~GPO~~ Native
SPI_CLK/GPIO162	VDD_34_ALW	null or SPI (strap dependent)	Input, 10K PD	SPI_CLK	Native	Native	Native	Native	Native
SPI_DO/GPIO163	VDD_35_ALW	null or SPI (strap dependent)	Input, 10K PD	SPI_DATAOUT	Native	Native	Native	Native	Native
SPI_DI/GPIO164	VDD_36_ALW	null or SPI (strap dependent)	Input, 10K PD	SPI_DATAIN	Native	Native	Native	Native	Native
SPI_CS1_L/GPIO165	VDD_37_ALW	null or SPI (strap dependent)	Input, 10K PU	~~SPI_CS1#~~ SPI_CS0_N	Native	Native	Native	Native	Native
SPI_CS2_L/GPIO166	VDD_38_ALW	null or SPI (strap dependent)	Input, 10K PU	Test Point	N/A	N/A	N/A	N/A	N/A
AZ_SDIN0/GPIO167	VDD_33_S/VDDIO_AZ_ALW	AZ	Input, 50K PD	AZ_SDIN0	Native	Native	Native	Native	Native
AZ_SDIN1/GPIO168	VDD_33_S/VDDIO_AZ_ALW	AZ	Input, 50K PD	AZ_SDIN1	Native	Native	Native	Native	Native
AZ_SDIN2/GPIO169	VDD_33_S/VDDIO_AZ_ALW	AZ	Input, 50K PD	~~no use~~ AZ_SDIN2	Native	Native	Native	Native	Native
AZ_SDIN3/GPIO170	VDD_33_S/VDDIO_AZ_ALW	AZ	Input, 50K PD	~~no use~~ AZ_SDIN3	Native	Native	Native	Native	Native
GPIO174	VDD_33_ALW	null	Input	no use	N/A	N/A	N/A	N/A	N/A
IR_LED_L/LLB_L/ GPIO184	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
SCL1/GPIO227	VDD_33_ALW	null	Input, Tri-State	SMB1_CLK	Native	Native	Native	Native	Native
SDA1/GPIO228	VDD_33_ALW	null	Input, Tri-State	SMB1_DAT A	Native	Native	Native	Native	Native
GA20IN/GEVENT0#	VDD_33	null	Input, 8.2K PU	KA20GAT E	Native	Native	Native	Native	Native
GEVENT2#	VDD_33_ALW	null	Input, 10K PU	SPI_SW	~~APU_T HERM T RIP_N1~~ GPI	GPI	GPI	GPI	GPI
LPC_PME#/ GEVENT3#	VDD_33_ALW	null	Input, 10K PU	PM E#_M	Native	Native	Native	Native	Native
GEVENT4#	VDD_33_ALW	null	Input, 10K PU	T HERM AL_SHUT #	GPI	GPI	GPI	GPI	GPI
LPC_PD#/ GEVENT5#	VDD_33_ALW	null	Input, 10K PU	LPC_PD_N（Test point）	N/A	N/A	N/A	N/A	N/A
IR_TX1/ GEVENT6#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT7#	VDD_33_ALW	~~DDR3_RST#~~ null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
WAKE#/ GEVENT8#	VDD_33_ALW	null	Input, 10K PU	PCI_WAKE_N	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	null	Input, 10K PU	~~SST_HOLD_L~~ SST_HOLD_L_R	Native	Native	Native	Native	Native
GEVENT10#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT11#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
USB_OC0#/ SPI_TPM_CS#/ TRST#/ GEVENT12#	VDD_33_ALW	~~GEVEN T12#~~ null	Input, 10K PU	USB_OC_01	Native	Native	Native	Native	Native
USB_OC1#/TDI/ GEVENT13#	VDD_33_ALW	null	Input, 10K PU	~~USB_OC_23~~ USB_OC_23	Native	Native	Native	Native	Native
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	null	Input, 10K PU	~~USB_OC_23~~ USB_OC_45	Native	Native	Native	Native	Native
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	null	Input, 10K PU	~~USB_OC_23~~ USB_OC_67	Native	Native	Native	Native	Native
AC_PRES/IR_RX0/ GEVENT16#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT17#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
CLKRU GEVENT18#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
SYS_RESET#/ GEVENT19#	VDD_33_ALW	null	Input, 10K PU	FP_RST _N	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native	~~GPI~~ Native
IR_RX1/ GEVENT20#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
IR_TX0/ GEVENT21#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
RI#/GEVENT22#	VDD_33_ALW	null	Input, 10K PU	no use	N/A	N/A	N/A	N/A	N/A
LPC_SMI#/ GEVENT23#	VDD_33_ALW	null	Input, 8.2K PU	no use	N/A	N/A	N/A	N/A	N/A

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Title: GPIO table

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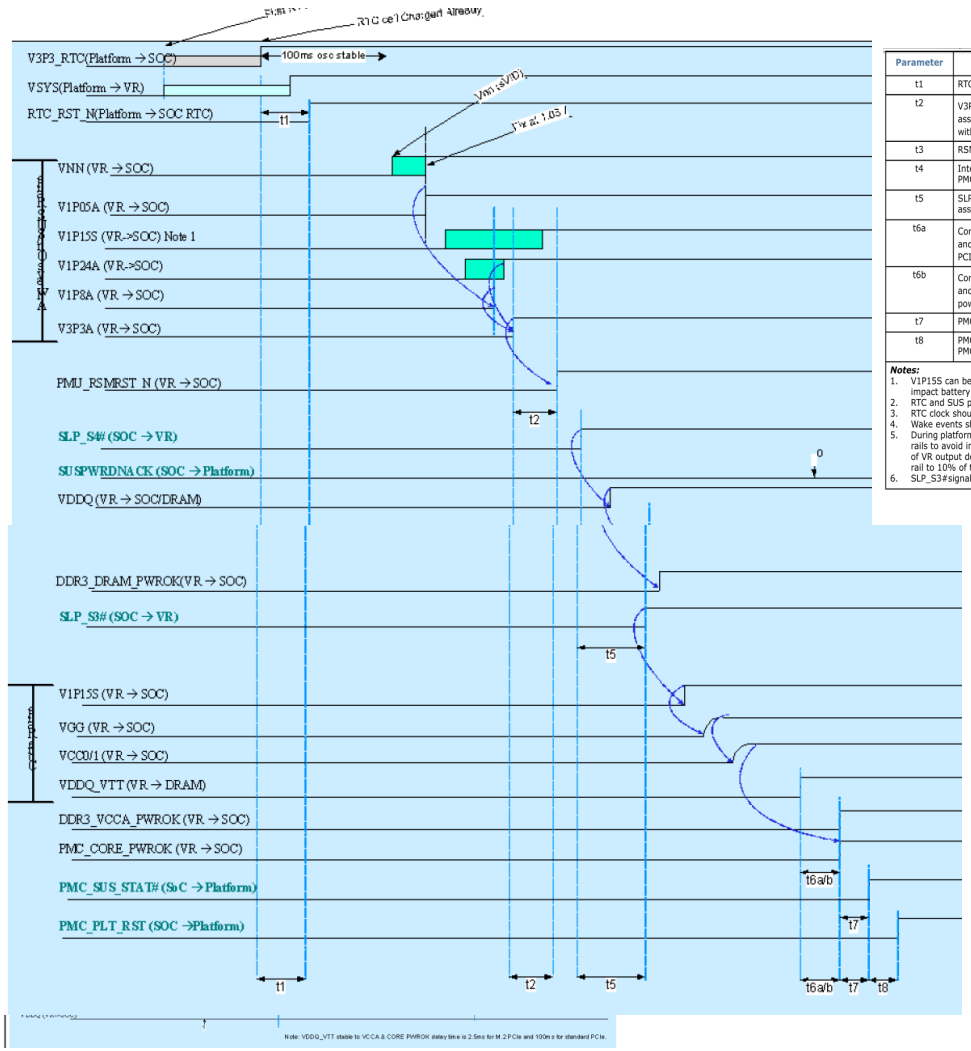
Braswell Power-up Sequencing

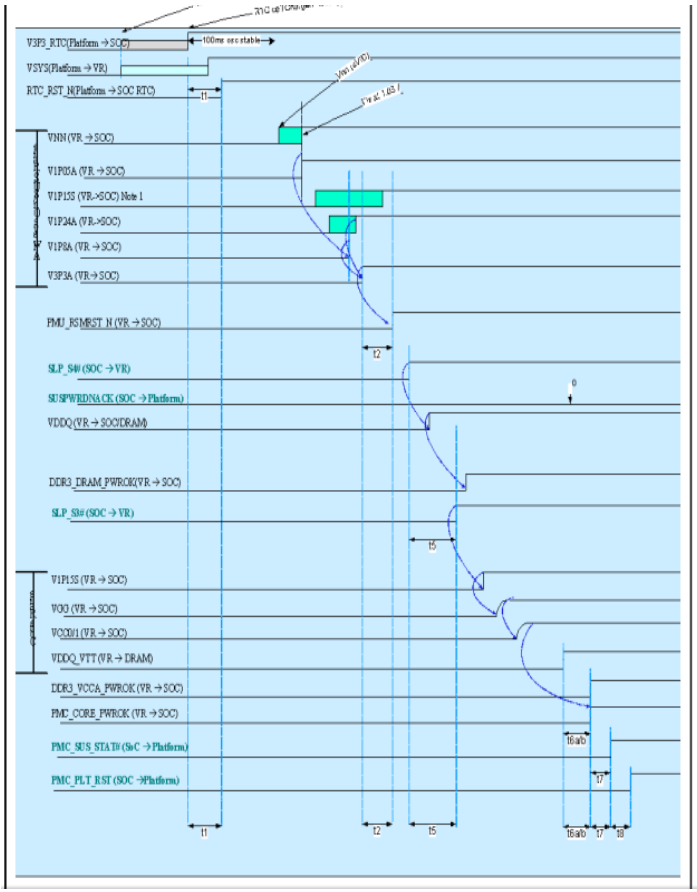


Parameter	Description	Minimum	Maximum	Units
t1	RTC_VCC to RTC_RST_N de-assertion	9	-	ms
t2	V3P3A (SUS Rails) valid to RSMRST_N de-assertion (t1 still applies in applications without RTC battery)	10		µS
t3	RSMRST_N to Internal RTC Clock stable2	95		ms
t4	Internal RTC Clock stable to PMC_SUSCLK[0] toggling	5		ms
t5	SLP_S4# de-assertion to SLP_S3# de-assertion	26		µs
t6a	Core well stable to DDR3_VCCA_PWROK and PMC_CORE_PWROK assertion (NO PCIe* devices)	10		ms
t6b	Core well stable to DDR3_VCCA_PWROK and PMC_CORE_PWROK assertion (for power rails needed by PCIe* devices)	99		ms
t7	PMC_CORE_PWROK to PMC_SUS_STAT#	1		ms
t8	PMC_SUS_STAT# de-assertion to PMC_PLTRST_N de-assertion	60		us

Notes:

1. V1P15S can be a "always" rail and be turned on sooner in the platform sequence but this will impact battery life as it will be ON in Sx states.
2. RTC and SUS power rails may come up at the same time if no RTC battery is used.
3. RTC clock should be oscillating, but may not be at 32.768 KHz yet.
4. Wake events shown in figure are optional and depending on platform configuration
5. During platform power-up, design should ensure that there is proper power rail sequences between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output de-coupling. Ensure that there is Minimum time = 10 µs from 90% level of previous rail to 10% of the preceding rail.
6. SLP_S3#signal should be used as platform does not support S0iX.

Braswell Power-Down Sequencing



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Title: Power Sequence				
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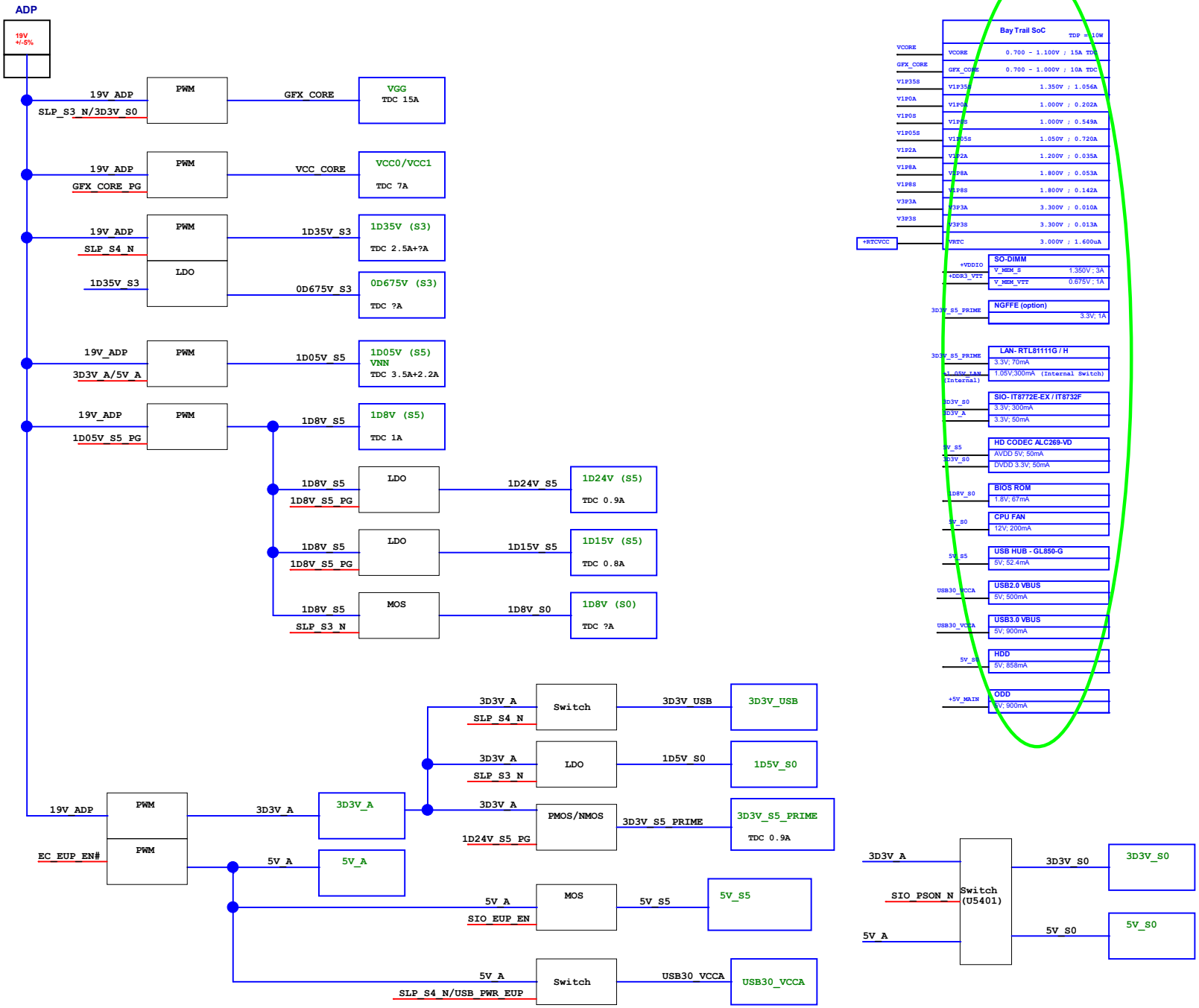

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Title: Power Block Diagram

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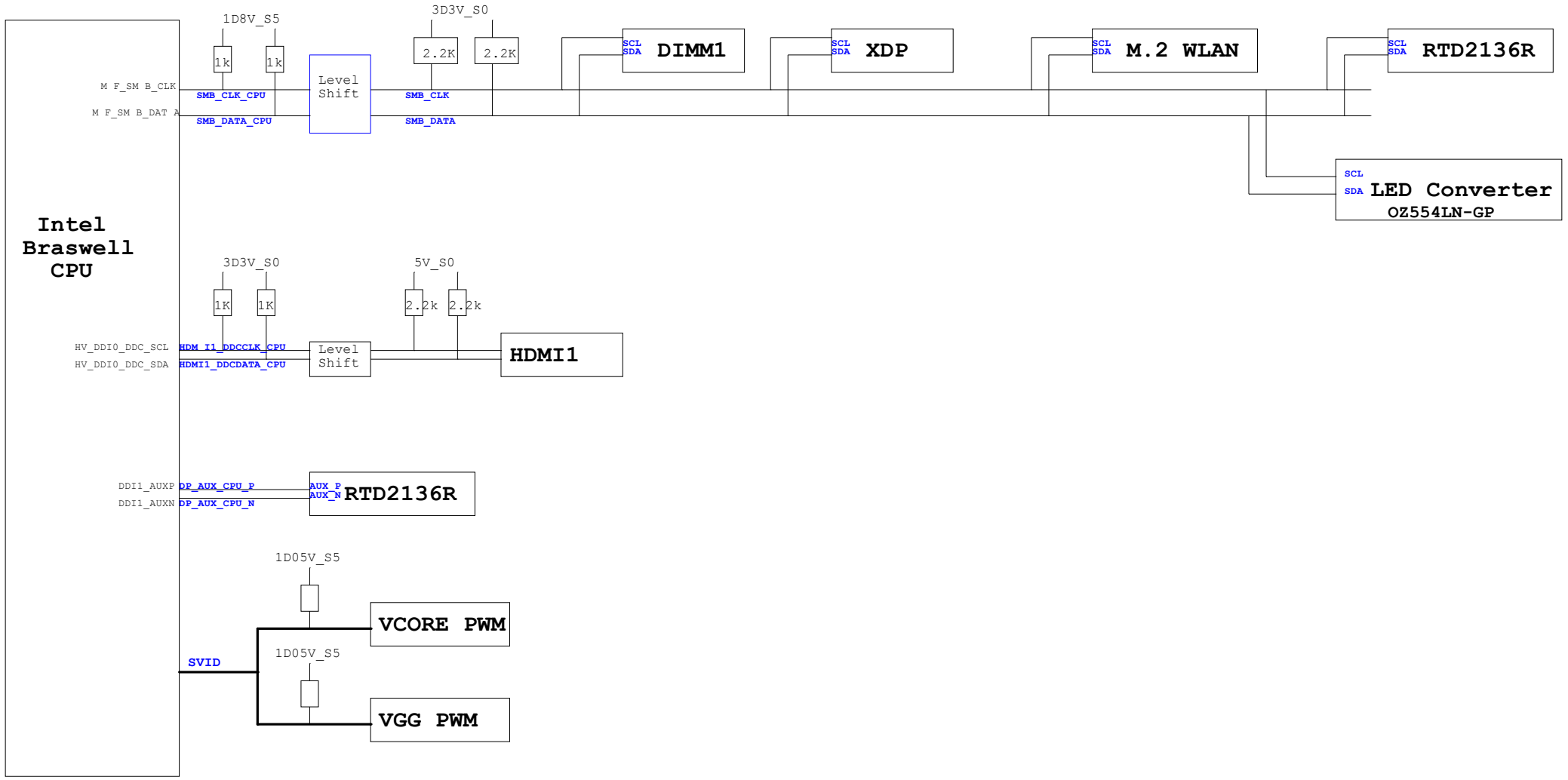
SMBUS Block Diagram



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Title: SMBUS Block Diagram		
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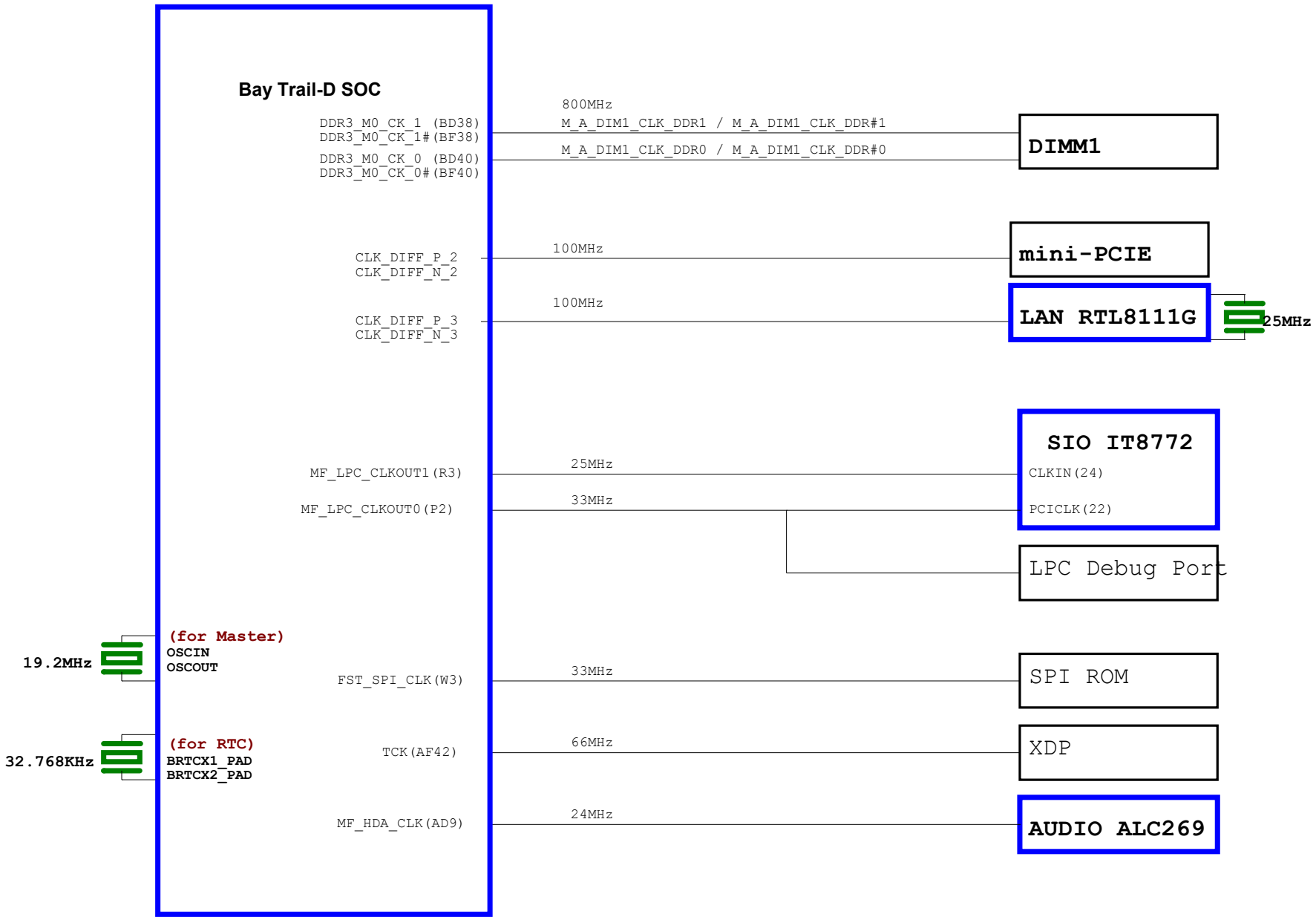

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Title: Clock MAP

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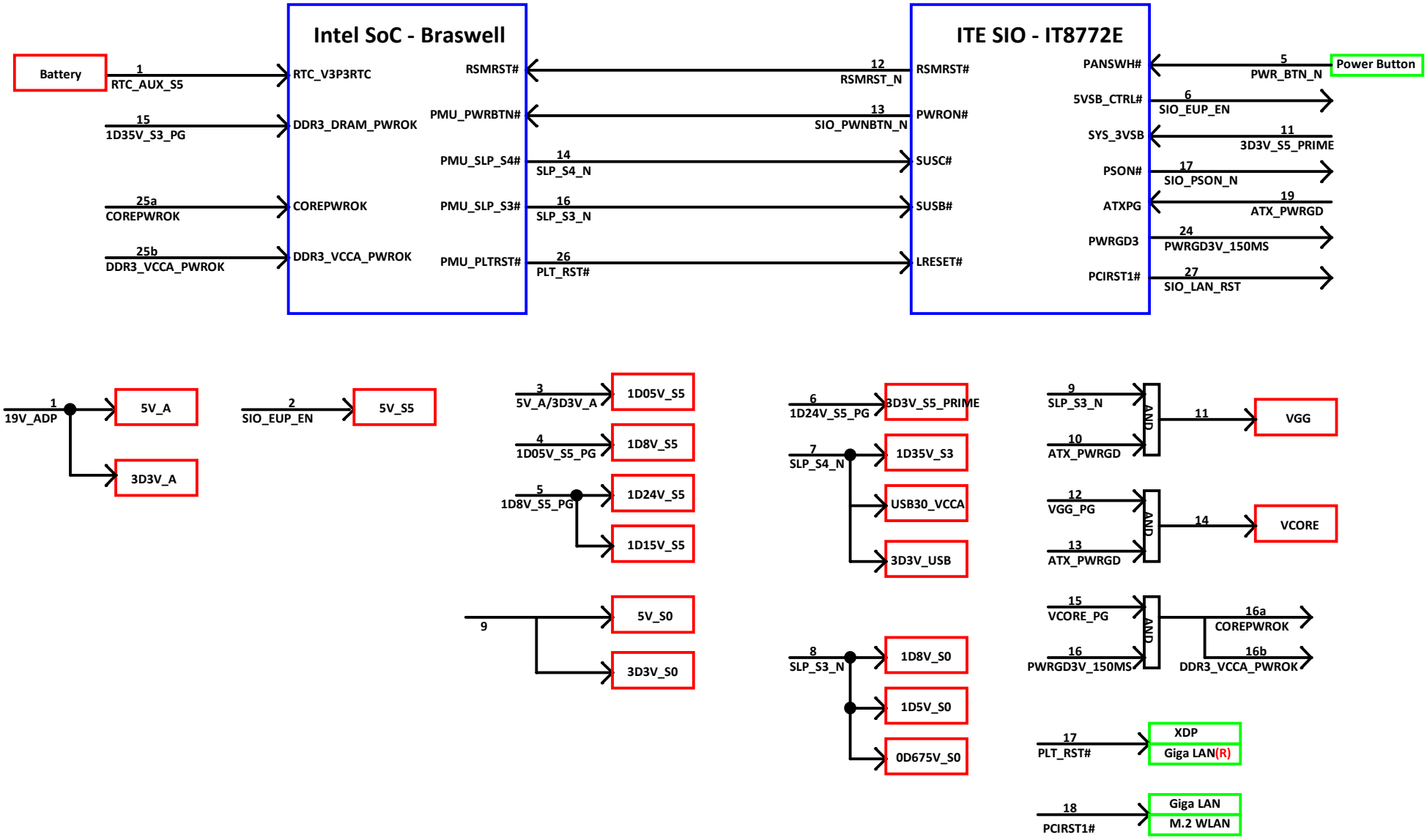

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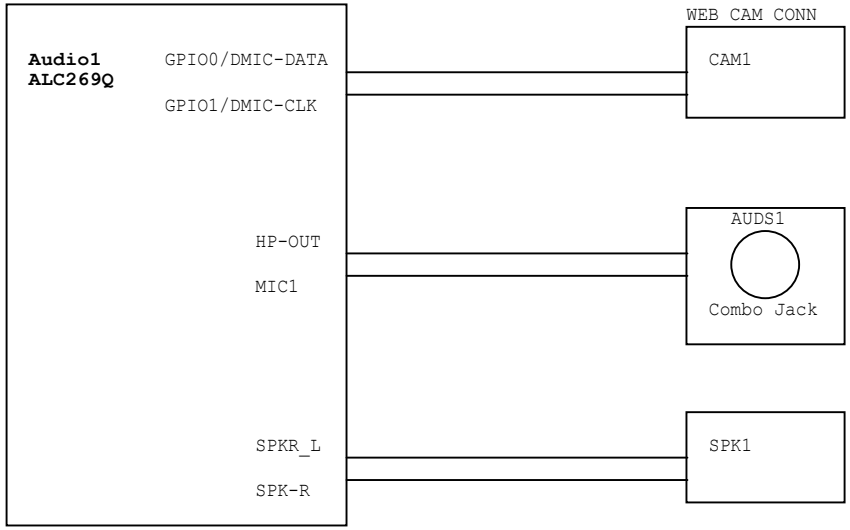

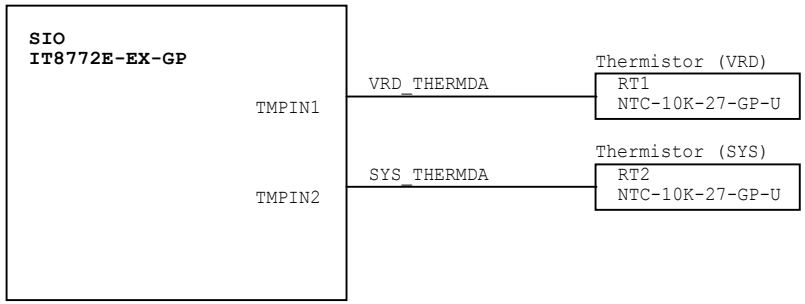

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