PCB Number: 14088-1
Project Code : 3PD039010001
Project Name : TAHOE MT CBB

PCB BOARD SIZE
4 Layers 244mm X 266mm

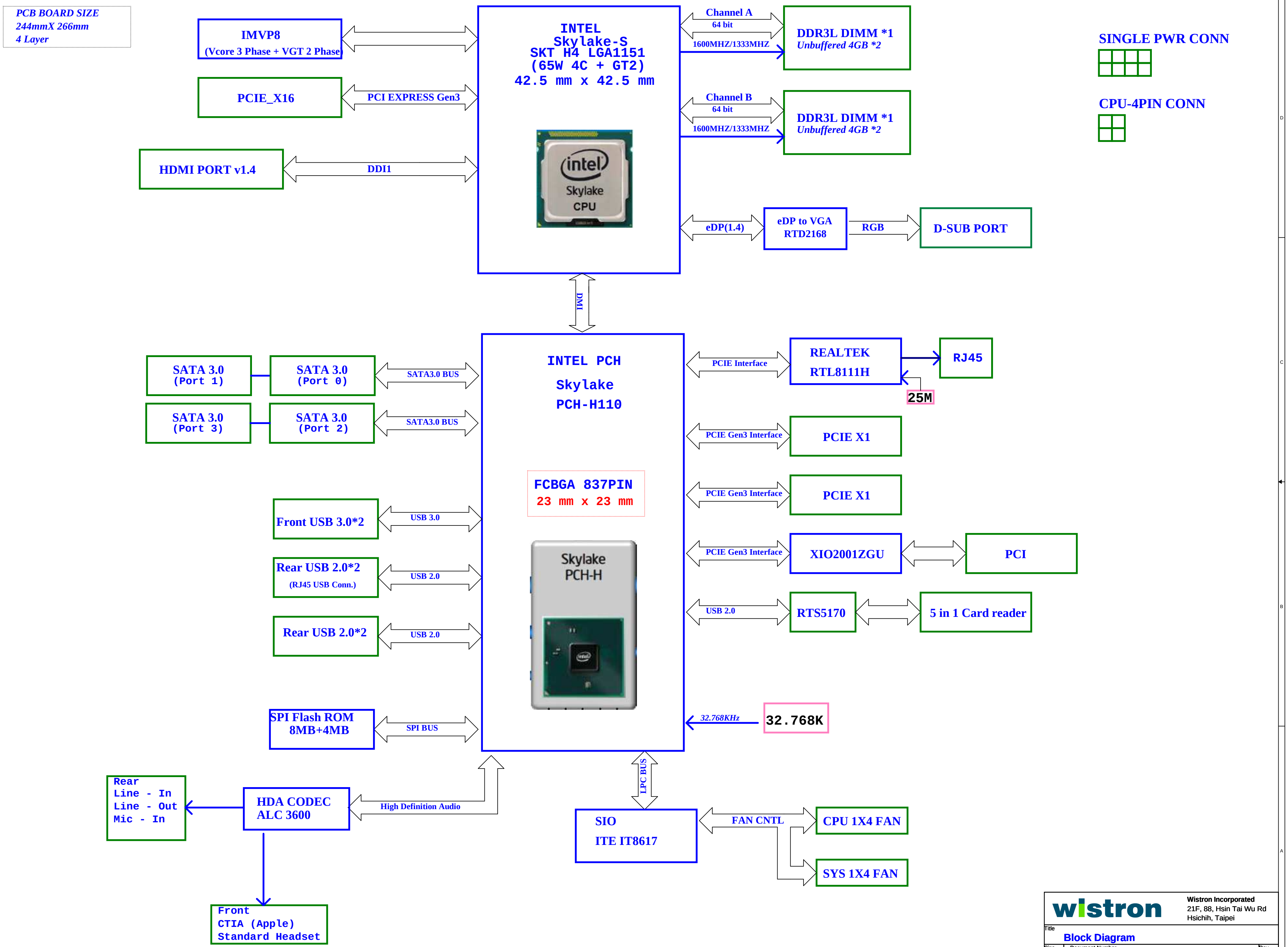
Jumper SETTING		
CMCLR1	1-2 Short	With Jumper to Clear CMOS
MECLR1	2-3 Short	With Jumper to Disable ME
DB1	PD 1K	PD 1K to GND for Debug Mode, All power on
PWCLR1	1-2 Short	Without Jumper to Clear PassWord

BOM Configuration

(R_):Unmount
(X_):Debug
(A_):Tahoe MT
(B_):Tahoe CBB

Power sates

	Name	G3	DSW	S5	S4	S3	S0
+12V	V_12P0_A		O	O	O	O	O
	+12V V_12V_CPU_S0						O
	12V_DUAL		O	O	O	O	O
-12V	-12V						O
5V	5V_S0 5V_AUD_S0						O
	5V_SB 5VDUAL_USB_F 5VDUAL_USB_R USBVCC9 USBVCC12 USBVCC37 USBVCC45 USBVCC1213 KEYBRD_PWR1			O	O	O	O
	5V_S5 5V_AUD_S5 USBVCC68 5V_USB_CHAR		O	O	O	O	O
3.3V	3P3V_S0 3P3V_AUD_S0 3P3V_M2VAUX						O
	3P3V_SB 3P3V_SPI 3P3V_PCIVAUX +DVDDIO_AUDIO +VCCPGPPD			O	O	O	O
	3P3V_S5 3P3V_LAN		O	O	O	O	O
3.0V	3P0V_BAT_VREG VBAT1 VBAT2	O	O	O	O	O	O
1.5V	1P5V_AUD_S0 1P5V_S0_PCI						O
1.35V	+VCCPLL_OC						O
DIMM	V_SM					O	O
	V_SM_VTT						O
PCH	V1P0_PCH_SB +V1P0A_VCCAPLL +V1P0A_VCCF24_1P0 +V1P0A_VCCAMPHYPLL V_CPU_ST_PLL			O	O	O	O
CPU	V_CPU_CORE V_CPU_GT V_CPU_IO V_CPU_SA +VCCFUSEPRG						O



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Title: Block Diagram

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 2 of 107

DDR DATA

(11) M_DATA_A[0..63]
(13) M_DATA_B[0..63]

(11) M_DQS_A_DP[0..7]
(11) M_DQS_A_DN[0..7]

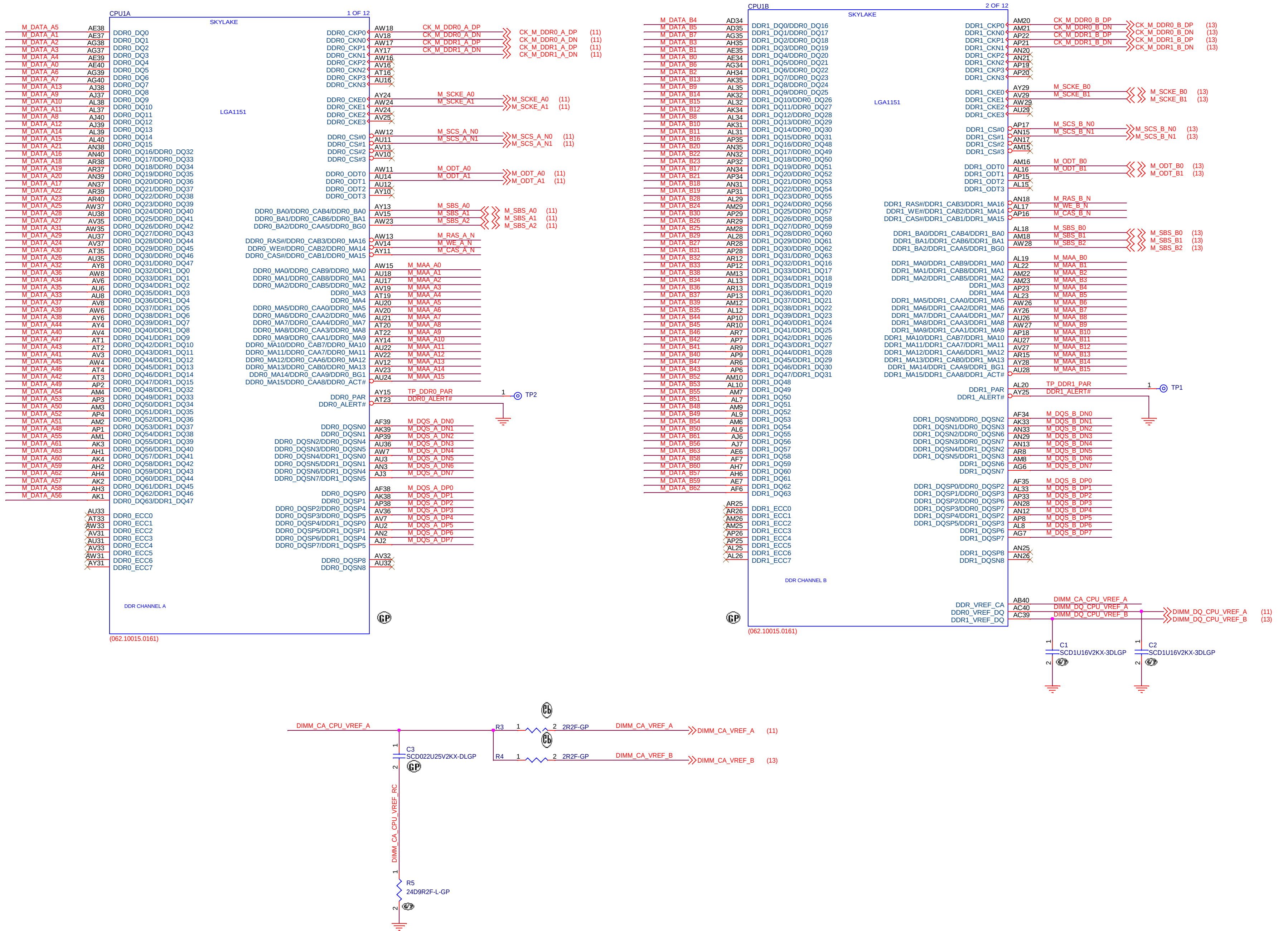
(13) M_DQS_B_DP[0..7]
(13) M_DQS_B_DN[0..7]

DDR CMD/ADD

(11) M_MAA_A[0..15]
(13) M_MAA_B[0..15]

(11) M_WE_A_N
(11) M_CAS_A_N
(11) M_RAS_A_N

(13) M_WE_B_N
(13) M_CAS_B_N
(13) M_RAS_B_N



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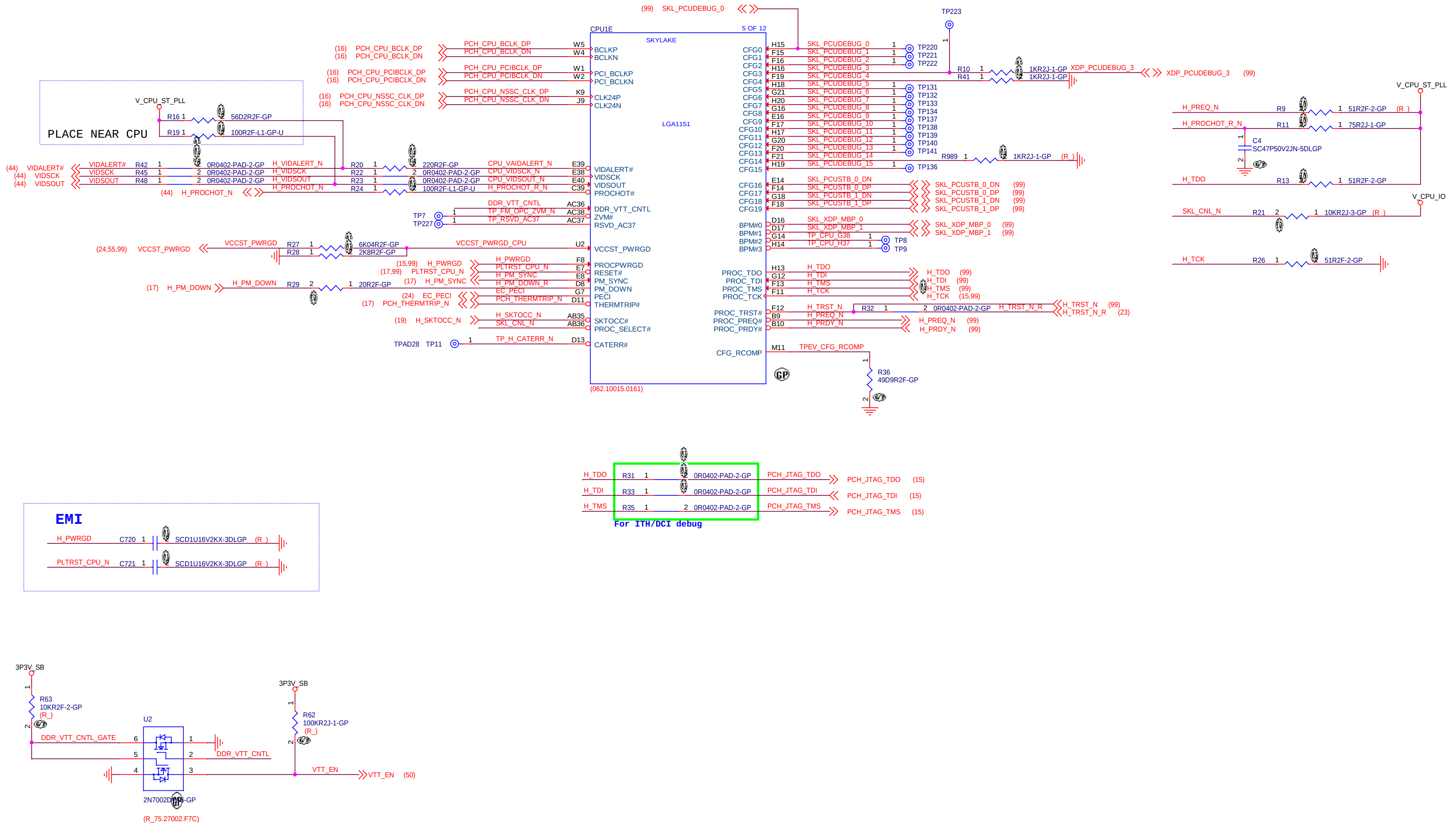
Title	CPU_(DDRA_DDRB)		
Size C	Document Number TAHOE_MT		Rev -1
Date: Thursday, July 02, 2015	Sheet 3 of 107		

VIDSCK
VIDSOUT
VIDALERT#
Need to add Pull UP on both CPU and VR side.

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	



CPU1C 3 OF 12

SKYLAKE

LGA1151

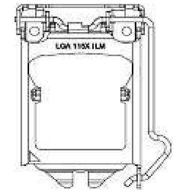
Net (page)	Pin	CPU pin	CPU pin	Pin	Net (page)
(93) EXP_A_RX_DP0	B8	PEG_RXP0	PEG_TXP0	A5	EXP_A_TX_DP0 (93)
(93) EXP_A_RX_DN0	B7	PEG_RXN0	PEG_TXN0	A6	EXP_A_TX_DN0 (93)
(93) EXP_A_RX_DP1	C7	PEG_RXP1	PEG_TXP1	B4	EXP_A_TX_DP1 (93)
(93) EXP_A_RX_DN1	C6	PEG_RXN1	PEG_TXN1	B5	EXP_A_TX_DN1 (93)
(93) EXP_A_RX_DP2	D6	PEG_RXP2	PEG_TXP2	C3	EXP_A_TX_DP2 (93)
(93) EXP_A_RX_DN2	D5	PEG_RXN2	PEG_TXN2	C4	EXP_A_TX_DN2 (93)
(93) EXP_A_RX_DP3	E5	PEG_RXP3	PEG_TXP3	D2	EXP_A_TX_DP3 (93)
(93) EXP_A_RX_DN3	E4	PEG_RXN3	PEG_TXN3	D3	EXP_A_TX_DN3 (93)
(93) EXP_A_RX_DP4	F6	PEG_RXP4	PEG_TXP4	E1	EXP_A_TX_DP4 (93)
(93) EXP_A_RX_DN4	F5	PEG_RXN4	PEG_TXN4	E2	EXP_A_TX_DN4 (93)
(93) EXP_A_RX_DP5	G5	PEG_RXP5	PEG_TXP5	F2	EXP_A_TX_DP5 (93)
(93) EXP_A_RX_DN5	G4	PEG_RXN5	PEG_TXN5	F3	EXP_A_TX_DN5 (93)
(93) EXP_A_RX_DP6	H6	PEG_RXP6	PEG_TXP6	G1	EXP_A_TX_DP6 (93)
(93) EXP_A_RX_DN6	H5	PEG_RXN6	PEG_TXN6	G2	EXP_A_TX_DN6 (93)
(93) EXP_A_RX_DP7	J5	PEG_RXP7	PEG_TXP7	H2	EXP_A_TX_DP7 (93)
(93) EXP_A_RX_DN7	J4	PEG_RXN7	PEG_TXN7	H3	EXP_A_TX_DN7 (93)
(93) EXP_A_RX_DP8	K6	PEG_RXP8	PEG_TXP8	J1	EXP_A_TX_DP8 (93)
(93) EXP_A_RX_DN8	K5	PEG_RXN8	PEG_TXN8	J2	EXP_A_TX_DN8 (93)
(93) EXP_A_RX_DP9	L5	PEG_RXP9	PEG_TXP9	K2	EXP_A_TX_DP9 (93)
(93) EXP_A_RX_DN9	L4	PEG_RXN9	PEG_TXN9	K3	EXP_A_TX_DN9 (93)
(93) EXP_A_RX_DP10	M6	PEG_RXP10	PEG_TXP10	L1	EXP_A_TX_DP10 (93)
(93) EXP_A_RX_DN10	M5	PEG_RXN10	PEG_TXN10	L2	EXP_A_TX_DN10 (93)
(93) EXP_A_RX_DP11	N5	PEG_RXP11	PEG_TXP11	M2	EXP_A_TX_DP11 (93)
(93) EXP_A_RX_DN11	N4	PEG_RXN11	PEG_TXN11	M3	EXP_A_TX_DN11 (93)
(93) EXP_A_RX_DP12	P6	PEG_RXP12	PEG_TXP12	N1	EXP_A_TX_DP12 (93)
(93) EXP_A_RX_DN12	P5	PEG_RXN12	PEG_TXN12	N2	EXP_A_TX_DN12 (93)
(93) EXP_A_RX_DP13	R5	PEG_RXP13	PEG_TXP13	P2	EXP_A_TX_DP13 (93)
(93) EXP_A_RX_DN13	R4	PEG_RXN13	PEG_TXN13	P3	EXP_A_TX_DN13 (93)
(93) EXP_A_RX_DP14	T6	PEG_RXP14	PEG_TXP14	R2	EXP_A_TX_DP14 (93)
(93) EXP_A_RX_DN14	T5	PEG_RXN14	PEG_TXN14	R1	EXP_A_TX_DN14 (93)
(93) EXP_A_RX_DP15	U5	PEG_RXP15	PEG_TXP15	T2	EXP_A_TX_DP15 (93)
(93) EXP_A_RX_DN15	U4	PEG_RXN15	PEG_TXN15	T3	EXP_A_TX_DN15 (93)
V_CPU_IO — R64 1 24D9R2F-L-GP — PEG_COMP	L7	PEG_RCOMP			
(18) DMI_IT_MR_DP0	Y3	DMI_RXP0	DMI_TXP0	AC2	DMI_MT_IR_DP0 (18)
(18) DMI_IT_MR_DN0	Y4	DMI_RXN0	DMI_TXN0	AC1	DMI_MT_IR_DN0 (18)
(18) DMI_IT_MR_DP1	AA4	DMI_RXP1	DMI_TXP1	AD3	DMI_MT_IR_DP1 (18)
(18) DMI_IT_MR_DN1	AA5	DMI_RXN1	DMI_TXN1	AD2	DMI_MT_IR_DN1 (18)
(18) DMI_IT_MR_DP2	AB4	DMI_RXP2	DMI_TXP2	AE2	DMI_MT_IR_DP2 (18)
(18) DMI_IT_MR_DN2	AB3	DMI_RXN2	DMI_TXN2	AE1	DMI_MT_IR_DN2 (18)
(18) DMI_IT_MR_DP3	AC4	DMI_RXP3	DMI_TXP3	AF2	DMI_MT_IR_DP3 (18)
(18) DMI_IT_MR_DN3	AC5	DMI_RXN3	DMI_TXN3	AF3	DMI_MT_IR_DN3 (18)

GP

(062.10015.0161)

SKYLAKE SOCKET

SKT1



Load Plate
(22.78003.021)

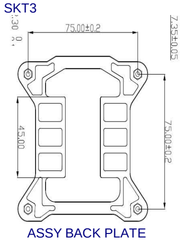
SKT2

Back Plate
(22.78006.031)

SKT4

ILMCOVER
(22.78005.171)

SKT3



ASSY BACK PLATE
(60.3EQ19.002)

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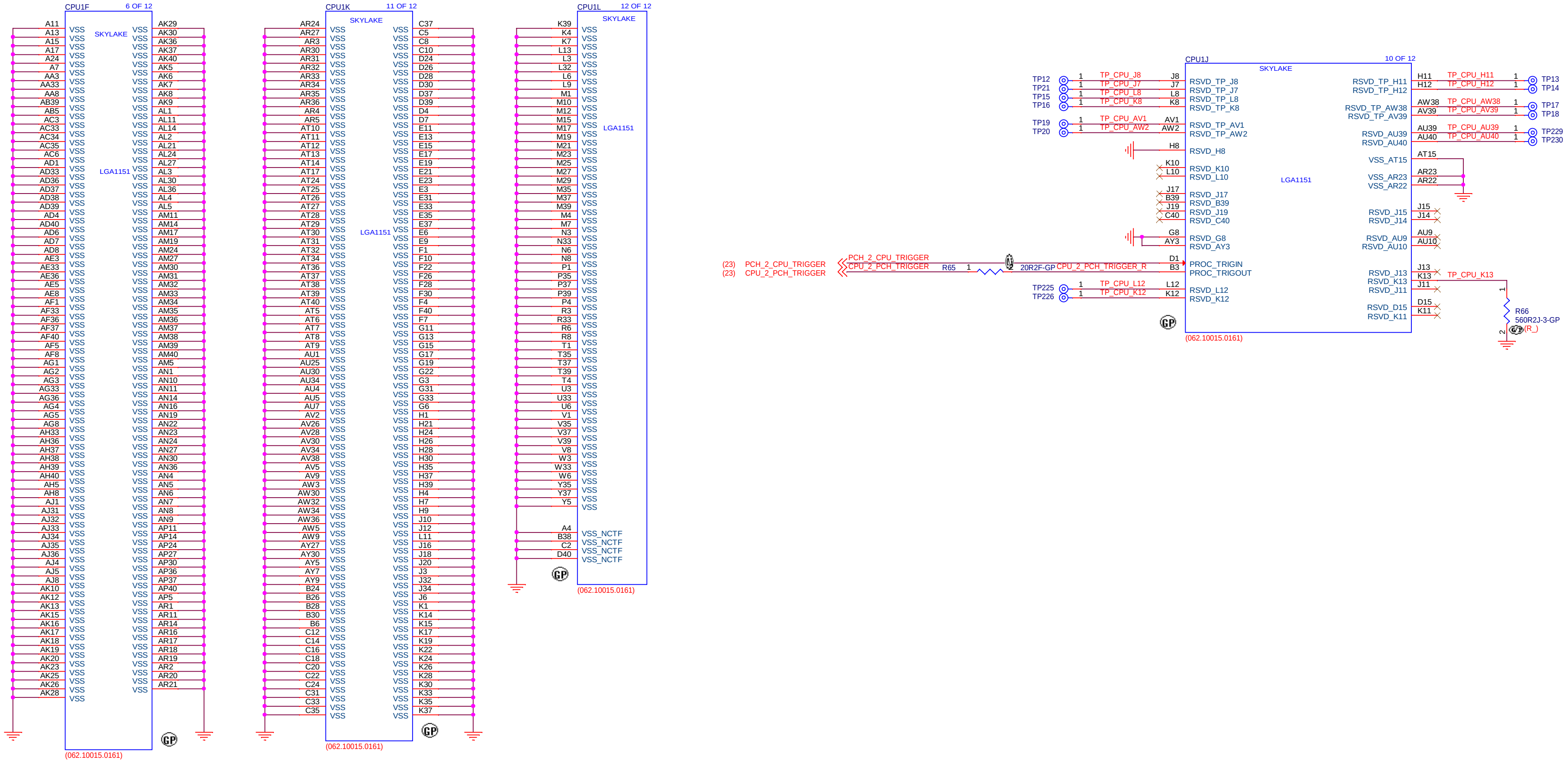
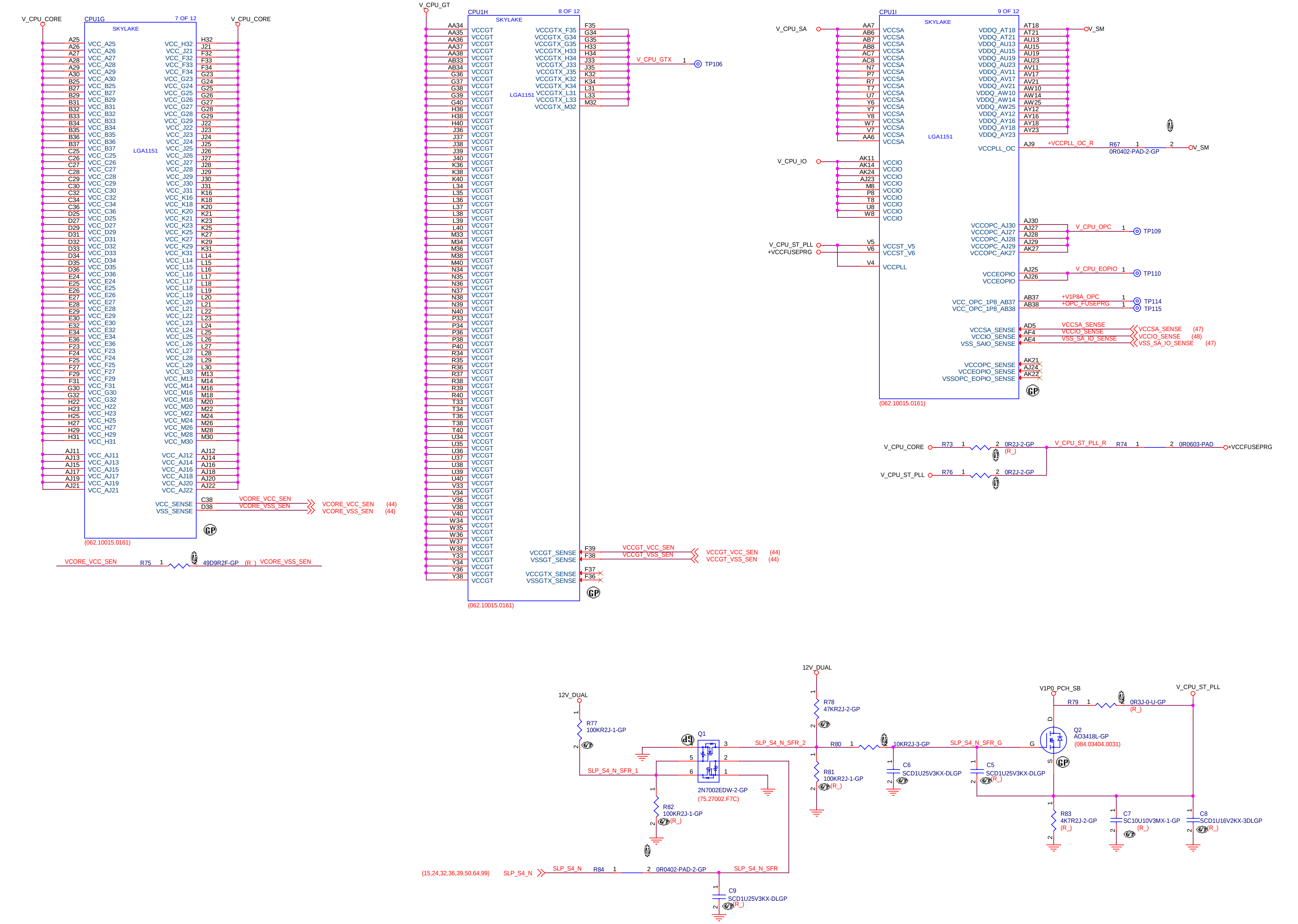
Title	CPU_(PCIE)		
Size B	Document Number TAHOE_MT		Rev -1
Date:	Thursday, July 02, 2015	Sheet 5 of 107	



wistron	**Wistron Incorporated** 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	**CPU_(VSS)**
Size C	Document Number **TAHOE_MT** — Rev -1
Date: Thursday, July 02, 2015	Sheet 6 of 107



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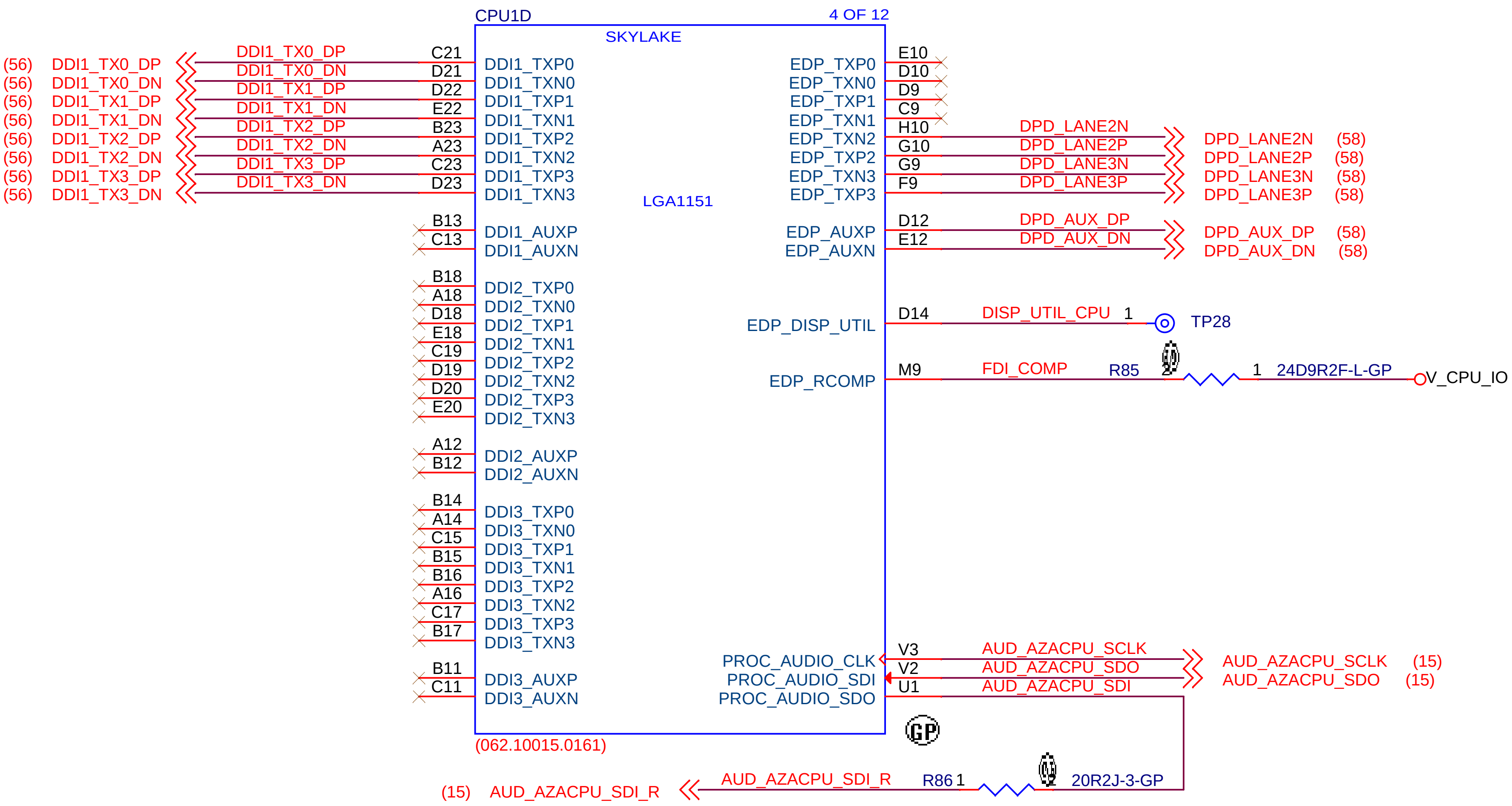
Title: **CPU_(VCC_CORE/SENCE)**

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 7 of 107



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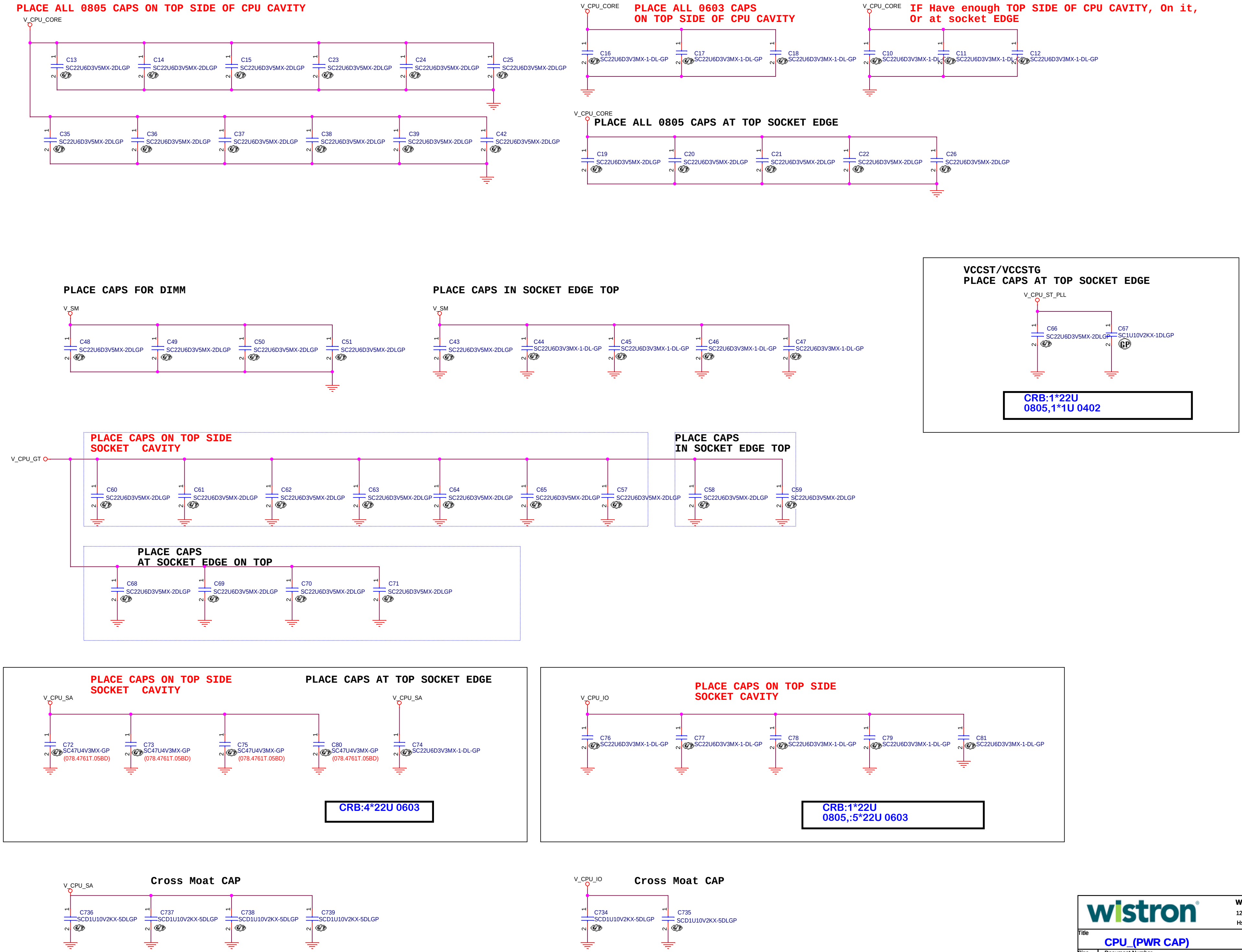
Title
CPU_(DDI/EDP)

Size	Document Number	Rev
A	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 8 of 107



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Title: CPU_(PWR CAP)

Size: C | Document Number: TAHOE_MT | Rev: -1

5 4 3 2 1

D

C

B

A

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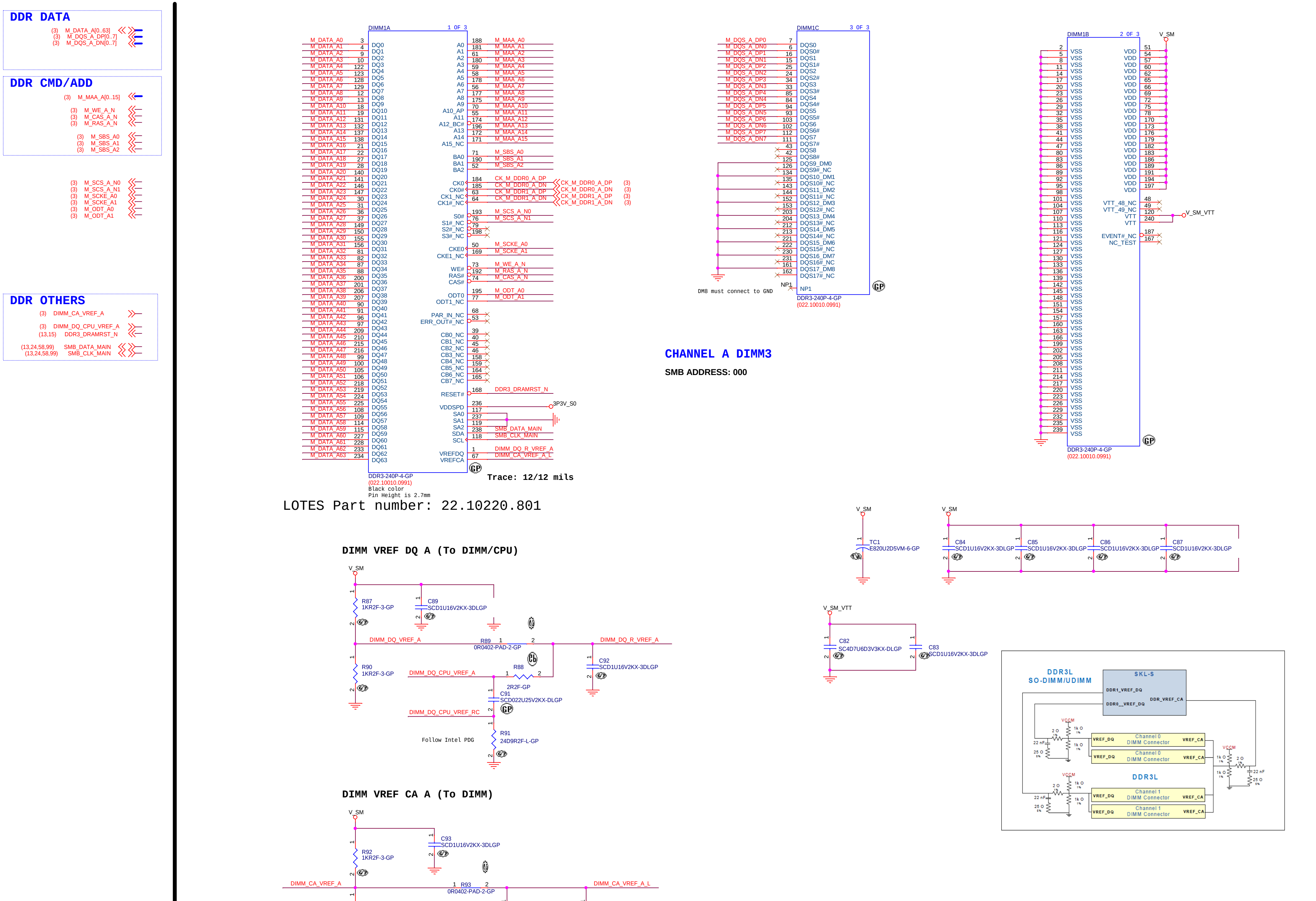
Title
CPU_(TBD)

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 10 of 107



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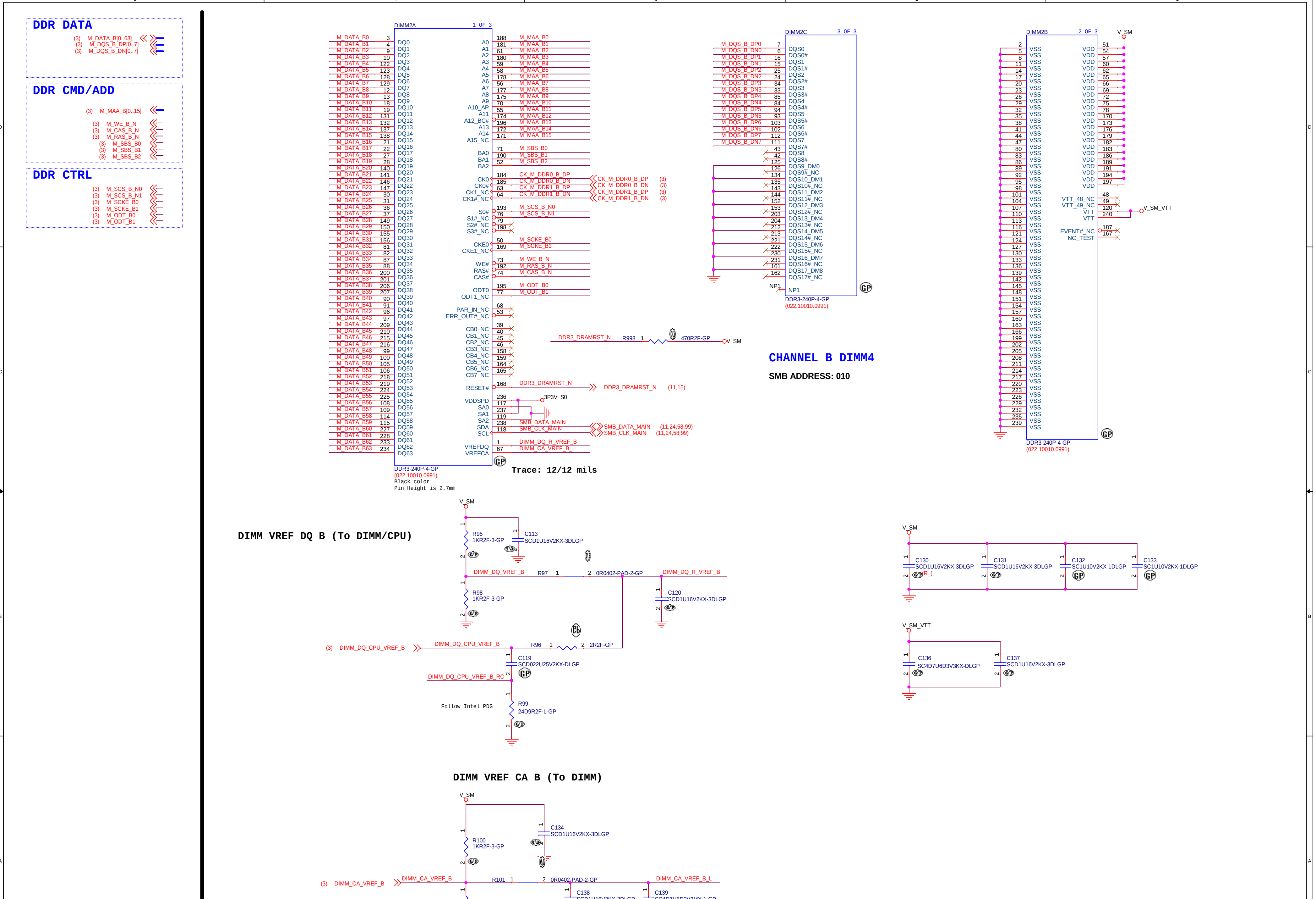
Title	DDR3 CHA DIMM 0	
Size: C	Document Number: TAHOE_MT	Rev: -1
Date: Thursday, July 02, 2015	Sheet 11 of 107	

wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	DDR3 CHA DIMM 1	
Size C	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 12 of 107	



wistron

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Title: DDR3 CHB DIMM 0		
Size: C	Document Number: TAHOE_MT	Rev: -1
Date: Thursday, July 02, 2015	Sheet 13 of 107	

5 4 3 2 1

D C B A

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Title
DDR3 CHB DIMM 1

Size	Document Number	Rev
C	TAHOE_MT	-1

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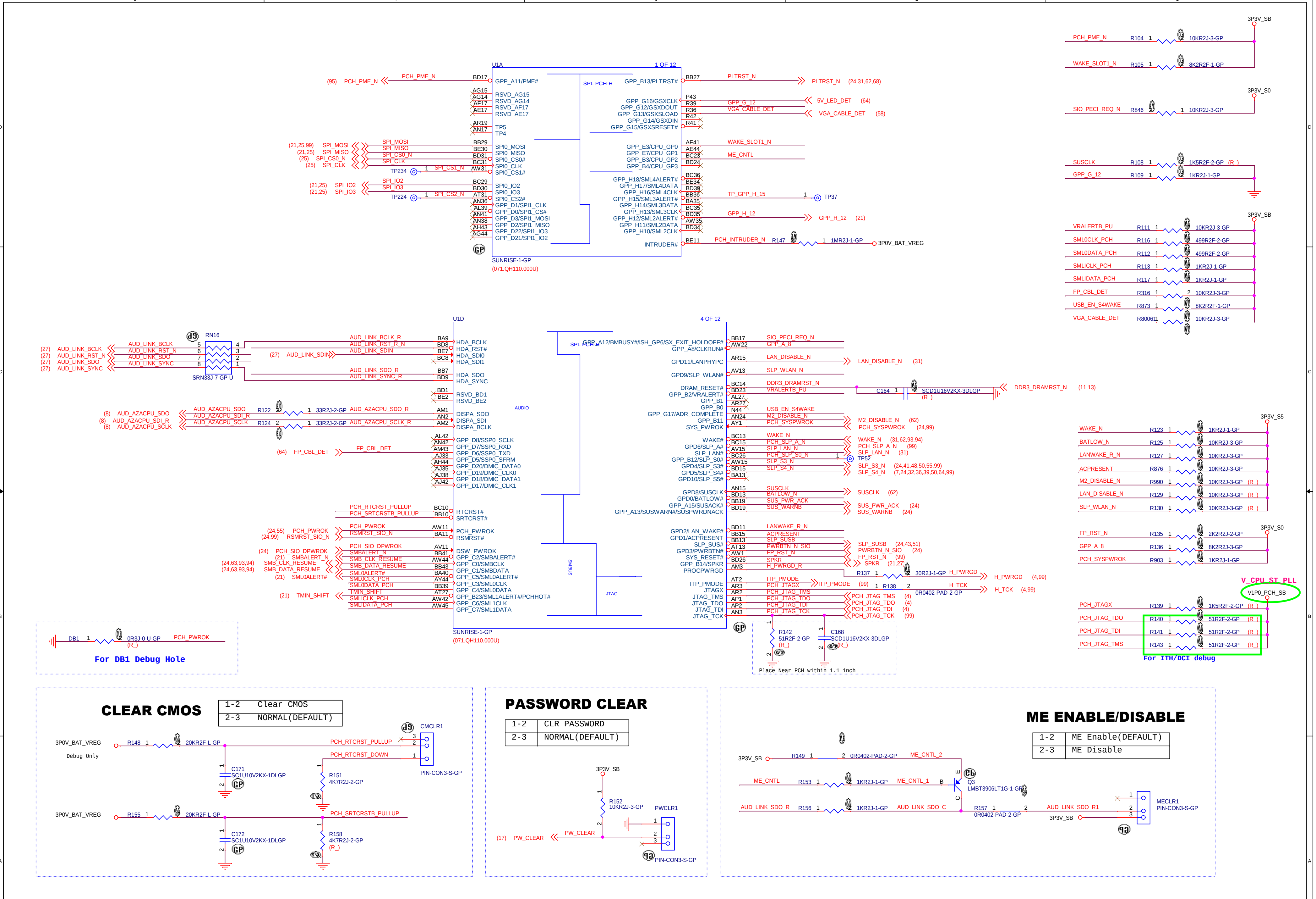

CLEAR CMOS

1-2	Clear CMOS
2-3	NORMAL(DEFAULT)

PASSWORD CLEAR

1-2	CLR PASSWORD
2-3	NORMAL(DEFAULT)

ME ENABLE/DISABLE

1-2	ME Enable(DEFAULT)
2-3	ME Disable

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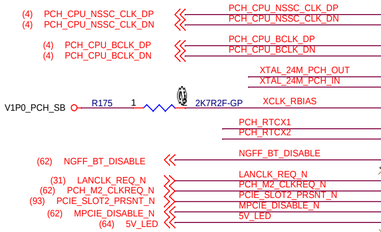
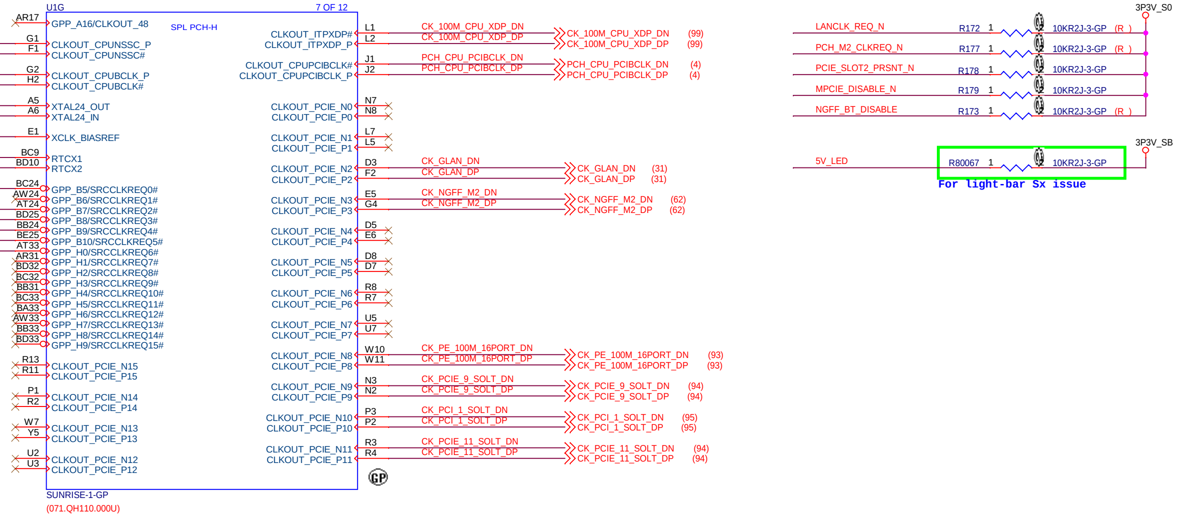
Title		
PCH_(Audio/SMBUS/JTAG/GPIO)		
Size C	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 15 of 107	

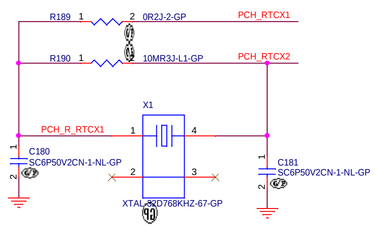
TO CPU CLOCK

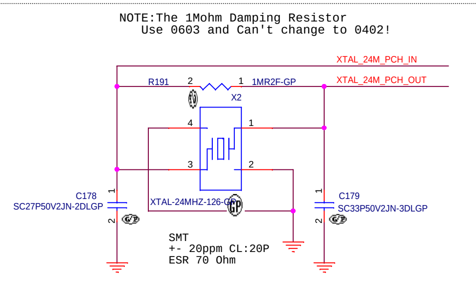




The 10-kΩ pull-up should be on the rail that the corresponding SRCCLKRQ[15:0] pin resides in.

PCI Express devices or add-in cards that do NOT support clock request should terminate the SRCCLKRQ[15:0]# pins on the PCH with 10 kΩ ±10% external pull-up resistor.



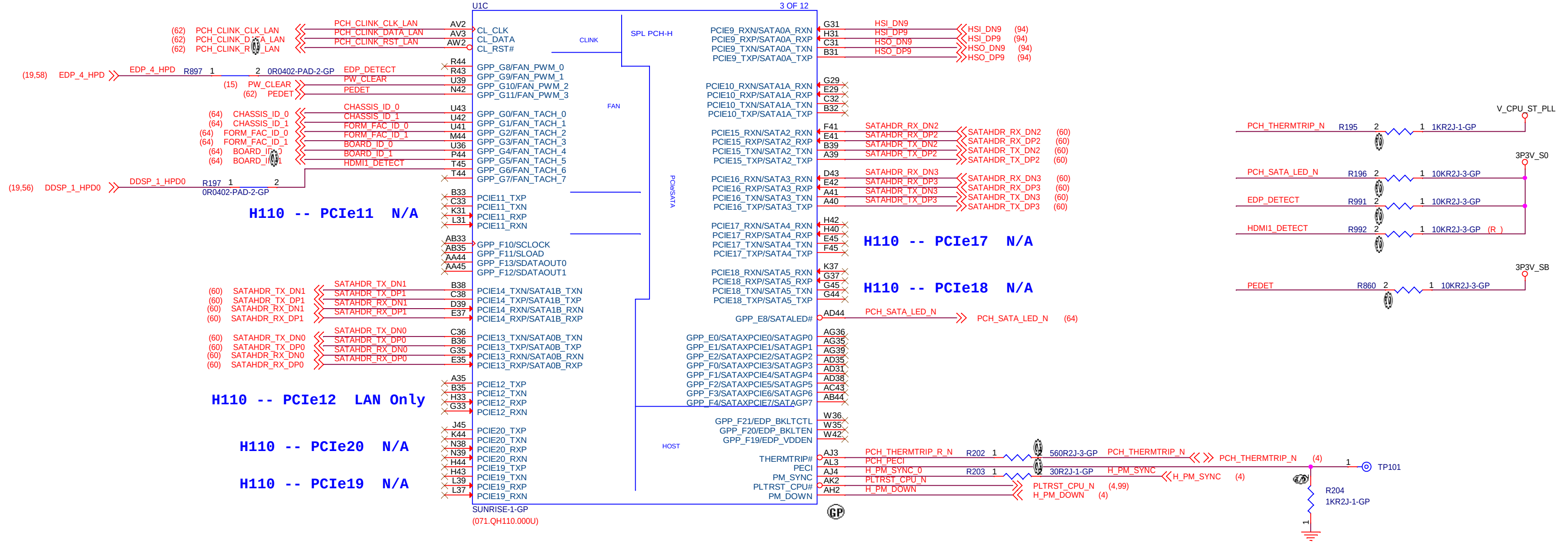


WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMV:

REMOVE R383, X2, C322

REPLACE C321 WITH 50OHM RES 0402 PACKAGE

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	PCH_(CLK)
Size C	Document Number TAHOE_MT — Rev -1
Date: Thursday, July 02, 2015	Sheet 16 of 107



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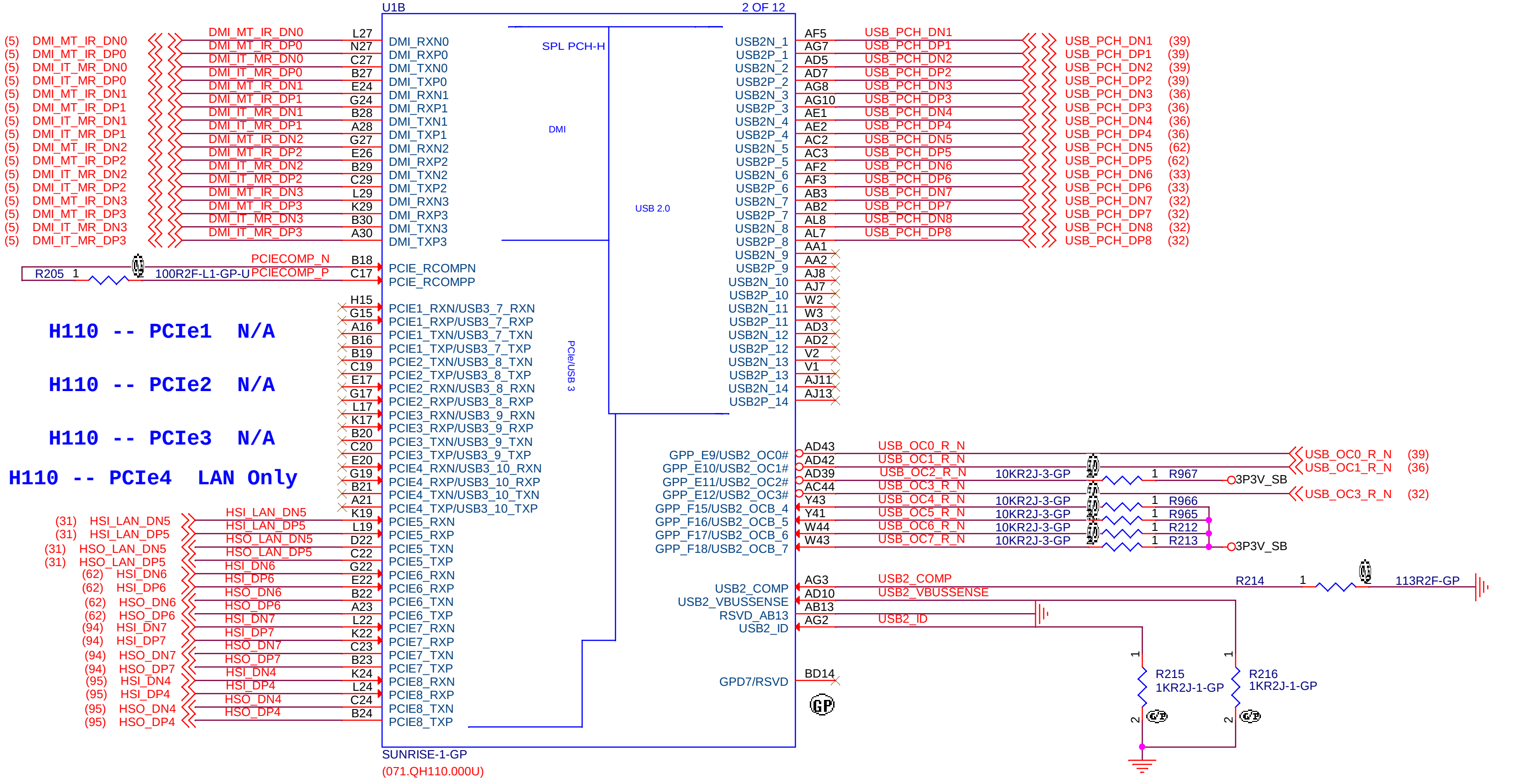
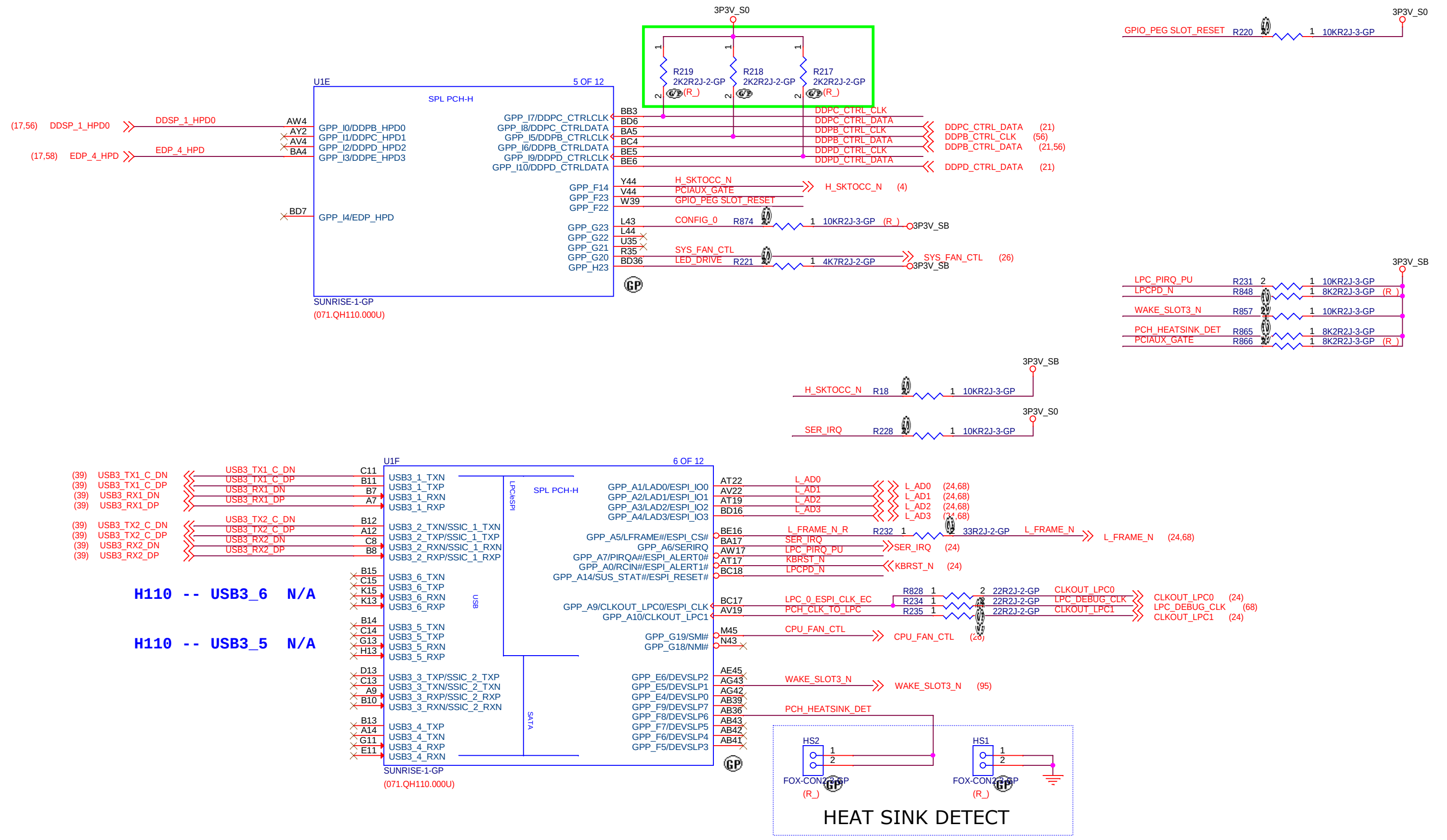
Title
PCH_(SATA/PCIE/HOST)

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 17 of 107



wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	PCH_(DMI/USB2/USB3/PCIE)	
Size B	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 18 of 107	



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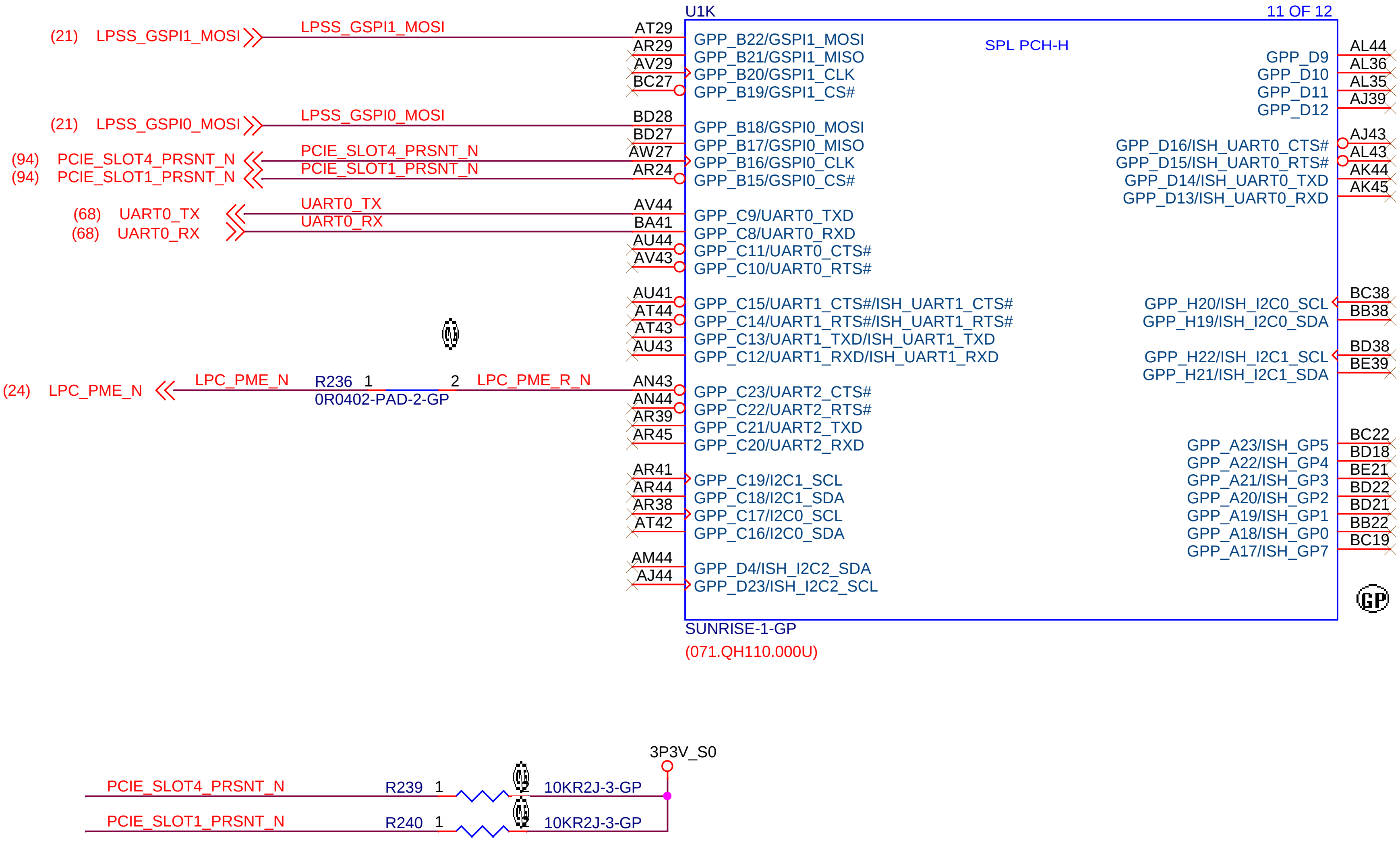
Title: PCH_(DDI/USB3/GPIO)

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 19 of 107



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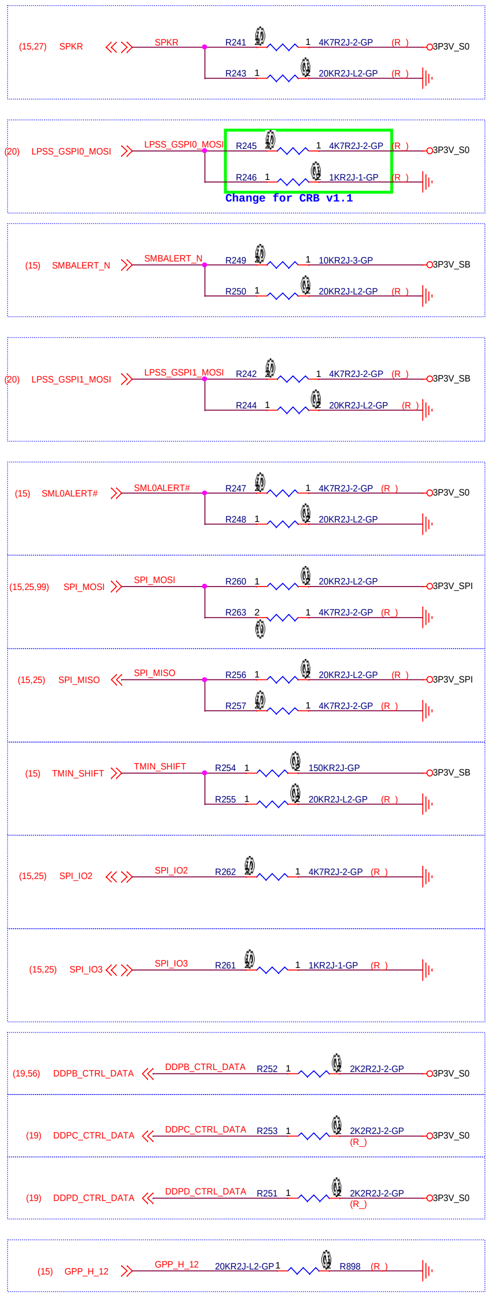
Title	PCH_(UART/GPIO/I2C)	
Size: A	Document Number: TAHOE_MT	Rev: -1
Date: Thursday, July 02, 2015	Sheet 20 of 107	

SPKR/GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable “Top Swap” mode. (Default) 1 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap
GSPI0_MOSI/ GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable “No Reboot” mode. (Default) 1 = Enable “No Reboot” mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SMBALERT#/ GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6 Boot BIOS Destination 0 SPI (Default) 1 LPC
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT#/ PCHHOT#/ GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
DDPB_CTRLDATA /GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected.
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected.
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected.
GPP_H12	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



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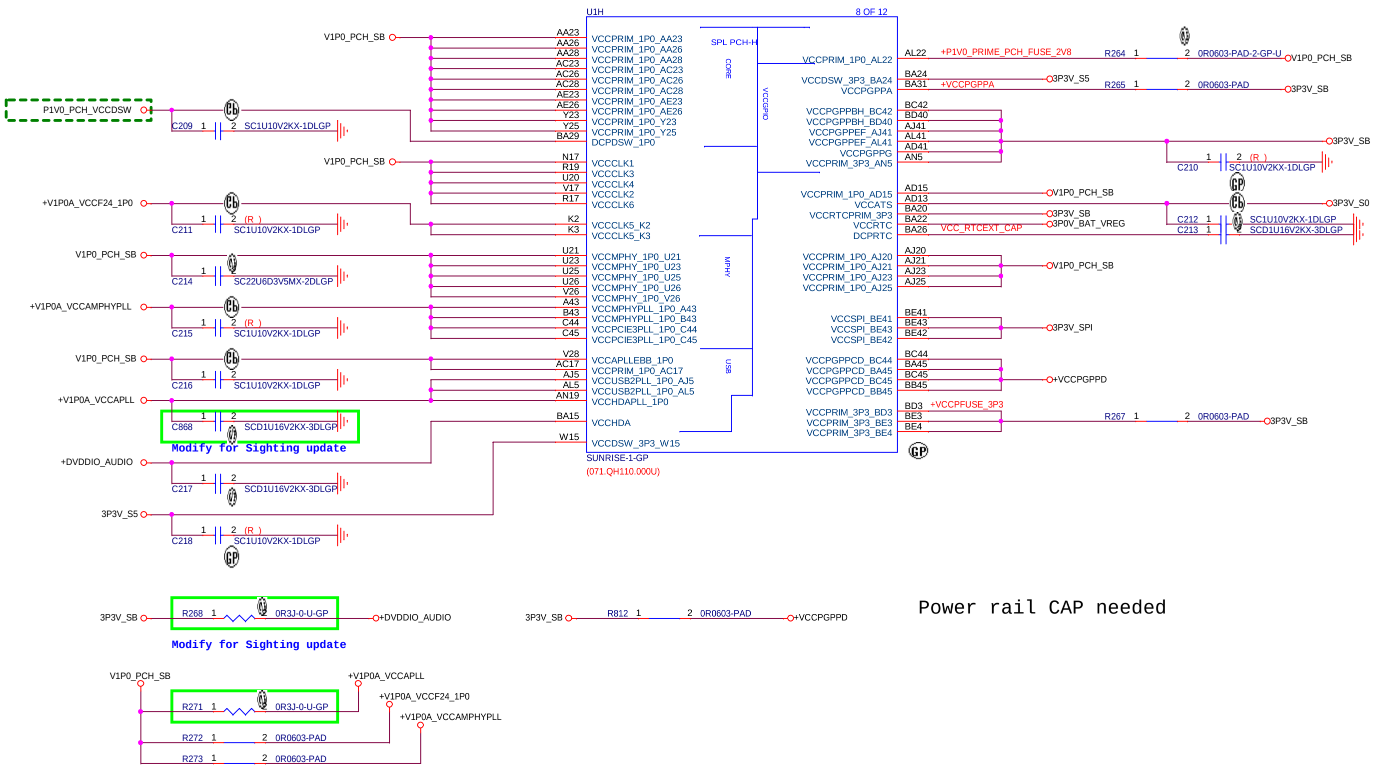
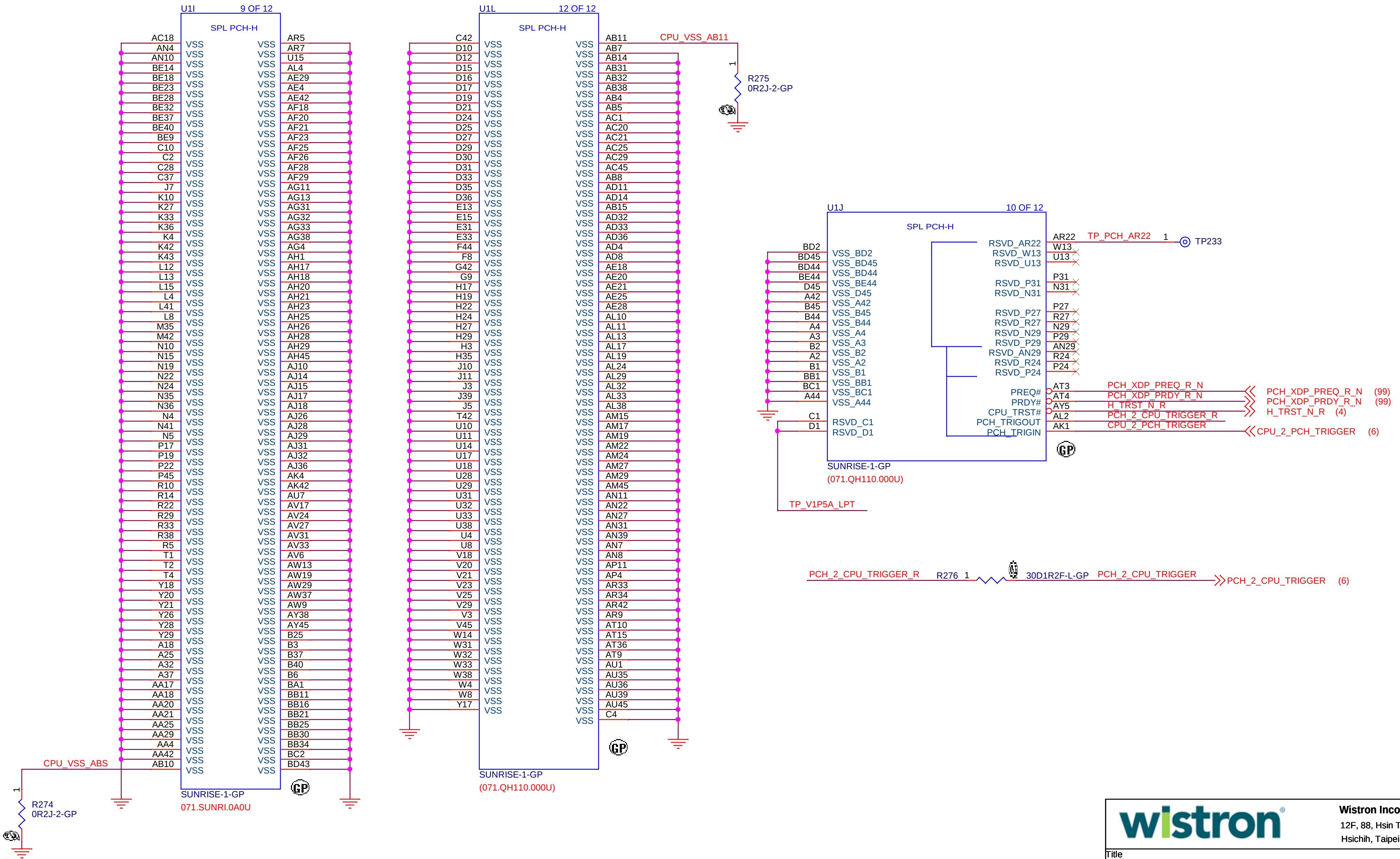
Title	PCH_(Strap Pin)	
Size C	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 21 of 107	



Power rail CAP needed



wistron

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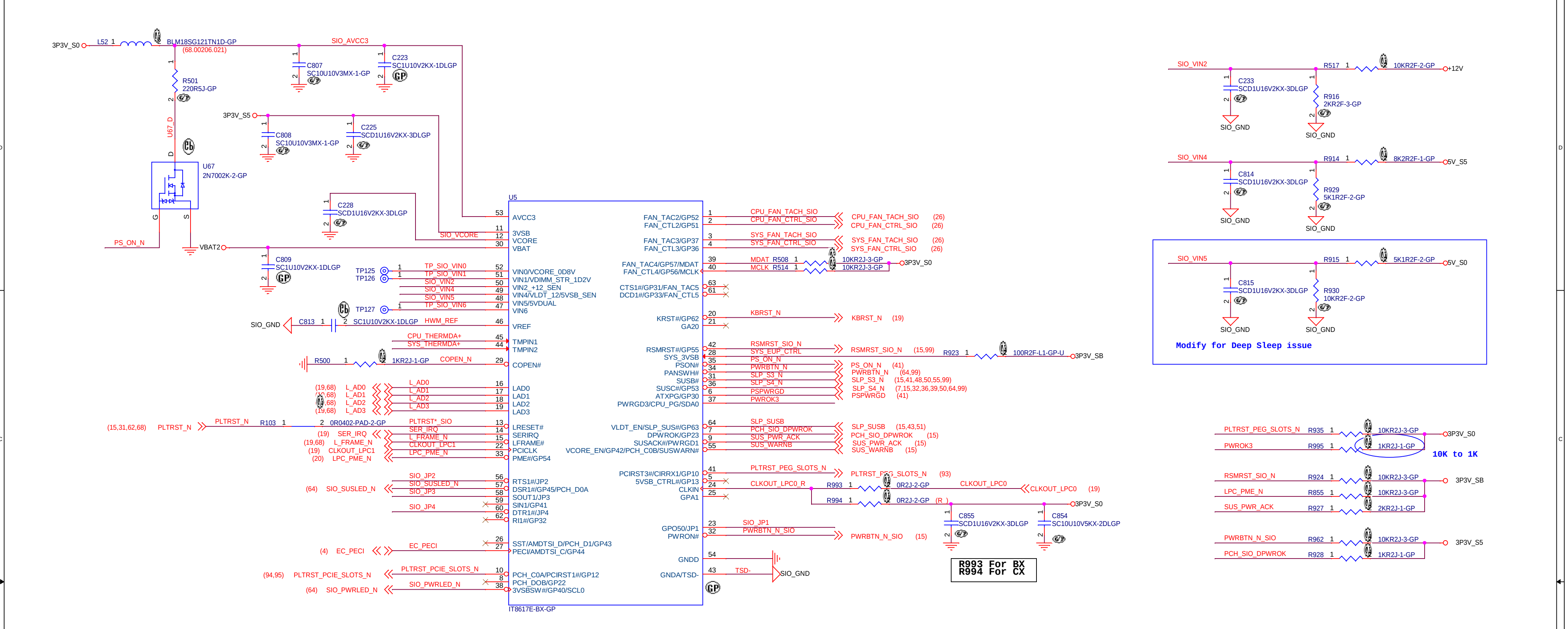
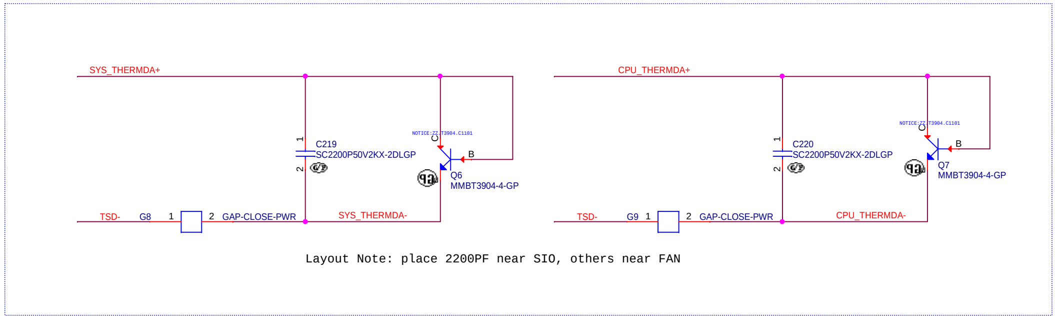
Hsichih, Taipei

Title: **PCH_(VSS/GPIO)**

Size	Document Number	Rev
B	TAHOE_MT	-1

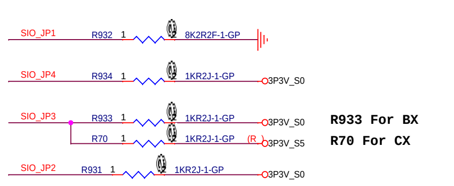
Date: Thursday, July 02, 2015 Sheet 23 of 107

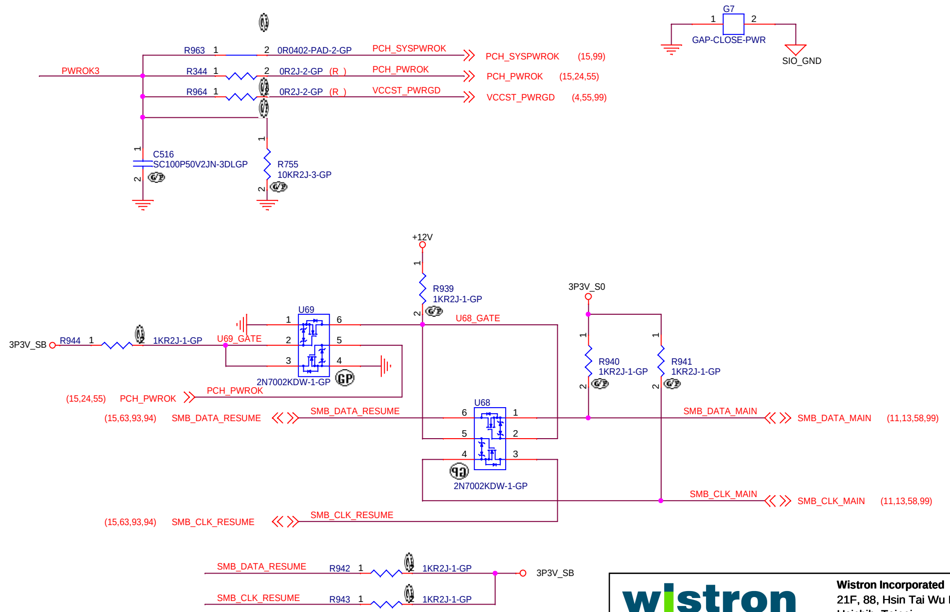




IT8772 Power On Strapping Options

	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 23		0	DSW(defult)
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 60		0	K8 power sequence function is enabled
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin 58		0	EC Index 63h/73h/7B/A3 is 00h
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin56		0	Enable WDT to rest PWROK





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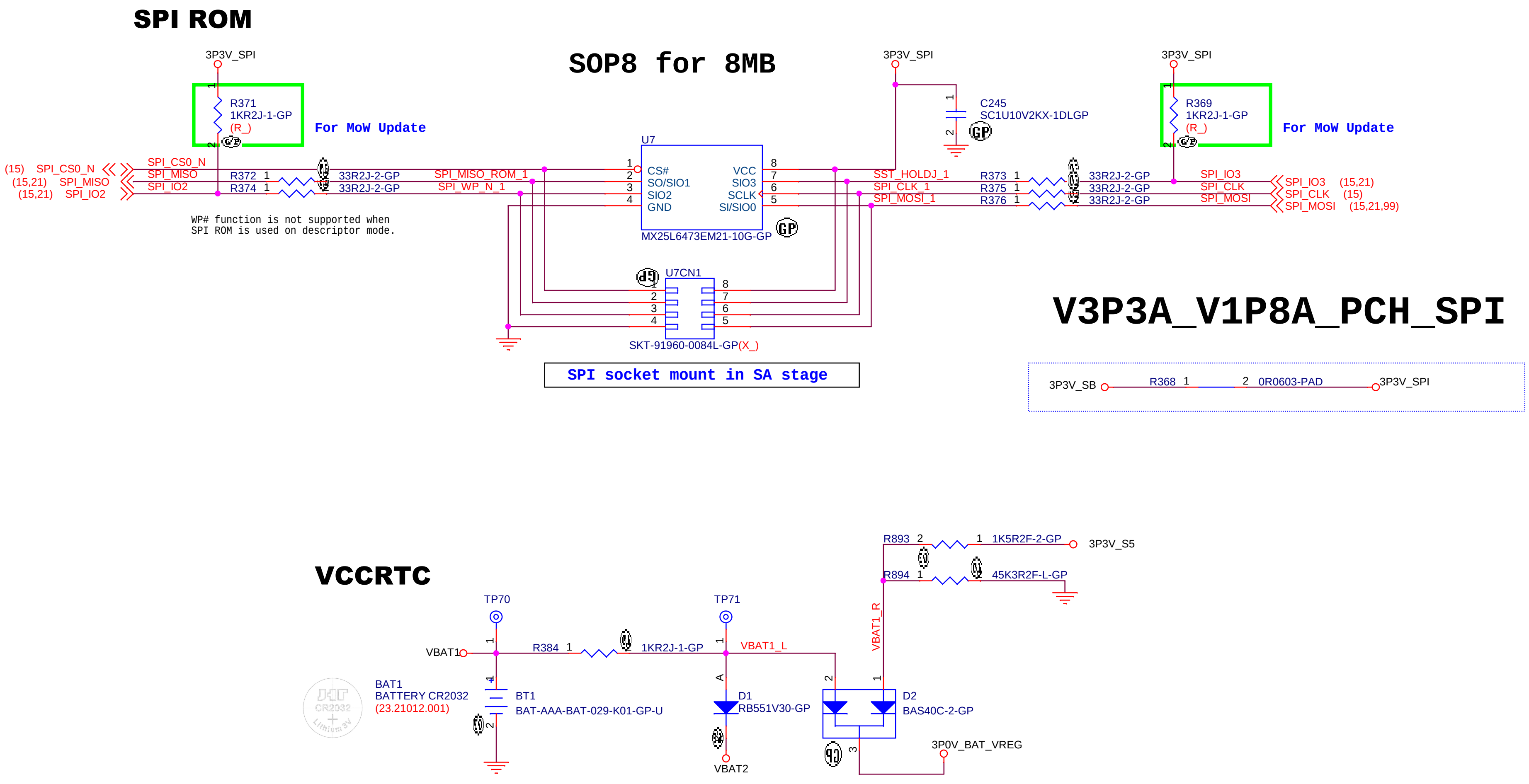
Hsichih, Taipei

Title: SIO_(IT8617)

Size: C | Document Number: TAHOE_MT | Rev: -1

Date: Thursday, July 02, 2015 | Sheet 24 of 107



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Title	SPI/RTC/BAT	
Size B	Document Number TAHOE_MT	Rev -1
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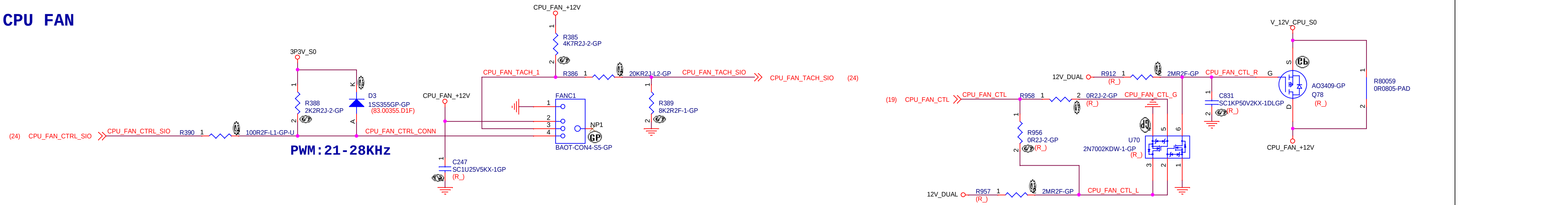
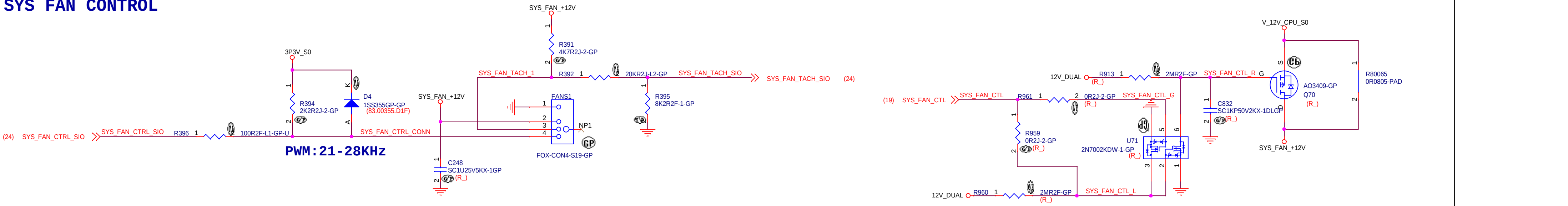
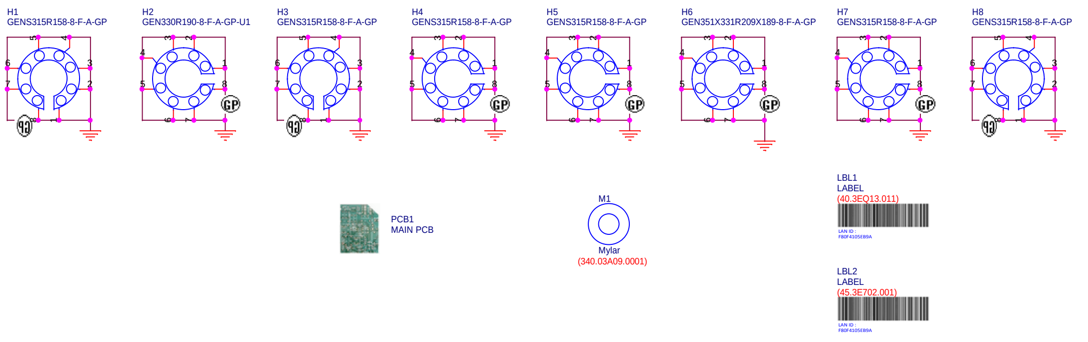
CPU FAN



SYS FAN CONTROL





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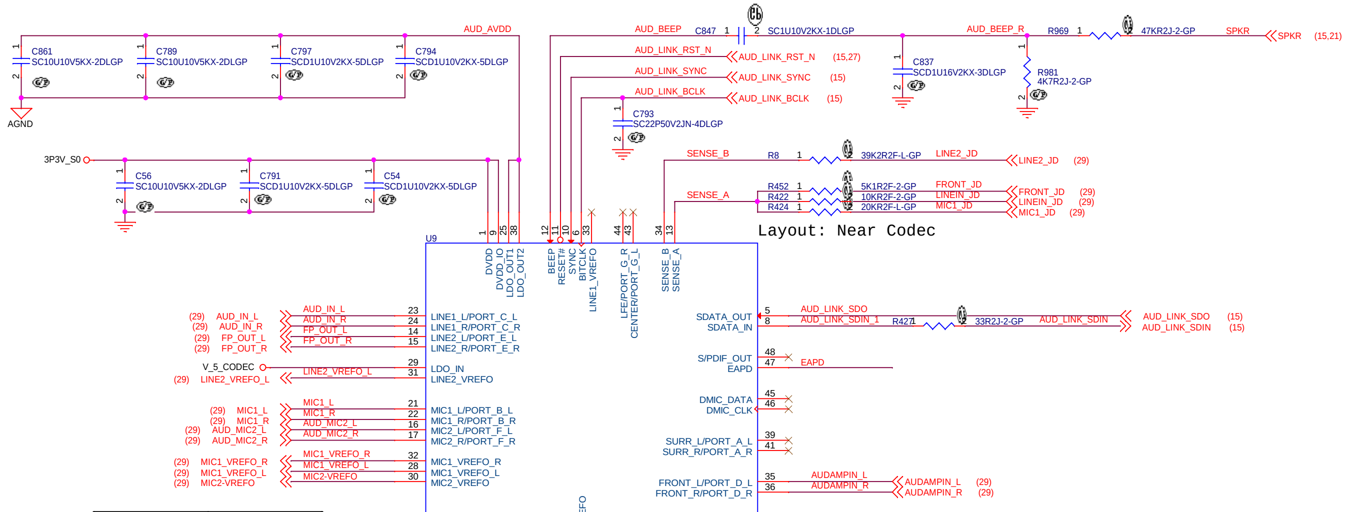
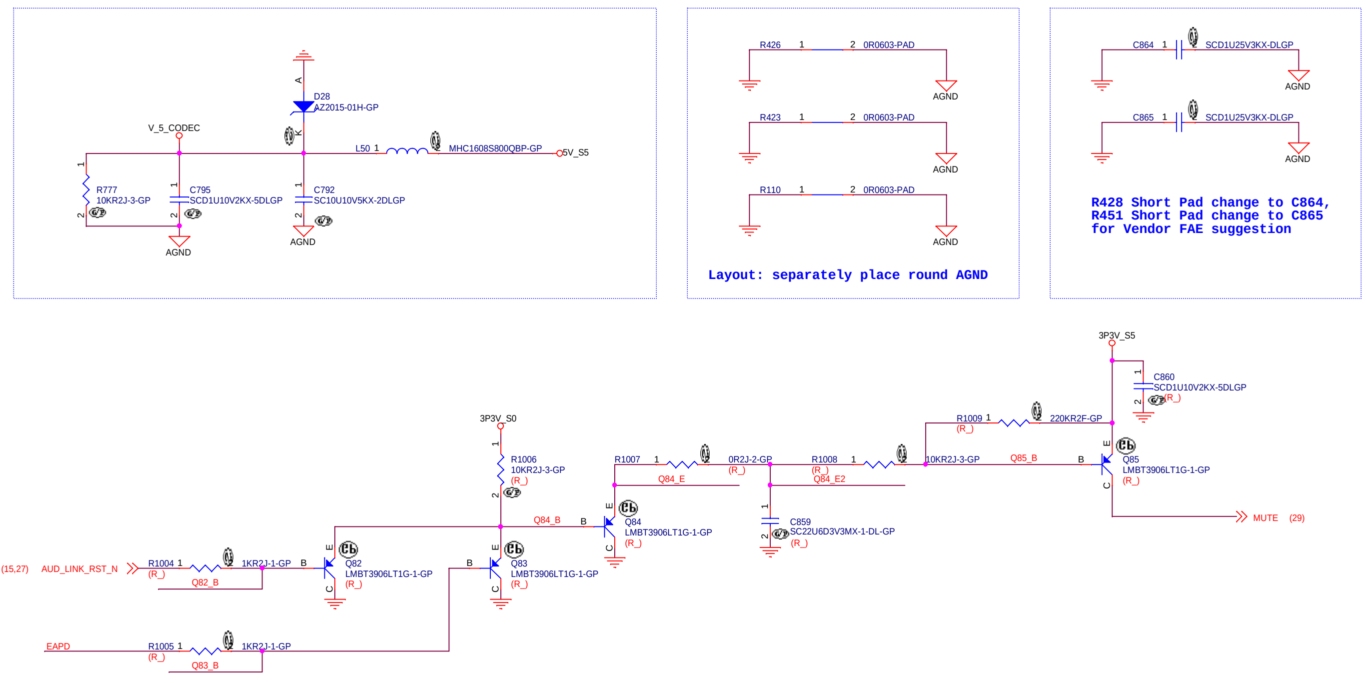
Title			
FAN CIRCUITS/HOLE			
Size: C	Document Number: TAHOE_MT		Rev: -1
Date: Wednesday, July 08, 2015	Sheet 26 of 107		



	ALC3600
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
HP-out	pin14/15



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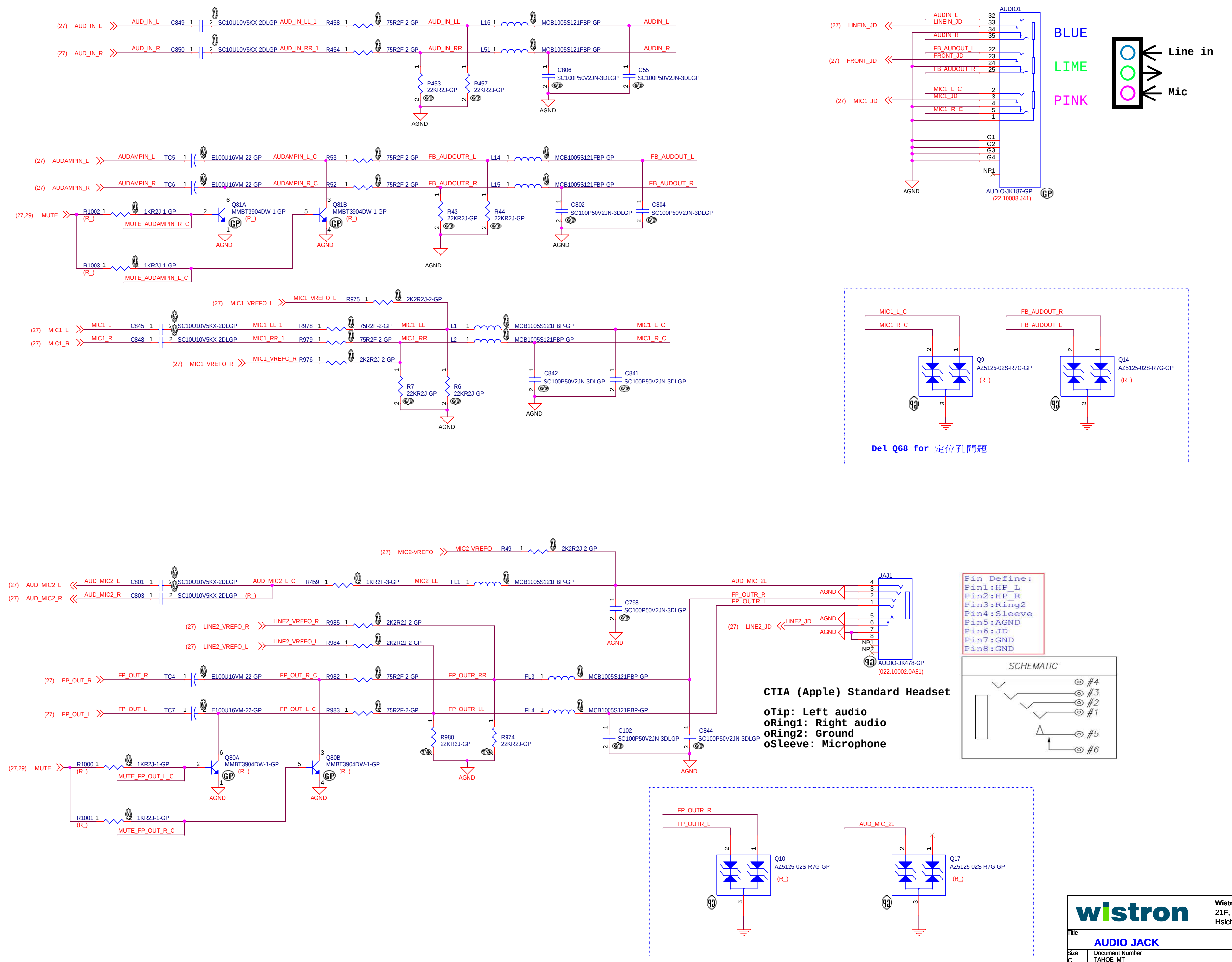
Title
AUDIO_ALC3600

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 27 of 107

Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei			
Title	Reserved		
Size A	Document Number TAHOE_MT		Rev -1
Date:	Thursday, July 02, 2015	Sheet 28 of 107	



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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **AUDIO JACK**

Size	Document Number	Rev
C	TAHOE_MT	-1

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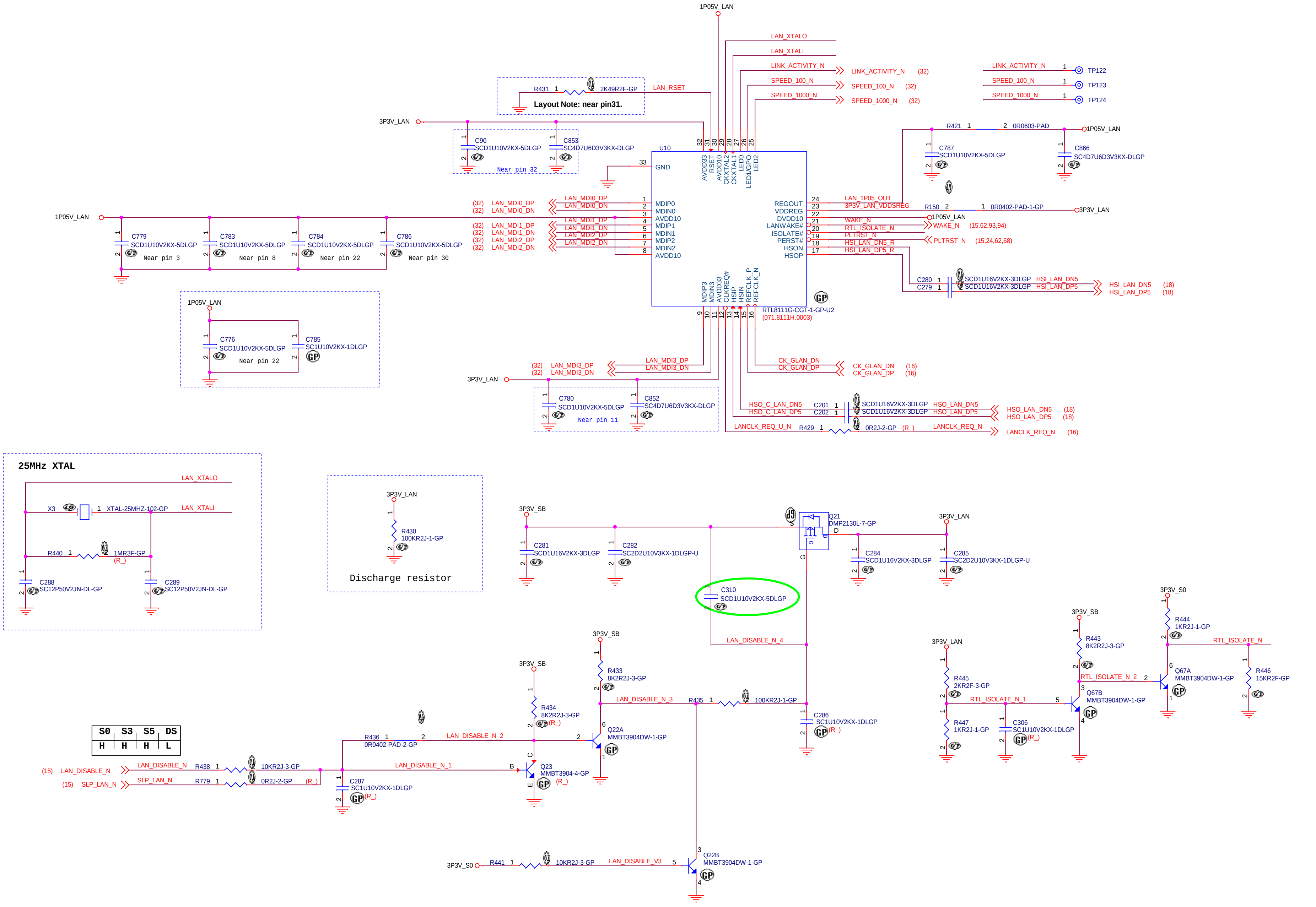
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	RTL8151GD(R)	
Size A	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 30 of 107	

5 4 3 2 1



S0	S3	S5	DS
H	H	H	L

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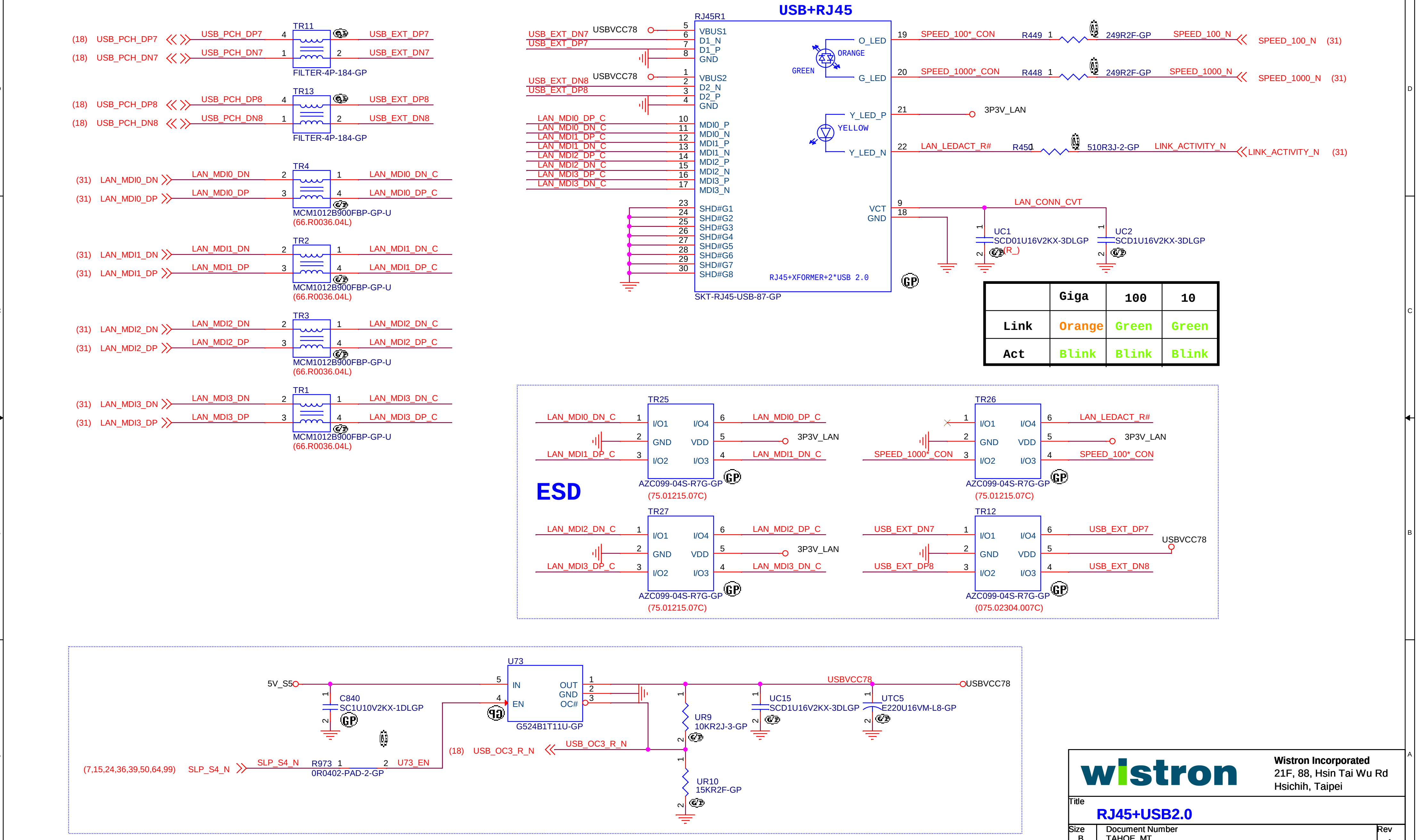
Hsichih, Taipei

Title: **LAN RTL8111H**

Size: C | Document Number: TAHOE_MT | Rev: -1

Date: Thursday, July 02, 2015 | Sheet 31 of 107



	Giga	100	10
Link	Orange	Green	Green
Act	Blink	Blink	Blink

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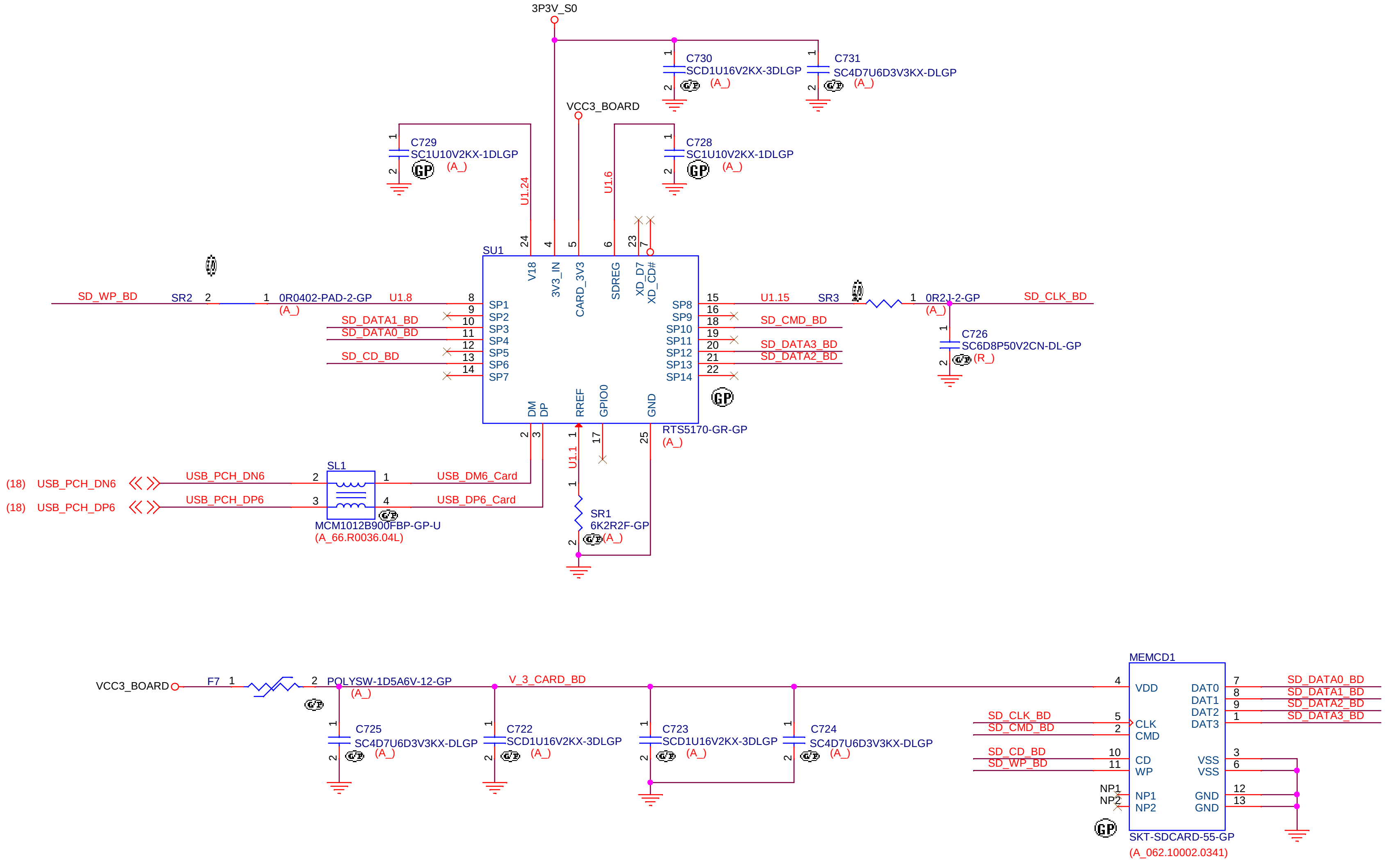
Hsichih, Taipei

Title: RJ45+USB2.0

Size	Document Number	Rev
B	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 32 of 107



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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
RTS5170

Size	Document Number	Rev
B	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 33 of 107

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wistron		**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	Reserved	
Size C	Document Number TAHOE_MT	Rev -1
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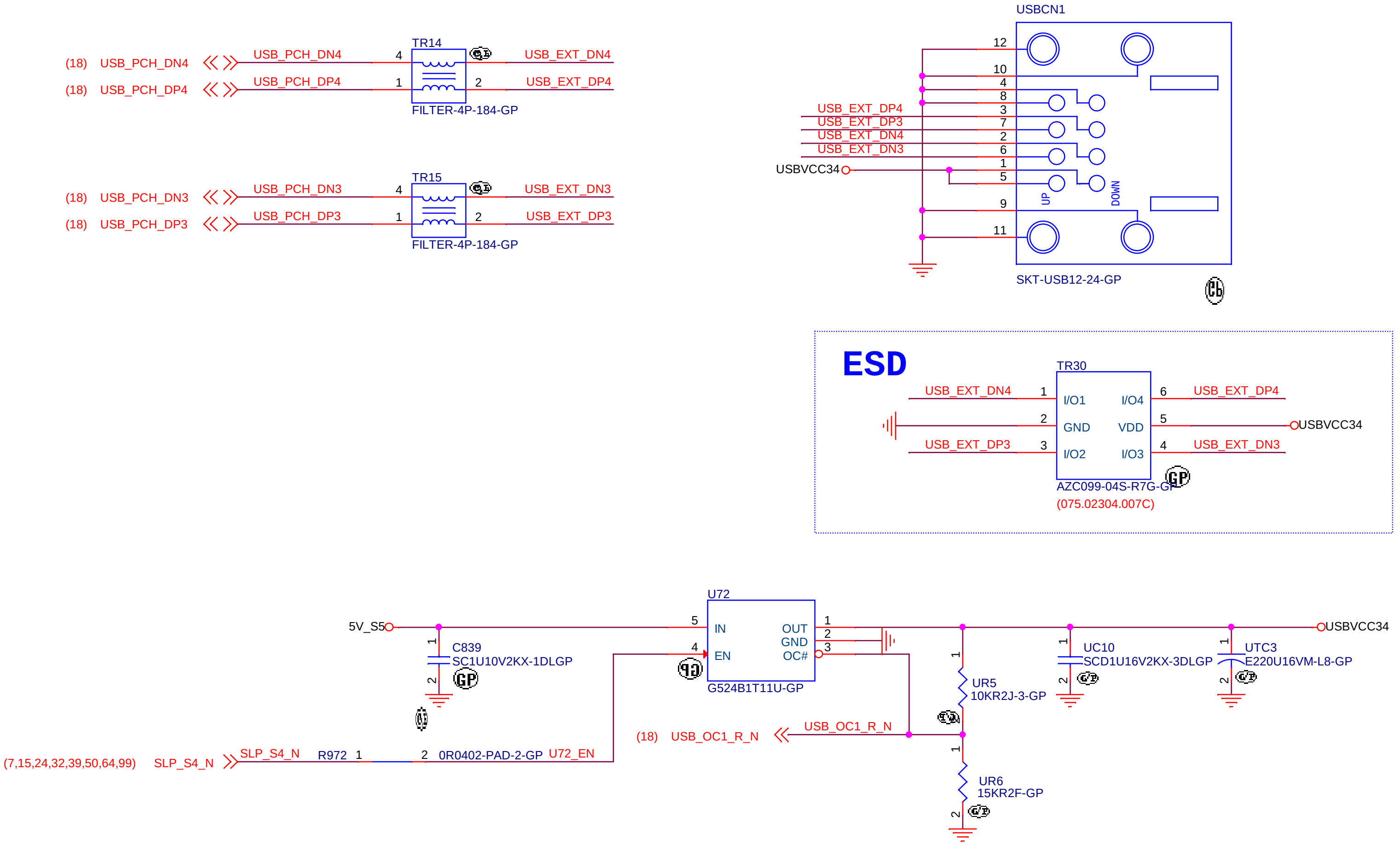

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Hsichih, Taipei

Title
REAR USB 2.0

Size	Document Number	Rev
B	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 36 of 107

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Wistron Incorporated
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Title	Front USB2.0(R)	
Size: Custom	Document Number: TAHOE_MT	Rev: -1
Date: Thursday, July 02, 2015	Sheet 37 of 107	

5 4 3 2 1

5 4 3 2 1

D C B A

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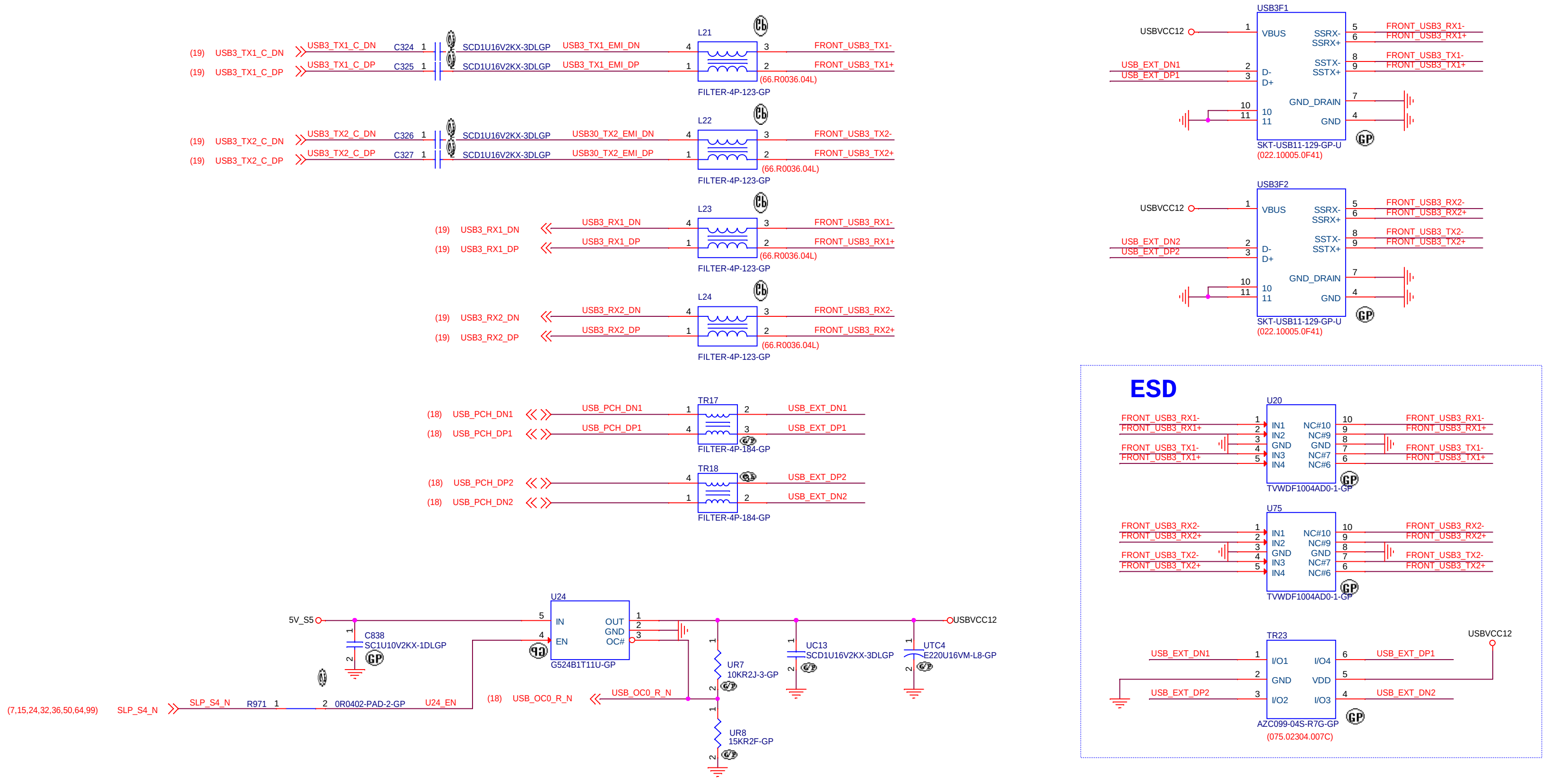
Hsichih, Taipei

Title	Rear USB3.0*4	
Size Custom	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 38 of 107	



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Hsichih, Taipei

Title: Front USB3.0

Size	Document Number	Rev
C	TAHOE_MT	-1

Date: Thursday, July 02, 2015 Sheet 39 of 107

5 4 3 2 1

D C B A

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	TBD		
Size A	Document Number TAHOE_MT		Rev -1
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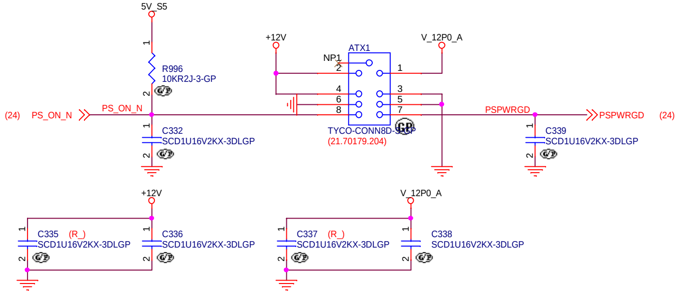
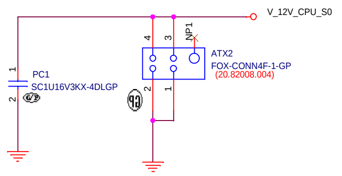
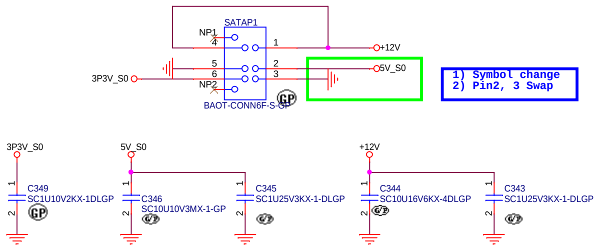
1	+12VSB	5	COM
2	+12VBDC	6	COM
3	COM	7	P_OK
4	+12VBDC	8	PS_ON

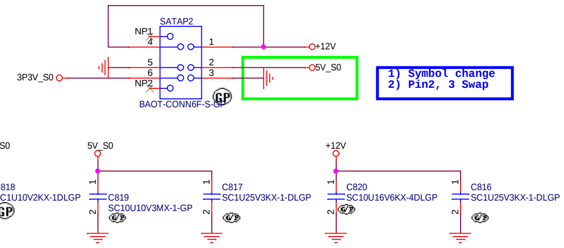


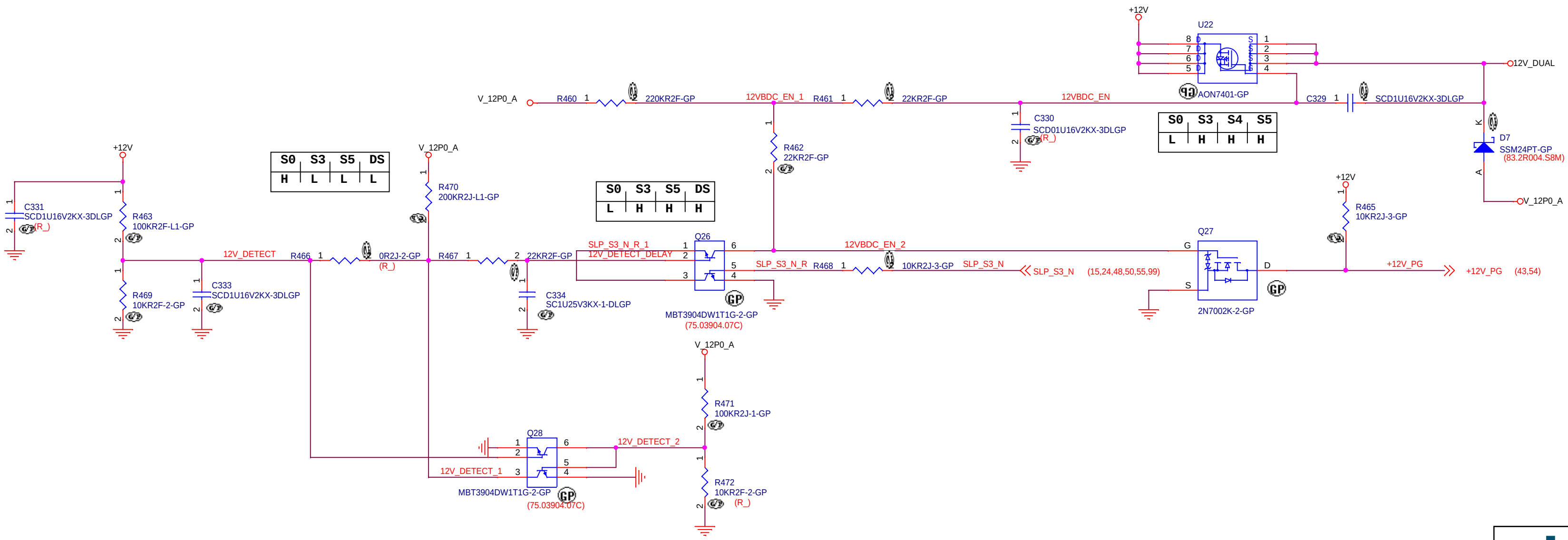


3.5" SATA POWER CONNECTOR



2.5" SATA POWER CONNECTOR





S0	S3	S5	DS
H	L	L	L

S0	S3	S5	DS
L	H	H	H

S0	S3	S4	S5
L	H	H	H

5 4 3 2 1

D

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Hsichih, Taipei

Title	Run PWR/USB PWR	
Size C	Document Number TAHOE_MT	Rev -1
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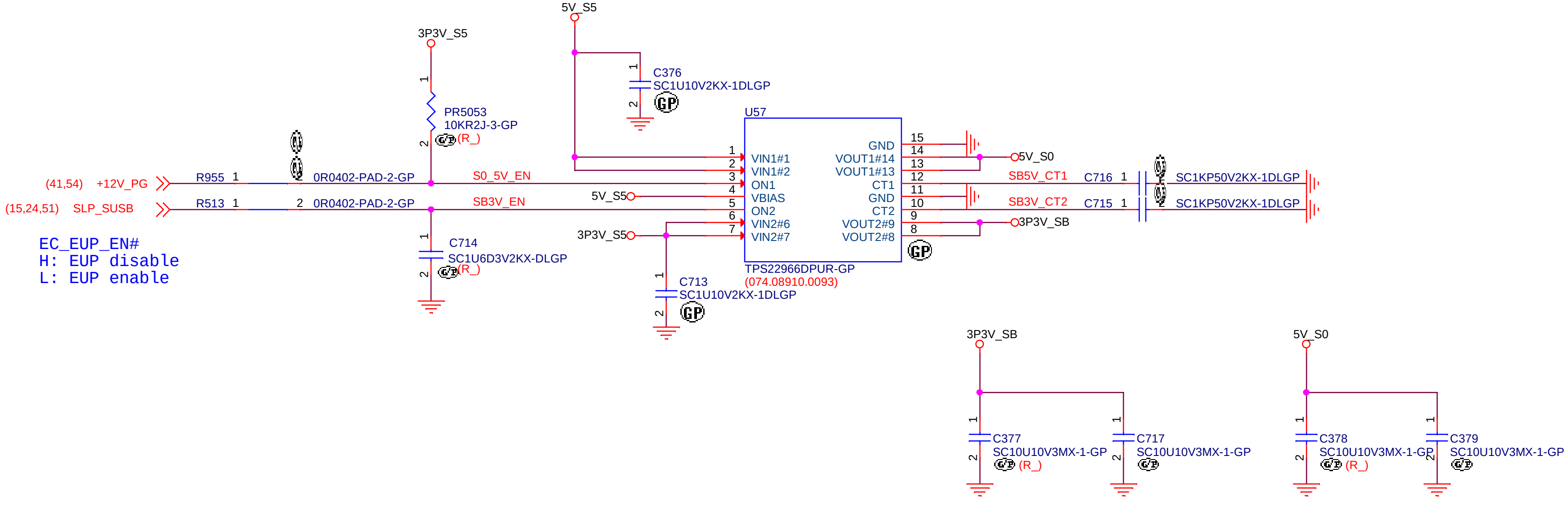

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Hsichih, Taipei

Title	DSW_PWR_CTRL	
Size B	Document Number TAHOE_MT	Rev -1
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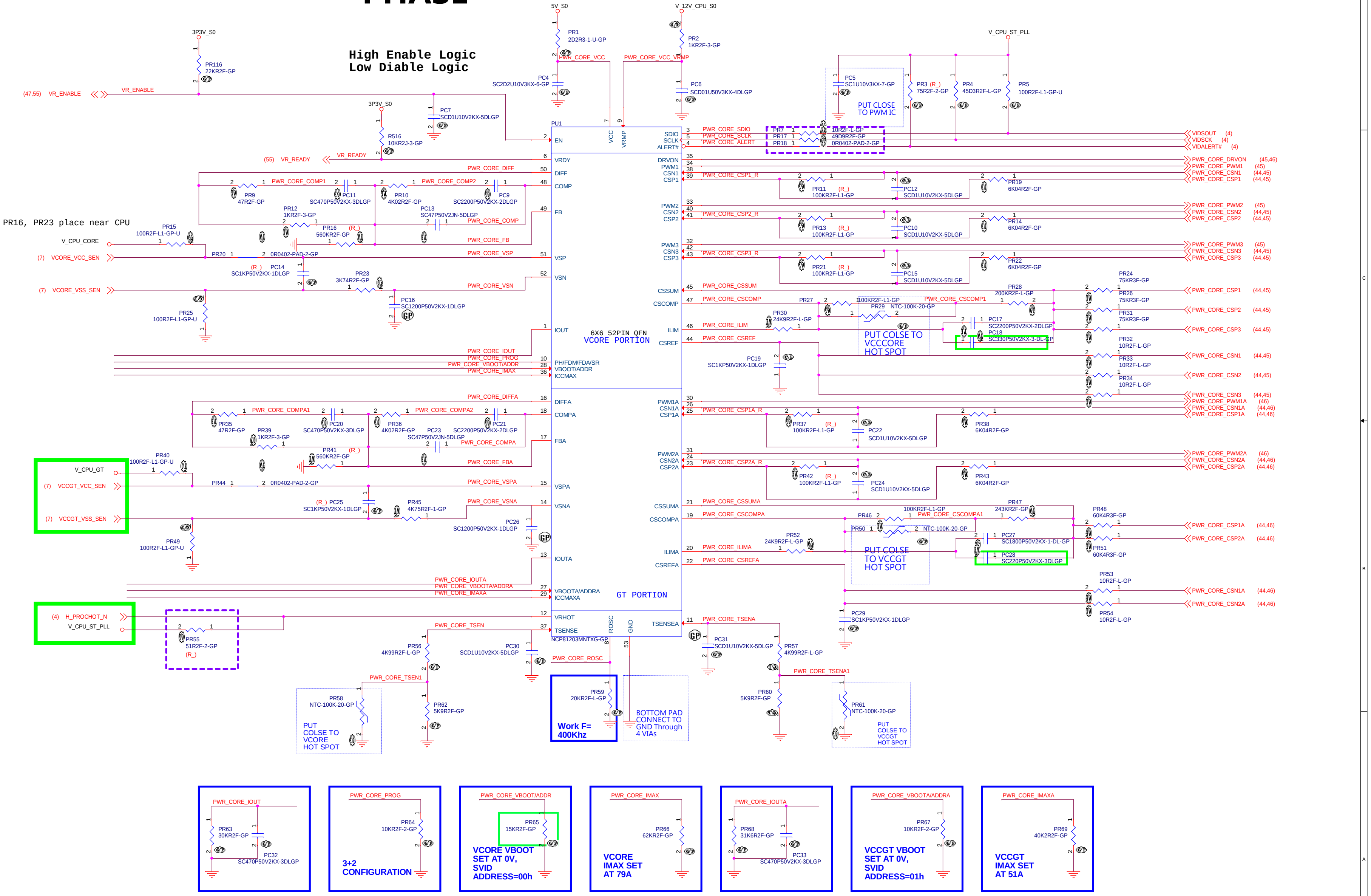
VCC CORE&GT_PWR

Intel SKYLAKE IMVP8 POWER CKT 3+2 PHASE



wistron
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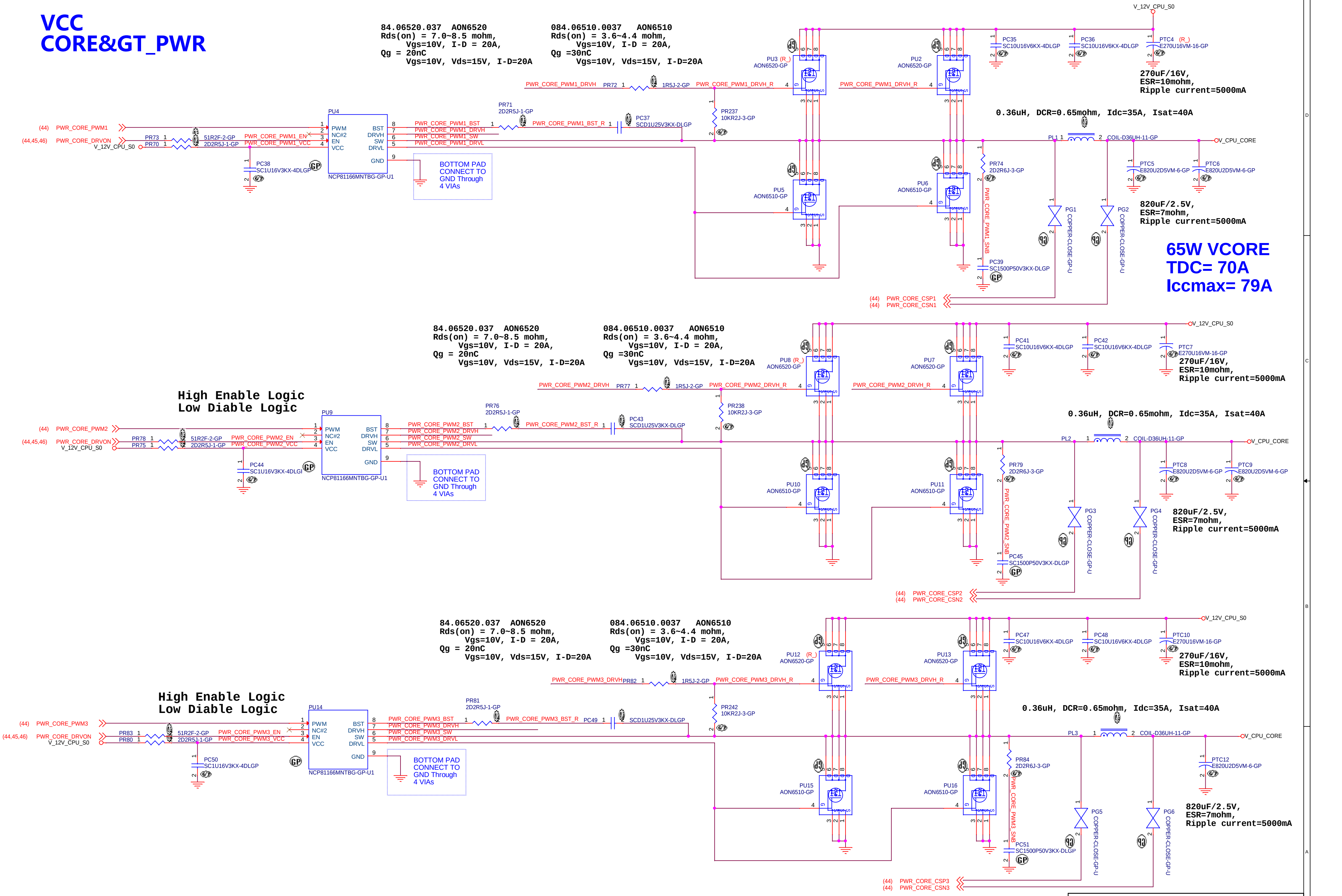
Hsichih, Taipei

Title: VCORE & V_GT(NCP81203)

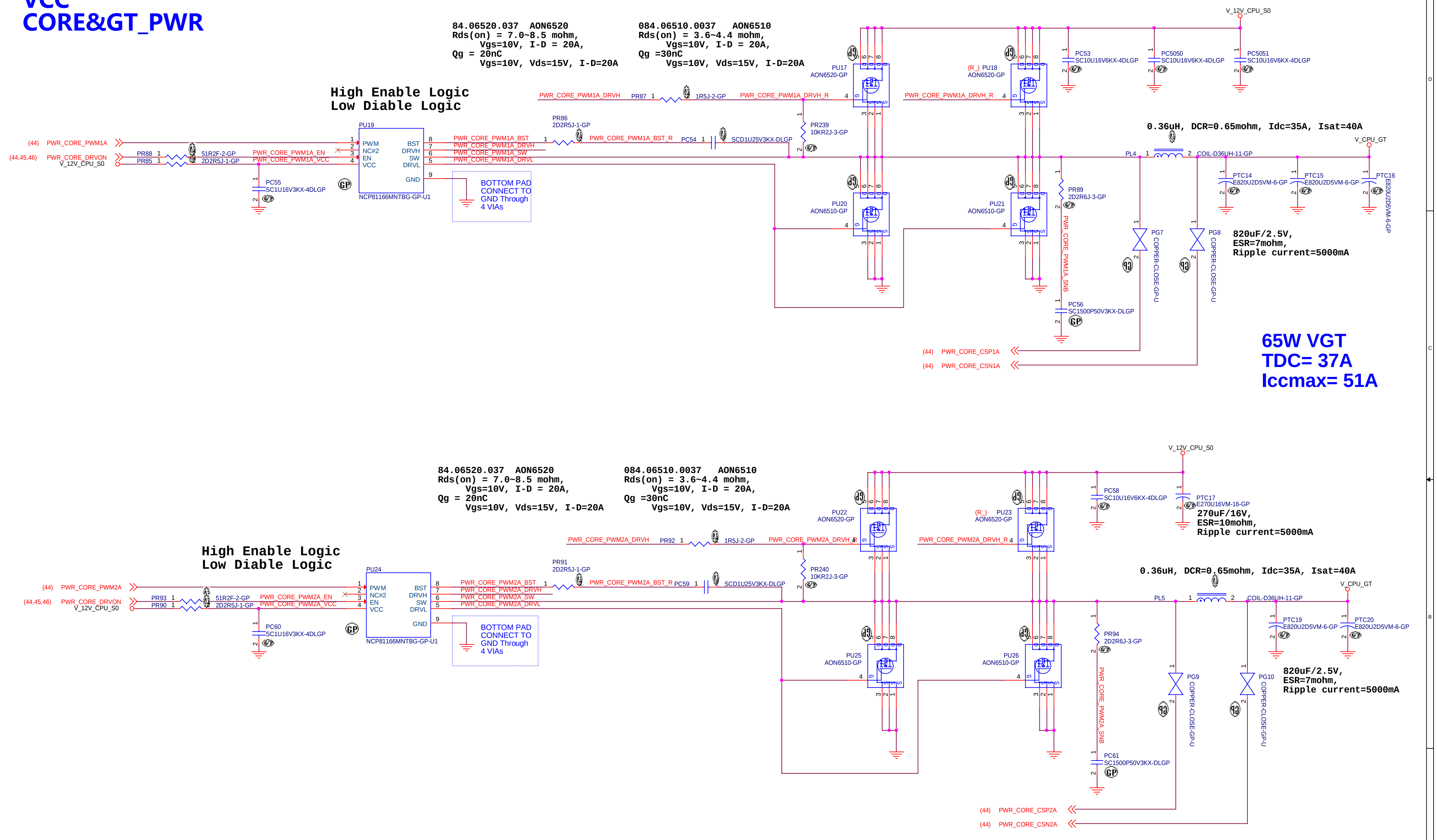
Size: Custom | Document Number: TAHOE_MT | Rev: -1

VCC CORE&GT_PWR



wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	VCORE Output(NCP81161)
Size C	Document Number TAHOE_MT — Rev -1
Date: Thursday, July 02, 2015	Sheet 45 of 107

VCC CORE&GT_PWR



wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	V_GT Output(NCP81161)
Size C	Document Number TAHOE_MT
Rev	-1
Date:	Thursday, July 02, 2015
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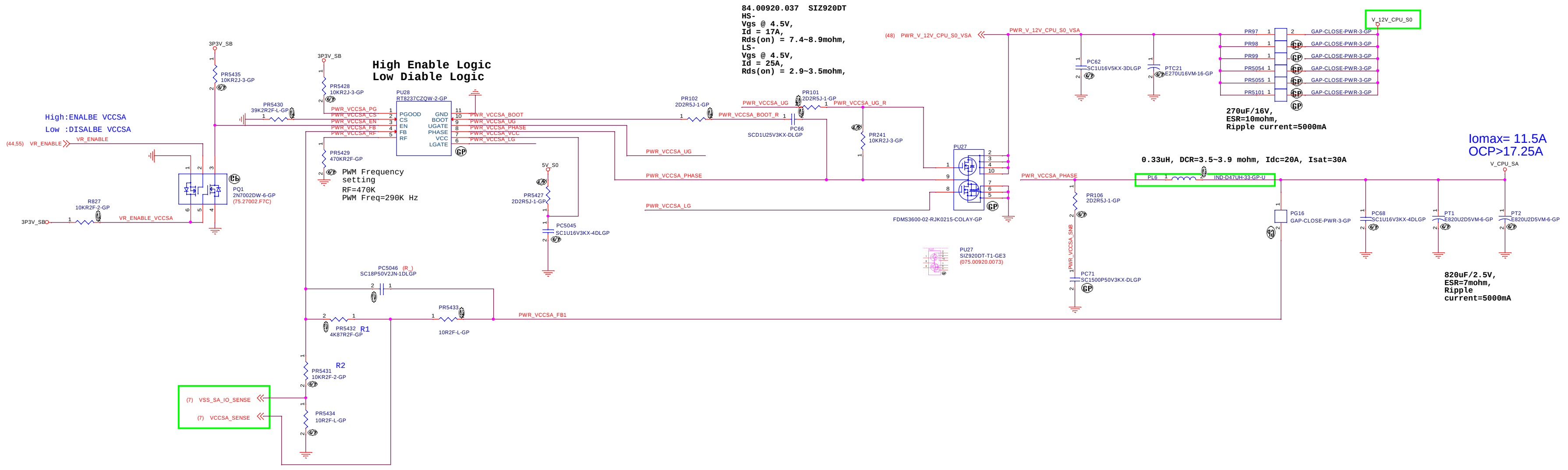

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
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Title: VCCSA(NCP1589D)

Size	Document Number	Rev
D	TAHOE_MT	-1

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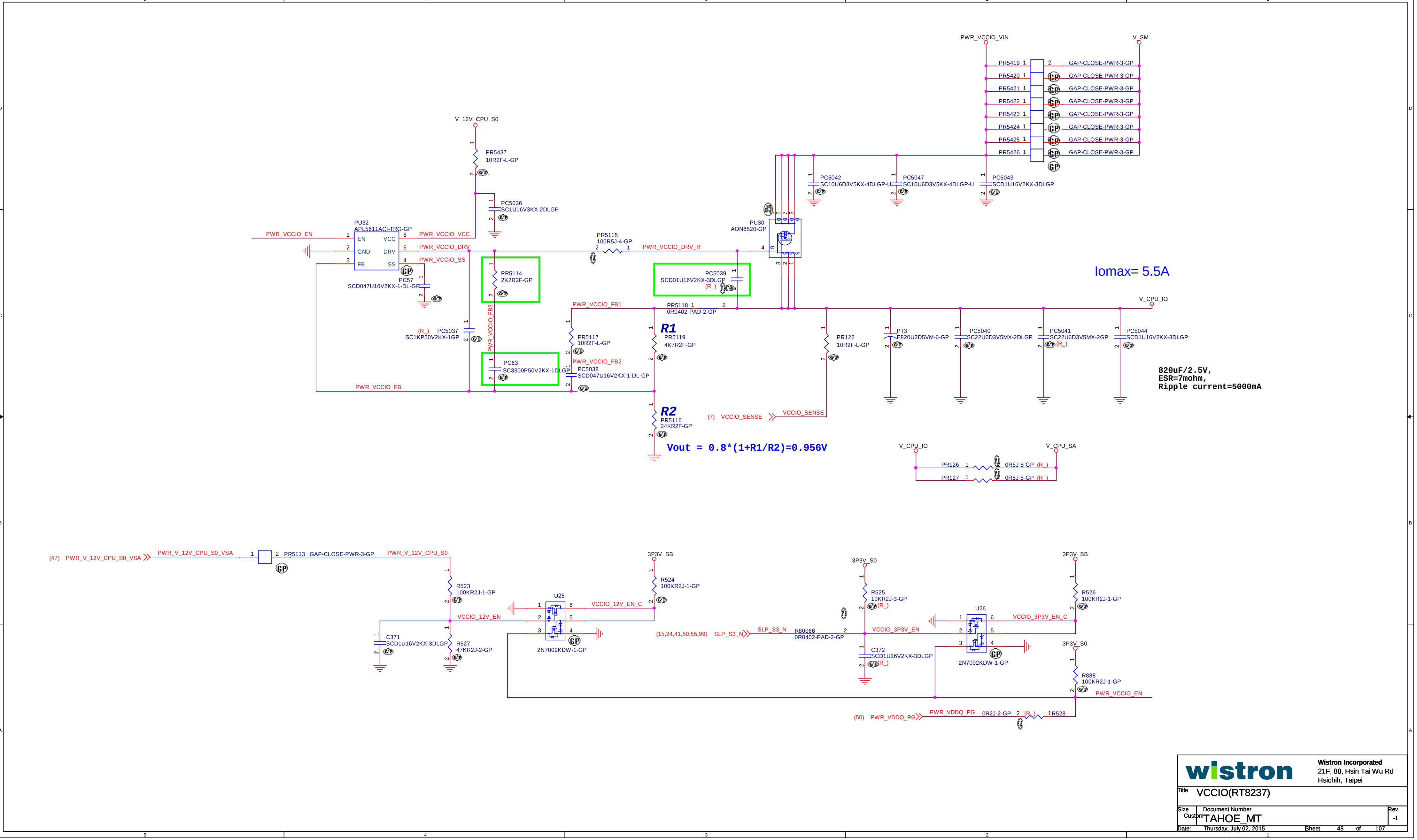

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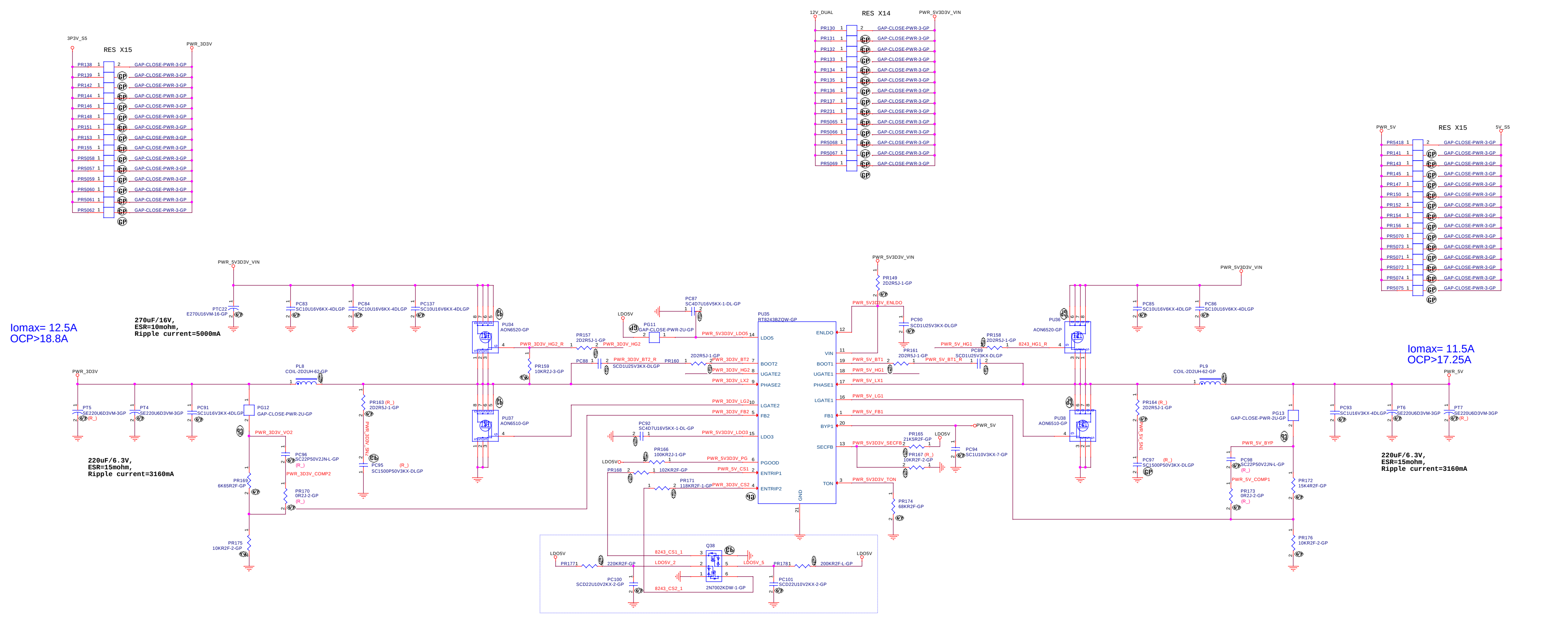
Hsichih, Taipei

Title: VCCIO(RT8237)

Size: Custom | Document Number: TAHOE_MT | Rev: -1

Date: Thursday, July 02, 2015 | Sheet 48 of 107



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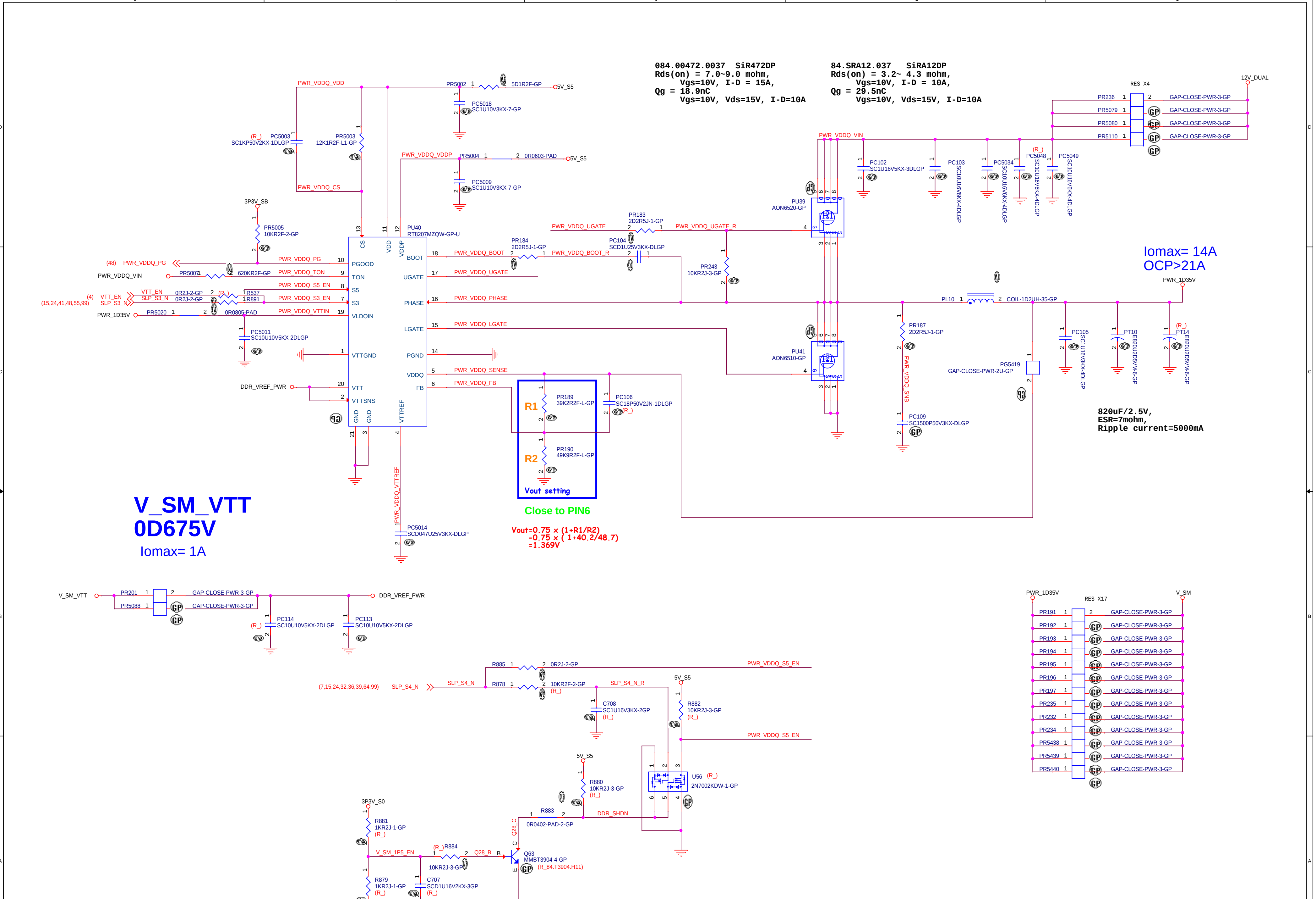
Hsichih, Taipei

Title	5V/3P3V_S5 (RT8243B)	
Size D	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 49 of 107	



wistron

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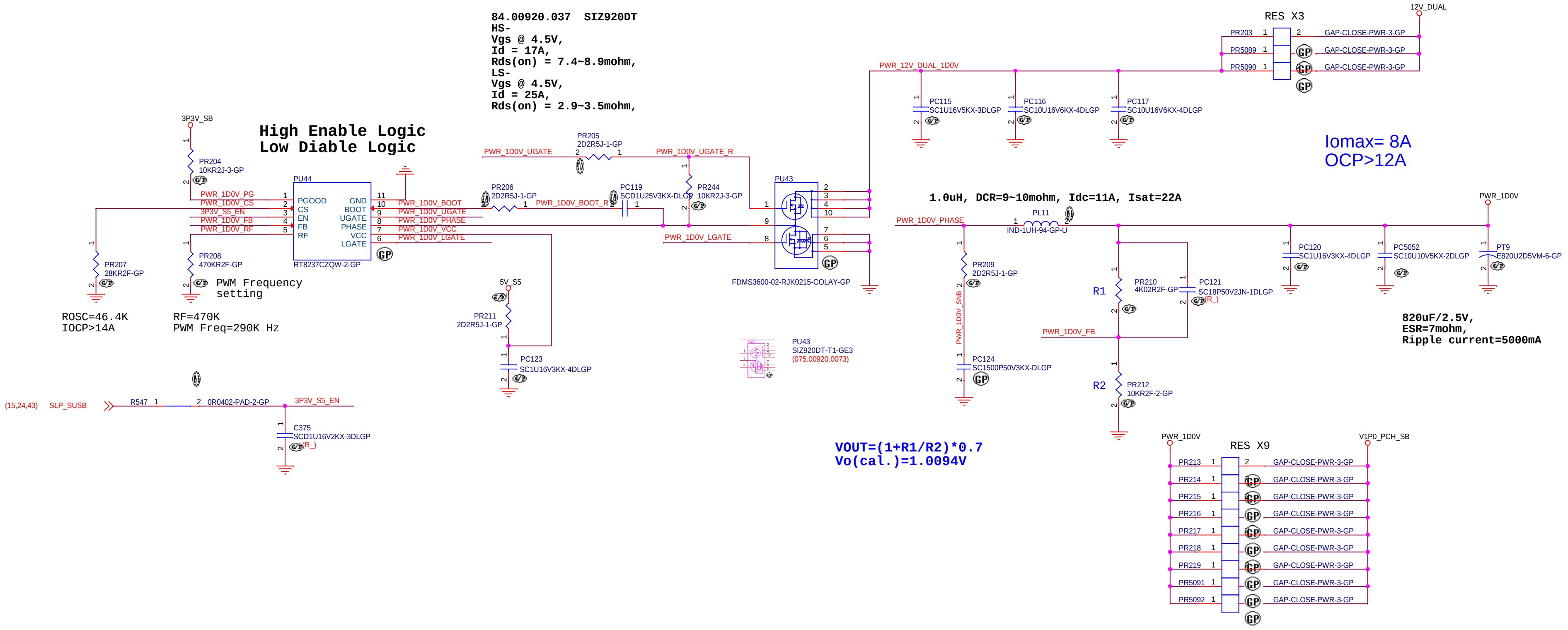
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	DDR PWR(RT8237C)	
Size C	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 50 of 107	



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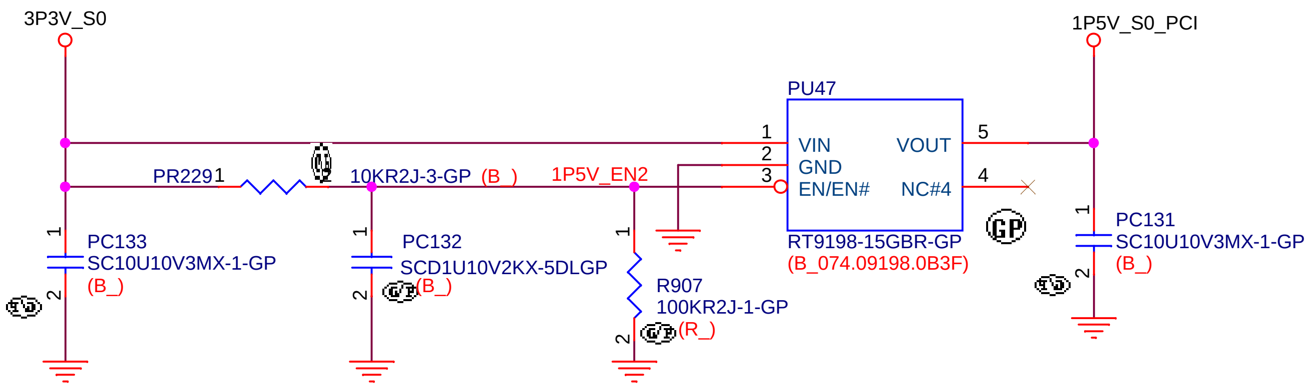
Hsichih, Taipei

Title	PCH 1D0V(RT8237C)		
Size C	Document Number TAHOE_MT		Rev -1
Date: Thursday, July 02, 2015	Sheet 51 of 107		



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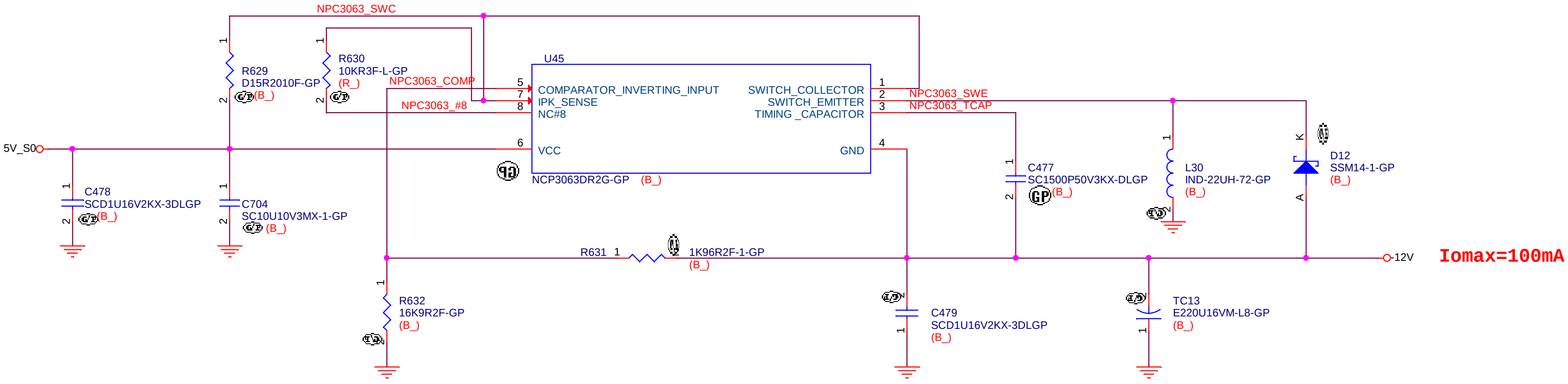
Hsichih, Taipei

Title	1D5V_PCI	
Size A	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 52 of 107	



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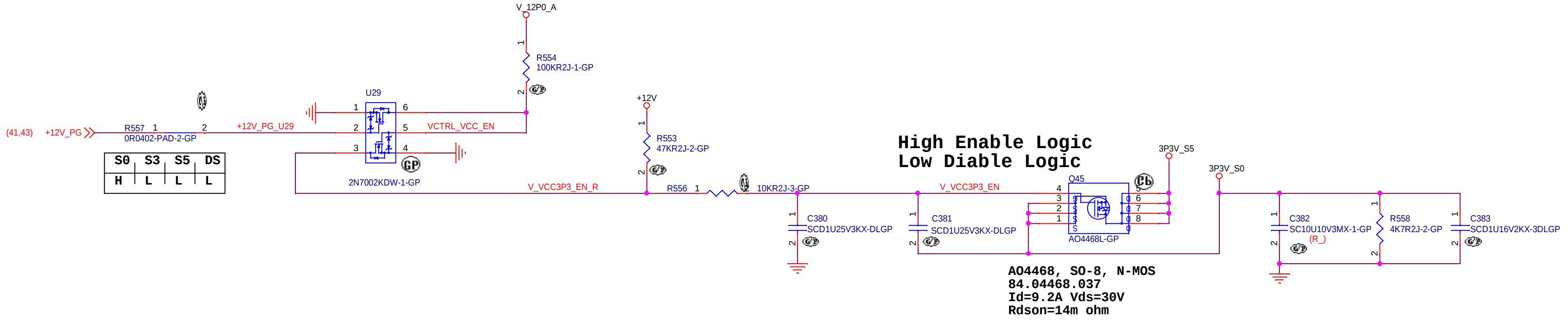
Hsichih, Taipei

Title	MINUS 12V (NCP3063)	
Size B	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 53 of 107	



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Title	5V/3P3V_S0	
Size: C	Document Number: TAHOE_MT	Rev: -1
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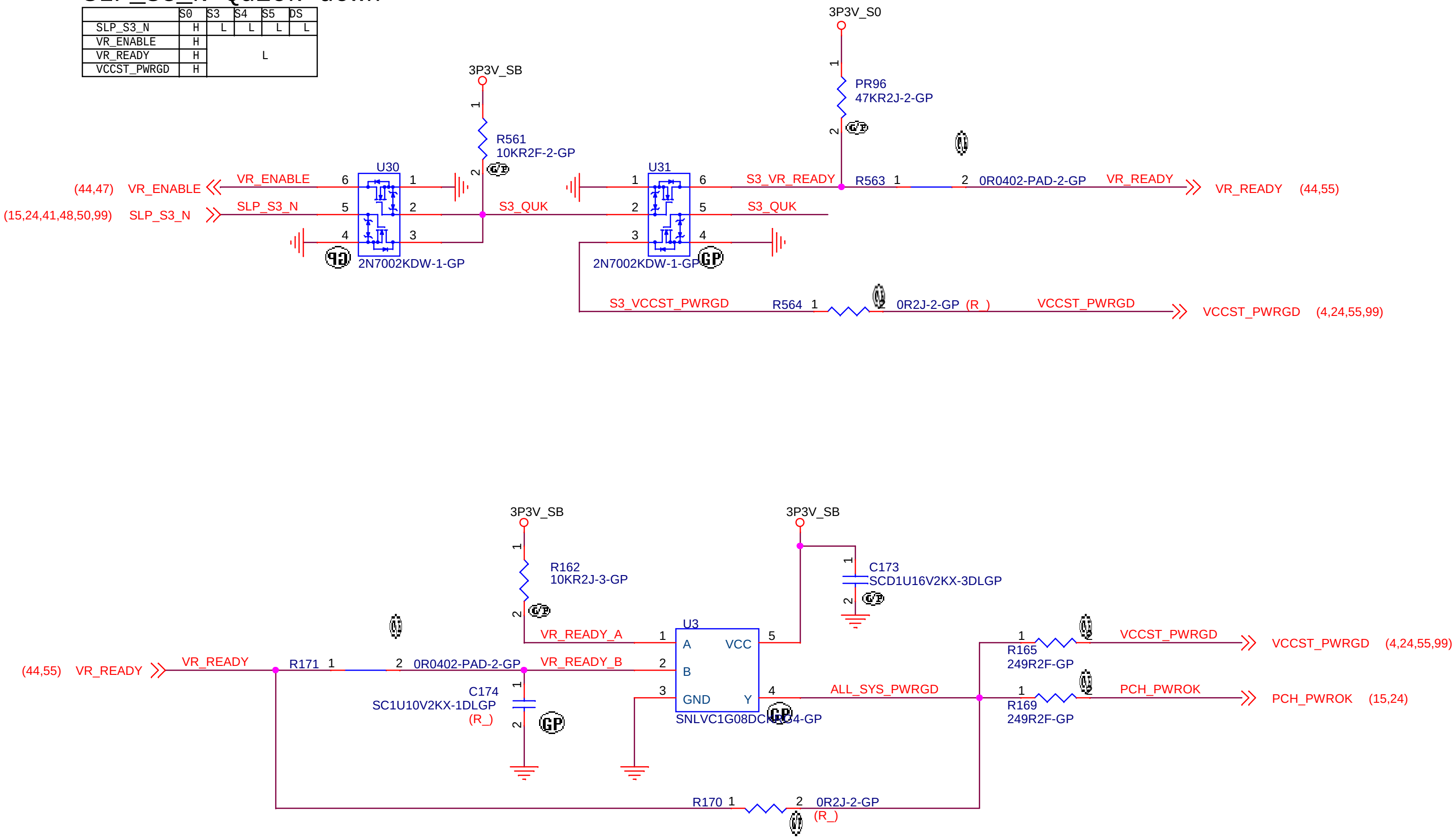
SLP_S3_N Quick down

	S0	S3	S4	S5	DS
SLP_S3_N	H	L	L	L	L
VR_ENABLE	H	L			
VR_READY	H				
VCCST_PWRGD	H				



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Hsichih, Taipei

Title: Sequence Circuit

Size	Document Number	Rev
B	TAHOE_MT	-1

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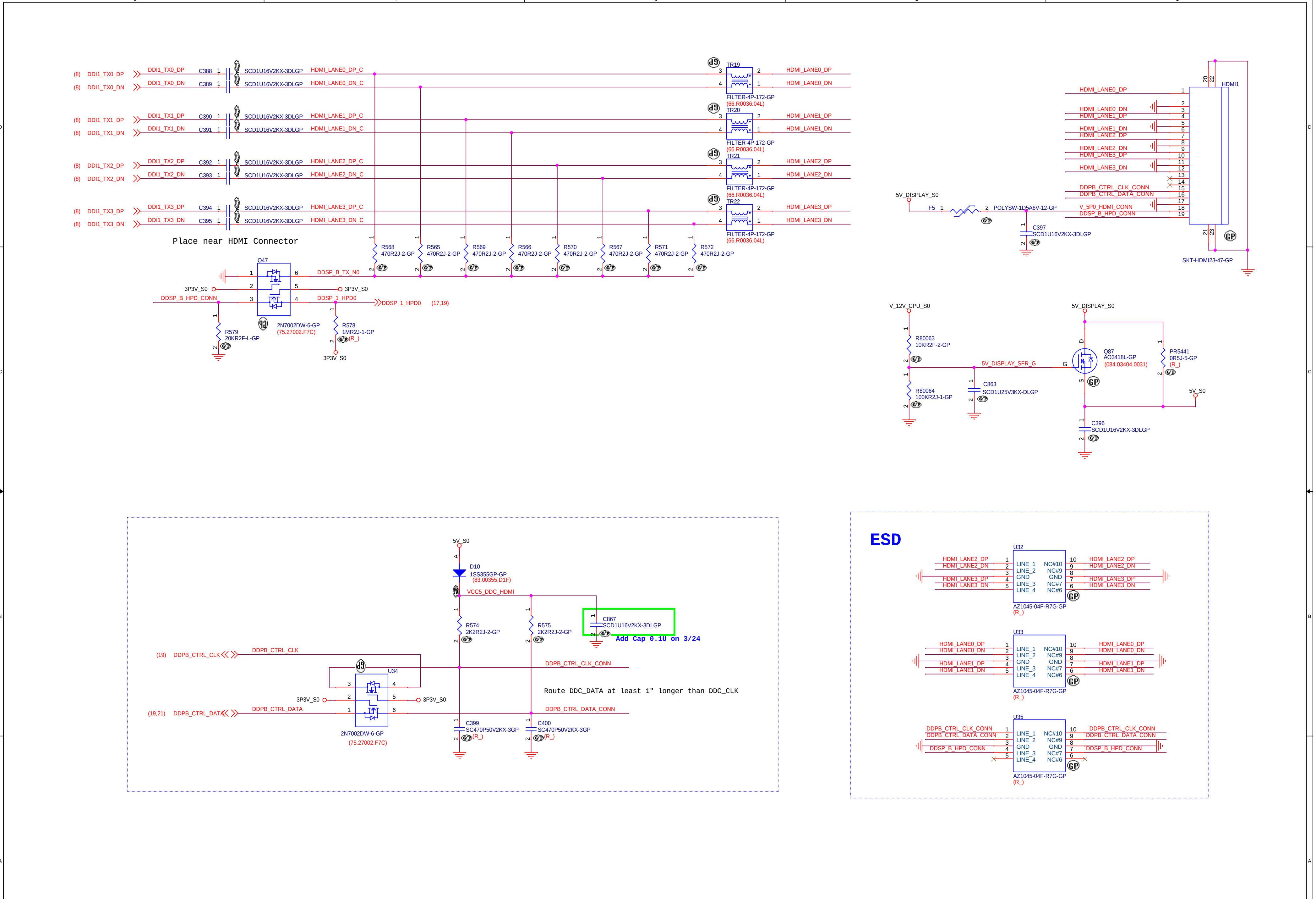

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Hsichih, Taipei

Title	HDMI(Input)	
Size C	Document Number TAHOE_MT	Rev -1
Date: Wednesday, July 08, 2015	Sheet 56 of 107	

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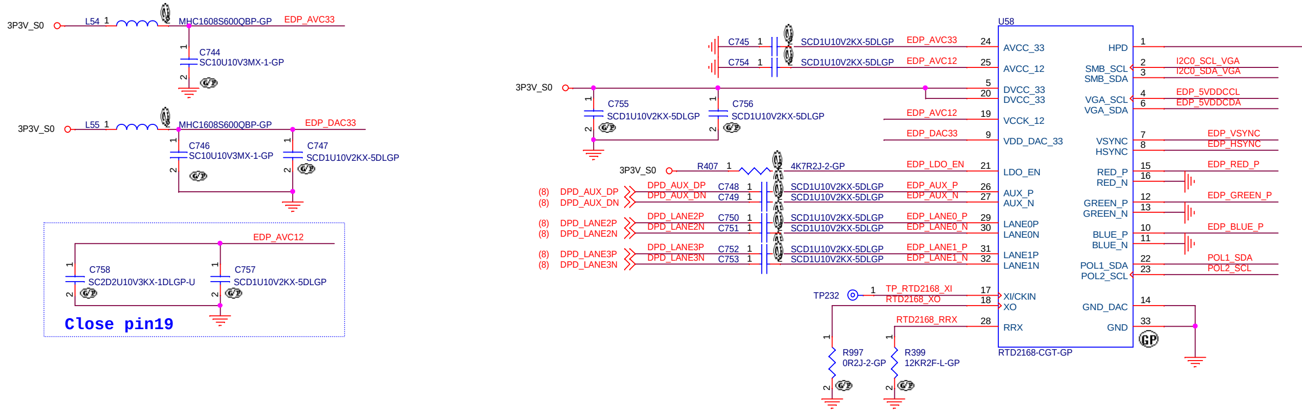
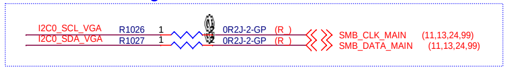
Hsichih, Taipei

Title	Disply Port(Input/Output)	
Size C	Document Number TAHOE_MT	Rev -1
Date: Thursday, July 02, 2015	Sheet 57 of 107	

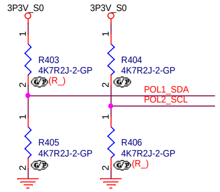


For EP Mode Debug



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

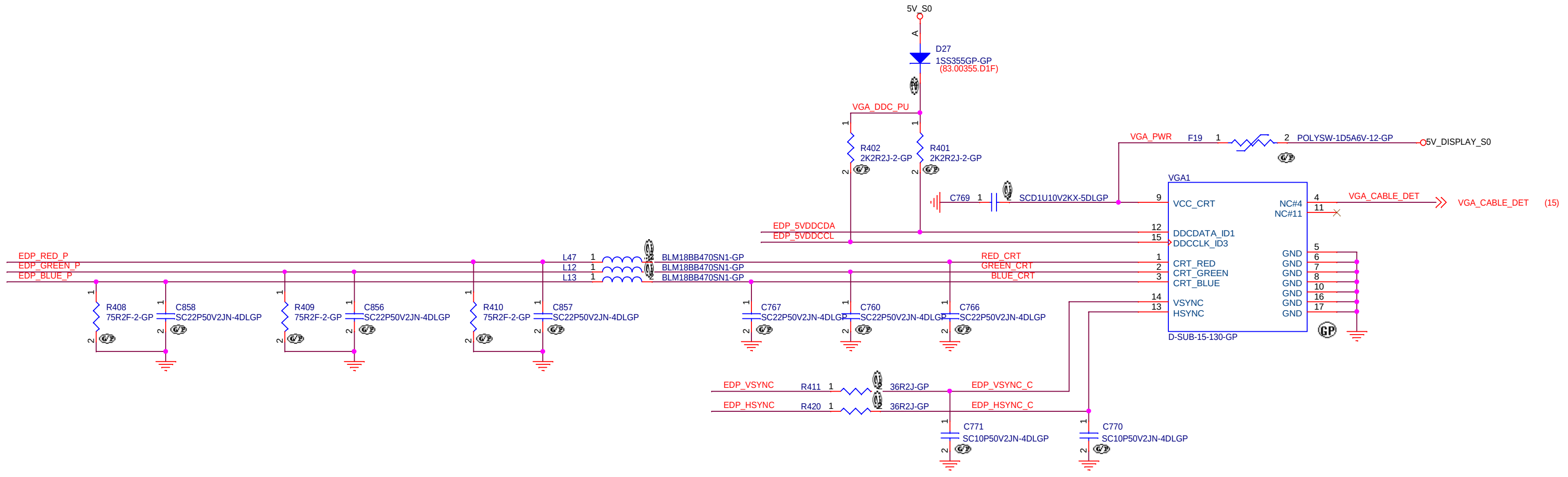


EP Mode

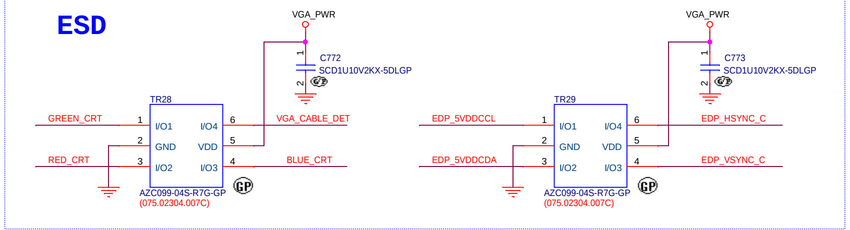
RTD2168 Slave Address:
0x64/0x65

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high



ESD



wistron

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Title	Edp to VGA pin header		
Size: C	Document Number: TAHOE_MT		Rev: -1
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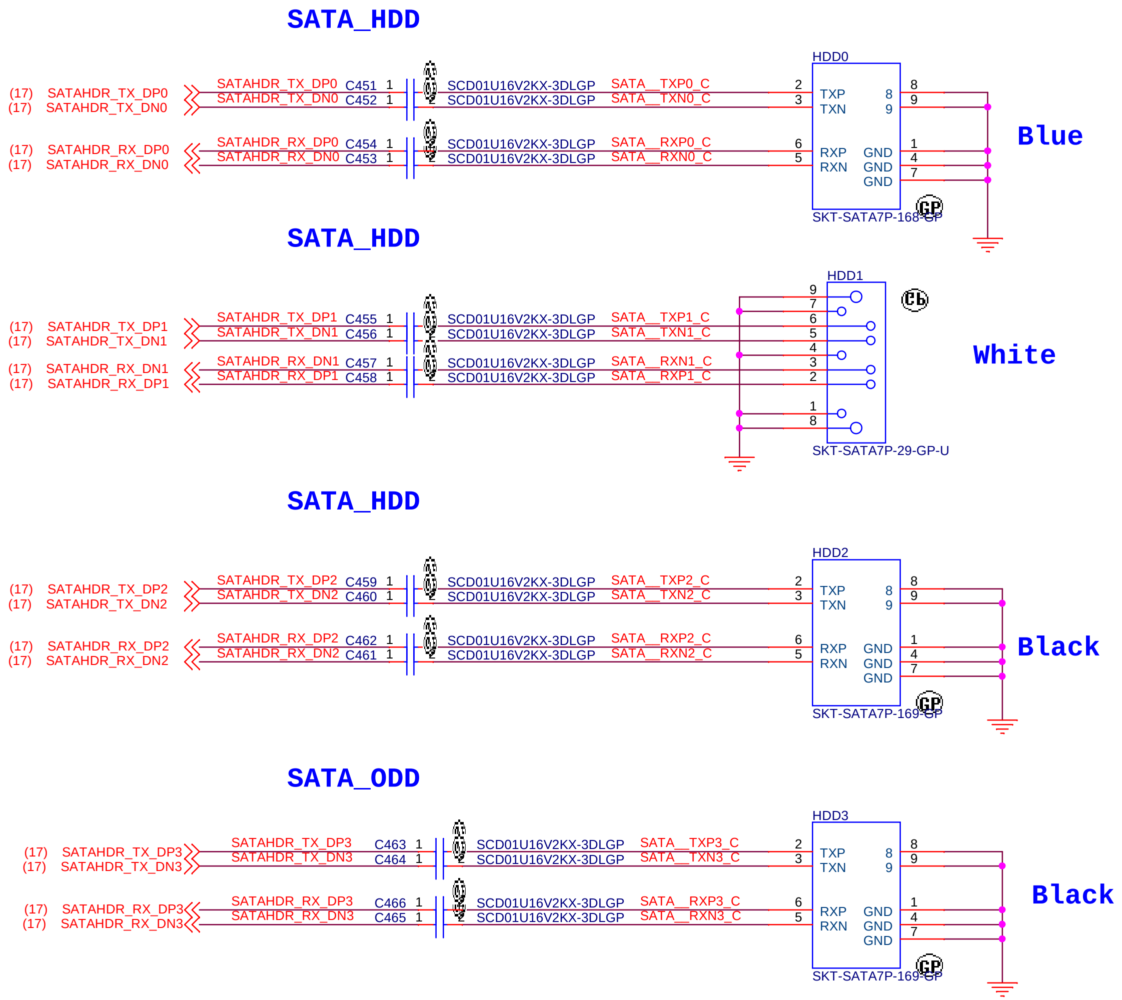
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	Reserved	
Size A	Document Number TAHOE_MT	Rev -1
Date:	Thursday, July 02, 2015	Sheet 59 of 107



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	HDD/ODD	
Size B	Document Number TAHOE_MT	Rev -1
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wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	CLINK/BT Header
Size: Custom	Document Number: TAHOE_MT
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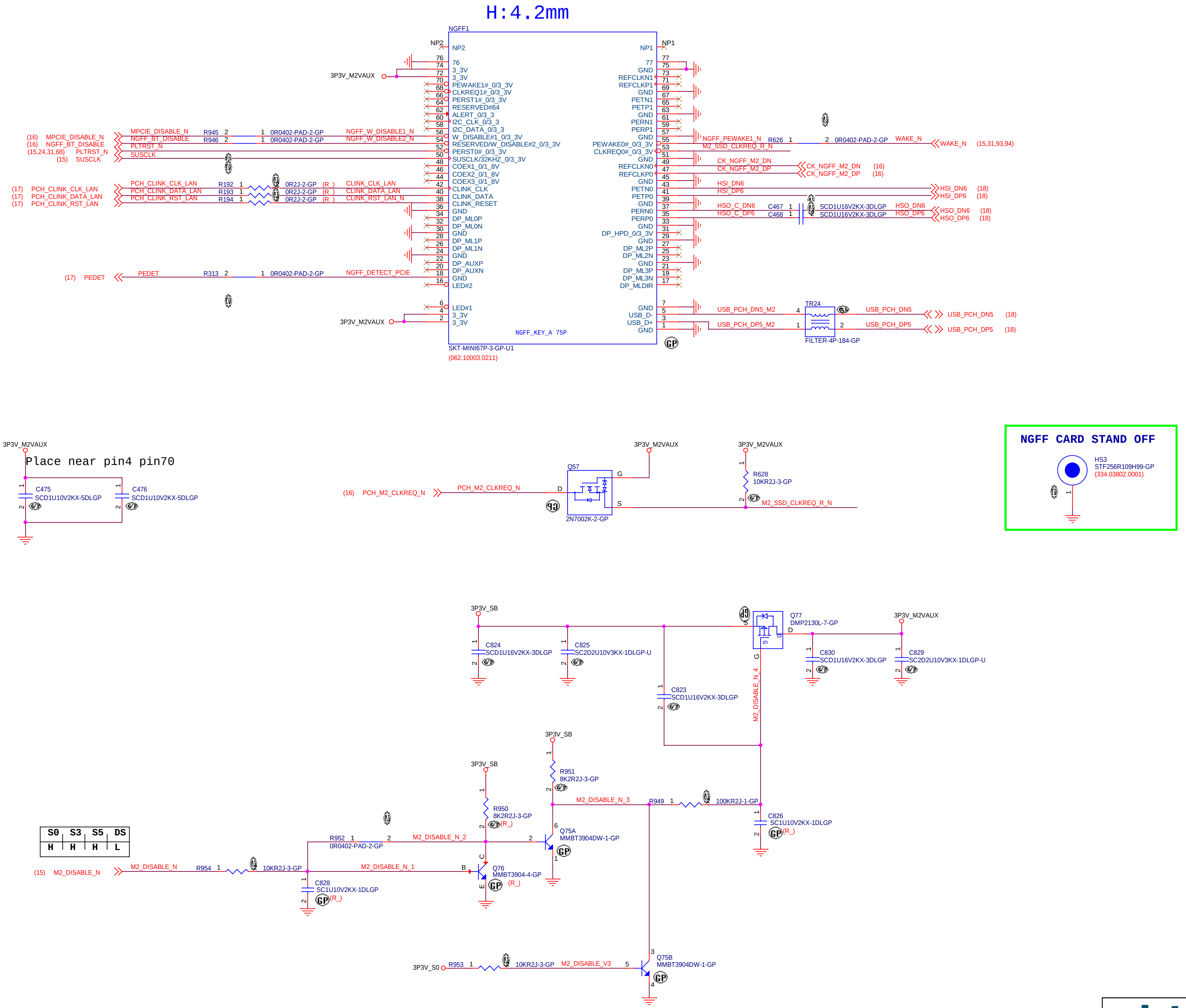

S0	S3	S5	DS
H	H	H	L

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Title: M2_SSD

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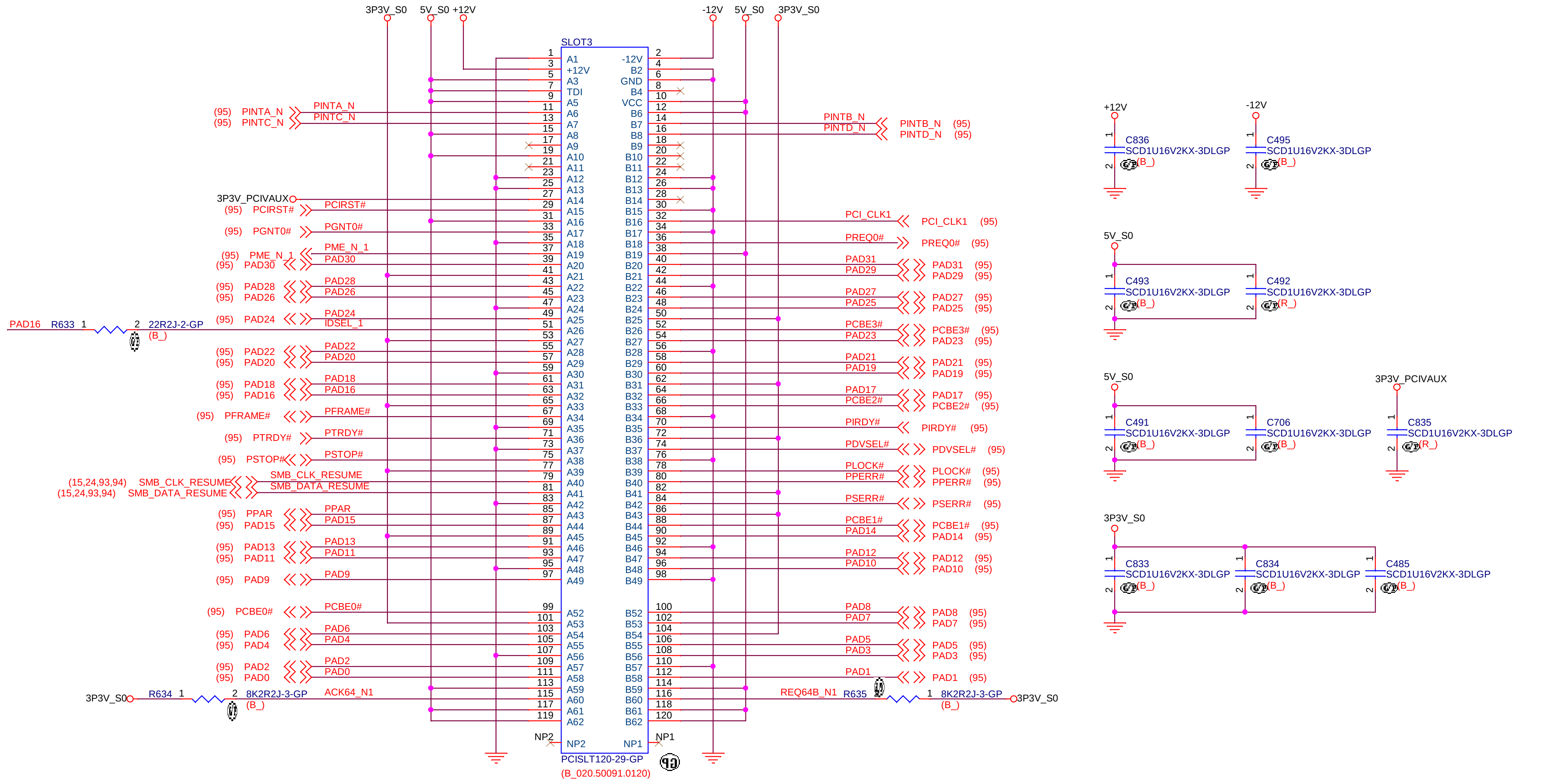

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Title
PCI Slot

Size	Document Number	Rev
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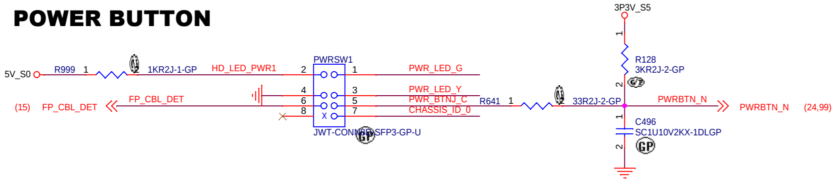
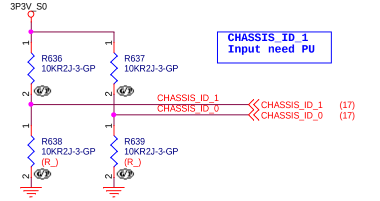
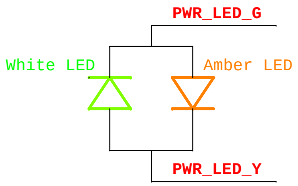
POWER BUTTON



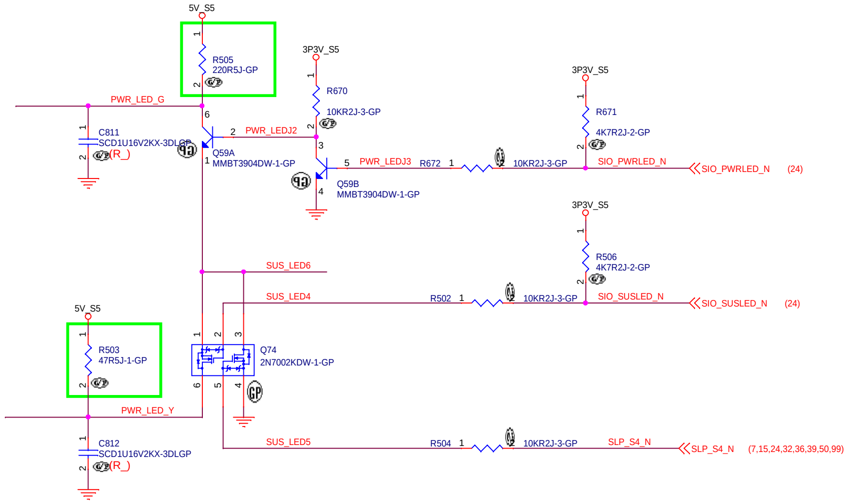
CHASSIS ID

TYPE	ID_0
Inspiron	1
Vostro	0



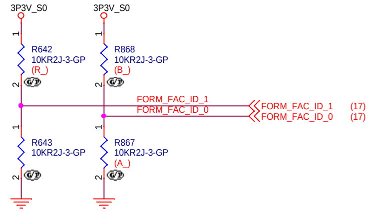


S0	White
S3	White(blinking)
S4/S5	LED off
No Post	Amber
Failure to Post	Amber(blinking)



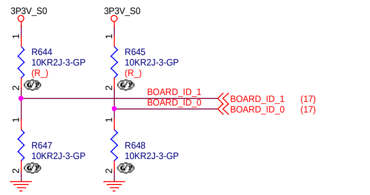
SKU ID

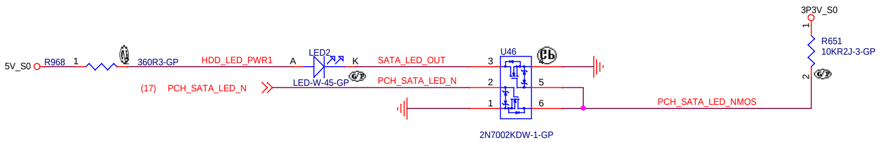
TYPE	ID_1	ID_0
Tahoe/Lotus MT	0	0
Tahoe CBB MT	0	1
Tahoe/Lotus SFF	1	0
TBD	1	1

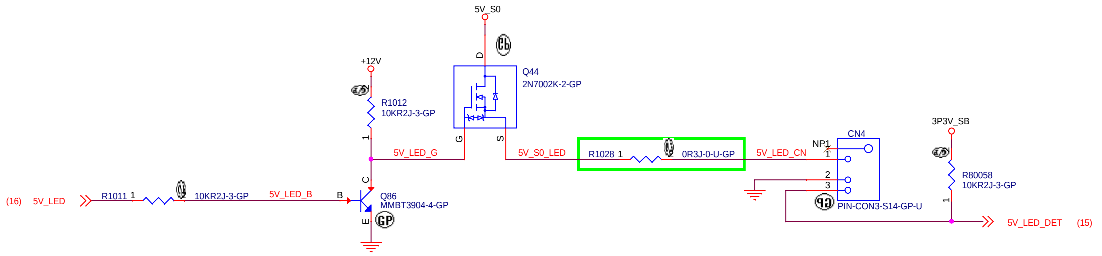


BOARD ID

TYPE	ID_1	ID_0
X00	0	0
X01	0	1
	1	0
	1	1







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Title: PWR Button/LED

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Title			
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wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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wistron		**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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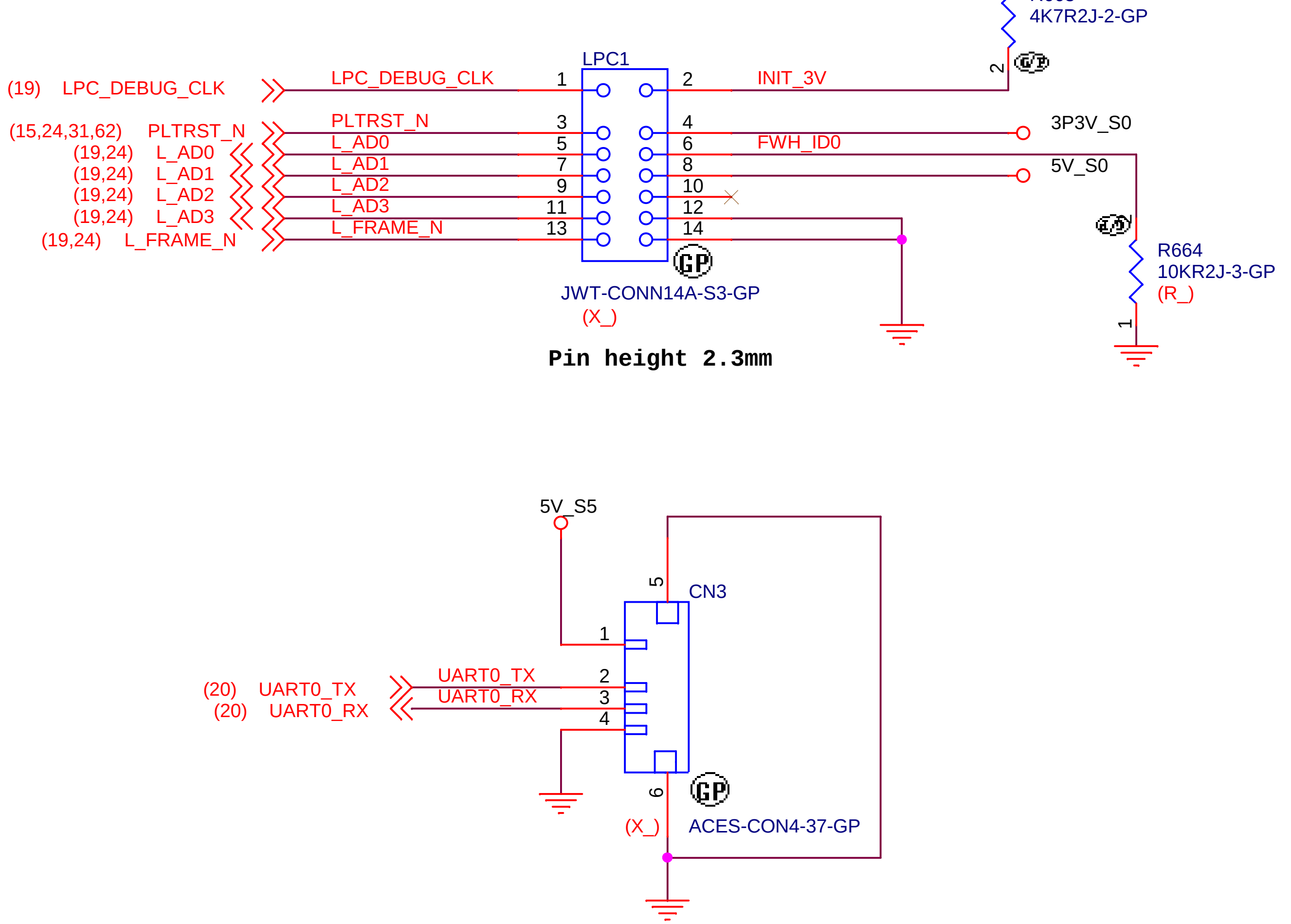
LPC DEBUG PORT



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wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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Wistron Incorporated
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Title: Reserved

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Rev: -1

Date: Thursday, July 02, 2015

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PU for I2CC

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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Title: Reserved

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wistron	**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	TPM
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Title	PS2/RS232	
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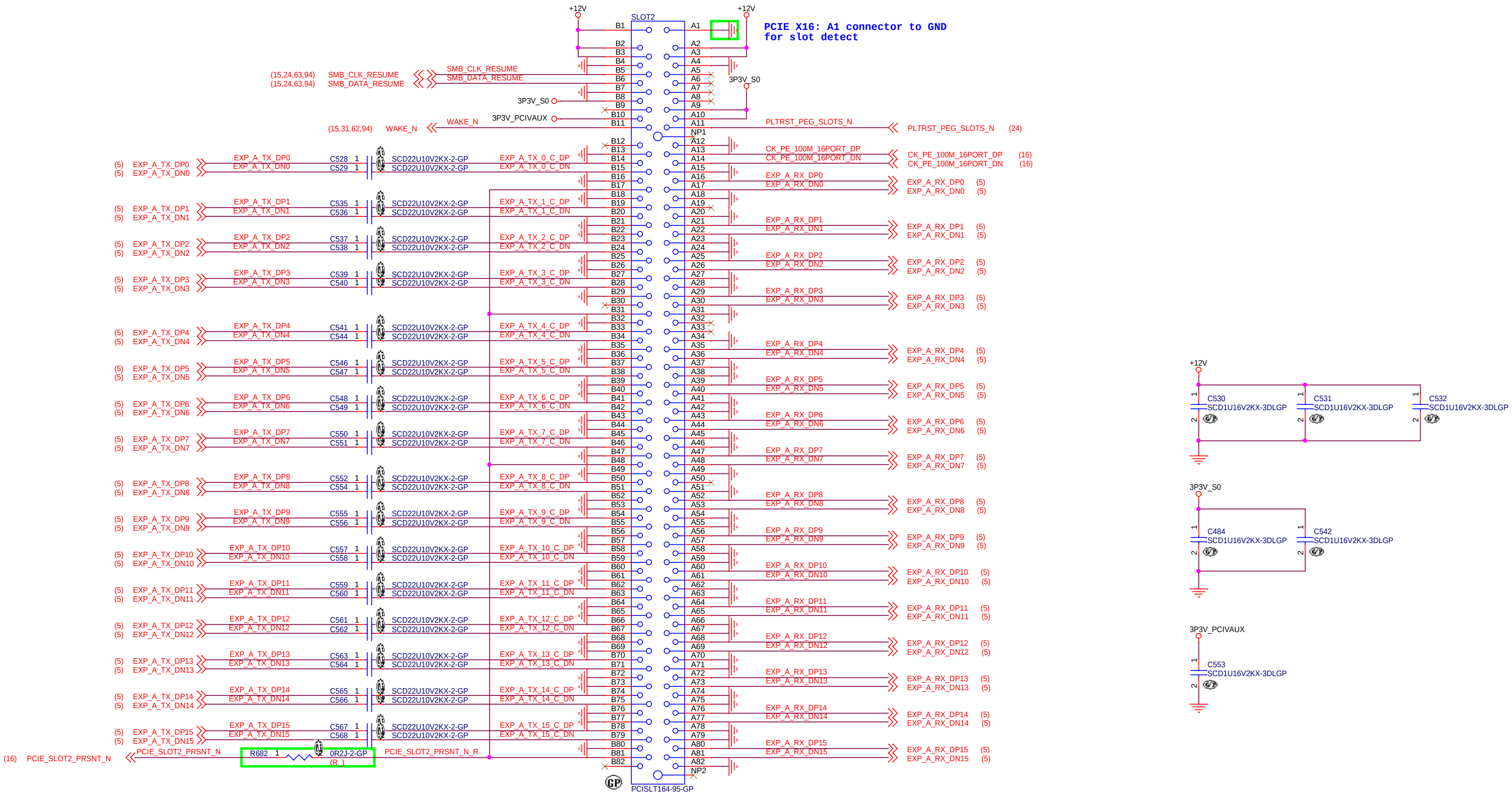

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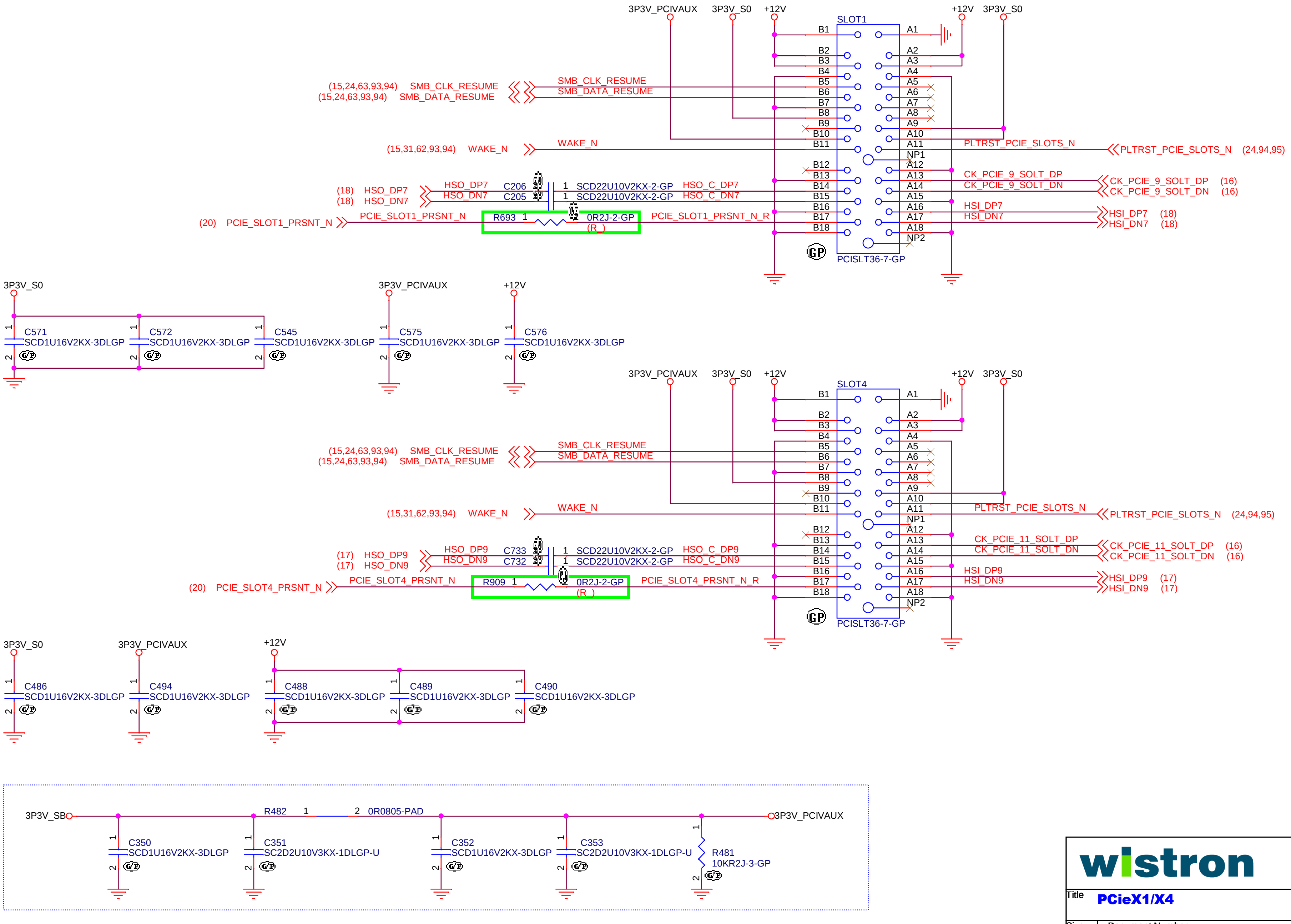

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Title: **PCIeX1/X4**

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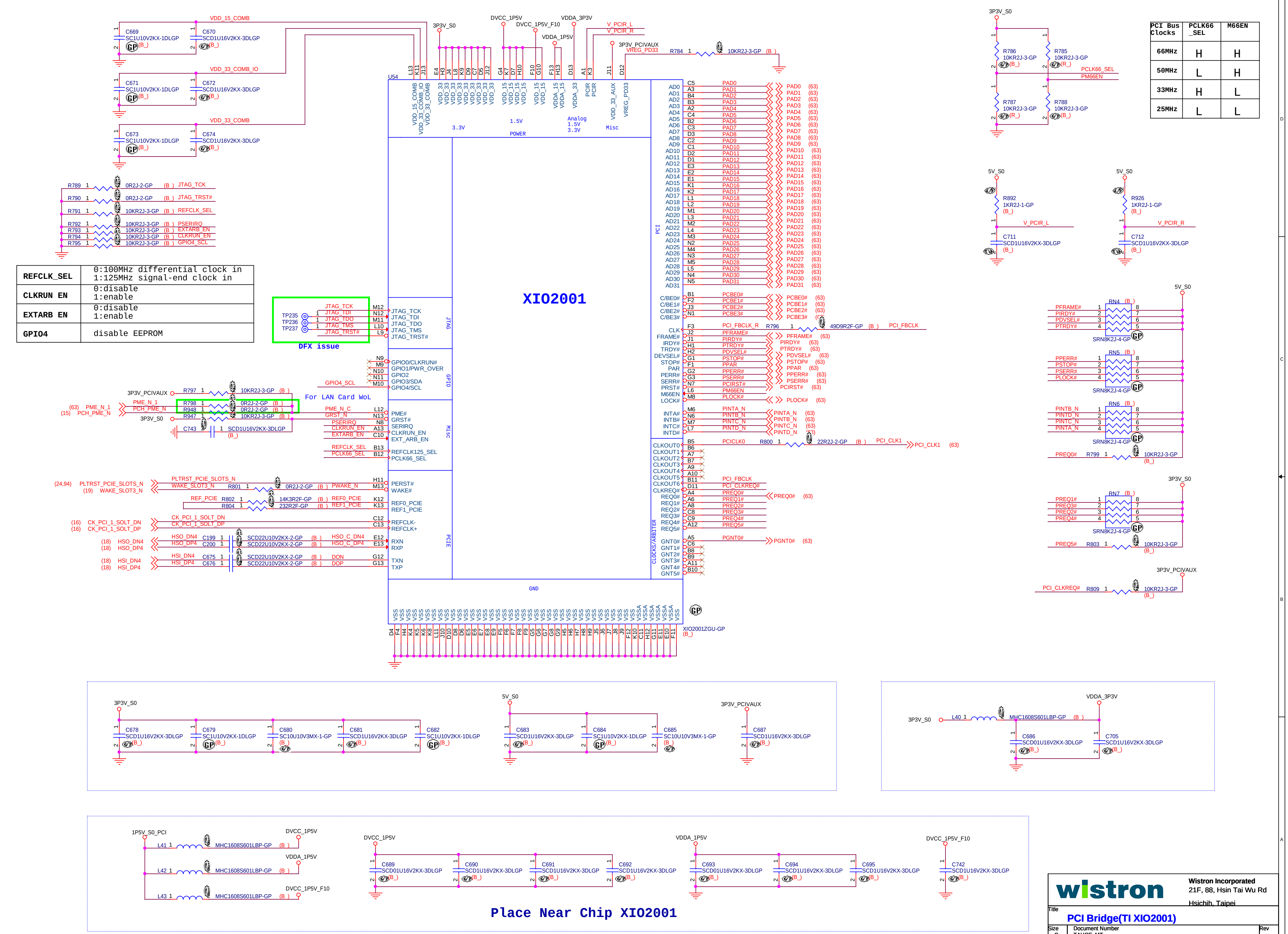

PCI Bus Clocks	PCLK66 _SEL	M66EN
66MHz	H	H
50MHz	L	H
33MHz	H	L
25MHz	L	L

REFCLK_SEL	0:100MHz differential clock in 1:125MHz signal-end clock in
CLKRUN EN	0:disable 1:enable
EXTARB EN	0:disable 1:enable
GPIO4	disable EEPROM

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Title
PCI Bridge(TI XIO2001)

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wistron		**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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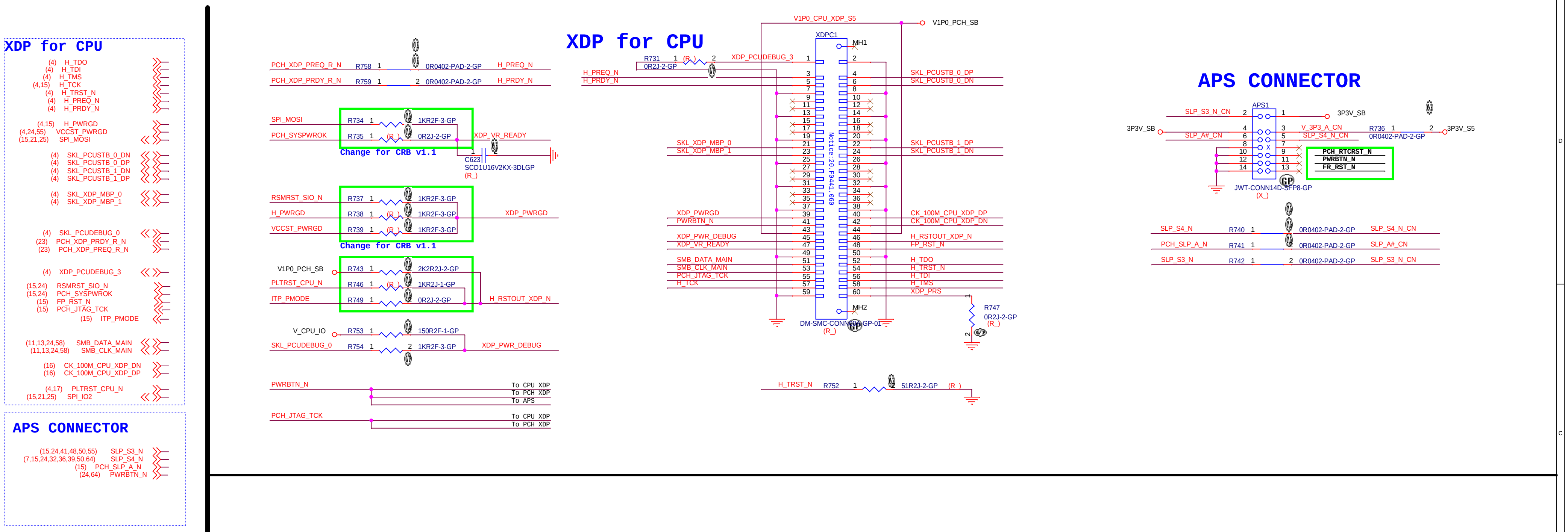
XDP for CPU

APS CONNECTOR



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Title	XDP/80 PORT HEADER/APS	
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wistron		**Wistron Incorporated** 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title		
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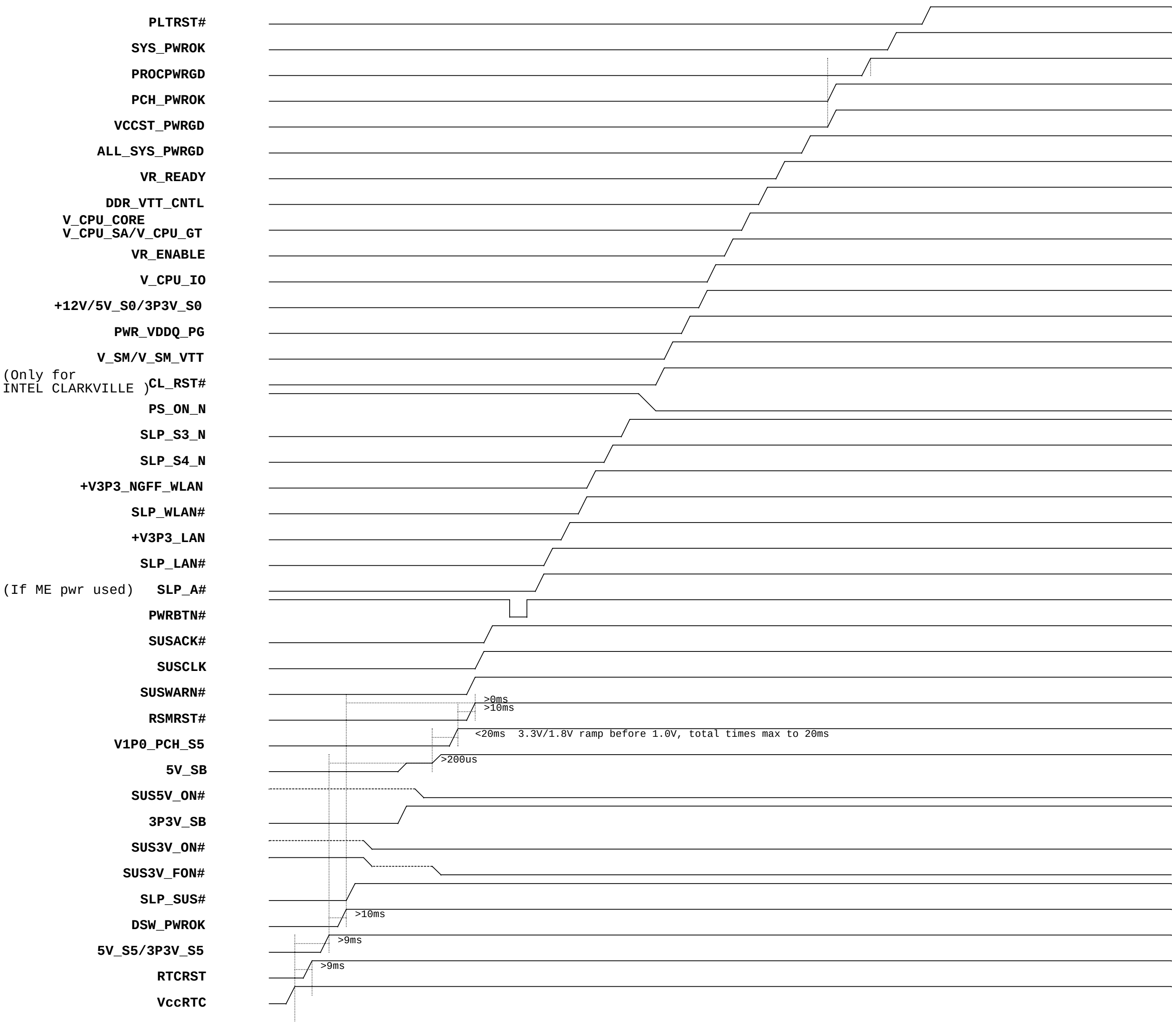
POWER ON SEQUENCE



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Title: Power Sequence		
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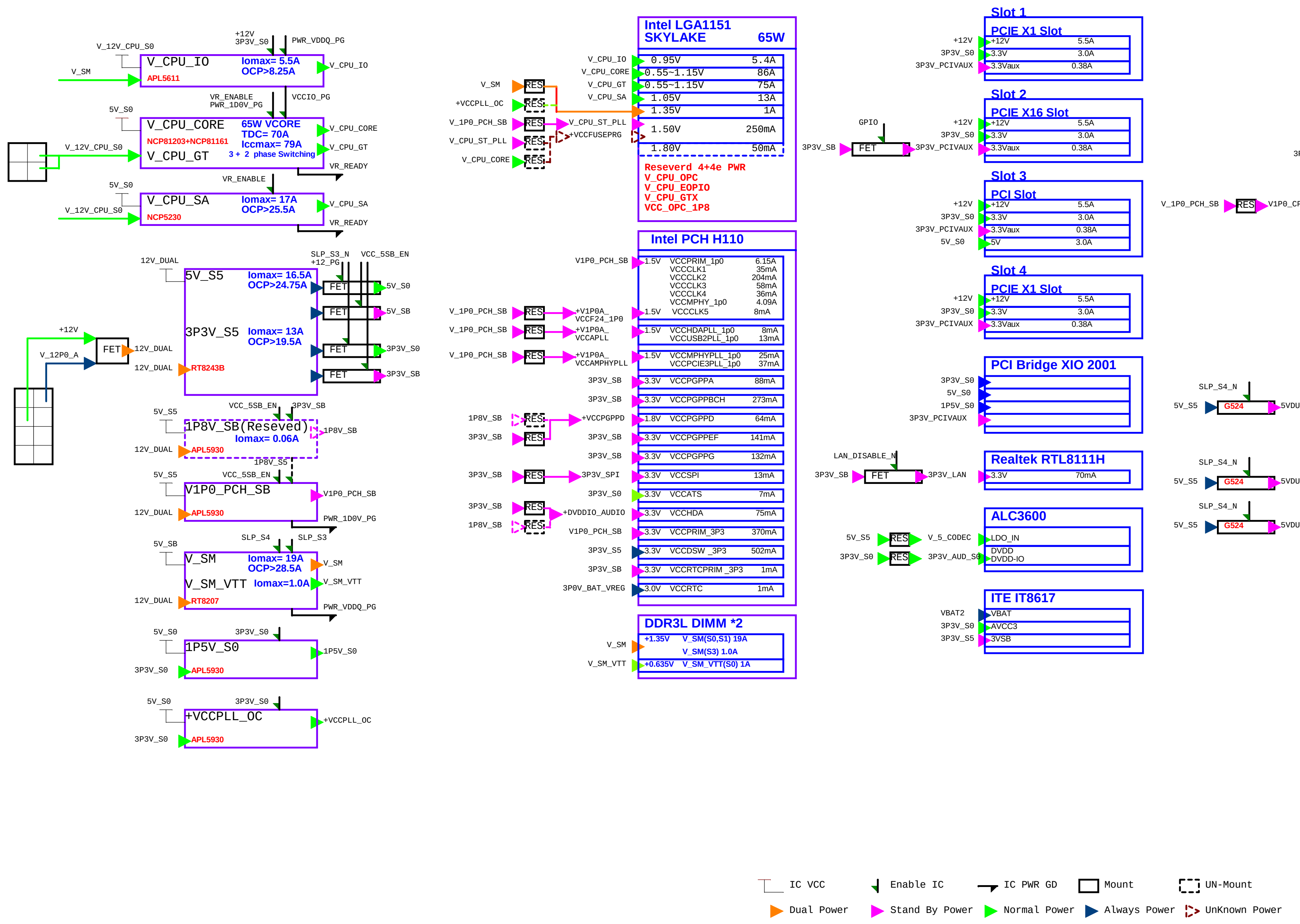

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Title: Power Delivery

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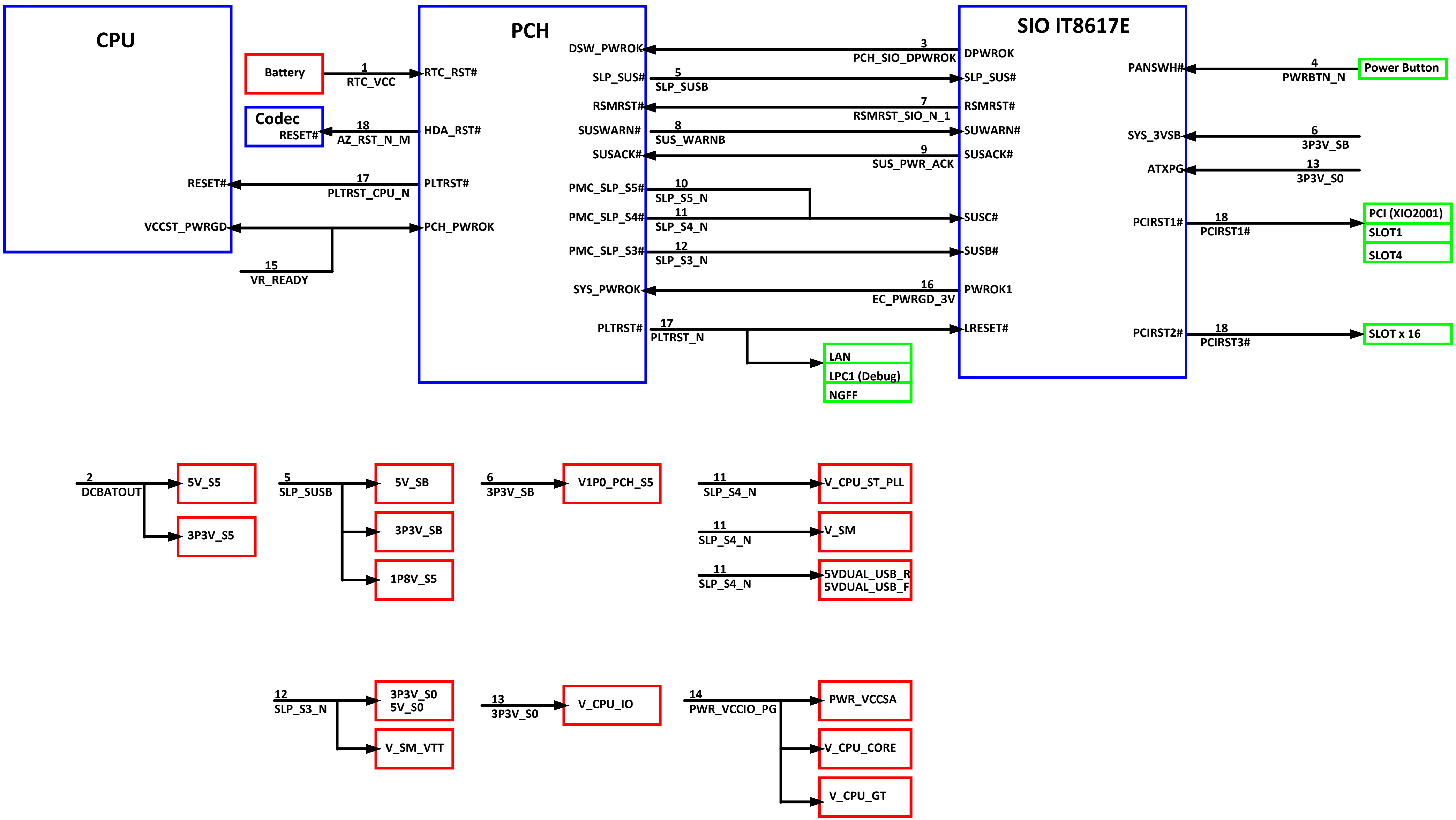

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Title: Power Good & Reset Diagram

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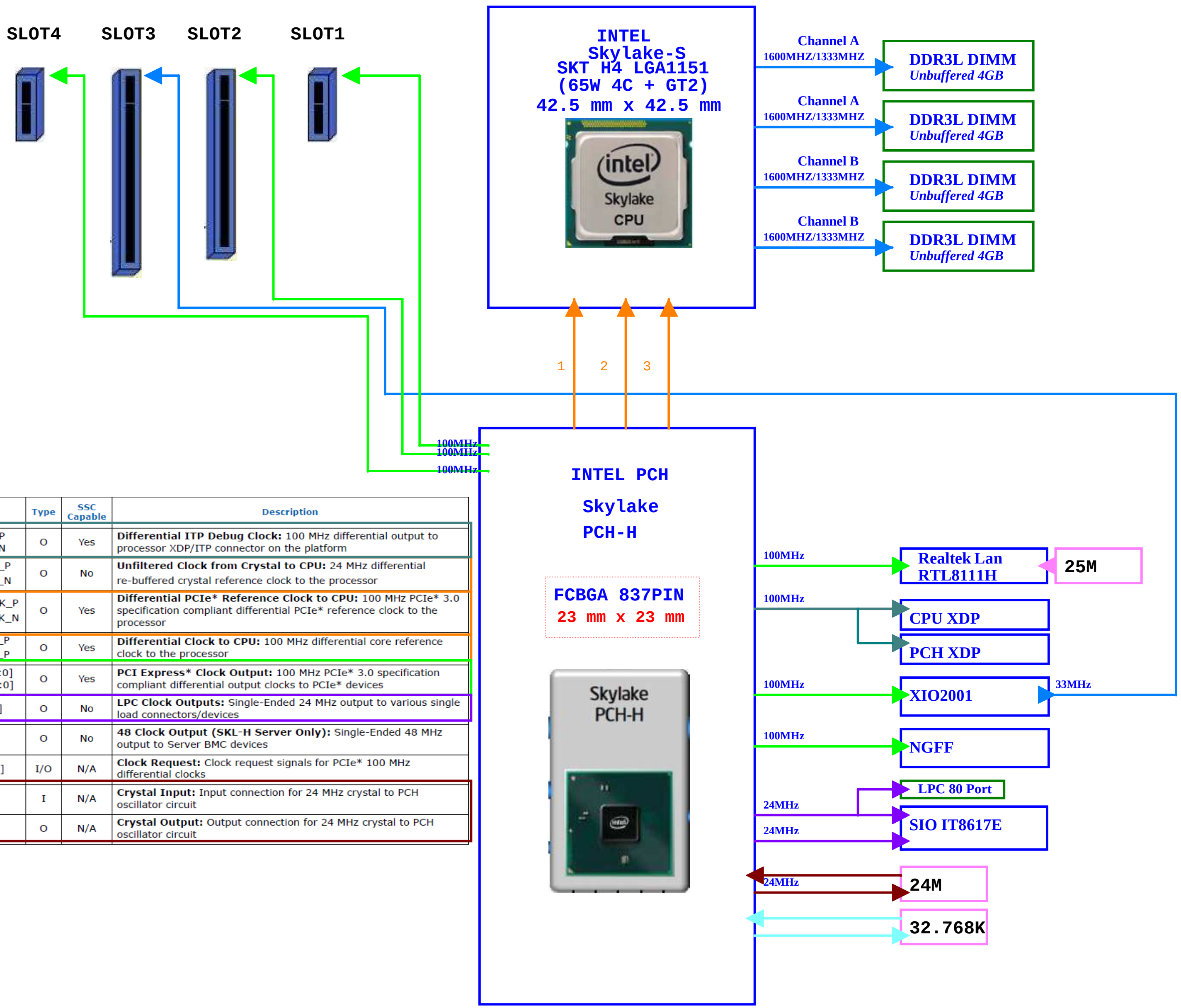

	Name	Type	SSC Capable	Description
	CLKOUT_ITPXDP_P CLKOUT_ITPXDP_N	O	Yes	**Differential ITP Debug Clock:** 100 MHz differential output to processor XDP/ITP connector on the platform
1	CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N	O	No	**Unfiltered Clock from Crystal to CPU:** 24 MHz differential re-buffered crystal reference clock to the processor
2	CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N	O	Yes	**Differential PCIe* Reference Clock to CPU:** 100 MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor
3	CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_P	O	Yes	**Differential Clock to CPU:** 100 MHz differential core reference clock to the processor
	CLKOUT_SRC_P[15:0] CLKOUT_SRC_N[15:0]	O	Yes	**PCI Express* Clock Output:** 100 MHz PCIe* 3.0 specification compliant differential output clocks to PCIe* devices
	CLKOUT_LPC[1:0]	O	No	**LPC Clock Outputs:** Single-Ended 24 MHz output to various single load connectors/devices
	CLKOUT_48	O	No	**48 Clock Output (SKL-H Server Only):** Single-Ended 48 MHz output to Server BMC devices
	SRCCLKRQ#[15:0]	I/O	N/A	**Clock Request:** Clock request signals for PCIe* 100 MHz differential clocks
	XTAL24_IN	I	N/A	**Crystal Input:** Input connection for 24 MHz crystal to PCH oscillator circuit
	XTAL24_OUT	O	N/A	**Crystal Output:** Output connection for 24 MHz crystal to PCH oscillator circuit

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Title: REST Flow Chart

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Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
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