Foxconn Precision Co. Inc.
G31M04 Schematic

Fab.A
Data: 2007/6/15

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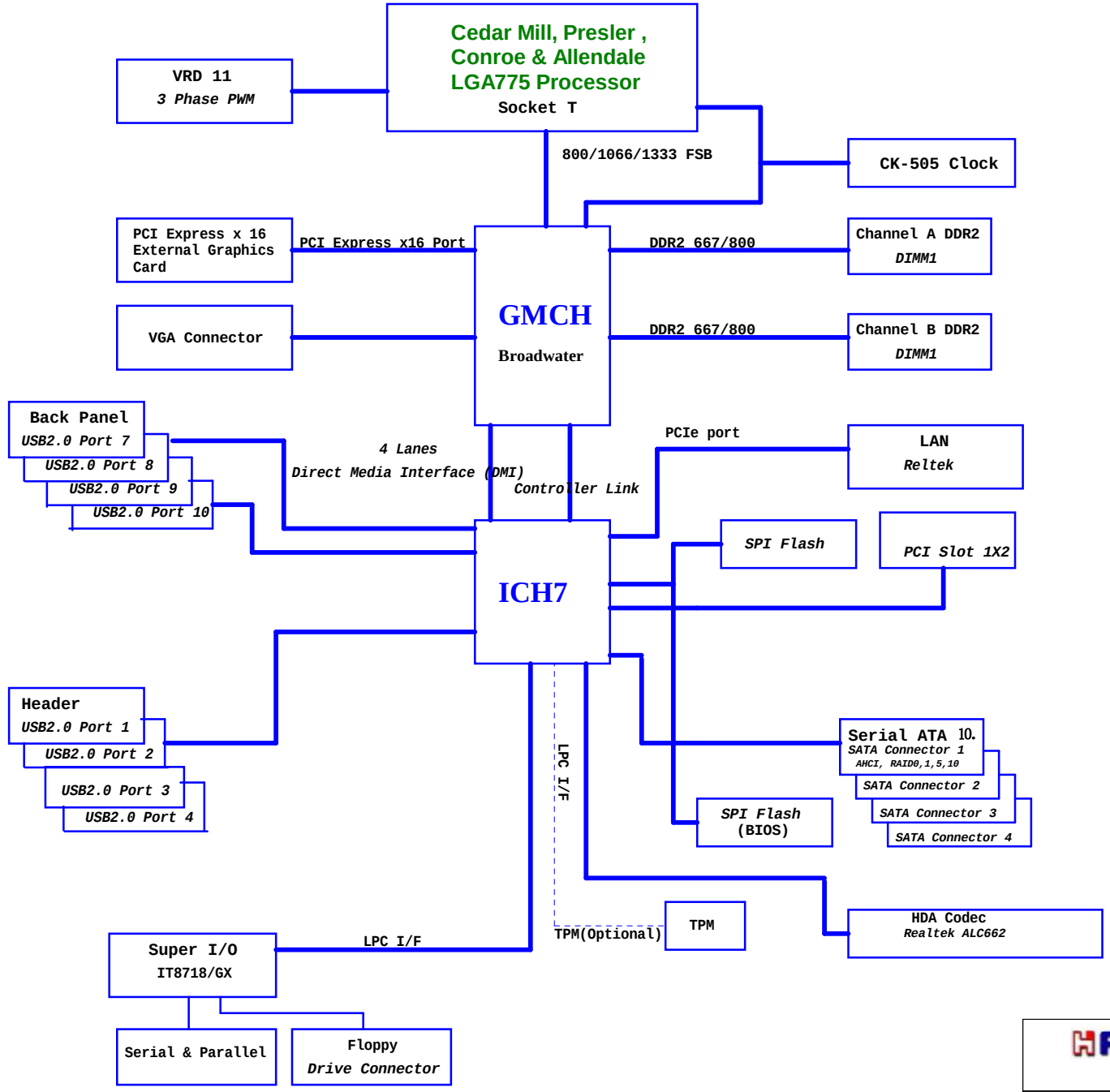

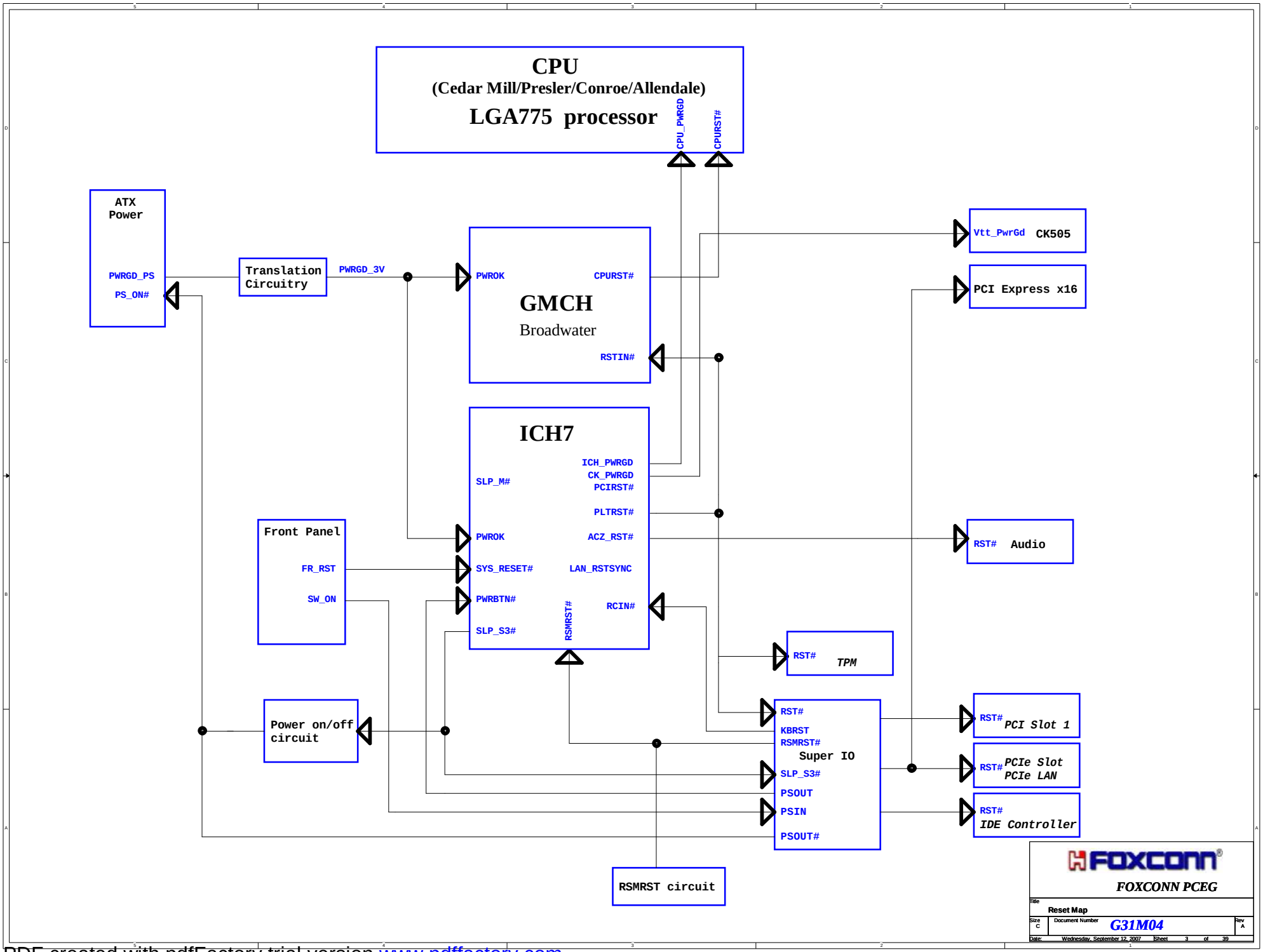

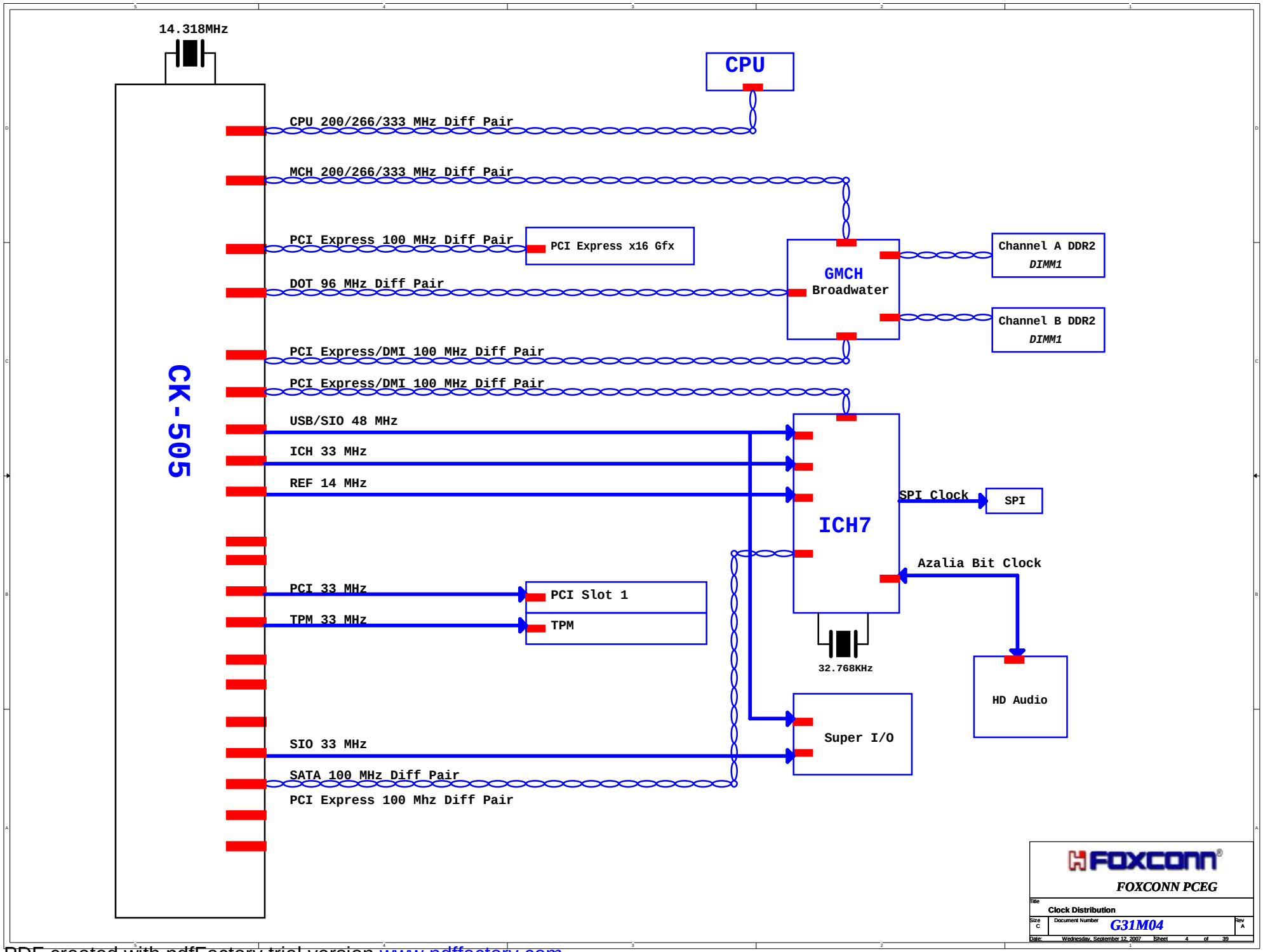

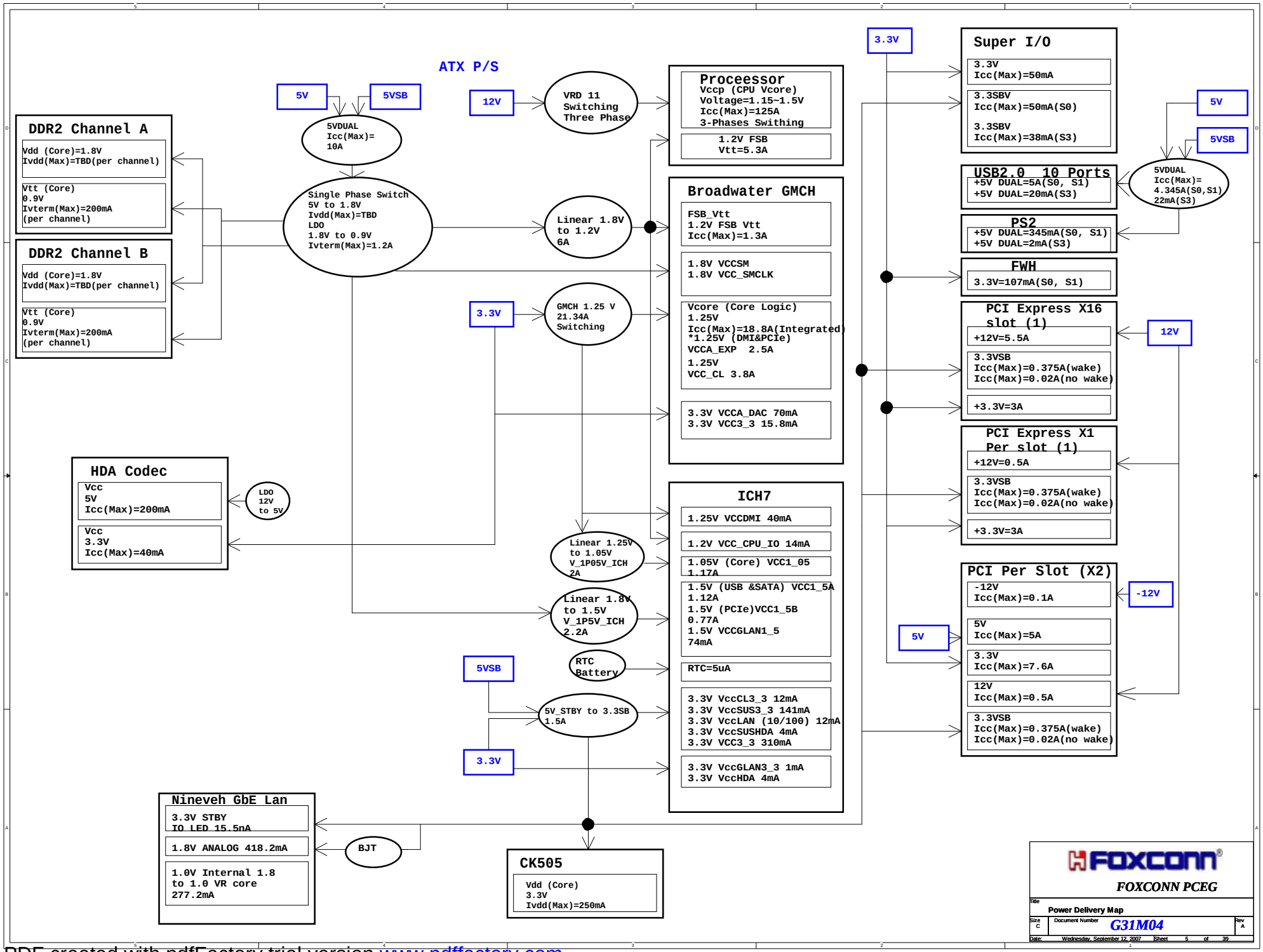

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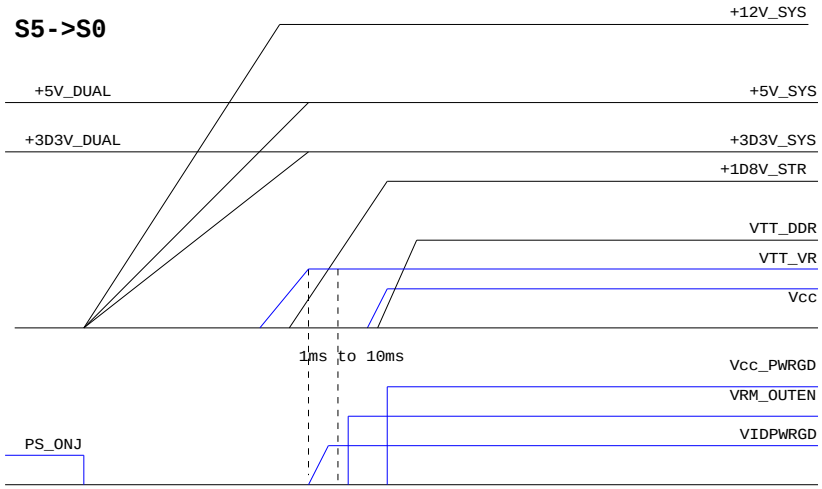

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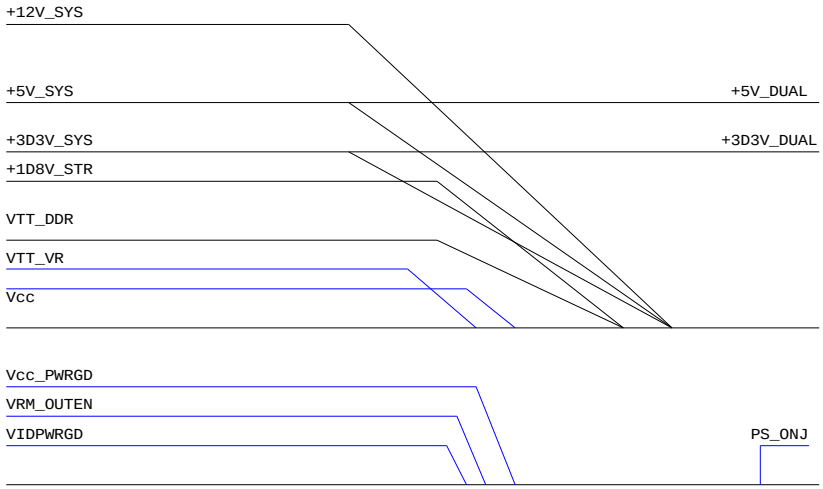

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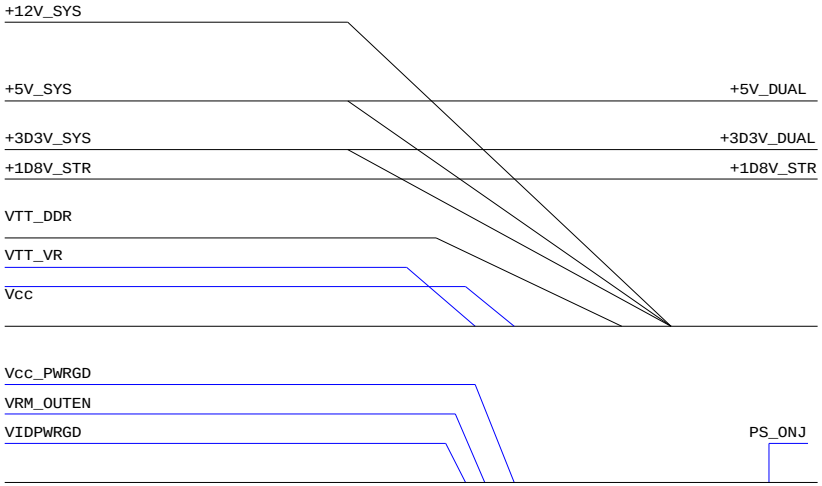

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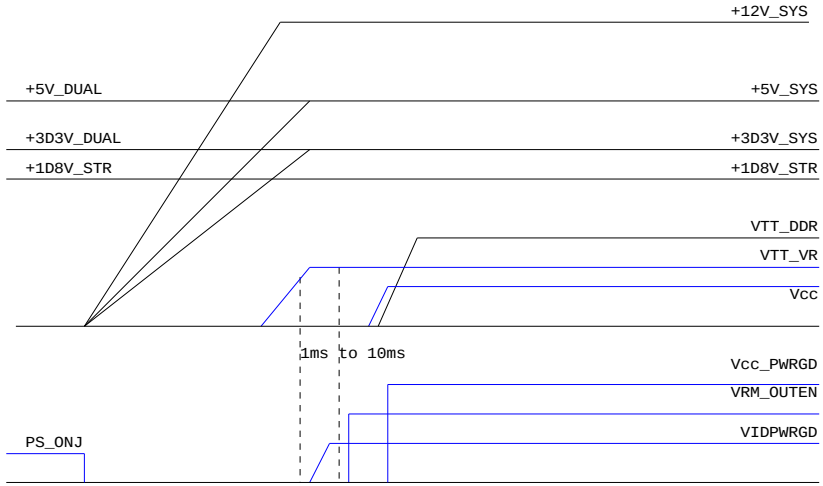

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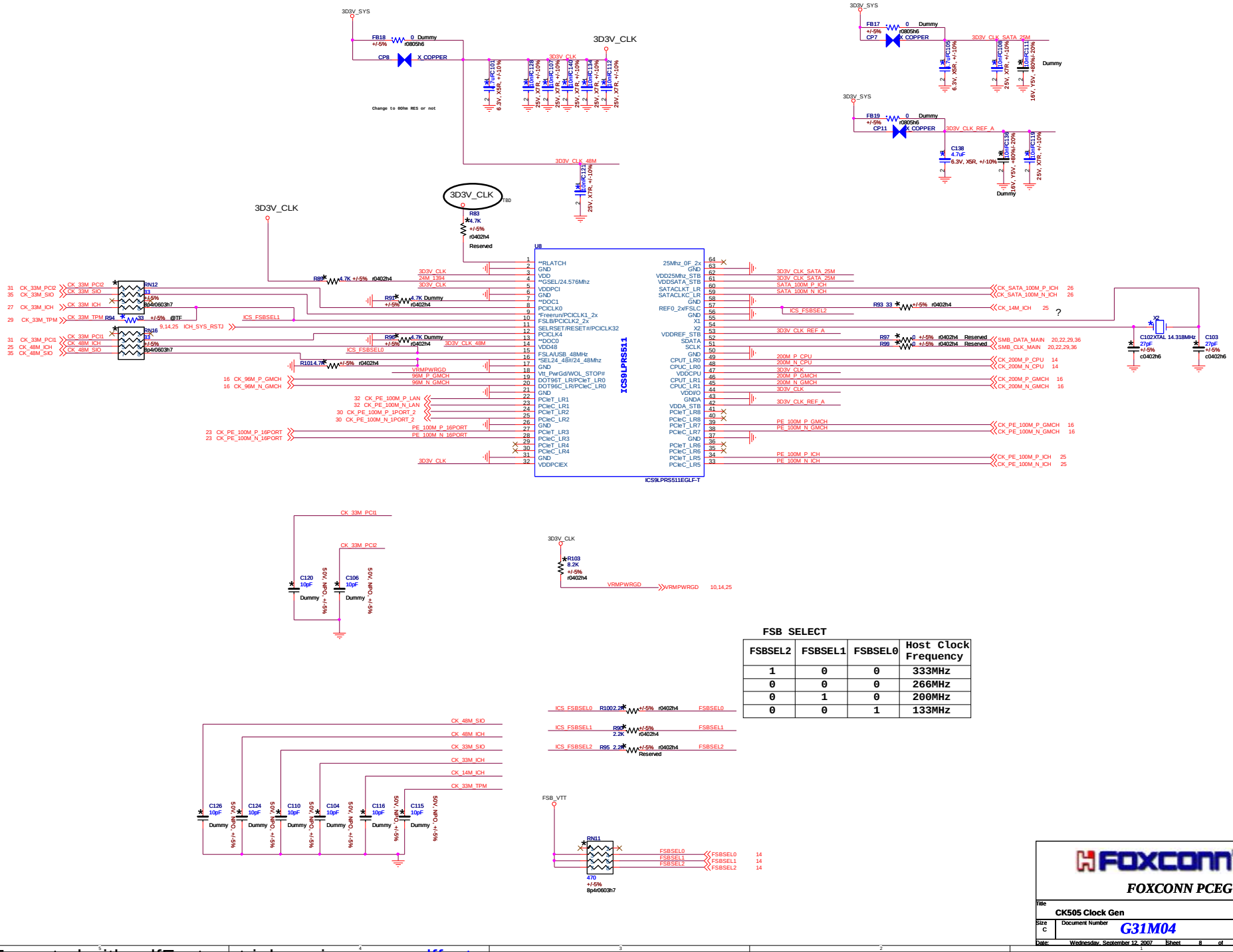
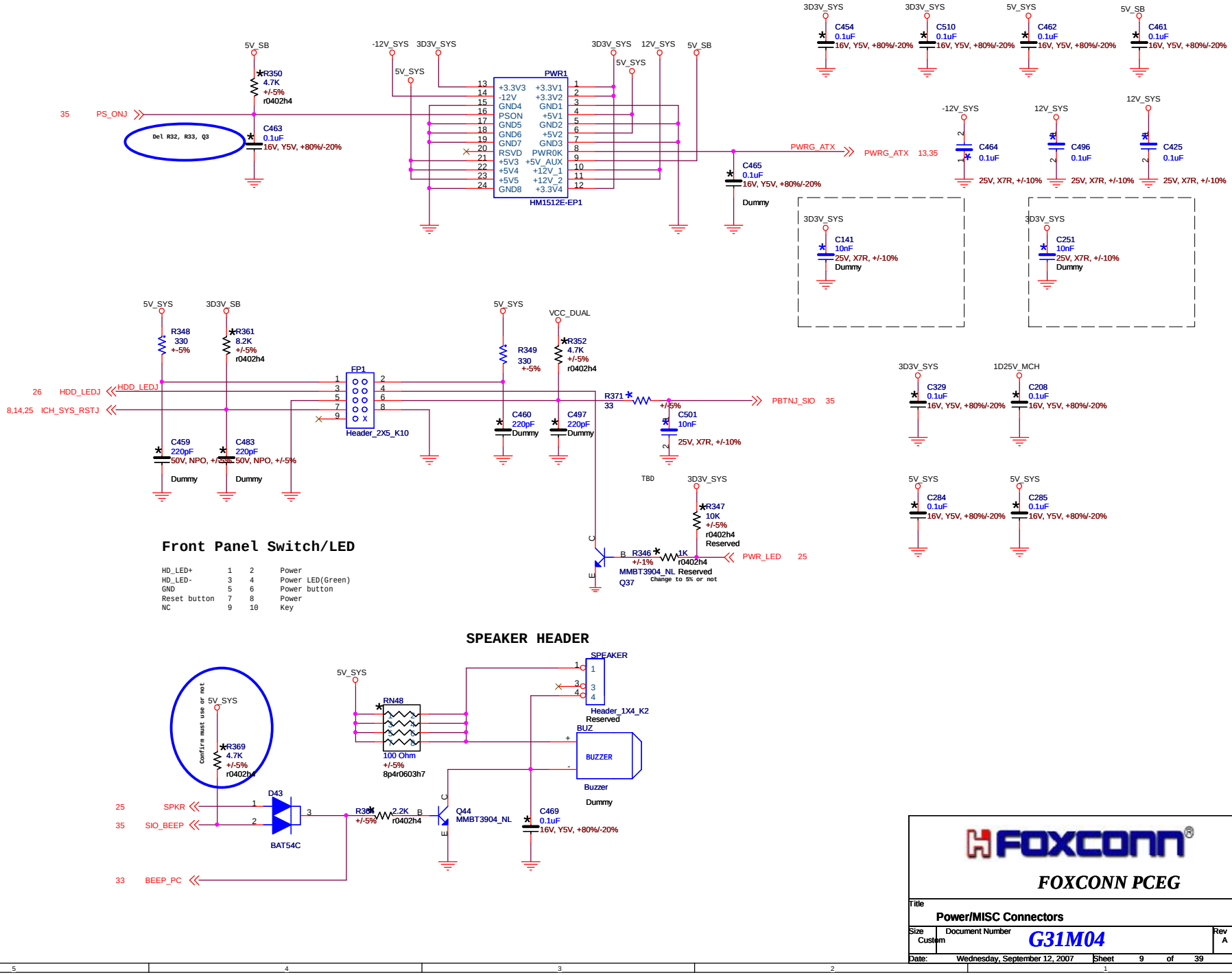


FSB SELECT			
FSBSEL2	FSBSEL1	FSBSEL0	Host Clock Frequency
1	0	0	333MHz
0	0	0	266MHz
0	1	0	200MHz
0	0	1	133MHz



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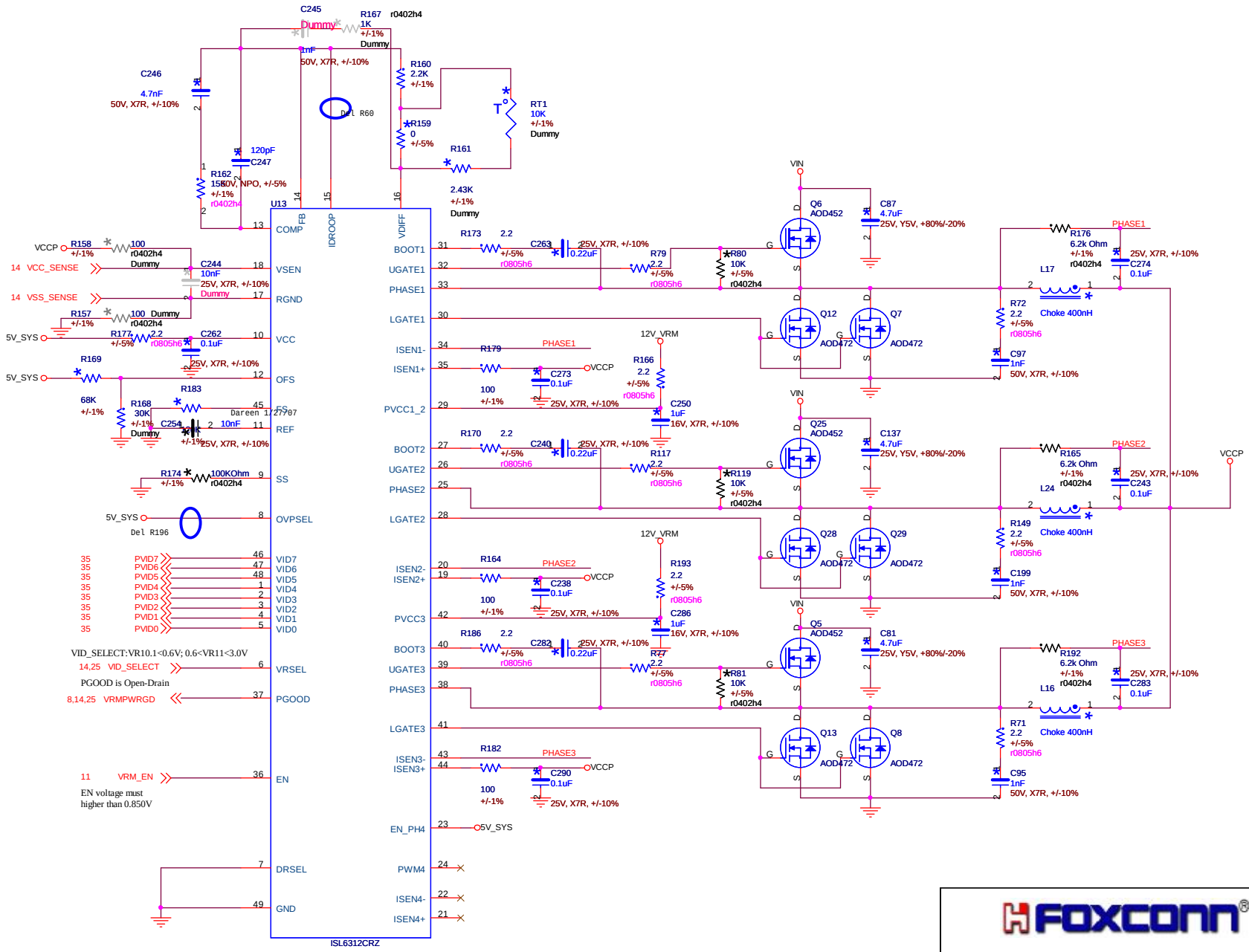

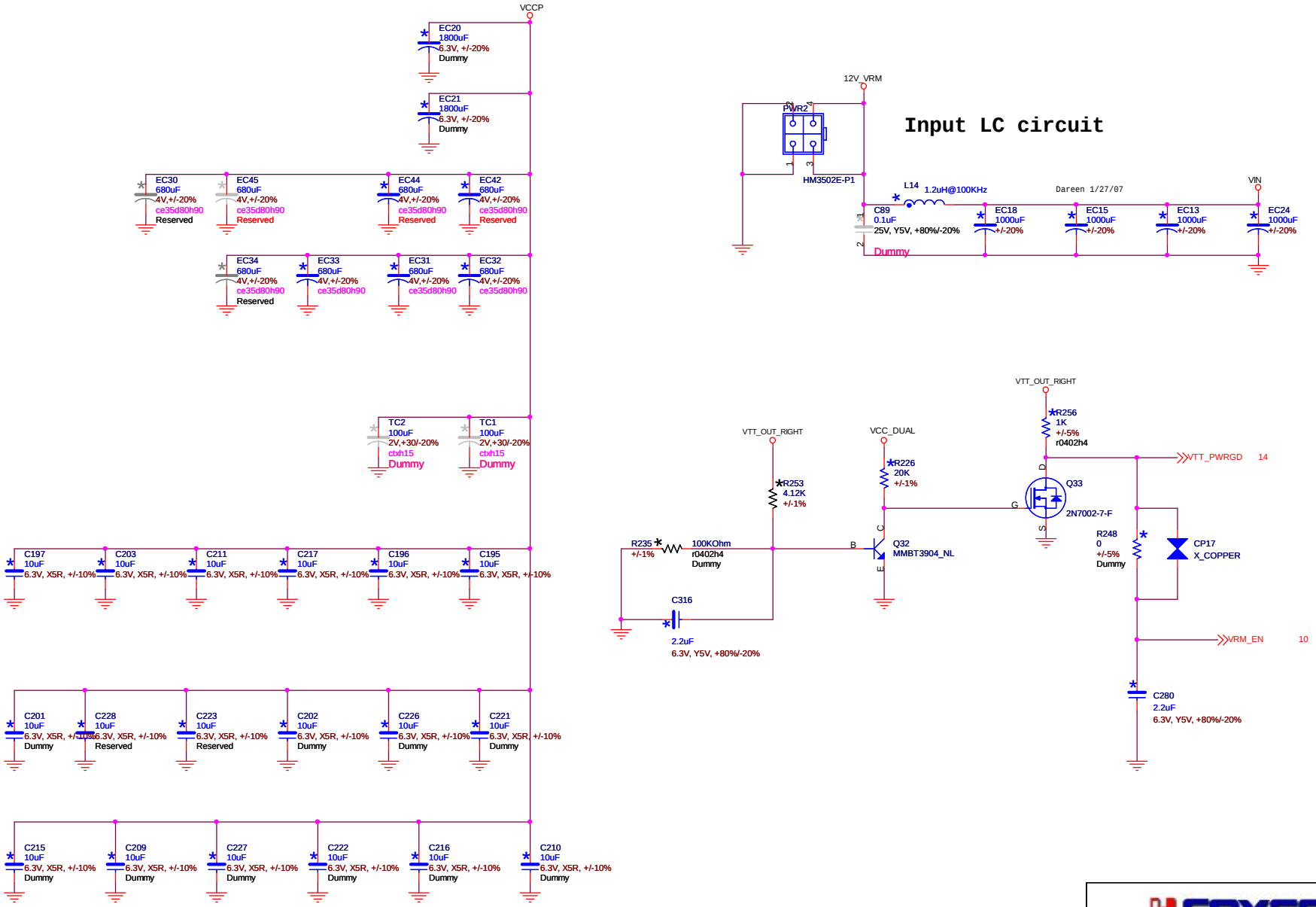

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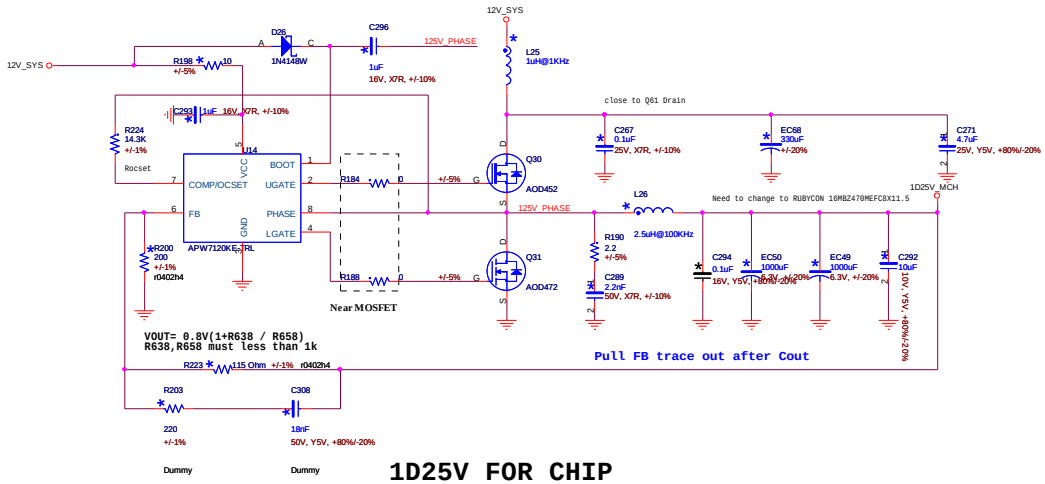

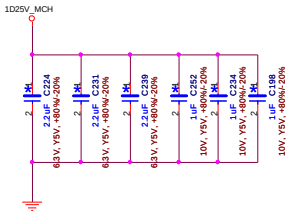

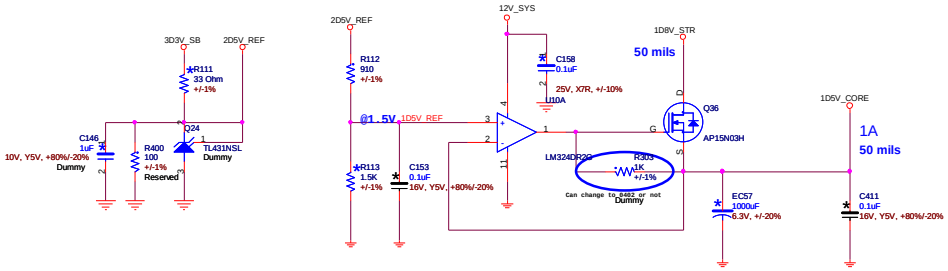

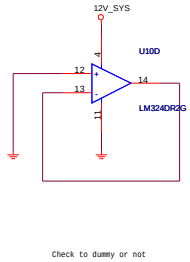

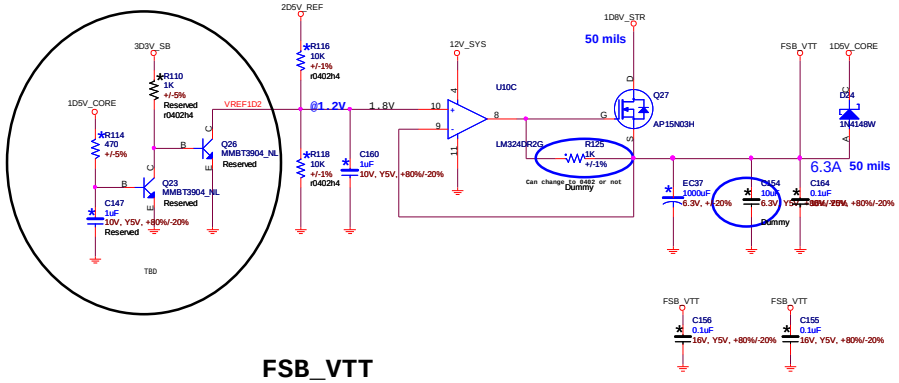

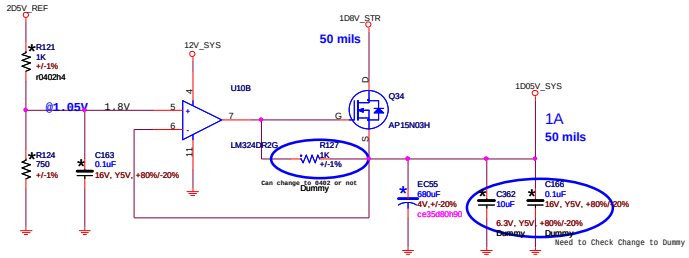

FSB_VTT

1D05V_SYS

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Title: 1D25V 1D5V FSB

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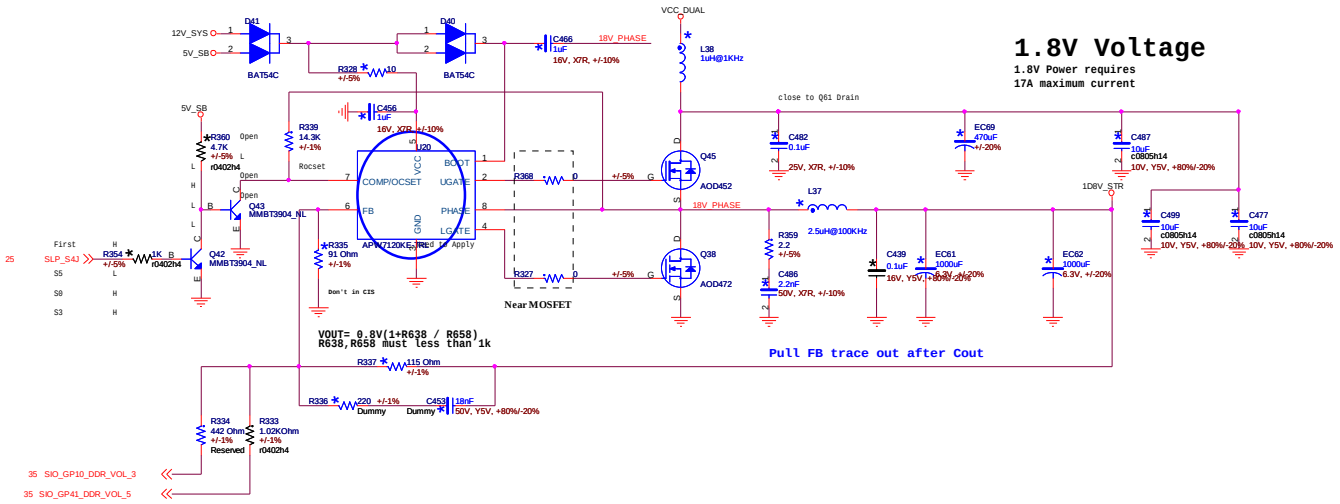

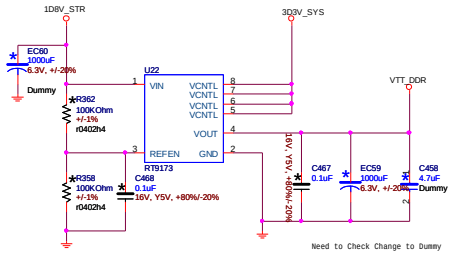

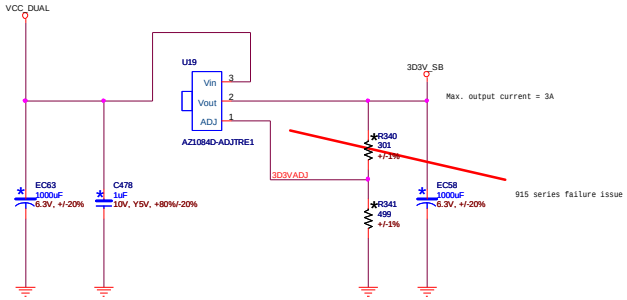

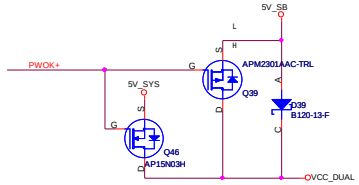
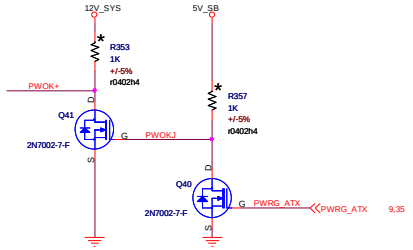

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Title: STR 1D8V 3D3V_DUAL 5V_DUAL

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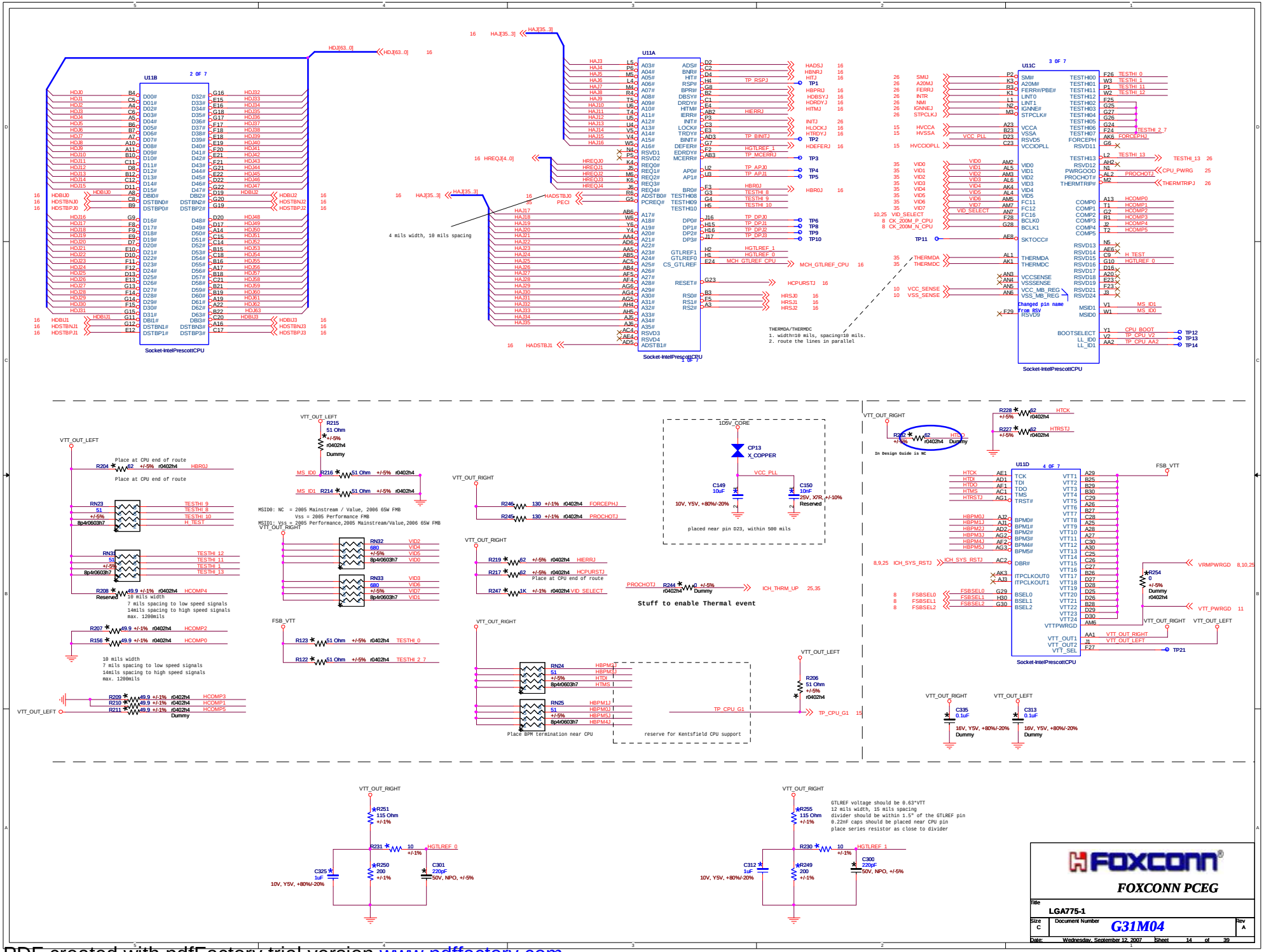

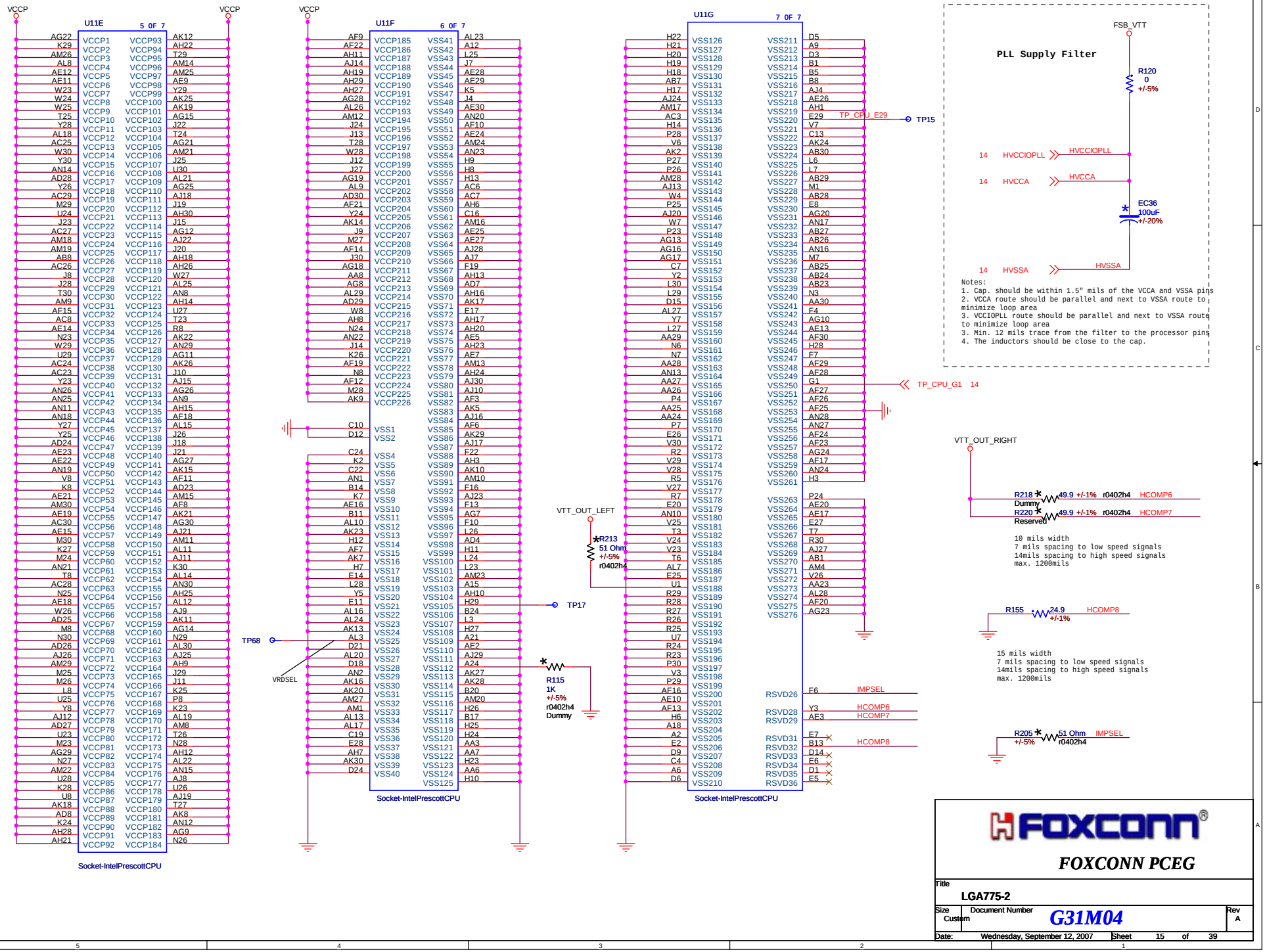

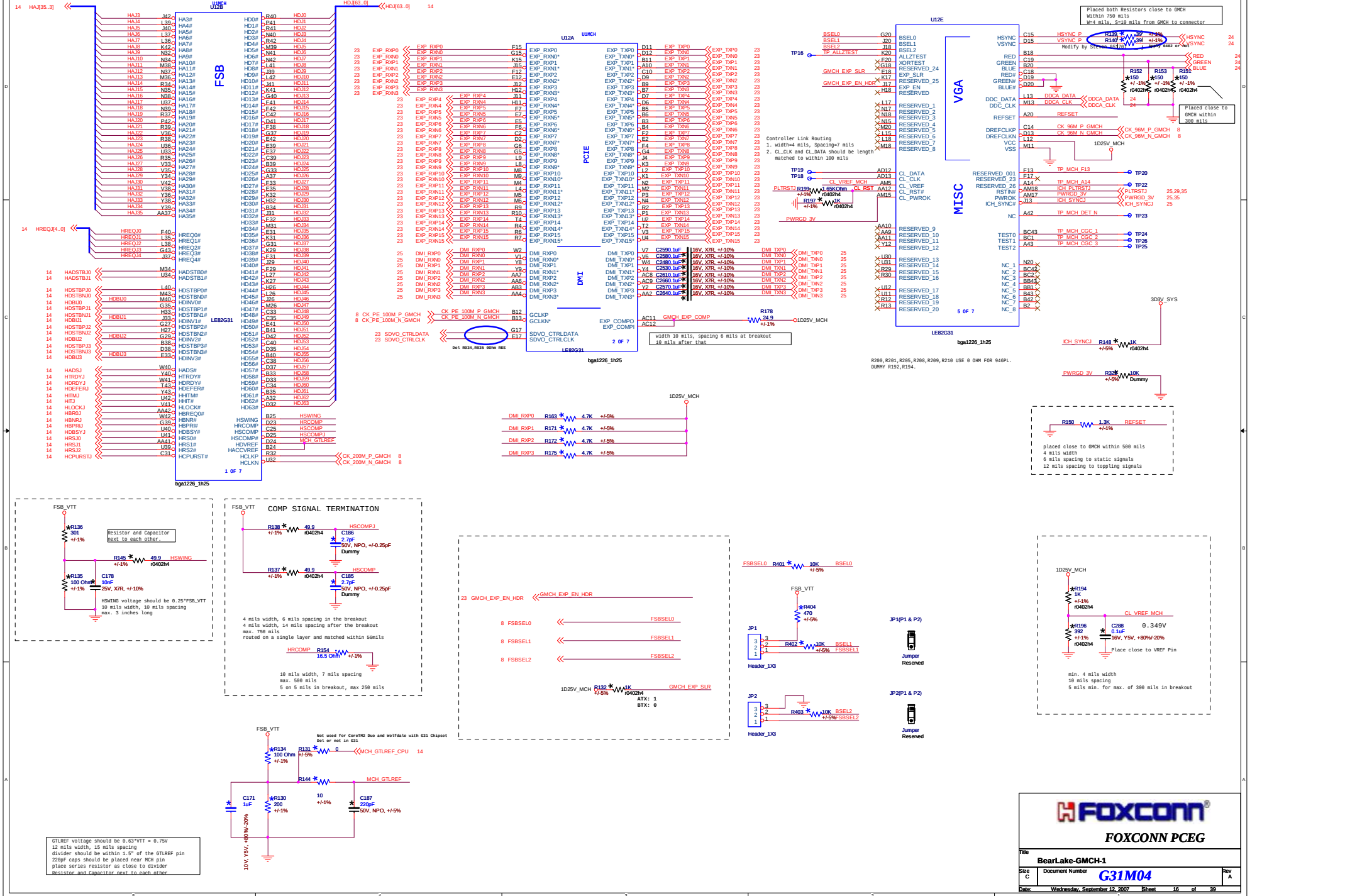

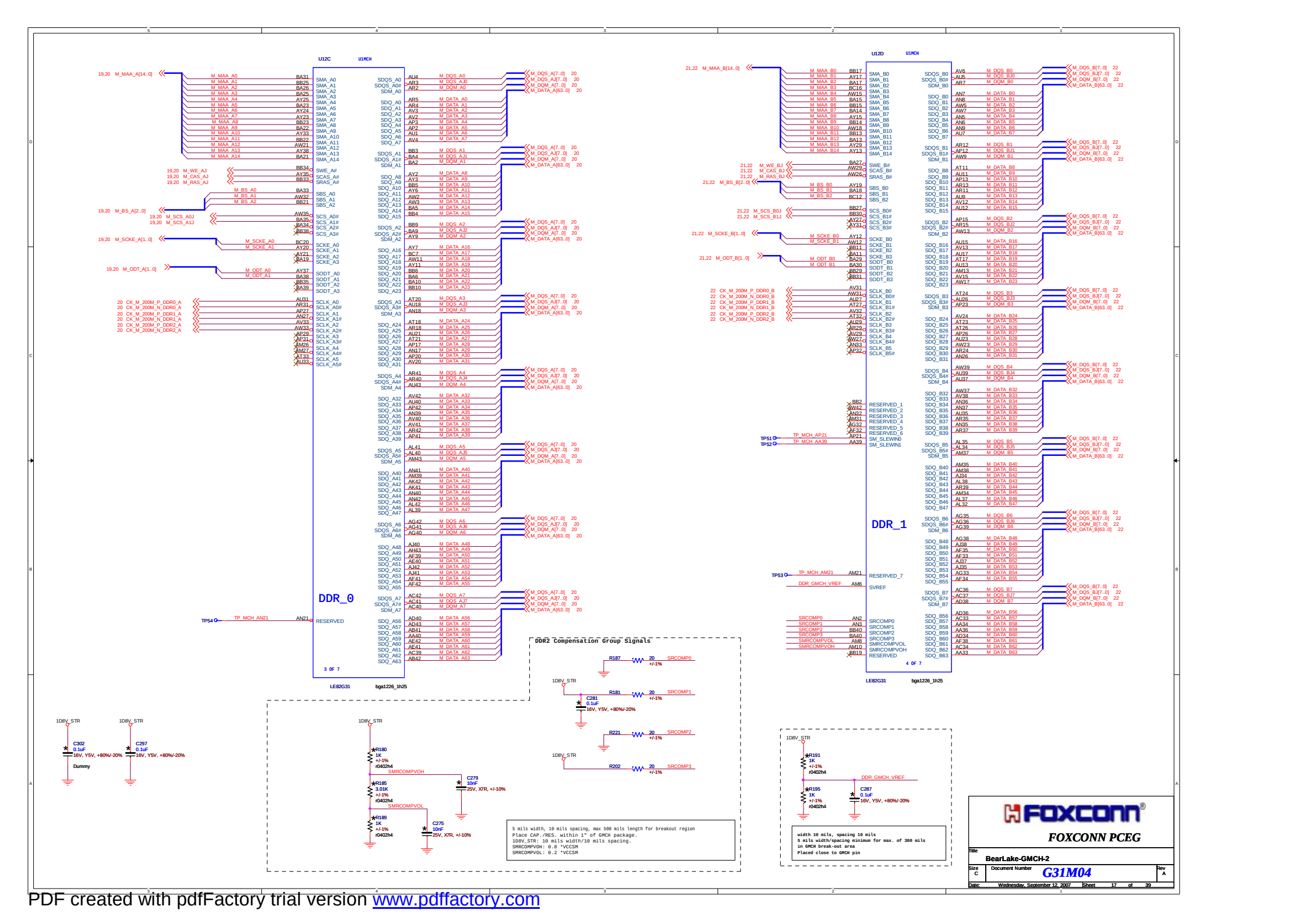

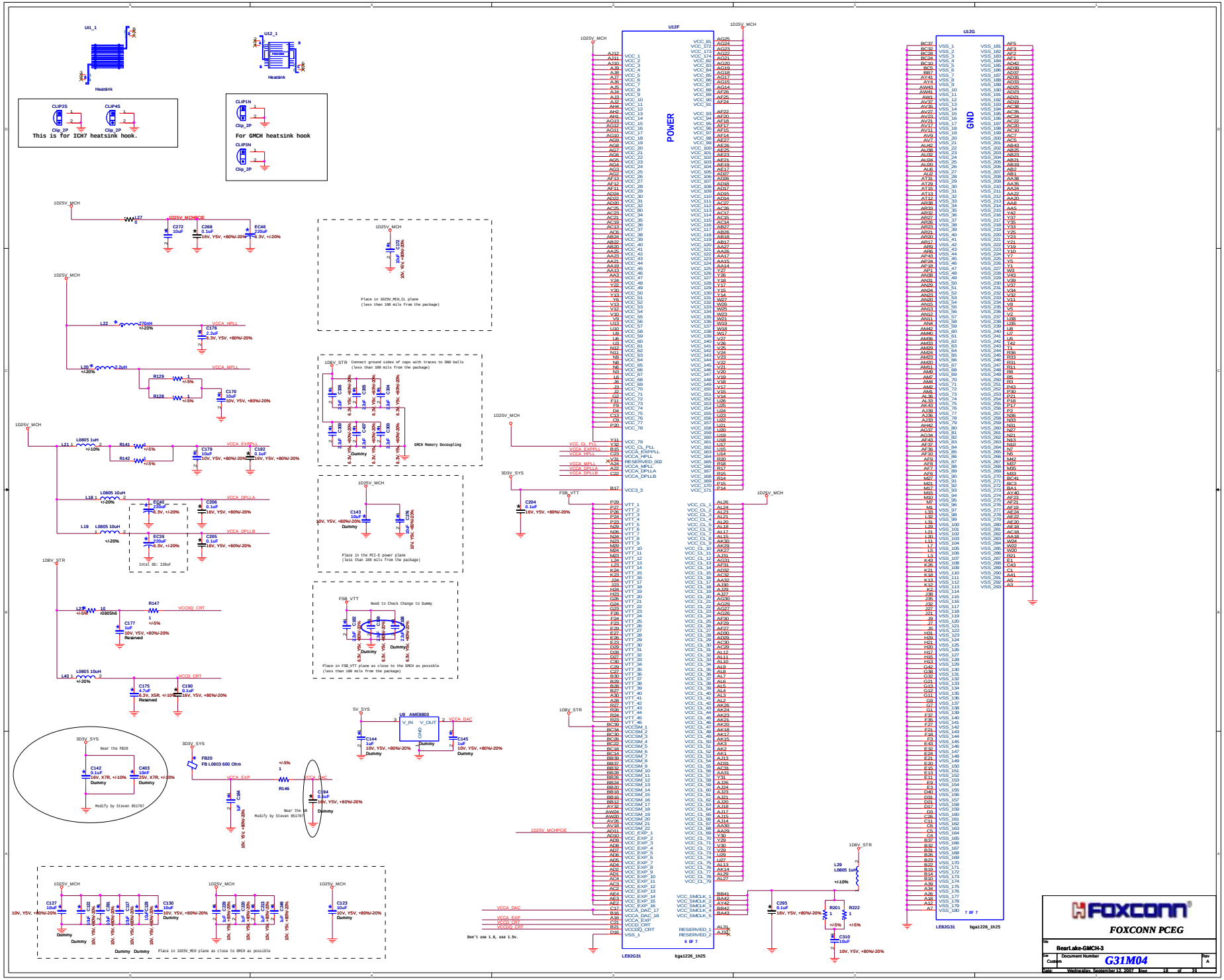

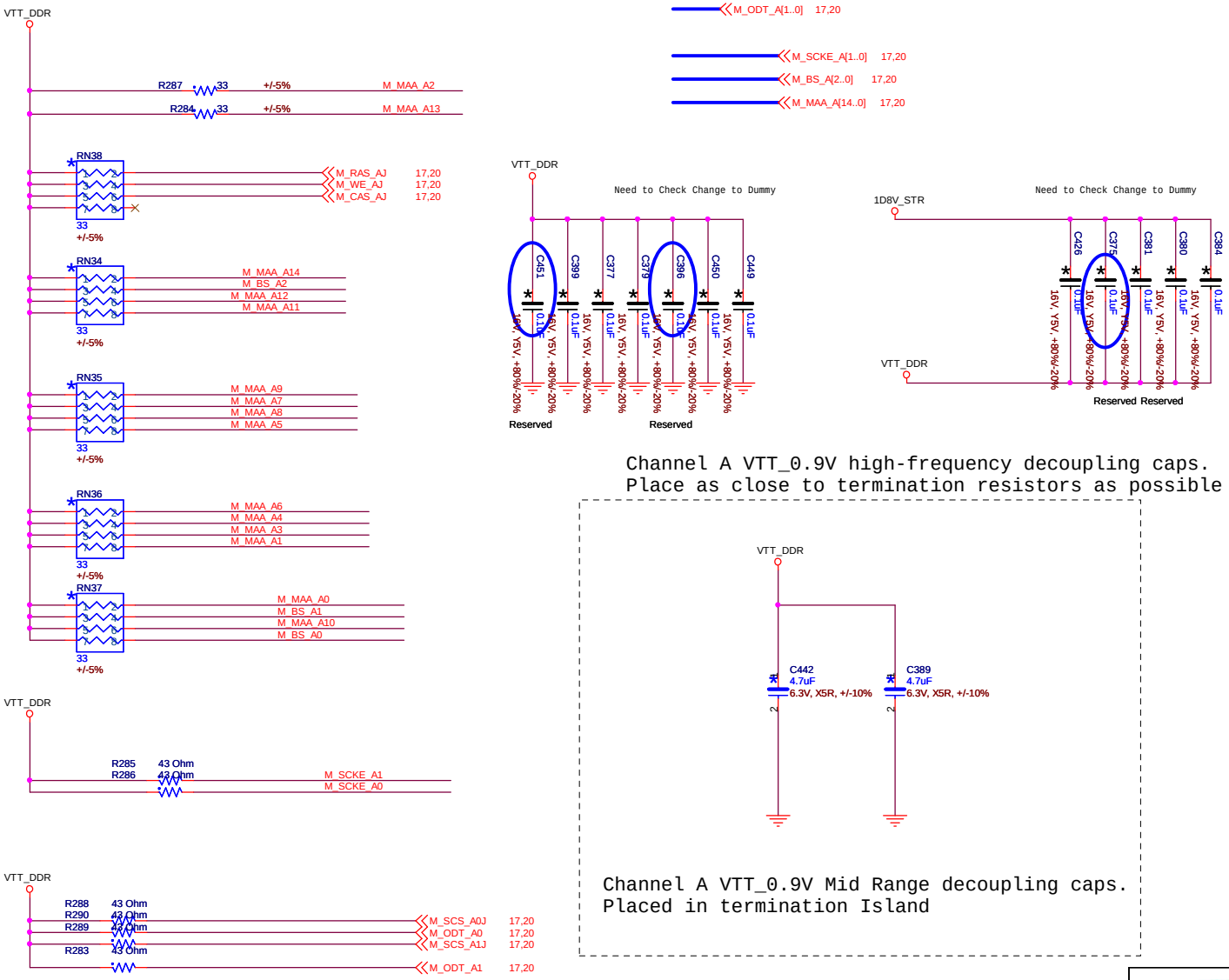

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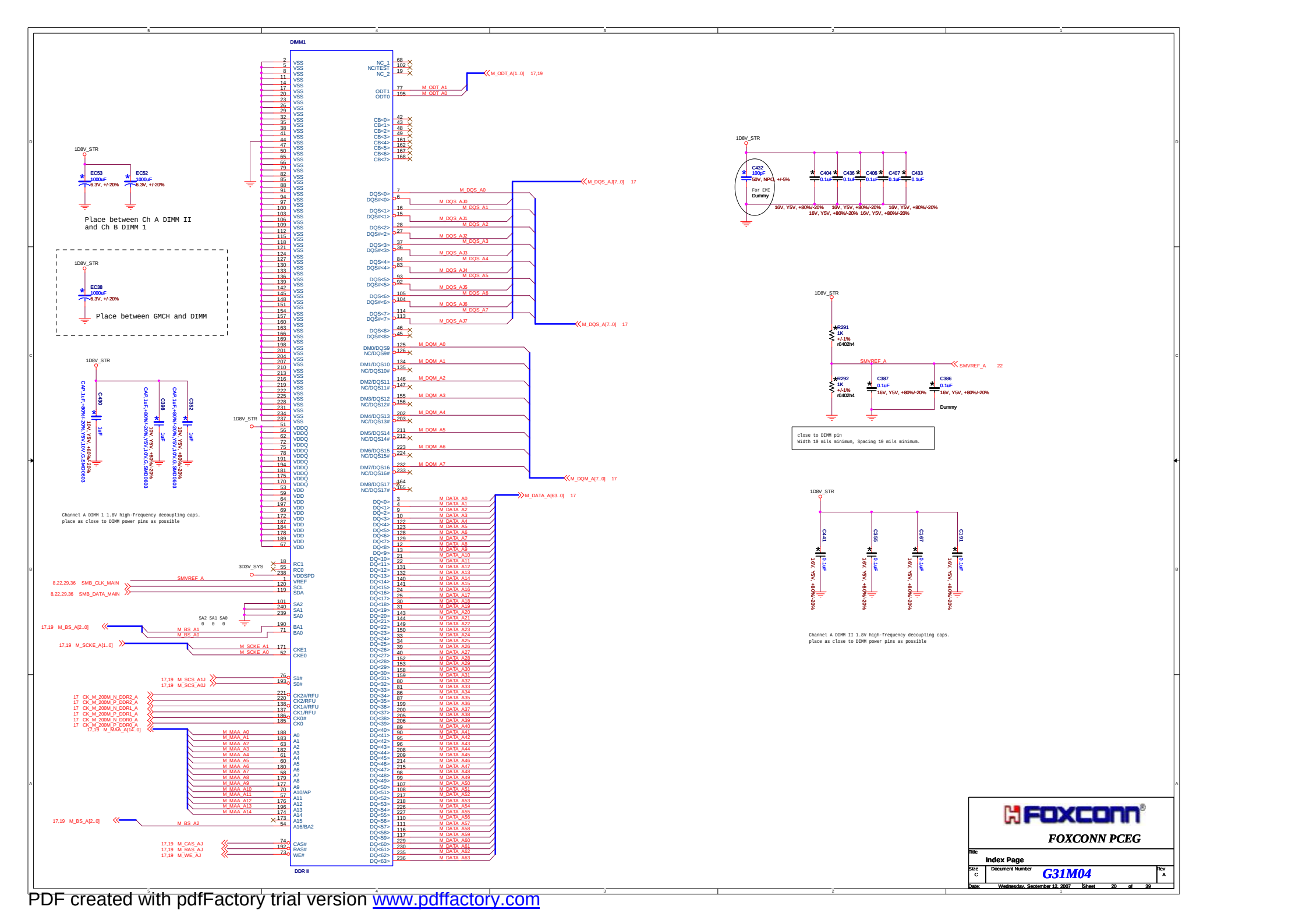
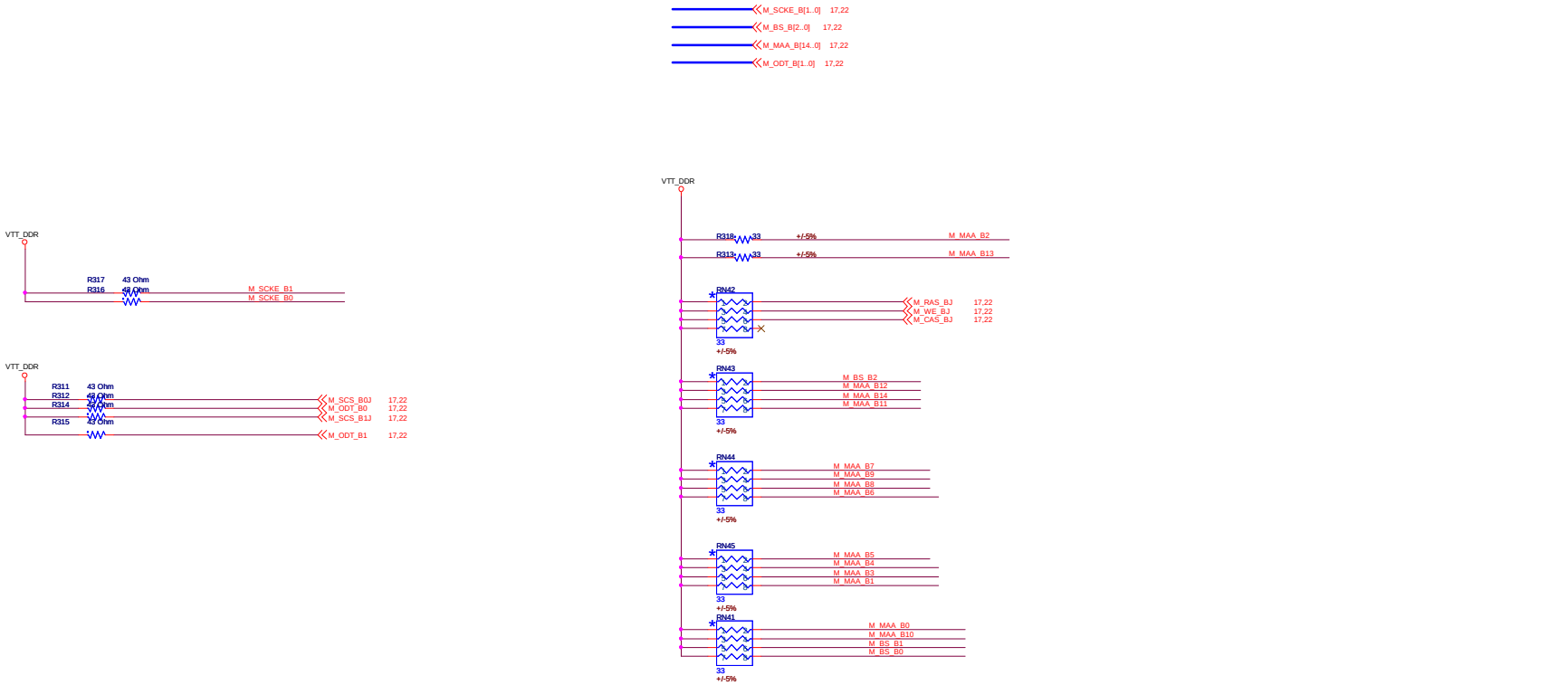
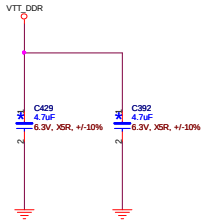
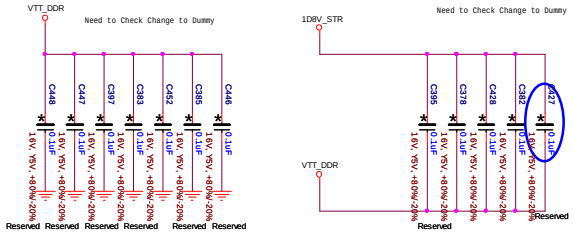






Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

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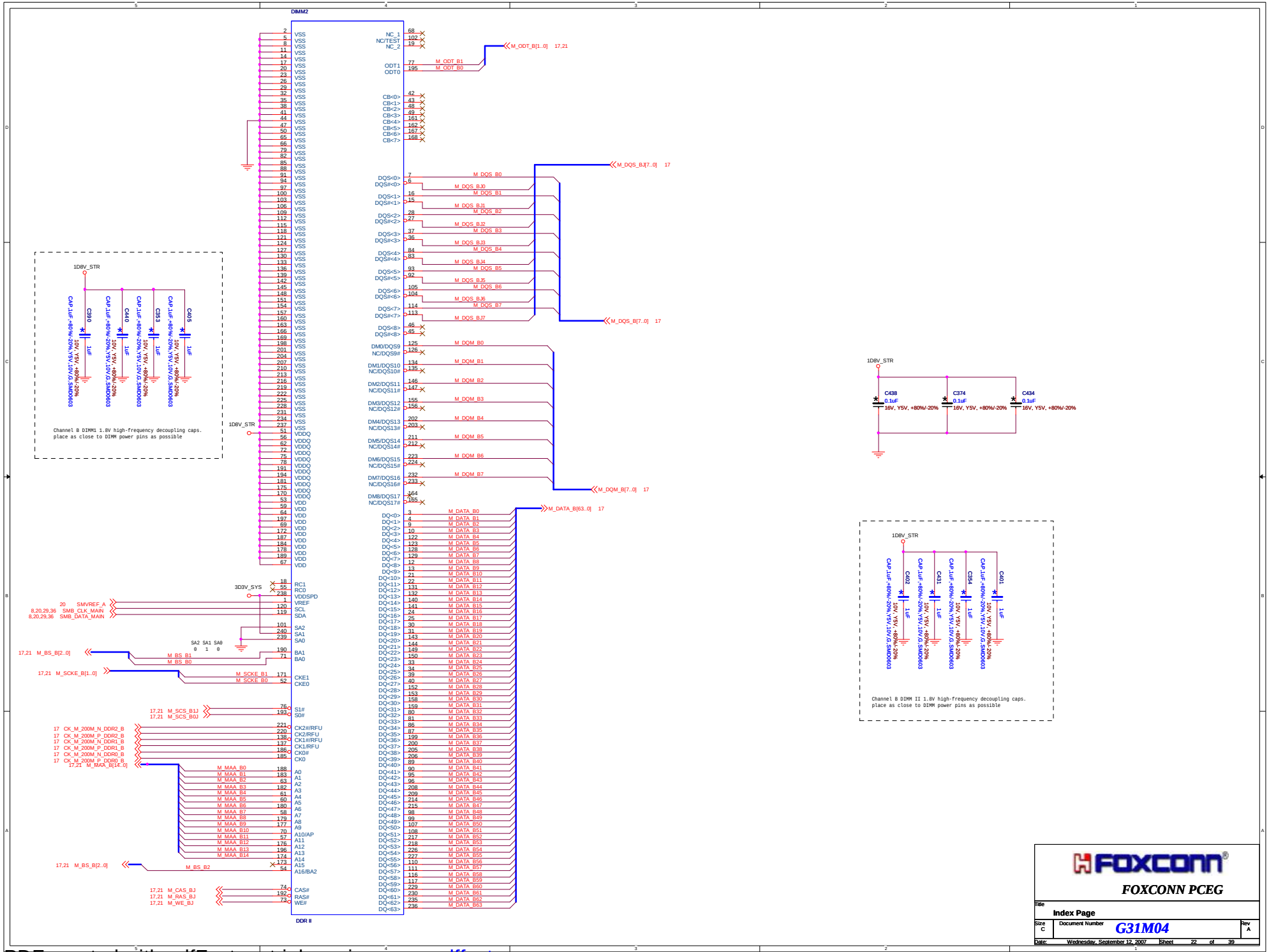

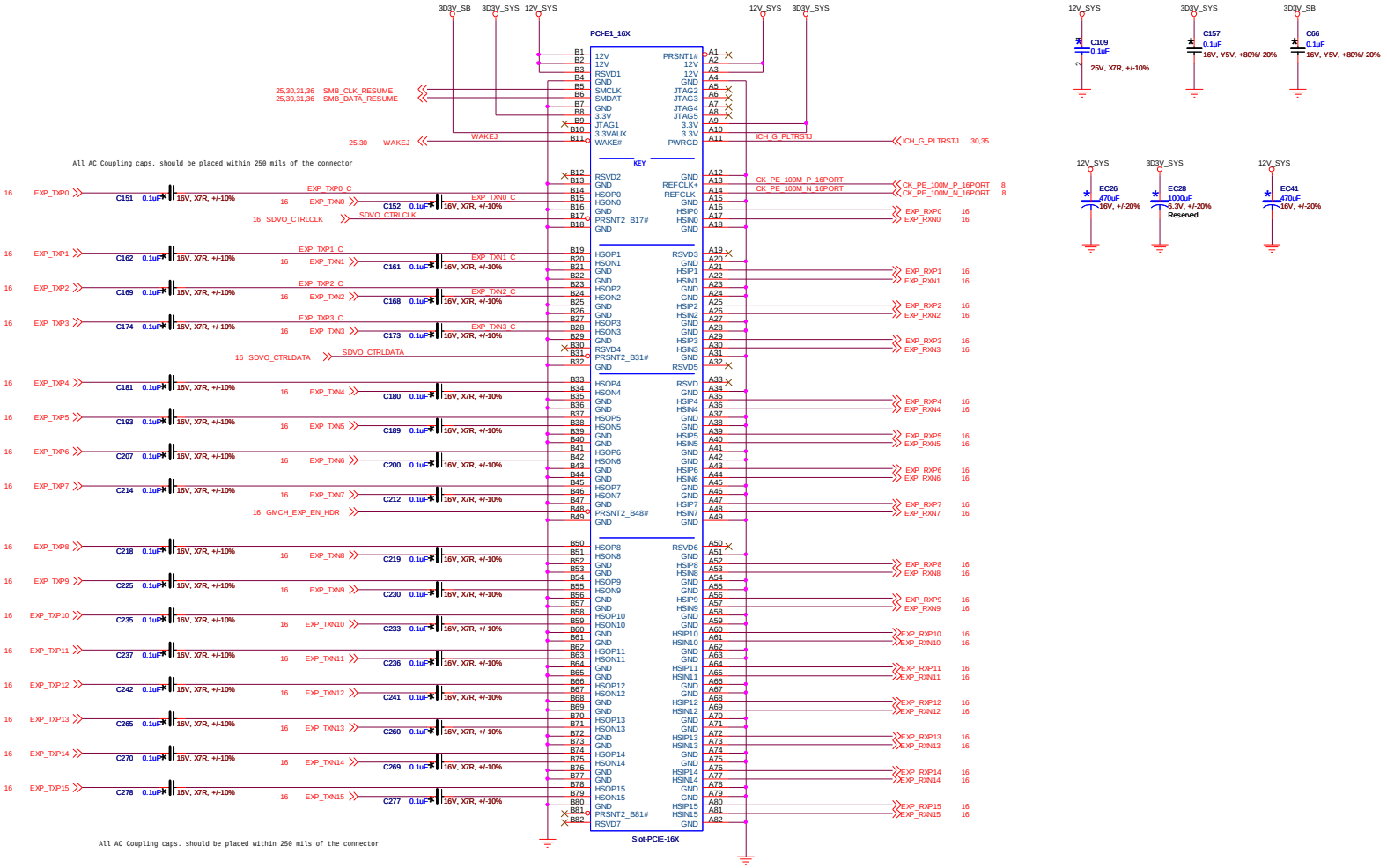

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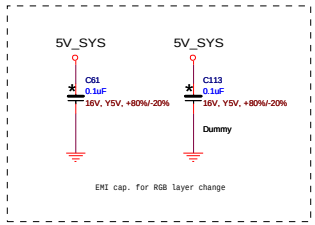
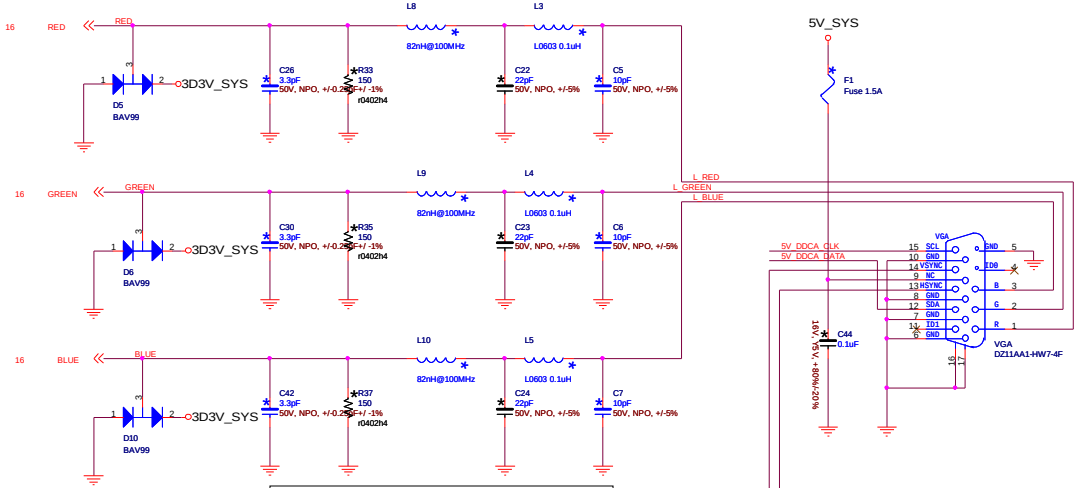
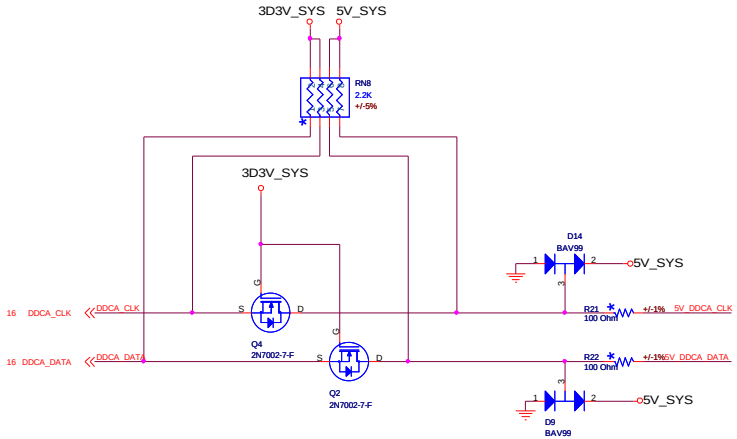
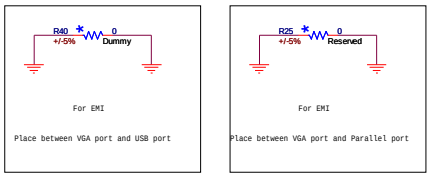
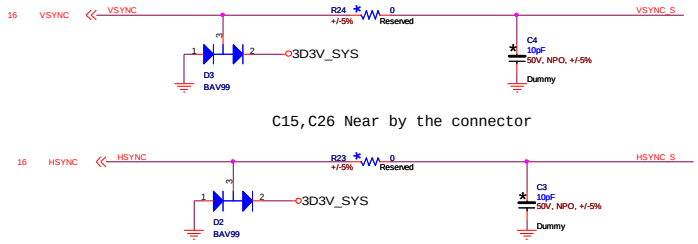


RGB routing
1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. is 8400 mils
6. R,G,B signals should be ground referenced









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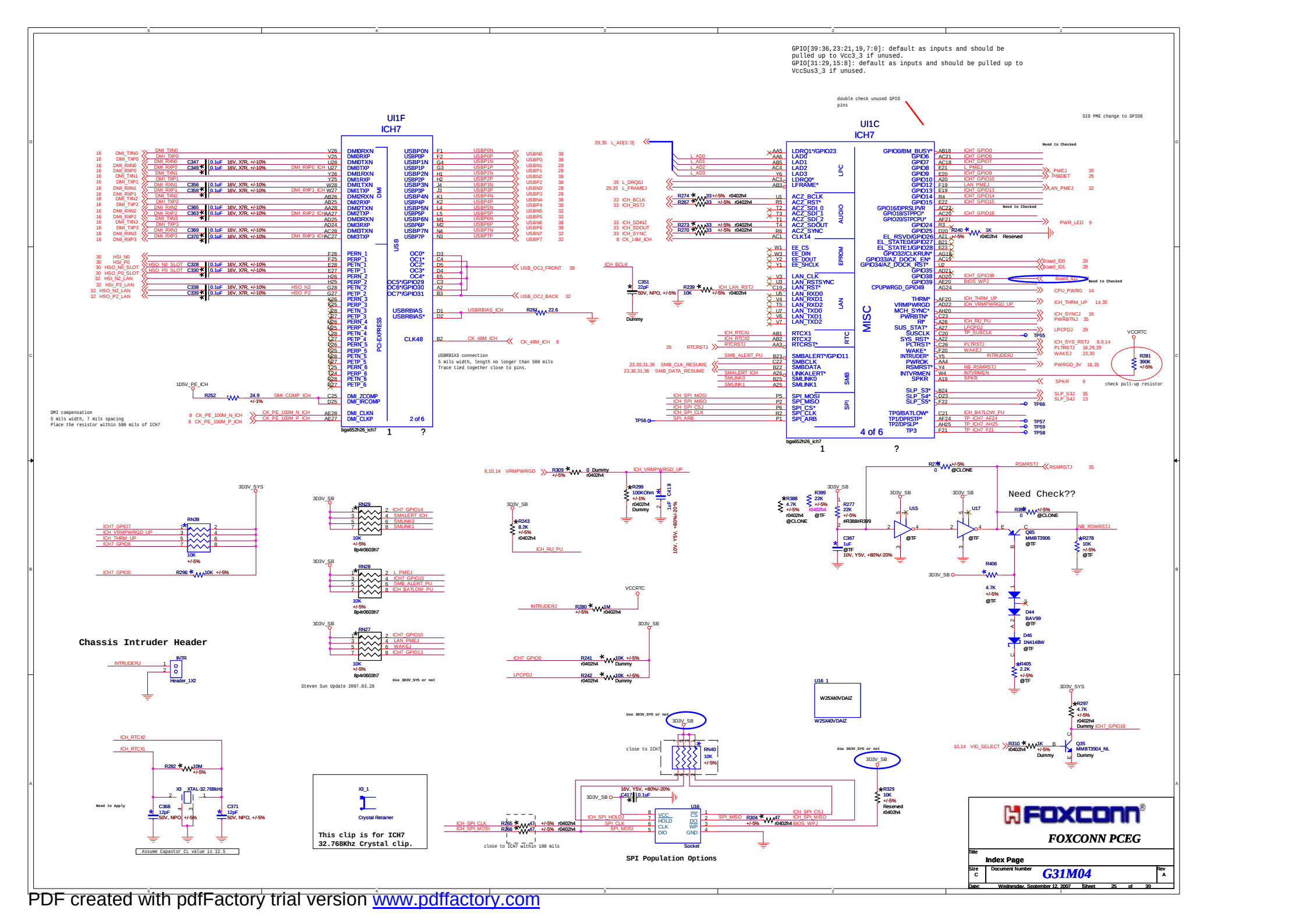
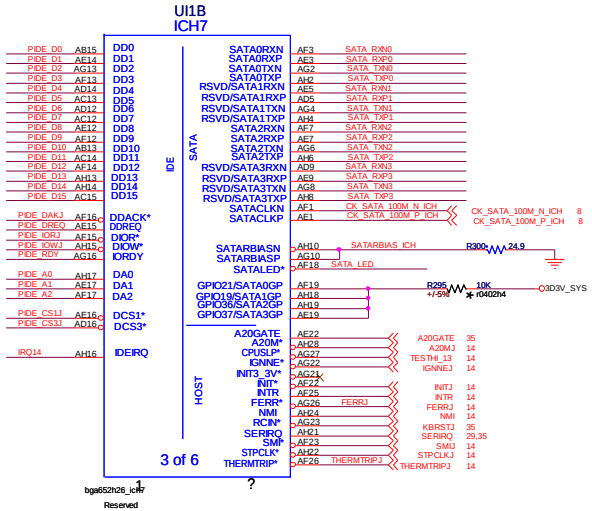
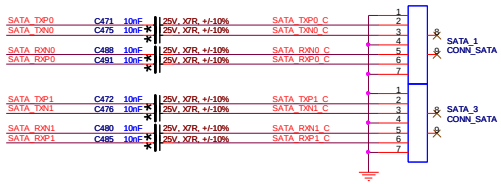
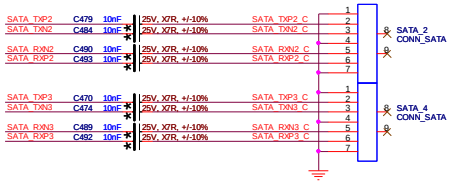
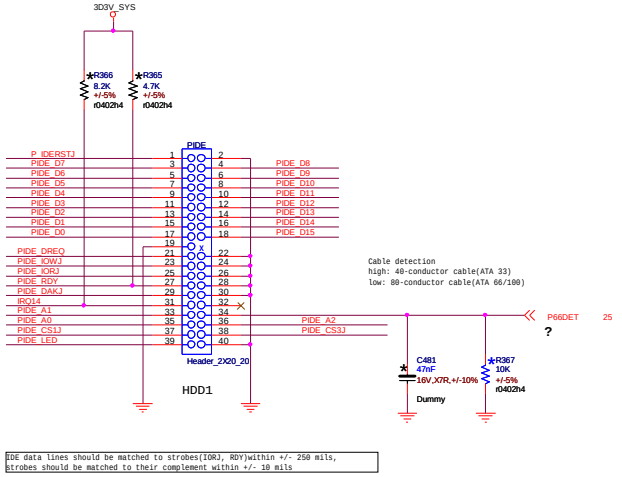




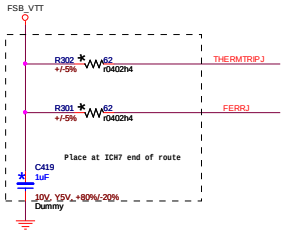


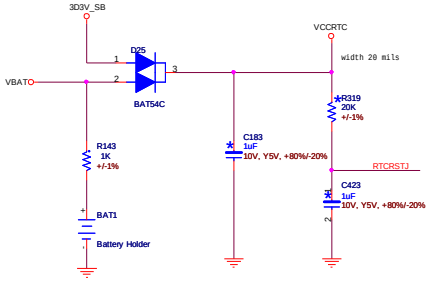
SATARBIAS connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.

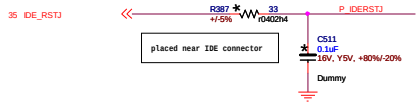


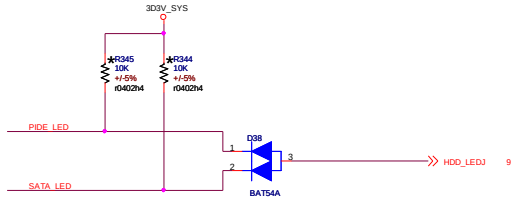


IDE data lines should be matched to strobes(IORJ, RDY)within +/- 250 mils, strobes should be matched to their complement within +/- 10 mils



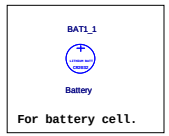






Clear CMOS

CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3) **Default**



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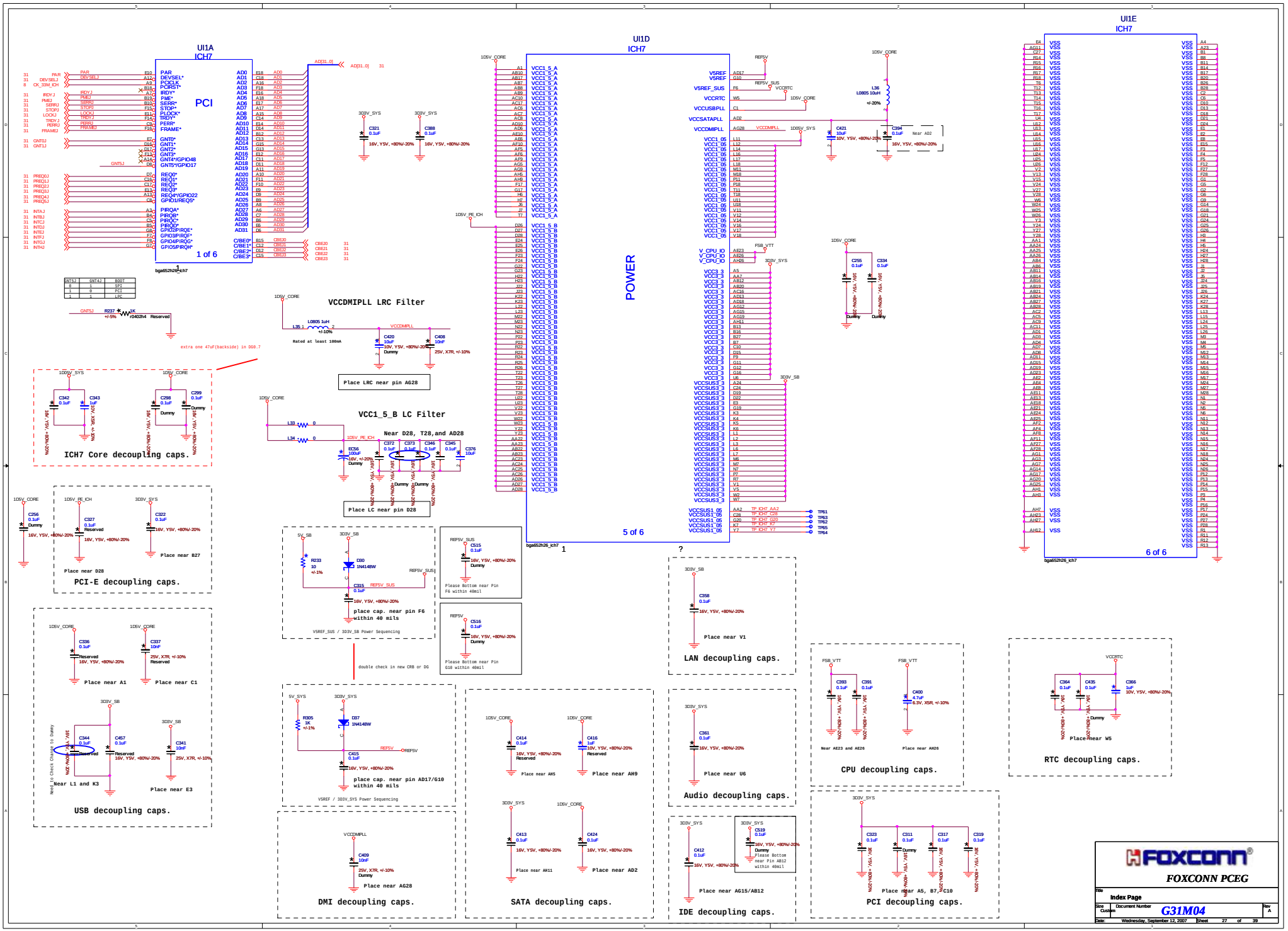
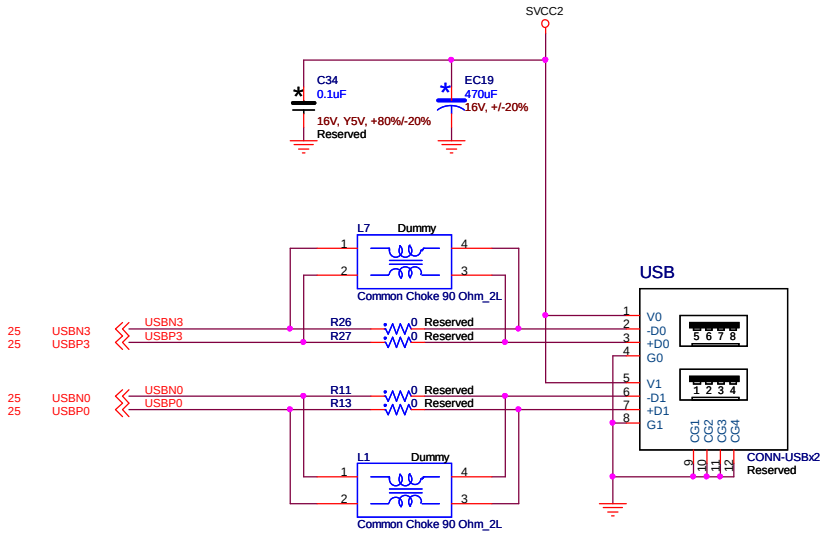
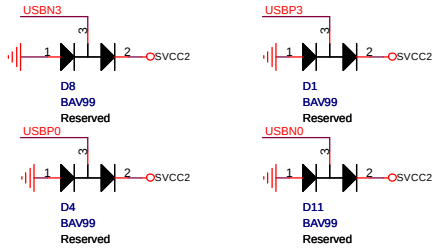


Rear Dual USB Connector





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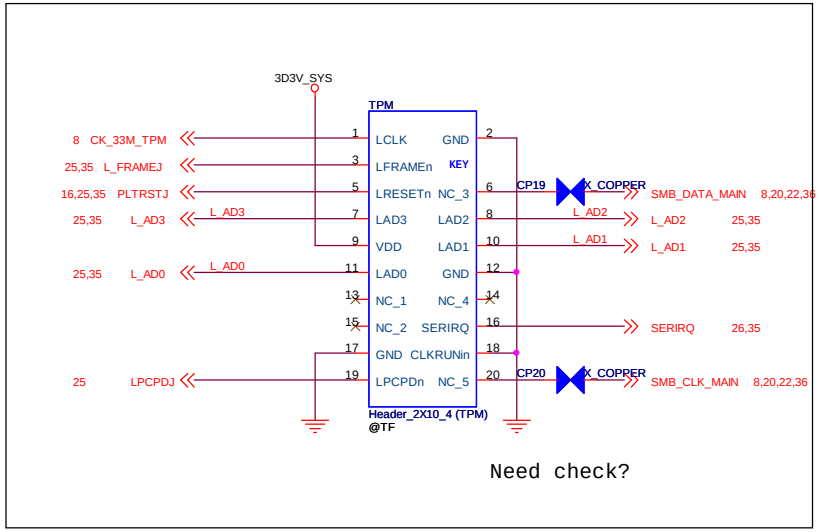

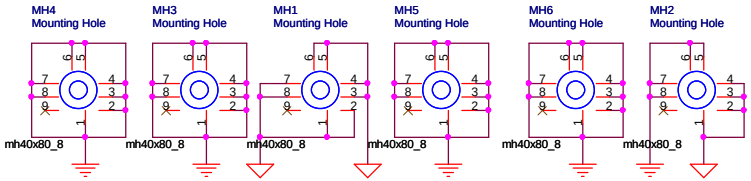

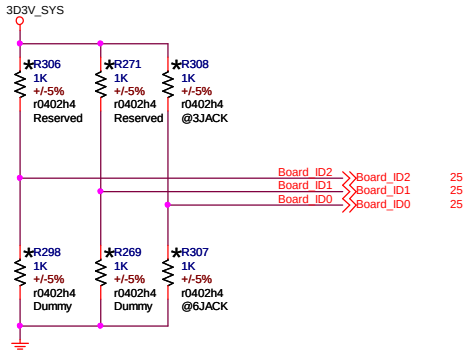

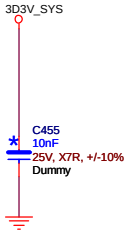

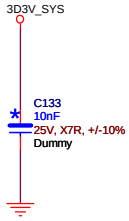

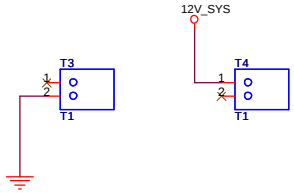

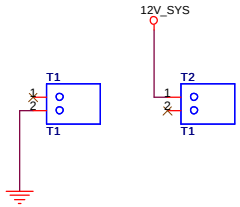

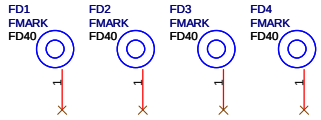

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Title: FWH			
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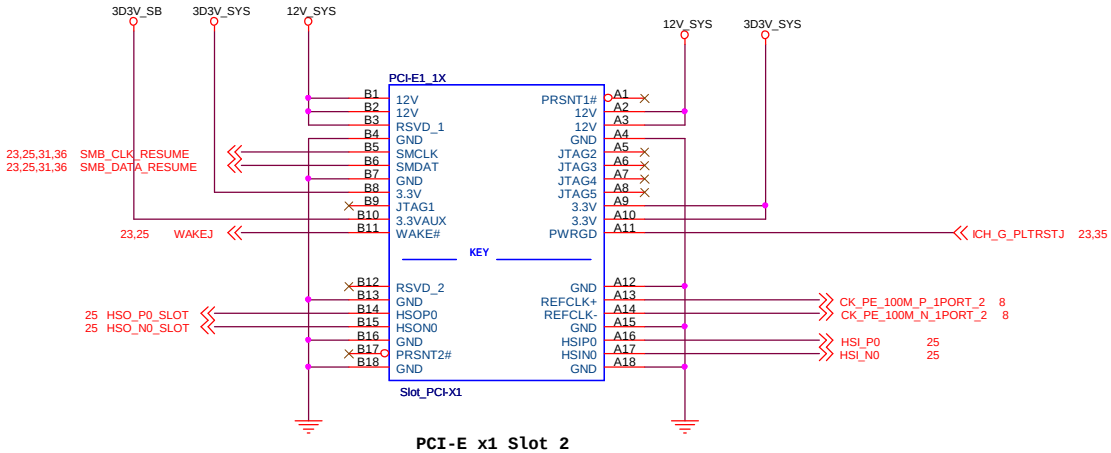
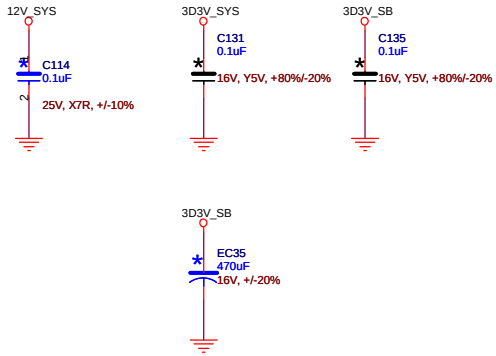


PCI-E x1 Slot 2



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Title: PCI Express x1 Slot			
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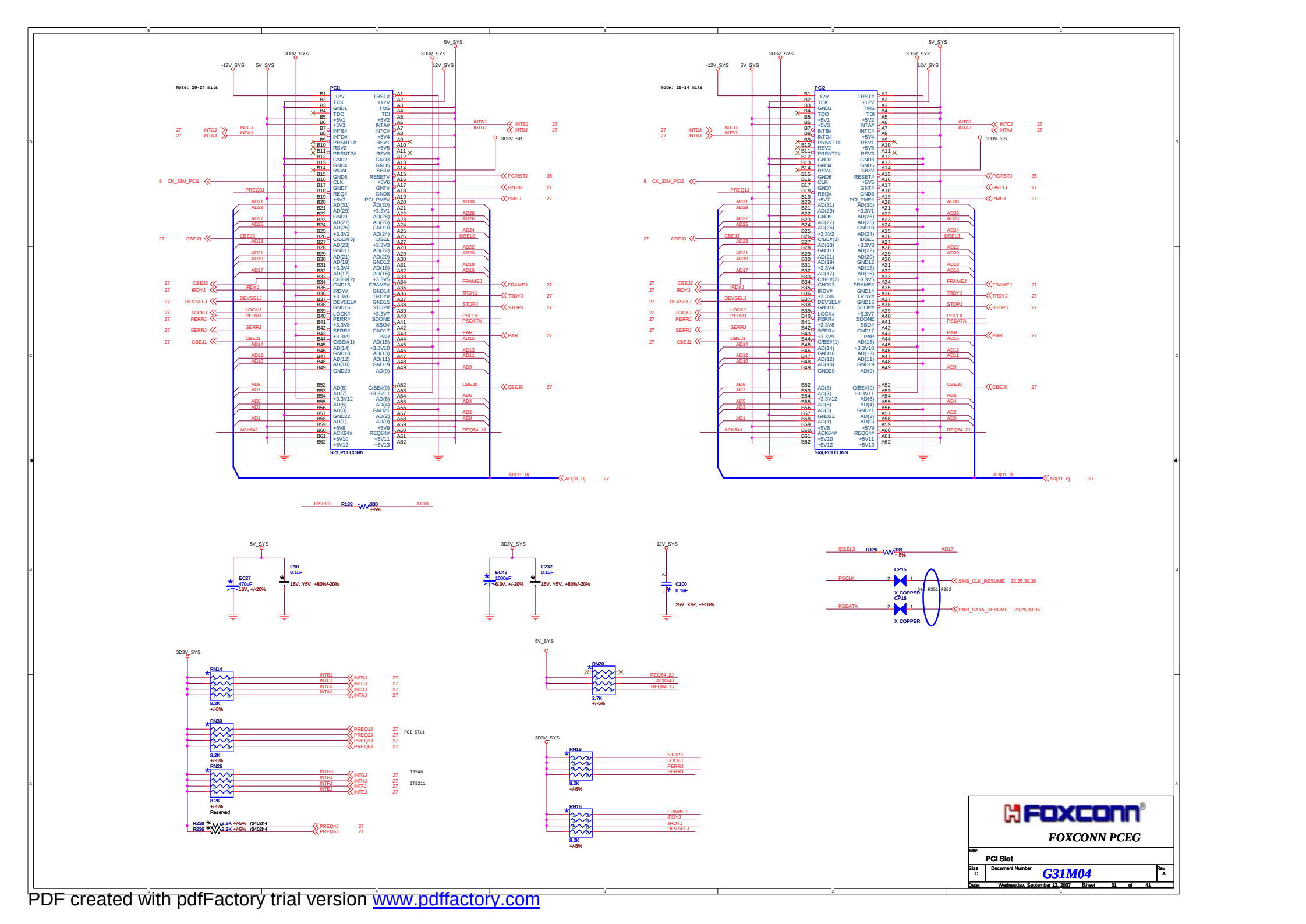
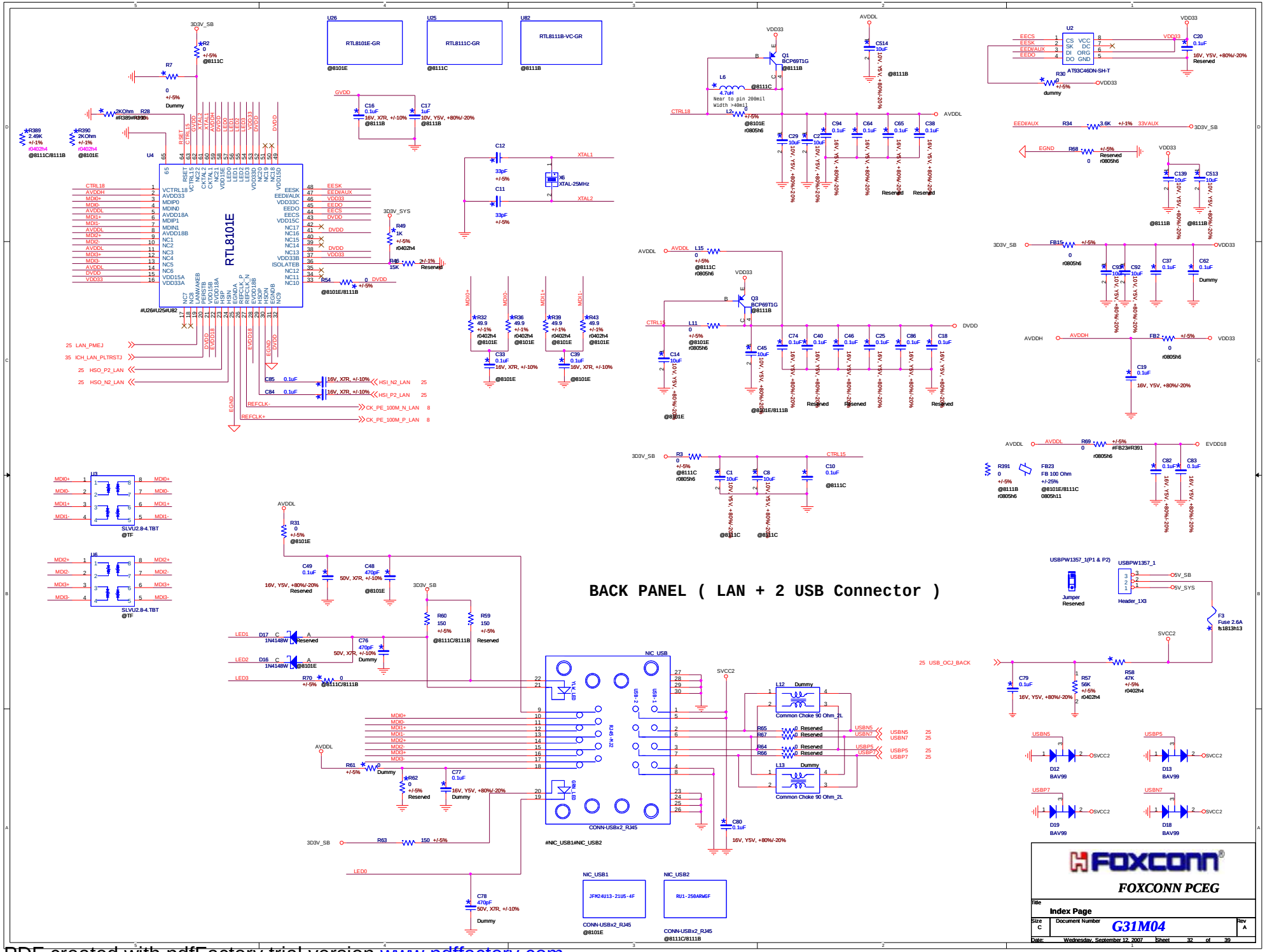
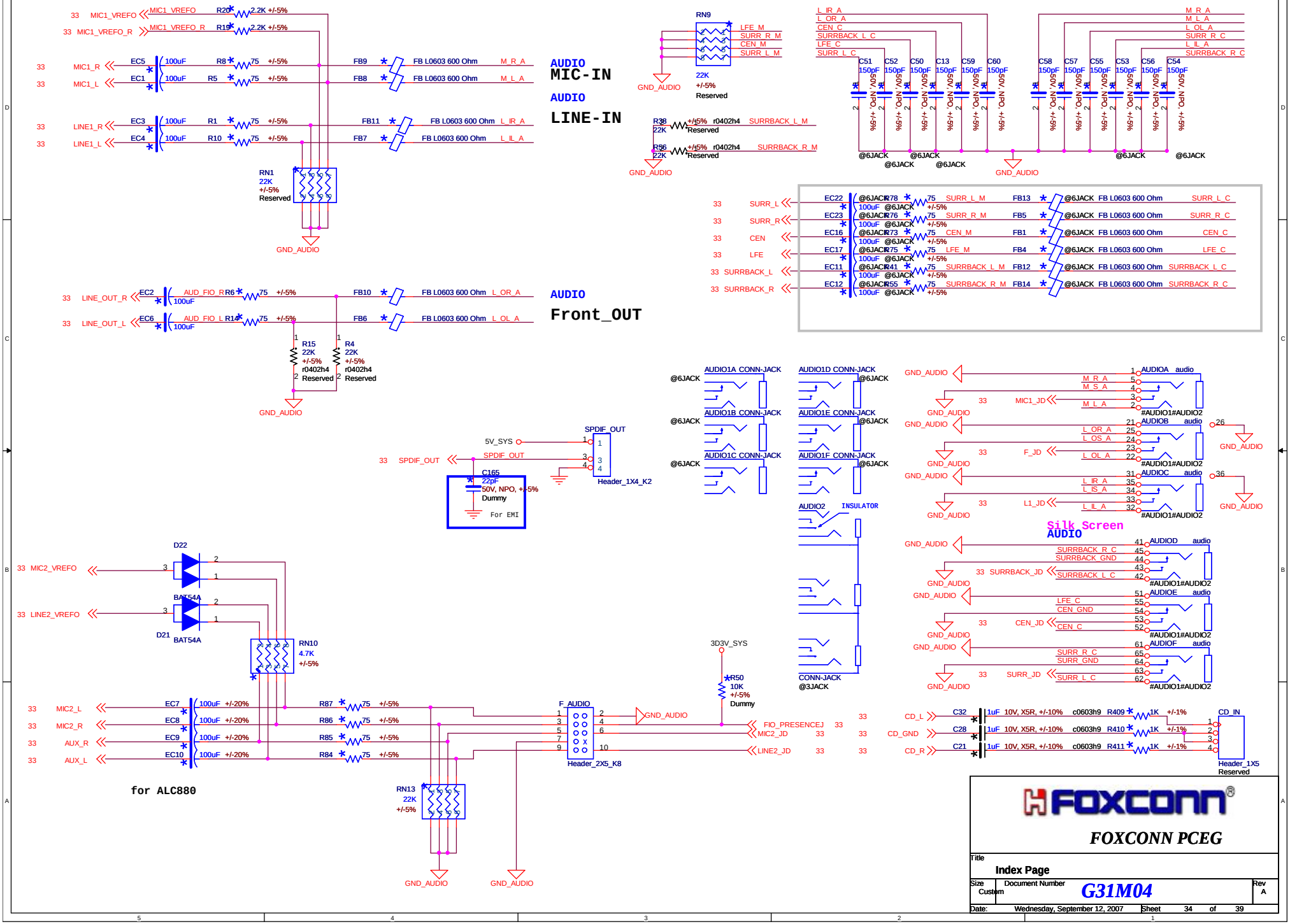
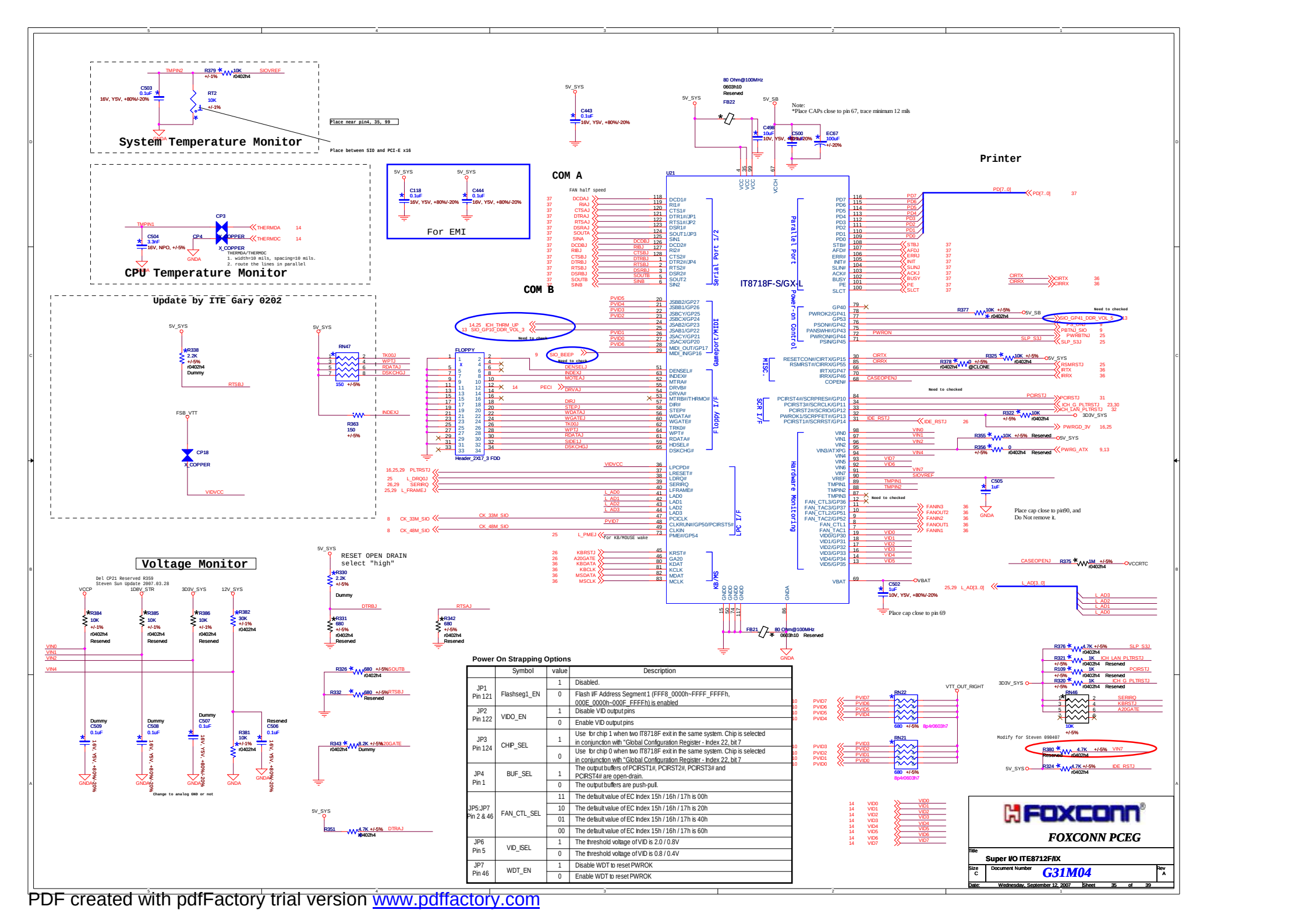
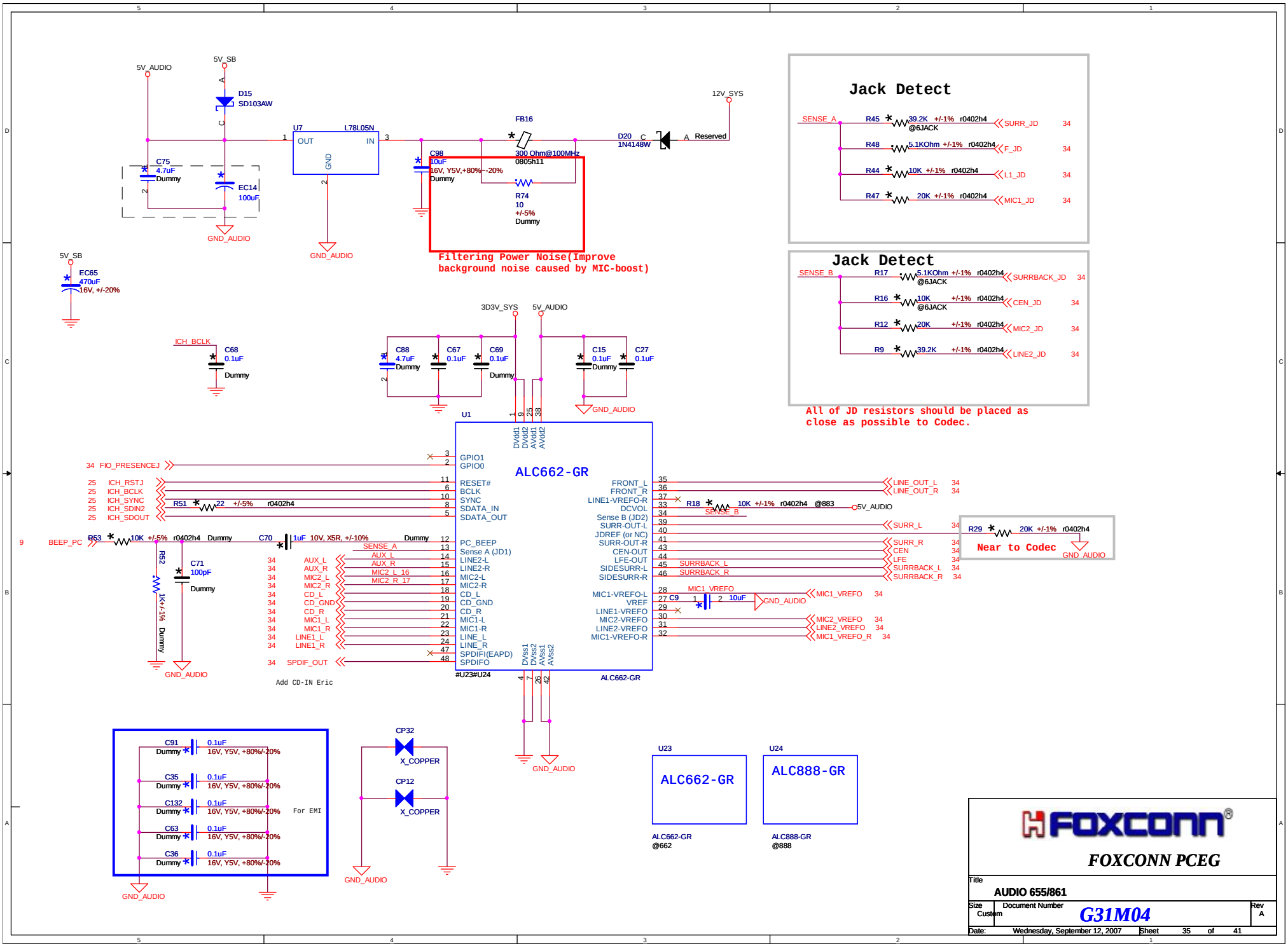






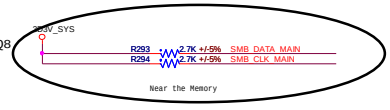


	Symbol	value	Description
JP1 Pin 121	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2 Pin 122	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 124	CHIP_SEL	1	Use for chip 1 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7
		0	Use for chip 0 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7
JP4 Pin 1	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3# and PCIRST4# are open-drain.
		0	The output buffers are push-pull.
JP5:JP7 Pin 2 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h / 16h / 17h is 00h
		10	The default value of EC Index 15h / 16h / 17h is 20h
		01	The default value of EC Index 15h / 16h / 17h is 40h
		00	The default value of EC Index 15h / 16h / 17h is 60h
JP6 Pin 5	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V
JP7 Pin 46	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK



SM Bus Bridge

If use SUIO power good function, dummy Q7,Q6,Q8 pop R25,R18



8,20,22,29 SMB_DATA_MAIN — CP9 X_COPPER — SMB_DATA_RESUME 23,25,30,31

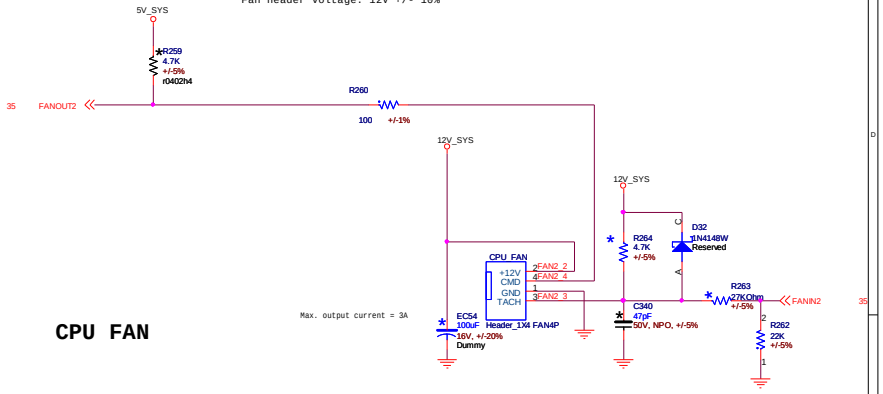
for Clock Generator/DIMMs/TPM/Clock Buffer

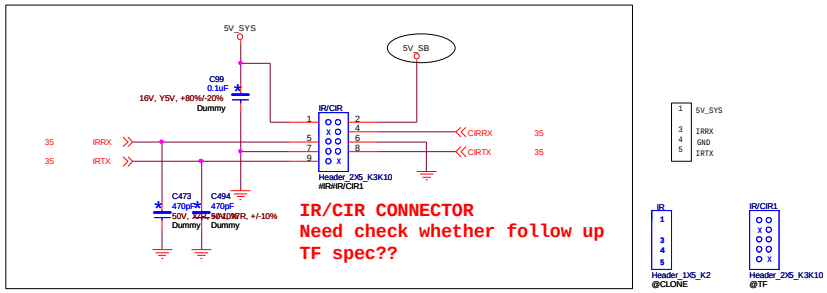
for PCI-E x16/ICH7/LAN/PCI/PCI-E x1/Riser Card/New Card

8,20,22,29 SMB_CLK_MAIN — CP10 X_COPPER — SMB_CLK_RESUME 23,25,30,31 ?

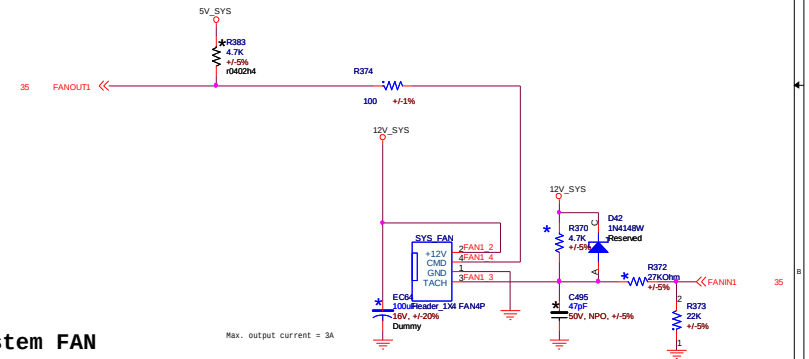
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

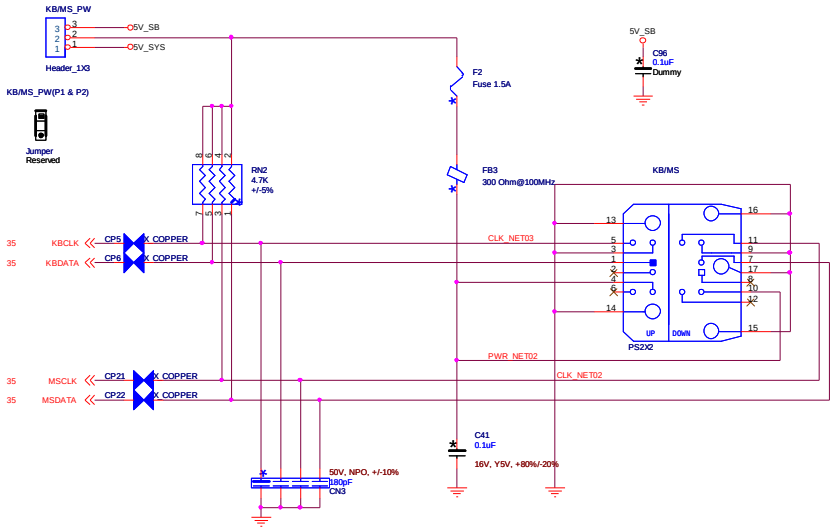
CPU FAN



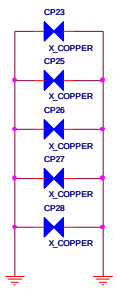


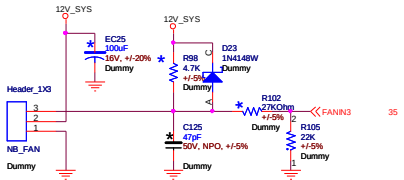
System FAN





KB\MS





NB FAN

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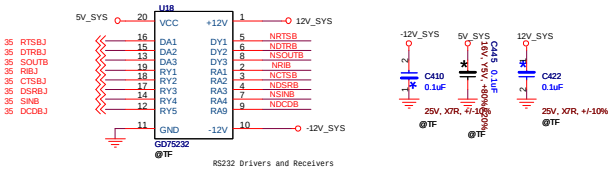
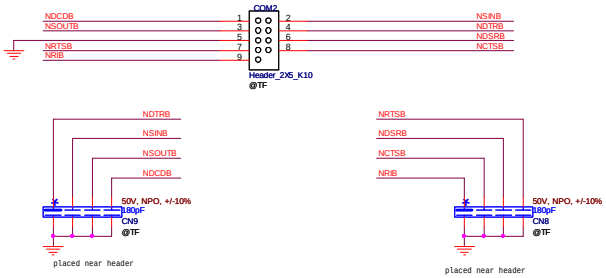
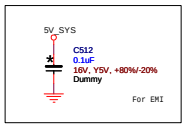
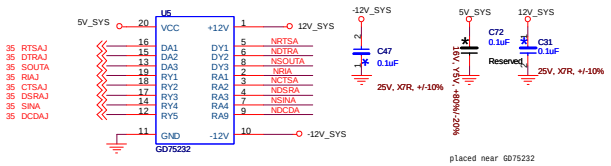
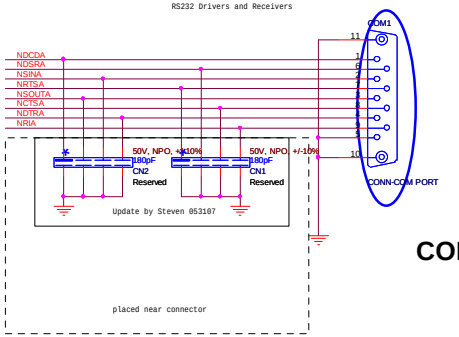




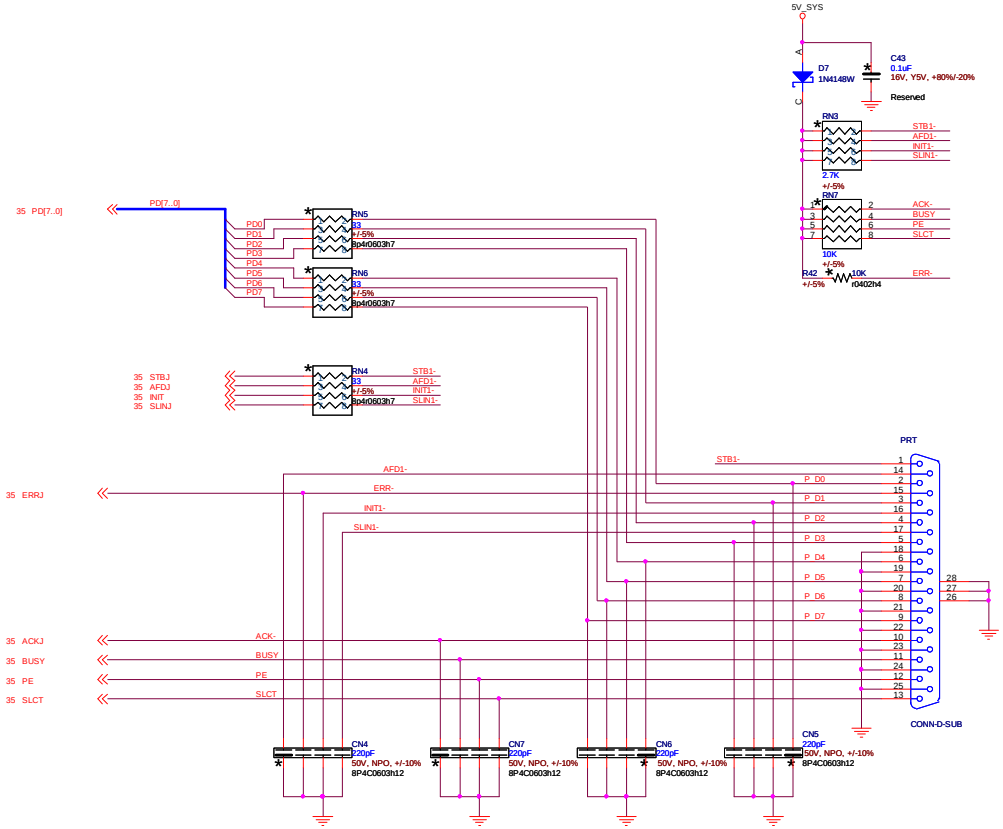
COM 2 Header







COM 1



PRT PORT

Ring

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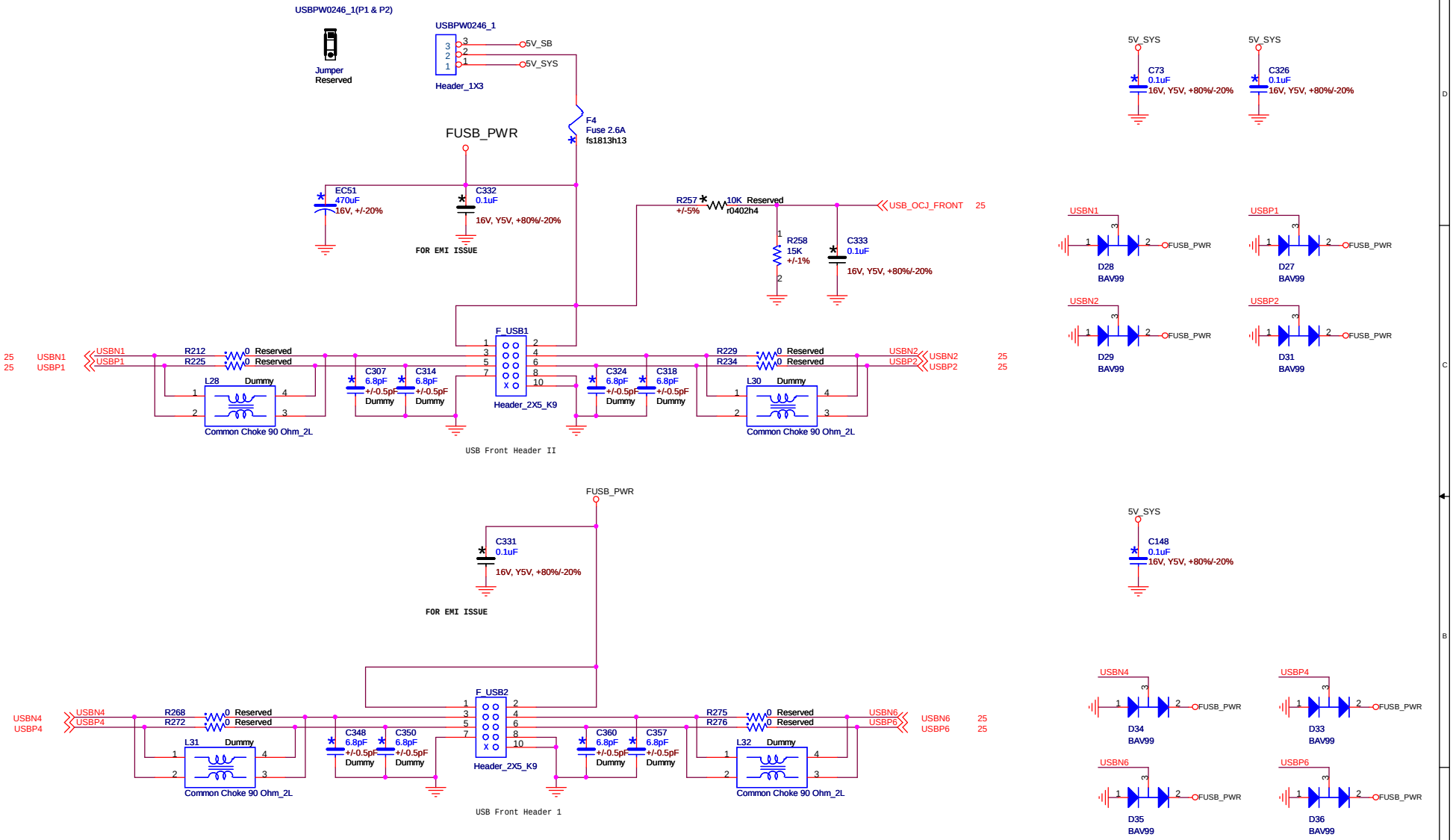

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1. Change Lan RTL8111B colay RTL8101E to RTL8111C colay RTL8101E
2. Change Audio ALC888 colay ALC883 to ALC662 colay ALC888
3. Reserved Memory ratio schematic for over clock.
4. Del R108,C139,Q22,Q20,R107 and then connect VRMPWGD directly for VRD11.
5. Add R371,C501 for power button debounce circuit.
6. Reserved U15,U17 for TF spec.
7. Reserved TPM Header for TF spec.
8. Reserved U3,U6 for TF spec.
9. Add R8,R1,R5,R10,R6,R14,R87,R86,R85,R84,R78,R76,R73,R75,R41,R55 for Audio ESD
10. Reserved CIR function for TF spec.
11. Reserved NB FAN.
12. Reserved C307,C314,C324,C318,C348,C350,C360,C357 for TF Front Panel
13. Change R335 to 91ohm,R337 to 115ohm for Memory Power
14. Remove R338 and stuff R332 for FAN half speed when Power on.
15. Reserved R46 for realtek's suggestion
16. Reserved U9,C144,C145 for VCCA_DAC
17. Add RT8111B SCH
18. Del EC72,EC55,EC54,EC73 for placement issue
19. Reserved R40,R25 For EMI
21. Add C16,C17 For RTL8111B LAN Chip EMI
22. Add FB22 For ITE suggestion
23. Reserved C497 for Front Panel ESD
24. Del Power V15SFR SCH
25. Add R208,R220 for further CPU
26. Reserved R321,R109,R320 for PCI RST
27. Disconnect SLP_S4 with CLK Gen
28. Change C368,C371 from 18pF to 12pF
29. Change F_AUDIO Pin7 connect to Audio_GND directly and connect Pin6,Pin10 to codec through the resistor.

After Gerber Out:

30. Reserved C506
31. Change R363 size from 0402 to 0603
32. Change R111 to 33ohm 1%
33. Add R400 100ohm 1%
34. Dummy Q24 C146
35. Reserved R94 In 8KS2H SKU
36. Reserved R114,C147,R110,Q23,Q26
37. Change R116,R118 to 10K 1%
38. Change C160 to 1uF 0603
39. Reserved Q39
40. Del CP2
41. Del EC29
42. Reserved R356
43. Change PCIe_16x slot to 2EG48211-S7Y-4F
44. Del EC65,EC66
45. Add EC68
46. Change L25,L38 to 630307400-176-G
47. Reserved C451,C396,C375,C381,C430,C441,C355,C436,C447,C448,C397,C385,C446,C427,C405,C401,C395,C353,C390
48. Del RN17
49. Add R401,R402,R403 10K 5%
50. Add JP1,JP2, JP1(P1&P2),JP2(P1&P2)
51. Add R404 470ohm
52. Add EC69
53. Del EC46,EC47
54. Change L26,L37 to APL1108P-2R5L
55. Change C5,C6,C7 to 10pf
56. Change L8,L9,L10 to GL1608082NJT
57. Reserved C38,C65
58. Change CP14 to L40 10uH
59. Change L23 to 10uH
60. Add C139,C513,C514 10uF
61. Add EC65
62. Del CP24
63. Add R25 for EMC
64. Add R409,R410,R411 for Audio codec ESD protection
65. Change EC55 to 680uF
66. Change L23 From 10uH Inductor to 10ohm Resistor

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