ZZZ

PCB EH5AW LA-G521P LS-G521P 02
DAZ2CE00100

ZZZ

HDMI LOGO LOGO@
RO0000003HM

ZZZ X4E@

SMT EMC AG521 EH5AW
X4EAD5BOL01

ES2

UC1

S IC FJ8068404000016 QQAU W0 1.6G BGA
QQAU@
SA0000C1620

UC1

S IC FJ8068403999819 QQAT W0 1.8G BGA 1528
QQAT@
SA0000C1520

ES1

UC1

S IC FH8068403419526 QPHY D0 1.4G BGA
QPHY@
SA0000BX100

QS

UC1

S IC FJ8068404064702 QQK9 W0 2.1G BGA
QQK9@
SA0000C6R20

UC1

S IC FJ8068404064604 QQTG W0 1.6G BGA
QQTG@
SA0000C6Q20

UC1

S IC FJ8068404064403 QQK6 W0 1.8G BGA
QQK6@
SA0000C6P20

preMP

UC1

S IC FJ8068404064702 SRD1V W0 2.1G ABO!
8145@
SA0000C6R60

UC1

S IC FJ8068404064604 SREJQ W0 1.6G ABO!
8265@
SA0000C6Q60

UC1

S IC FJ8068404064405 SREJP W0 1.8G ABO!
8565@
SA0000C6P60

Compal Confidential

EH5AW MB Schematic Document

LA-G521P

Rev: 1A

2018.03.09

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Cover Sheet

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HDMI x 4 lanes

eDP

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eDP

DDI

Intel Whiskey lake U

Whiskey lake U

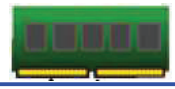
Processor

Quad Core + GT2

15W
15 28 pin BGA
page 07~18

Memory BUS
Dual Channel
1.2V DDR4 2133/2400

260pin DDR4-SO-DIMM X1



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260pin DDR4-SO-DIMM X1

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Nvidia N16S-GTR /
N17S-G0,G1,G2
with GDDR5 x2
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PCIe 3.0 x 4
8GT/s
port 1-4

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PCIE 3.0 x4
8GT/s
Port 9-12

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Base-U PCI 2.0
Premium-U PCI 3.

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USB3 port 1
USB2 port 1

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USB 2.0
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CMOS
Camera
USB2 port 7

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USB2 port2

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USBx8 48MHz

HD Audio 3.3V 24MHz

SPI

NGFF
WLAN
support CNVi
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PCIe 1.0
2.5GT/s
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PCIe 1.0
2.5GT/s
port 5

LAN(GbE)
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LPC/eSPI BUS
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9USB2 port 6
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Int. DMIC
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Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 5 (FP)

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RTC CKT.
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Power On/Off CKT.
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DC/DC Interface CKT.
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Power Circuit DC/DC
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Fan Control
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Sub Board

LS-G521
IO/B
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Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Tuesday, January 22, 2019	Sheet 2 of 57		

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1(EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	0.2(DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	1.0(PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.A(MP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.05VALW_PRIM	+1.05V Always power rail	ON	ON	ON*1
+1.05V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.05VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VS_1.0VSDGPU	+1.05VS power rail for N16X/ +1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+3VS_1.8VSDGPU_AON	+3VS power rail for N16X/ +1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+3VS_1.8VSDGPU_MAIN	+3VS power rail for N16X/ +1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON*2	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
Acer BYOC	BYOC@ / NBYOC@
CODEC	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
LAN Mode Select	SWR@ / LDO@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
CPU Selection	U42@/U22@
DGPU Serial Select	N16X@/N17S@
TPM	TPM@
Finger Print	FP@/FPEMC@/ETU@
Finger print power	FP3V@/FP5V@
UMA or DGPU	UMA@/VGA@

BOM Option Table

Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
N16SGTR or N17SG1	N16SGTR@ / N17SG1@
G Sensor	GSEN@
For over 3 cell battery	3S@
BOM Select	X76@
VRAM BOM Select	X7604@ ~ X7609@
VPRO SKU	VPRO@
CPU Code	8145@ 8265@ 8565@

43 level BOM table

43 Level	Description	BOM Structure
431AD5BOL18	SMT MB AG521 EH5AW I38145U UMA HDMI	DAZ@/8145@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/MP@/X4E@/RTC@
431AD5BOL19	SMT MB AG521 EH5AW I58265U UMA HDMI	DAZ@/8265@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/MP@/X4E@/RTC@
431AD5BOL20	SMT MB AG521 EH5AW I78565U UMA HDMI	DAZ@/8565@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/MP@/X4E@/RTC@
431AD5BOL21	SMT MB AG521 EH5AW I38145U N16 HDMI	DAZ@/8145@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N16X@/N16SGTR@/X7605@/MP@/X4E@/RTC@
431AD5BOL22	SMT MB AG521 EH5AW I58265U N16 HDMI	DAZ@/8265@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N16X@/N16SGTR@/X7605@/MP@/X4E@/RTC@
431AD5BOL23	SMT MB AG521 EH5AW I78565U N16 HDMI	DAZ@/8565@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N16X@/N16SGTR@/X7605@/MP@/X4E@/RTC@
431AD5BOL24	SMT MB AG521 EH5AW I38145U N17 HDMI	DAZ@/8145@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG1@/N17X76@/MP@/X4E@/RTC@
431AD5BOL25	SMT MB AG521 EH5AW I58265U N17 HDMI	DAZ@/8265@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG1@/N17X76@/MP@/X4E@/RTC@
431AD5BOL26	SMT MB AG521 EH5AW I78565U N17 HDMI	DAZ@/8565@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG1@/N17X76@/MP@/X4E@/RTC@
431AD5BOL27	SMT MB AG521 EH5AW I38145U N16 V6 HDMI	DAZ@/8145@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N16X@/N16SGTR@/X76793BOL03@/MP@/X4E@/RTC@
431AD5BOL28	SMT MB AG521 EH5AW I58265U N16 V6 HDMI	DAZ@/8265@/CNVI@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N16X@/N16SGTR@/X76793BOL03@/MP@/X4E@/RTC@

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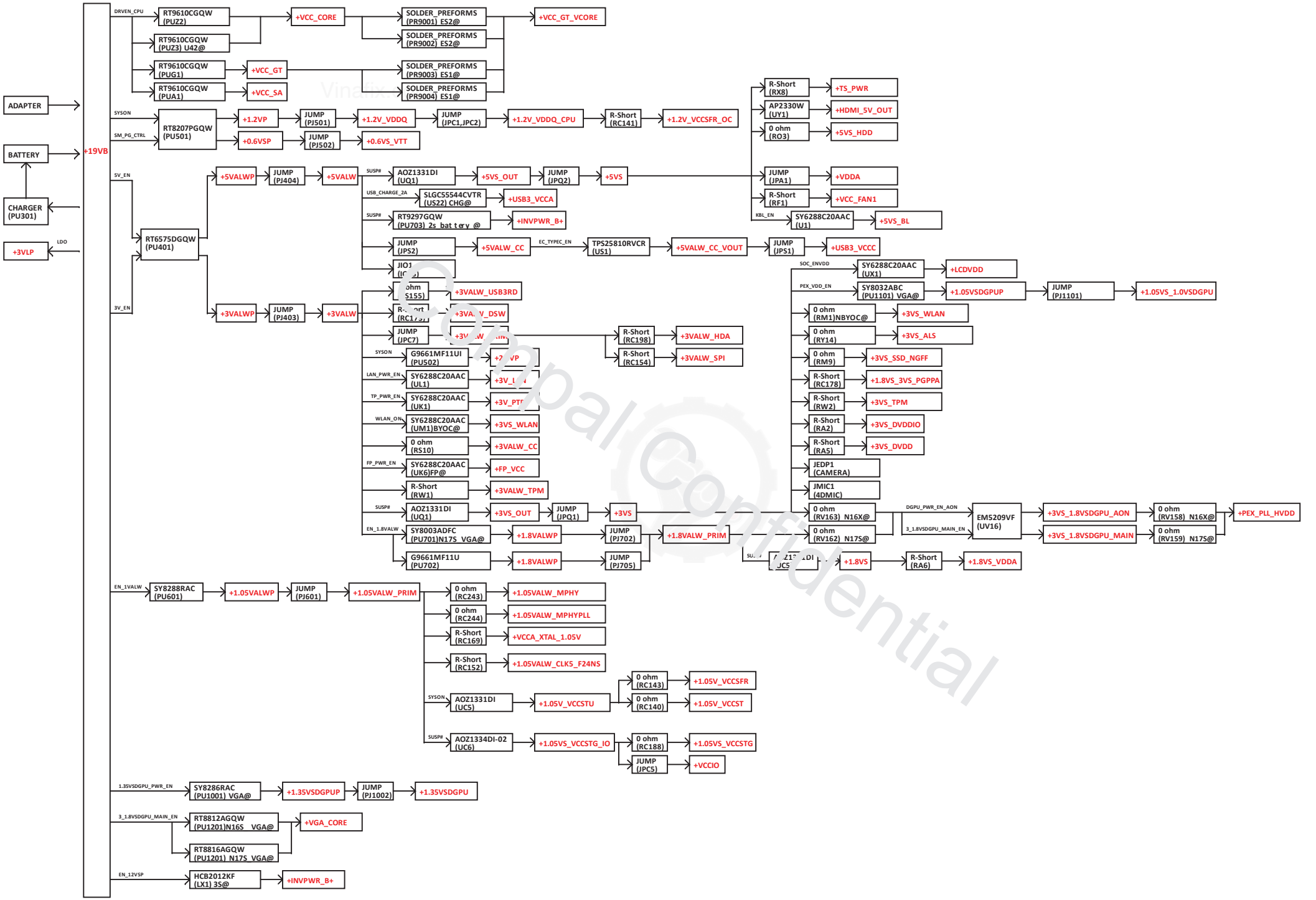
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

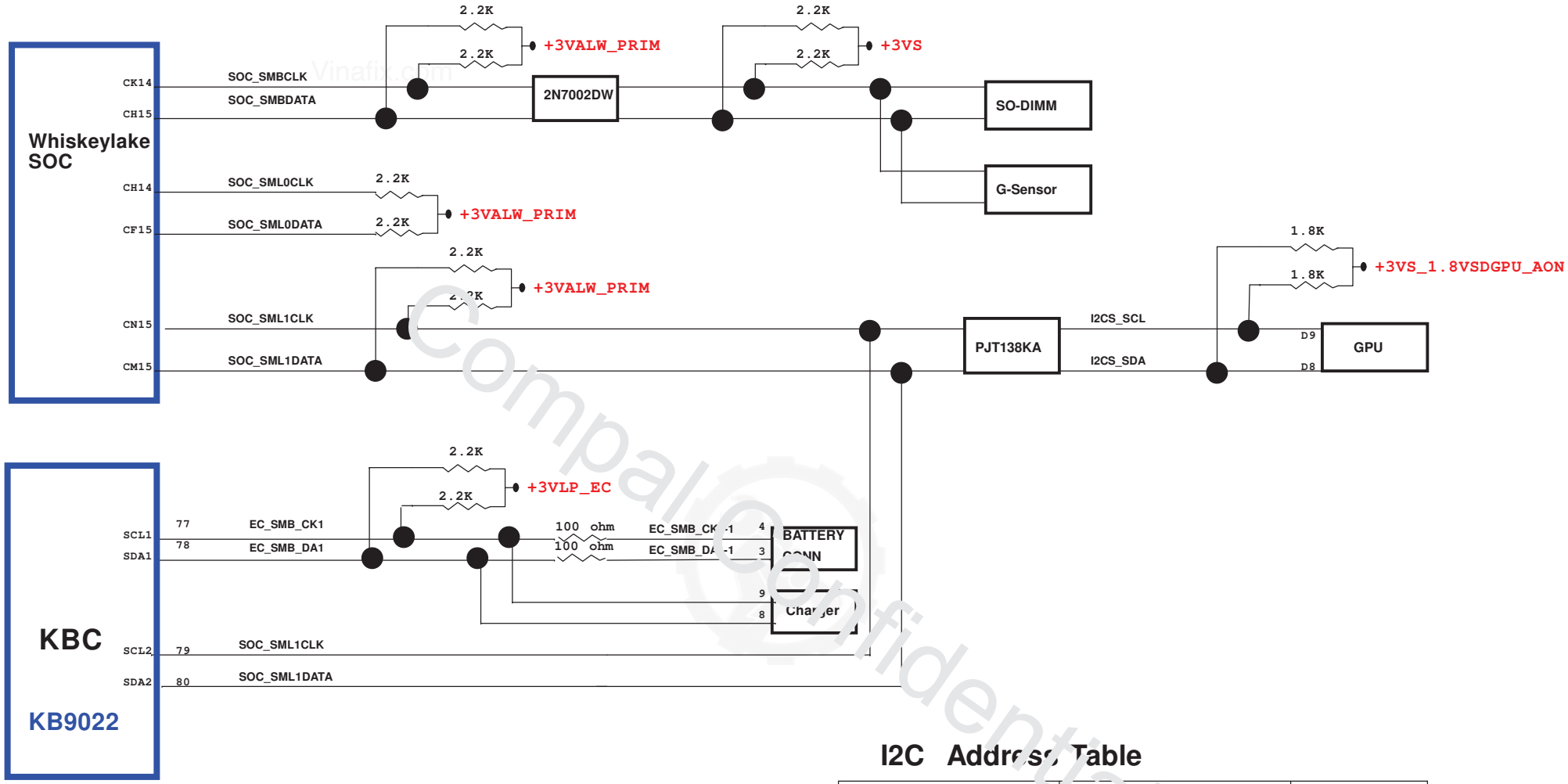
Title: Notes List

Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Friday, August 17, 2018 | Sheet 3 of 57



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date 2018/11/04	Title: Power Rail
			Size: A3 Document Number: EH5AW M/B LA-G521P Rev: 0.1
			Date: Thursday, July 12, 2018 Sheet 4 of 57



I2C Address Table

BUS	Device	Address (8 bit)
I2C_0 (+3VS)	Reserved	
I2C_1 (+3VALW_PRIM)	TM-P2969-001 (TP)	0x2C
	SB8787-1200 (TP-ELAN)	0x15
SOC_SMBCLK (+3VS)	SO-DIMM1	0xA0
	SO-DIMM2	0xA4
	G-Sensor	0x30
SOC_SML1CLK (+3VALW_PRIM)	GPU	0x9E
	EC	
EC_SMB_CK1 (+3VLP)	ISL88739 (Charger IC)	0x12
	BATTERY PACK	0x16

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SMBUS Routing Table

Size	Document Number	Rev
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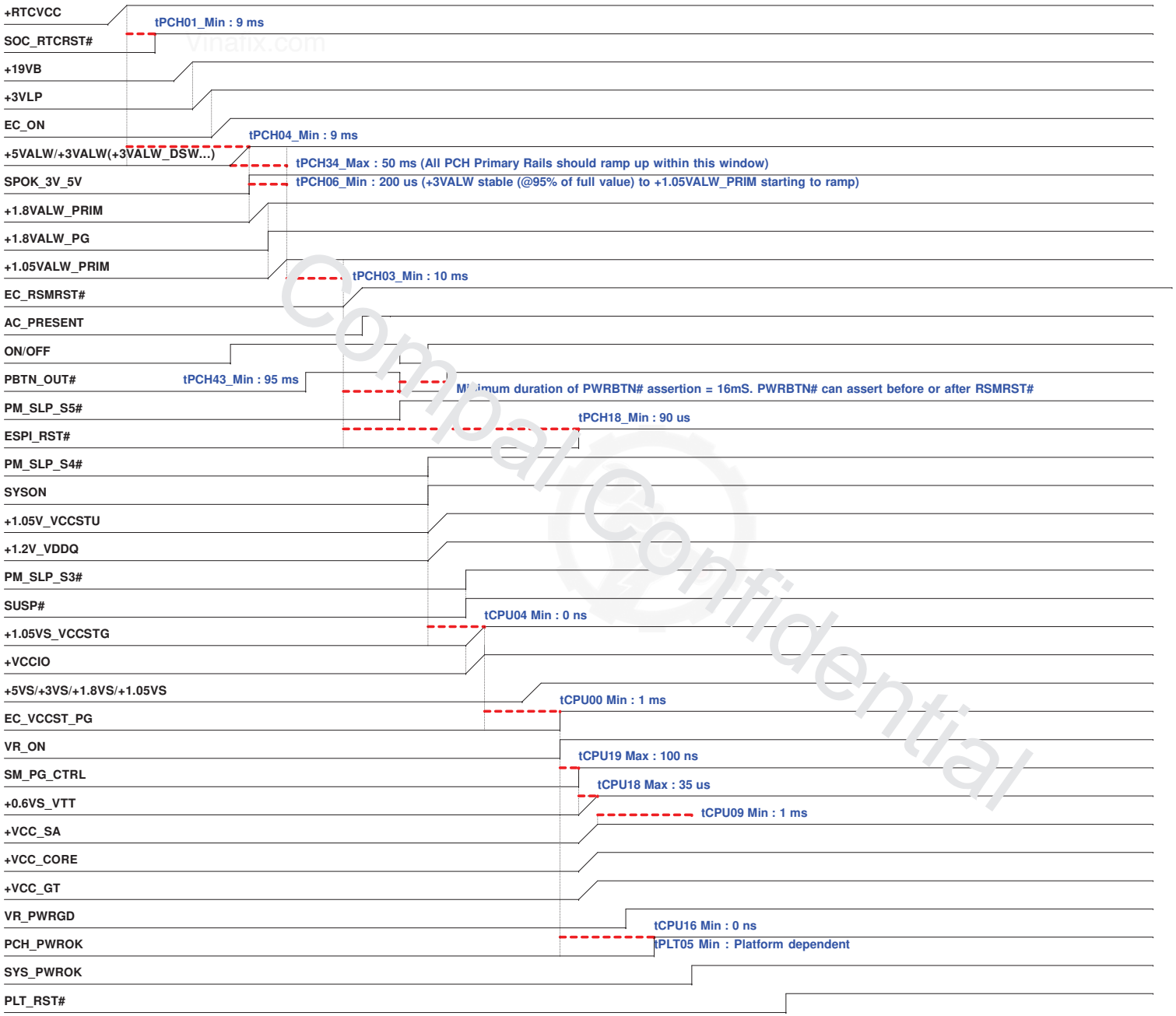
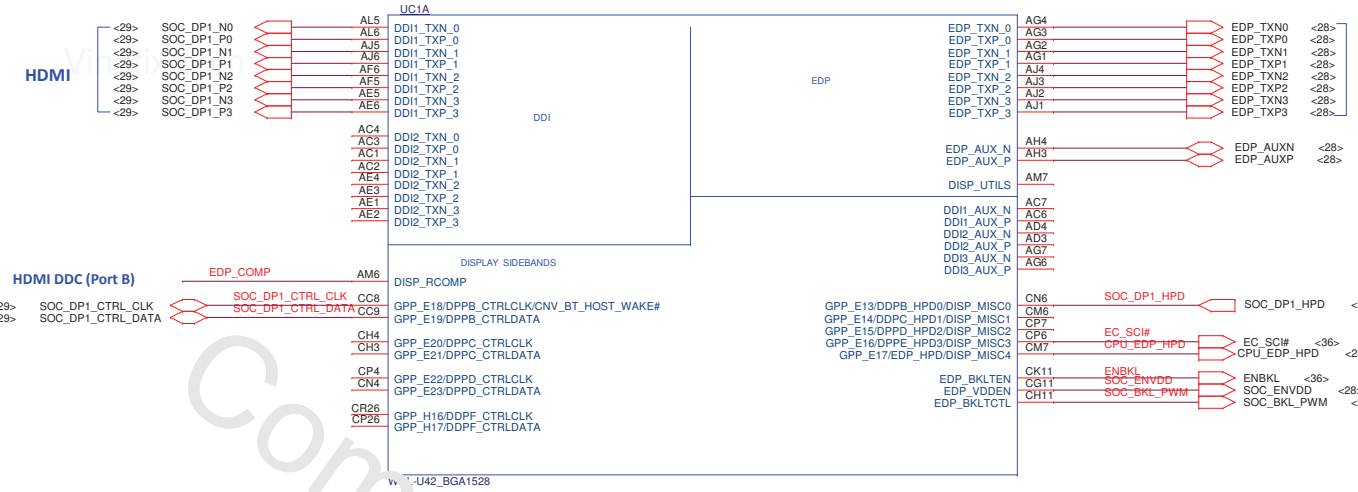
PWR Sequence_WHL-U_DDR4_Value_NON CS



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.		
Title: Power Sequence		
Size: Custom	Document Number: EH5AW M/B LA-G521P	Rev: 0.1
Date: Friday, August 17, 2018	Sheet 6 of 57	

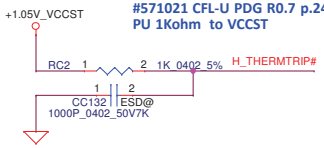


#571021 CFL-U PDG R0.7 p.104

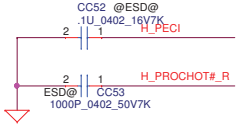
Table 5-13. DDI Disabling and Termination Guidelines

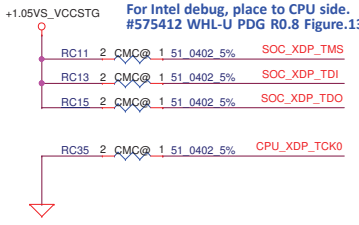
Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

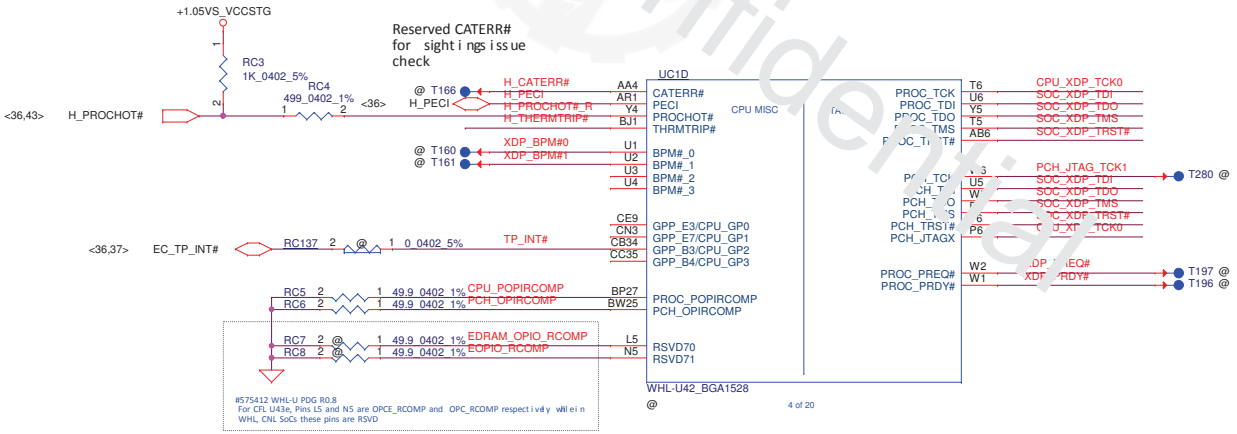
#571021 CFL-U PDG R0.7 p.39
PU 24.9ohm for eDP



#571021 CFL-U PDG R0.7 p.248
PU 1Kohm to VCCST



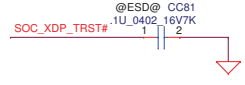




EC_SCI# SOC internal PU

#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:

- GPP_B14 GPP_B20 GPP_B23
- GPP_C [23 : 22]
- GPP_D [4 : 0]
- GPP_E [8: 0], GPP_E [16 : 13]



UC1
S IC FJ8068404000016 QQAU W0 1.6G BGA
QQAU@
SA0000C1620

UC1
S IC FJ8068403999819 QQAT W0 1.8G BGA 1528
QQAT@
SA0000C1520

UC1
S IC FH8068403419526 QPHY D0 1.4G BGA
QPHY@
SA0000BX100
ES1

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: WHL-U(1/12)DDI,MSIC,XDP,EDP

Size	Document Number	Rev
Custom	EH5AW M/B LA-G521P	0.1

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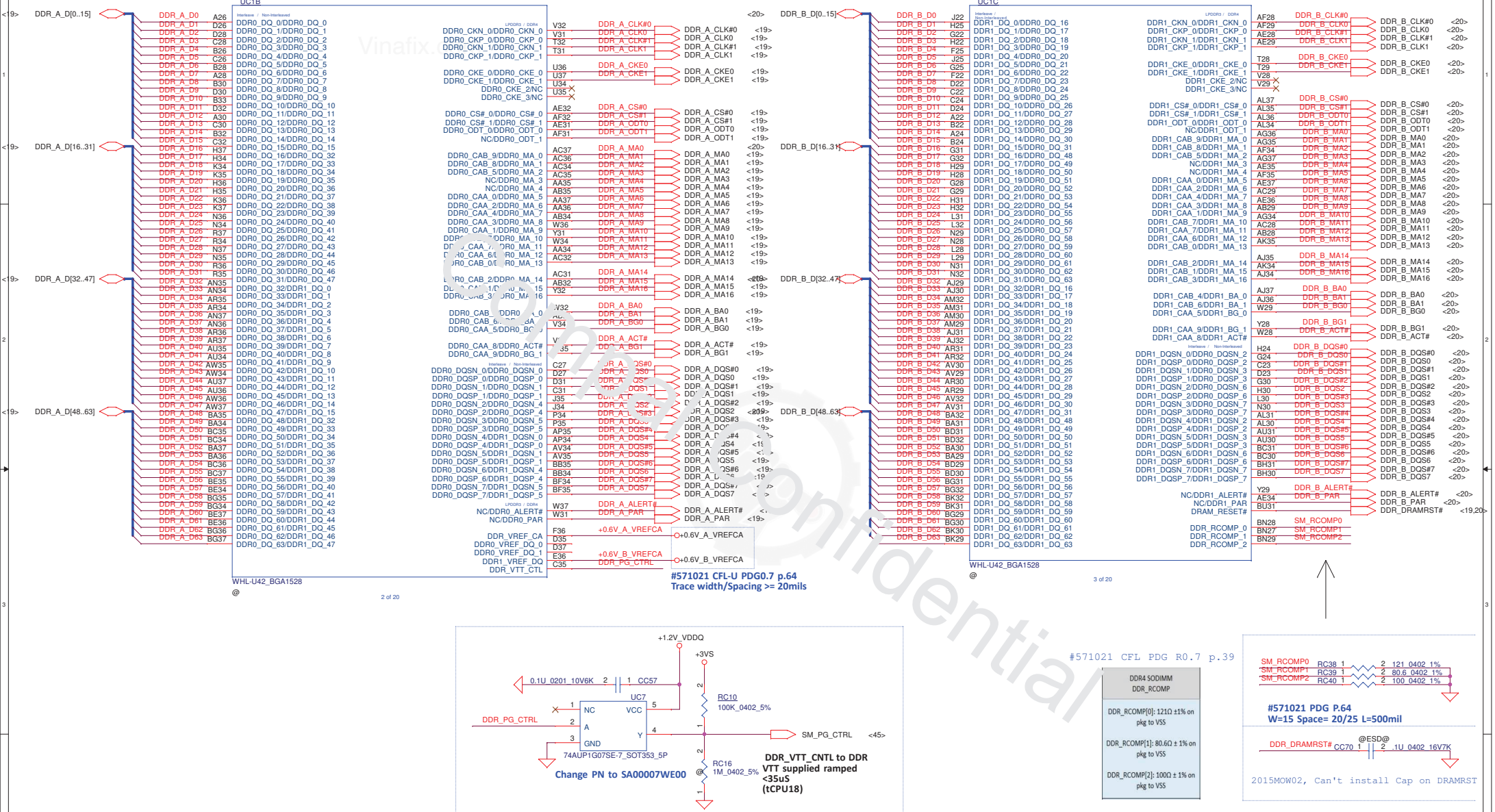
Interleaved Memory



Security Classification	Compal Secret Data		
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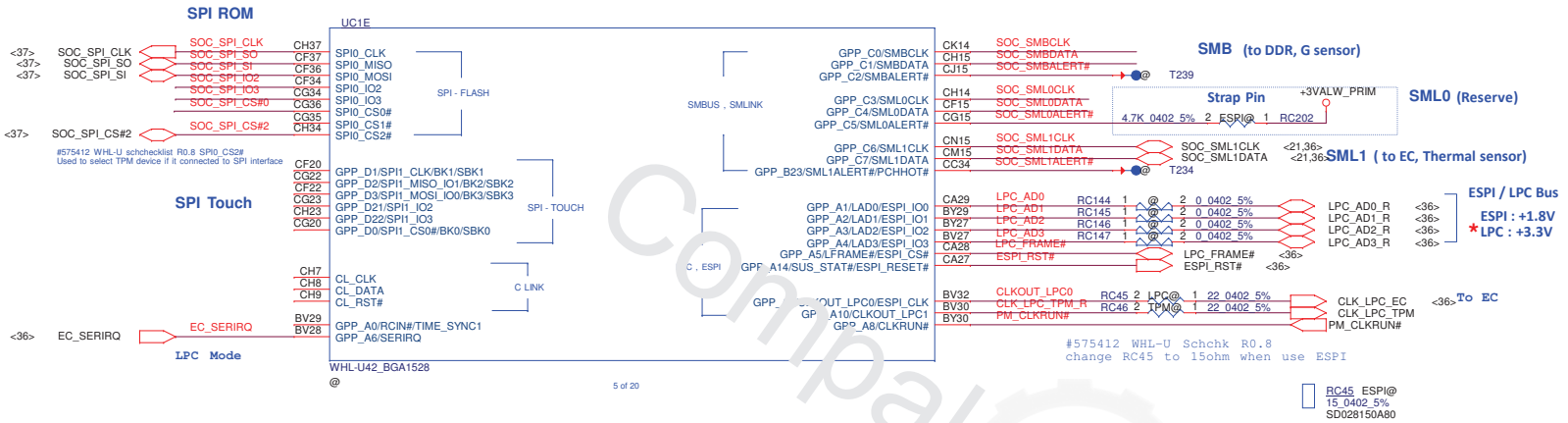
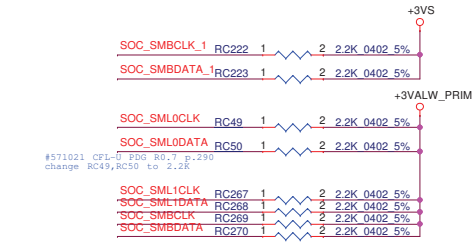
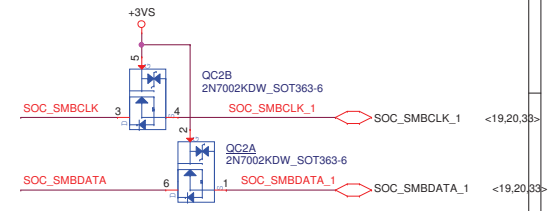
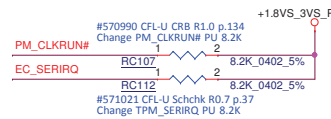
Compal Electronics, Inc.			
Title	WHL-U(2/12)DDR4		
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, July 12, 2018	Sheet 8 of 57		







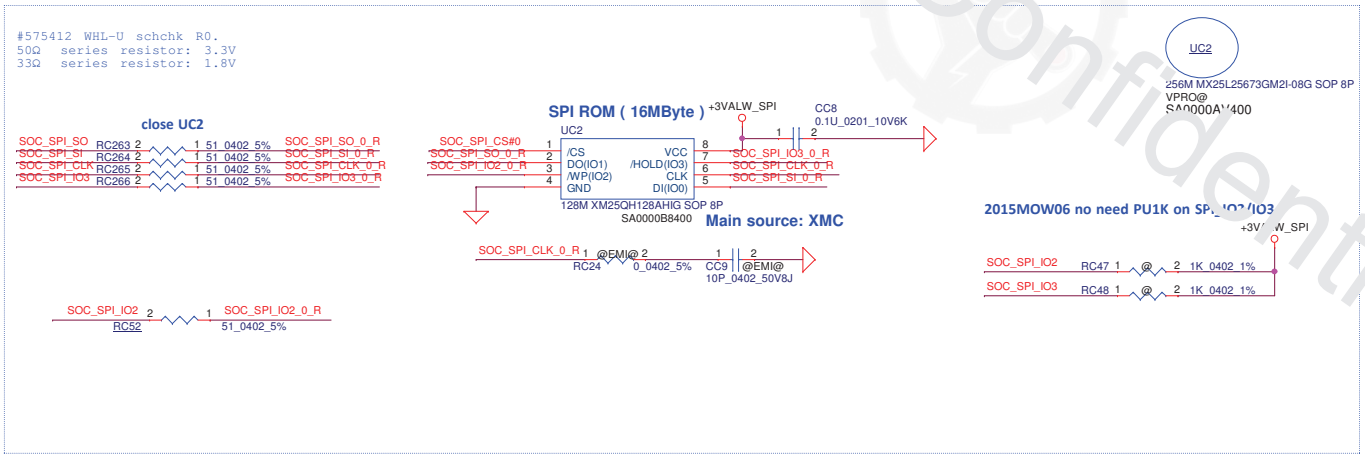


SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
***0 = LPC is selected for EC --> For KB9022/9032 Use**
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

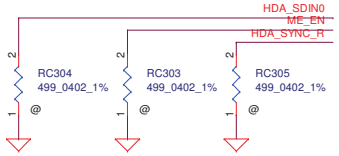
TLS Confidentiality
***0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)**
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



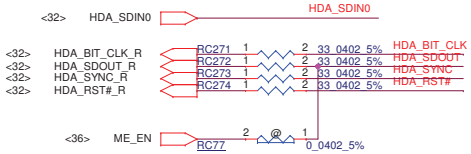
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	WHL-U(3/12)SPI,ESPI,SMB,LPC		
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, July 12, 2018		Sheet 9 of 57	

for PCH leakage voltage issue



HDA for AUDIO



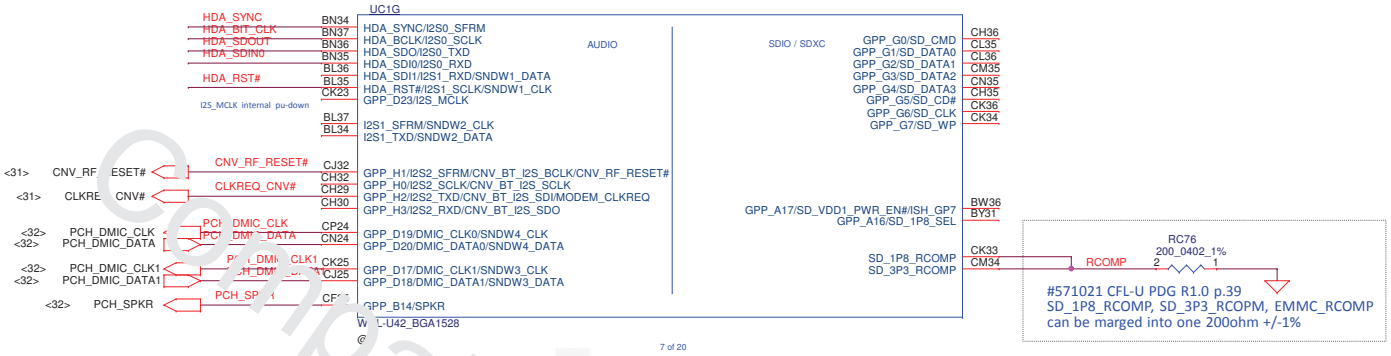
HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures def i nedi nt he fl ash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

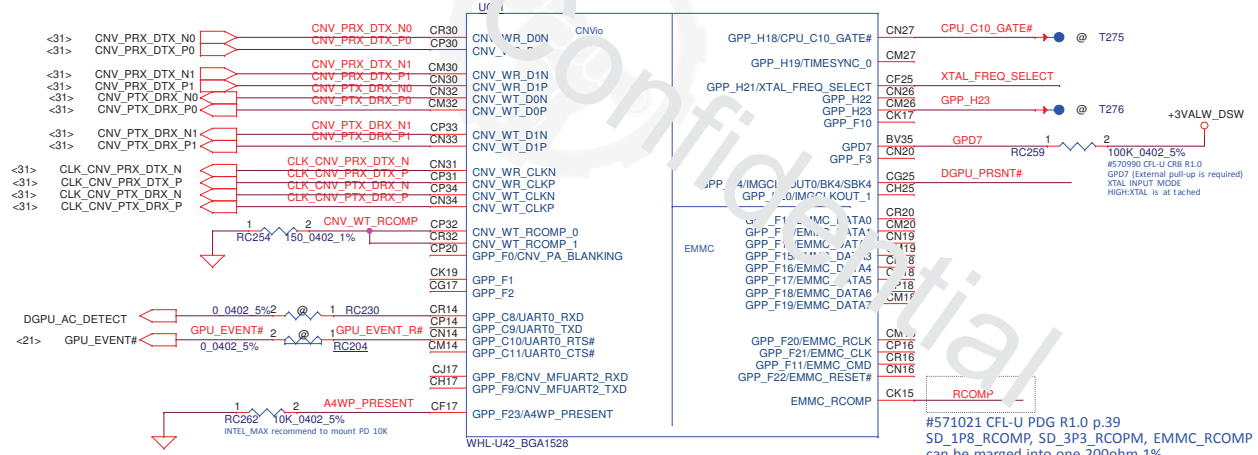
SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

*** TOP Swap Override**
0 = Disable TOP Swap mode.
1 = Enable TOP Swap Mode.

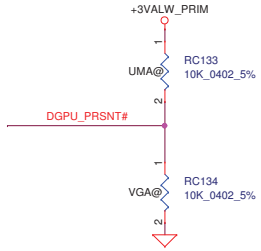
Intel HD Audio link capabilit i es
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



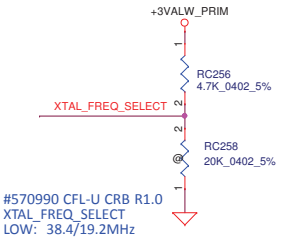
#571021 CFL-U PDG R1.0 p.39
SD_1P8_RCOMP, SD_3P3_RCOPM, EMMC_RCOMP can be marged into one 200ohm +/-1%



#571021 CFL-U PDG R1.0 p.39
SD_1P8_RCOMP, SD_3P3_RCOPM, EMMC_RCOMP can be marged into one 200ohm 1%



	DGPU_PRSNT#
DIS,Optimus	0
UMA	1



#570990 CFL-U CRB R1.0
XTAL_FREQ_SELECT
LOW: 38.4/19.2MHz
HIGH: 24MHz

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	WHL-U(4/12)HDA,EMMC,SDIO,CNVI		
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, July 12, 2018	Sheet 10 of 57		

#571021 CFL-U PDG R0.7 p.256

+RTCVCC
RC91 20K 0402 5% SOC_SRTCRST#
CC10 1U_0201_6.3V6M
RC93 20K 0402 5% SOC_RTCRST#
CC11 1U_0201_6.3V6M
JCMOS1 @ 0_0603_5% CLR CMOS
Place at RAM DOOR
RC941 1M 0402 5% SM_INTRUDER#

SOC_RTCRST# <36>

+3VS
RC121 10K 0402 5% CLKREQ_PCIE#1
R115 10K 0402 5% CLKREQ_PCIE#0
RC282 10K 0402 5% CLKREQ_PCIE#5
RC281 10K 0402 5% CLKREQ_PCIE#4
RC280 10K 0402 5% CLKREQ_PCIE#3
RC279 10K 0402 5% CLKREQ_PCIE#2

+1.05V_VCCST
From EC(open-drain)
RC113 1K_0402_5%
RC116 60.4_0402_1%
<36,40> EC_VCCST_PG_R EC_VCCST_PG

+3VALW_PRIM
+3VALW_DSW
RC277 10K 0402 5% SYS_RESET#
RC278 10K 0402 5% LAN_WAKE#
RC275 10K 0402 5% PCH_PWROK
RC276 10K 0402 5% EC_RSMRST#
RC110 10K 0402 5% SYS_PWROK

+3VALW_DSW
RC104 1K 0402 5% WAKE#

#575412 WHL-U schchecklist R0.8
1 Kohm pull-up to VCCDSW_3p3.
The pull-up is required even if PCIe* interface is not used on the plat f or m

ESD@ 1000P_0402_50V7K CC131 EC_VCCST_PG
@ESD@ CC51 .1U_0402_16V7K SYS_RESET#
ESD@ 1000P_0402_50V7K CC50 H_CPUPWRGD
ESD@ CC66 .1U_0402_16V7K SYS_PWROK
ESD@ 1000P_0402_50V7K CC65 PCH_PWROK_R
ESD@ CC69 .1U_0402_16V7K EC_RSMRST#

#543016 PDG2.0 P.599
PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the plat f or m

UC1J
CLOCK SINGNALS
DGPU <21> CLK_PCIE_N0 CLK_PCIE_N0 AW2
<21> CLK_PCIE_P0 CLK_PCIE_P0 AY3
<21> CLKREQ_PCIE#0 CLKREQ_PCIE#0 CF32
GLAN <30,38> CLK_PCIE_N1 CLK_PCIE_N1 BC1
<30,38> CLK_PCIE_P1 CLK_PCIE_P1 BC2
<30,38> CLKREQ_PCIE#1 CLKREQ_PCIE#1 CE32
WLAN <31> CLK_PCIE_N2 CLK_PCIE_N2 BD3
<31> CLK_PCIE_P2 CLK_PCIE_P2 BC3
<31> CLKREQ_PCIE#2 CLKREQ_PCIE#2 CF30
M.2/SSD <31> CLK_PCIE_N3 CLK_PCIE_N3 BH3
<31> CLK_PCIE_P3 CLK_PCIE_P3 BH4
<31> CLKREQ_PCIE#3 CLKREQ_PCIE#3 CE31
CLKREQ_PCIE#4 BA1 BA2 CE30
CLKREQ_PCIE#5 BE1 BE2 CF31
CLKOUT_PCIE_N_0 CLKOUT_PCIE_P_0 GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N_1 CLKOUT_PCIE_P_1 GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N_2 CLKOUT_PCIE_P_2 GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N_3 CLKOUT_PCIE_P_3 GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N_4 CLKOUT_PCIE_P_4 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N_5 CLKOUT_PCIE_P_5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN XTAL_OUT
XCLK_BIASREF CLKIN_XTAL
RTCX1 RTCX2
SRTCRST# RTCRST#
AU1 CLK_CPU_ITP# T164 @
AU2 CLK_CPU_ITP T165 @
BT32 SUSCLK SUSCLK <31>
CK3 SOC_XTAL24_IN
CK2 SOC_XTAL24_OUT
CJ1 XCLK_BIASREF
CM3
BN31 SOC_RTCX1
BN32 SOC_RTCX2
BR37 SOC_SRTCRST#
BR34 SOC_RTCRST#
WHL-U42_BGA1528
@ 10 of 20

SOC_XTAL24_IN RC235 1 2 33 0402 1% SOC_XTAL24_IN_R
SOC_XTAL24_OUT RC236 1 2 33 0402 1% SOC_XTAL24_OUT_R
563377 Intel MOW 33
RC92 1M_0402_5%
YC1 24MHZ_18PF_XRCGB24M000F2P51R0
NC NC
CC12 27P_0402_50V8J
CC13 27P_0402_50V8J

REFCLK_CNV <31>
RC255 10K_0402_5%

Follow 2014MOW48
Skylake U PU 2.7k ohm to 1V
Cannonlake U PD 60.4 ohm
+1.05VALW_CLK5_F24NS
XCLK_BIASREF RC96 @ 2.7K_0402_1%
RC136 60.4_0402_1%

XCLK_BIASREF
T:50ohm S:12/15 L:1000 Via:2

+3VALW_PRIM
EXT_PWR_GATE# RC295 100K_0402_5%
PM_SLP_S0# RC296 100K_0402_5%
PM_SLP_S3# RC297 100K_0402_5%
PM_SLP_S4# RC298 100K_0402_5%
PM_SLP_A# RC299 100K_0402_5%
SLP_WLAN# RC300 100K_0402_5%
SLP_SUS# RC301 100K_0402_5%
SLP_LAN# RC302 100K_0402_5%
INTEL WHL-U Schchecklist R0.9

2014MOW48:
Skylake-U use 24M 50 ohm ESR
Cannonlake U use 38.4M 30 ohm ESR
SOC_RTCX2
SOC_RTCX1 RC98 10M_0402_5%
YC2 32.768KHZ_9PF_X1A000141000200
Change PN to SJ10000Q400
CC15 8.2P_50V_0402
CC16 8.2P_50V_0402

UC1K
SYSTEM POWER MANAGEMENT
<36,37> PLT_RST# PLT_RST# BJ35
GPP_B13/PLTRST#
SYS_RESET# CN10
EC_RSMRST# BR36
<36> EC_RSMRST# RSMRST#
T95 @ H_CPUPWRGD AR2
EC_VCCST_PG BJ2
PROCPWRGD
VCCST_PWRGOOD
T89 @ SYS_PWROK CR10
PCH_PWROK_R BP31
RC20 10_0402_5% PCH_PWROK BP30
PCH_DPWROK
SYS_PWROK
PCH_PWROK
DSW_PWROK
<36,40> SYS_PWROK
<36,40> PCH_PWROK
<36> SUSPWRDNACK SUSPWRDNACK BV34
SUSACK# BV32
T92 @
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE# BU30
LAN_WAKE# BU32
GPD2/LAN_WAKE# BU34
GPD11/LANPHYPC
WAKE#
GPP_B12/SLP_S0# BJ37 PM_SLP_S0# PM_SLP_S0# <36,37>
GPD4/SLP_S3# BU36 PM_SLP_S3# PM_SLP_S3# <36,40>
GPD5/SLP_S4# BU27 PM_SLP_S4# PM_SLP_S4# <36,40>
GPD10/SLP_S5# BT29 PM_SLP_S5# @ T84
SLP_SUS# BU29 SLP_SUS# @ T90
SLP_LAN# BT31 SLP_LAN# @ T87
SLP_WLAN# BT30 SLP_WLAN# SLP_WLAN# <36>
PM_SLP_A# BU37 PM_SLP_A# PM_SLP_A# <36>
PBTN_OUT#_R BU28
AC_PRESENT BU35 AC_PRESENT AC_PRESENT <36>
PM_BATLOW# BV36
SM_INTRUDER#
EXT_PWR_GATE#
VRALERT# CC36
@ T93
INPUT3VSEL
WHL-U42_BGA1528
@ 11 of 20

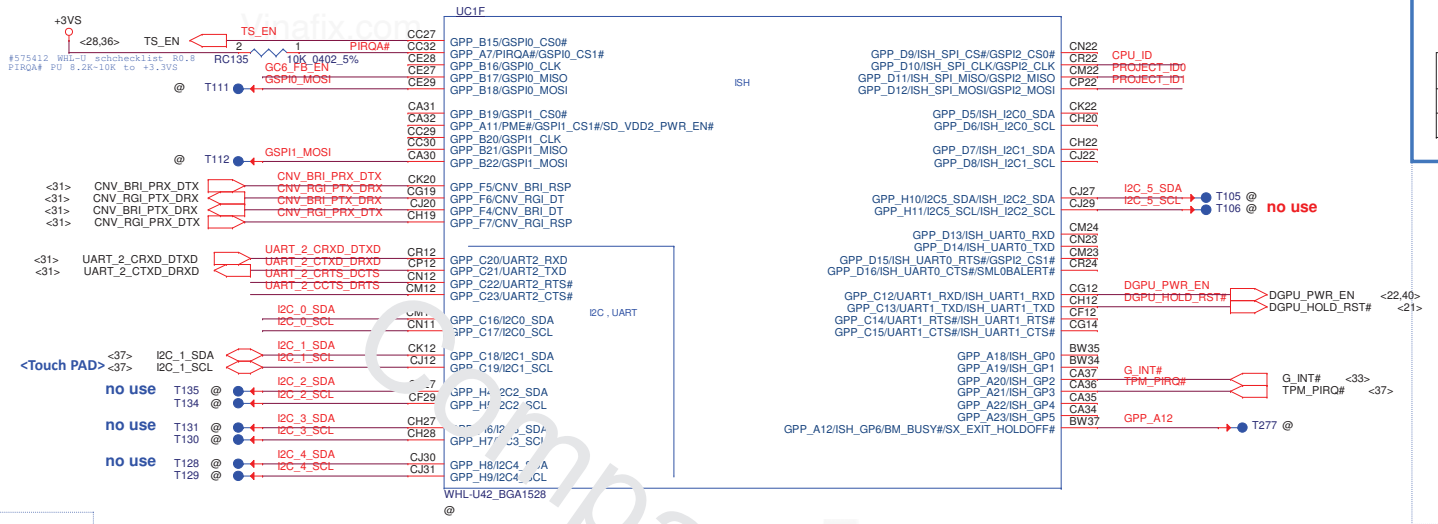
PCH internal PU
PBTN_OUT#_R RC111 @ 100K_0402_5%
EC internal PU
AC_PRESENT RC106 @ 10K_0402_5%
PM_BATLOW# RC103 10K_0402_5%
Default : GPI
SOC_VRALERT# RC115 @ 10K_0402_5%

PCH PLTRST Buffer
<36> PBTN_OUT# RC109 @ PBTN_OUT#_R 0_0402_5%
EC_RSMRST# RC114 @ PCH_DPWROK 0_0402_5%
SYS_PWROK RC122 @ PCH_PWROK 0_0402_5%
PLT_RST# UC3 MC74VHC1G08DFT2G_SC70-5 PLT_RST_BUF# PLT_RST_BUF# <21,30,31,38>
RC118 100K_0402_5%
RC125 @ 0_0402_5%
PLT_RST_BUF# CC130 100P_0402_50V8J ESD@
Reserved for ESD place near UC2.1

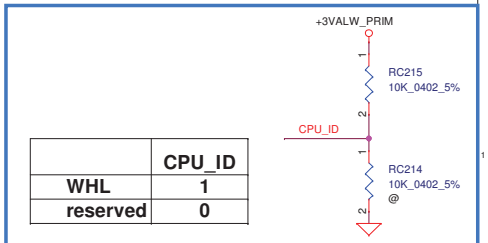
+3VALW_DSW
RC260 @ 4.7K_0402_5%
INPUT3VSEL
#570990 CFL-U CRB R1.0
INPUT3VSEL
L : supply is 3.3V +- 5%
H : supply is 3.0V +- 5%
RC261 4.7K_0402_5%

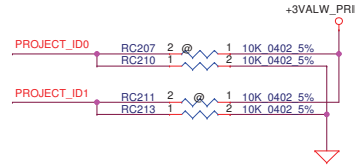
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.
Title: WHL-U(5/12)CLK,GPIO
Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1
Date: Thursday, July 12, 2018 | Sheet 11 of 57

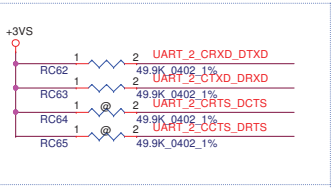


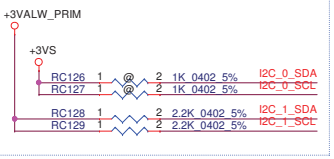
	CPU_ID
WHL	1
reserved	0

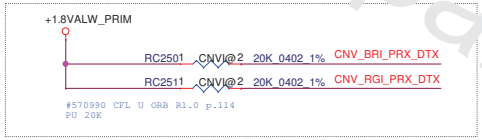


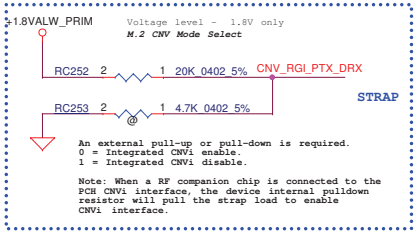


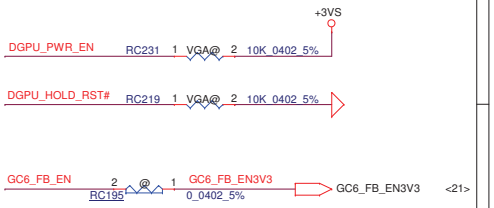
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* EH5AW	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1











Functional Strap Definitions

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

***0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
***0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

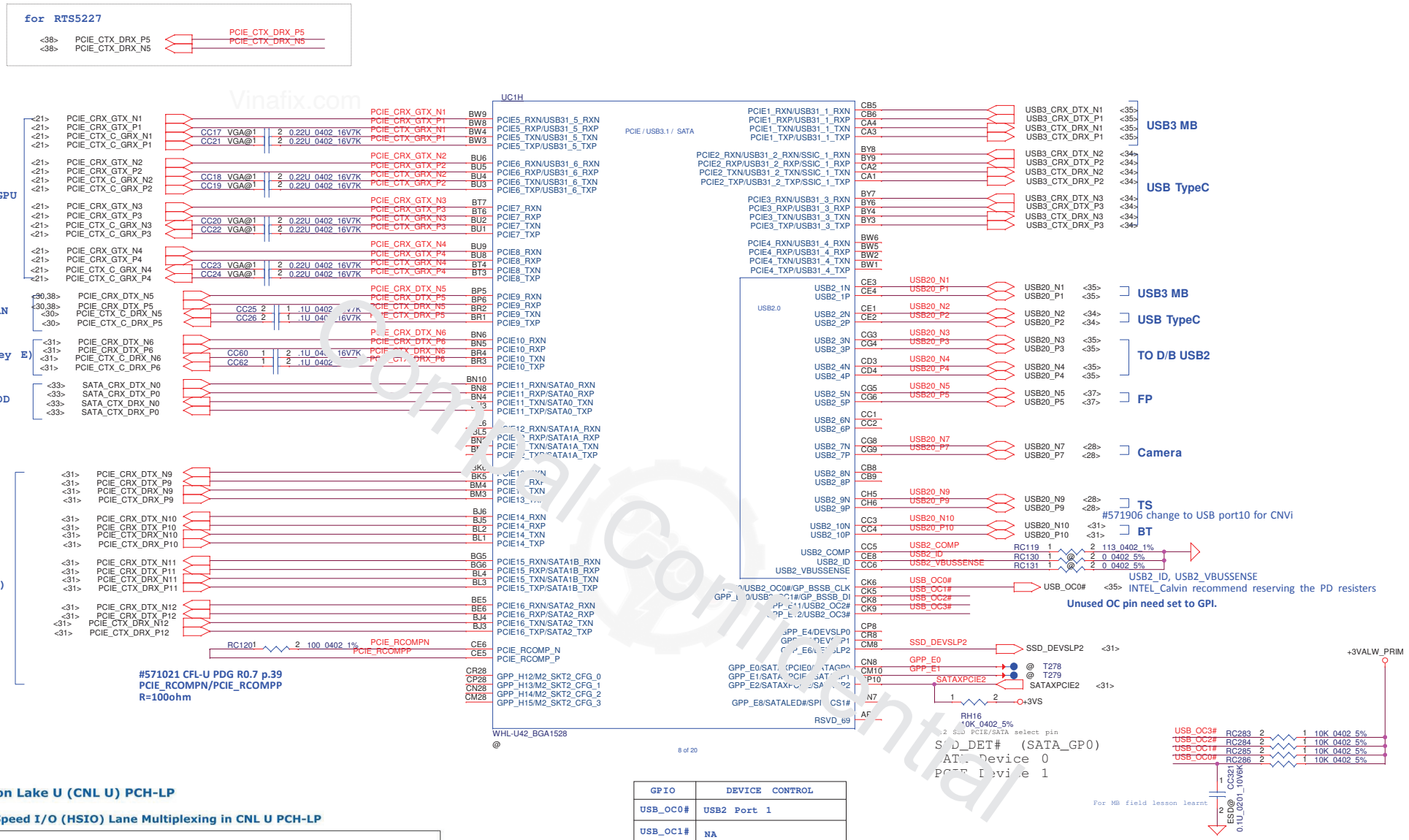
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: WHL-U(6/12)GPIO

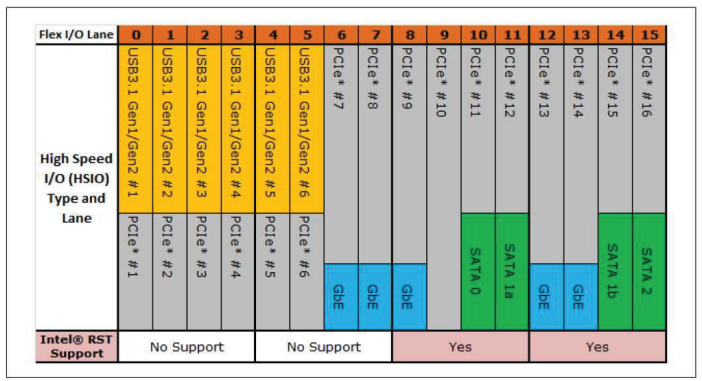
Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Thursday, July 12, 2018 | Sheet 12 of 57



6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

- When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL U.

These signals can be configured as interlock switch inputs corresponding to a given SATA port.

- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.

If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

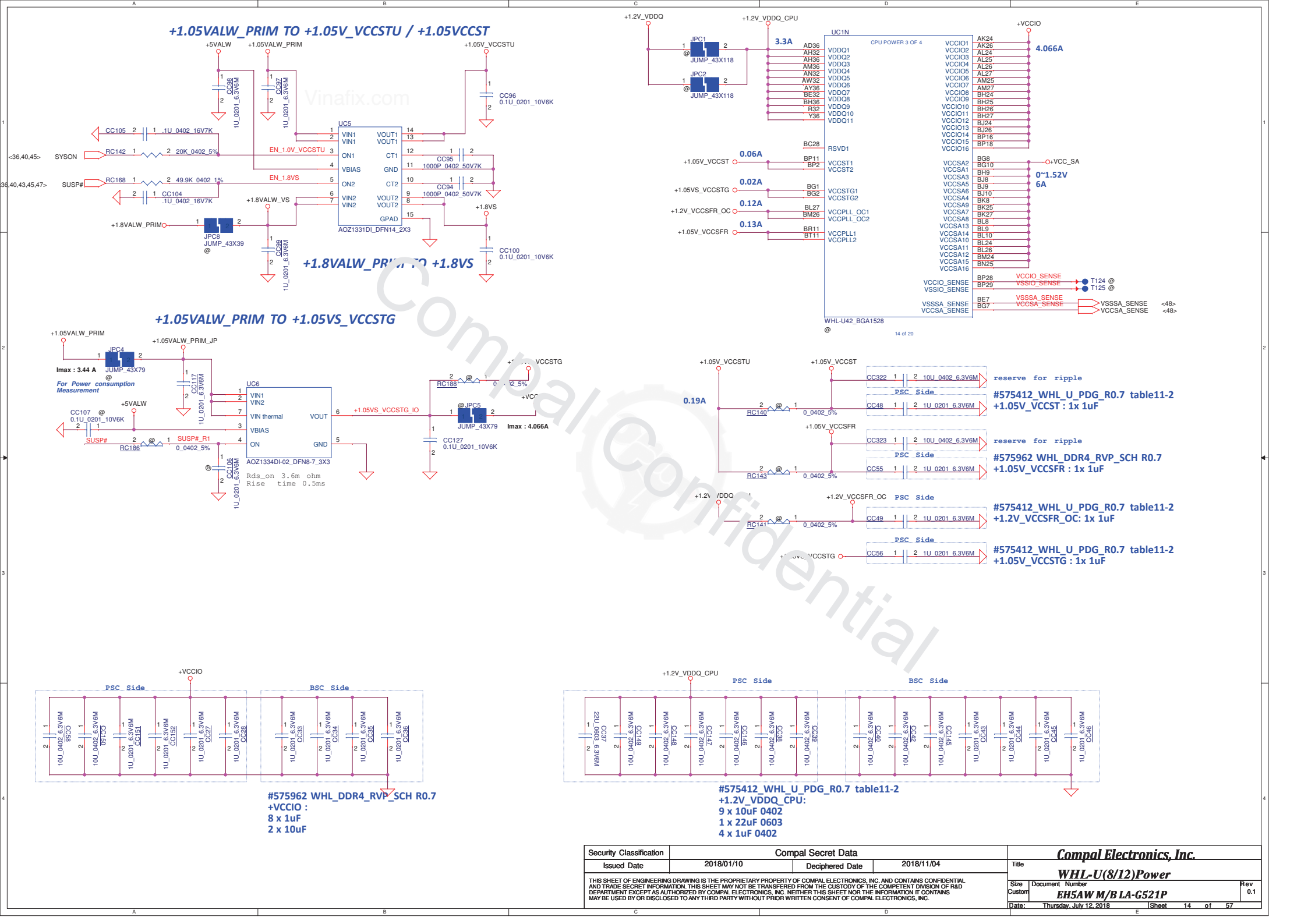
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: WHL-U(7/12)PCIE,USB,SATA

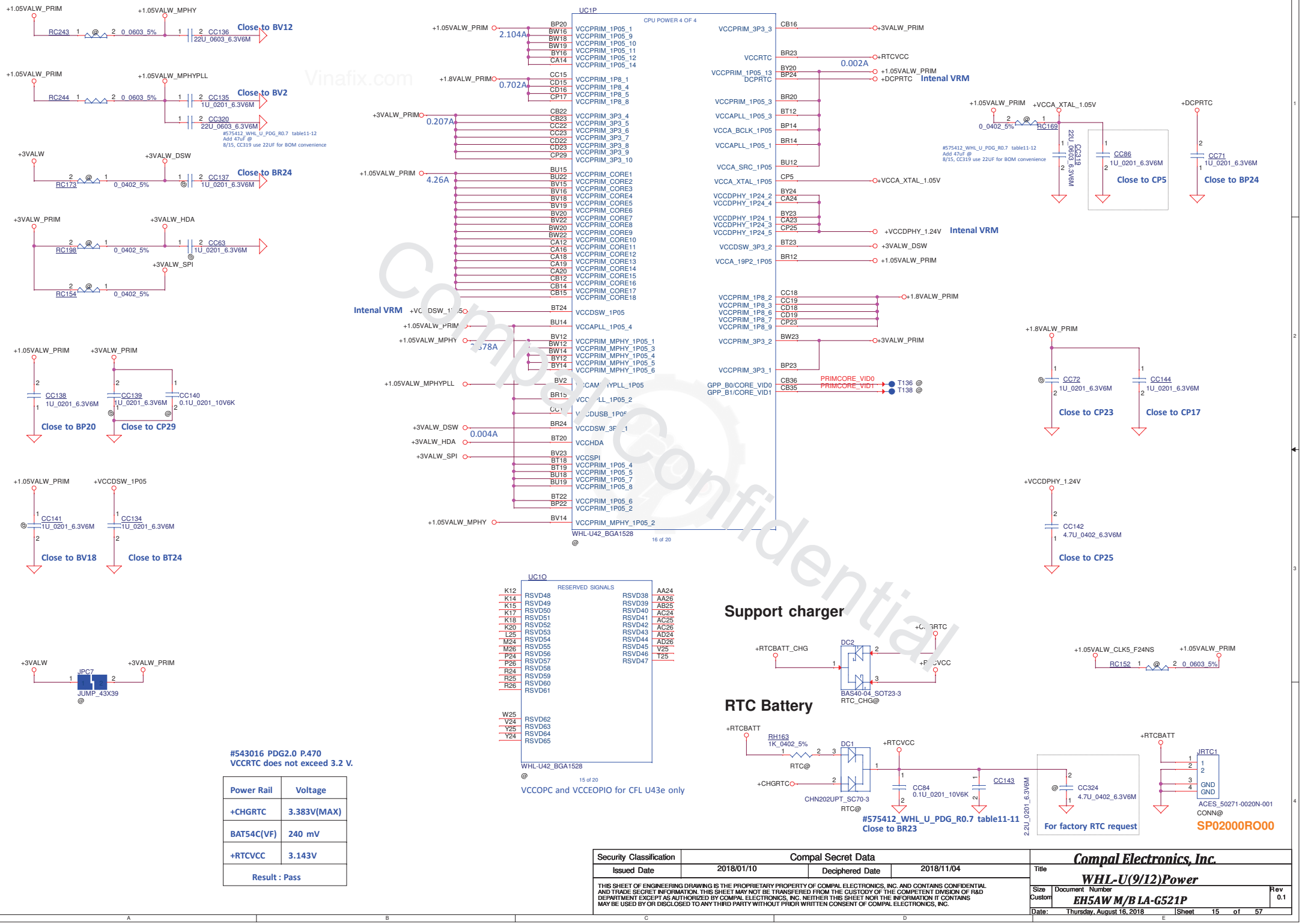
Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Thursday, July 12, 2018 | Sheet 13 of 57



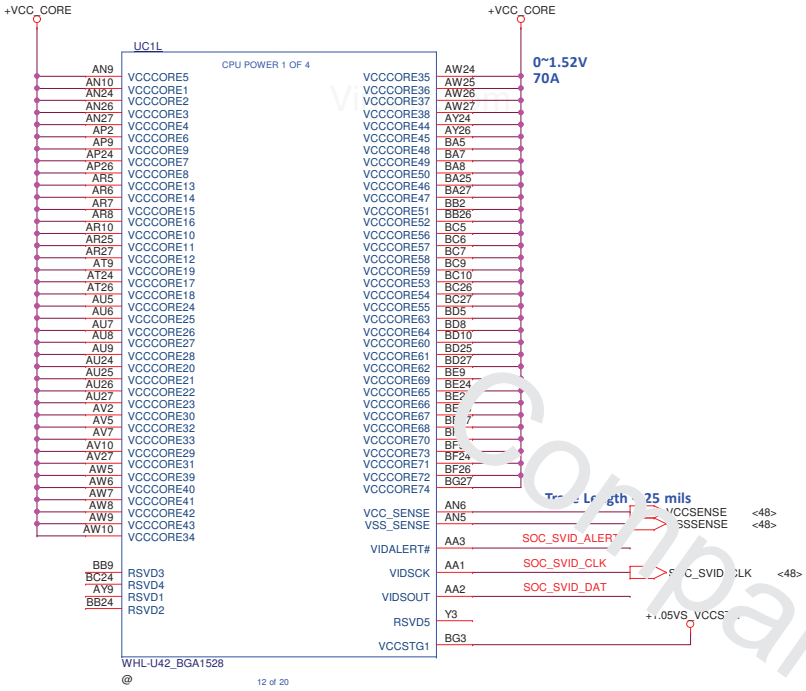
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

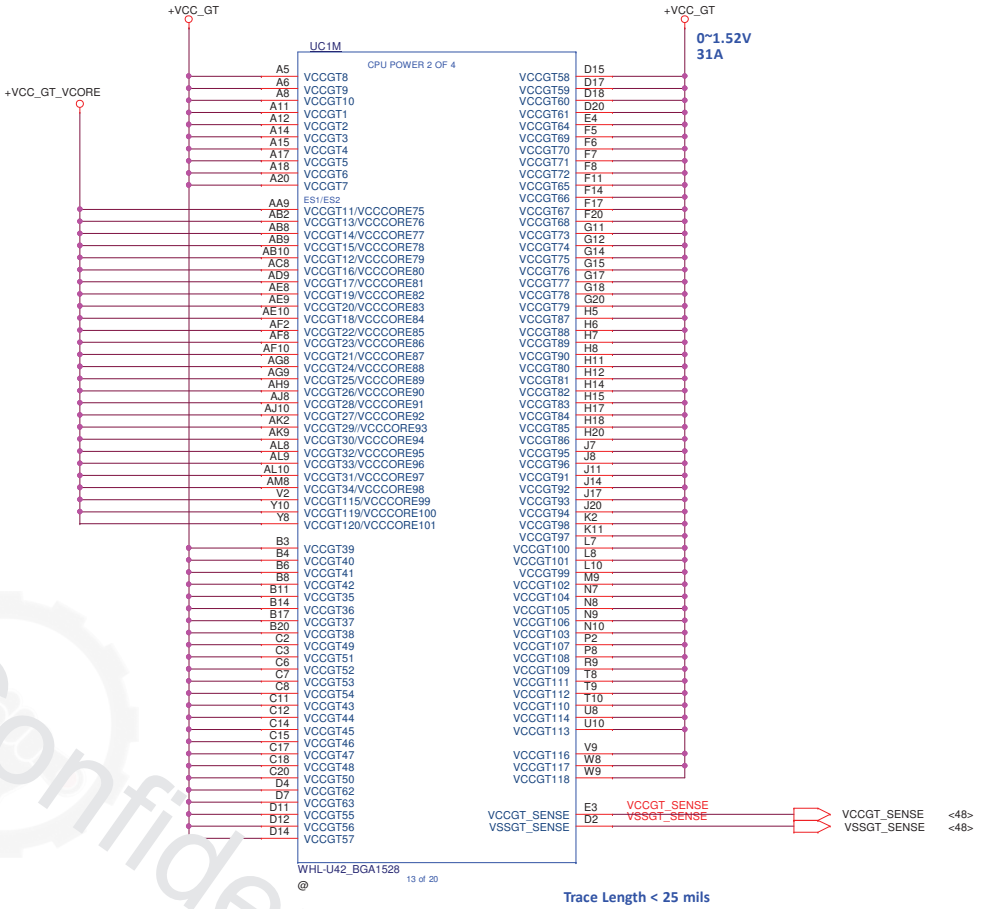
Compal Electronics, Inc.			
Title: WHL-U(8/12)Power			
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, July 12, 2018	Sheet 14 of 57		

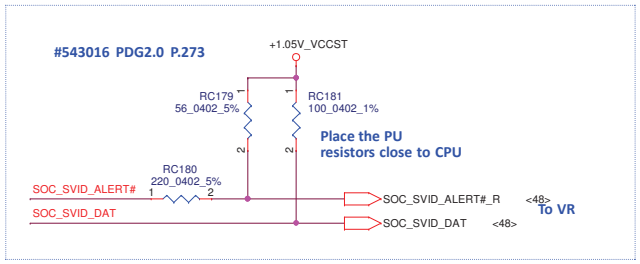


Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	WHL-U(9/12)Power		
Size	Document Number		Rev
Custom	EH5AW M/B LA-G521P		0.1
Date:	Thursday, August 16, 2018	Sheet	15 of 57







Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

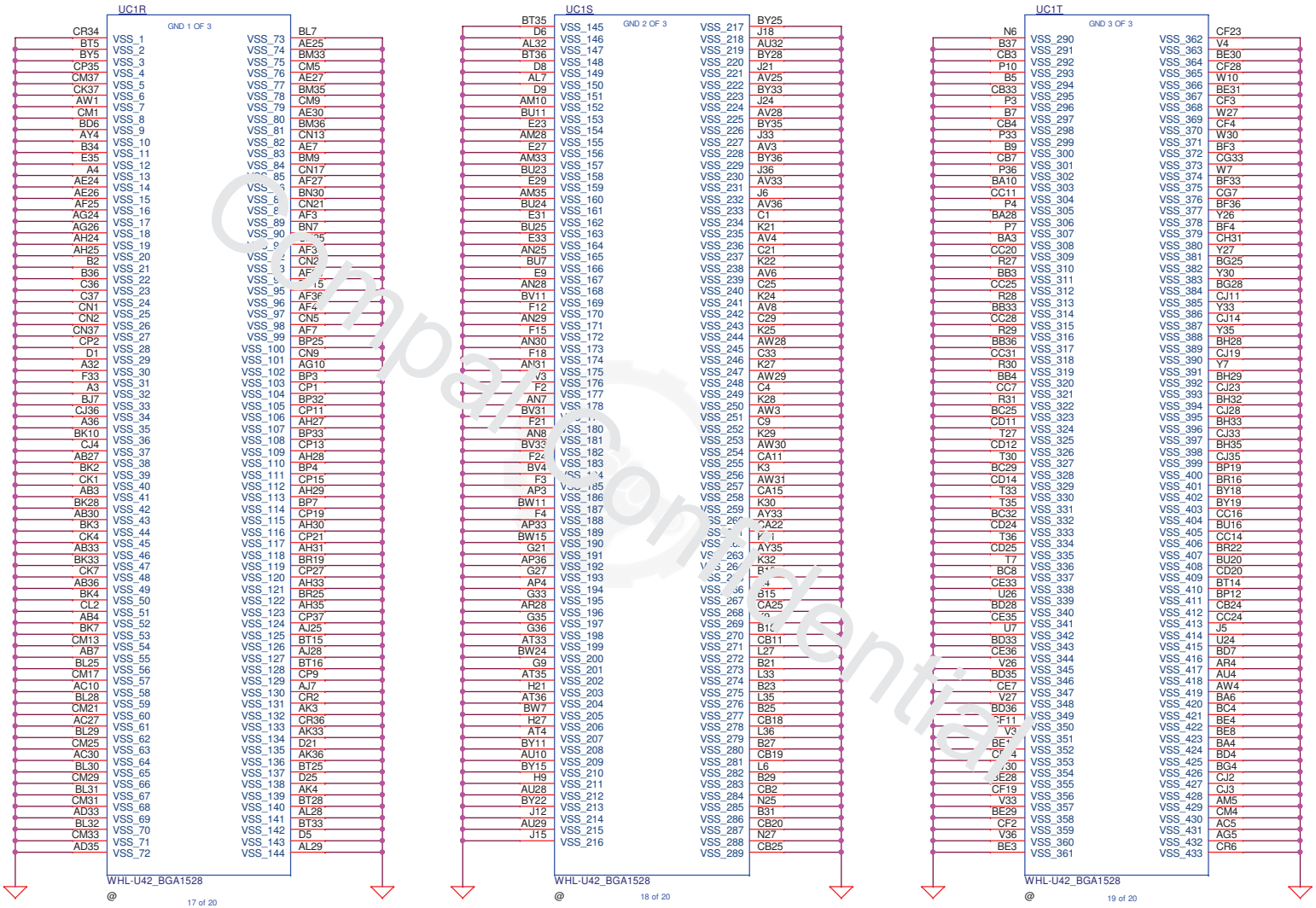
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: WHL-U(10/12)Power,SVID

Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Thursday, July 12, 2018 | Sheet 16 of 57



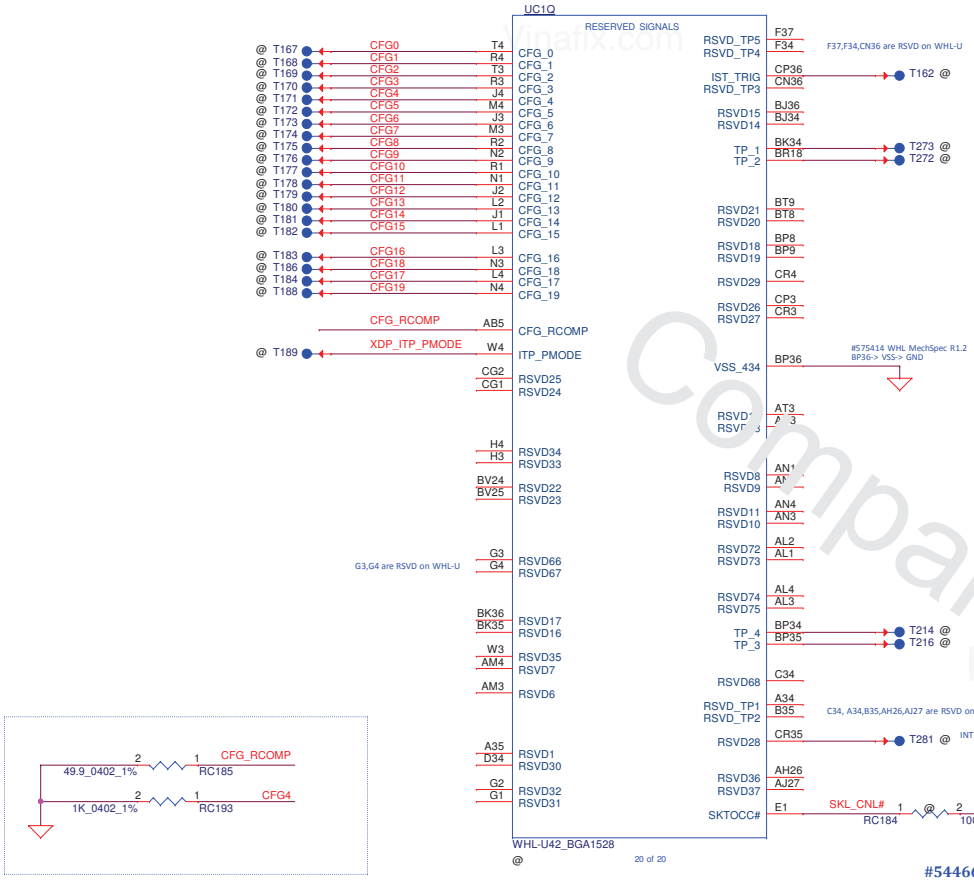
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **WHL-U(11/12)GND**

Size	Document Number	Rev
Custom	EH5AW M/B LA-G521P	0.1

Date: Thursday, July 12, 2018 | Sheet 17 of 57



#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

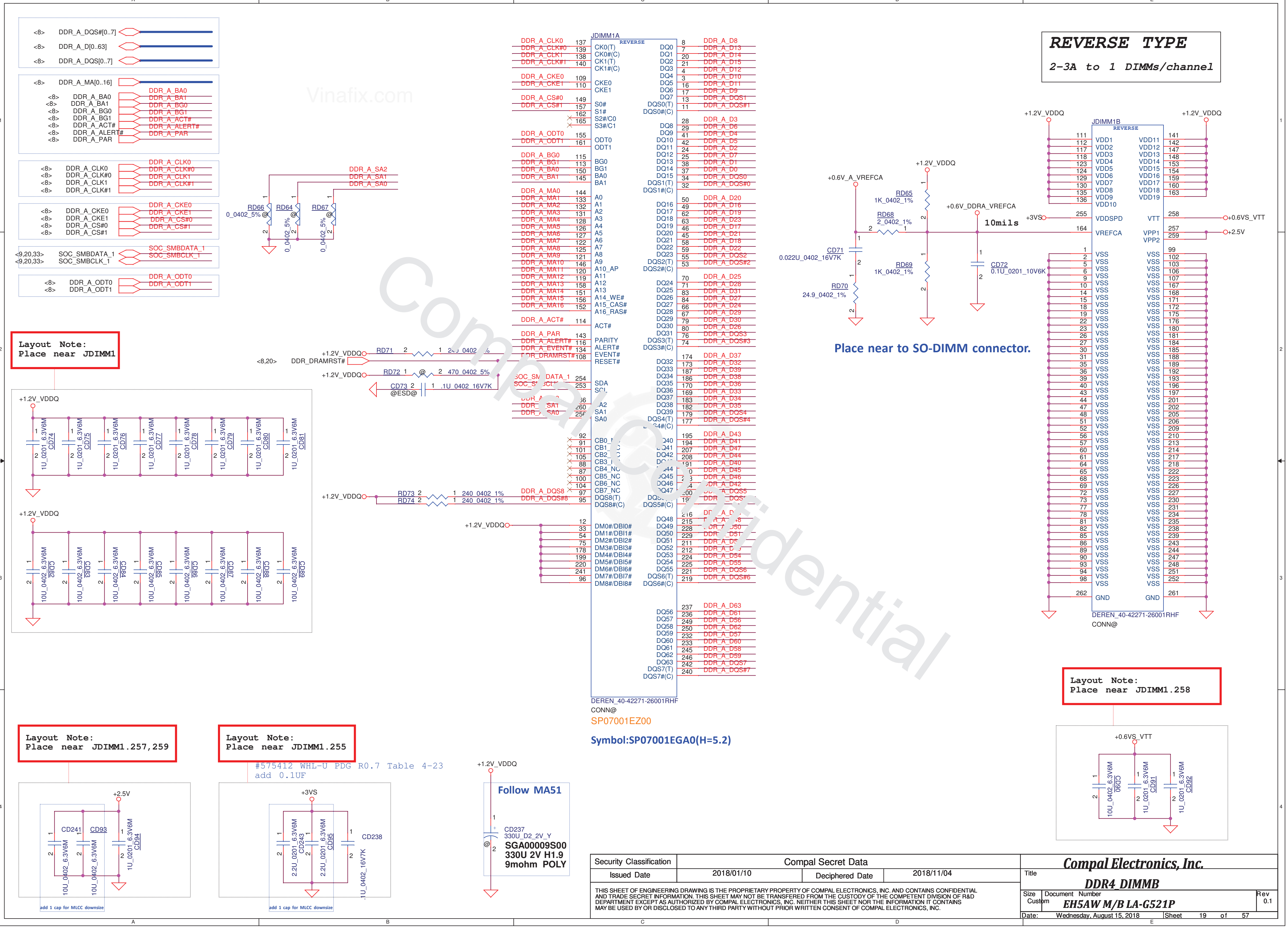
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: WHL-U(12/12)RSVD

Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Thursday, July 12, 2018 | Sheet 18 of 57


REVERSE TYPE
2-3A to 1 DIMMs/channel
DDR_A_DQS#[0..7]
DDR_A_D[0..63]
DDR_A_DQS[0..7]
DDR_A_MA[0..16]
DDR_A_BA0
DDR_A_BA1
DDR_A_BG0
DDR_A_BG1
DDR_A_ACT#
DDR_A_ALERT#
DDR_A_PAR
DDR_A_CLK0
DDR_A_CLK#0
DDR_A_CLK1
DDR_A_CLK#1
DDR_A_CKE0
DDR_A_CKE1
DDR_A_CS#0
DDR_A_CS#1
SOC_SMBDATA_1
SOC_SMBCLK_1
DDR_A_ODT0
DDR_A_ODT1
DDR_A_SA2
DDR_A_SA1
DDR_A_SA0
RD66
RD64
RD67
0_0402_5%
JDIMM1A
JDIMM1B
DDR_DRAMRST#
RD71
RD72
470_0402_5%
CD73
@ESD@
.1U_0402_16V7K
RD73
RD74
240_0402_1%
+1.2V_VDDQ
+0.6V_A_VREFCA
+0.6V_DDRA_VREFCA
RD65
1K_0402_1%
RD68
2_0402_1%
RD69
1K_0402_1%
CD71
0.022U_0402_16V7K
RD70
24.9_0402_1%
CD72
0.1U_0201_10V6K
10mils
+3VS
+0.6VS_VTT
+2.5V
VDDSPD
VREFCA
VTT
VPP1
VPP2
GND
Place near to SO-DIMM connector.
Layout Note:
Place near JDIMM1
Layout Note:
Place near JDIMM1.258
Layout Note:
Place near JDIMM1.257,259
Layout Note:
Place near JDIMM1.255
#575412 WHL-U PDG R0.7 Table 4-23
add 0.1UF
Follow MA51
CD237
330U_D2_2V_Y
SGA00009S00
330U 2V H1.9
9mohm POLY
CD241
CD93
CD94
CD243
CD95
CD238
CD90
CD91
CD92
add 1 cap for MLCC downsize
DEREN_40-42271-26001RHF
CONN@
SP07001EZ00
Symbol:SP07001EGA0(H=5.2)
Security Classification
Compal Secret Data
Issued Date
2018/01/10
Deciphered Date
2018/11/04
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DDR4_DIMMB
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Custom
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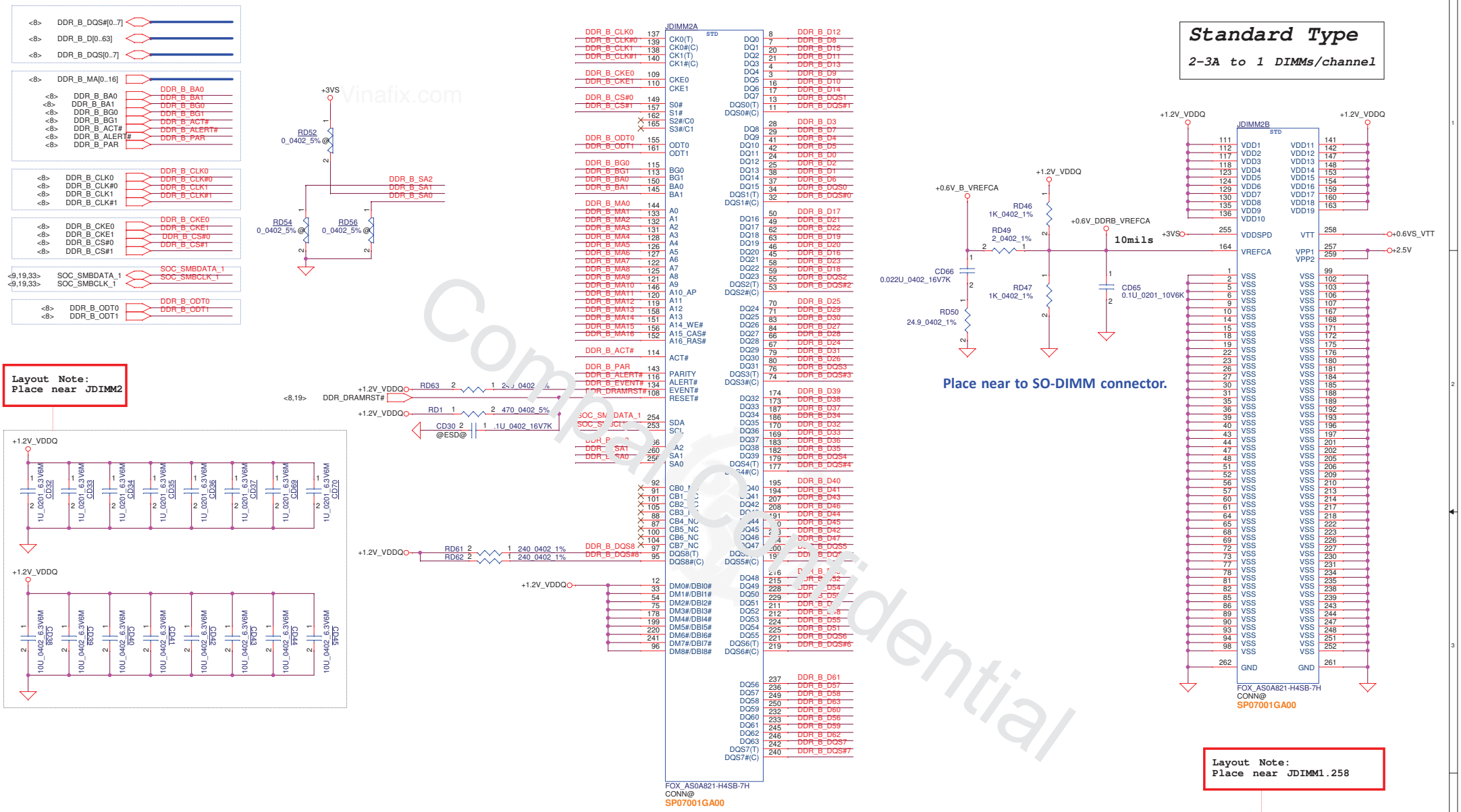
Rev
0.1
Date: Wednesday, August 15, 2018
Sheet 19 of 57
Compal Confidential

Standard Type

2-3A to 1 DIMMs/channel



Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM1.257,259

add 1 cap for MLCC downsize

Layout Note:
Place near JDIMM2.255

#575412 WHL-U PDG R0.7 Table 4-23
add 0.1UF

add 1 cap for MLCC downsize

Layout Note:
Place near JDIMM1.258

Security Classification	Compal Secret Data		
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N16 GPU

GPIO	I/O	USAGE
GPIO0	O	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	I	FRAME_LOCK#
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		

N17 GPU

GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	I/O	NVVDDS_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16		Reserved
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D_VISION
GPIO20		Reserved
GPIO21		Reserved (OC_WARN)
GPIO22		Reserved
GPIO23		Reserved

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Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: X5_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU

GC6 2.0 function

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (multi-GPU usage)

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

Crystals must have a max ESR of 80 ohm

2016/11/10
C2007 change to 22uF
1. NV reference design
2. Top side only 1.2mm high

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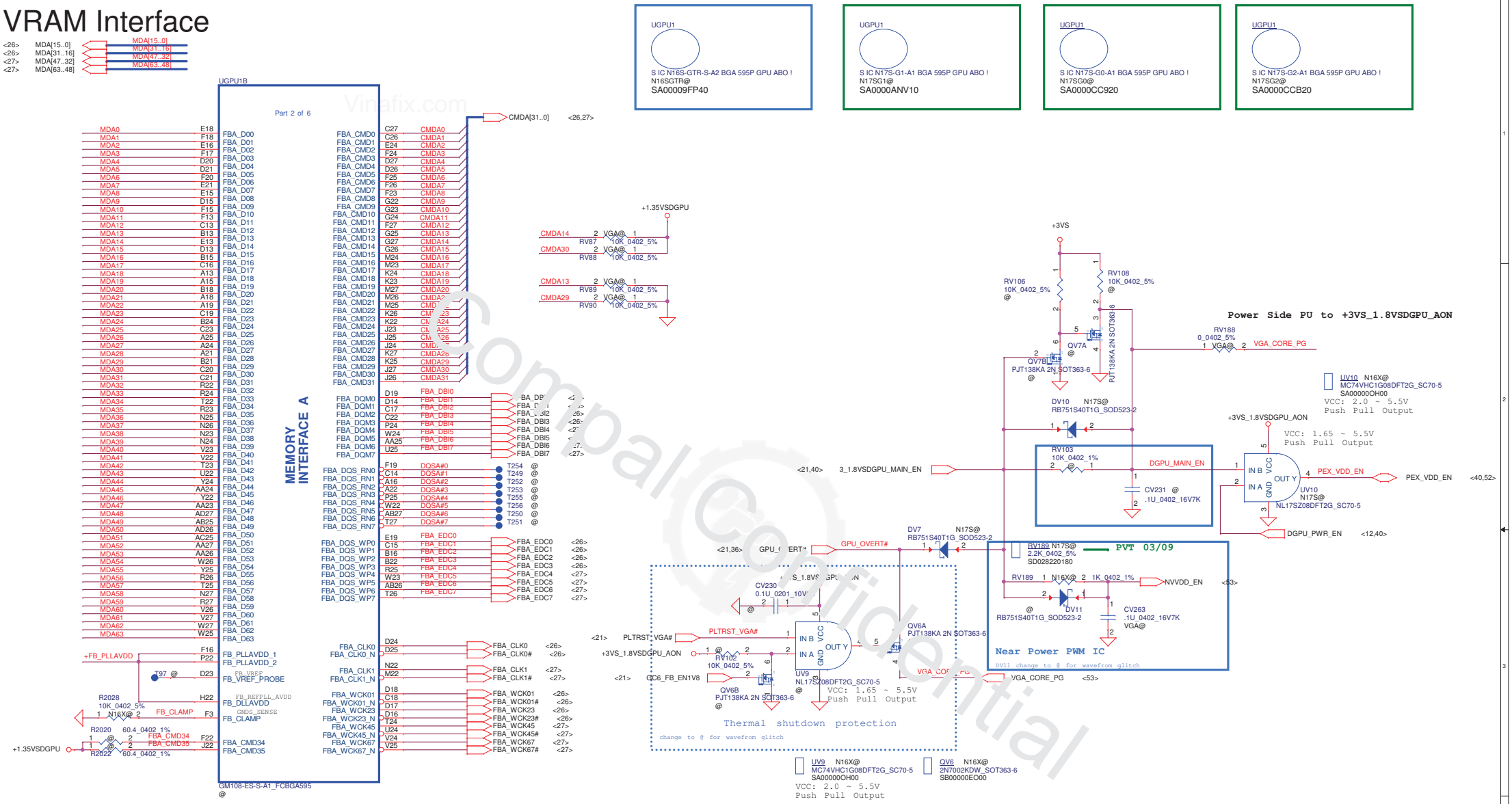
VRAM Interface



DA-08329-001_V01

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X65	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

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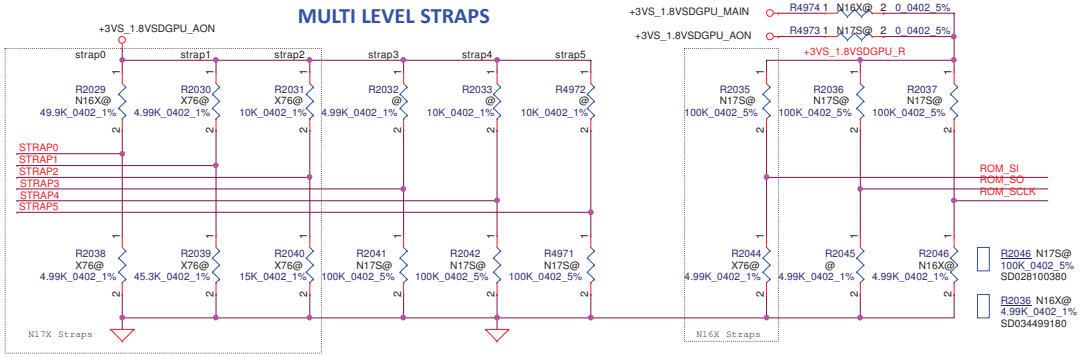
MULTI LEVEL STRAPS



Multi strap table

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N16V-GMR1 N16S-GTR	+1.35V		X76793BOL03	2.5GHz	256Mx32x2 2G	0x8 (SA00009TV50) Micron MT51J256M32HF-70:B	PU 49.9K	NC	NC	NC	NC	NC	PU 4.99K	PU 4.99K	PD 4.99K
			X76793BOL04			0x9 (SA00009U160) Hynix H5GC8H24AJR-R0C							PU 10K		
			X76739BOL04			0x0 (SA000094R30) Samsung K4G80325FB-HC03							PD 4.99K		
			X76739BOL05			0x5(SA00009ZG20) Hynix H5GC8H24MJR-T2C							PD 30.1K		
			X76739BOL06			0x1 (SA000096K30) Micron MT51J256M32HF-60:A							PD 10K		

MX110 Decive ID : N16V-GMR1 0x174E
MX130 Decive ID : N16S-GTR 0x174D

Multi strap table

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S- G1	+1.35V		X76793BOL01	3.0G	256Mx32x2 2G	0x4 (SA00009TV50) Micron MT51J256M32HF-70:B	PD 100K	PD 100K	PD 100K	PD 100K			PU 100K	PU 100K	PU 100K
			X76793BOL02			0x5 (SA00009U160) Hynix H5GC8H24AJR-R0C	PU 100K	PU 100K	PU 100K						PD 100K
			X76739BOL07			0x0 (SA000092D00) Samsung K4G80325FB-HC28	PD 100K	PD 100K	PD 100K						
			X76739BOL08			0x2 (SA00009U110) Hynix H5GC8H24MJR-R0C	PD 100K	PU 100K	PD 100K						
			X76739BOL09			0x1 (SA00009TV10) Micron MT51J256M32HF-70:A	PU 100K	PD 100K	PD 100K						

MX150 Decive ID : N17S-G1-A1 0x1D10

NV16x Straps set t…
(ROM_SI => follow RVL)

Physical Strapping pin	Bit3		Bit2		Bit1		Bit0		Result
ROM_SO	DEVID_SEL	*0 1	PCIE_CFG	*0 1	SMB_ALT_DP	0: 0x9… 1: 0x…	VGA_DEVICE	0: 3D device (Optimus)* 1: VGA device	PH 4.99K
ROM_SCLK	SOR3_EXPOSED (FPGPIO)	0 1	SOR2_EXPOSED (FPD)	0 1	SOR1_EXPOSED (FPD)	0 1	SOR0_EXPOSED (FPD)	0 1	PL 4.99K
ROM_SI	RAMCFG[3]	0 1	RAMCFG[2]	0 1	RAMCFG[1]	0 1	RAMCFG[0]	0 1	PL 4.99K
STRAP4									NA
STRAP3									NA
STRAP2	Reserve PH on 3V3_AON /PL foot print for further …								NA
STRAP1									NA
STRAP0	Pull up 49.9 KΩ to 3V3_AON and reserve Pull down resister foot print.								PH49.9K

NV 16x DG-07158-V05

Table 3-4. GPU Core Sensing Line Routing Constrains

Constraint Parameter	Requirement
Single-ended impedance	25 Ω ± 10%
Differential Trace Impedance	50 Ω ± 15%
Reference Plane	GND Reference
Routing Type	Stripline or Microstrip
Dielectric spacing	Stripline: ≥ 3.0x dielectric Microstrip: ≥ 4.0x dielectric
Intrapair skew	≤ 5 ps
Via stub	
Trace length	GPU to R_S/R_C ≤ 250 mm (9842.5 mil) R_S/R_C to VR ≤ 50 mm (1968.5 mil)

Note:
1. Stripline is recommended to minimize EMI. Do not route over any voids.

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

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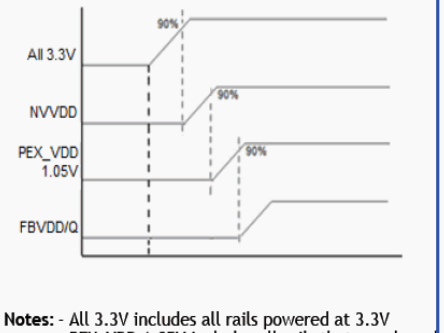
Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 µF X7R	0402	N/A	1	Under GPU
	4.7 µF X6S	0603	N/A	1	Near GPU
	22 µF X6S	0805	N/A	1	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU

VGA Power Sequence (N16X)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

NV 17S DG-07785-001_V07

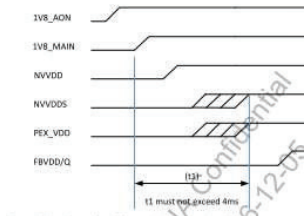


Figure 7.5 Example of Power-Up Sequencing Order

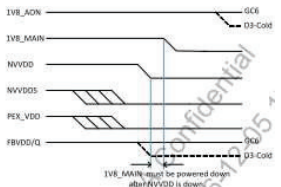


Figure 7.6 Example of Power-Down Sequencing Order

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Date: Thursday, July 12, 2018 | Sheet 23 of 57

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Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

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Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	2	0	Under GPU
	1 μF	X7R	0603	2	8	Under GPU
	4.7 μF	X6S	0603	2	0	Under GPU
	10 μF	X6S	0603	0	2	Under GPU
	10 μF	X6S	0603	1	1	Near GPU
	22 μF	X6S	0603W	1	3	Near GPU

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Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

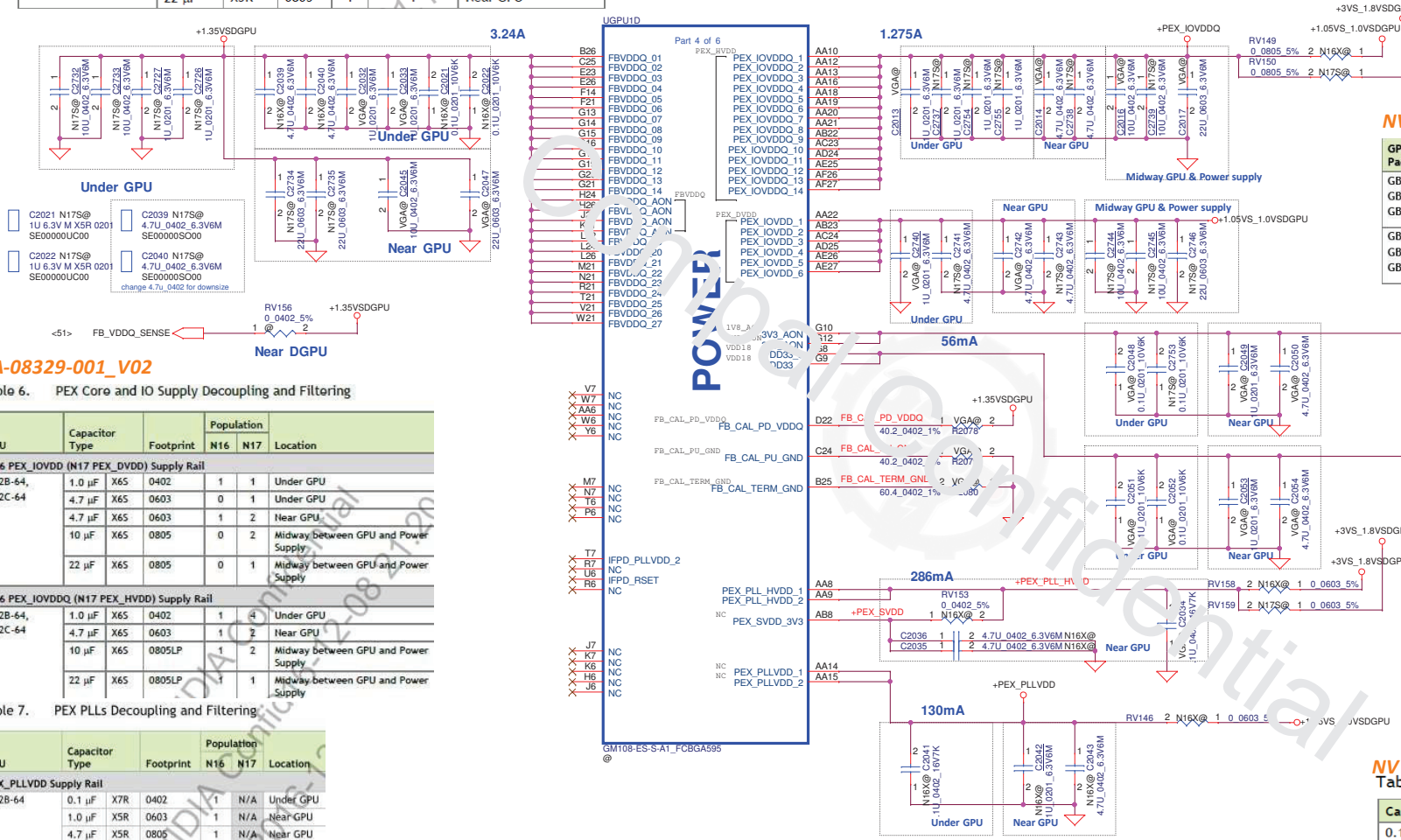

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Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5 / BGA-170	1.35 V or 1.50 V	40.2 Ω	40.2 Ω	60.4 Ω

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GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

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Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 μF	X6S	0402	1	1	Under GPU
	4.7 μF	X6S	0603	0	1	Under GPU
	4.7 μF	X6S	0603	1	2	Near GPU
	10 μF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 μF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 μF	X6S	0402	1	1	Under GPU
	4.7 μF	X6S	0603	1	2	Near GPU
	10 μF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 μF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64	0.1 μF	X7R	0402	1	N/A	Under GPU
	1.0 μF	X5R	0603	1	N/A	Near GPU
	4.7 μF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 μF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	1	1	Near GPU

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Table 9. VDD AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1 μF	X7R	0402	2	2	Under GPU
	1.0 μF	X6S	0603	1	1	Near GPU
	4.7 μF	X6S	0603	1	1	Near GPU
N16 3V3_AON (N17 1V8_AON) Supply Rail						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	1	1	Under GPU
	1.0 μF	X6S	0603	1	1	Near GPU
	4.7 μF	X6S	0603	1	1	Near GPU

NV 16x DG-07158-V05

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

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Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

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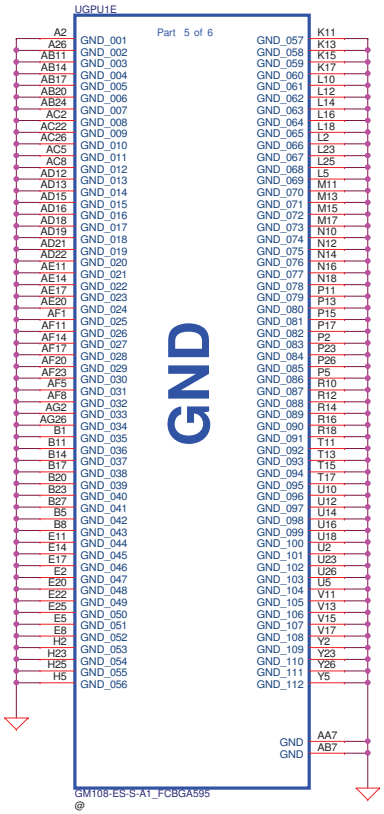

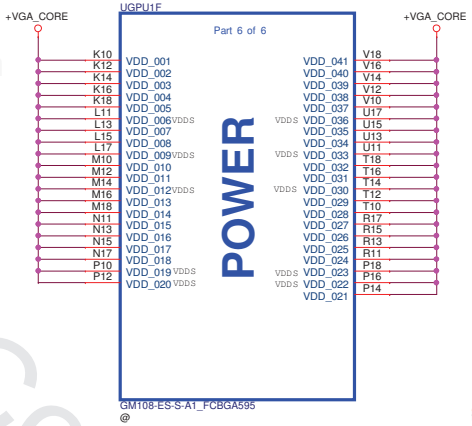

NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

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Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	3.3 µF	POS	7343	N/A	1	Near GPU

DA-07750-000-V02

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core –	GPU FBIO 1.5V [4]	GPU FBIO 1.35V [4]	FB Total [1,5] 1.5V [4]	FB Total [1,5] 1.35V [4]	1.05V Total [2] 1.05V [4]	3.3V Total 3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0		2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	–	2.0	–	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	–	2.0	–	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core –	GPU FBIO 1.5V [4]	GPU FBIO 1.35V [4]	FB Total [1,5] 1.5V [4]	FB Total [1,5] 1.35V [4]	1.05V Total [2] 1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	–	2.9	–	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	–	3.1	–	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

DA-07751-000-V02

Table 5. EDP-Continuous [3]

Product	VRAM Type	GPU Core –	GPU FBIO 1.5V [4]	GPU FBIO 1.35V [4]	FB Total [1,5] 1.5V [4]	FB Total [1,5] 1.35V [4]	1.05V Total [2] 1.05V [4]	3.3V Total 3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16V-GMR1	GDDR5 @ 2.0 GHz	18.5	–	2.0	–	4.2	0.8	0.06
	GDDR5 @ 2.5 GHz	18.5	–	2.0	–	4.7	0.8	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06

Table 6. EDP-Peak [3]

Products	VRAM Type	GPU Core –	GPU FBIO 1.5V [4]	GPU FBIO 1.35V [4]	FB Total [1,5] 1.5V [4]	FB Total [1,5] 1.35V [4]	1.05V Total [2] 1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16V-GMR1	GDDR5 @ 2.0 GHz	30.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	–	3.1	–	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

SP-08318-001_V03

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	60.1	3.2	6.6	0.2

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Title: N16X POWER & GND 5/9			
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VRAM GDDR5 chips

<22,27> MDA[63..0] — MDA[63..0]
<22,27> CMDA[31..0] — CMDA[31..0]

X76 for N16X 2G VRAM

- ZZZ X7604@ — Samsung_256Mx32x2 X76739BOL04
- ZZZ1 X76793BOL03@ — Micron_MT51J256M32HF-70:B X76793BOL03
- ZZZ X7605@ — Hynix_256Mx32x2 X76739BOL05
- ZZZ2 X76793BOL04@ — Hynix_ H5GC8H24AJR-R0C X76793BOL04
- ZZZ X7606@ — Micron_256Mx32x2 X76739BOL06

New

X76 for N17S 2G VRAM

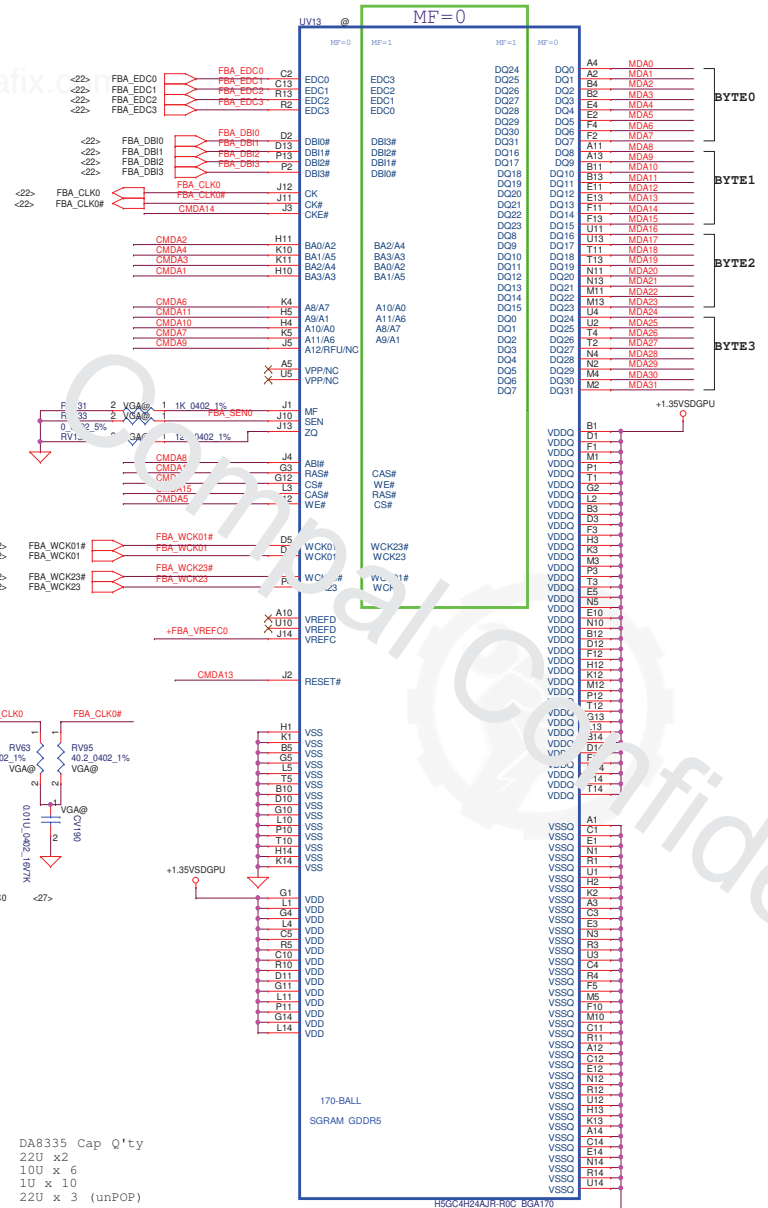
- ZZZ X7607@ — Samsung_256Mx32x2 X76739BOL07
- ZZZ4 X76793BOL01@ — Micron_MT51J256M32HF-70:B X76793BOL01
- ZZZ X7608@ — Hynix_256Mx32x2 X76739BOL08
- ZZZ3 X76793BOL02@ — Hynix_ H5GC8H24AJR-R0C X76793BOL02
- ZZZ X7609@ — Micron_256Mx32x2 X76739BOL09

New

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 0 BOT SIDE



+1.35VSDGPU

RV136 549_0402_1% VGA@
RV135 931_0402_1% VGA@
RV56 1.33K_0402_1% VGA@
CV195 820PF_0402_50V7K VGA@
QV3 BSS138W-7-F_SOT323-3 VGA@
FBA_VREFC_L
+FBA_VREFC0
<21> VRAM_VREF_CTL

FBA_CLK0 FBA_CLK0#
RV63 40.2_0402_1% VGA@
RV95 40.2_0402_1% VGA@
CV190 0.01U_0402_16V7K VGA@

DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6

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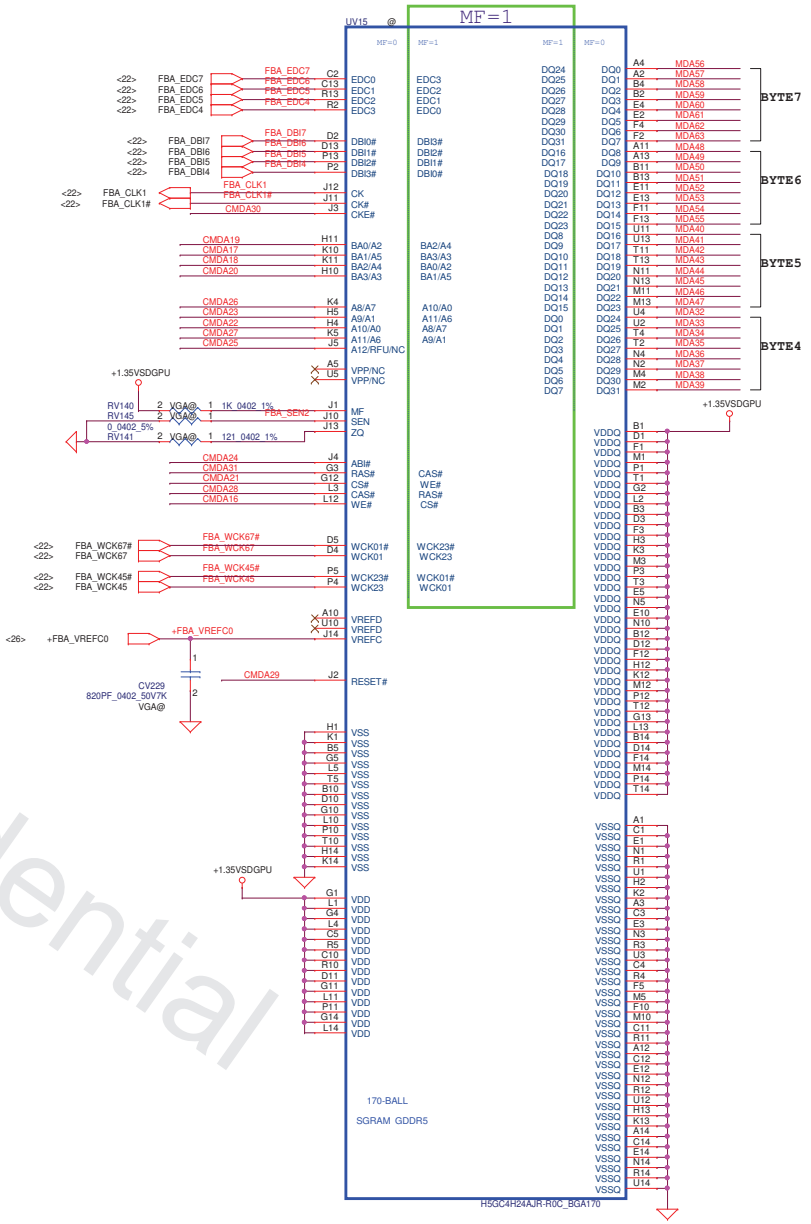
VRAM GDDR5 chips

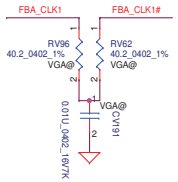
<22,26> MDA[63..0] → MDA[63..0]
<22,26> CMDA[31..0] → CMDA[31..0]

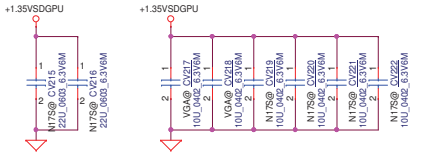
GDDR5 Mode H Mapping

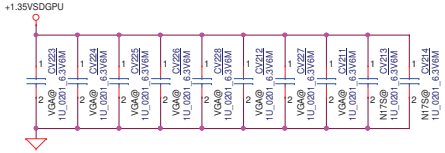
	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 1 BOT SIDE



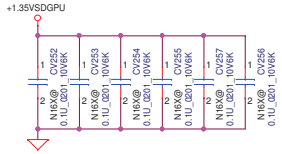






DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6



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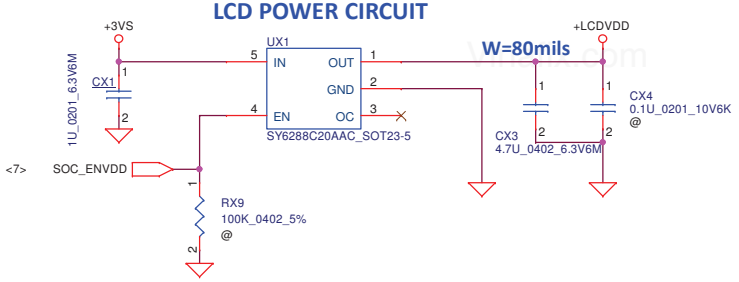
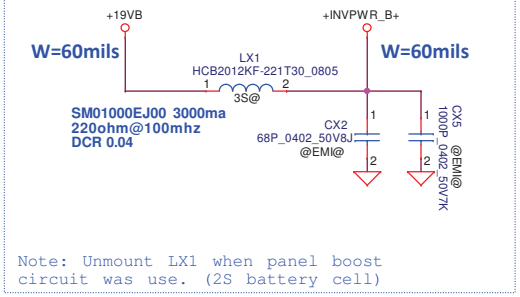
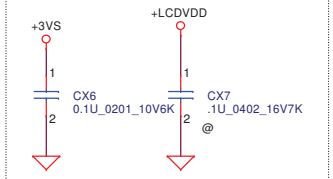
LCD POWER CIRCUIT

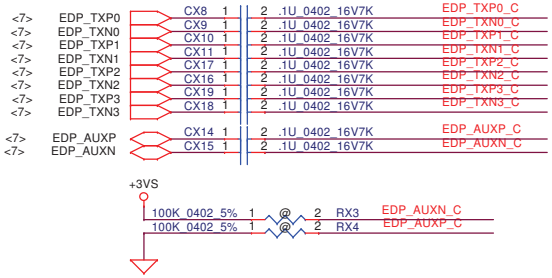


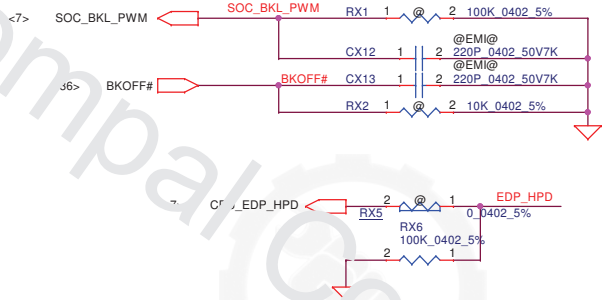


Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

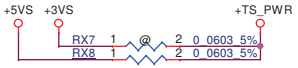
Place closed to JEDP1



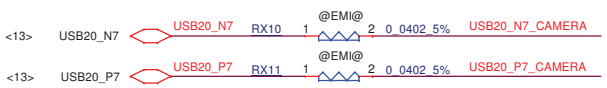




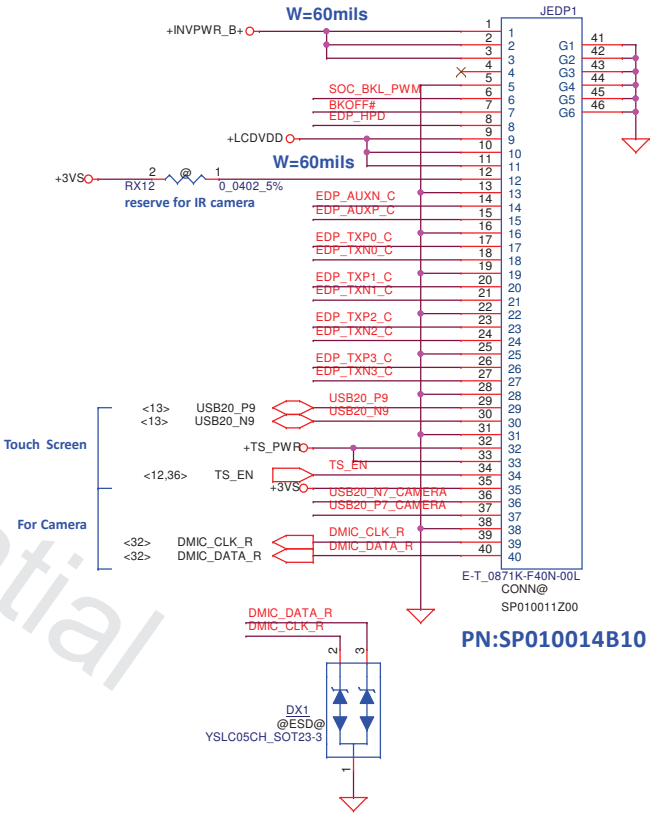
Touch Screen



Camera



LED PANEL Conn.



PN:SP010014B10

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Title: eDP Connector

Size	Document Number	Rev
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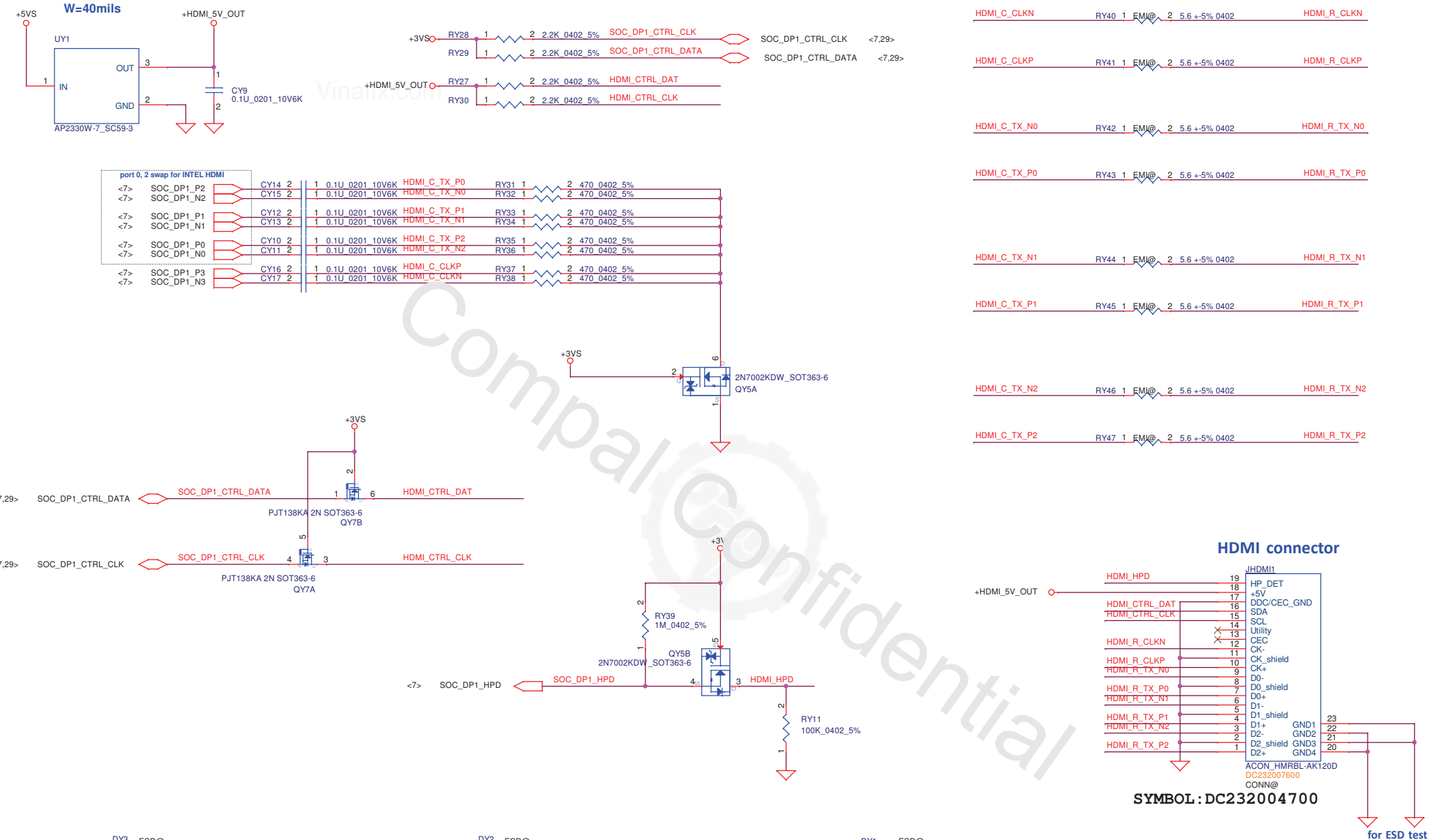

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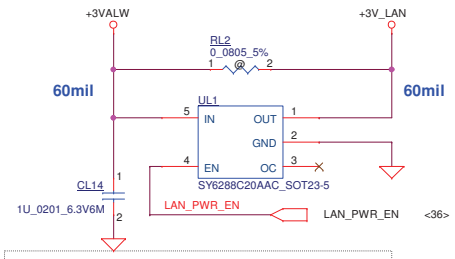
Title: HDMI CONN.			
Size: Custom	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Wednesday, July 18, 2018	Sheet 29 of 57		

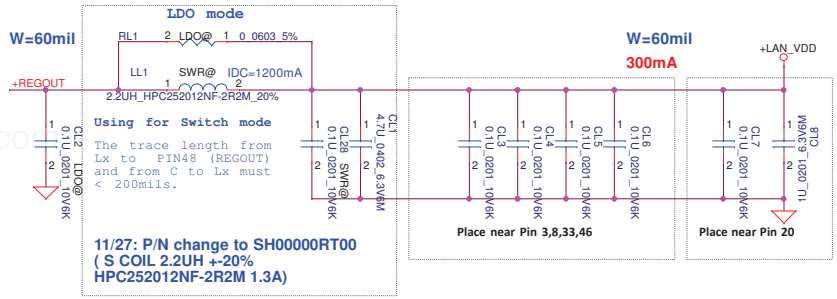
LAN-RTL8411B

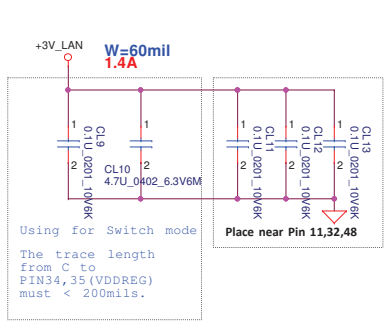


From EC

High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms

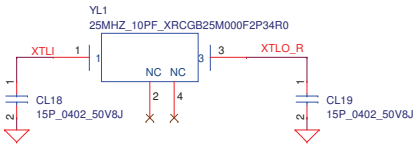


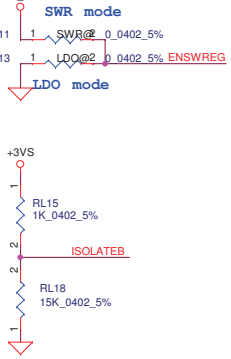


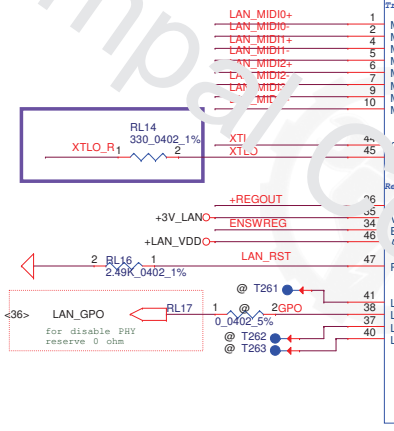
11/27: P/N change to SH00000RT00
(S COIL 2.2UH +-20%
HPC252012NF-2R2M 1.3A)

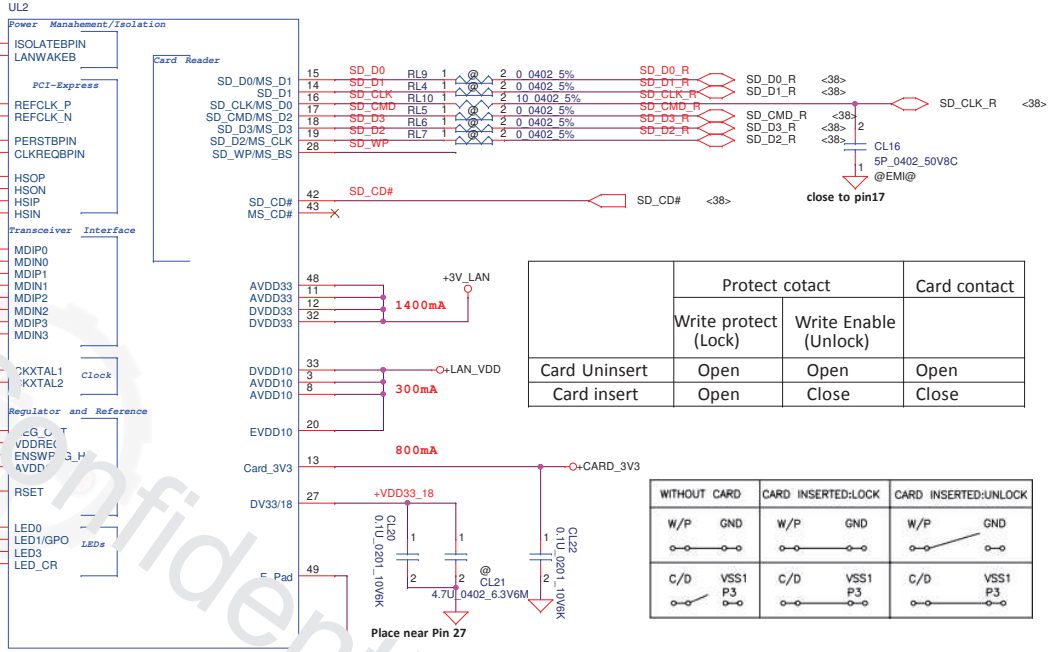
reserve EC_PME# pull high 100K to +3VALW_EC

PU at PCH side

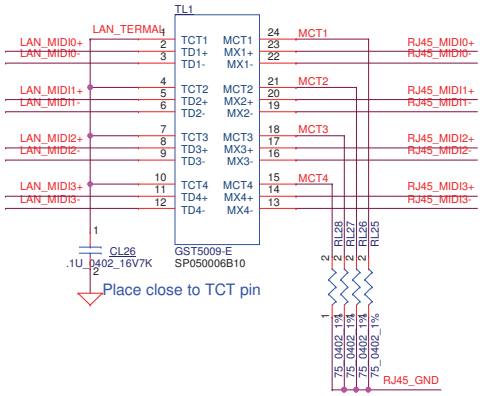


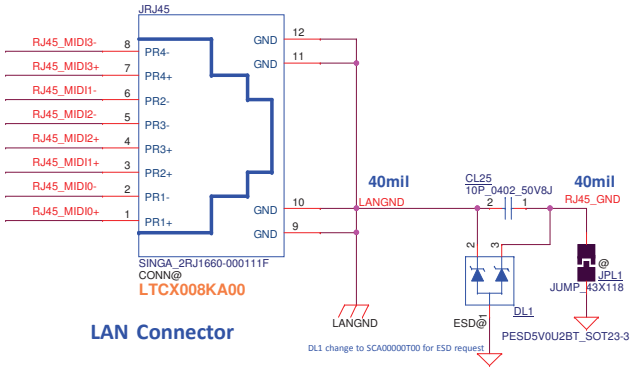




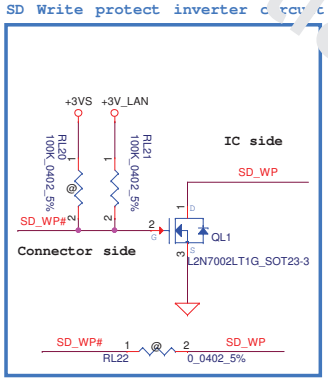


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

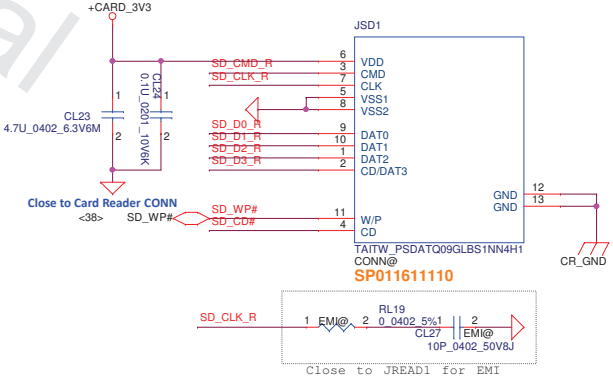




LAN Connector



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: LAN RTL8411B-CG/Card Reader

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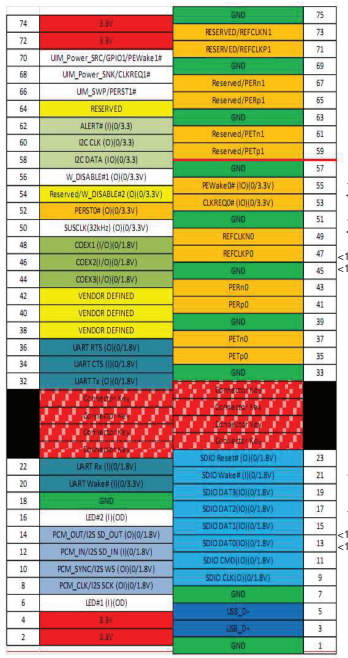
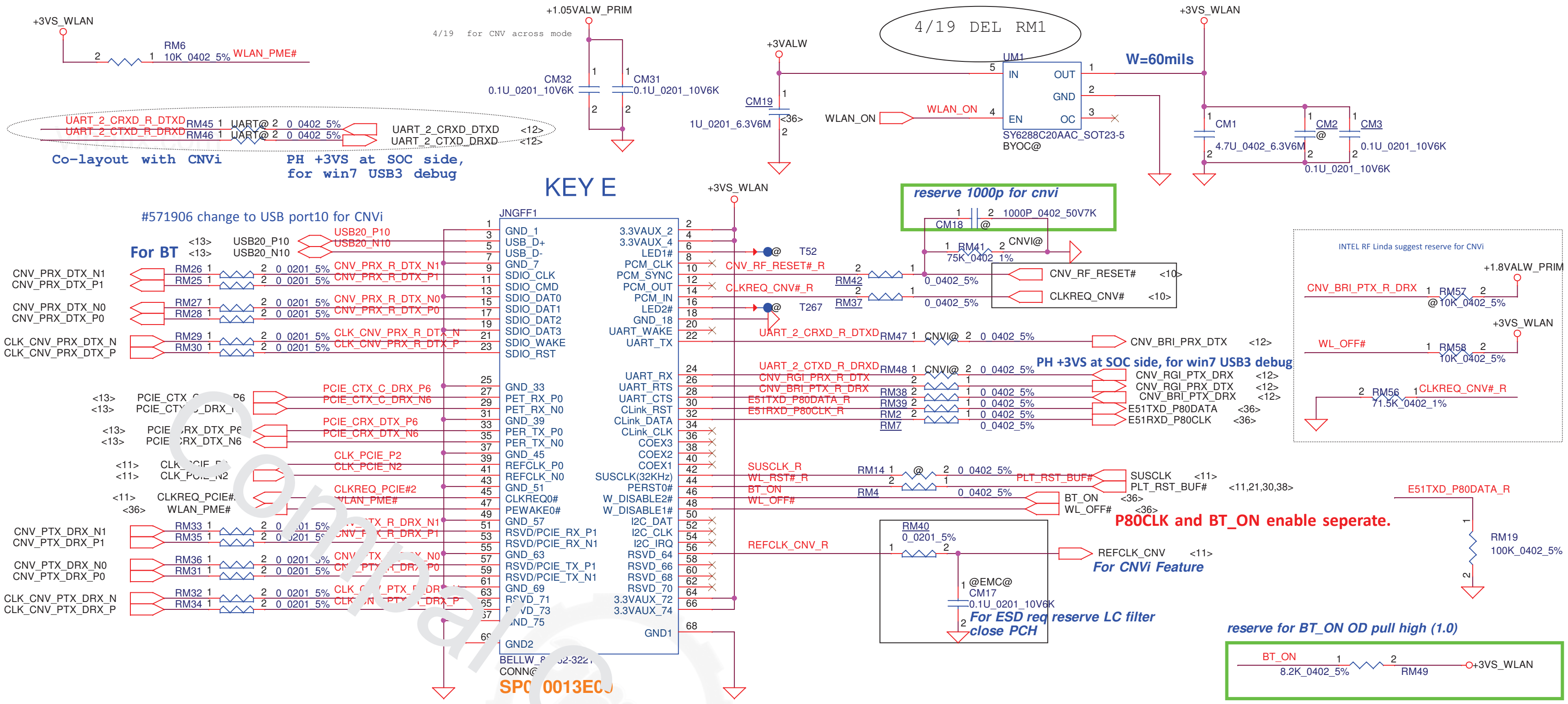
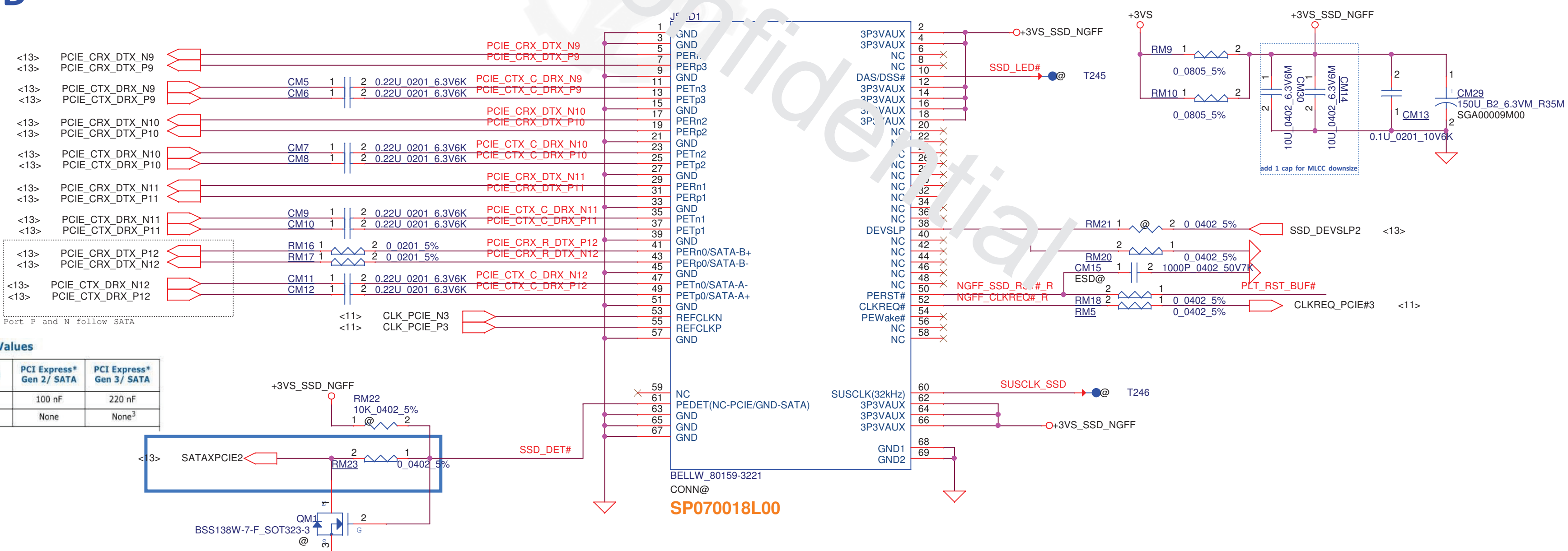
Wireless LAN

NGFF WL+BT (KEY E)





mSATA/SSD



PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

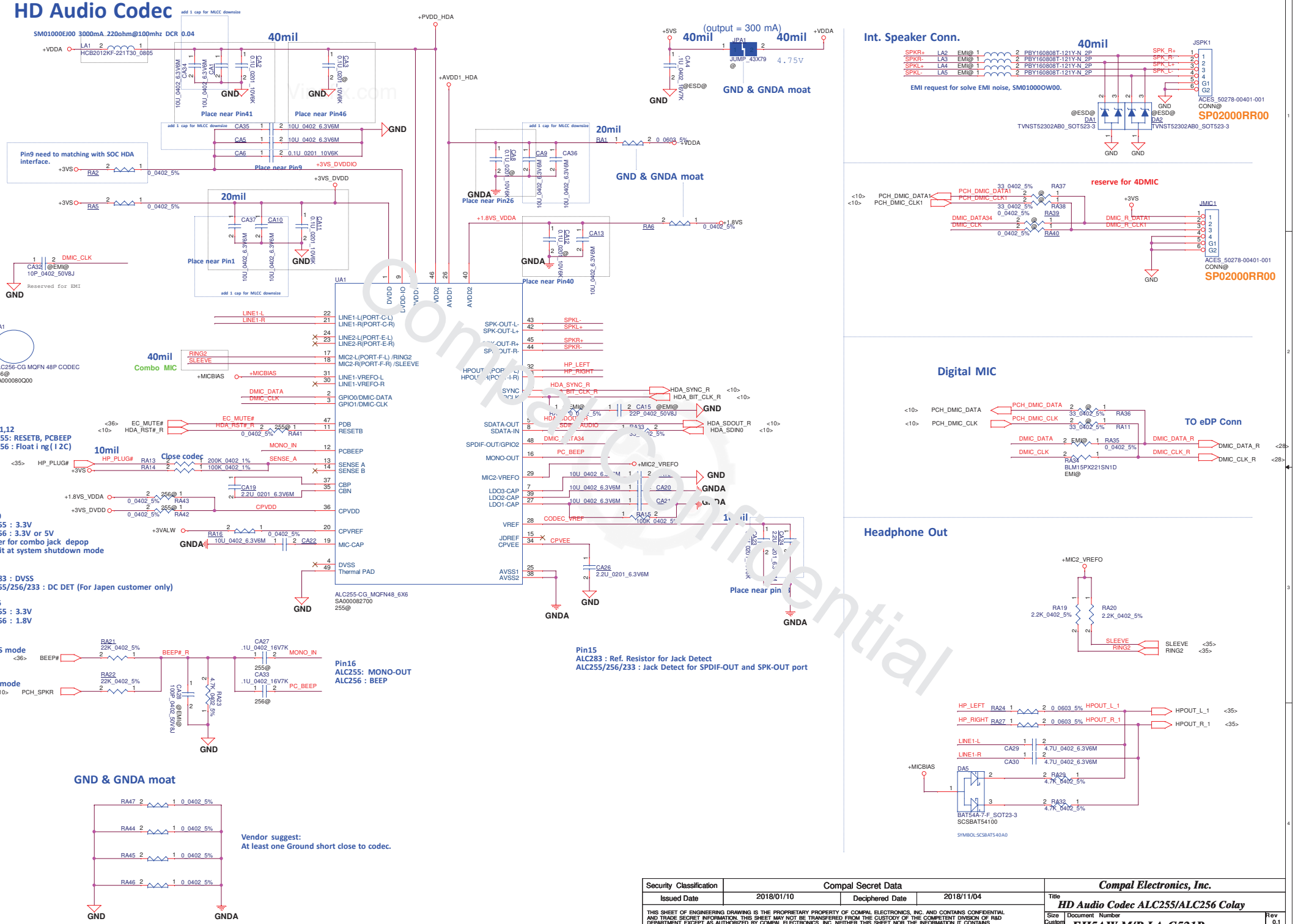
SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date	2018/11/04	Title: M.2 Key E (WLAN)/Key M(SSD)

Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev 0.1

Date: Monday, July 23, 2018 |

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: *HD Audio Codec ALC255/ALC256 Colay*

Size	Document Number	Rev
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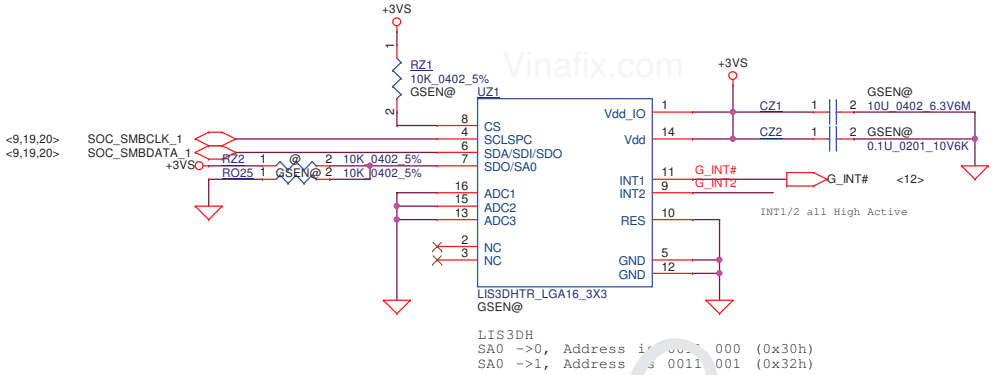
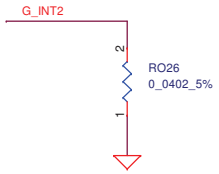
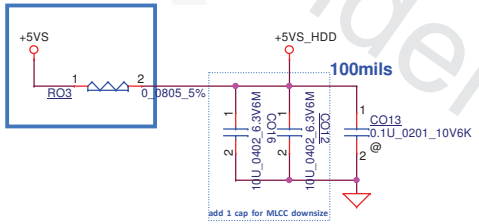
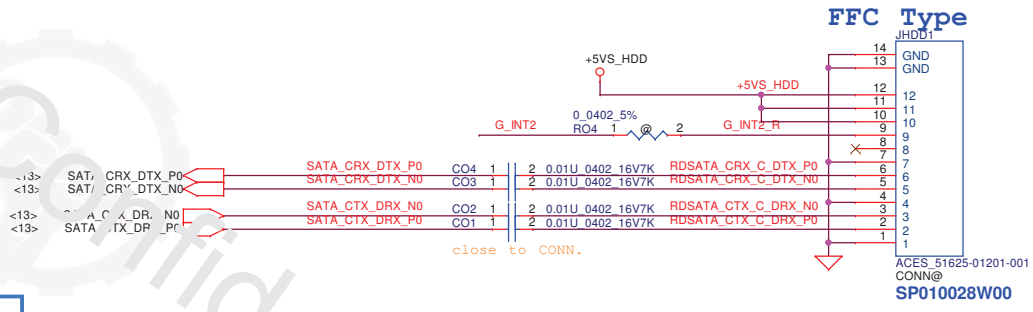
G-Sensor reserved for BA serial









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Compal Electronics, Inc.

Title: HDD/ HDD Re-Driver

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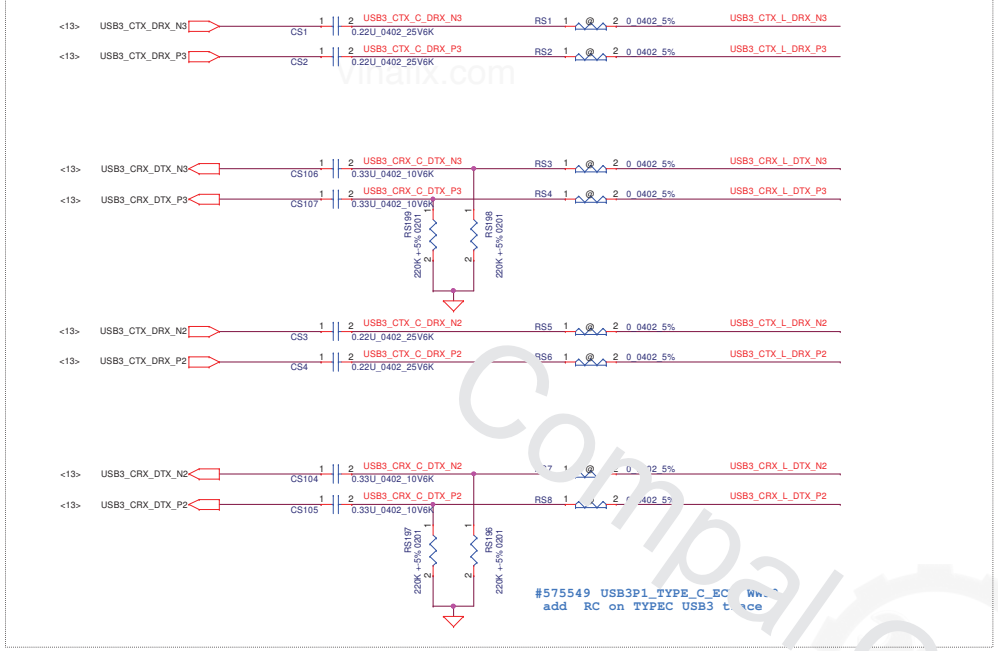
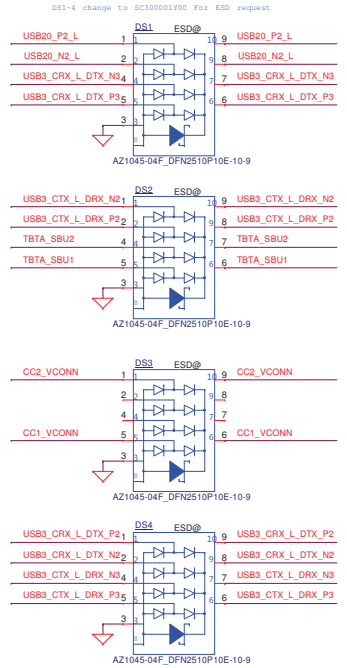
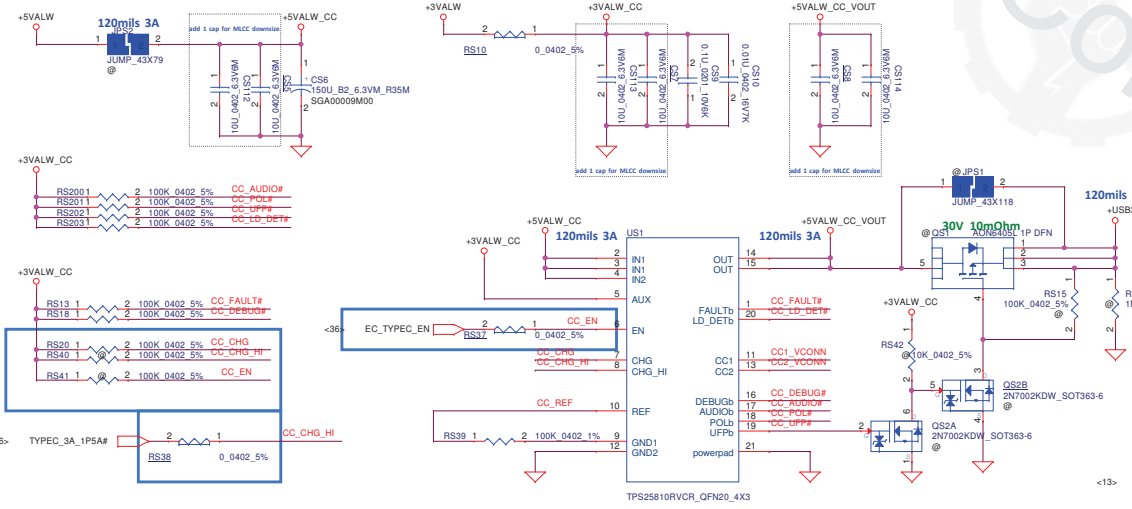
TypeC USB3.0 Gen1







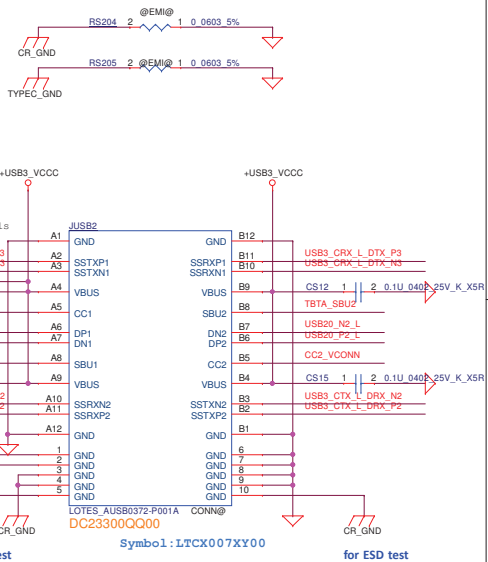


Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On[1]	Off

Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

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Compal Electronics, Inc.

Title: CC+USB TYPE C

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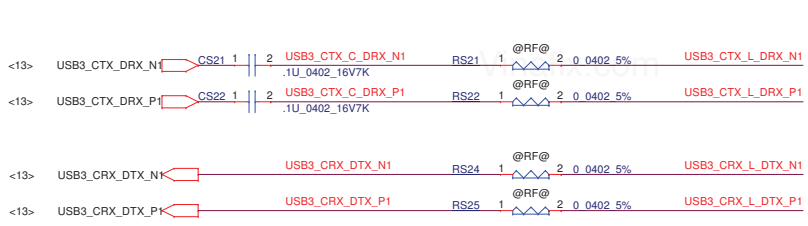
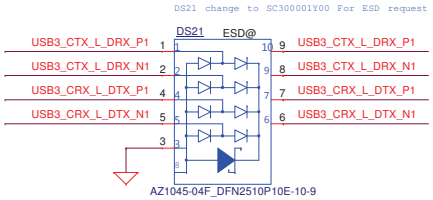
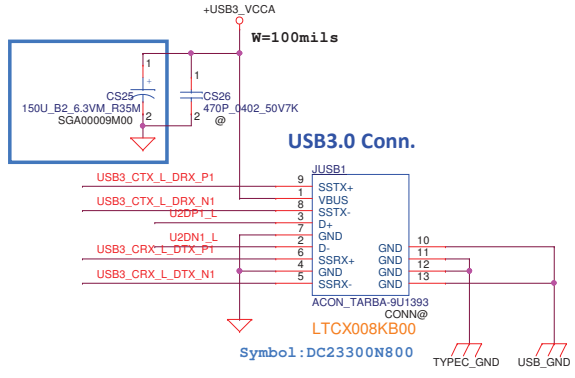
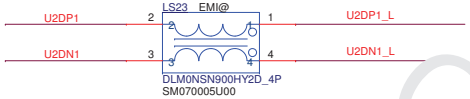
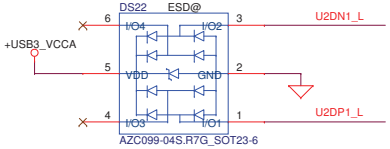
USB3.0 (Port 1)

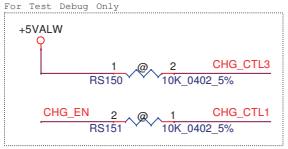


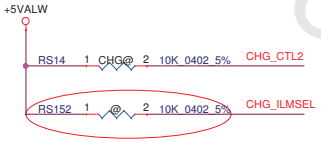




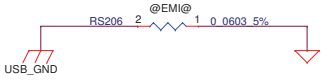


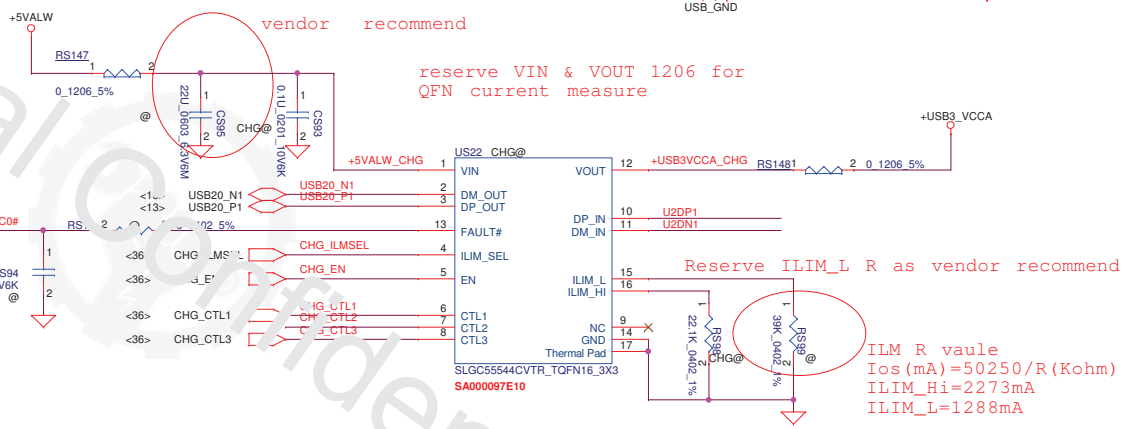






Rerserve PU, vendor suggest to EC control if future need support SDP2

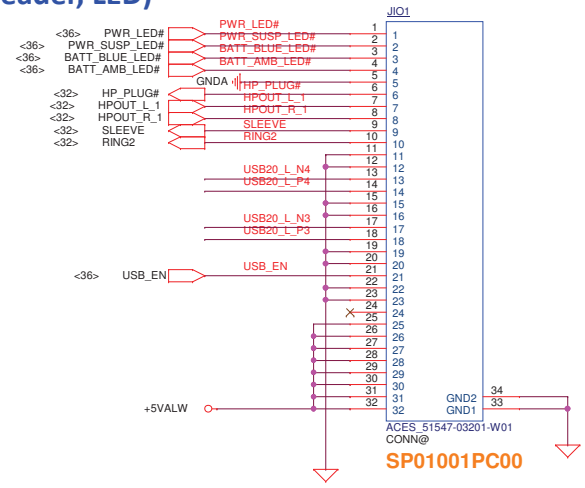


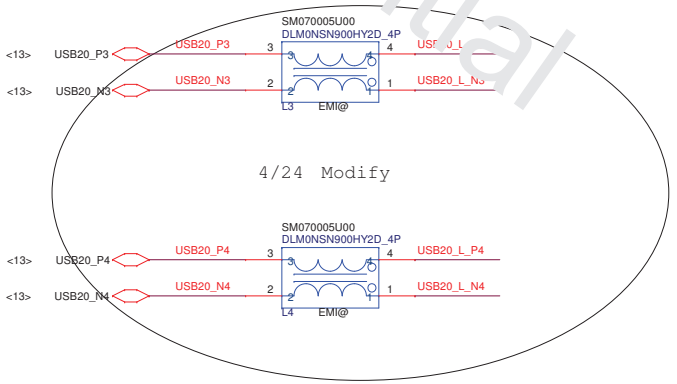


USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

IO/B (USBx2, Card reader, LED)





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Title: USB3 Conn/IOB

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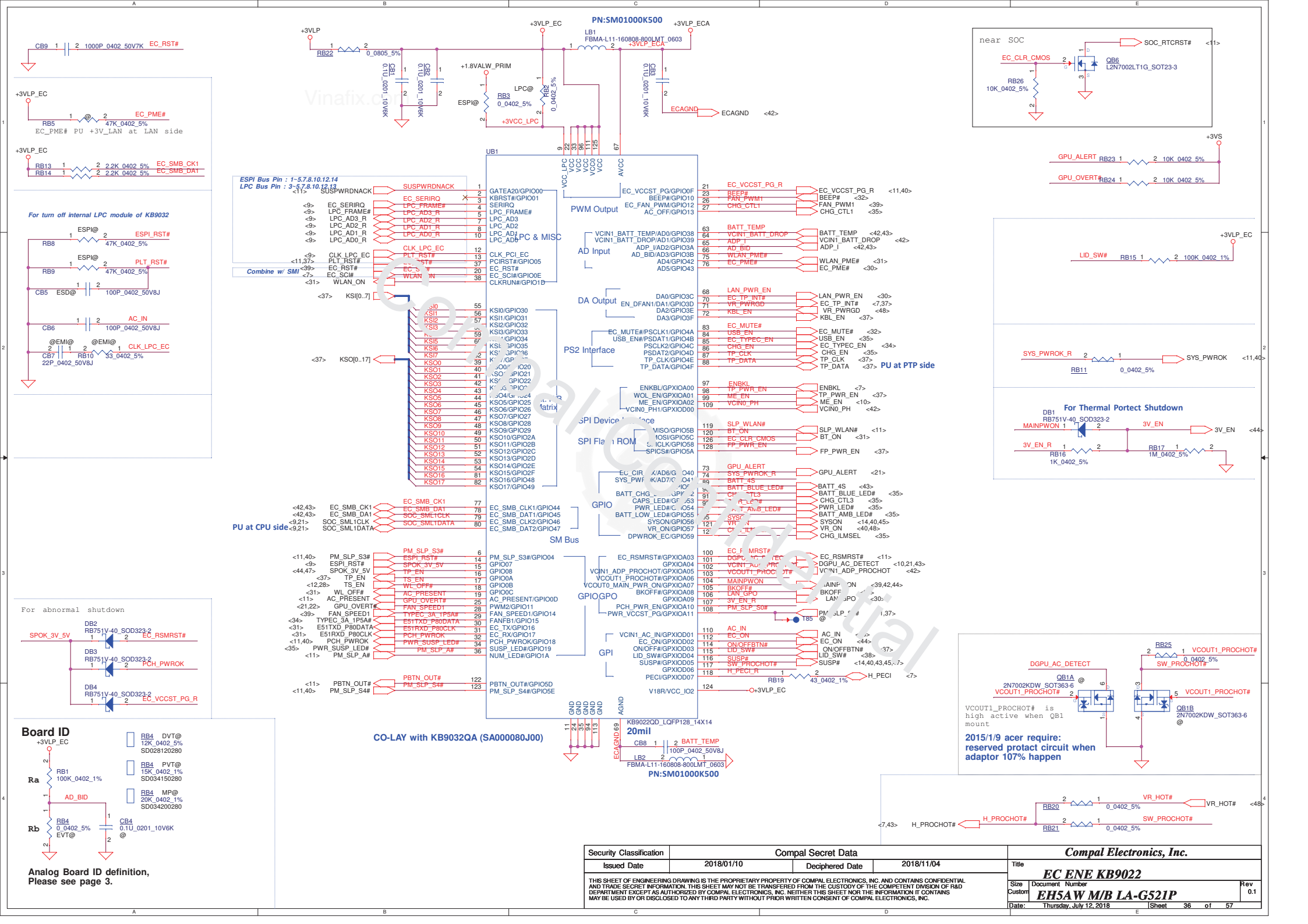

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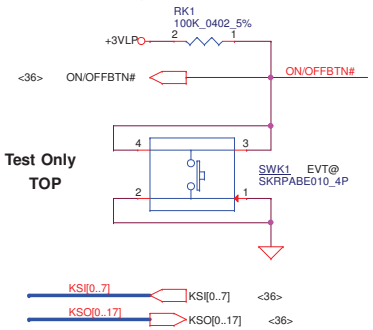
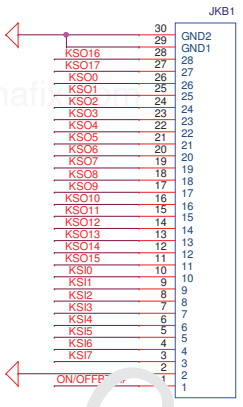
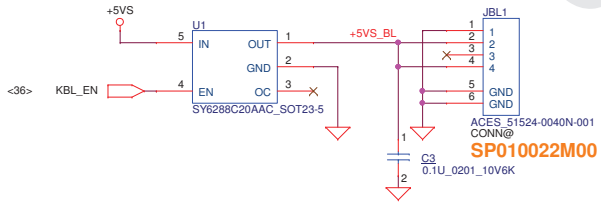
KB Conn.

ON/OFF BTN

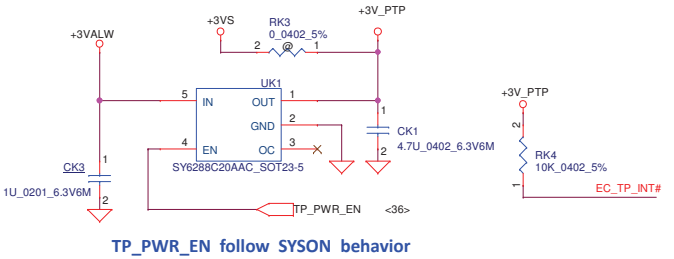




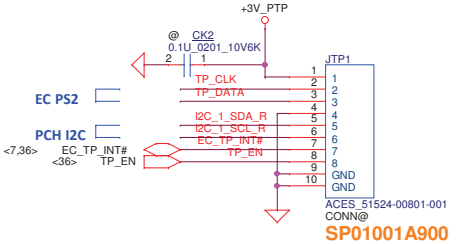
KB BackLight

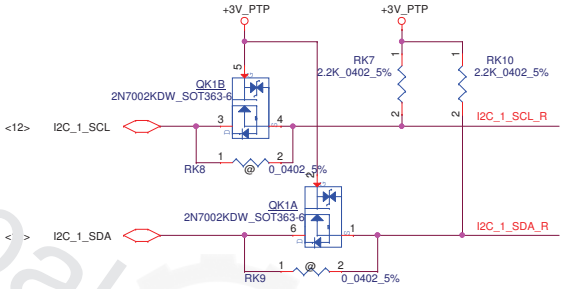


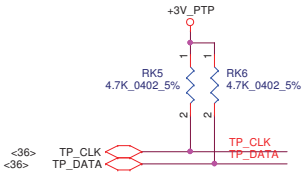
TP/B Conn.



TP_PWR_EN follow SYSON behavior







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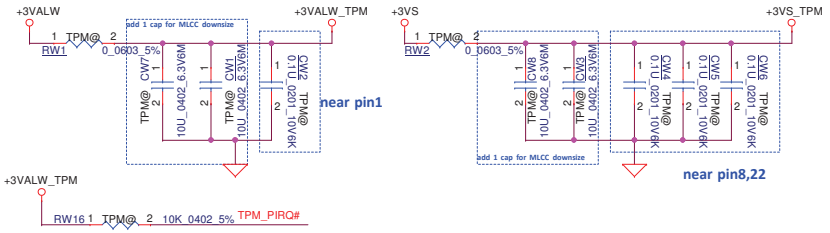
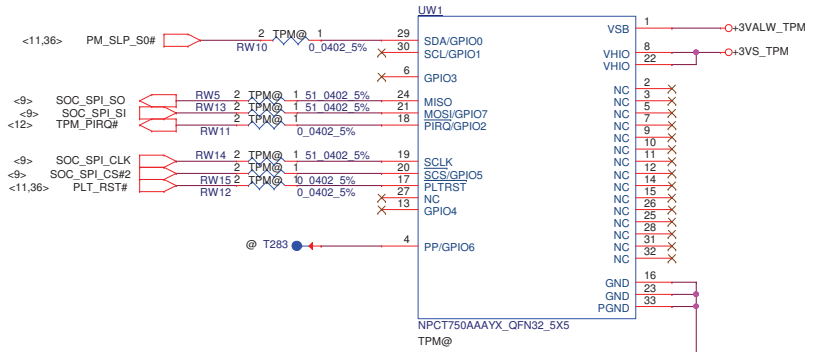
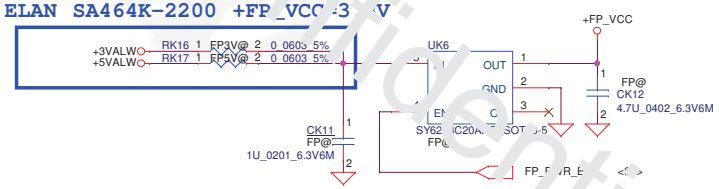


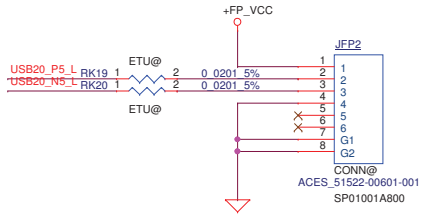


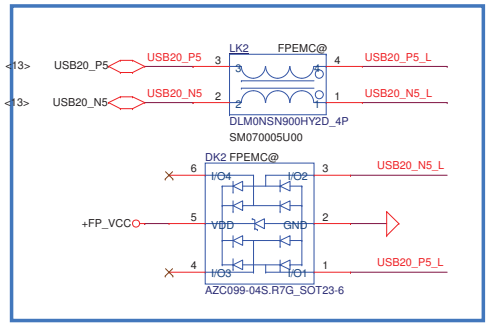
SA0000AQ230, S IC NPCT750AAAYX QFN 32P TPM (SPI interface)

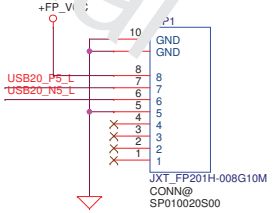
Finger Print

Power Souce Chec
EGIS ETU801 +FP_V
ELAN SA464K-2200 +FP_VCC 3.3V









PIN	ETU801	SA464K-2200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

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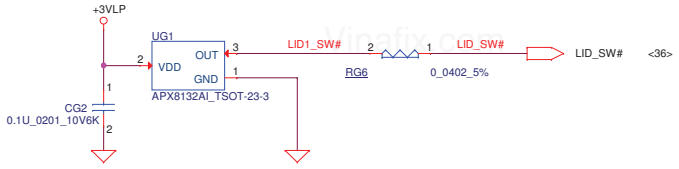
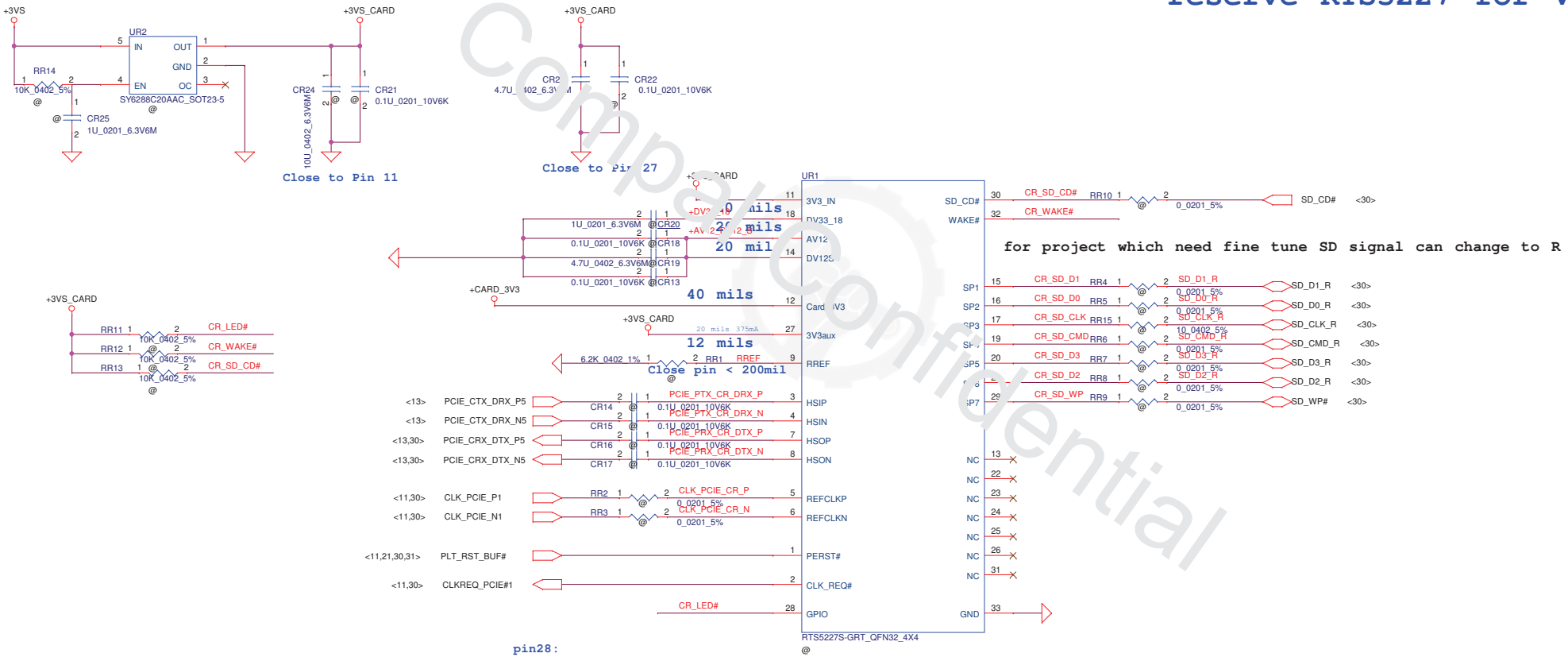
LID



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

reserve RTS5227 for VPRO



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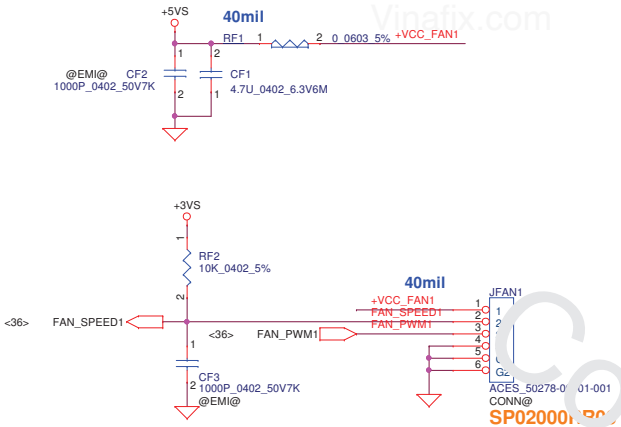
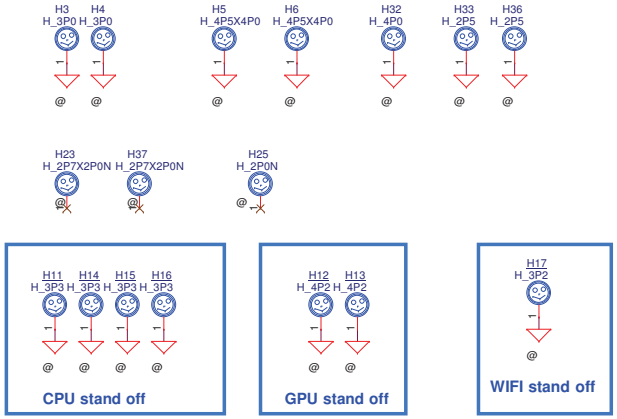
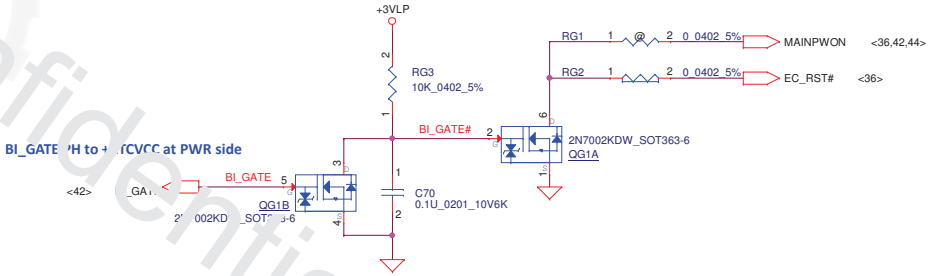
FAN1 Conn



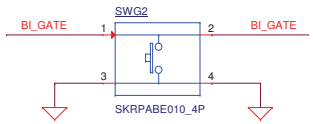
Screw Hole



Reset Circuit



Reset Button



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Title: FAN & Screw Hole & Reset

Size	Document Number	Rev
Custom	EH5AW M/B LA-G521P	0.1

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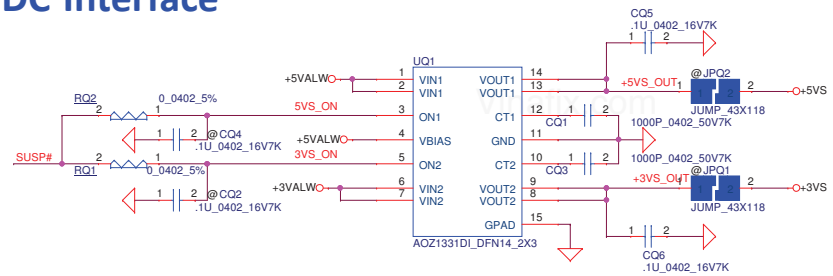
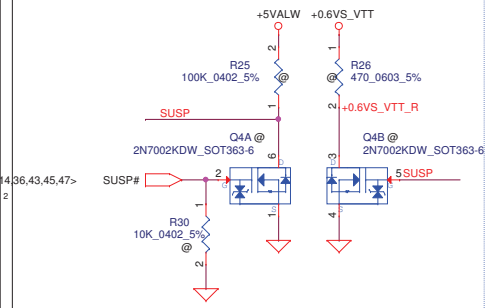
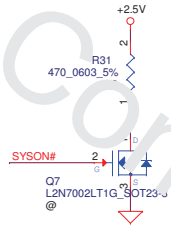
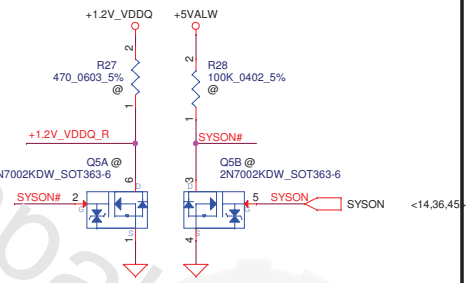
DC Interface

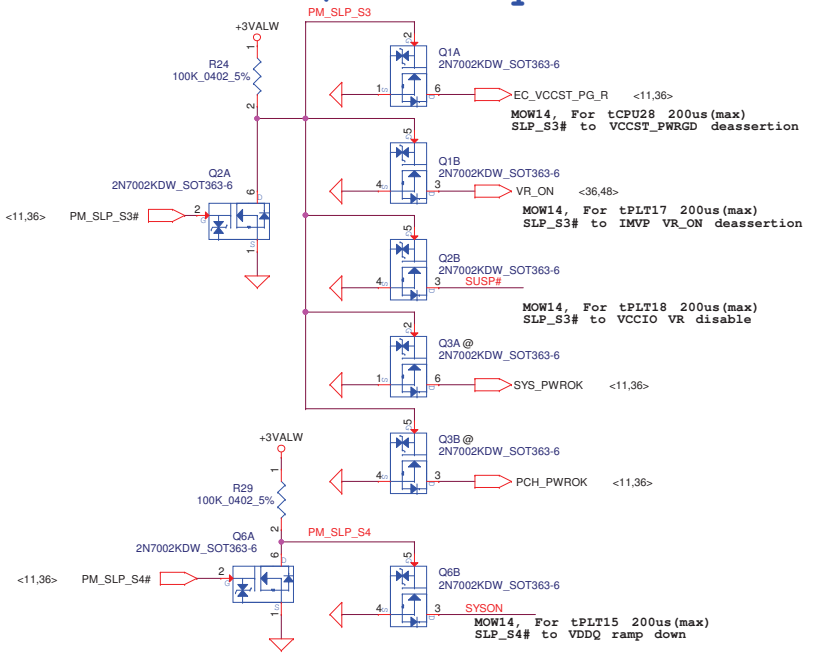


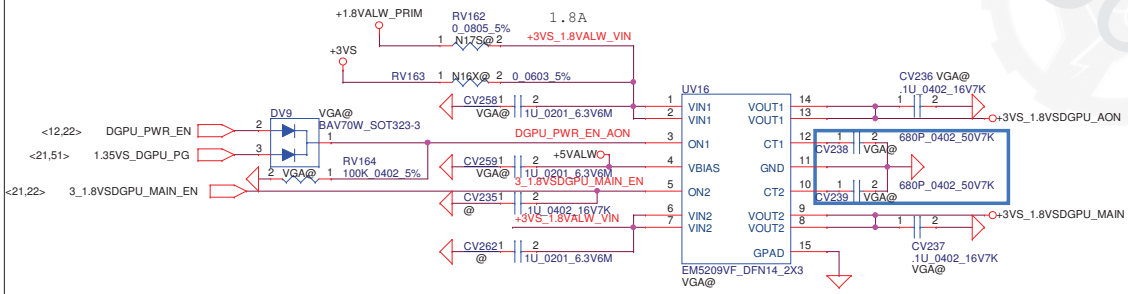


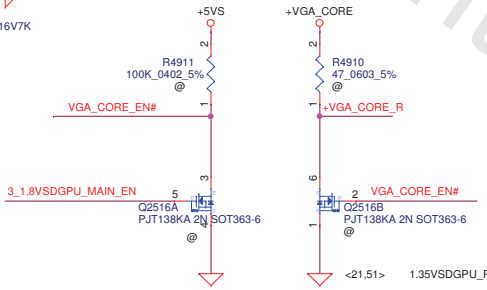


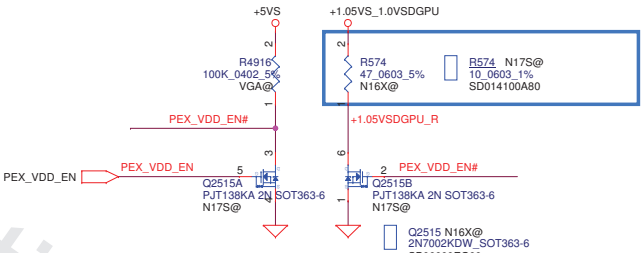


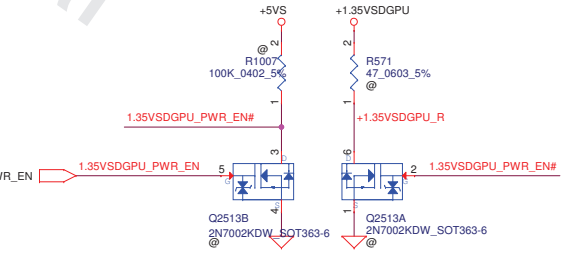
For Power ON/Off Sequence











+3VS to +3VSDGPU_AON for GPU

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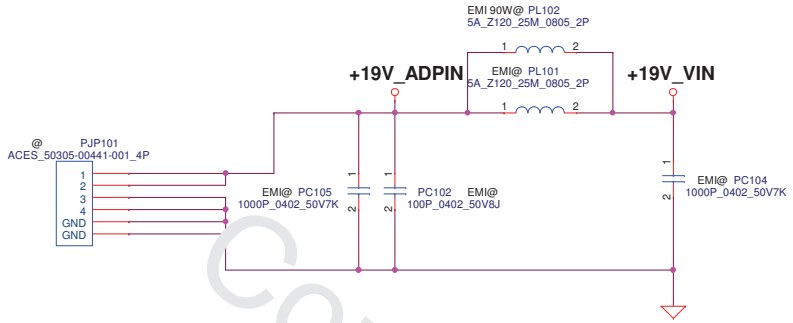

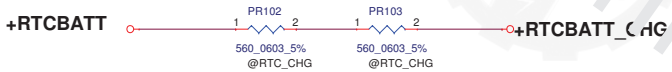

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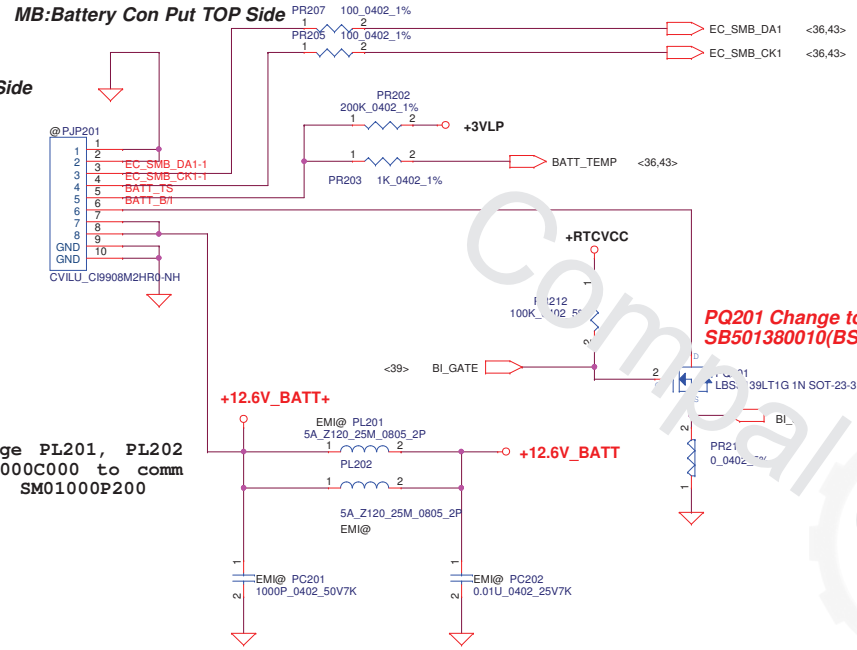
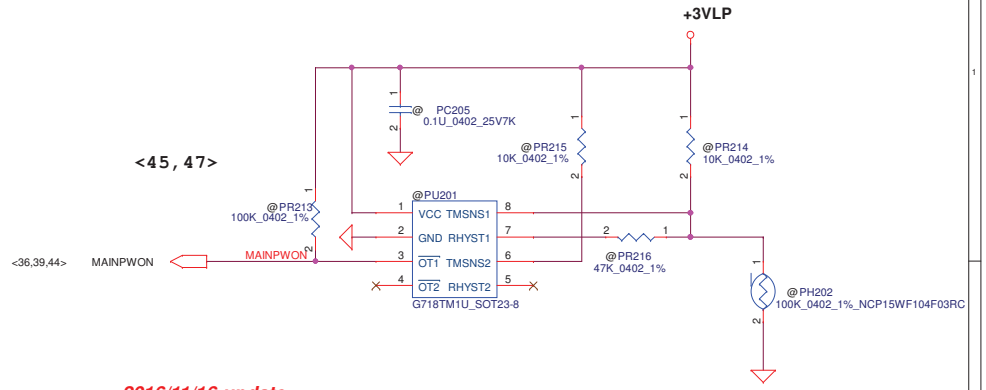
2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200



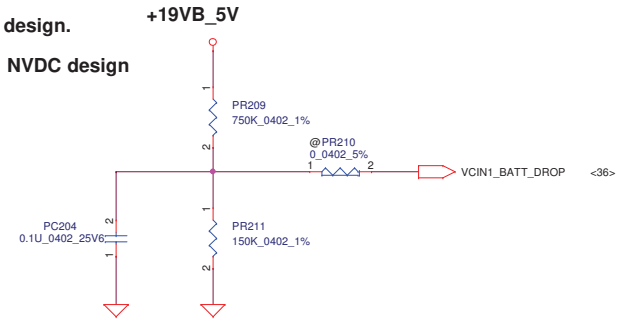
2016/11/16 update

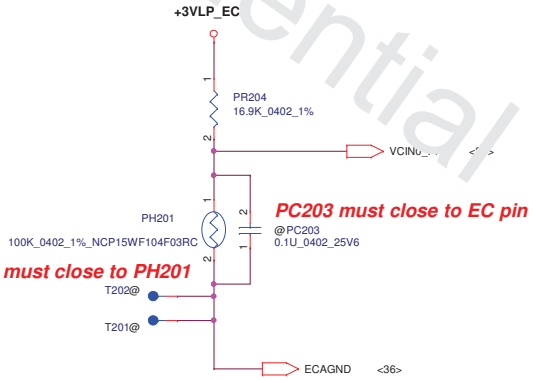
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm	58.5W,0.61V	Active=recovery
65W PR206 19.1K ohm	84.5W,0.61V	Active=recovery
90W PR206 30.1K ohm	117W,0.61V	Active=recovery
PH1	2V	1V

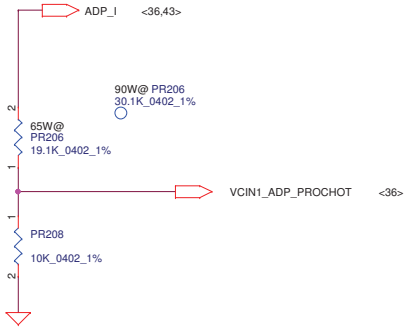
PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





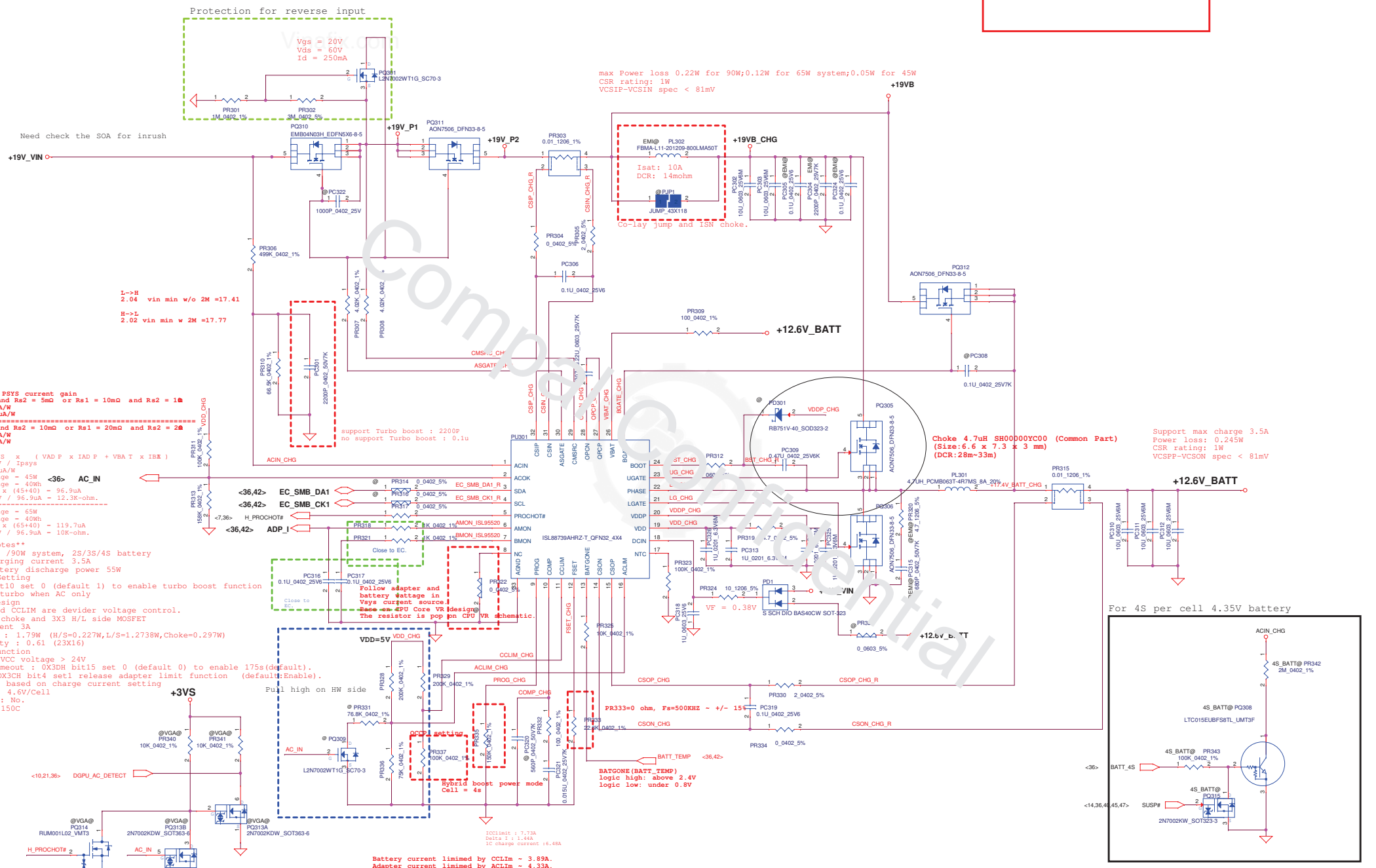


Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size Custom	Document Number EH5AW M/B LA-G521P		Rev 0.1
Date: Thursday, July 12, 2018	Sheet 42 of 57		

Module model information

ISL95520_Hybrid_Boost_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_CHARGER		
Size	Document Number		Rev 1.0
Date: Thursday, July 12, 2018		Sheet 43 of 57	

Module model information

RT6575D_DMOS_single_V1.mdd
RT6575D_DMOS_dual_V1.mdd

H/S Rds(on):typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
Ploss=0.42W

L/S Rds(on):typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A, Idsm(TA=70)=9A
Ploss=0.14W

CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, ... will pull high on V ... transfer circuit

5V-OCP=13.5A
3V-OCP=8.9A

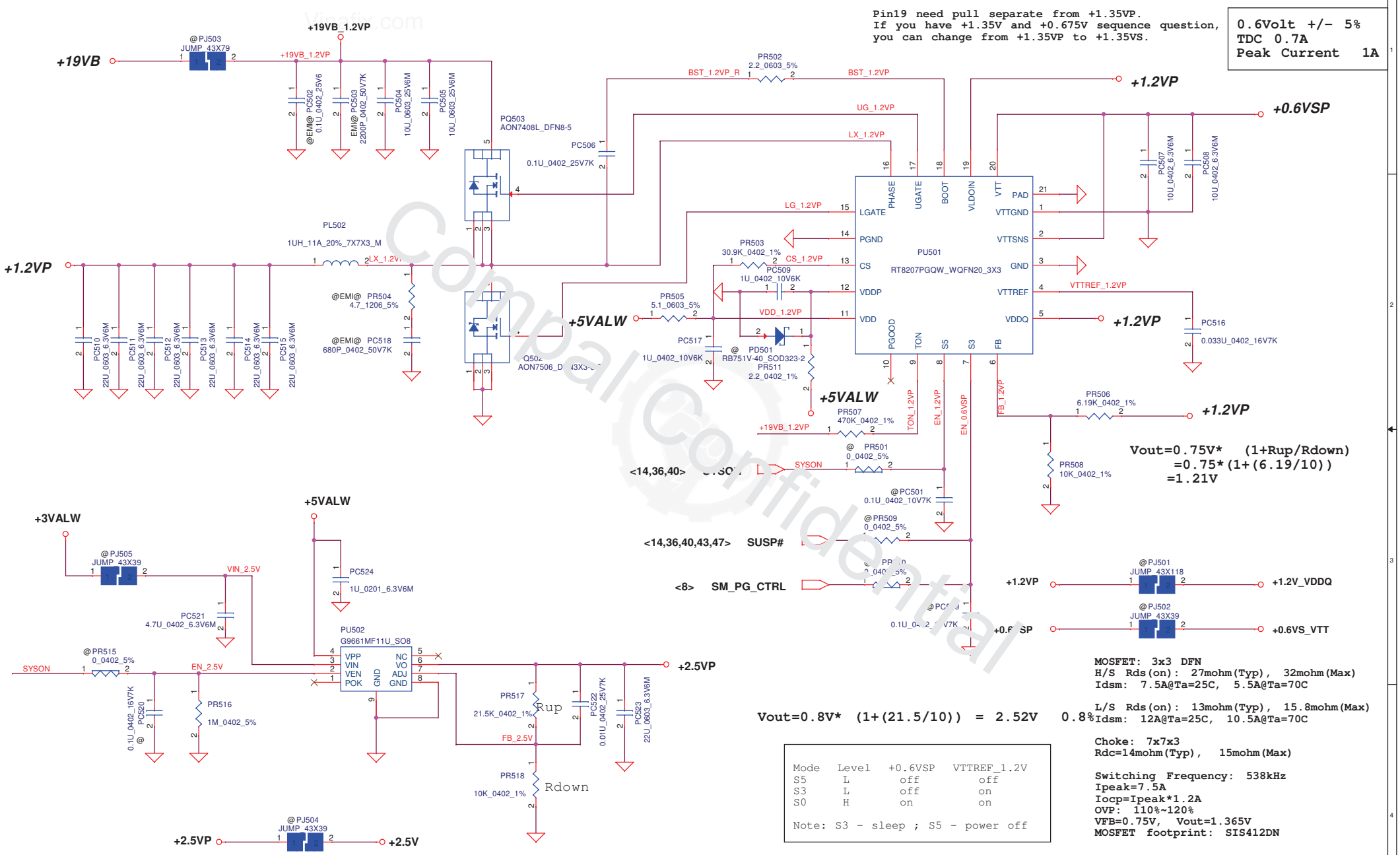
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Thursday, July 12, 2018 | Sheet 44 of 57



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 0.1

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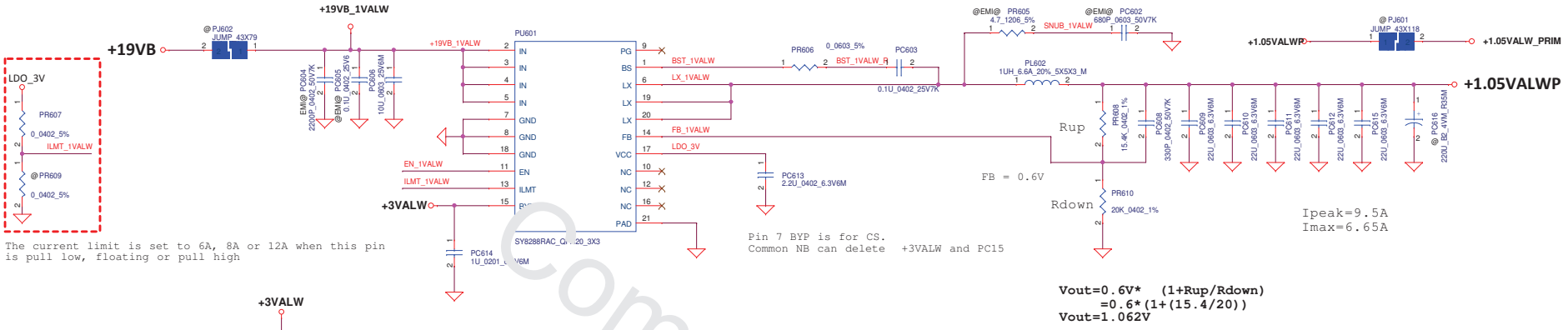
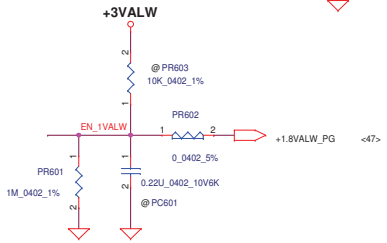
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(15.4/20))
Vout=1.062V



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

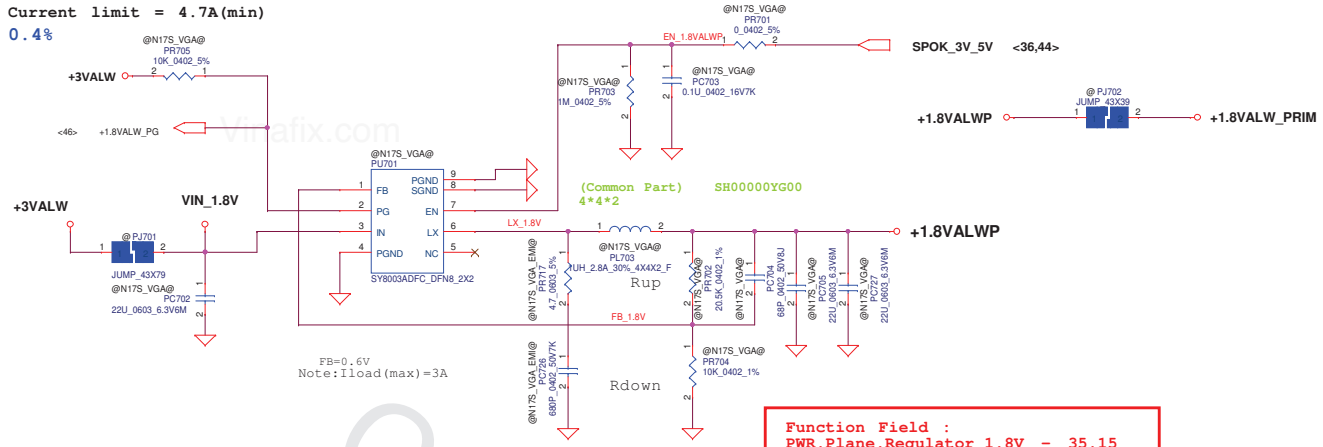
Compal Electronics, Inc.

Title: VCCP

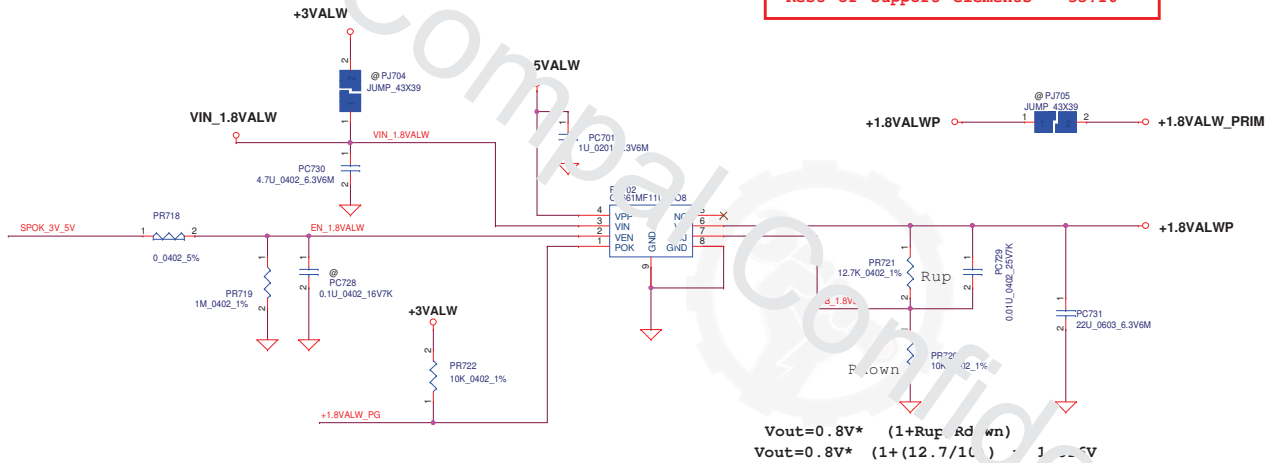
Size	Document Number	Rev
C	EH5AW M/B LA-G521P	0.1

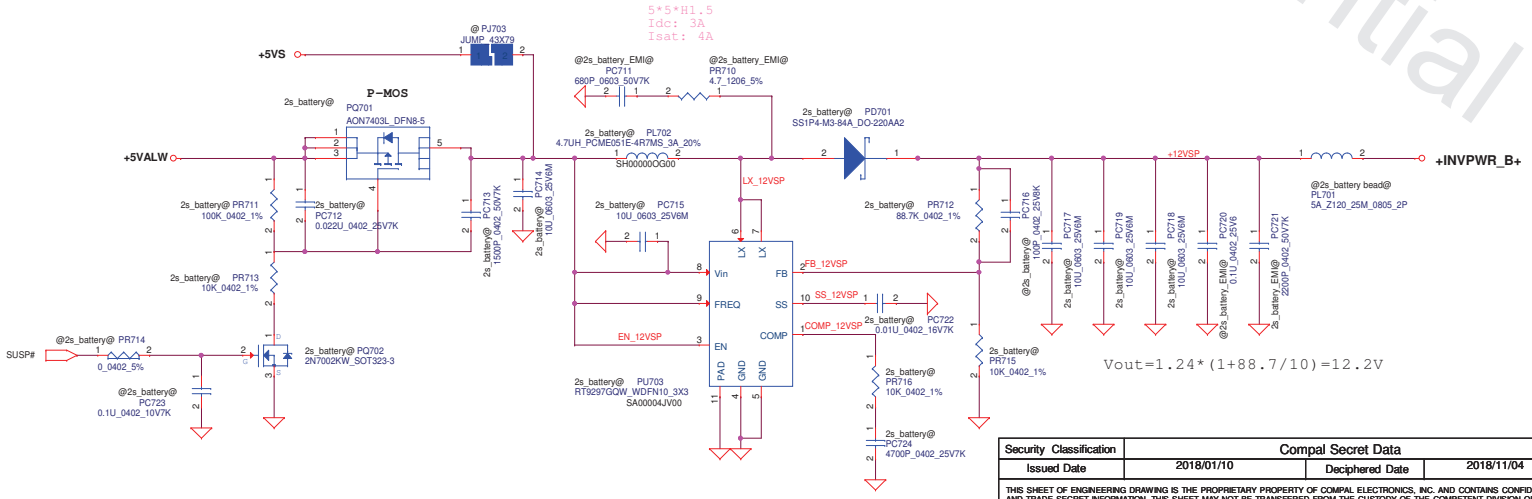
Date: Thursday, July 12, 2018 Sheet 46 of 57

Current limit = 4.7A(min)
0.4%



Function Field :
PWR.Plane.Regulator_1.8V - 35.15
Rest of support elements - 35.16





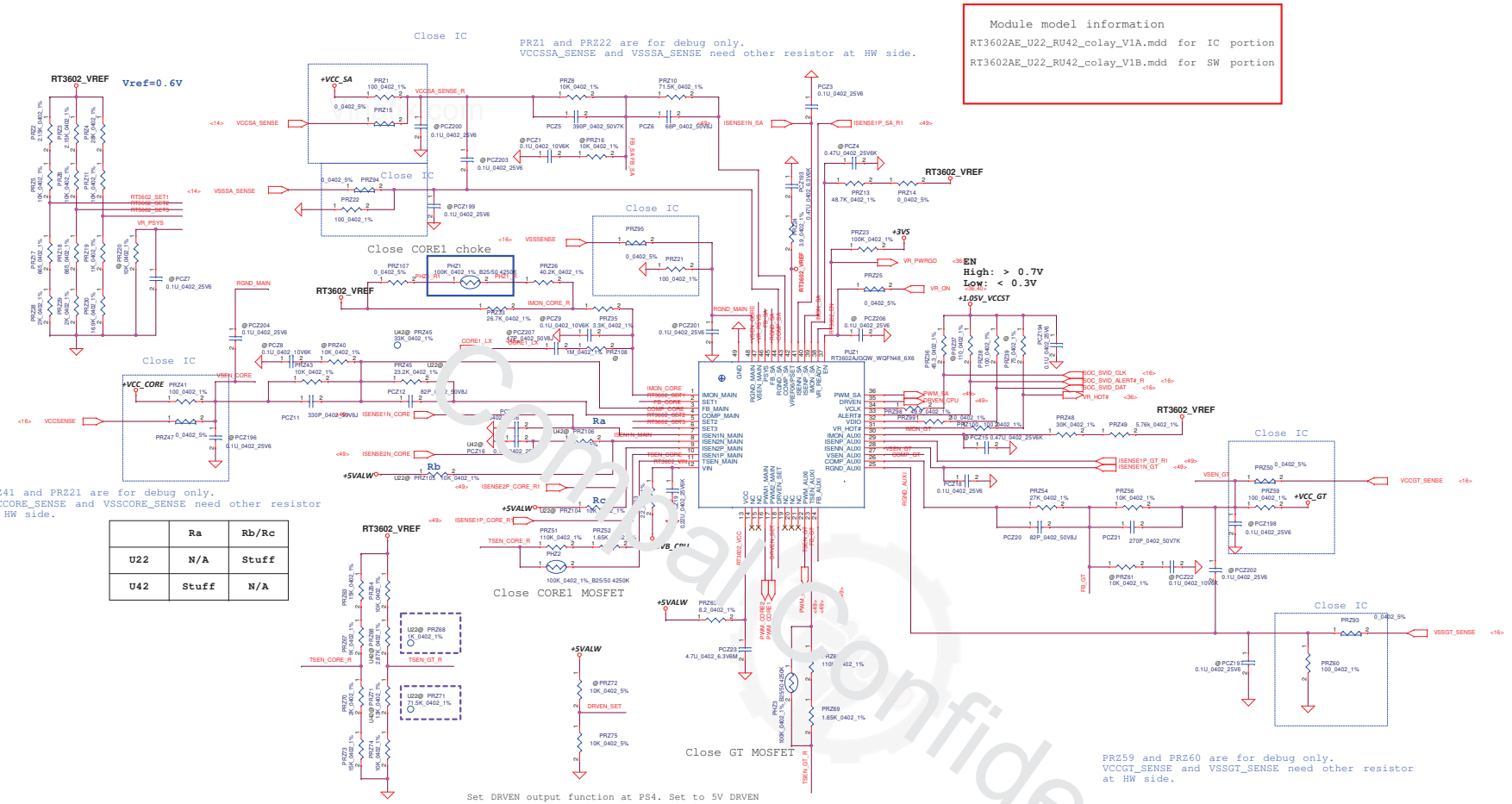
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	0.1

Date: Thursday, July 12, 2018 Sheet 47 of 57



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

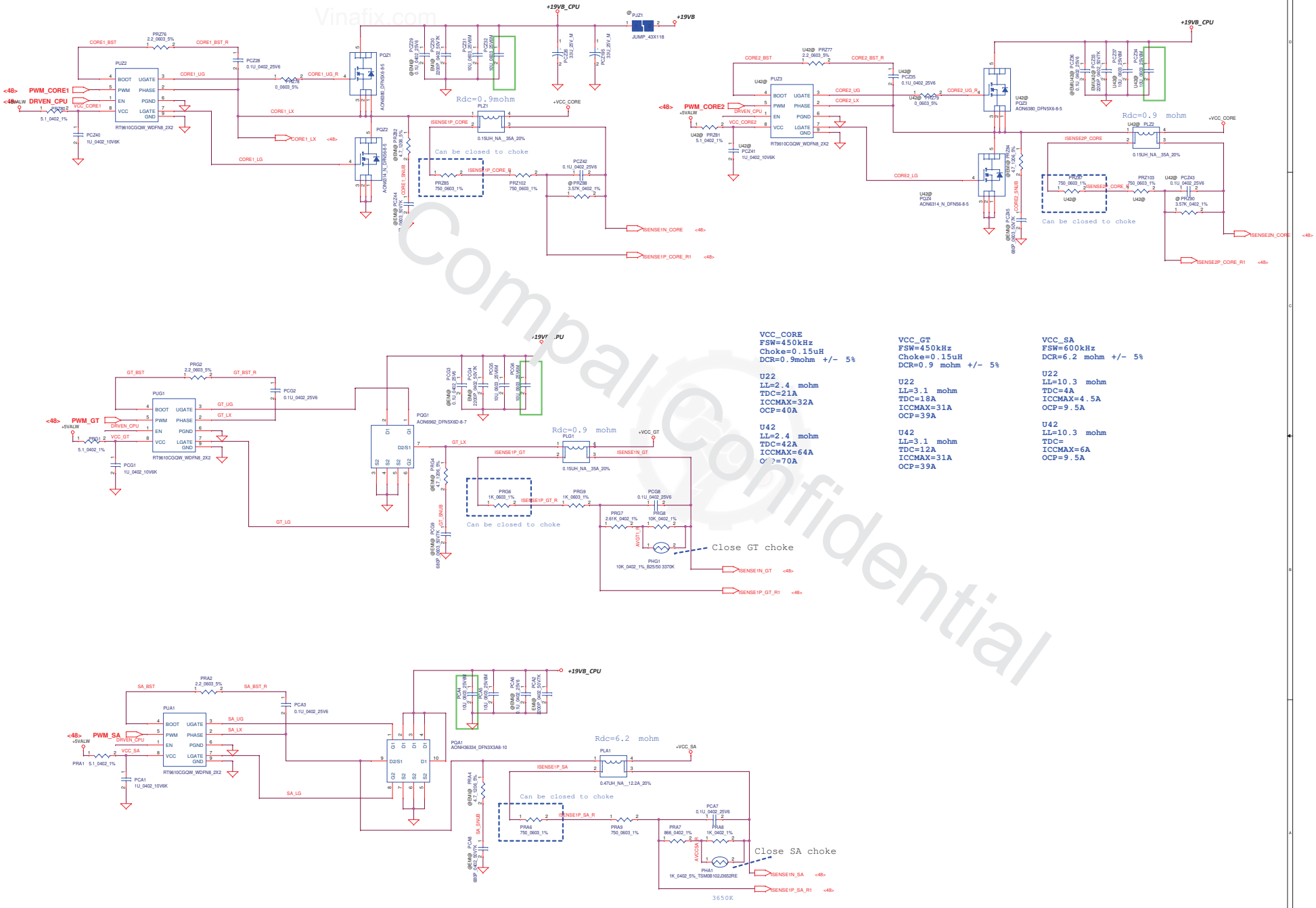
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: CPU_CORE

Size: Document Number: EH5AW M/B LA-G521P Rev: 0.1

Date: Thursday, July 12, 2018 Sheet 48 of 57



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

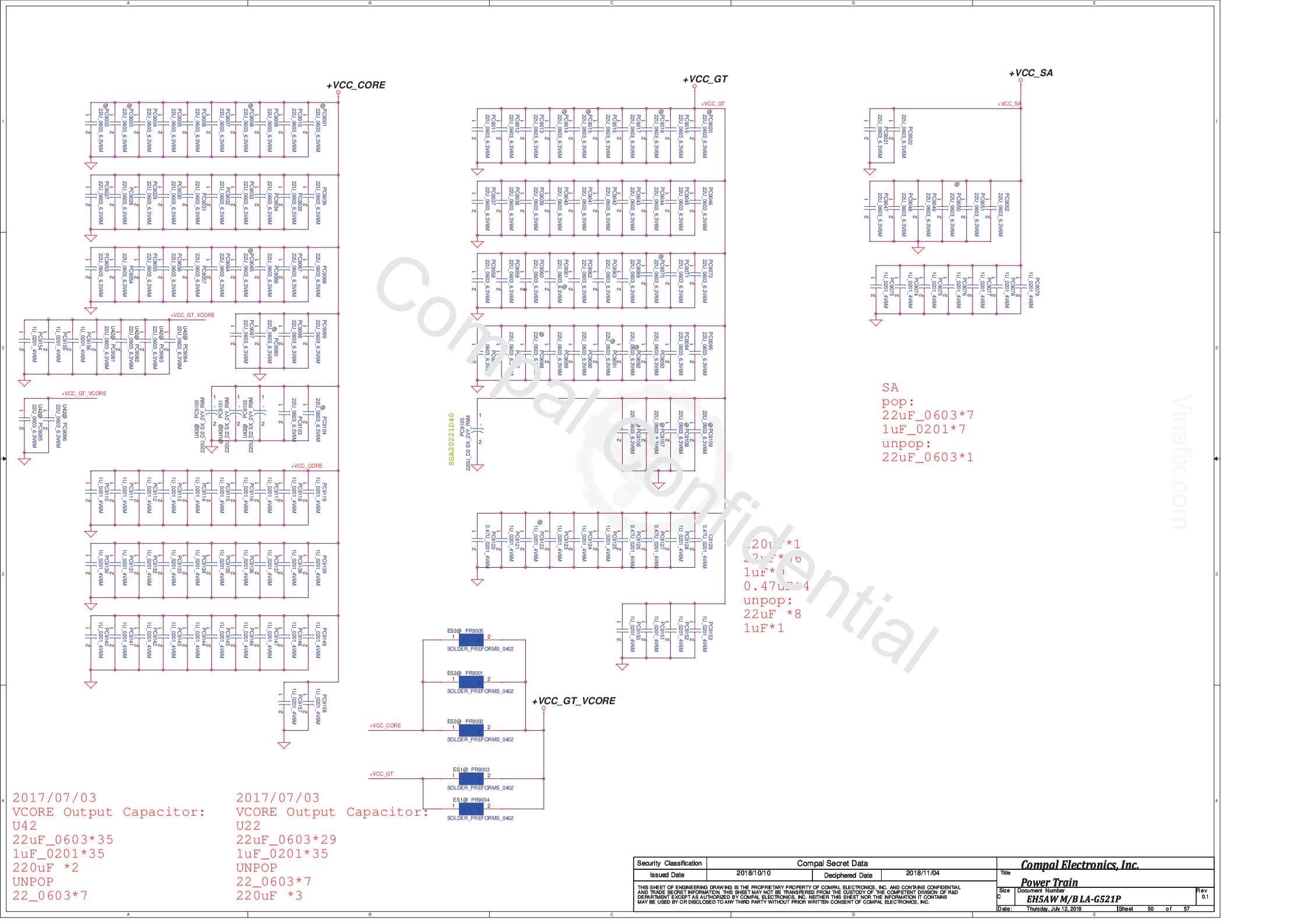
U42
LL=3.1 mohm
TDC=12A
ICCMAX=31A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=6A
OCP=9.5A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date	2019/09/01
Title	CPU Power stage		
Size	Document Number		Rev
	EH5AW M/B LA-G521P		0.1
Date:	Thursday, July 12, 2018	Sheet 49 of 57	



Security Classification	Compal Secret Data		
Issued Date	2018/10/10	Deciphered Date	2018/11/04

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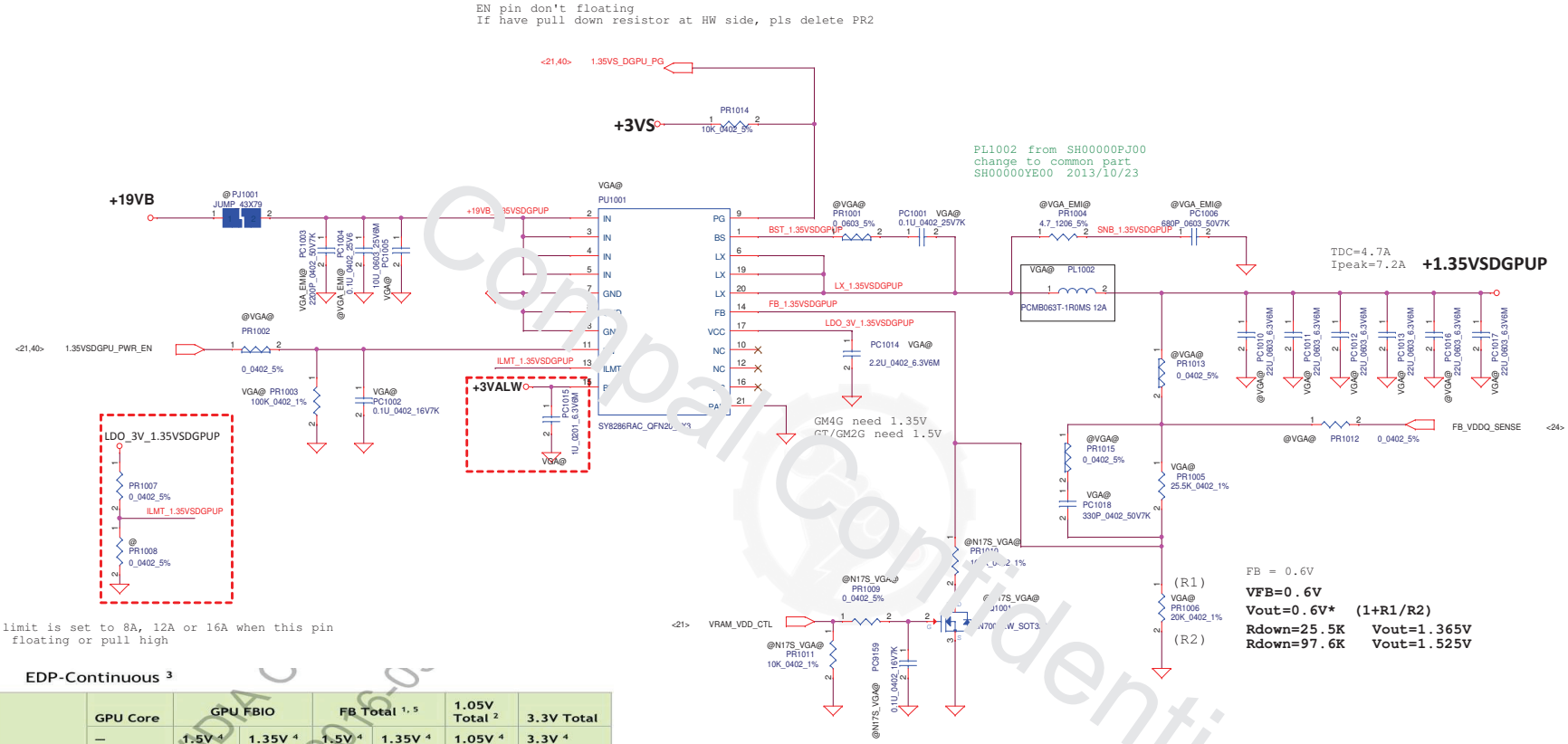
Compal Electronics, Inc.			
Title: Power Train			
Size: C	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, July 12, 2018	Sheet 50 of 57		



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6	—	9.5	2.9

Table 7. Output EDP-Continuous

Product	NVVDD	GPU FBIO	FB Total[5]	1.0V Total[1]	1.8V Total[2]
	—	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	—	1.35V[3]	1.35V[3]	1.0V[3]
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

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Title: Power Train

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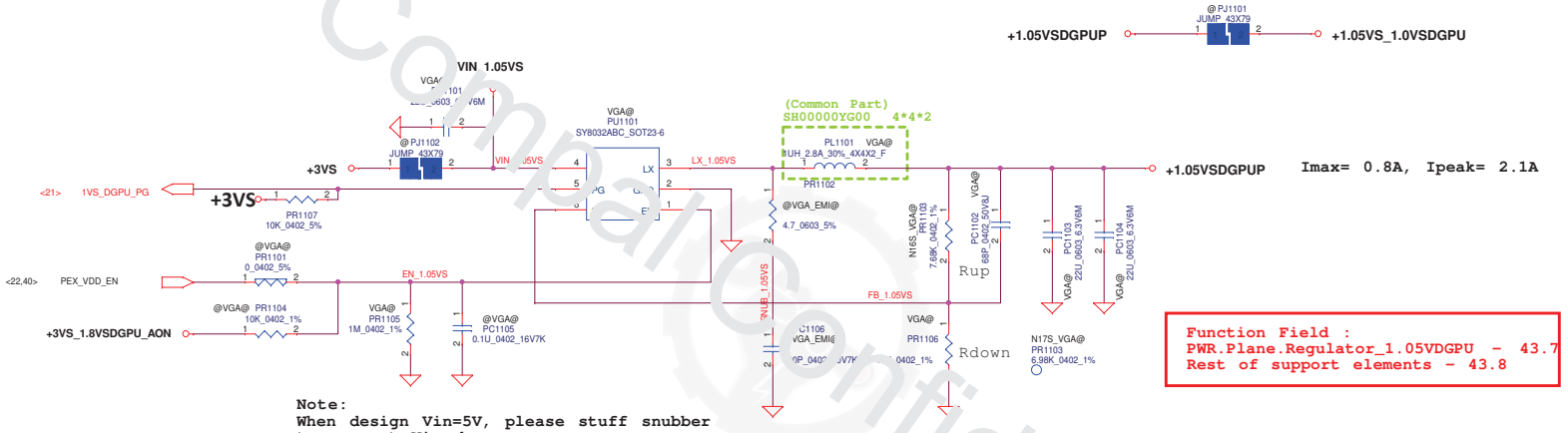
Date: Thursday, July 12, 2018 Sheet 51 of 57

Module model information

SY8032_V2.mdd



Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
N16=>1.05V
=>0.6V*(1+7.68/10)=1.061 (1.01%)
=>0.6V*(1+6.32/10)=1.039 (-1%)

N17=>1.0V
Vout=0.6V*(1+(6.98/10)=1.01 V (1.02)

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Power Train

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C	EH5AW M/B LA-G521P	0.1

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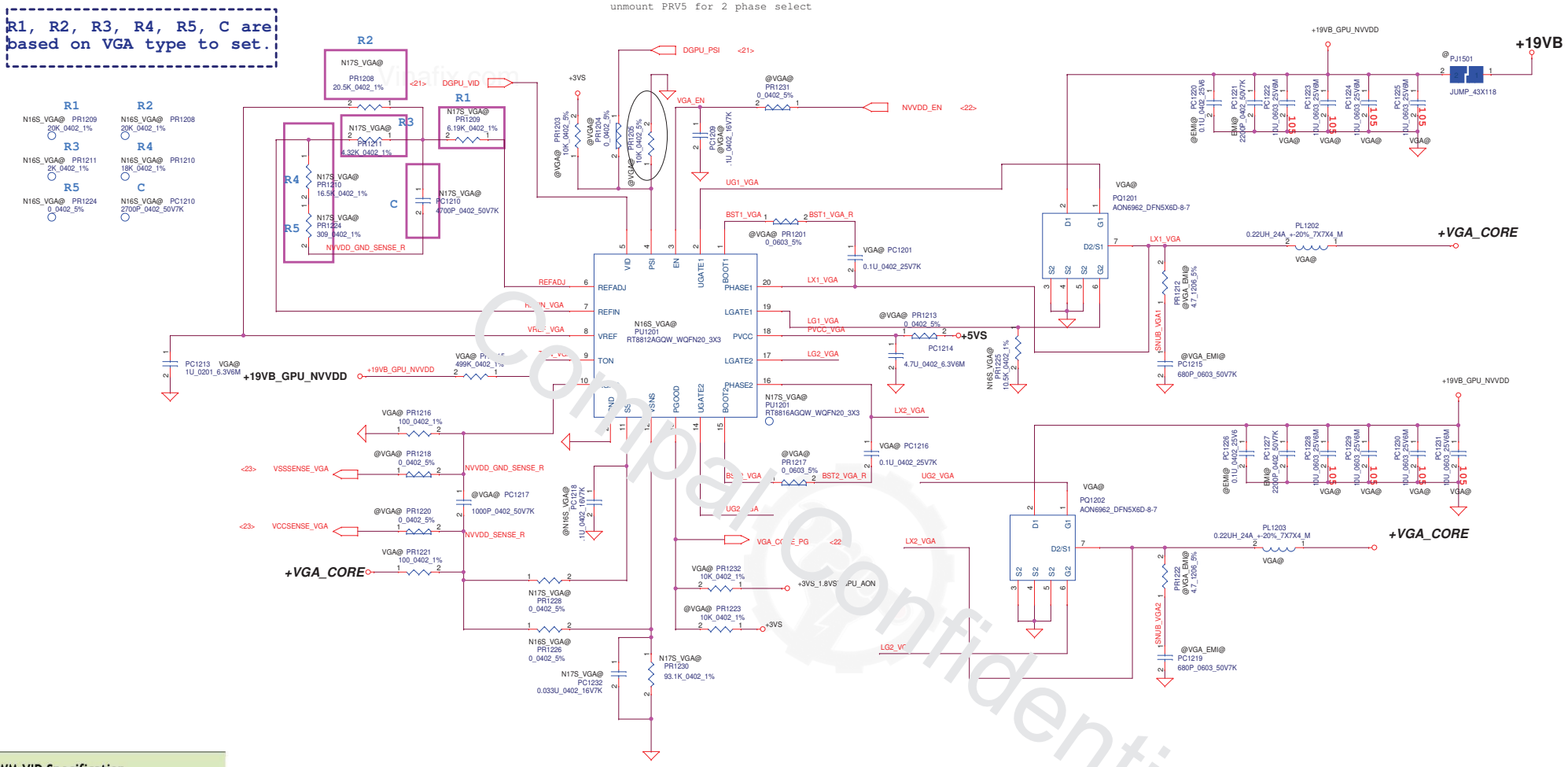
R1, R2, R3, R4, R5, C are based on VGA type to set.



PWM-VID Specification		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F_{PWM}	MHz	1.125
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core — (A)
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core — (A)
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

Product	NVVDD — (A)	GPU FBIO — 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD — (A)	GPU FBIO — 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	0.1

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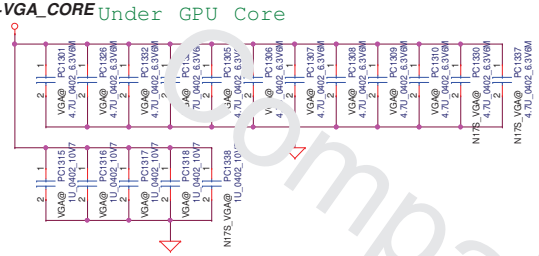
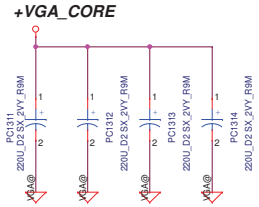
GB4-128 package

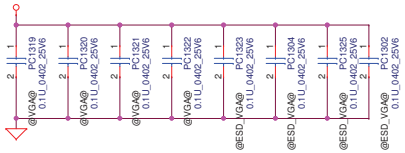
+VGA_CORE Under GPU Core



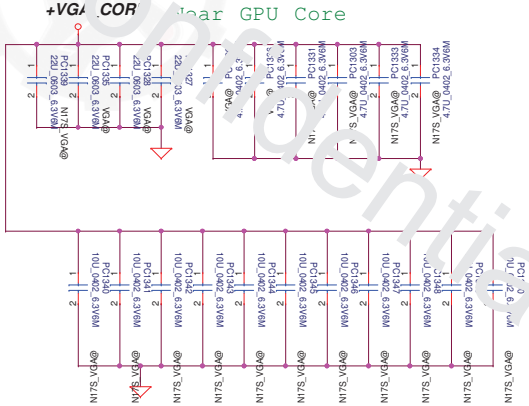
+VGA_CORE



+VGA_CORE



+VGA_CORE Under GPU Core



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **Power Train**

Size	Document Number	Rev
C	EH5AW M/B LA-G521P	0.1

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