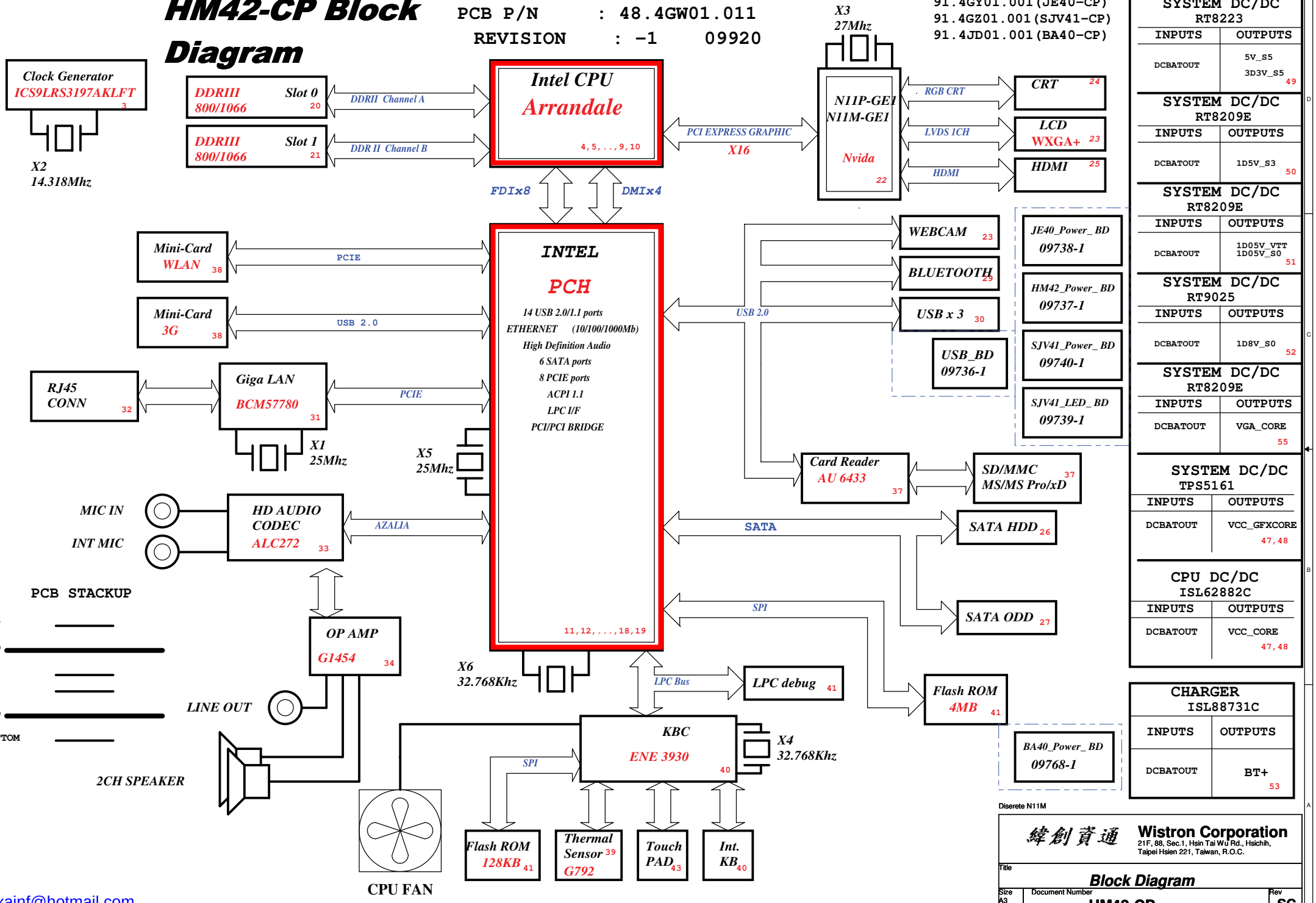
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001(HM42-CP)
91.4GY01.001(JE40-CP)
91.4GZ01.001(SJV41-CP)
91.4JD01.001(BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51

SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55

SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47,48

CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

Diserete N11M

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Title: Block Diagram
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

<Variant Name>

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Title: Table of Content

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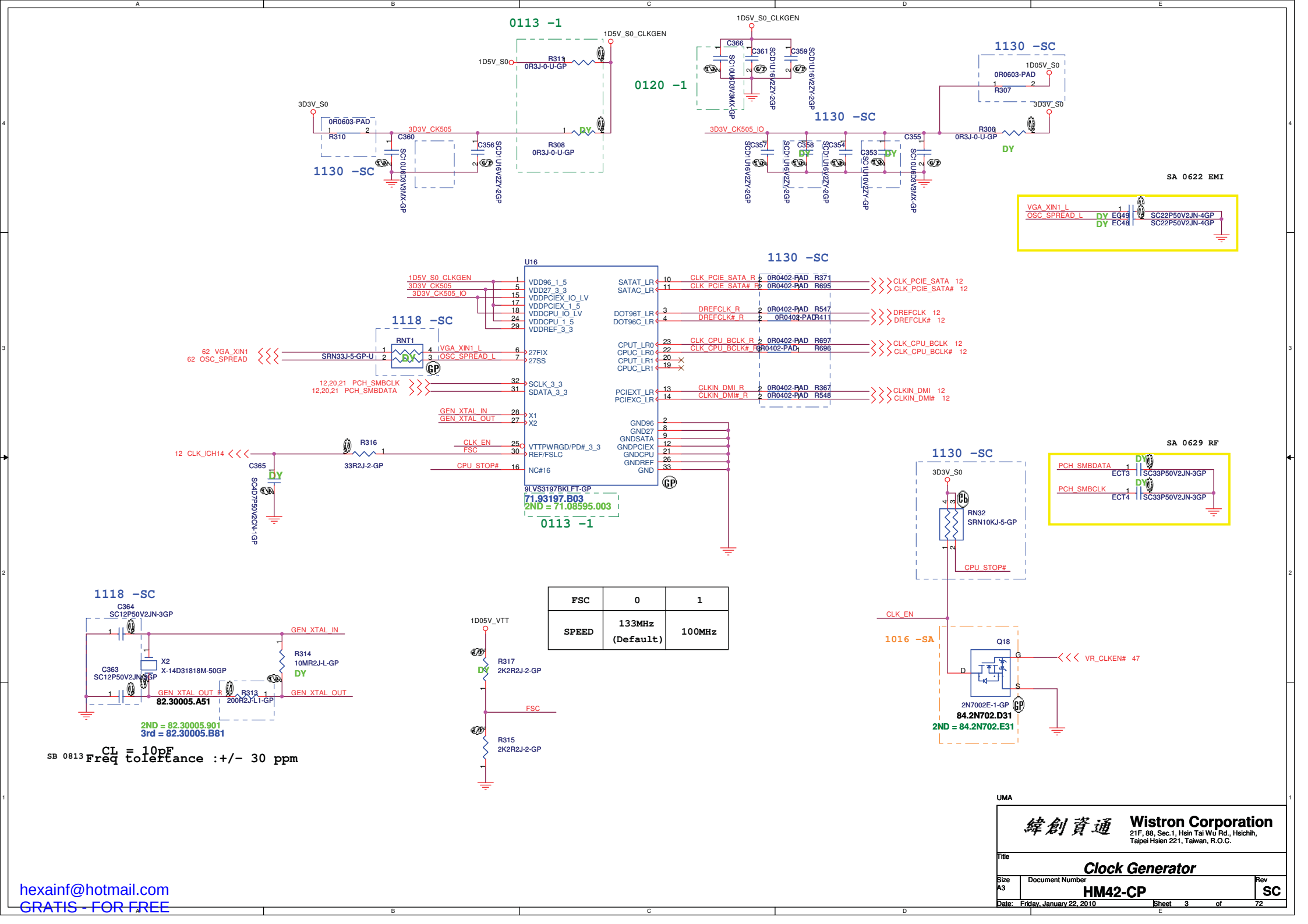

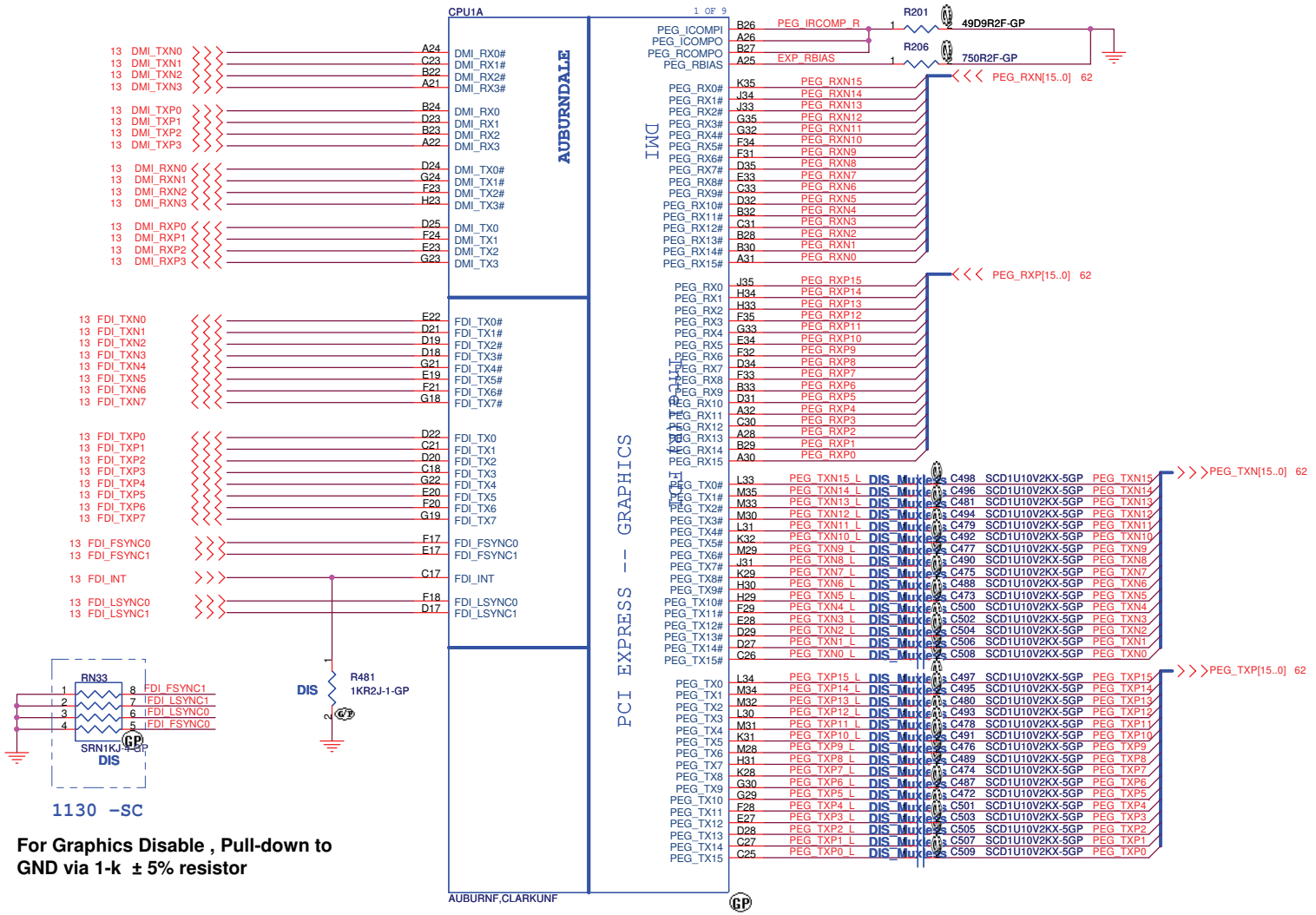

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Title: CPU (1/7)

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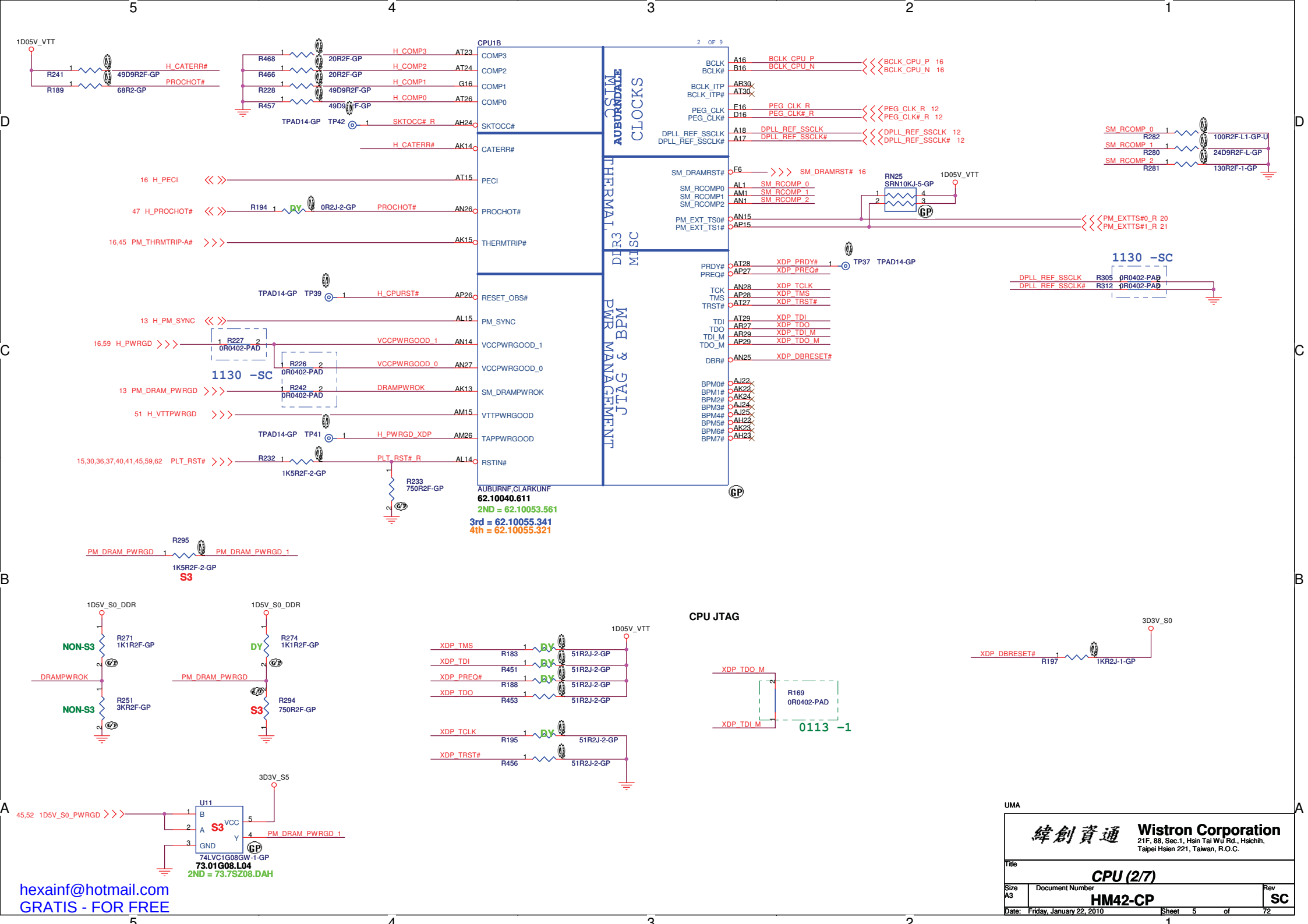
CPU1B
AUBURNDALE
CLOCKS
THERMAL, DIR3 MISC
JTAG & BPM
PWR MANAGEMENT
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
1130 -SC
S3
CPU JTAG
0113 -1
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
hexainf@hotmail.com
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UMA
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CPU (2/7)
HM42-CP
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Friday, January 22, 2010
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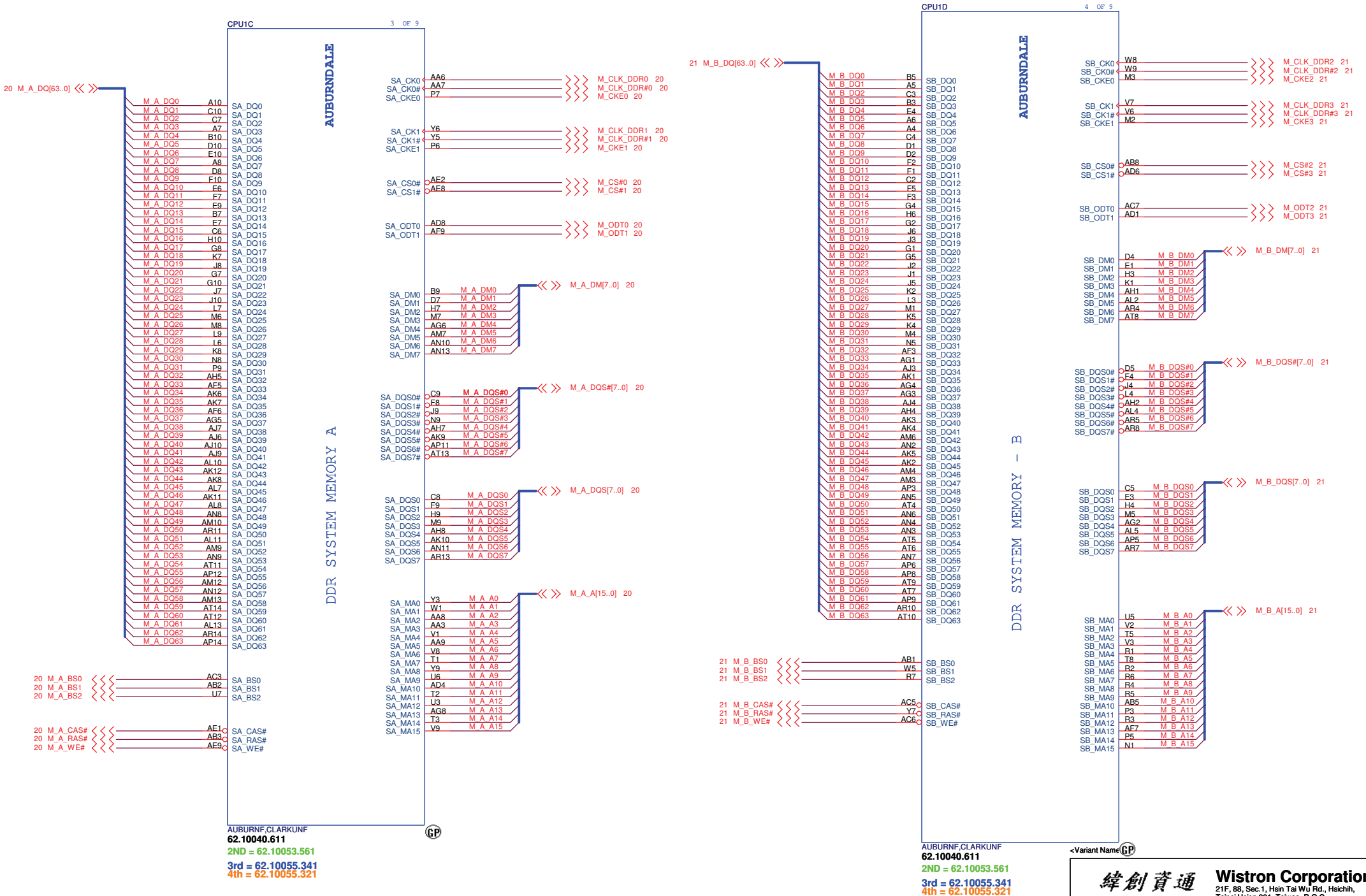

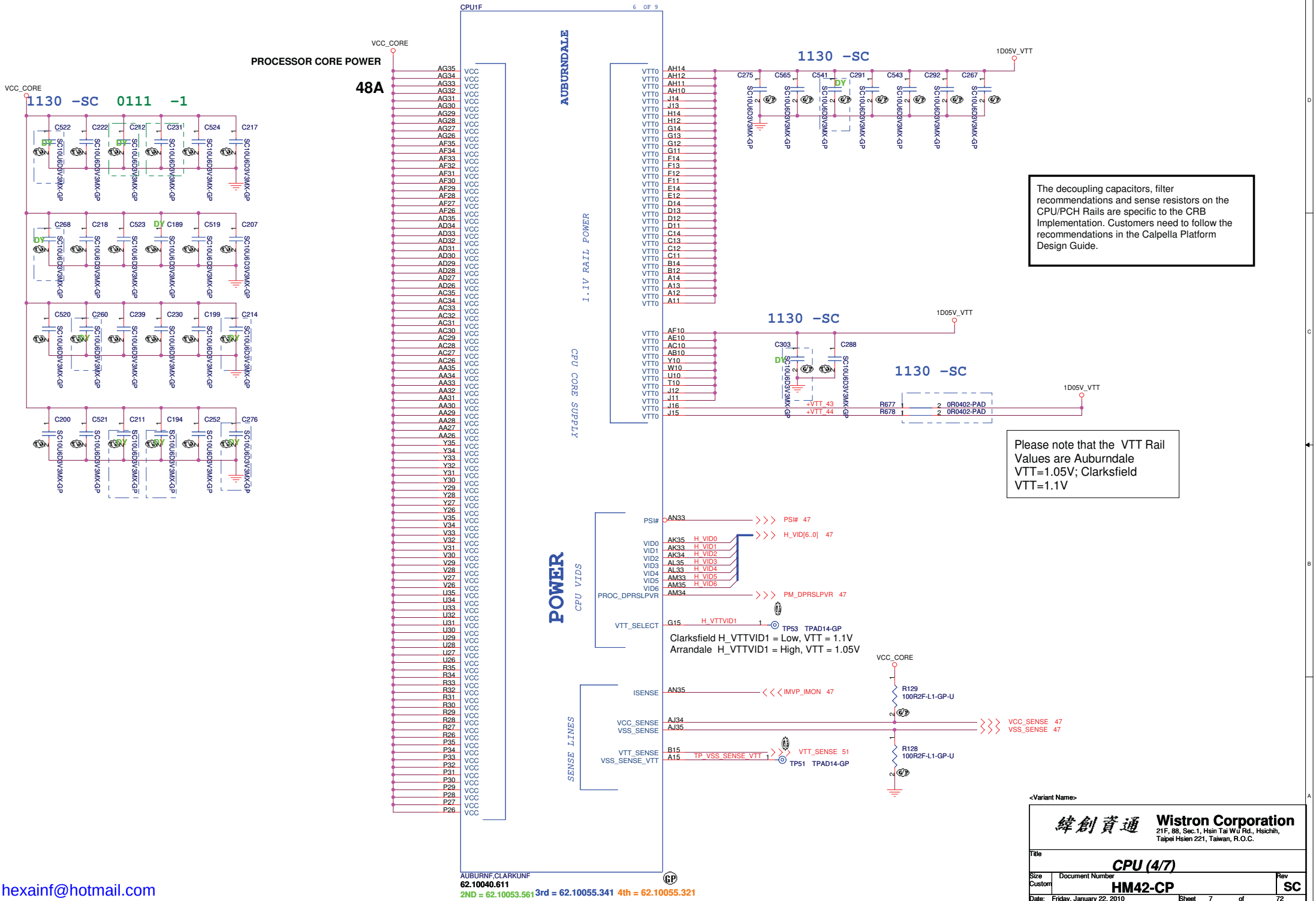

<Variant Name>

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Title: CPU (4/7)

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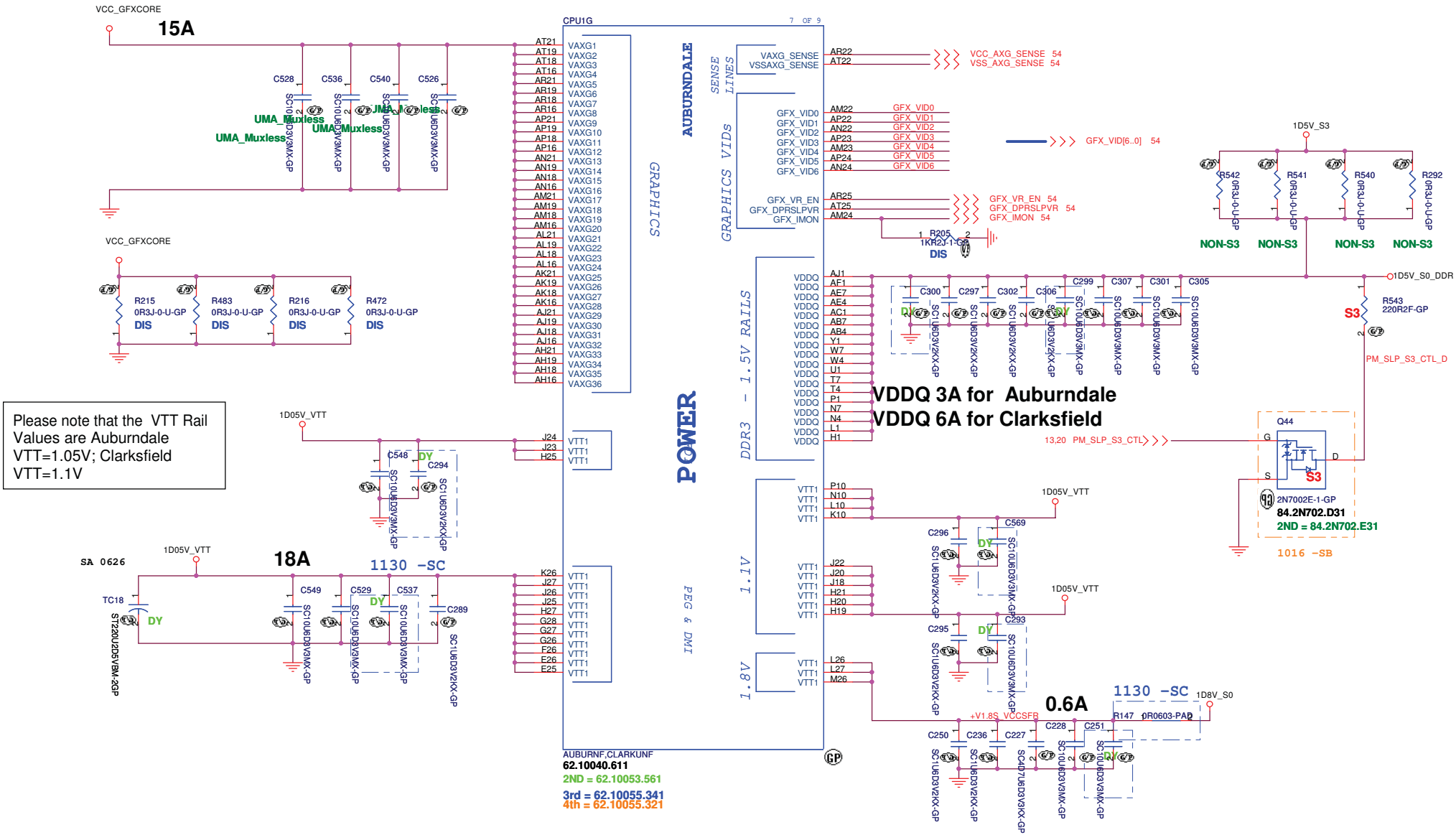

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Title: ***CPU (5/7)***		
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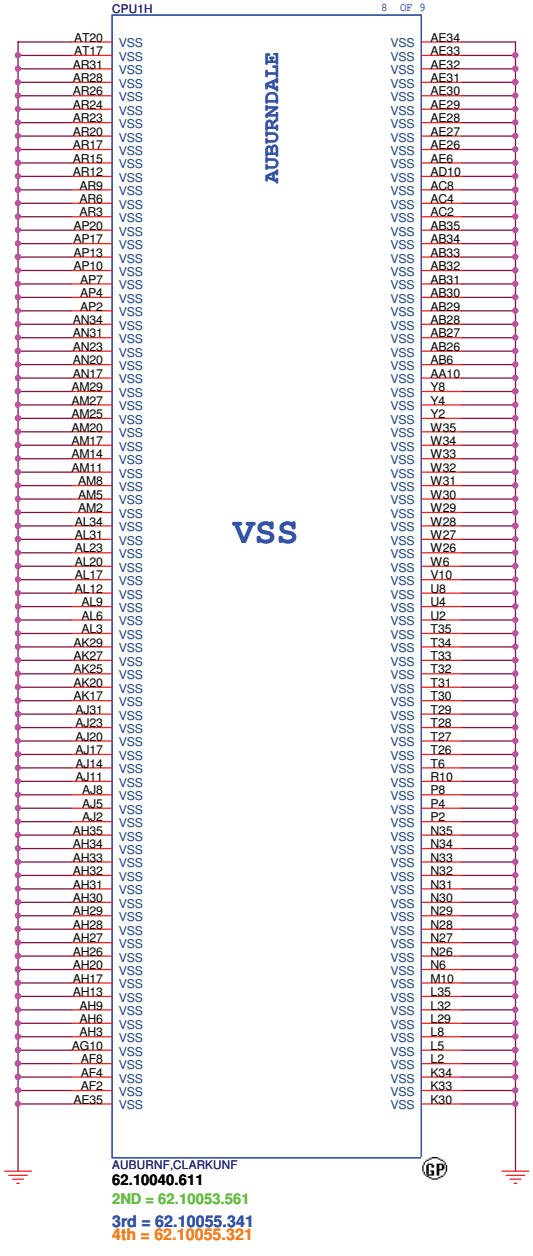

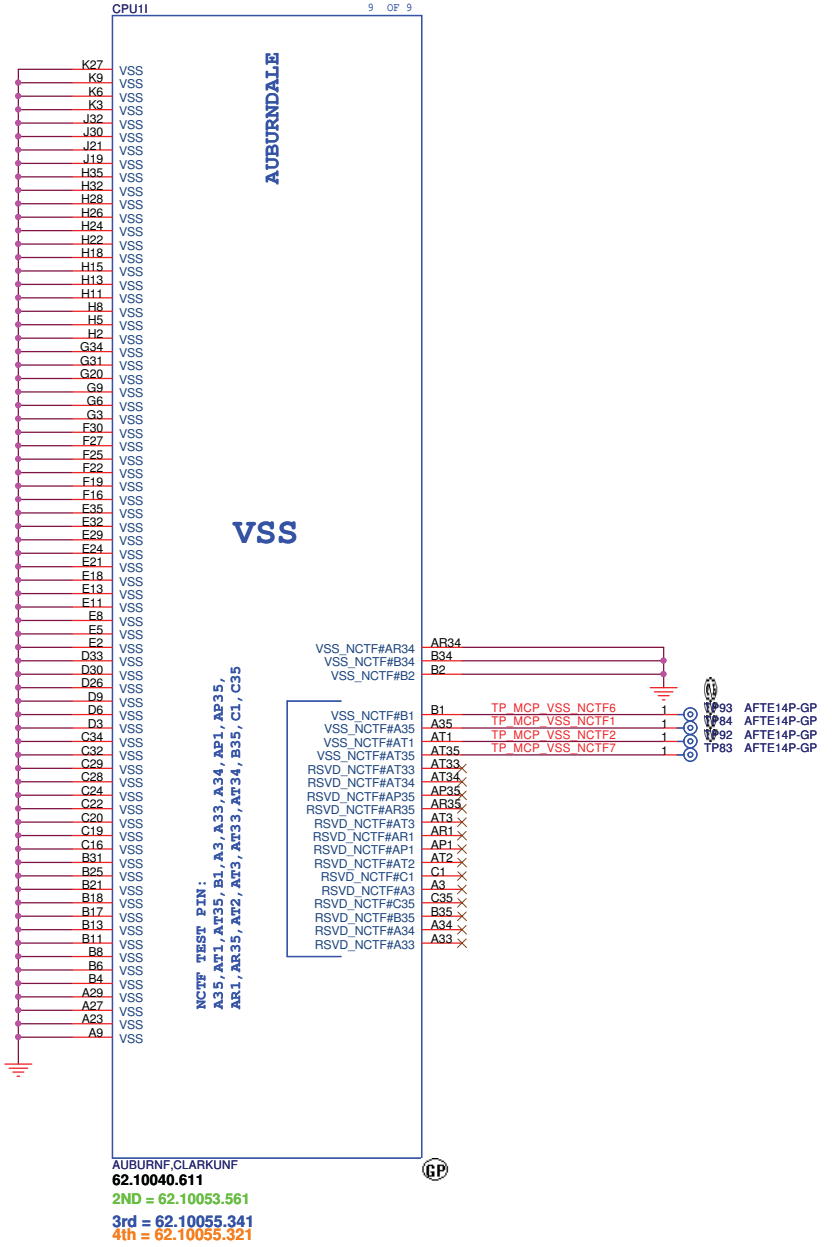

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Title: CPU (6/7)

Size: A3 | Document Number: HM42-CP | Rev: SC

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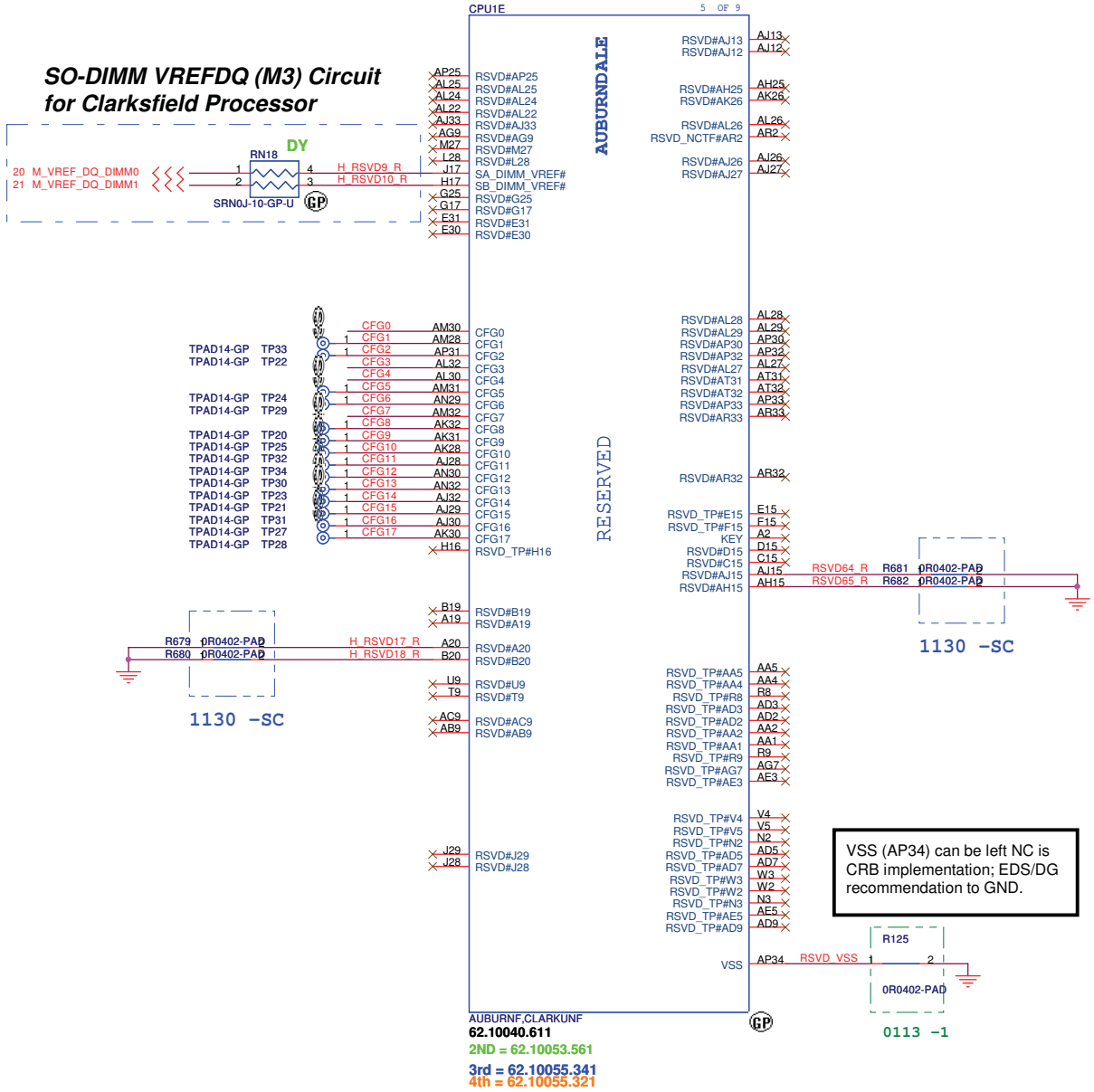

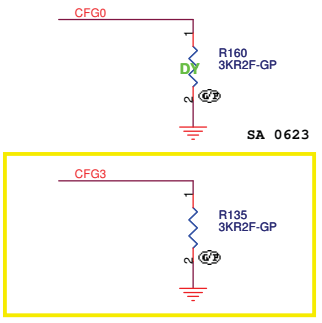

Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Variant Name>

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Title: CPU (7/7)

Size: A3 | Document Number: HM42-CP | Rev: SC

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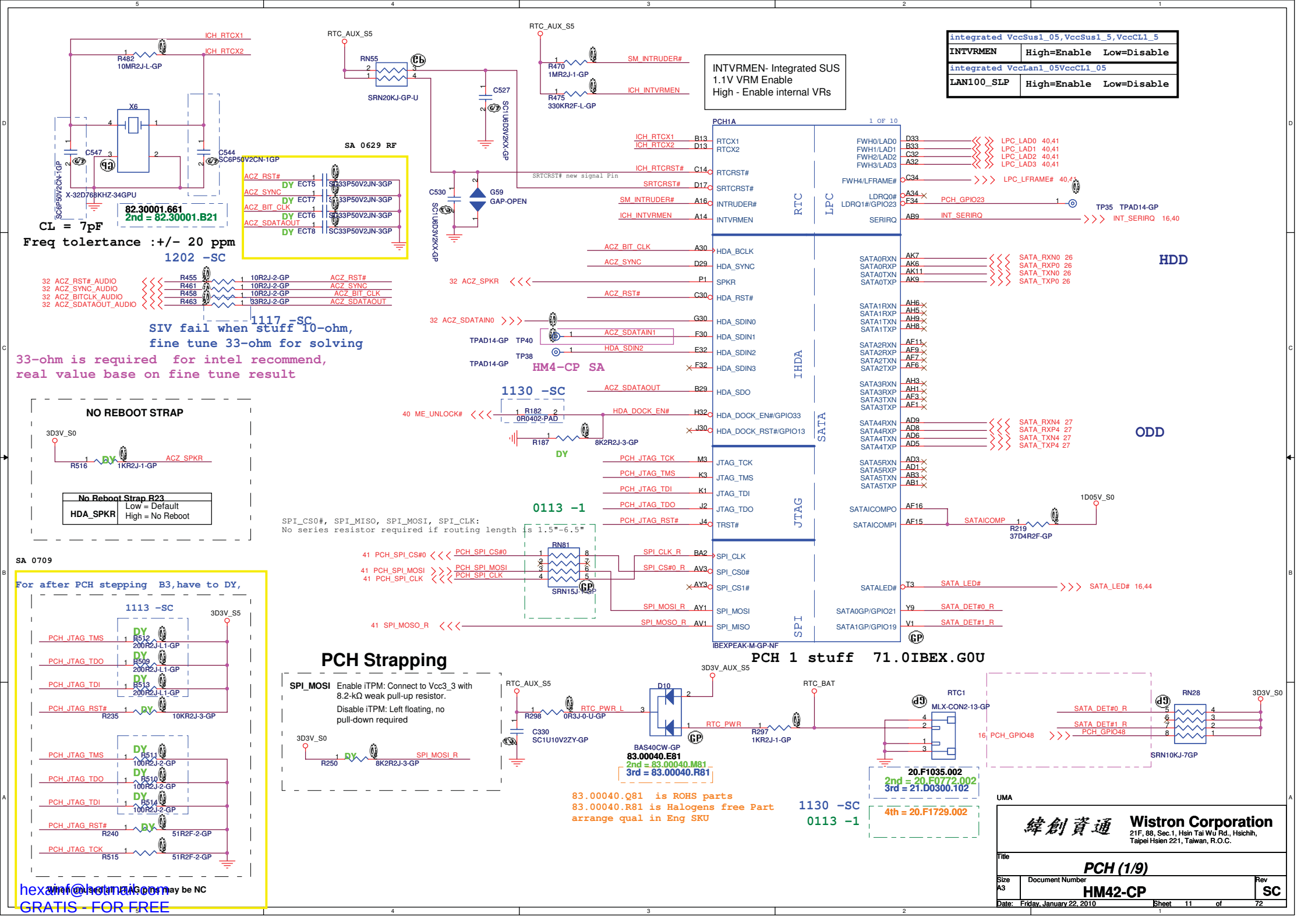

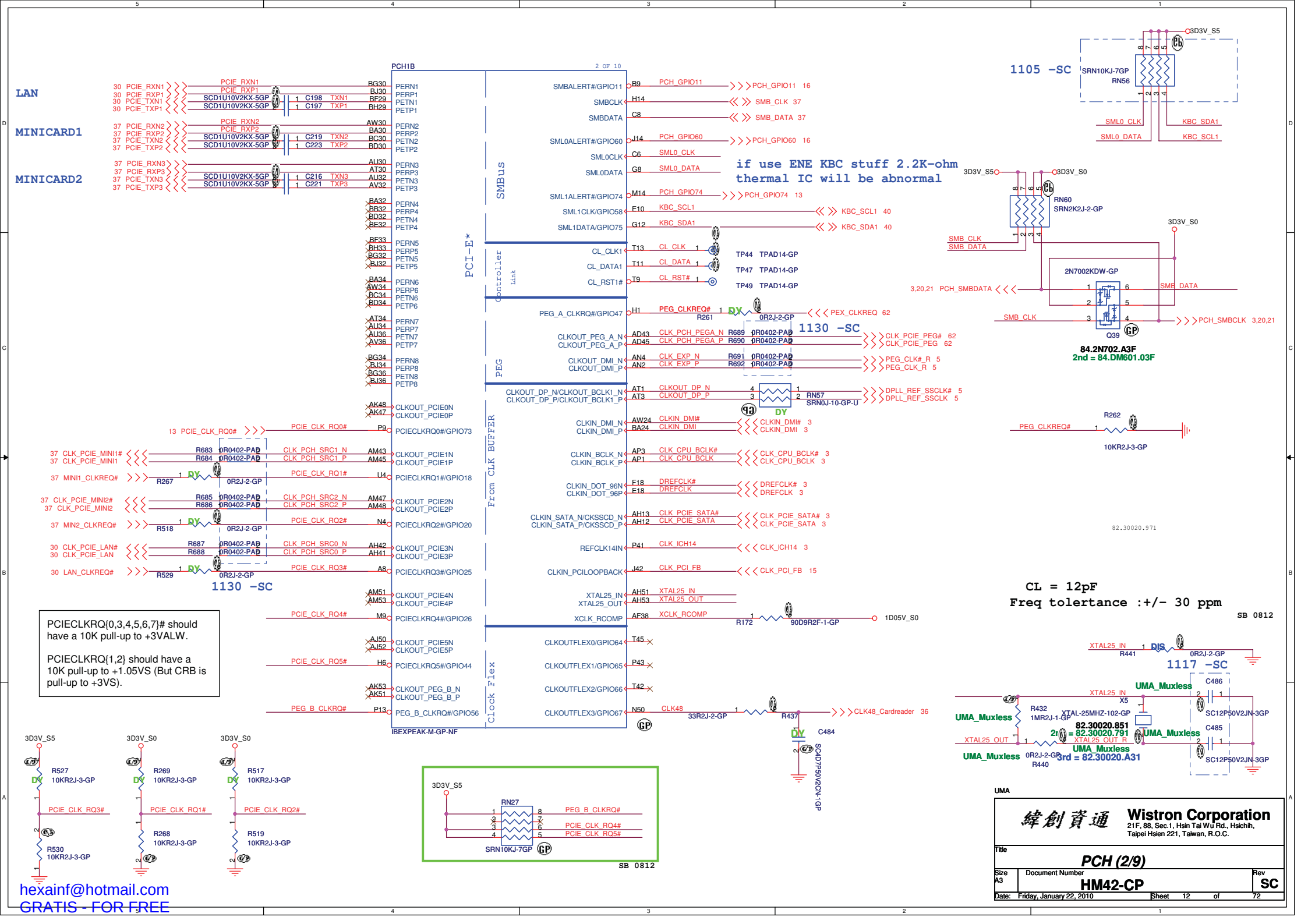
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal
1130 -SC
1105 -SC
1117 -SC
CL = 12pF
Freq tolertance :+/- 30 ppm
SB 0812
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
84.2N702.A3F
2nd = 84.DM601.03F
82.30020.971
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
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PCH (2/9)
HM42-CP
Rev SC
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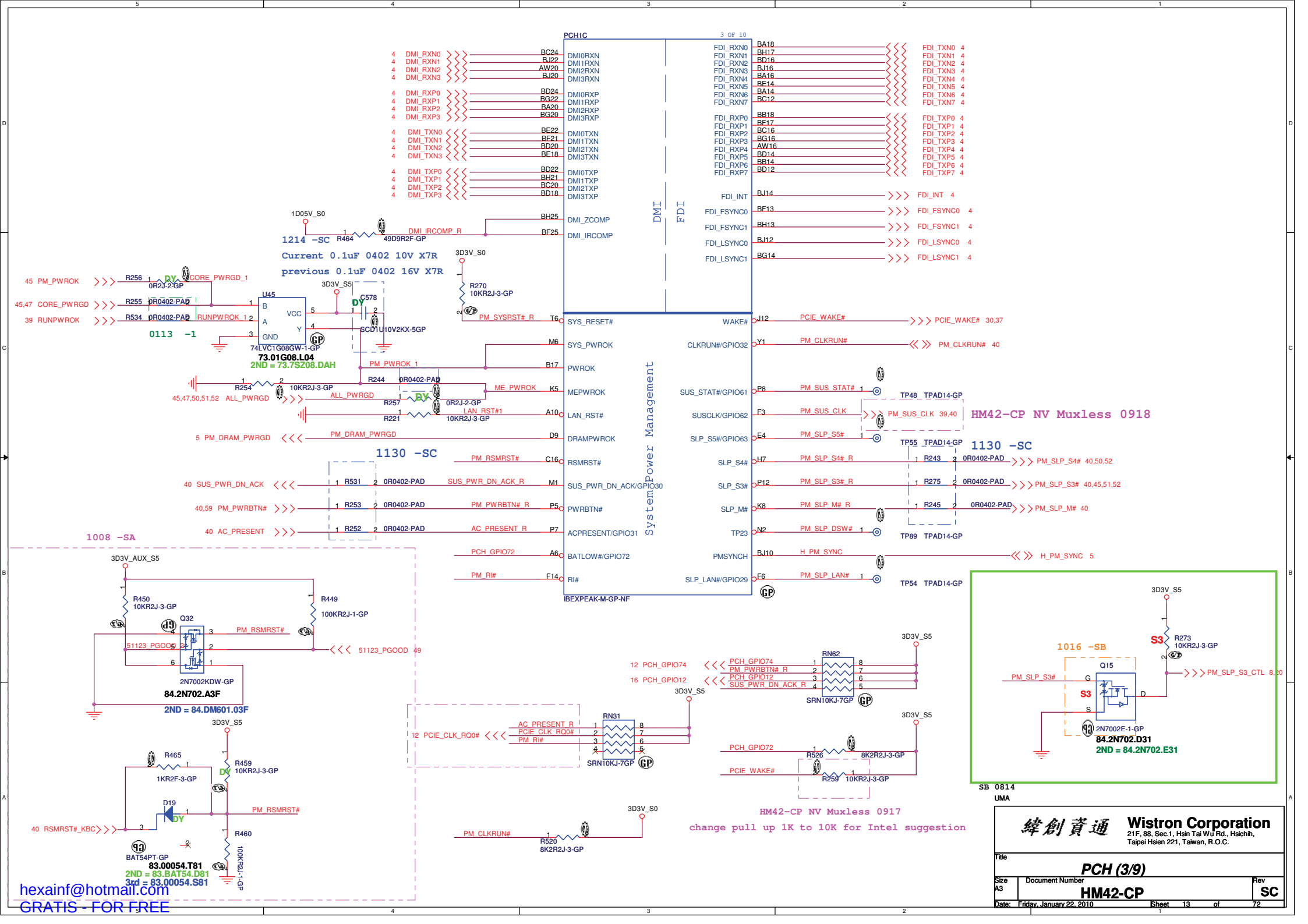

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Title	PCH (3/9)
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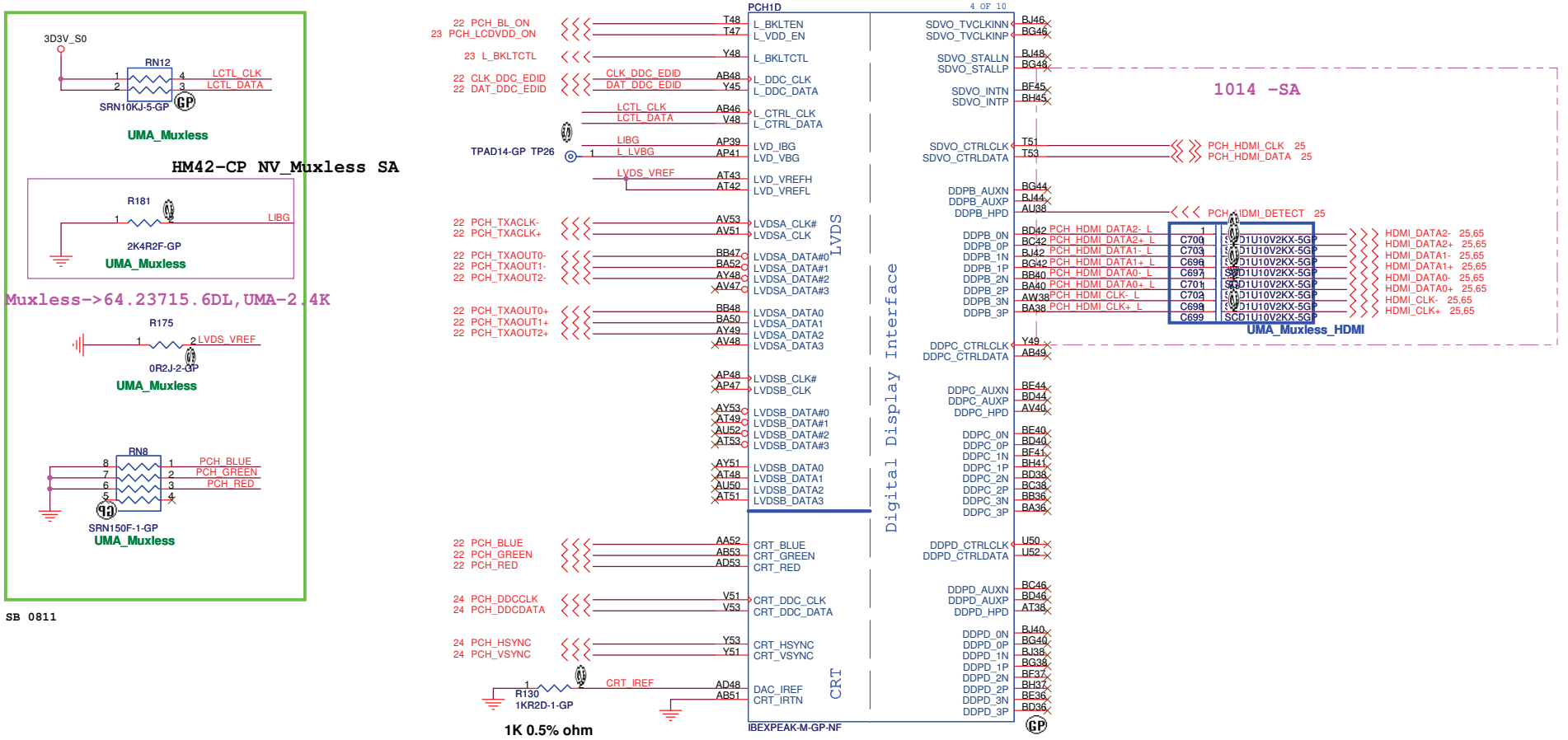

<Core Design>

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Title: PCH (4/9)

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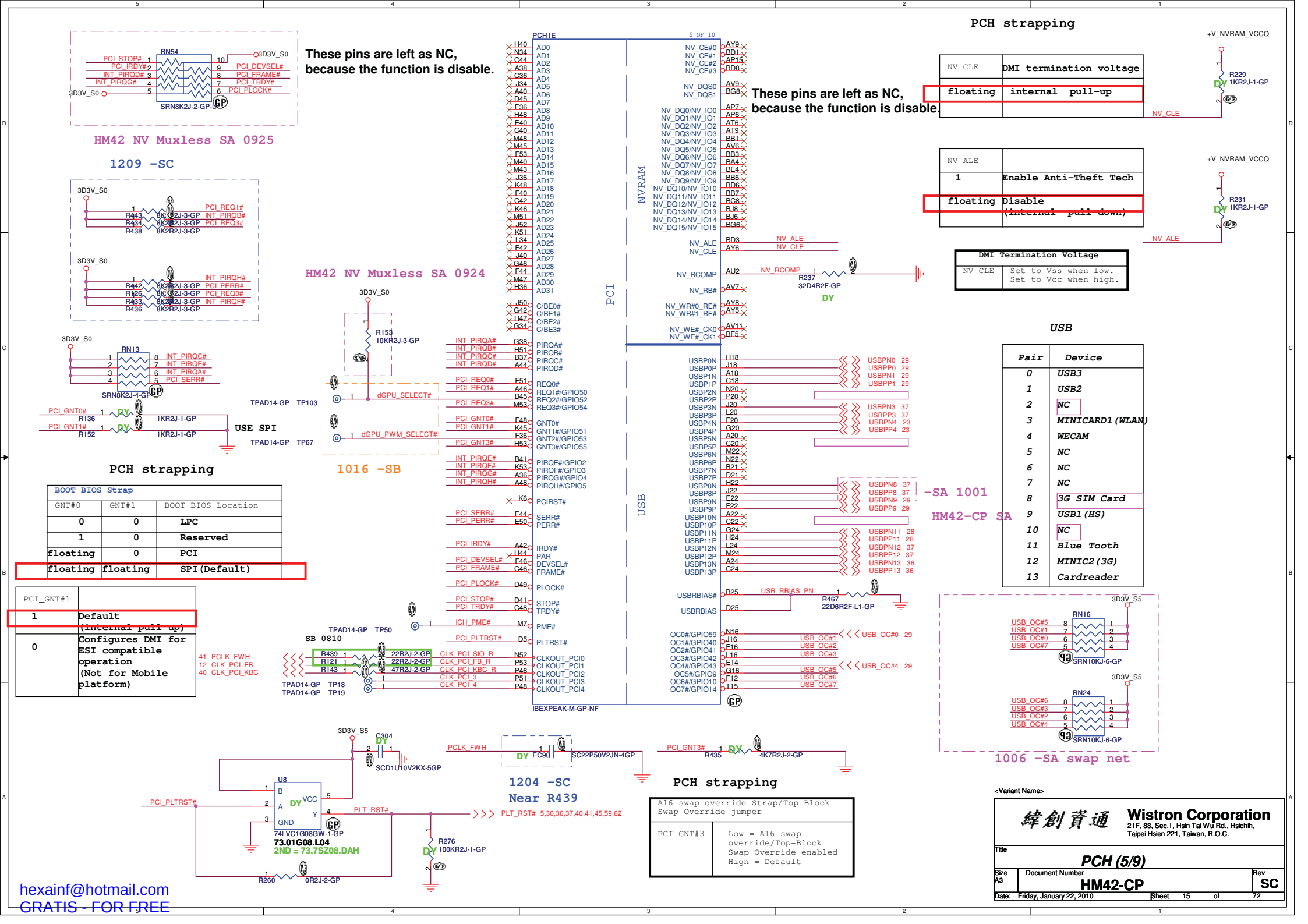
These pins are left as NC, because the function is disable.
HM42 NV Muxless SA 0925
1209 -SC
HM42 NV Muxless SA 0924
1016 -SB
USE SPI
These pins are left as NC, because the function is disable.
PCH strapping
NV_CLE | DMI termination voltage
floating | internal pull-up
NV_ALE
1 | Enable Anti-Theft Tech
floating | Disable (internal pull down)
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
USB
Pair | Device
0 | USB3
1 | USB2
2 | NC
3 | MINICARD1 (WLAN)
4 | WECAM
5 | NC
6 | NC
7 | NC
8 | 3G SIM Card
9 | USB1 (HS)
10 | NC
11 | Blue Tooth
12 | MINIC2 (3G)
13 | Cardreader
-SA 1001
HM42-CP SA
1006 -SA swap net
PCH strapping
BOOT BIOS Strap
GNT#0 | GNT#1 | BOOT BIOS Location
0 | 0 | LPC
1 | 0 | Reserved
floating | 0 | PCI
floating | floating | SPI(Default)
PCI_GNT#1
1 | Default (internal pull up)
0 | Configures DMI for ESI compatible operation (Not for Mobile platform)
1204 -SC
Near R439
PCH strapping
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled
High = Default
PCH1E
IBEXPEAK-M-GP-NF
NVRAM
PCI
USB
SB 0810
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
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PCH (5/9)
HM42-CP
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

HM42-CP_NV _Muxless SA

HM42-CP_NV _Muxless SA

HM42-CP_NV _Muxless SA

SB 0819

SB 0814

SB 0722

SB 0812

1016 -SB

Placed Within 2" from PCH

0121 -1

H: No SG function
L: SG Support

UMA

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Title: PCH (6/9)	
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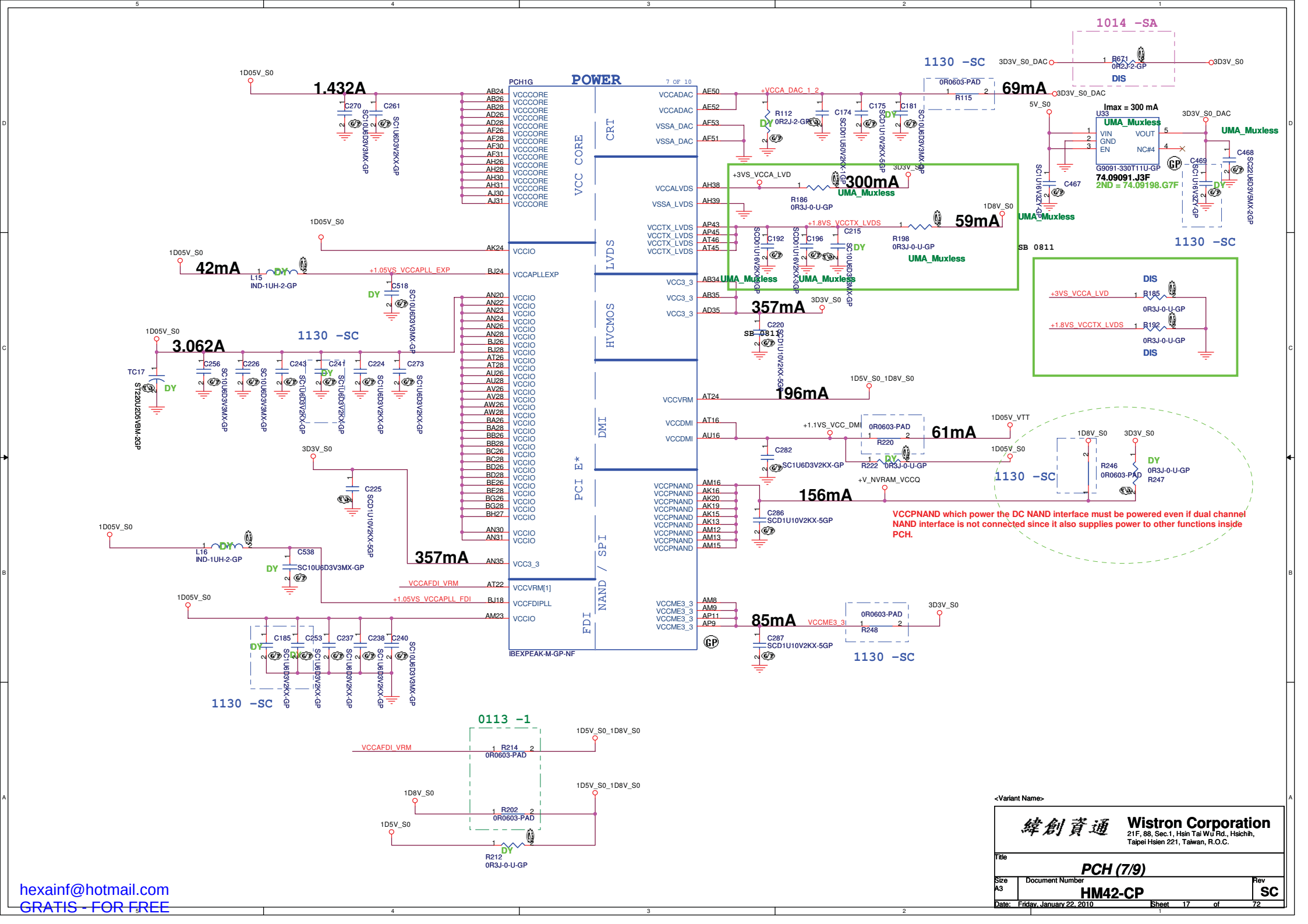
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
1014 -SA
1130 -SC
0113 -1
SB 0811
UMA_Muxless
DY
DIS
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
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PCH (7/9)
HM42-CP
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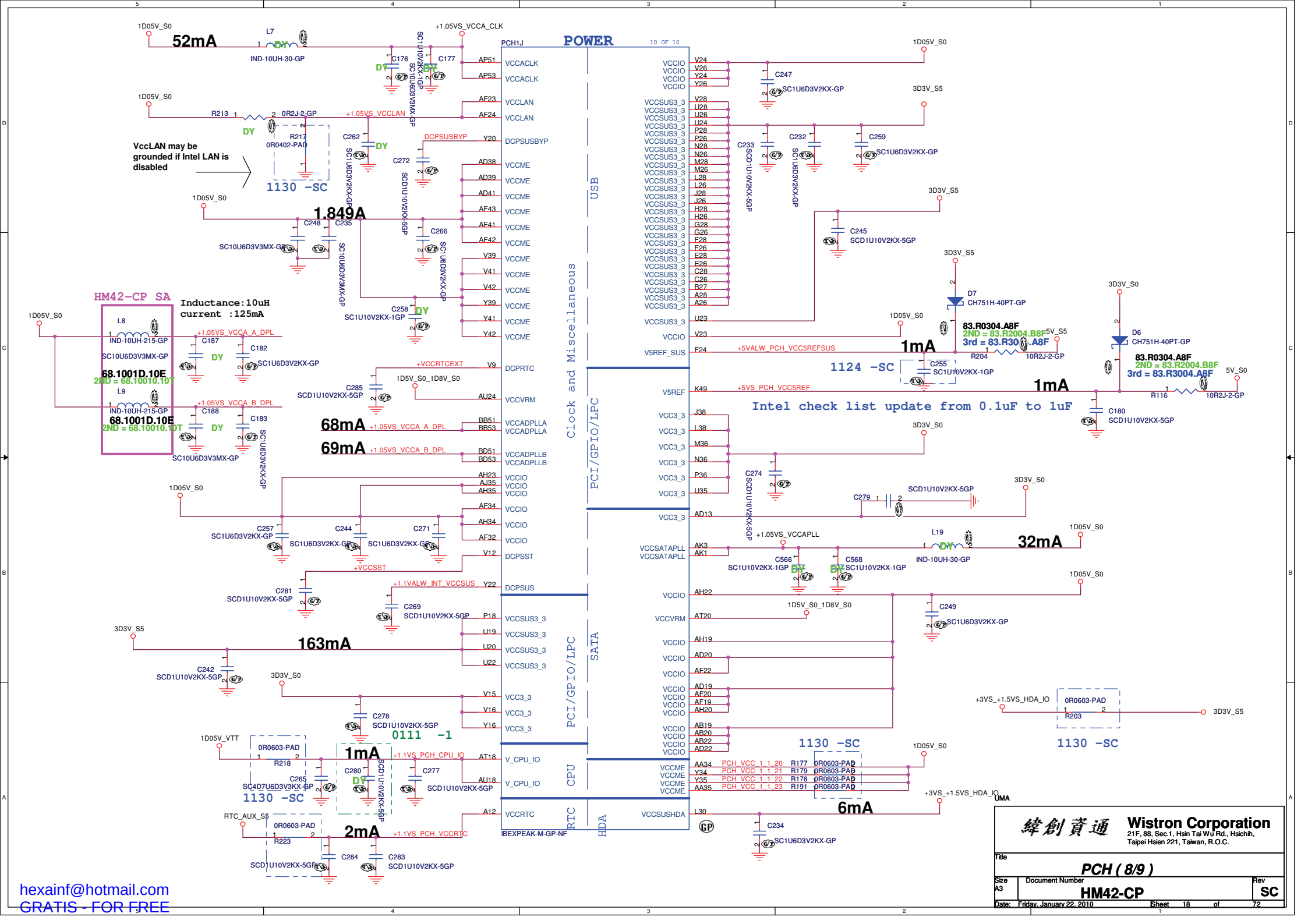
POWER
PCH1J
10 OF 10
HM42-CP SA
Inductance:10uH
current :125mA
VccLAN may be grounded if Intel LAN is disabled
Intel check list update from 0.1uF to 1uF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
32mA
1130 -SC
0111 -1
IBEXPEAK-M-GP-NF
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PCH (8/9)
HM42-CP
SC
Friday, January 22, 2010
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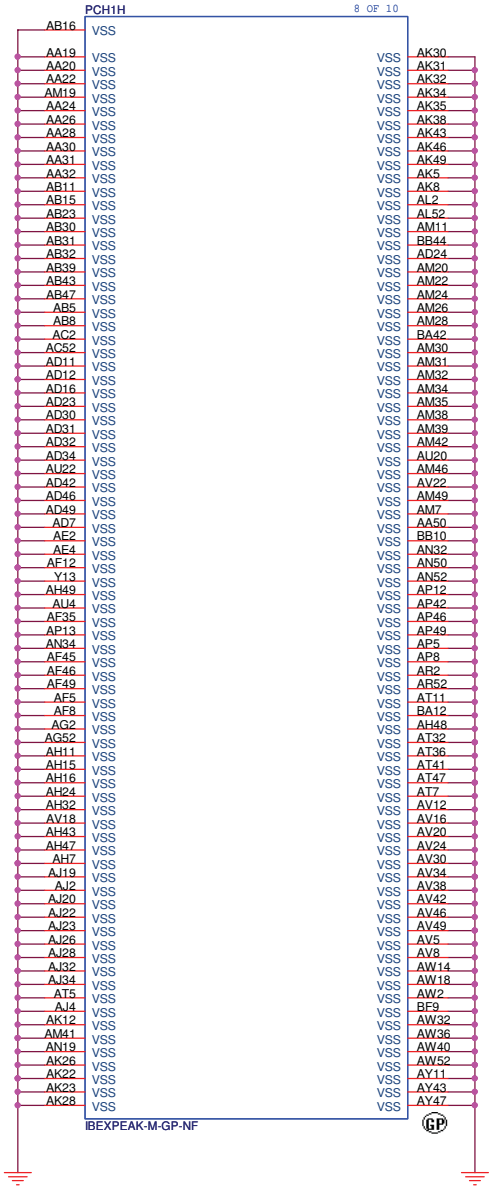

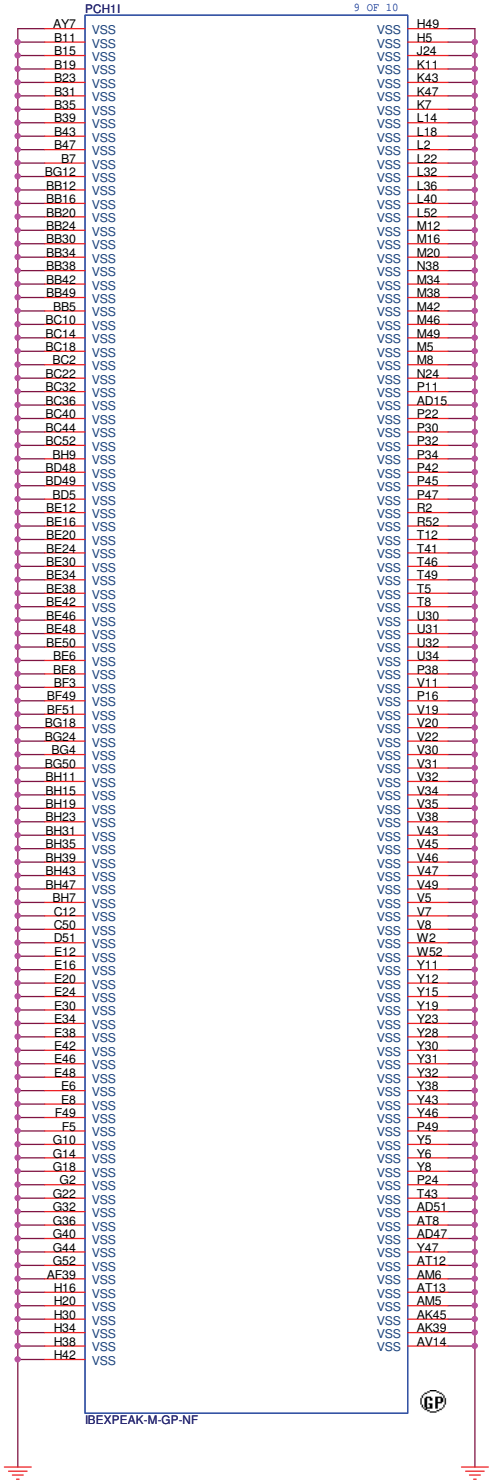

<Variant Name>

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Title: **PCH (9/9)**

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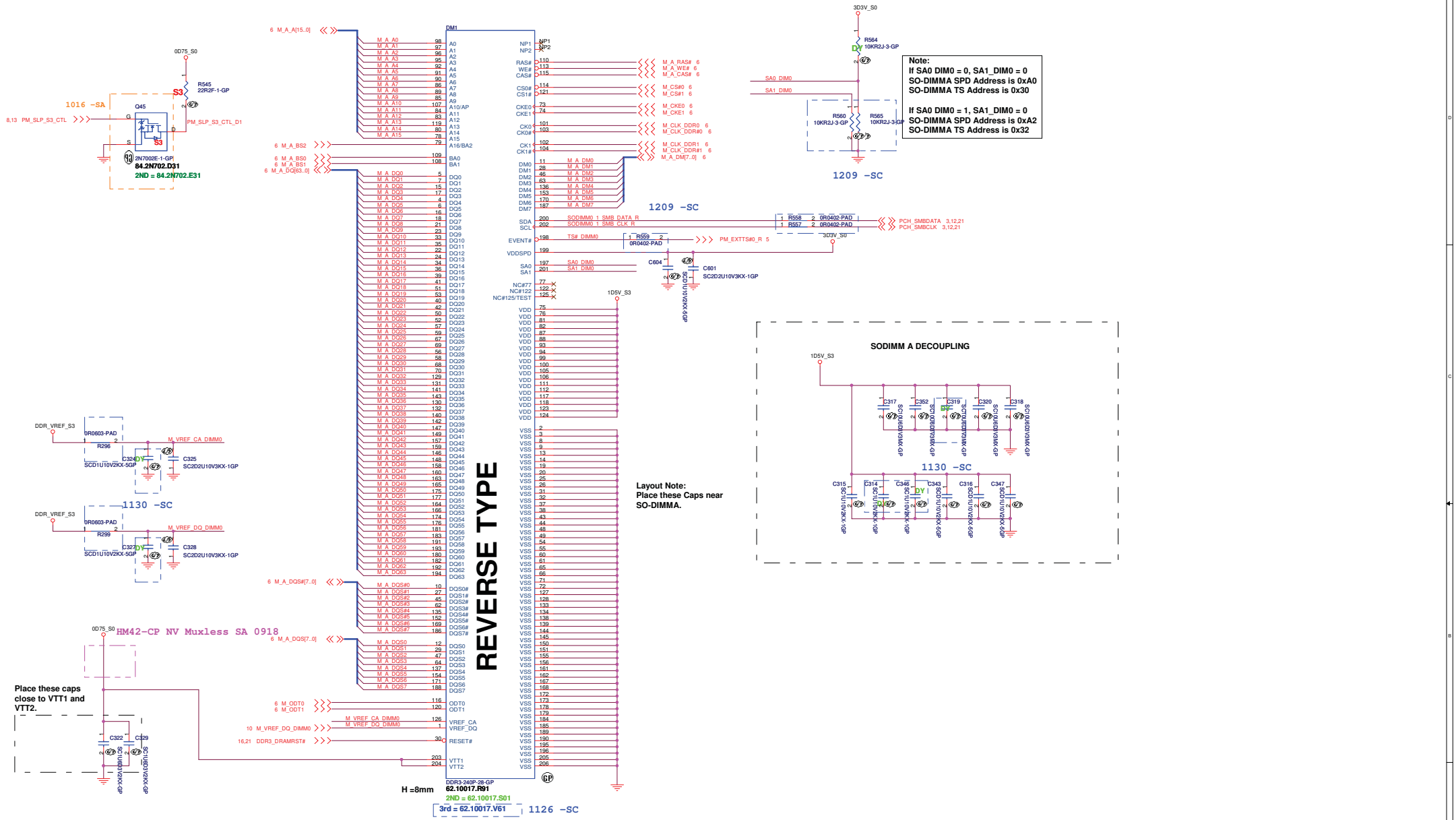

Diserete N11M

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Title: DDRIII Socket DM1

Size	Document Number	Rev
A2	HM42-CP	SC

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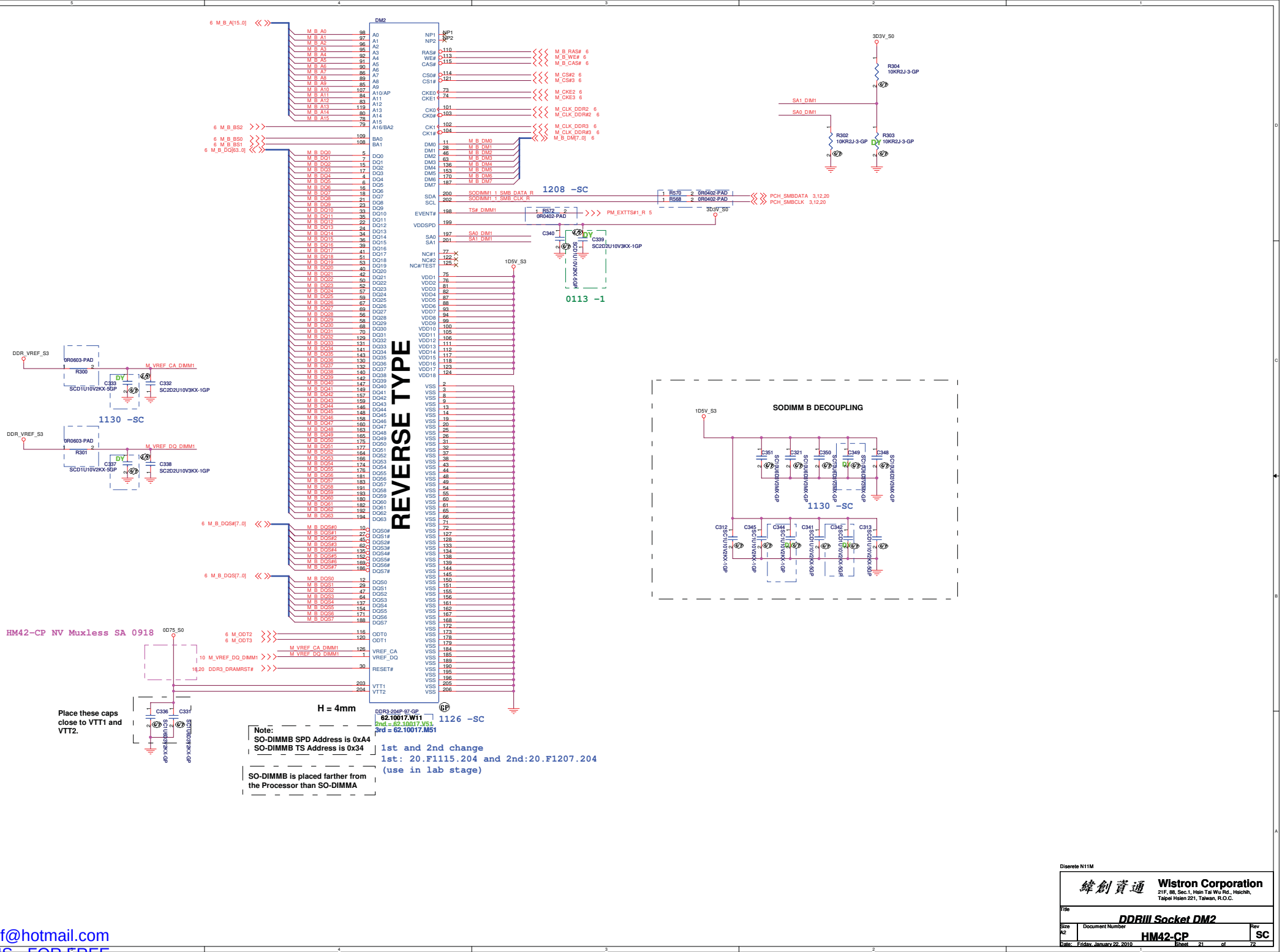
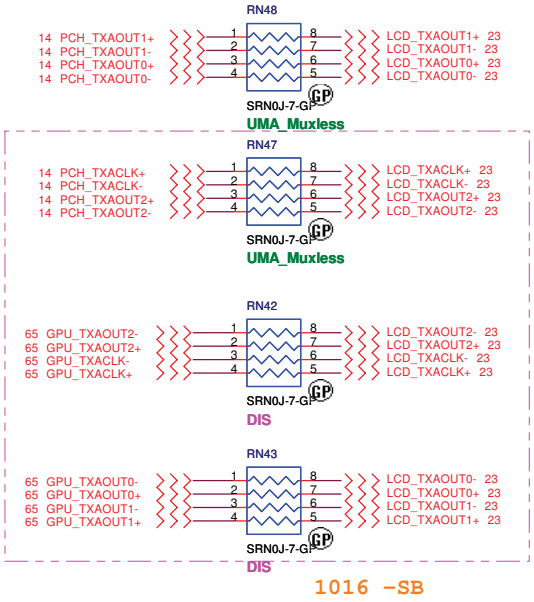
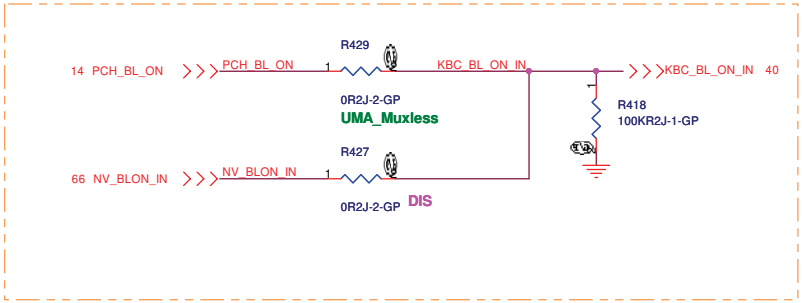
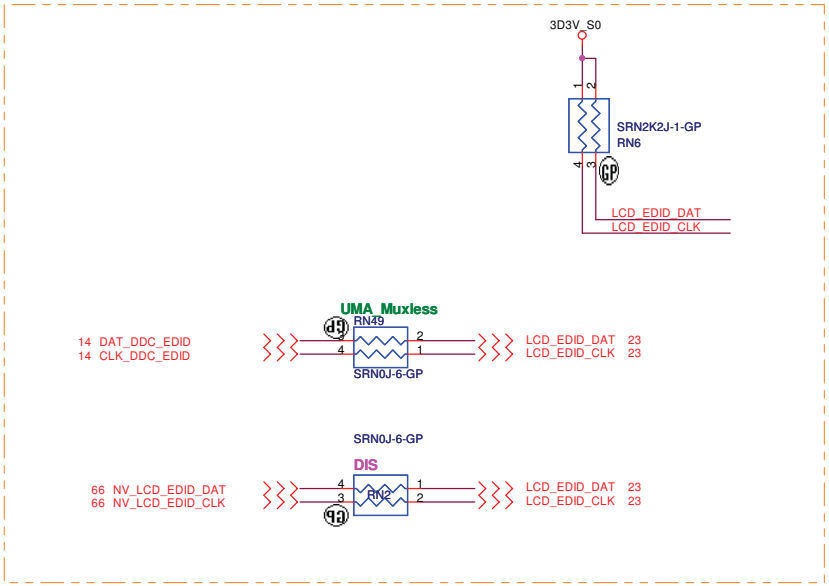


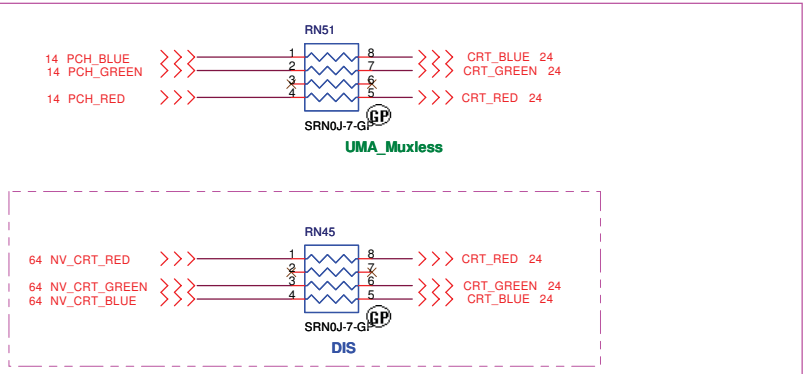


1016 -SB





1016 -SB



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

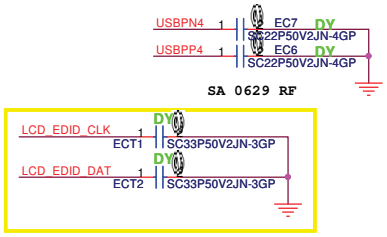
Title: Function

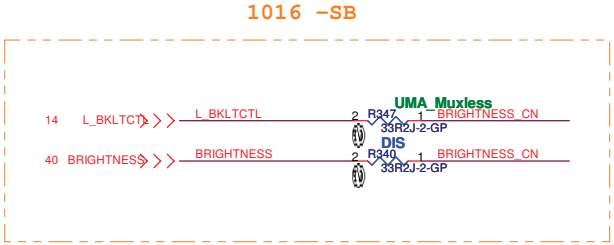
Size	Document Number	Rev
A3	HM42-CP	SC

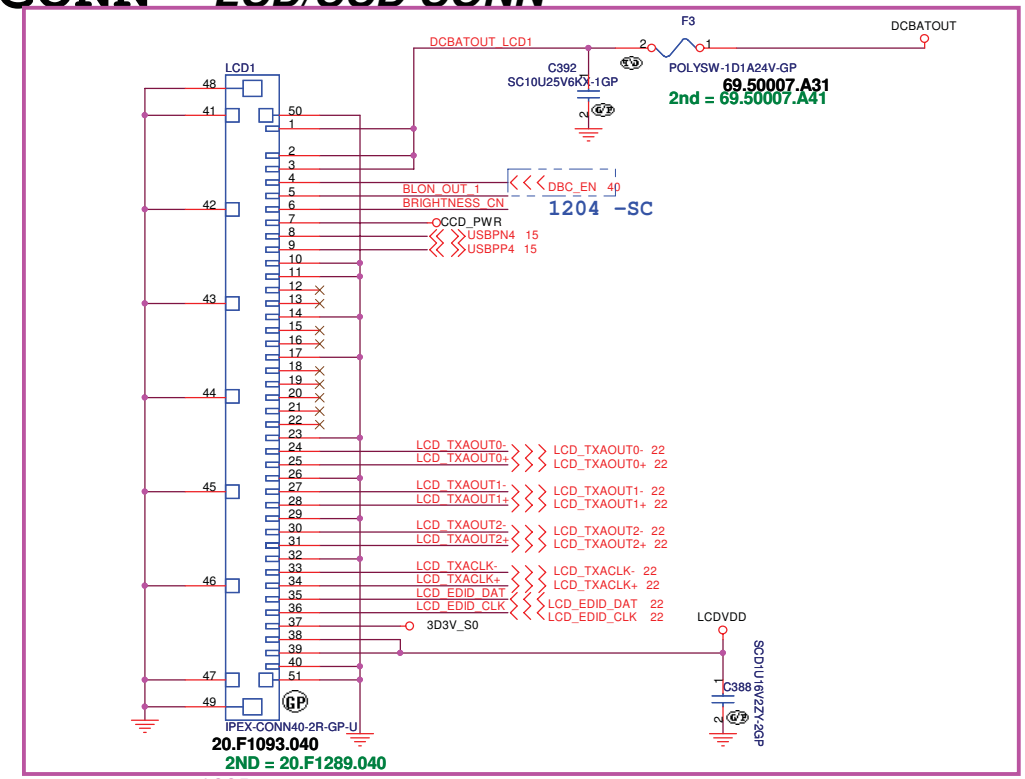
Date: Friday, January 22, 2010 Sheet 22 of 72

LCD/INVERTER/CCD CONN

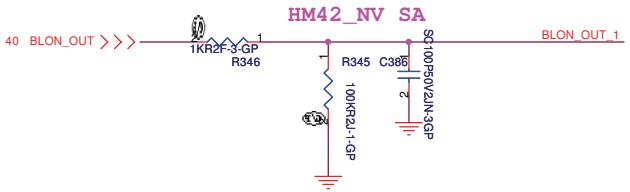
LCD/CCD CONN

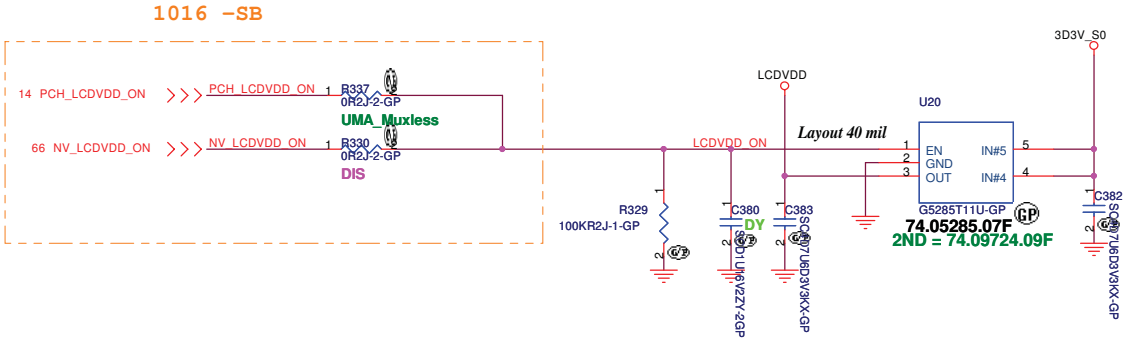




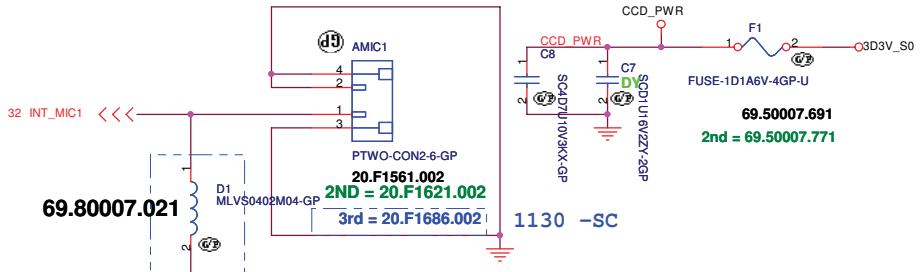


1005 -SA
define same as SJM50-PU,can use SJM50 Cable





Internal Mic



1209 -SC
request by EMI Aaron

Pin 1- >right side
20.F1240.002 Pin1->left side
same as JV70-CP

Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: HM42-CP	Rev: SC
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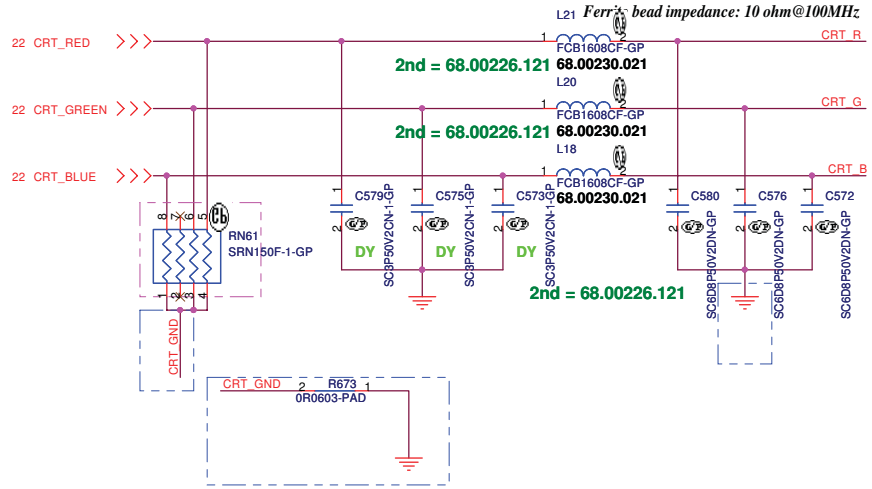
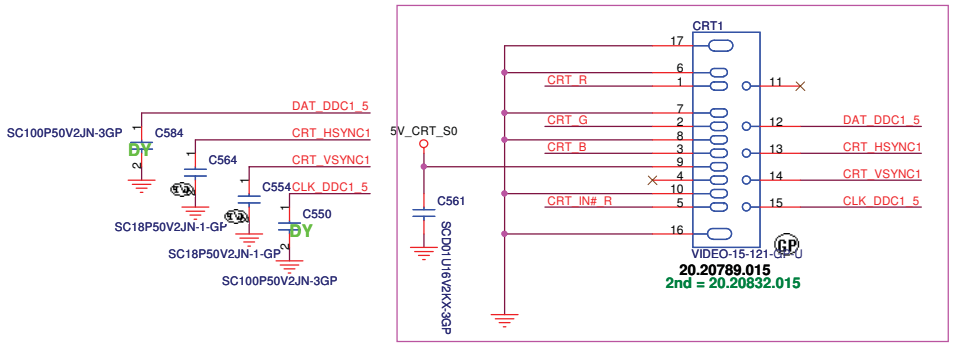
Layout Note:
Place these resistors close to the CRT-out connector

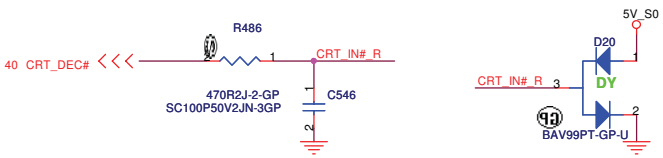


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

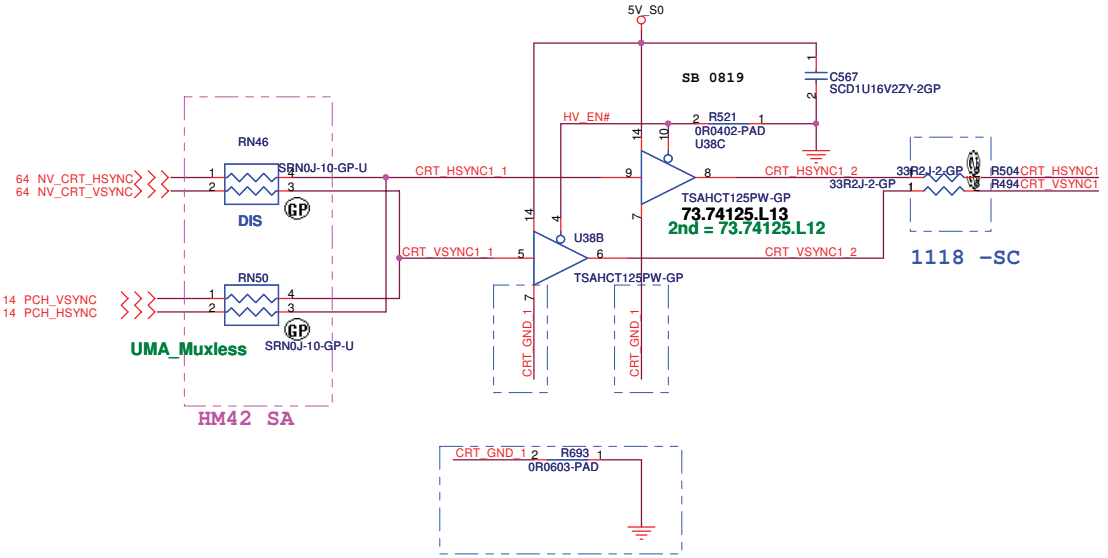
CRT I/F & CONNECTOR



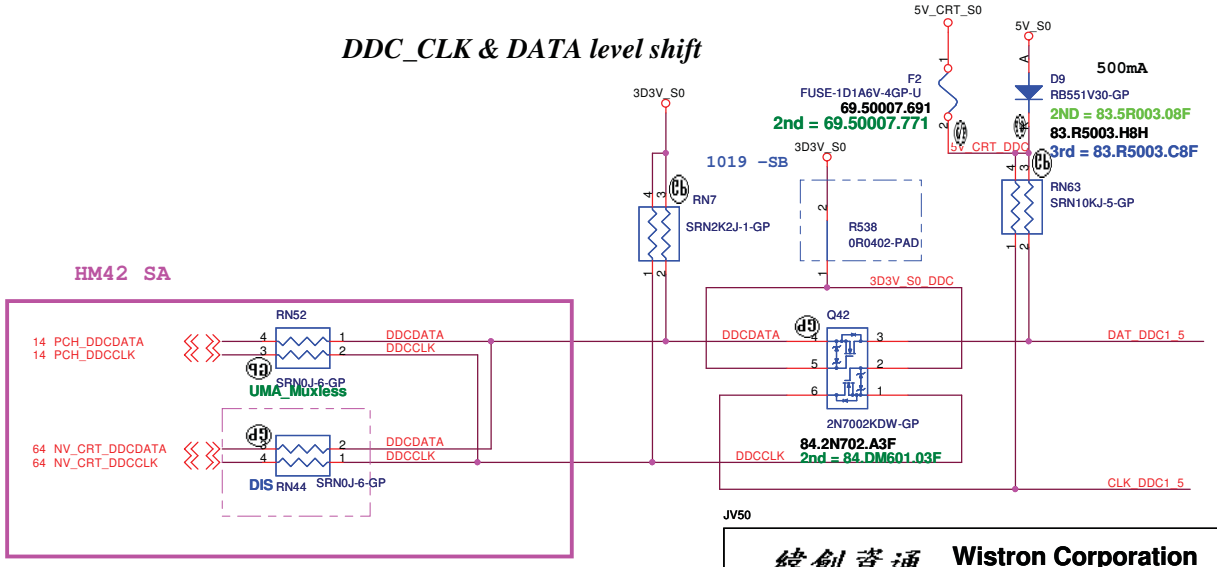
HM42 CP NV Muxless



Hsync & Vsync level shift



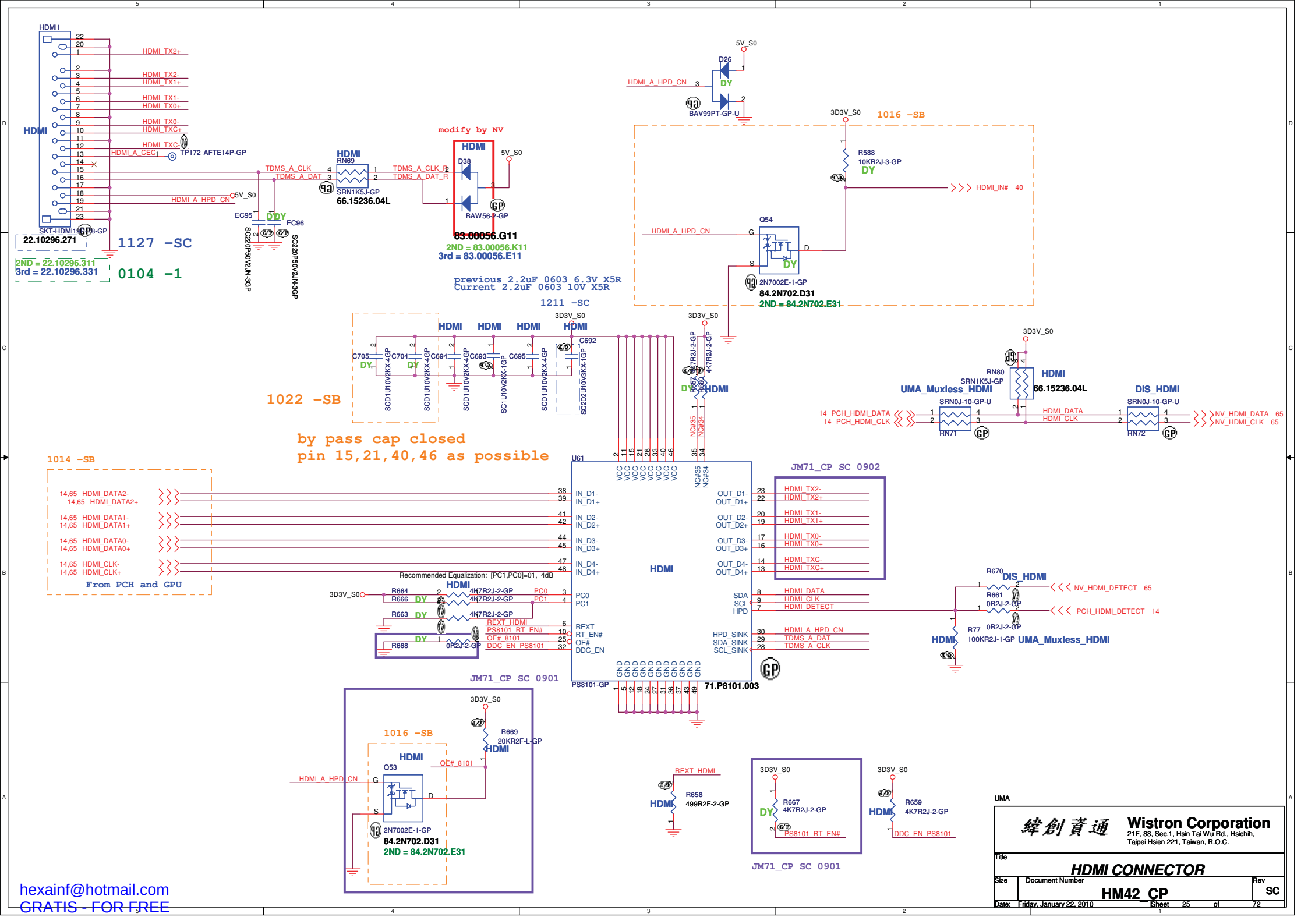
DDC_CLK & DATA level shift



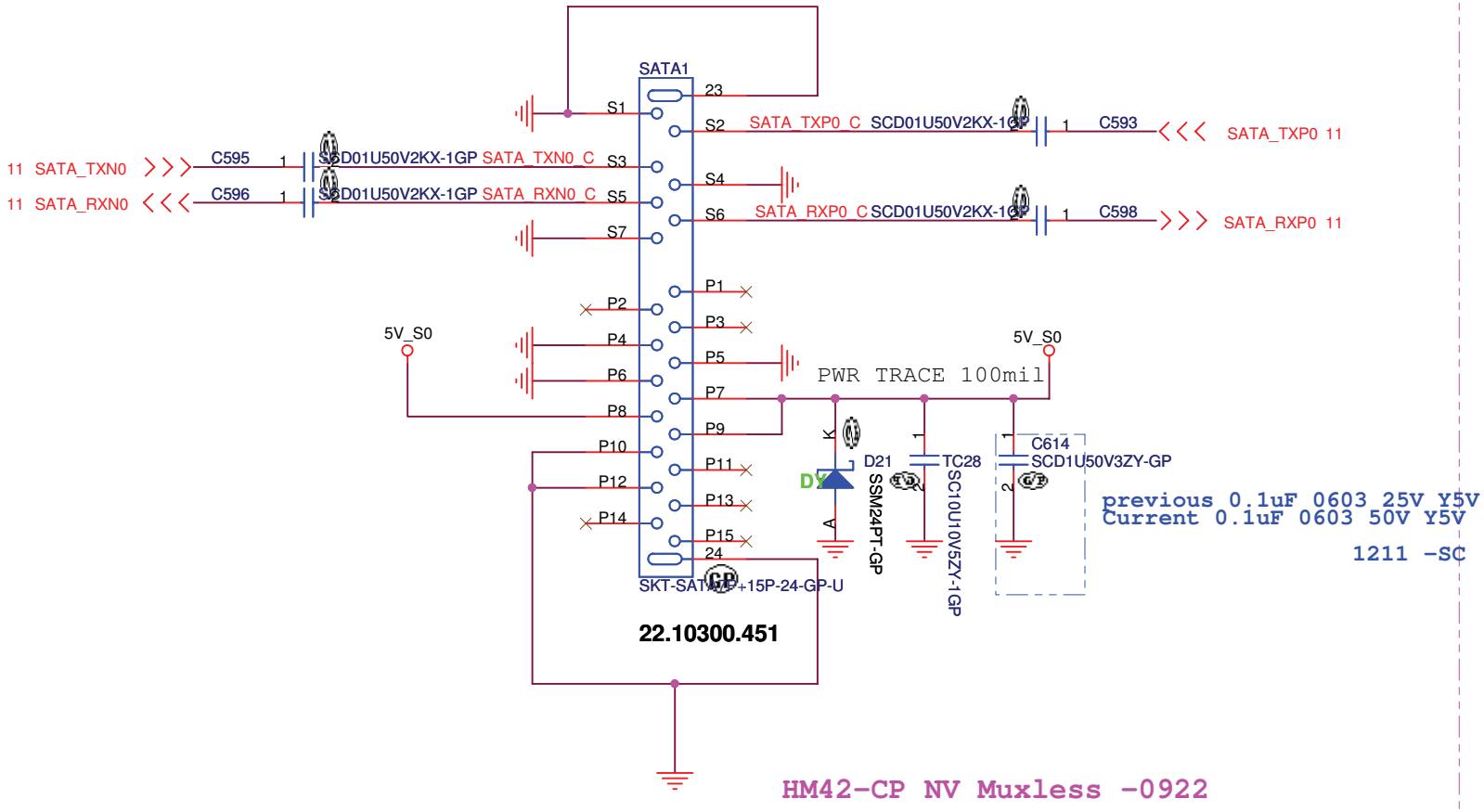
JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT CONN**	
Size	Document Number **HM42-CP**	Rev SC
Date: Friday, January 22, 2010	Sheet 24 of 72	

6 1 7 2 8 3 9 4 10


HDMI1
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP172 AFTE14P-GP
SKT-HDMI19SB-GP
22.10296.271
1127 -SC
2ND = 22.10296.311
3rd = 22.10296.331
0104 -1
HDMI_A_HPD_CN
5V_S0
EC95
EC96
SC220P50V2JN-3GP
TDMS_A_CLK
TDMS_A_DAT
RN69
SRN1K5J-GP
66.15236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
modify by NV
D38
BAW56-2-GP
83.00056.G11
2ND = 83.00056.K11
3rd = 83.00056.E11
D26
BAV99PT-GP-U
1016 -SB
R588
10KR2J-3-GP
HDMI_IN# 40
Q54
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
previous 2.2uF 0603 6.3V X5R
Current 2.2uF 0603 10V X5R
1211 -SC
1022 -SB
C705
C704
C694
C693
C695
C692
SCD1U10V2KX-4GP
SC1U10V2KX-1GP
SC2D2U10V3KX-1GP
R667
R668
4K7R2J-2-GP
by pass cap closed
pin 15,21,40,46 as possible
RN80
SRN1K5J-GP
66.15236.04L
UMA_Muxless_HDMI
DIS_HDMI
SRN0J-10-GP-U
RN71
RN72
14 PCH_HDMI_DATA
14 PCH_HDMI_CLK
HDMI_DATA
HDMI_CLK
NV_HDMI_DATA 65
NV_HDMI_CLK 65
1014 -SB
14,65 HDMI_DATA2-
14,65 HDMI_DATA2+
14,65 HDMI_DATA1-
14,65 HDMI_DATA1+
14,65 HDMI_DATA0-
14,65 HDMI_DATA0+
14,65 HDMI_CLK-
14,65 HDMI_CLK+
From PCH and GPU
U61
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
HDMI_TX2-
HDMI_TX2+
HDMI_TX1-
HDMI_TX1+
HDMI_TX0-
HDMI_TX0+
HDMI_TXC-
HDMI_TXC+
JM71_CP SC 0902
Recommended Equalization: [PC1,PC0]=01, 4dB
R664
R666
R663
R668
0R2J-2-GP
PC0
PC1
REXT_HDMI
PS8101_RT_EN#
OE#_8101
DDC_EN_PS8101
REXT
RT_EN#
OE#
DDC_EN
SDA
SCL
HPD
HDMI_DATA
HDMI_CLK
HDMI_DETECT
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
PS8101-GP
71.P8101.003
JM71_CP SC 0901
R670
R661
R77
100KR2J-1-GP
NV_HDMI_DETECT 65
PCH_HDMI_DETECT 14
1016 -SB
R669
20KR2F-L-GP
Q53
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
R658
499R2F-2-GP
R667
4K7R2J-2-GP
R659
4K7R2J-2-GP
JM71_CP SC 0901
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size
Document Number
HM42_CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 25 of 72
hexainf@hotmail.com
GRATIS - FOR FREE

SATA Connector



hexainf@hotmail.com
GRATIS - FOR FREE

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **HM42-CP**	Rev SC
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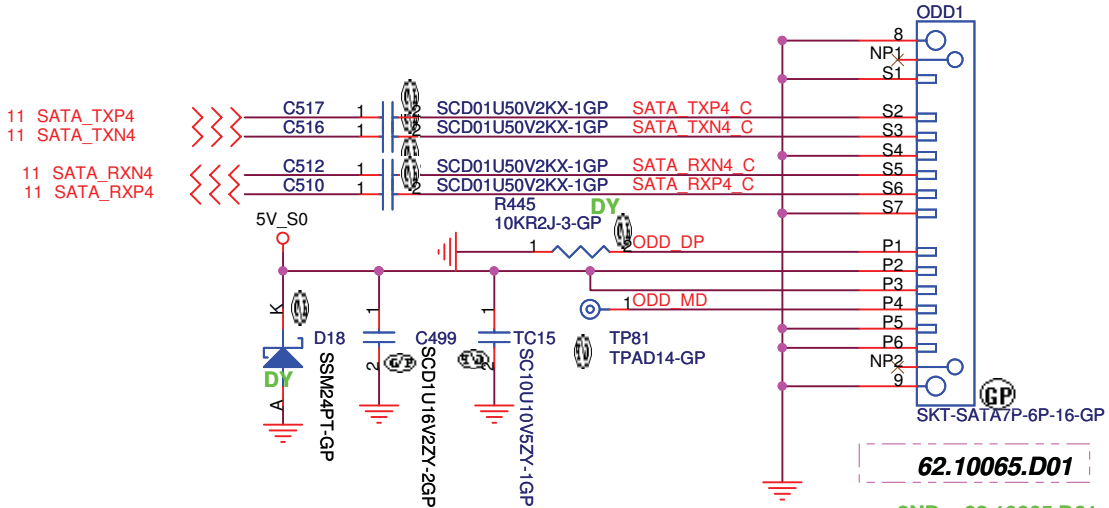
ODD Connector



UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ODD***

Size	Document Number	Rev
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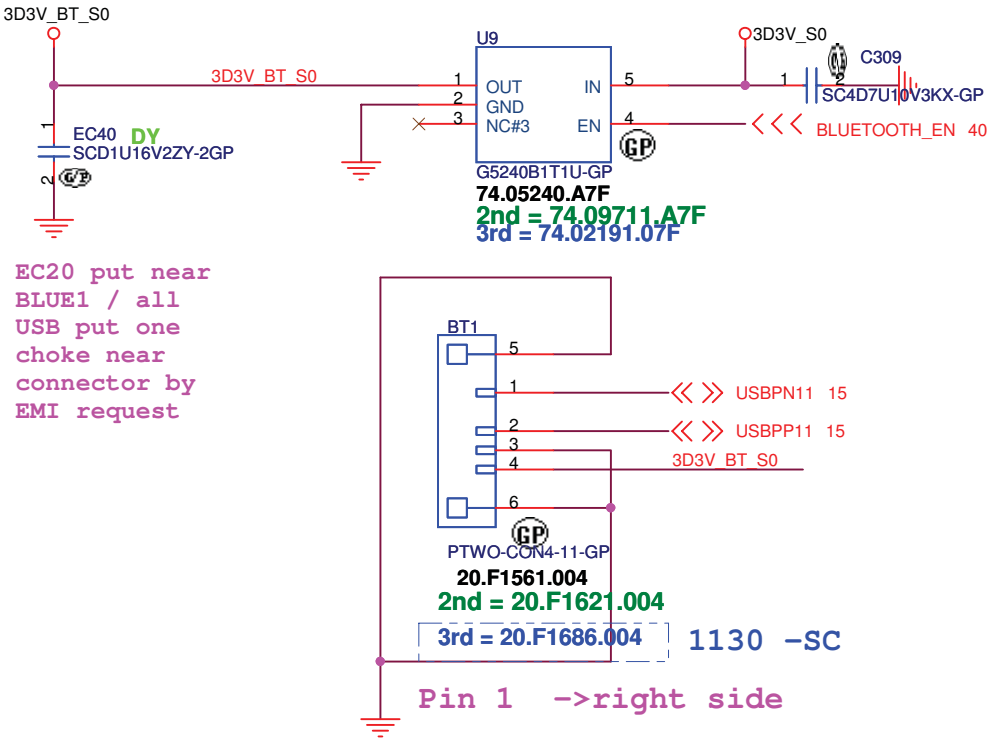
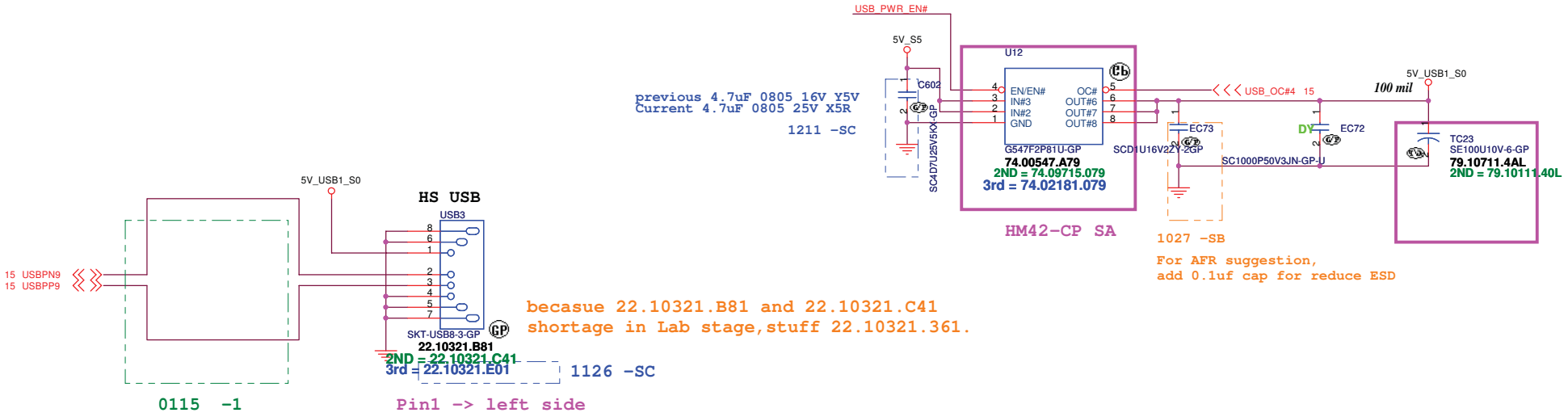
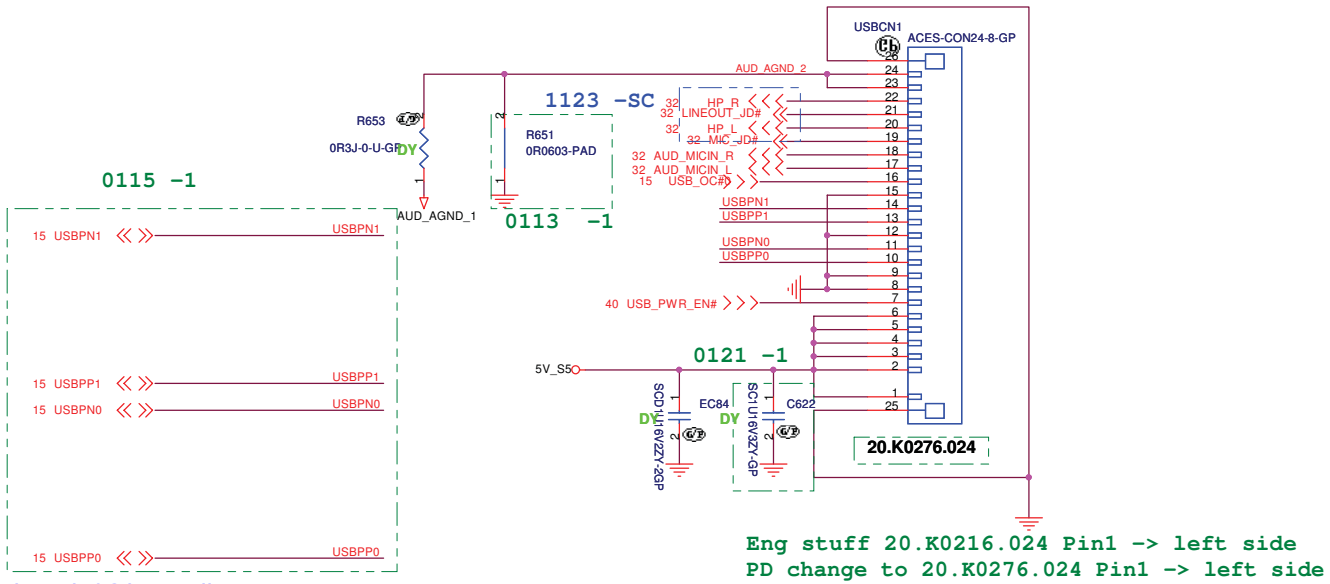
BLUETOOTH MODULE



JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 28 of 72	





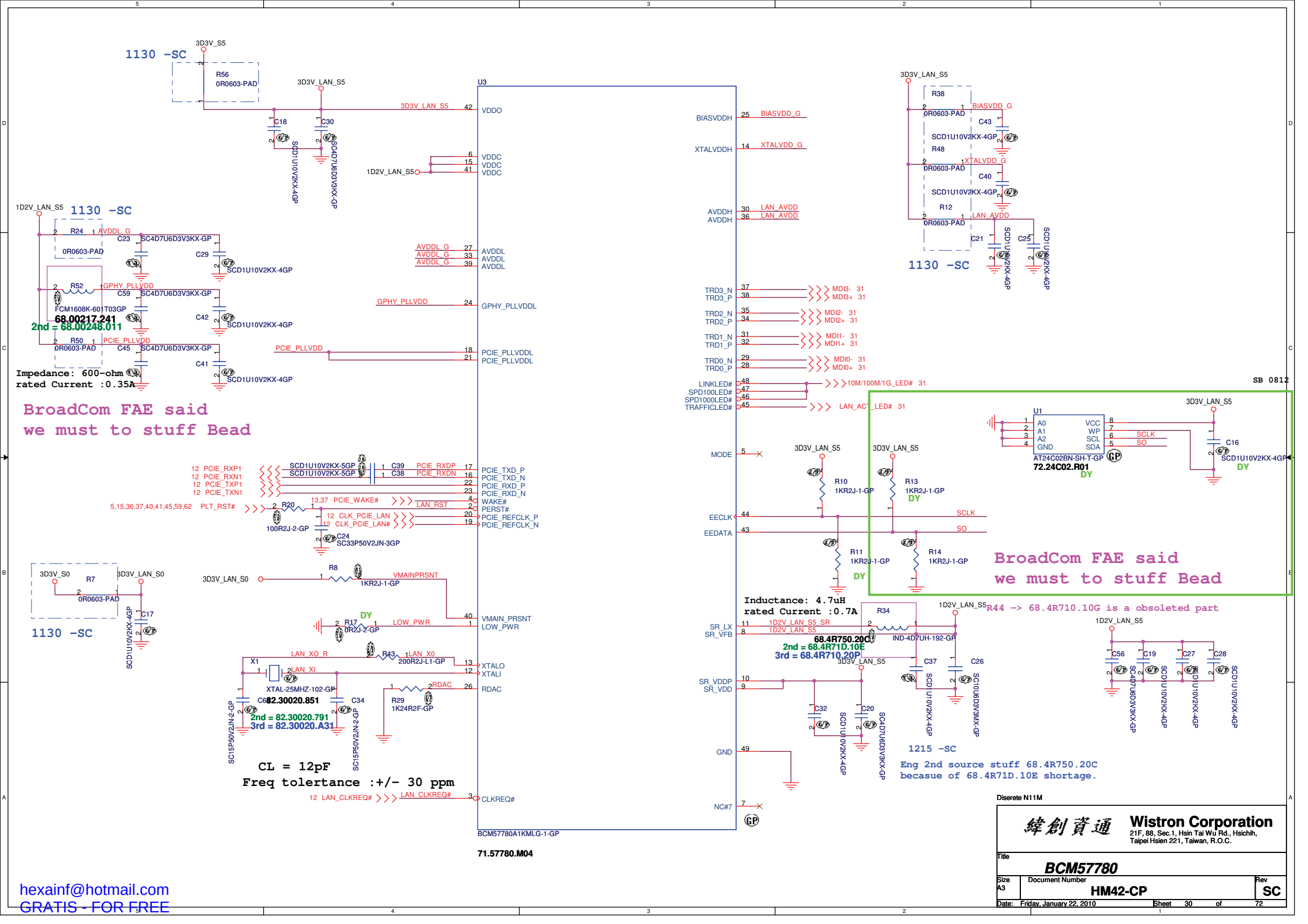
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB and Audio CONN*

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 29 of 72



Diserete N11M

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***BCM57780***		
Size: A3	Document Number: **HM42-CP**	Rev: **SC**
Date: Friday, January 22, 2010	Sheet 30 of 72	

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

GIGA Lan Transformer

XF2

30 MDI1+ 1 12 RJ45_3
XRF_TDC1 3 10 MCT2
30 MDI1- 2 11 RJ45_6
30 MDI0- 5 8 RJ45_2
XRF_TDC2 4 9 MCT1
30 MDI0+ 6 7 RJ45_1

XFORM-276-GP-U
68.68160.30B
2ND = 68.HD081.30B
3rd = 68.0NS14.301

C14 DY SCD1U10V2KX-4GP
C15 DY SCD1U10V2KX-4GP

XF1

30 MDI3+ 1 12 RJ45_7
XRF_TDC3 3 10 MCT4
30 MDI3- 2 11 RJ45_8
30 MDI2- 5 8 RJ45_5
XRF_TDC4 4 9 MCT3
30 MDI2+ 6 7 RJ45_4

XFORM-276-GP-U
68.68160.30B
2ND = 68.HD081.30B
3rd = 68.0NS14.301

C12 DY SCD1U10V2KX-4GP
C13 DY SCD1U10V2KX-4GP

LAN_ACT_LED#
10M/100M/1G_LED#
C368 SC1KP50V2KX-1GP DY
C389 SC1KP50V2KX-1GP DY

RJ45

30 10M/100M/1G_LED#
CONN_PWR
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
CONN_PWR2
30 LAN_ACT_LED#

RJ45-13P-5-GP

22.10177.C01
2ND = 22.10177.B51
3rd = 22.10177.C21
4th = 22.10177.B81
5th = 22.10177.H31

2 LED LAYOUT

13 12

NODE	COLOR
12(+)	13(-) YELLOW

3 LED LAYOUT

11 9
ORANGE GREEN
10

NODE	COLOR
9(-)	10(+) GREEN
11(-)	10(+) ORANGE

3D3V_S5
RN36 SRN470J-4-GP-U
CONN_PWR2
CONN_PWR

SB 1208

EC52 SC100P50V2JN-3GP
EC53 DY SC100P50V2JN-3GP

HM42 CP NV Muxless SA

MCT1
MCT2
MCT3
MCT4
RN39 SRN75J-1-GP
MCT_R
C385 SC1KP2KV6KX-GP

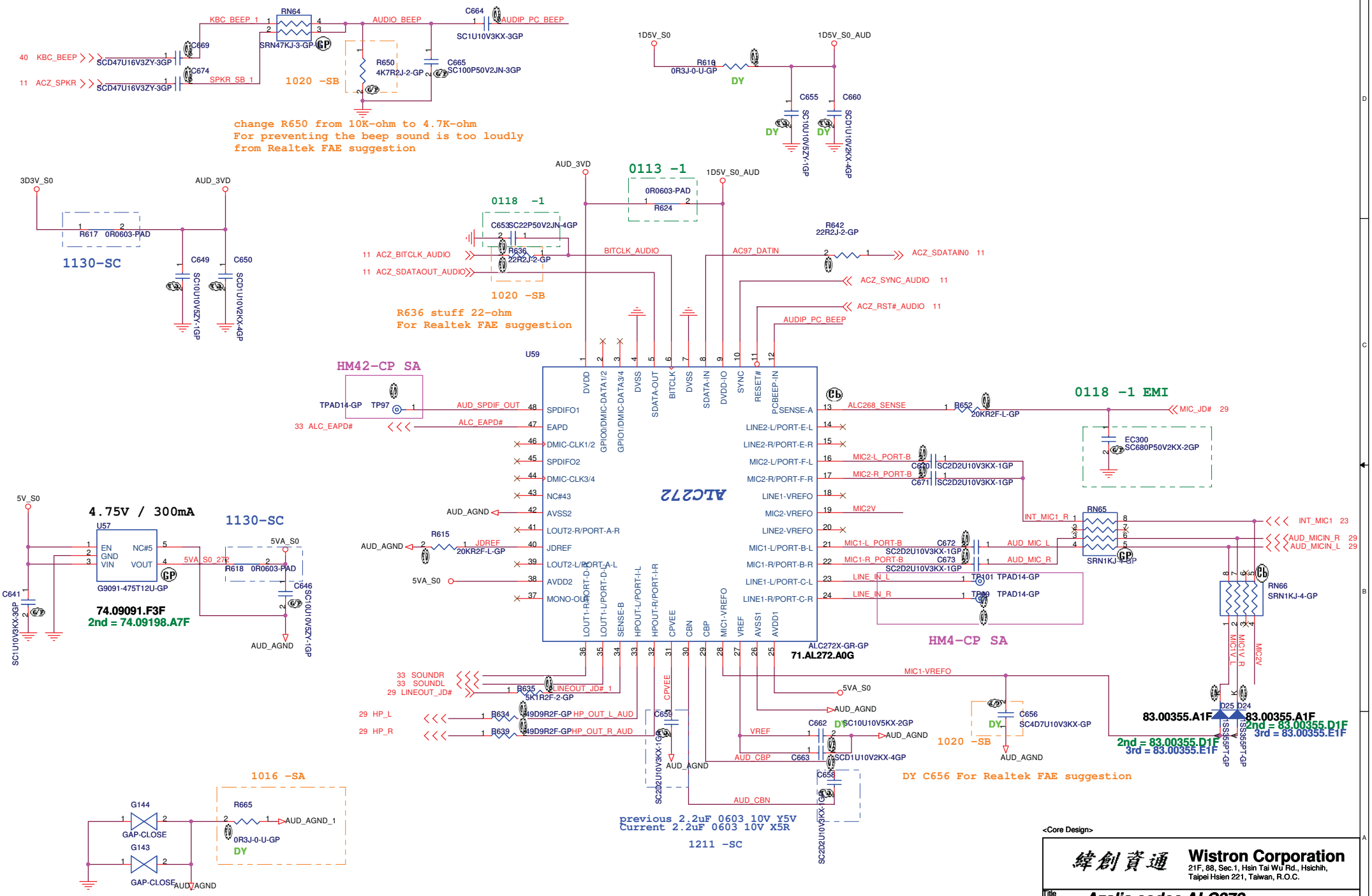
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 31 of 72



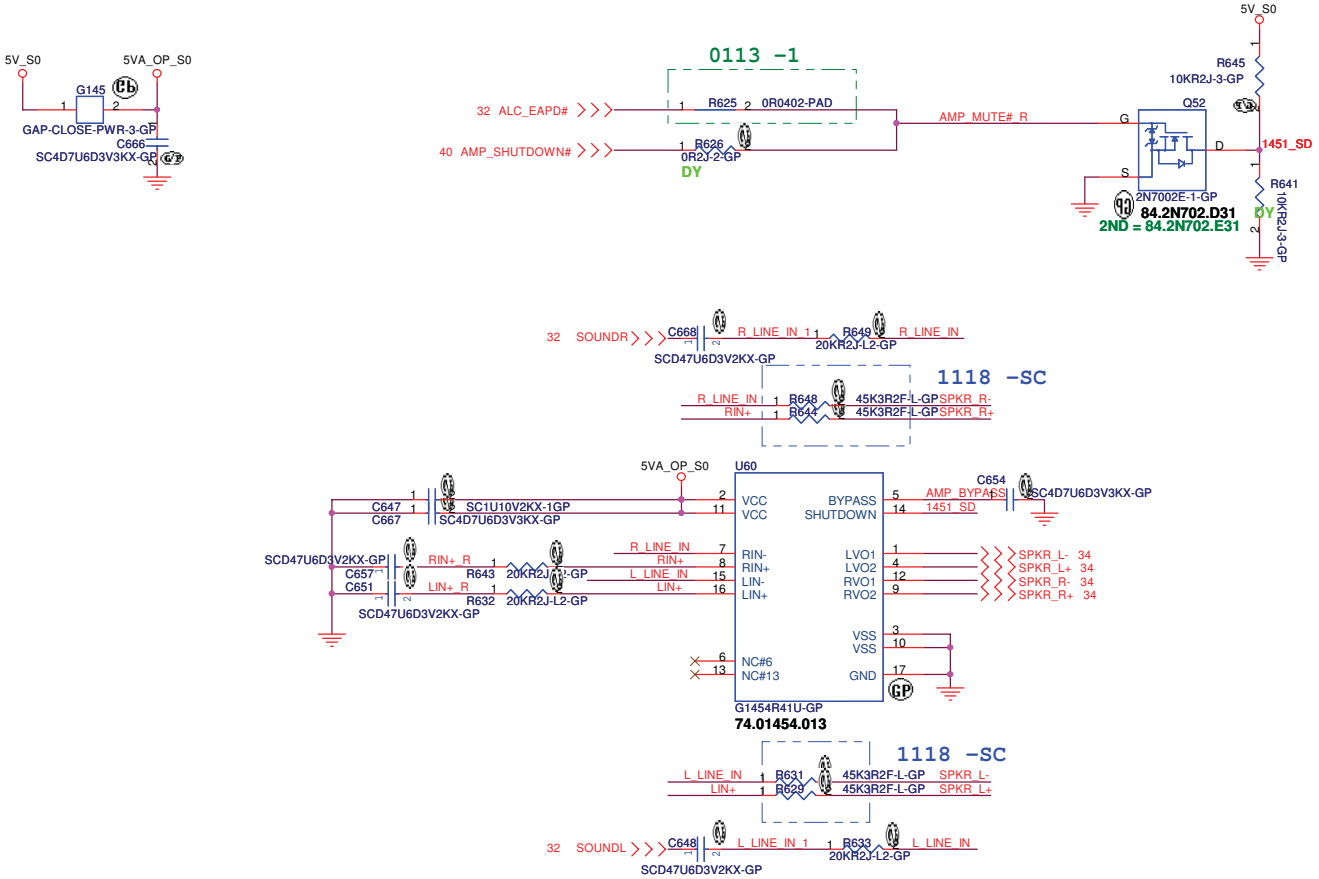
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC272

Size: A3 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 32 of 72




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.446^2/4=1.5W
```

UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

Size	Document Number	Rev
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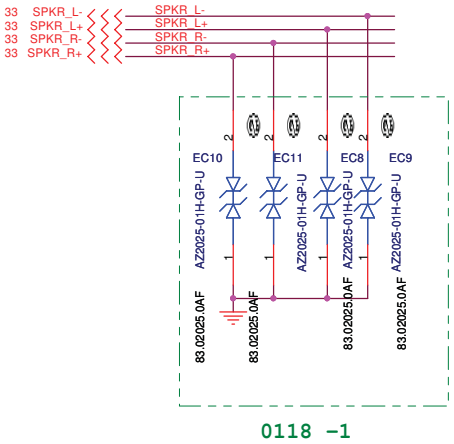
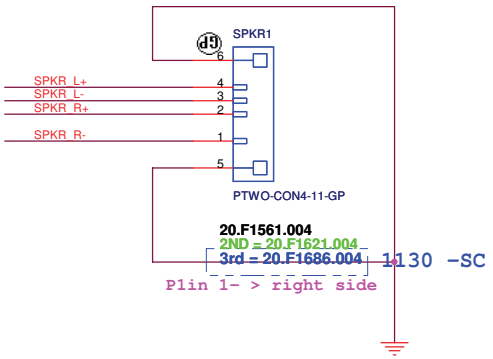
Internal Speaker





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO SPEARK*		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 34 of 72	

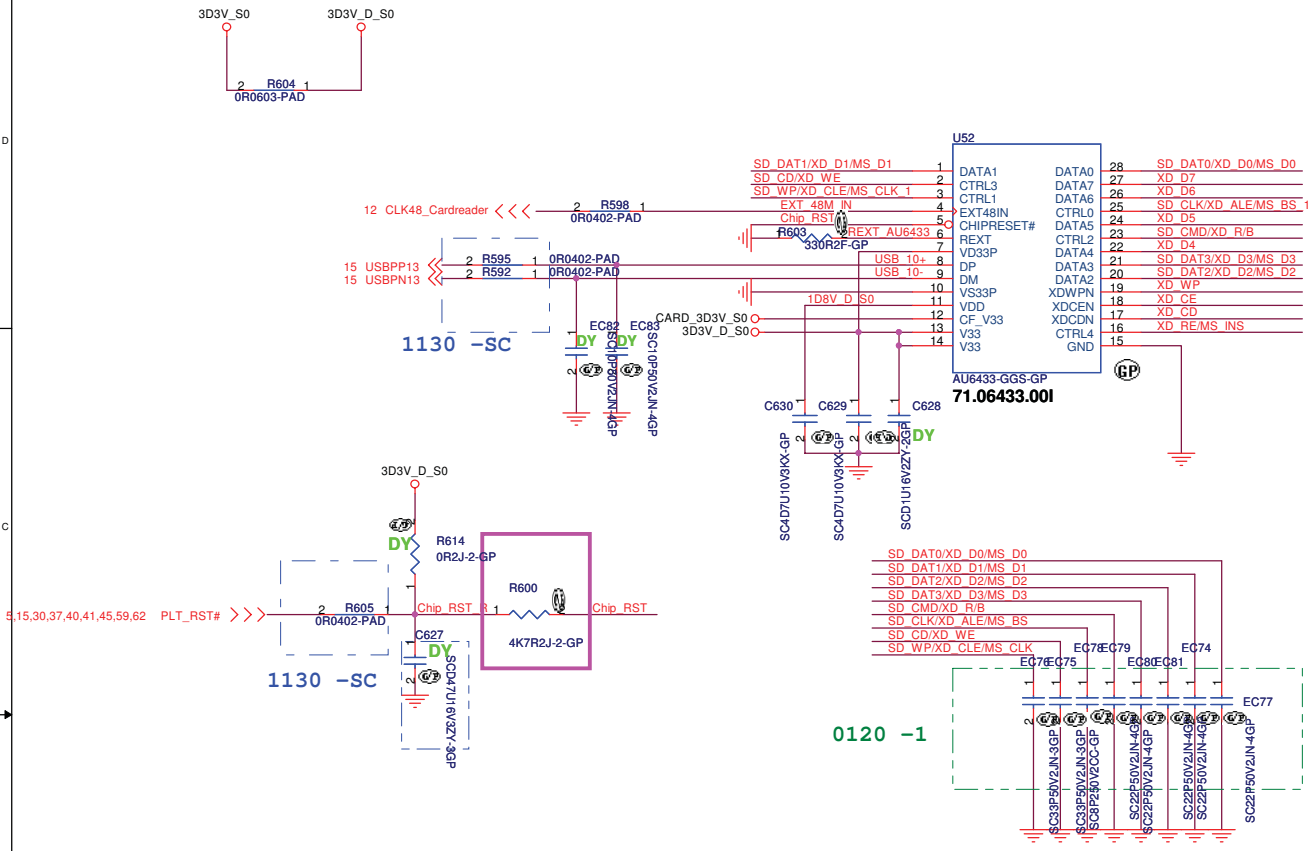
JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Resrve_MDC

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 35 of 72

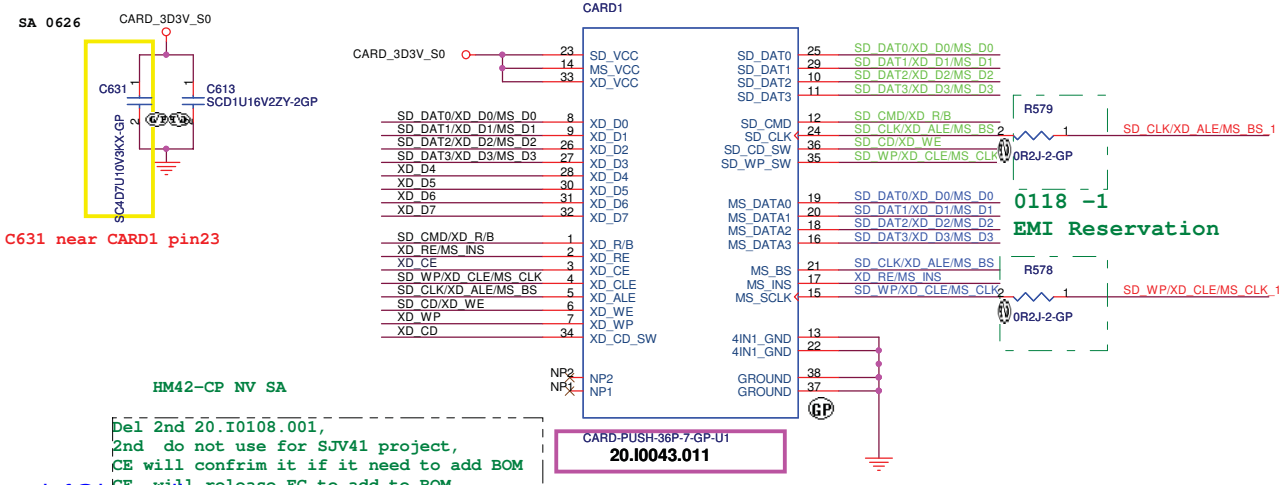


Pin	SD Mode	
	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1 xD-R/B			2P
P2 xD-RE			3P
P3 xD-CE			4P
P4 xD-CLE			5P
P5 xD-ALE			6P
P6 xD-WE			7P
P7 xD-WP			8P
P8 xD-D0			10P
P9 xD-D1			11P
P10 SD-DAT2	9P		
P11 SD-DAT3	1P		
P12 SD-CMD	2P		
P13 4in1-GND	3P/6P	1P/10P	1P/9P
P14 MS-VCC		9P	
P15 MS-SCLK		8P	
P16 MS-DATA3		7P	
P17 MS-INS		6P	
P18 MS-DATA2		5P	
P19 MS-DATA0		4P	

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2,7V - 3,6V)
10	VSS	Vss

Del 2nd 20.I0108.001,
2nd do not use for SJV41 project,
CE will confrim it if it need to add BOM
CE will release EC to add to BOM

UMA

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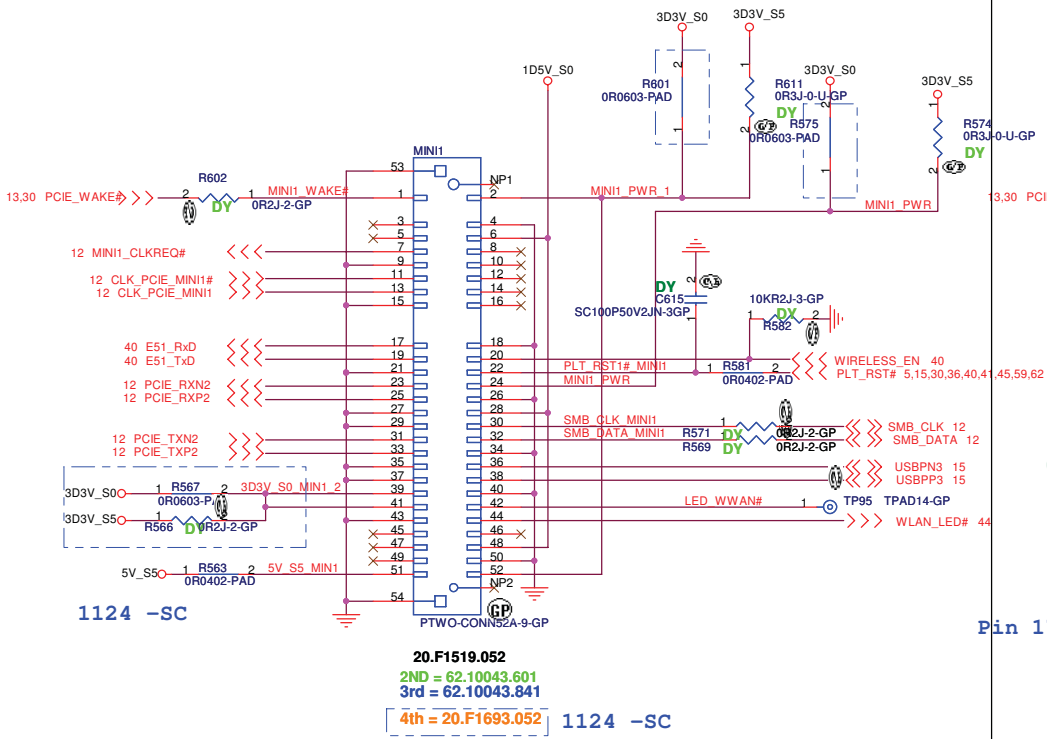
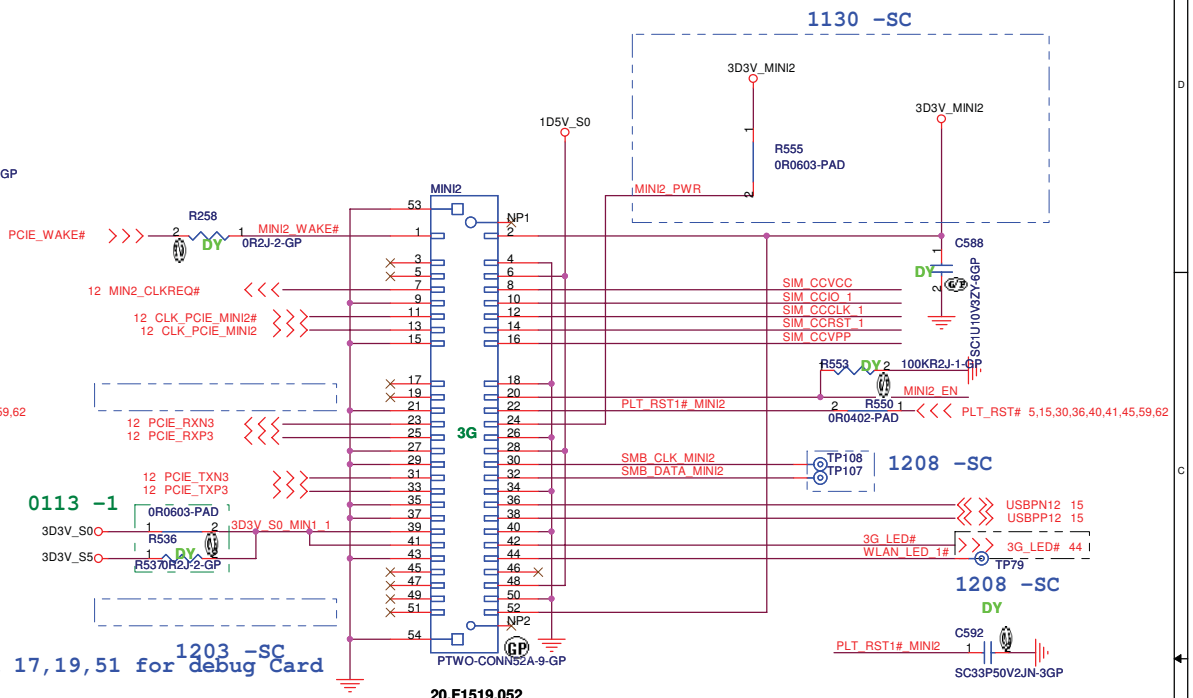
Title: Cardreader
Size: Document Number: HM42-CP
Rev: SC
Date: Friday, January 22, 2010 Sheet 36 of 72

Mini Card Connector(WLAN)
Support debug-card

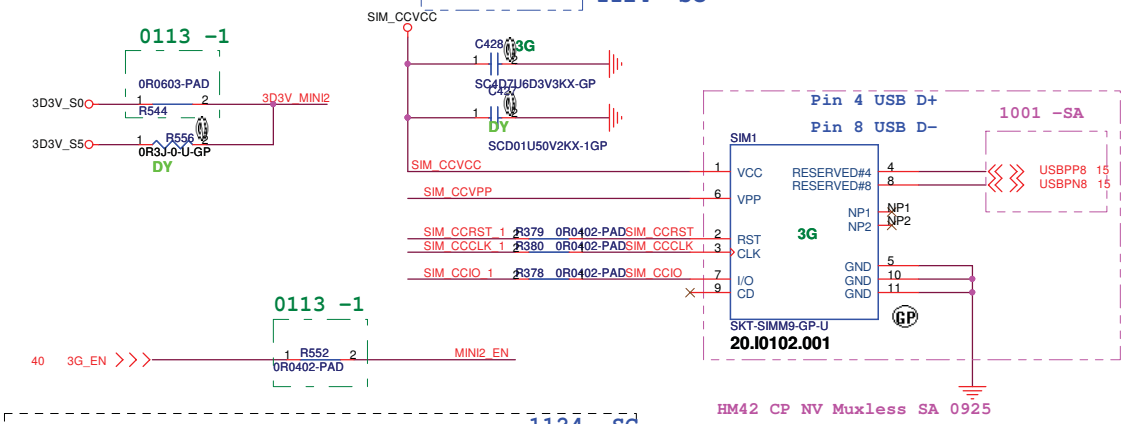


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC

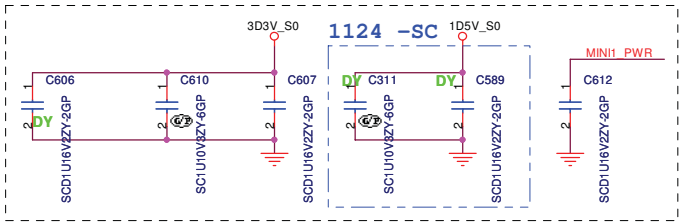
Mini Card Connector(Robson2 and 3G)

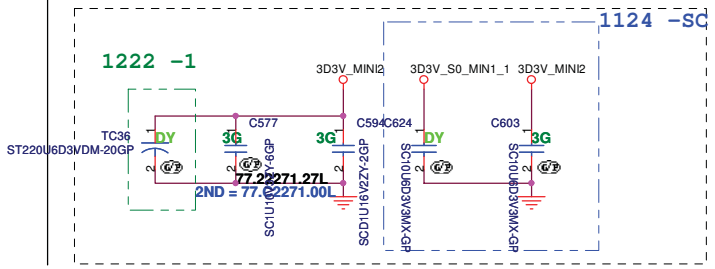


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC



Place near MINI1





Diserete N11M

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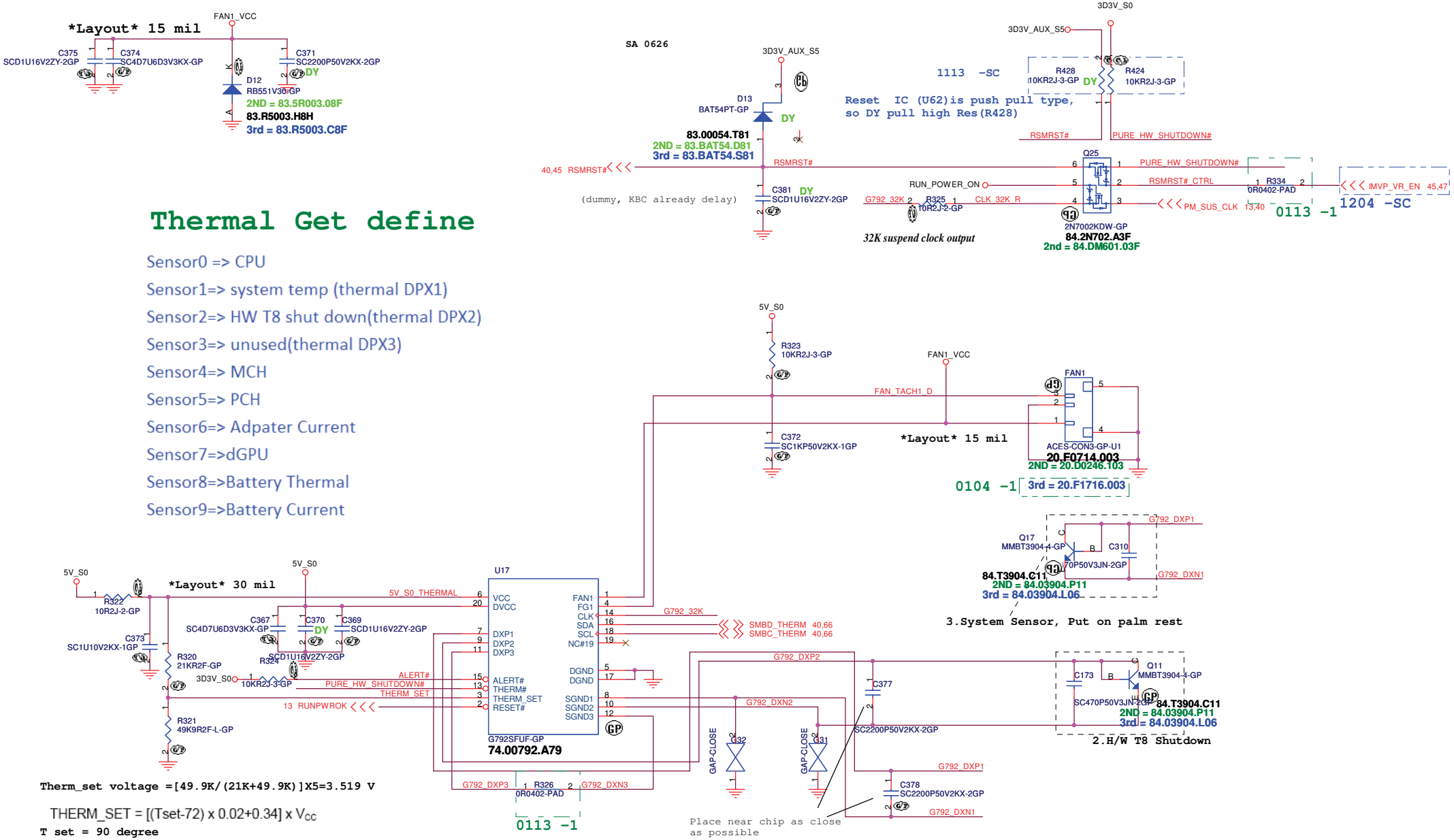
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 37 of 72



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Connector

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 39 of 72

Prevent BIOS data loss solution
1019 -SB

L16 -> 68.00082.011 is a obsoleted part
0930 -SA

Impedance: 60-ohm
rated Current :3A

83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.00054.S81

74.00690.I7B
2ND = 74.00809.V7B

84.03906.R11
2ND = 84.03906.F11
3rd = 84.T3906.A11

68.00230.091
2nd = 68.00206.191

0113 -1

1204 -SC

1016 -SB

SA 0928
ENE suggest 1pF if stuff

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	10.0 K	1.0 K	3.0 V
SB	10.0 K	2.0 K	2.75 V
SC	10.0 K	3.0 K	2.54 V
-1	10.0 K	4.7 K	2.24 V
Reserved	10.0 K	6.98 K	1.94 V
Reserved	10.0 K	8.2 K	1.81 V
Reserved	10.0 K	10.0 K	1.65 V

Model ID
14" PH 10K 3.3V_AUX_S5
17" PL 10K GND

Value	PN
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

0111 -1

1118 -SC

1204 -SC

add test point for debug

1123 -SC

1015 -SB

1202 -SC

2nd = 82.30001.B21
82.30001.661

CL = 7pF
Freq tolertance :+/- 20 ppm

1009 -SA

0105 -1

20.K0320.026
2ND = 20.K0382.026

change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 ->left side
20.K0320.026 Pin 1 -> right side(use in lab stage)
so swap net

74.05711.07B
2nd = 74.09132.C7B

do not use 74.00268.07B in project for Deark suggestion
10-28 -SB

Internal KeyBoard Connector

Cover Up Switch

UMA

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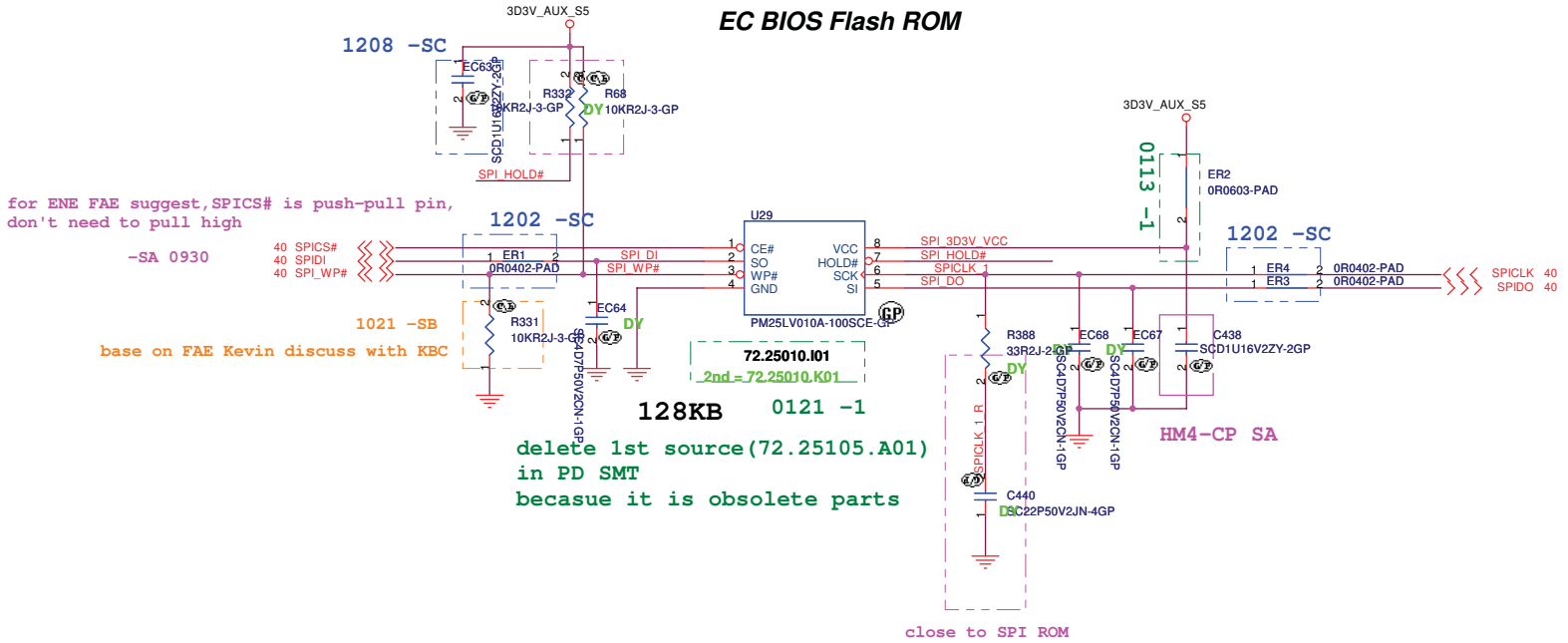
Title: KBC_KB3930

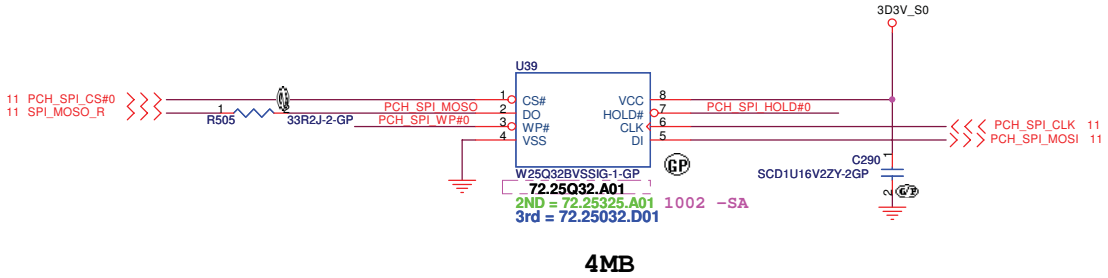
Size	Document Number	Rev
	1	SC

Date: Friday, January 22, 2010 Sheet 40 of 72

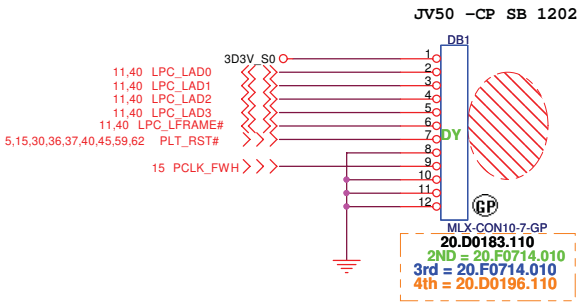
EC BIOS Flash ROM

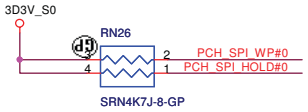


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





Diserete N11M

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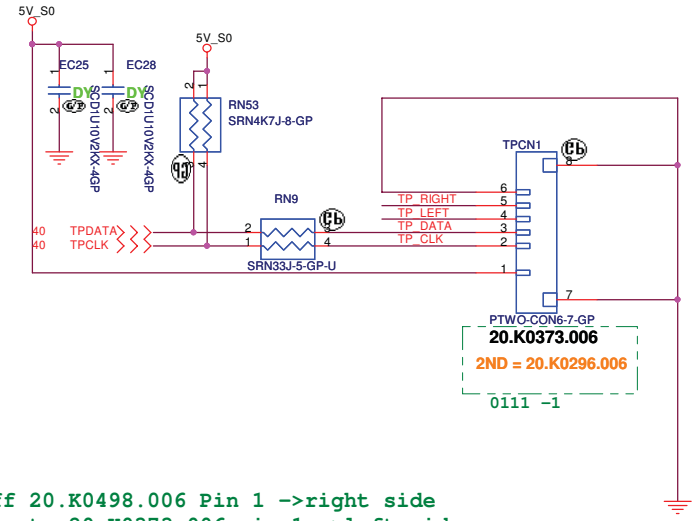
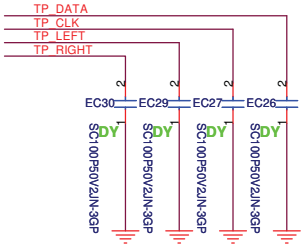
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

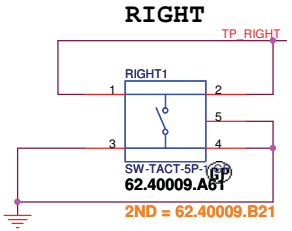
Size	Document Number	Rev
	HM42-CP	SC

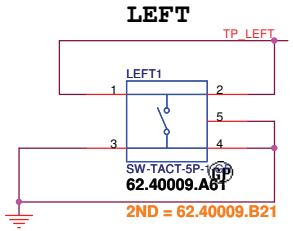
Date: Friday, January 22, 2010 Sheet 41 of 72





Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically

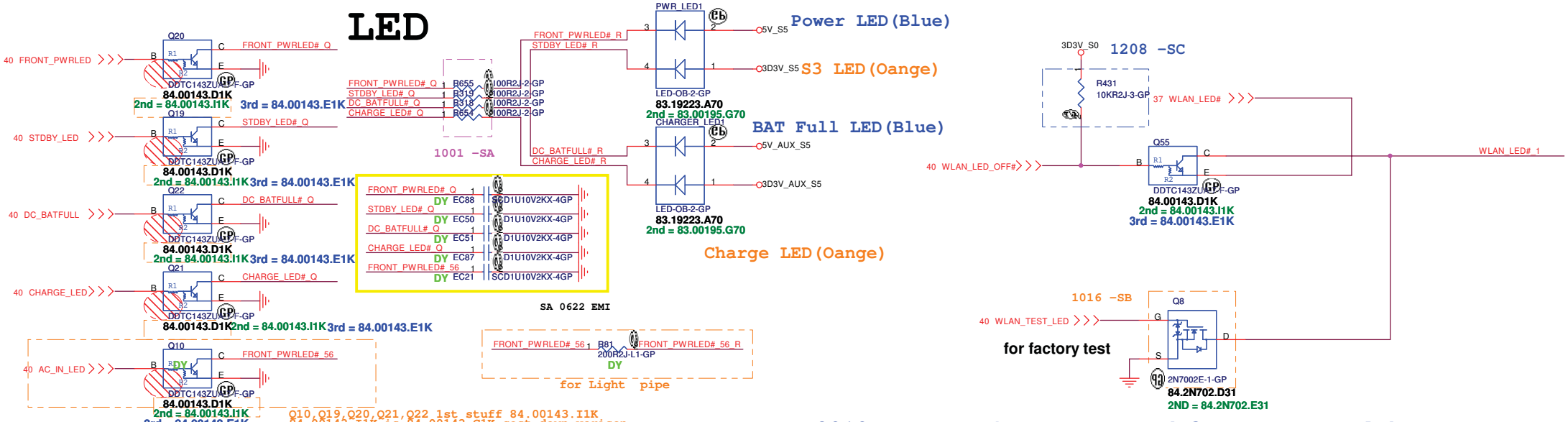




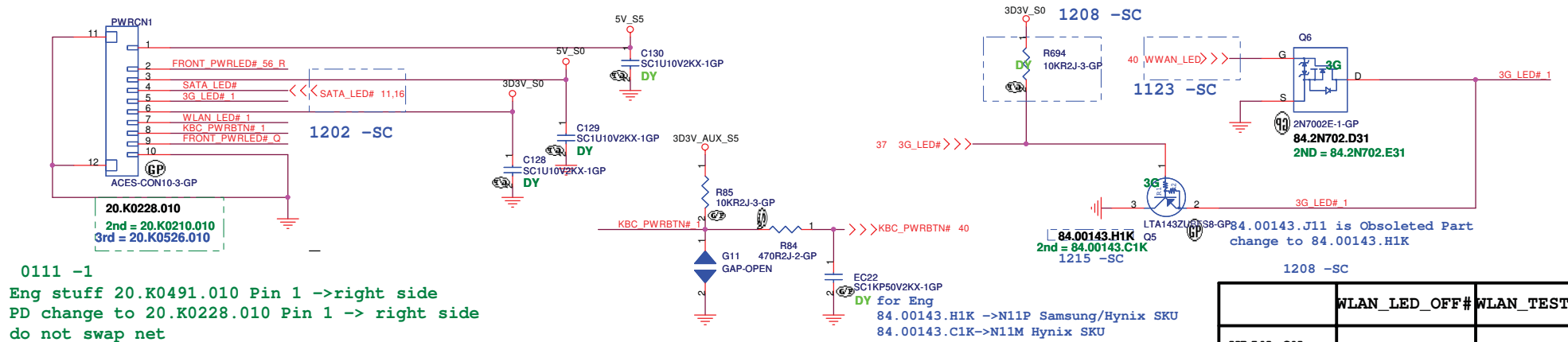
Diserete N11M

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Touch PAD*
Size / Document Number	HM42-CP / Rev SC
Date: Friday, January 22, 2010	Sheet 43 of 72

LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

緯創資通 Wistron Corporation
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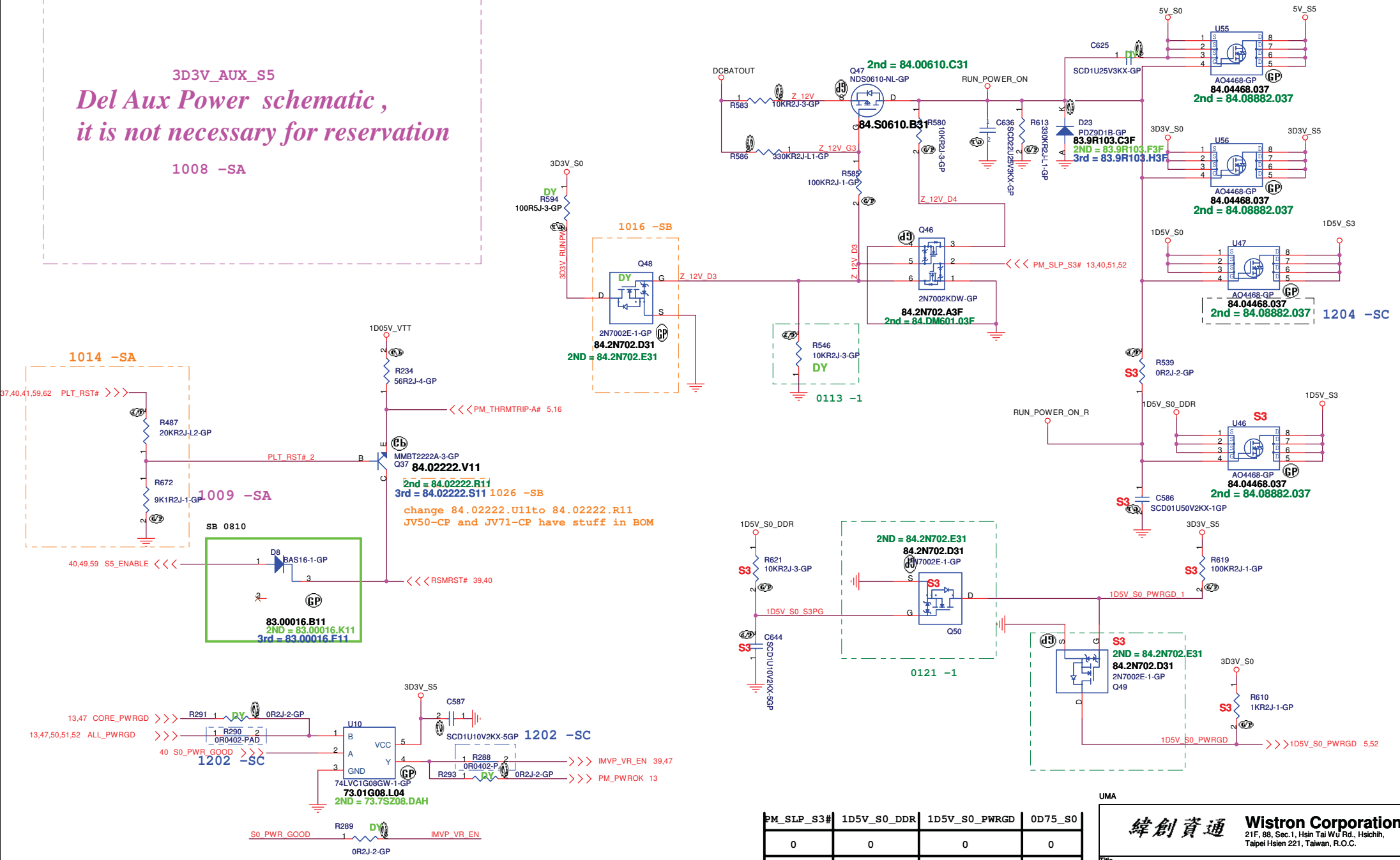
Title: LED&POWERBD CONN
Size | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 Sheet 44 of 72

Run Power

3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

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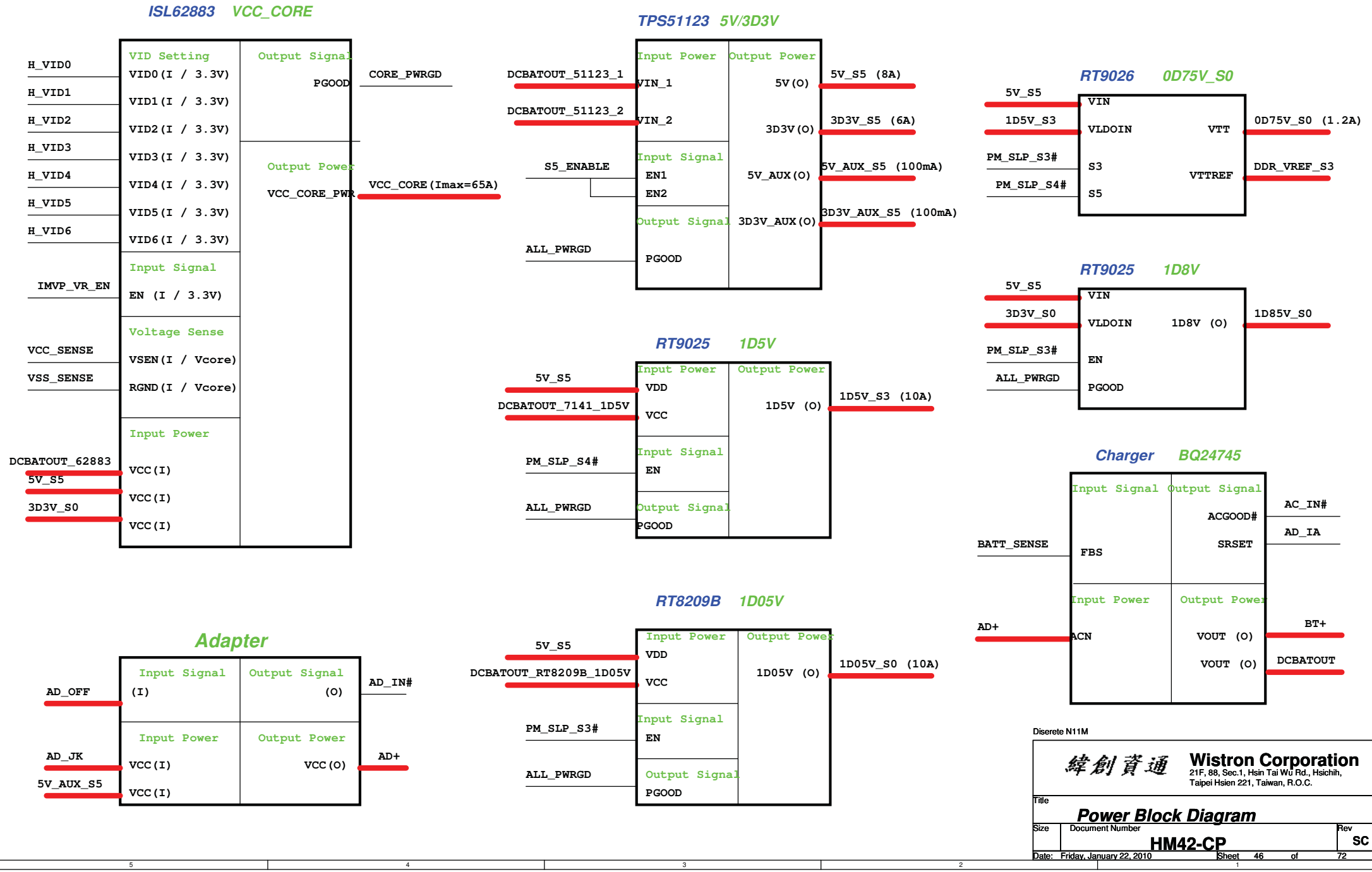
Title: **RUN POWER and 3D3V_AUX_S5**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 45 of 72



Diserete N11M

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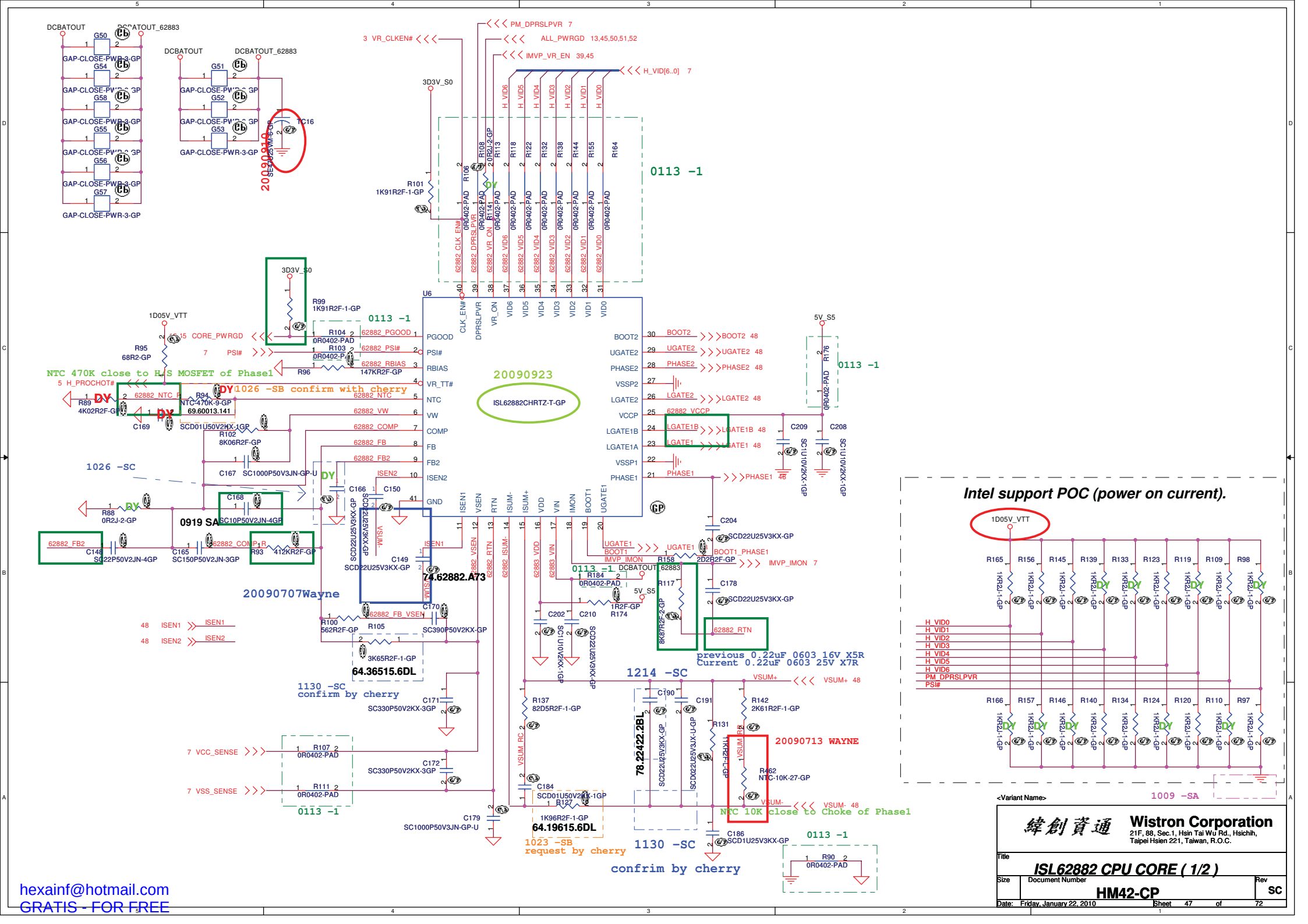
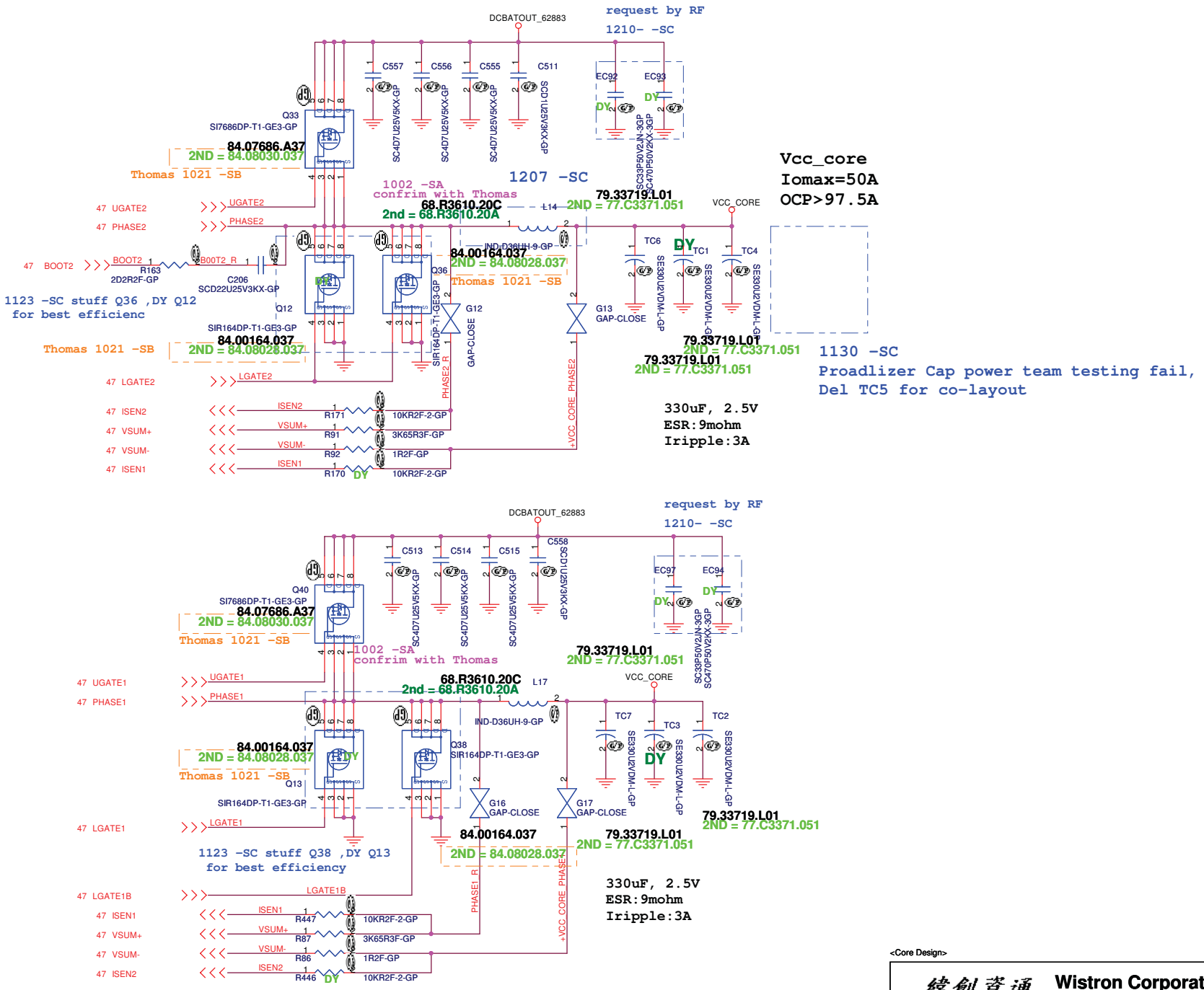
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 46 of 72


DCBATOUT
DCBATOUT_62883
GAP-CLOSE-PWR-3-GP
SE402510M80-GP
20090910
3 VR_CLKEN#
PM_DPRSLPVR 7
ALL_PWRGD 13,45,50,51,52
IMVP_VR_EN 39,45
H_VID[6..0] 7
3D3V_S0
R101 1K91R2F-1-GP
R106 0R0402-PAD
R108 2DR2J-2-GP
R113 0R0402-PAD
R118 R122 R132 R138 R144 R155 R164
0113 -1
DY
62882_CLK_EN#
62882_DPRSLPVR
62882_VR_ON
62882_VID6
62882_VID5
62882_VID4
62882_VID3
62882_VID2
62882_VID1
62882_VID0
U6
CLK_EN#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
ISL62882CHRTZ-T-GP
20090923
1D05V_VTT
5V_S5
R99 1K91R2F-1-GP
R104 0R0402-PAD
R103 0R0402-PAD
R96 147KR2F-GP
R95 68R2-GP
R89 4K02R2F-GP
R94 NTC-470K-9-GP
69.60013.141
NTC 470K close to H_LS MOSFET of Phase1
5 H_PROCHOT#
1026 -SB confirm with cherry
C169 SCD01U50V2KX-1GP
R102 8K06R2F-GP
C167 SC1000P50V3JN-GP-U
1026 -SC
R88 0R2J-2-GP
C168 SC10P50V2JN-4GP
0919 SA
C166 SCD22U25V3KX-GP
C150 SC1U10V2KX-1GP
C148 SC22P50V2JN-4GP
C165 SC150P50V2JN-3GP
R93 412KR2F-GP
C149 SCD22U25V3KX-GP
74.62882.A73
20090707Wayne
C170 SC390P50V2KX-GP
R100 562R2F-GP
R105 3K65R2F-1-GP
64.36515.6DL
1130 -SC confirm by cherry
C171 SC330P50V2KX-3GP
C172 SC330P50V2KX-3GP
7 VCC_SENSE
7 VSS_SENSE
R107 0R0402-PAD
R111 0R0402-PAD
0113 -1
C179 SC1000P50V3JN-GP-U
C184 SCD01U50V2KX-1GP
R127 1K96R2F-1-GP
64.19615.6DL
1023 -SB request by cherry
C190 SCD22U25V3KX-GP
C191 SCD22U25V3JX-U-GP
78.22422.2BL
1214 -SC
R137 82D5R2F-1-GP
R131 1KR2F-1-GP
R142 2K61R2F-1-GP
R462 NTC-10K-27-GP
20090713 WAYNE
NTC 10K close to Choke of Phase1
C186 SCD1U25V3KX-GP
1130 -SC confrim by cherry
R184 0R0402-PAD
R174 1R2F-GP
C202 SCD22U25V3KX-GP
C210 SC1U10V2KX-1GP
R158 2D2R2F-GP
R117 8K87R2F-2-GP
C178 SCD22U25V3KX-GP
62882_RTN
previous 0.22uF 0603 16V X5R
Current 0.22uF 0603 25V X7R
C204 SCD22U25V3KX-GP
R176 0R0402-PAD
C209 SC1U10V2KX-1GP
C208 SC1U10V2KX-1GP
BOOT2
UGATE2
PHASE2
LGATE2
VCCP
LGATE1B
LGATE1
PHASE1
62882_PGOOD
62882_PSI#
62882_RBIAS
62882_NTC
62882_VW
62882_COMP
62882_FB
62882_FB2
62882_ISEN2
62882_VSEN
62882_RTN
62882_ISUM-
62882_FB_VSEN
62882_VCCP
62883_VDD
62883_VIN
IMVP_IMON
BOOT1_PHASE1
VSUM+
VSUM-
VSUM_RC
VSUM_FB
ISEN1
ISEN2
48 ISEN1
48 ISEN2
IMVP_IMON 7
VSUM+ 48
VSUM- 48
Intel support POC (power on current).
1009 -SA
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
R165 R156 R145 R139 R133 R123 R119 R109 R98
R166 R157 R146 R140 R134 R124 R120 R110 R97
1KR2J-1-GP
DY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 47 of 72
hexainf@hotmail.com
GRATIS - FOR FREE



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ISL62882 CPU CORE (1/2)***

Size	Document Number	Rev
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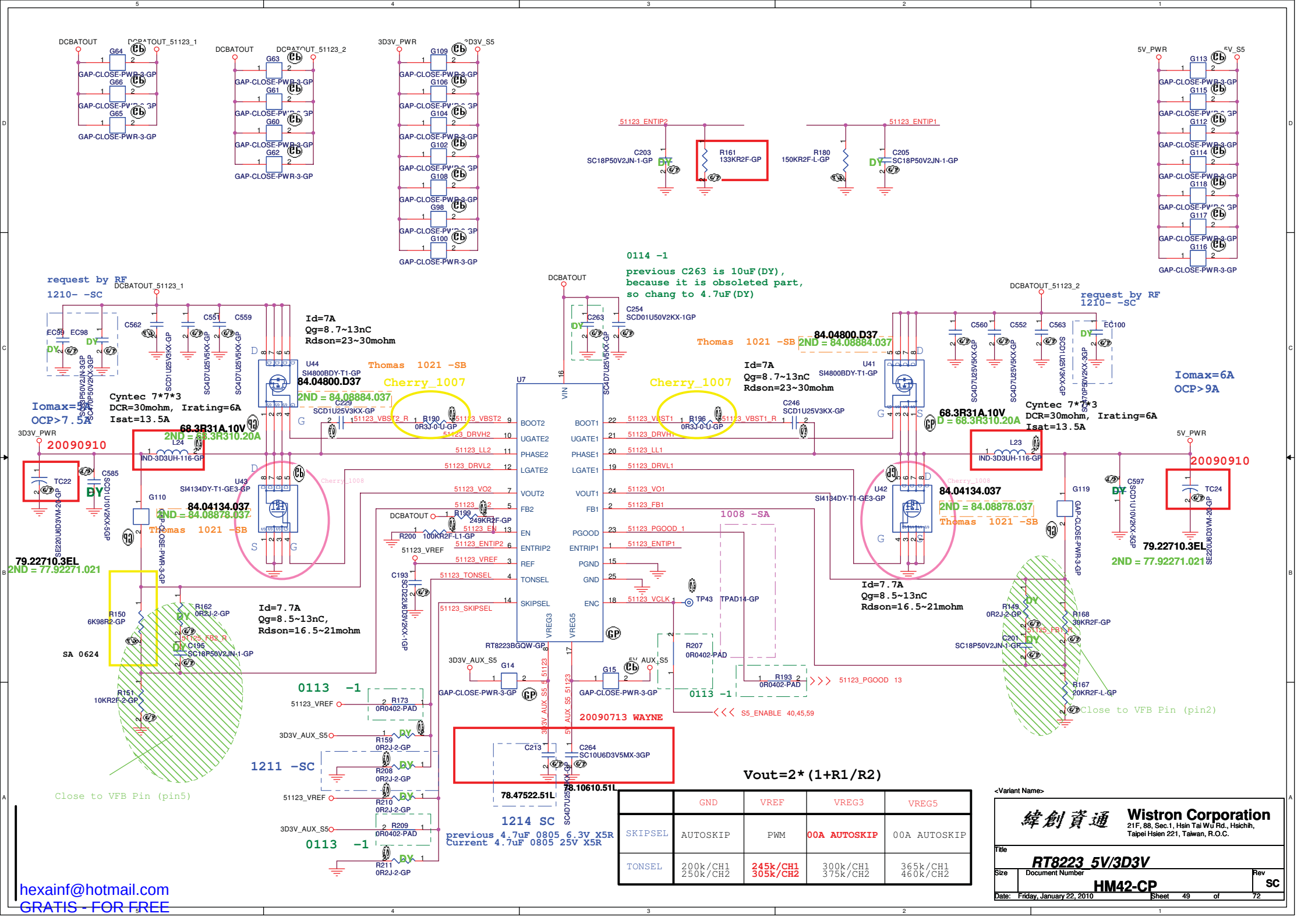
Date: Friday, January 22, 2010 Sheet 48 of 72



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

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Title: RT8223_5V/3D3V

Size | Document Number: HM42-CP | Rev: SC

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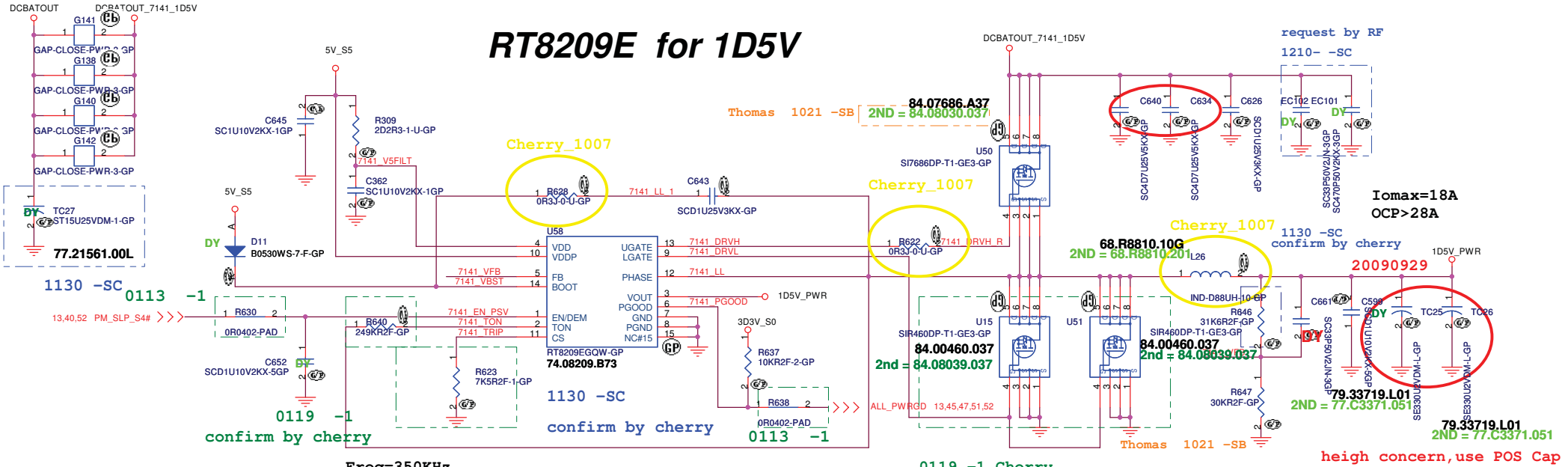
RT8209E for 1D5V



$$V_{CS}\,(mV) = R_{CS}\,(k\Omega) \times 10\,(\mu A)$$

$$I_{LOAD\_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{V_{IN}}$$

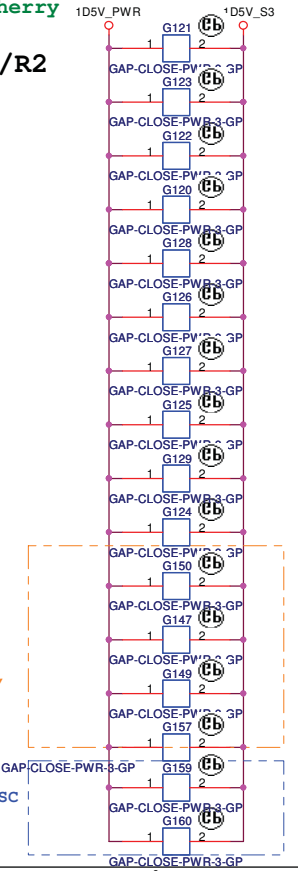
VCS(mV)=9.09KX10uA=90.9mV

I_OCP=[(90.9mV/3.2mohm)+(1/2*350Khz* 0.88uH)*[(19-1.5)*1.5/19]

=28.4 +1.623 *1.38 =30A

Iocp = Io *1.5

Vout=0.75V*(R1+R2)/R2

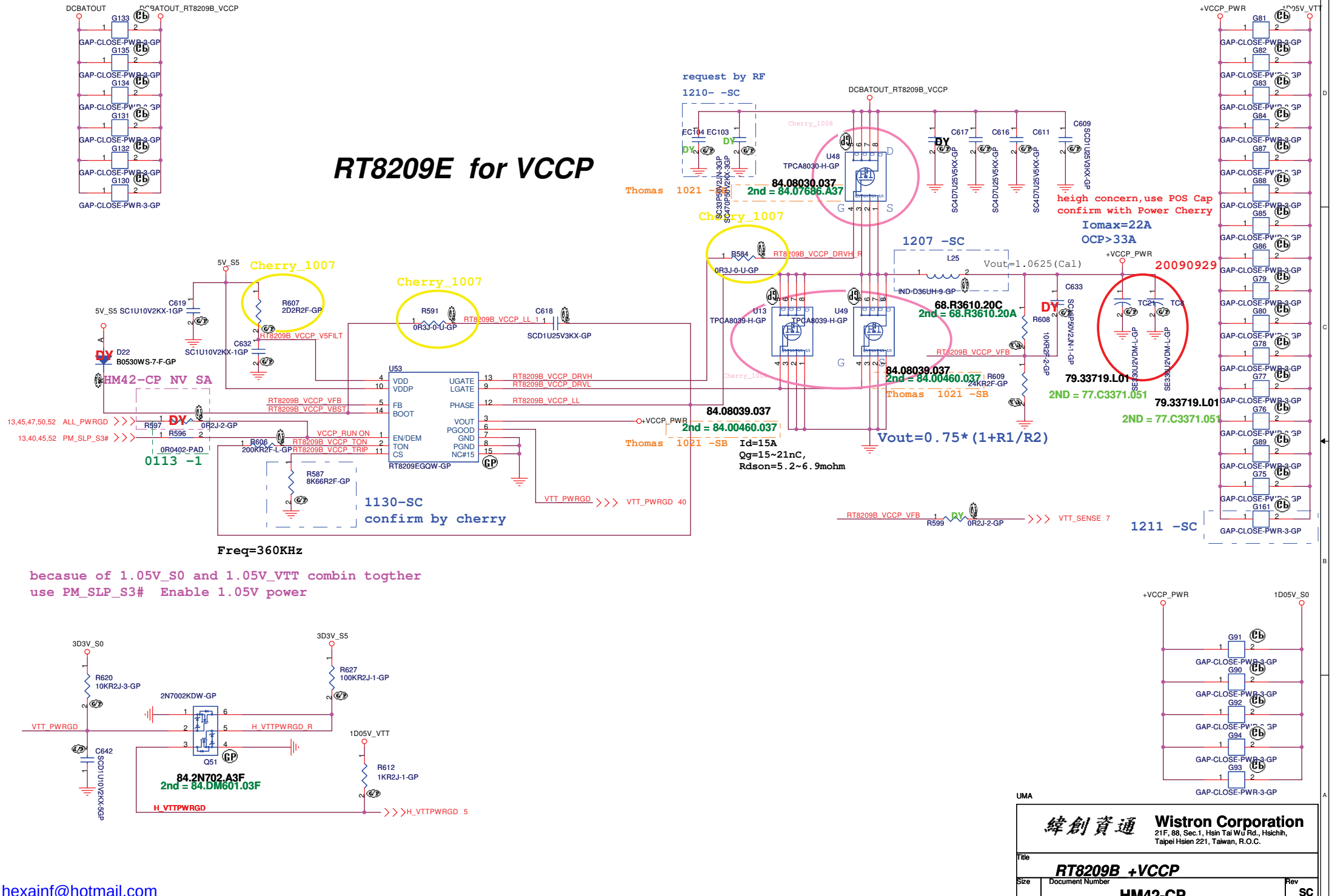


1022 -SB
cherry request 8 pcs Gap,
becasue of space concern,
only add 4pcs Cap.

Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209B 1D5V		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 50 of 72	

RT8209E for VCCP



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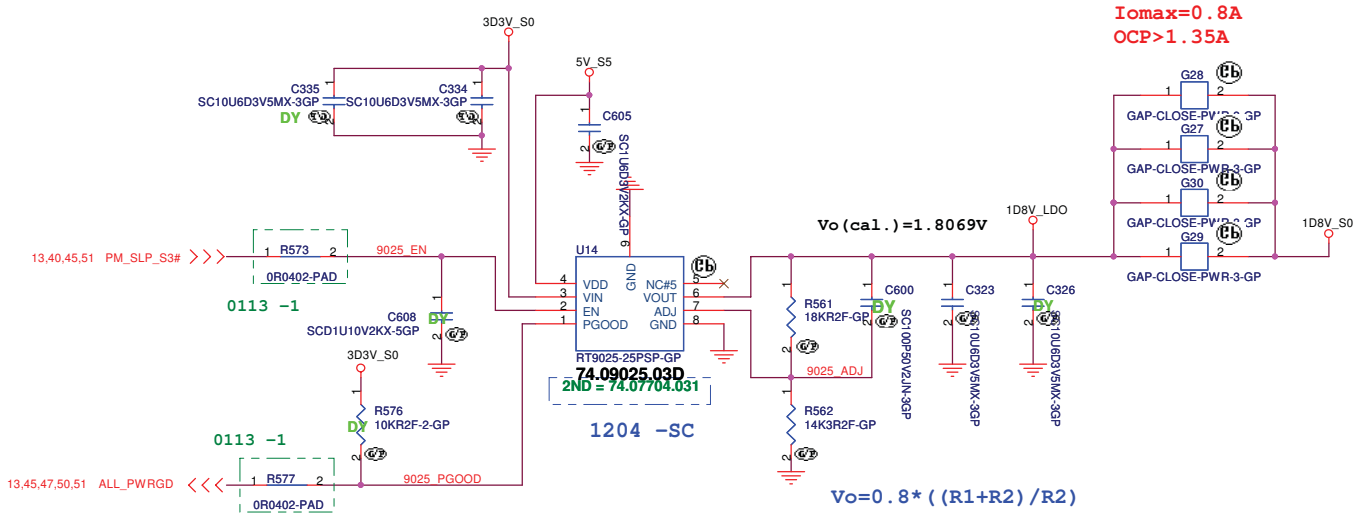
Taipei Hsien 221, Taiwan, R.O.C.

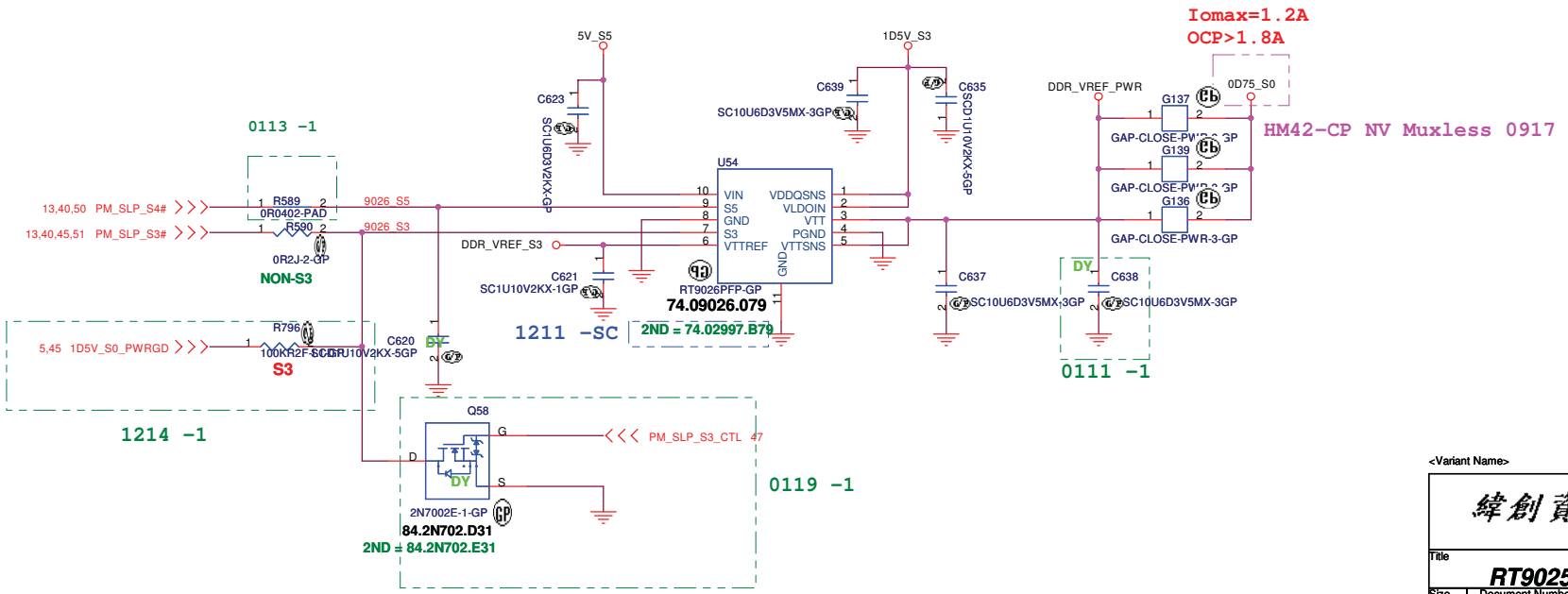
Title	RT8209B +VCCP	
Size	Document Number HM42-CP	Rev SC
Date: Friday, January 22, 2010	Sheet 51 of 72	

RT9025 for 1D8V_S0

20090915



RT9026 for 0D75V_S0



<Variant Name>

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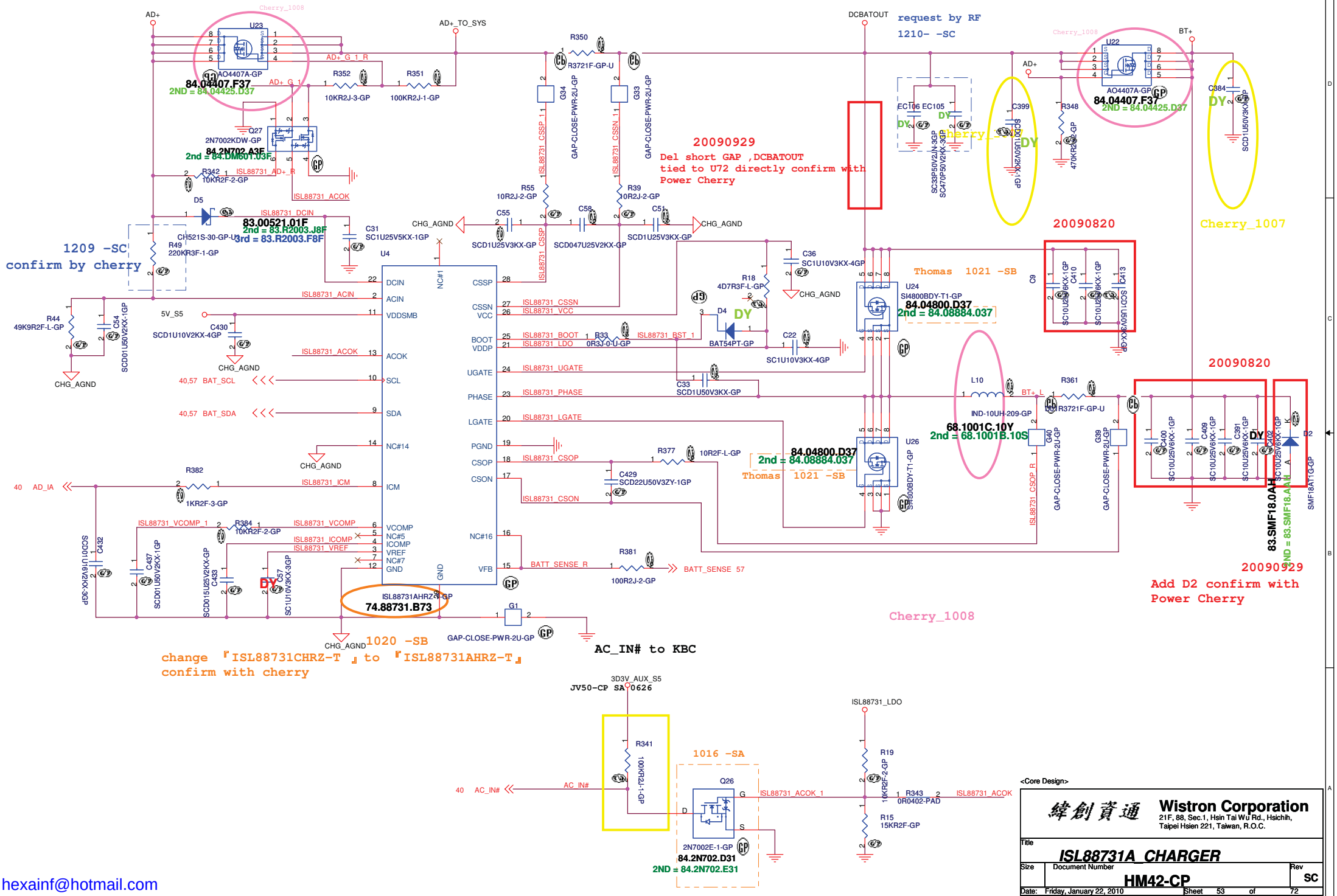
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V/RT9026_0D75

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 52 of 72



<Core Design>
緯創資通 Wistron Corporation
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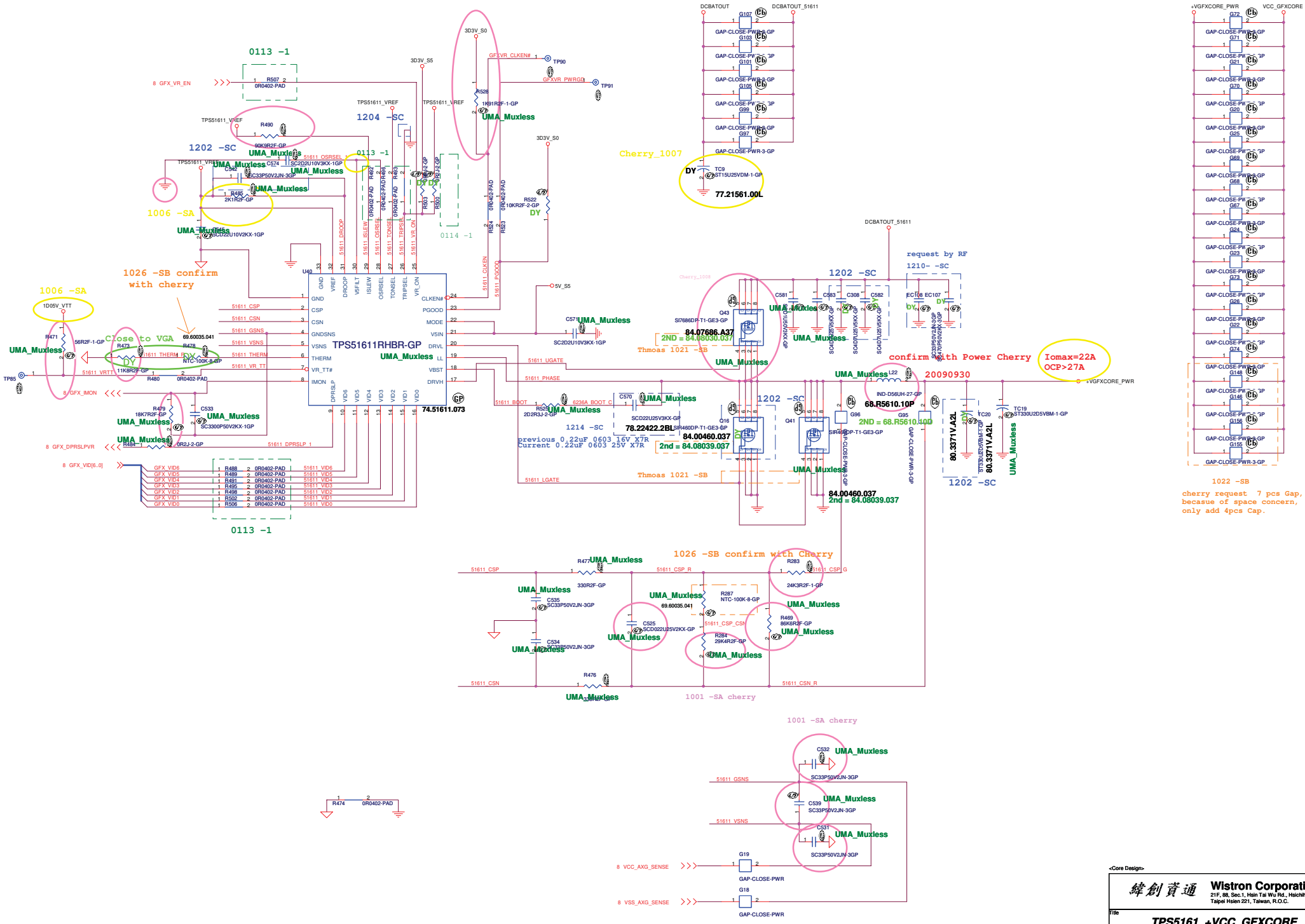
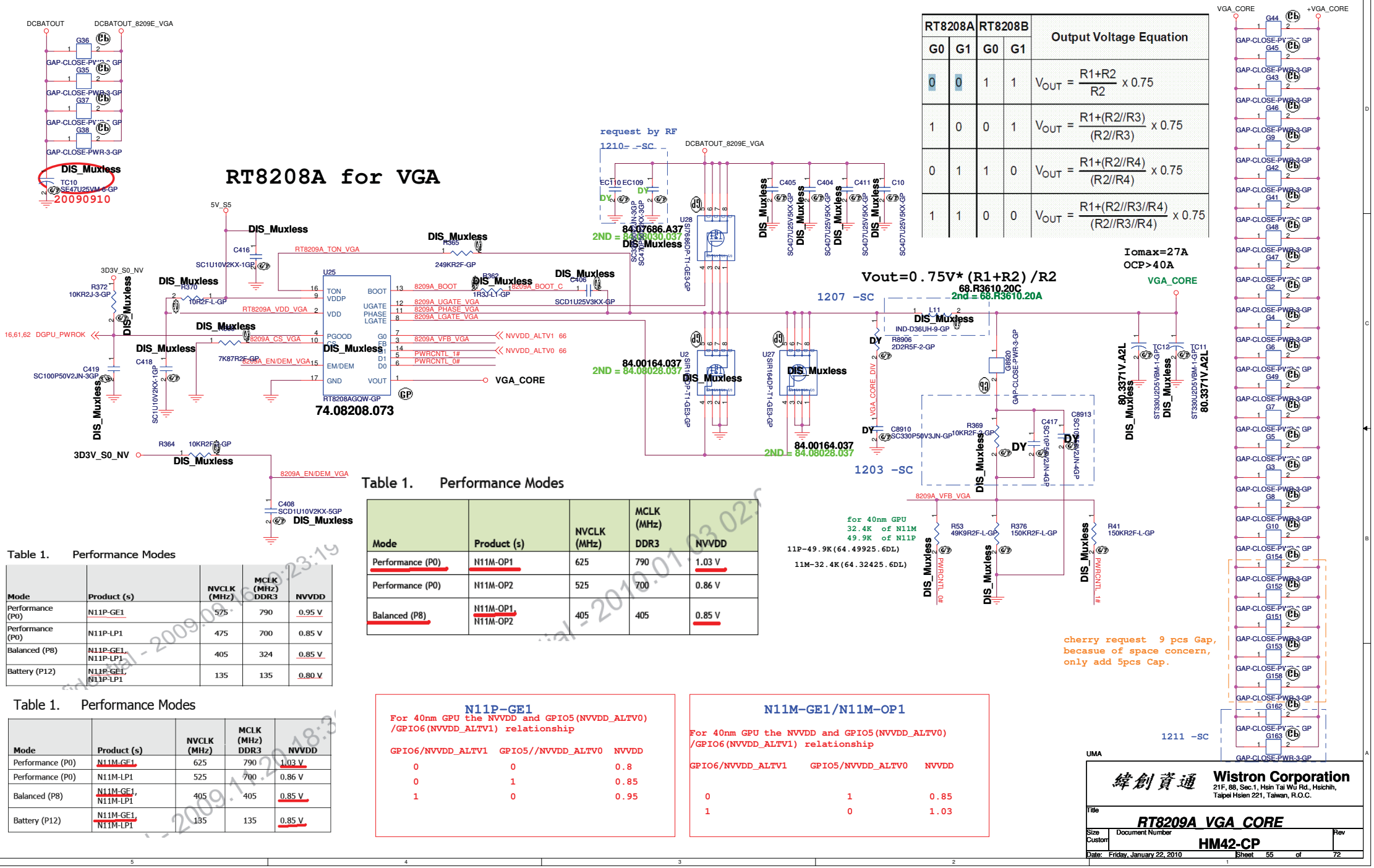
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL88731A_CHARGER
Size: | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 53 of 72





RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-OP1	405	405	0.85 V

N11P-GE1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5//NVVDD_ALTV0	NVVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5/NVVDD_ALTV0	NVVDD
0	1	0.85
1	0	1.03

UMA

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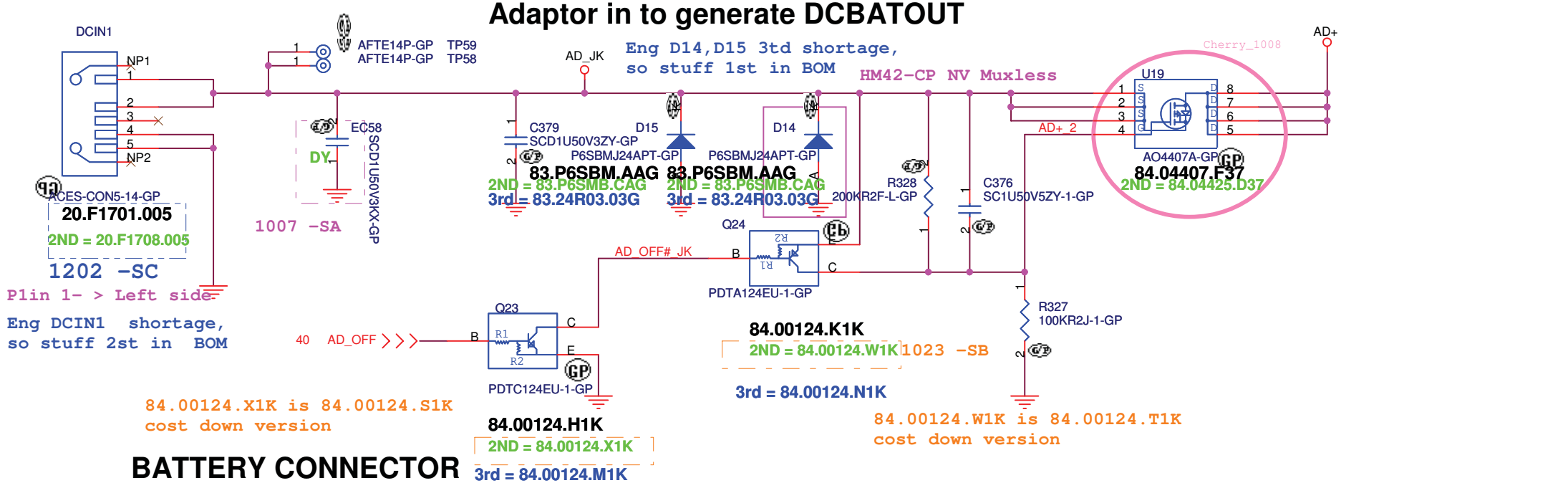
Title: RT8209A_VGA_CORE

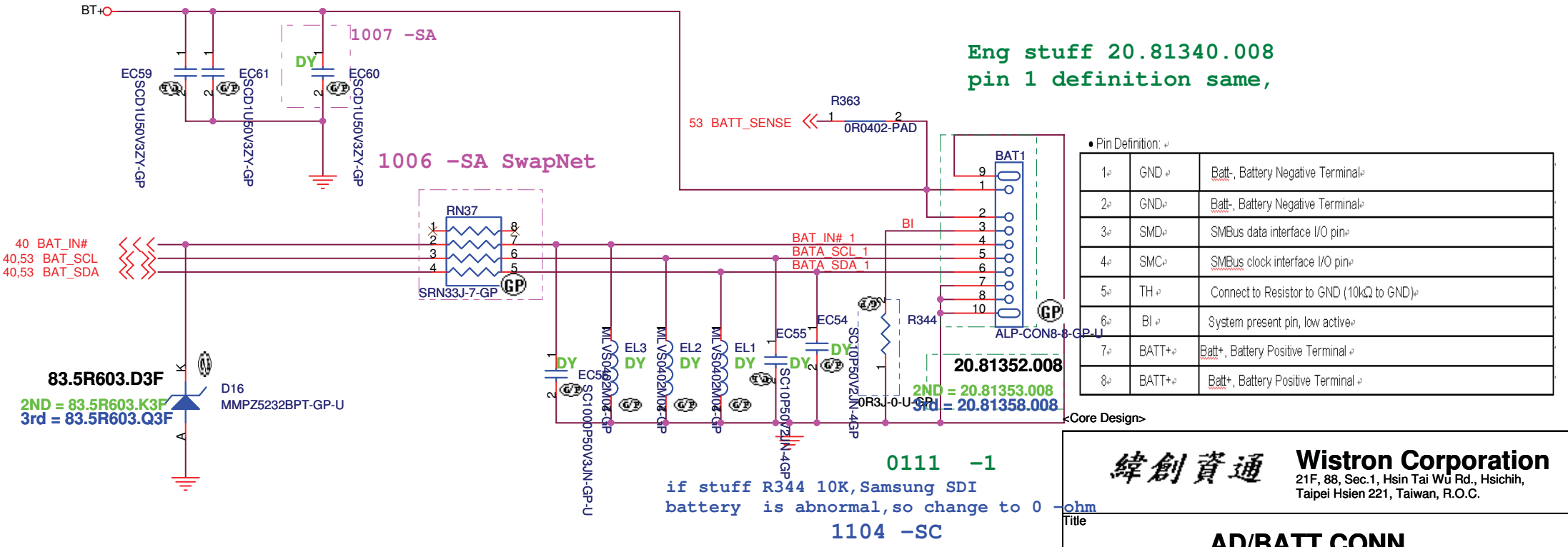
Size: Custom | Document Number: HM42-CP | Rev:

Date: Friday, January 22, 2010 | Sheet 55 of 72

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

緯創資通 Wistron Corporation
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Title: **AD/BATT CONN**

Size	Document Number	Rev
	HM42-CP	SC

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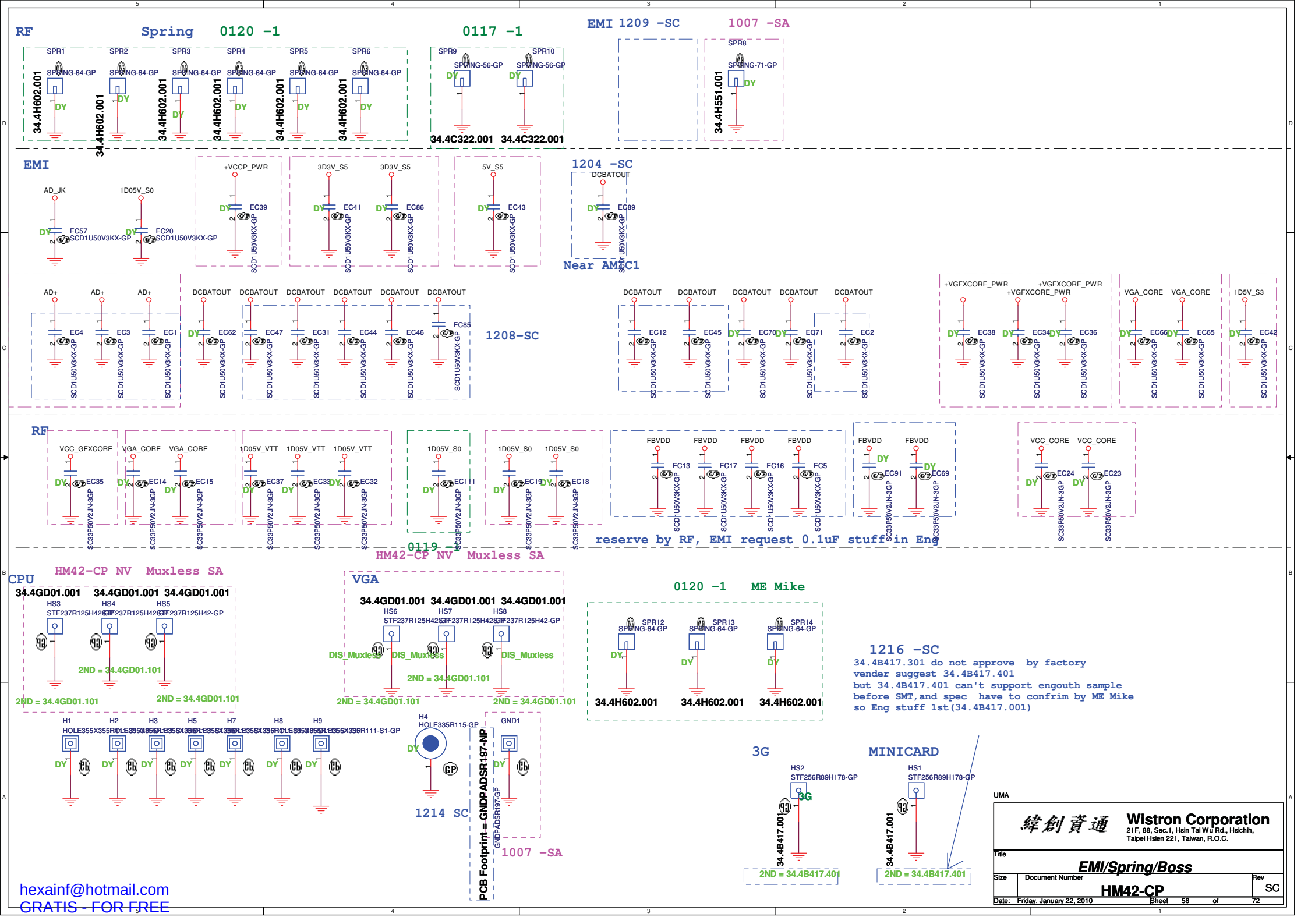
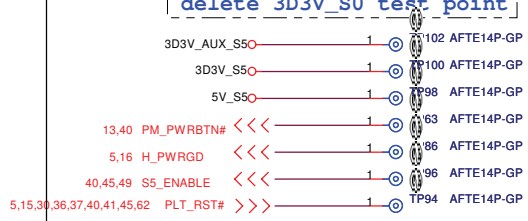


Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

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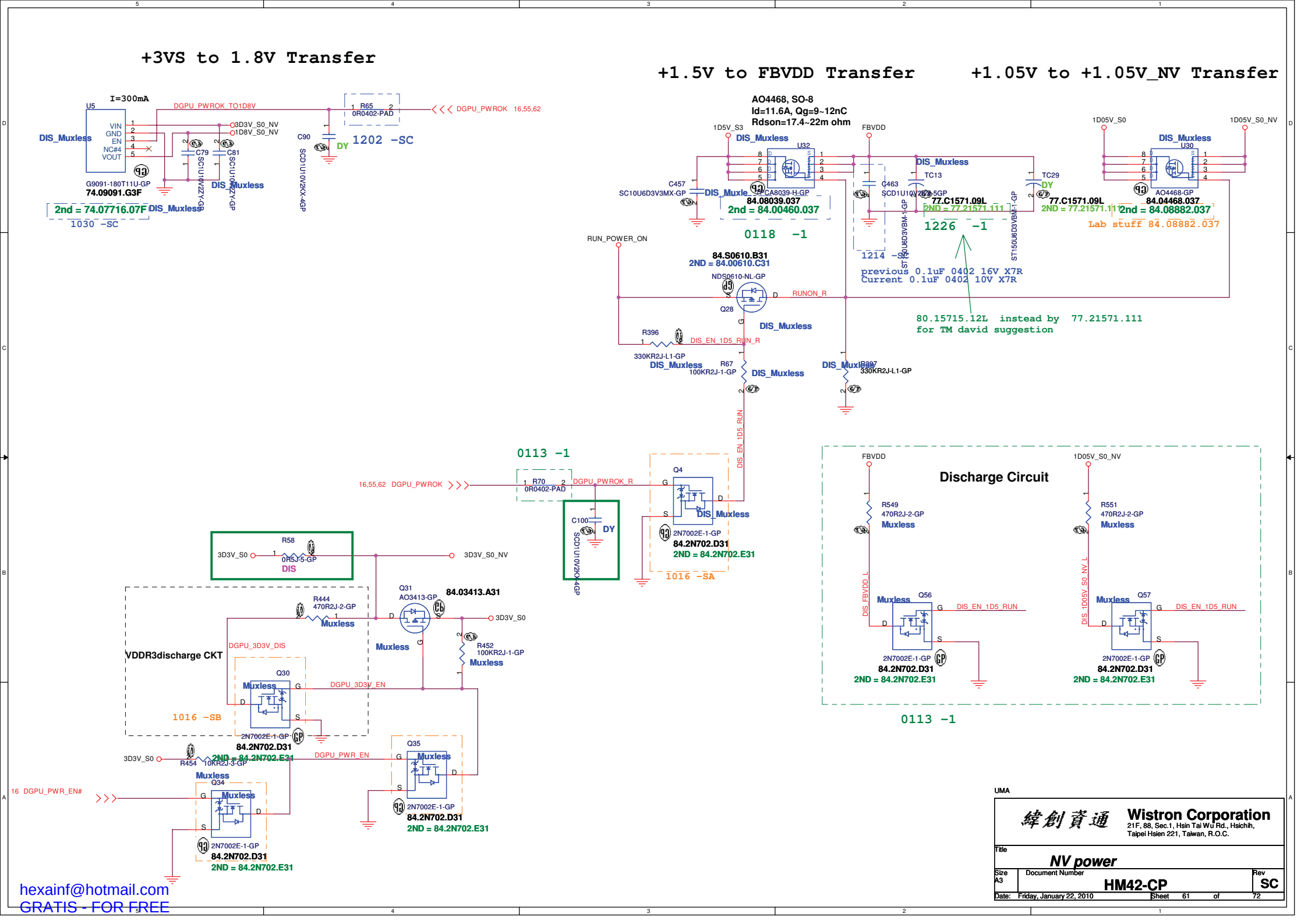
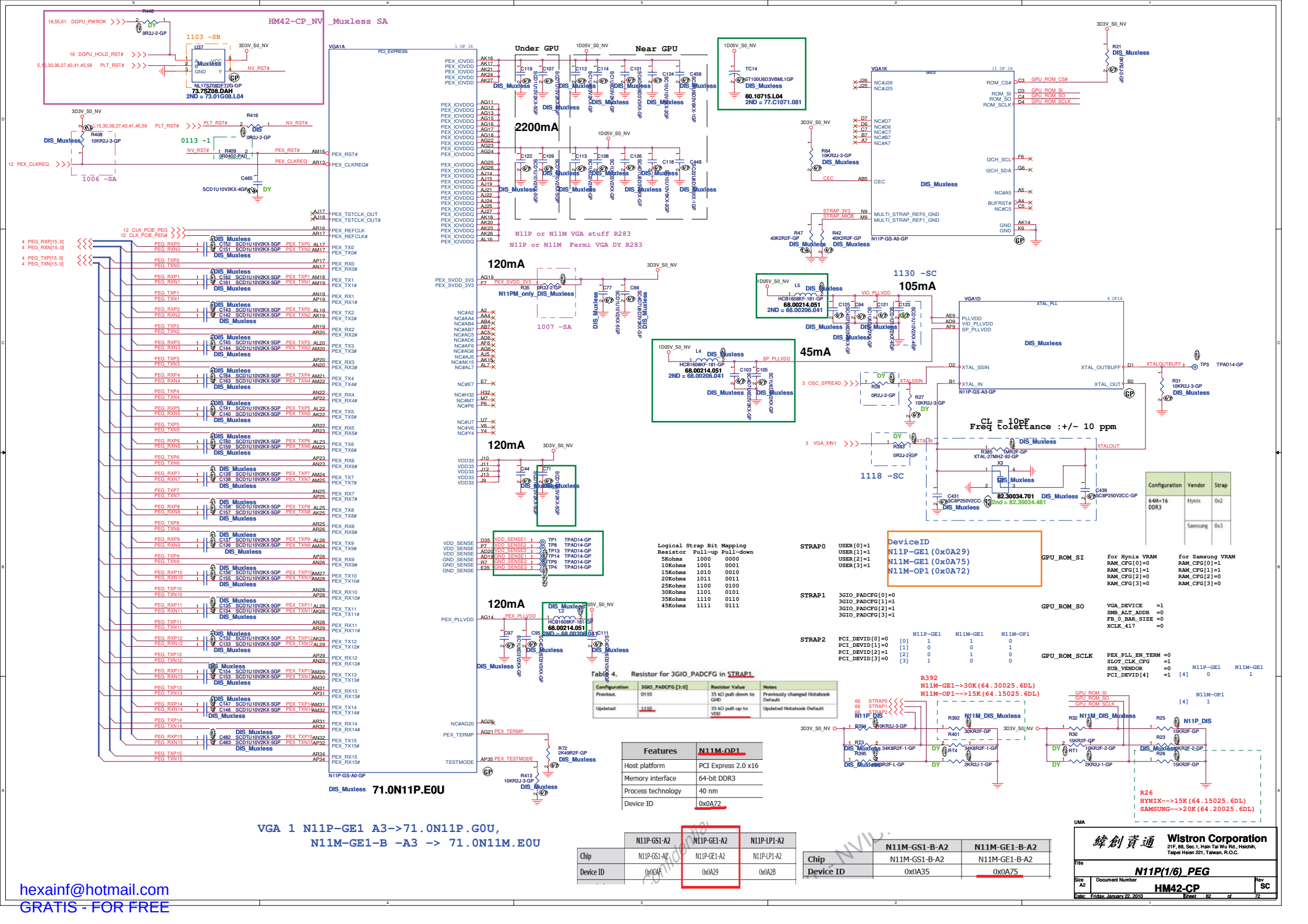
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AFTE_TP

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 59 of 72





Configuration	Vendor	Strap
64M×16 DDR3	Hynix	0x2
	Samsung	0x3

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

STRAP0
USER[0]=1
USER[1]=1
USER[2]=1
USER[3]=1

STRAP1
3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=1

STRAP2

	N11P-GE1	N11M-GE1	N11M-OP1
PCI_DEVID[0]=0	[0] 1	1	0
PCI_DEVID[1]=0	[1] 0	0	1
PCI_DEVID[2]=1	[2] 0	1	0
PCI_DEVID[3]=0	[3] 1	0	0

GPU_ROM_SI
for Hynix VRAM
RAM_CFG[0]=0
RAM_CFG[1]=1
RAM_CFG[2]=0
RAM_CFG[3]=0
for Samsung VRAM
RAM_CFG[0]=1
RAM_CFG[1]=1
RAM_CFG[2]=0
RAM_CFG[3]=0

GPU_ROM_SO
VGA_DEVICE =1
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0

GPU_ROM_SCLK
PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 [4] N11P-GE1 0, N11M-GE1 1, N11M-OP1 1

Table 4. Resistor for 3GIO_PADCFG in STRAP1

Configuration	3GIO_PADCFG [3:0]	Resistor Value	Notes
Previous	0110	35 kΩ pull-down to GND	Previously changed Notebook Default
Updated	1110	35 kΩ pull-up to VDD	Updated Notebook Default

Features	N11M-OP1
Host platform	PCI Express 2.0 x16
Memory interface	64-bit DDR3
Process technology	40 nm
Device ID	0x0A72

	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0CA0	0x0A29	0x0A2B

	N11M-GS1-B-A2	N11M-GE1-B-A2
Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75

UMA

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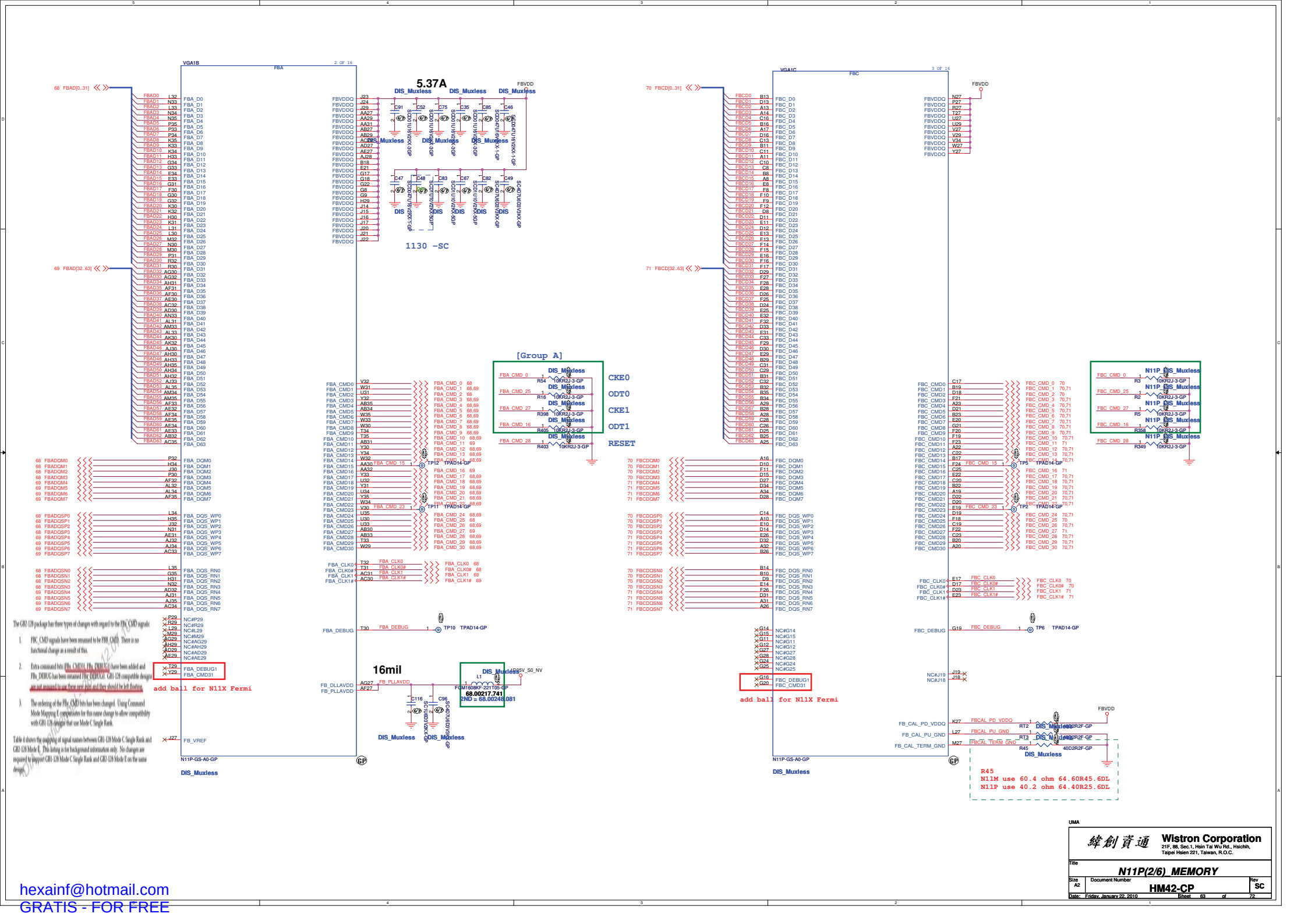
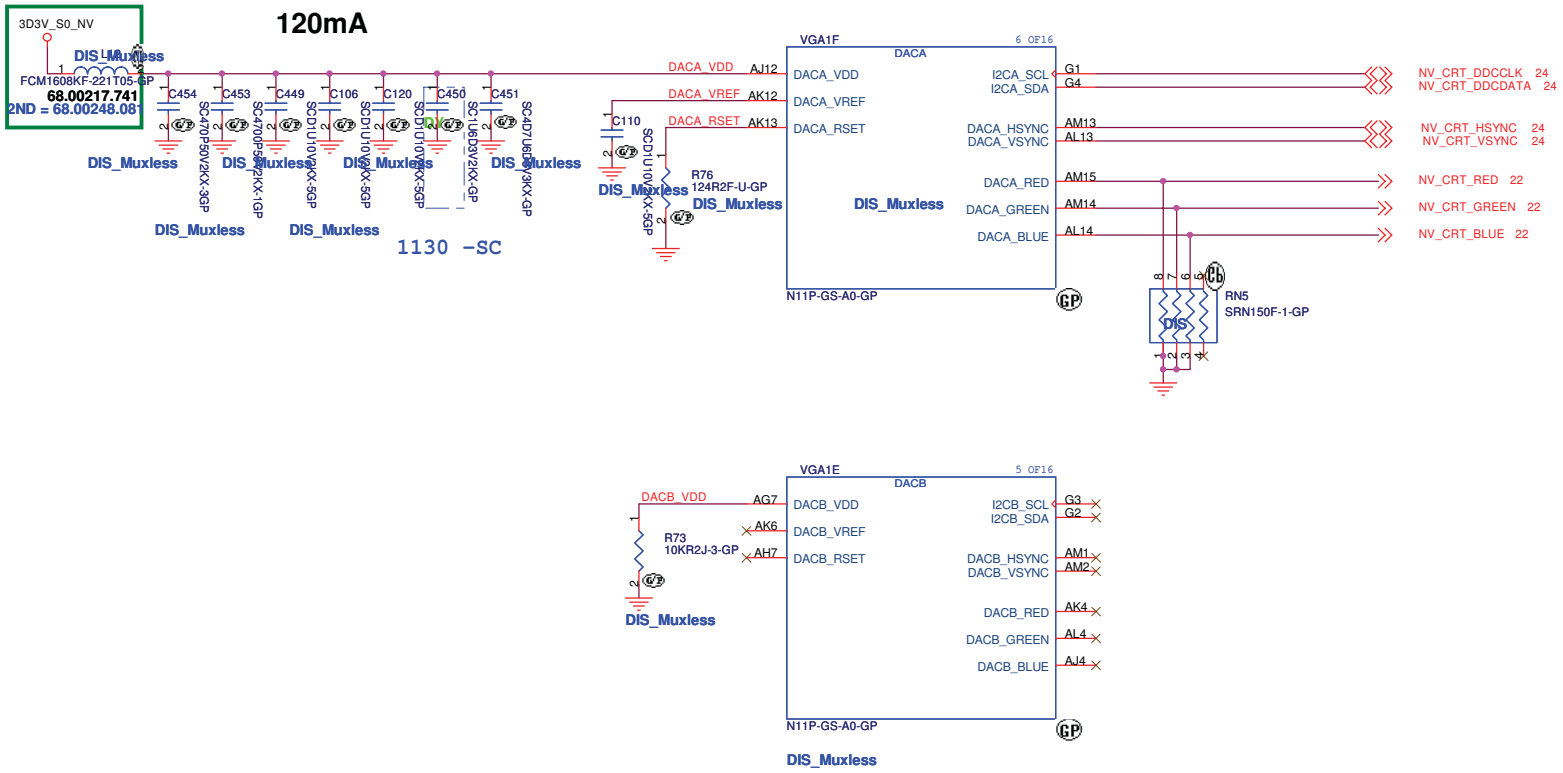
Title: N11P(1/6)_PEG
Size: A2 | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 62 of 72





Diserete N11M

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Taipei Hsien 221, Taiwan, R.O.C.

Title: N11P(3/6)_DAC

Size	Document Number	Rev
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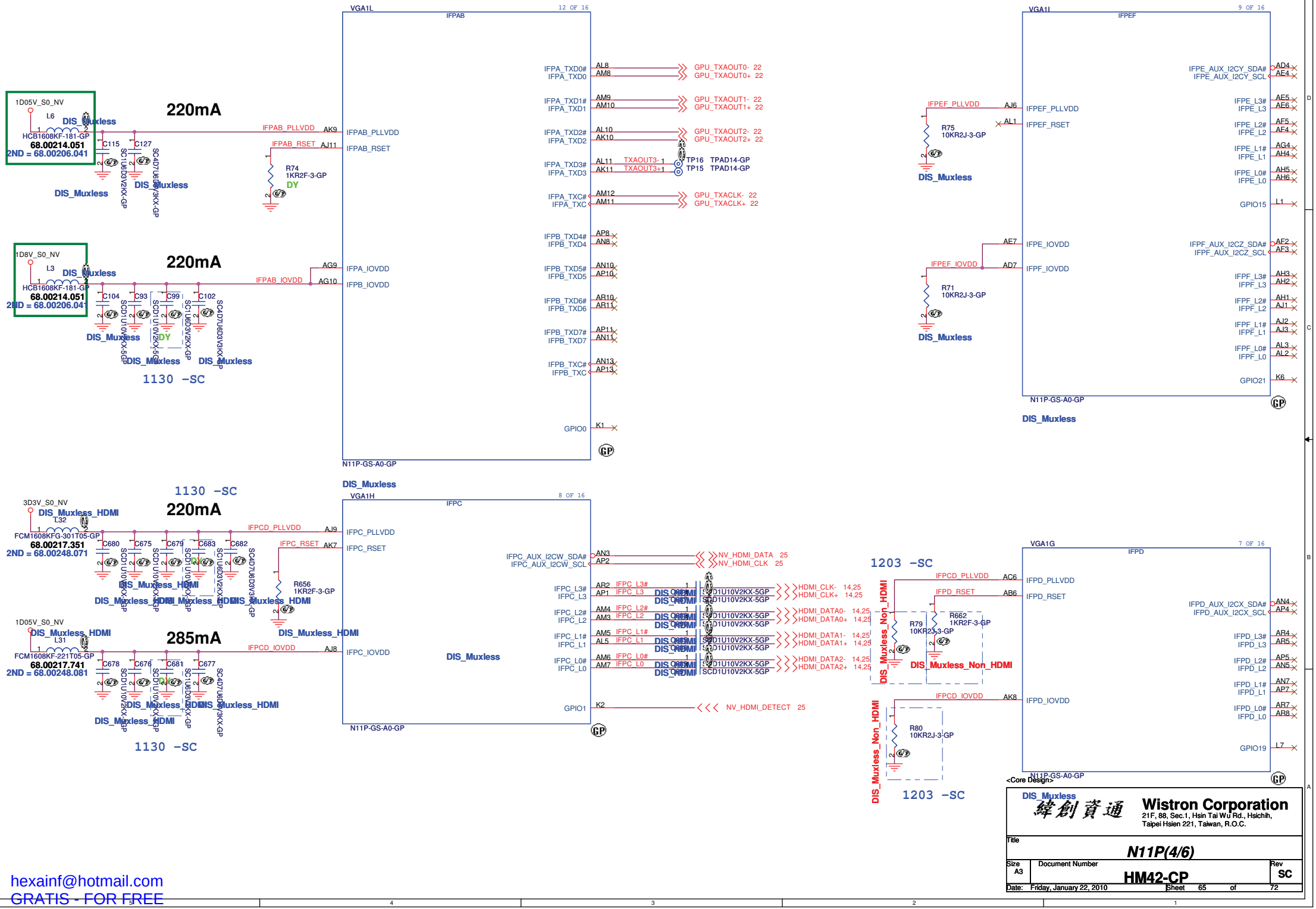
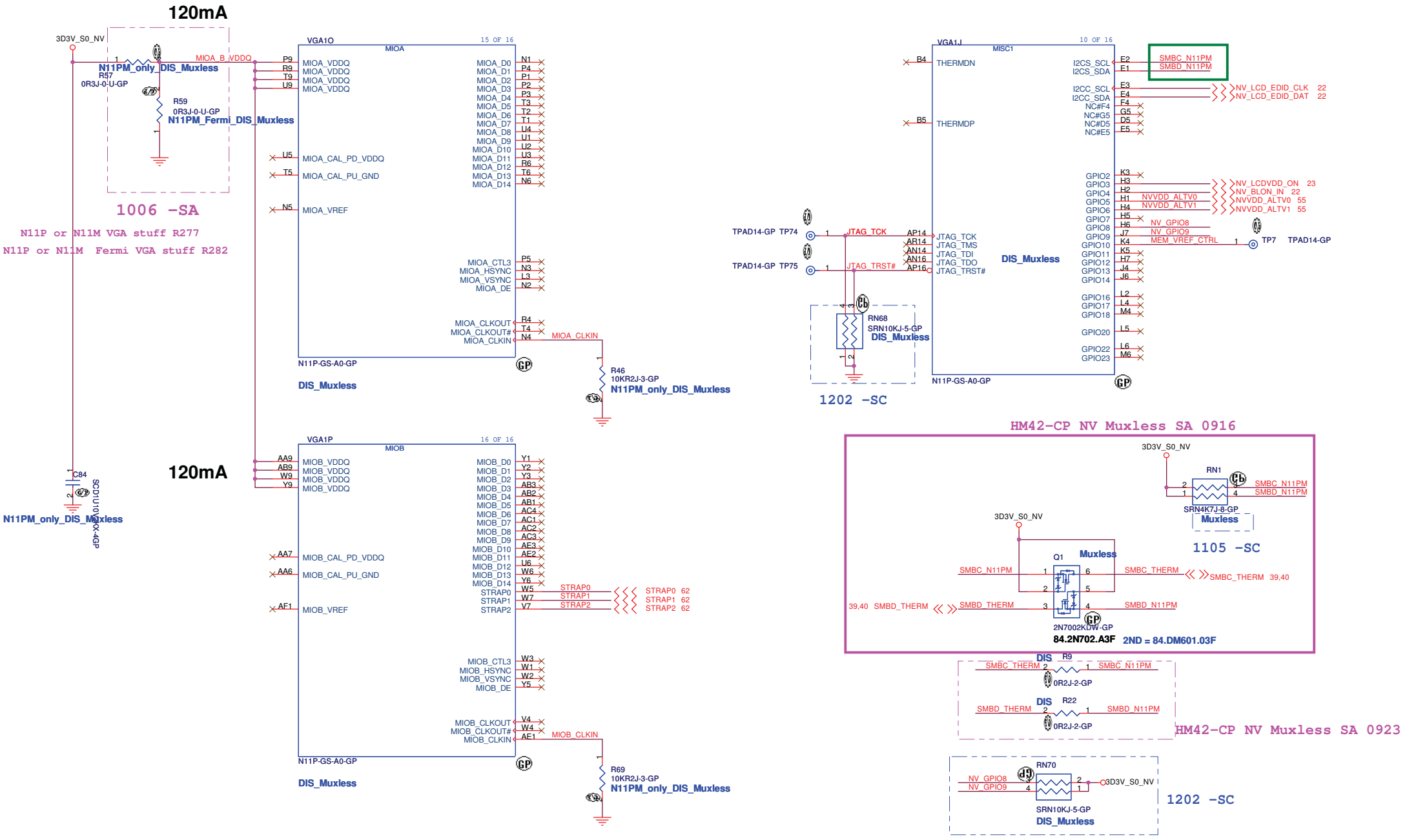
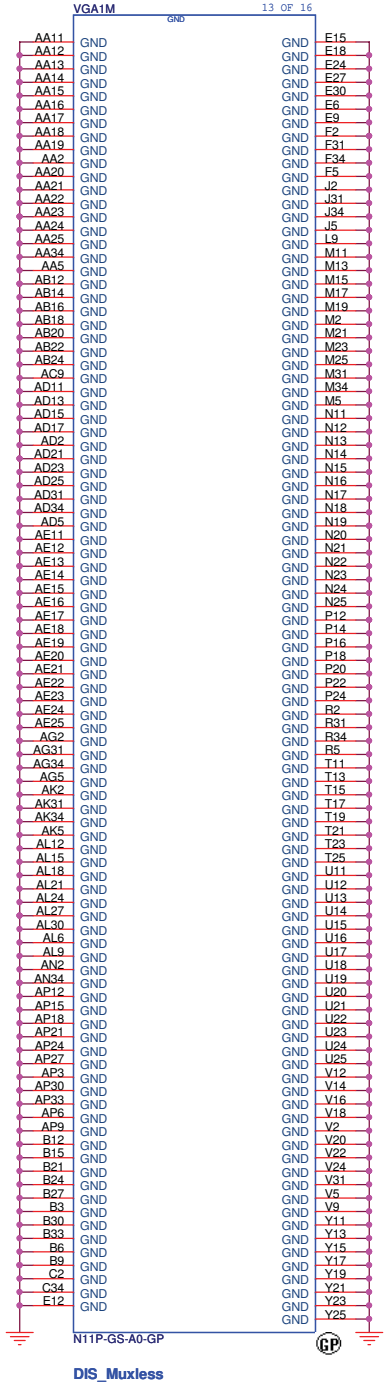
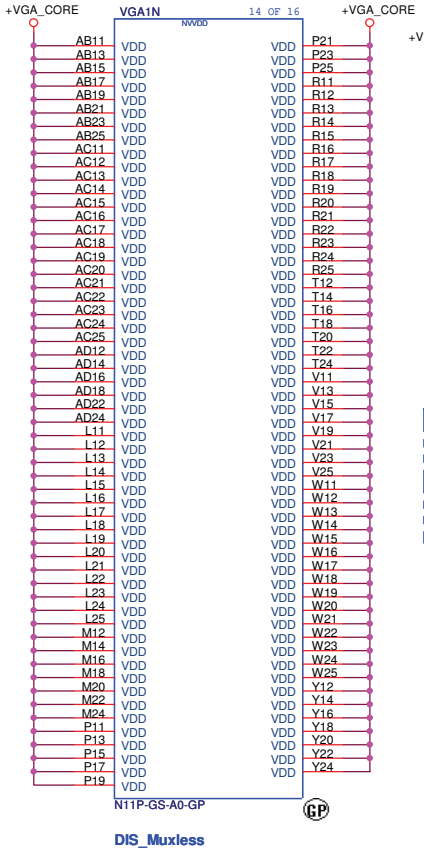


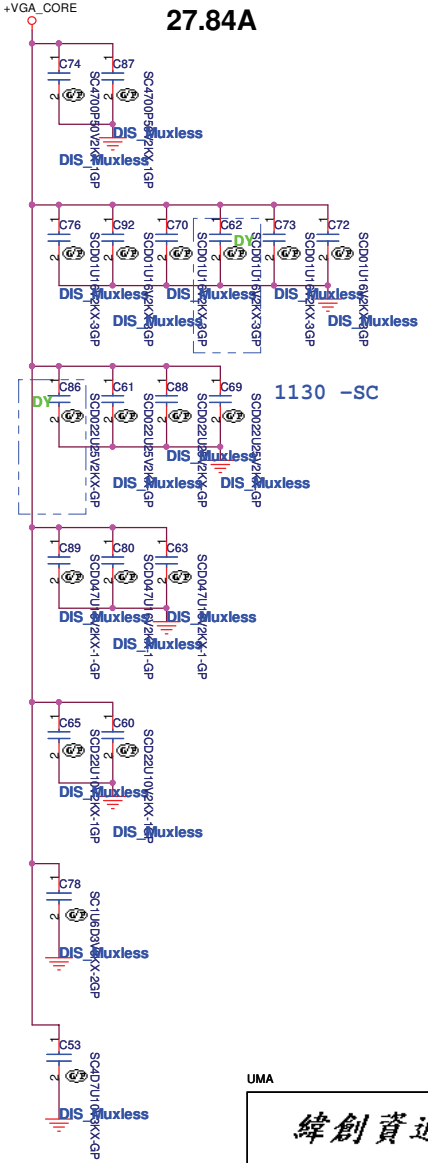


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N11P(5/6)_MIO/ GPIO*		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 66 of 72	







UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N11P(6/6)_POWER*		
Size: A3	Document Number: HM42-CP	Rev: SC
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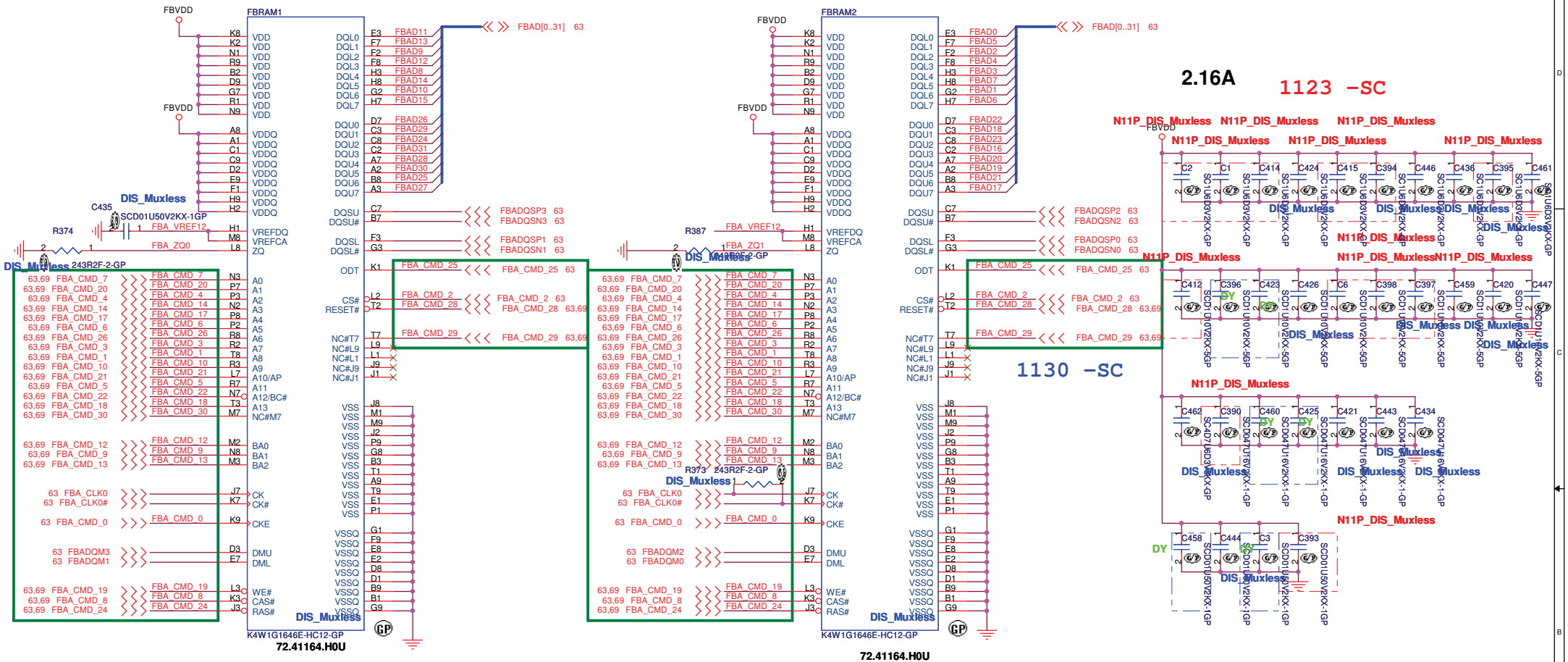
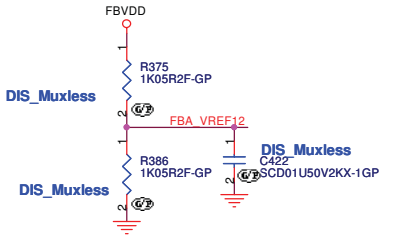
DDR3



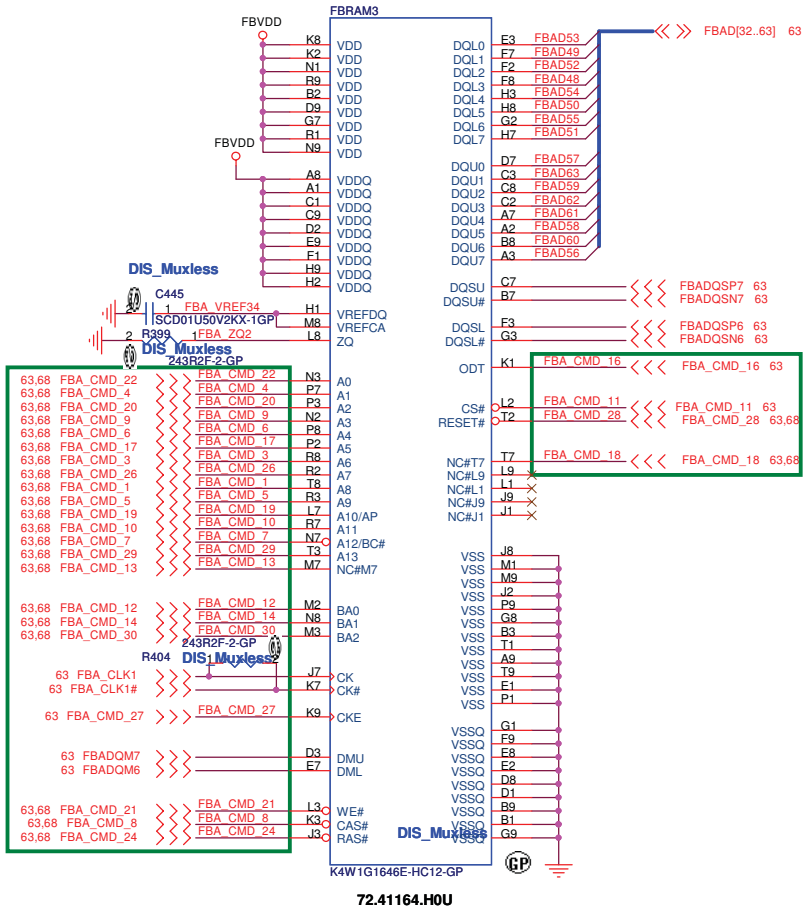
SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)

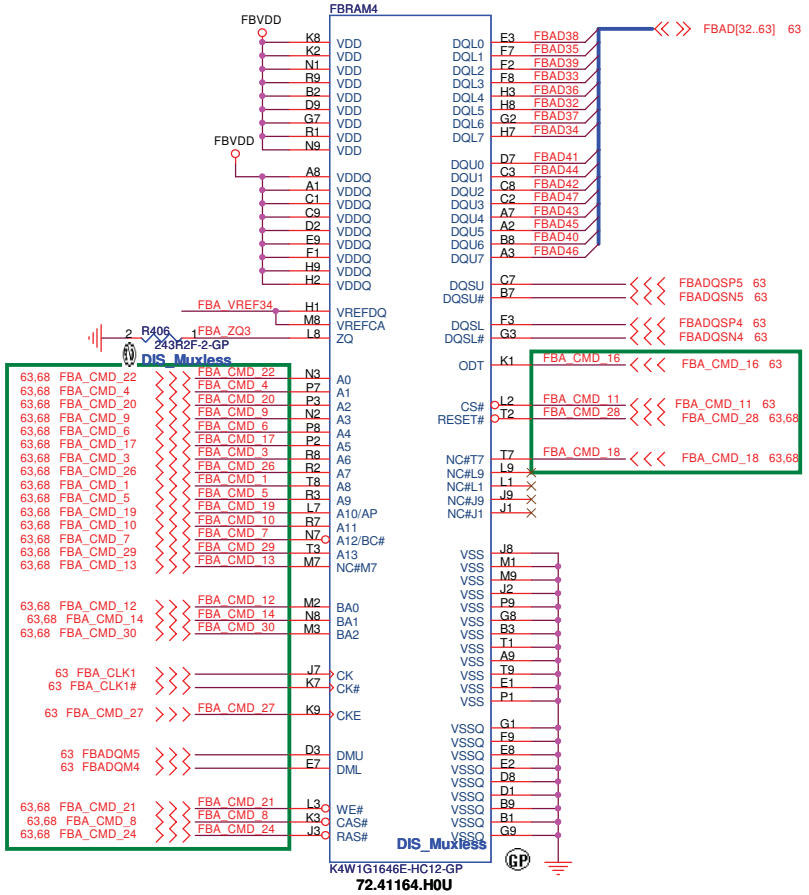


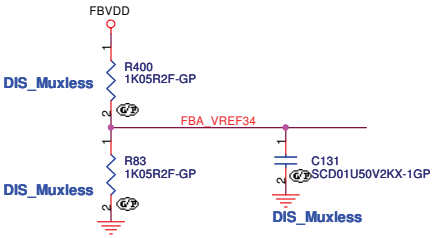
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(1/4)		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 68 of 72	

DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

HM42-CP

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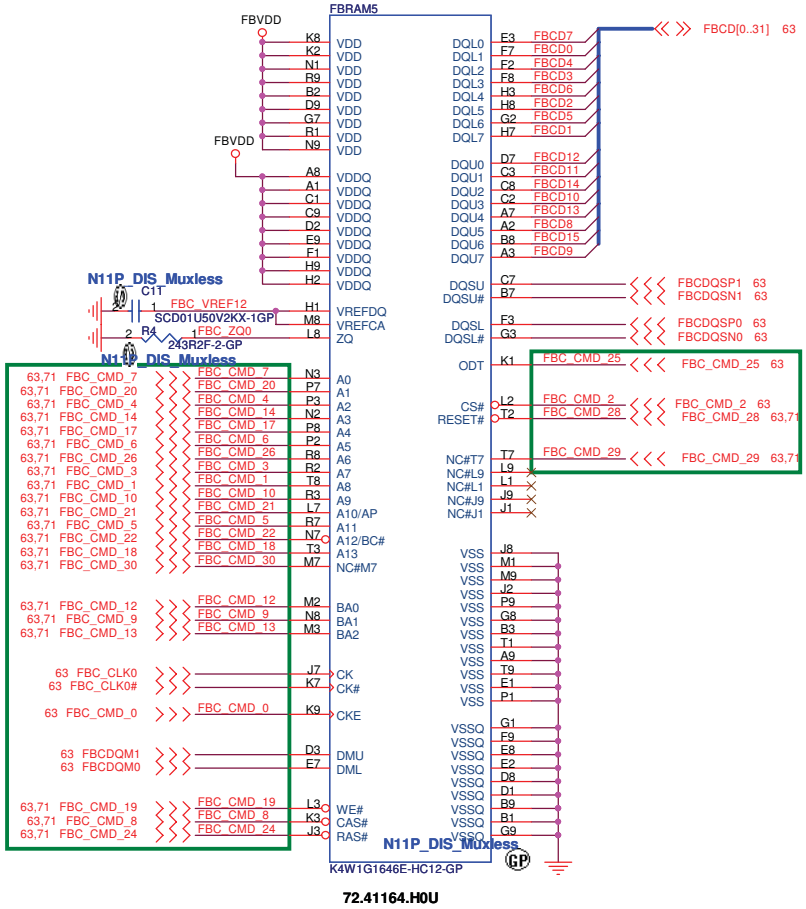
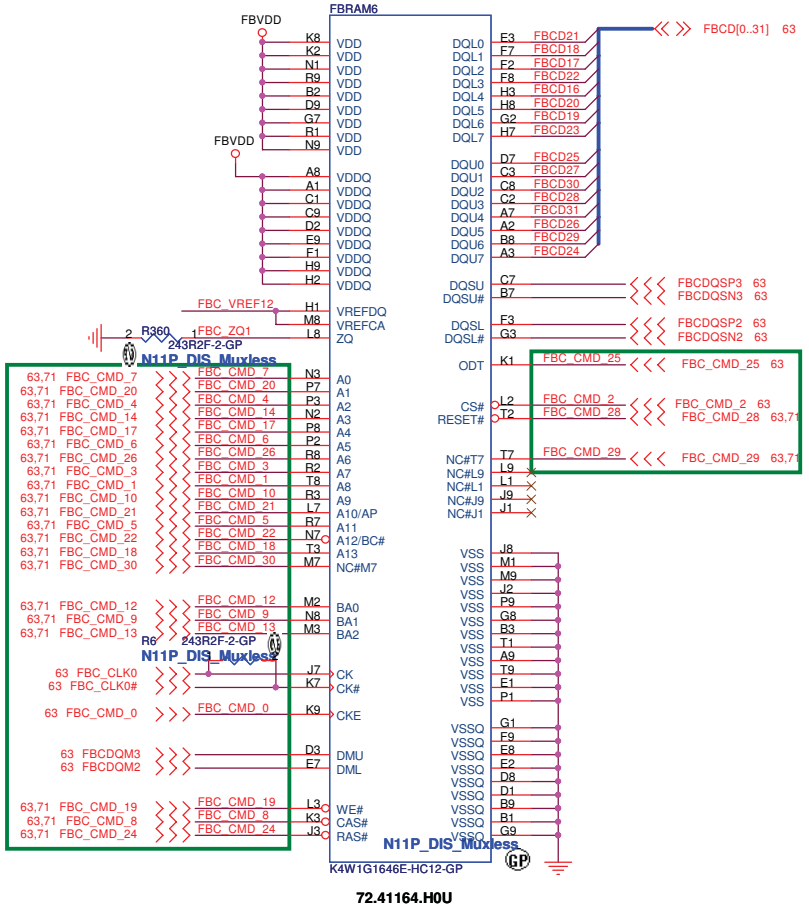
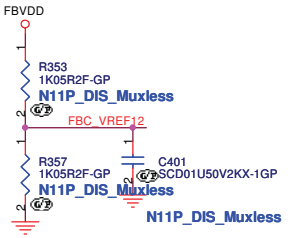
Title		
VRAM(2/4)		
Size: A3	Document Number: **HM42-CP**	Rev: SC
Date: Friday, January 22, 2010	Sheet 69 of 72	

DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



HM42-CP

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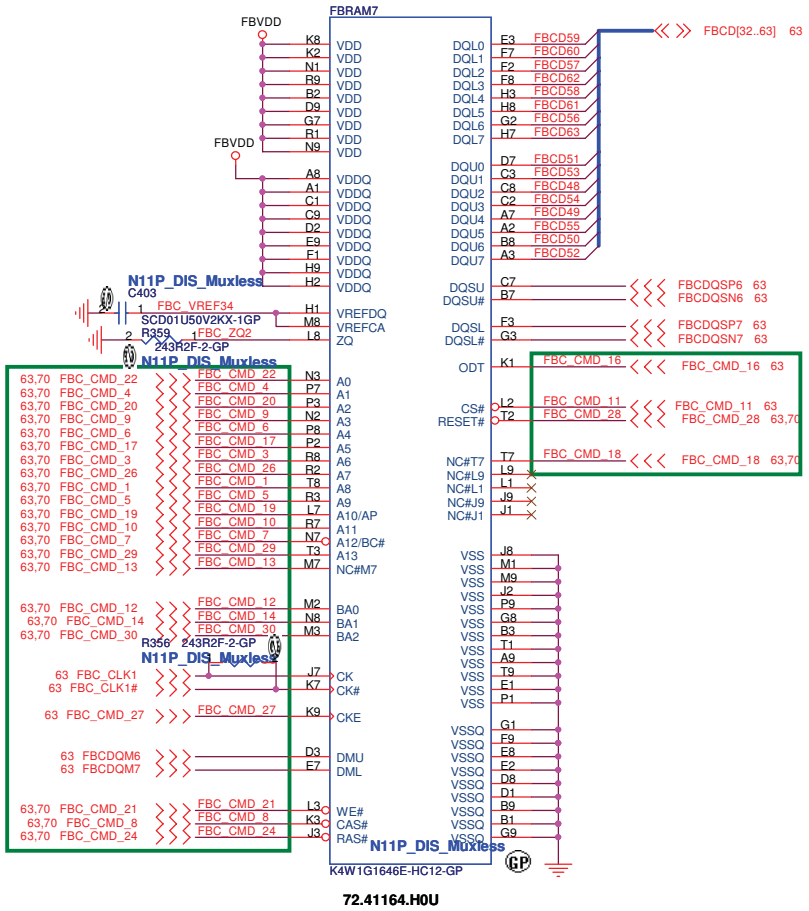
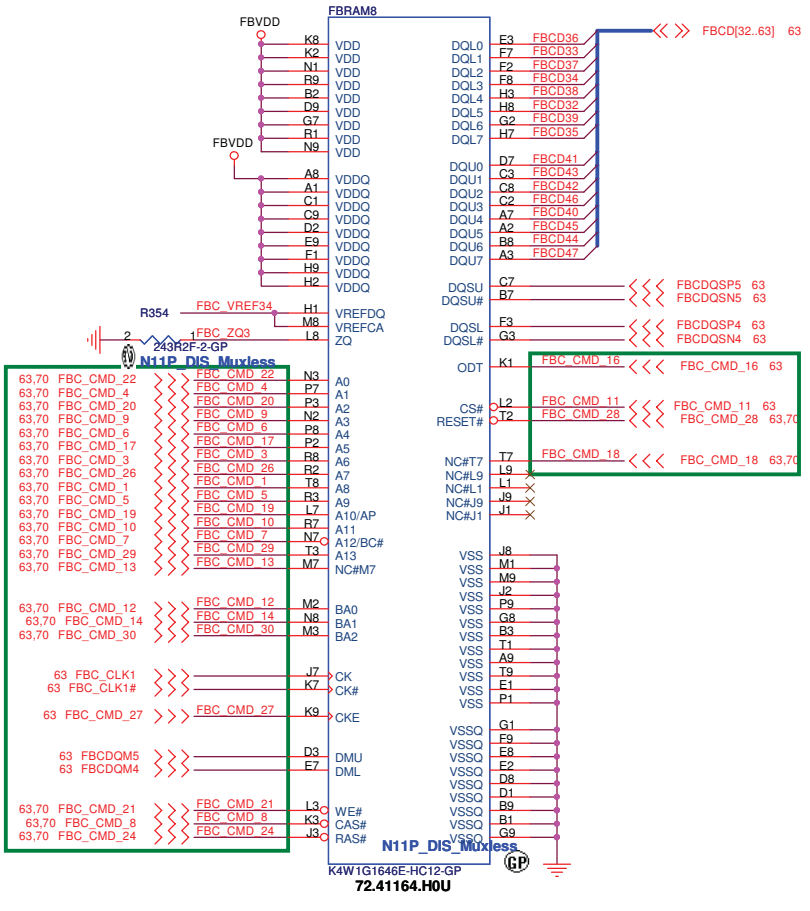
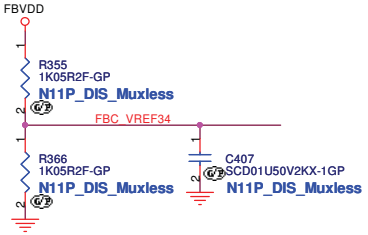
Title: VRAM(3/4)		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 70 of 72	

DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4/4)***

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A3	HM42-CP	SC

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)

1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)
Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st
Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd
UMA Non 3G (55.4GY01.M04G)
Diserete N11M Hynix_3G(55.4GY01.M05G)
Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st
Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)
qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd
qual RTC1 4th source
qual BT1 2nd and 3 source

[Old]
PCH1 PN : 71.0IBEX.A0U
[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

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