GA-M68M-S2P

P-Code:U96133-0

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01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR CONTROL & DEBUG
07	PROCESSOR Power & Gnd
08	DIMM 1,2
09	DIMM TERMINATION
10	DDRII POWER
11	MCP61-CPU
12	MCP61-PCIe
13	MCP61-DAC, RGMII
14	MCP61-PCI
15	MCP61-SATA, IDE
16	MCP61-USB, HD-Audio, GPIO
17	MCP61-Power, Gnd
18	PCI EXPRESS x16, x1 SLOT
19	PCI 1,2,SLOT
20	ITE 8718GB/HX
21	Realtek 8201 CL
22	H/W MONITOR & FAN CONTROL
23	IDE,FDD,COM,LPT
24	F_USB, R_USB
25	ALC888B HD-AUDIO

SHEET	TITLE
26	AUDIO JACK, L_OUT, F_AUDIO
27	ATX, VCC12_DUAL, VDDA25 F_PANEL POWER SEQ
28	PWM ISL6324

Revision: 1.01

<OrgAddr1>

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M68M-S2P | Rev: 1.01

Date: Tuesday, November 10, 2009 | Sheet 1 of 28

Model Name:GA-M68M-S2P Rev.1.01

Component value change history

P-Code: U96133-0

Date	Change Item		Reason
2009.08.05	1.0A E_BOM issue	PCB:1.0	Copy from M61PME-S2P 1.0H BOM, only change NB chipset.
2009.10.20	1.0A E_BOM issue	PCB:1.0	change back to W83303+W83320
2009.11.10	1.01A E_BOM issue	PCB:1.01	MP-BOM

Circuit or PCB layout change for next version

Date	Change Item	Reason
2009.10.??	1.0 Gerber Out	Modify from M68M-S2 1.3 EUP version.

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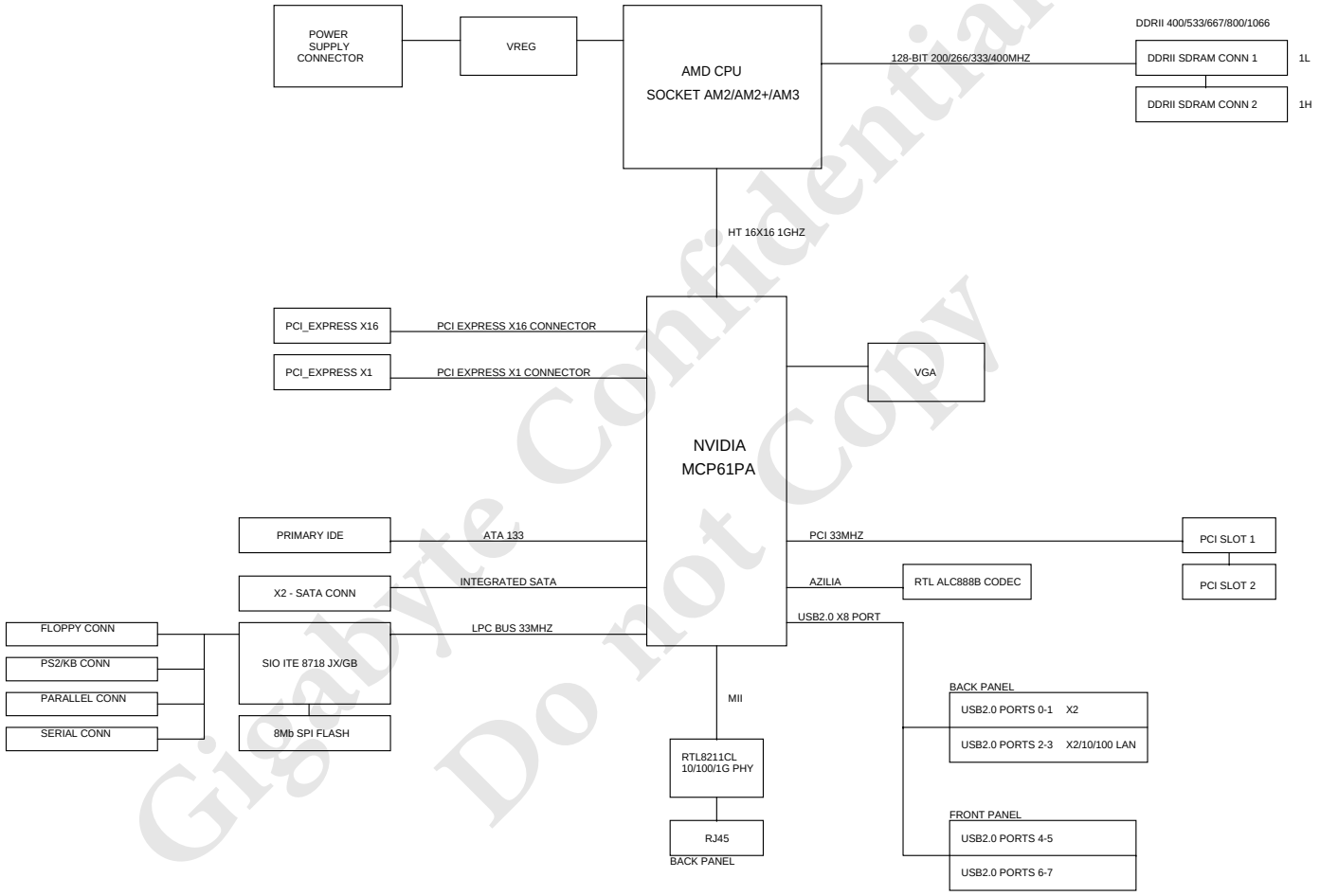
Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M68M-S2P | Rev: 1.01

Date: Wednesday, November 11, 2009 | Sheet 2 of 28

BLOCK DIAGRAM



<OrgAddr1>	GIGABYTE	
Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

VCC12_HT
R3 49.9/4/1
R4 49.9/4/1
GND

<11> L0_CTLIN_H0
<11> L0_CTLIN_L0

L0_CTLOUT_H0 <11>
L0_CTLOUT_L0 <11>

TP78
TP79

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1
	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1
L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0
L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-11R]

<OrgAddr1>

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Title: CPU HYPER TRANSPORT

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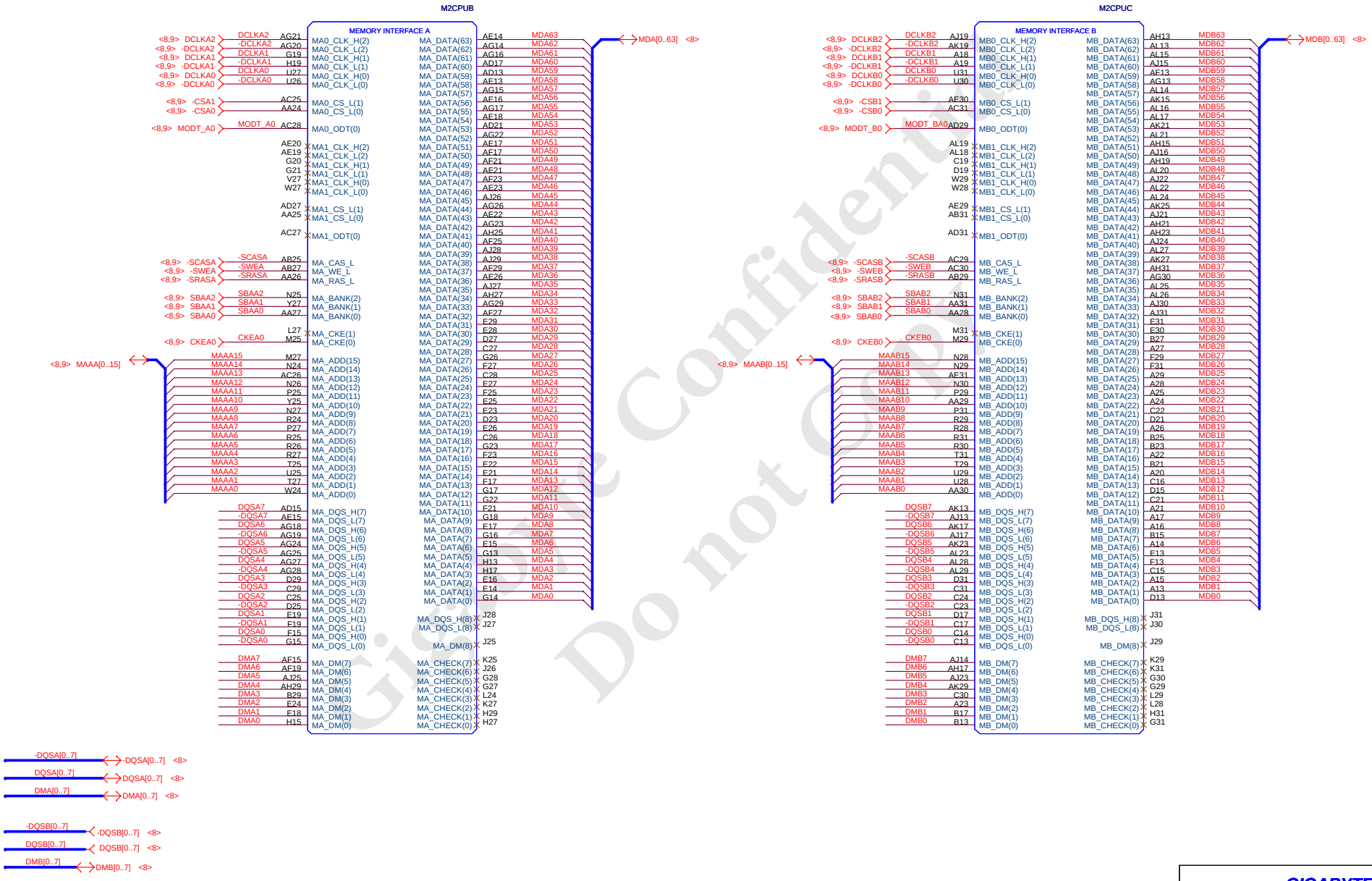

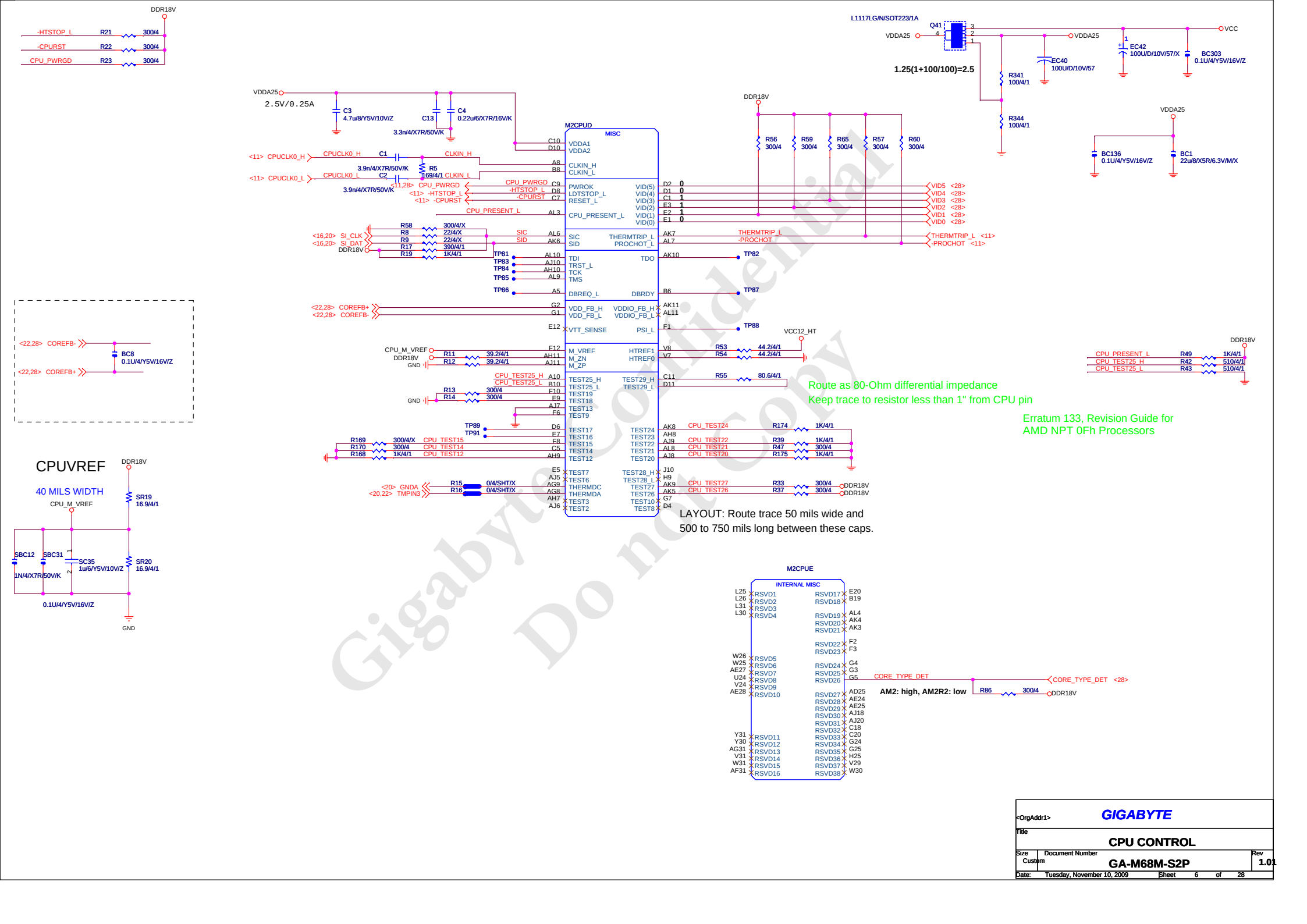
DDR18V
-HTSTOP_L R21 300/4
-CPURST R22 300/4
CPU_PWRGD R23 300/4
L1117LG/N/SOT223/1A
Q41
VDDA25
VCC
1.25(1+100/100)=2.5
R341 100/4/1
R344 100/4/1
EC40 100U/D/10V/57
EC42 100U/D/10V/57/X
BC303 0.1U/4/Y5V/16V/Z
BC136 0.1U/4/Y5V/16V/Z
BC1 22u/8/X5R/6.3V/M/X
2.5V/0.25A
C3 4.7u/8/Y5V/10V/Z
C13 3.3n/4/X7R/50V/K
C4 0.22u/6/X7R/16V/K
M2CPUD
MISC
R56 300/4
R59 300/4
R65 300/4
R57 300/4
R60 300/4
CPUCLK0_H C1 3.9n/4/X7R/50V/K CLKIN_H
CPUCLK0_L C2 3.9n/4/X7R/50V/K R5 169/4/1 CLKIN_L
CPU_PWRGD
-HTSTOP_L
-CPURST
CPU_PRESENT_L
SIC
SID
THERMTRIP_L
-PROCHOT
TDI
TDO
TRST_L
TCK
TMS
DBREQ_L
DBRDY
COREFB+
COREFB-
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VTT_SENSE
PSI_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
R58 300/4/X
R8 22/4/X
R9 22/4/X
R17 390/4/1
R19 1K/4/1
TP81
TP83
TP84
TP85
TP86
TP82
TP87
TP88
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
R11 39.2/4/1
R12 39.2/4/1
R53 44.2/4/1
R54 44.2/4/1
R55 80.6/4/1
VCC12_HT
CPU_TEST25_H
CPU_TEST25_L
TEST25_H
TEST25_L
TEST29_H
TEST29_L
R13 300/4
R14 300/4
TP89
TP91
R169 300/4/X
R170 300/4
R168 1K/4/1
CPU_TEST15
CPU_TEST14
CPU_TEST12
CPU_TEST24
CPU_TEST22
CPU_TEST21
CPU_TEST20
R174 1K/4/1
R39 1K/4/1
R47 300/4
R175 1K/4/1
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
R15 0/4/SHT/X
R16 0/4/SHT/X
GNDA
TMPIN3
R33 300/4
R37 300/4
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
CPU_PRESENT_L R49 1K/4/1
CPU_TEST25_H R42 510/4/1
CPU_TEST25_L R43 510/4/1
BC8 0.1U/4/Y5V/16V/Z
CPUVREF
40 MILS WIDTH
CPU_M_VREF
SR19 16.9/4/1
SR20 16.9/4/1
SBC12 1N/4/X7R/50V/K
SBC31
SC35 1u/6/Y5V/10V/Z
0.1U/4/Y5V/16V/Z
GND
M2CPUE
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
CORE_TYPE_DET
AM2: high, AM2R2: low
R86 300/4
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CPU CONTROL
GA-M68M-S2P
1.01
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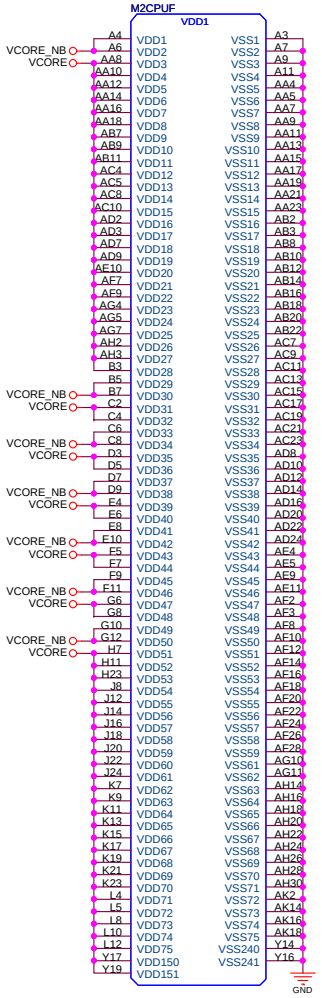
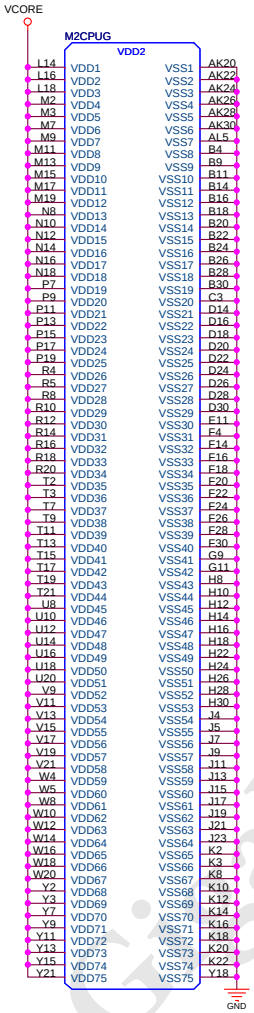
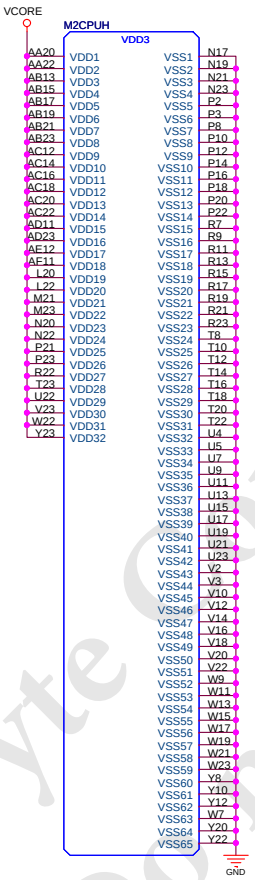
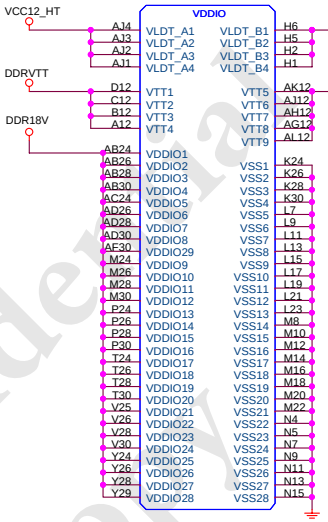
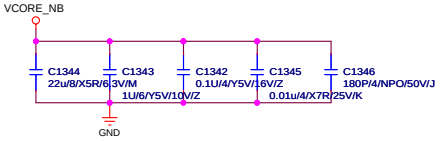
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

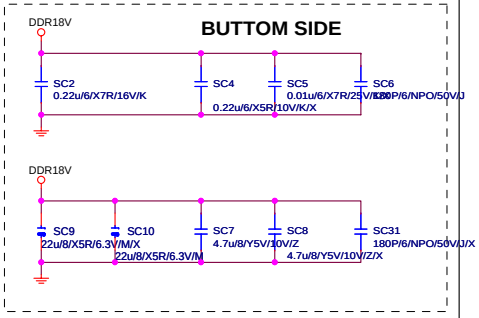


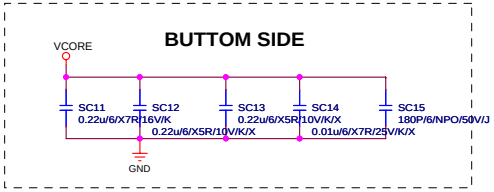


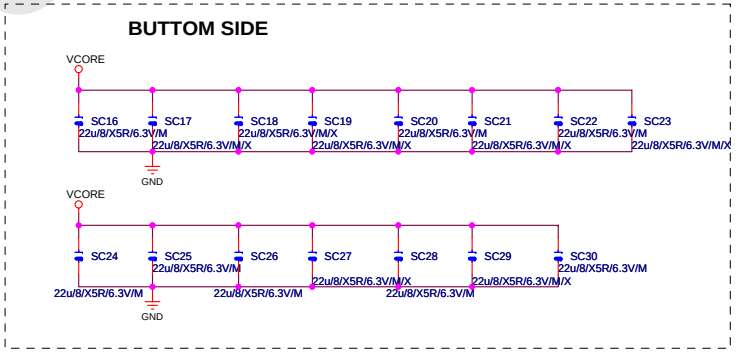


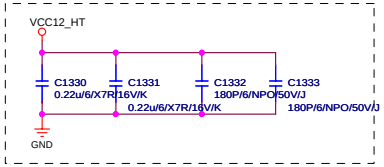


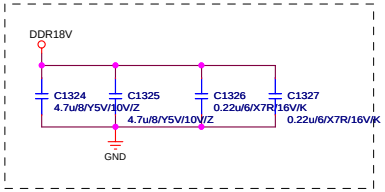


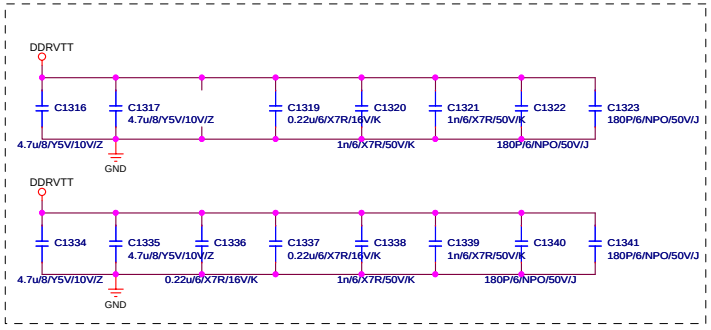












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Title	CPU POWER & GND		
Size: Custom	Document Number: GA-M68M-S2P		Rev: 1.01
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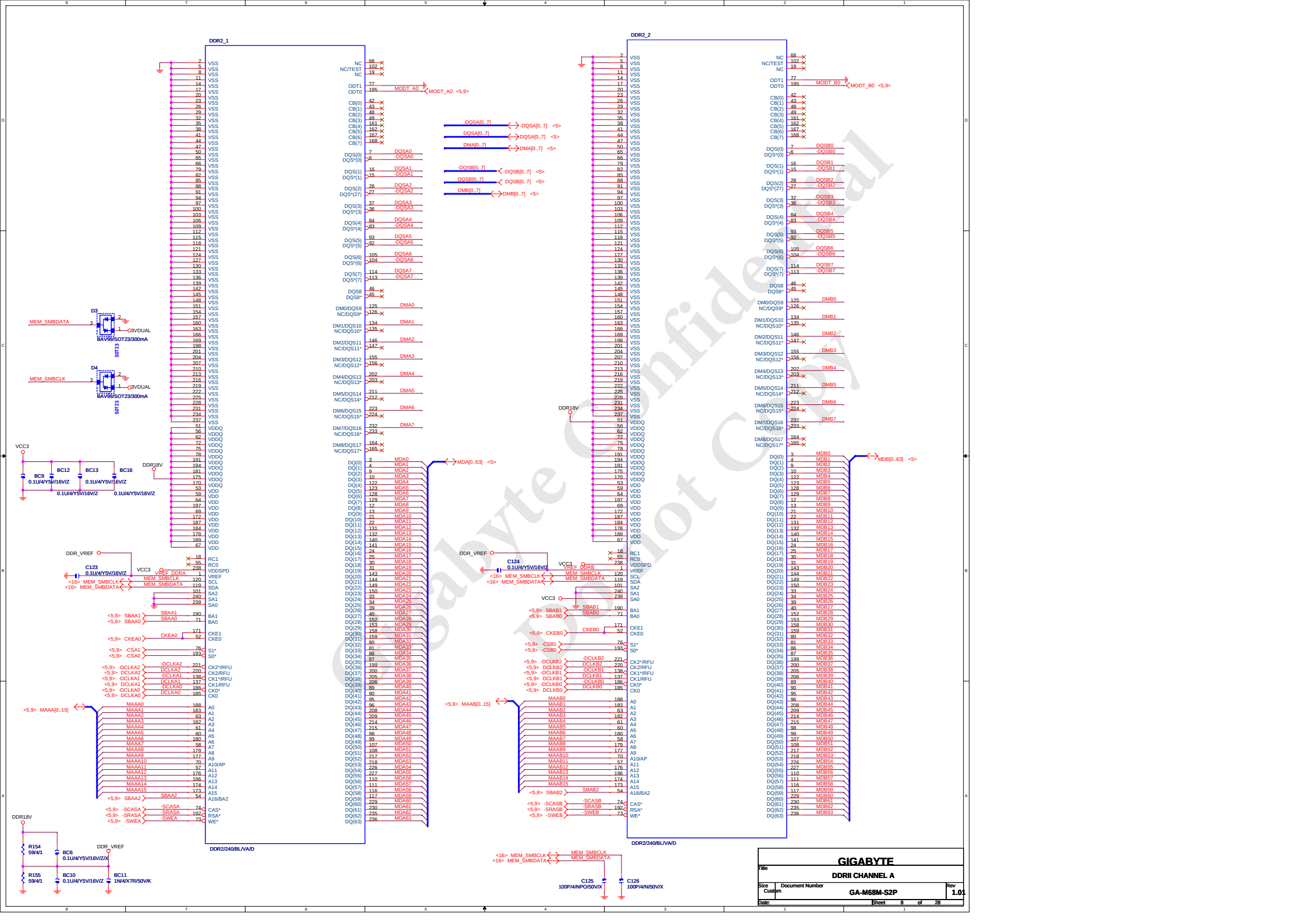
DDR2_1
DDR2_2
DDR2/240/BL/VA/D
DDR2/240/BL/VA/D
MEM_SMBDATA
MEM_SMBCLK
D3
D4
BAV99/SOT23/300mA
3VDUAL
VCC3
DDR18V
DDR_VREF
BC9 0.1U/4/Y5V/16V/Z
BC12
BC13
BC16
C123 0.1U/4/Y5V/16V/Z
C124 0.1U/4/Y5V/16V/Z
C125 100P/4/NPO/50V/X
C126 100P/4/N/50V/X
R154 59/4/1
R155 59/4/1
BC6 0.1U/4/Y5V/16V/Z/X
BC10 0.1U/4/Y5V/16V/Z
BC11 1N/4/X7R/50V/K
MODT_A0
MODT_B0
MDA[0..63]
MDB[0..63]
MAAA[0..15]
MAAB[0..15]
DQSA[0..7]
DQSB[0..7]
DMA[0..7]
DMB[0..7]
GIGABYTE
DDRII CHANNEL A
GA-M68M-S2P
Rev 1.01
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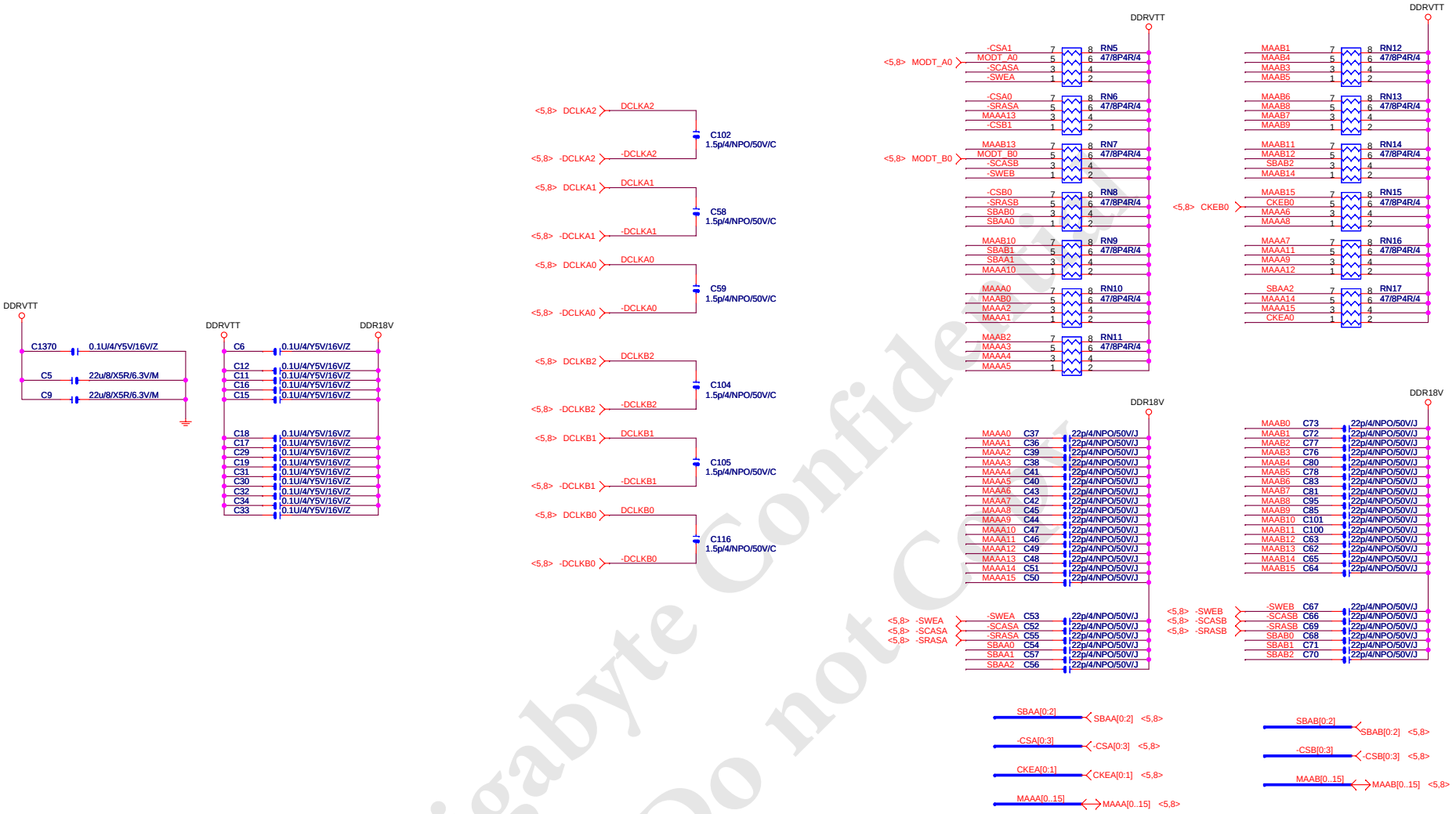
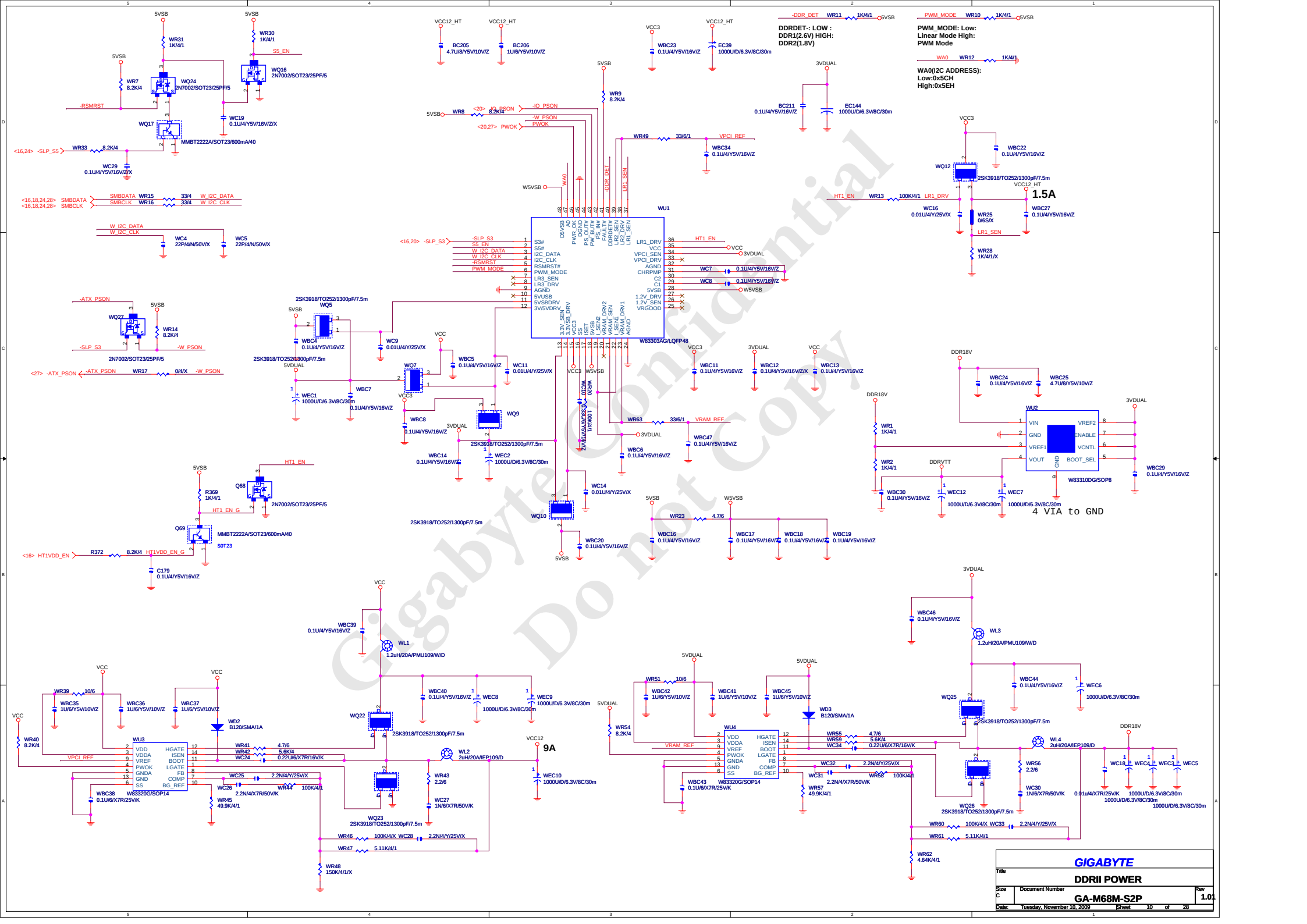


GIGABYTE		
Title	DDRII TERMINATOR	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
Date: Tuesday, November 10, 2009	Sheet 9 of 28	


DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
9A
4 VIA to GND
W83303AG/LQFP48
W83320G/SOP14
W83310DG/SOP8
2N7002/SOT23/25PF/5
MMBT2222A/SOT23/600mA/40
2SK3918/TO252/1300pF/7.5m
B120/SMA/1A
1.2uH/20A/PMU109/W/D
1.2uH/20A/IEP109/D
GIGABYTE
DDRII POWER
GA-M68M-S2P
1.01
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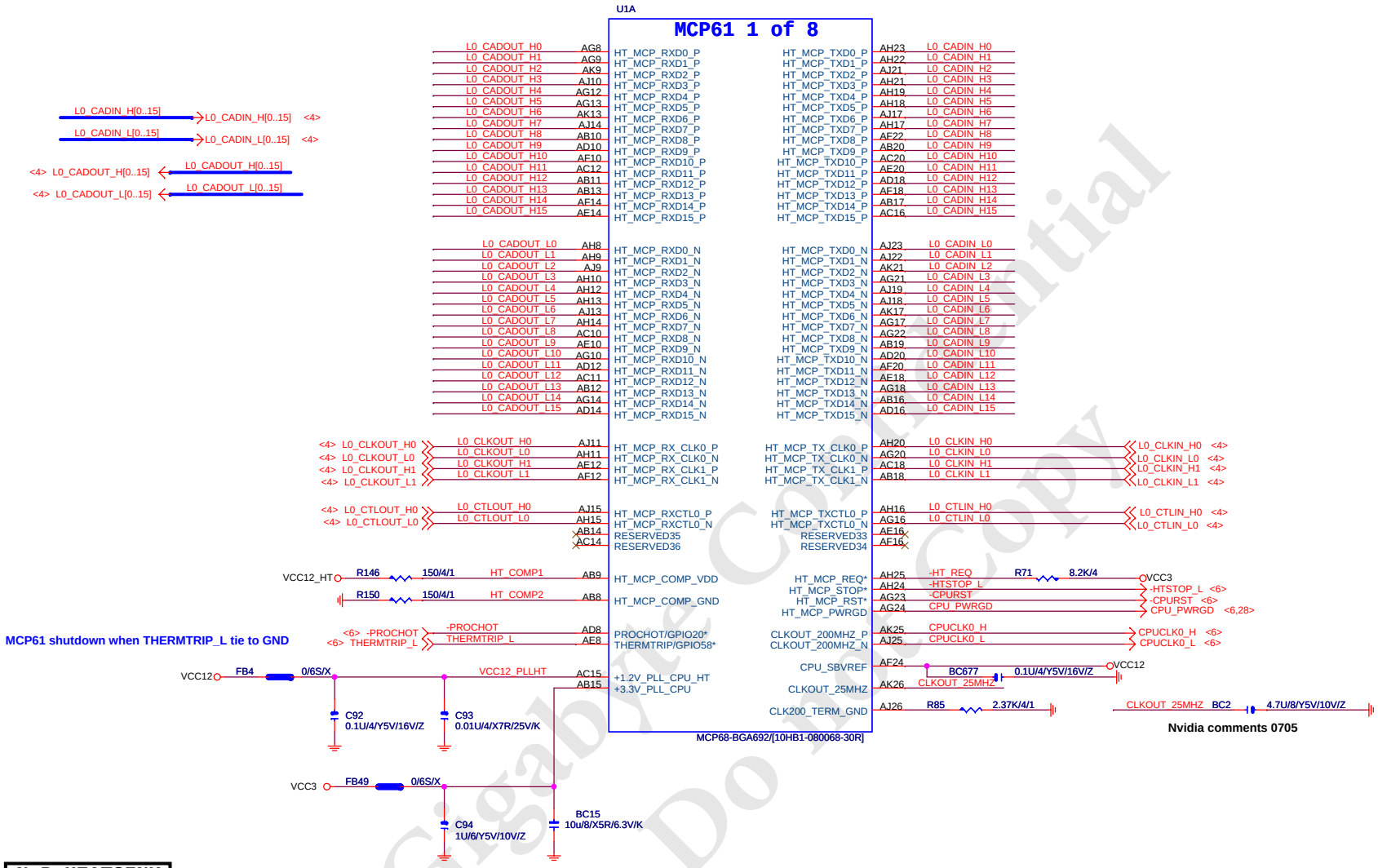
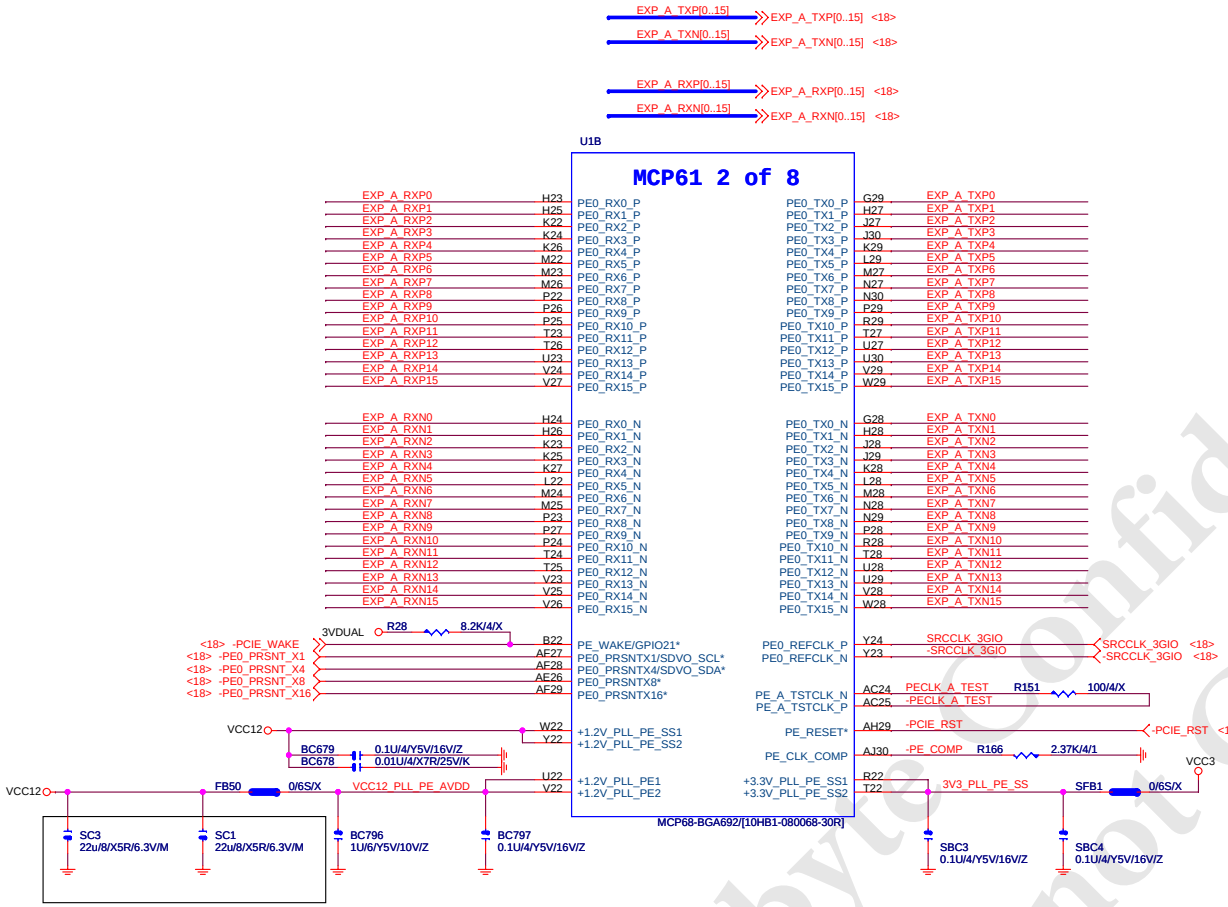


GIGABYTE		
Title	MCP61-HOST	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
Date: Tuesday, November 10, 2009	Sheet 11 of 28	

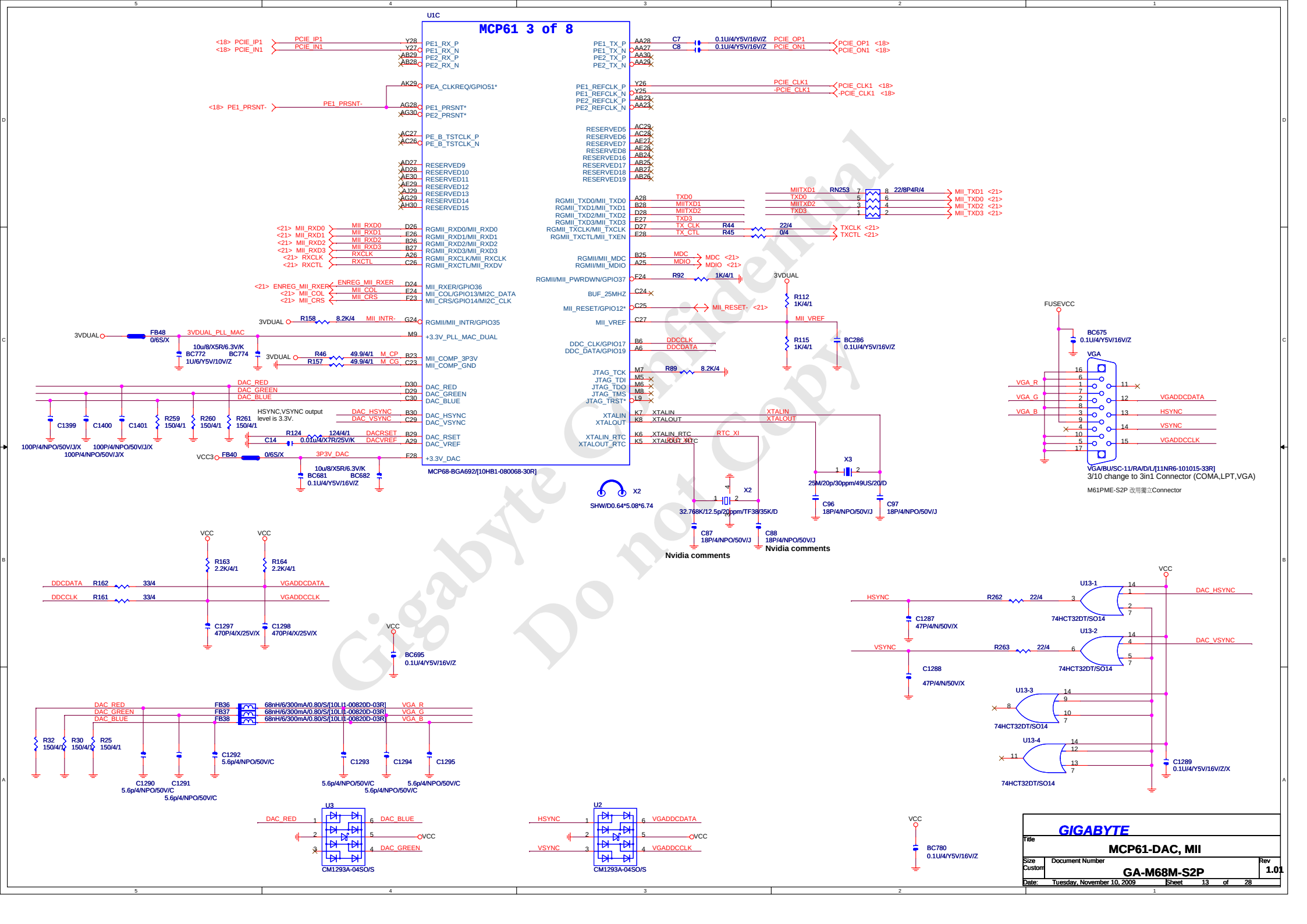


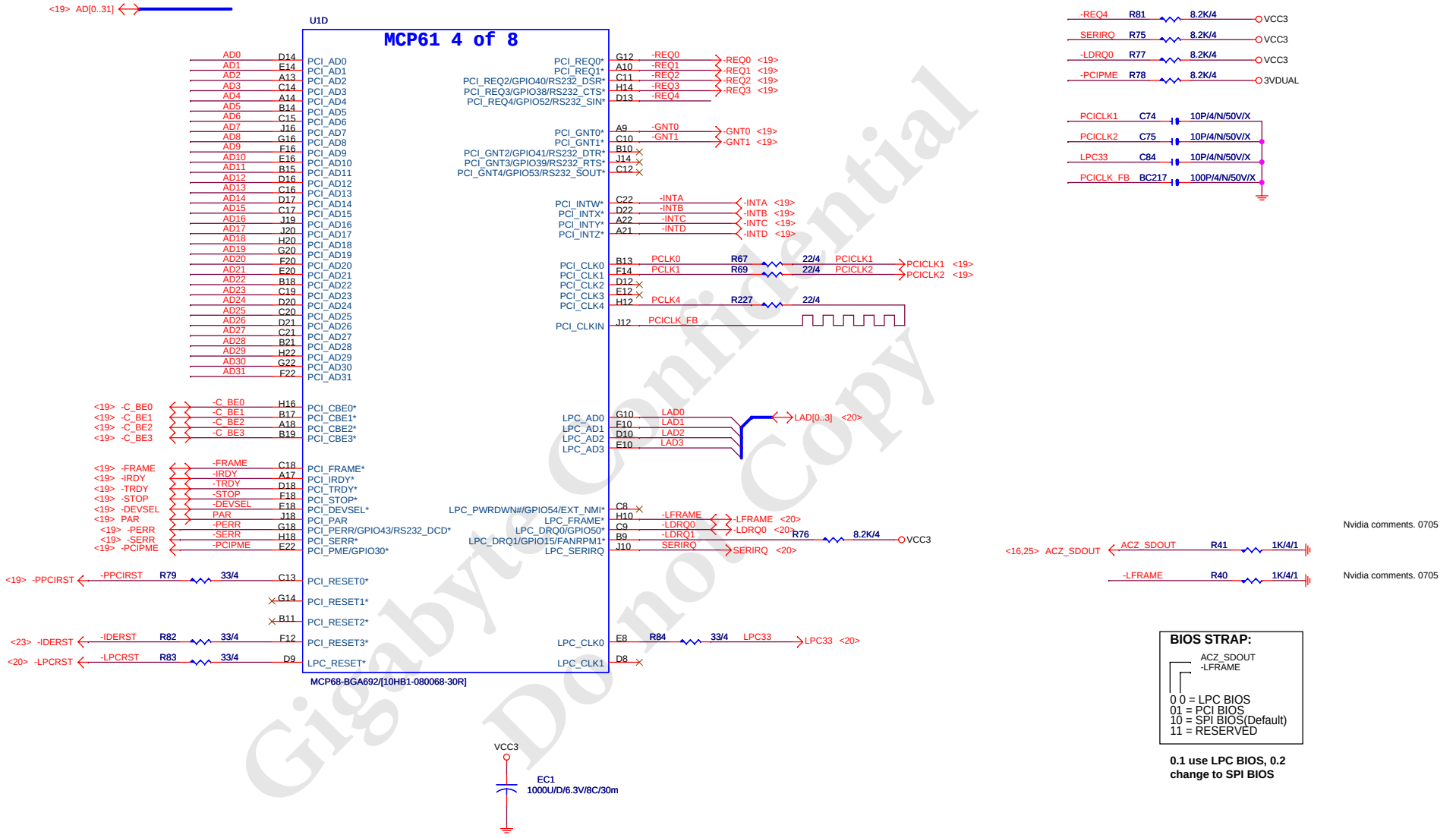
GIGABYTE

Title: MCP61-PCI EXPRESS

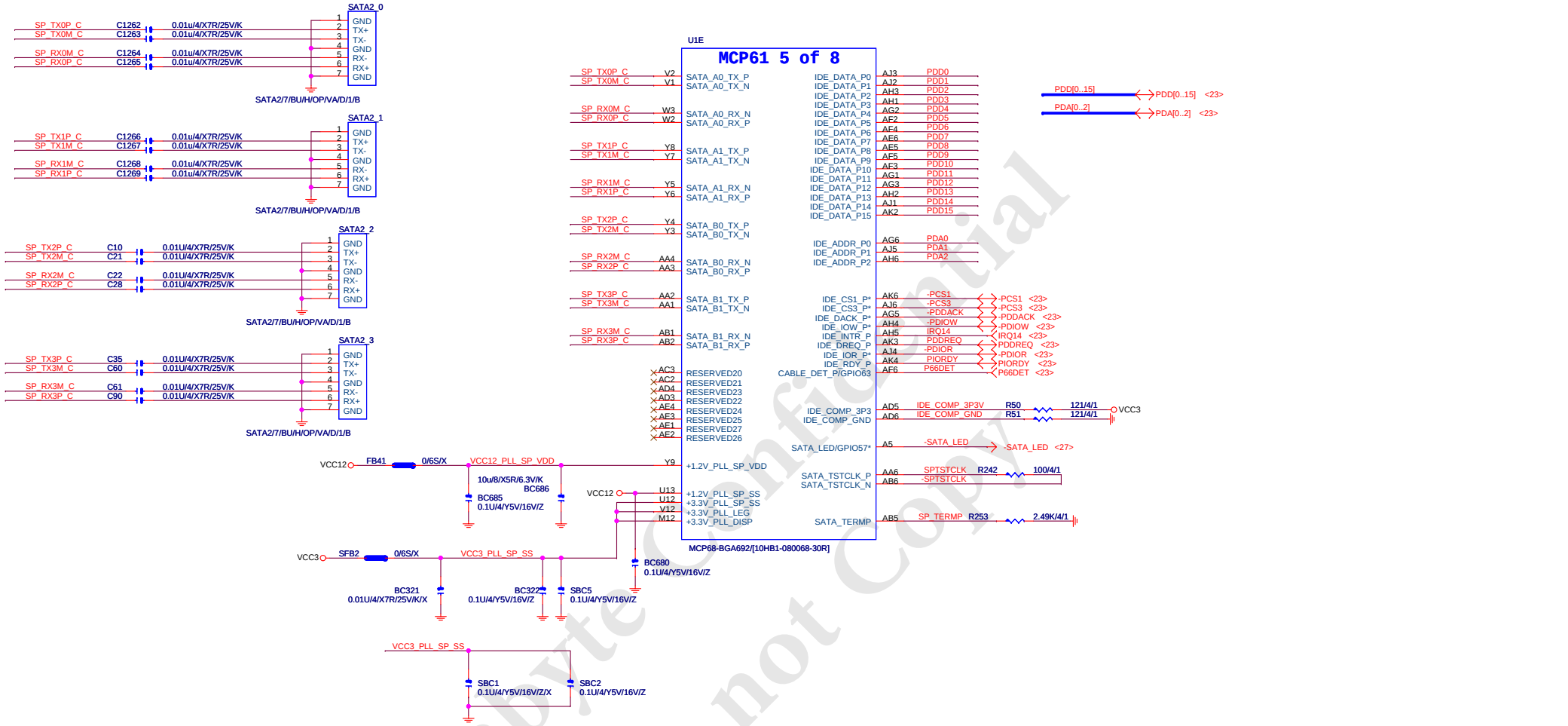
Size: Custom | Document Number: GA-M68M-S2P | Rev: 1.01

Date: Tuesday, November 10, 2009 | Sheet 12 of 28





GIGABYTE		
Title	MCP61-PCI BUS	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
Date: Tuesday, November 10, 2009	Sheet 14 of 28	



GIGABYTE

Title	MCP61-SATA/IDE	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
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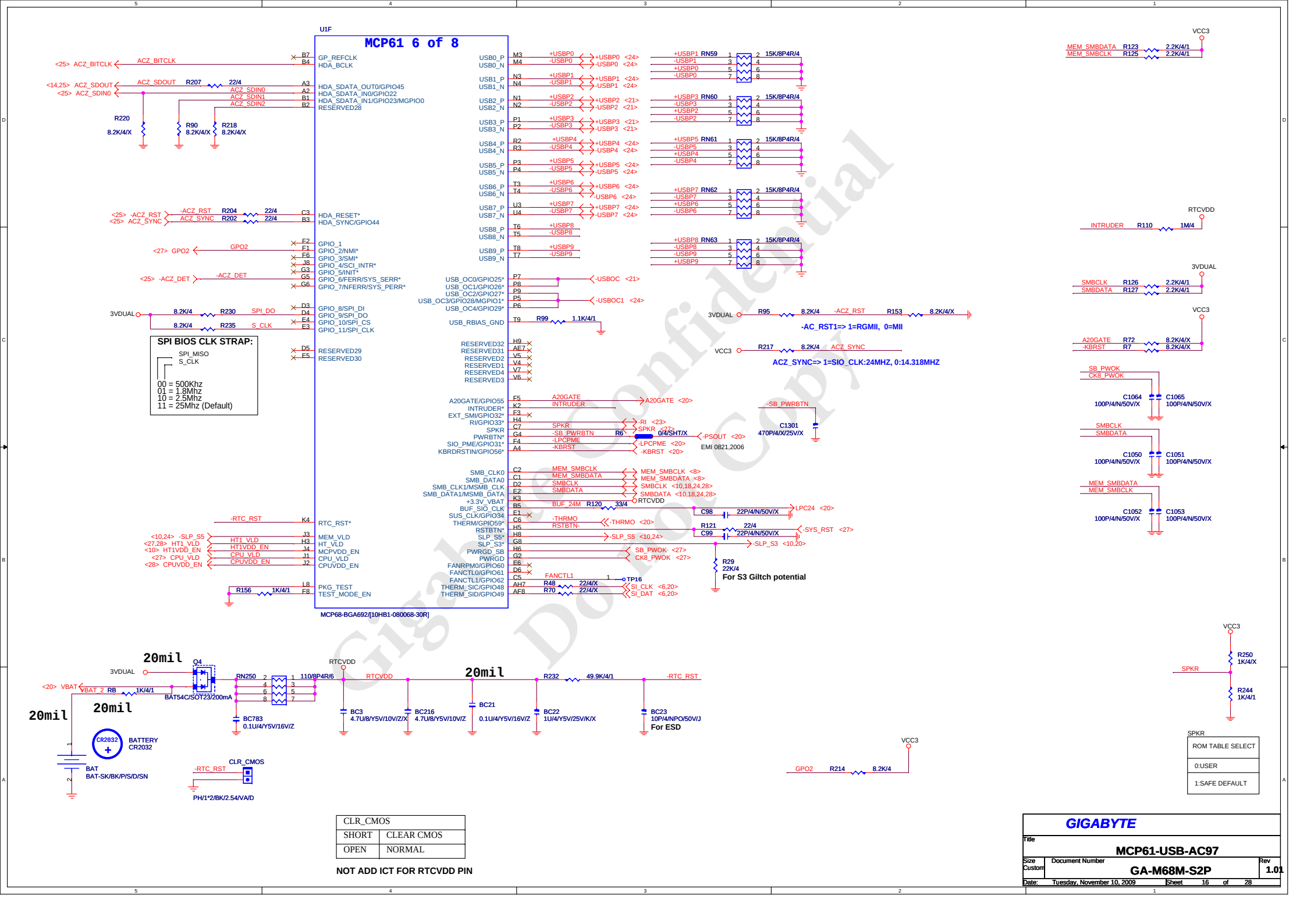
MCP61 6 of 8
U1F
MCP68-BGA692/[10HB1-080068-30R]
SPI BIOS CLK STRAP:
SPI_MISO
S_CLK
00 = 500Khz
01 = 1.8Mhz
10 = 2.5Mhz
11 = 25Mhz (Default)
-AC_RST1=> 1=RGMII, 0=MII
ACZ_SYNC=> 1=SIO_CLK:24MHZ, 0:14.318MHZ
EMI 0821,2006
For S3 Giltch potential
For ESD
BATTERY CR2032
BAT-SK/BK/P/S/D/SN
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SPKR
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
GIGABYTE
MCP61-USB-AC97
GA-M68M-S2P
1.01
Tuesday, November 10, 2009
Sheet 16 of 28
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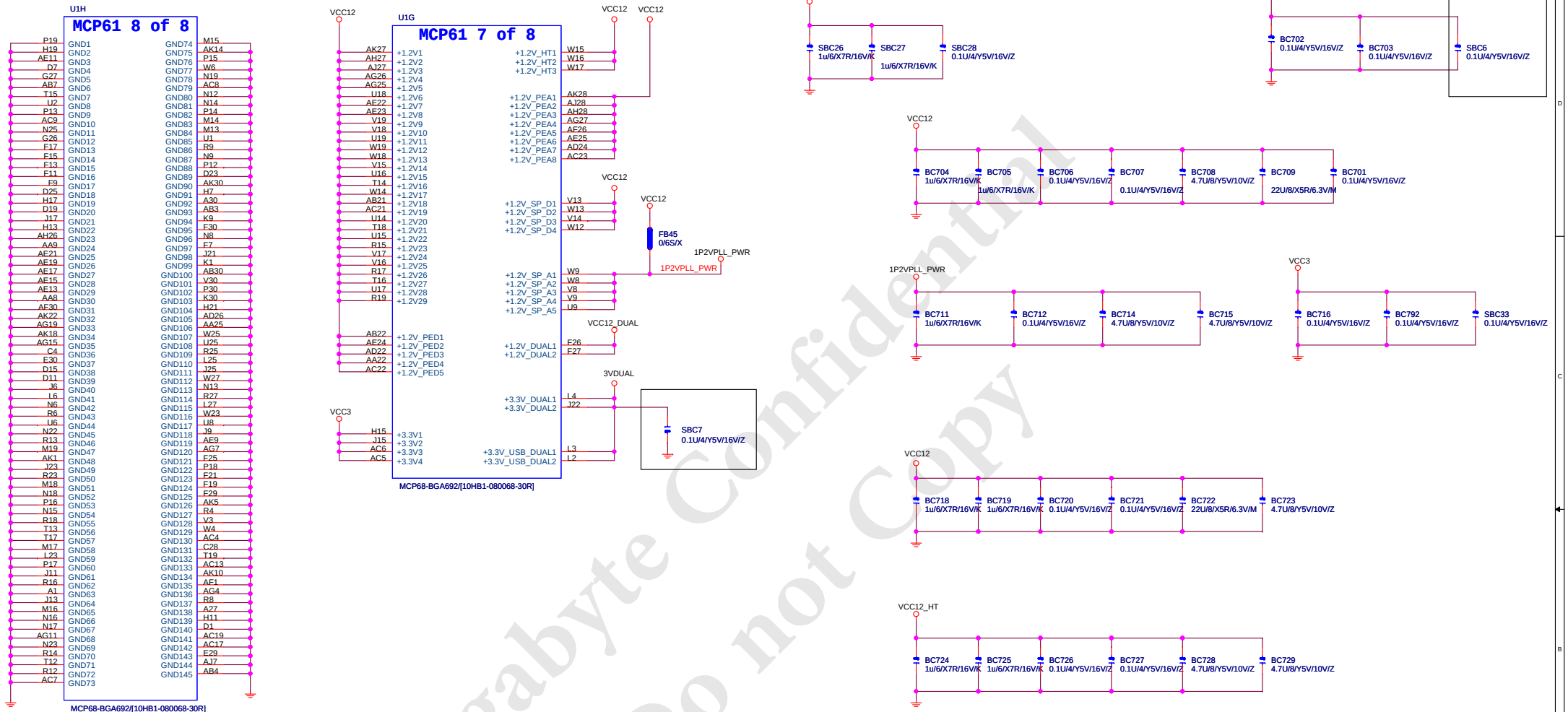

GIGABYTE

Title: MCP61-Power

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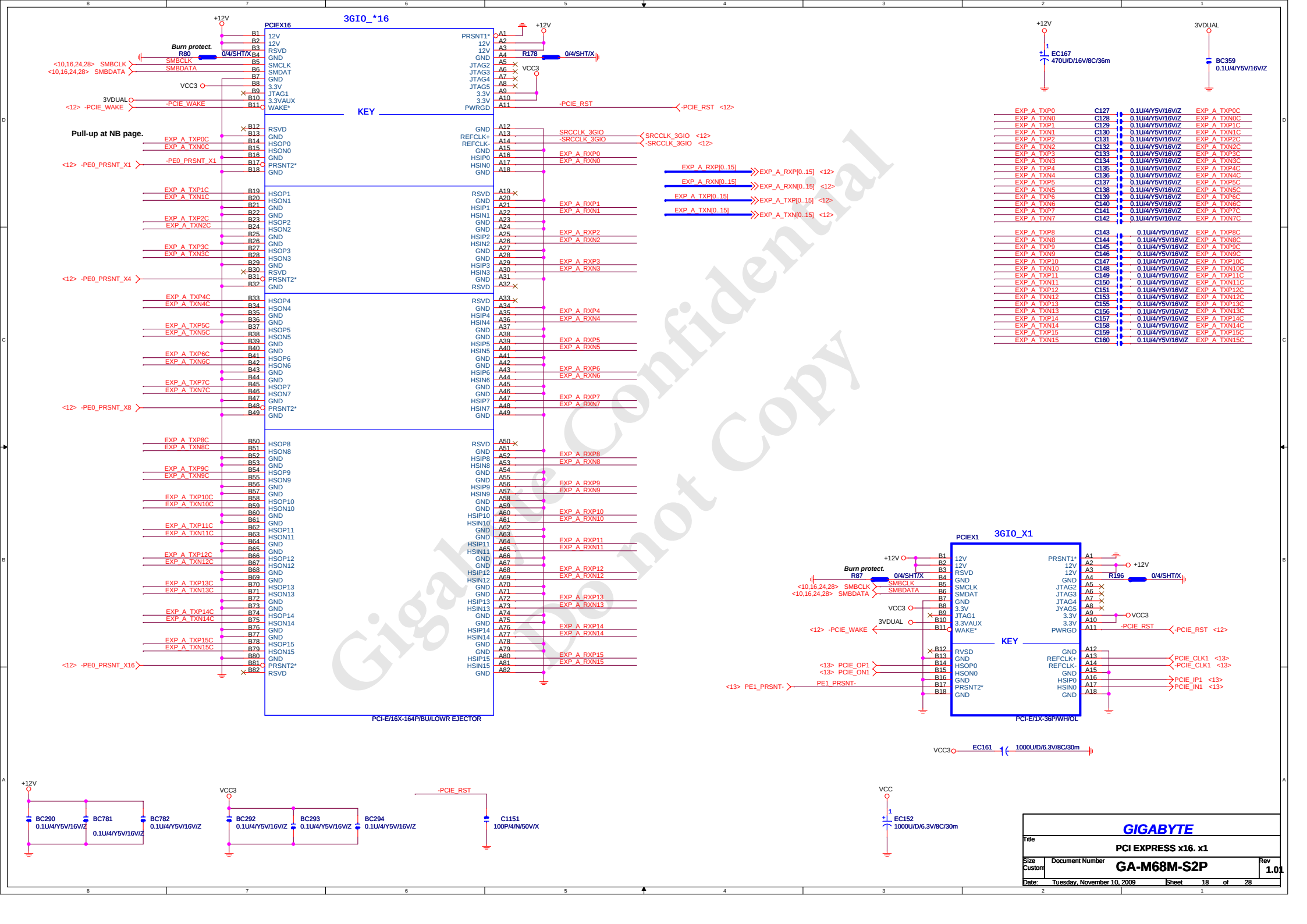
3GIO_*16
PCIEX16
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
3GIO_X1
PCIEX1
PCI-E/1X-36P/WH/OL
Pull-up at NB page.
Burn protect.
R80
R87
R178
R196
0/4/SHT/X
SMBCLK
SMBDATA
-PCIE_WAKE
-PCIE_RST
-PE0_PRSNT_X1
-PE0_PRSNT_X4
-PE0_PRSNT_X8
-PE0_PRSNT_X16
PE1_PRSNT-
PCIE_OP1
PCIE_ON1
SRCCLK_3GIO
-SRCCLK_3GIO
EC167
470U/D/16V/8C/36m
BC359
0.1U/4/Y5V/16V/Z
EC161
1000U/D/6.3V/8C/30m
EC152
1000U/D/6.3V/8C/30m
BC290
BC781
BC782
BC292
BC293
BC294
C1151
100P/4/N/50V/X
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PCI EXPRESS x16. x1
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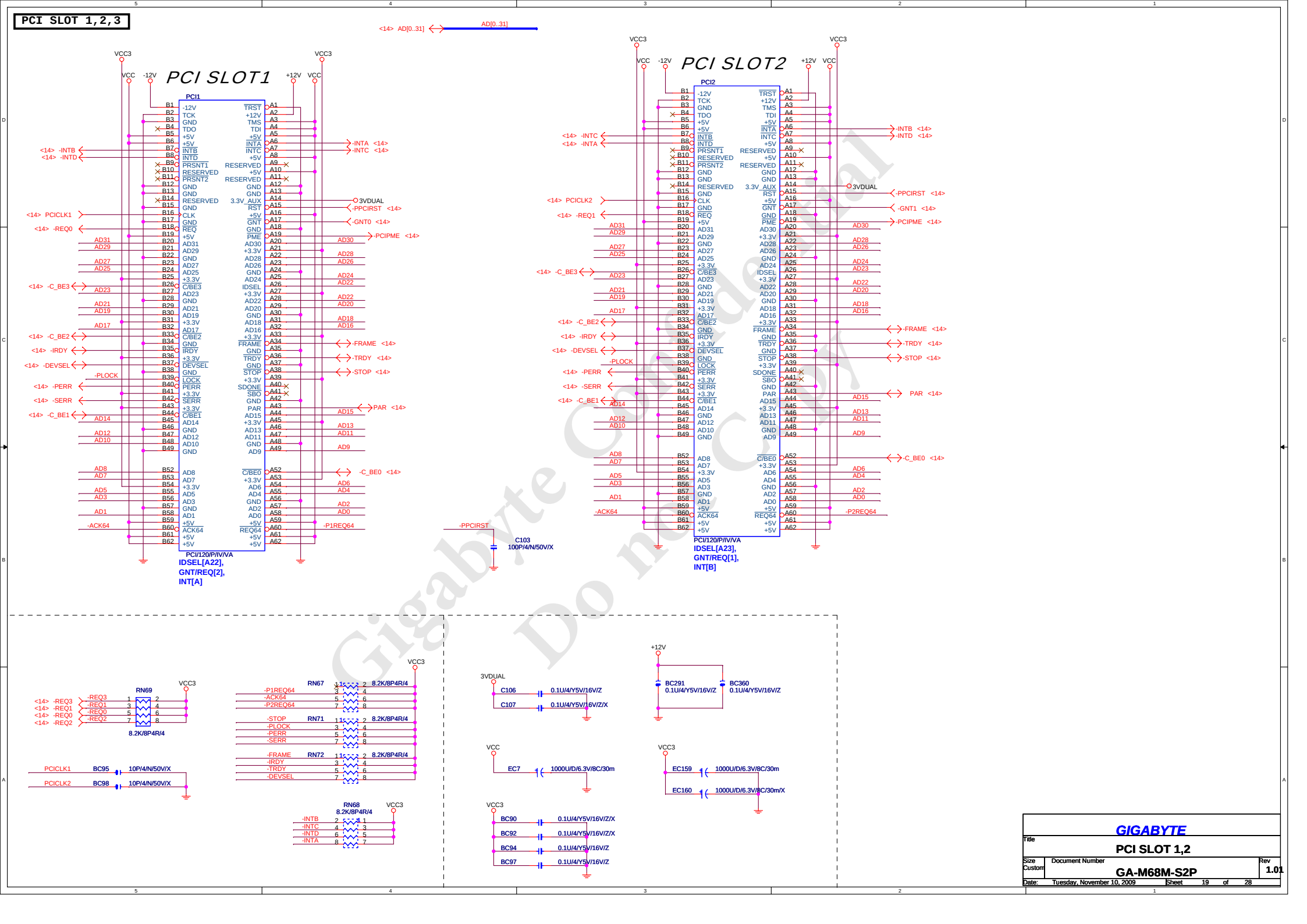
PCI SLOT 1,2,3



GIGABYTE			
Title	PCI SLOT 1,2		
Size: Custom	Document Number: GA-M68M-S2P		Rev: 1.01
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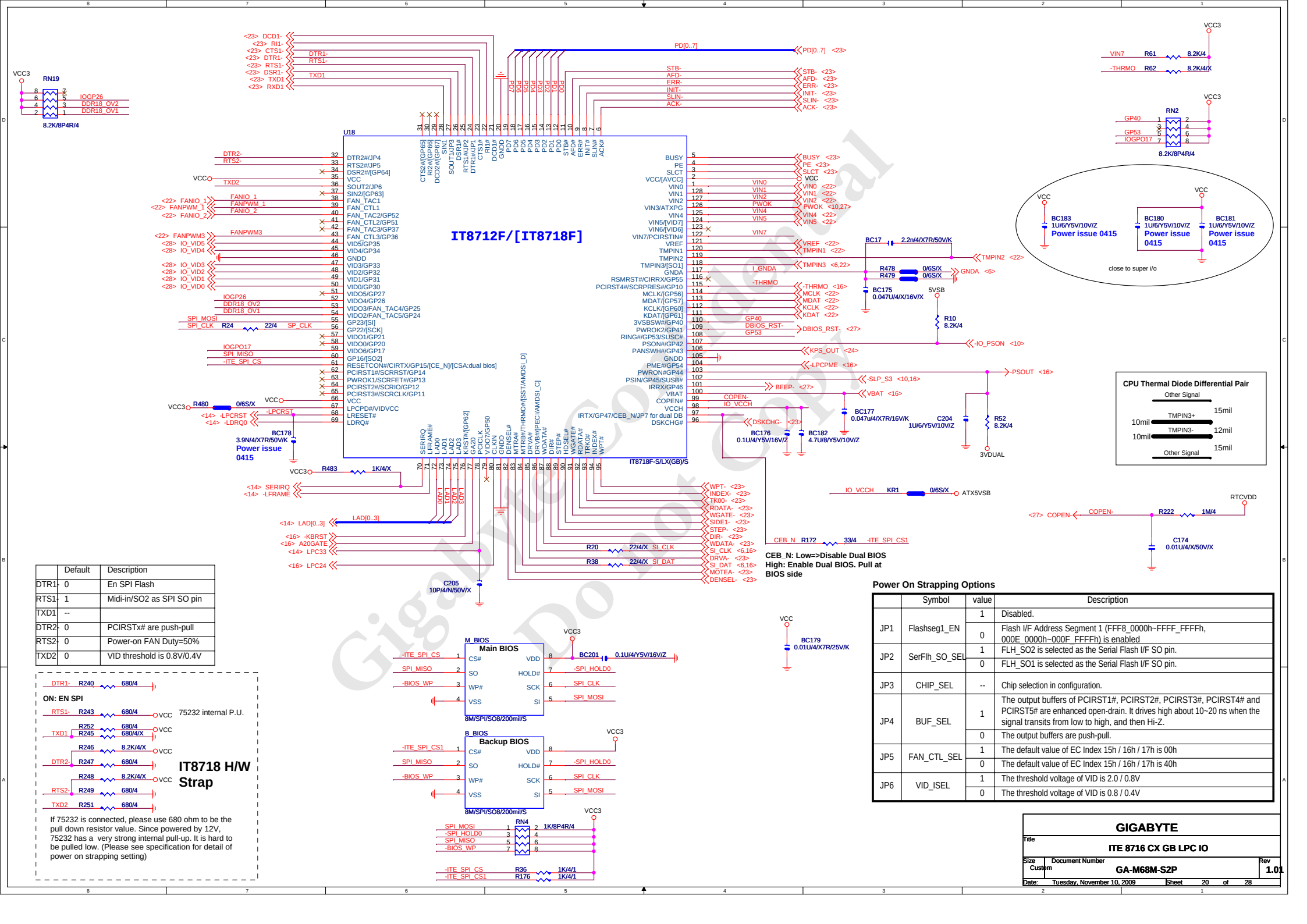
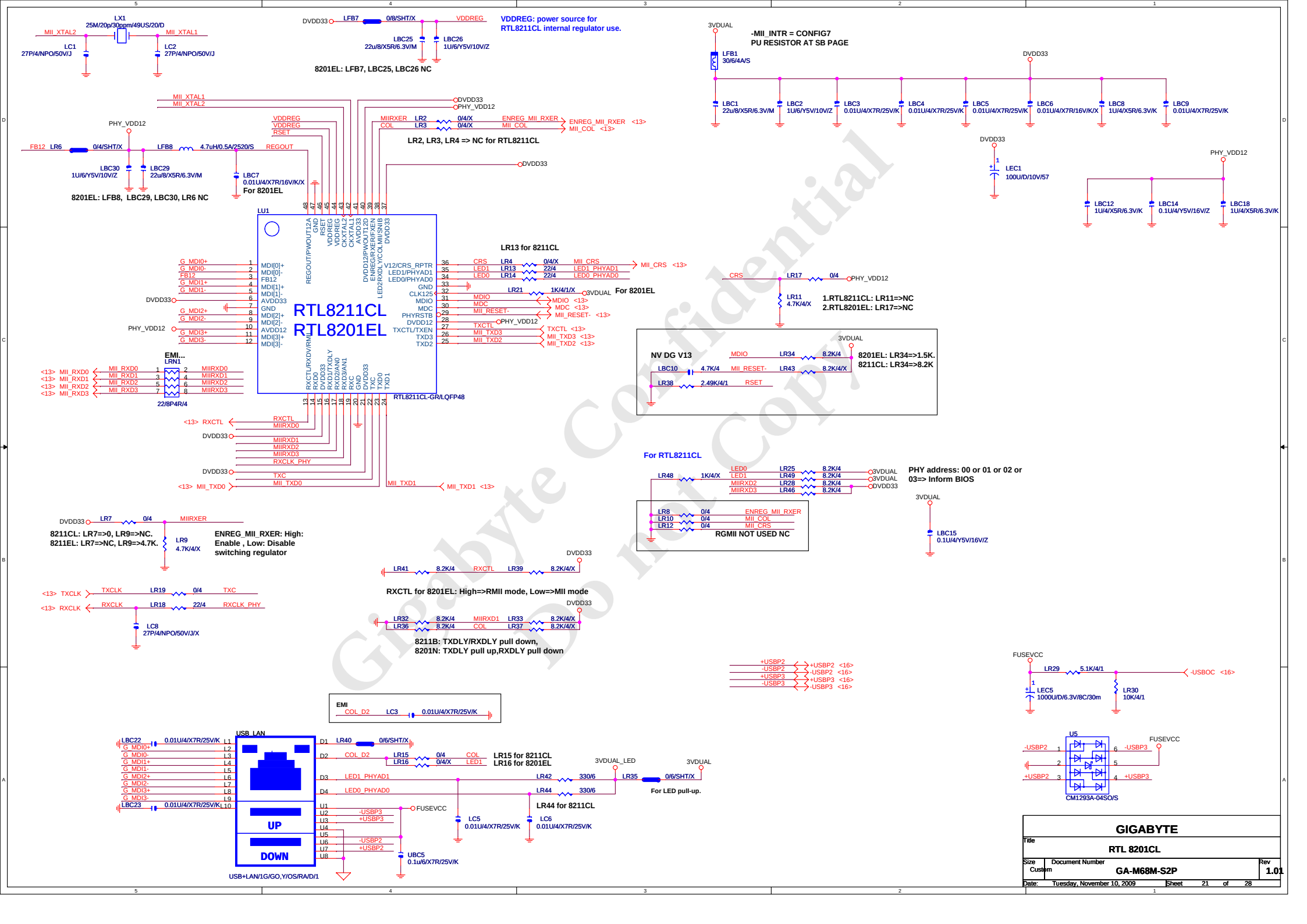
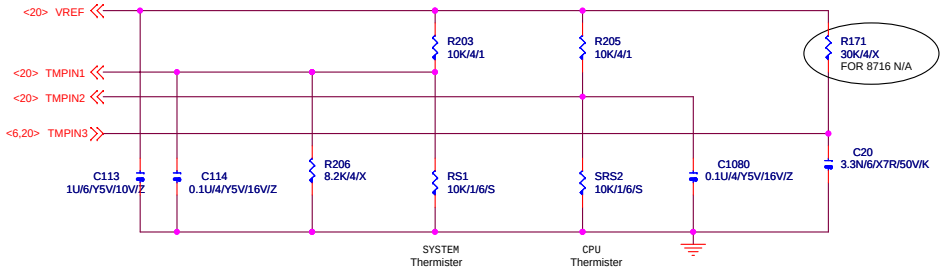


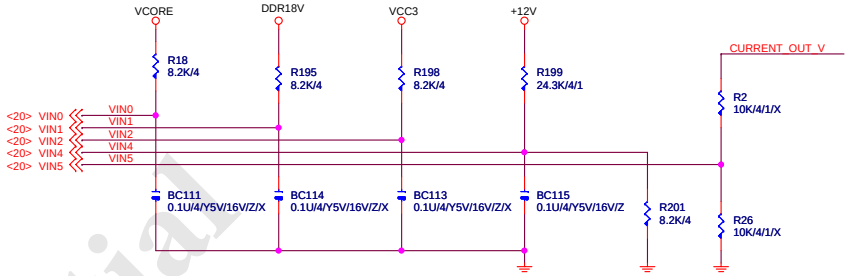
	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

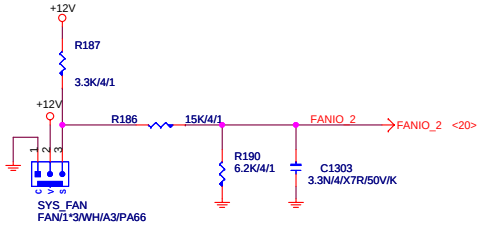


Hardware Monitor circuits

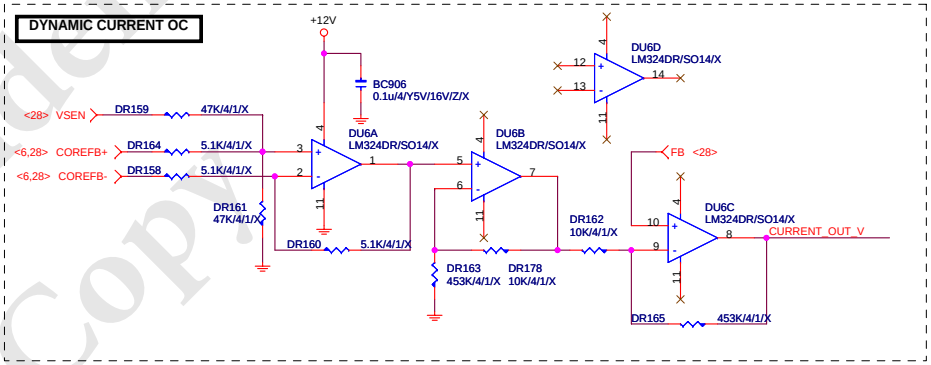




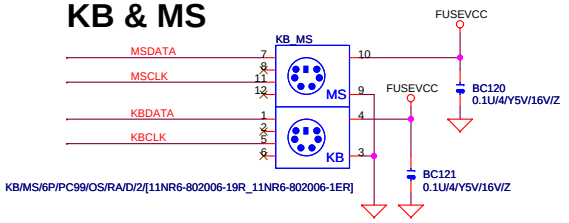
SYSTEM FAN



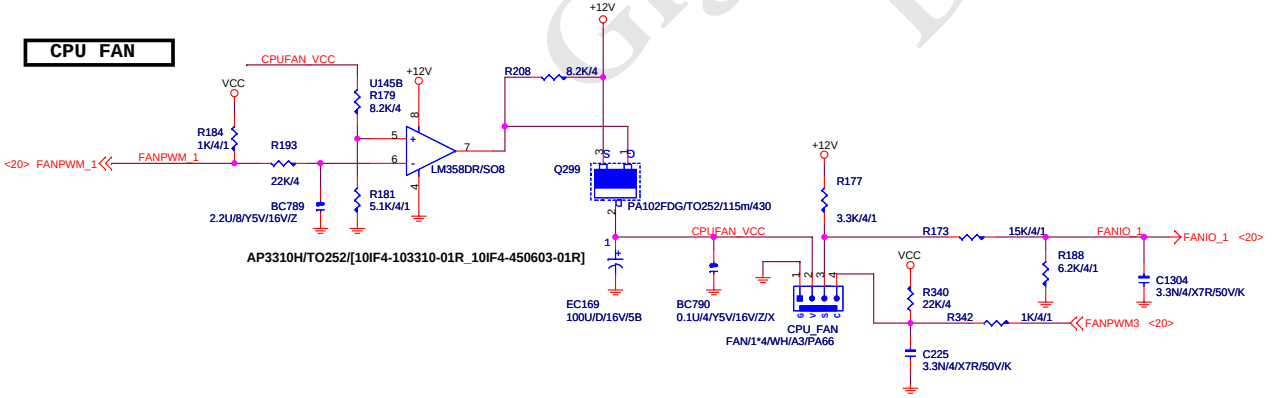
DYNAMIC CURRENT OC

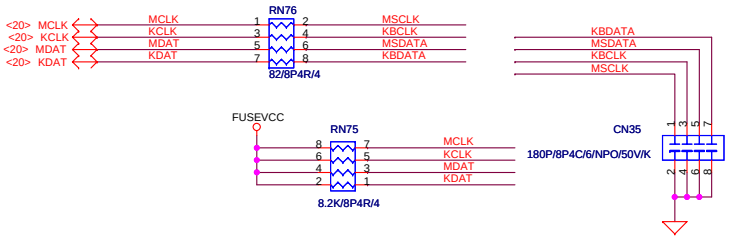


KB & MS



CPU FAN





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Title	FAN/HWMO KB/MS
Size	Custom
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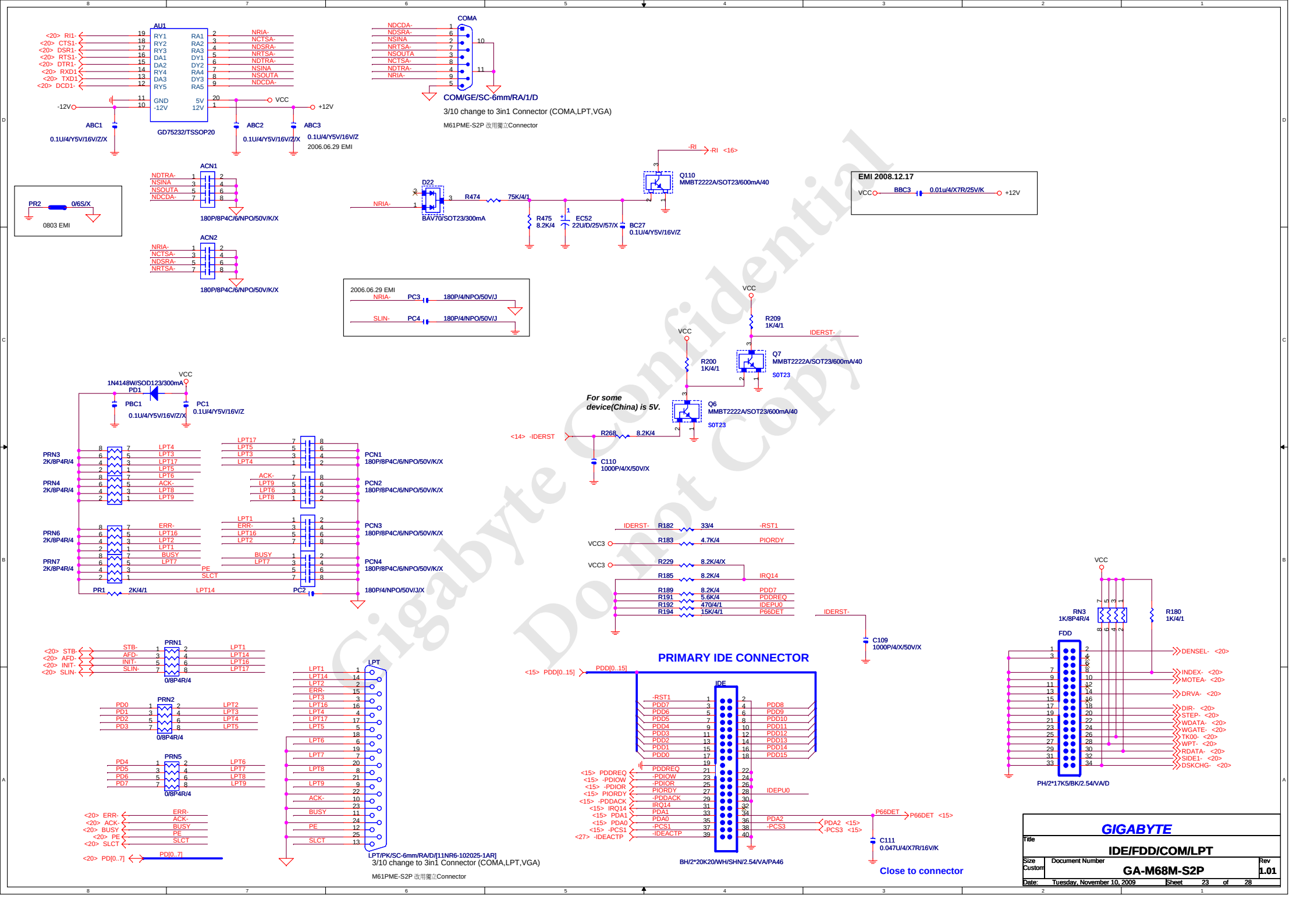

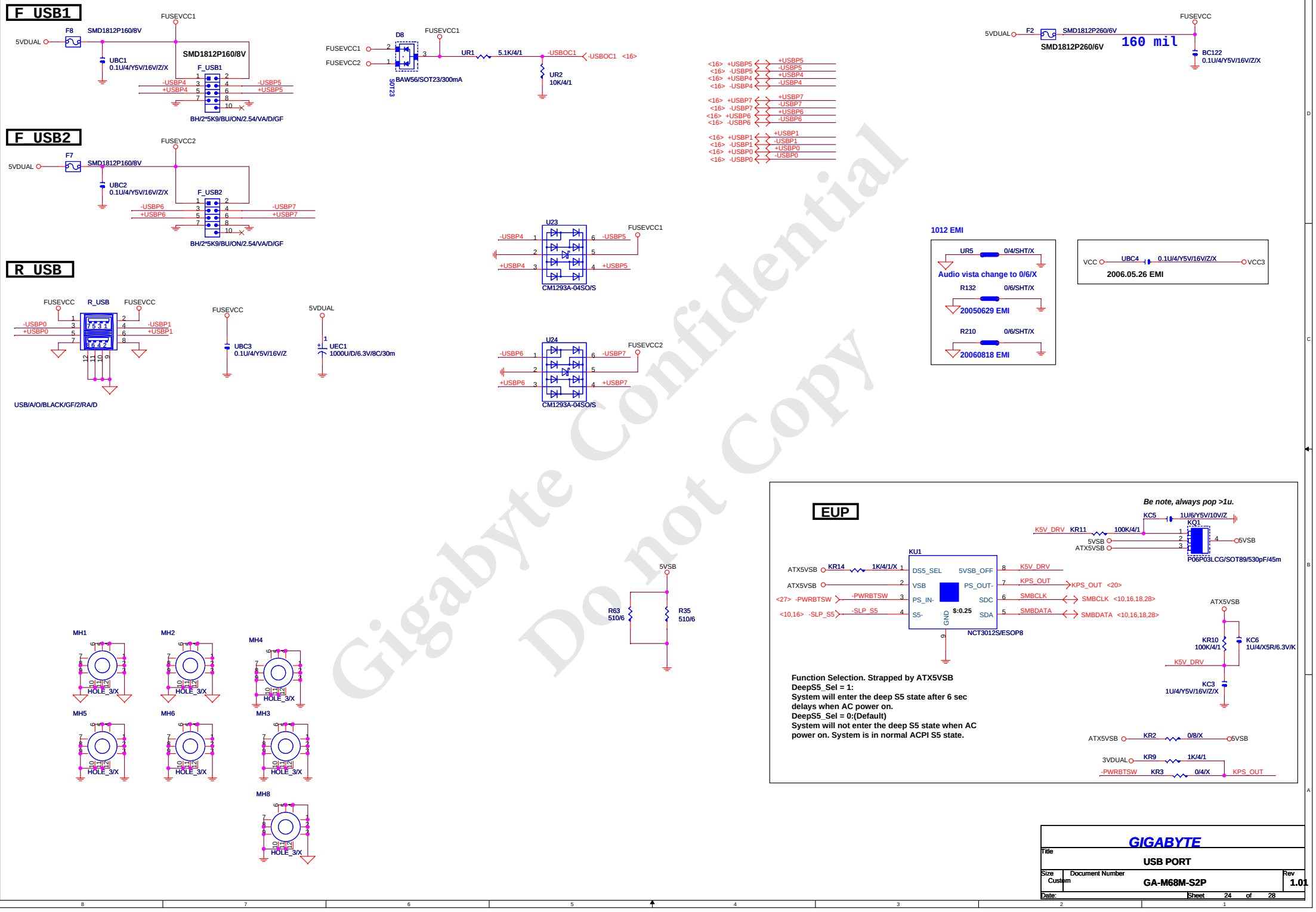
F_USB1
F8
SMD1812P160/8V
5VDUAL
FUSEVCC1
UBC1
0.1U/4/Y5V/16V/Z/X
SMD1812P160/8V
F_USB1
-USBP4
+USBP4
-USBP5
+USBP5
BH/2*5K9/BU/ON/2.54/VA/D/GF
D8
FUSEVCC1
FUSEVCC2
BAW56/SOT23/300mA
SOT23
UR1
5.1K/4/1
-USBOC1
UR2
10K/4/1
<16> +USBP5
<16> -USBP5
<16> +USBP4
<16> -USBP4
<16> +USBP7
<16> -USBP7
<16> +USBP6
<16> -USBP6
<16> +USBP1
<16> -USBP1
<16> +USBP0
<16> -USBP0
5VDUAL
F2
SMD1812P260/6V
FUSEVCC
160 mil
BC122
0.1U/4/Y5V/16V/Z/X
F_USB2
F7
FUSEVCC2
UBC2
F_USB2
-USBP6
+USBP6
-USBP7
+USBP7
R_USB
R_USB
FUSEVCC
-USBP0
+USBP0
-USBP1
+USBP1
USB/A/O/BLACK/GF/2/RA/D
UBC3
0.1U/4/Y5V/16V/Z
UEC1
1000U/D/6.3V/8C/30m
U23
CM1293A-04SO/S
U24
1012 EMI
UR5
0/4/SHT/X
Audio vista change to 0/6/X
R132
0/6/SHT/X
20050629 EMI
R210
0/6/SHT/X
20060818 EMI
VCC
UBC4
0.1U/4/Y5V/16V/Z/X
VCC3
2006.05.26 EMI
EUP
Be note, always pop >1u.
KC5
1U/6/Y5V/10V/Z
KQ1
K5V_DRV
KR11
100K/4/1
5VSB
ATX5VSB
P06P03LCG/SOT89/530pF/45m
KU1
KR14
1K/4/1/X
DS5_SEL
VSB
PS_IN-
S5-
5VSB_OFF
PS_OUT-
SDC
SDA
GND
S:0.25
NCT3012S/ESOP8
KPS_OUT
SMBCLK
SMBDATA
-PWRBTSW
-SLP_S5
KR10
100K/4/1
KC6
1U/4/X5R/6.3V/K
KC3
1U/4/Y5V/16V/Z/X
KR2
0/8/X
3VDUAL
KR9
1K/4/1
KR3
0/4/X
Function Selection. Strapped by ATX5VSB
DeepS5_Sel = 1:
System will enter the deep S5 state after 6 sec delays when AC power on.
DeepS5_Sel = 0:(Default)
System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.
R63
510/6
R35
510/6
MH1
MH2
MH4
MH5
MH6
MH3
MH8
HOLE_3/X
GIGABYTE
Title
USB PORT
Size
Custom
Document Number
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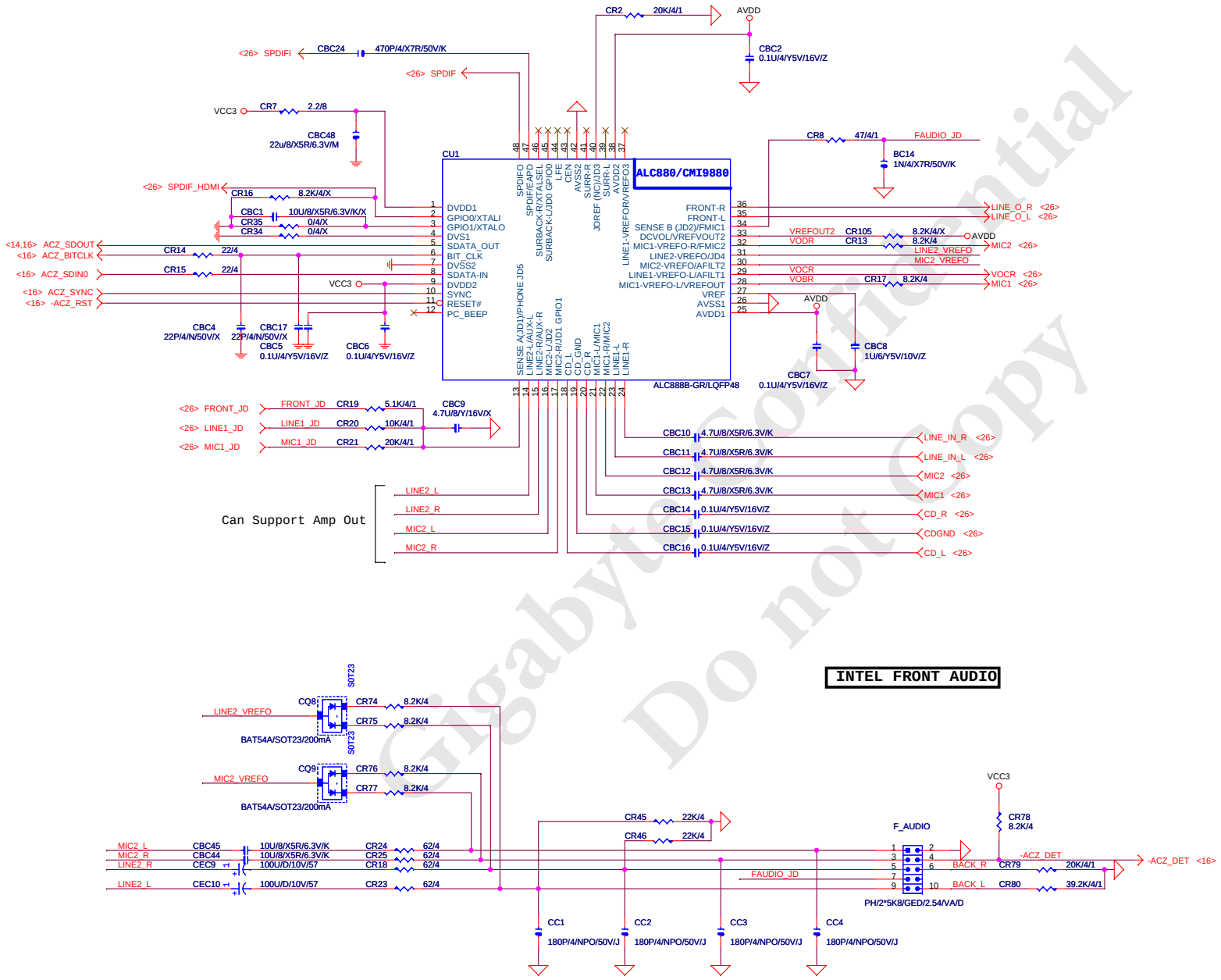

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Title	ALC888	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 1.01
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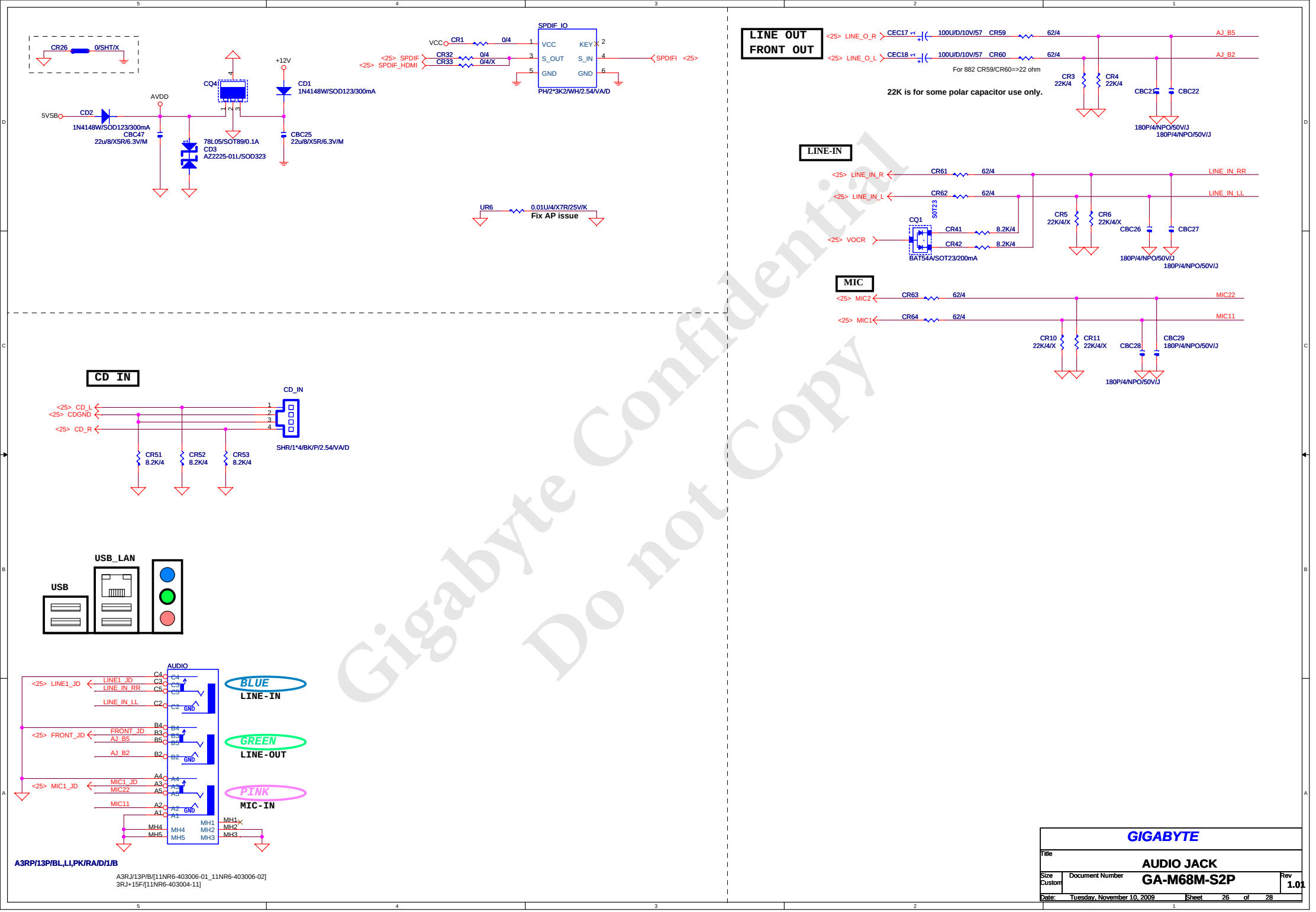
CR26 0/SHT/X
5VSB
CD2
1N4148W/SOD123/300mA
CBC47
22u/8/X5R/6.3V/M
AVDD
CQ4
78L05/SOT89/0.1A
CD3
AZ2225-01L/SOD323
+12V
CD1
1N4148W/SOD123/300mA
CBC25
22u/8/X5R/6.3V/M
SPDIF_IO
VCC CR1 0/4
<25> SPDIF CR32 0/4
<25> SPDIF_HDMI CR33 0/4/X
VCC KEY S_OUT S_IN GND GND
SPDIFI <25>
PH/2*3K2/WH/2.54/VA/D
UR6 0.01U/4/X7R/25V/K
Fix AP issue
LINE OUT
FRONT OUT
<25> LINE_O_R CEC17 100U/D/10V/57 CR59 62/4 AJ_B5
<25> LINE_O_L CEC18 100U/D/10V/57 CR60 62/4 AJ_B2
For 882 CR59/CR60=>22 ohm
22K is for some polar capacitor use only.
CR3 22K/4
CR4 22K/4
CBC21
CBC22
180P/4/NPO/50V/J
180P/4/NPO/50V/J
LINE-IN
<25> LINE_IN_R CR61 62/4 LINE_IN_RR
<25> LINE_IN_L CR62 62/4 LINE_IN_LL
SOT23
CQ1
<25> VOCR
CR41 8.2K/4
CR42 8.2K/4
BAT54A/SOT23/200mA
CR5 22K/4/X
CR6 22K/4/X
CBC26
CBC27
180P/4/NPO/50V/J
180P/4/NPO/50V/J
MIC
<25> MIC2 CR63 62/4 MIC22
<25> MIC1 CR64 62/4 MIC11
CR10 22K/4/X
CR11 22K/4/X
CBC28
CBC29
180P/4/NPO/50V/J
CD IN
CD_IN
<25> CD_L
<25> CDGND
<25> CD_R
CR51 8.2K/4
CR52 8.2K/4
CR53 8.2K/4
SHR/1*4/BK/P/2.54/VA/D
USB_LAN
USB
AUDIO
<25> LINE1_JD
LINE1_JD
LINE_IN_RR
LINE_IN_LL
BLUE
LINE-IN
<25> FRONT_JD
FRONT_JD
AJ_B5
AJ_B2
GREEN
LINE-OUT
<25> MIC1_JD
MIC1_JD
MIC22
MIC11
PINK
MIC-IN
GND
MH1 MH2 MH3 MH4 MH5
A3RP/13P/BL,LI,PK/RA/D/1/B
A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]
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GIGABYTE
Title
AUDIO JACK
Size Custom
Document Number
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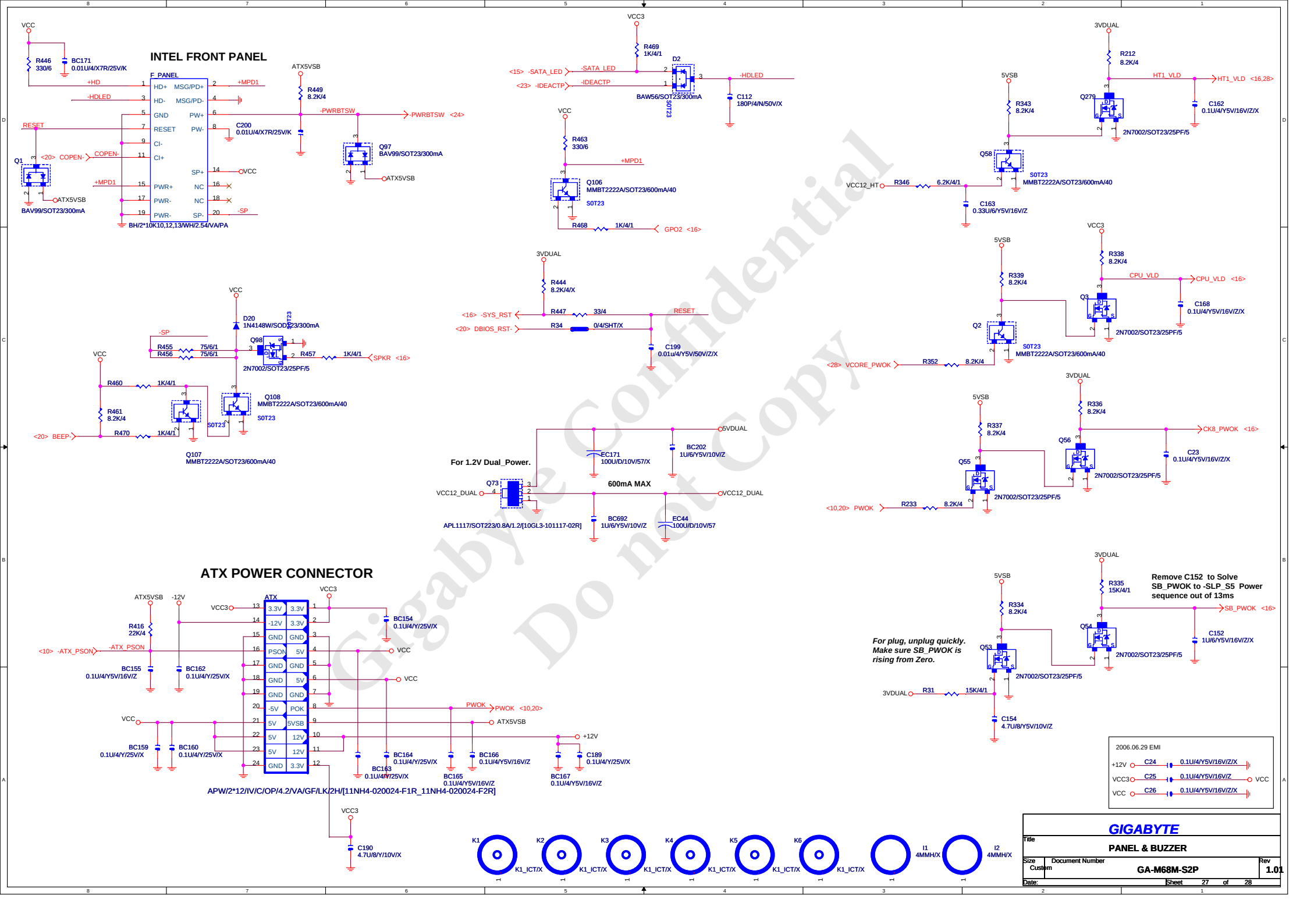
INTEL FRONT PANEL
F_PANEL
BH/2*10K10,12,13/WH/2.54/VA/PA
ATX POWER CONNECTOR
APW/2*12/IV/C/OP/4.2/VA/GF/LK/2H/[11NH4-020024-F1R_11NH4-020024-F2R]
For 1.2V Dual_Power.
600mA MAX
APL1117/SOT223/0.8A/1.2/[10GL3-101117-02R]
Remove C152 to Solve SB_PWOK to -SLP_S5 Power sequence out of 13ms
For plug, unplug quickly. Make sure SB_PWOK is rising from Zero.
2006.06.29 EMI
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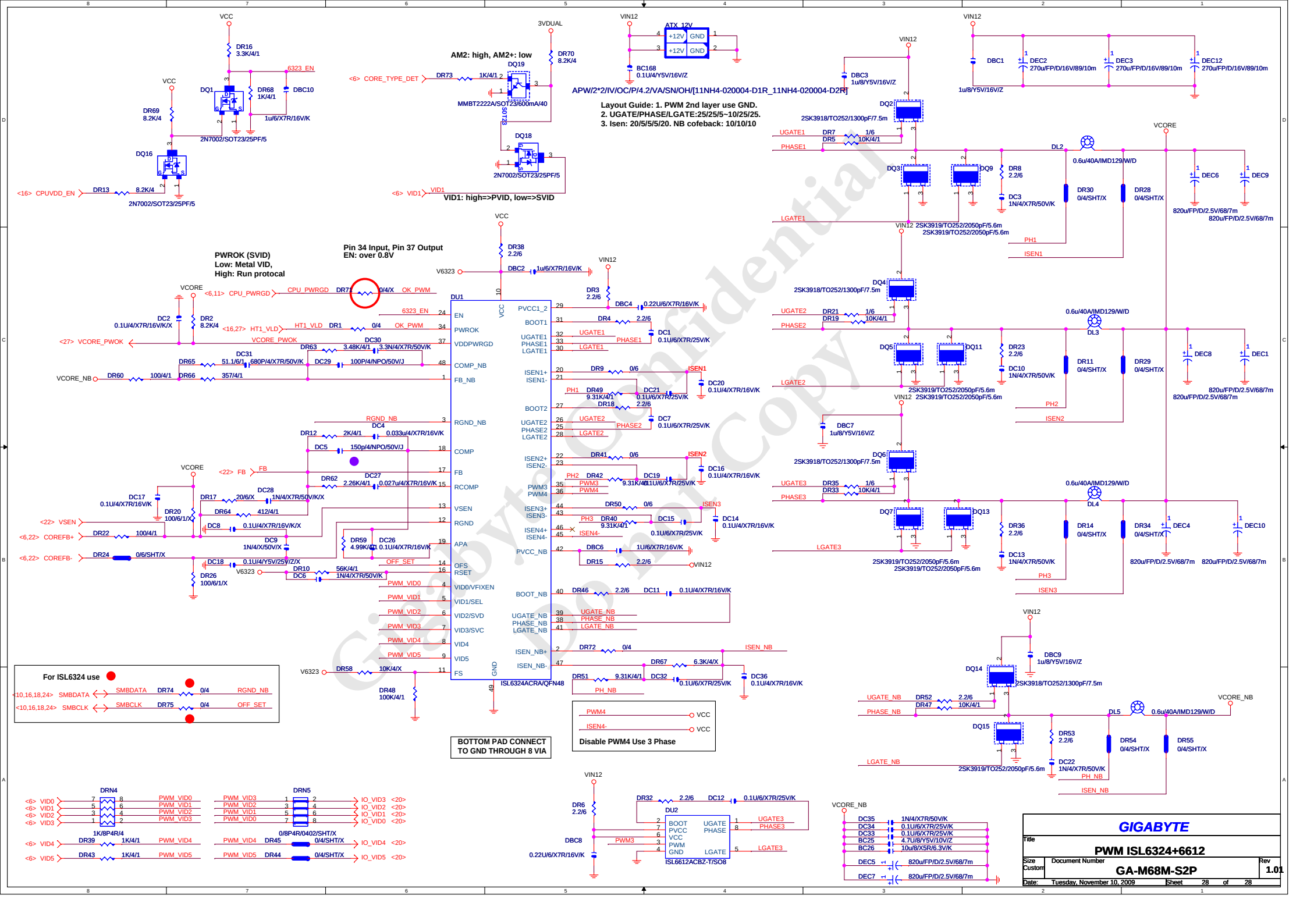
PANEL & BUZZER
GA-M68M-S2P
1.01


AM2: high, AM2+: low
VID1: high=>PVID, low=>SVID
PWROK (SVID)
Low: Metal VID,
High: Run protocal
Pin 34 Input, Pin 37 Output
EN: over 0.8V
APW/2*2/IV/OC/P/4.2/VA/SN/OH/[11NH4-020004-D1R_11NH4-020004-D2R]
Layout Guide: 1. PWM 2nd layer use GND.
2. UGATE/PHASE/LGATE:25/25/5~10/25/25.
3. Isen: 20/5/5/5/20. NB cofeback: 10/10/10
For ISL6324 use
BOTTOM PAD CONNECT
TO GND THROUGH 8 VIA
Disable PWM4 Use 3 Phase
ISL6324ACRA/QFN48
ISL6612ACBZ-T/SO8
GIGABYTE
PWM ISL6324+6612
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