Compal Confidential

EH7L1/EH5L1 MB Schematic Document

LA-H782P

Rev: 1.A

2019.05.13

Compal Electronics, Inc.
Title: Cover Sheet
Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1A
Date: Tuesday, May 14, 2019 | Sheet 1 of 47

HDMI Conn.

page 22

DDI1
HDMI x 4 lanes

eDP

page 21

eDP

DDI

Intel Kabylake U

Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)
(KBL-U_23E Fuse Down)
Processor

Dual Core + GT2
Quad Core + GT2

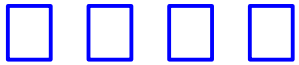
15W
1356pin BGA
page 07~18

Memory BUS
Dual Channel

1.2V DDR4 2133/2400

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16



page 19

260pin DDR4-SO-DIMM X1

page 20

page 24

(Reserved PCIE 3.0 x4)
(Port 9-12, 8GT/s)

SATA3.0
6.0 Gb/s
port 12
(SATA2)

Flexible IO
Base-U PCIE2.0
Premium-U PCIE3.0

NGFF
WLAN
USB2 port 5

PCIe 1.0
2.5GT/s
port 6
page 24

LAN(GbE)
Realtek 8111H
page 25

RJ45 conn.

PCIe 1.0
2.5GT/s
port 5

SATA HDD
Conn.

page 26

SATA3.0
6.0 Gb/s
port 7
(SATA0)

SATA CDROM
Conn.

page 26

SATA3.0
6.0 Gb/s
port 8
(SATA1)

USB 3.0
conn x1
USB3 port1
USB2 port1

page 27

USB 2.0
conn x2
USB2 port2
USB2 Port3 on SUB/B

page 28

CMOS
Camera
USB2 port7

page 22

USBx8 48MHz

HD Audio 3.3V 24MHz

Touch
Screen
USB2 port 6
page 22

HDA Codec
ALC255 page 25

SPI

SPI ROM
64Mb page 9

LPC/eSPI BUS
CLK=24MHz

ENE
KB9022
page 29

Int. Speaker
page 25

Int. DMIC
on Camera
page 25

UAJ
page 25

Fan Control
page 31

Sub Board

LS-H781P IO/B
page 28

LSH783P HS/B
page 31

LSH784P ODD/B
page 26

RTC CKT.
page 15

Power On/Off CKT.
page 30

DC/DC Interface CKT.
page 32

page 31~44

Int.KBD

page 30

Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

page 30

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Issued Date	2018/12/11	Deciphered Date	2018/11/04

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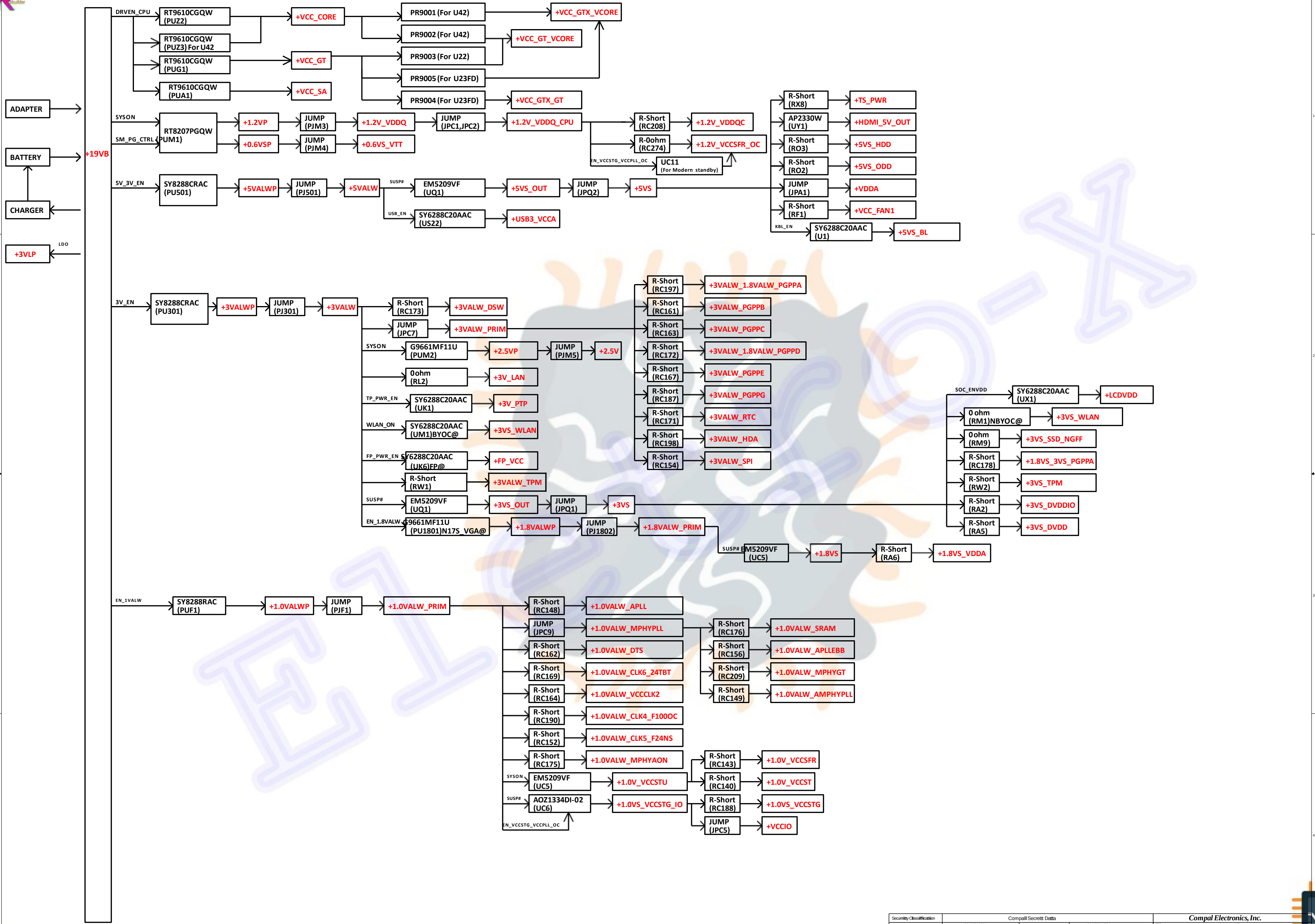
Title: Block Diagrams

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1A

Date: Monday, May 13, 2019 | Sheet 2 of 47



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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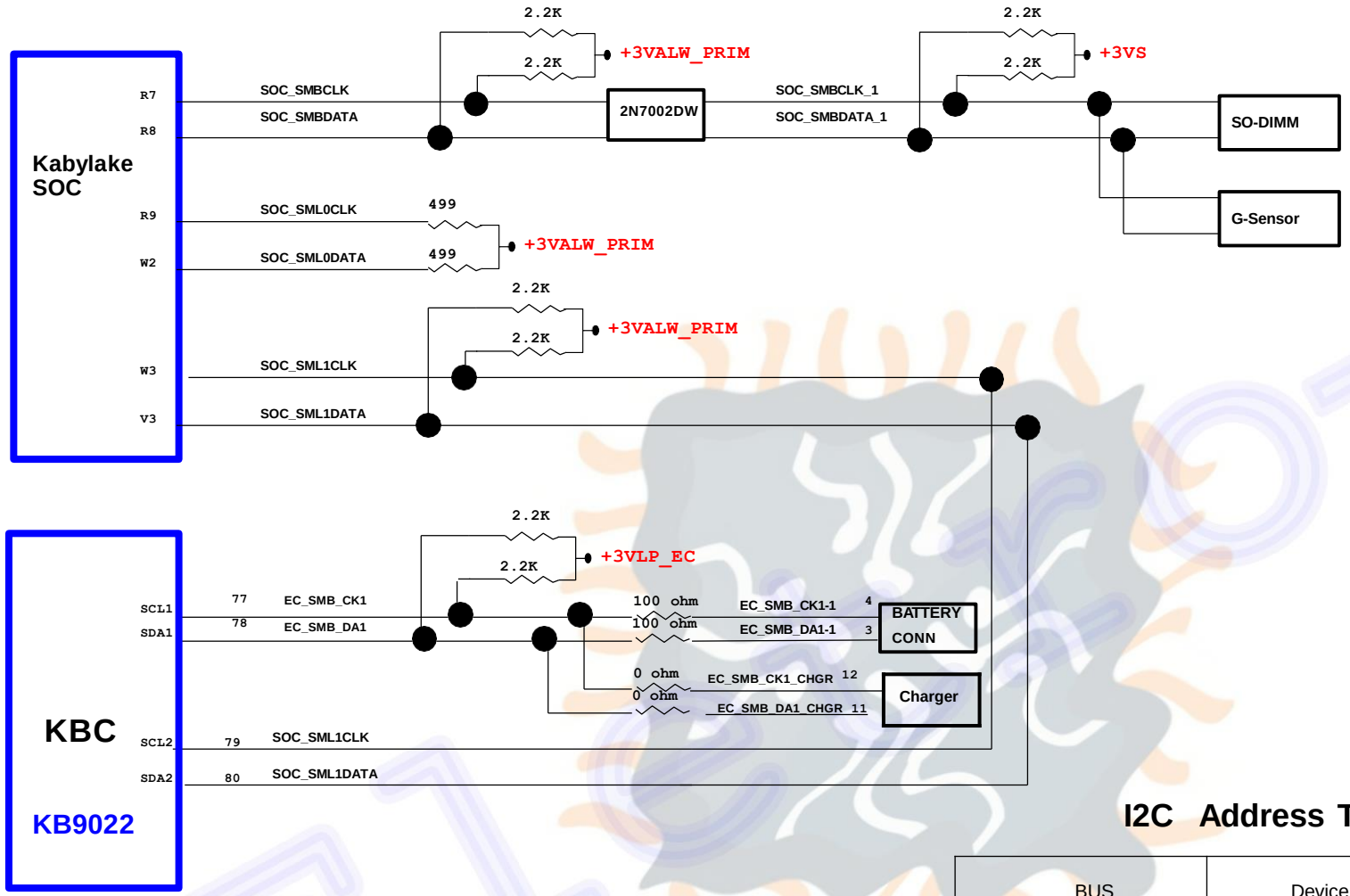
Size Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 Sheet 4 of 47



I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved			
I2C_1 (+3VALW_PGPPC_E)	TM-P3393-003 (TP)	0x2C		
	FA577E-1206 (TP-ELAN)	0x15		
	SA577C-12A0 (TP-ELAN)	0x15		
SOC_SMBCLK (+3VS)	SO-DIMM	0xA4		
	G-Sensor	0x30		
SOC_SML1CLK (+3VALW_PRIM)	VGA	0x9E		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24781RUYR (Charger IC)	0x12		
	BATTERY PACK	0x16		

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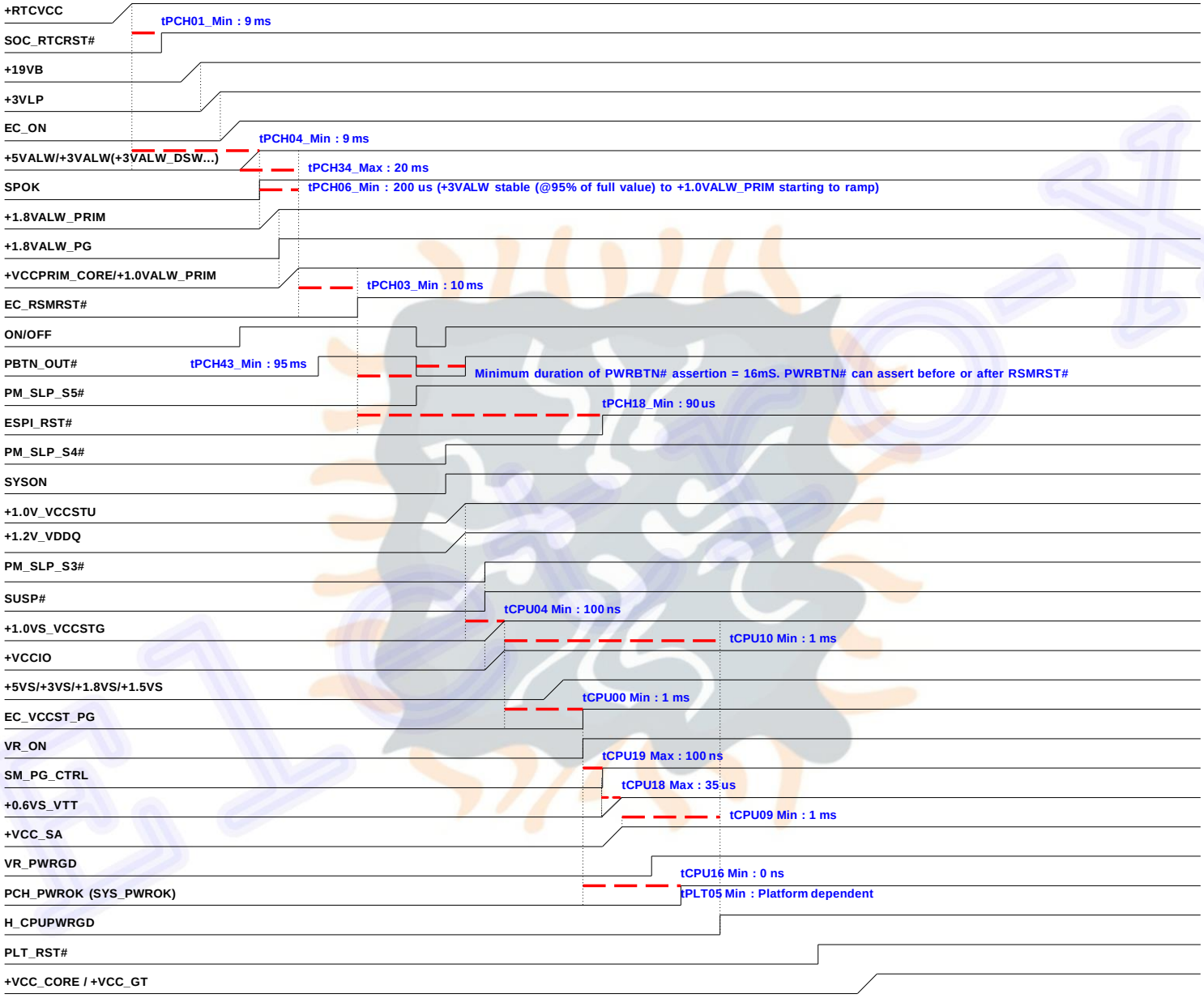
Title: SMBUS Routing Table

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1A

Date: Monday, May 13, 2019 | Sheet 5 of 47

PWR Sequence_KBL-U22/U42



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Title: Power Sequence

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 6 of 47

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	0.1(DVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.0(PVT)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	1.A(MP)
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
Acer BYOC	BYOC@ / NBYOC@
CODEC(ALC255/256)	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
CPU Selection	U42@/U22@
ODD Support	ODD@
G Sensor	BA@
TPM	TPM@ / NTPM@
Finger Print	FP@/FPEMC@
UMA or DGPU	UMA@/VGA@
Intel Modern Standby	MSB@/NMSB@
MB Stage	EVT@/DVT@/PVT@/MP@
Memory Select	X76H4G@/X76M4G@/ X76S4G@
Memory Mode	SDP@ / DDP@
BOM Select	15@/15DIS@

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

43 level BOM table

43 Level	Description	BOM Structure
431AI4BOL03	SMT MB AH782 EH5L1 I370U23E HDMI	U22@/CMC@/LPC@/NRD@/NBYOC@/255@/MP@/MEM@/NMSB@/NTPM@/UMADAZ1A@/X76M@/X4EUMA@/UMA@/15@/EH5L1@/SR3N6@
431AI4BOL04	SMT MB AH782 EH5L1 I370U22 HDMI	U22@/CMC@/LPC@/NRD@/NBYOC@/255@/MP@/MEM@/NMSB@/NTPM@/UMADAZ1A@/X76M@/X4EUMA@/UMA@/15@/EH5L1@/SR3TK@
431AI4BOL54	SMT MB AH782 EH7L1 I370U23E HDMI	
431AI4BOL55	SMT MB AH782 EH7L1 I370U22 HDMI	U22@/CMC@/LPC@/RD@/NBYOC@/255@/MP@/MEM@/NMSB@/NTPM@/ODD@/UMADAZ1A@/X76M@/X4EUMA@/UMA@/EH7L1@/SR3QR@

Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/11/04

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Title: Notes List

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 3 of 47

Functional Strap Definitions

#543016 PDG2.0 P.844

DDPB_CTRLDATA
DDPC_CTRLDATA
Display Port B/C Detected
NC =Port is not detected.
PU =Port is detected.

+VCCIO
RC1 1 2 24.9_0402_1% EDP_COMP

#543016 PDG2.0 P.225
COMPENSATION PU for eDP
Trace width=5 mils,Spacing=25mil,Max length=600mils

+1.0V_VCCST **#543016 PDG2.0 P.857**
PU 1K to VCCST
RC2 1 2 1K_0402_5% H_THERMTRIP#
CC132 ESD@ 1000P_0402_50V7K

CC163 2 1 .1U_0402_16V7K @ESD@
CC52 2 1 .1U_0402_16V7K @ESD@
H_PECI
2 1 ESD@ CC53 1000P_0402_50V7K
H_PROCHOT#_R

+1.0VS_VCCSTG **For Intel debug, place to CPU side.**
#543016 PDG2.0 P.629
RC11 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC13 2 @ 1 51_0402_5% SOC_XDP_TDI
RC15 2 CMC@ 1 51_0402_5% SOC_XDP_TDO
RC35 2 CMC@ 1 51_0402_5% CPU_XDP_TCK0

HDMI

UC1A SKL-U Rev_0.53

<22> SOC_DP1_N0 E55 DDI1_TXN[0]
<22> SOC_DP1_P0 F55 DDI1_TXP[0]
<22> SOC_DP1_N1 E58 DDI1_TXN[1]
<22> SOC_DP1_P1 F58 DDI1_TXP[1]
<22> SOC_DP1_N2 F53 DDI1_TXN[2]
<22> SOC_DP1_P2 G53 DDI1_TXP[2]
<22> SOC_DP1_N3 F56 DDI1_TXN[3]
<22> SOC_DP1_P3 G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI EDP DISPLAY SIDEBANDS

HDMI DDC (Port B)

<22> SOC_DP1_CTRL_CLK SOC_DP1_CTRL_CLK L13 GPP_E18/DDPB_CTRLCLK
<22> SOC_DP1_CTRL_DATA SOC_DP1_CTRL_DATA L12 GPP_E19/DDPB_CTRLDATA
N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA
EDP_COMP E52 EDP_RCOMP

1 OF 20

SKL-U_BGA1356 @

EDP_TXN[0] C47 EDP_TXN0 <21>
EDP_TXP[0] C46 EDP_TXP0 <21>
EDP_TXN[1] D46 EDP_TXN1 <21>
EDP_TXP[1] C45 EDP_TXP1 <21>
EDP_TXN[2] A45 EDP_TXN2 <21>
EDP_TXP[2] B45 EDP_TXP2 <21>
EDP_TXN[3] A47 EDP_TXN3 <21>
EDP_TXP[3] B47 EDP_TXP3 <21>
eDP

EDP_AUXN E45 EDP_AUXN <21>
EDP_AUXP F45 EDP_AUXP <21>
EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 SOC_DP1_HPD SOC_DP1_HPD <22> **From HDMI**
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9 EC_SCI# EC_SCI# <29>
GPP_E17/EDP_HPD L10 CPU_EDP_HPD CPU_EDP_HPD <21> **From eDP**

EDP_BKLTEN R12 ENBKL ENBKL <29>
EDP_BKLTCTL R11 SOC_BKL_PWM SOC_BKL_PWM <21>
EDP_VDDEN U13 SOC_ENVDD SOC_ENVDD <21>

+1.0VS_VCCSTG
RC3 1K_0402_5%
RC4 499_0402_1%
<29,36> H_PROCHOT#

UC1D SKL-U Rev_0.53

Reserved CATERR# for sight i ngs i ss ue check
@ T166 H_CATERR# D63 CATERR#
H_PECI A54 PECI
H_PROCHOT#_R C65 PROCHOT#
H_THERMTRIP# C63 THERMTRIP#
A65 SKTOCC#

@ T160 XDP_BPM#0 C55 BPM#[0]
@ T161 XDP_BPM#1 D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

CPU MISC

<29,30> EC_TP_INT# RC137 2 @ 1 0_0402_5% TP_INT#
A6 GPP_E3/CPU_GP0
A5 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

RC5 2 1 49.9_0402_1% CPU_POPIRCOMP AT16 PROC_POPIRCOMP
RC6 2 1 49.9_0402_1% PCH_OPIRCOMP AU16 PCH_OPIRCOMP
RC7 2 1 49.9_0402_1% EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
RC8 2 1 49.9_0402_1% EOPIO_RCOMP H65 OPC_RCOMP

4 OF 20

SKL-U_BGA1356 @

JTAG

PROC_TCK B61 CPU_XDP_TCK0
PROC_TDI D60 SOC_XDP_TDI
PROC_TDO A61 SOC_XDP_TDO
PROC_TMS C60 SOC_XDP_TMS
PROC_TRST# B59 SOC_XDP_TRST# T194 @

PCH_JTAG_TCK B56 PCH_JTAG_TCK1
PCH_JTAG_TDI D59 SOC_XDP_TDI
PCH_JTAG_TDO A56 SOC_XDP_TDO
PCH_JTAG_TMS C59 SOC_XDP_TMS
PCH_TRST# C61 SOC_XDP_TRST#
JTAGX A59 CPU_XDP_TCK0 T195 @

#543016 PDG2.0 P.873
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB1.1 P.52
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD 50ohm

RC212 10K_0402_5% +3VS
EC_SCI#

EC_SCI# SOC internal PU

#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- **GPP_B14, GPP_B20, GPP_B23**
- **GPP_C 23 : 22**
- **GPP_D 4 : 0**
- **GPP_E 8 : 0 , GPP_E 16 : 13**

@ESD@ CC81 .1U_0402_16V7K
SOC_XDP_TRST#

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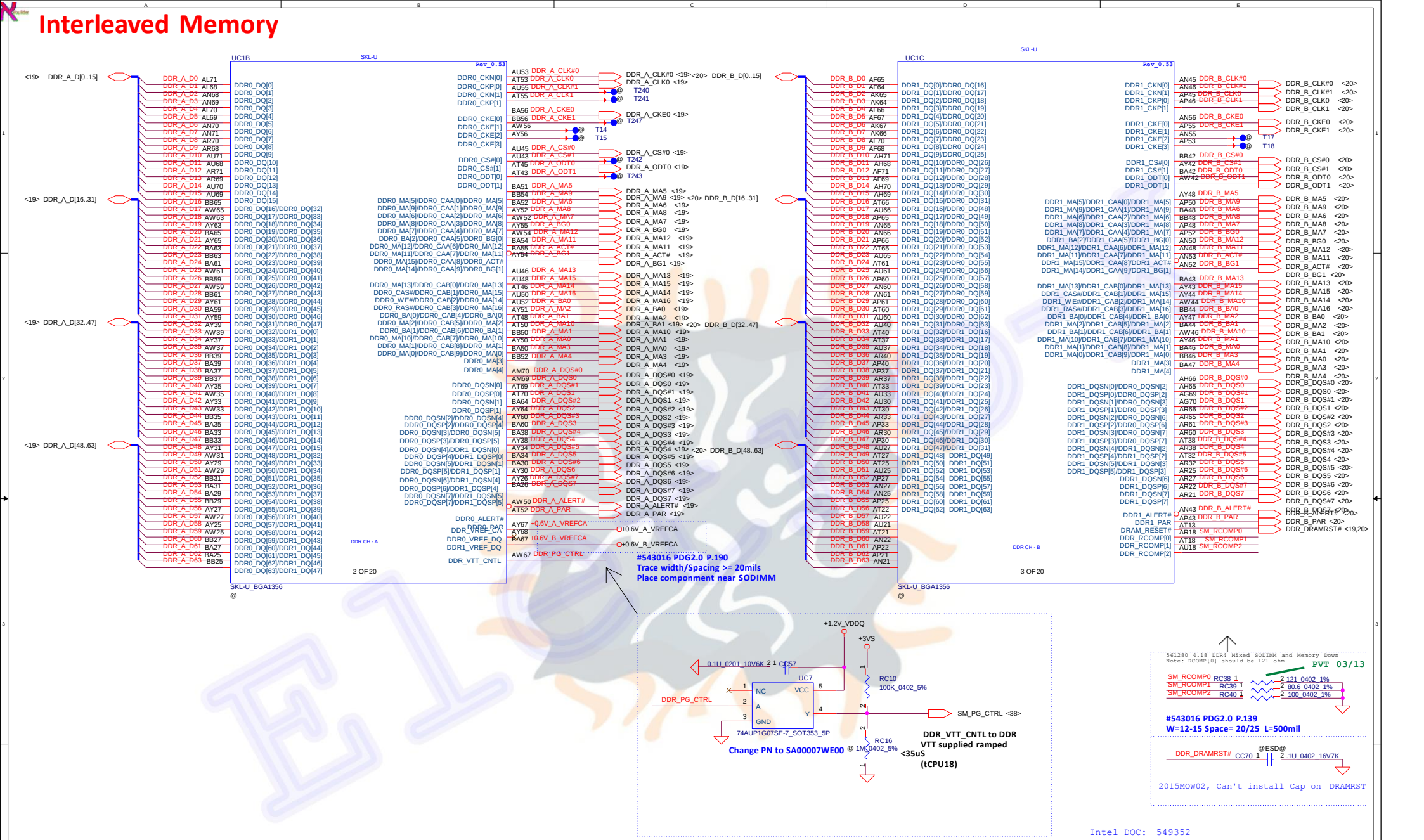
Title: KBL-U(1/12)DDI,MSIC,XDP,EDP
Size: Custom Document Number: EH7L1 LA-H782P
Date: Monday, May 13, 2019 Sheet 7 of 47

Interleaved Memory



Intel DOC: 549352

3. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm

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Title: KBL-U(2/12)DDR4

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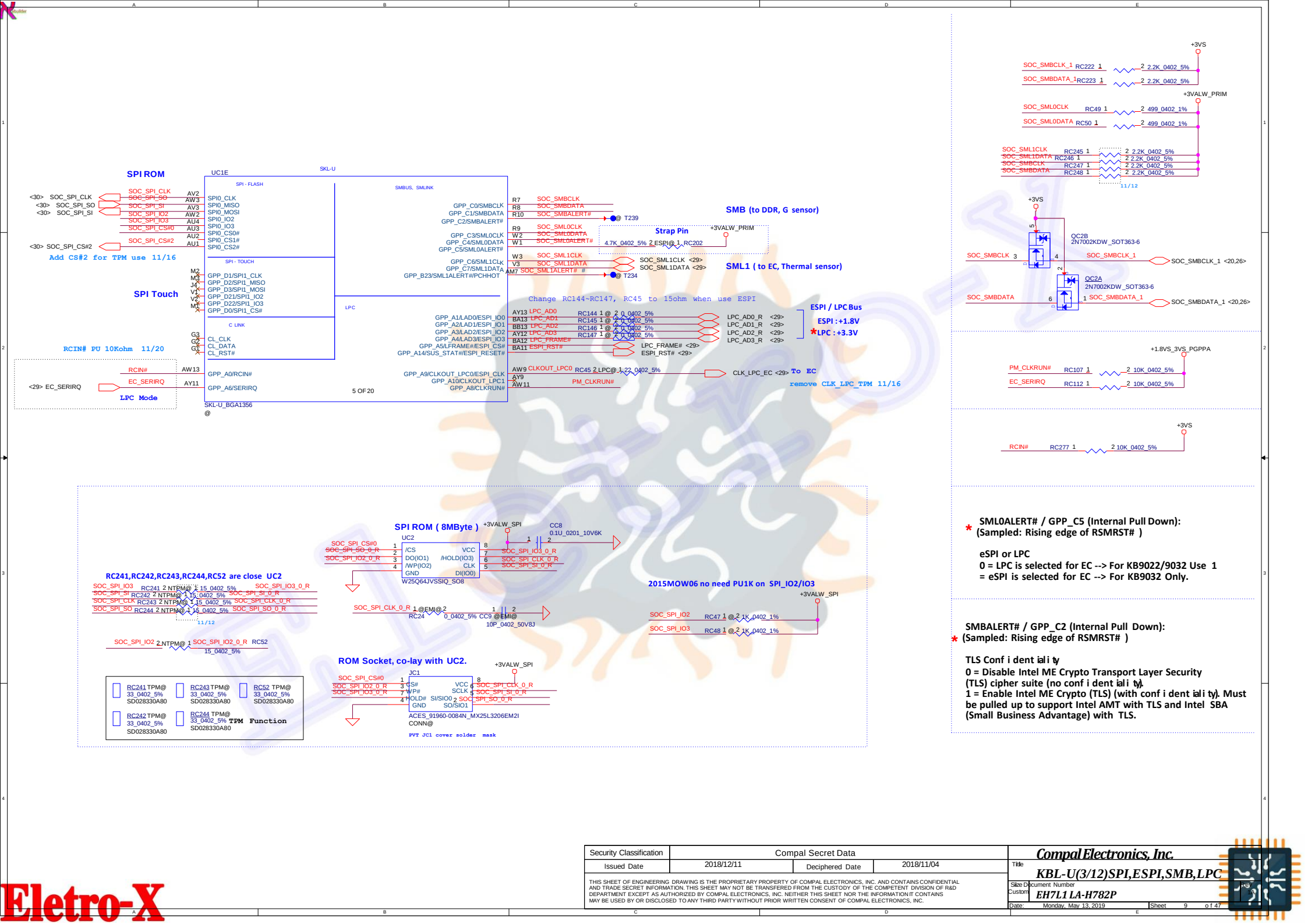
Date: Monday, May 13, 2019 | Sheet 8 of 47



* SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use 1
= eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
* (Sampled: Rising edge of RSMRST#)

TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

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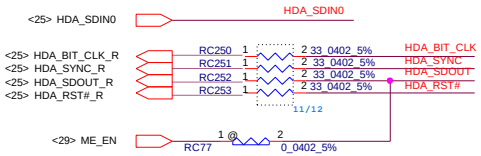
Title: KBL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 9 of 47

HDA for AUDIO



HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures def i nedi nt he flas h Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

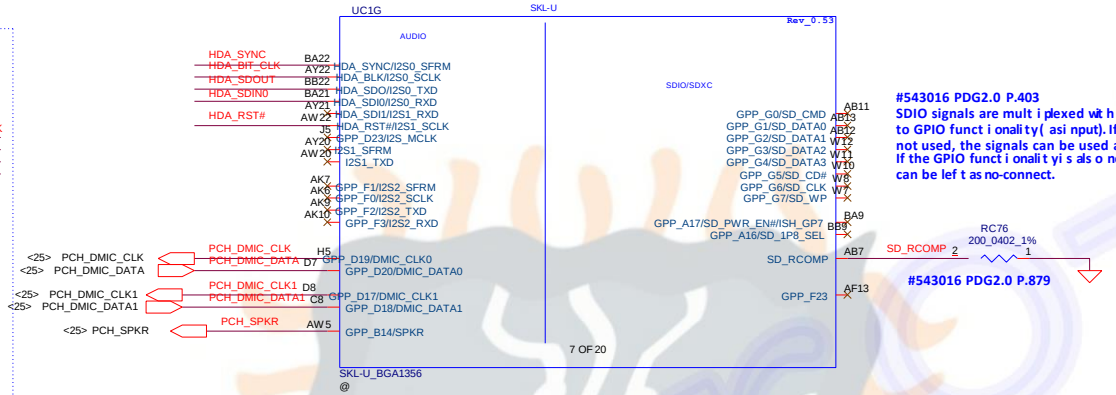
For 4Mic 11/29

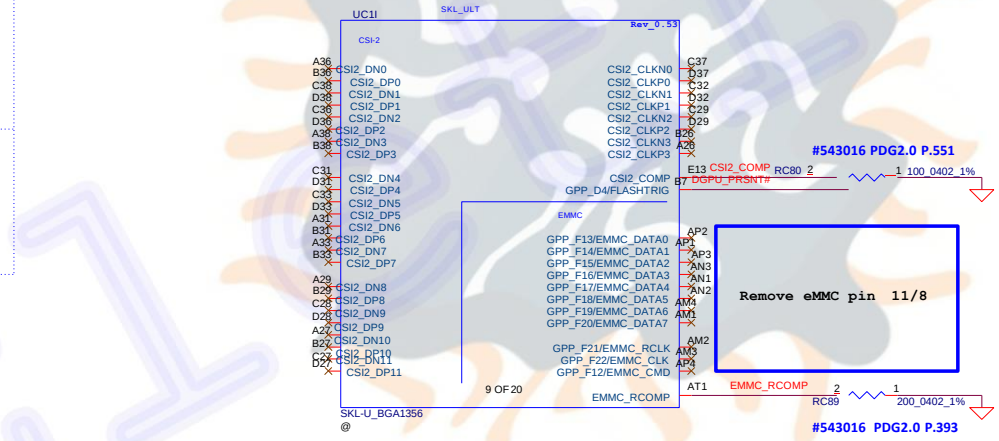
SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

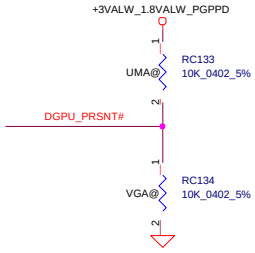
TOP Swap Override

*** 0 = Disable TOP Swap mode.**
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilit i es
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.







	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

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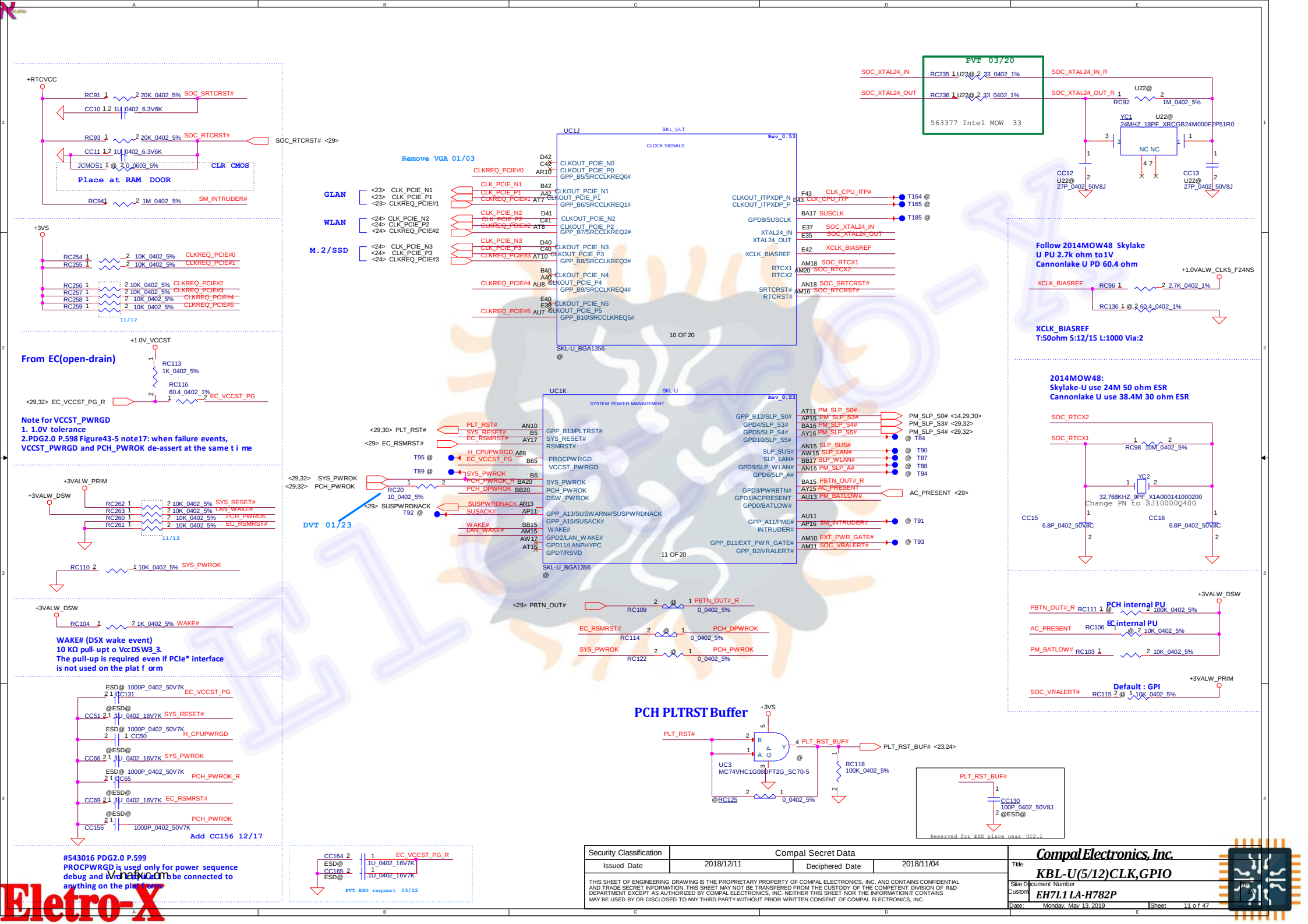
Title: KBL-U(4/12)HDA,EMMC,SDIO,GSP

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 10 of 45



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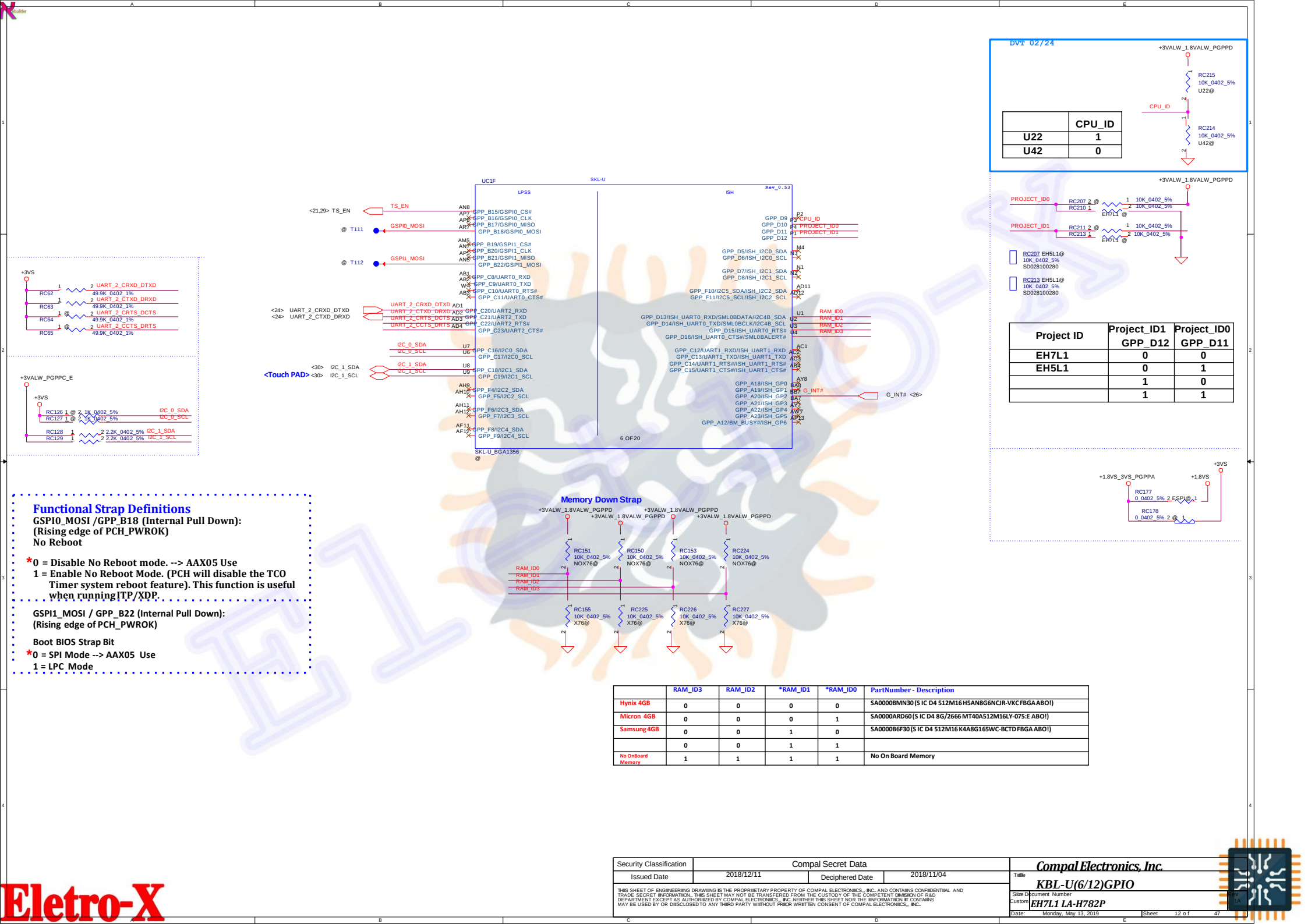
Title: KBL-U(5/12)CLK,GPIO

Size: Custom | Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 | Sheet: 11 of 47



Functional Strap Definitions

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

***0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
***0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABO!)
Micron 4GB	0	0	0	1	SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABO!)
Samsung 4GB	0	0	1	0	SA0000B6F30 (S IC D4 512M16 K4A8G165WC-BCTD FBGA ABO!)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory

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Compal Electronics, Inc.

Title: KBL-U(6/12)GPIO

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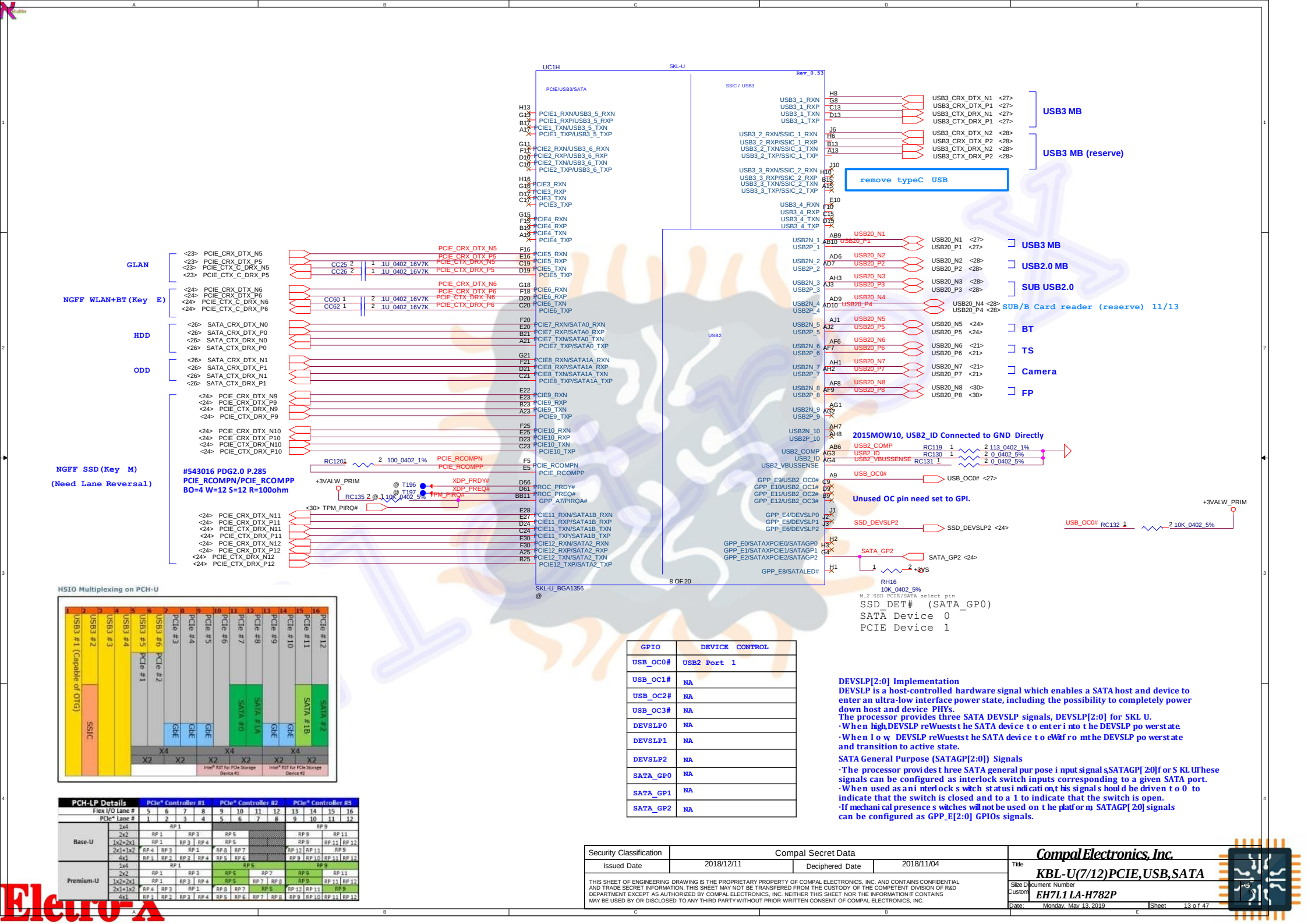
Date: Monday, May 13, 2019 | Sheet 12 of 47



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

- When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
- When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
- If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

PCH-LP Details	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #	5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U 1x4	RP 1								RP 9			
Base-U 2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
Base-U 1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
Base-U 2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7			RP 12	RP 11	RP 9	
Base-U 4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U 1x4	RP 1				RP 5				RP 9			
Premium-U 2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
Premium-U 1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
Premium-U 2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
Premium-U 4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

Compal Electronics, Inc.

Title: KBL-U(7/12)PCIE,USB,SATA

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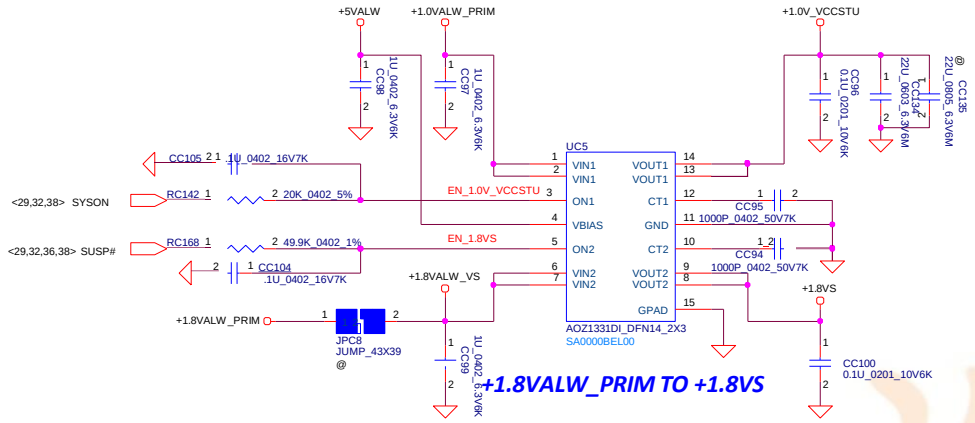
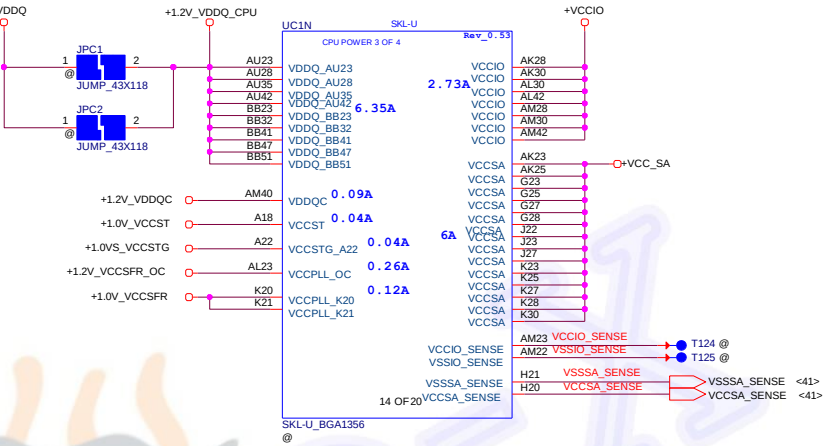
Date: Monday, May 13, 2019 | Sheet 13 of 47

+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

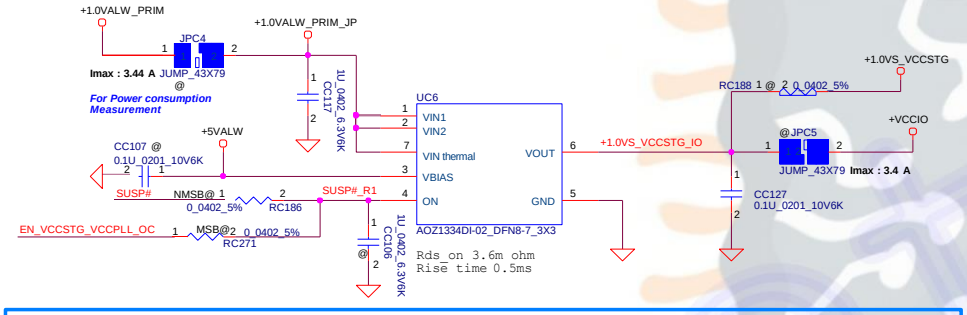


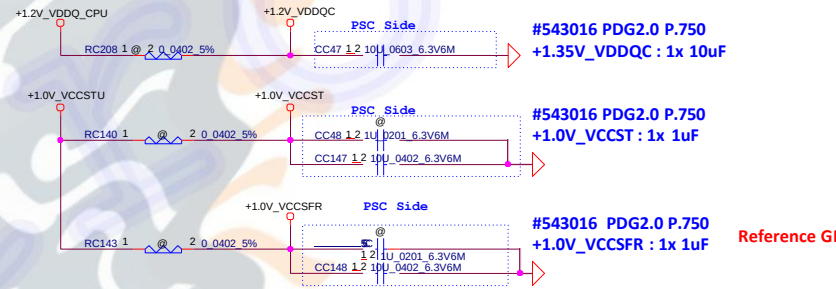
+1.8VALW_PRIM TO +1.8VS

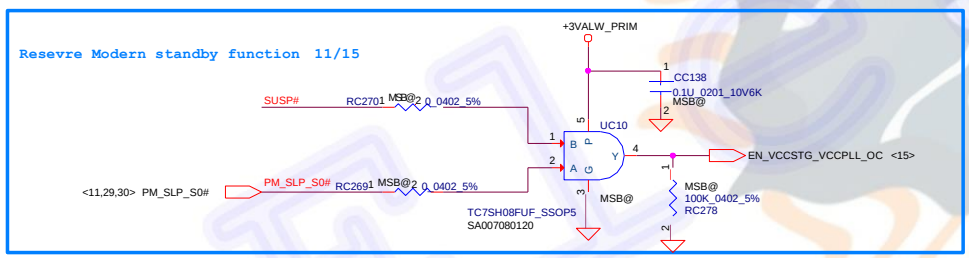
PVT UC5 Change to SA0000BEL00 3/28

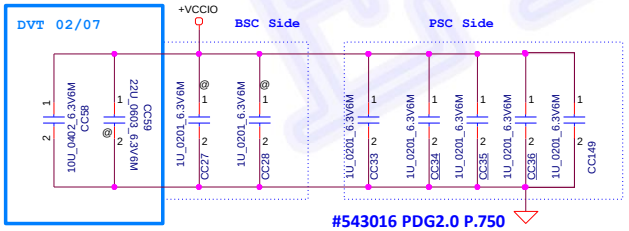


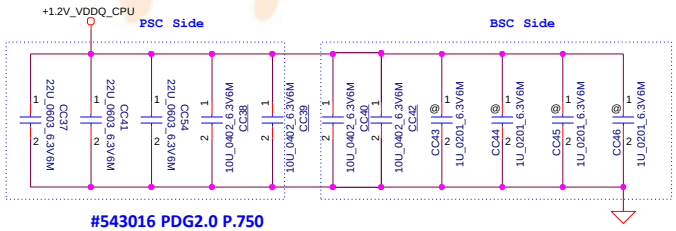
+1.0VALW_PRIM TO +1.0VS_VCCSTG











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Compal Electronics, Inc.

Title: KBL-U(8/12)Power

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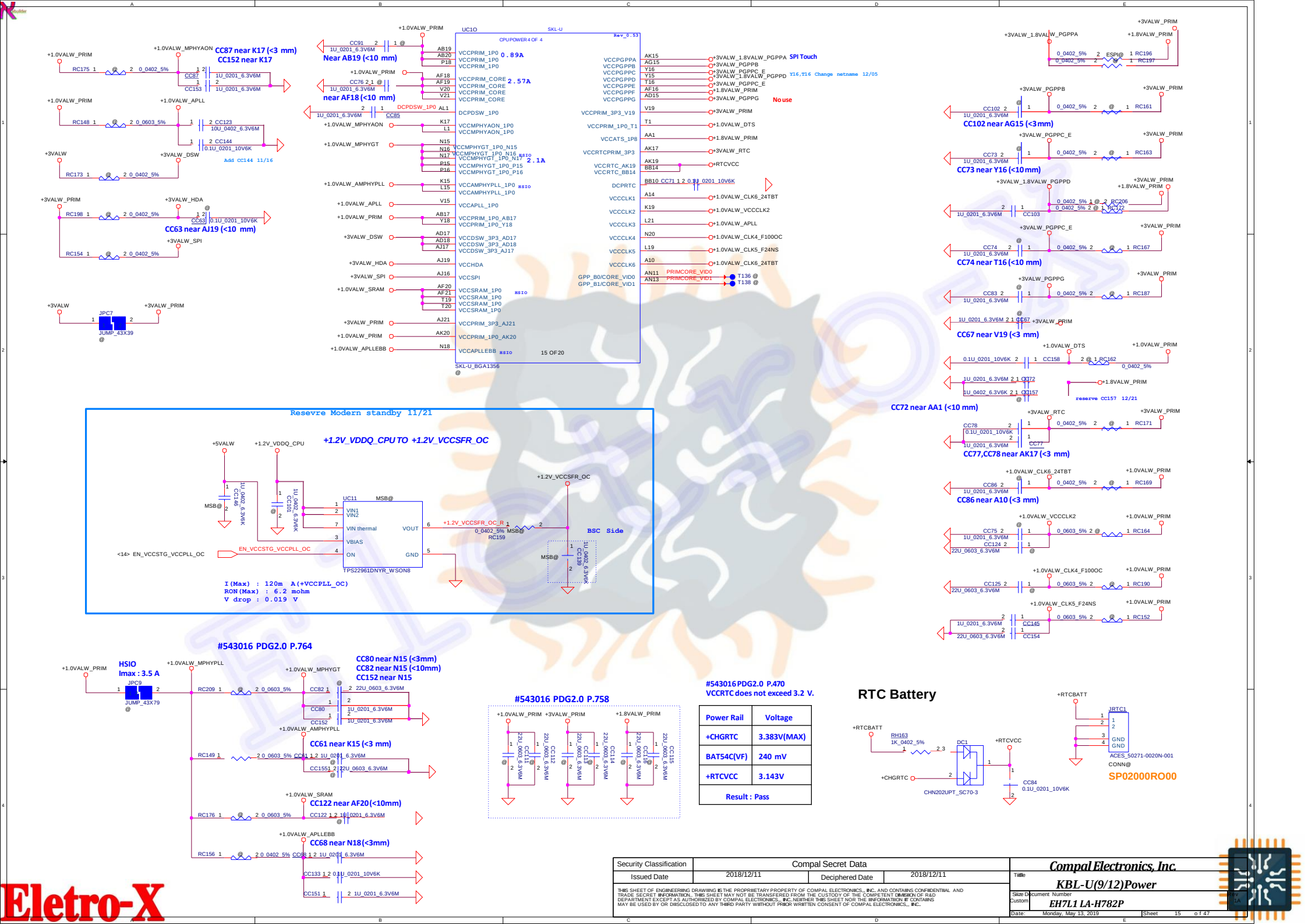
Date: Monday, May 13, 2019 | Sheet 14 of 47



#544924 SKL EDS1.2 P.134
VCC U(15W)-dual core GT2 29A(MAX)
0.55-1.52V

#544924 SKL EDS1.2 P.136
VCCGT U(15W)-dual core GT2 31A(MAX)
0.55-1.5V

#544924 SKL EDS1.2 P.141
VCCOPC 1.0V 3.2A
VCC_OPC_1P8 1.8V 50mA
VCCEOPIO 0.8V,1.0V 2A

For CPU2+3e SKU

Trace Length < 25 mils

+1.0VS(SUSP#)

+VCC_GT_VCORE (10pin)
U22 --> +VCC_GT
U42 --> +VCC_CORE

+VCC_GTX_VCORE(12 pin)
U22 --> NC
U42 --> +VCC_CORE
U23e-> +VCC_GT

569110 U42/U22 common
baord K52/AK52 NC

CPU2+3e fuse down SKU
+VCC_GTX_GT (16 pin)
U22 / U42--> NC U23e-> +VCC_GT

Trace Length < 25 mils

#543016 PDG2.0 P.273

Place the PU resistors close to CPU

To VR

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Title: KBL-U(10/12)Power,SVID

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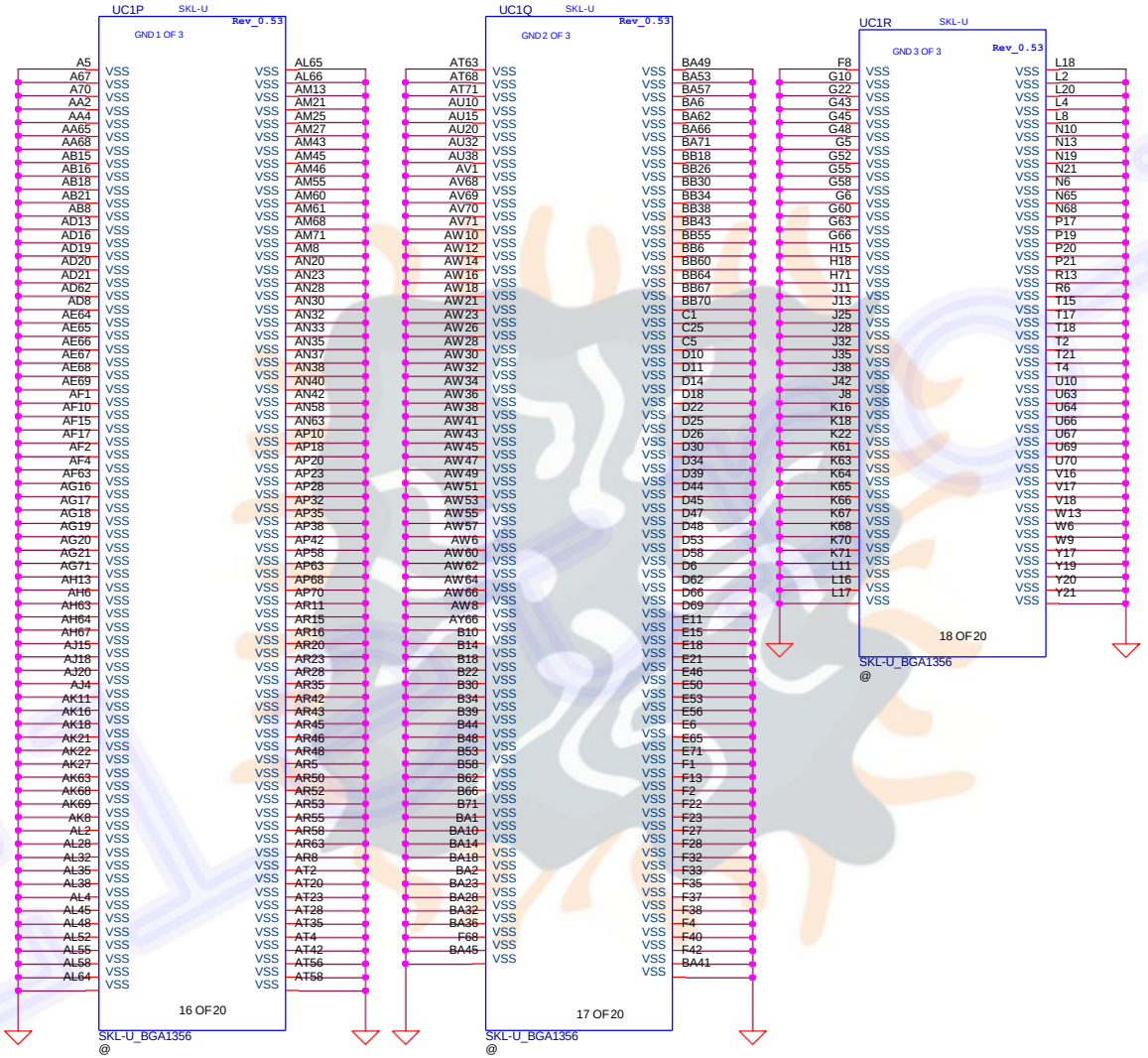
Date: Monday, May 13, 2019 | Sheet 16 of 47



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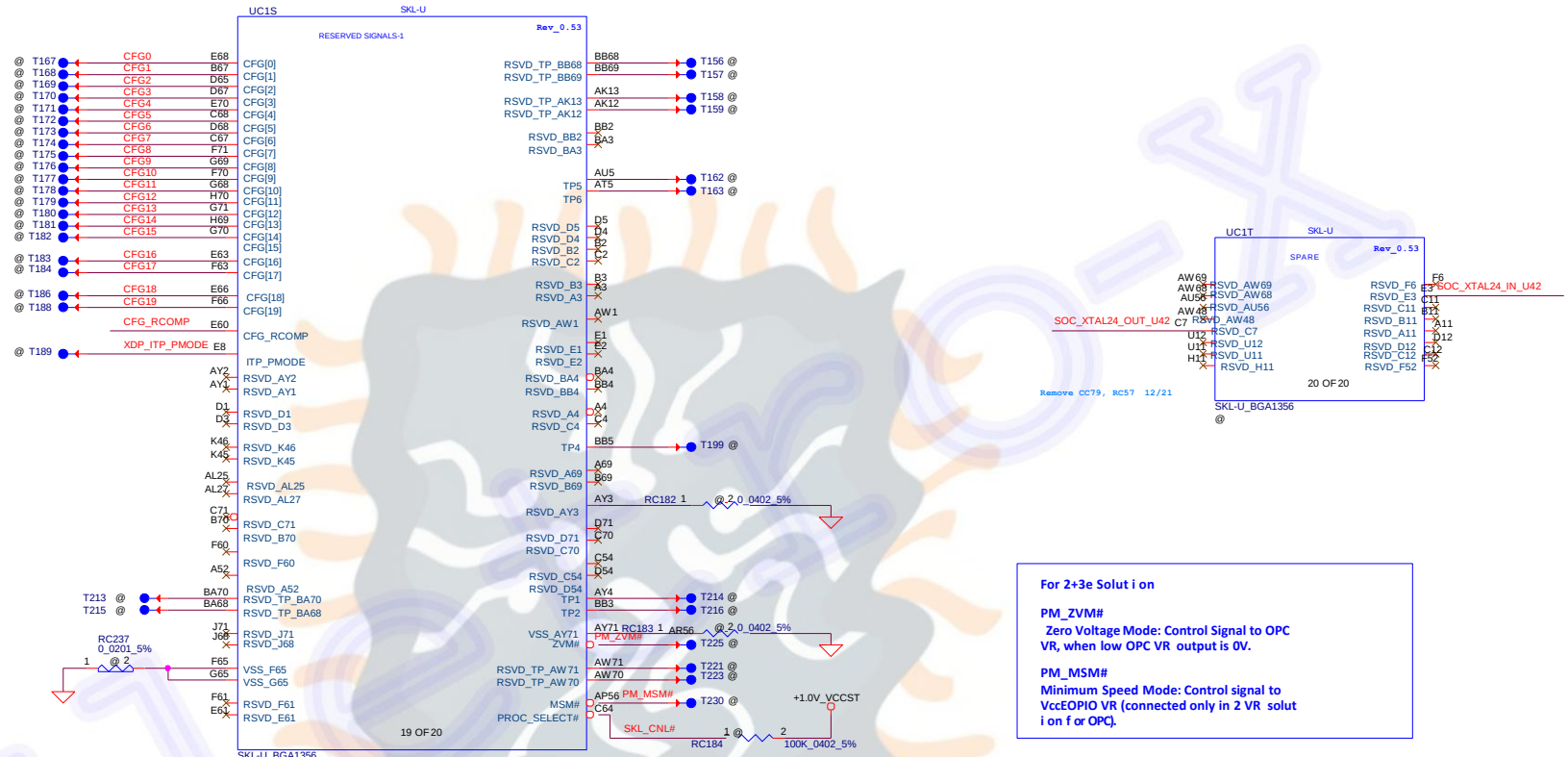
Compal Electronics, Inc.

Title: **KBL-U(11/12)GND**

Size: Custom | Document Number: **EH7L1 LA-H782P** | Rev: 1A

Date: Monday, May 13, 2019 | Sheet 17 of 47



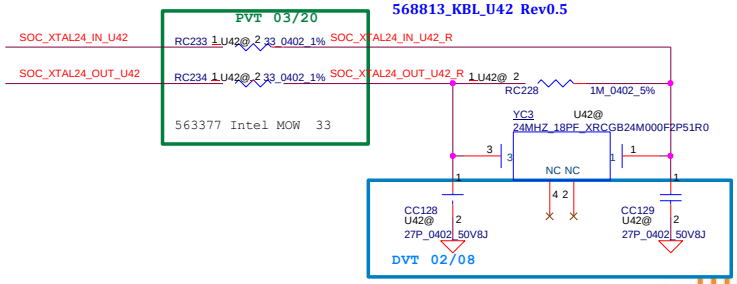
For 2+3e Solut i on

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solut i on f or OPC).

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at t ached t o E mbedded Ds play Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



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Issued Date	2018/12/11	Deciphered Date	2018/12/11

Compal Electronics, Inc.

Title: KBL-U(12/12)RSVD

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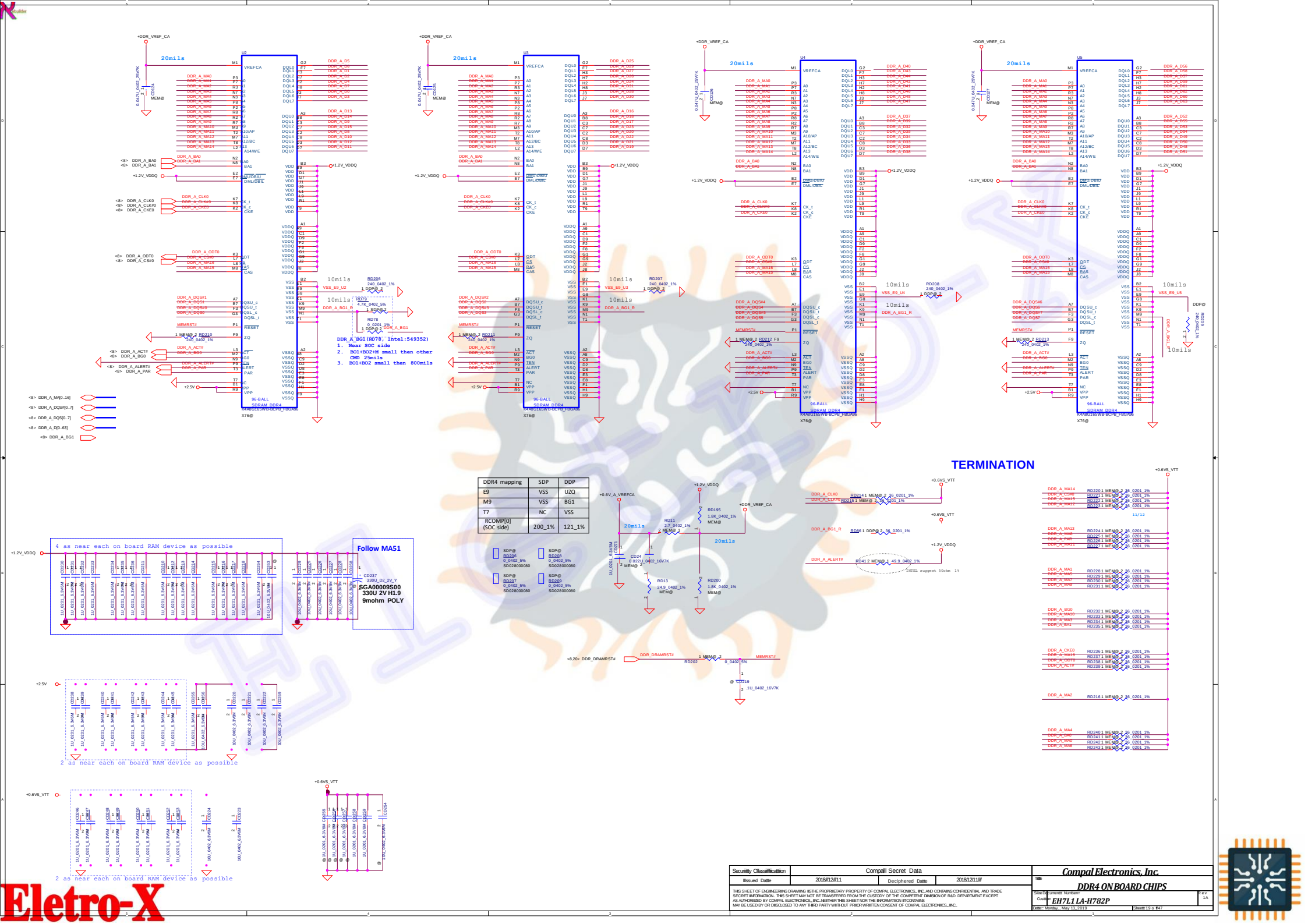
Date: Monday, May 13, 2019 | Sheet 18 of 47



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Compal Electronics, Inc.

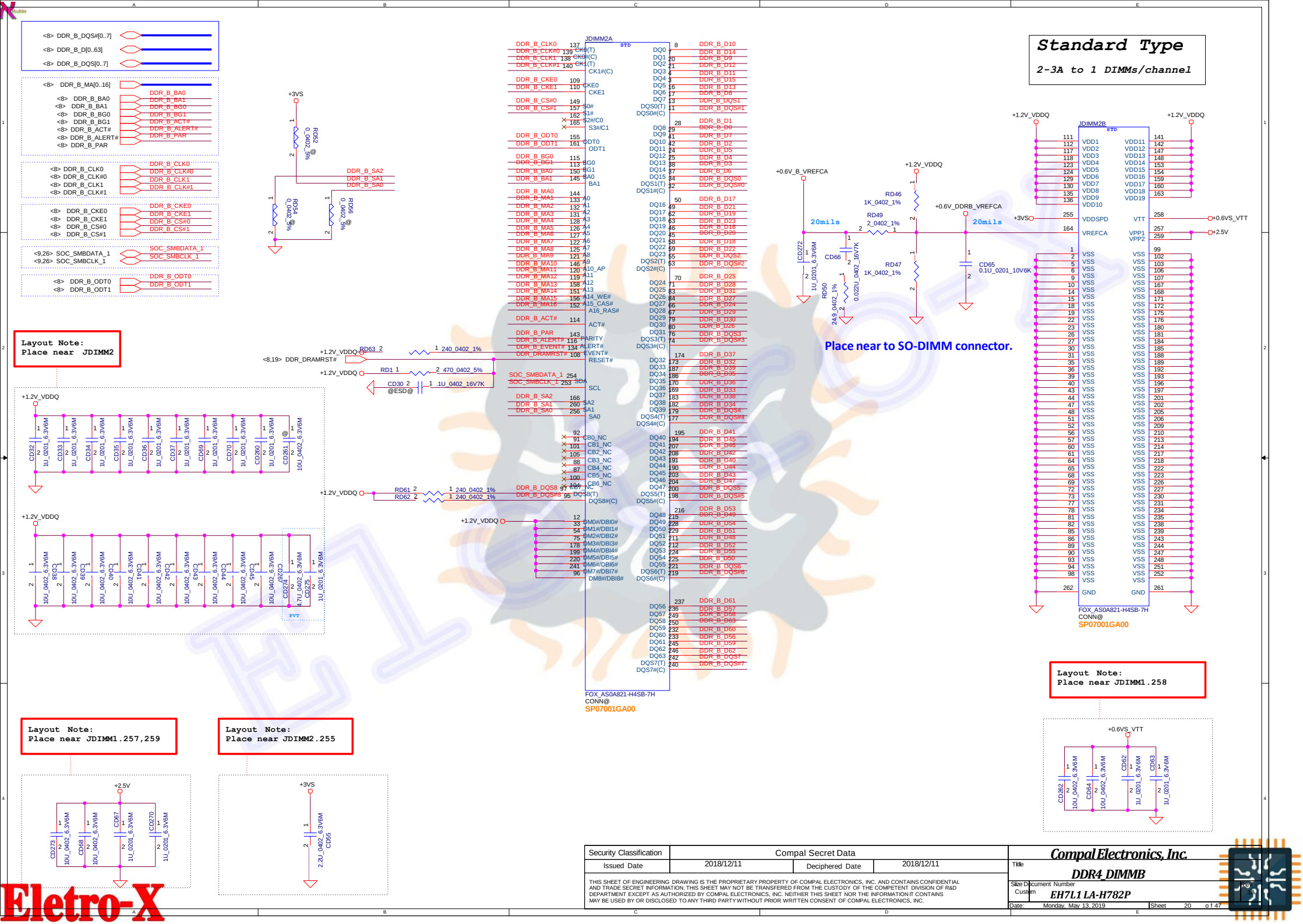
Title: DDR4 ON BOARD CHIPS

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1A

Date: Monday, May 13, 2019 | Sheet 19 of 47

Standard Type

2-3A to 1 DIMMs/channel



Security Classification	Compal Secret Data		
Issued Date	2018/12/11	Deciphered Date	2018/12/11

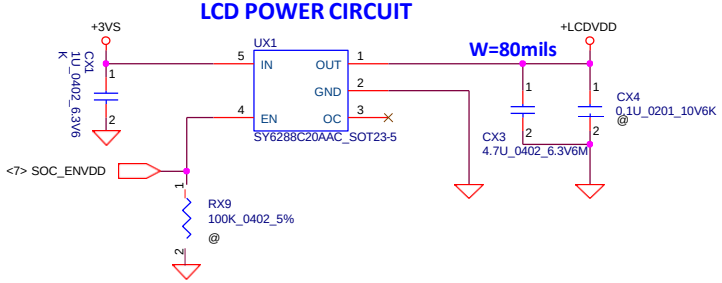
Compal Electronics, Inc.

Title: DDR4_DIMMB

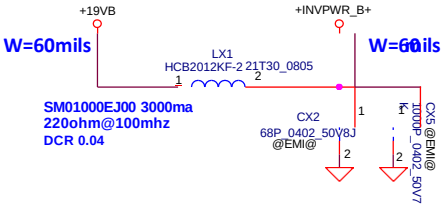
Size: Custom | Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 | Sheet 20 of 47

LCD POWER CIRCUIT

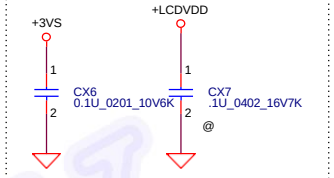


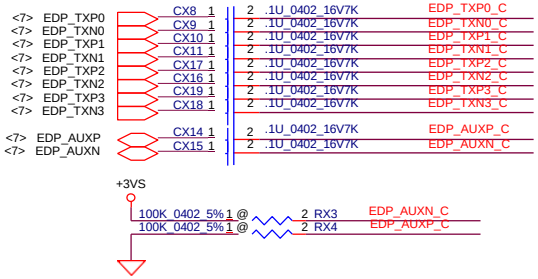
Change to +19VB 11/16

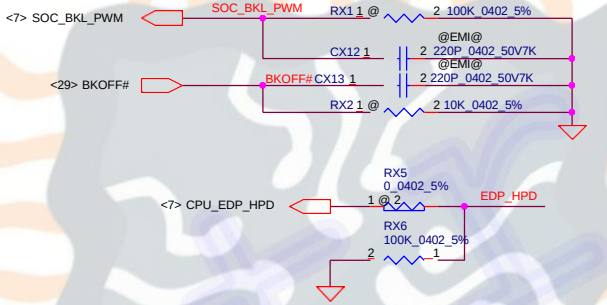


Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

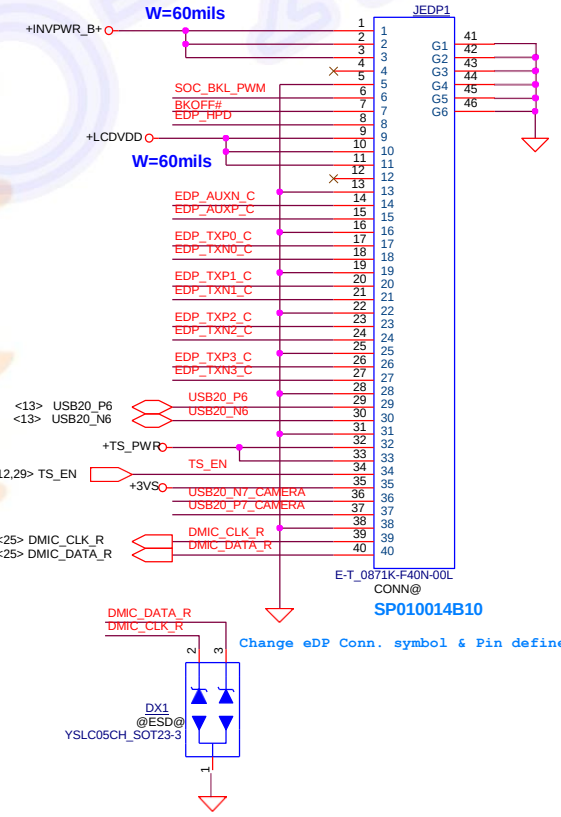
Place closed to JEDP1





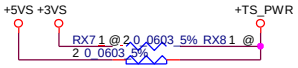


LED PANEL Conn.

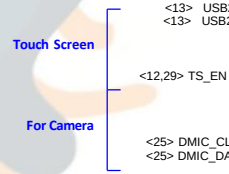


Change eDP Conn. symbol & Pin define 11/20

Touch Screen



Camera



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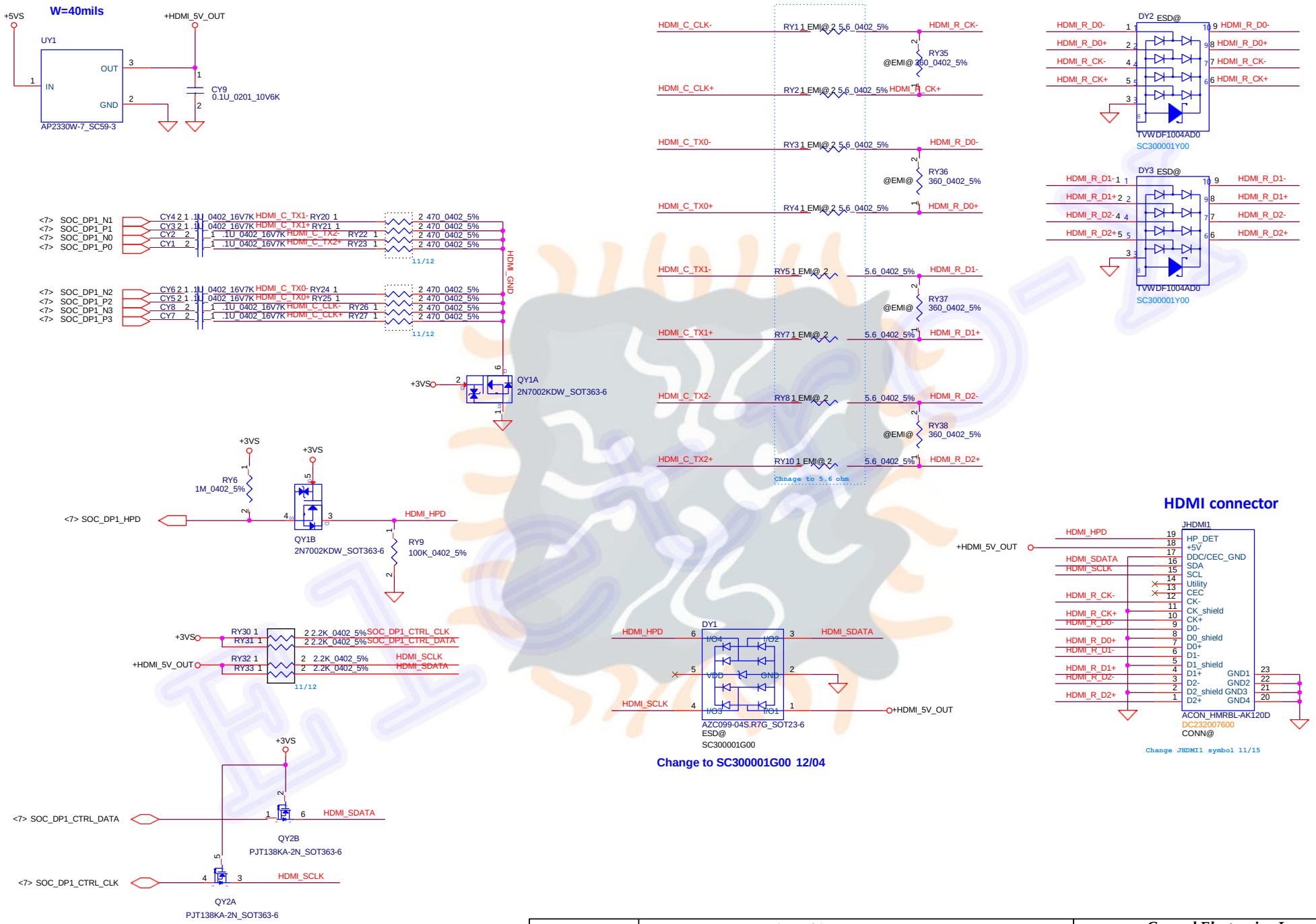
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	eDP Connector
Size / Document Number	EH7L1 LA-H782P
Custom	Rev 1.0
Date: Monday, May 13, 2019	Sheet 21 of 47



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

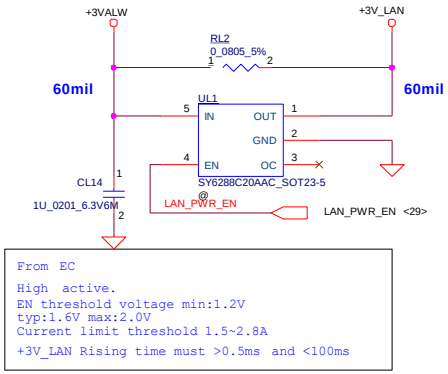
Compal Electronics, Inc.

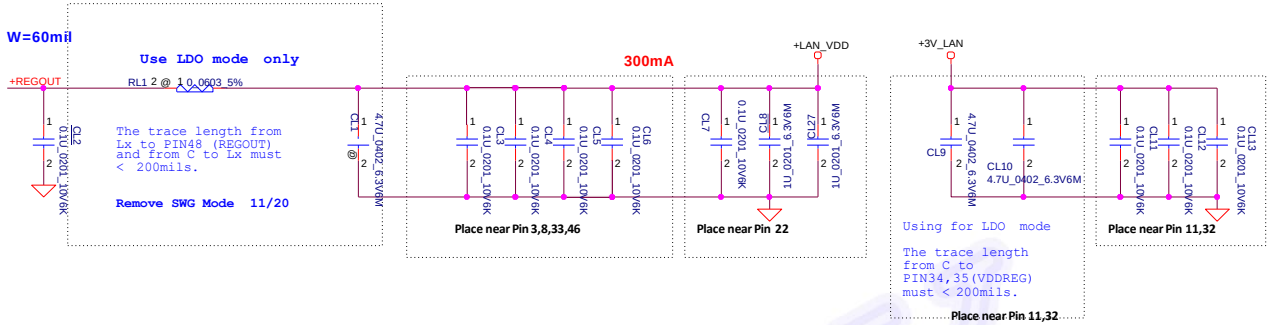
Title: HDMI CONN.

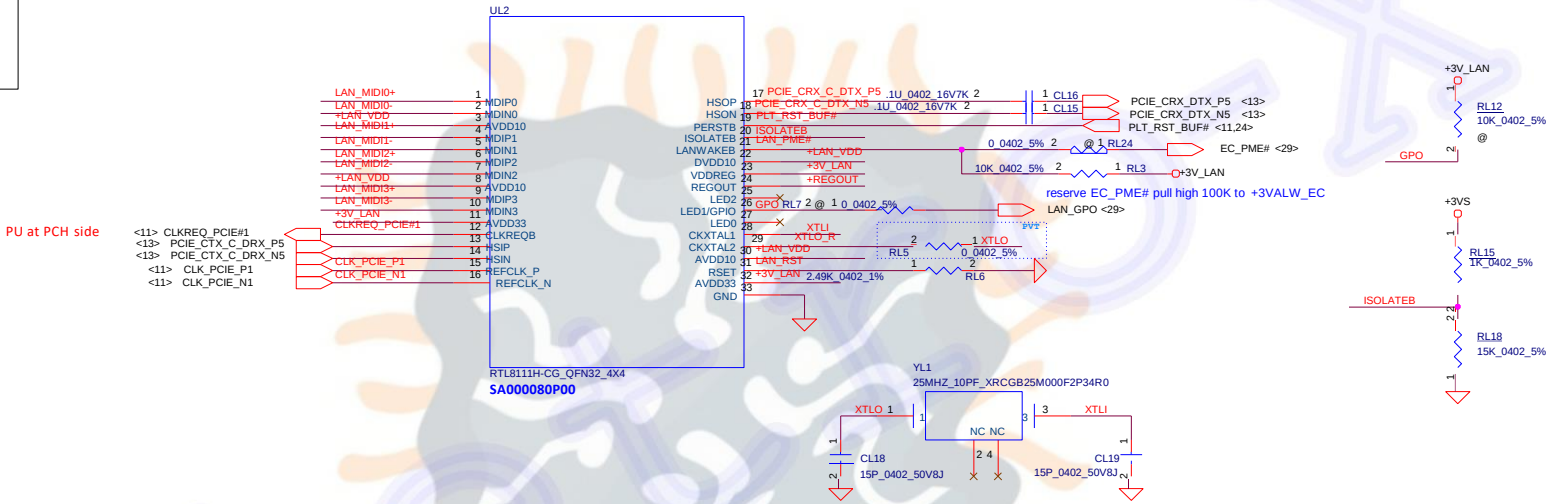
Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

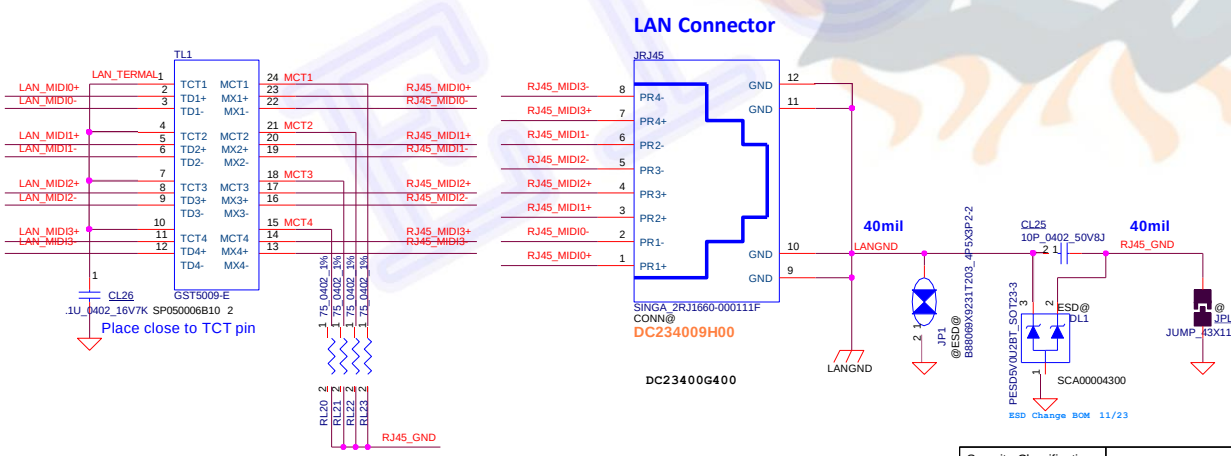
Date: Monday, May 13, 2019 | Sheet 22 of 47

LAN-RTL8111H









LAN Connector

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **LAN RTL8111H**

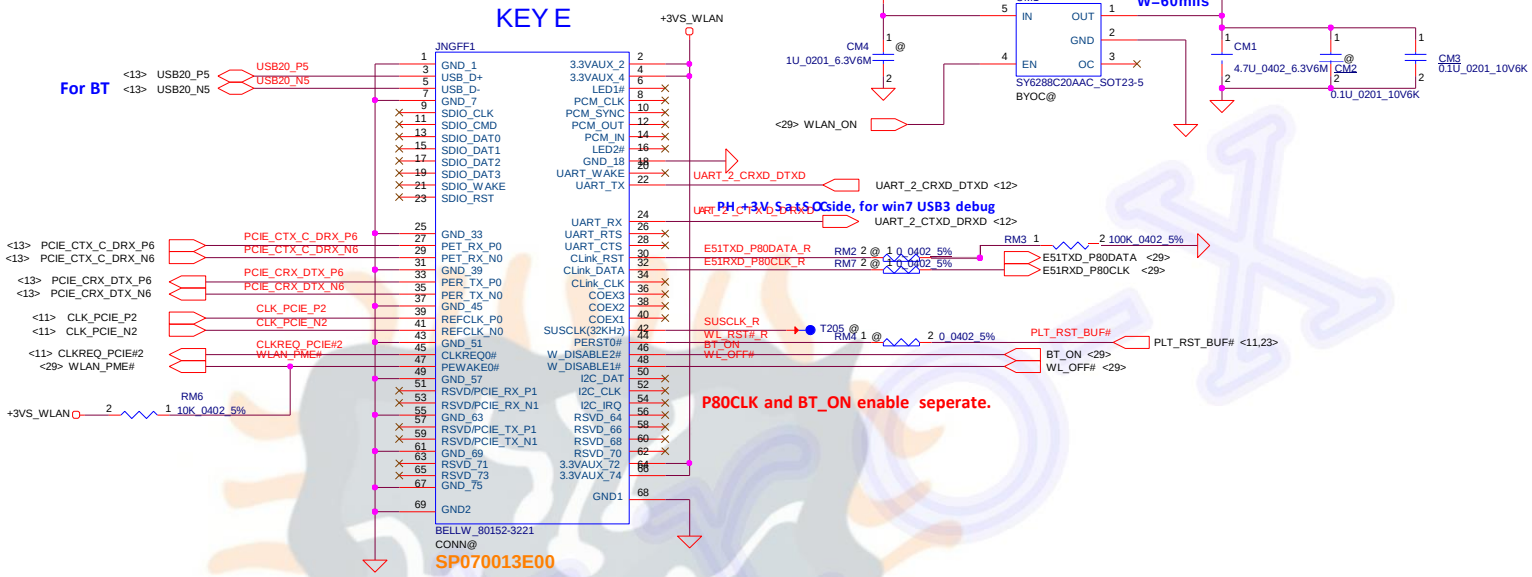
Size: Custom | Document Number: **EH7L1 LA-H782P**

Date: Monday, May 13, 2019 | Sheet 23 of 47

Wireless LAN

NGFF WL+BT (KEY E)

KEY E



mSATA/SSD

KEY M

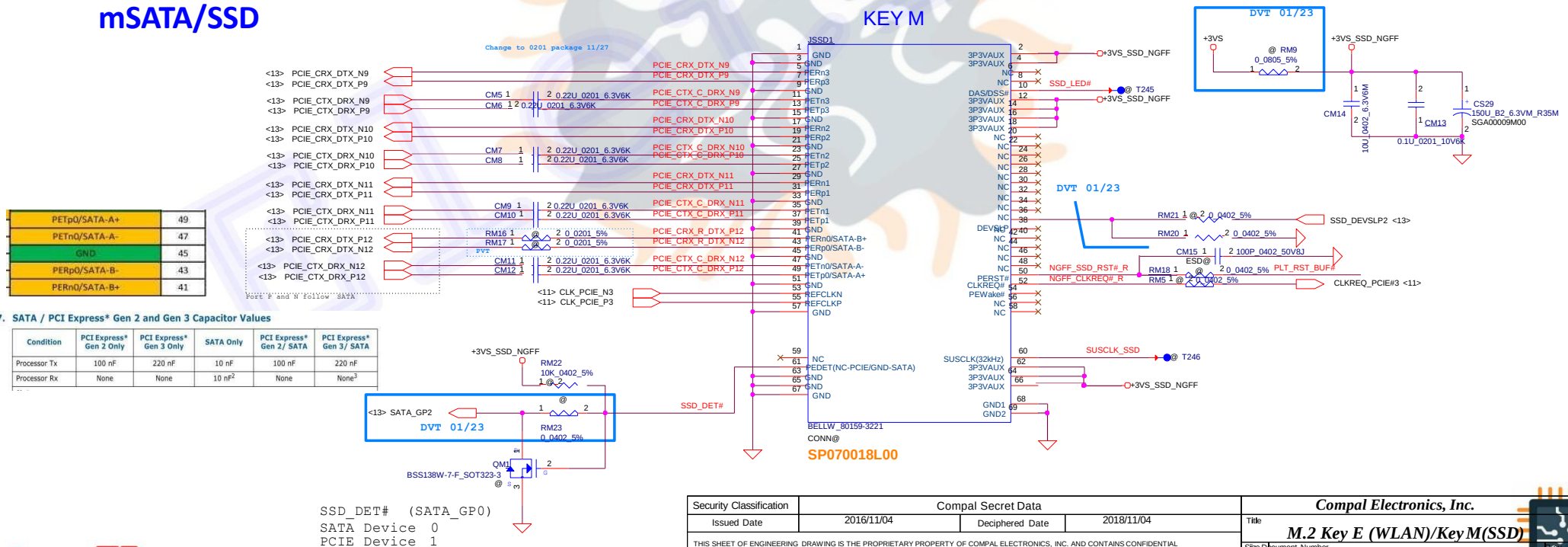


Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

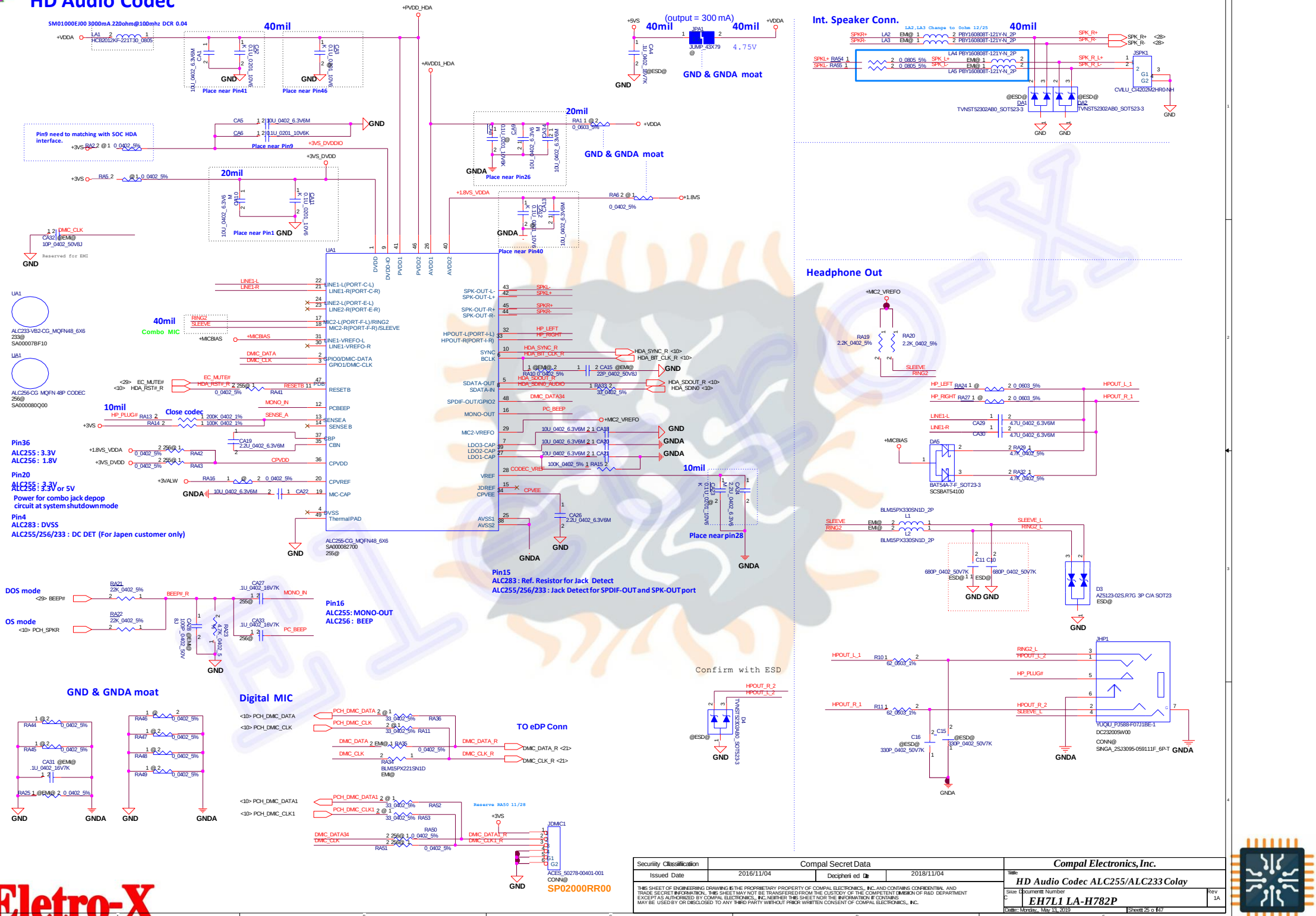
Compal Electronics, Inc.

Title: M.2 Key E (WLAN)/Key M(SSD)

Size: Custom | Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 | Sheet 24 of 47

HD Audio Codec



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Compal Electronics, Inc.

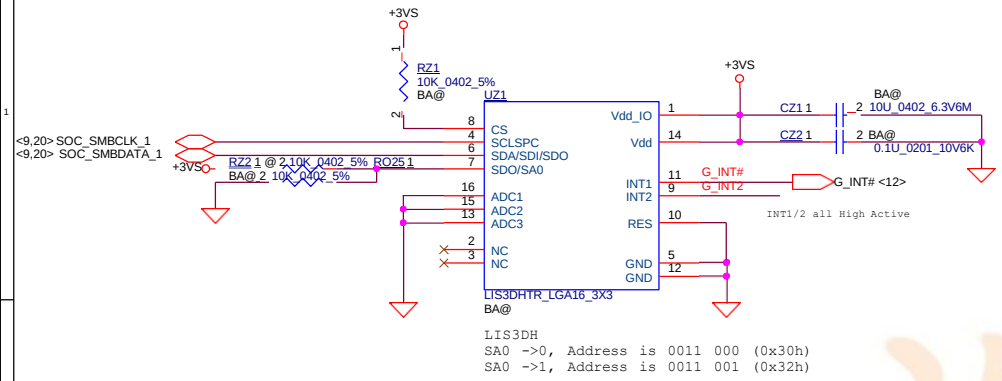
Title: *HD Audio Codec ALC255/ALC233 Colay*

Size	Document Number	Rev
C	*EH7L1 LA-H782P*	1A

Date: Monday, May 13, 2019 Sheet 25 of 47

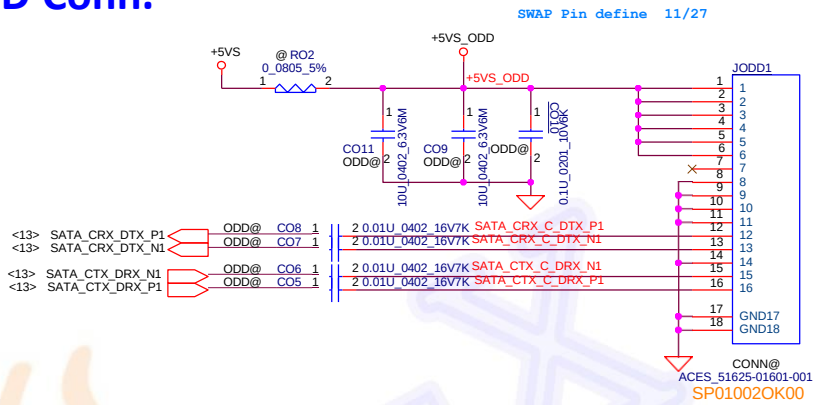
Eletro-X

G-Sensor reserved for BA serial

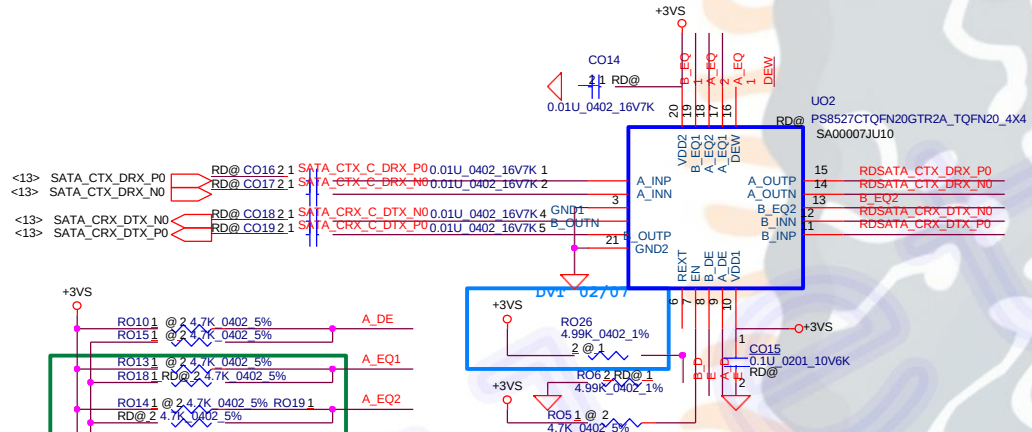


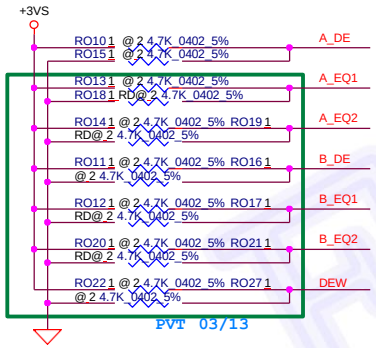
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

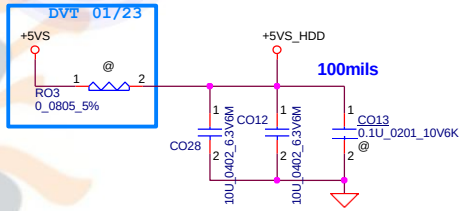
SATA ODD Conn.

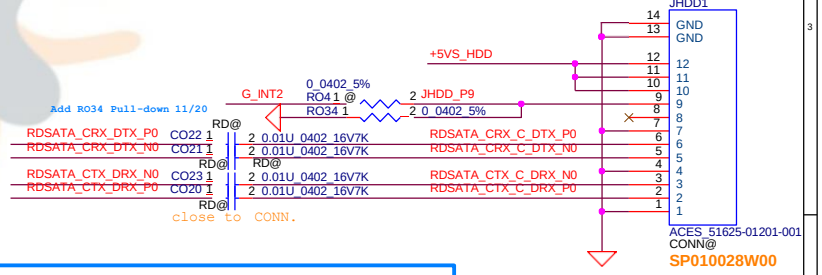


SATA Re-Driver and cable HDD Conn.





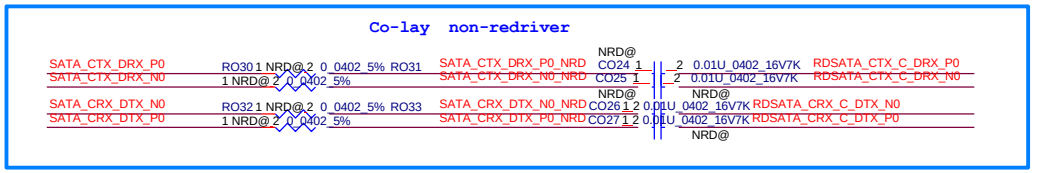




PS8527C EQ and DE

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
* L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

A_DE	De_Emphasis
* M	-3.5dB(Default)
L	0dB
H	-6dB



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

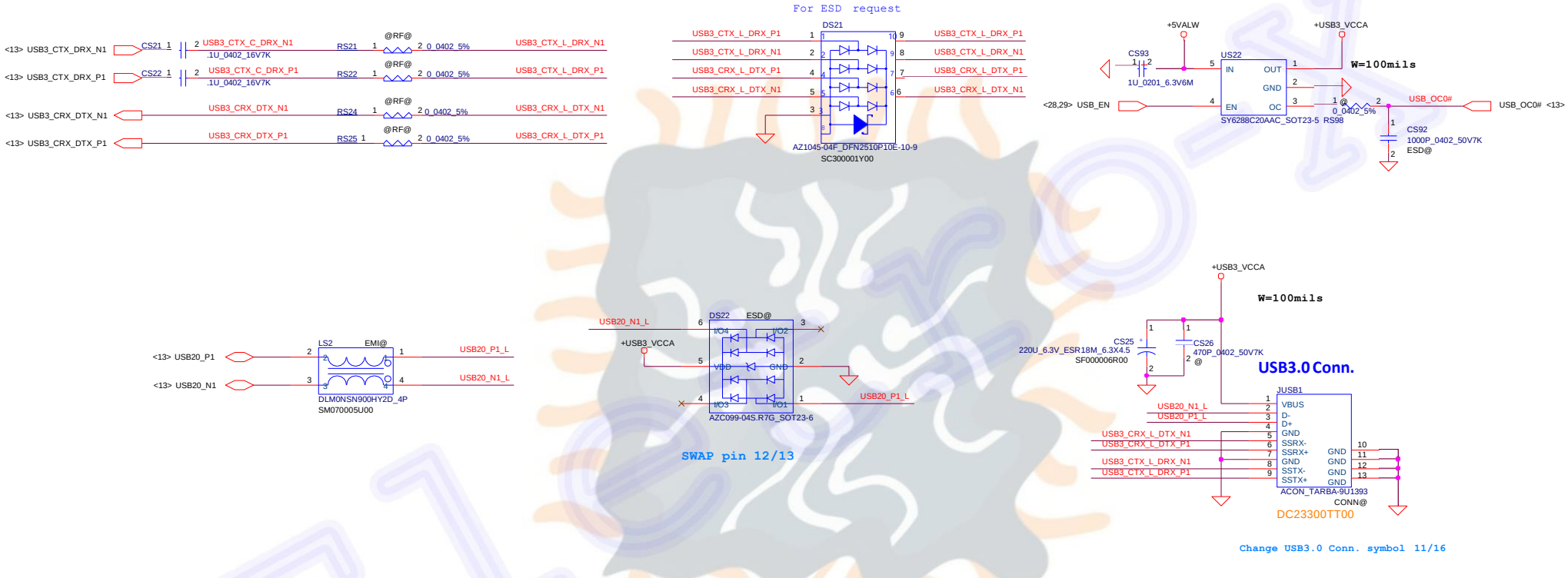
Compal Electronics, Inc.

Title: HDD/ODD/ HDD Re-Driver

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 26 of 47

USB3.0 (Port 1)



remove USB Charger IC 12/12

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

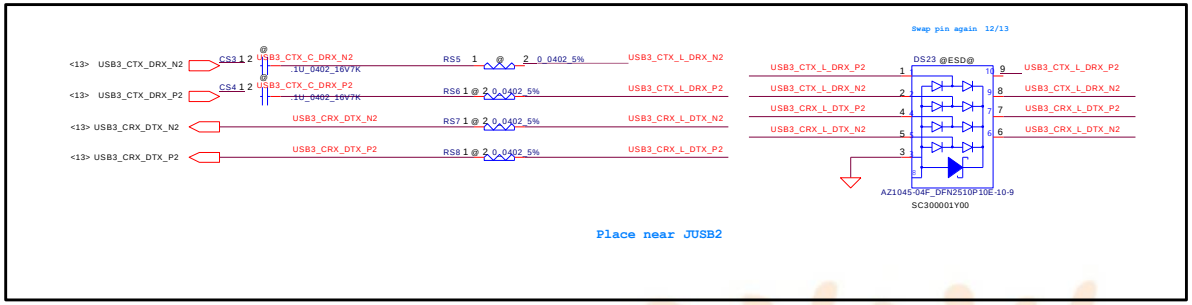
Compal Electronics, Inc.

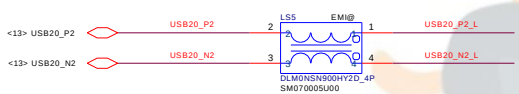
Title: USB Conn/USB_B

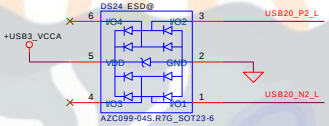
Size: Custom | Document Number: EH7L1 LA-H782P | Rev: A

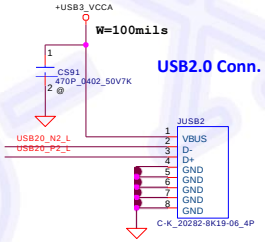
Date: Monday, May 13, 2019 | Sheet 27 of 47

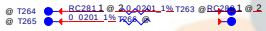
USB2.0 (Port 2)





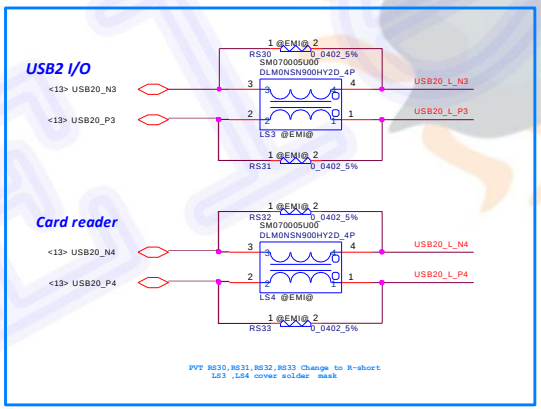


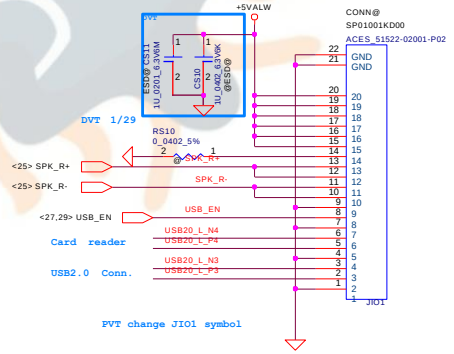




Change USB3.0 Conn. symbol
Reserve U3 first 11/16

USB/B (USBx1,Card Reader,SPK)





Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

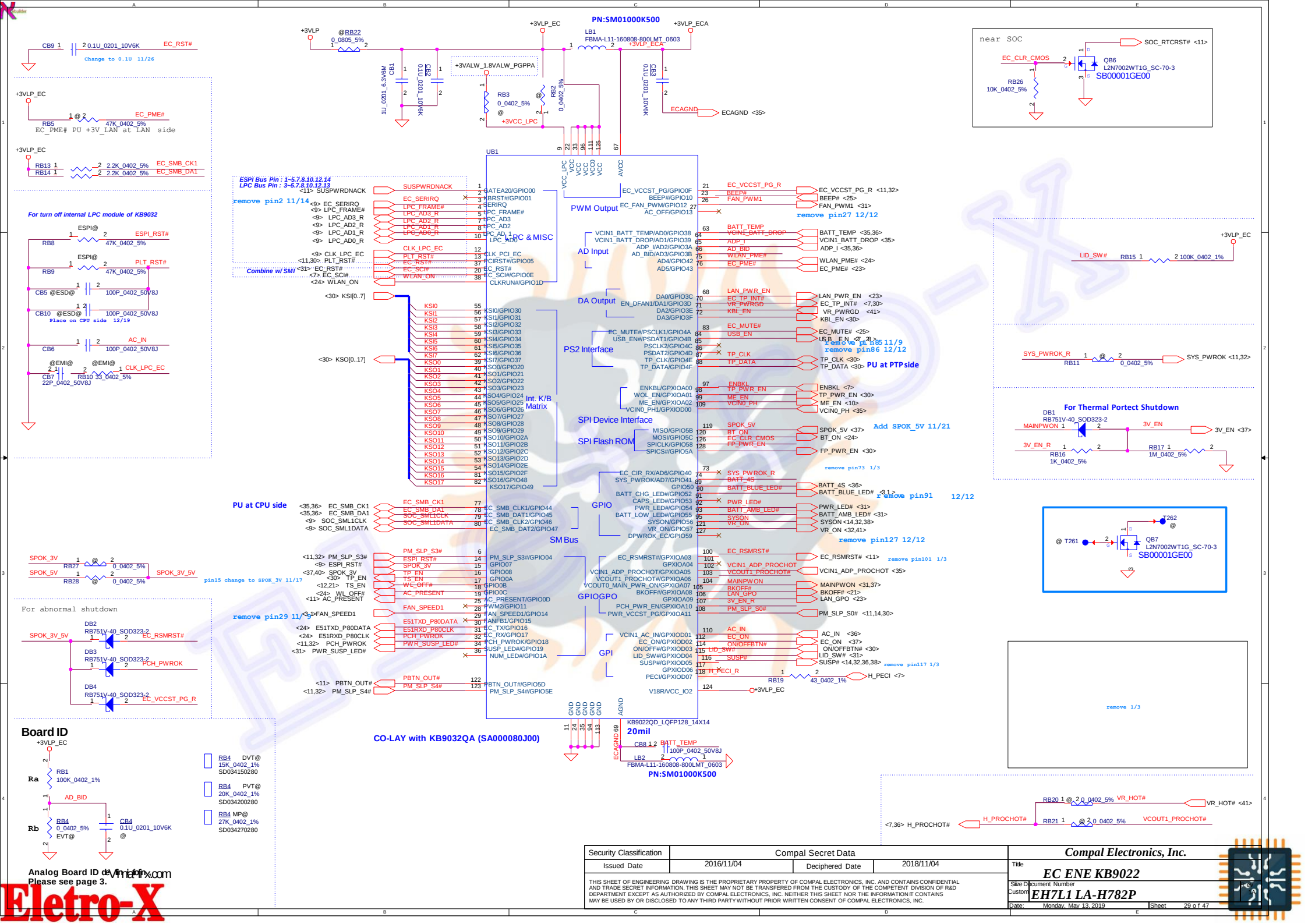
Title: USB2.0 / IO_B

Size: Document Number: EH7L1 LA-H782P

Rev: 1A

Custom:

Date: Monday, May 13, 2019 Sheet 28 of 42



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: EC ENE KB9022

Size: Custom | Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 | Sheet: 29 of 47

change Pin define same as EH5AW 11/16

ON/OFF BTN

RK1 100K_0402_5%
+3VLP
<29> ON/OFFBTN#
ON/OFFBTN#

PVT Remove SWK1 3/27

KSI[0..7]
KSO[0..17]
KSI[0..7] <29>
KSO[0..17] <29>

KB Conn.

JKB1 ACES_85201-2805 CONN@
GND2 GND1
KSO16 KSO17 KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
ON/OFFBTN#

SP01000GO00

KB BackLight

+5VS
U1 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
<29> KBL_EN
+5VS_BL
JBL1 ACES_51524-0040N-001 CONN@
GND GND
C3 0.1U_0201_10V6K

SP010022M00

TP/B Conn.

+3VALW
+3VS
RK3 0_0402_5%
+3V_PTP
UK1 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
CK13 1U_0201_6.3V6M
CK3 1U_0201_6.3V6M
CK1 4.7U_0402_6.3V6M
RK4 10K_0402_5%
EC_TP_INT#
TP_PWR_EN <29>

TP_PWR_EN follow SYSON behavior

EC PS2
PCH I2C
<7,29> EC_TP_INT#
<29> TP_EN
@ CK2 0.1U_0201_10V6K
JTP1 ACES_51524-00801-001 CONN@
TP_CLK TP_DATA I2C_1_SDA_R I2C_1_SCL_R EC_TP_INT# TP_EN GND GND

SP01001A910

QK1B 2N7002KDW_SOT363-6
RK7 2.2K_0402_5%
RK10 2.2K_0402_5%
<12> I2C_1_SCL
I2C_1_SCL_R
RK8 @ 0_0402_5%
QK1A 2N7002KDW_SOT363-6
<12> I2C_1_SDA
I2C_1_SDA_R
RK9 0_0402_5%

RK5 4.7K_0402_5%
RK6 4.7K_0402_5%
<29> TP_CLK
<29> TP_DATA
TP_CLK
TP_DATA

TPM

change TPM to NPCT750 11/16

+3VALW
RW1 0_0603_5%
+3VALW_TPM
near pin1
+3VS
RW2 0_0603_5%
+3VS_TPM
near pin8,22

+3VALW_TPM
RW10 10K_0402_5% TPM_PIRQ#

<9> SOC_SPI_SO
<9> SOC_SPI_SI
<9> SOC_SPI_CLK
SOC_SPI_SO RW5 33_0402_5% SOC_SPI_SO_TPM_R
SOC_SPI_SI RW6 33_0402_5% SOC_SPI_SI_TPM_R
SOC_SPI_CLK RW7 33_0402_5% SOC_SPI_CLK_TPM_R

UW1 place close and before UC7

UW1 TPM@ NPCT750AAAYX_QFN32_5X5
<11,14,29> PM_SLP_S0#
RW11 0_0402_5%
SDA/GPIO0
SCL/GPIO1
GPIO3
MISO
MOSI/GPIO7
PIRQ/GPIO2
<13> TPM_PIRQ#
SCLK
SCS/GPIO5
<9> SOC_SPI_CS#2
<11,29> PLT_RST#
PLTRST
GPIO4
PP/GPIO6
VSB VHIO
GND GND PGND

SA0000AQ230 S IC NPCT750AAAYX QFN 32P TPM
SA0000AQ250 S IC NPCT750AABYX QFN 32P TPM

Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

+3VALW
+5VALW
RK16 FP@ 0_0603_5%
RK17 FP@ 0_0603_5%
UK6 SY6288C20AAC_SOT23-5
IN OUT GND EN OC
FP@ CK11 1U_0201_6.3V6M
+FP_VCC
FP@ CK12 4.7U_0402_6.3V6M
FP_PWR_EN <29>

<13> USB20_N8
<13> USB20_P8
USB20_N8
USB20_P8
LK2 FPEMC@ DLM0NSN900HY2D_4P SM070005U00
USB20_N8_L
USB20_P8_L

DK2 FPEMC@ AZC099-04S.R7G_SOT23-6
I/O4 I/O2 VDD GND I/O3 I/O1

+FP_VCC
SP010020S00 CONN@ JXT_FP201H-008G10M
USB20_P8_L
USB20_N8_L
JFP1
GND GND

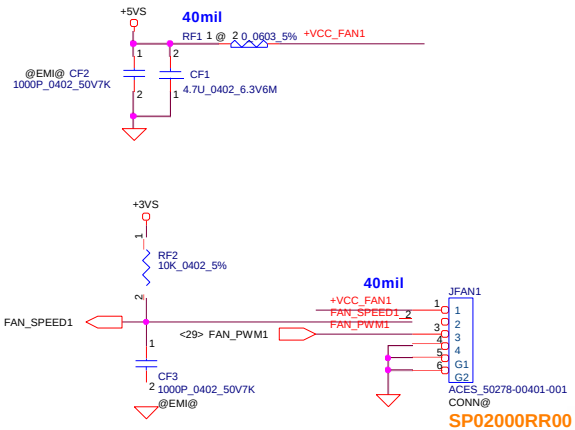
Update pin define 01/19

PIN	ETU801	SA464K-2200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.
Title: KB & TP & TPM & LID & FP
Size: Custom Document Number: EH7L1 LA-H782P
Date: Monday, May 13, 2019 Sheet 30 of 47

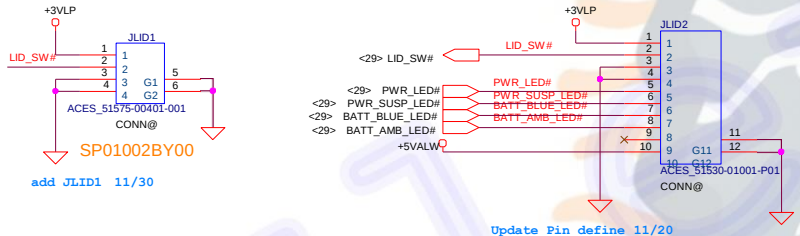
FAN1 Conn

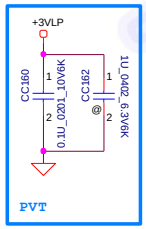


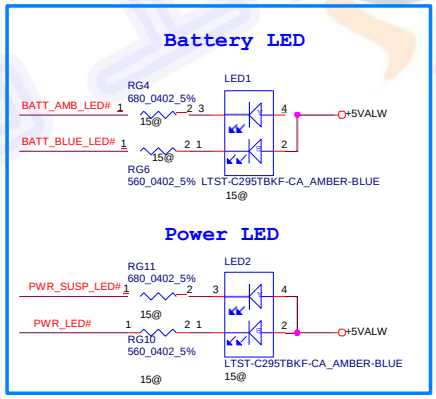
Screw Hole

Lid Switch

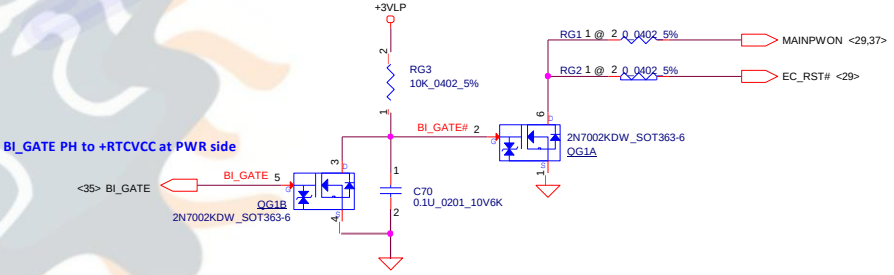
(Hall Effect Switch)



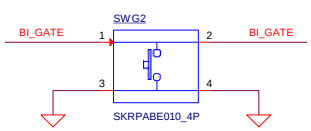




Reset Circuit



Reset Button



remove SWG1 11/27

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

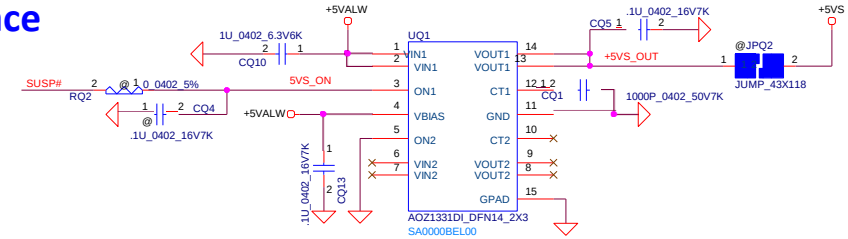
Compal Electronics, Inc.

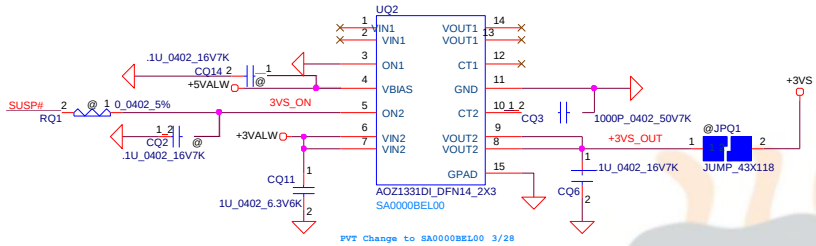
Title: FAN &LID& Screw Hole & Reset

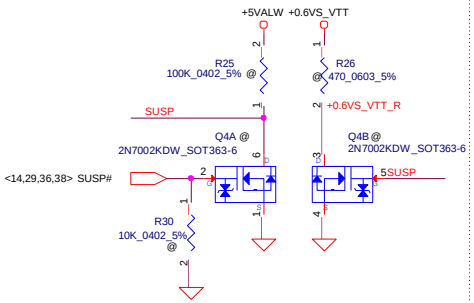
Size: Custom | Document Number: EH7L1 LA-H782P

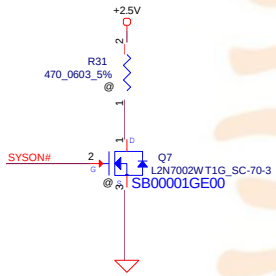
Date: Monday, May 13, 2019 | Sheet 31 of 47

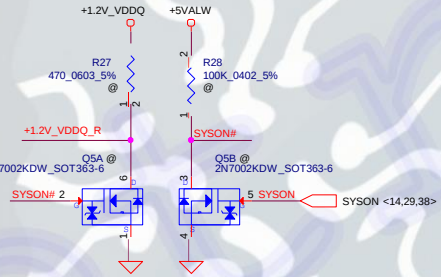
DC Interface



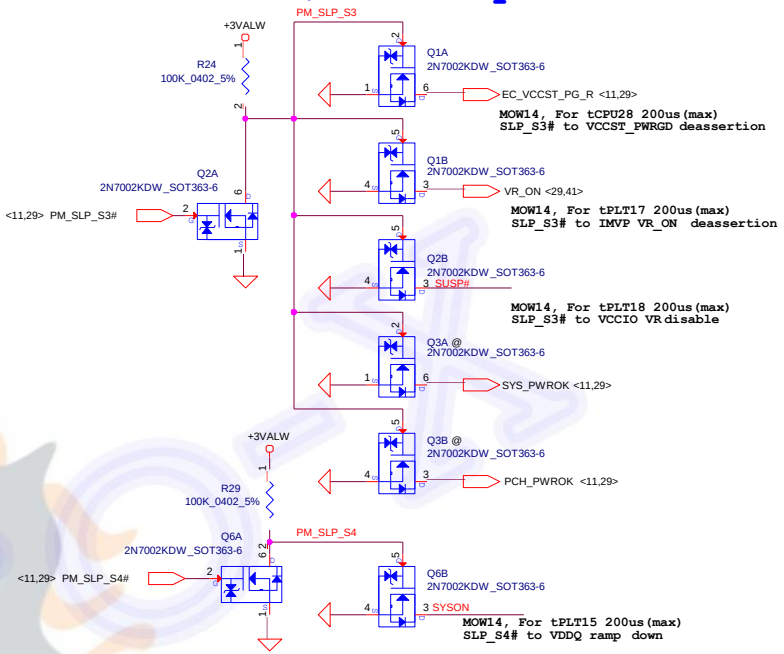








For Power ON/Off Sequence



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: EH7L1 LA-H782P

Date: Monday, May 13, 2019 | Sheet 32 of 47

Kabylake_U22 CPU Part Number

HDCP2.2

- UC1 SR343@ CPU_KBL_H0_i3-7100U_2.4G SA0000A38M0
- UC1 SR343BR@ CPU_KBL_H0_i3-7100U_2.4G SA0000A38O0
- UC1 SR342@ CPU_KBL_H0_i5-7200U_2.5G SA0000A37N0
- UC1 SR342BR@ CPU_KBL_H0_i5-7200U_2.5G SA0000A37O0
- UC1 SR341@ CPU_KBL_H0_i7-7500U_2.7G SA0000A34L0
- UC1 SR341BR@ CPU_KBL_H0_i7-7500U_2.7G SA0000A34M0
- UC1 SR3JY@ CPU_KBL_H0_i3-7130U_2.7G SA0000B2Y70
- UC1 SR3TK@ CPU_KBL_H0_i3-7020U_2.3G SA0000BLH60

Kabylake_R U42 CPU Part Number

- UC1 SR3LA@ CPU_KBL_Y0_U42_I5-8250U_1.6G SA0000AWB40
- UC1 SR3LABR@ CPU_KBL_Y0_U42_I5-8250U_1.6G SA0000AWB90
- UC1 SR3LC@ CPU_KBL_Y0_U42_I7-8550U_1.8G SA0000AWC40
- UC1 SR3LCBR@ CPU_KBL_Y0_U42_I7-8550U_1.8G SA0000AWC70

PCB Number

- ZZZ PCB@ PCB 2MD LA-H782P REV0 MB 3 DA60026S000
- ZZZ UMADAZ10@ PCB EH7L1 LA-H782P LS-H781P/H783P/H784P DAZ2MD00200
- ZZZ UMADAZ1A@ PCB EH7L1 LA-H782P LS-H781P/H783P/H784P DAZ2MD00202

Kabylake_RU22 CPU Part Number

- UC1 SR3W 0@ CPU_KBL_Y0_RU22_I3-8130U_2.2G SA0000BKN60
- UC1 SR3W 0BR@ CPU_KBL_Y0_RU22_I3-8130U_2.2G SA0000BKN70
- UC1 SR3LD@ CPU_KBL_Y0_RU22_I3-7020U_2.3G SA0000BLD70

Kabylake_U23E Fuse Down CPU

- UC1 SR3N6@ CPU_KBL_J1_i3-7020U_2.3G SA0000BVB10
- UC1 QNMU@ CPU_KBL_J1_i3-7020U_2.3G QS SA0000BVB00

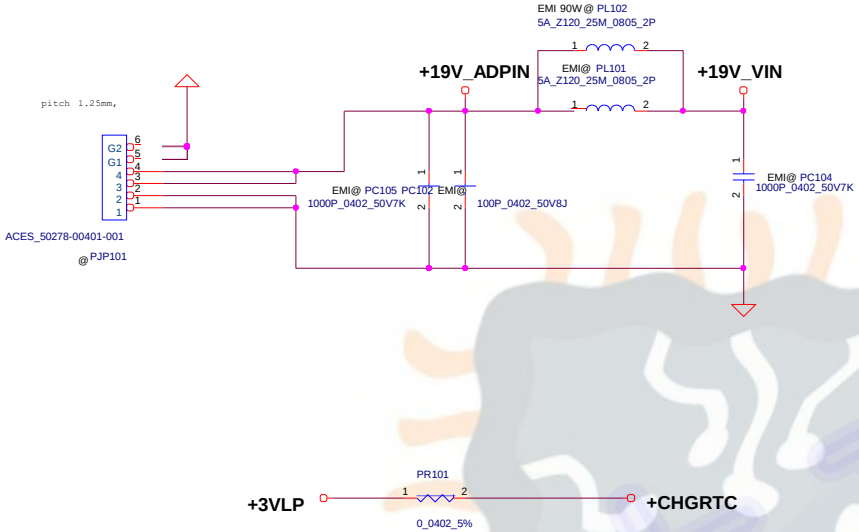
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: CPU/X76 BOM

Size: Custom | Document Number: EH7L1 LA-H782P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 33 of 47



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

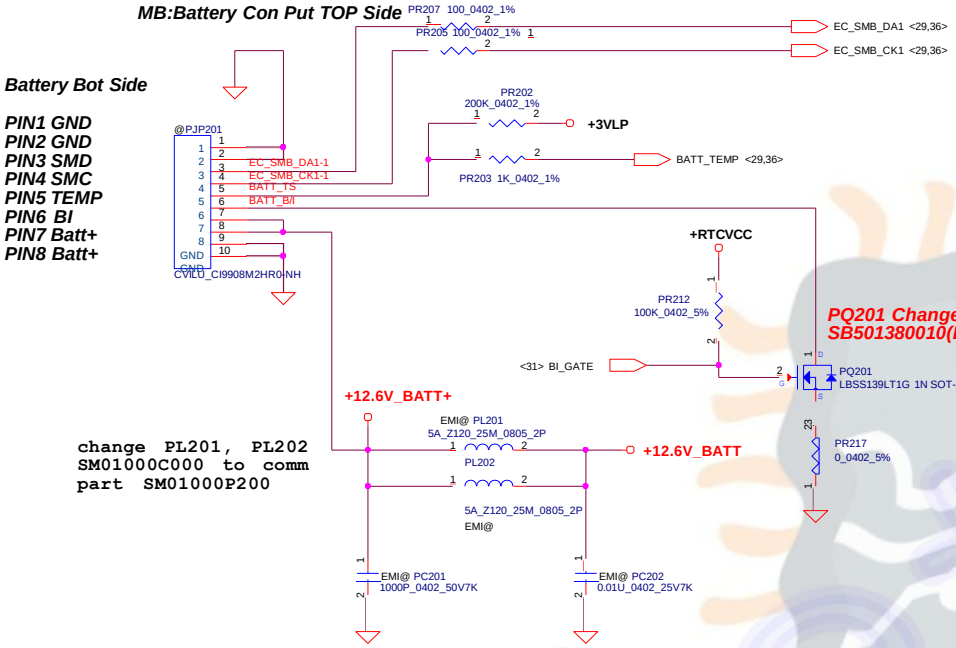
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: EH5AW M/B LA-G521P

Date: Monday, May 13, 2019 | Sheet 34 of 47

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200

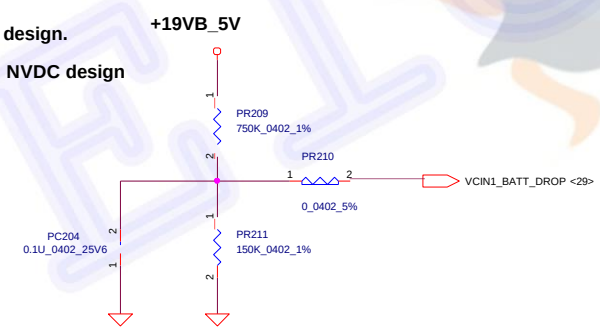
2016/11/16 update

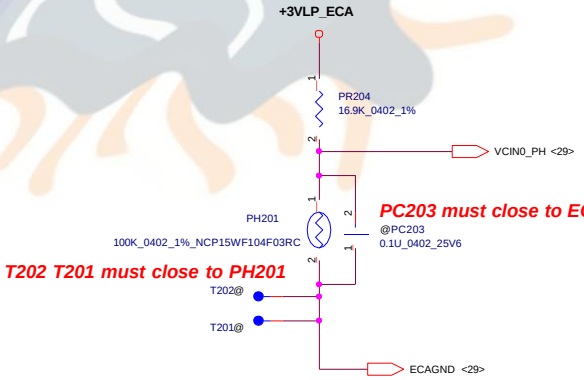
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm	58.5W,0.61V	Active=recovery
65W PR206 19.1K ohm	84.5W,0.61V	Active=recovery
90W PR206 30.1K ohm	117W,0.61V	Active=recovery
PH1	2V	1V

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

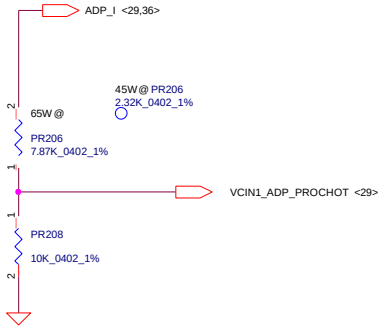
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





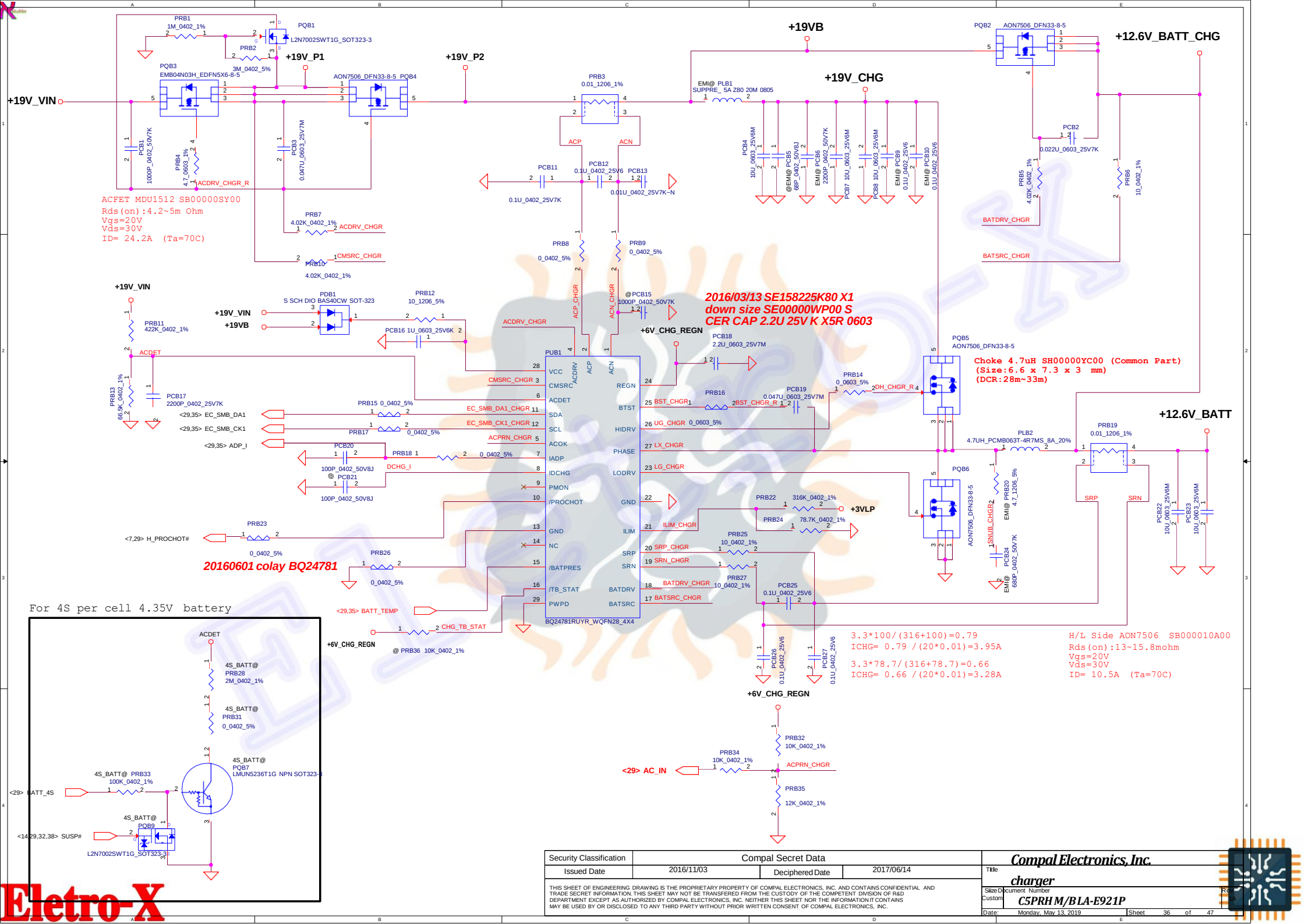
PC203 must close to EC pin

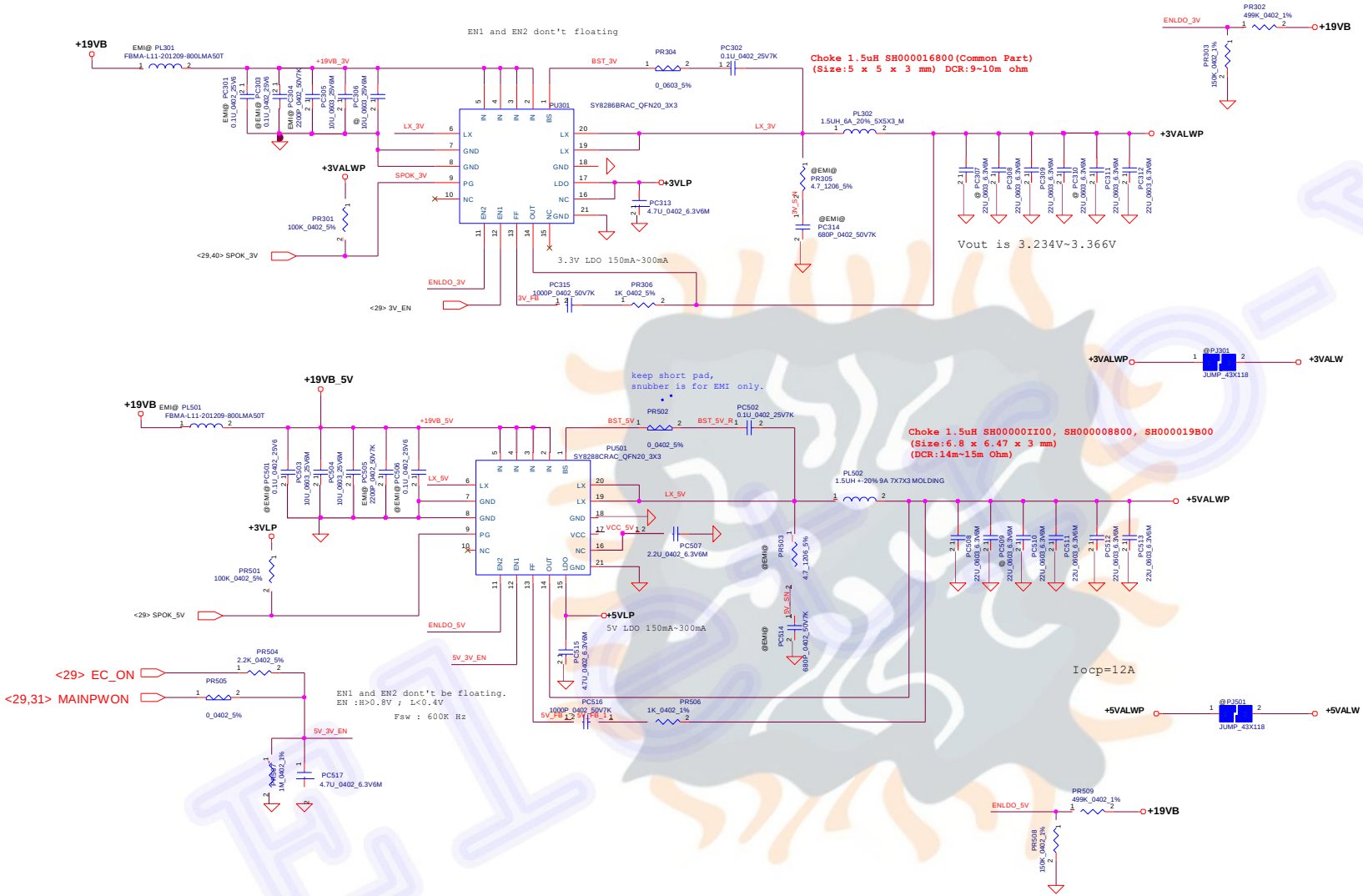
T202 T201 must close to PH201



Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.
Title: PWR-BATTERY CONN/OTP
Size: Custom | Document Number: EH5AW M/B LA-G521P
Date: Monday, May 13, 2019 | Sheet 35 of 47


+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+12.6V_BATT_CHG
+12.6V_BATT
+6V_CHG_REGN
+3VLP
ACFET MDU1512 SB00000SY00
Rds(on):4.2~5m Ohm
Vgs=20V
Vds=30V
ID= 24.2A (Ta=70C)
2016/03/13 SE158225K80 X1
down size SE00000WP00 S
CER CAP 2.2U 25V K X5R 0603
Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)
20160601 colay BQ24781
BQ24781RUYR_WQFN28_4X4
For 4S per cell 4.35V battery
3.3*100/(316+100)=0.79
ICHG= 0.79 /(20*0.01)=3.95A
3.3*78.7/(316+78.7)=0.66
ICHG= 0.66 /(20*0.01)=3.28A
H/L Side AON7506 SB000010A00
Rds(on):13~15.8mohm
Vgs=20V
Vds=30V
ID= 10.5A (Ta=70C)
Eletro-X
Compal Electronics, Inc.
charger
C5PRHM/BLA-E921P
Security Classification
Compal Secret Data
Issued Date
2016/11/03
Deciphered Date
2017/06/14
Monday, May 13, 2019
Sheet 36 of 47

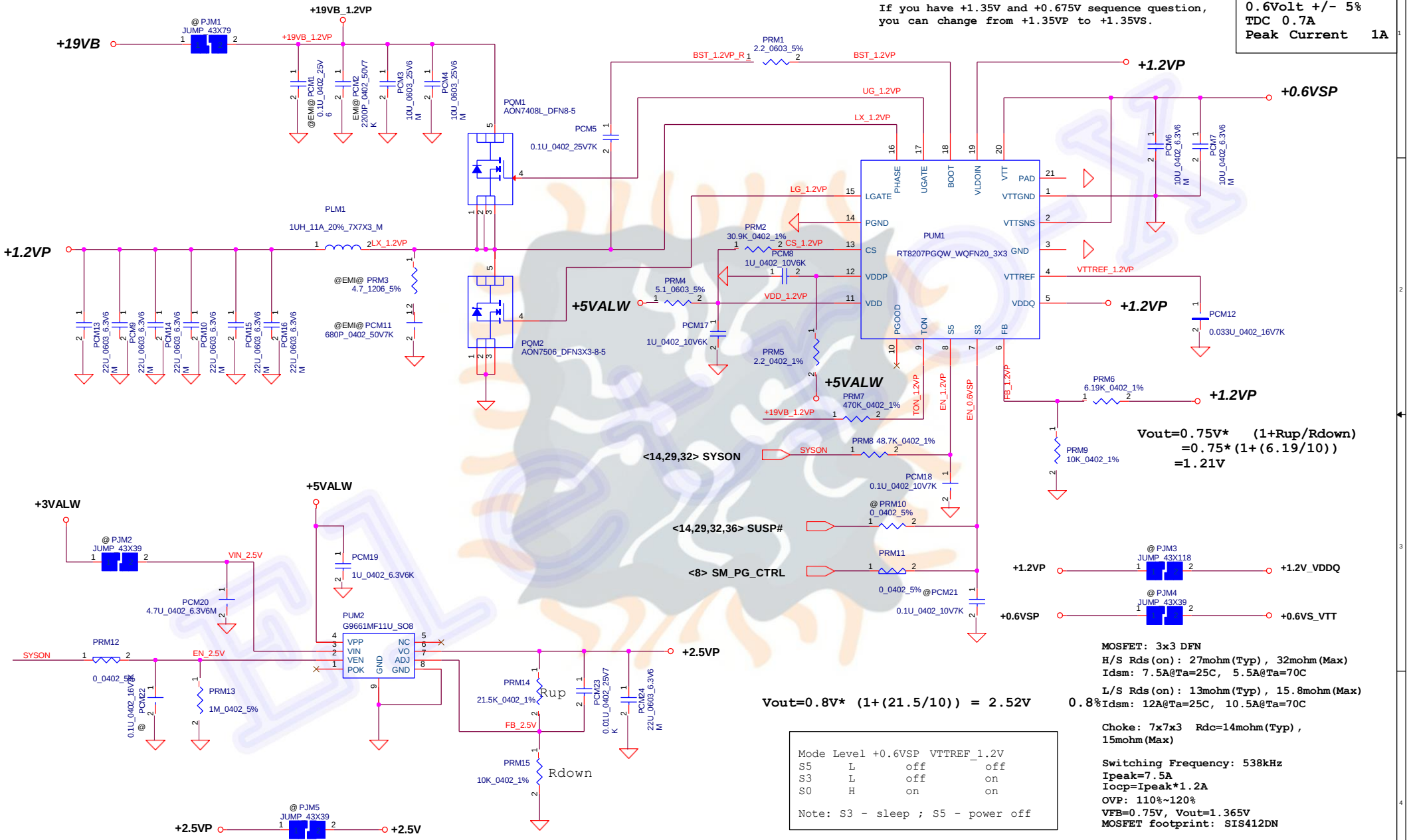


Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2019/11/15

Compal Electronics, Inc.	
Title:	+3VALW/+5VALW
Size: Custom	Document Number: DH5AV_JV_0V_LA-G021P
Rev: 1A	
Date: Monday, May 13, 2019	Sheet 37 of 47

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 32mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C
L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3 Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 538kHz
Ipeak=7.5A
Iocp=Ipeak*1.2A
OVP: 110%~120%
VFB=0.75V, Vout=1.365V
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

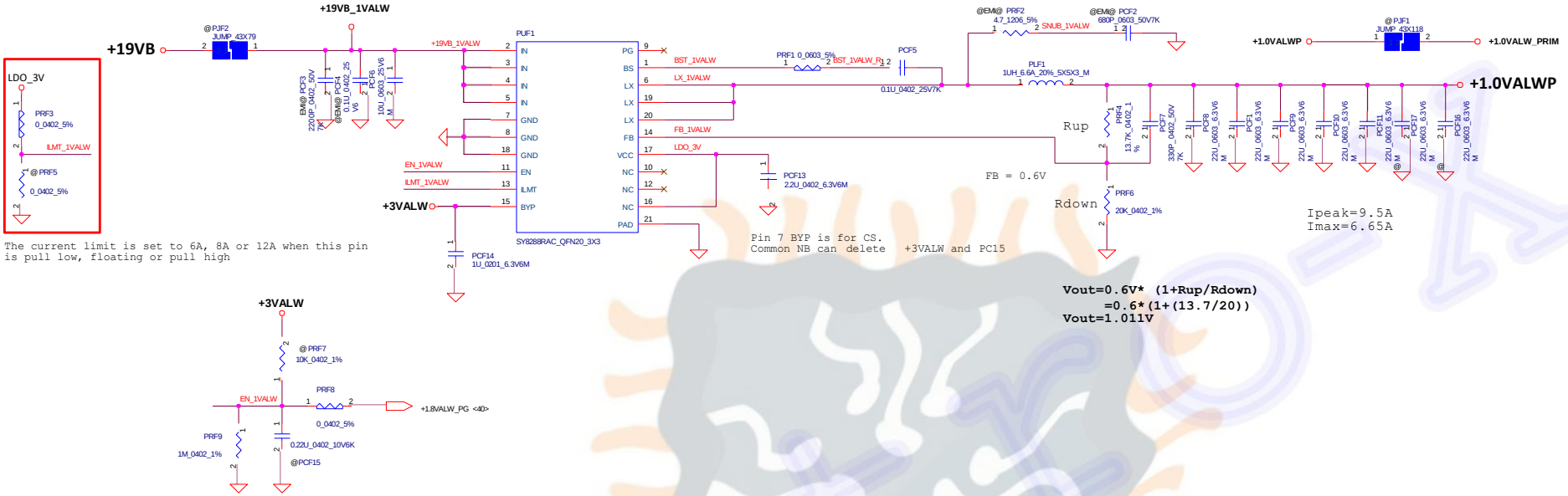
Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.0

Date: Monday, May 13, 2019 | Sheet 38 of 47

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



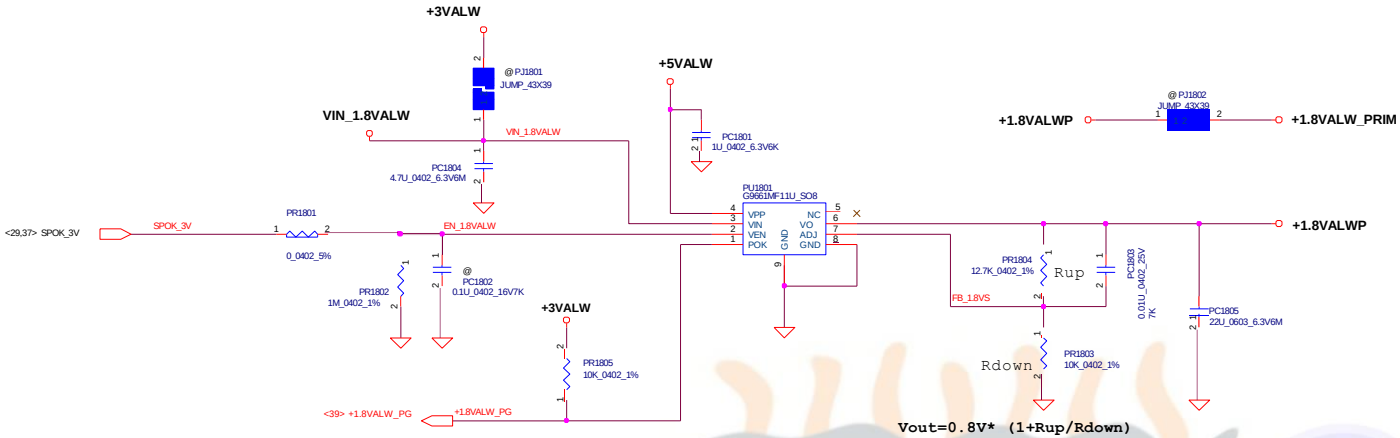
Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: VCCP

Size: C | Document Number: EH5AW M/B LA-G521P | Rev: 1A

Date: Monday, May 13, 2019 | Sheet: 39 of 47

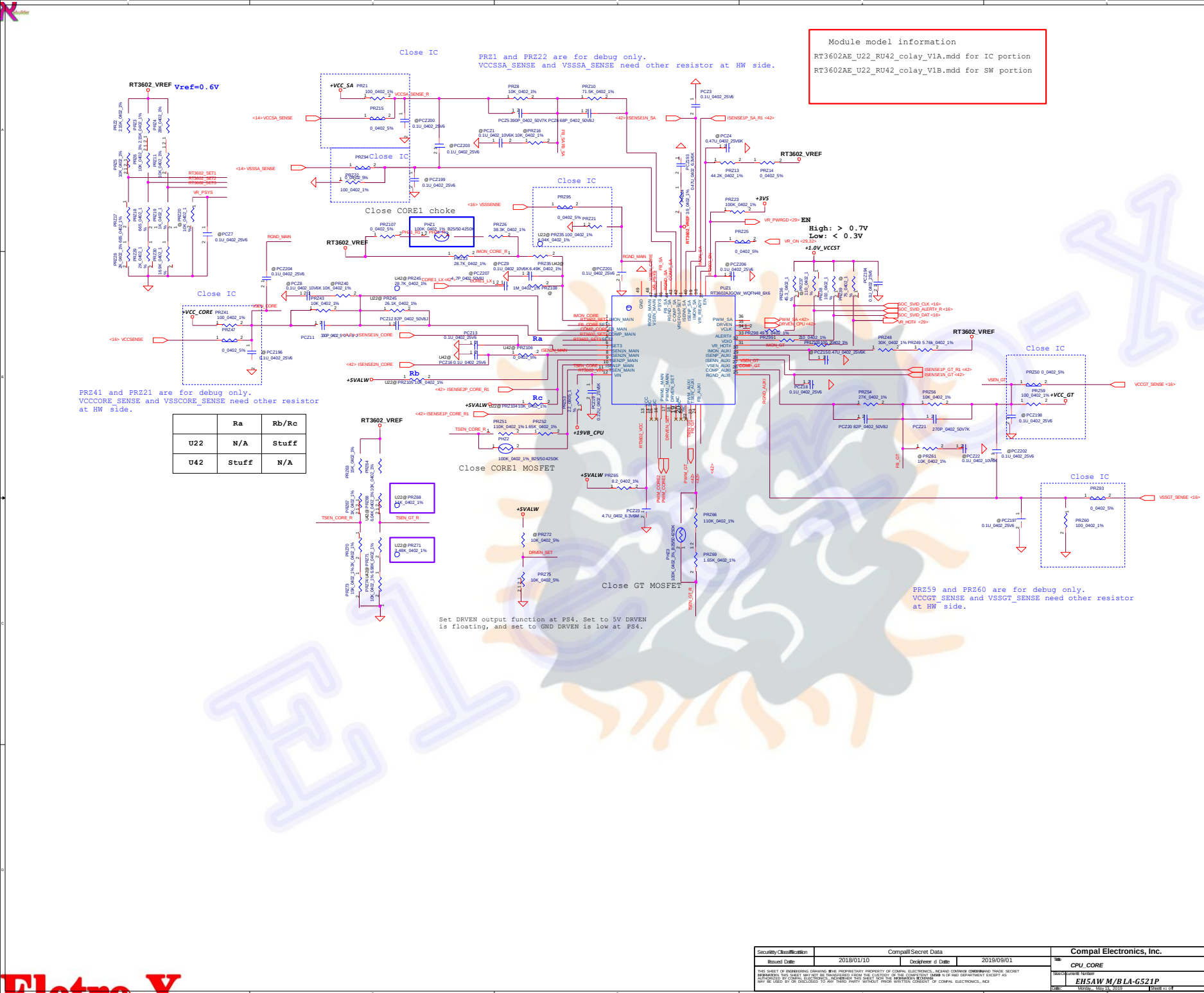


Vout=0.8V* (1+Rup/Rdown)

Vout=0.8V* (1+(12.7/10)) = 1.816V

Security Classification	Compal Secret Data		
Issued Date	2018/01/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.		
Title: SY8032		
Size: C	Document Number: EH5AW M/B LA-G521P	Rev: 1A
Date: Monday, May 13, 2019	Sheet: 40 of 47	



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

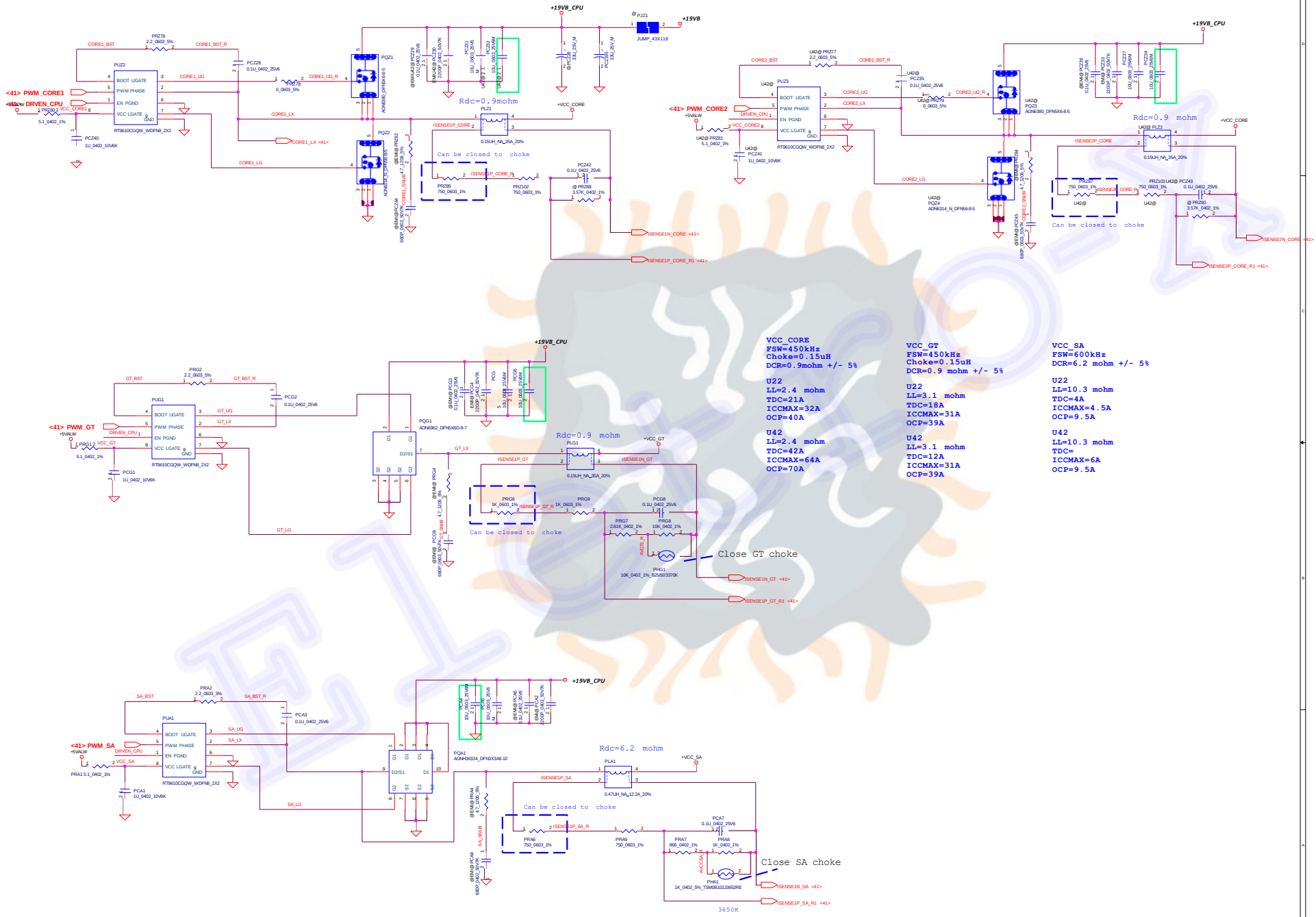
Security Classification	Compall Secret Data	
Issued Date	2018/01/10	Deciphered Date 2019/09/01

Compal Electronics, Inc.

Title: CPU_CORE

Size: Document Number: EH5AW M/B LA-G521P Rev: 1A

Date: Monday, May 13, 2019 Sheet 41 of 47



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

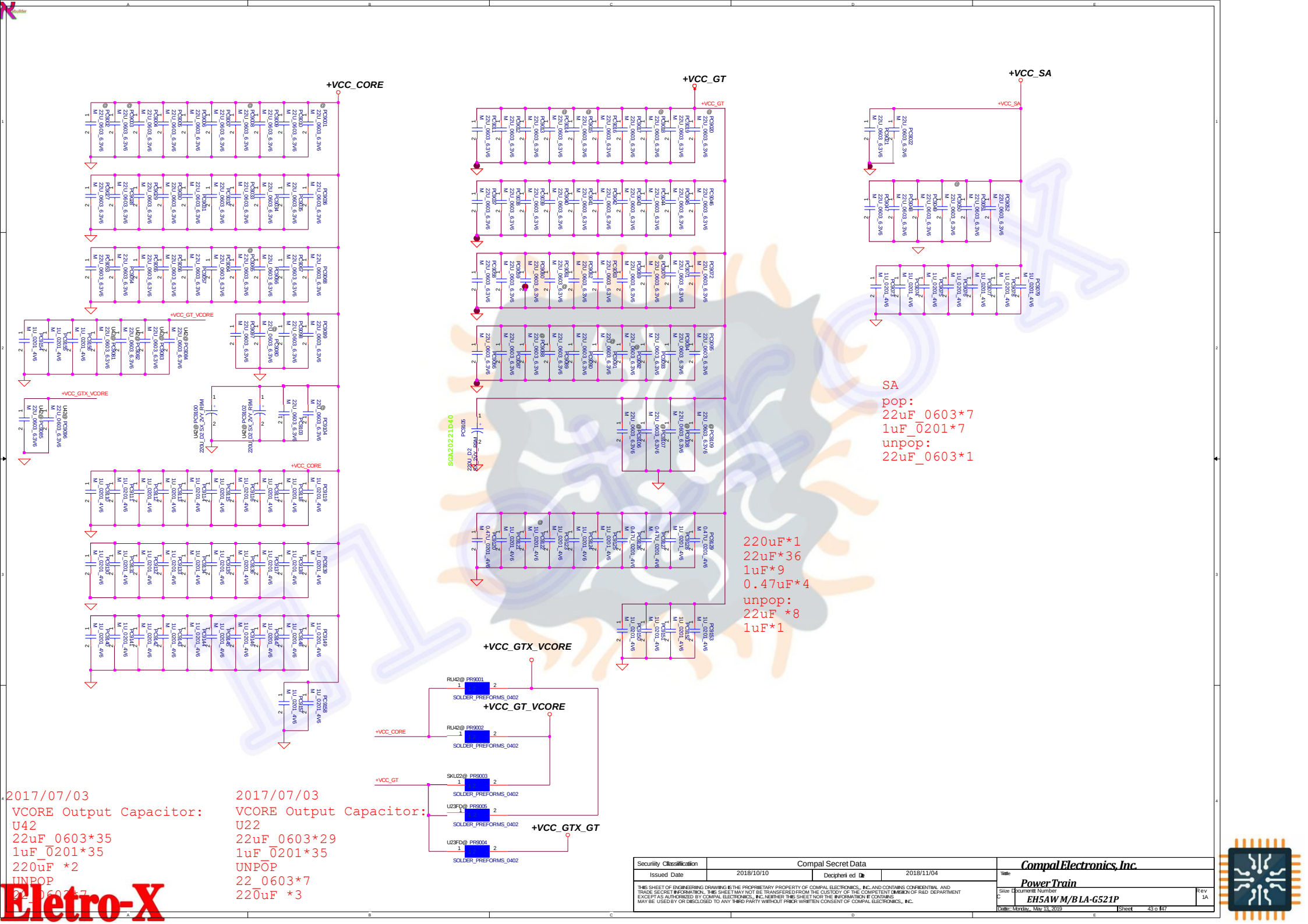
U42
LL=3.1 mohm
TDC=12A
ICCMAX=31A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=6A
OCP=9.5A

Security Classification	Compall Secret Data		Compal Electronics, Inc.
Issued Date	2018/01/10	Deciphered Date	2019/09/01
Title	CPU Power stage		
Size	Document Number		Rev
	EH5AW M/B LA-G521P		1A
Date:	Monday, May 20, 2019	Sheet	of


+VCC_CORE
+VCC_GT
+VCC_SA
+VCC_GT_VCORE
+VCC_GTX_VCORE
+VCC_CORE
SGA20221D40
SA
pop:
22uF_0603*7
1uF_0201*7
unpop:
22uF_0603*1
220uF*1
22uF*36
1uF*9
0.47uF*4
unpop:
22uF *8
1uF*1
+VCC_GTX_VCORE
+VCC_GT_VCORE
+VCC_CORE
+VCC_GT
+VCC_GTX_GT
SOLDER_PREFORMS_0402
2017/07/03
VCORE Output Capacitor:
U42
22uF_0603*35
1uF_0201*35
220uF *2
UNPOP
2_0603*7
2017/07/03
VCORE Output Capacitor:
U22
22uF_0603*29
1uF_0201*35
UNPOP
22_0603*7
220uF *3
Eletro-X
Security Classification
Compal Secret Data
Issued Date
2018/10/10
Deciphered Date
2018/11/04
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Document Number
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Rev
1A
Date: Monday, May 13, 2019
Sheet
43 of 47