LF14M
Schematics Document

M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

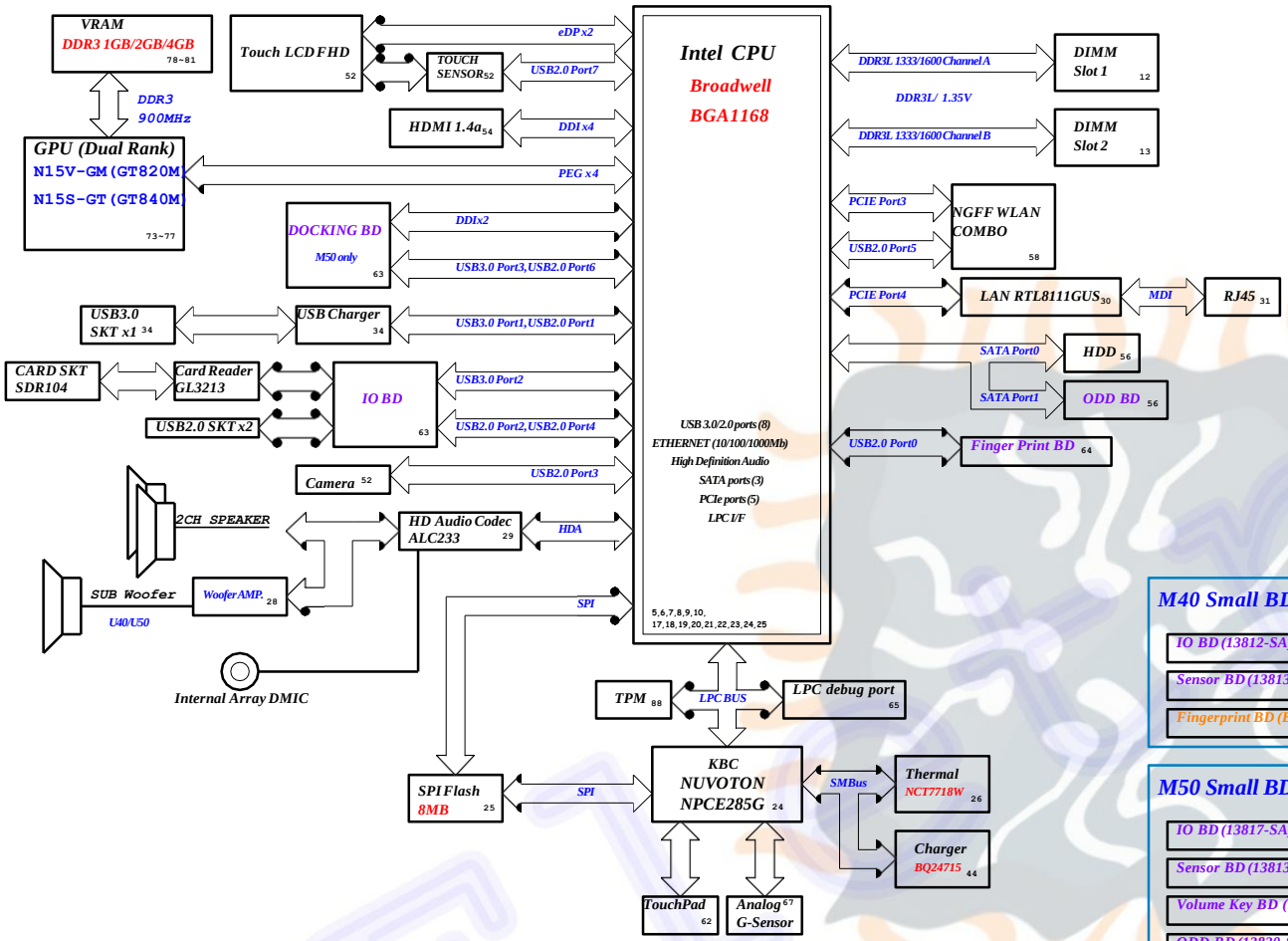
Title: **Cover Page**

Size: A3 | Document Number: **LF14M** | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 1 of 1

LF14M Board Block Diagram

Project code : 4PD00X010001
PCB P/N : 13281
Revision : SC



M40 Small BD & PCB P/N:

- IO BD (13812-SA) 63
- Sensor BD (13813-SA) 63
- Fingerprint BD (Buy) 63

Mybo14 Small BD & PCB P/N:

- IO BD (13812-SA) 63
- Sensor BD (13813-SA) 63

M50 Small BD & PCB P/N:

- IO BD (13817-SA) 63
- Sensor BD (13813-SA) 63
- Volume Key BD (13819-SA) 63
- ODD BD (13820-SA) 63
- DOCKING BD (13818-SA) 63
- Fingerprint BD (Buy) 63

Mybo15 Small BD & PCB P/N:

- IO BD (13814-SA) 63
- Sensor BD (13813-SA) 63
- Volume Key BD (13816-SA) 63
- ODD BD (13820-SA) 63
- Power BTN BD (13815-SA) 63

CHARGER BQ24715 44

INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51275 45

INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_S5

CPU DC/DC TPS51624 46-47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SYS8208A 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM DC/DC

INPUTS	OUTPUTS

SYSTEM DC/DC TLV70215 51

INPUTS	OUTPUTS
DCBATOUT	1D5V_S0

RT8812A 82

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 83

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D35V_S0	1D35V_VGA_S0
1D05V_VTT	1D05V_VGA_S0

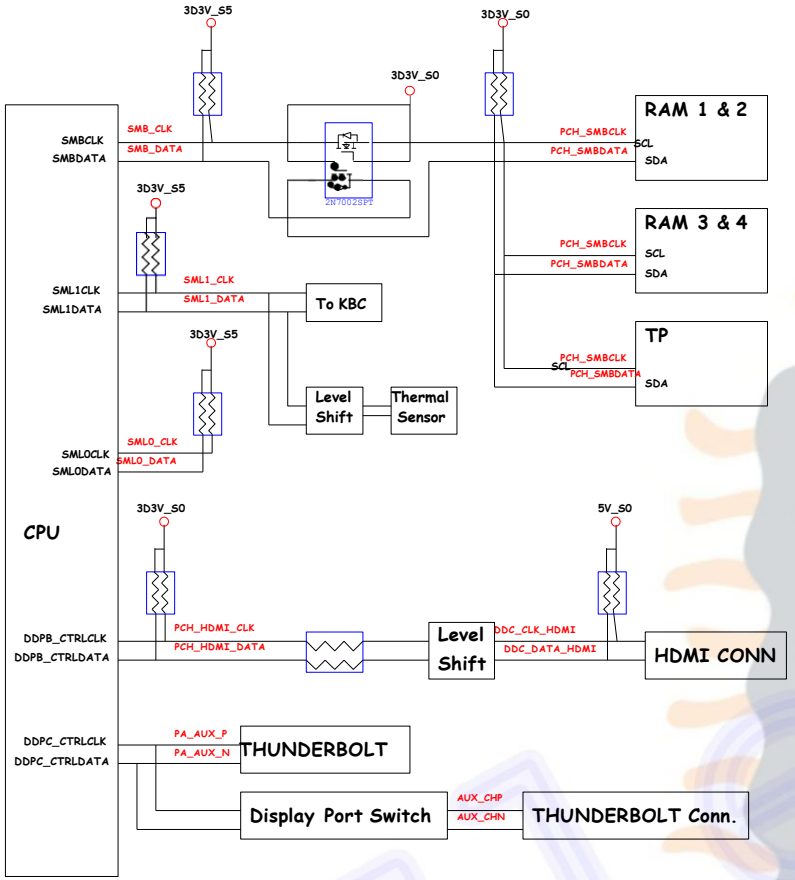
PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

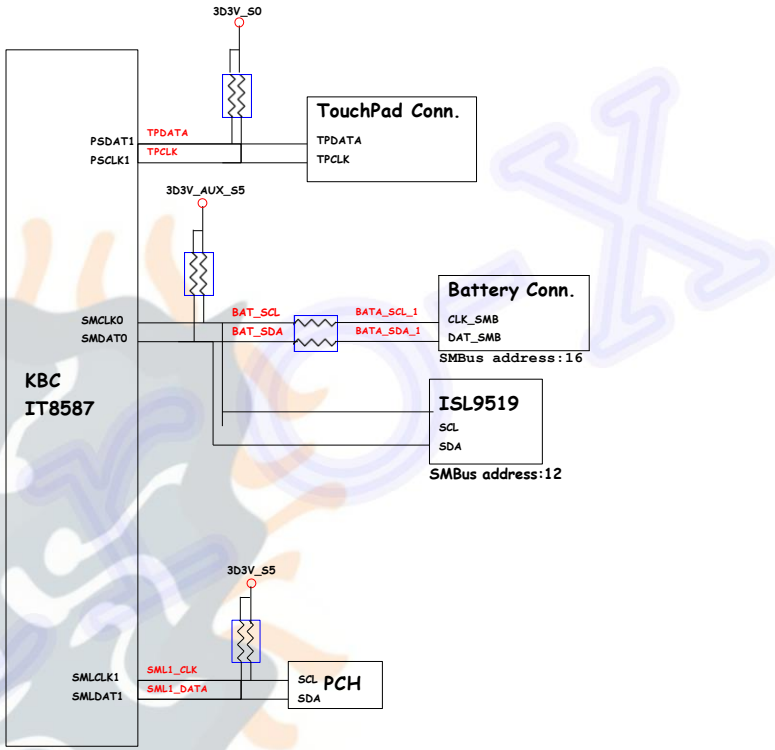
<Core Design>
緯創資通 Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A2 | Document Number: LF14M | Rev:
Date: Wednesday, February 26, 2014 | Sheet 2 of

PCH SMBus Block Diagram



KBC SMBus Block Diagram



M40

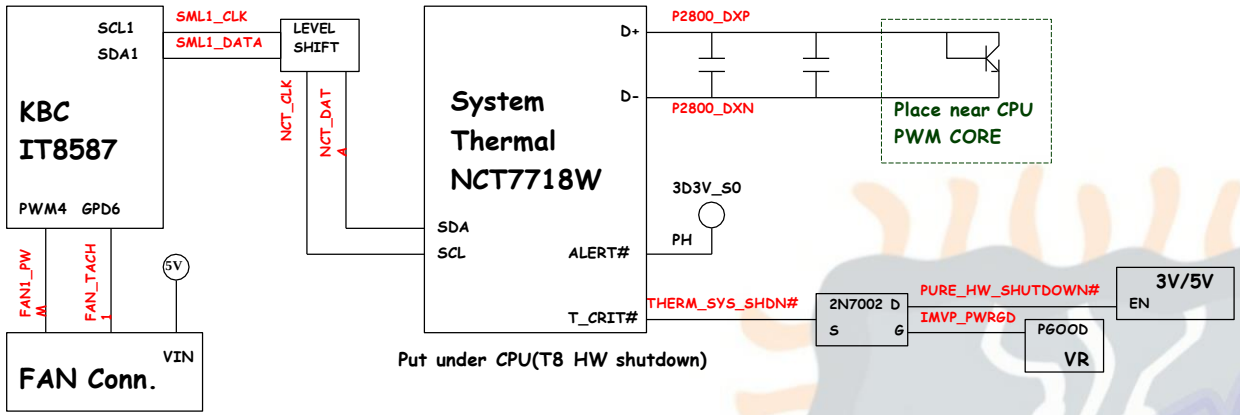
緯創資通 Wistron Corporation

Title: SMBUS BLOCK DIAGRAM

Size: A2 | Document Number: LF14M | Rev: 1.0

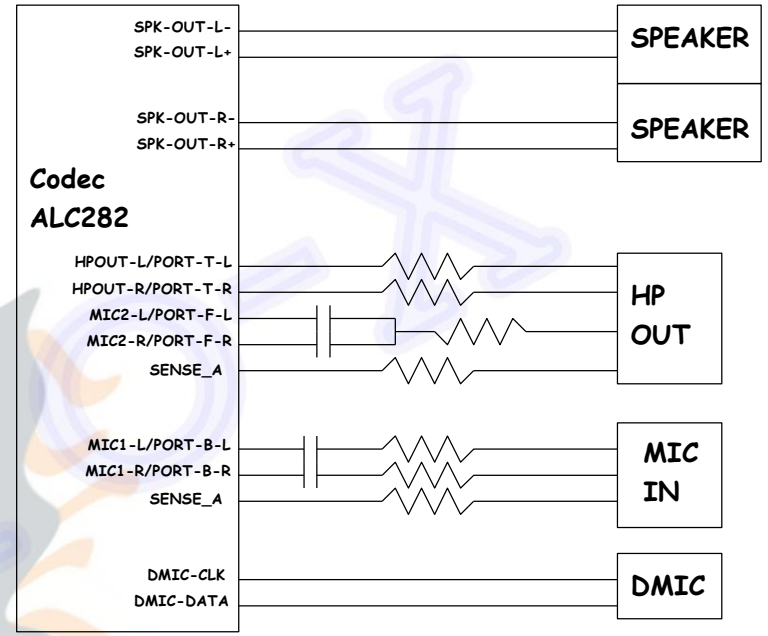
Date: Wednesday, February 26, 2014 | Sheet 101 of

Thermal Block Diagram



Put under CPU(T8 HW shutdown)

Audio Block Diagram



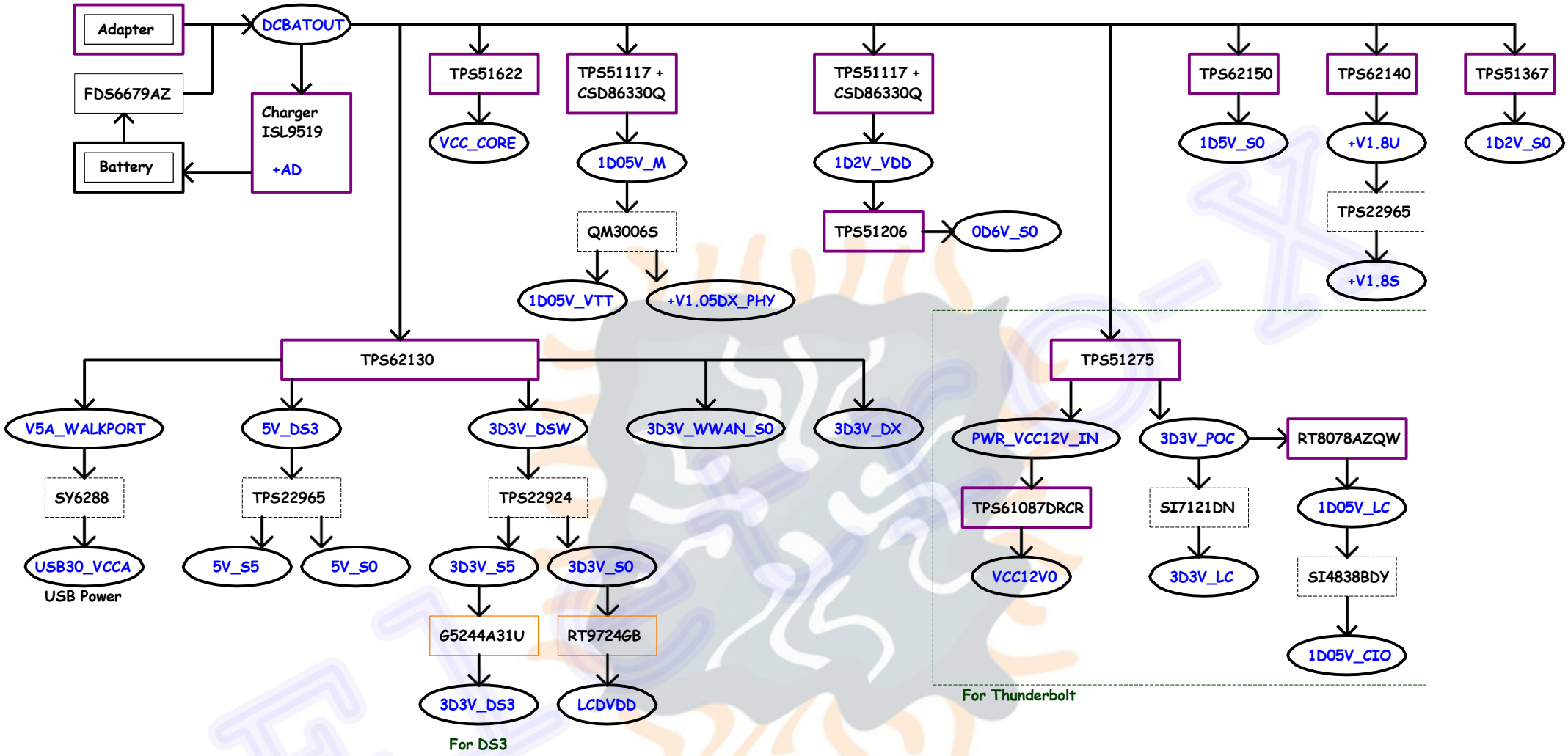
M40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM

Size: Custom | Document Number: LF14M | Rev: 1

Date: Wednesday, February 26, 2014 | Sheet 102 of 102



Power Shape

Regulator	LDO	Switch

M40

緯創資通 Wistron Corporation

21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, TaipeiHsien221, Taiwan, R.O.C.

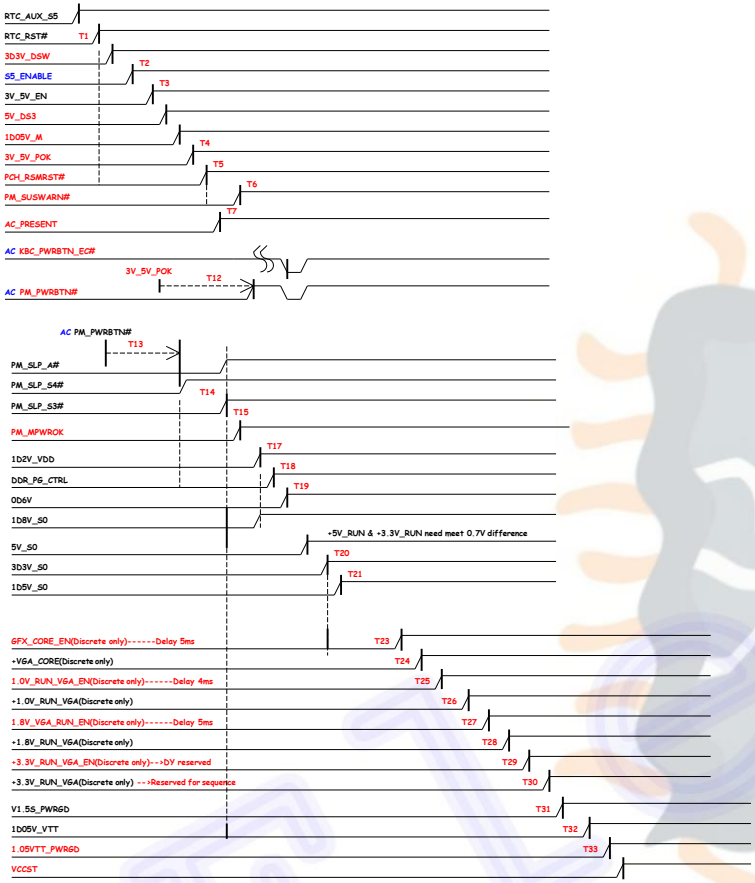
Title: Power Block Diagram

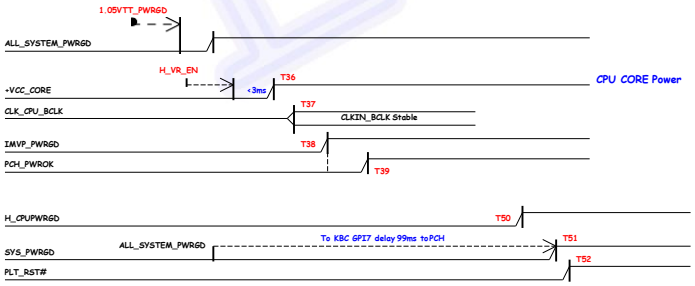
Size: A3 | Document Number: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 100 of 100

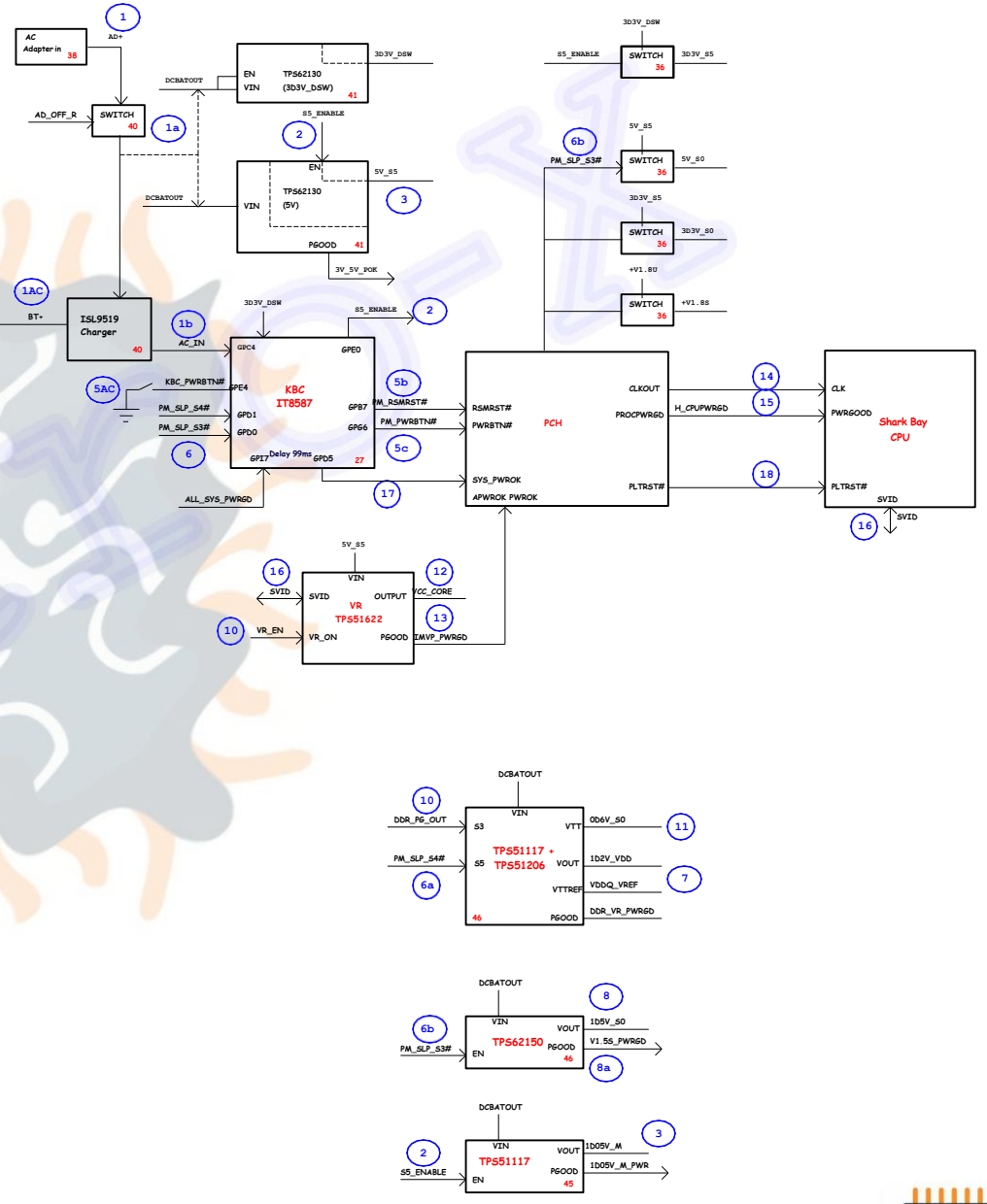
Intel-Power Up Sequence

(AC mode)





SHARK BAY POWER UP SEQUENCE DIAGRAM



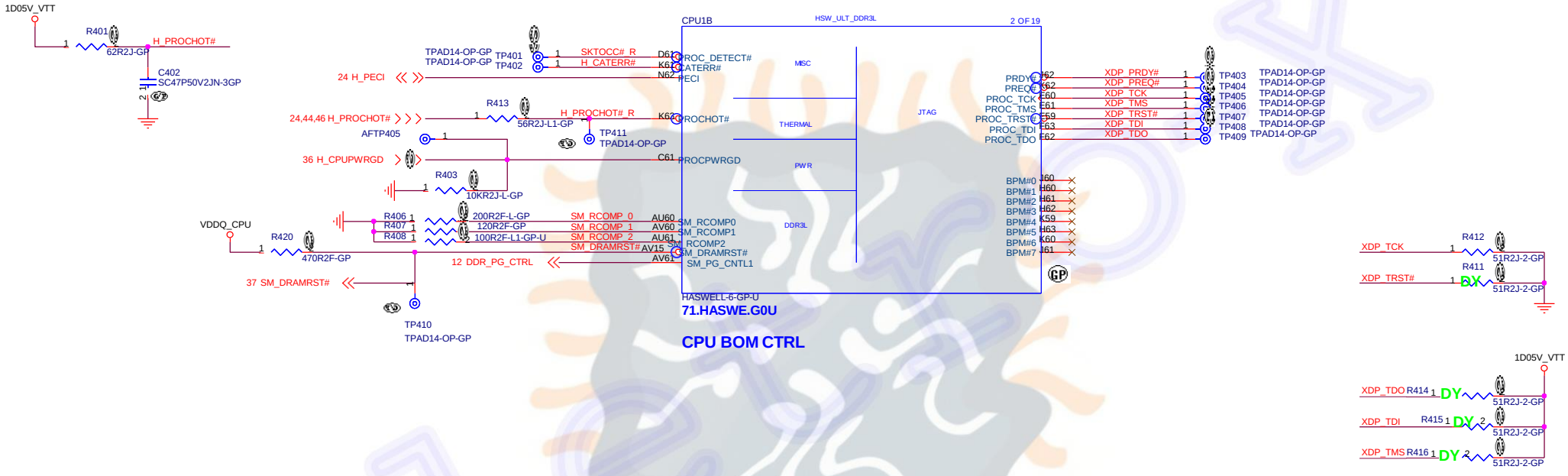
Eletro-X

Power Sequence

Document Number: LF14M

Wednesday, February 26, 2014

SSID = CPU



CPU BOM CTRL

<Core Desiign>

緯創資通 Wistron Corporation

21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, TaipeiHsien 221, Taiwan, R.O.C.

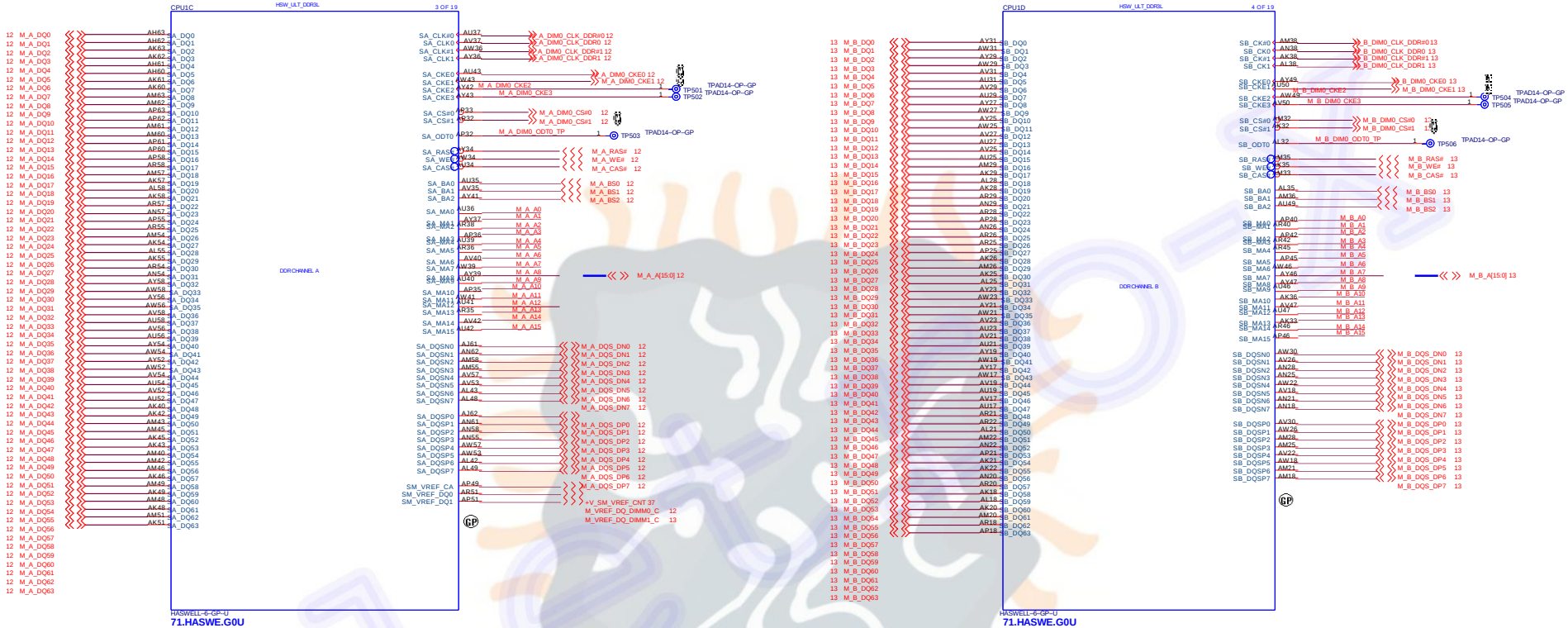
Title: CPU (THERMAL/CLOCK/PM)

Size: A3 | DocumentNumber: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 4 of 102

Eletro-X

SSID = CPU



Eletro-X

M40

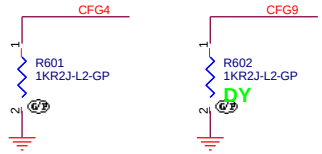
Wistron Corporation

CPU (DDR)

LF14M

SSID = CPU

eDP Enable	
CFG4	1:Disable 0:Enable

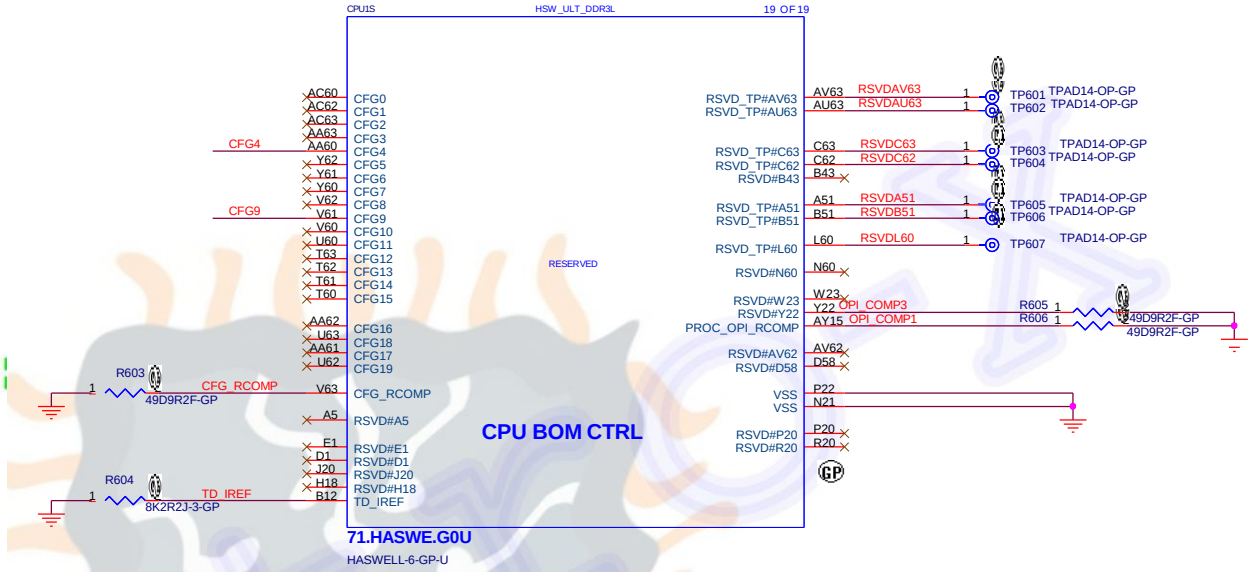


Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
		continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

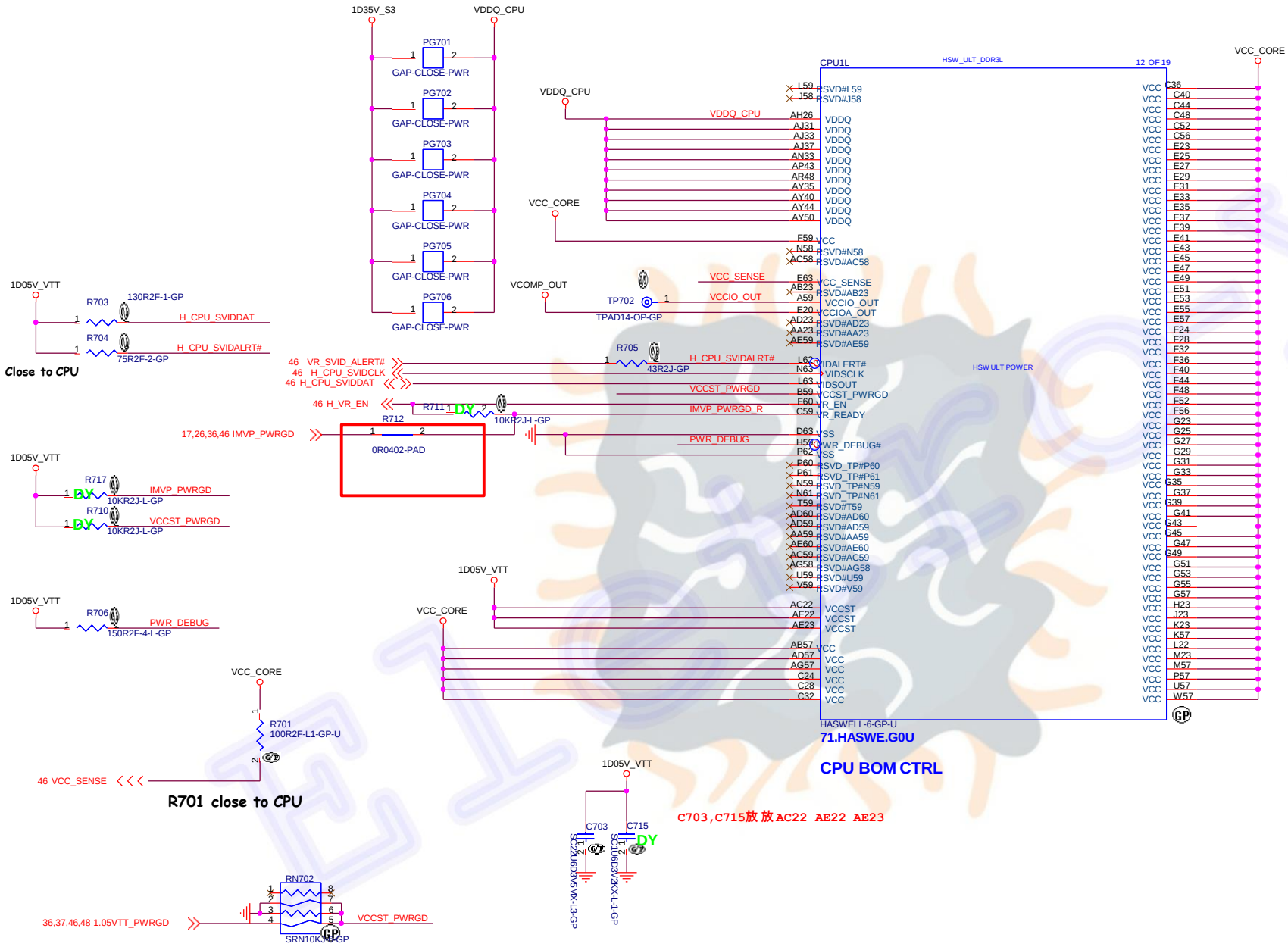
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected



M40

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, TaipeiHsien 221, Taiwan, R.O.C.
Title	*CPU (CFG)*
Size: Custom	Document Number: LF14M — Rev: -1
Date: Wednesday, February 26, 2014	Sheet 6 of 102

SSID = CPU



Eletro-X

M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

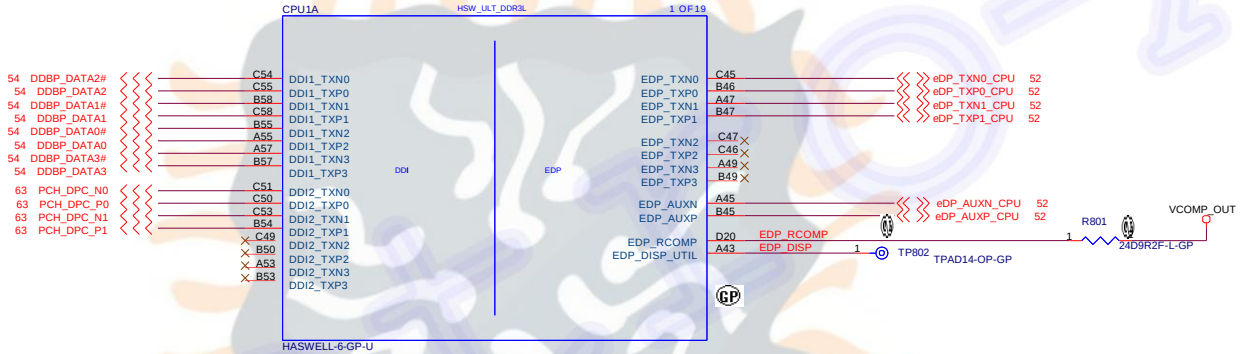
Size	Document Number	Rev
A3	LF14M	1

Date: Wednesday, February 26, 2014 Sheet 7 of

SSID = CPU

HDMI

DP to DOCKING



71.HASWE.G0U

CPU BOM CTRL

M40

緯創資通 Wistron Corporation

21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

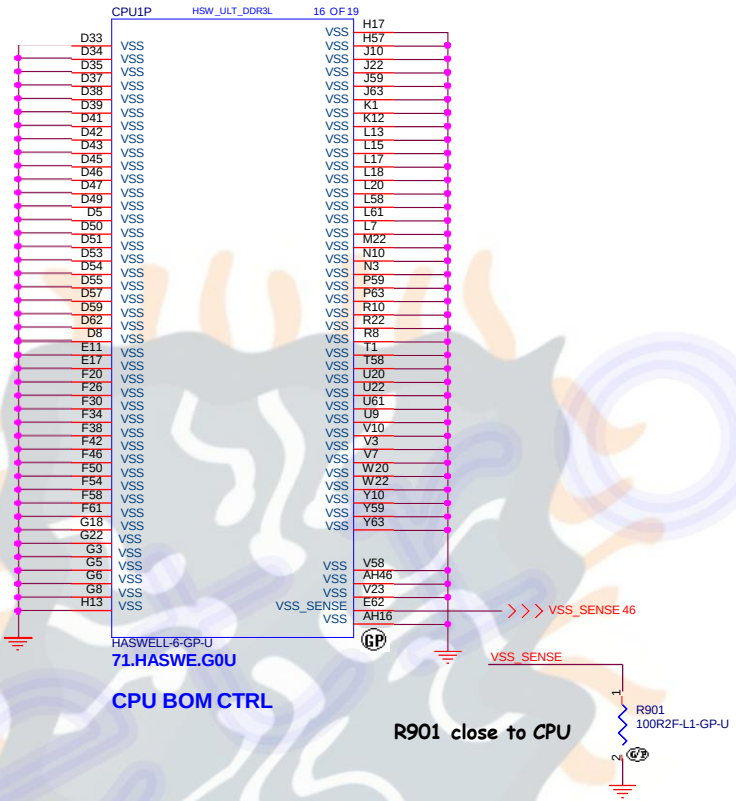
Title: CPU (DDI/EDP)

Size: Custom | Document Number: LF14M | Rev: 0A1

Date: Wednesday, February 26, 2014 | Sheet 8 of

Eletro-X

SSID = CPU



M40

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (VSS)	
Size: A3	Document Number: LF14M
Date: Wednesday, February 26, 2014	Sheet 9 of 10

SSID = MEMORY

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

ODT resistor must be 66.5 ohm

Q1201 Q1202限限限84.05067.031
因因因因Vth因1V

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.

For Intel Recommend Close to DIMM

H = 4mm

62.10024.S61

1ST = 62.10024.S61

2ND = 62.10024.M51

Close RAM1 CA & DQ pin

M40

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

DDR3L-SODIMM1

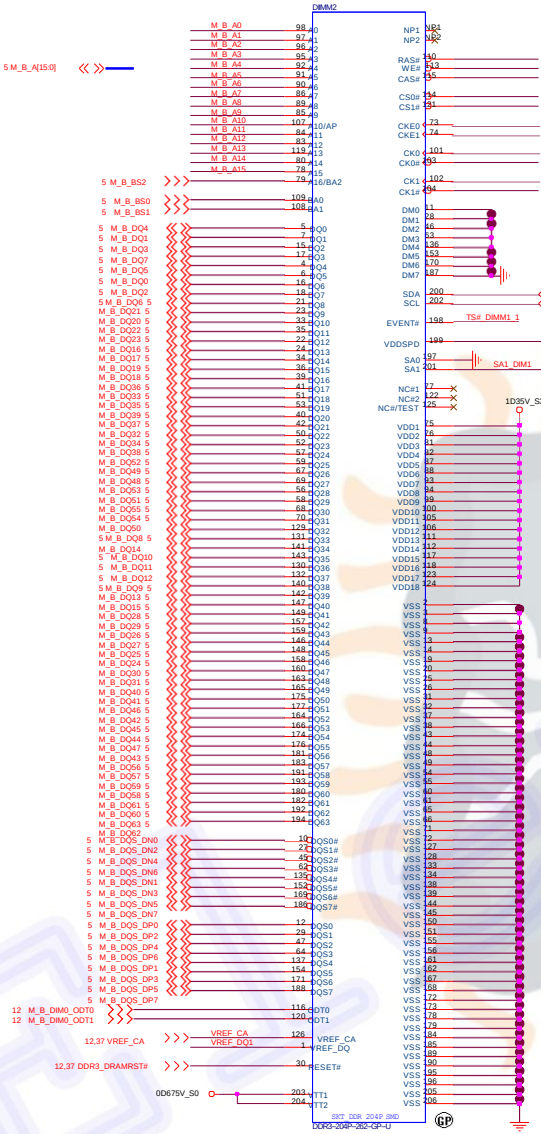
LF14M

Wednesday, February 26, 2014

Sheet 12

Eletro-X

SSID = MEMORY



62.10024.S21

1ST = 62.10024.S21

2ND = 62.10024.M31

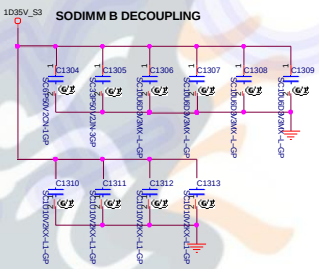
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

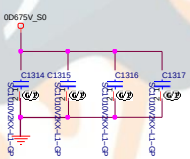
SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

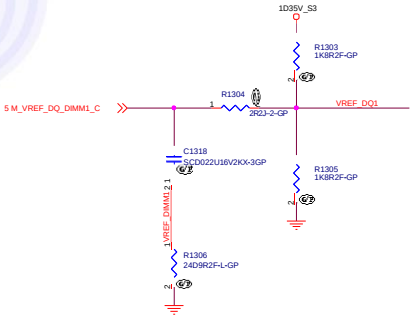
Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING

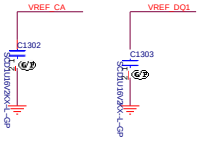




Place these caps close to VTT1 and VTT2.



For Intel Recommend Close to DIMM



Close RAM3 CA & DQ pin

M40

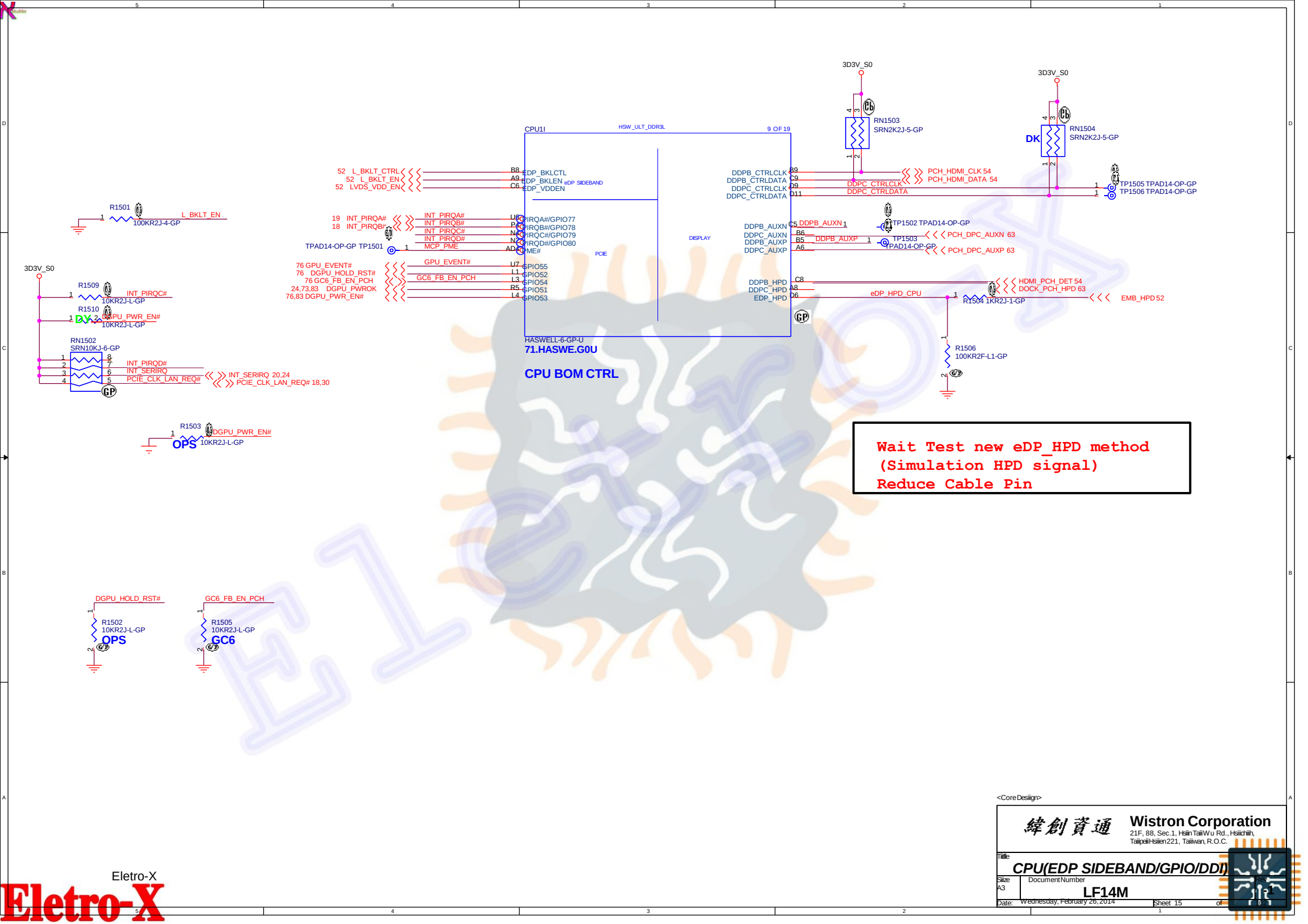
緯創資通 Wistron Corporation

21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DDR3L-SODIMM2

Size: A2 | Document Number: LF14M | Rev: 1

Date: Wednesday, February 26, 2014 | Sheet 13


CPU1I
HSW_ULT_DDR3L
9 OF 19
HASWELL-6-GP-U
71.HASWE.G0U
CPU BOM CTRL
DISPLAY
PCIE
eDP SIDEBAND
3D3V_S0
R1501 100KR2J-4-GP L_BKLT_EN
R1509 10KR2J-L-GP INT_PIRQC#
R1510 10KR2J-L-GP DGPU_PWR_EN#
DY
RN1502 SRN10KJ-6-GP
INT_PIRQD#
INT_SERIRQ
PCIE_CLK_LAN_REQ#
INT_SERIRQ 20,24
PCIE_CLK_LAN_REQ# 18,30
R1503 10KR2J-L-GP DGPU_PWR_EN#
OPS
DGPU_HOLD_RST#
R1502 10KR2J-L-GP
OPS
GC6_FB_EN_PCH
R1505 10KR2J-L-GP
GC6
52 L_BKLT_CTRL
52 L_BKLT_EN
52 LVDS_VDD_EN
EDP_BKLCTL
EDP_BKLEN
EDP_VDDEN
19 INT_PIRQA#
18 INT_PIRQB#
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
MCP_PME
TPAD14-OP-GP TP1501
GPU_EVENT#
76 GPU_EVENT#
76 DGPU_HOLD_RST#
76 GC6_FB_EN_PCH
24,73,83 DGPU_PWROK
76,83 DGPU_PWR_EN#
GPIO55
GPIO52
GPIO54
GPIO51
GPIO53
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
RN1503 SRN2K2J-5-GP
PCH_HDMI_CLK 54
PCH_HDMI_DATA 54
DDPC_CTRLCLK
DDPC_CTRLDATA
3D3V_S0
DK
RN1504 SRN2K2J-5-GP
TP1505 TPAD14-OP-GP
TP1506 TPAD14-OP-GP
DDPB_AUXN
DDPC_AUXN
DDPB_AUXP
DDPC_AUXP
DDPB_AUXN
DDPB_AUXP
TP1502 TPAD14-OP-GP
TP1503 TPAD14-OP-GP
PCH_DPC_AUXN 63
PCH_DPC_AUXP 63
DDPB_HPD
DDPC_HPD
EDP_HPD
eDP_HPD_CPU
R1504 1KR2J-1-GP
HDMI_PCH_DET 54
DOCK_PCH_HPD 63
EMB_HPD 52
R1506 100KR2F-L1-GP
Wait Test new eDP_HPD method
(Simulation HPD signal)
Reduce Cable Pin
<Core Desiign>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(EDP SIDEBAND/GPIO/DDI)
Size A3
Document Number
LF14M
Rev 1
Date: Wednesday, February 26, 2014
Sheet 15 of 60
Eletro-X

SSID = PCH

2014/2/6
USB_PP1/PN1改改改USB2.0 Port 0
USB_PP0/PN0改改改USB2.0 Port 1
NET維維維維

USB2.0 Table

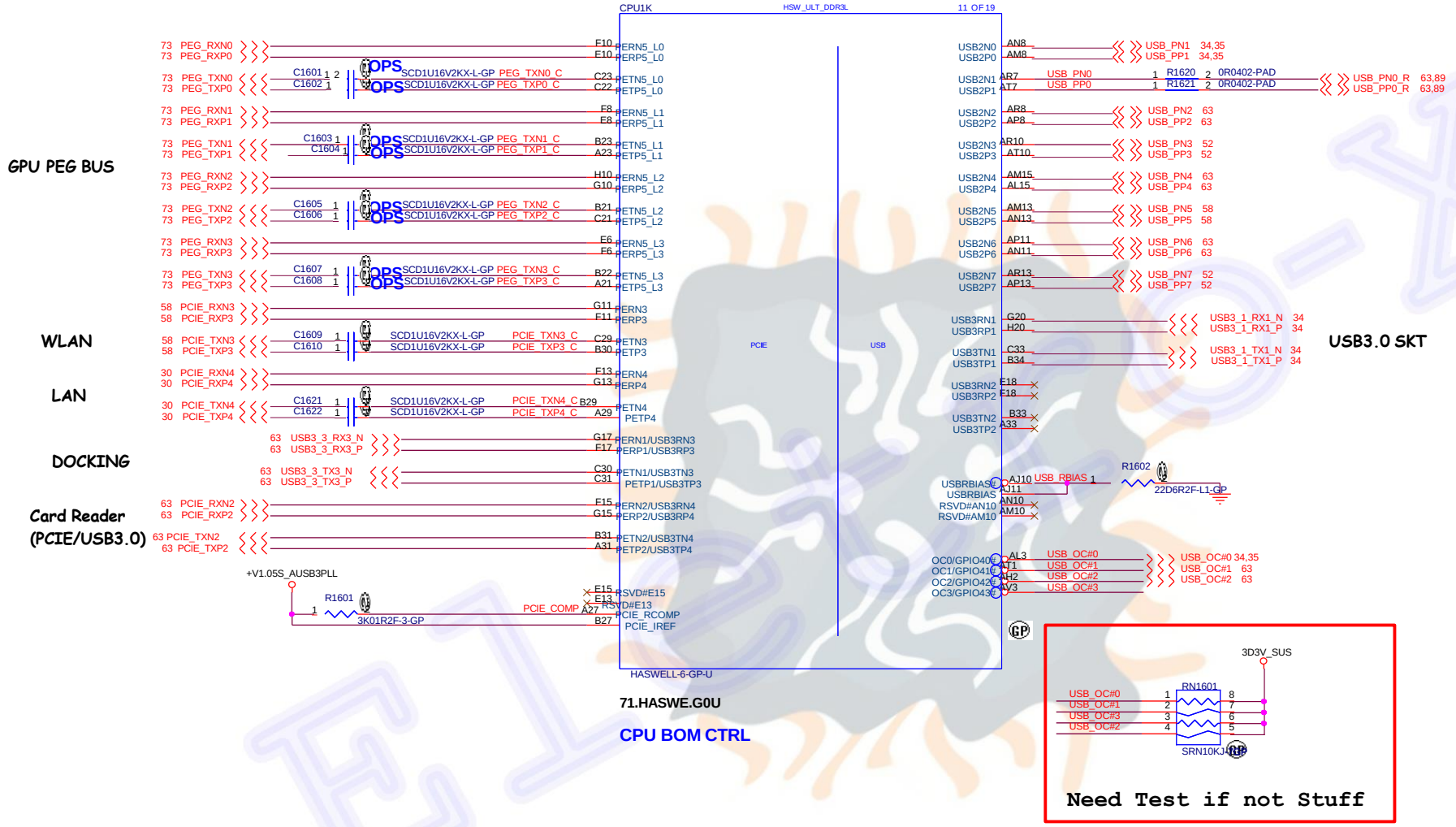
Pair	Device
0	USB3.0 Port 1 (with Debug Function)
1	Fingerprint / USB3.0 Card Reader(DY)
2	USB2.0 Port 2
3	Camera
4	USB2.0 Port 3
5	WLAN(Bluetooth)
6	USB3.0 to DOCKING
7	Panel Touch

USB 3.0 Table

Pair	Device
1	Combined with USB2.0 port1
2	Reserved
3	USB3.0 to DOCKING
4	USB 3.0 Card Reader

USB OverCurrent (OC#)

Pair	Device
OC#0	USB3.0 port1
OC#1	USB2.0 port2
OC#2	USB2.0 port3
OC#3	Reserved



M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien221, Taiwan, R.O.C.

Title: CPU (PCI/USB)

Size: A3 | DocumentNumber: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 16 of 40

Eletro-X

SSID = PCH

Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

TP1707 TPAD14-OP-GP — R1721 330KR2J-L-GP (RTC_AUX_S5) — R1722 330KR2J-L-GP (DY) — DSWODVREN

Follow Intel CRB

3D3V_S0 — R1701 10KR2J-L-GP — SYS_RESET#

TP1702 PCH_PWROK_R TPAD14-OP-GP

CPU1H — HSW_ULT_DDR3L — 8 OF 19 — SYSTEM POWER MANAGEMENT

7,26,36,46 IMVP_PWRGD — R1702 0R2J-L-GP (DY)
24 S0_PWR_GOOD
36 PCH_PWROK — R1703 0R0402-PAD
24,30,36,58,63,65,76 PLT_RST# — R1704 0R0402-PAD — PCH_PWROK_R

24 PM_SUSACK# — PM_SUSACK#
SYS_RESET#
SYS_PWROK_R
SYS_PWROK
PCH_PWROK
APWROK
PLTRST#

TP1701 TPAD14-OP-GP

R1705 10KR2J-L-GP (DY) — S0_PWR_GOOD
R1706 10KR2J-L-GP (DY) — PCH_PWROK — TP1706 TPAD14-OP-GP
R1707 10KR2J-L-GP — PM_RSMRST#

24 PM_SUSWARN# — TPAD14-OP-GP — TP1721 — PM_RSMRST# / PM_SUSWARN#
24 PM_PWRBTN#
24 AC_PRESENT
BATLOW#
PM_SLP_S0#
SLP_WLAN#
TP1720 TPAD14-OP-GP — TP1719 TPAD14-OP-GP

PM_SUSWARN# — R1708 0R0402-PAD — PM_SUSACK#

PM_RSMRST#
PM_SUSWARN#/SUSPWRDNACK#/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
SLP_S0#
SLP_WLAN#/GPIO29

HASWELL-6-GP-U
71.HASWE.G0U

CPU BOM CTRL

DSWVRMEN
DPWROK
WAKE#
DSWODVREN
PCH_DPWROK

TP1705 TPAD14-OP-GP — Non DS3 — R1714 0R2J-2-GP — PM_RSMRST# — PCIE_WAKE# 58

CLKRUN#/GPIO32 — PM_CLKRUN#_EC 24
SUS_STAT#/GPIO61 — PM_SUS_STAT# — TP1704 TPAD14-OP-GP
SUSCLK/GPIO62 — PCH_SUSCLK_KBC — PCH_SUSCLK_KBC 58
SLP_S5#/GPIO63 — PM_SLP_S5# — TP1703 TPAD14-OP-GP

SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
SLP_LAN#

AFTP1702 — R1715 0R2J-L-GP — PM_SLP_S4# 24,49 / PM_SLP_S3# 24 / PM_SLP_A# 24 / PM_SLP_SUS# 24,38
PM_SLP_S3# — DY — AFTP1705

PCH_DPWROK — R1716 0R2J-L-GP (DS3) — KBC_DPWROK 24 (DS3)
R1717 10KR2J-L-GP (DY)
SLP_A# — TP1708 TPAD14-OP-GP

3D3V_AUX_KBC — Non DS3 — R1710 100KR2J-4-GP — R1711 100KR2J-4-GP
3V_5V_POK_# — Q1701 2N7002KDW-GP — 84.2N702.A3F — 3V_5V_POK_C
PM_RSMRST# — R1712 1KR2J-L2-GP — RSMRST#_KBC 24
R1713 0R2J-L-GP — PM_SLP_SUS# — TP1709 TPAD14-OP-GP — DS3
3V_5V_POK_C — R1712 0R2J-2-GP — 3V_5V_POK 45
Non DS3

2ND = 75.00601.07C

3D3V_S5 — RN1701 SRN10KJ-L-GP — PM_PWRBTN# / BATLOW#

3D3V_S5 — R1724 10KR2J-L-GP — PCIE_WAKE#
R1723 10KR2J-L-GP — AC_PRESENT

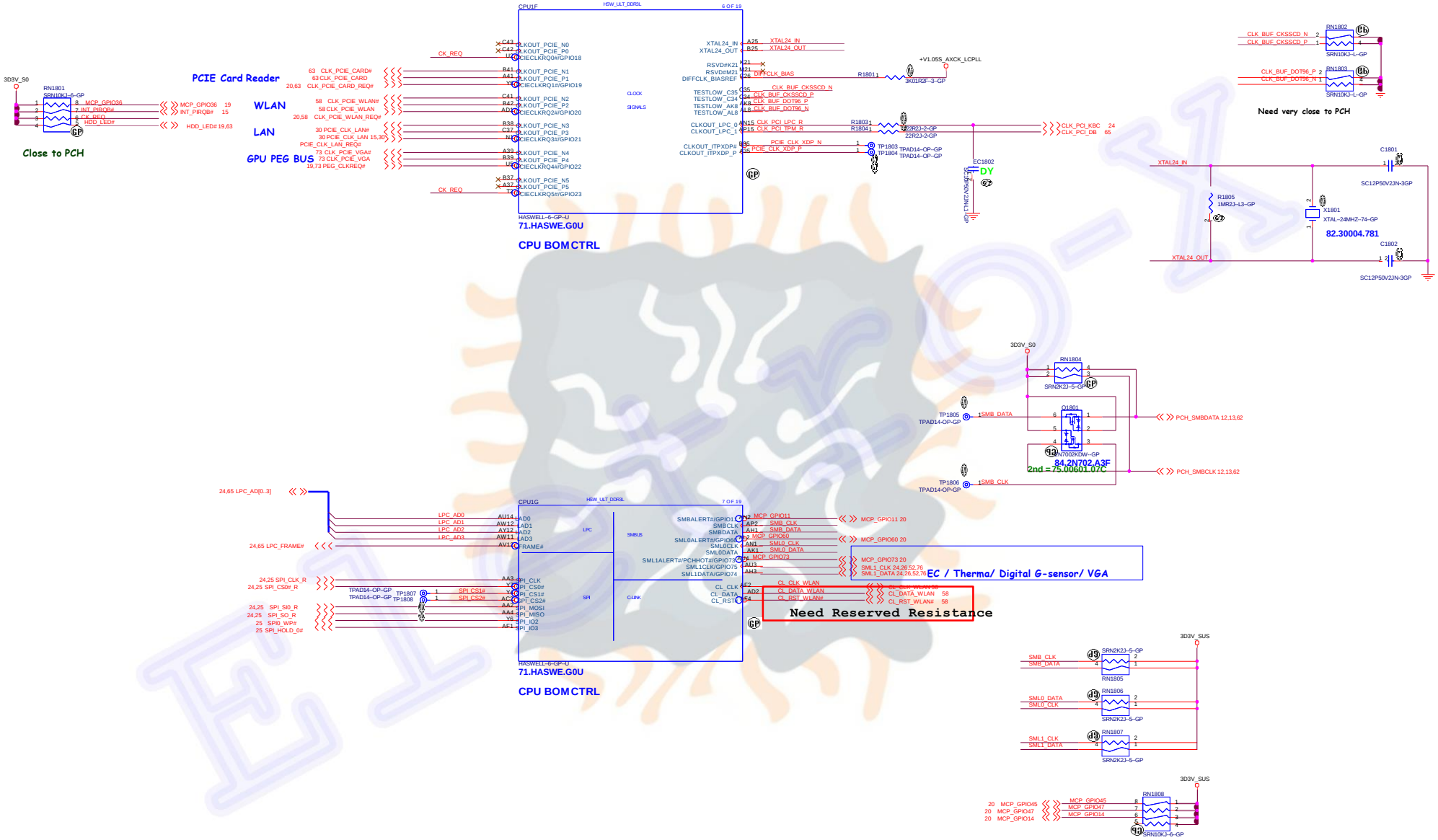
PM_SUSWARN# — R1718 1KR2J-L2-GP — 3D3V_SUS
PM_CLKRUN#_EC — R1719 8K2R2J-3-GP — 3D3V_S0
PM_SUS_STAT# — R1720 10KR2J-L-GP — 3D3V_SUS

<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DMI/FDI/PM)
Size: A3 | Document Number: LF14M | Rev: 1.0
Date: Wednesday, February 26, 2014 | Sheet 17 of 40

SSID = PCH



<Core Design>

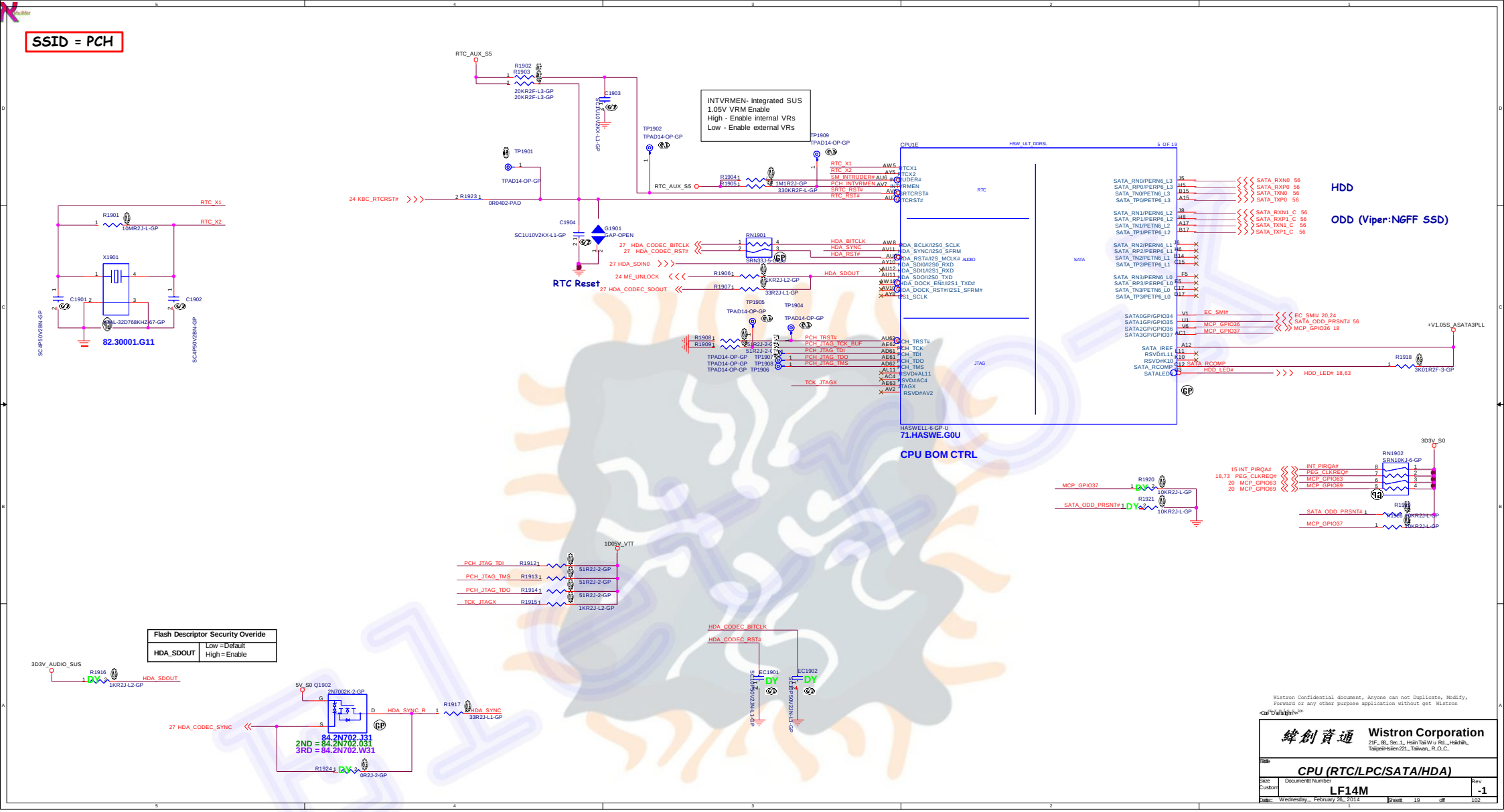
Wistron Corporation

CPU (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: LF14M | Rev: 1A

Date: Wednesday, February 26, 2014 | Sheet 18

Eletro-X



Eletro-X

SSID = PCH

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

	GSPI0_MOSI_BBS0_R(SSD_PWR)
PU	RESERVED
PD	SPI BUS

CPU BOM CTRL

R2013	10KR2J-L-GP	UMA
R2014	10KR2J-L-GP	OPS
R2019	10KR2J-L-GP	TOUCH
R2020	10KR2J-L-GP	NON TOUCH
R2021	10KR2J-L-GP	VRAM_4PCS
R2022	10KR2J-L-GP	VRAM_8PCS
R2035	10KR2J-L-GP	900MHz
R2036	10KR2J-L-GP	1000MHz
R2037	10KR2J-L-GP	NCT7718
R2038	10KR2J-L-GP	TV

M40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

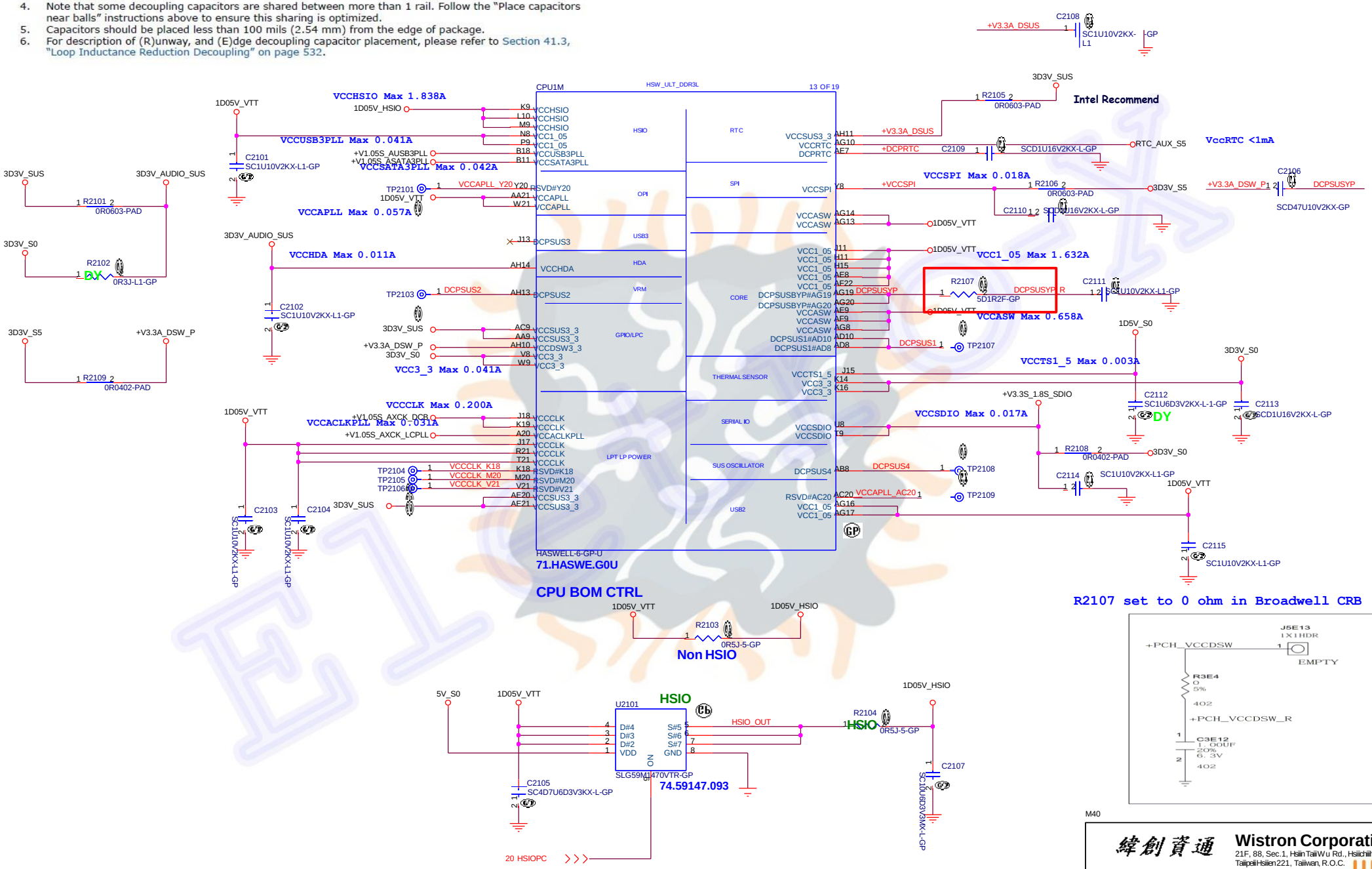
Title: CPU (GPIO/MISC)

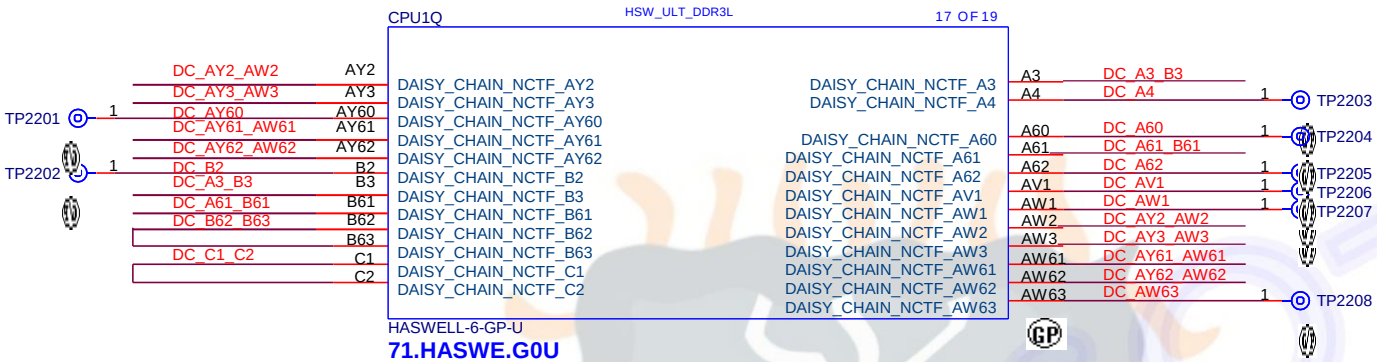
Size: Custom | Document Number: LF14M | Rev: 1.1

Date: Wednesday, February 26, 2014 | Sheet 20 of 40

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.





CPU BOM CTRL

CPU BOM CTRL

M40

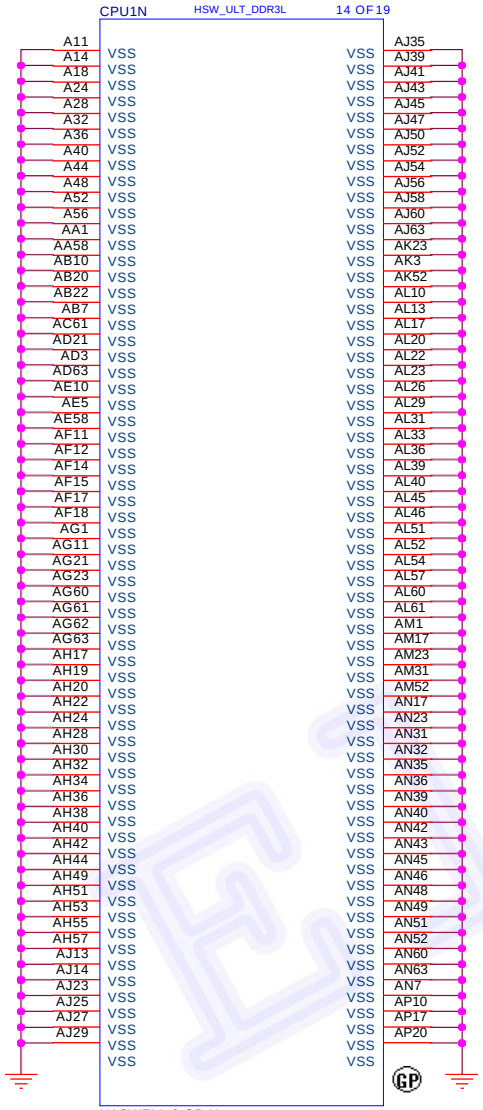
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

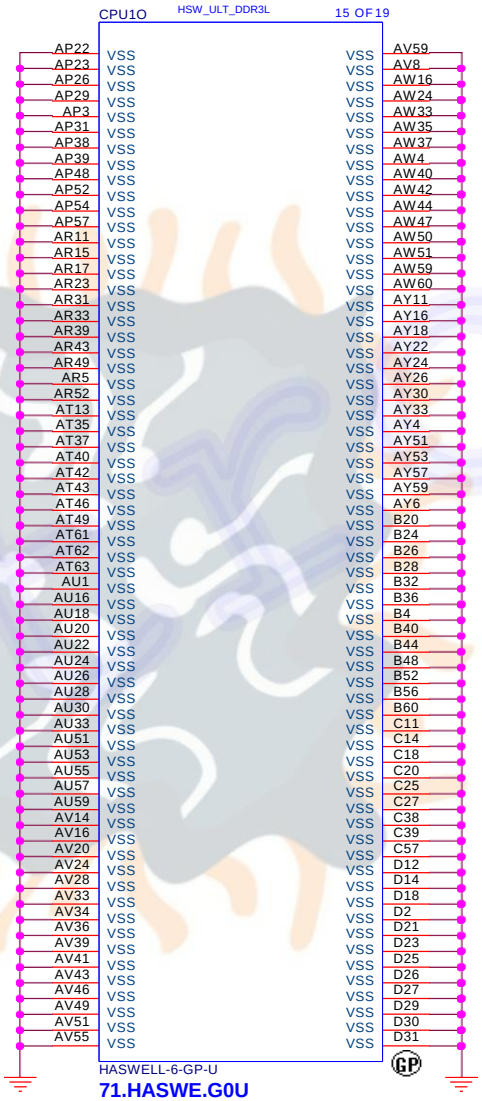
Title: CPU (RSVD)

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 22 of 102

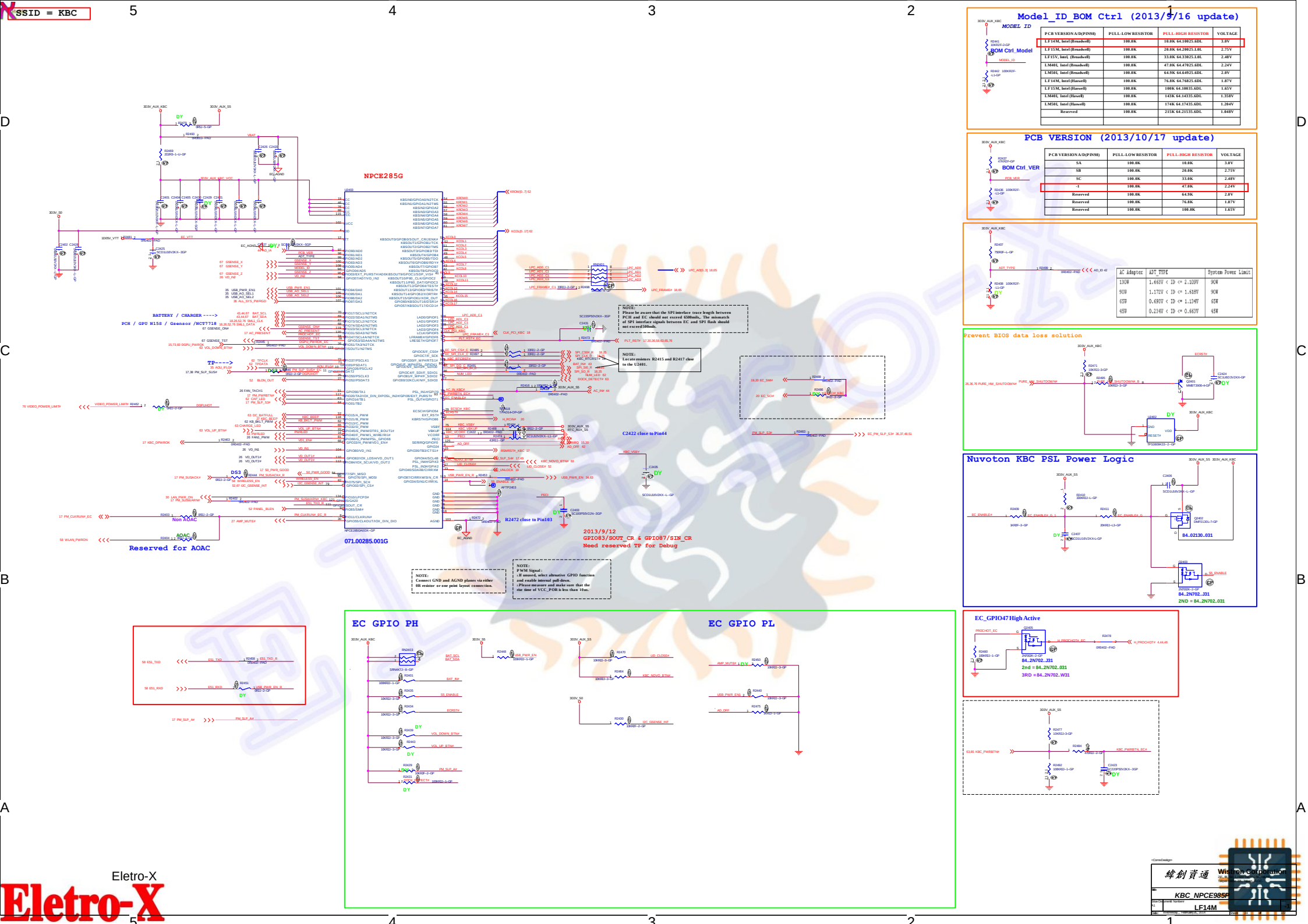
SSID = PCH





M40

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (VSS)***
Size: Custom	Document Number: **LF14M**
Date: Wednesday, February 26, 2014	Sheet 23 of 102



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LF14M, Intel (Broadwell)	100.0K	10.0K 64.10025.6DL	3.0V
LF15M, Intel (Broadwell)	100.0K	20.0K 64.20025.1.0L	2.75V
LF15V, Intel, (Broadwell)	100.0K	33.0K 64.33025.1.0L	2.48V
LM40I, Intel (Broadwell)	100.0K	47.0K 64.47025.6DL	2.24V
LM50I, Intel (Broadwell)	100.0K	64.9K 64.64925.6DL	2.0V
LF14M, Intel (Haswell)	100.0K	76.8K 64.76825.6DL	1.87V
LF15M, Intel (Haswell)	100.0K	100K 64.10035.6DL	1.65V
LM40I, Intel (Haswell)	100.0K	143K 64.14335.6DL	1.358V
LM50I, Intel (Haswell)	100.0K	174K 64.17435.6DL	1.204V
Reserved	100.0K	215K 64.21535.6DL	1.048V

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-I	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

AC Adapter	ADT TYPE	System Power Limit
130W	1.663V < ID <= 2.109V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

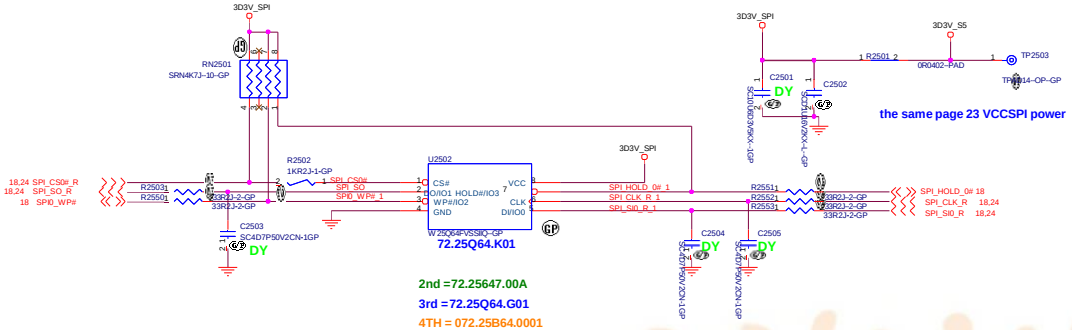
Eletro-X

KBC_NPCE985P

LF14M

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

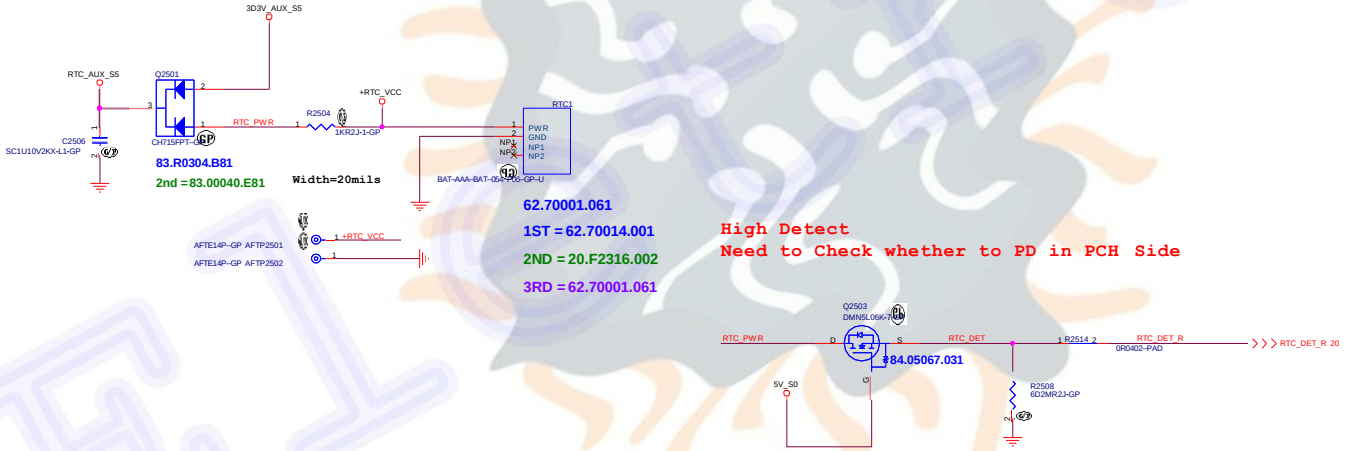


2nd =72.25647.00A

3rd =72.25Q64.G01

4TH = 072.25B64.0001

SSID = RBATT



83.R0304.B81

2nd = 83.00040.E81

Width=20mils

62.70001.061

1ST = 62.70014.001

2ND = 20.F2316.002

3RD = 62.70001.061

High Detect

Need to Check whether to PD in PCH Side

884.05067.031

M40

緯創資通 Wistron Corporation

21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

Size: A2 | Document Number: LF14M | Rev: 1A

Date: Wednesday, February 26, 2014 | Sheet 25

SSID = Thermal

Thermal sensor NCT 7718W

Layout 15 mil

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm rest

84.03904.E11

74.07718.0B9

2ND = 074.00788.00B9

84.2N702.A3F

2nd = 75.00601.07C

83.R5003.H8H

20.F1621.004

1ST = 020.F0156.0004

2ND = 20.F1937.004

ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

System Sensor

69.60013.201

CPU Sensor

69.60013.201

T8=85 degree

83.00056.Q11

84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31

PTC Function M40/M50 (All Series Reserved)

5V *100K/(100K+40K) = 3.57V

84.2N702.J31

2ND = 84.2N702.031

3RD = 84.2N702.W31

74.00331.A2F

	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

PTC Placement List

	PTC Position
RT2606	5V_PWR_DC/DC_High_side_FET (PU4507)
RT2605	3V_PWR_DC/DC_High_side_FET (PU4504)
RT2609	BT+ High side FET (PU4403)
RT2607	1D05V_PWR_DC/DC_High_side_FET (PU4802)
RT2603	1D35V_S3_DC/DC_High_side_FET (PU4902)
RT2610	
RT2602	1D5V_PWR_DC/DC_High_side_FET (PU5110)
RT2601	VCC_CORE_Driver-2 (PU4701)
RT2608	VGA_CORE_DC/DC_MOSFET (PU8202)

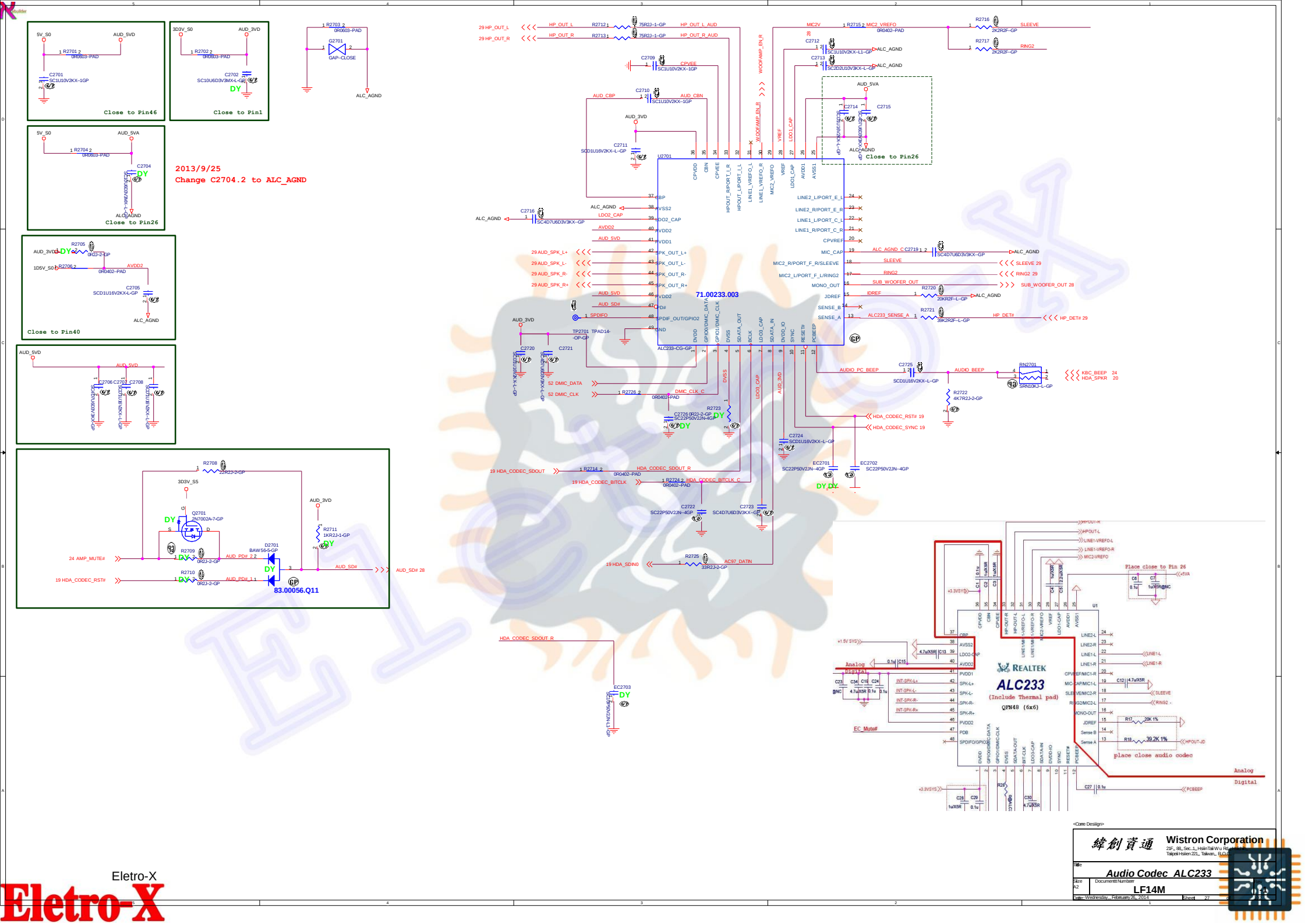
<Core Design>

Wistron Corporation

Title: Thermal 7718/Fan Controllor P2793

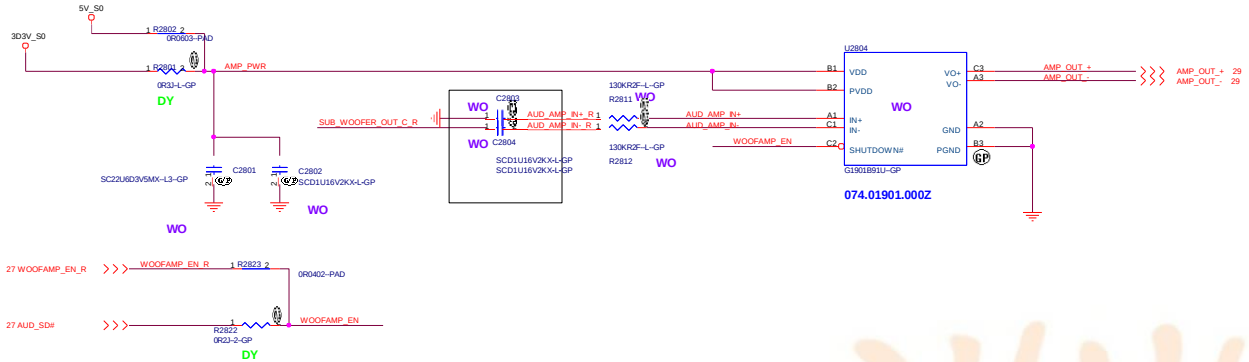
Size: A2 | Document Number: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 26

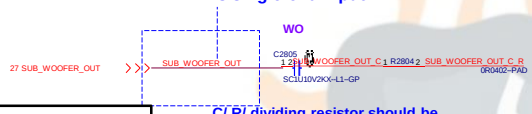

Close to Pin46
Close to Pin1
Close to Pin26
2013/9/25
Change C2704.2 to ALC_AGND
Close to Pin40
71.00233.003
83.00056.Q11
ALC233-CG-GP
ALC233
(Include Thermal pad)
QFN48 (6x6)
REALTEK
Close to Pin26
place close audio codec
Analog
Digital
Wistron Corporation
Audio Codec ALC233
LF14M

Eletro-X

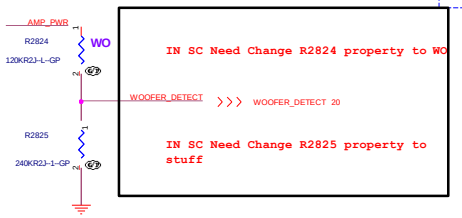
WOOFER AMP. U40/U50



1.2V vrms single-end input



C/ R/ dividing resistor should be placed nearby amp side.



<Core Design>

Wistron Corporation

Audio Codec ALC233

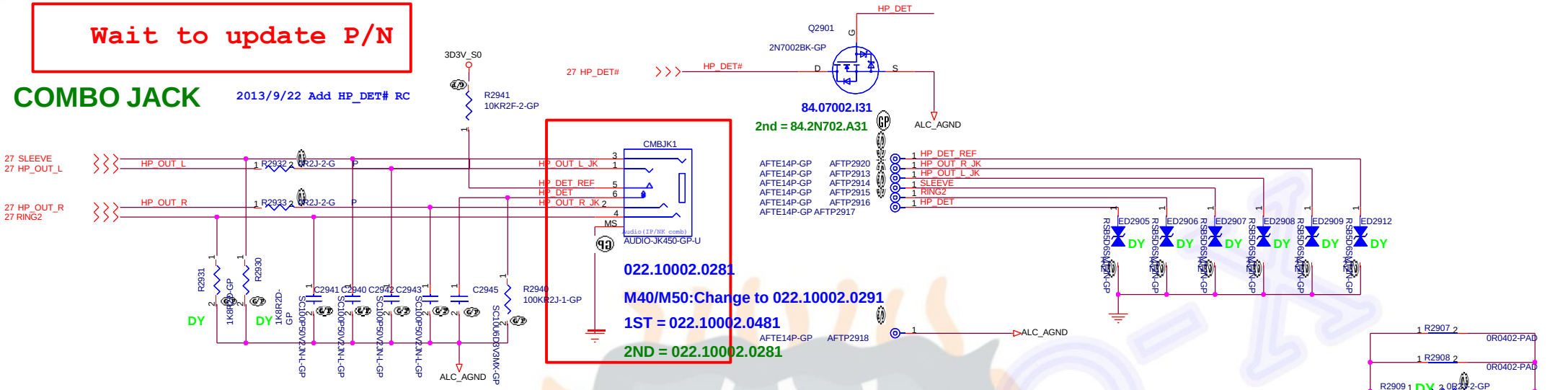
LF14M

Size: A2 | Date: Wednesday, February 26, 2014 | Sheet 28

Wait to update P/N

COMBO JACK

2013/9/22 Add HP_DET# RC



022.10002.0281

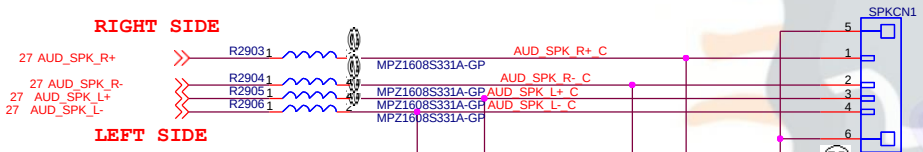
M40/M50:Change to 022.10002.0291

1ST = 022.10002.0481

2ND = 022.10002.0281

RIGHT SPEAKER

RIGHT SIDE



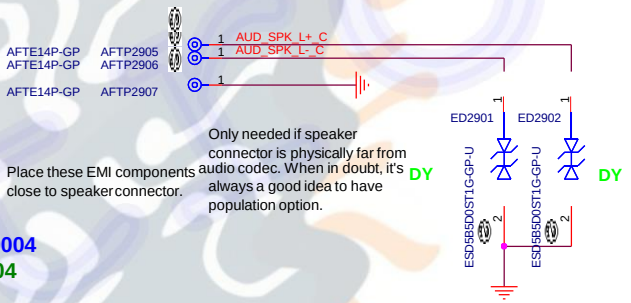
LEFT SIDE

LEFT SPEAKER

20.F1621.004

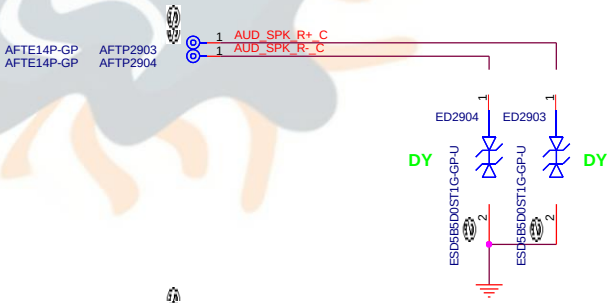
1ST = 020.F0156.0004

2ND = 20.F1937.004

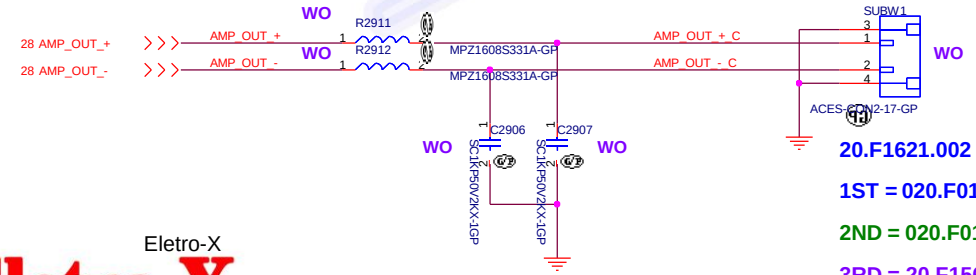


Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



SUB WOOFER (U40/U50)

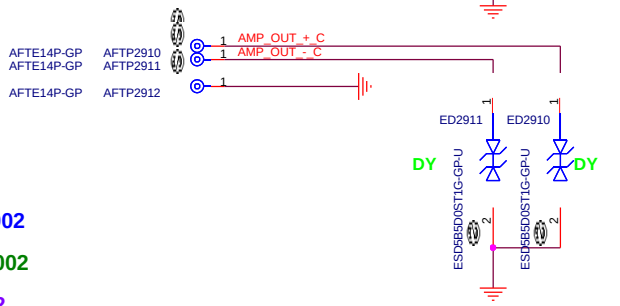


20.F1621.002

1ST = 020.F0156.0002

2ND = 020.F0157.0002

3RD = 20.F1561.002



<Core Desiign>

Wistron Corporation

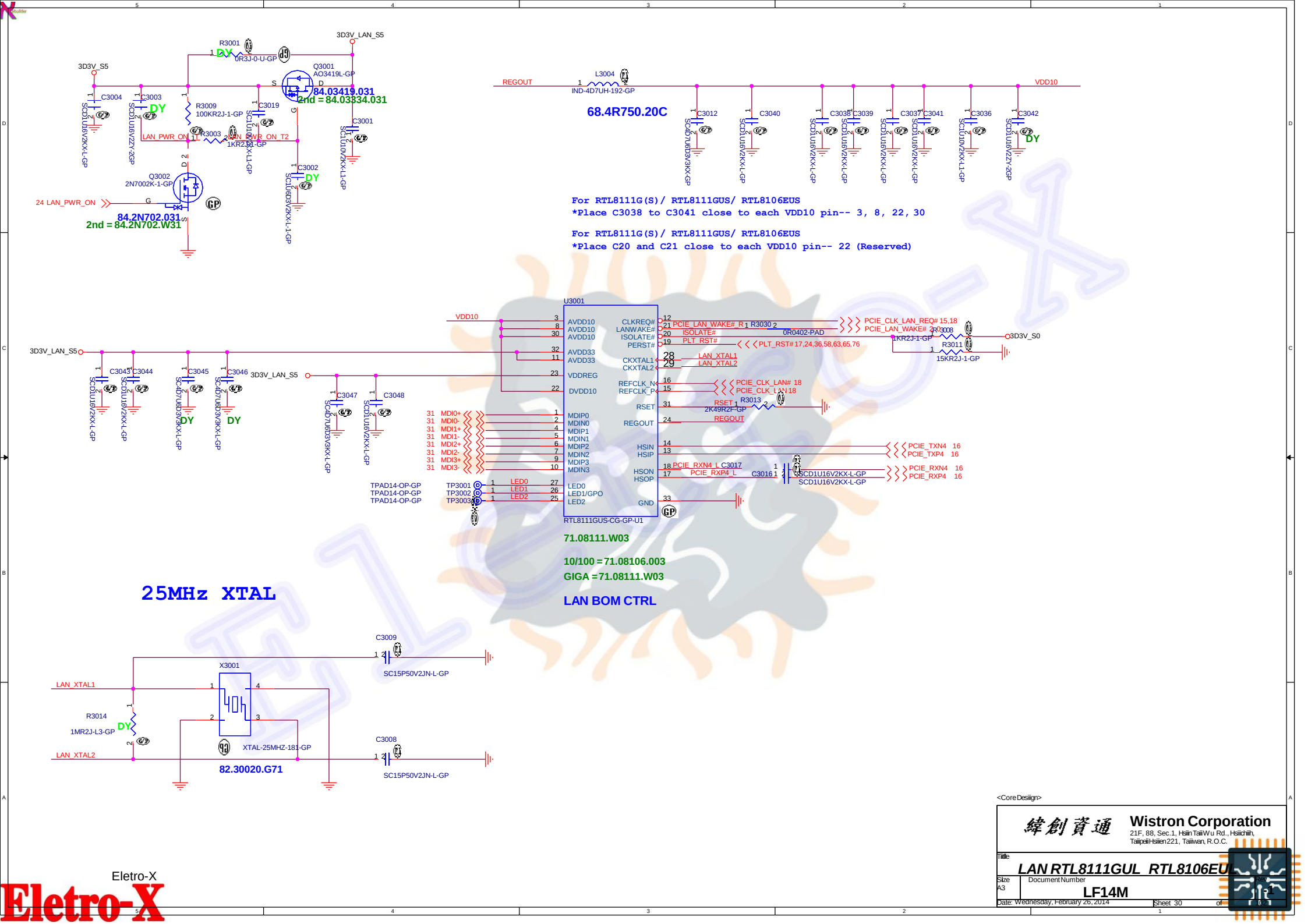
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size: A3 | Document Number: LF14M | Rev: 1

Date: Wednesday, February 26, 2014 | Sheet 29 of 101

Eletro-X



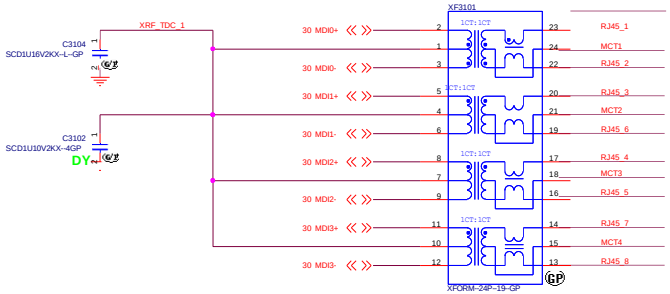
<Core Desiign>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111GUL RTL8106EU

Size	Document Number	Rev
A3	LF14M	1.0

Date: Wednesday, February 26, 2014 Sheet 30 of 40

10/100M/1000M Lan Transformer

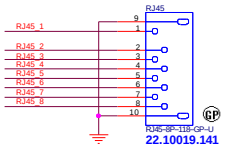


68.IH601.301

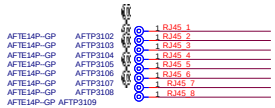
1ST = 068.IH219.3001

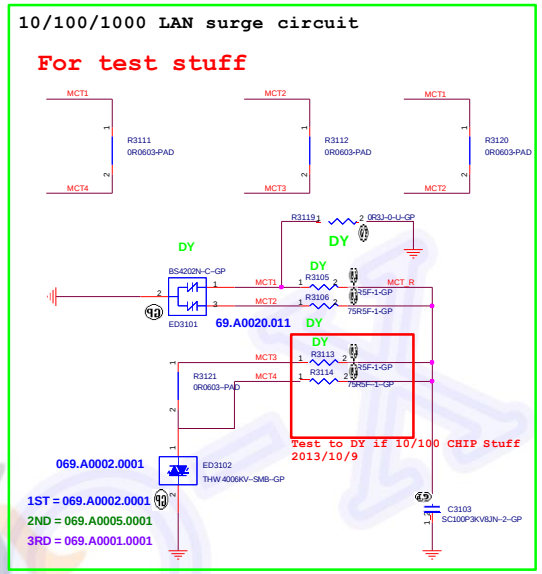
2ND = 68.89246.301

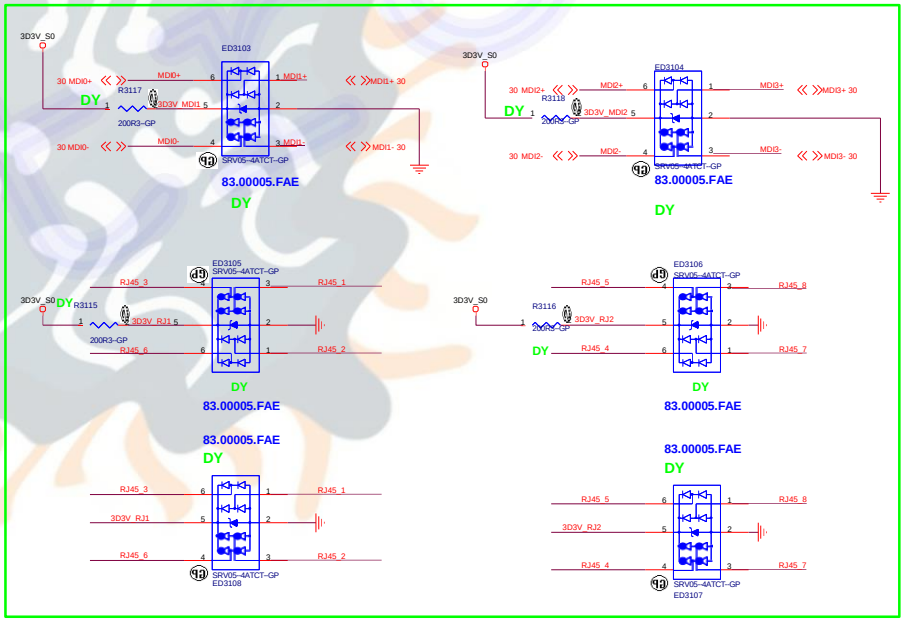
LAN Connector



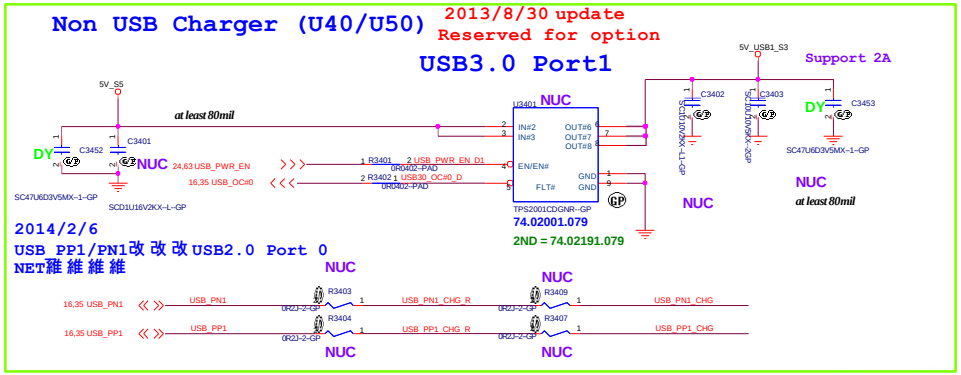
22.10019.141

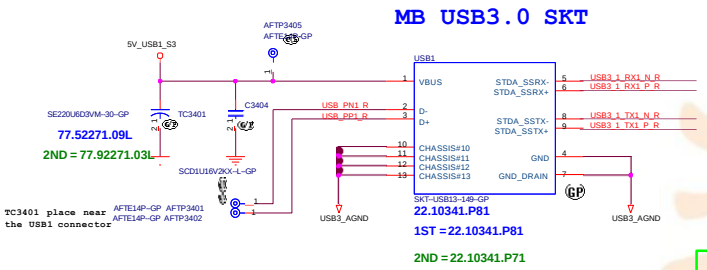


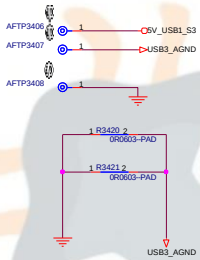


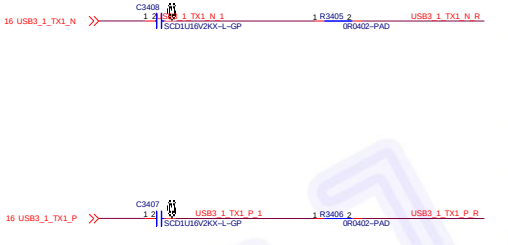


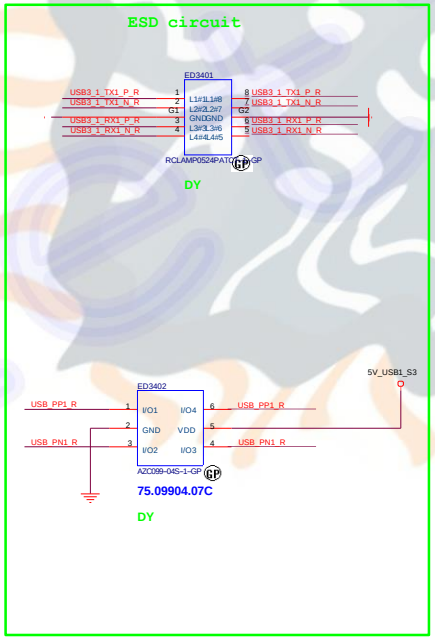
<Core Design>
緯創資通 Wistron Corporation
21F., 88, Sec. 1, HsinTai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: LAN CONNECTOR
Size: A2
Document Number: LF14M
Rev:
Date: Wednesday, February 26, 2014
Sheet 31











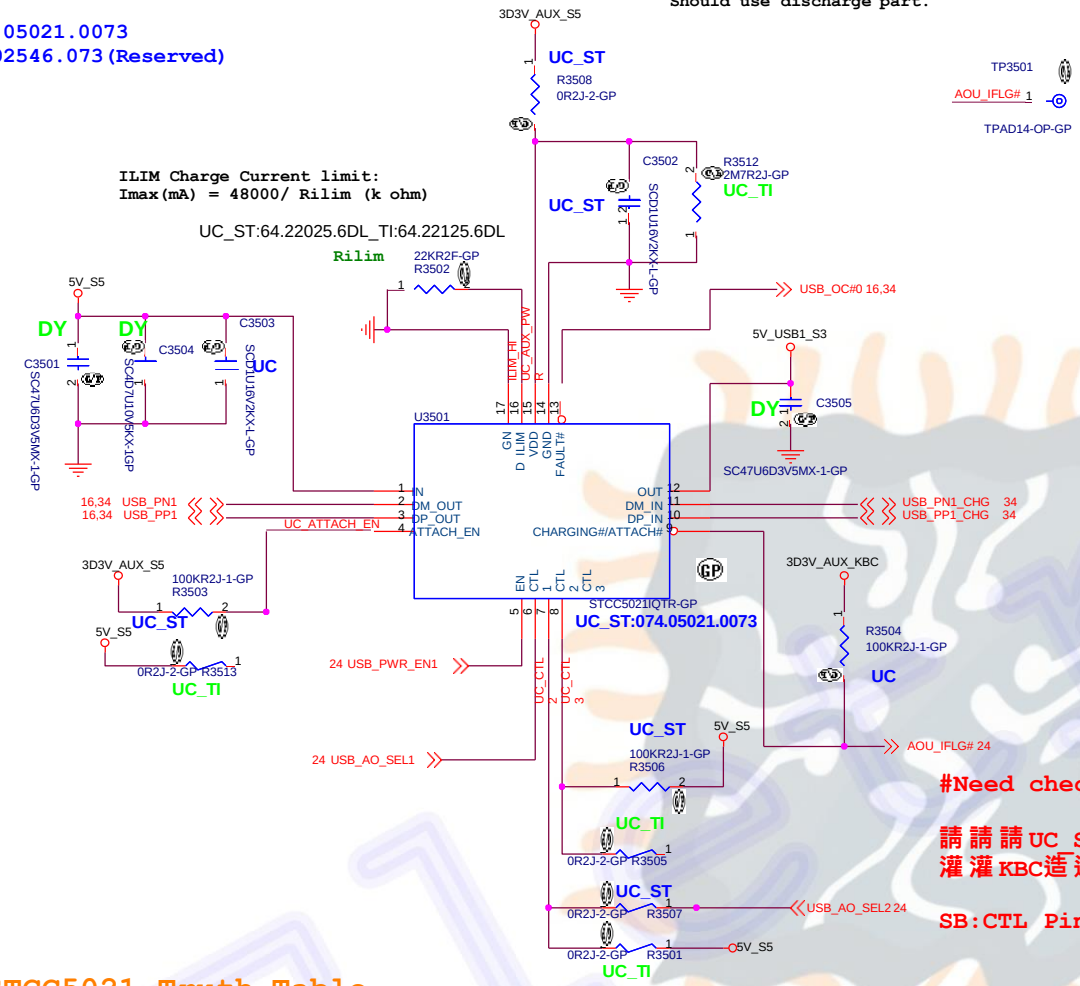
<Comp Desiign>
緯創資通 Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
USB 2.0 / 3.0 Port
Size A2
Document Number
LF14M
Date: Wednesday, February 26, 2014
Sheet 34

USB Charger (M40/M50)

ST:074.05021.0073
TI:74.02546.073(Reserved)

2013/9/10 Change Power Source to 5V_S5
2013/9/18 Change Charger IC to STCC5021

Should use discharge part.



#Need check KBC GPIO Port is PSL_IN

請請請UC_ST和UC_TI同同同同，以以5V電電灌灌KBC造造造造

SB:CTL Pin改造3D3V_S5 Source

STCC5021 Truth Table

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

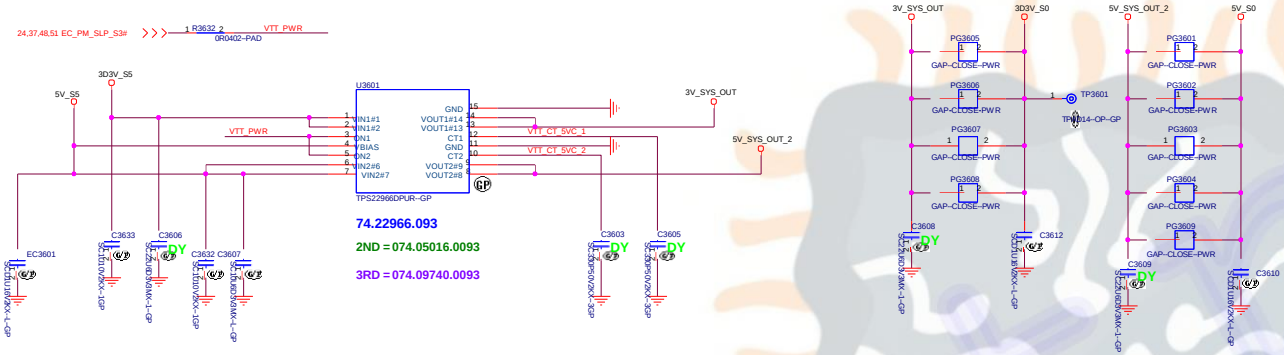
M40

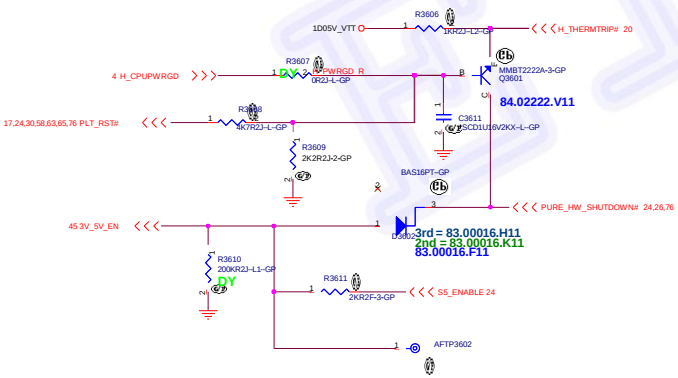
緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, TaipeiHsien 221, Taiwan, R.O.C.

Title: USB 3.0
Size: A3
Document Number: LF14M
Rev: 1.0
Date: Wednesday, February 26, 2014
Sheet 35 of 40

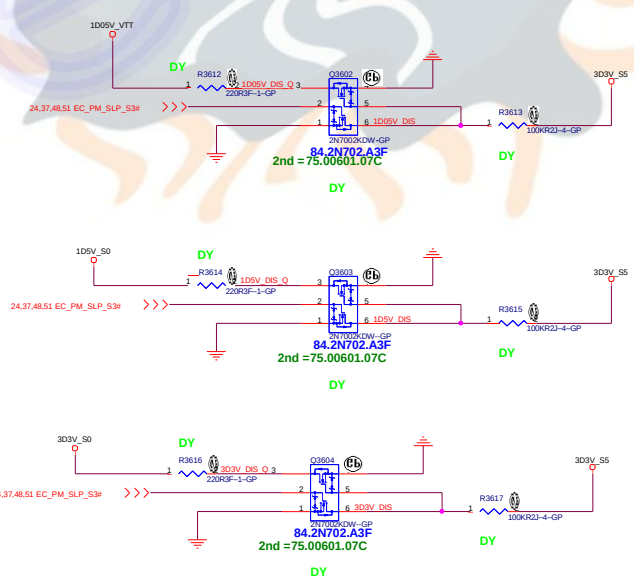
Power Sequence

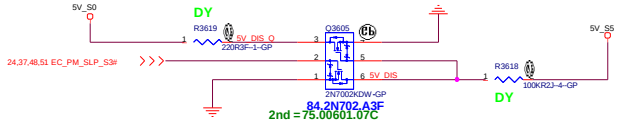
Run Power





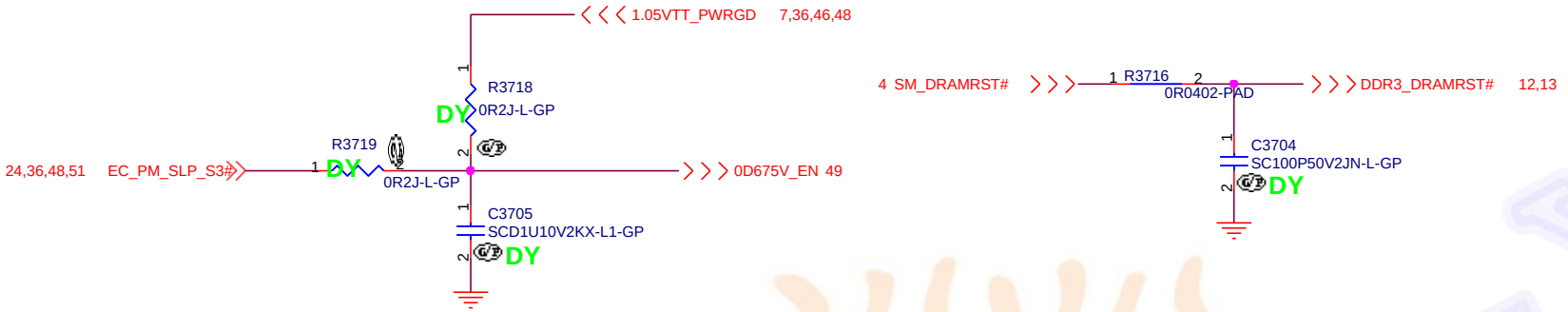
Discharge circuit

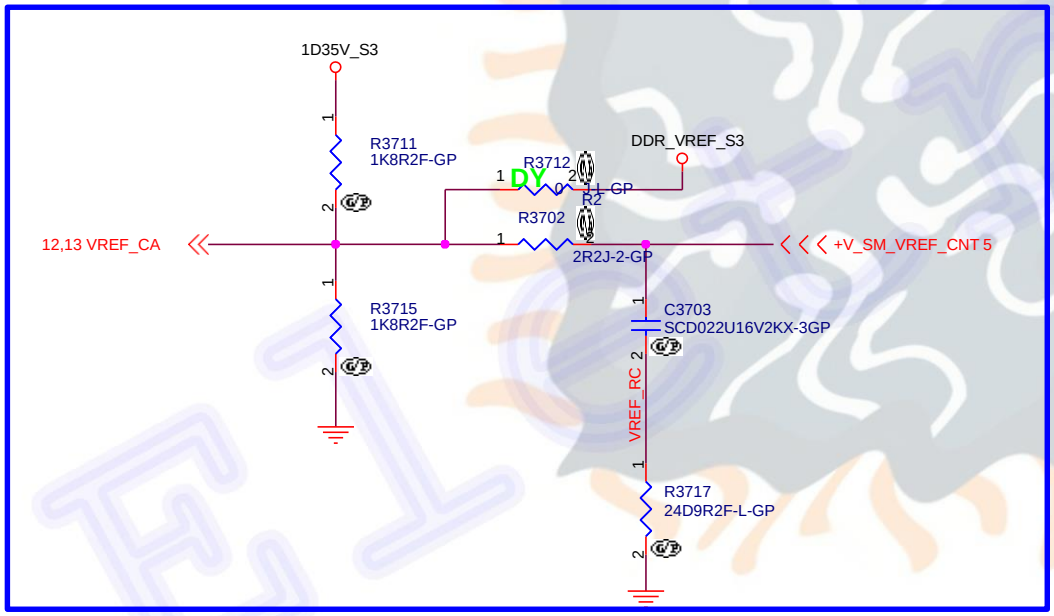




M40

緯創資通	Wistron Corporation
Title	Power Plane Enable & SEQUENCE
Size A2	Document Number LF14M
Date: Wednesday, February 26, 2014	Sheet 36





For Intel Recommend Close to DIMM

M40

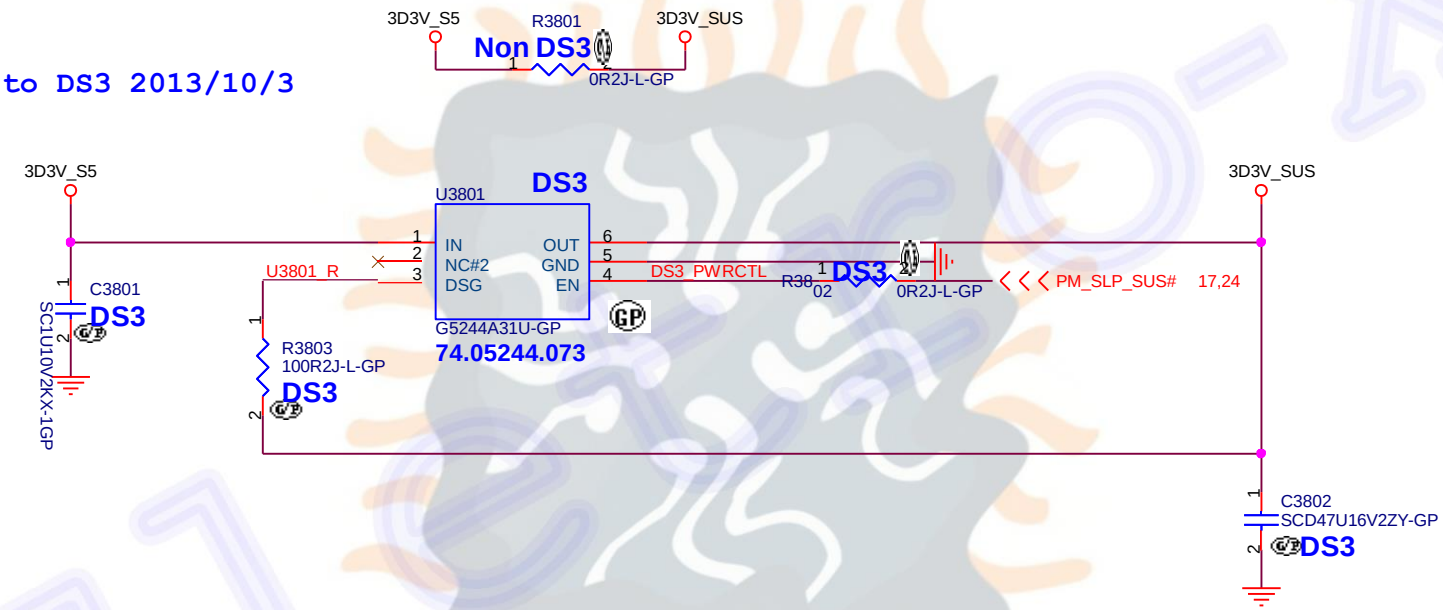
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ADAPTER OCP / S3 reduction

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 37 of 102

C3801 Change to DS3 2013/10/3



M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

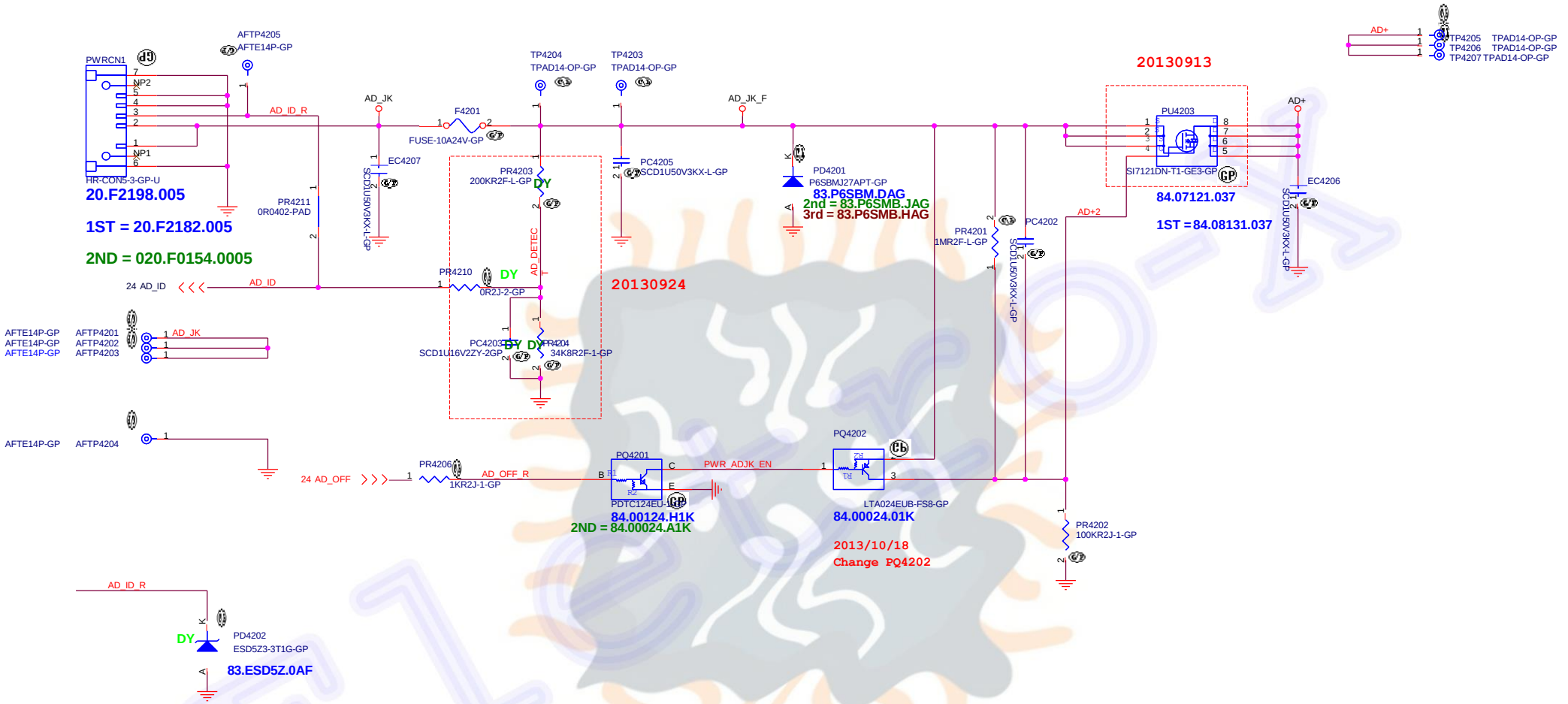
Title: *(Reserved)*

Size	Document Number	Rev
A4	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 38 of 102

DC Jack

Adaptor in to generate DCBATOUT



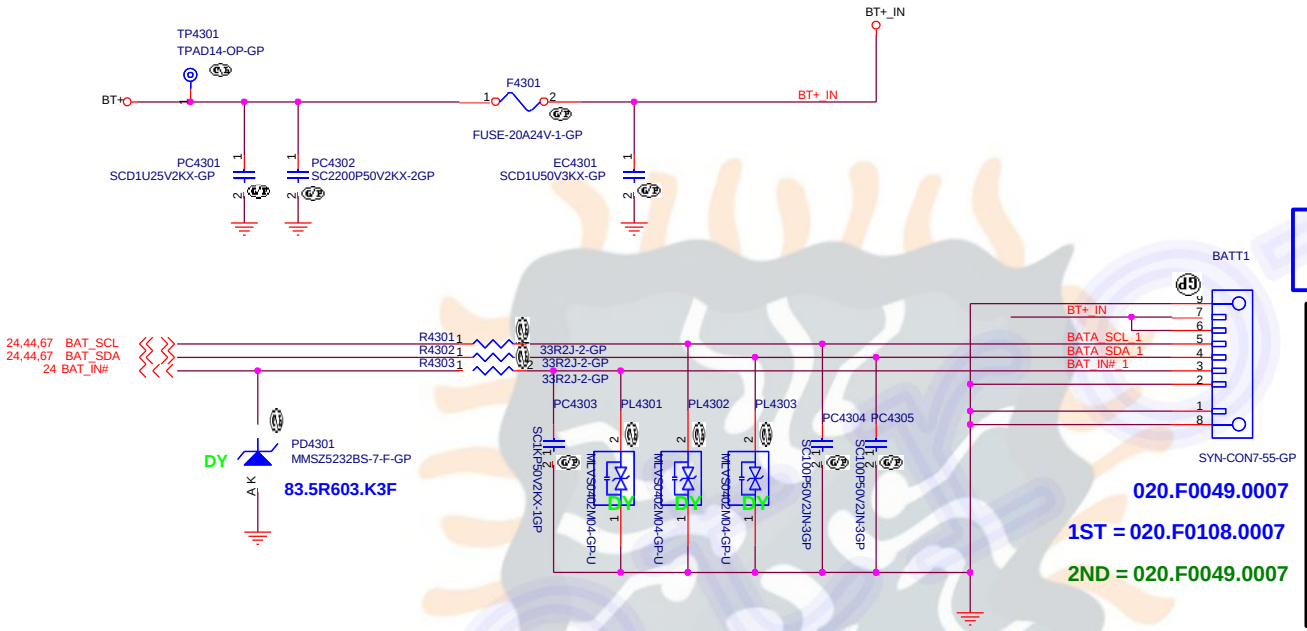
<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN JACK		
Size: A3	Document Number: LF14M	Rev: 1
Date: Wednesday, February 26, 2014	Sheet 42	of 0

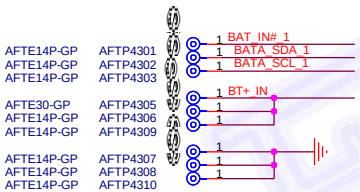
Eletro-X

BATTERY CONNECTOR



2013/10/4
Pin Define

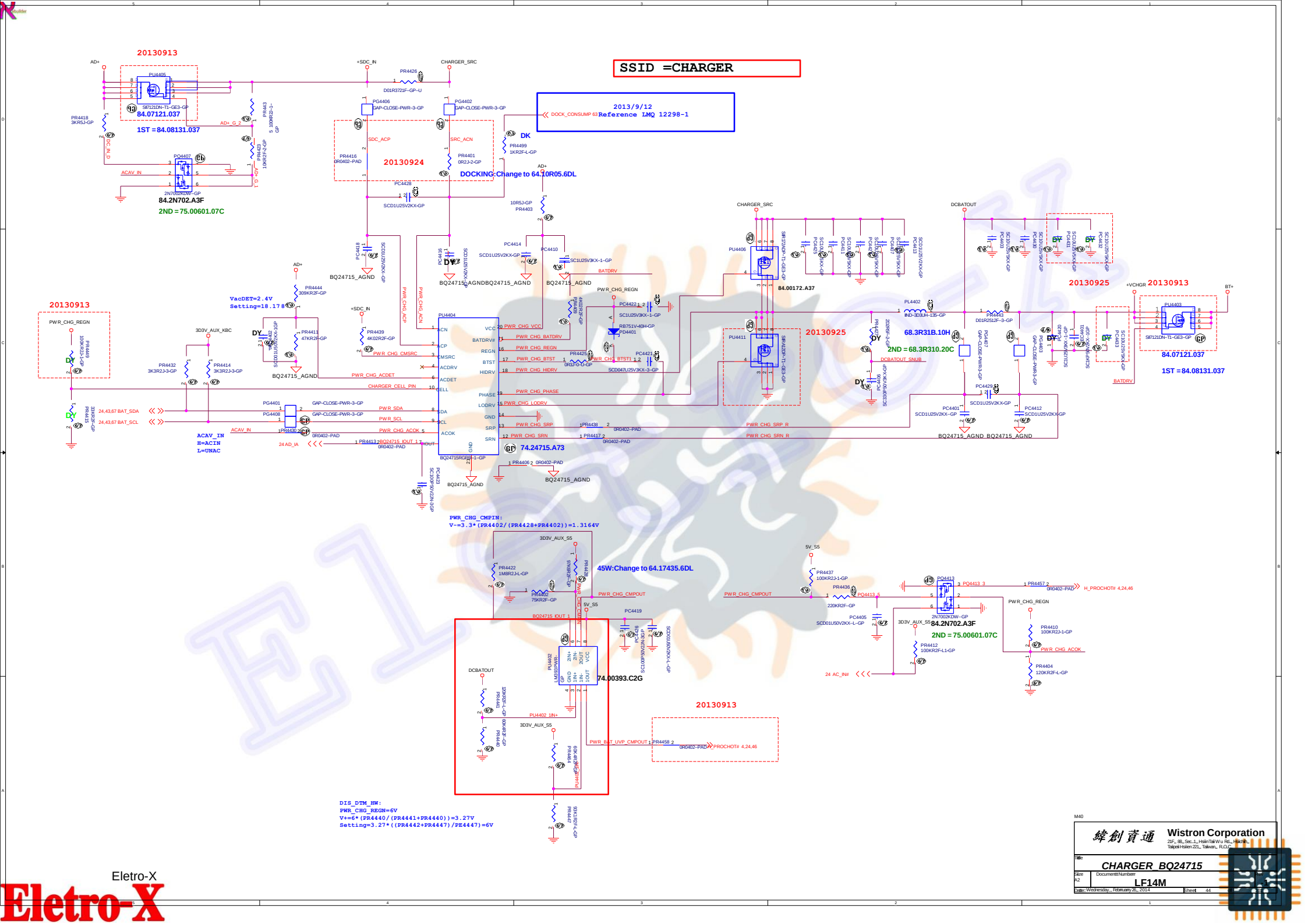
Pin#	Comments	Color
1	GND-	BLACK
2	GND-	BLACK
3	ID	WHITE
4	SMD	GREEN
5	SMC	BLUE
6	BATT+	RED
7	BATT+	RED

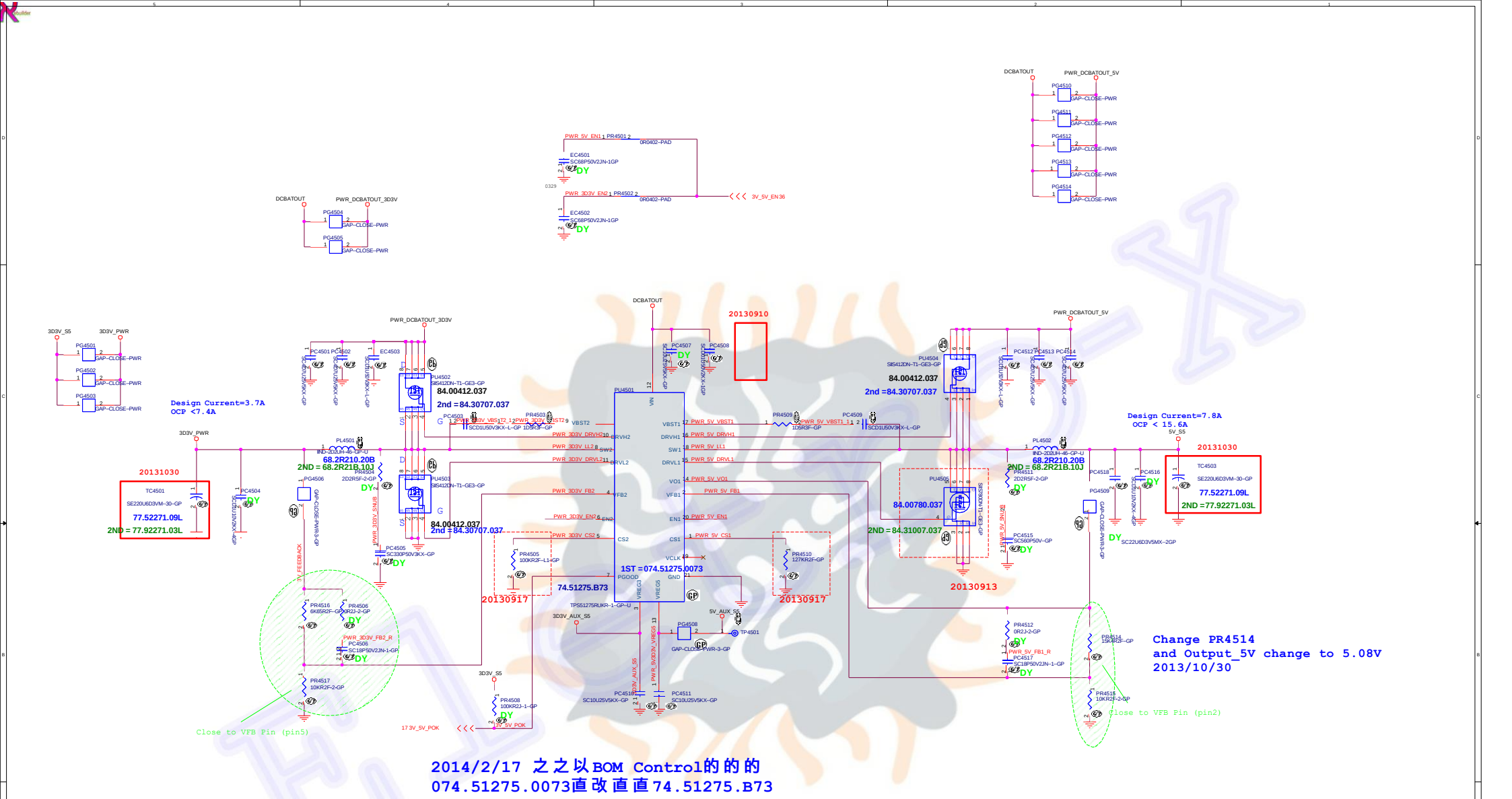


<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichiih, TaiipeiiHsiien221, Taiiiwan, R.O.C.

Tiitle: BATT CONN
Size: A3
Document Number: LF14M
Rev: 1
Date: Wednesday, February 26, 2014
Sheet 43 of 101


SSID =CHARGER
2013/9/12
Reference LMQ 12298-1
20130913
20130924
20130925
84.07121.037
1ST = 84.08131.037
84.2N702.A3F
2ND = 75.00601.07C
DOCKING:Change to 64.10R05.6DL
VacDET=2.4V
Setting=18.178
84.00172.A37
68.3R31B.10H
2ND = 68.3R310.20C
74.24715.A73
74.00393.C2G
45W:Change to 64.17435.6DL
PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.3164V
ACAV_IN
H=ACIN
L=UNAC
DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PE4447)=6V
BQ24715_AGND
BQ24715_IOUT
PWR_CHG_REGN
PWR_CHG_CMPOUT
PWR_BAT_UVP_CMPOUT
PWR_CHG_ACOK
PWR_CHG_CMSRC
PWR_CHG_ACDET
CHARGER_CELL_PIN
PWR_SDA
PWR_SCL
24,43,67 BAT_SDA
24,43,67 BAT_SCL
DCBATOUT
CHARGER_SRC
+SDC_IN
AD+
Wistron Corporation
CHARGER_BQ24715
LF14M



Eletro-X

M40

緯創資通 Wistron Corporation

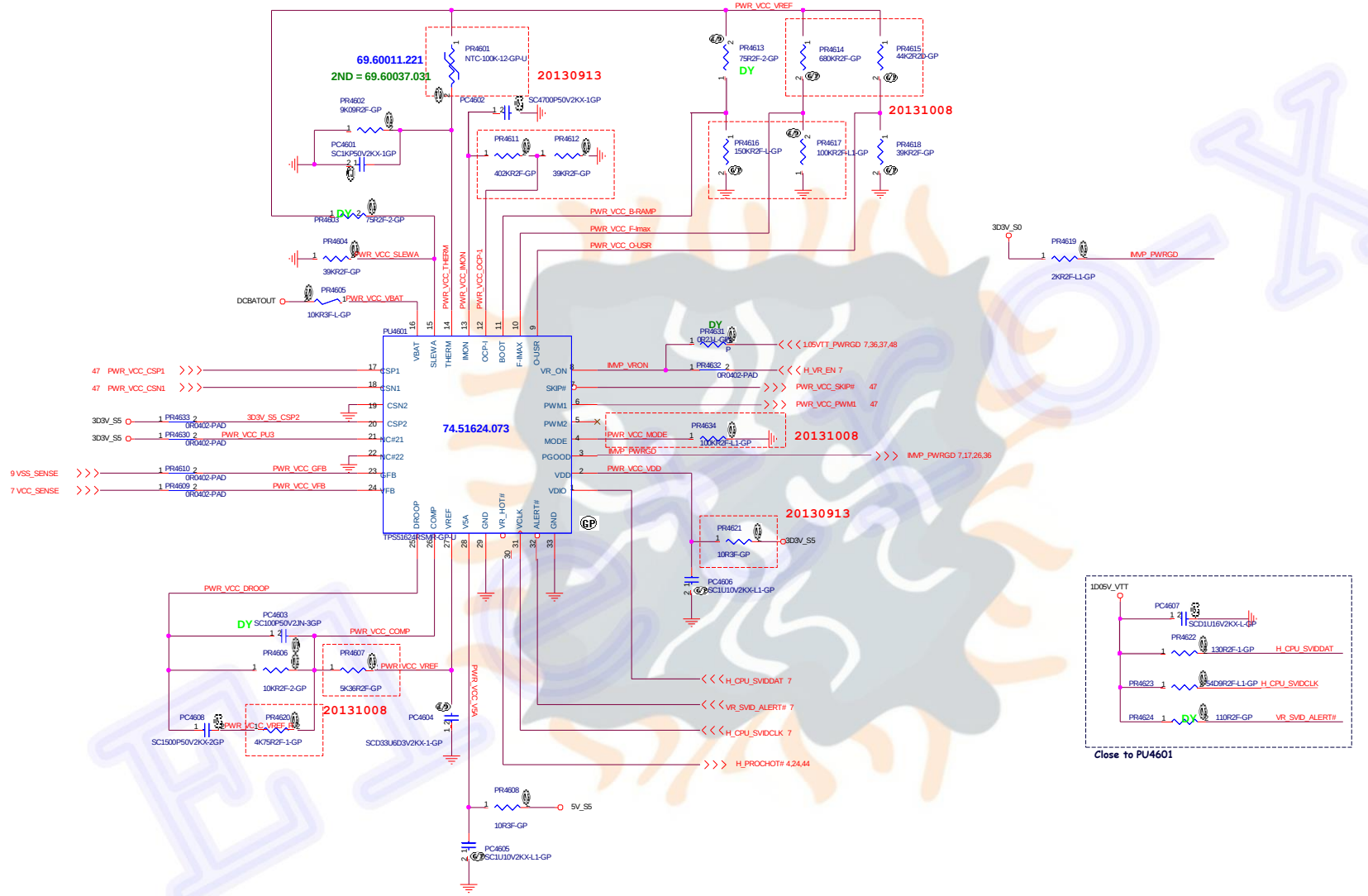
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

TPS51225 5V/3D3V

Size: A2 | Document Number: LF14M

Date: Wednesday, February 26, 2014 | Sheet 45

SSID = CPU.Regulator



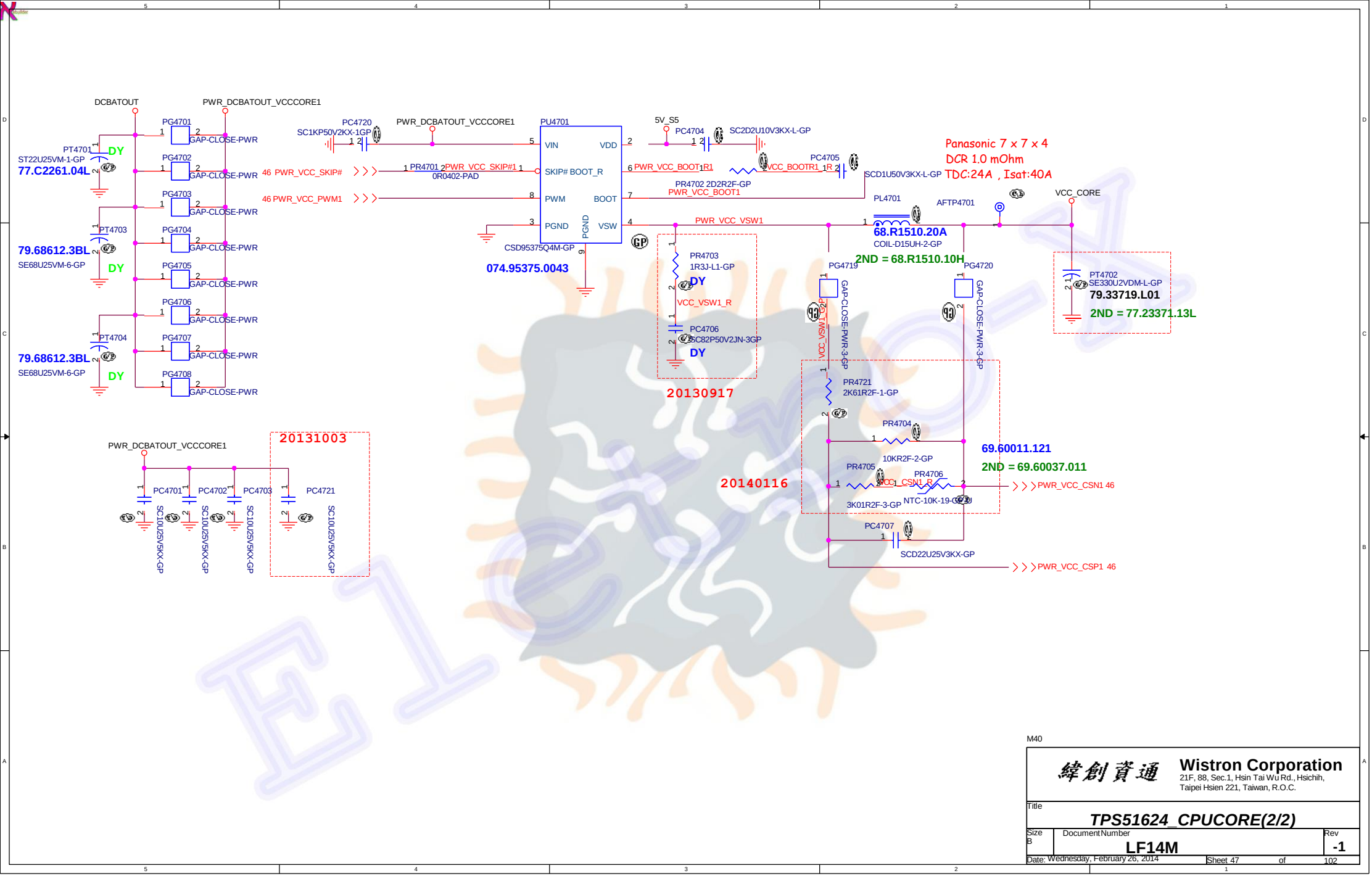
M40

Wistron Corporation
21F., 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: TPS51624_CPUCORE(1/2)

Size: C | Document Number: LF14M | Rev: -1

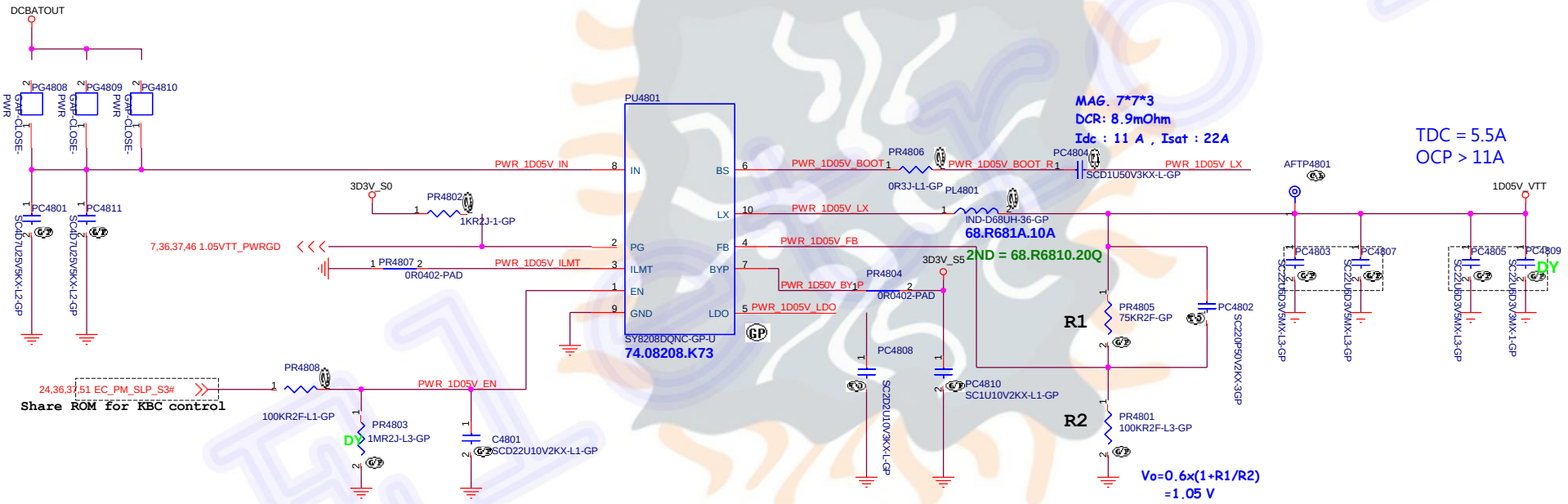
Date: Wednesday, February 26, 2014 | Sheet 45 of 102



M40

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *TPS51624_CPUCORE(2/2)*		
Size: B	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 47 of 102	

SY8208D for 1D05V



M40

Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien221, Taiwan, R.O.C.

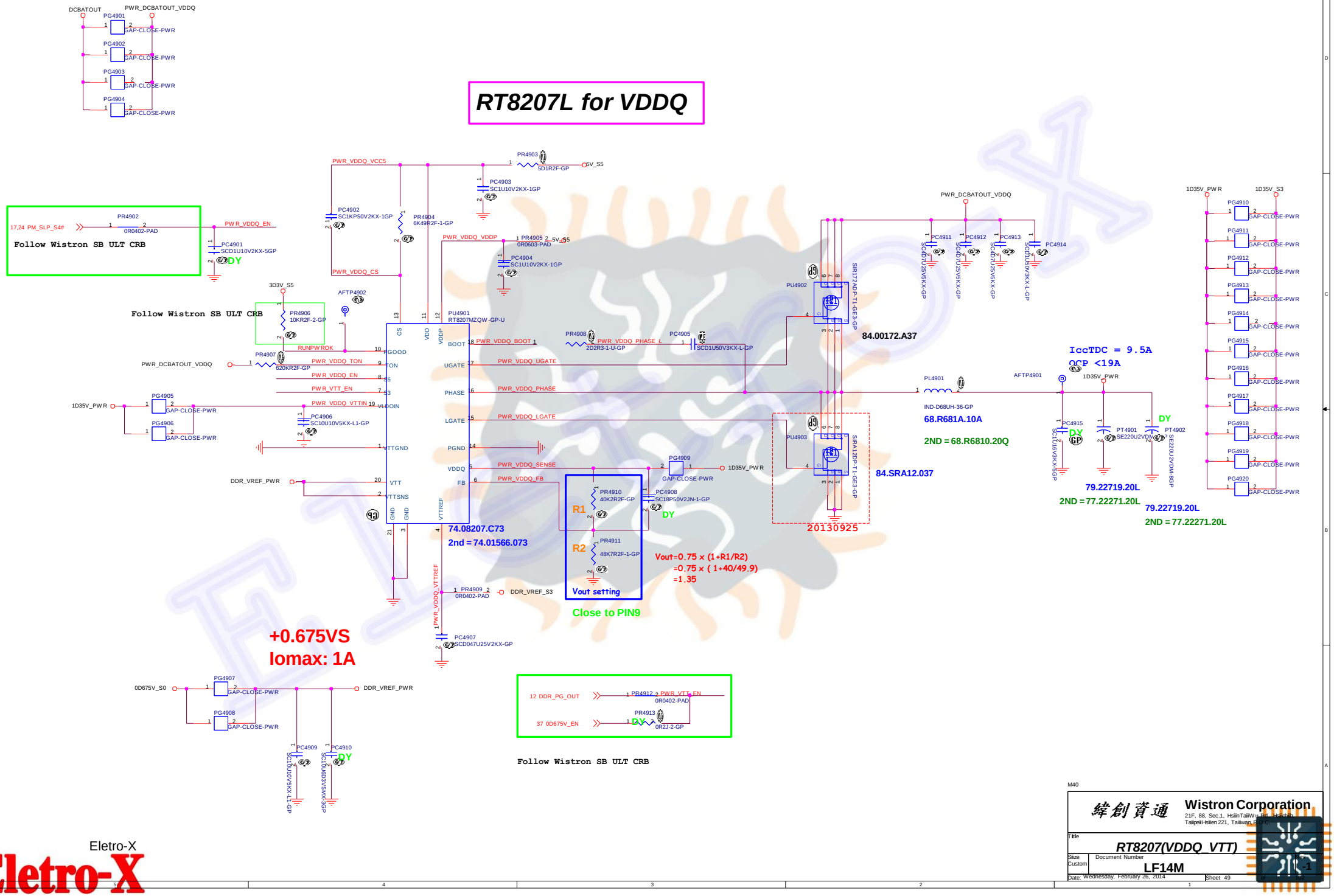
Title: DC to DC_1D05V(SY8208)

Size: A3 | Document Number: LF14M | Rev: 1

Date: Wednesday, February 26, 2014 | Sheet 48 of 101

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8207L for VDDQ



M40

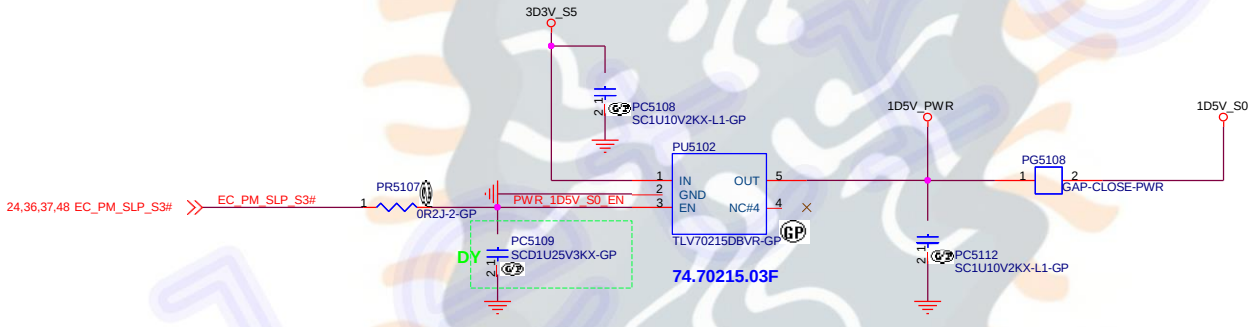
Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: RT8207(VDDQ_VTT)

Size: Custom | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 49

TLV70215 for 1D5V_S0



M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D5V_S0 TLV70215

Size: A3 | Document Number: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 51 of 60

SSID = VIDEO

INVERTER POWER

DCBATOUT_LCD → F5201 POLYSW-1D1A24V-GP-U → DCBATOUT

69.50007.A31

2nd = 69.50007.A41

C5206 SC4D7U6D3V3KX-GP DY
C5204 SC4D7U6D3V3KX-GP
C5205 SC4D7U6D3V3KX-GP
C5211 SC4D7U6D3V3KX-GP DY

CAMERA POWER

Layout 40 mil

3D3V_CAMERA_S0 → R5218 0R2J-0-U-GP → 3D3V_S0

R5222 0R2J-0-U-GP 3D3V_S0_CAMERA

U5204 SY6288C20AAC-GP (OUT, GND, OC#, IN, EN) DY

CAMERA_EN 20

C5231 SC4D7U6D3V3KX-GP

C5230 SC4D7U6D3V3KX-GP

074.06288.007B

Close to eDP connector

LCD_BRIGHTNESS → EC5202 SC2200P2KN-3GP DY

SSID = VIDEO

LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

Layout 40 mil

3D3V_S0 → U5201 SY6288C20AAC-GP (OUT, GND, OC#, IN, EN) → LCDVDD

15 LVDS_VDD_EN → R5207 0R0402-PAD → LCDVDD_EN

R5214 100KR2J-1-GP

C5209 SC4D7U6D3V3KX-GP DY

C5207 SC4D7U6D3V3KX-GP

C5208 SC4D7U6D3V3KX-GP

074.06288.007B

eDP connector

2-lane eDP Compare with LM440T 12306-1:

BLON_OUT_C:LM440T PCH->EC->PANEL

eDP_HPD:LM440T & LE443 invert to eDP_HPD#

Panel BL brightness/Power En/BL En

15 L_BKLT_EN → R5210 0R0402-PAD → PANEL_BLEN 24

24 BLON_OUT → R5203 1KR2J-1-GP → BLON_OUT_C

15 L_BKLT_CTRL → R5208 0R0402-PAD → L_BKLT_CTRL_1

R5230 100KR2J-1-GP

C5210 SC4D7U6D3V3KX-GP

R5232 100KR2J-1-GP DY

C5227 SC100P50V2JN-3GP

Need Check I2C Gsensor Power source and determine whether to add I2C block Circuit

ACES-CON40-18-GP → EDP1

DCBATOUT_LCD

3D3V_AUX_S5_HALL

LID_CLOSE# → R5219 33R2J-Z-GP → BKLT_CTRL_1 → LID_CLOSE# 24

LCD_BRIGHTNESS

BLON_OUT_C

I2C_GSENSE_INT → I2C_GSENSE_INT 24,67

SML1_DATA 18,24,26,76

SML1_CLK 18,24,26,76

DMIC_DATA_R

DMIC_CLK_R

USB_PP7_eDP

USB_PN7_eDP

TOUCH_RST_C

USB_PP3 → USB_PN3 16, USB_PP3 16

eDP_AUXN_C_C S5228 0.1U-16V2KX-L-GP → eDP_AUXN_CPU 8

eDP_AUXP_C_C S5226 0.1U-16V2KX-L-GP → eDP_AUXP_CPU 8

eDP_TXN1_C_C S5214 0.1U-16V2KX-L-GP

eDP_TXP1_C_C S5213 0.1U-16V2KX-L-GP → eDP_TXN1_CPU 8, eDP_TXP1_CPU 8

eDP_TXN0_C_C S5232 0.1U-16V2KX-L-GP

eDP_TXP0_C_C S5229 0.1U-16V2KX-L-GP → eDP_TXN0_CPU 8, eDP_TXP0_CPU 8

EMB_HPD_R → R5242 0R0402-PAD → EDP_PCB_EN → EMB_HPD 15

DMIC1_VCC

Touch_3V3

3D3V_GSENSE

3D3V_CAMERA_S0

LCDVDD_R → R5228 0R0603-PAD → LCDVDD

C5222 SC4D7U6D3V2KX-L-GP

C5224 SC4D7U6D3V2KX-L-GP

20.K0678.040

1ST = 20.K0678.040

2ND = 20.K0809.040

AFTP5225 AFTE14P-GP

LCDVDD_R, USB_PP3, USB_PN3, DCBATOUT_LCD, BLON_OUT_C, LCD_BRIGHTNESS, DMIC_DATA_R, DMIC_CLK_R → AFTP5201–AFTP5236 AFTE14P-GP

3D3V_CAMERA_S0, DMIC1_VCC, 3D3V_GSENSE, 3D3V_AUX_S5_HALL, EDP_DCR_EN, EMB_HPD_R, SML1_DATA, SML1_CLK, LID_CLOSE# → AFTP5208–AFTP5250 AFTE14P-GP

Touch_3V3 → R5294 0R2J-2-GP DY → 3D3V_S0

R5223 3D3V_S0_Touch 0R2J-0-U-GP

U5205 SY6288C20AAC-GP (OUT, GND, OC# EN/EN#, IN, EN) TOUCH

C5243 SC4D7U6D3V3KX-GP TOUCH

C5233 SC4D7U6D3V3KX-GP TOUCH

TOUCH_EN → R5225 0R2J-0-U-GP TOUCH → LID_CLOSE#

74.06288.07F

DMIC1_VCC → R5231 0R0402-PAD → 3D3V_S0

C5234 SC4D7U6D3V3KX-GP

3D3V_GSENSE → R5234 0R0402-PAD → 3D3V_S0

C5235 SC4D7U6D3V3KX-GP

3D3V_AUX_S5_HALL → R5235 0R2J-2-GP DY → 3D3V_AUX_S5

C5236 SC4D7U6D3V3KX-GP

D5201 RB551V30-GP

83.R5003.H8H

DMIC_DATA_R → R5236 0R0402-PAD → DMIC_DATA 27

DMIC_CLK_R → R5237 0R0402-PAD → DMIC_CLK 27

USB_PP3

ED5203 ED5204 ED5205 ED5206 ESD5B5D05T1G-GP-U DY

C5225 C5237 SC100P50V2JN-3GP DY

Touch Control BD M40/M50/U40/U50

USB_PP7_eDP → R5292 0R0402-PAD → USB_PP7 16

USB_PN7_eDP → R5241 0R0402-PAD → USB_PN7 16

USB_PP7_CON → R5291 0R2J-2-GP DY

USB_PN7_CON → R5240 0R2J-2-GP DY

CTLBD1 HRS-CON8-GP-GP

Touch_3V3

USB_PP7_CON

USB_PN7_CON

TOUCH_INT_C → R5290 0R2J-2-GP DY → TOUCH_INT 20

TOUCH_RST_C → R5289 0R0402-PAD → TOUCH_RST 20

20.K0823.006

DY

TOUCH_INT_C

TOUCH_RST_C

ED5201 ED5202 ESD5B5D05T1G-GP-U DY

TOUCH_INT_C, TOUCH_RST_C, Touch_3V3, USB_PP7, USB_PN7 → AFTP5238–AFTP5244 AFTE14P-GP

AFTP5226 AFTE14P-GP

<Core Design>

Wistron Corporation

Title: LCD Connector

Size: A2 | Document Number: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 52 of 82

Eletro-X

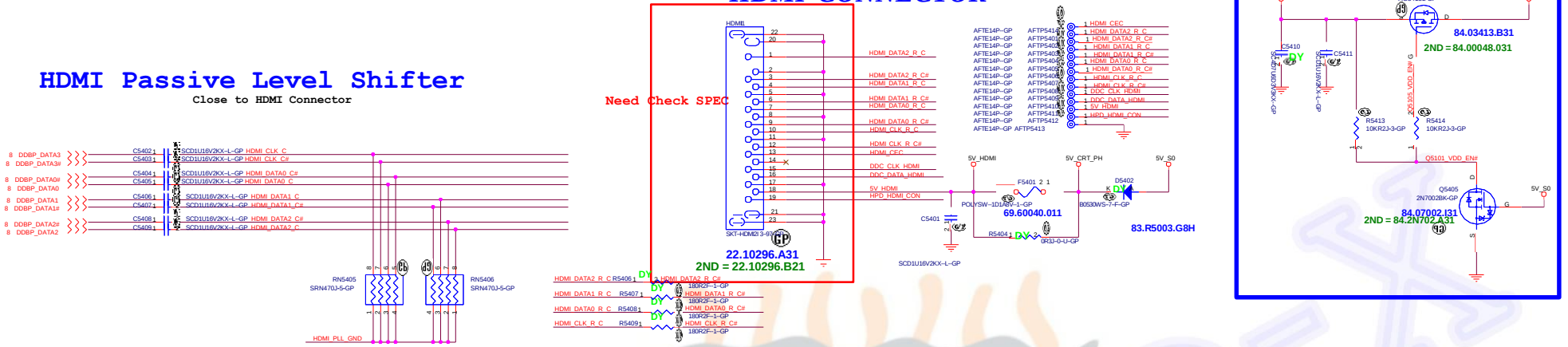
SSID = VIDEO

HDMI CONNECTOR

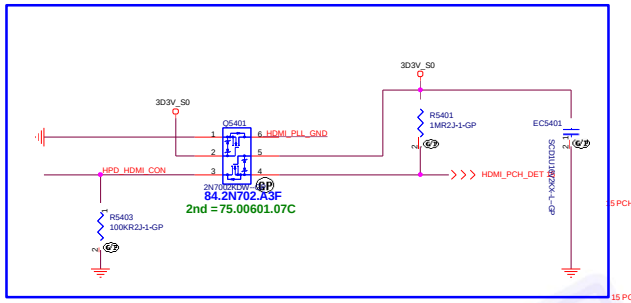
HDMI Passive Level Shifter

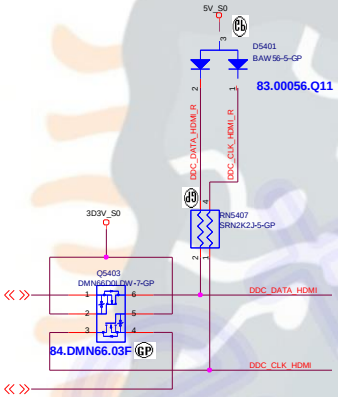
Close to HDMI Connector

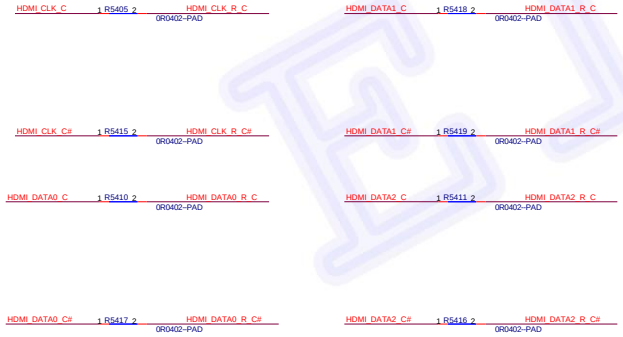
Need Check SPEC

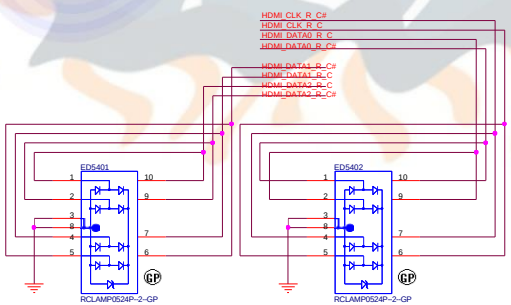


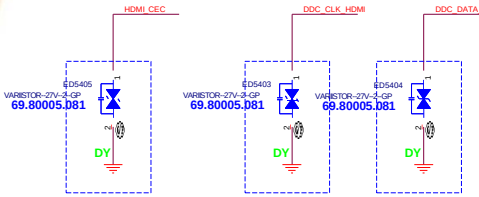
HDMI DDC Passive Level Shifter











DY DY

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

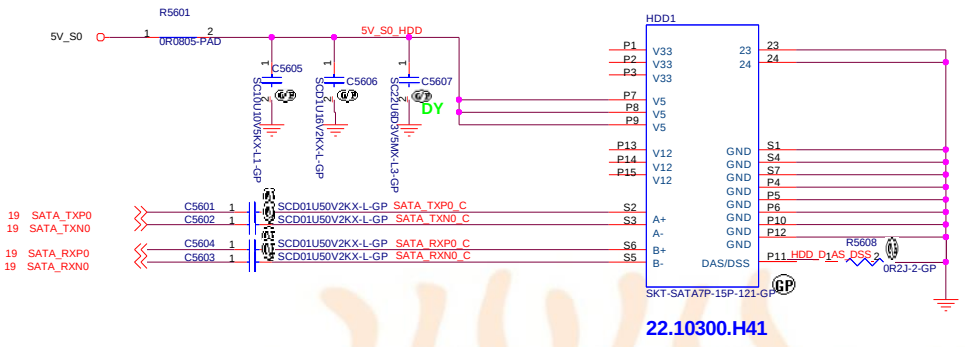
HDMI Level Shifter/Connector

Size A2 | Document Number LF14M | Rev

Date: Wednesday, February 26, 2014 | Sheet 54

SSID = SATA

SATA HDD Connector



2013/9/12
Add Reserved U5602
TVS near HDD connector

ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

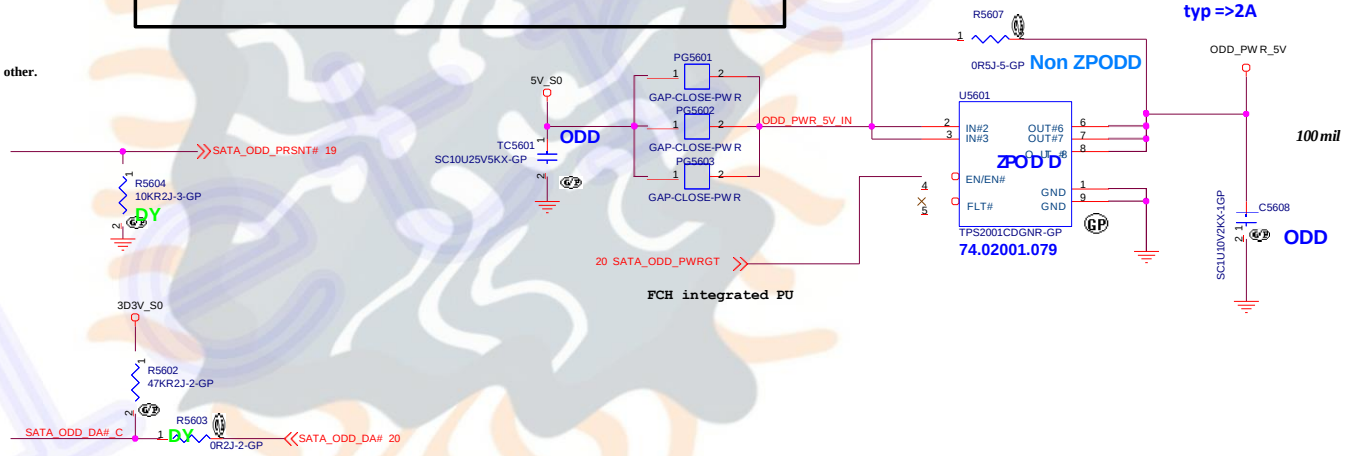
Need Check 2spindle series & Components

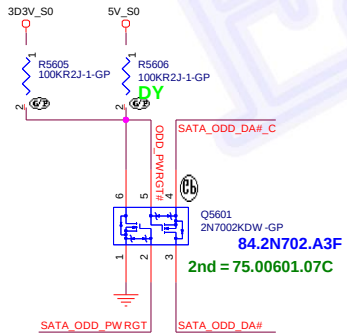
SATA Zero Power ODD

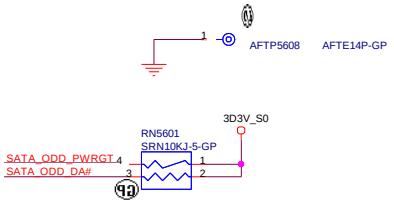
Current limit
Active High
typ =>2A

Follow Intel Zero Power ODD SPEC

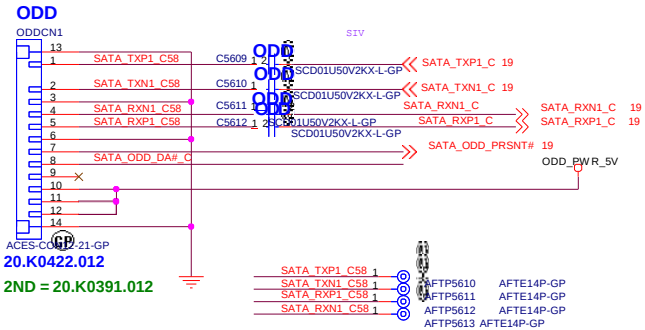
ODD (M50/U50)



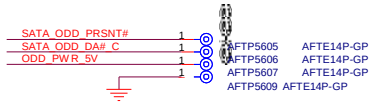




SUPPORT ZERO SATA ODD



原 TC5602,TC5603,FC5604移移改移移



<Core Design>

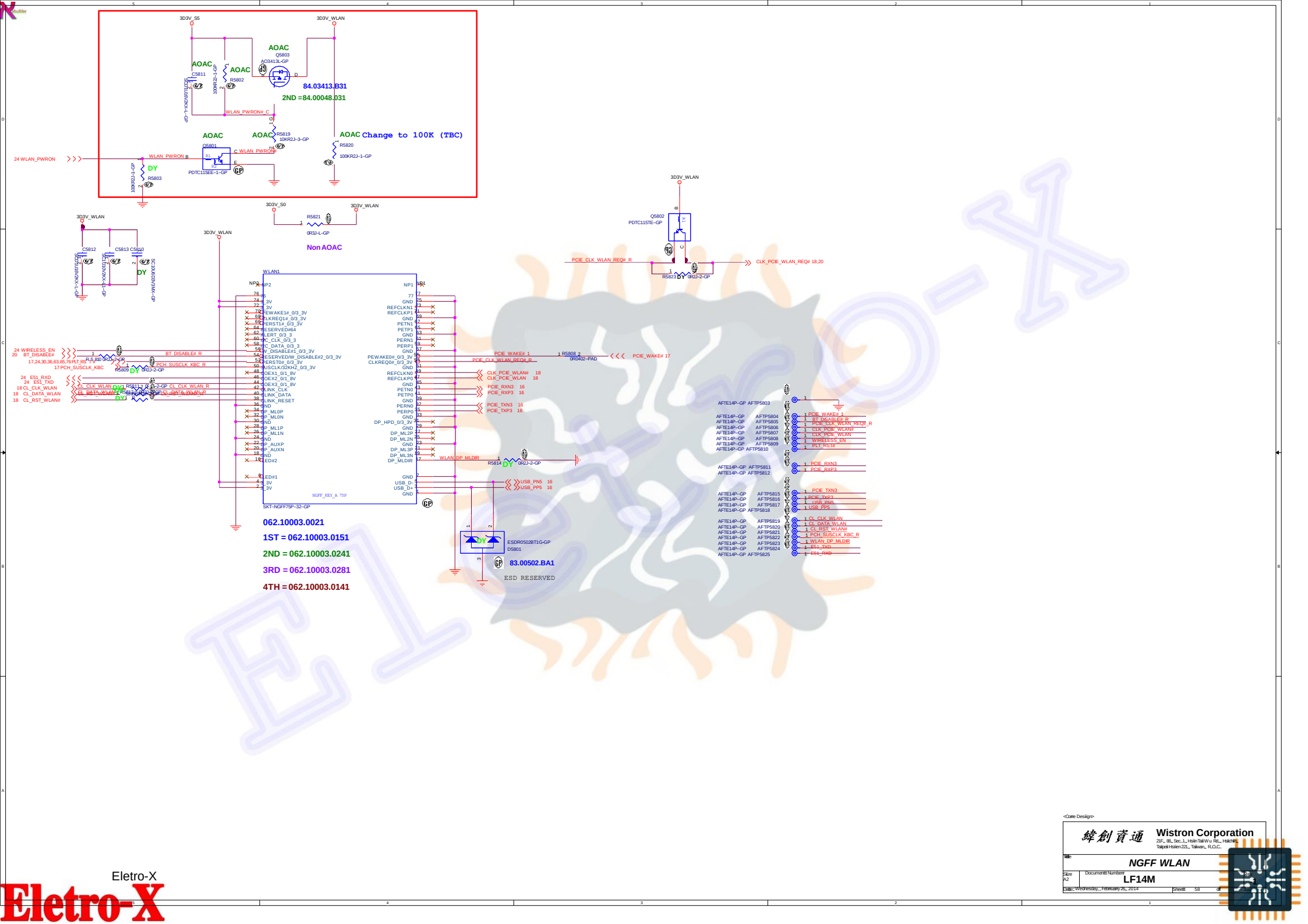
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD / NGFF_SSD

Size: Custom | Document Number: LF14M | Rev: 1.01

Date: Wednesday, February 26, 2014 | Sheet 56 of 102

Eletro-X



<Core Design>

Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN

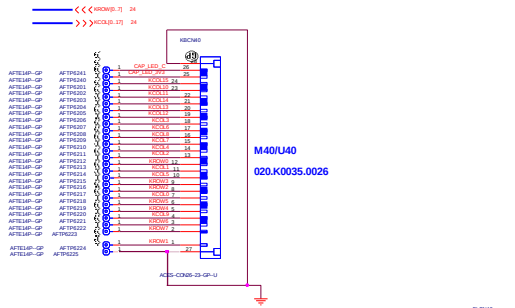
Size: A2 | Document Number: LF14M | Rev:

Date: Wednesday, February 26, 2014 | Sheet 58 of

Eletro-X

SSID = KBC

Internal KeyBoard Connector

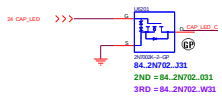


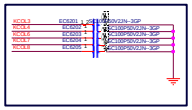
Check Date:2013/9/15

14" (Ref. Chicony G40 BL KB CCY 2D 0905 X7)

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2	25	26
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	S1	S2	S3	S4	S5	S6	S7	S8	VDD	Caps

CAP LED:all series





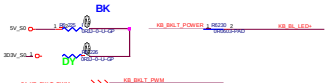
For EMCRecommend

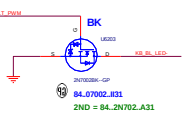
AFTP6201-AFTP6225
CLOSE keyboard connector

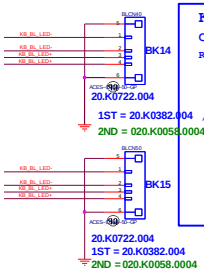
Keyboard Backlight CN

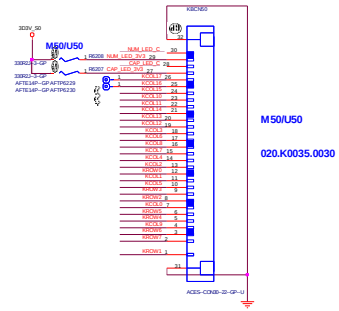
Check Date:2013/9/15

Ref. Chicony G40 BL KB CCY 2D 0905 X7









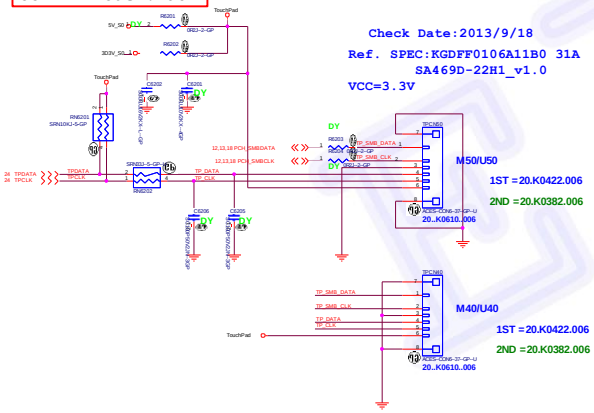
Check Date:2013/9/15

15" (Ref. Chicony G50 NBL KB CCY 2D 0904 X8)

Membrane PIN Out Top View

Pin #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
AS-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	S1	S2	S3	S4	S5	S6	S7	S8

SSID = Touch.Pad

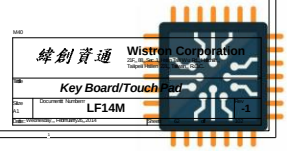


Check Date:2013/9/18

Ref. SPEC:KGDFF0106A11B0 31A
SA469D-22H1_v1.0
VCC=3.3V

1ST =20.K0422.006
2ND =20.K0382.006

1ST =20.K0422.006
2ND =20.K0382.006



USB 2.0 port2/4 Power SW

U6301 place near to IOCN1 add 47uF input/output

at least 80 mil

High Enable

74..02064..B79

IO BD
M40/U40/M50/U50

2014/2/6
USB_PP0/PN0改改改USB2.0 Port 1
NET雅維維維

Reserved for USB2.0 Card Reader (DY)

USB3.0 CARD READER

USB2.0 PORT4

USB2.0 PORT2

Change P/N
2013/11/1

84..00024..01K

PCIECARD

USB2CARD

2014/2/12 Add for GL3213 Card Reader
If PCIE Card Reader is stuff,then dummy R6317
U40/U50 only

Change IOCN1 P/N
Need Check Pin Define with Small BD
2013/10/30

主板PIN定義維持
只移移移
移移CN腳只改腳腳PIN
其其NC

20.K0678.044

1ST = 20.K0678.044
2ND = 20.K0809.044

Volume BD
M50/U50

+ PH 3d3v_s0

2014/2/7
SPEC維要因直變變變變

20.K0397.004

DOCKING BD
M50 only

Modified 10/5

AC CAP IN SMALL BD

20.K0848.030

2ND = 20.K0809.030

Figure 14-2. USB 3.0 Docking Topology Overview

Figure 14-3. Detailed USB 3.0 Docking Topology from Broadwell Processor To Re-driver

BTN BD
U50 only

Check with small BD 9/25

20.K0529.008

2ND = 20.K0481.008

Novo Button
M40/U40

M40/U40 Novo Button

062..40001..0141

Eletro-X

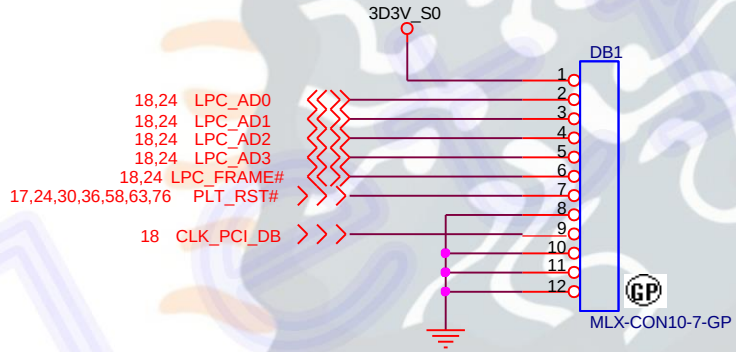
Wistron Corporation

IO Board Connector

Document Number: LF14M

Rev: -1

Debug Connector



20.D0183.110

DB Change to 20.F0714.010

M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug connector***

Size	Document Number	Rev
A4	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 65 of 102

Free Fall Sensor

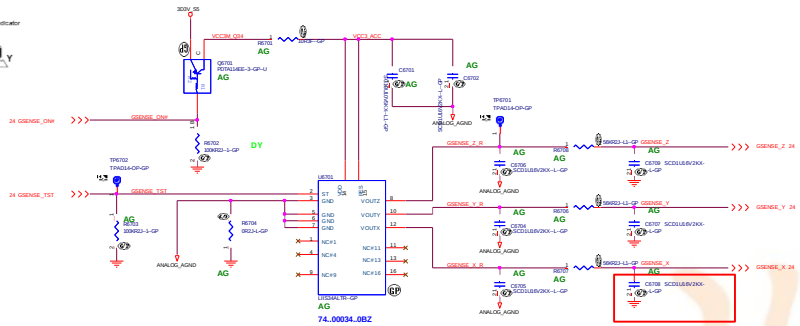
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Need Stuff

Analog G-Sensor

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"



74.00034.0BZ
1ST = 74..00034..0BZ
2ND = 74..KXTC8..0BZ
STMicro LIS34AL: 74.00034.0BZ
2nd = 74.KXTC8.0BZ

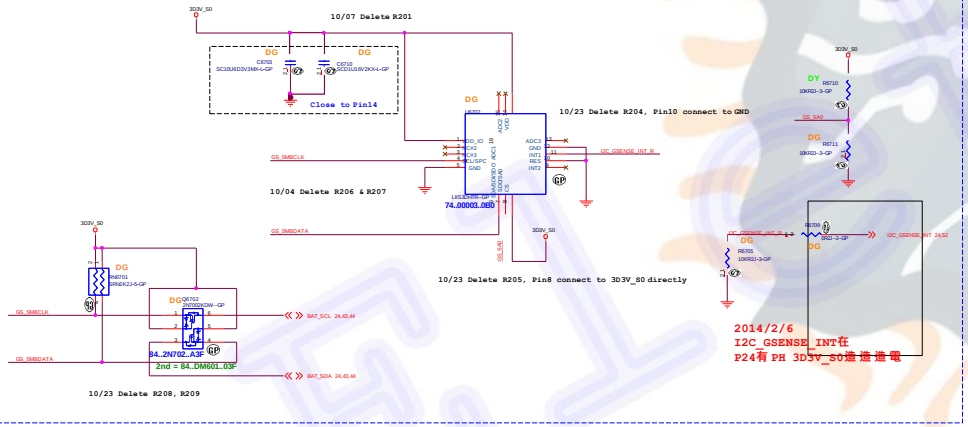
Layout Comment :
(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

If Analog Gsensor Not USE Please Change C6708 to 10K ohm

SC Digital_G-sensor

The Slave ADdress (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



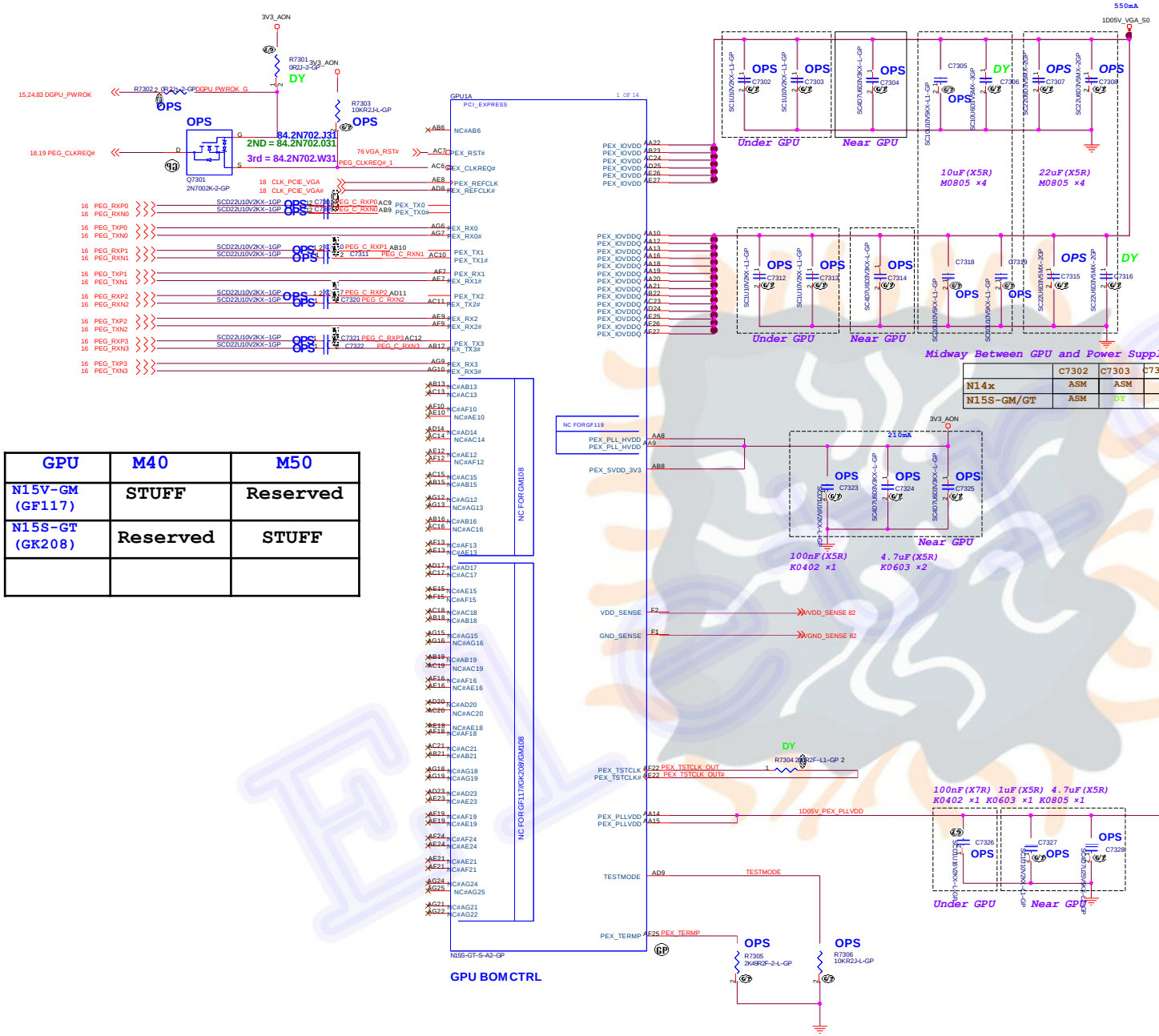
Eletro-X

Wistron Corporation

G Sensor

Document Number: LF14M

-1



GPU	M40	M50
N15V-GM (GF117)	STUFF	Reserved
N15S-GT (GK208)	Reserved	STUFF

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
1uF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N15S-GM/GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY

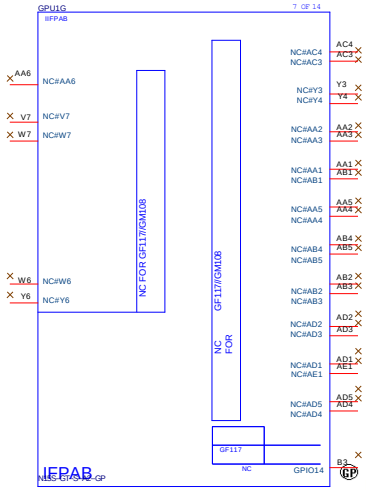
M40

Wistron Corporation

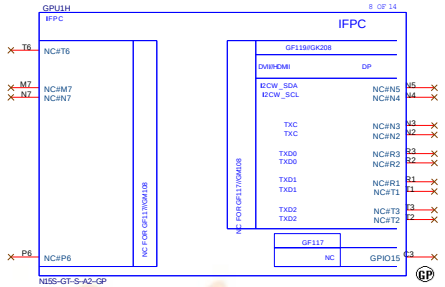
GPU(PEG)

LF14M

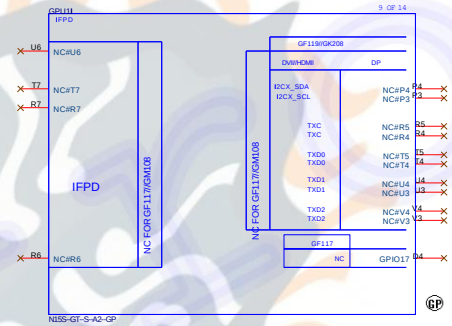
Wednesday, February 26, 2014



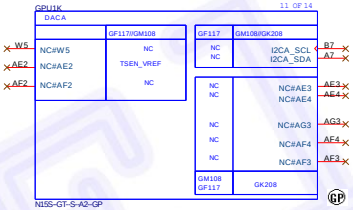
GPU BOM CTRL



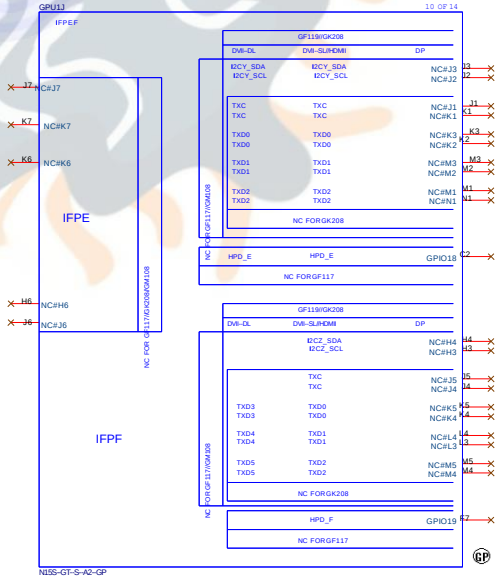
GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL

M40

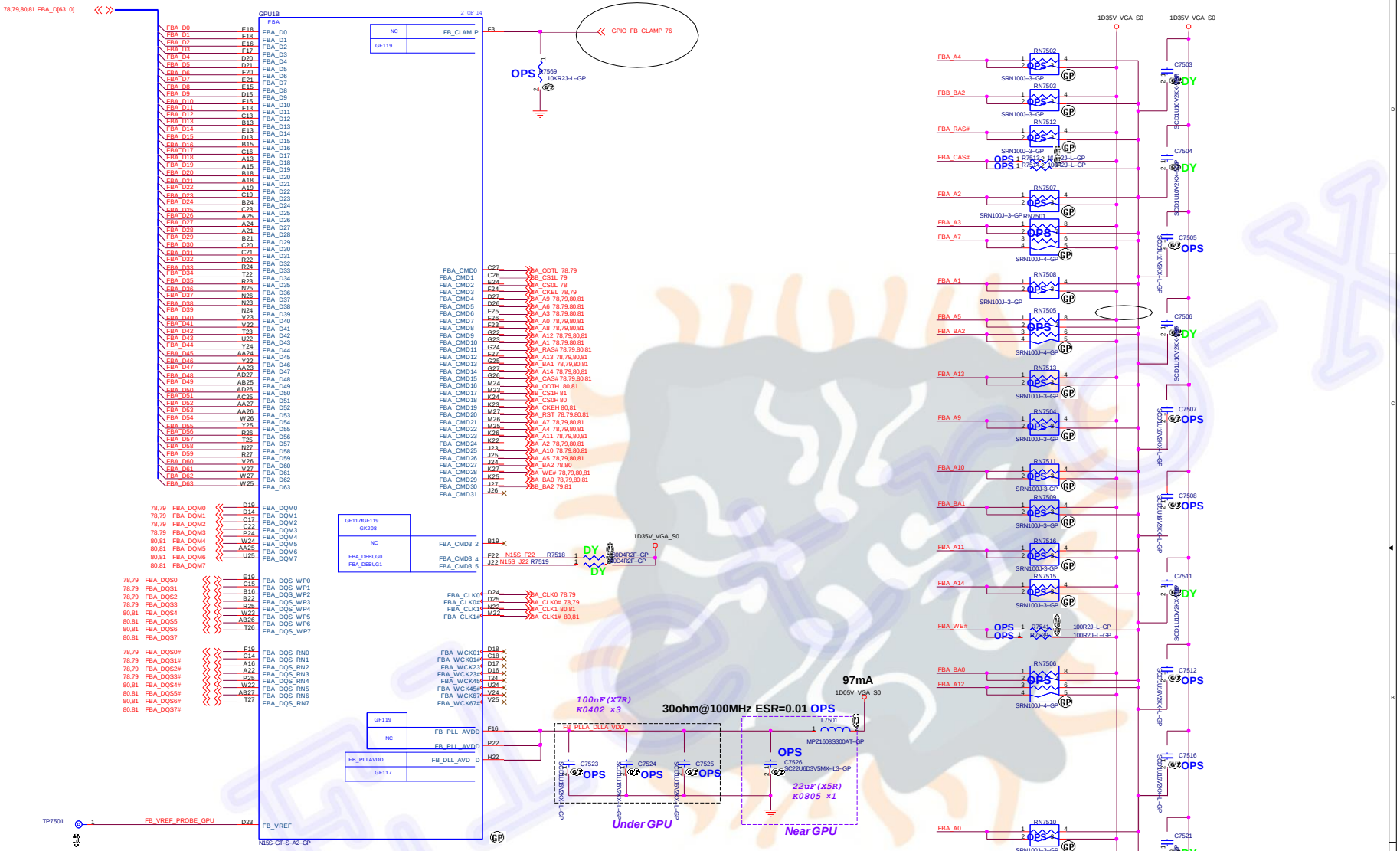
Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (DIGITALOUT)

Size: A2 | Document Number: LF14M | Rev: 1A

Date: Wednesday, February 26, 2014 | Sheet 74 of 74

check "EC_FB_CLAMP" is original name



M40

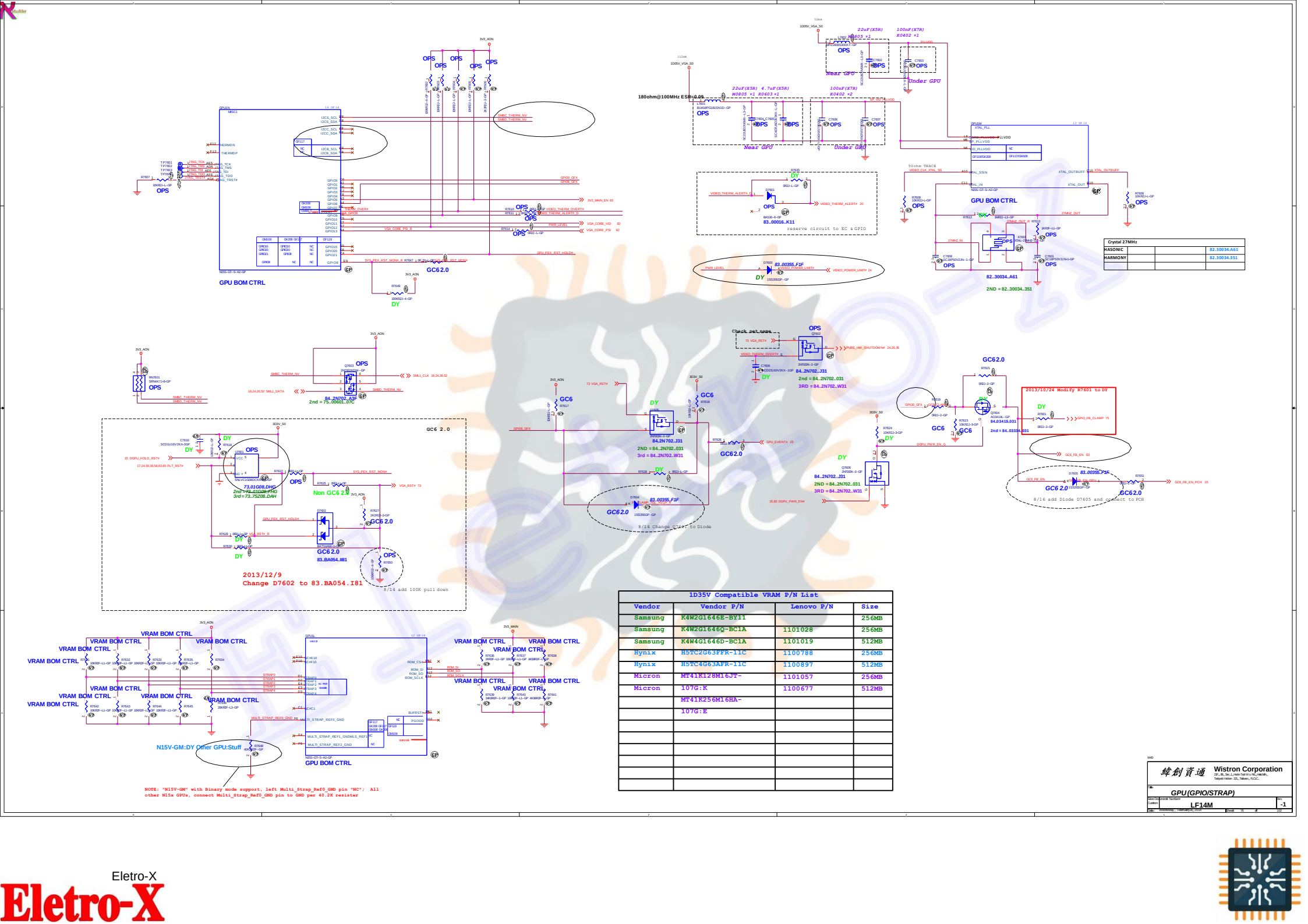
緯創資通 Wistron Corporation

21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

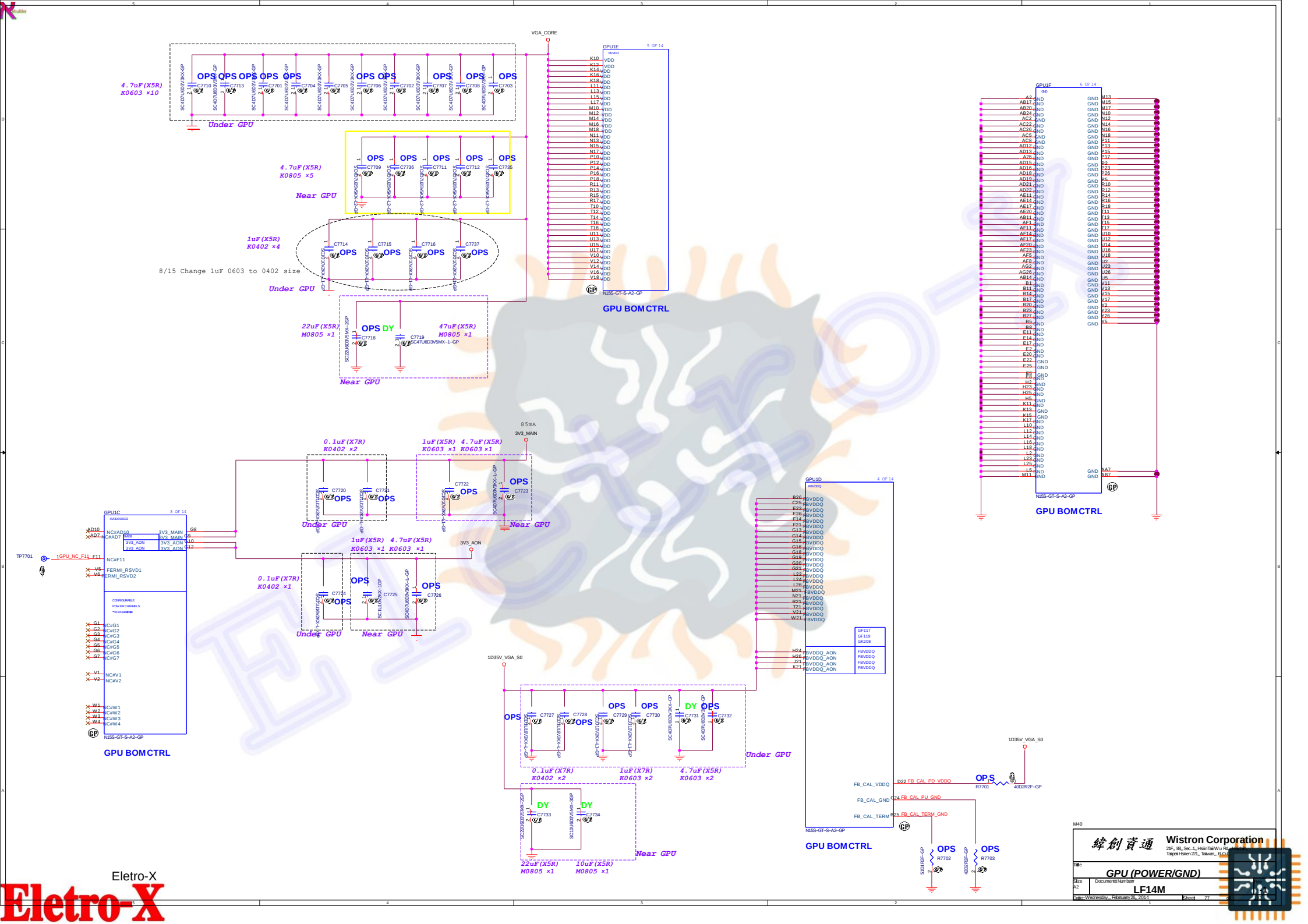
Size: Custom | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 75 of 102

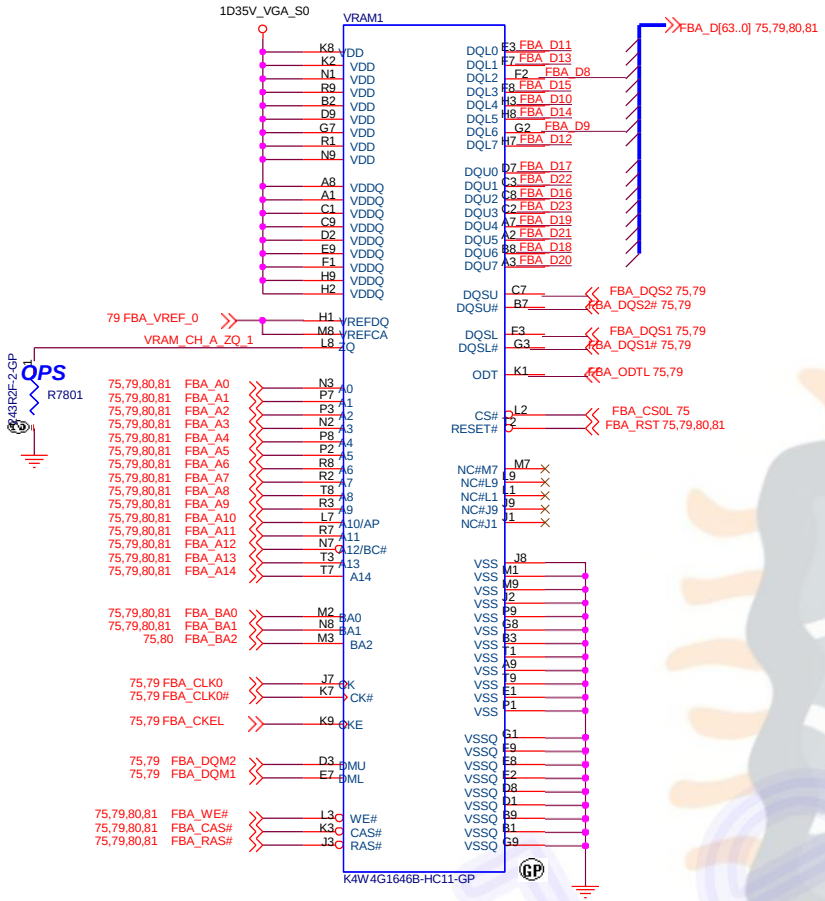


1D35V Compatible VRAM P/N List

Vendor	Vendor P/N	Lenovo P/N	Size
Samsung	K4W2G1646E-BY11		256MB
Samsung	K4W2G1646Q-BC1A	1101028	256MB
Samsung	K4W4G1646D-BC1A	1101019	512MB
Hynix	H5TC2G63FFR-11C	1100788	256MB
Hynix	H5TC4G63AFR-11C	1100897	512MB
Micron	MT41K128M16JT-	1101057	256MB
Micron	107G:K	1100677	512MB
	MT41K256M16HA-		
	107G:E		

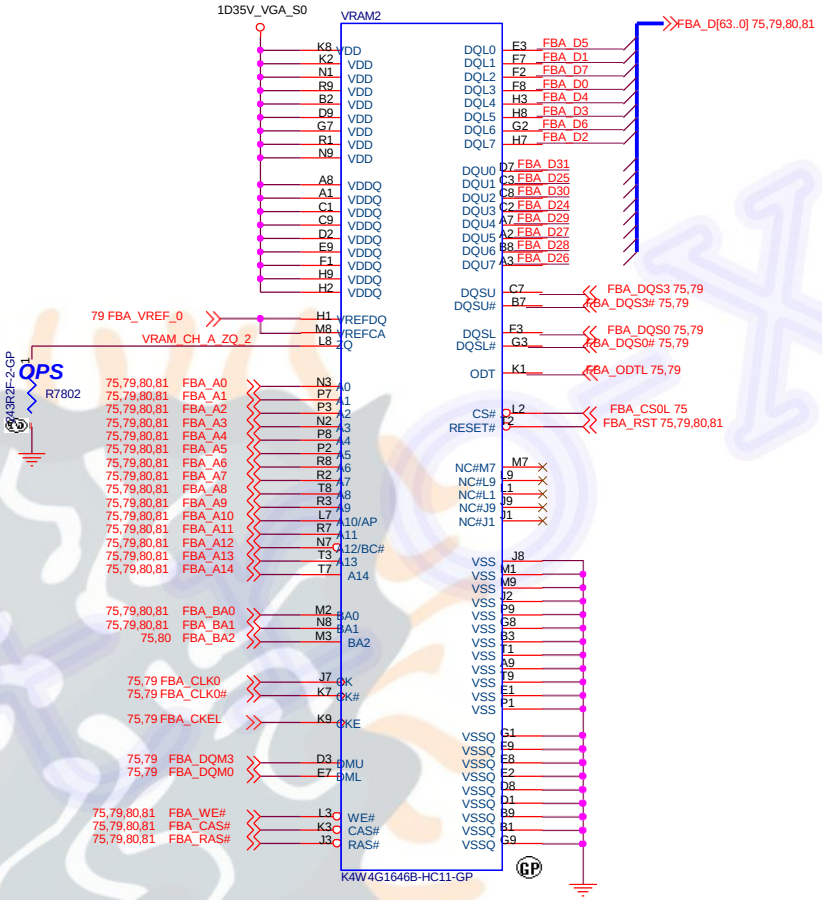

VGA_CORE
GPU1E
5 OF 14
N15S-GT-S-A2-GP
GPU BOM CTRL
4.7uF(X5R) K0603 ×10
Under GPU
4.7uF(X5R) K0805 ×5
Near GPU
1uF(X5R) K0402 ×4
8/15 Change 1uF 0603 to 0402 size
22uF(X5R) M0805 ×1
47uF(X5R) M0805 ×1
GPU1F
6 OF 14
GPU1C
3 OF 14
GPU1D
4 OF 14
0.1uF(X7R) K0402 ×2
1uF(X5R) K0603 ×1
4.7uF(X5R) K0603 ×1
3V3_MAIN
3V3_AON
1D35V_VGA_S0
TP7701
1GPU_NC_F11
FB_CAL_VDDQ
FB_CAL_GND
FB_CAL_TERM
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R7701
R7702
R7703
Wistron Corporation
GPU (POWER/GND)
LF14M

Data Bits 31:0 RANK 0



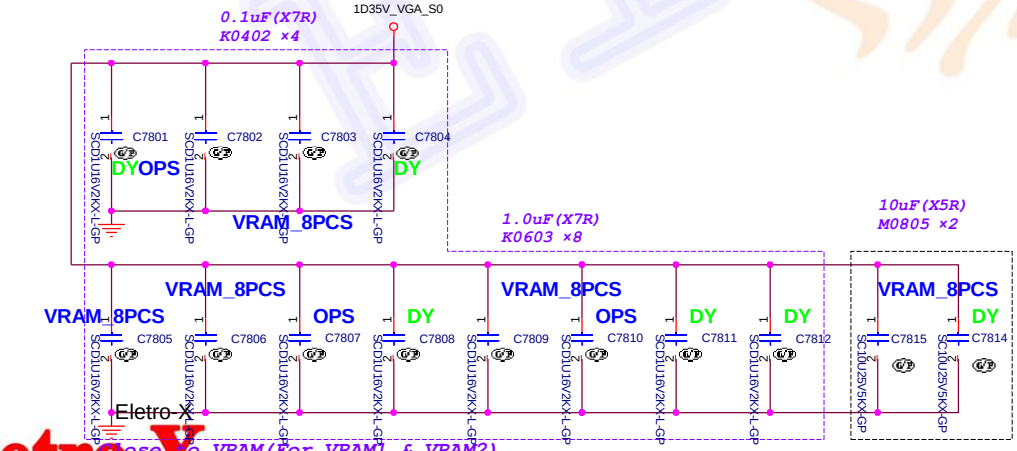
72.41646.00U

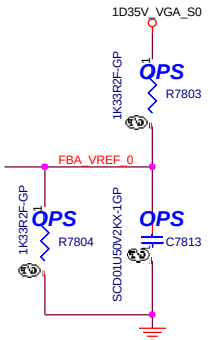
VRAM BOM CTRL



72.41646.00U

VRAM BOM CTRL





M40

緯創資通 Wistron Corporation

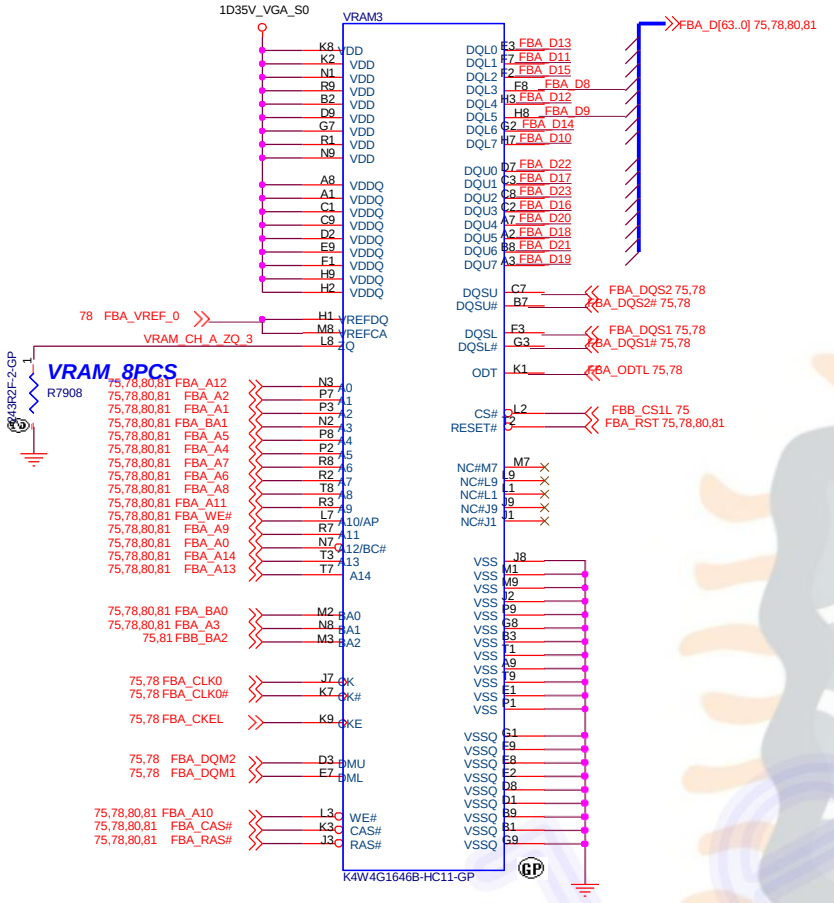
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

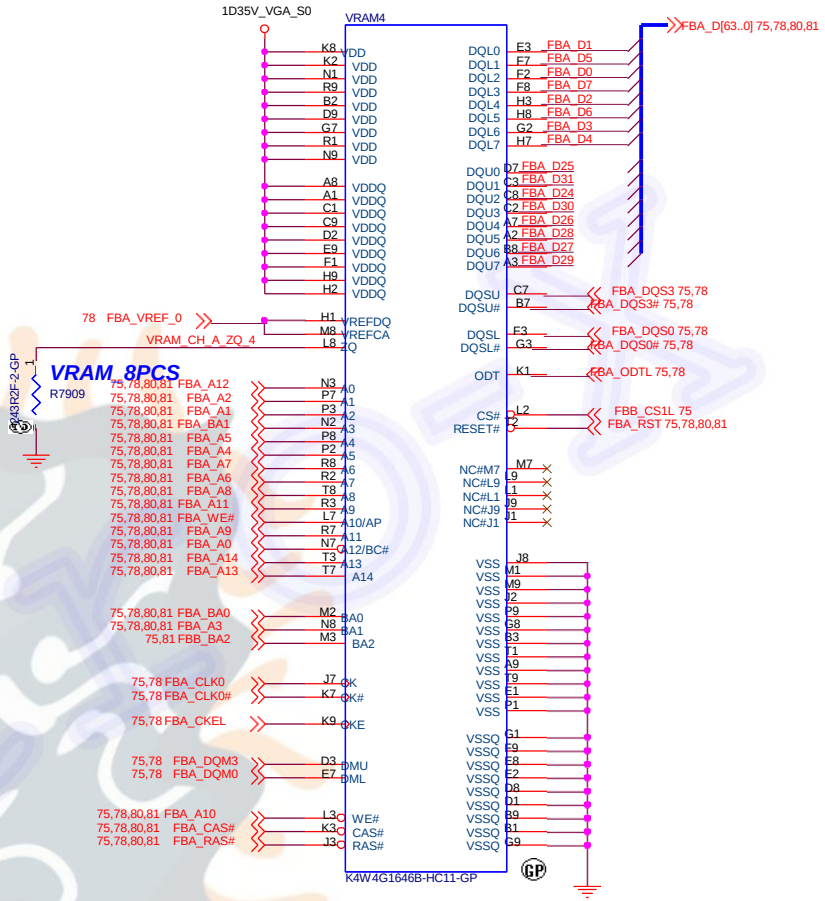
Title: GPU-VRAM1,2 (1/4)

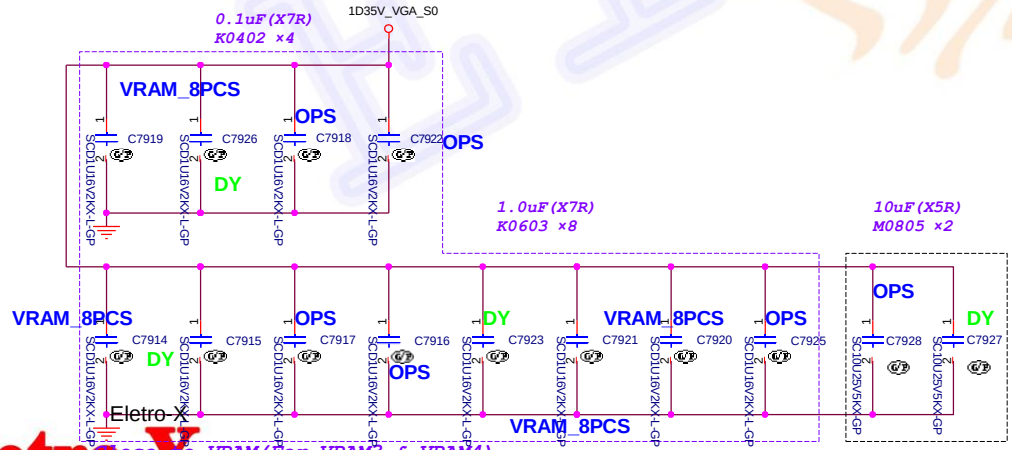
Size: A3 | Document Number: LF14M | Rev: 1A

Date: Wednesday, February 26, 2014 | Sheet 78 of 100

Data Bits 31:0 RANK 1



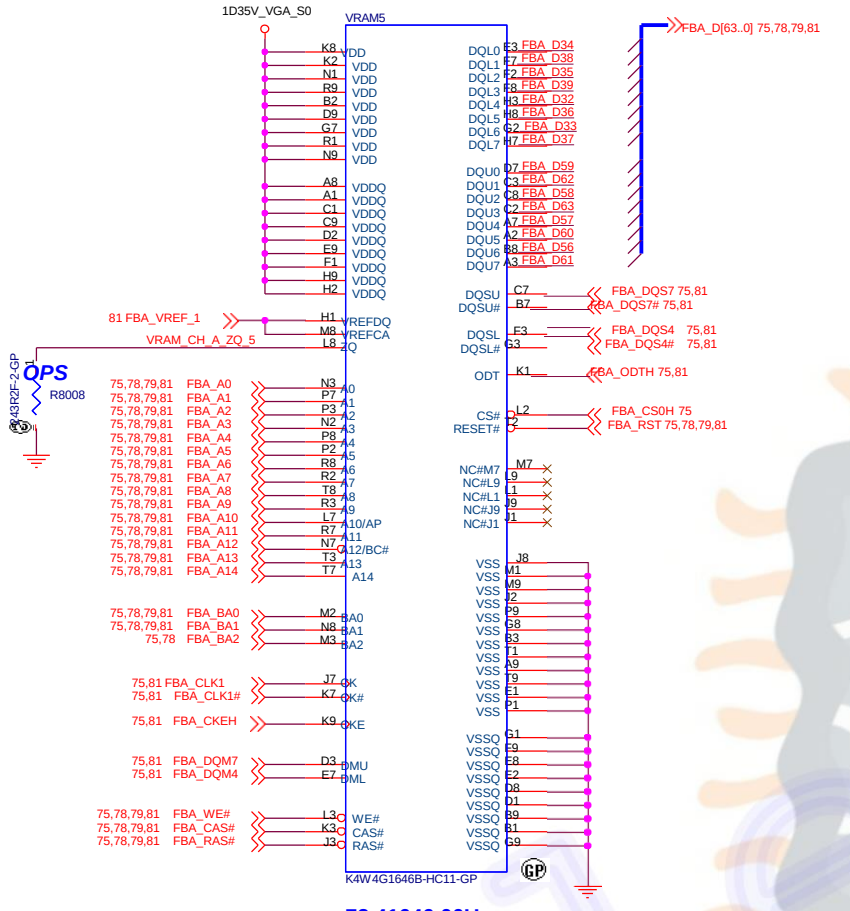


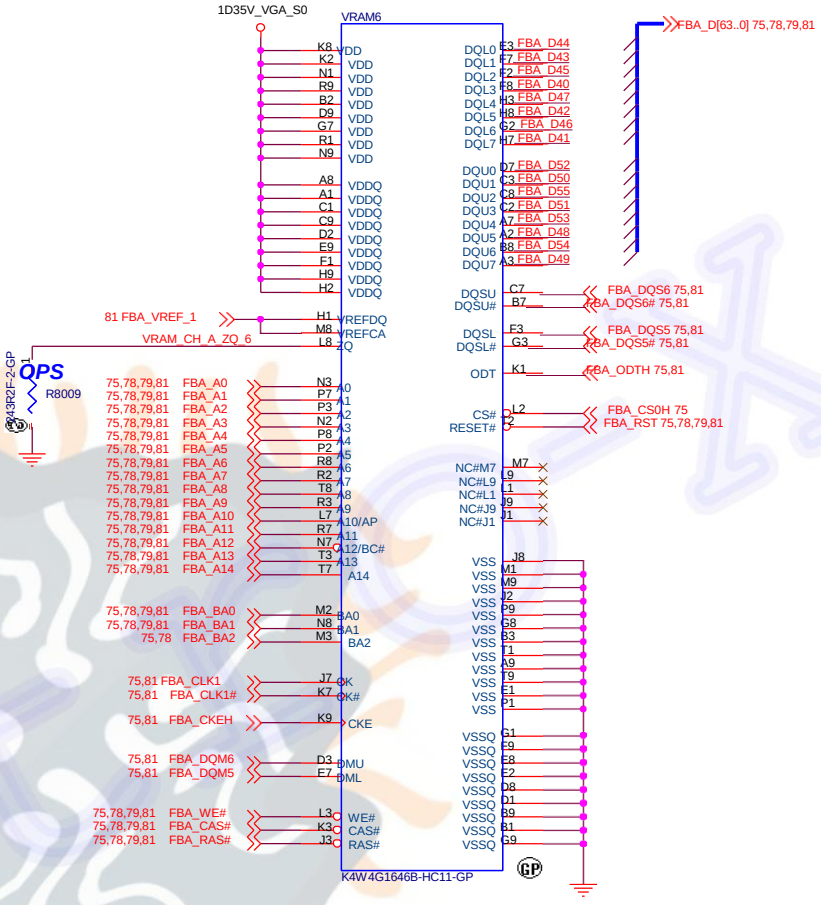


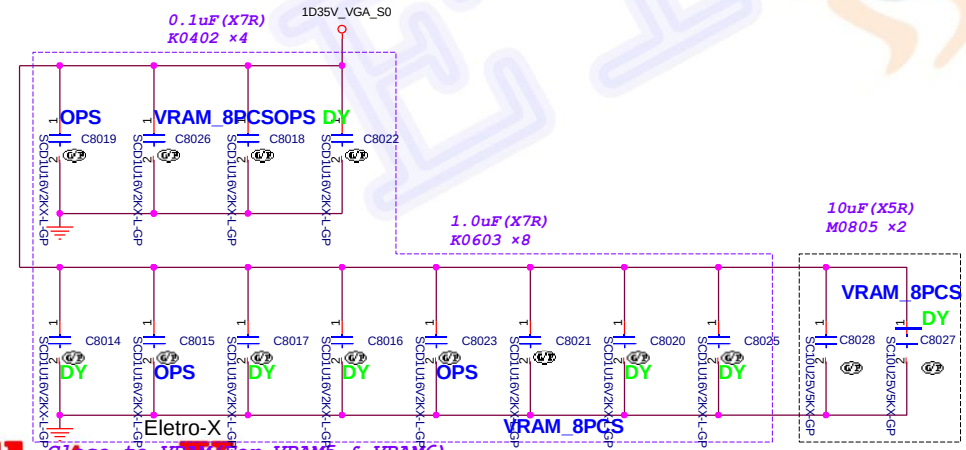
M40

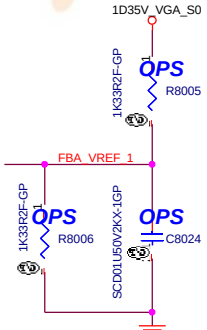
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU-VRAM3,4 (2/4)
Size A3	Document Number LF14M
Date: Wednesday, February 26, 2014	Sheet 79 of 100

Data Bits 63:32 RANK 0









M40

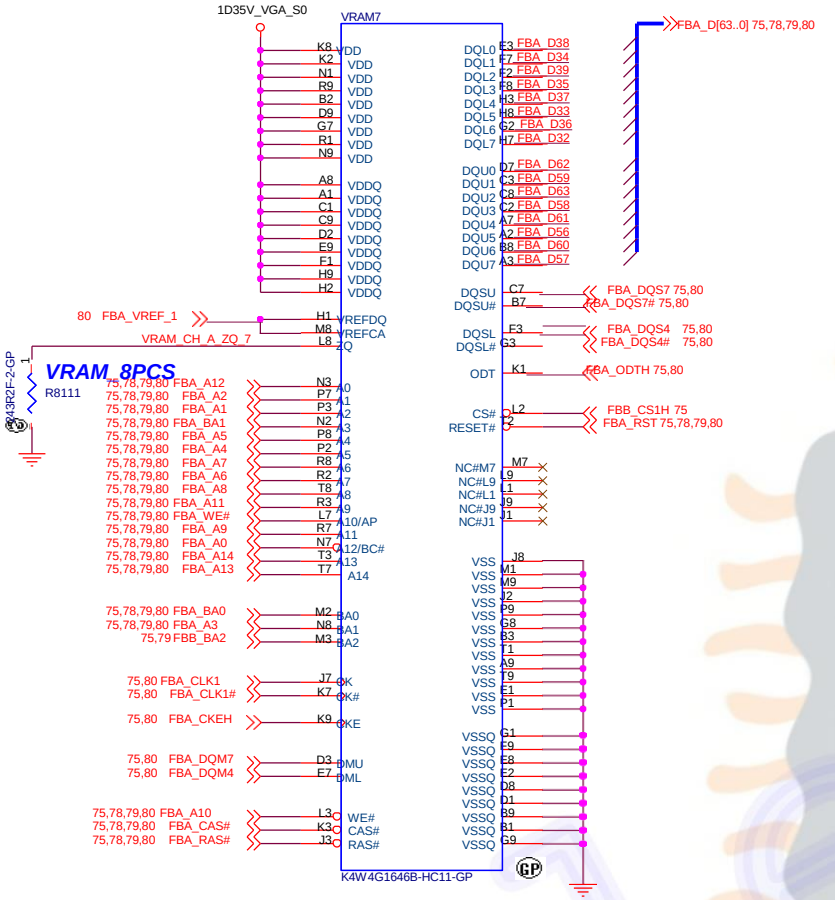
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

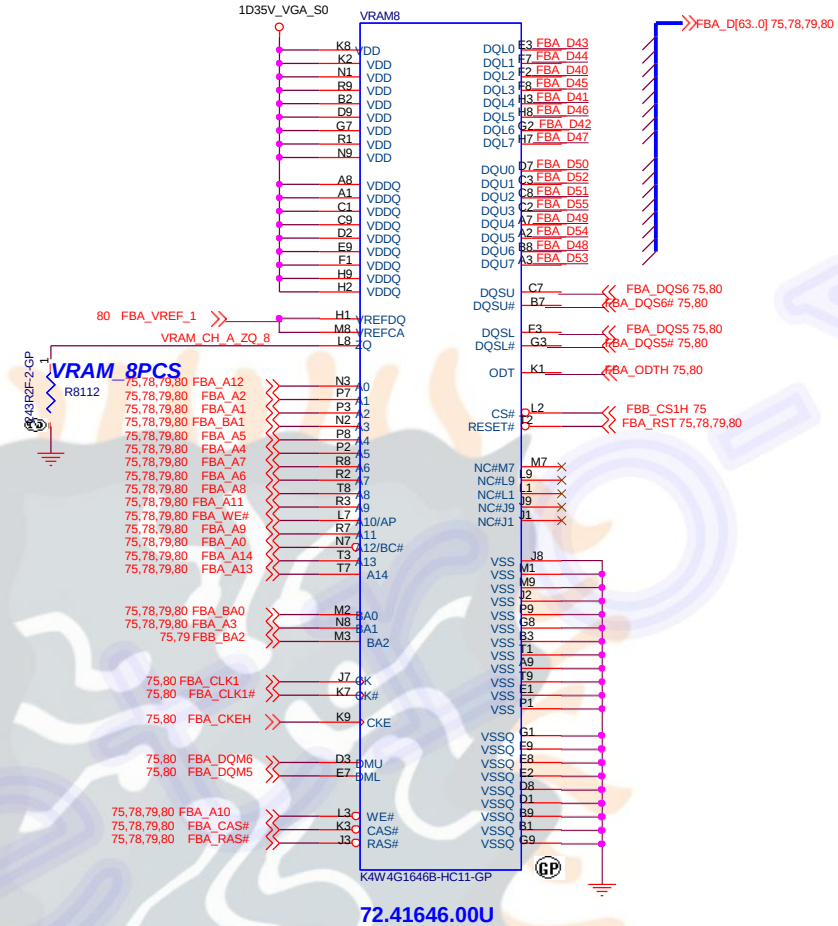
Title: GPU-VRAM5,6 (3/4)

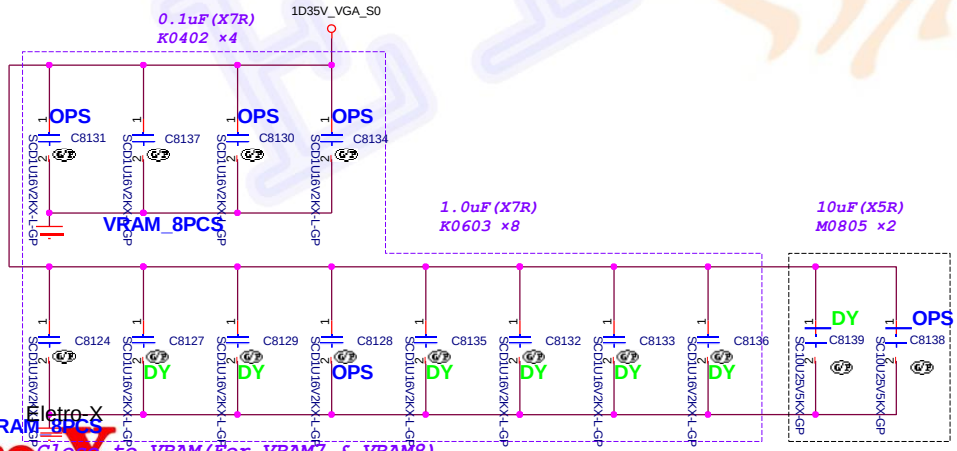
Size	Document Number	Rev
A3	LF14M	1A

Date: Wednesday, February 26, 2014 Sheet 80 of 100

Data Bits 63:32 RANK 1







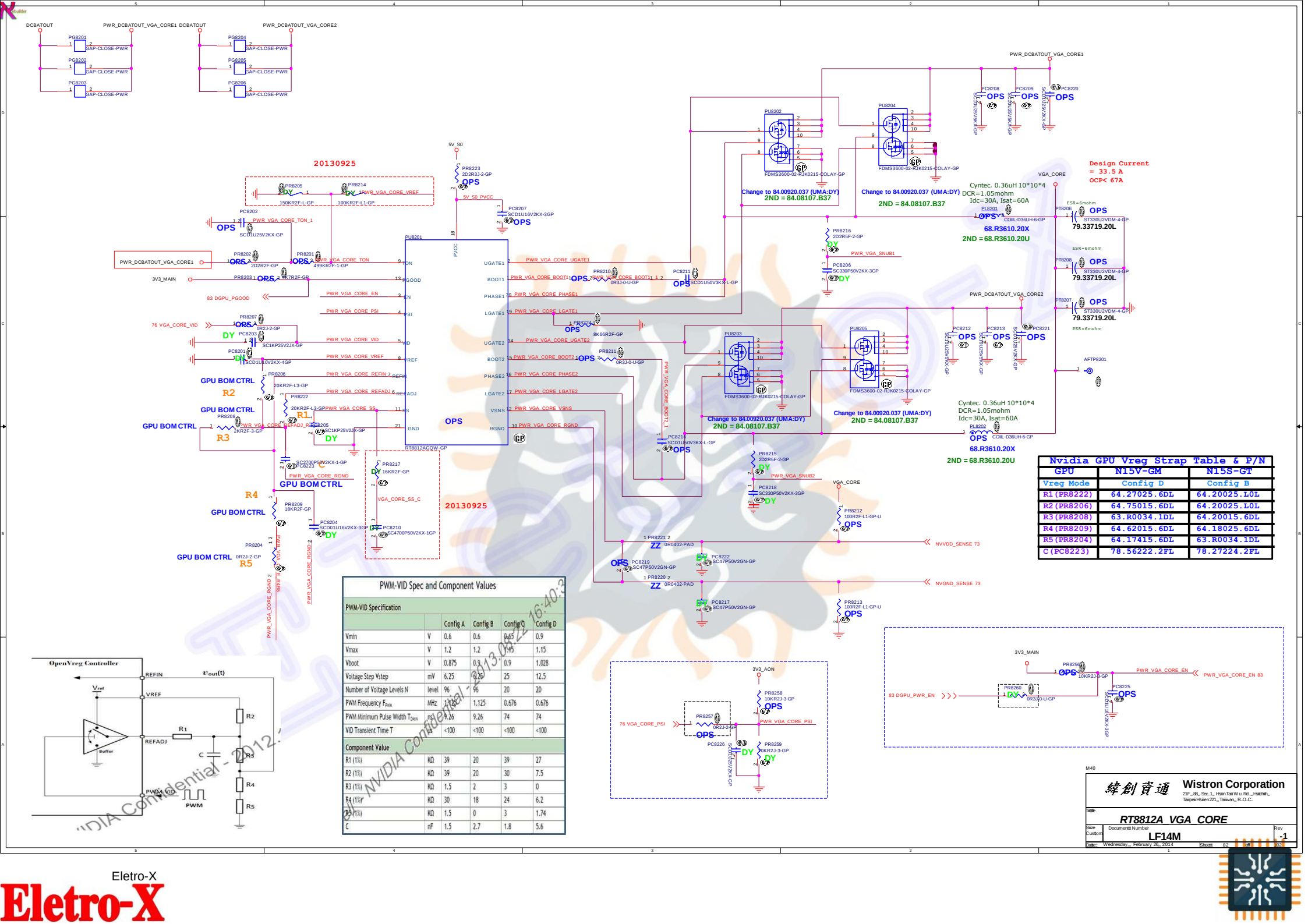
M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: LF14M | Rev: 1.0

Date: Wednesday, February 26, 2014 | Sheet 81 of 100



Nvidia GPU Vreg Strap Table & P/N

GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222)	64.27025.6DL	64.20025.L0L
R2(PR8206)	64.75015.6DL	64.20025.L0L
R3(PR8208)	63.R0034.1DL	64.20015.6DL
R4(PR8209)	64.62015.6DL	64.18025.6DL
R5(PR8204)	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL

PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T		<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

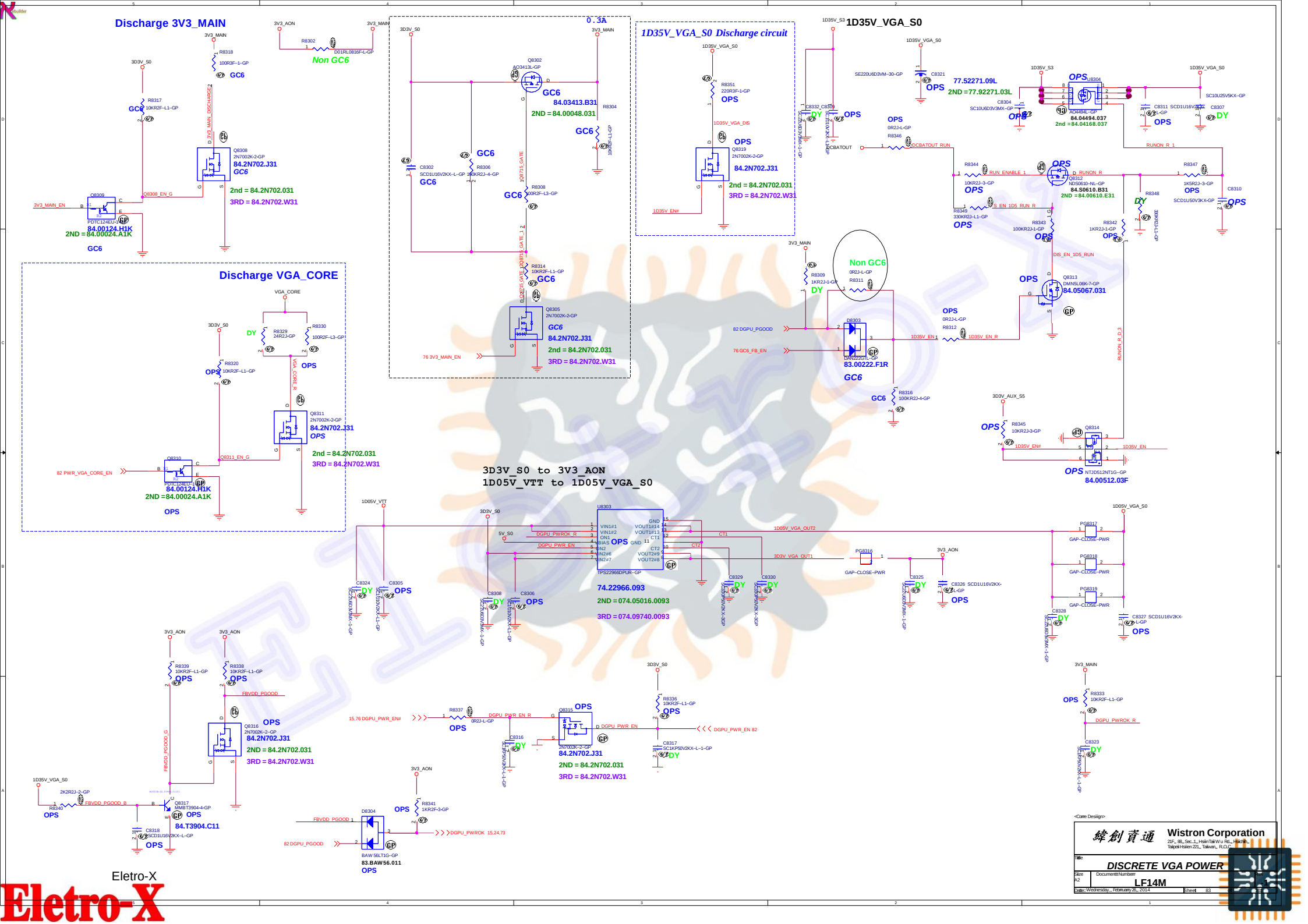
M40

Wistron Corporation
21F., 88, Sec. 1, HsinTaiWu Rd., HsichihTown, TaipeiHsien 221, Taiwan, R.O.C.

RT8812A_VGA_CORE

Size: Custom | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet: 82 of 102


Discharge 3V3_MAIN
Non GC6
0.3A
1D35V_VGA_S0 Discharge circuit
1D35V_VGA_S0
Discharge VGA_CORE
3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0
74.22966.093
2ND = 074.05016.0093
3RD = 074.09740.0093
83.00222.F1R
84.00512.03F
84.00124.H1K
2ND = 84.00024.A1K
84.T3904.C11
83.BAW56.011
Wistron Corporation
DISCRETE VGA POWER
LF14M

Eletro-X

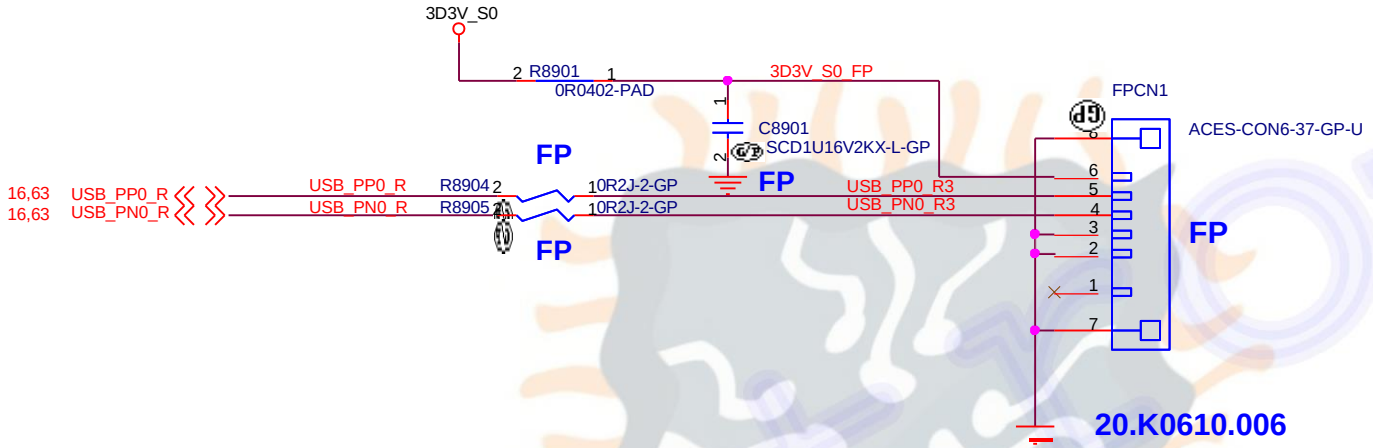
Check Date:2013/9/18

2014/2/6

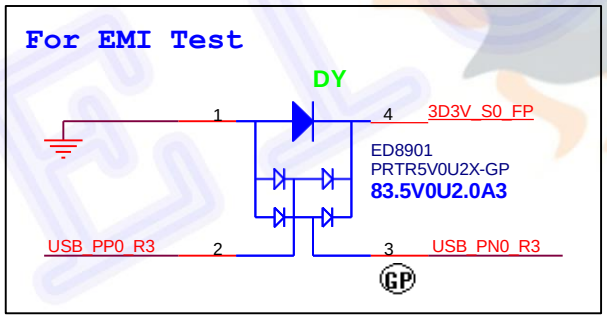
USB_PP0/PN0改改改USB2.0 Port 1

NET維維維維

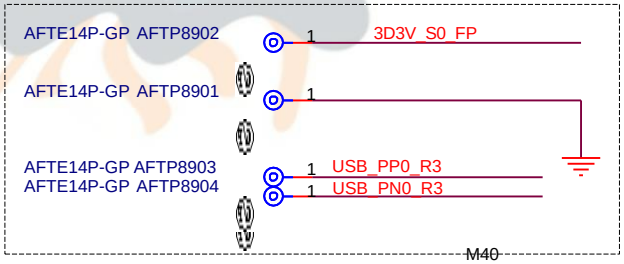
FingerPrint BD
M40/M50



M40,M50 have Finger Print, USB2.0 Port isn't enough,
USB2.0 PN1/PP1 combine CR2.0 with FP



Near FPCN1

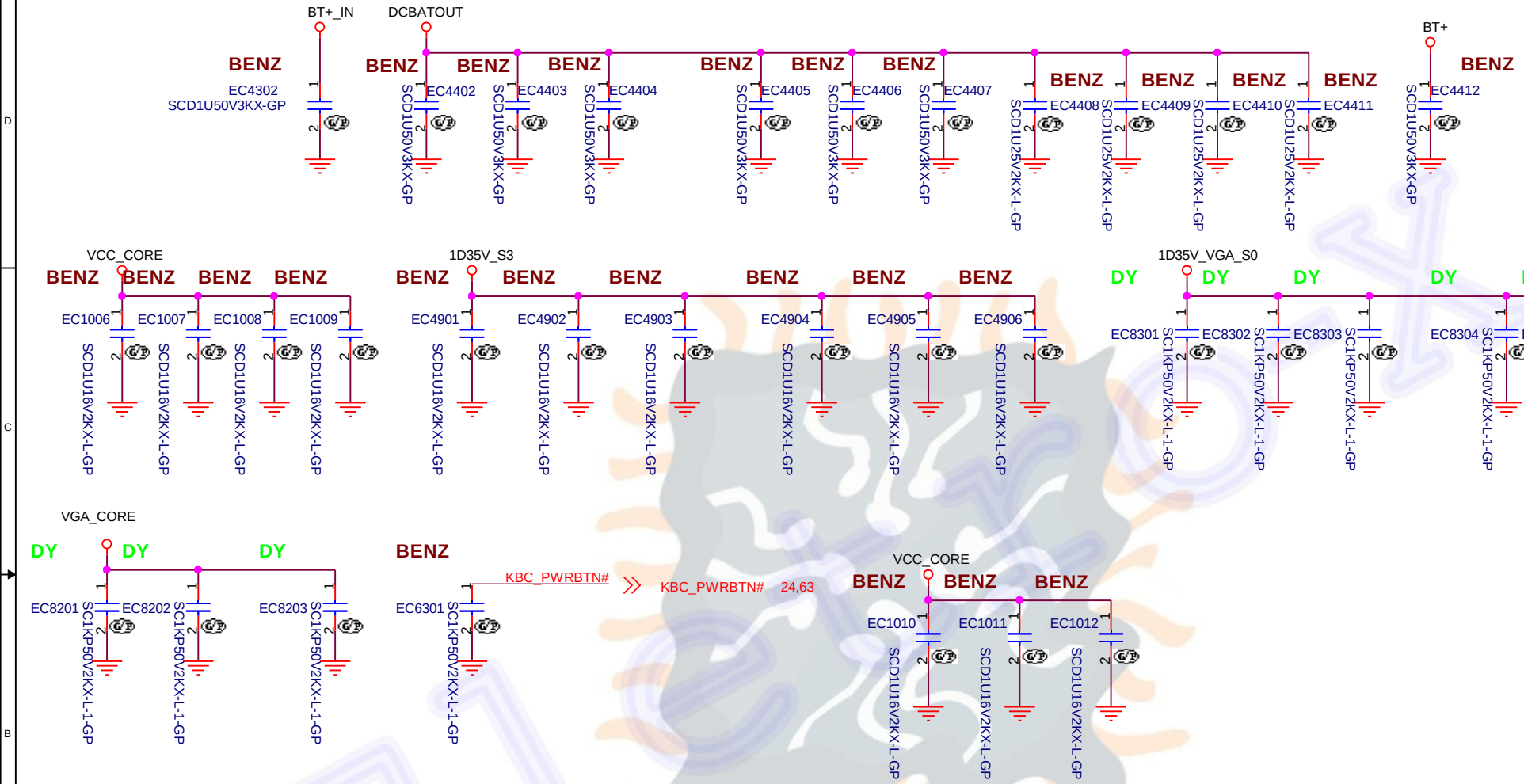


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Print

Size: A4 | Document Number: LF14M | Rev:

Date: Wednesday, February 26, 2014 | Sheet 89 of 103



M40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Benz Only***

Size	Document Number	Rev
A4	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 85 of 102

Eletro-X

CPU Std-Off

HS2 STF236R128H22-GP
434.00X01.0001
2ND = 434.00X01.1001

HS3 STF236R128H22-GP
434.00X01.0001
2ND = 434.00X01.1001

HS4 STF236R128H22-GP
434.00X01.0001
2ND = 434.00X01.1001

VGA Std-Off

HS1 STF236R128H22-GP
OPS
434.00X01.0001
2ND = 434.00X01.1001

WLAN Std-Off

HS6 STF236R128H88-GP
34.4LY03.001
2ND = 34.4LY03.101

Structure boss

H1 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H4 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H5 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H6 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H7 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H8 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H9 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H10 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H12 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H13 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H14 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H15 HOLE237R95-GP ZZ.00PAD.921 GP ZZ
H16 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H17 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
H3 HT65B8X8R29-GP ZZ.00PAD.3E1 ZZ
H19 HOLE315X315R99-S1-GP ZZ.00PAD.1M1 ZZ
AH18 HOLE237R95-GP ZZ.00PAD.921 GP ZZ

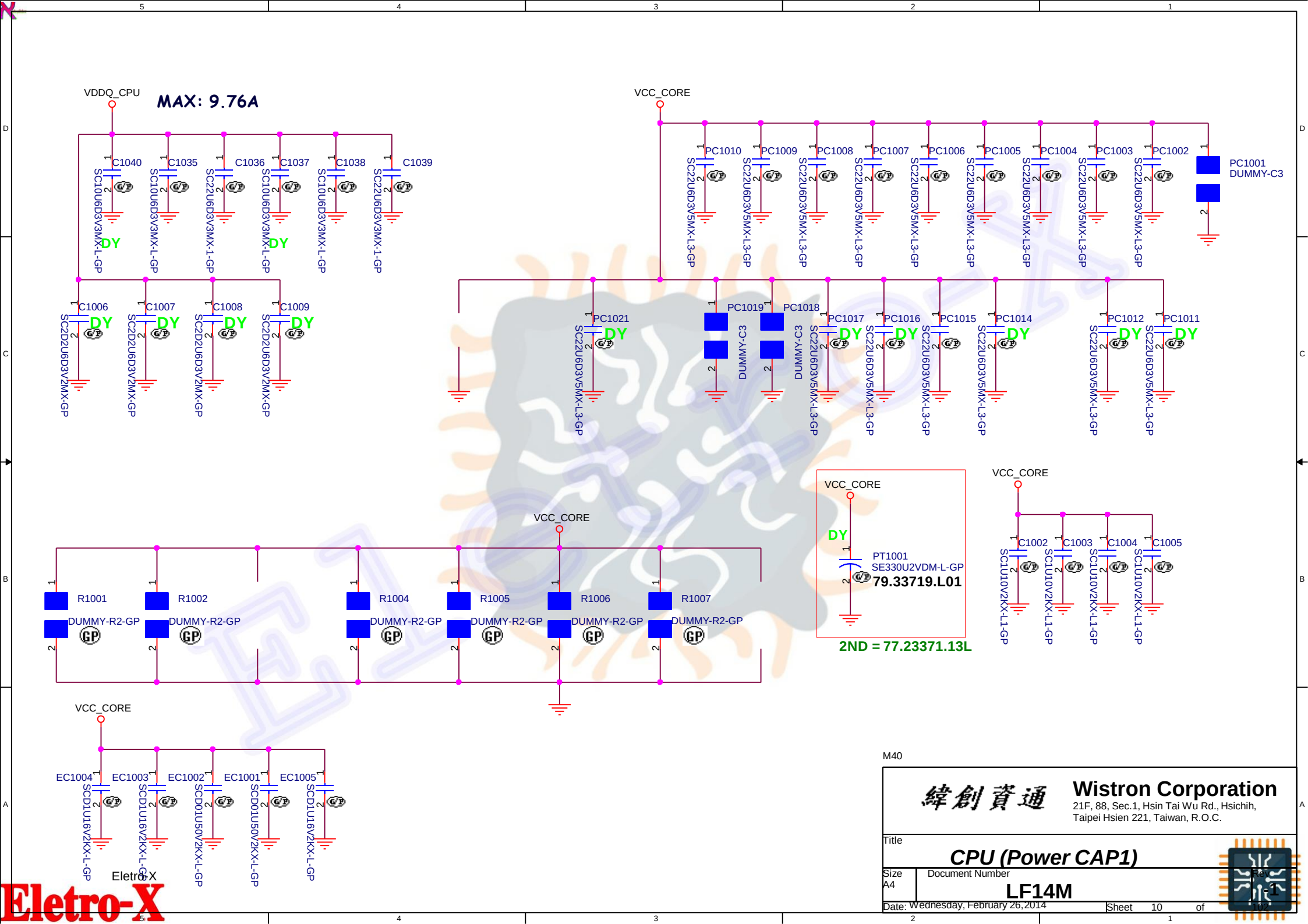
EMI

SP1 SPRING-62-GP 34.39S07.003 EMI BOM CTRL
SP2 SPRING-62-GP 34.39S07.003 EMI BOM CTRL
SP4 SPRING-13-GP-U 34.43E24.001 EMI BOM CTRL
SP5 SPRING-62-GP 34.39S07.003 EMI BOM CTRL
SP6 SPRING-98-GP 34.34S02.002 EMI BOM CTRL

M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, TaipeiHsien221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LF14M | Rev: 1.1
Date: Wednesday, February 26, 2014 | Sheet 86 of 101



M40

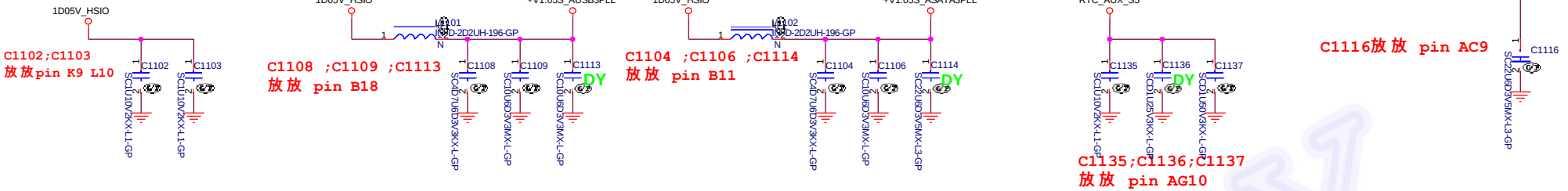
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)

Size: A4 | Document Number: LF14M | Rev: -1

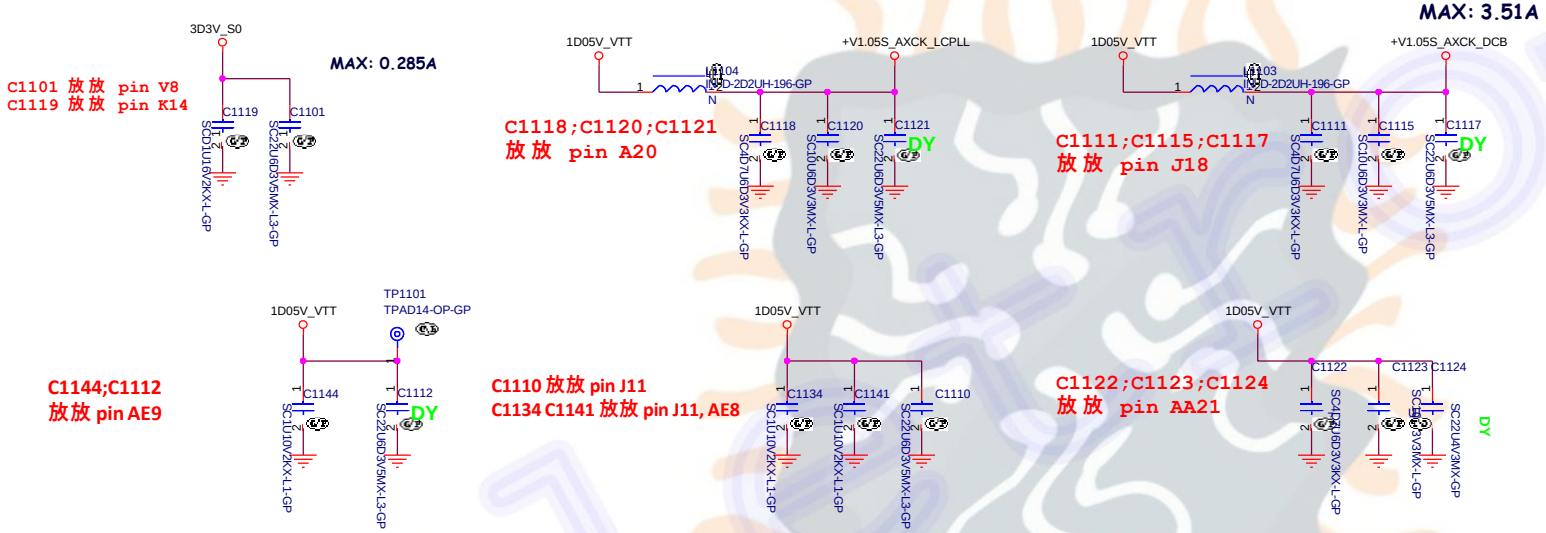
Date: Wednesday, February 26, 2014 | Sheet 10 of 102

MAX: 1.92A



MAX: 0.285A

MAX: 3.51A



M40

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (Power CAP2)		
Size: Custom	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 11 of 102	

BOM Option Table

Function	Acronym	BOM Models (V=Stuff) N46	N50	U40	U50
Woofer AMP	WO			V	V
USB Charger	UC	V with UC_ST	V with UC_ST		
Non USB Charger	NUC			V	V
TPM	TPM	V	V		
PTC	PTC	V	V		
ODD	ODD		V with ZPODD		V with Non ZPODD
Thermal VD	TV				
DOCKING	DK		V		
Fingerprint	FP	V	V		
Backlight Keyboard	BK	V with BK14	V with BK15		
Analog Geasor	AG	V	V	V	V
For Debug CN	DB	V (in SA)	V (in SA)	V (in SA)	V (in SA)
HighSpeed I/O	HSIO				
Non HighSpeed I/O	Non HSIO	V	V	V	V
Platform type					
Haswell	BOM Ctrl_Model R2441	64.14335.6DL	64.17435.6DL	64.76825.6DL	64.10035.6DL
Broadwell		64.47025.6DL	64.64925.6DL	64.10025.6DL	64.20025.L0L
PCB Ver. (in SA)	BOM Ctrl_VER R2437	64.10025.6DL	64.10025.6DL	64.10025.6DL	64.10025.6DL
CPU	CPU BOM CTRL	See Config	See Config	See Config	See Config
LAN	LAN BOM CTRL LAN_SURGE	See Config	See Config	See Config	See Config
GIGA LAN	GIGA LAN_SURGE GIGA TOUCH	See Config	See Config	See Config	See Config
Touch Panel	(DY:Non Touch)	See Config	See Config	See Config	See Config
Do Not Stuff	DY/ZZ				

GPU BOM CTRL		For Detail see P82
GPU	N15V-GM	N15S-GT
Lenovo P/N	11202477	11202478
OPS (UMA:DY)	V	V
PR8222	64.27025.6DL	64.20025.L0L
PR8206	64.75015.6DL	64.20025.L0L
PR8208	63.R0034.1DL	64.20015.6DL
PR8209	64.62015.6DL	64.18025.6DL
PR8204	64.17415.6DL	63.R0034.1DL
PC8223	78.56222.2FL	78.27224.2FL

NVIDIA GC6 Power Management		
GPU	N15V-GM	N15S-GT
GC6 Support	Not Support GC6 2.0 only	
GC6		V
GC6 2.0		V
Non GC6	V	
Non GC6 2.0	V	

VRAM BOM CTRL (Default Setting:900MHZ)									
Lenovo P/N	1101057	1101018	1100788	1100897	1101028	1101019	1100661	1100677	
IC Vendor	Micron	Micron	Hynix	Hynix	Samsung	Samsung	Micron	Micron	
IC Vendor P/N	MT41K128M16JT-107G:K N15V-GM only	MT41J256M16HA-093G:E N15S-GT only	H5TC2G63FFR-11C N15V-GM/N15S-GT	H5TC4G63AFR-11C N15V-GM/N15S-GT	K4W2G1646Q-BC1A	K4W4G1646D-BC1A N15V-GM/N15S-GT	MT41J128M16JT-093G:K N15S-GT only	MT41K256M16HA-107G:E N15V-GM only	
RAMS0 VRAM1,VRAM2,VRAM5,VRAM6	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB		Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB		
RAMS1 VRAM3,VRAM4,VRAM7,VRAM8		Stuff with Discrete 4GB		Stuff with Discrete 4GB		Stuff with Discrete 4GB			
R7642(Strap0-L)			N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L					
R7631(Strap0-H)	N15V-GM:64.10025.L0L	N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	
R7643(Strap1-L)	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7632(Strap1-H)									
R7644(Strap2-L)	N15V-GM:64.10025.L0L					N15V-GM:64.10025.L0L			
R7633(Strap2-H)			N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L				N15V-GM:64.10025.L0L	
R7645(Strap3-L)	N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L					
R7635(Strap3-H)			N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7646(Strap4-L)	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7634(Strap4-H)									
R7639(ROM_SI-L)	N15V-GM:64.10025.L0L	N15S-GT:64.24925.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L N15S-GT:64.20025.L0L		N15V-GM:64.10025.L0L N15S-GT:64.30025.6DL		N15V-GM:64.10025.L0L	
R7636(ROM_SI-H)			N15S-GT:64.10025.L0L				N15S-GT:64.15025.6DL		
R7640(ROM_SO-L)	N15V-GM:64.10025.L0L	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	
R7637(ROM_SO-H)									
R7641(ROM_SCLK-L)	N15V-GM:64.10025.L0L	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	
R7638(ROM_SCLK-H)									

Eletro-X

蜂创资通 Wistron Corporation

title of content

LF14M

Undefined Sys <-> GPU IO

KBC <-> GPU

GPIO_FB_CLAMP_EC → KBC output

-FB_CLAMP_TGL_REQ ← KBC input

VIDEO_THERM_ALERT# → KBC GPIO (Reserved)

-VIDEO_POWER_LIMIT ← KBC output (Reserved)

PCH <-> GPU

GC6_FB_EN → PCH input

-GPU_EVENT ← PCH output

DGPU_HOLD_RST# ← PCH output

PLT_RST# ← PCH output

Thermal IC <-> GPU

VIDEO_THERM_OVERT# → Thermal IC input(Reserved)

VIDEO_THERM_ALERT# → Thermal IC GPIO(Reserved)

-VIDEO_POWER_LIMIT ← Thermal IC output(Reserved)

M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Switchable GFX LCD(1/2)***

Size	Document Number	Rev
A4	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 84 of 102

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRST#	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

M40

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH_XDP

Size A4 | Document Number **LF14M** | Rev

Date: Wednesday, February 26, 2014 | Sheet 96 of 103