Compal Confidential

Kabylake-U M/B Schematics Document

Intel ULV Processor with DDR4 SODIMMx2

Date : 2016/05/11

Version : 4.0

Project :*Diner_Crepe1.1(15")*
BDL50 : LA-D704P

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Cover Page

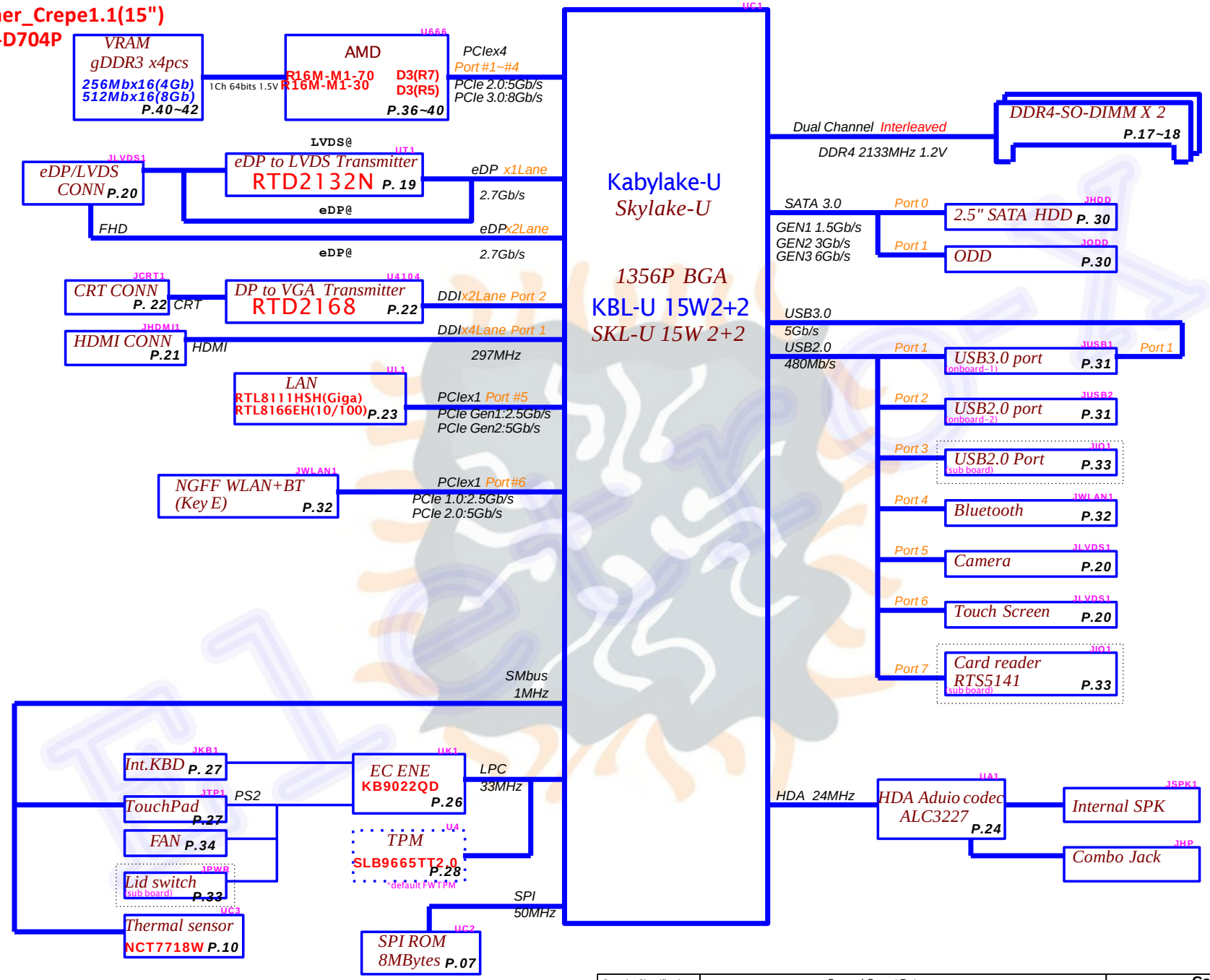
Size: Custom | Document Number: LA-D704P | Rev: 4.0

Date: Wednesday, May 11, 2016 | Sheet 1 of 6

Compal Confidential

Model Name : Diner_Crepe1.1(15")

File Name : LA-D704P



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Title: Block Diagrams

Size: Custom | Document Number: LA-D704P | Rev: 0.2

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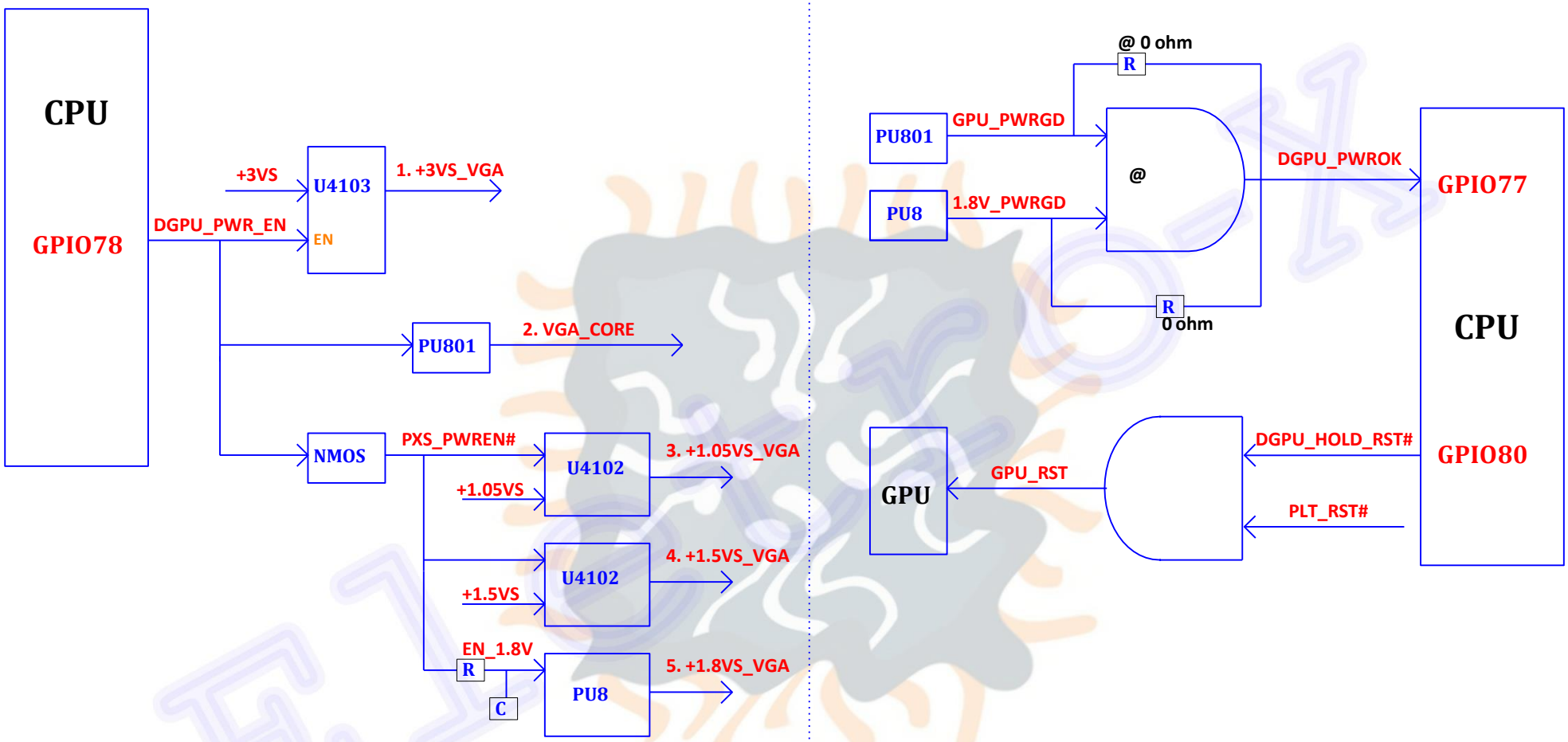

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Issued Date	Deciphered Date	Title: RSVD
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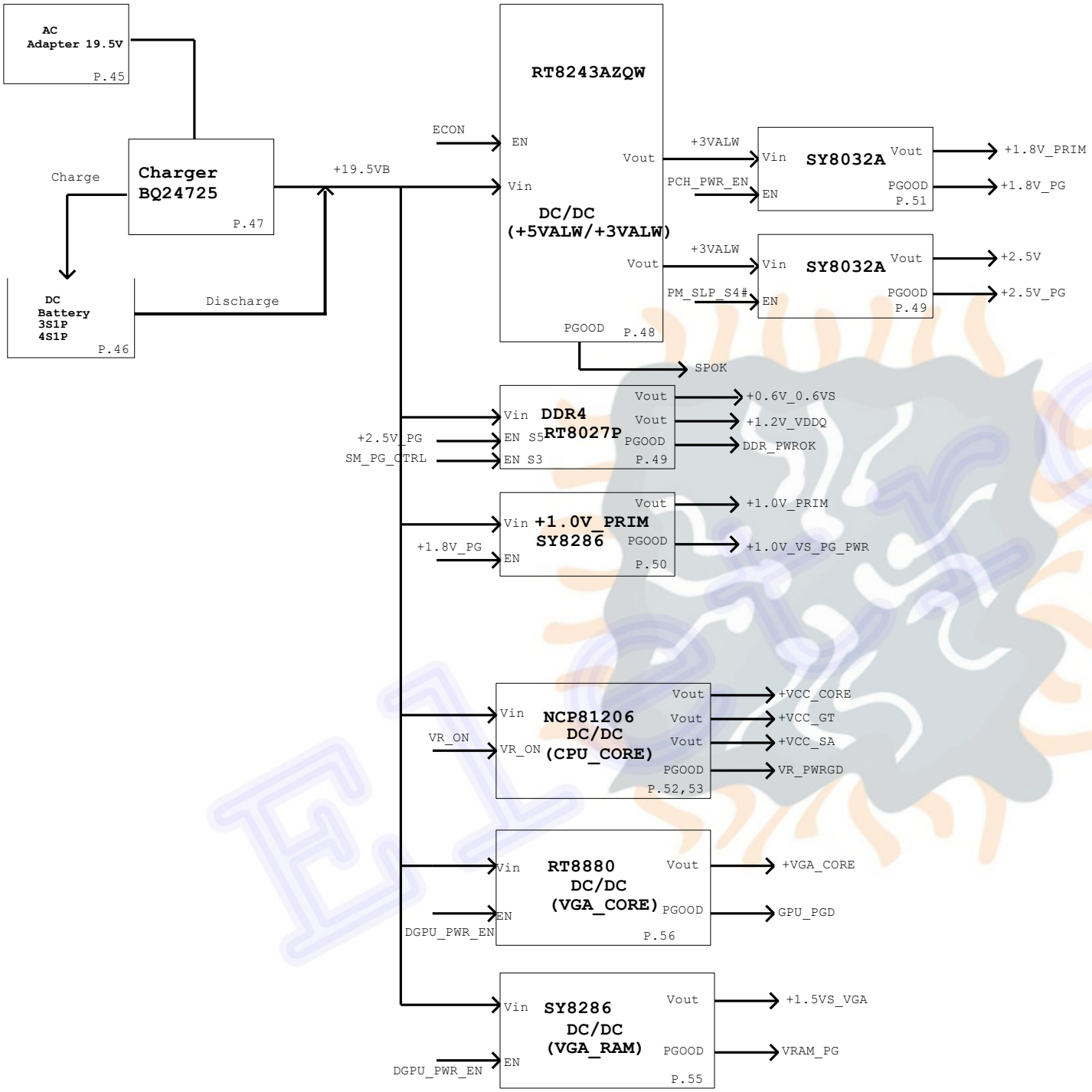


CPU DC/DC NCP81206 52~54	
INPUTS	OUTPUTS
B+	VCC_SA VCC_GT VCC_VORE

SYSTEM DC/DC RT8243AZQW 48	
INPUTS	OUTPUTS
B+	+5VALW/+3VALW

SYSTEM DC/DC RT8207P / 8032 49	
INPUTS	OUTPUTS
B+	+1.2V_VDDQ +0.6V_0.6VS +2.5V_VS

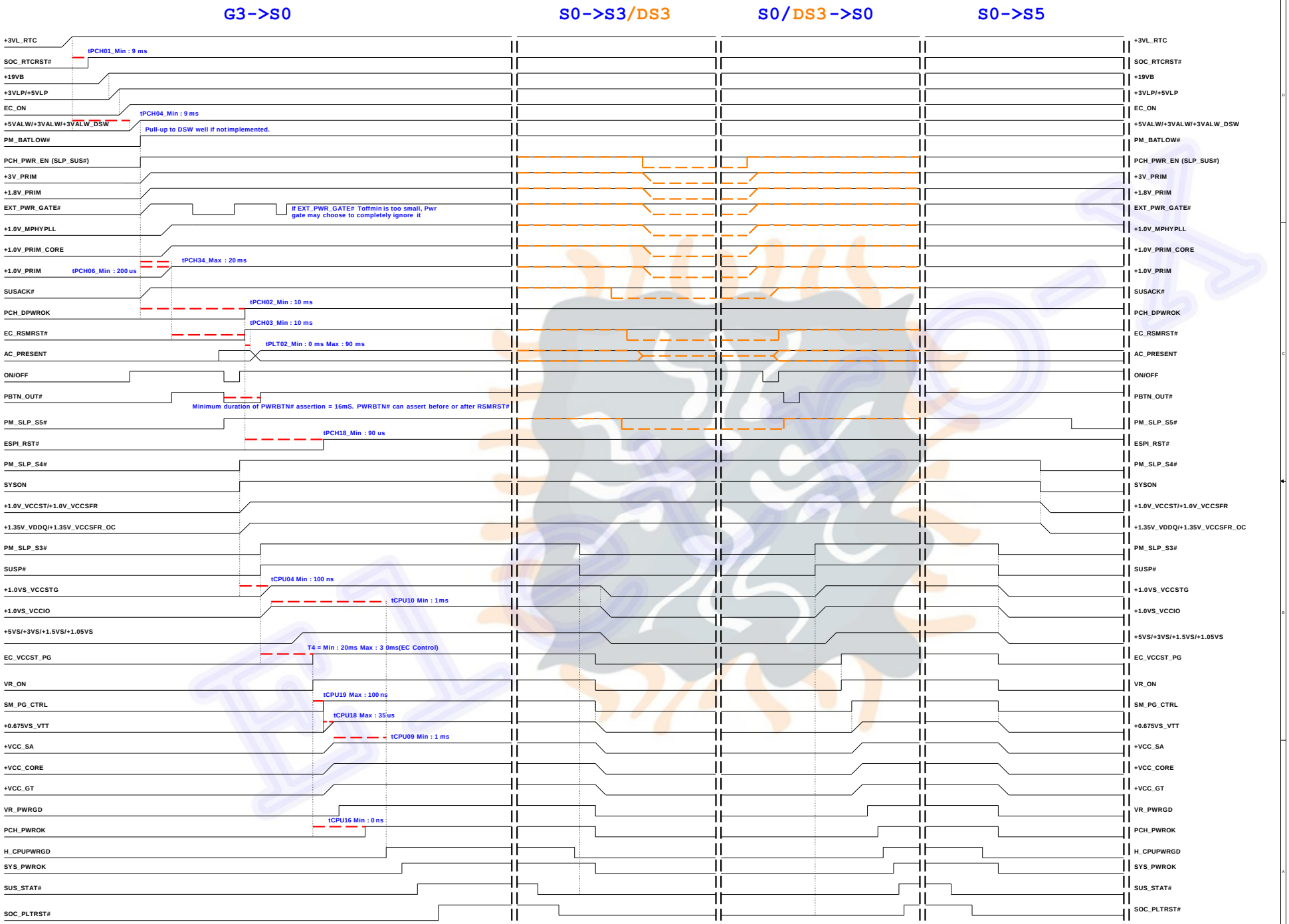
SYSTEM DC/DC SY8286 50	
INPUTS	OUTPUTS
B+	+1.0V_PRIM

SYSTEM DC/DC SY8032A 51	
INPUTS	OUTPUTS
+3VALW	+1.8V_PRIM

SYSTEM DC/DC RT8880 56~57	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8286 55	
INPUTS	OUTPUTS
B+	+1.5VS_VGA

[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Funct i on	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
SPI_IO3(MOW36)	ES@	
Crystal (DIS)	XTALPX@	
Crystal	XTAL@	
Green CLK(UMA)	GCLK@	
Green CLK(DIS)	GCLKPX@	
TPM	TPM@	

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA2
		Touch PAD	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS	ME FW	0x48/0x49	TBC	0x90/0x92
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		DGPU	TBC	TBC	TBC
		PCH	TBC	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C
		PCH	TBC

Power State

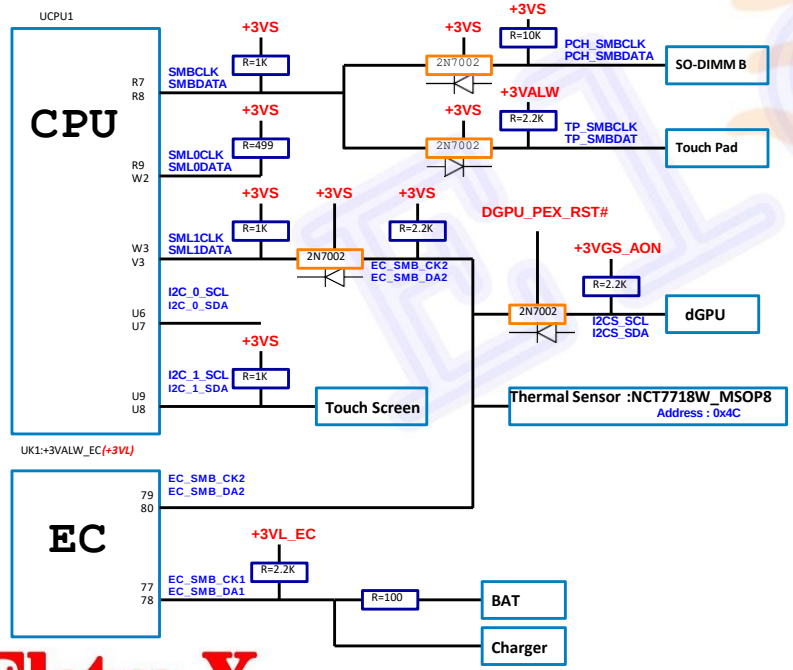
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION UMA	DESTINATION Dis
1	USB 2.0/3.0	USB 2.0/3.0
2	USB 2.0/3.0	USB 2.0/3.0
3	USB 2.0 OFF BOARD	USB 2.0 OFF BOARD
4	WLAN	WLAN
5	Camera	Camera
6	TOUCH SCREEN	TOUCH SCREEN
7	CR	CR
8		
9		
10		

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION UMA	DESTINATION Dis	CLK
1			1	USB3.0	USB3.0	X
2			2	USB3.0	USB3.0	X
3			3	USB3.0(Charger)	USB3.0(Charger)	X
4			4	USB3.0(IO Board)	USB3.0(IO Board)	X
5	1		5	X	GPU(DIS only)	CLK0
6	2		6	X	GPU(DIS only)	
7	3			X	GPU(DIS only)	
8	4			X	GPU(DIS only)	
9	5			LAN	LAN	CLK1
10	6			WLAN	WLAN	CLK2
11	7	0		2.5"HDD	2.5"HDD	X
12	8	1		ODD	ODD	X
13	9			Card reader(PCI-E)	Card reader(PCI-E)	CLK3
14	10			X	X	X
15	11	1*		X	X	X
16	12	2				X



Load BOM Opt i on Tabl e

BOM Number	Load BOM Opt ion
4519YN32L01(UMA)	
4519YN32L02(DIS)	

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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

<HDMI>

<eDP to CRT>

<eDP>

<DB> Check

<DB> DP port C enable

HDMI DDC (Port B)

UC1A SKL-U Rev_0.53

SKL-U_BGA1356

1 OF 20

UC1D SKL-U Rev_0.53

SKL-U_BGA1356

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COMPENSATION PU FOR eDP

CAD note:
Trace width=20 mils,Spacing=25mil,Max length=100mils

XDP CONN

SD000008H80

SD000008H80

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom Document Number: LA-D707P Rev: 1.0

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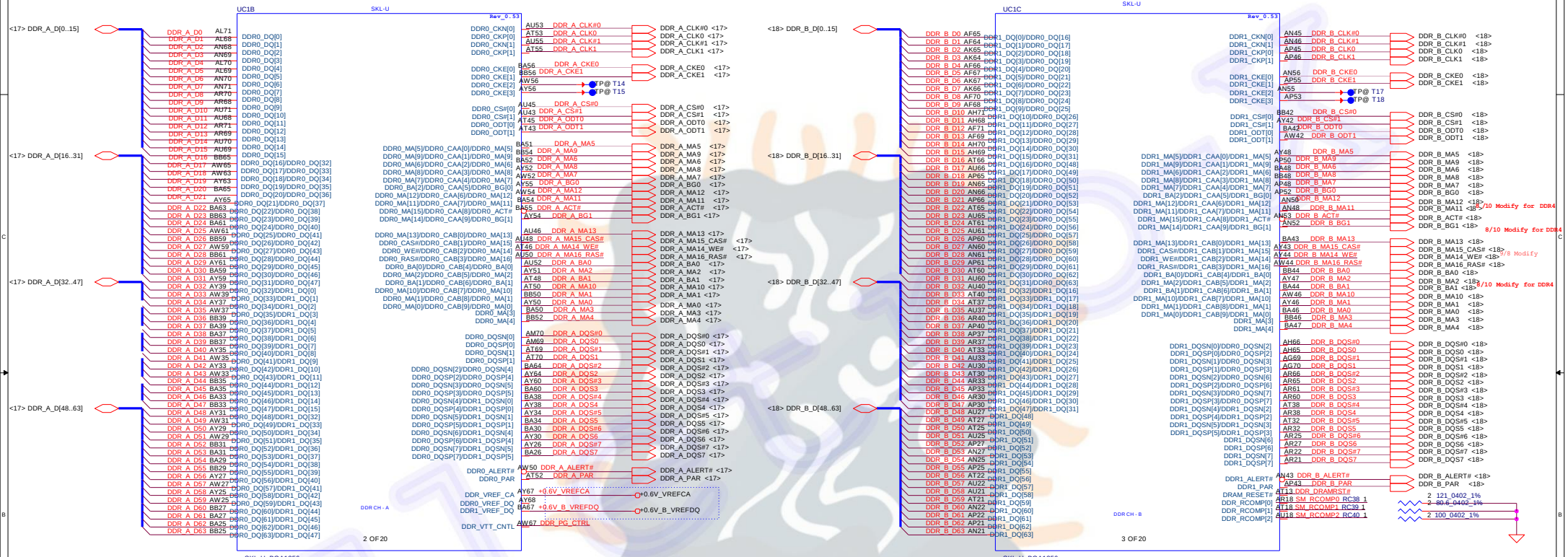
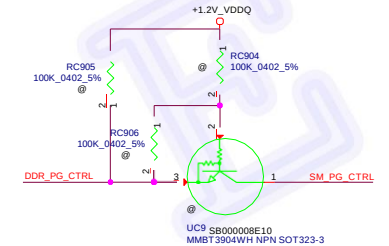
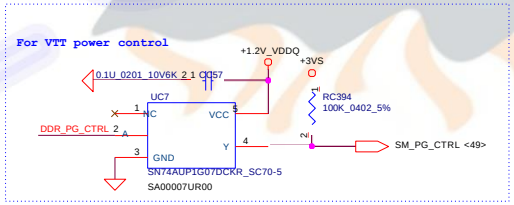
Interleaved Memory

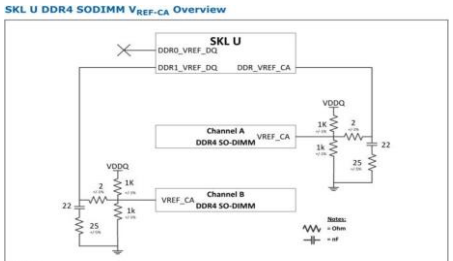
Interleaved Memory

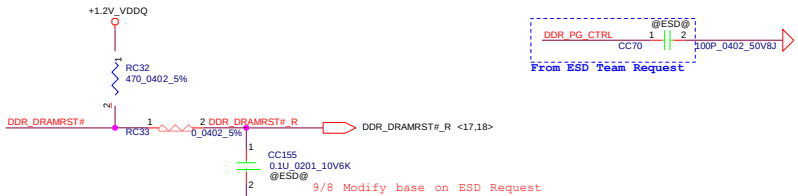
<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)











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Title: SKL-U(2/12)DDRIII

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SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E
SKL-U
SPI - FLASH
SPI - TOUCH
C LINK
LPC
SMBUS, SMLINK
Rev_0.53
SKL-U_BGA1356
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PCH_SPI_CLK AV2 SPI0_CLK
PCH_SPI_SO AW3 SPI0_MISO
PCH_SPI_SI AV3 SPI0_MOSI
PCH_SPI_SIO2 AW2 SPI0_IO2
PCH_SPI_SIO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

12/11_Delete TP

<26> EC_KBRST# EC_KBRST# AW13 GPP_A0/RCIN#
To TPM <26,28> SERIRQ SERIRQ AY11 GPP_A6/SERIRQ
LPC Mode

GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 SMBALERT# TP@ T239
GPP_C3/SML0CLK R9 SML0CLK
GPP_C4/SML0DATA W2 SML0DATA
GPP_C5/SML0ALERT# W1 SML0ALERT#
GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 1 2 SML1ALERT#
RC902 @ 0_0201_5%
TP@ T234

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME#
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#
TP@ T242

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI0 RC387 1 2 22_0402_5%
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI1 RC53 1 TPM@2 22_0402_5%
GPP_A8/CLKRUN# AW11 PM_CLKRUN#

LPC_AD0 <26,28>
LPC_AD1 <26,28>
LPC_AD2 <26,28>
LPC_AD3 <26,28>
LPC_FRAME# <26,28>
PM_CLKRUN# <26>
CLK_PCI_LPC <26>
CLK_PCI_TPM <28> To EC

SMB
(Link to XDP, DDR, TP)
SML1
(Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1%
+3V_PRIM
SML1ALERT# RC903 2 @ 1 150K_0402_1%
SML0ALERT# RC3602 @ 1 10K_0402_5%
+3VS
SMBALERT# 8 1
EC_KBRST# 7 2
6 3
5 4
RPC19 10K_0804_8P4R_5%

11/28_Follow Intel check list, add PU res

<SI>un-mount RC53
11/28 CPU side delete EC_PCIE_WAKE#

To SPI ROM UC2 Source From

RPH11
PCH_SPI_CS0#_R 1 8 EC_SPI_CS0#
PCH_SPI_CS0#_R 2 7 PCH_SPI_CS0#
PCH_SPI_SO_R 3 6 EC_SPI_SO
PCH_SPI_SO_R 4 5 PCH_SPI_SO
15_0804_8P4R_5%
EC_SPI_CS0# <26>
EC_SPI_SO <26>

RPH12
PCH_SPI_HOLD# 1 8 PCH_SPI_SIO3
PCH_SPI_SI_R 2 7 PCH_SPI_SI
PCH_SPI_SI_R 3 6 EC_SPI_SI
4 5
15_0804_8P4R_5%
EC_SPI_SI <26>

PCH_SPI_WP# 2 RC388 15_0402_5% 1 PCH_SPI_SIO2

SPI ROM (8MByte Only)
UC2
+3V_SPI
CC8 1 2 0.1U_0402_16V7K
PCH_SPI_CS0#_R 1 /CS VCC 8 PCH_SPI_HOLD#
PCH_SPI_SO_R 2 DO(IO1) /HOLD(IO3) 7 PCH_SPI_CLK_R
PCH_SPI_WP# 3 /WP(IO2) CLK 6 PCH_SPI_SI_R
4 GND DI(IO0) 5
W25Q64FVSSIQ_SO8 SA000039A30
PCB Footprint = ACES_91960-0084L_8P-T
Use socket footprint

SPI ROM:
Main:SA000039A30, S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
2nd :SA00007LA10, S IC FL 64M GD25B64CSIGR SOP 8P SPI ROM
3rd :SA000039300, S IC FL 64M N25Q064A13ESEDFF SOP8 8P SPI

RC368 15_0402_5% PCH_SPI_CLK 2 1 PCH_SPI_CLK_R PCH_SPI_CLK_R <26>
EMI@
CC9 1 2 10P_0402_50V8J @EMI@

+3VS +3VS
RC216 10K_0402_5% RC215 10K_0402_5%
QC1A SMBCLK 6 1 PCH_SMBCLK <17,18,19,22>
2N7002DWH_SOT363-6 SB00000I700
QC1B SMBDATA 3 4 PCH_SMBDATA <17,18,19,22>
2N7002DWH_SOT363-6 SB00000I700

+3VS
<Cocoa_1020>
add level shift
2N7002DWH_SOT363-6
QC2A SML1CLK 6 1 EC_SMB_CK2 <10,19,22,26,37>
SB00000I700
QC2B SML1DATA 3 4 EC_SMB_DA2 <10,19,22,26,37>
2N7002DWH_SOT363-6 SB00000I700

<DB> PWR Rail
+3V_PRIM +3VALW
RC81 10K_0402_5% RC82 10K_0402_5%
SB00000I700
QC7A SMBCLK 1 6 TP_SMBCLK <27>
2N7002DWH_SOT363-6
SMBDATA 4 3 TP_SMBDATA <27>
QC7B SB00000I700
2N7002DWH_SOT363-6

11/28_Change PWR rail from +3VS to +3V_PRIM

+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBDATA 3 6
SMBCLK 4 5
1K_0804_8P4R_5%

+3V_SPI
PCH_SPI_SIO2 RC3901 @ 2 1K_0402_1%
PCH_SPI_SIO3 RC3911 @ 2 1K_0402_1%
PCH_SPI_CS0#_R 1 @ 2 RC357 1K_0402_5%

PCH_SPI_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

+3VS_PGPPA
PM_CLKRUN# 1 RC107 2 8.2K_0402_5%
SERIRQ 1 RC122 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA000051L00 S IC FL 64M N25Q064A13ESEC0F SO8W 8P

ENE Fixed Code Block Diagram
CPU
EC
SPI_ROM
M:Master
S : Slave
O : Output
I : Input

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Compal Electronics, Inc.
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
Size: Custom | Document Number: LA-D707P | Rev: 1.0
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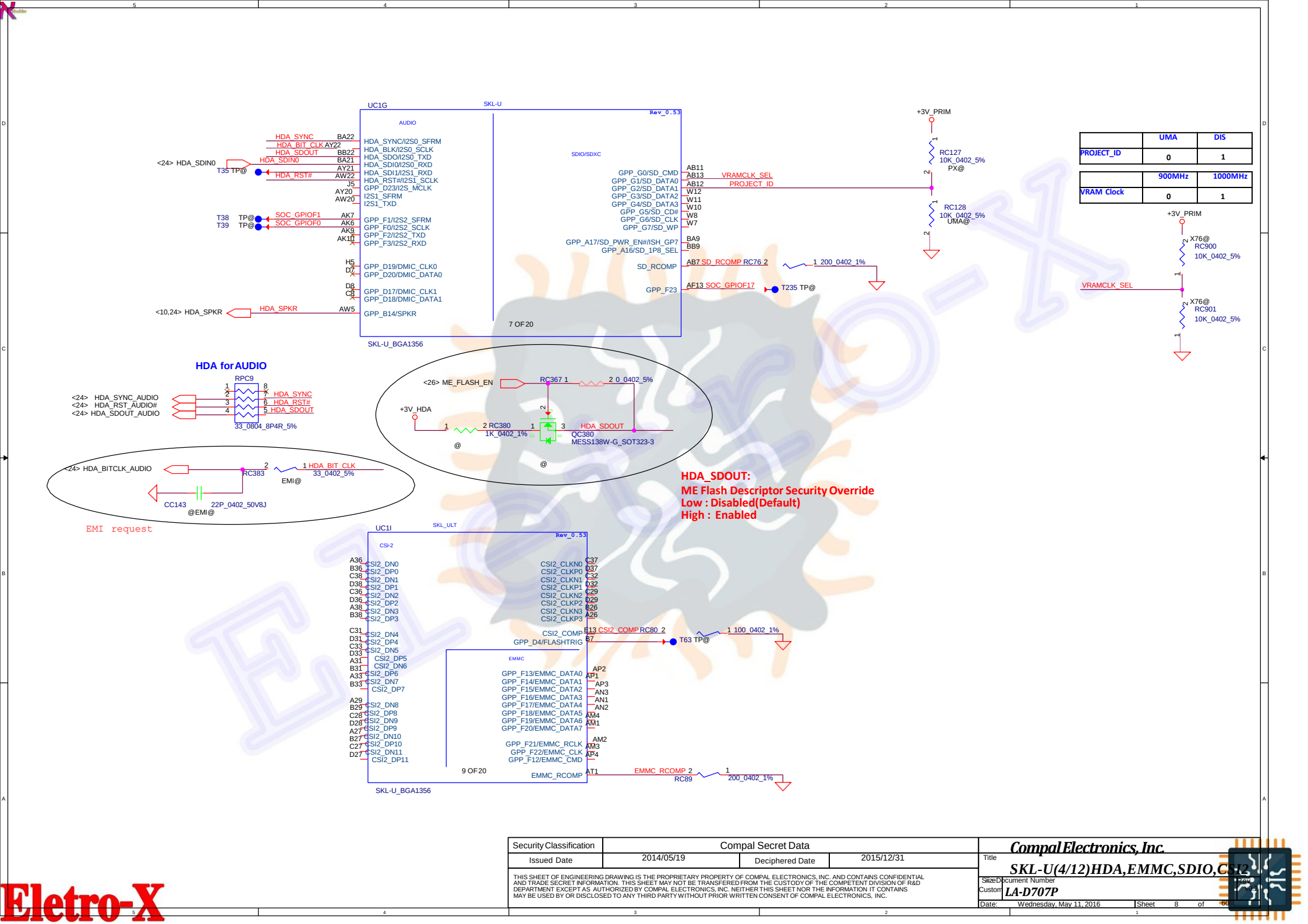

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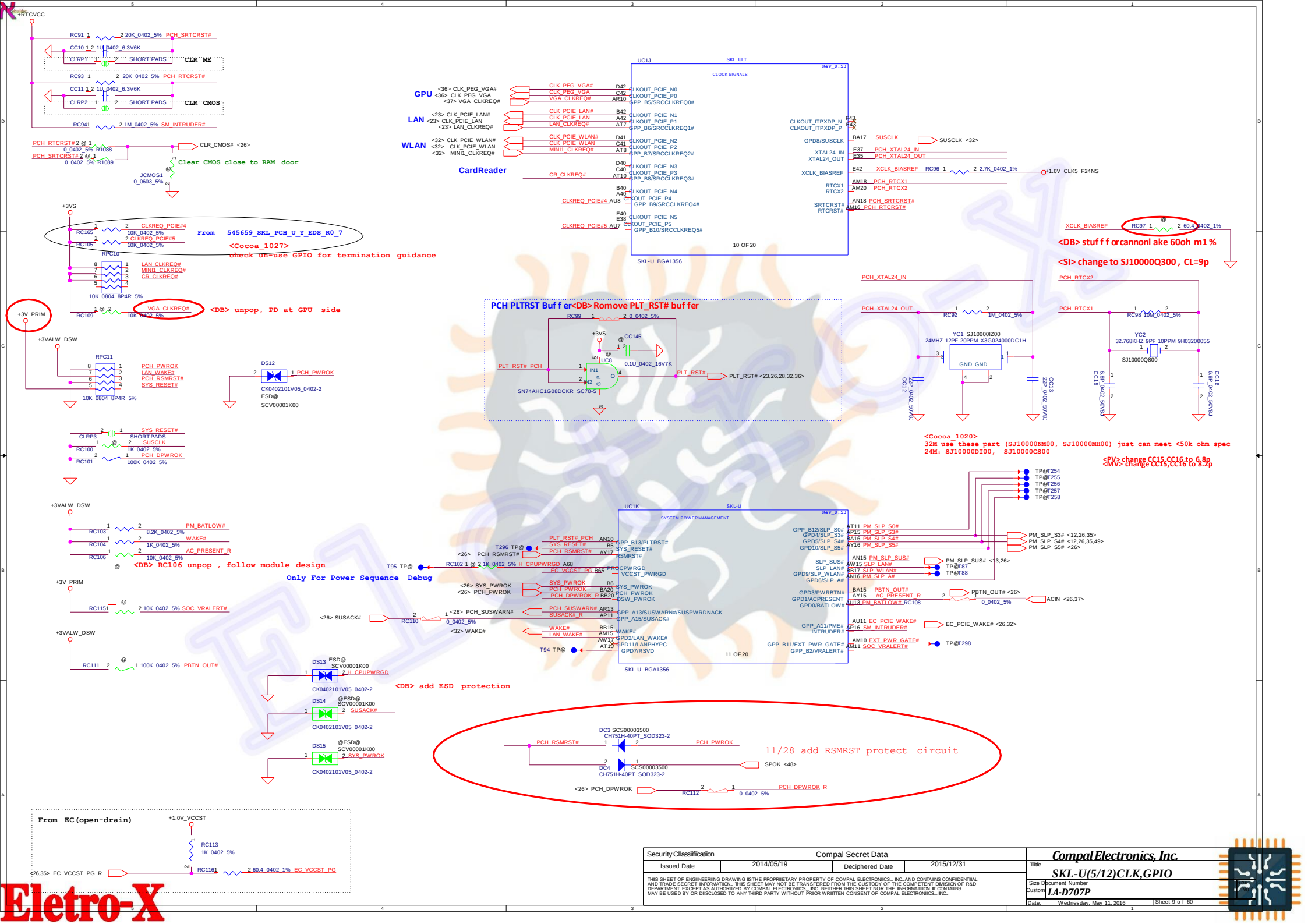
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 8 of 60



Security Classification	Compal Secret Data	
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Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

Size: Custom | Document Number: LA-D707P | Rev: 1.0

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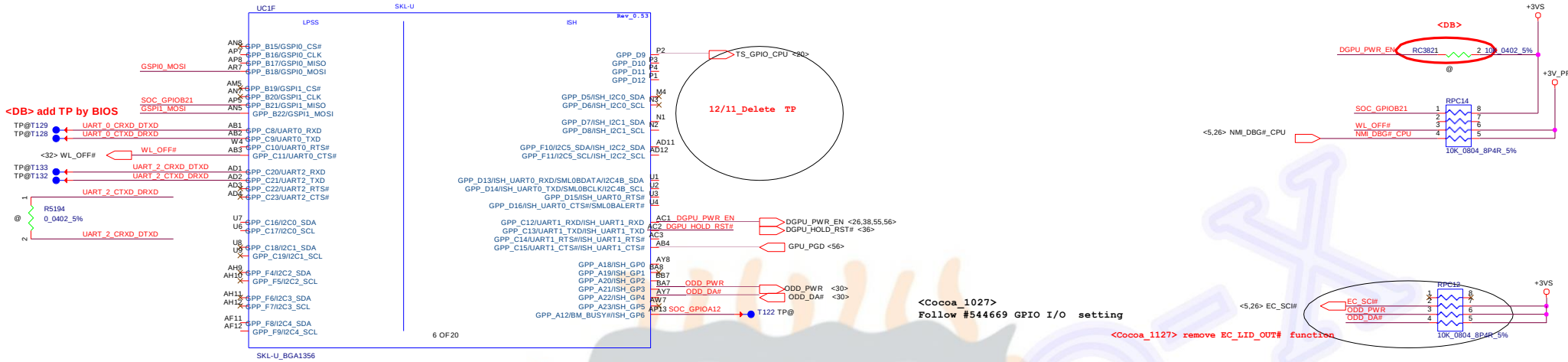


Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

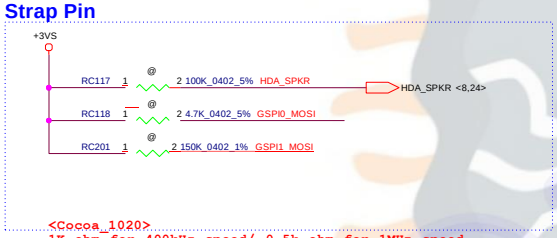
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

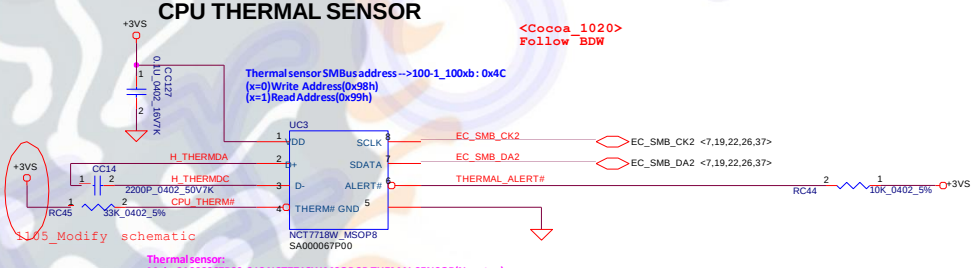
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

<Cocoa_1020>
Follow BDW



<DB>
Delete Win7 debug port

Compal Electronics, Inc.
Title: SKL-U(6/12)GPIO
Size: Custom
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Date: Wednesday, May 11, 2016
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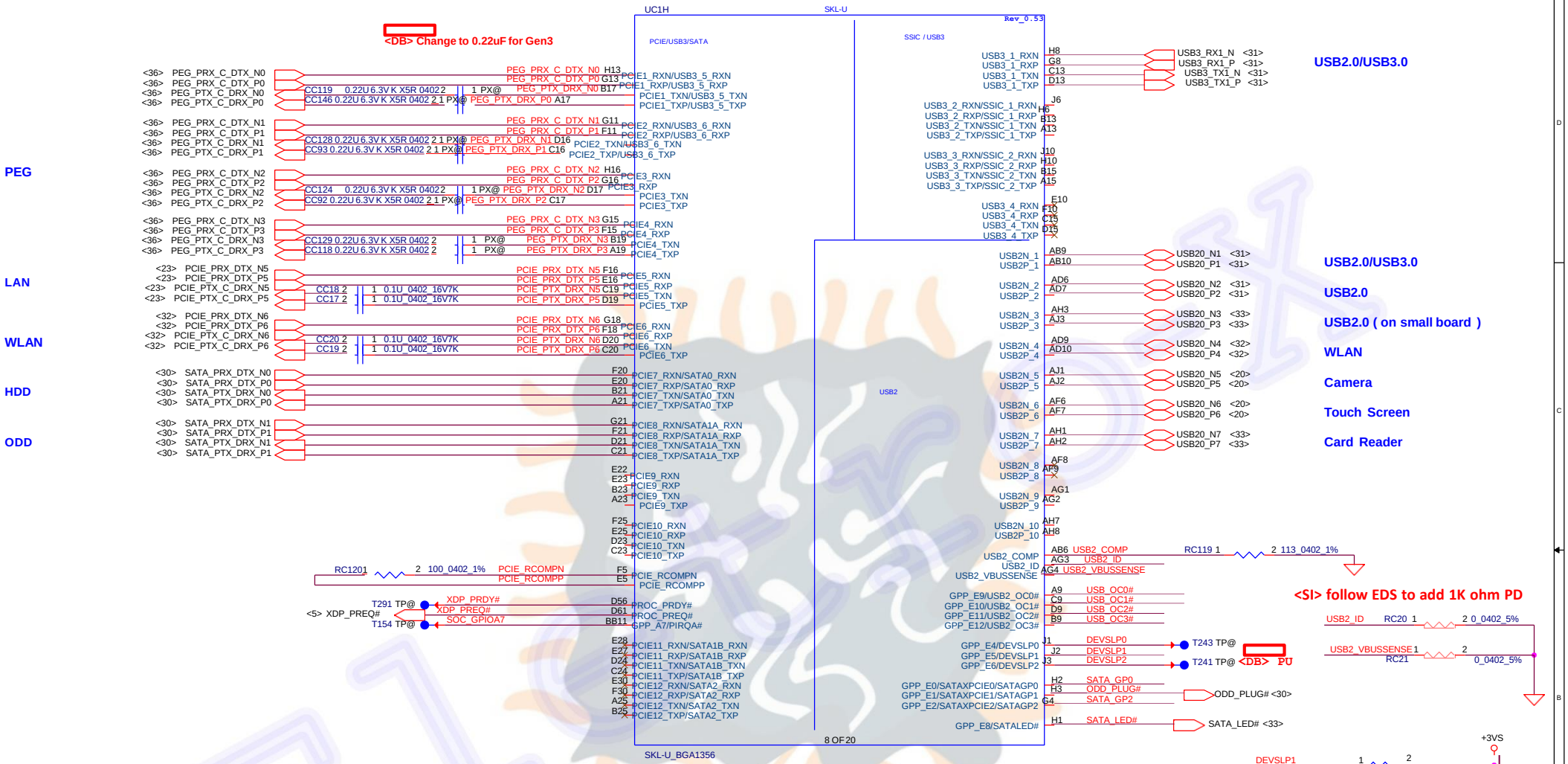
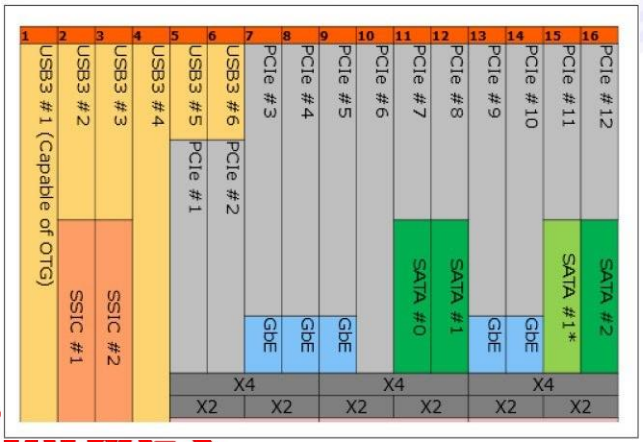


High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NGFF SSD KEY B
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	ODD_PLUG#

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

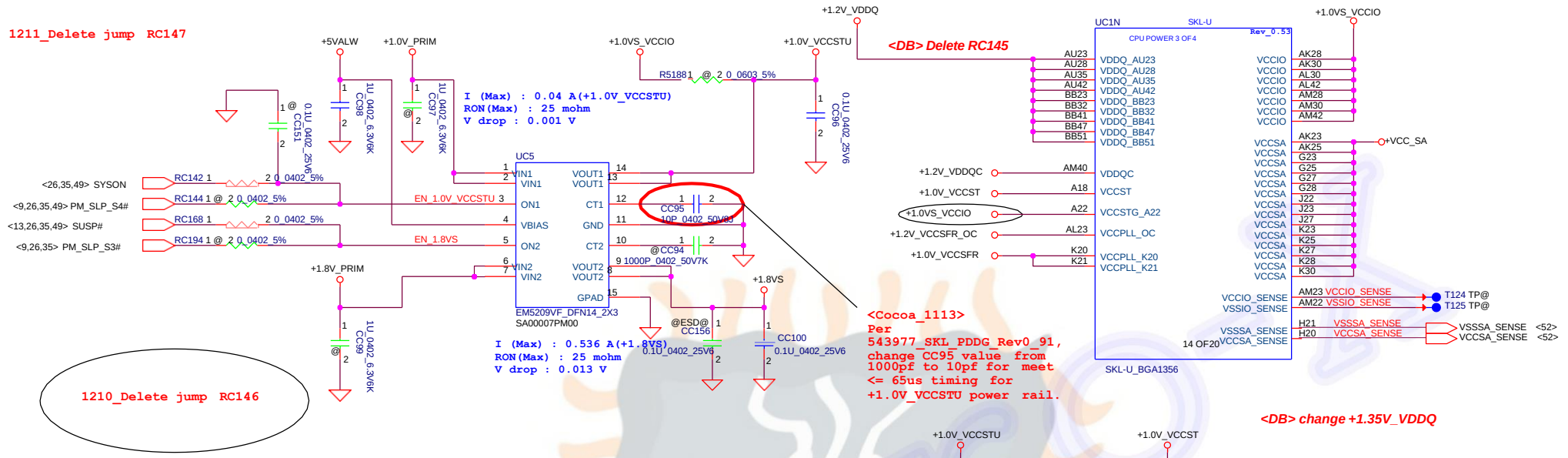
Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 11 of 60

+1.0V_PRIM TO +1.0V_VCCSTU

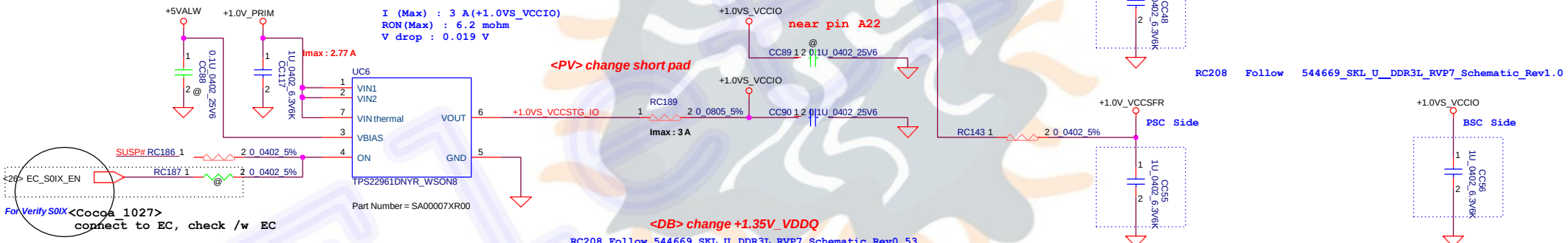
1211_Delete jump RC147

1210_Delete jump RC146



<DB> change +1.35V_VDDQ

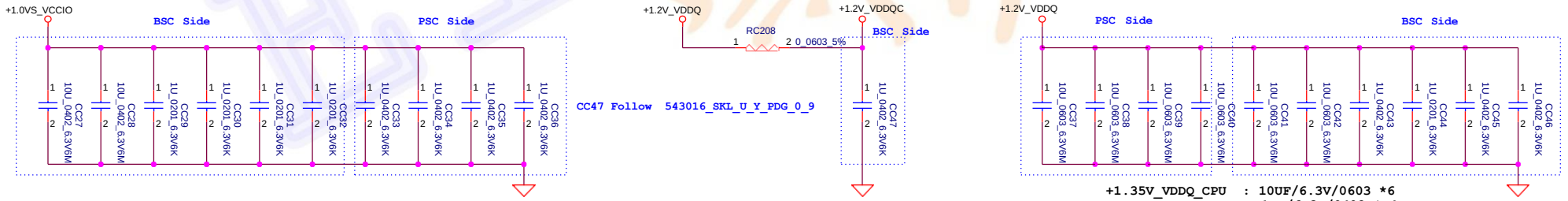
+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO



<DB> change +1.35V_VDDQ

RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53

<DB> change +1.35V_VDDQ



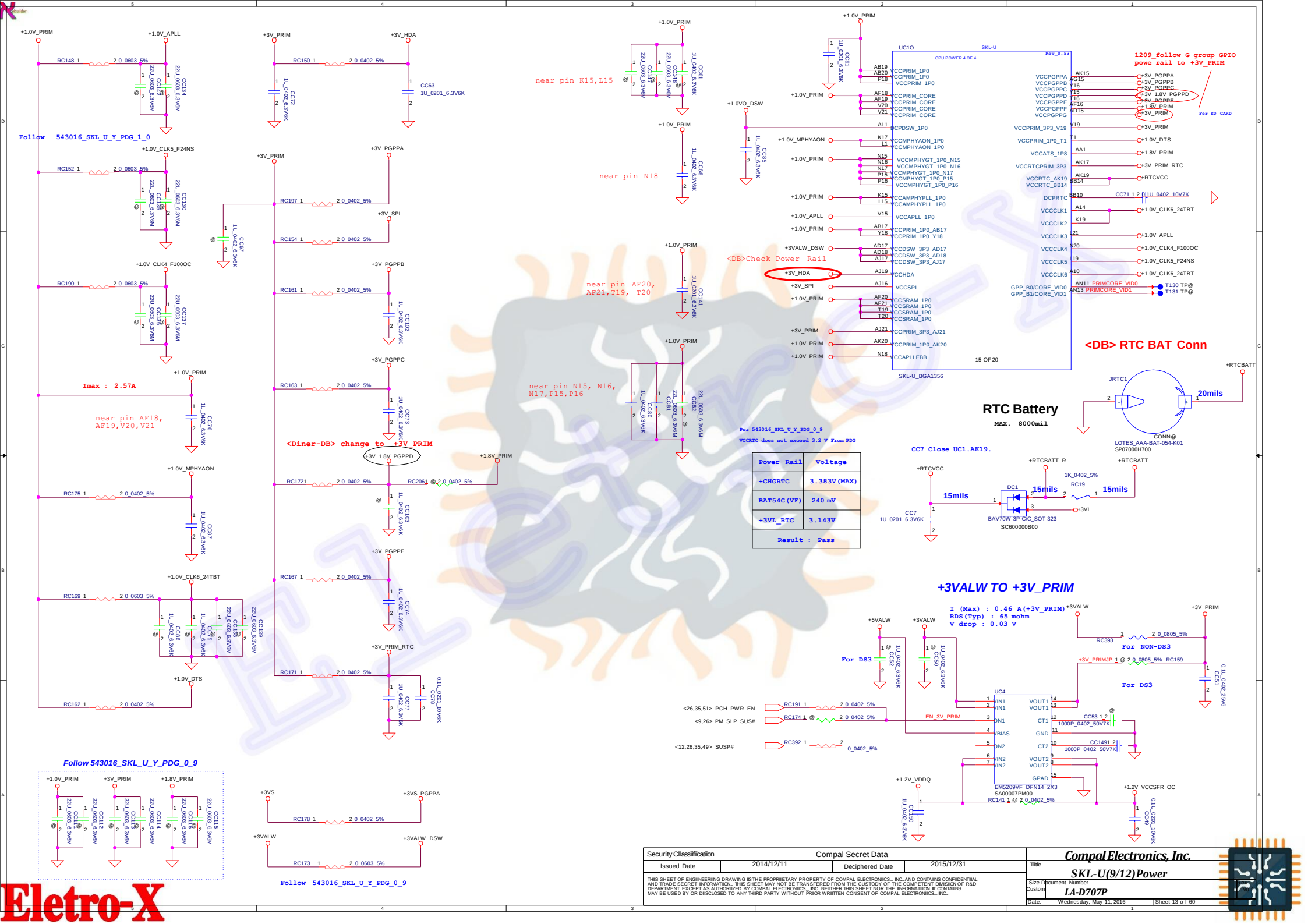
Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 12 of 60



Security Classification	Compal Secret Data	
Issued Date	2014/12/11	Deciphered Date 2015/12/31

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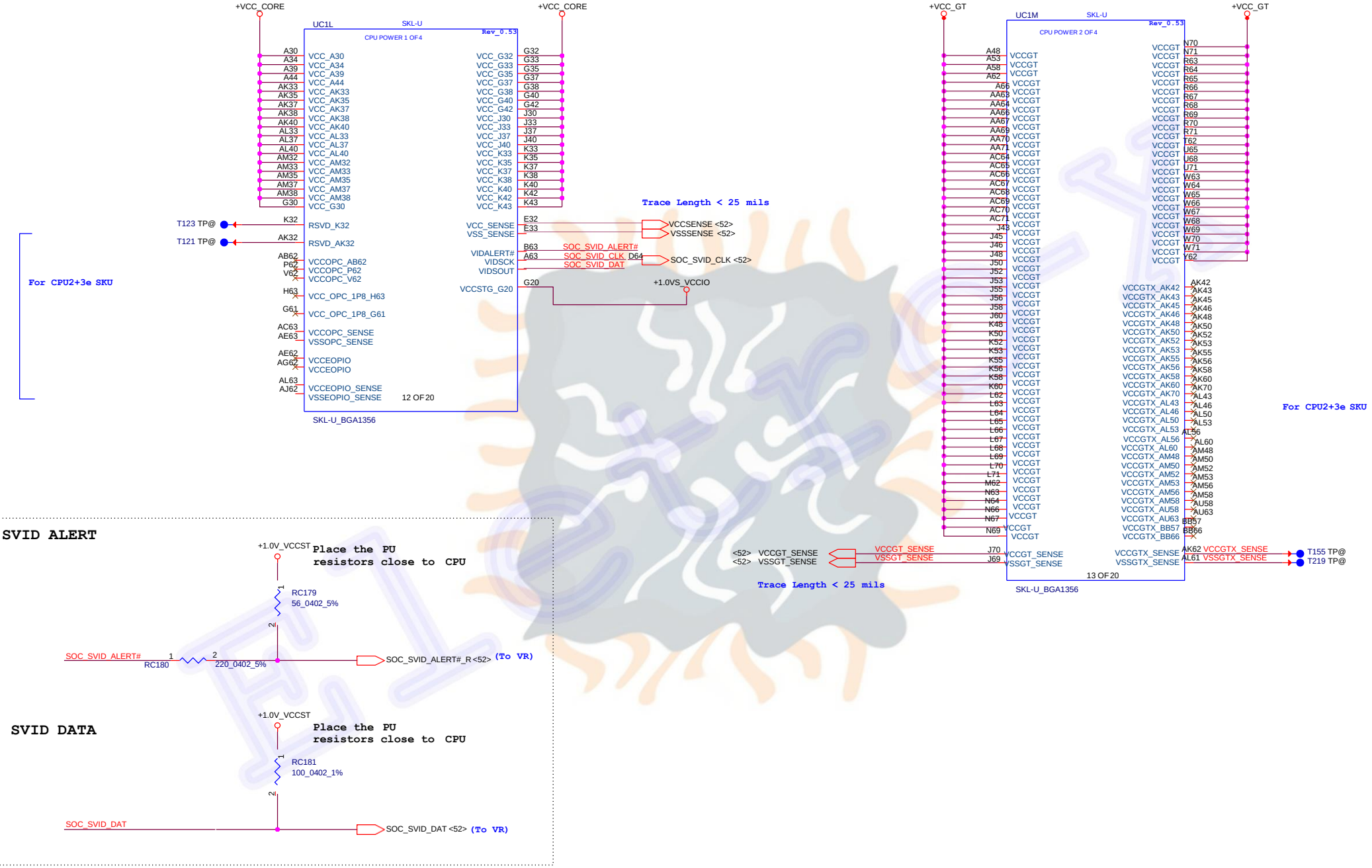
Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 13 of 60

Eletro-X



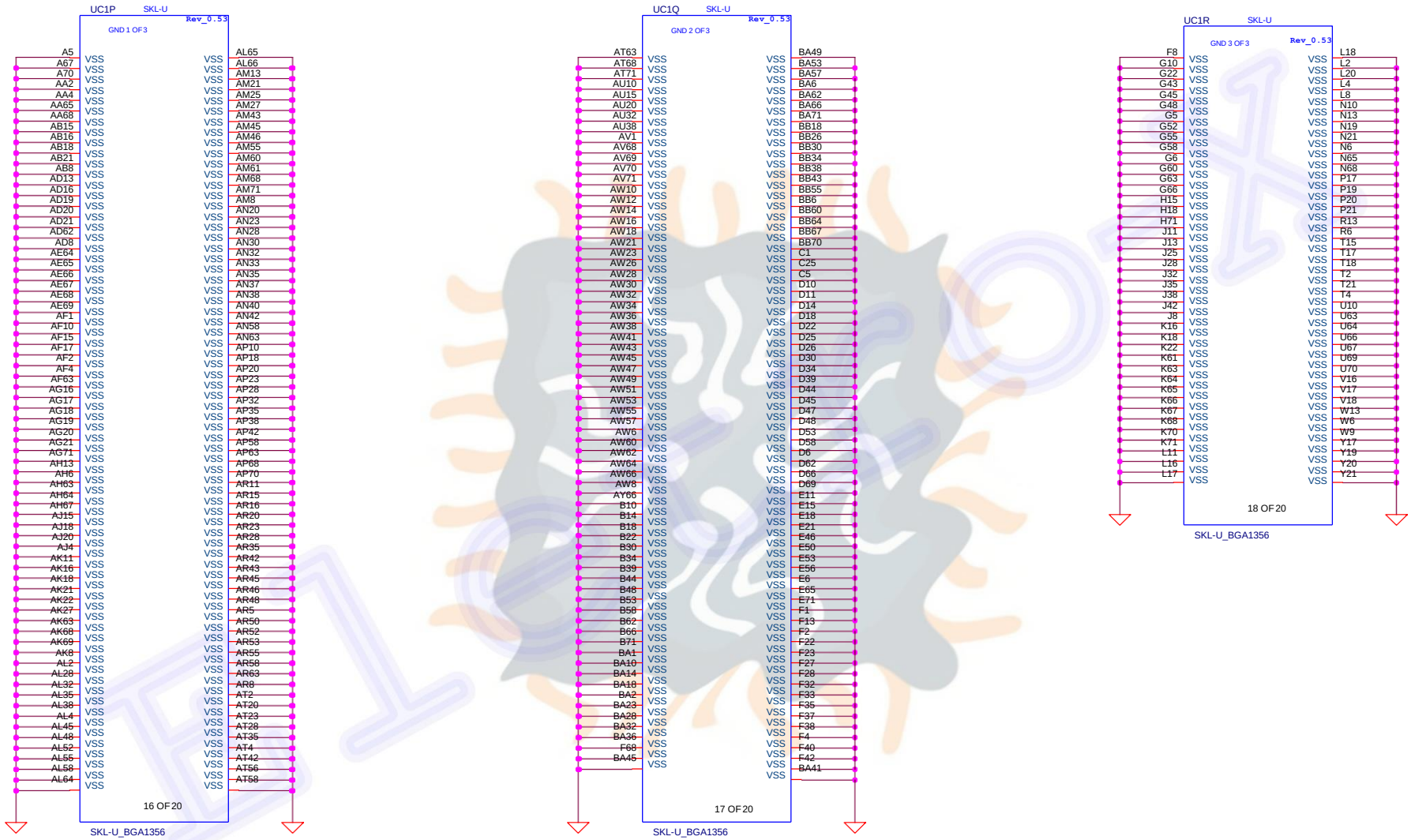
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-D707P	1.0

Date: Wednesday, May 11, 2016 Sheet 14 of 60



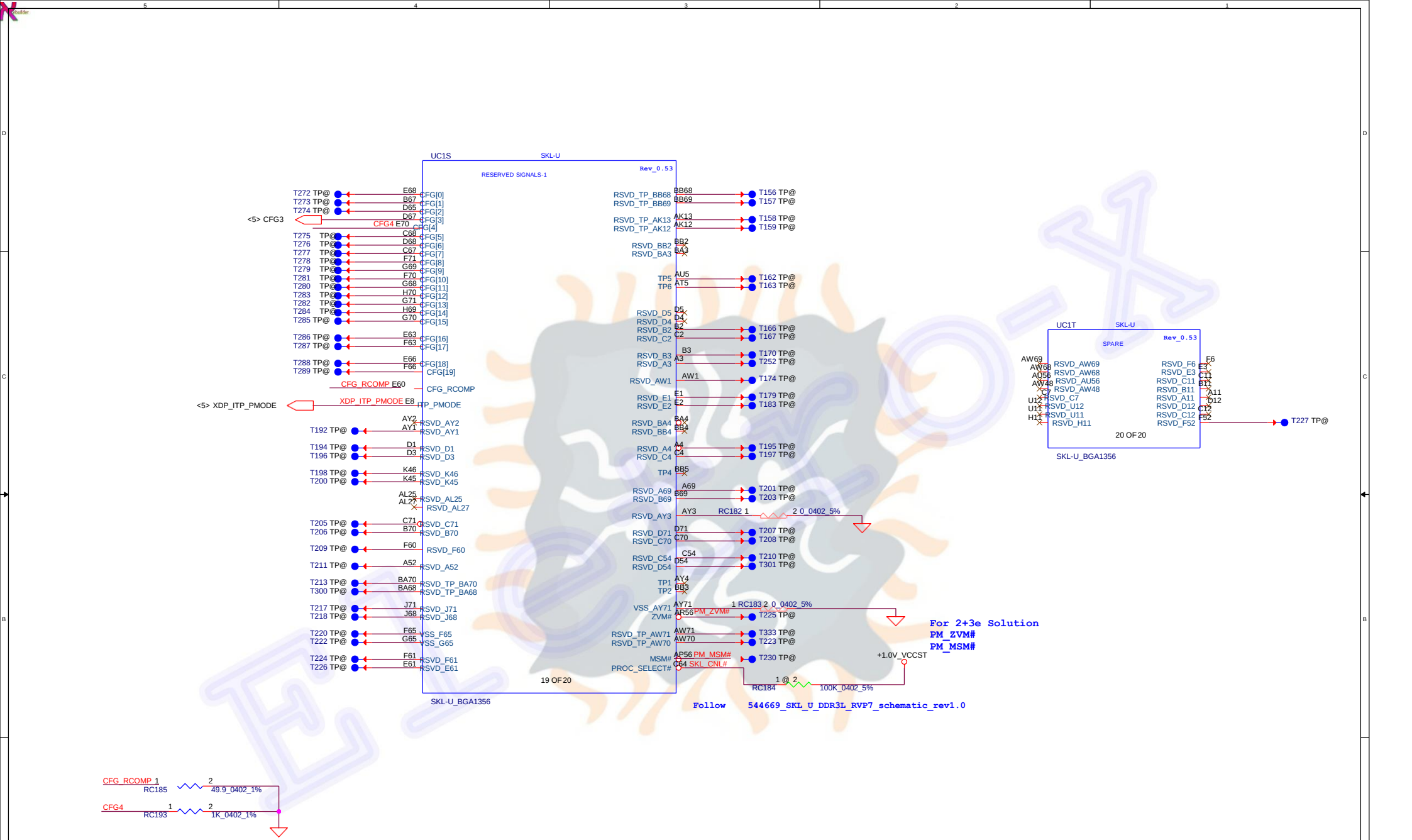
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(11/12)GND

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 15 of 60



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: LA-D707P | Rev: 0.2

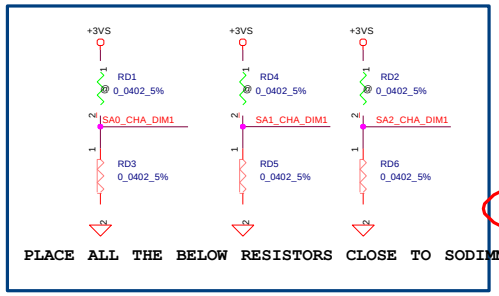
Date: Wednesday, May 11, 2016 | Sheet 16 of 60

CHANNEL-A

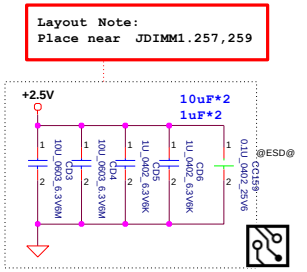
REVERSE TYPE (5.2 mm)

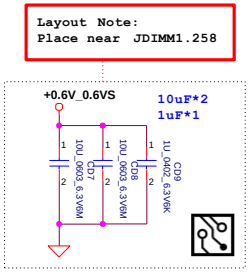
Interleaved Memory

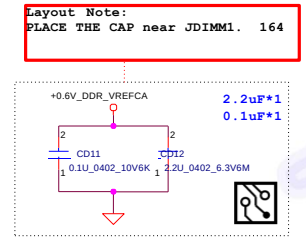
TOP: JDIMM1 CONN Non-ECC DIMM

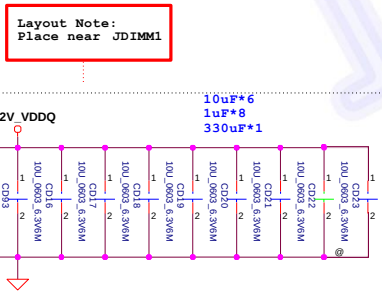


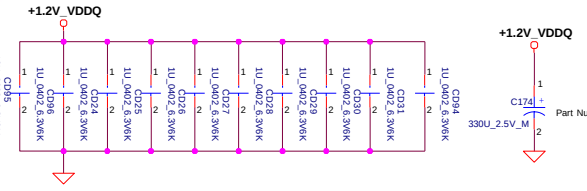
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

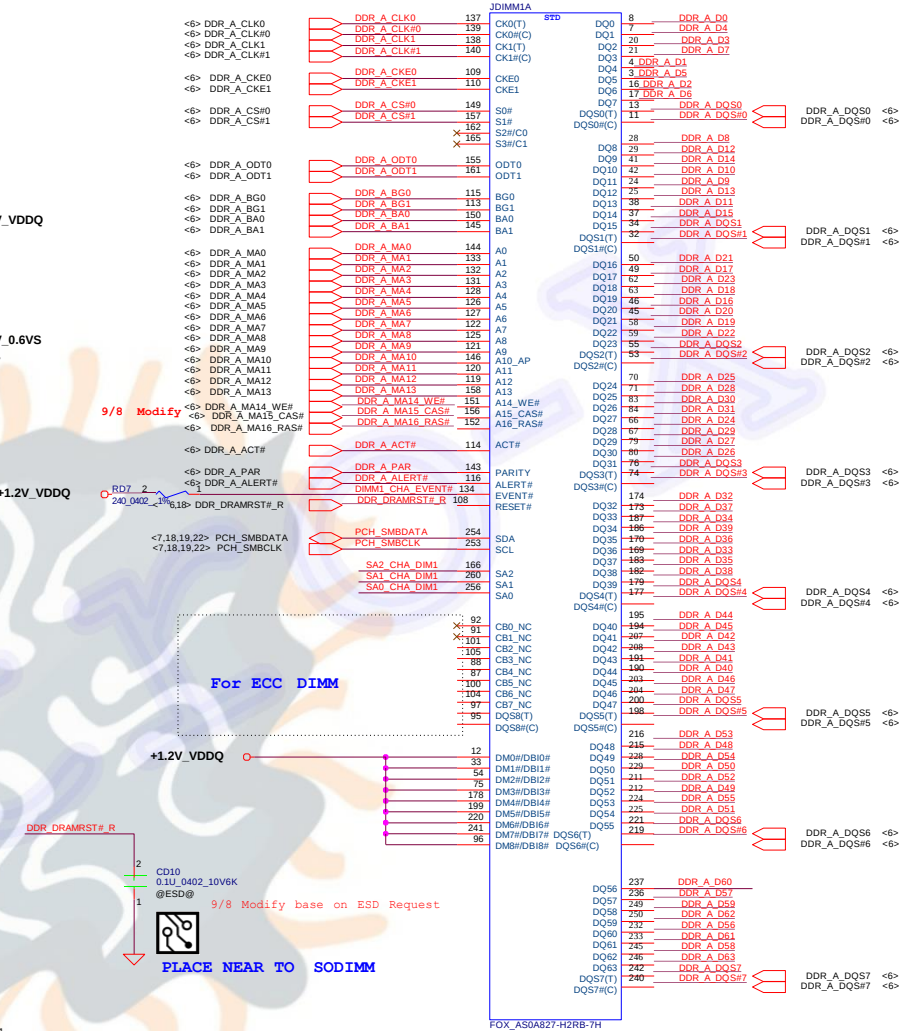




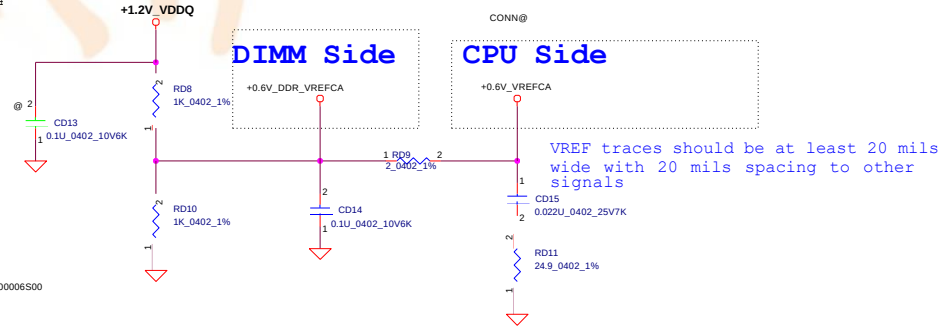








Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4



Security Classification	Compal Secret Data	
Issued Date	2015/08/03	Deciphered Date 2015/12/31

Compal Electronics, Inc.

Title: P18-DDRIV_CHA: DIMM0

Size: Document Number: LA-D707P

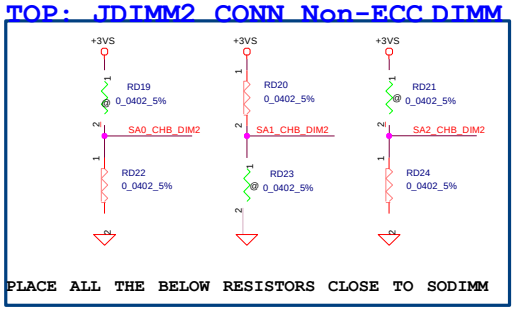
Date: Wednesday, May 11, 2016 Sheet 17 of 60

CHANNEL-B

Interleaved Memory

STD (5.2 mm)

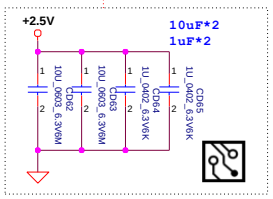
TOP: JDIMM2 CONN Non-ECC DIMM



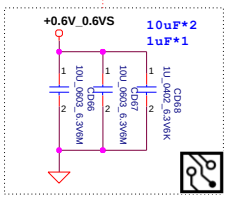
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

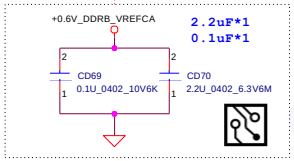
Layout Note:
Place near JDIMM2.257,259



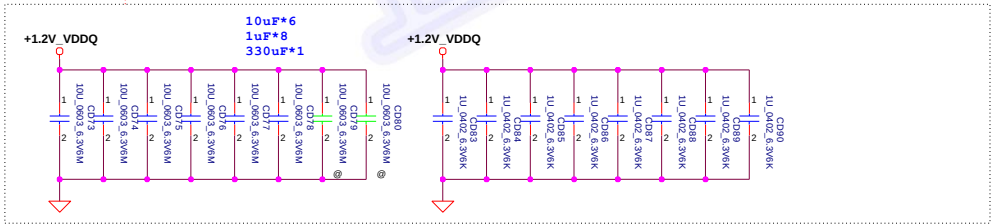
Layout Note:
Place near JDIMM2.258

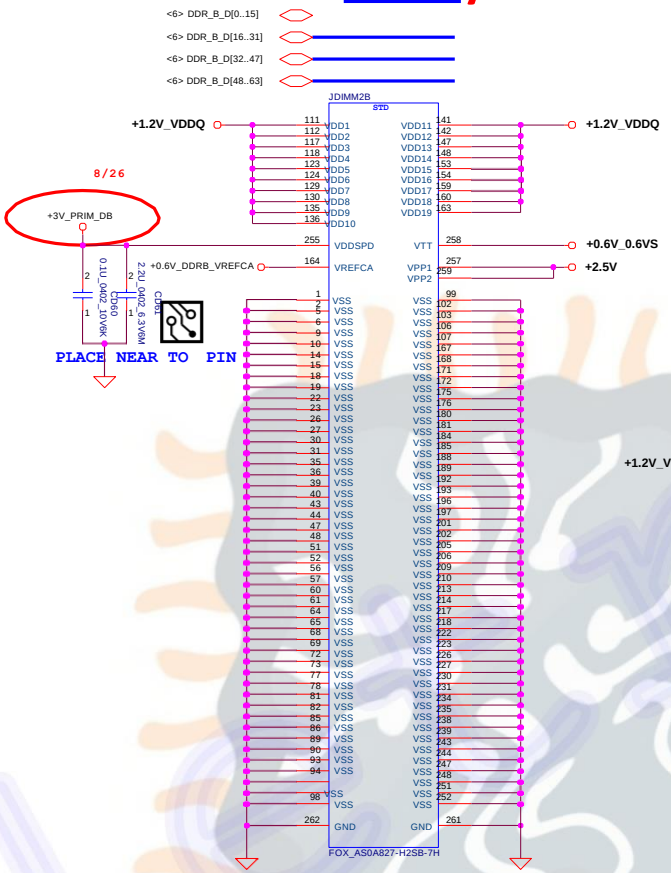


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

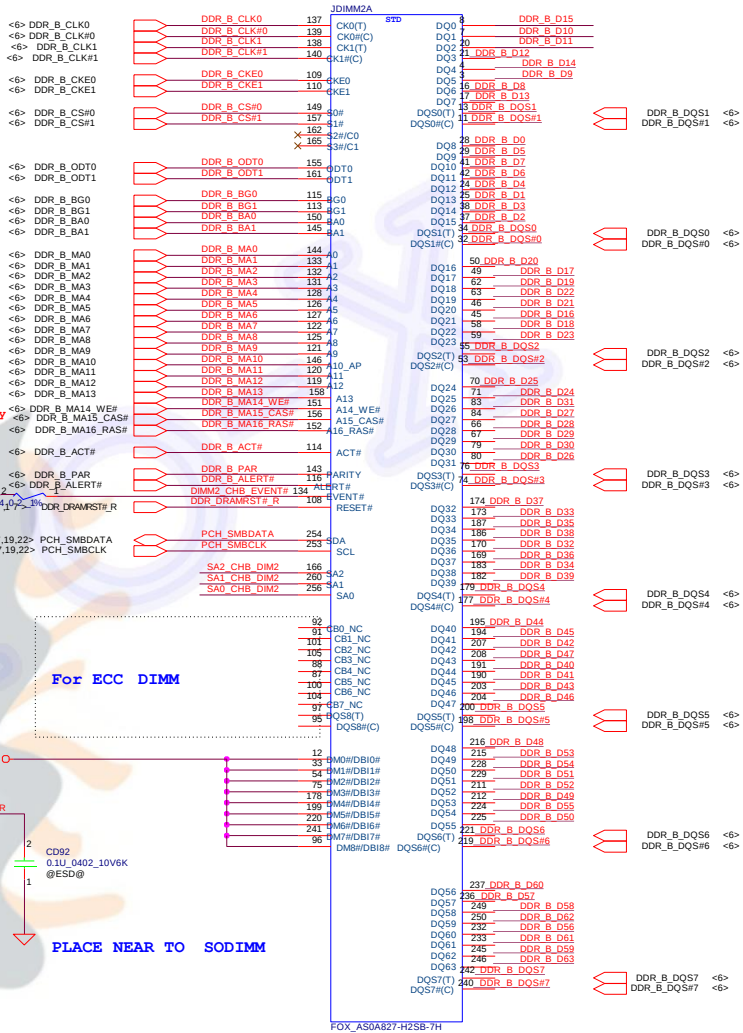


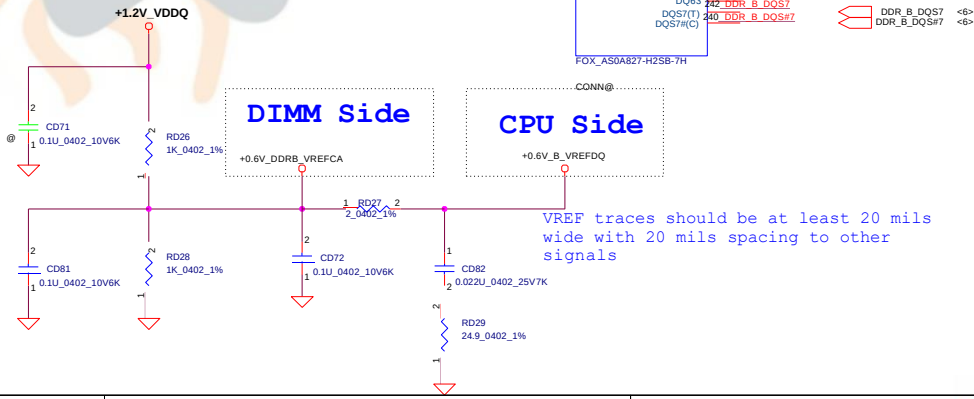
Layout Note:
Place near JDIMM2





Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2015/08/03	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: P19-DDRIV_CHB: DIMM0

Size: LA-D707P | Document Number | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 18 of 60

<5,6,7,9,10,11,13,17,18,20,21,22,23,24,26,28,32,33,34,35,36,37,38,52,55,56 +3VS +3VS

<CPU CTRL>

<5> EDP_HPD → EDP_HPD

RT11 100K_0402_5%

RTD2132 SMBus revrse to PCH

<7,10,22,26,37> EC_SMB_CK2 — RT193 1 2 0_0201_5% CIICSCL1
<7,10,22,26,37> EC_SMB_DA2 — RT194 1 2 0_0201_5% CIICSDA1
<7,17,18,22> PCH_SMBCLK — RT195 1 @ 2 0_0201_5% RT196 1 @ 2 0_0201_5%
<7,17,18,22> PCH_SMBDATA

Layout notes
CC97~CC102 must closed to connector

<CPU>

<5> EDP_CPU_AUX_C — CT102 1 2 .1U_0402_16V7K EDP_CPU_AUX
<5> EDP_CPU_AUX#_C — CT101 1 2 .1U_0402_16V7K EDP_CPU_AUX#
<5> EDP_CPU_LANE_P0_C — CT98 1 2 .1U_0402_16V7K EDP_CPU_LANE_P0
<5> EDP_CPU_LANE_N0_C — CT97 1 2 .1U_0402_16V7K EDP_CPU_LANE_N0
<5> EDP_CPU_LANE_P1_C — CT103 1 2 .1U_0402_16V7K EDP_CPU_LANE_P1
<5> EDP_CPU_LANE_N1_C — CT100 1 eDP@ 2 .1U_0402_16V7K EDP_CPU_LANE_N1

DB phase :
add eDP Lan1 for FHD
20141117

EDP_HPD — RT34 1 2 0_0201_5% EDP_HPD_PANEL → EDP_HPD_PANEL <20>

Delete BKL_PWM_CPU and DP_INT_PWM
20141113

<CPU by PASS eDP>

0_0804_8P4R_5%
EDP_CPU_LANE_N0 1 — 8 EDP_LANE_N0
EDP_CPU_LANE_P0 2 — 7 EDP_LANE_P0
EDP_CPU_AUX 3 — 6 EDP_AUX
EDP_CPU_AUX# 4 — 5 EDP_AUX#
RP6 eDP@ SD309000080
2

<eDP to connector>

RP9 eDP@ SD309000080
EDP_AUX 4 — 5 LCD_CLK — LCD_CLK <20>
EDP_AUX# 3 — 6 LCD_DATA — LCD_DATA <20>
EDP_LANE_N0 2 — 7 LVDS_TXN2_LN0 — LVDS_TXN2_LN0 <20>
EDP_LANE_P0 1 — 8 LVDS_TXP2_LP0 — LVDS_TXP2_LP0 <20>
0_0804_8P4R_5%
4

Layout notes
RP6 RP9 RP10 must closed to connector

EDP_CPU_LANE_P1 — RT16 1 2 0_0402_5% LVDS_TXP1_LP1 → LVDS_TXP1_LP1 <20>
EDP_CPU_LANE_N1 — RT17 1 2 0_0402_5% LVDS_TXN1_LN1 → LVDS_TXN1_LN1 <20>

DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

<RTS2132>
<ECCTRL>

<26> EC_BKOFF#
EC_BKOFF# — TS_BKOFF#
RT12 100K_0402_5% LVDS@

RT14 1 @ 2 0_0402_5%
CT24 1 2 @ 0.1U_0402_16V7K
+3VS
UT3 TC7SH08FUF_SSOP5 LVDS@
EC_TS_BKOFF# <20>
RT15 1 2 0_0402_5%

<LVDS Panel>

PD 100K on LVDS page

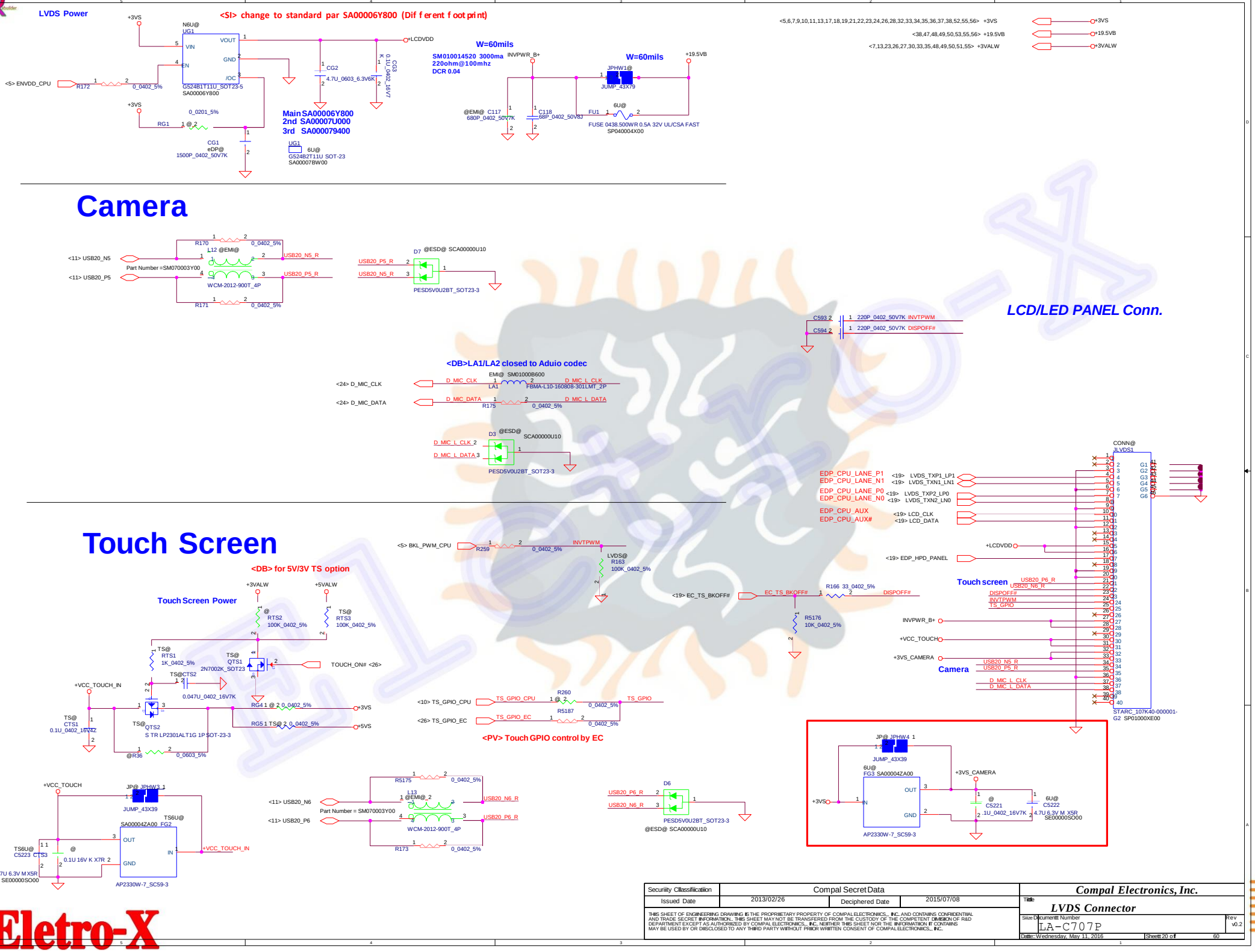
Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciiiphered Date	2015/3/1

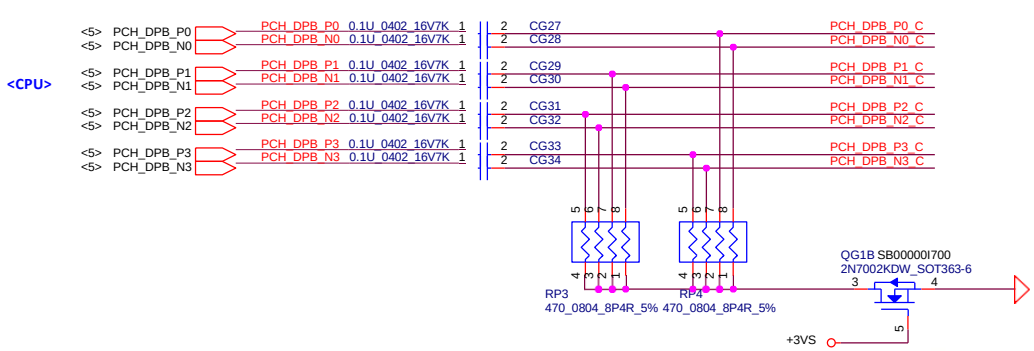
Compal Electronics, Inc.

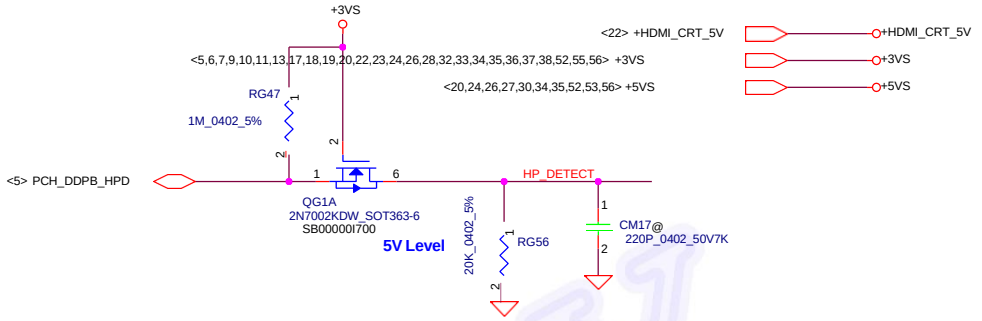
Title: *LVDS Translator-RTD2132N*

Size: Document Number: **LA-D707P** Rev: v0.2

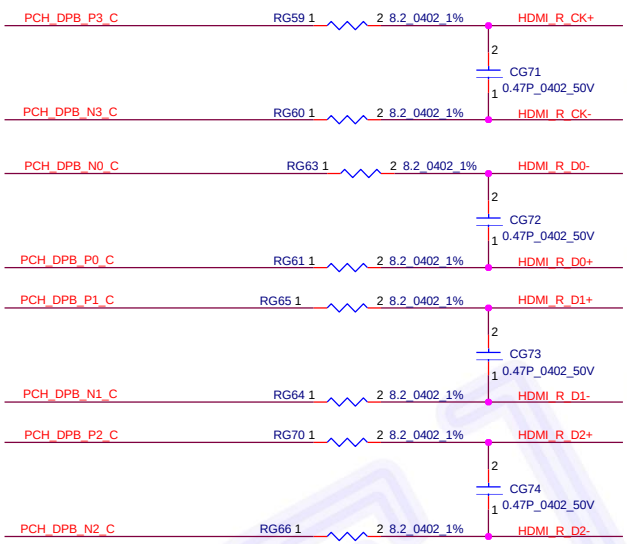
Date: Wednesday, May 11, 2016 Sheet 19 of 60


LVDS Power
<SI> change to standard par SA00006Y800 (Dif f erent f oot print)
W=60mils
SM010014520 3000ma
220ohm@100mhz
DCR 0.04
W=60mils
Main SA00006Y800
2nd SA00007U000
3rd SA000079400
Camera
LCD/LED PANEL Conn.
<DB>LA1/LA2 closed to Aduio codec
Touch Screen
<DB> for 5V/3V TS option
Touch Screen Power
<PV> Touch GPIO control by EC
Touch screen
Camera
Compal Secret Data
Compal Electronics, Inc.
LVDS Connector
LA-C707P
Issued Date 2013/02/26
Deciphered Date 2015/07/08
Wednesday, May 11, 2016

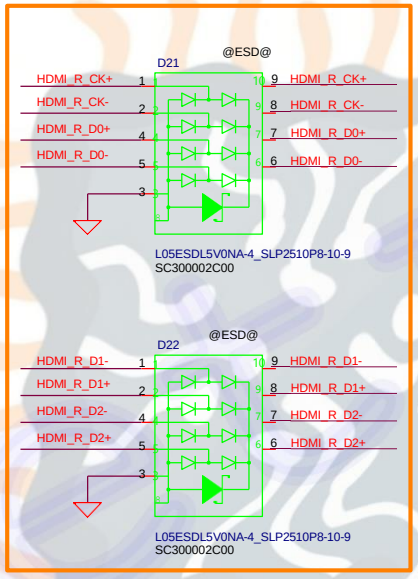


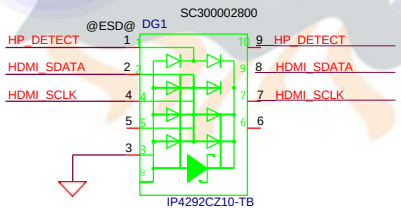


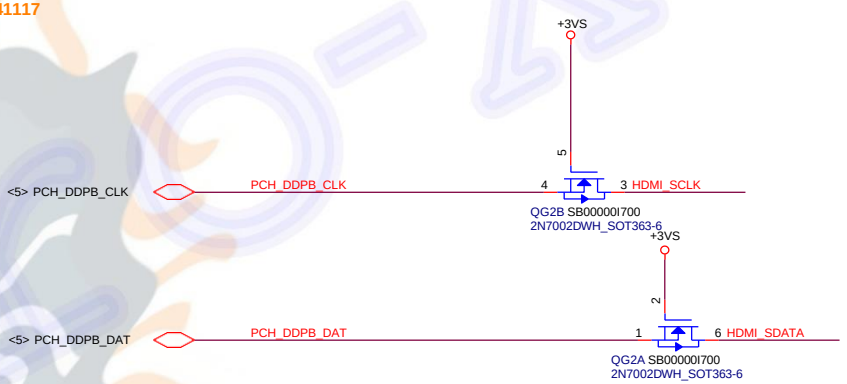
<Diner SI> change to 8.2 ohm and parallel 0.47p by EMI request
<PV> change to 10 ohm by EMI request
<DB> Delete Choke add parallel 150ohm

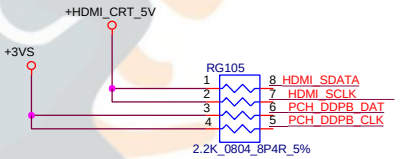


DB phase :
For ESD request
20141117

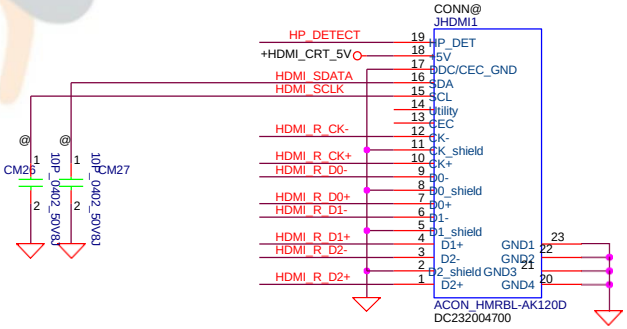








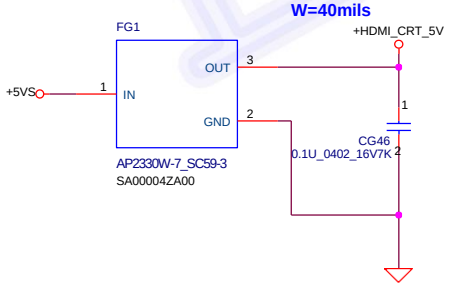
HDMI Conn.



HDMI Chock 2nd : SM070003K00

Layout notes
40 mils

W=40mils



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: HDMI Conn/Level shift

Size: Document Number: LA-D707P

Rev: 1.0

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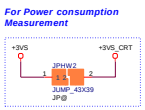
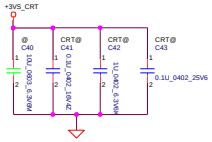
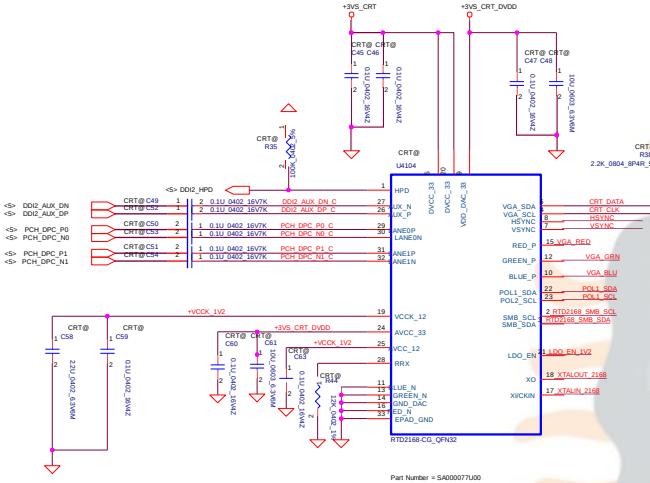
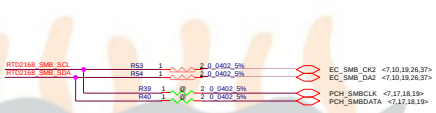
DP to CRT converter

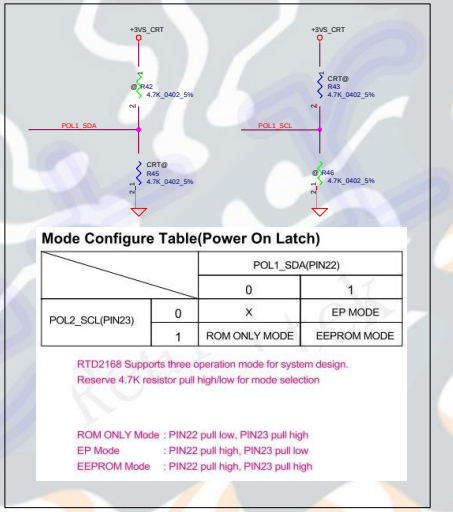






<SI> change to +HDMI_CRT_5V for SVTP test fail



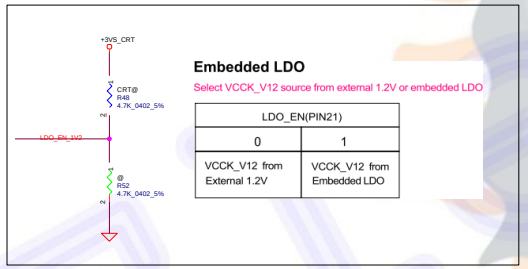


Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

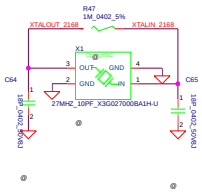
ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

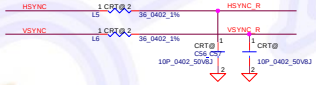


Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

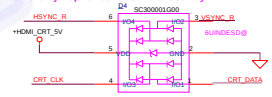
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

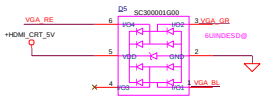




Layout notes
R61,R62,R58,R59 close to RTD2168
R55,R57,R60,R56 close to CONN

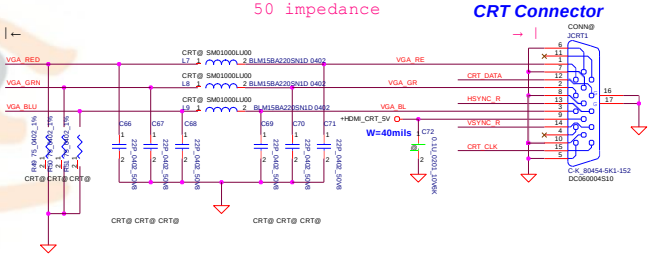
<KBL SI> Change ESD diode package
D4&D5 Only Pop for 6U SKU India Country





50 impedance

CRT Connector



Security Classification	Compall Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/18	Deciphered Date	2015/02/20
Title: DP to CRT RTD2168			
Size: Custom	Document Number: LA-D707P		Rev: v0.2
Date: Wednesday, May 11, 2016		Sheet 22 of 50	

+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

8/15 Change to LDO Mode

LDO mode	Switcing mode
LL1 SMT	@
CL21 SMT	@
LL2 @	SMT
CL8,CL23 @	SMT

CL13 & CL15 close UL1 Pin22
CL14 & CL27 close UL1 Pin30

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

Place CL11~CL12 close UL1 Pin 3,8

8151/8166 Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

0923 PV CNG from DP00 to E500

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

RTL8111G

EC control 08/17 Add 0ohm

SP050005L00 Footprint

Swap P/N 08/16

(SA000063500) 8166GSH 10/100
(SA000084T00) 8111HSH-CG Giga

2016-03-03:Change Single Source
(SP050008V00) 10/100
(SP050008Y00) Giga

11/18 modify vendor review results

11/15 change CONN.

11/17 reserver for ESD request

powe rail need to check

powe rail need to check

CR RTS5237S move to S/B

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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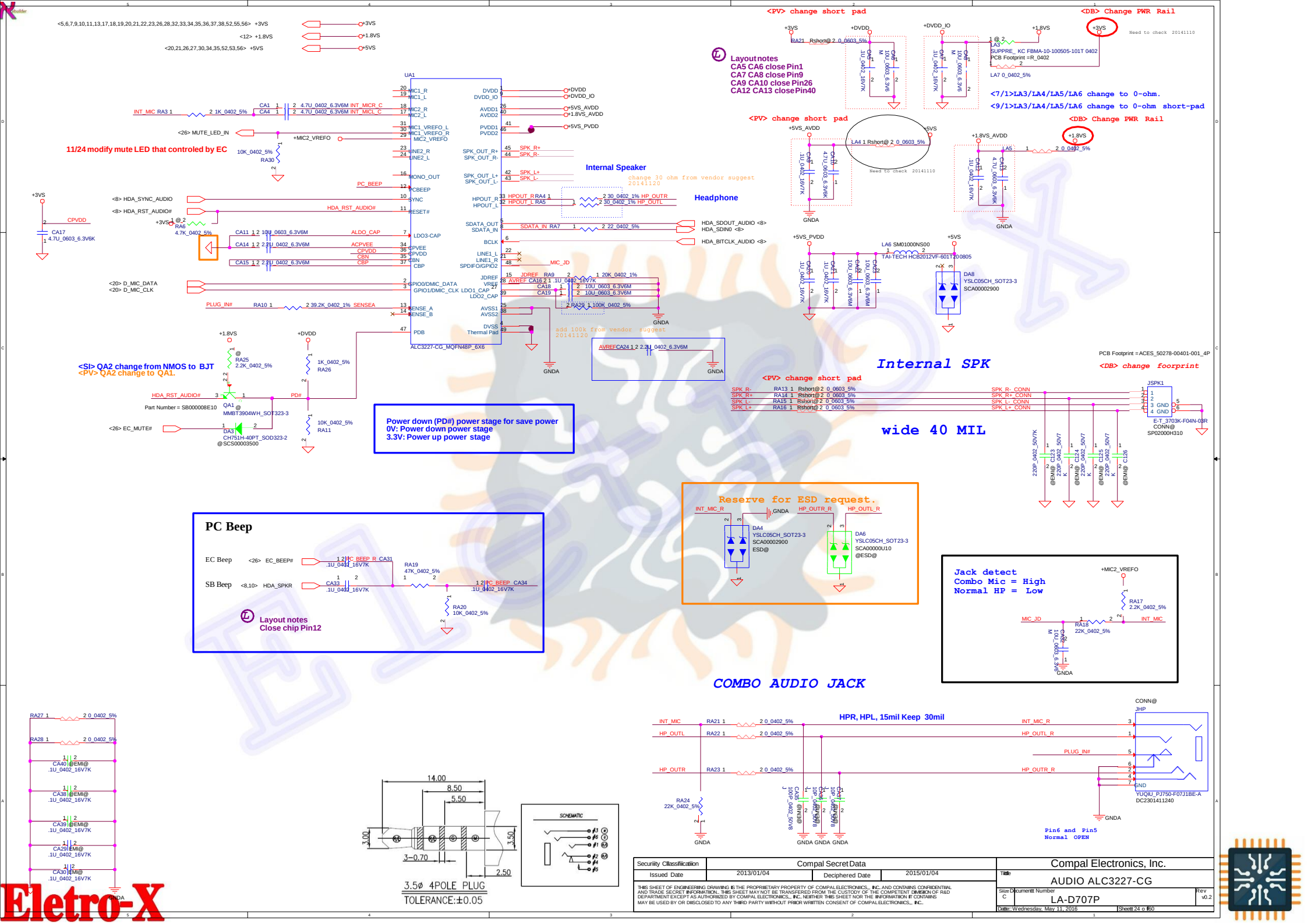
Compal Electronics, Inc.

Title: LAN 8151/8166_ CR RTS5238

Size: | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 23 of 50

Eletro-X


<PV> change short pad
<DB> Change PWR Rail
Layout notes
CA5 CA6 close Pin1
CA7 CA8 close Pin9
CA9 CA10 close Pin26
CA12 CA13 close Pin40
<7/1>LA3/LA4/LA5/LA6 change to 0-ohm.
<9/1>LA3/LA4/LA5/LA6 change to 0-ohm short-pad
11/24 modify mute LED that controled by EC
Internal Speaker
Headphone
change 30 ohm from vendor suggest 20141120
add 100k from vendor suggest 20141120
<SI> QA2 change from NMOS to BJT
<PV> QA2 change to QA1.
Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage
Internal SPK
wide 40 MIL
PCB Footprint = ACES_50278-00401-001_4P
<DB> change foorprint
Reserve for ESD request.
PC Beep
EC Beep
SB Beep
Layout notes
Close chip Pin12
Jack detect
Combo Mic = High
Normal HP = Low
COMBO AUDIO JACK
HPR, HPL, 15mil Keep 30mil
Pin6 and Pin5
Normal OPEN
3.5ø 4POLE PLUG
TOLERANCE:±0.05
SCHEMATIC
Compal Secret Data
Compal Electronics, Inc.
AUDIO ALC3227-CG
LA-D707P
2013/01/04
2015/01/04
Wednesday, May 11, 2016

EC Board ID (UMA, Dis, phase) control table

RK4	DB	SI	PV	MV	Note
UMA	15Kohm	27Kohm	43Kohm	75Kohm	
Dis	20Kohm	33Kohm	56Kohm	100Kohm	

Current

DB_UMA_15kohm:SD034150280, 5 RES 1/16W 15K +-1% 0402
DB_DIS_20kohm:SD034200280, 5 RES 1/16W 20K +-1% 0402

SI_UMA_27kohm:SD034270280, 5 RES 1/16W 27K +-1% 0402
SI_DIS_33kohm:SD034330280, 5 RES 1/16W 33K +-1% 0402

PV_UMA_43kohm:SD034430280, 5 RES 1/16W 43K +-1% 0402
PV_DIS_56kohm:SD034560280, 5 RES 1/16W 56K+-1%0402

MV_UMA_75kohm:SD034750280, 5 RES 1/16W 75K +-1% 0402
MV_DIS_100kohm:SD034100380, 5 RES 1/16W 100K +-1% 0402

Board ID control

<PV> change short pad

<SI> un-mount RC , Internal PU in 9022

Reserve EC_CLR_CMOS for clear CMOS
(2016-03-04 : Confirm intel platform not support EC Clear CMOS function)

<SI> EC request to add RK9

PWM Output

AD Input

DA Output

PS2 Interface

Int. K/B Matrix

SPI Device Interface

SPI Flash ROM

GPIO

SM Bus

GPIO

GPI

PC & MISC

UK1 KB9022QD_LQFP128_14X14

20mil

LK1 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402

LK2 TAI-TECH HCB1005KF-221T15 0402

<DB> for leakage of LED light

For Solve tPCH04(Min 9ms) Sequence Timing

2014-11-13:
Pin16 from MINI1_LED# to PM_SLP_SUS#
Pin29 from PM_SLP_SUS# remove
Pin25 from EC_INVT_PWM remove
Pin19 from EC_+1.05VS_PG to GPU_HOT#
Pin21 from GPU_HOT# to EC_+1.05VS_PG
Pin25 from EC_INVT_PWM remove
Pin122 from GPU_THERMAL_DET# to PBTN_OUT#
Pin123 from X to PM_SLP_S4#
Pin18 remove
Pin36 remove no support USB CHR

2014-11-13:
Pin64 from BOARD_ID to X no support KBL
Pin66 from X to BOARD_ID
Pin76 Pin97 swap
Pin84 from PM_SLP_S4# to USB_ON#
Pin68 from +1.05V_VS_PG_PWR to MINI1_LED#
Pin70 NC, no support
Pin72 NC, no support
Pin86 NC , no support

2014-11-18
Pin108 from USB_ON# to +1.05V_VS_PG_PWR
Pin106 NC, no support
2014-11-18
Pin108 from +1.05V_VS_PG_PWR to VGA_AC_BATT
2014-11-24
Pin108 from VGA_AC_BATT to 1.05V_VS_PG_PWR

2014-11-25
Reserve for co-lay Nuvoton NPCE388N

CC128 RC369 place near EC Side

EMI request

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

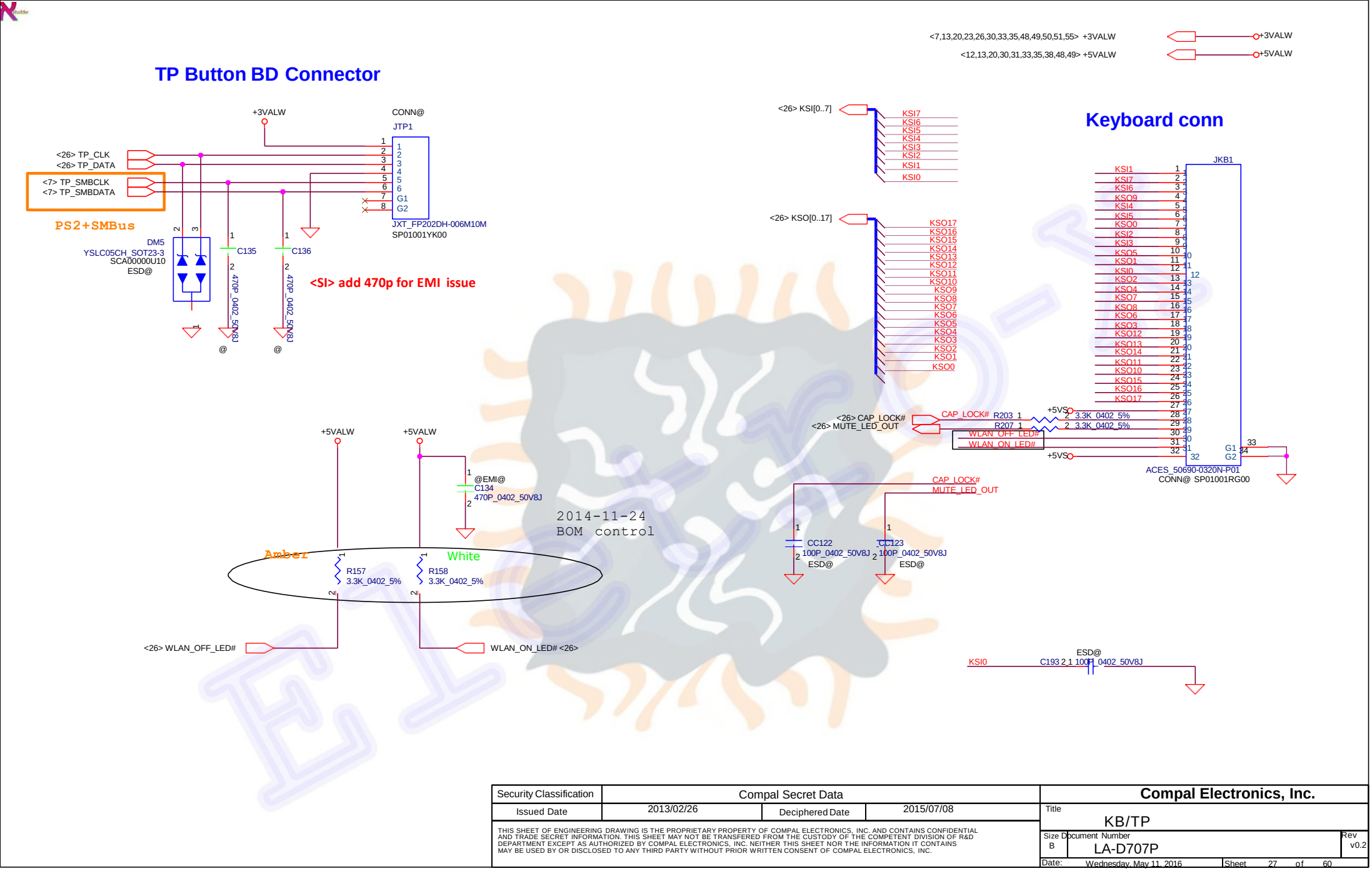
Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 26 of 1

Eletro-X



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

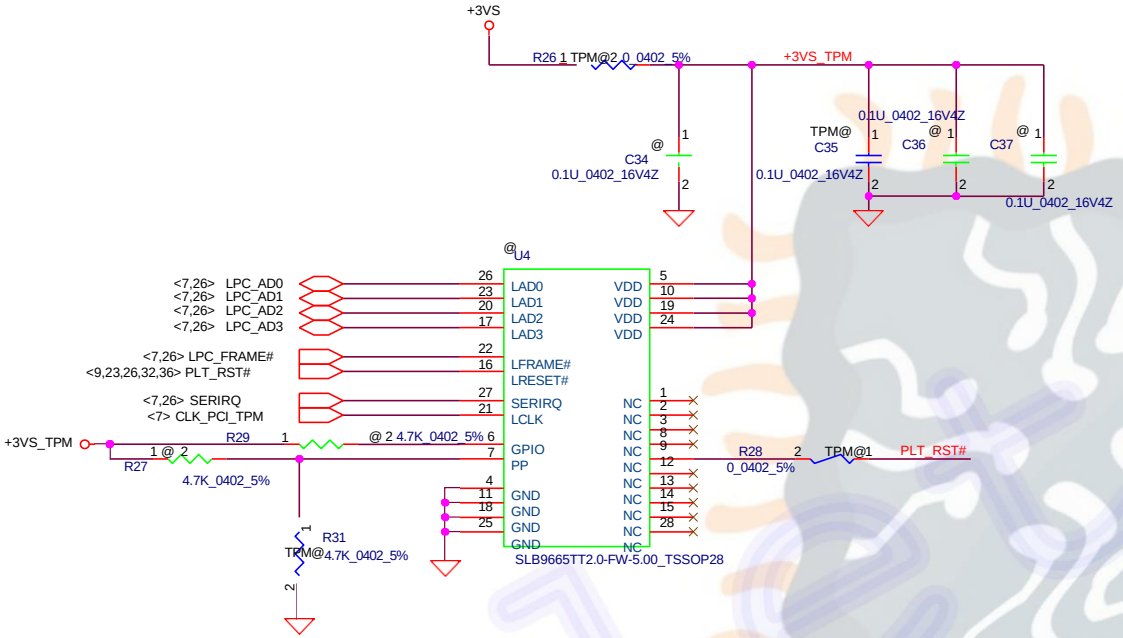
Compal Electronics, Inc.

Title: KB/TP

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 27 of 60

TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

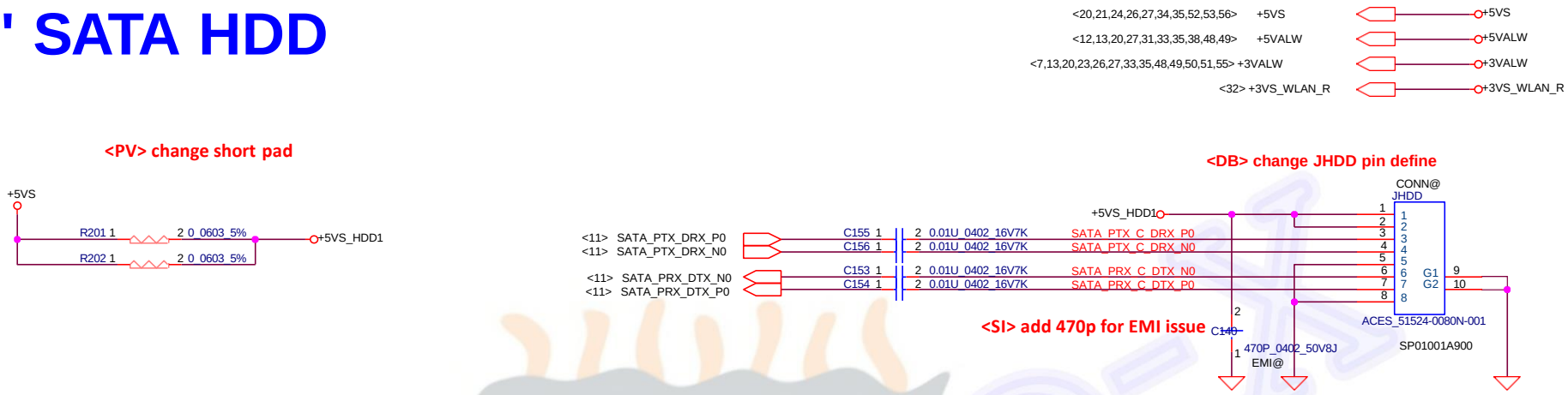
Compal Electronics, Inc.

Title: **TPM/Screw**

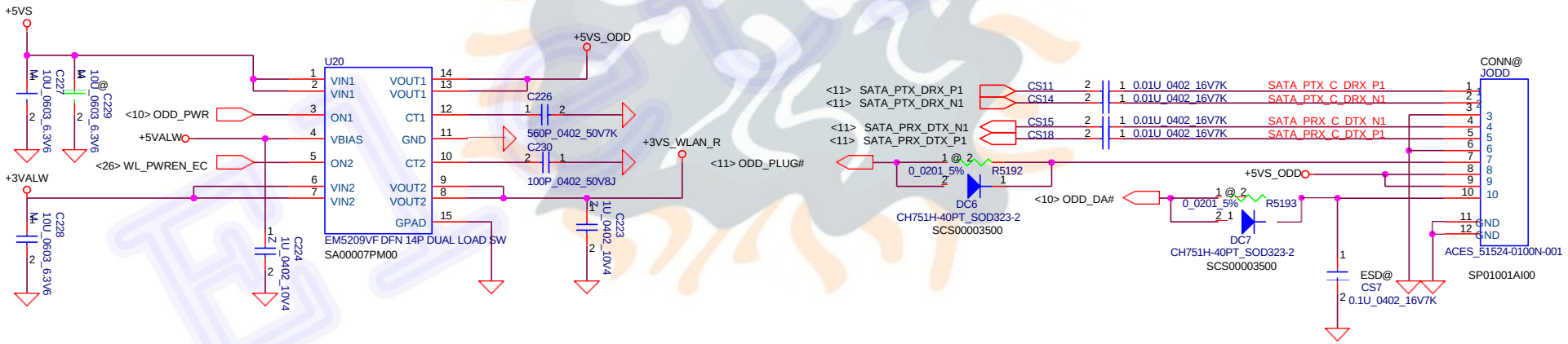
Size: Document Number: LA-D707P Rev: v0.2

Date: Wednesday, May 11, 2016 Sheet 28 of 60

2.5" SATA HDD



2.5" SATA ODD



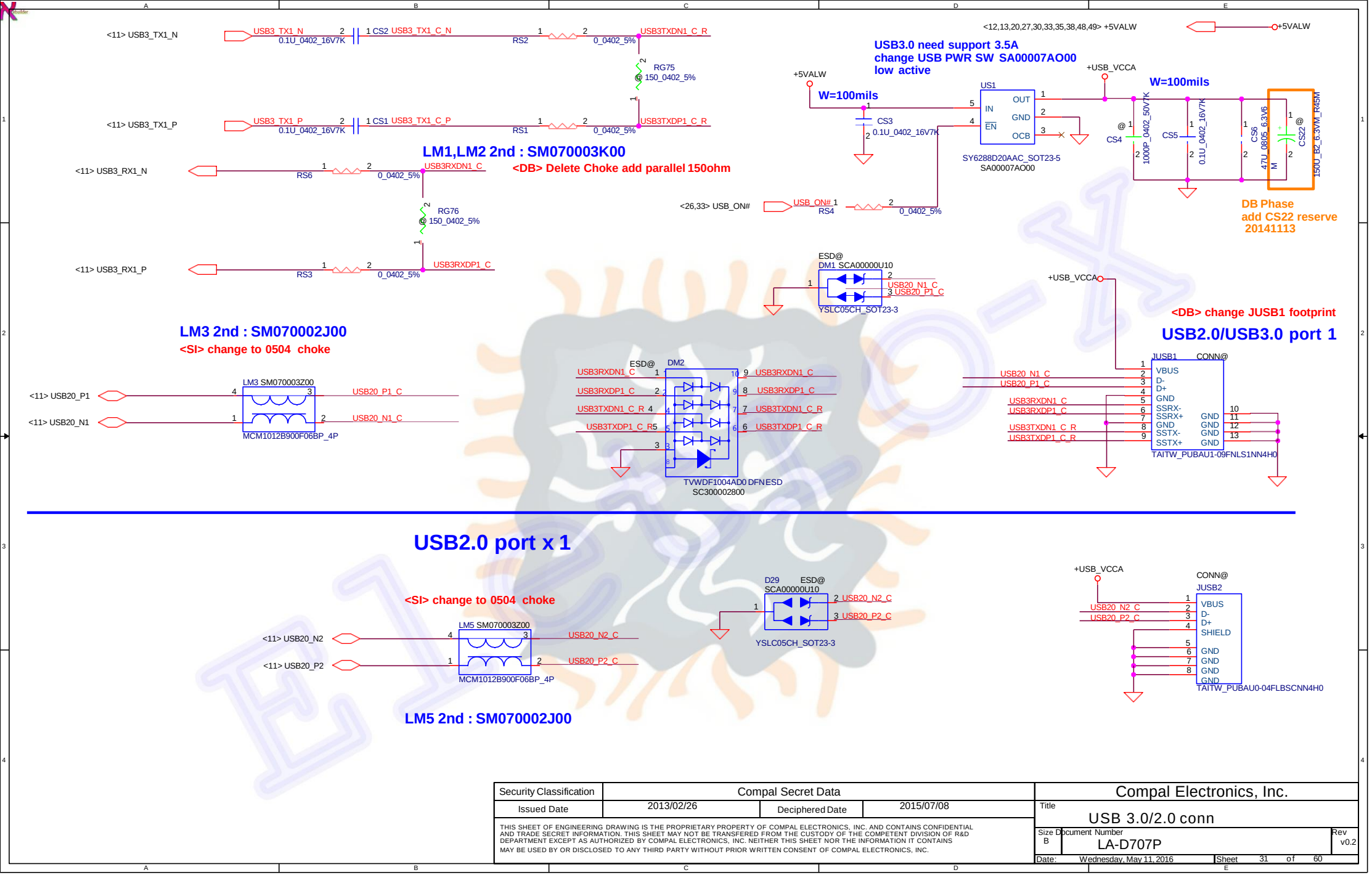
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: HDD/ODD Conn

Size: B | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 30 of 60



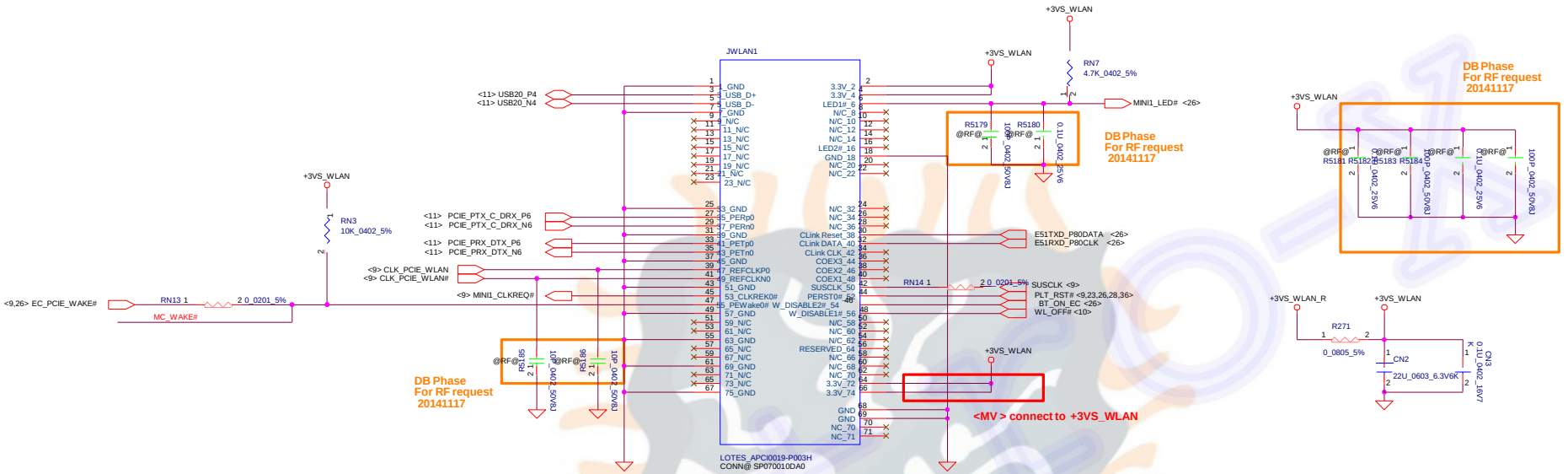
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

Size	Document Number	Rev
B	LA-D707P	v0.2

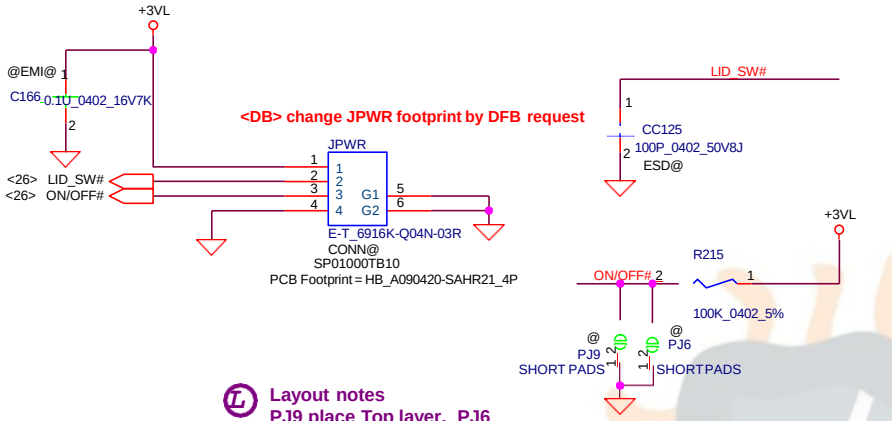
Date: Wednesday, May 11, 2016 Sheet 31 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title: WLAN-BT			
Size:	Document Number: LA-D707P		Rev: v0.2
Date: Wednesday, May 11, 2016		Sheet: 32 of	60

Powert Button Connector

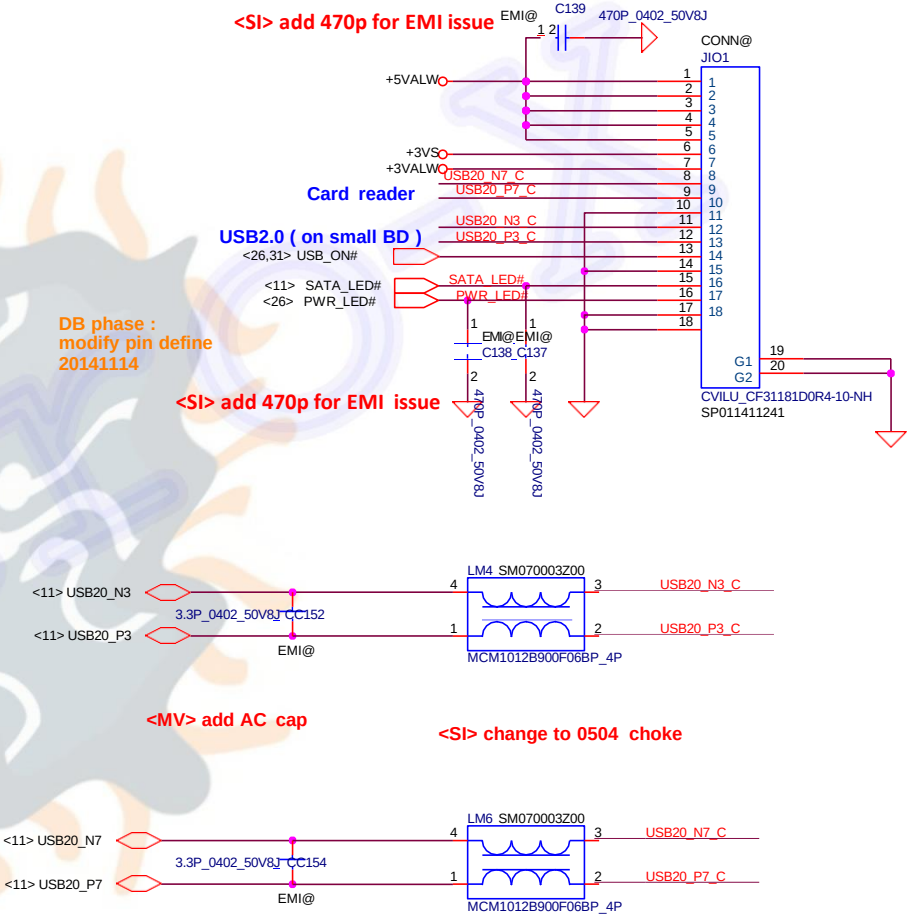


Layout notes
PJ9 place Top layer, PJ6 place Bottom layer

<13,26,46,47,48> +3VL
<12,13,20,27,30,31,35,38,48,49> +5VALW
<5,6,7,9,10,11,13,17,18,19,20,21,22,23,24,26,28,32,34,35,36,37,38,52,55,56> +3VS
<7,13,20,23,26,27,30,35,48,49,50,51,55> +3VALW

11/26 change CONN.

IO BD Connector (USB2.0,Card reader,HDD & PWR LED)



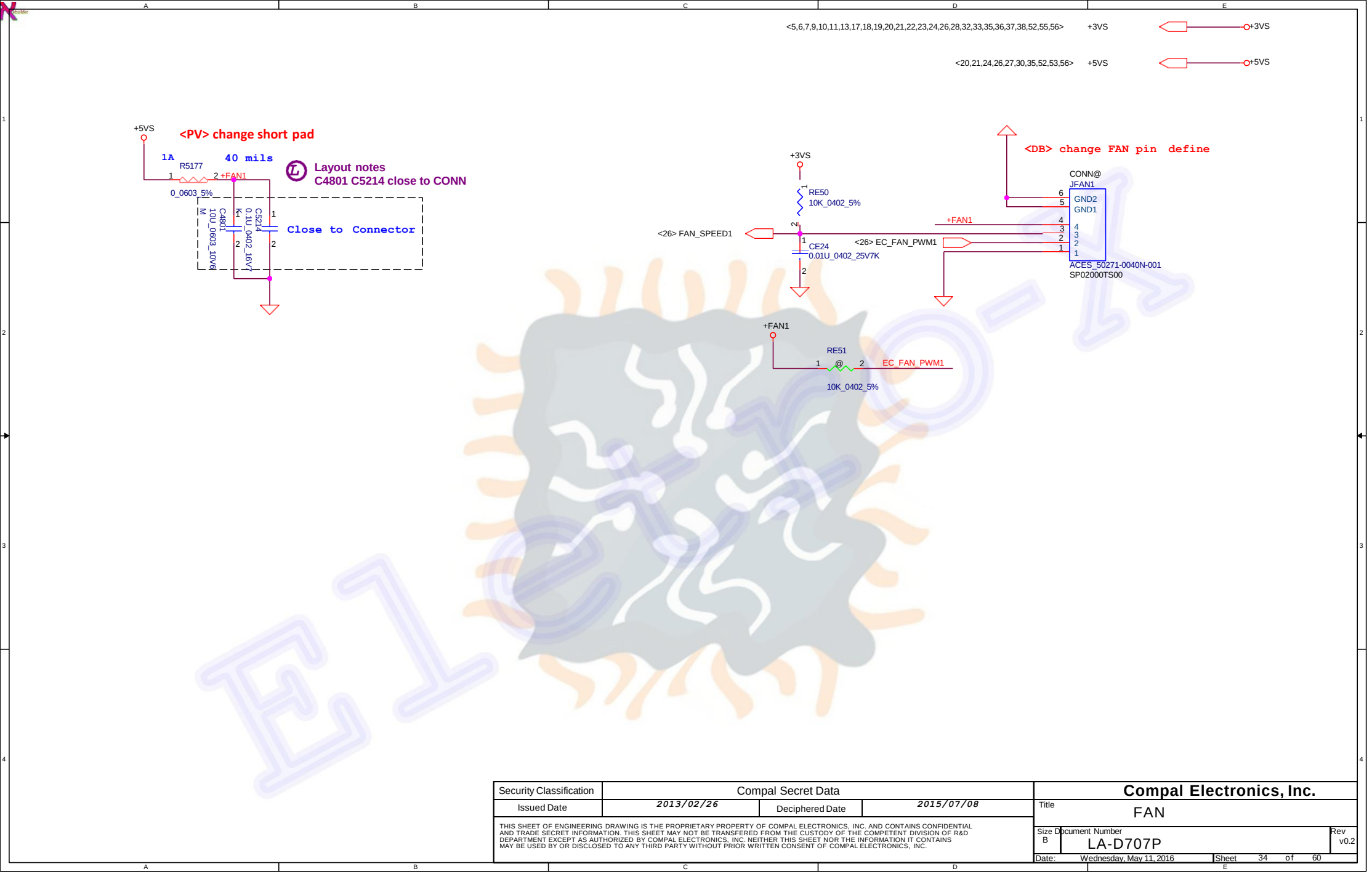
<MV> add AC cap

<SI> change to 0504 choke

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

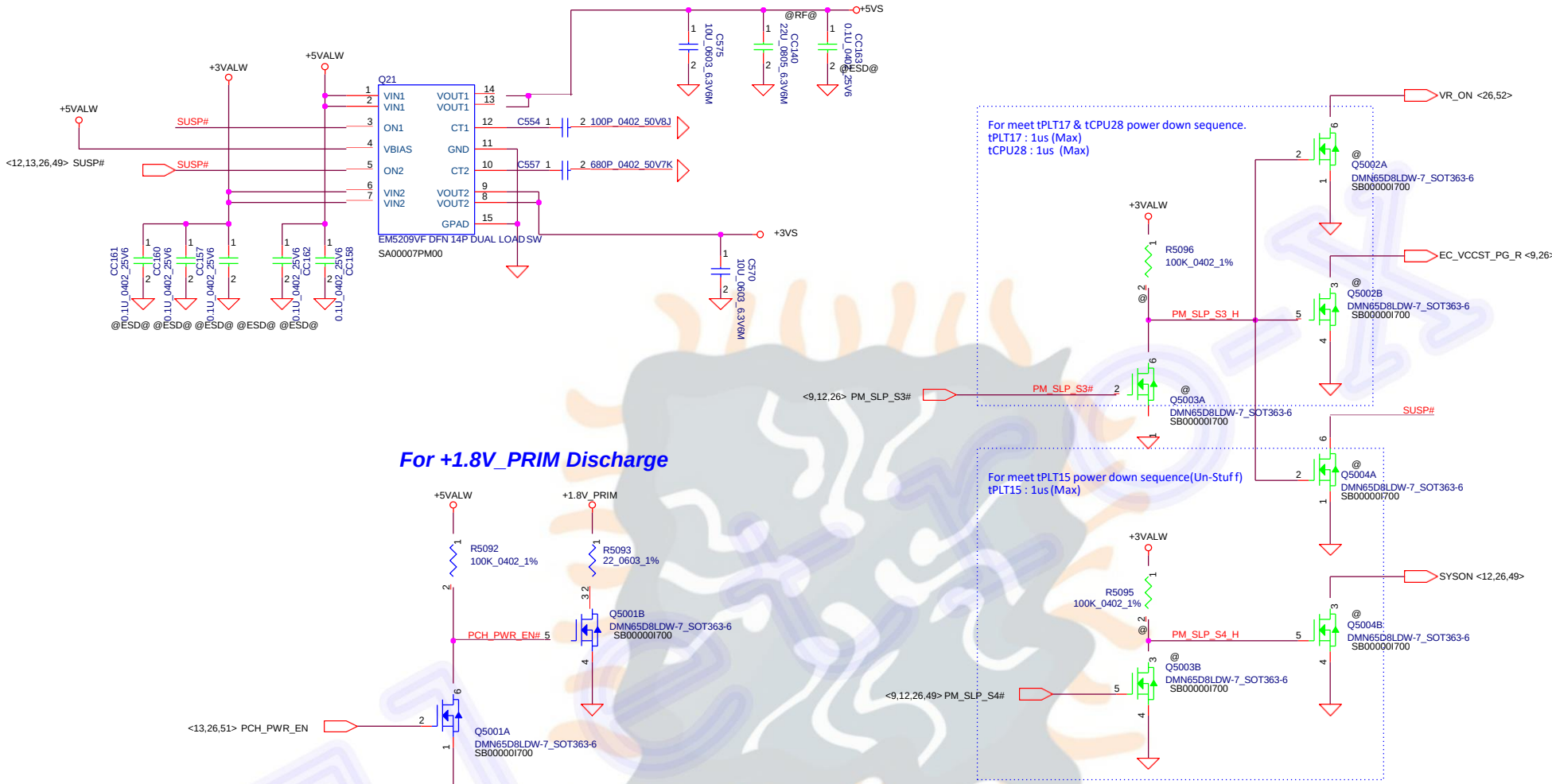
Title	IO CON	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 33 of 60	



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

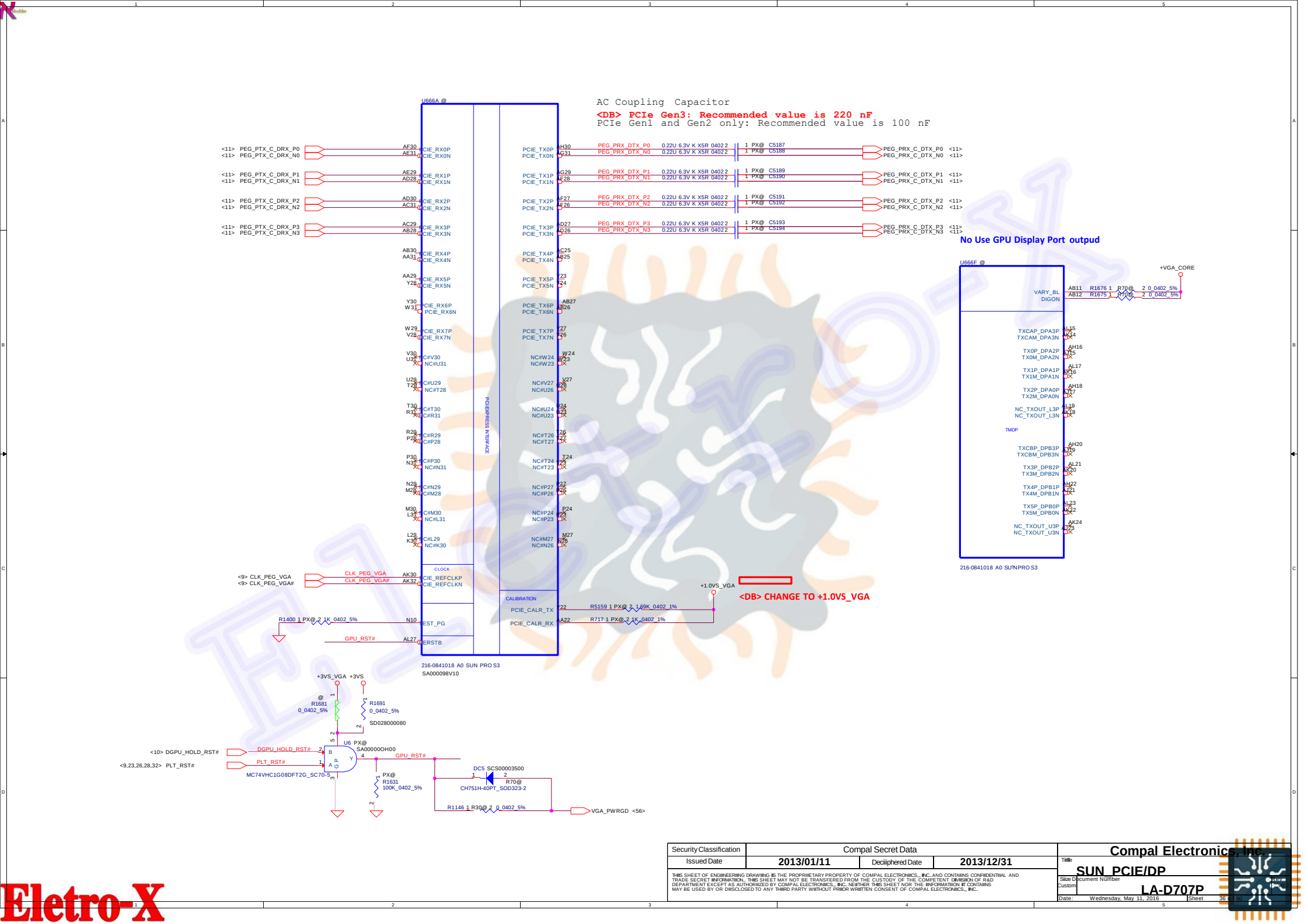
Title	FAN	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 34 of 60	



Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title	DC Interface		
Size	Document Number		Rev
Custom	LA-D707P		1.0
Date:	Wednesday, May 11, 2016	Sheet	35 of 60



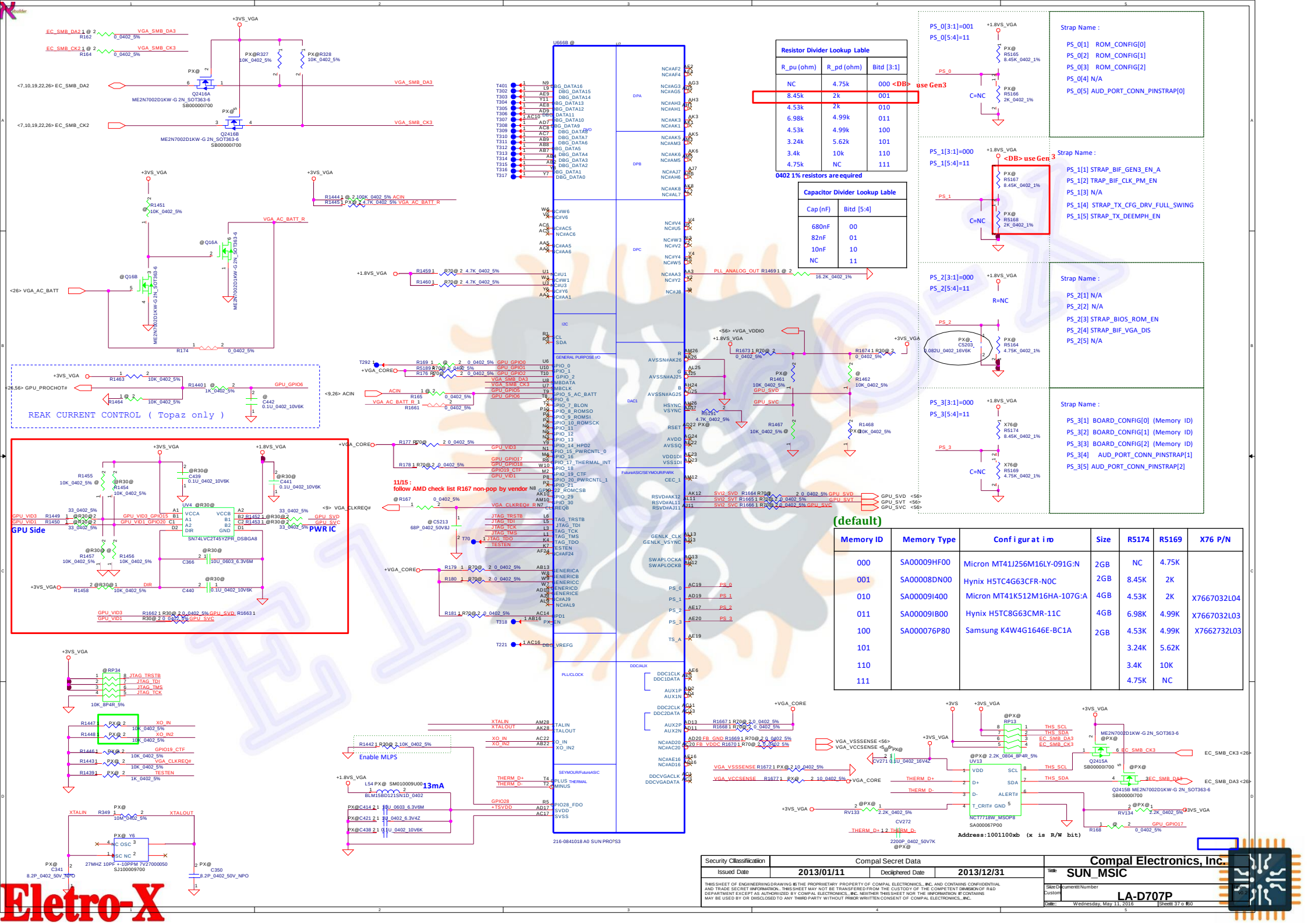
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciliphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_PCIE/DP

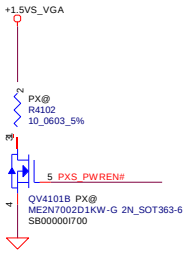
Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet: 35 of 60


Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000 <DB> use Gen3
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
<DB> use Gen3
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
REAK CURRENT CONTROL (Topaz only)
GPU Side
PWR IC
11/15 :
follow AMD check list R167 non-pop by vendor
(default)
Memory ID | Memory Type | Configuration | Size | R5174 | R5169 | X76 P/N
000 | SA00009HF00 | Micron MT41J256M16LY-091G:N | 2GB | NC | 4.75K |
001 | SA00008DN00 | Hynix H5TC4G63CFR-N0C | 2GB | 8.45K | 2K |
010 | SA00009I400 | Micron MT41K512M16HA-107G:A | 4GB | 4.53K | 2K | X7667032L04
011 | SA00009IB00 | Hynix H5TC8G63CMR-11C | 4GB | 6.98K | 4.99K | X7667032L03
100 | SA000076P80 | Samsung K4W4G1646E-BC1A | 2GB | 4.53K | 4.99K | X7662732L03
101 | | | | 3.24K | 5.62K |
110 | | | | 3.4K | 10K |
111 | | | | 4.75K | NC |
13mA
Enable MLPS
Address:1001100xb (x is R/W bit)
216-0841018 A0 SUN PRO?S3
Security Classification | Compal Secret Data
Issued Date | 2013/01/11 | Deciphered Date | 2013/12/31
Compal Electronics, Inc.
SUN_MSIC
LA-D707P
Wednesday, May 11, 2016
Sheet 37 of 60
Eletro-X

+1.5VS to +1.5VS_VGA (2.096A)

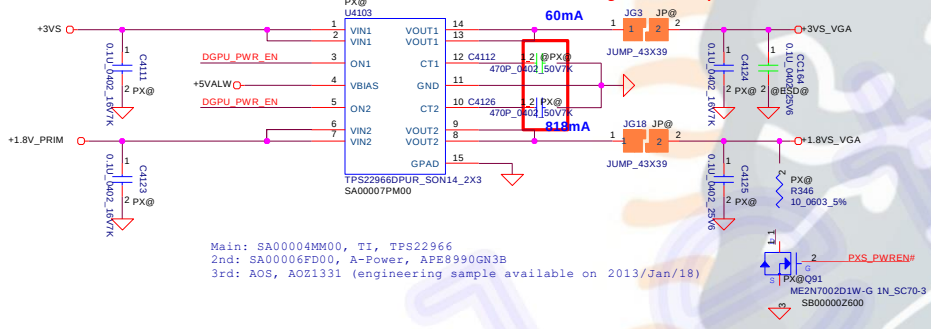
Delete +1.5VS to +1.5VS_VGA power switch



+3VS to +3VS_VGA (25mA)

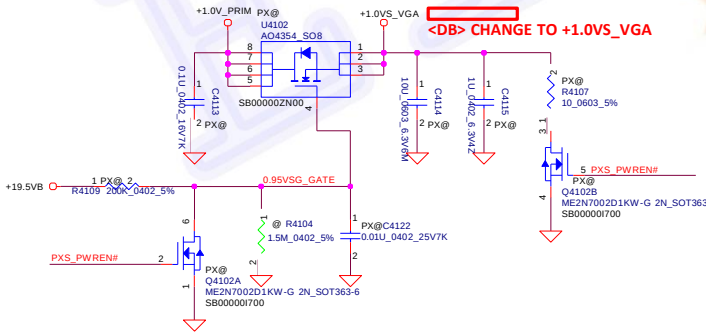
+1.8V_PRIM to +1.8VS_VGA (311mA)

<Diner SI> change to NC & 470p



Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

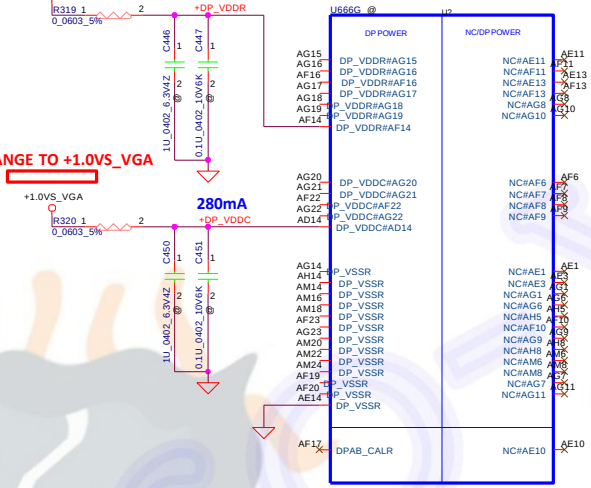
+1.0V_PRIM to +1.0VS_VGA (4.016A)

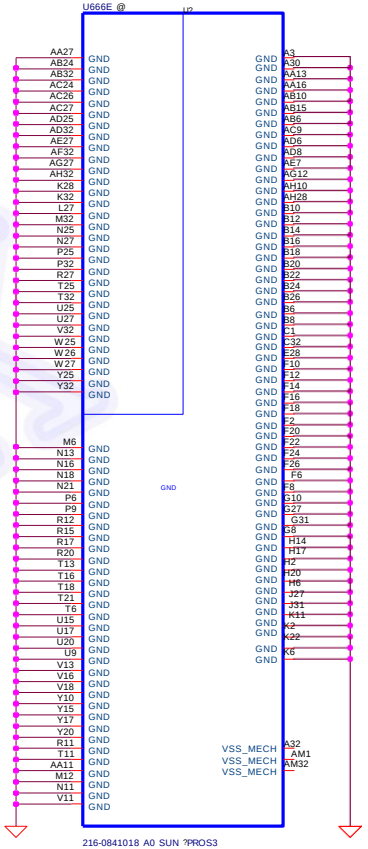


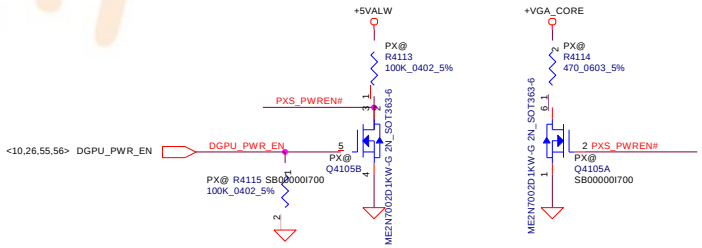
370mA (HDMI) 188mA (Display Port) No Use GPU Display Port outpud

<DB> CHANGE TO +1.0VS_VGA

280mA







Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciliphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-D707P

Date: Wednesday, May 11, 2016 | Sheet

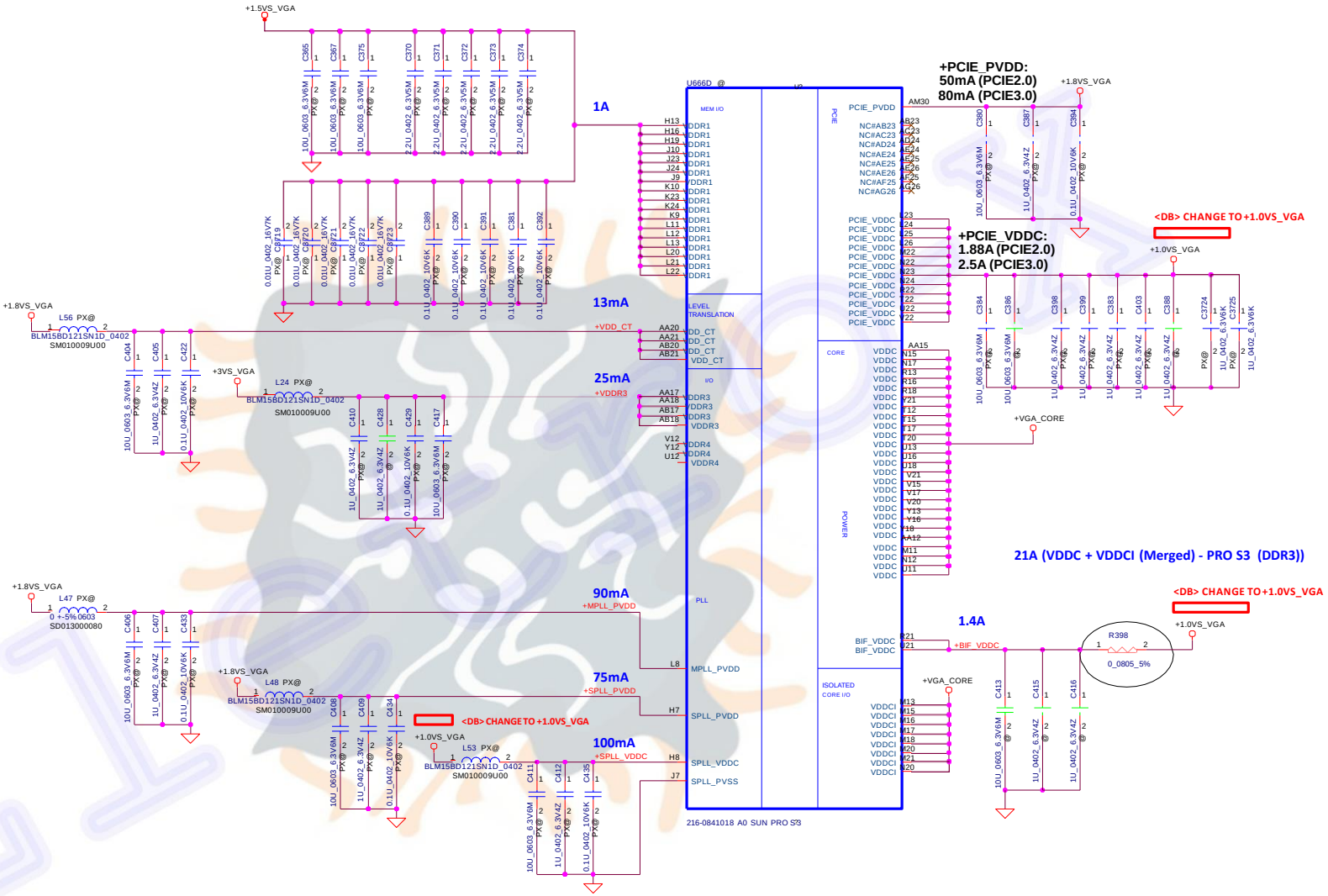
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+1.0VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



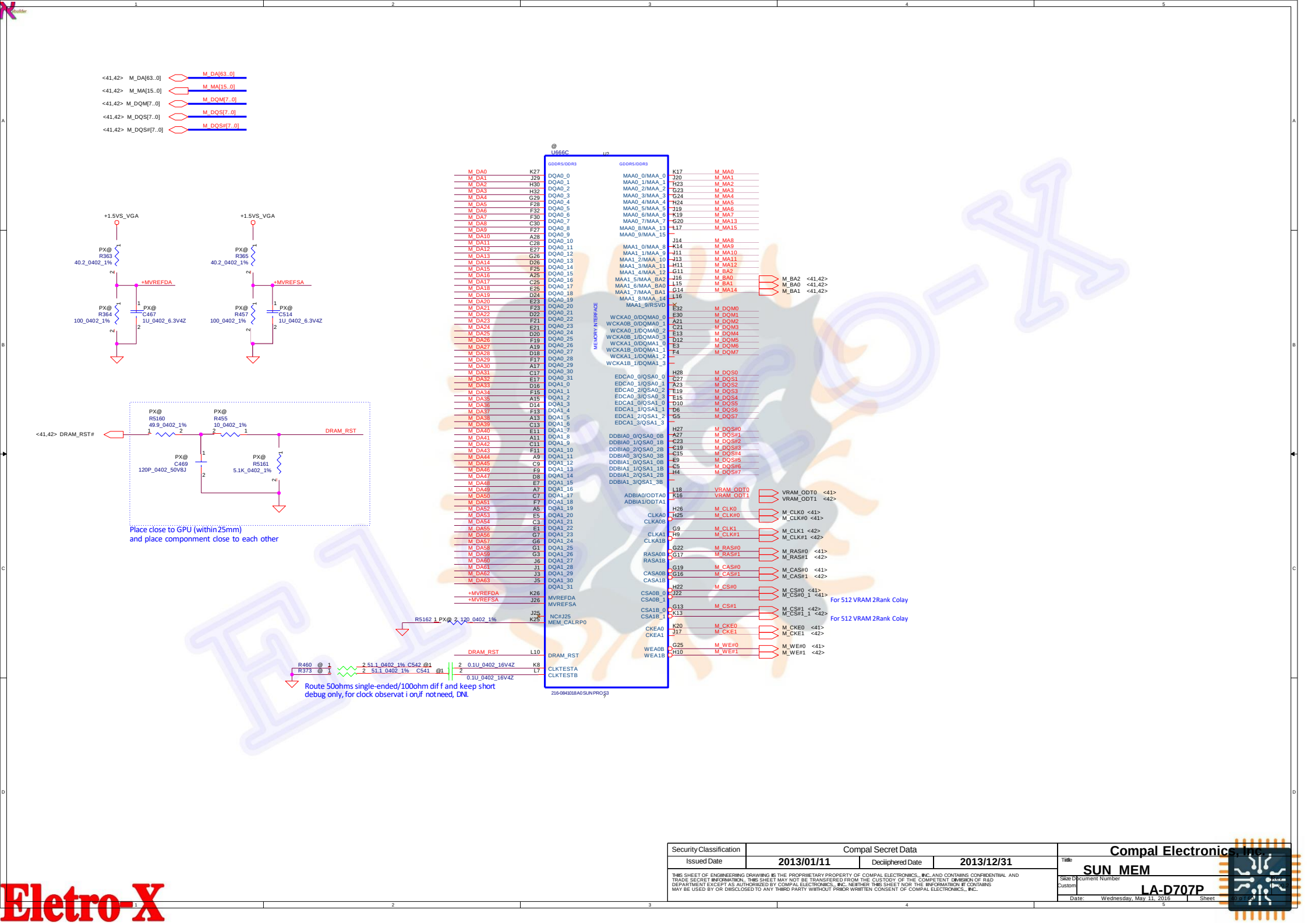
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciliphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet: 39 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciiphered Date	2013/12/31

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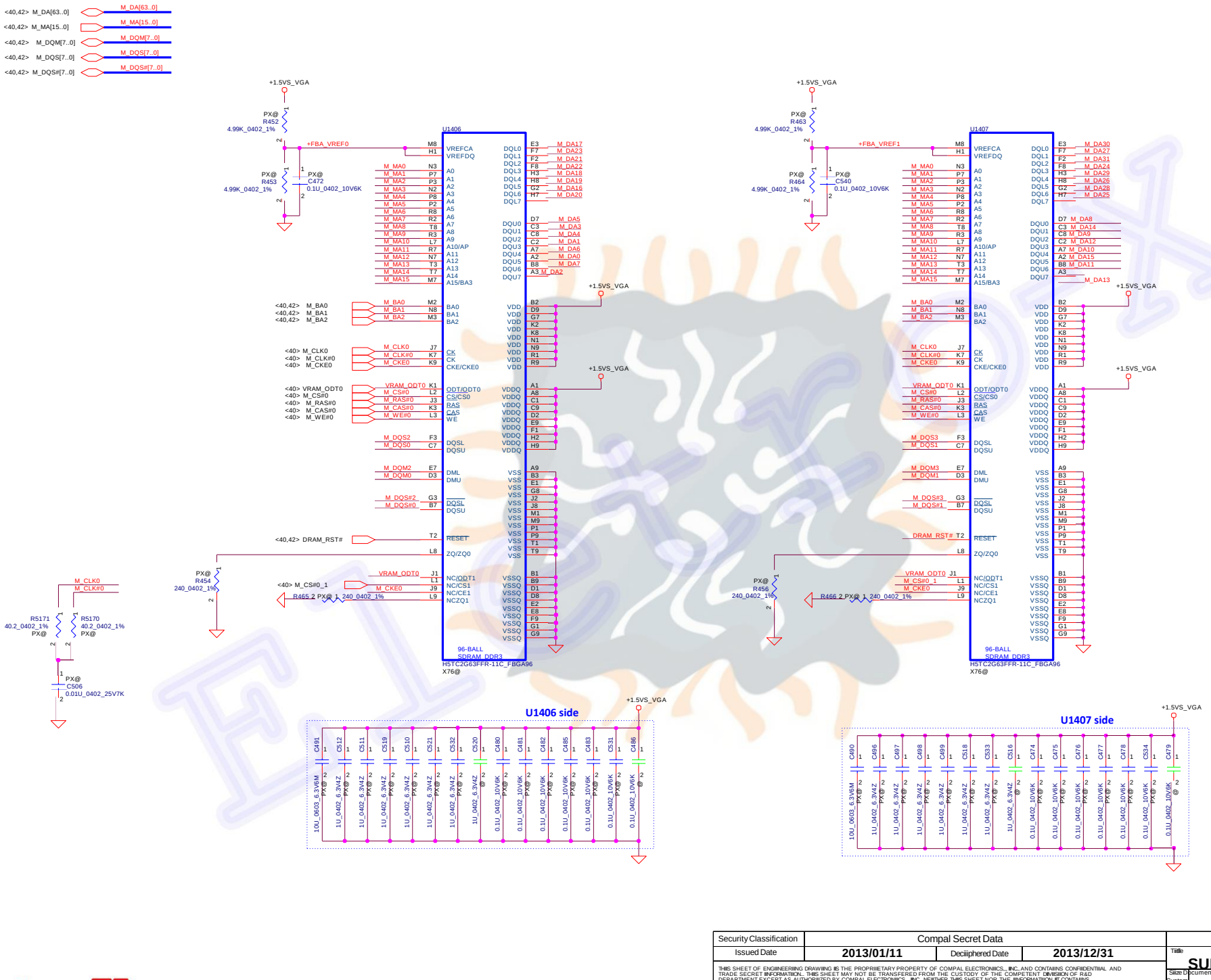
Title: **SUN_MEM**

Size: Custom | Document Number: **LA-D707P** | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet: 40 of 50

Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciliphered Date	2013/12/31

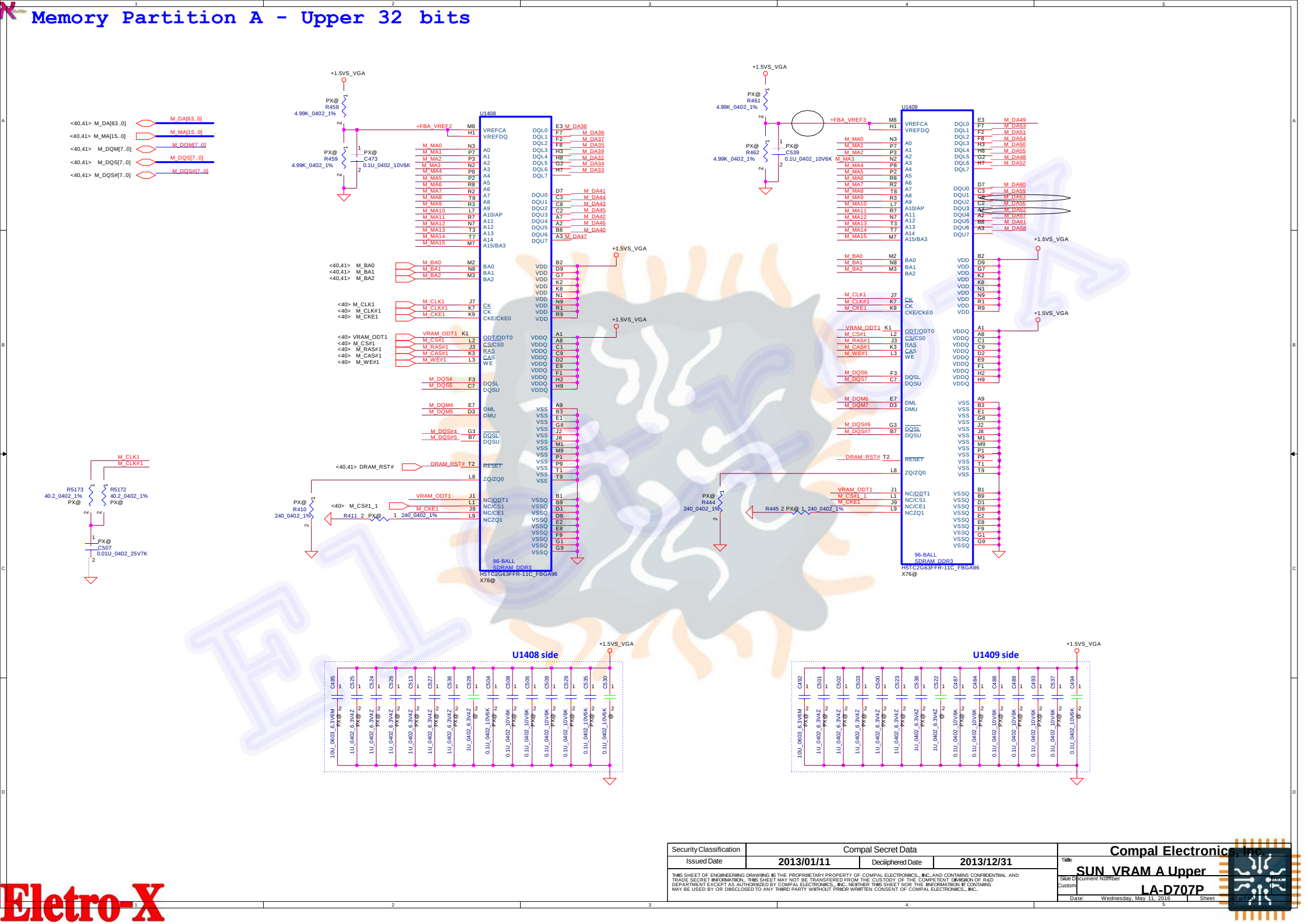
Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: Custom | Document Number: LA-D707P

Date: Wednesday, May 11, 2016 | Sheet: 1 of 1

Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciliphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_VRAM A Upper

Size: Custom | Document Number: LA-D707P

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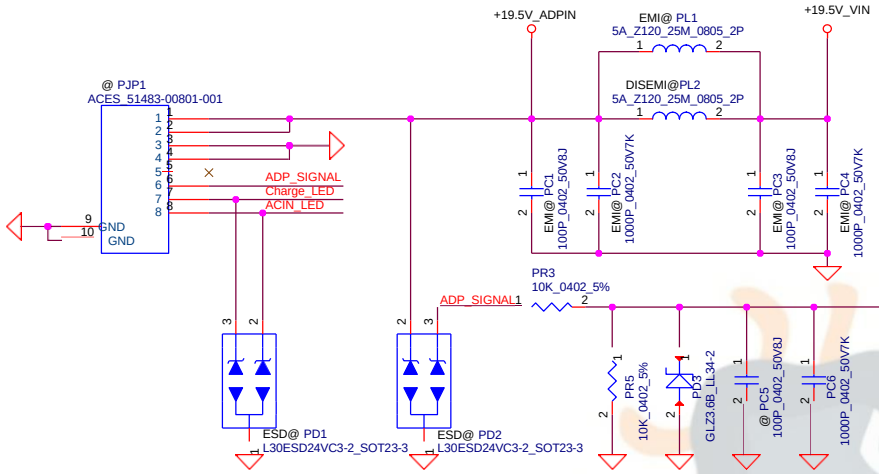
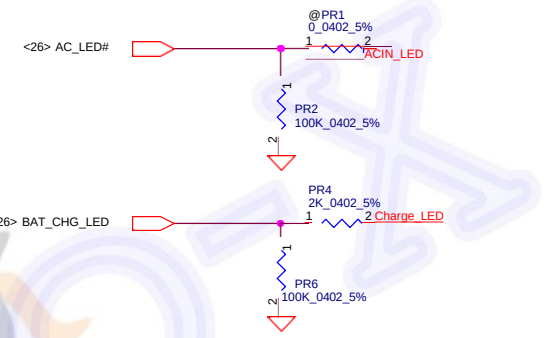
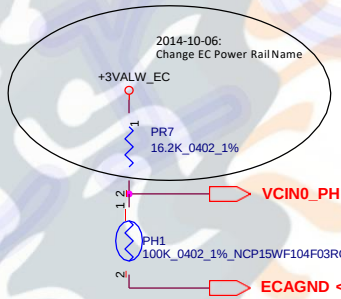
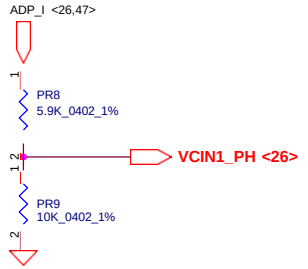




ADP_ID			
Adapter Type		Voltage Range (Dec)	Voltage Range (Hex)
None	Normal Adapter	<0.211V	< 10
	Air-Line Apdater	<0.334V	< 1A
40W	Normal Adapter	>=0.211V ;<0.349V	>= 10 < 1A
45W	Normal Adapter	>=0.349 ;<0.442	>= 1A < 20
65W	Normal Adapter	>=0.442V ;<0.549V	>=20 <2A
	Air-Line Apdater	>=0.334V ;<0.425V	>= 1A < 21
90W	Normal Adapter	>=0.549V ;<0.710V	>= 2A < 36
	Air-Line Apdater	>=0.425 ;<1.391V	>= 21 < 6A
120W	Normal Adapter	>=0.710V ;<1.391V	>= 36 < 6A
ID is shorted to VIN		>=1.391V with Normal and Air-Line	>= 6A





	Initail	Recovery
OTP	92 C	56 C

	Initail	Recovery
45W UMA	0.65V	0.45V
65W DIS	0.95V	0.67V

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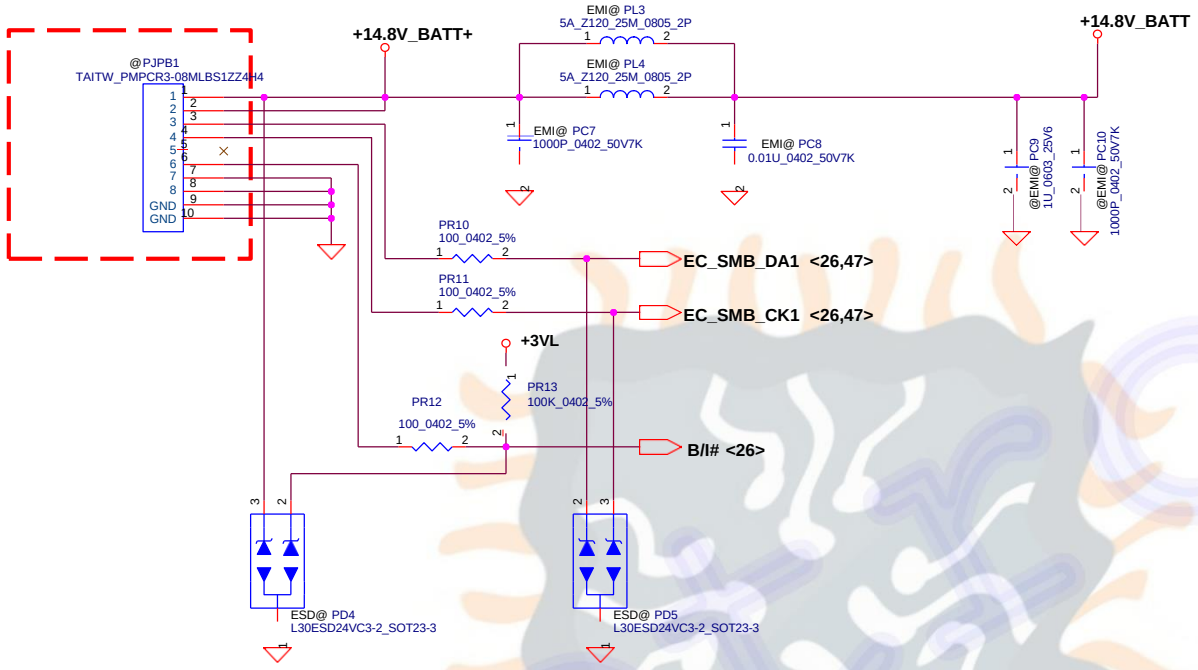
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Title	DC Conn		
Size	Document Number	LA-D707P	Rev 1.0
Date:	Wednesday, May 11, 2016	Sheet 45 of	



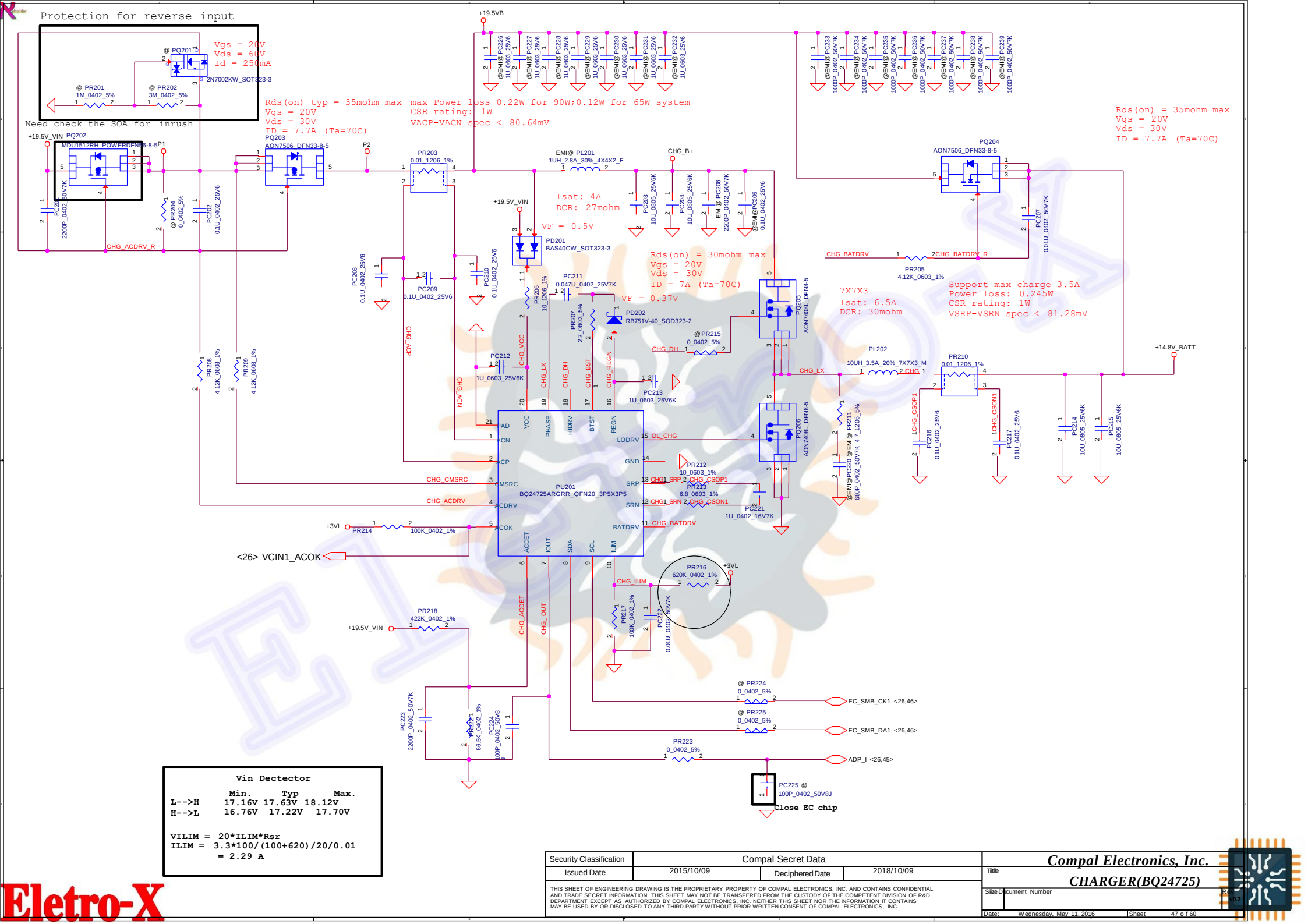
Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-D707P** | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 46 of


Protection for reverse input
Vgs = 20V
Vds = 60V
Id = 250mA
Need check the SOA for inrush
Rds(on) typ = 35mohm max max Power loss 0.22W for 90W;0.12W for 65W system
Vgs = 20V
Vds = 30V
CSR rating: 1W
ID = 7.7A (Ta=70C)
VACP-VACN spec < 80.64mV
Isat: 4A
DCR: 27mohm
VF = 0.5V
Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)
VF = 0.37V
Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
7X7X3
Isat: 6.5A
DCR: 30mohm
Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV
BQ24725ARGRR_QFN20_3P5X3P5
<26> VCIN1_ACOK
EC_SMB_CK1 <26,46>
EC_SMB_DA1 <26,46>
ADP_I <26,45>
Close EC chip
Vin Dectector
Min. Typ Max.
L-->H 17.16V 17.63V 18.12V
H-->L 16.76V 17.22V 17.70V
VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.01
= 2.29 A
Security Classification
Compal Secret Data
Issued Date
2015/10/09
Deciphered Date
2018/10/09
Compal Electronics, Inc.
CHARGER(BQ24725)
Date: Wednesday, May 11, 2016
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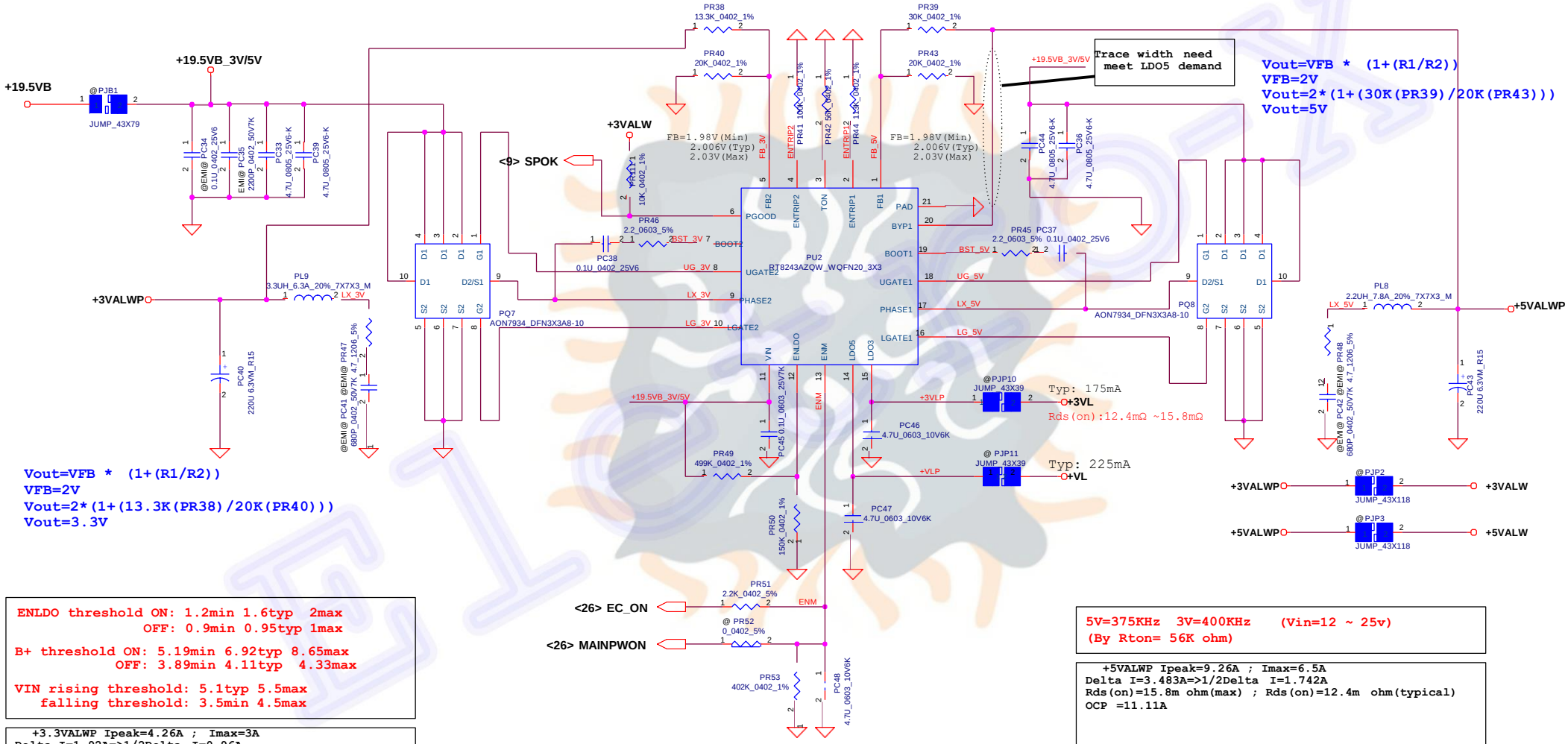
Module model information

RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.92A=>1/2Delta I=0.96A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP = 5.1A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W Δ T:12°C
L-MOS PD:0.2713W Δ T:7.9°C
Choke PD:1.5158W Δ T:24°C
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=3.483A=>1/2Delta I=1.742A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP =11.11A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W Δ T:13.4°C
L-MOS PD:0.3442W Δ T:10°C
Choke PD:1.9613W Δ T:30°C
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-D707P | Rev: 0.2

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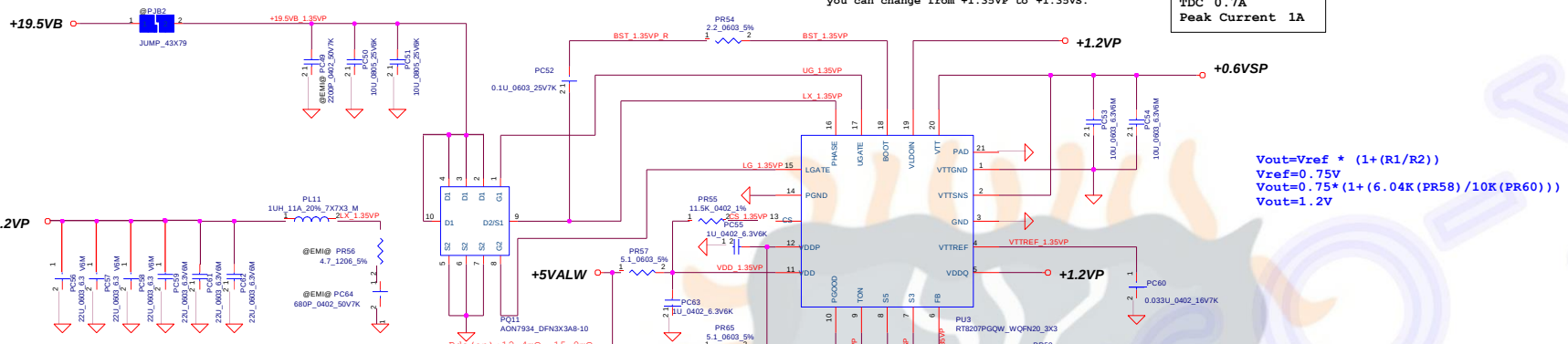
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Vout=Vref * (1+(R1/R2))
Vref=0.75V
Vout=0.75*(1+(6.04K(PR58)/10K(PR60)))
Vout=1.2V

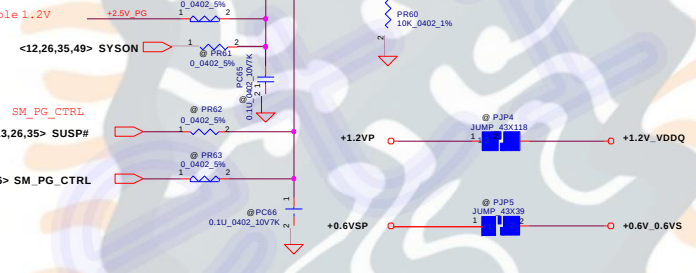
+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)

OCP = 8.88

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp=13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V

2.5V PG Enable 1.2V



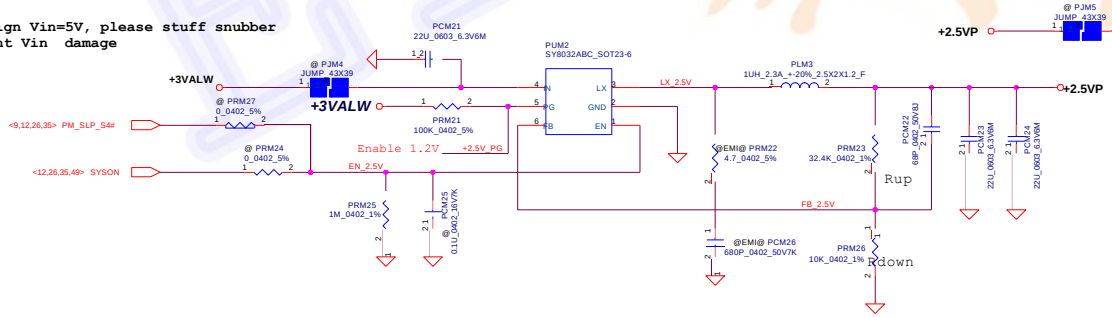
Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information

SY8032_V2.mdd

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage



Vout=0.6V * (1+(R1/R2))
Vout=0.6*(1+(32.4K(PRM23)/10K(PRM26)))
Vout=2.5V

Imax= 2A, Ipeak= 3A
FB=0.6V

Vout=0.6V* (1+Rup/Rdown)

Securiiity Cllassiificatiion	Compal Secret Data		
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Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5VP(RT8207P/SY8032A)

Size: Custom | Document Number | Rev: v0.2

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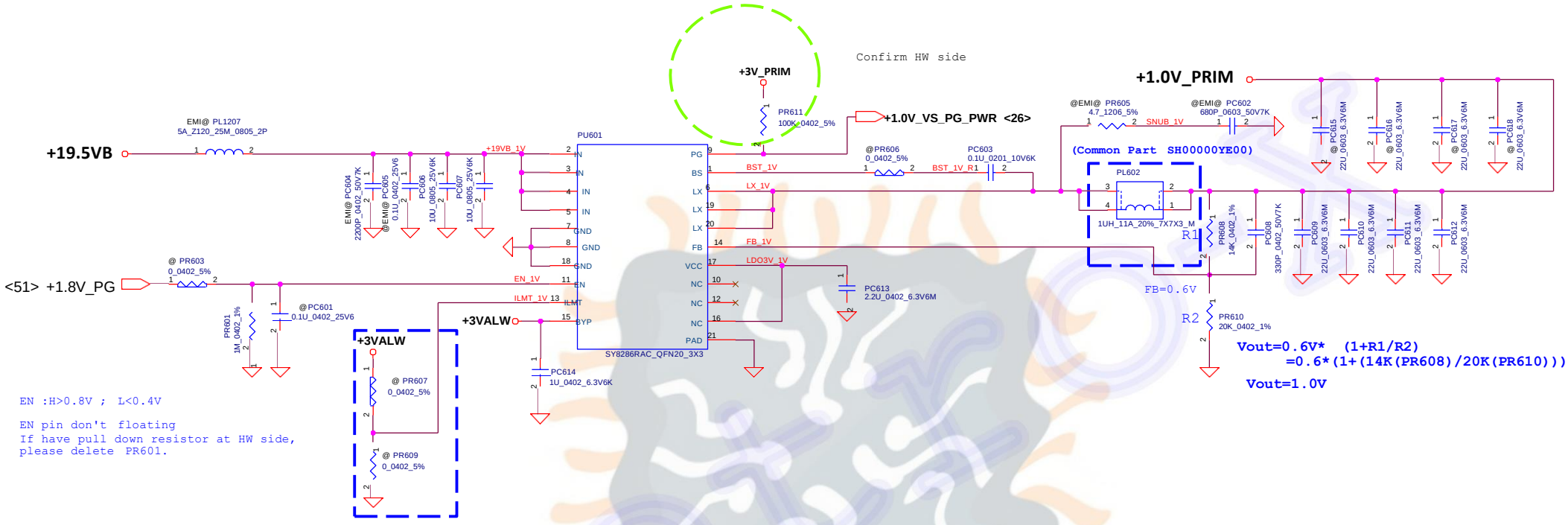

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Title: 1.0VS(SY8286)

Size: Custom | Document Number | Rev: 1.0.2

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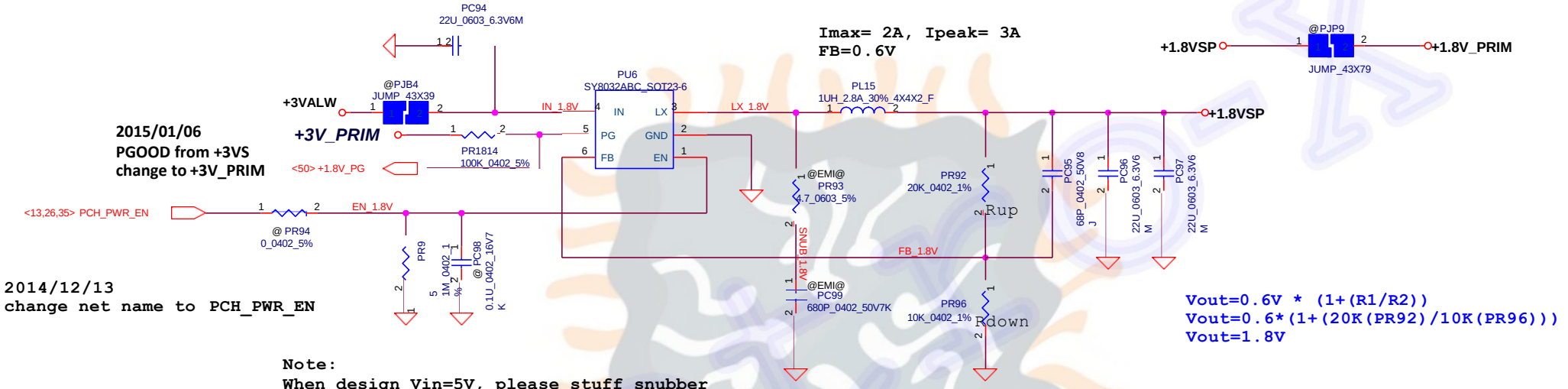


Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.		
Title: *1.8VS(SY8032A)*		
Size: B	Document Number: LA-D707P	Rev: v0.2
Date:	Sheet 51 of 60	

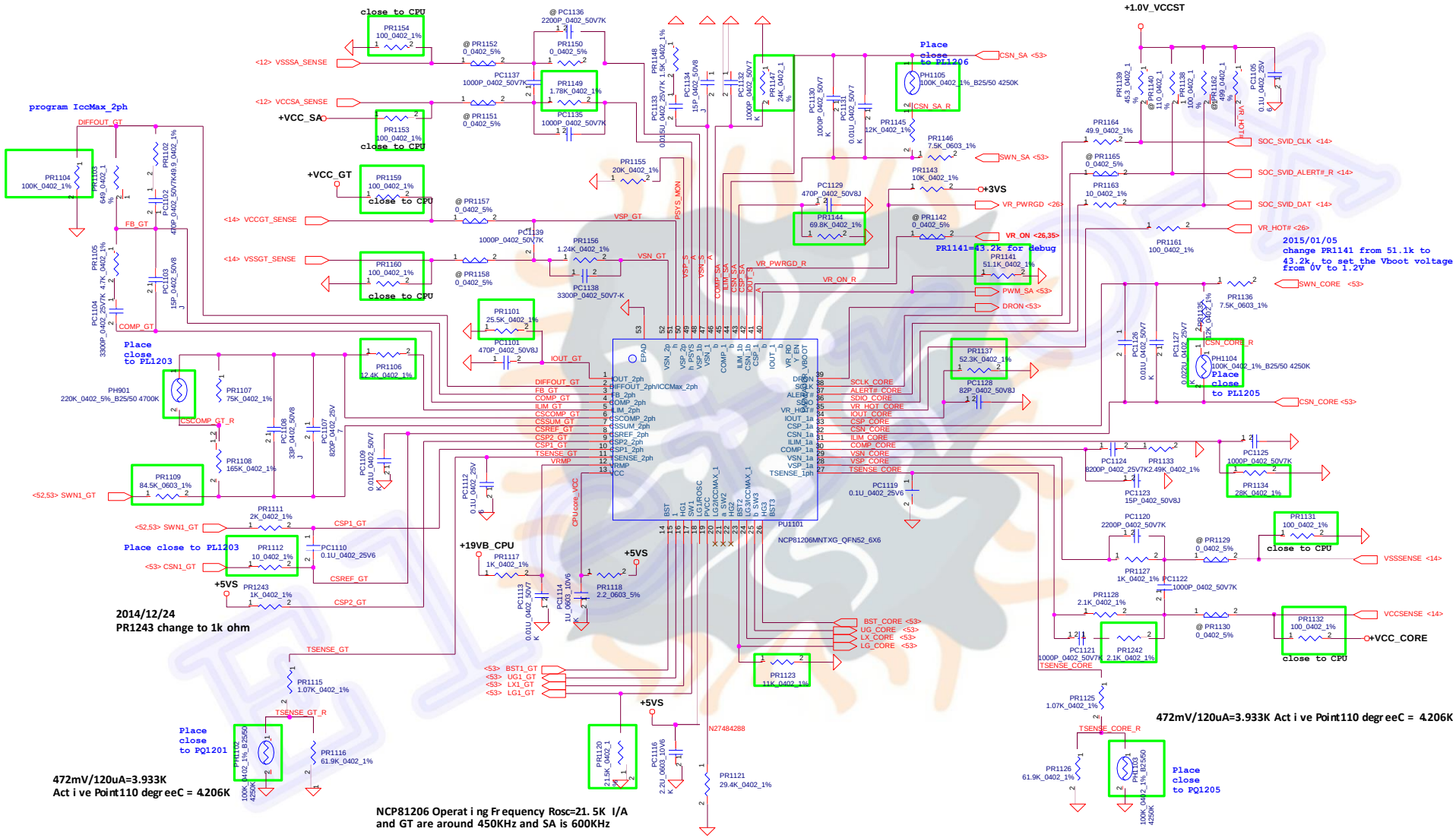
PR1101=2*PR1106/(10*IOUTmax*Load line) RIccMAX2ph(PR1104)= (IccMAX2Ph+32)*200kohm/ 127
U22 Iout@GT=31A U22 IccMAX@GT=31A
PR1101=25.5kohm PR1104= 100K

PR1106=Iout limit*Load line/10 Load line=(PR1108+(PR1107+PH901/(PR1107*PH901)))*Iout tltal*DCR/PR1109
U22 OCP@GT=40A U22 Load line@GT= 3.1m
PR1106=12.4kohm PR1109 ,PR1110@GT=84.5K

RDRPSP(PR1149)= Load line*(PR1146+PH1105+PR1145)/(gm * DCR) /(PH1105+PR1145)
Load line@SA= 10.3m
gm=1mS
PR1149=1.78K

RLIMSP(PR1147)= 1.3V/(gm*(PH1105+PR1145)*IoutLIMIT*DCR/(PR1146+PH1105+PR1145))
OCP@SA= 9.6A
gm=1mS
PR1147=24K

RIOUTSP(PR1144)= 2V/(gm*(PH1105+PR1145)*ICCMAX*DCR/(PR1146+PH1105+PR1146))
IOUTSP@SA= 5A
gm=1mS
PR1144=69.8K



NCP81206 Operat i ng Frequency Rosc=21. 5K I/A
and GT are around 450KHz and SA is 600KHz

IccMAX@SA= 5A
PR1123= 11K
Refer IccMAX table in datasheet

IccMAX@VCORE= 28A
RIccMAX@VCORE= 24.9K
Refer IccMAX table in datasheet

RDRPSP(PR1128)= Load line*(PR1136+PH1104+PR1135)/(gm * DCR) /(PH1104+PR1135)
Load line@VCORE= 2.1m
gm=1mS
PR1128=2.1K

RIOUTSP(PR1137)= 2V/(gm*(PH1104+PR1135)*ICCMAX*DCR/(PR1136+PH1104+PR1135))
IOUTSP@VCORE= 28A
gm=1mS
PR1137=64.9K

RLIMSP(PR1134)= 1.3V/(gm*(PH1104+PR1135)*IoutLIMIT*DCR/(PR1136+PH1104+PR1135))
OCP@VCORE= 35A
gm=1mS
PR1134=33.2K

Title	VCC_CORE_U22(NCP81206)
Size	Document Number / Rev v0.2
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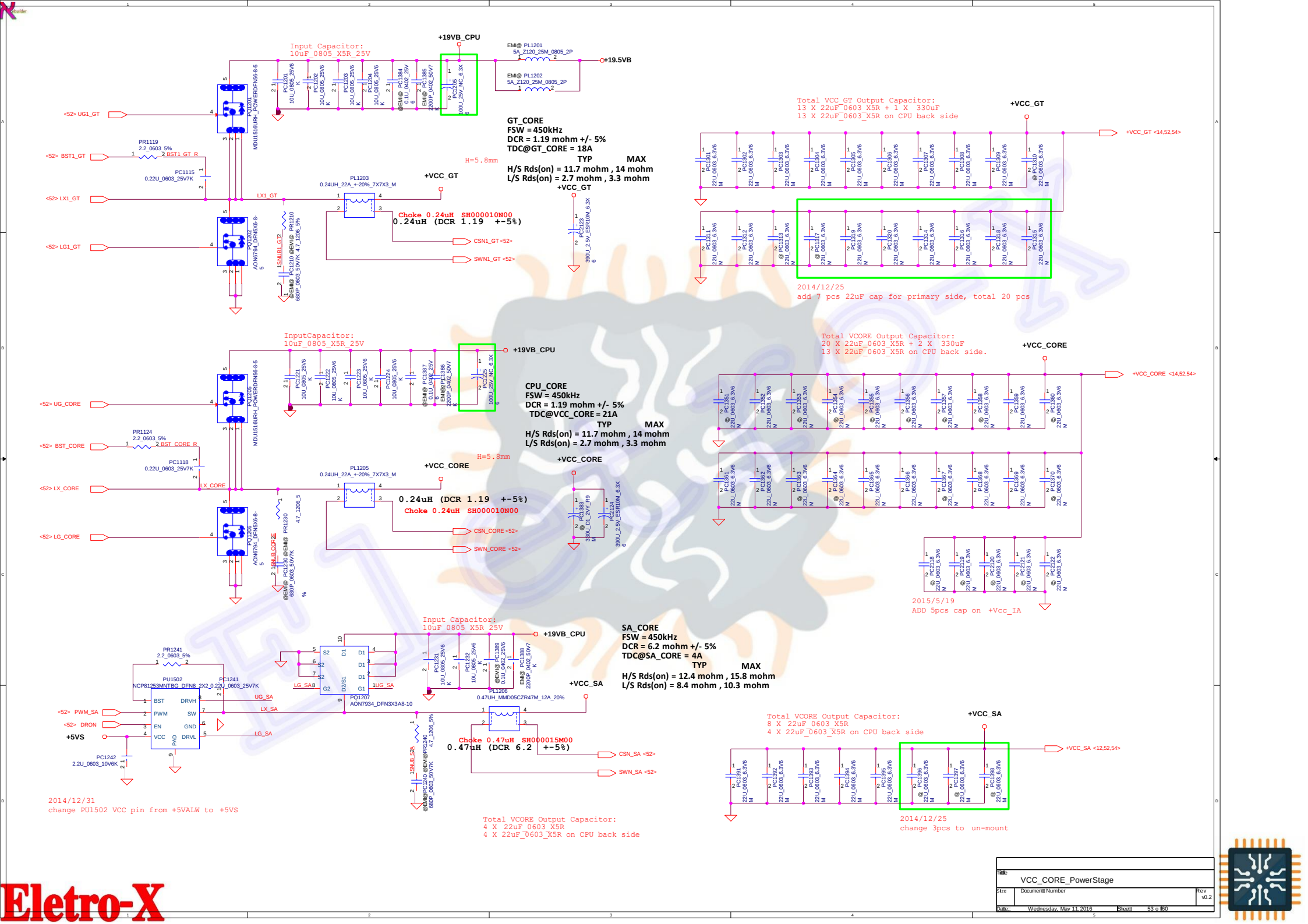
Input Capacitor:
10uF_0805_X5R_25V
+19VB_CPU
EMI@ PL1201
5A_Z120_25M_0805_2P
EMI@ PL1202
5A_Z120_25M_0805_2P
+19.5VB
<52> UG1_GT
<52> BST1_GT
<52> LX1_GT
<52> LG1_GT
PR1119
2.2_0603_5%
PC1115
0.22U_0603_25V7K
PL1203
0.24UH_22A_+-20%_7X7X3_M
+VCC_GT
LX1_GT
Choke 0.24uH SH000010N00
0.24uH (DCR 1.19 +-5%)
CSN1_GT <52>
SWN1_GT <52>
H=5.8mm
GT_CORE
FSW = 450kHz
DCR = 1.19 mohm +/- 5%
TDC@GT_CORE = 18A
TYP MAX
H/S Rds(on) = 11.7 mohm , 14 mohm
L/S Rds(on) = 2.7 mohm , 3.3 mohm
Total VCC_GT Output Capacitor:
13 X 22uF_0603_X5R + 1 X 330uF
13 X 22uF_0603_X5R on CPU back side
+VCC_GT
+VCC_GT <14,52,54>
2014/12/25
add 7 pcs 22uF cap for primary side, total 20 pcs
InputCapacitor:
10uF_0805_X5R_25V
+19VB_CPU
<52> UG_CORE
<52> BST_CORE
<52> LX_CORE
<52> LG_CORE
PR1124
2.2_0603_5%
PC1118
0.22U_0603_25V7K
PL1205
0.24UH_22A_+-20%_7X7X3_M
+VCC_CORE
LX_CORE
0.24uH (DCR 1.19 +-5%)
Choke 0.24uH SH000010N00
CSN_CORE <52>
SWN_CORE <52>
H=5.8mm
CPU_CORE
FSW = 450kHz
DCR = 1.19 mohm +/- 5%
TDC@VCC_CORE = 21A
TYP MAX
H/S Rds(on) = 11.7 mohm , 14 mohm
L/S Rds(on) = 2.7 mohm , 3.3 mohm
Total VCORE Output Capacitor:
20 X 22uF_0603_X5R + 2 X 330uF
13 X 22uF_0603_X5R on CPU back side.
+VCC_CORE
+VCC_CORE <14,52,54>
2015/5/19
ADD 5pcs cap on +Vcc_IA
Input Capacitor:
10uF_0805_X5R_25V
+19VB_CPU
PR1241
2.2_0603_5%
PU1502
NCP81253MNTBG_DFN8_2X2
PC1241
0.22U_0603_25V7K
<52> PWM_SA
<52> DRON
+5VS
PC1242
2.2U_0603_10V6K
PQ1207
AON7934_DFN3X3A8-10
PL1206
0.47UH_MMD05CZR47M_12A_20%
+VCC_SA
Choke 0.47uH SH000015M00
0.47uH (DCR 6.2 +-5%)
CSN_SA <52>
SWN_SA <52>
SA_CORE
FSW = 450kHz
DCR = 6.2 mohm +/- 5%
TDC@SA_CORE = 4A
TYP MAX
H/S Rds(on) = 12.4 mohm , 15.8 mohm
L/S Rds(on) = 8.4 mohm , 10.3 mohm
2014/12/31
change PU1502 VCC pin from +5VALW to +5VS
Total VCORE Output Capacitor:
4 X 22uF_0603_X5R
4 X 22uF_0603_X5R on CPU back side
Total VCORE Output Capacitor:
8 X 22uF_0603_X5R
4 X 22uF_0603_X5R on CPU back side
+VCC_SA
+VCC_SA <12,52,54>
2014/12/25
change 3pcs to un-mount
Eletro-X
VCC_CORE_PowerStage
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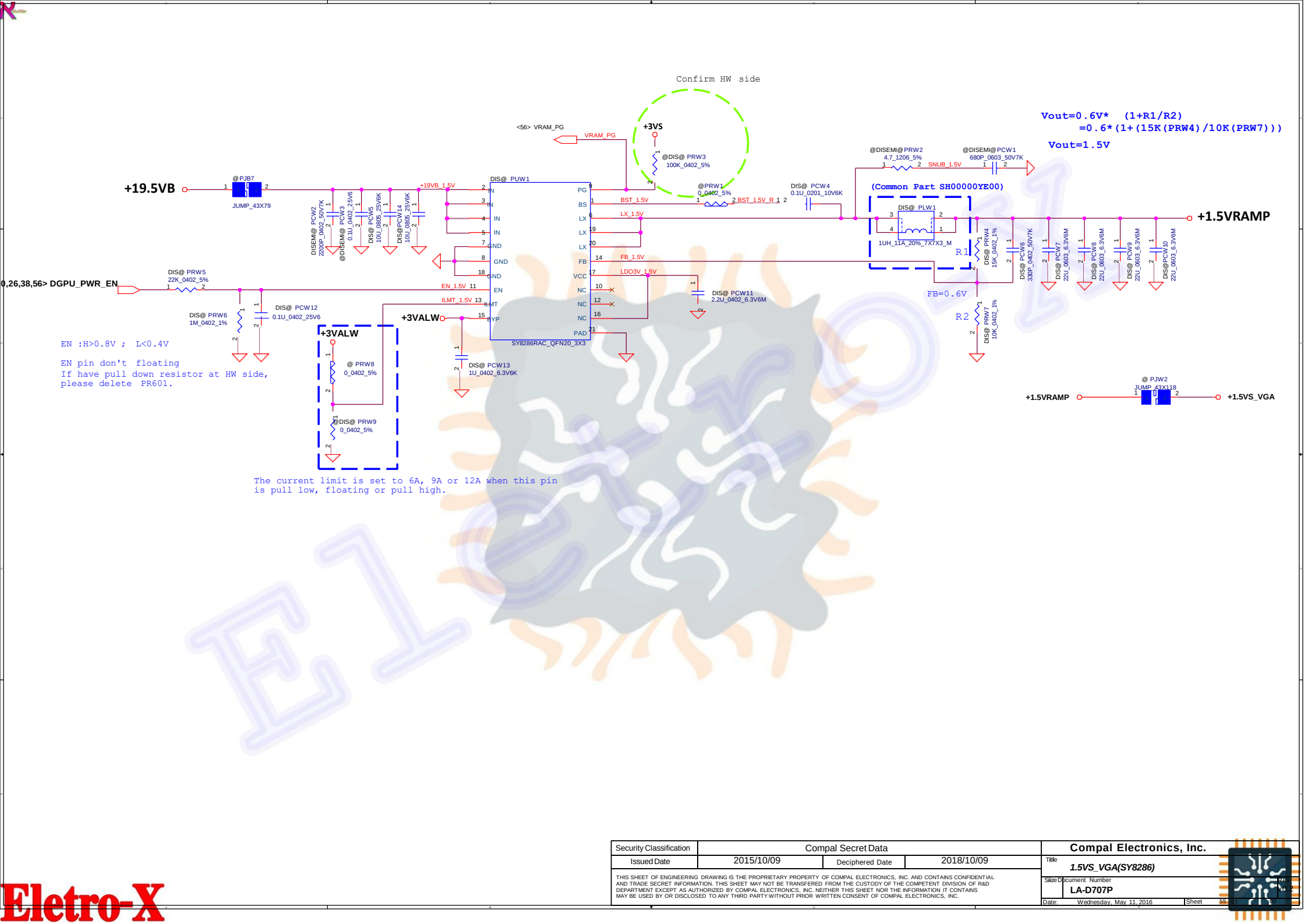

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *1.5VS_VGA(SY8286)*

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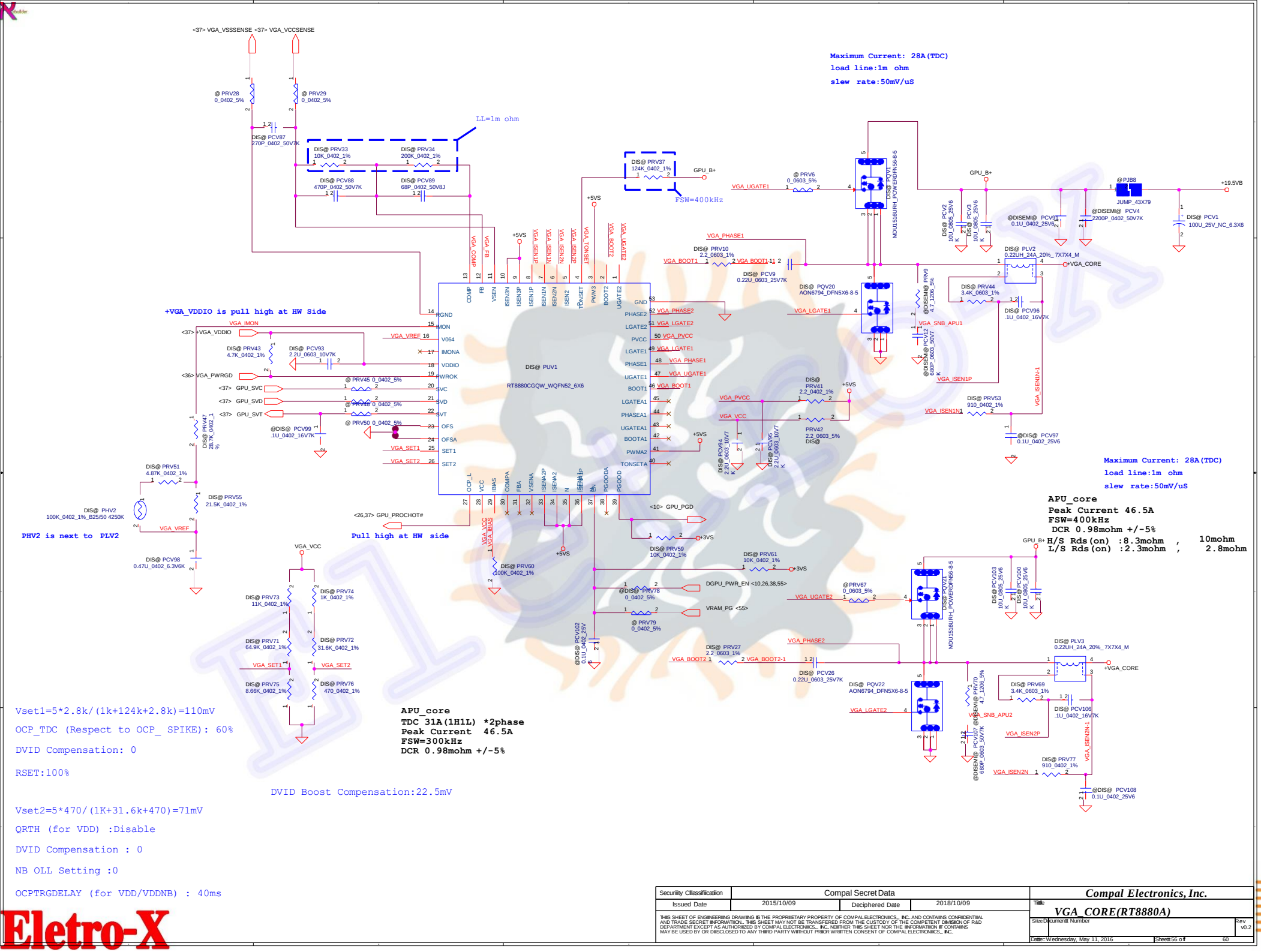
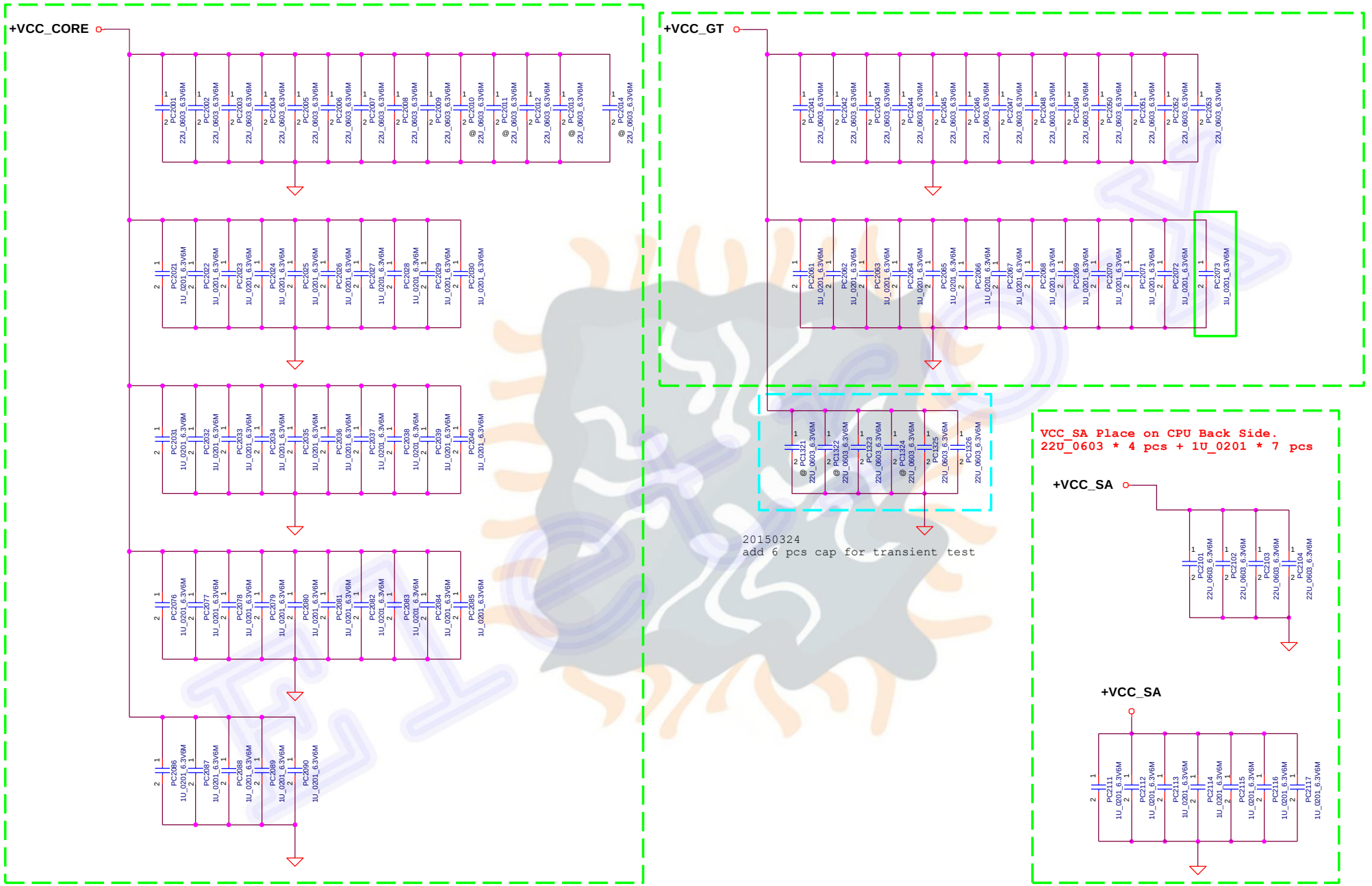

Maximum Current: 28A(TDC)
load line:1m ohm
slew rate:50mV/uS
LL=1m ohm
FSW=400kHz
+VGA_VDDIO is pull high at HW Side
PHV2 is next to PLV2
Pull high at HW side
DIS@ PUV1
RT8880CGQW_WQFN52_6X6
APU_core
Peak Current 46.5A
FSW=400kHz
DCR 0.98mohm +/-5%
H/S Rds(on) :8.3mohm , 10mohm
L/S Rds(on) :2.3mohm , 2.8mohm
Vset1=5*2.8k/(1k+124k+2.8k)=110mV
OCP_TDC (Respect to OCP_ SPIKE): 60%
DVID Compensation: 0
RSET:100%
DVID Boost Compensation:22.5mV
Vset2=5*470/(1K+31.6k+470)=71mV
QRTH (for VDD) :Disable
DVID Compensation : 0
NB OLL Setting :0
OCPTRGDELAY (for VDD/VDDNB) : 40ms
APU_core
TDC 31A(1H1L) *2phase
Peak Current 46.5A
FSW=300kHz
DCR 0.98mohm +/-5%
Compal Secret Data
Issued Date 2015/10/09
Deciphered Date 2018/10/09
Compal Electronics, Inc.
VGA_CORE(RT8880A)
Wednesday, May 11, 2016
Eletro-X

VCC_CORE Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*12 pcs

2014/12/25
add 1 pcs 1uF cap for back side, total 13 pcs



Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: VCC_CORE_PROCESSOR DECOUPLING

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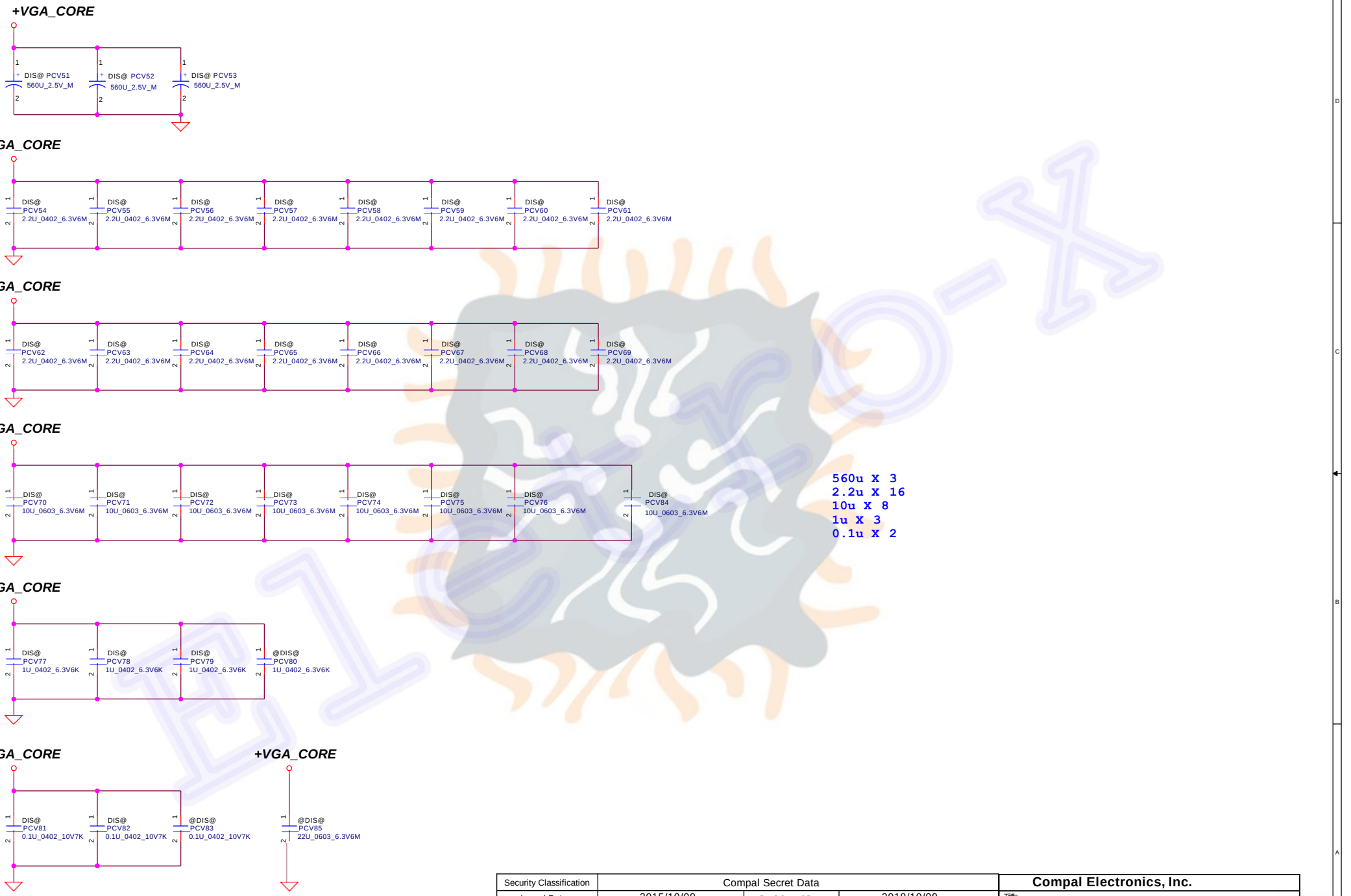

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *VGA_CORE_CHIP DECOUPLING*

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Item	Page	Title	Change Description	Date
1	50,55	Change 0 ohm to short pad	Change PR607,PRV28,PRV29 from 0 ohm to short pad PRW8 from unpop to pop , change PRW8 from 0 ohm to short pad	2016-2-19
2	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000S800 to SB00000JZ00(Change to Main source)	2016-2-19
3	54	Add IA_Core Output capacitor	Add IA_Core Output capacitor 0603 22uF(PC2014) for IccMAX=32A	2016-2-24

Item	Page	Title	Change Description	Date
1	47	ADP_I resistance	Change PR223 from short pad to 0 ohm	2016-4-28
2	52	ICCmax from 29A to 32A	Change PR1121 from 20.5K to 29.4K Change PR1137 from 61.9K to 52.3K Change PR1134 from 33.2K to 28K	2016-4-28
3	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800(Change to 2nd source)	2016-4-28
4	49	Add 2nd source	Change PU3 from RT8207P (SA00007IH00) to G5616B (SA0008PH00)	2016-4-28
5	48	Add 2nd source	Change PU2 from RT8243A(SA00005VH00) to UP1590PQKF(SA0007DS00)	2016-4-28

Title: Power_PIR(PV)		
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	Change Value	11/06	Power	(Set VR prochot# from 110C to 120C)	Change PR1115 and PR1125 Value 0 ohm to 1.07K ohm	
2	50	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PL602 part number from SH00000Z200 to SH00000YE00	
3	55	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PLW1 part number from SH00000Z200 to SH00000YE00	
4	48	Add Jump	11/18	Power	For easy debug	+3VL and +VL add Jump	
5	55	Add Net	11/18	EE	For VGA CORE sequence and VID error issue	Delete PG pin test point VRAM_PG Add Net VRAM_PG	
6	56	pop to unpop unpop to pop	11/18	EE	For VGA CORE sequence and VID error issue	PRV61 from unpop to pop PRV78 and PCV102 from pop to unpop	
7	56	Add Net and R	11/18	EE	For VGA CORE sequence and VID error issue	Add Net VRAM_PG Add PRV79	
8	47	Change jump to ISN choke	11/24	EMI	EMI ISN issue	Delete jump PJB9 Add ISN choke PL201	
9	48	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL7	
10	49	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL10	
11	50	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB3 Add Bead PL1207	
12	53	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB5 Add Bead PL1201 PL1202	
13	55	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1208	
14	56	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1209 and PL1210	
15	55	Change R Value Change C unpop to pop	11/24	EE	HW f i net une VRA Mpo wersequence	Change PRW5 value from 0 ohm to 22K ohm Change PCW12 from unpop to pop (VGA sequence)	
16	53	Change Common part	11/6	Power	(Change to Common part)	Change PC1331 PC1383 PC1390 from SGA20331E10 to SGA00009S00	

Item	Page	Title	Change Description	Date
1	56	Modify VGA_CORE OCP	1.Change PRV73 Value 1K ohm to 11K ohm 2.Change PRV71 Value 124K ohm to 64.9K ohm 3.Change PRV75 Value 2.8K ohm to 8.66K ohm	2015-12-12
2	47	space saving	Change PC221 0603 to 0402 size	2015-12-12
3	47,49,50,51,52,56	Change 0 ohm to short pad	Change PR63,PR94,PR215,PR603,PR1129,PR1130,PR1142,PR1151,PR1152,PR1157,PR1158,PR1165,PR1815,PRM27,PRV45,PRV48,PRV50,PRV79,PRV6,PRV67 from 0 ohm to short pad	2016-1-4
4	48,49,55,56	Delete Jump or Bead(Co-lay)	Delete Co-Lay Bead PL7,PL10,PL1208,PL1209,PL1210	2016-1-7
5	53	Delete VCC_GT,VCC_CORE Co-Lay caps	Delete Location PC1331 Footprint,PC2123 from unpop to pop Delete Location PC1390 Footprint,PC2124 from unpop to pop	2015-12-12
6	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800	2015-12-12
7	52,53,54	CPU transient request	Change PC1353,PC1363,PC1355,PC1356,PC1357,PC1354,PC1364,PC1358,PC1351,PC1370,PC1360,PC2010,PC2013,PC2011,PC1367 from pop to unpop Change PC1107 from 1000P to 820P PC1108 from 390P to 33P,PC1108 from unpop to pop PC1104 from 2200P to 3300P PR1103 from 1K to 649	2015-12-12
8	50	1V OVP issue (HW Low switch second source issue)	Delete jump PJ601 and add output MLCC PC615,PC616,PC617,PC618 PR607 from unpop to pop	2016-1-7

Title	Power_PIR(SI)		
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BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	GCLKPX@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: GCLK

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