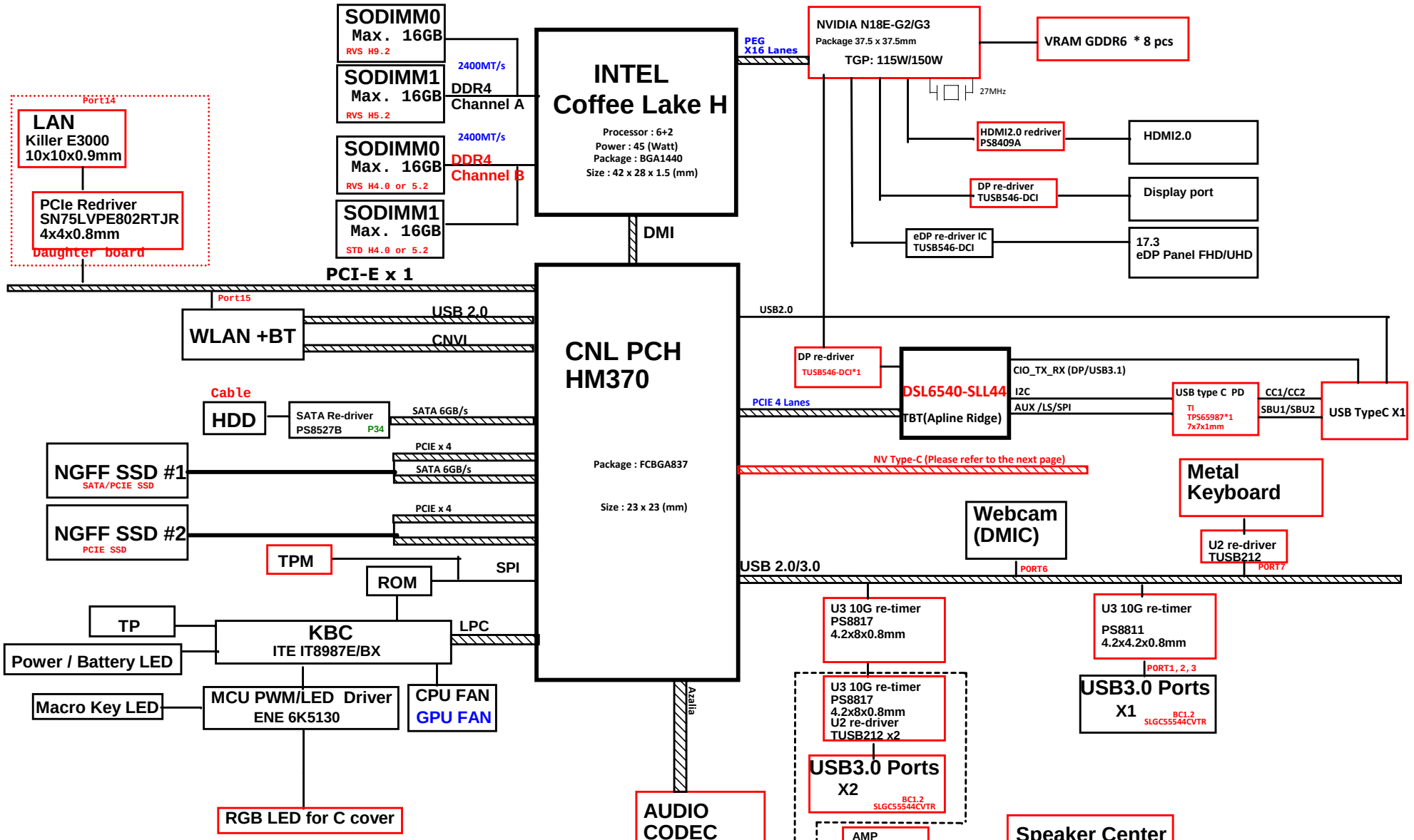
Levante_CFS CFL-H/K +1170/1180 MAX-P SYSTEM DIAGRAM 01



G3@ : NV G3 GPU
ADP@ : For 330W
GSY@ : For G-SYNC panel
NGSY@ : For Non- GSYNC panel
SAM@ : SAMSUNG VRAM
MIC@ : MICRON VRAM
TPM@ : TPM
i9@ : i9 CPU

Quanta Computer Inc.
PROJECT : ZGE
Size | Document Number: BLOCK DIAGRAM | Rev: 1A
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CFL-H Processor (CLK,MISC,JTAG)

02

For debug only remove from MV

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

EMI RESERVE

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

Close to CPU
SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

Close to CPU
SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS

Close to CPU
SVID DATA

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

Ra Not install in SKL-H

Note: please keep plane is enough for VDDQ 2.8A
Placement close to CPU.

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

Modify 8/10

Configuration Signals: The CFG signals have a default value of '1' if not terminated
on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the
board for CFG pins.
. CFG[0]:Stall reset sequence after PCU PLL lock until de-asserted:
-1=(Default) Normal Operation; No stall.
-0=Stall.
.CFG[1]:Reserved configuration lane.
.CFG[2]:PCI Express*Static x16 Lane Numbering Reversal.
-1=Normal operation
-0=Lane numbers reversed.
.CFG[3]:Reserved configuration lane.
.CFG[4]:eDP enable:
-1=Disabled.
-0=Enabled.
.CFG[6:5]:PCI Express* Bifurcation
-00=1x8,2x4 PCI Express*
-01=reserved
-10=2x8 PCI Express*
-11=1x16 PCI Express*
.CFG[7]:PEG Training:
-1=(default) PEG Train immediately following RESET# de assertion.
-0=PEG Wait for BIOS for assertion.
.CFG[19:8]:Reserved configuration lanes.

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Size	Document Number	Rev
	CFL 1/7 (JTAG/MISC)	1A
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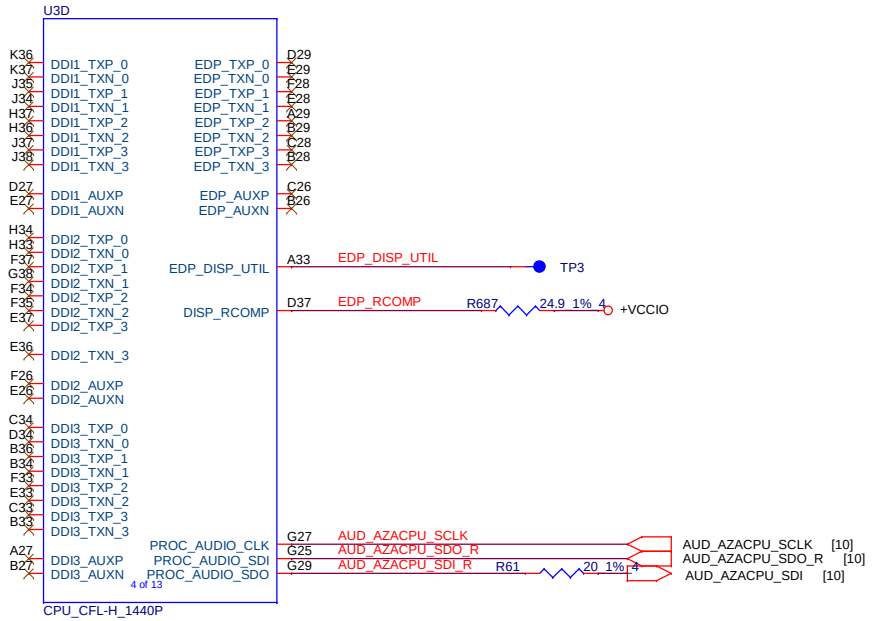
CFL Processor (DMI,PEG,FDI)

DMI RX

DMI TX



DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 Mils Trace Spacing 25 Mils

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_RCOMP

Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

+1.2VSUS [2,6,10,14,17,18,19,20,46,59,60,64,75]

+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,63,64,65,68,70,73,75]

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	CFL 2/7 (DMI/EDP/PEG)	1A
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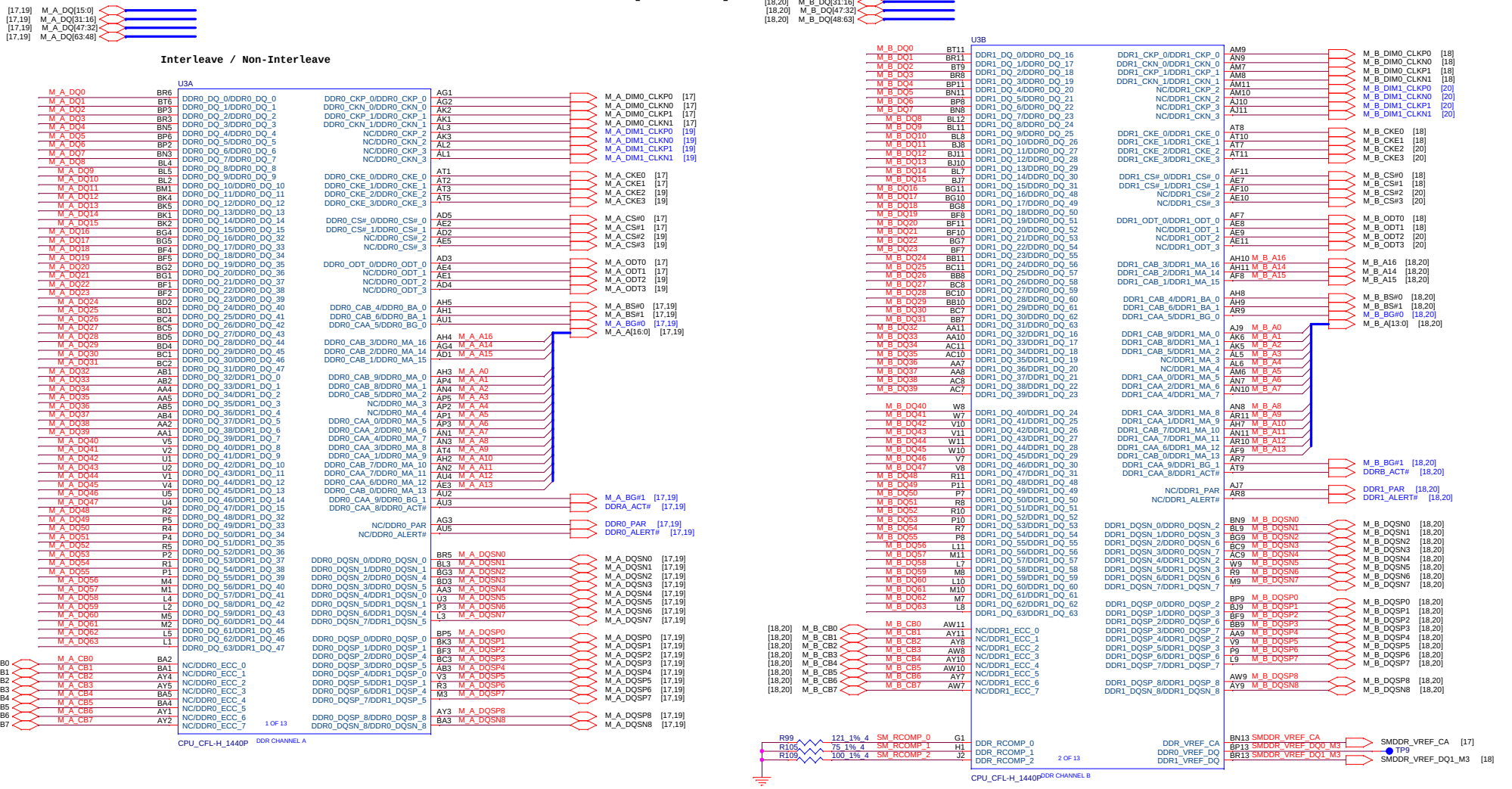
CFL Processor (DDR4)

Interleave / Non-Interleave



Quanta Computer Inc.	
PROJECT : ZGE	
Size	Document Number: CFL 3/7 (DDR4 I/F) — Rev: 1A
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VCCGT

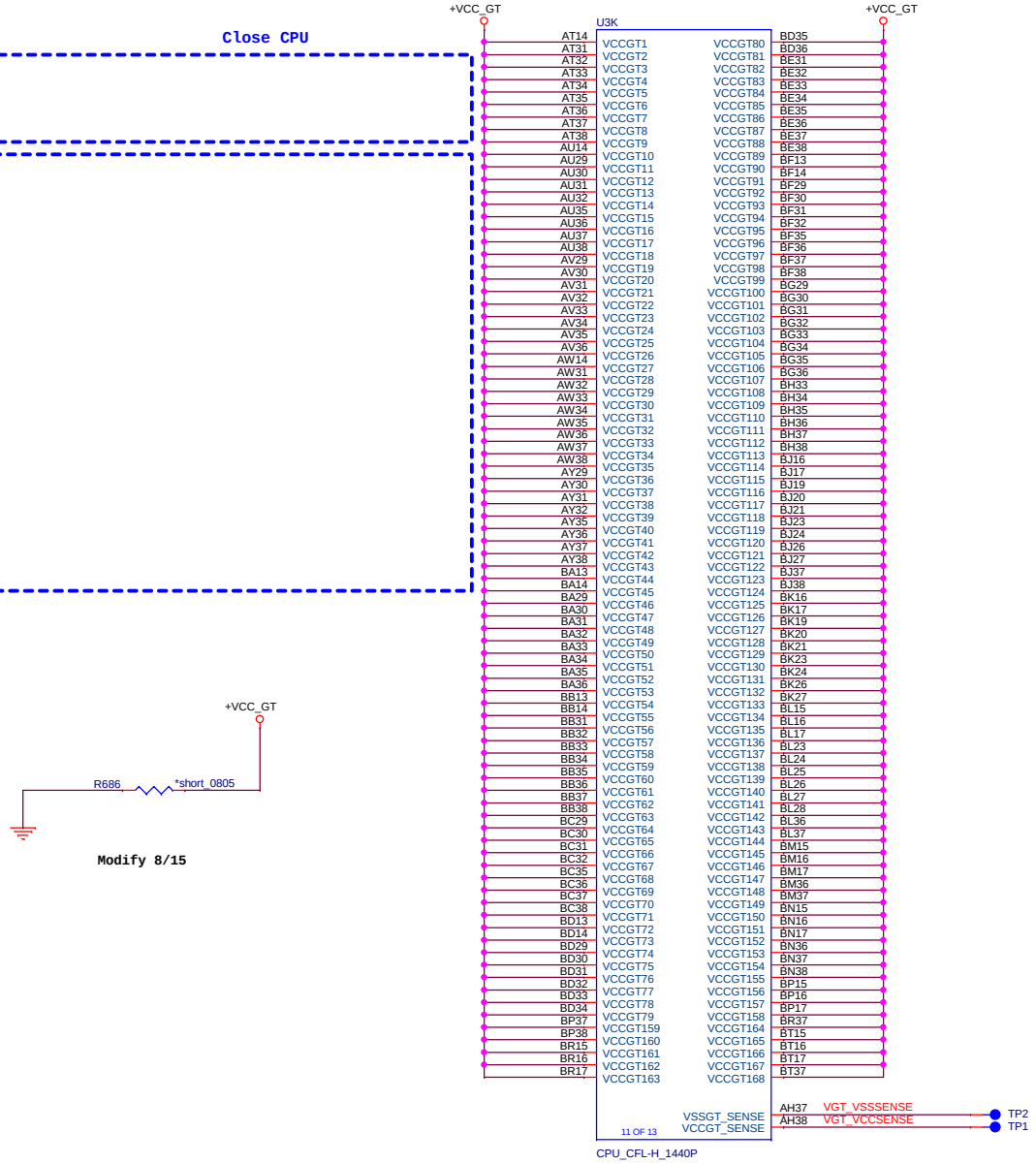
Edge cap
4x 47uF 0805
7x 22uF 0603

Backside cap
10x 10uF 0402
12x 1uF 0201

CFL Processor (POWER)

05

Close CPU



Modify 8/15

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PROJECT : ZGE		
Size	Document Number: CFL 4/7 (POWER)	Rev: 1A
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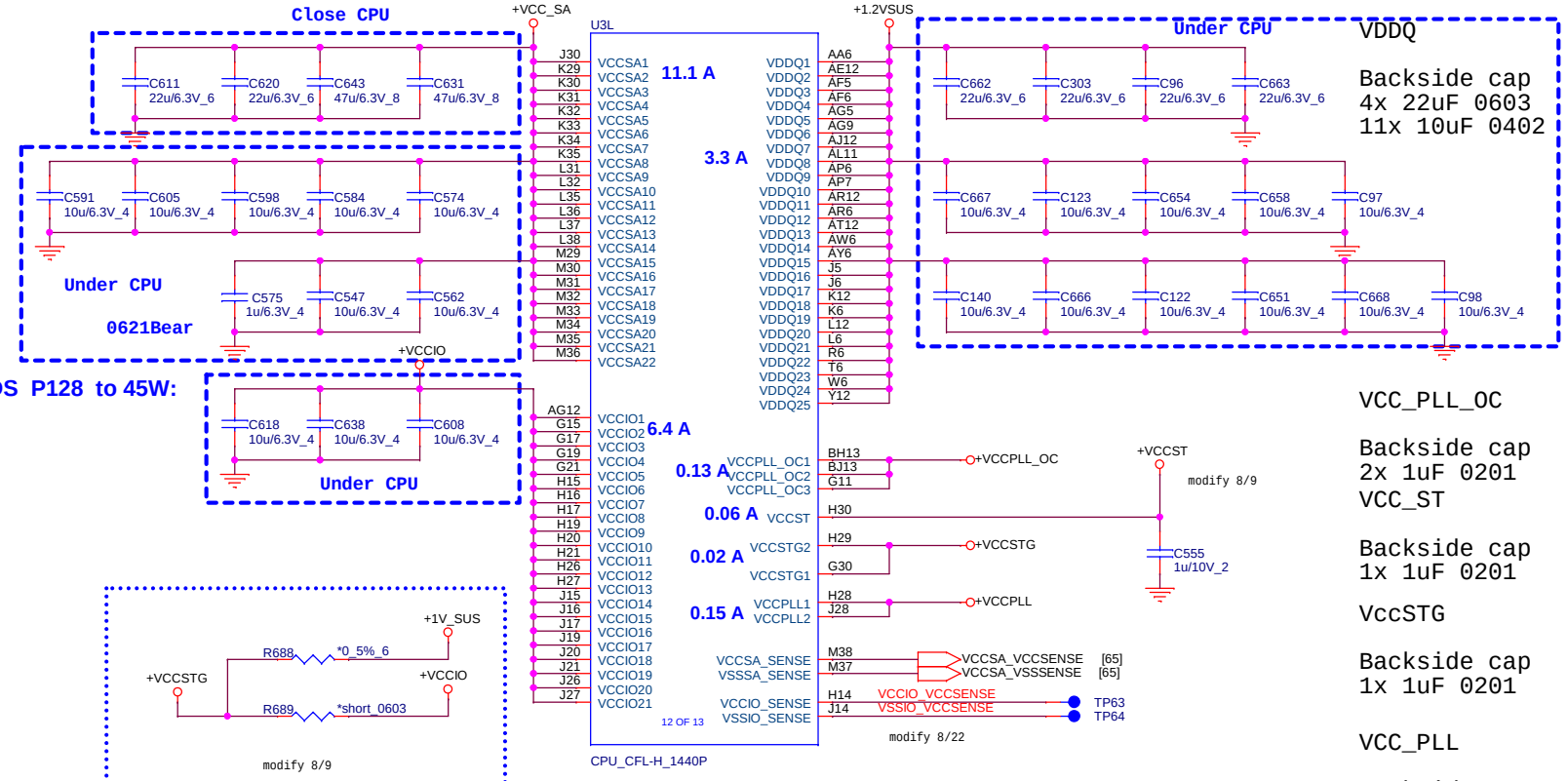
Follow CFL H EDS page 128 to 45W(GT2): VCCSA=11.1A

Follow CFL H EDS page 127 45W: VDDQ=3.3A (LPDDR4)

+VCC_SA

Edge cap
2x 47uF 0805
2x 22uF 0805

Backside cap
7x 10uF 0402



+VCC_IO

Backside cap
3x 10uF 0402

VCC_PLL_OC

Backside cap
2x 1uF 0201

VCC_ST

Backside cap
1x 1uF 0201

VccSTG

Backside cap
1x 1uF 0201

VCC_PLL

Backside cap
4x 22uF 0603
11x 10uF 0404

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	CFL 5/7 (POWER&GND)	1A
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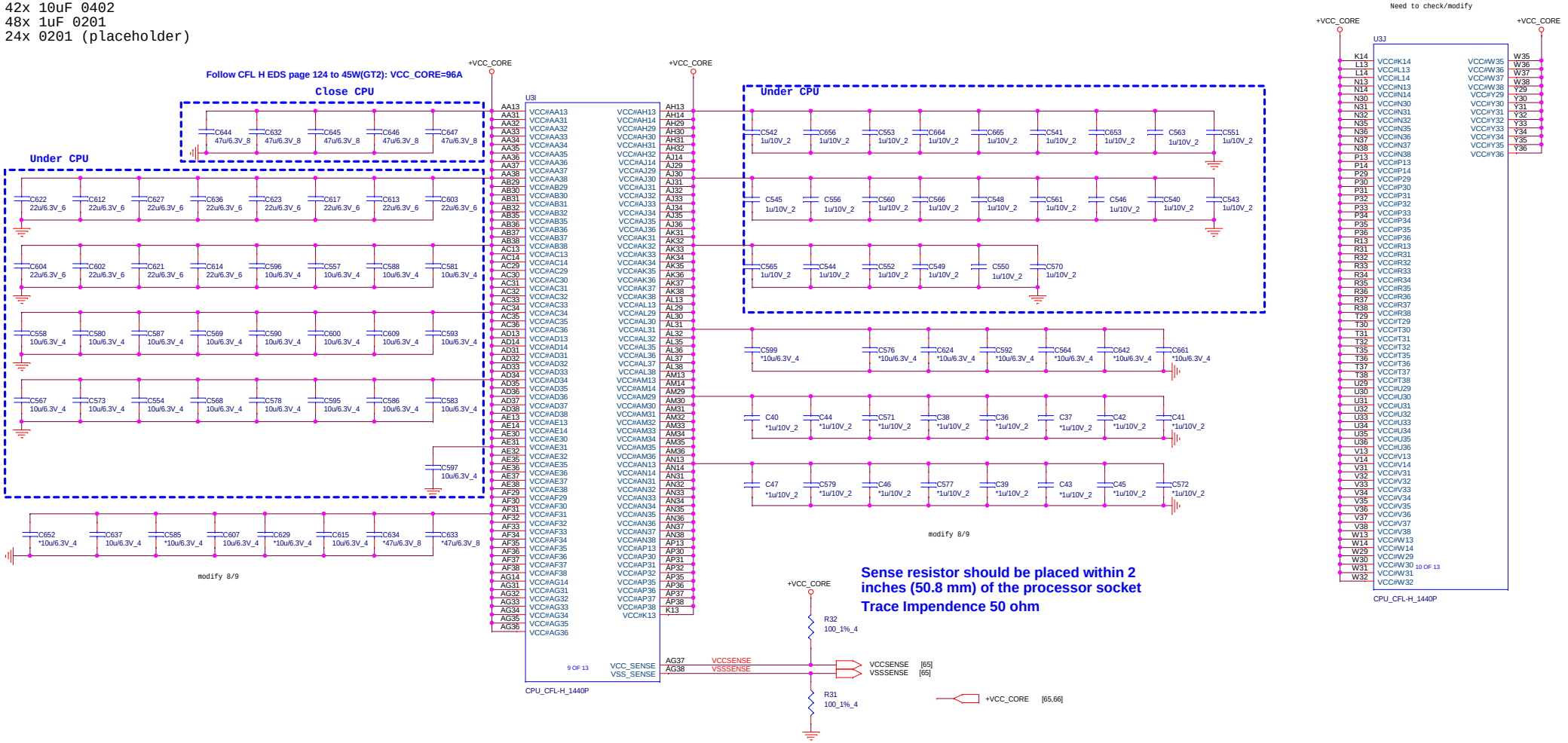
Vcc (VCC_CORE)

Edge cap
8 x 47uF 0805

Backside cap
12x 22uF 0603
42x 10uF 0402
48x 1uF 0201
24x 0201 (placeholder)



Quanta Computer Inc.		
PROJECT : ZGE		
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	CFL 6/7 (POWER&GND)	1A
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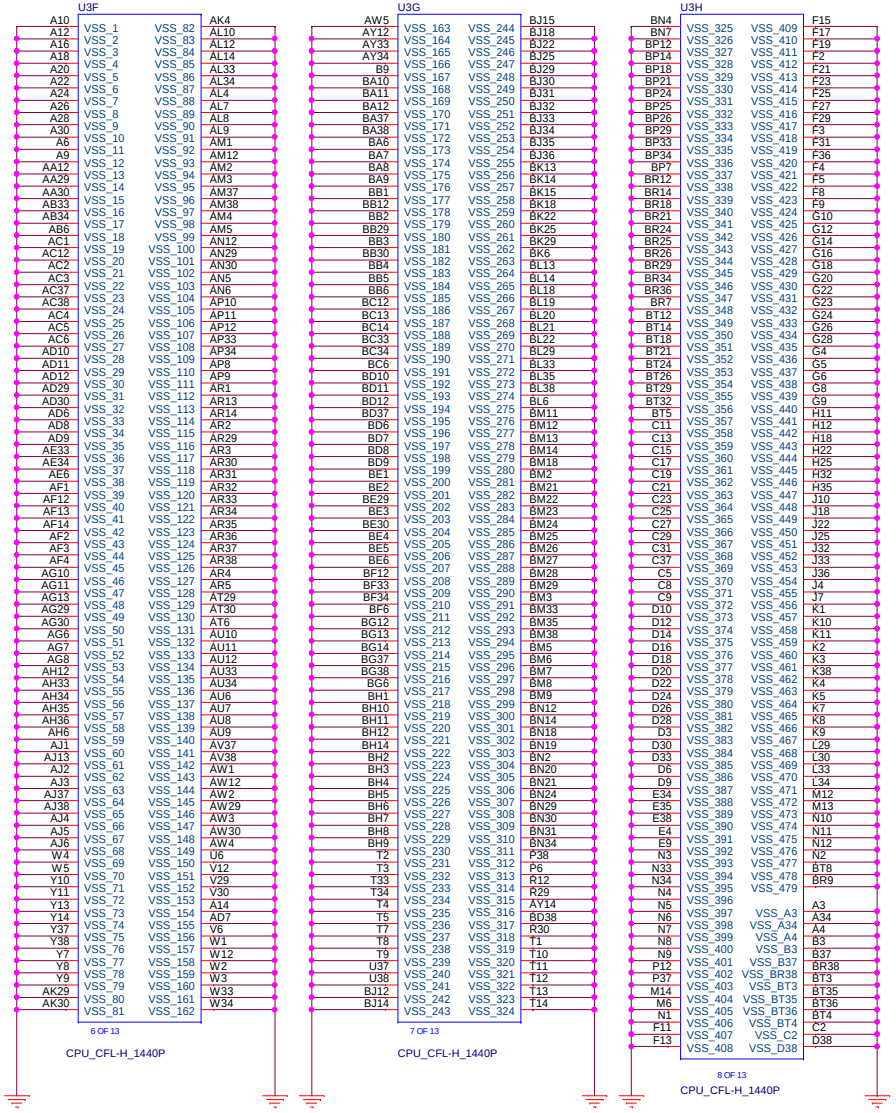
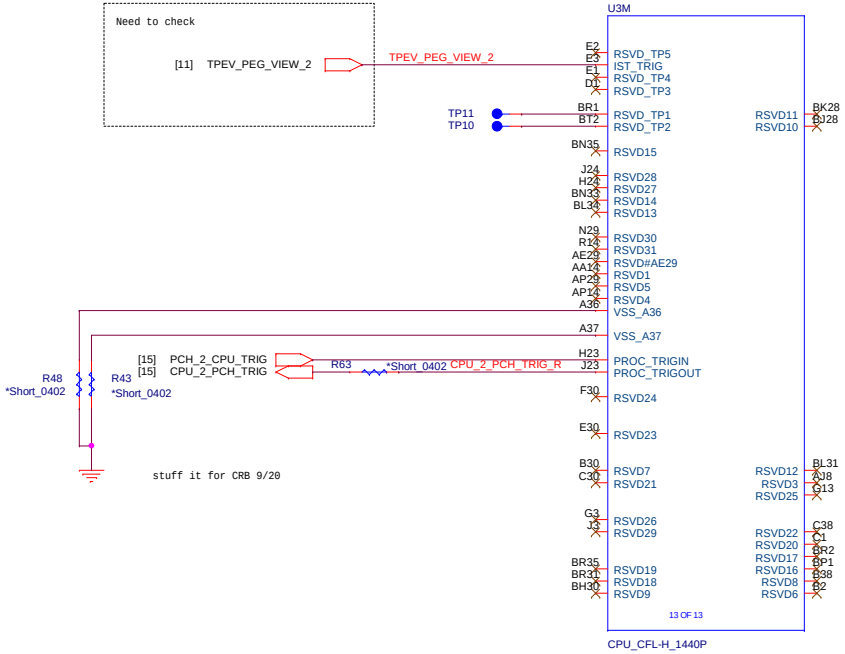
CFL-H Processor (GND)



CFL-H Processor (RESERVED, CFG)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

Quanta Computer Inc.

PROJECT : ZGE

Size	Document Number	Rev
	CFL 7/7 (GND)	1A

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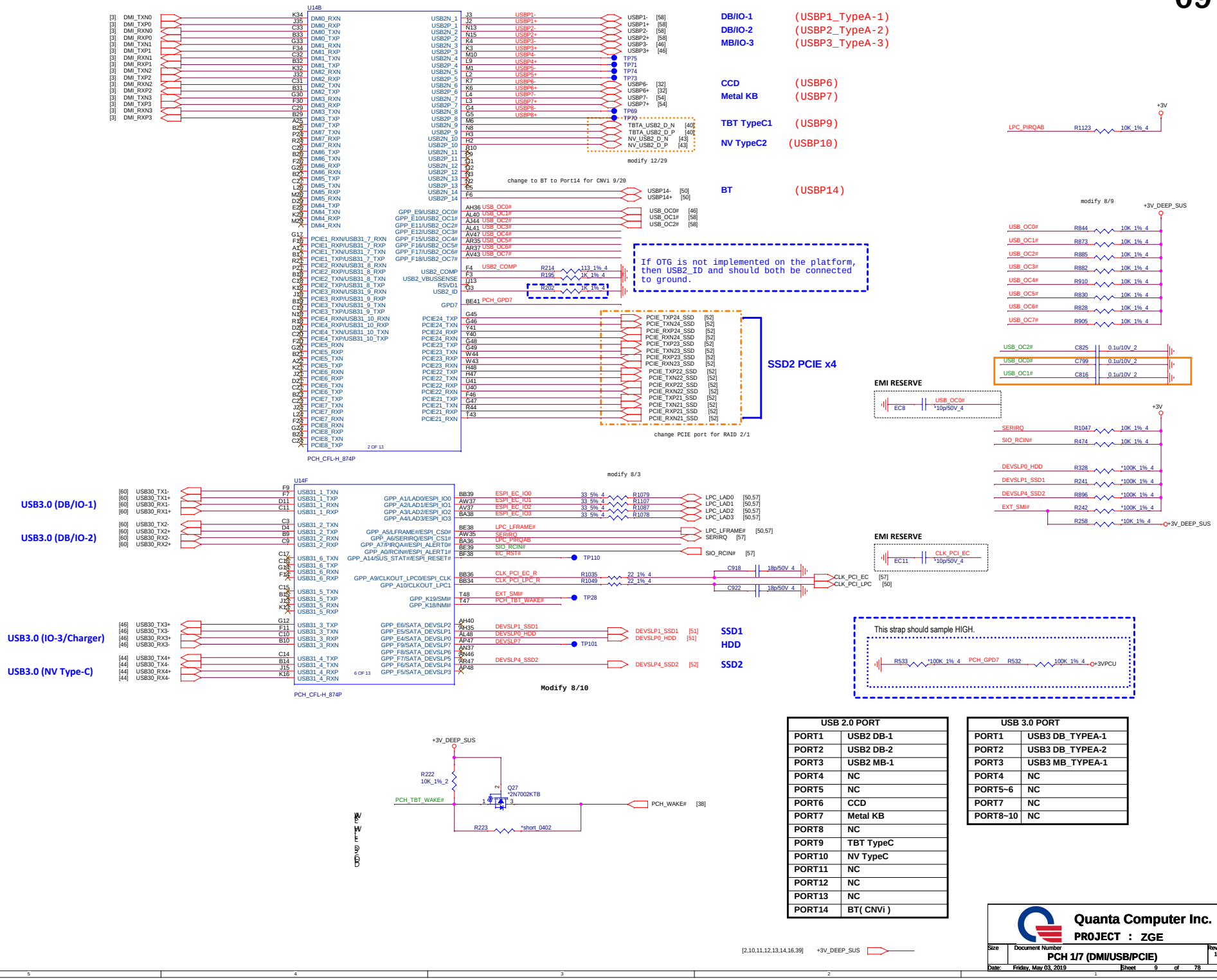

USB 2.0 PORT	
PORT1	USB2 DB-1
PORT2	USB2 DB-2
PORT3	USB2 MB-1
PORT4	NC
PORT5	NC
PORT6	CCD
PORT7	Metal KB
PORT8	NC
PORT9	TBT TypeC
PORT10	NV TypeC
PORT11	NC
PORT12	NC
PORT13	NC
PORT14	BT(CNVi)

USB 3.0 PORT	
PORT1	USB3 DB_TYPEA-1
PORT2	USB3 DB_TYPEA-2
PORT3	USB3 MB_TYPEA-1
PORT4	NC
PORT5~6	NC
PORT7	NC
PORT8~10	NC

[2,10,11,12,13,14,16,39] +3V_DEEP_SUS

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	1A
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HDA Bus(CLG)

C442 *47p/50V_4 ACZ_BCLK

U14D — PCH_CFL-H_874P (4 OF 13)

[47] PCH_AZ_CODEC_BITCLK	R488 33_5% 4	ACZ_BCLK	BD11	HDA_BCLK/I2S0_SCLK
[47] PCH_AZ_CODEC_SDIN0	R491 *short 0402	ACZ_SDIN0_R	BE11	HDA_SDI0/I2S0_RXD
[47] PCH_AZ_CODEC_SDOUT	R492 33_5% 4	ACZ_SDO	BF12	HDA_SDO/I2S0_TXD
[47] PCH_AZ_CODEC_SYNC	R494 33_5% 4	ACZ_SYNC	BG13	HDA_SYNC/I2S0_SFRM
[47] PCH_AZ_CODEC_RST#	R496 33_5% 4	ACZ_RST#	BE10	HDA_RST#/I2S1_SCLK
			BF10	HDA_SDI/I2S1_RXD
			BE12	I2S1_TXD/SNDW2_DATA
			BD12	I2S1_SFRM/SNDW2_CLK
[3] AUD_AZACPU_SDO_R	R358 30_1% 4	AUD_AZACPU_SDO	AM2	HDACPU_SDO
[3] AUD_AZACPU_SDI		AUD_AZACPU_SDI	AN3	HDACPU_SDI
[3] AUD_AZACPU_SCLK	R313 30_1% 4	AUD_AZACPU_SCLK_R	AM3	HDACPU_SCLK

Modify 8/10

[50] PCM_CLK	R1118 *0_5% 4	I2S2_SCLK	AV18	GPP_D8/I2S2_SCLK
[50] PCM_IN	R1117 *0_5% 4	I2S2_RXD	AW18	GPP_D7/I2S2_RXD
		MODEM_CLKREQ_C	BA17	GPP_D6/I2S2_TXD/MODEM_CLKREQ
		CNV_RF_RESET#_C	BE16	GPP_D5/I2S2_SFRM/CNV_RF_RESET#
[32] PCH_DMICDAT			BF15	GPP_D20/DMIC_DATA0/SNDW4_DATA
[32] PCH_DMICCLK			BD16	GPP_D19/DMIC_CLK0/SNDW4_CLK
			AV16	GPP_D18/DMIC_DATA1/SNDW3_DATA
			AW15	GPP_D17/DMIC_CLK1/SNDW3_CLK

Add R1204 for CNVi 9/29 — CNV_RF_RESET#_C — 75K_1%_4 — R988

MODEM_CLKREQ_C — R447 71.5K_1%_4

modify 8/9

[16] RTC_RST#		RTC_RST#	BE47	RTCRST#
		SRTC_RST#	BD46	SRTCRST#
[57] RSMRST#	R1068 *0_5% 4 / R981 *short 0402	EC_PWROK_R / PCH_RSMRST#	AY42 / BA47	PCH_PWROK / RSMRST#
PCH_RSMRST# R965	*short 0402	DPWROK_R	AW41	DSW_PWROK
		SMBALERT#	BE25	GPP_C2/SMBALERT#
		SMB_PCH_CLK	BE26	GPP_C0/SMBCLK
		SMB_PCH_DAT	BF26	GPP_C1/SMBDATA
		SML0ALERT#	BF24	GPP_C5/SML0ALERT#
		SMB_ME0_CLK	BF25	GPP_C3/SML0CLK
		SMB_ME0_DAT	BE24	GPP_C4/SML0DATA
		SMB1ALERT#	BD33	GPP_B23/SML1ALERT#/PCHHOT#
		SMB_ME1_CLK	BF27	GPP_C6/SML1CLK
		SMB_ME1_DAT	BE27	GPP_C7/SML1DATA

		GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#	BF36	
		GPP_A8/CLKRUN#	AV32	CLKRUN# — CLKRUN# [57]
		GPD11/LANPHYPC	BF41	LAN_DIS# — TP119
		GPD9/SLP_WLAN#	BD42	SLP_WLAN_N — TP113
			BB46	DDR_DRAMRST#_L — R437 *short 0402 — C407 *0.1u/16V_4
		DRAM_RESET#	BE32	GPP_B2 — R620 *0_5% 4 — DDR_DRAMRST# [17,18,19,20] / UART_WAKE_N [50]
		GPP_B2/VRALERT#	BF33	
		GPP_B1/GSPI1_CS1#/TIME_SYNC1	BE29	PIRQ# [49]
		GPP_B0/GSPI0_CS1#	BJ47	
		GPP_K17/ADR_COMPLETE	AP29	MPHY_EXT_PWR_GATE — TP111
		GPP_B11/I2S_MCLK	AU3	SYS_PWROK_R — R1037 *short 0402 — SYS_PWROK
		SYS_PWROK		modify 8/9
		WAKE#	BB47	PCH_WAKE#_L — R449 *short 0402 — PCIE_WAKE# [38,50,59]
		GPD6/SLP_A#	BE40	SLP_A# — R540 *short 0402 — SLP_A# [16]
		SLP_LAN#	BF40	SLP_LAN# — TP112
		GPP_B12/SLP_S0#	BC28	PCH_SLP_S0ix#_L — R552 *short 0402 — PCH_SLP_S0ix# [16,49]
		GPD4/SLP_S3#	BF42	SLP_S3#_L — R480 *short 0402 — SUSB# [16,57] change BOM 9/4
		GPD5/SLP_S4#	BE42	SLP_S4#_L — R541 *short 0402 — SUSC# [16,57]
		GPD10/SLP_S5#	BC42	SLP_S5#_L — R479 *short 0402 — SLP_S5# [16]
		GPD8/SUSCLK	BE45	SUSCLK32 — R983 *0_5% 4 — SUSCLK [50]
		GPD0/BATLOW#	BF44	BATLOW# — BATLOW# [38]
		GPP_A15/SUSACK#	BE35	SUSACK# — R486 *short 0402
		GPP_A13/SUSWARN#/SUSPWRDNACK	BC37	SUSWARN#
		GPD2/LAN_WAKE#	BG44	LANWAKE_N — R543 *0_5% 4 — TP122
		GPD1/ACPRESENT	BG42	ACPRESENT — ACPRESENT [57]
		SLP_SUS#	BD39	PCH_SLP_SUS# — TP105
		GPD3/PWRBTN#	BE46	DNBSWON# — DNBSWON# [57]
		SYS_RESET#	AU2	XDP_DBRESET# — XDP_DBRESET# [16]
		GPP_B14/SPKR	AW29	ACZ_SPKR — ACZ_SPKR [47]
		CPUPWRGD	AE3	PROCPWRGD — PROCPWRGD [2]
		ITP_PMODE	AL3	ITP_PMODE — TP99
		ITP_PMODE	AH4	PCH_JTAGX — R248 *short 0402 — H_TCK [2]
		PCH_JTAGX	AJ4	PCH_TMS — R264 *short 0402 — H_TMS [2]
		PCH_JTAG_TMS	AH3	PCH_TDO — R188 *short 0402 — H_TDO [2]
		PCH_JTAG_TDO	AH2	PCH_TDI — R244 *short 0402 — H_TDI [2]
		PCH_JTAG_TDI	AJ3	PCH_TCK — R283 51_5% 4
		PCH_JTAG_TCK		

+1.2VSUS

DDR_DRAMRST# — R336 470 1% 4

+3V_DEEP_SUS

MPHY_EXT_PWR_GATE	R1097 200K_1% 4	
PCH_WAKE#_L	R436 4.7K_1% 4	change R1007 to 4.7K for CNVi 9/29
GPP_B2	R579 4.7K_1% 4	change R985 to 4.7K for CNVi 9/29
LANWAKE_N	R481 4.7K_1% 4	
SUSACK#	R617 *10K_1% 4	
XDP_DBRESET#	R935 10K_1% 4	
SUSCLK32	R1011 *10K_1% 4	
SUSWARN#	R615 *10K_1% 4	
BATLOW#	R534 10K_1% 4	
ACPRESENT	R542 100K_1% 4	
PCH_SLP_S0ix#_L	R495 100K_1% 4	
SMB_ME0_CLK	R537 2.2K_5% 4	
SMB_ME0_DAT	R535 2.2K_5% 4	
SMB_ME1_CLK	R606 *2.2K_5% 4	
SMB_ME1_DAT	R603 *2.2K_5% 4	
SMB_PCH_CLK	R478 2.2K_5% 4	
SMB_PCH_DAT	R477 2.2K_5% 4	

modify 8/9

+1V_S5

PCH_TDO — R189 *51_5% 4

+3V

CLKRUN# — R1121 10K_1% 4

ME Lock

[57] ME_WR# — R493 1K_1% 4 — ACZ_SDO

0 = *Enable security in the Flash Description (iPD 20K)

1 = Disable Flash Descriptor Security (Override)

TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)

LOW: security measures defined in the Flash Descriptor. (Default)

+3V_DEEP_SUS — R1088 1K_1%_2 — ME_WR# — R1053 1K_1%_2

[2,9,11,12,13,14,16,39] +3V_DEEP_SUS

EC reset RTC

[57] CLR_CMOS — Q41 *2N7002KTB — R586 100K_1%_4

SRTC_RST#

RTC_RST# — CLR_CMOS — Q49 2N7002KTB

PCH/EC

+3V_DEEP_SUS

[40,57,60] 2ND_MBDATA — *2N7002KDW Q55A — R1156 *short 0402 — SMB_ME1_DAT

[40,57,60] 2ND_MBCLK — *2N7002KDW Q55B — R1157 *short 0402 — SMB_ME1_CLK

modify 3/21

XDP/DDR

+3V

[17,18,19,20] PCH_SMBDATA — R723 4.7K_1%_4 — 2N7002KDW Q66A — SMB_PCH_DAT

[17,18,19,20] PCH_SMBCLK — R726 4.7K_1%_4 — 2N7002KDW Q66B — SMB_PCH_CLK

modify 8/9

CNVi

+3V_DEEP_SUS +1.8V_DEEP_SUS

R498 10K_1%_4 — Q38A — CNV_RF_RESET#_C

R473 4.7K_1%_4 — Q38B — CNV_RF_RESET# [50]

PJX138K

Modify the circuit 10/19

Add 10/18 Intel#571006

R460 10K_1%_4 — Q35A — MODEM_CLKREQ_C

R468 4.7K_1%_4 — Q35B — MODEM_CLKREQ [50]

PJX138K

GPP_C5/SML0ALERT#
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)

+3V_DEEP_SUS — R577 *4.7K_1%_4 — SML0ALERT# — R476 100K_1%_4

modify 8/9

RTC Circuitry(RTC)

RTC Power trace width 20mils.

+3VPCU — D58 BAT54CW — +3V_RTC_0 — R566 1K_1% 4 — +3V_RTC

30mils

+3V_RTC — R619 20K_5%_4 — RTC_RST# — C489 1u/6.3V_4 — J1 *SHORT_PAD

R618 20K_5%_4 — SRTC_RST# — C488 1u/6.3V_4 — C476 1u/6.3V_4

(20mils)

update footprint to bat-aaa-bat-046-k03-2p-smt and change pin defined 4/17

CN6 50273-0020N-V09

modify 8/9

SYSPWOK

+3V_DEEP_SUS — C881 *0.1u/10V_2

SYS_PWROK — U42 *NL17SZ08DFT2G — EC_PWROK — EC_PWROK [57] / IMVP_PWRGD [2,65]

R1019 *0_5% 4

R1023 *short 0402

R1006 *10K_1%_2

EC_PWROK_R — R1108 *short 0402 — PCH_PWROK [57]

SYS_PWROK_R — R1073 *0_5% 4 — R1024 *0_5% 4 — EC_PWROK

DP_PWROK

DPWROK_R — R960 680K_1% 4

SYS_PWROK_R — R1032 10K_1% 2

PCH_RSMRST# — R951 *10K_1% 2

modify 8/9

TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)

ACZ_SPKR — R1040 20K_1%_4

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB

+3V_DEEP_SUS — R1103 150K_1%_4 — SMB1ALERT# — R1071 *20K_1%_4

modify 8/9

TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)

LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

+3V_DEEP_SUS — R575 4.7K_1%_4 — SMBALERT# — R574 *20K_1%_4

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	1A
Date: Friday, May 03, 2019	Sheet 10 of 78	

HSIO MUX PORT	
PCIE1-8	NC
PCIE9-12	SSD1 SATA/PCIE * 4
PCIE13	HDD (SATA2)
PCIE14	LAN
PCIE15	WLAN
PCIE16	NC
PCIE17-20	Apline Ridge
PCIE21-24	SSD2 PCIE * 4

CNVi

Modify 8/10

EMI RESERVE

SSD1 PCIE x4

LAN

HDD SATA

SSD1 PCIE x4

modify it 9/20

TBT PCIE x4

2/5 modify

RESERVE

24-MHz Crystal Specifications (Sheet 2 of 2)

Parameter	Symbol	Recommended Value
Temperature Stability	Df/f$_o$	±30ppm
Aging	Df/f$_o$	±5ppm
Crystal Loading	C$_{load}$	18-20pF

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

01/31 Modify value and Y5 PN

Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz

chang P/N to CS84872FB11 8/18

48.7 ohm no symbol link

Swap SSD2 and TBT REQ for PCIE SSD RAID 2/1

Swap SSD2 and TBT CLK for PCIE SSD RAID 2/1

SSD1

GFX

LAN

WLAN

SSD2

TBT

CNVI for WLAN

Close PCH

modify 8/9

modify 10/20

HRESET

VCCIO Power Gate control for C10

For SSD1 Det

SSD SATA I/F --> H

SSD PCIE I/F --> L

stuff R1037 and unstuff R1039 for PCIE SSD RAID 2/1

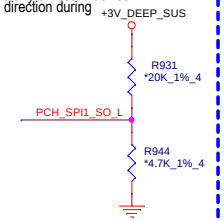
Add 12/19

Quanta Computer Inc.			
PROJECT : ZGE			
Size	Document Number		Rev
	PCH 3/7 (SATA/LPC/CLK)		1A
Date: Friday, May 03, 2019	Sheet 11 of 78		

PCH Strap Pin

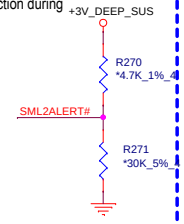
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

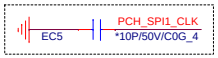


ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

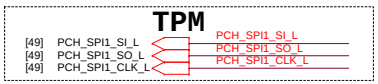


EMI RESERVE

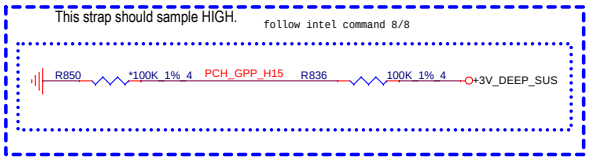


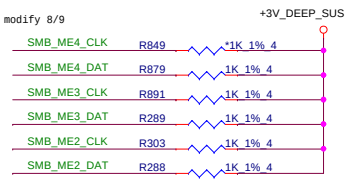
PLTRST#(CLG)

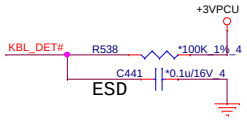
TPM



This strap should sample HIGH.

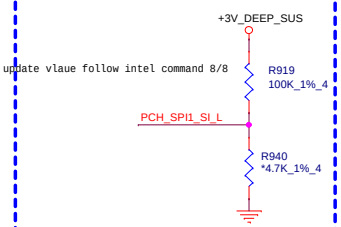






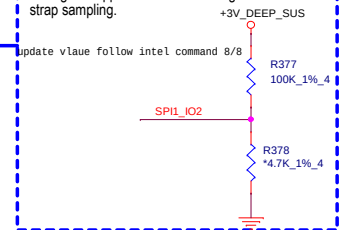
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



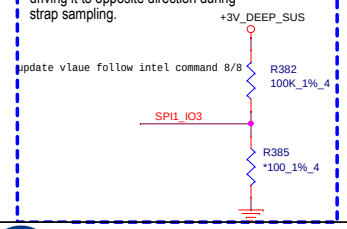
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

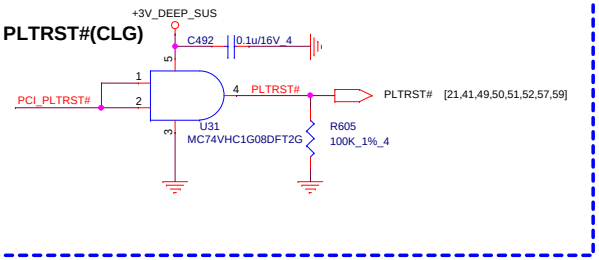


RESERVED

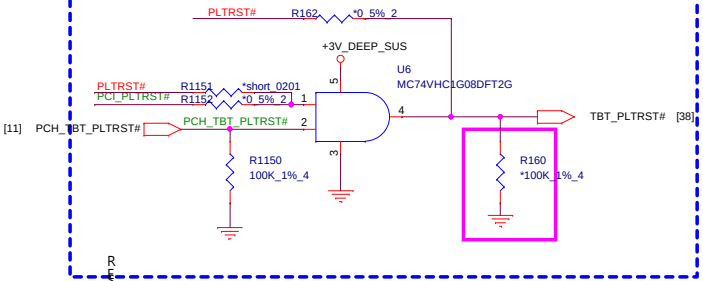
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



PLTRST#(CLG)



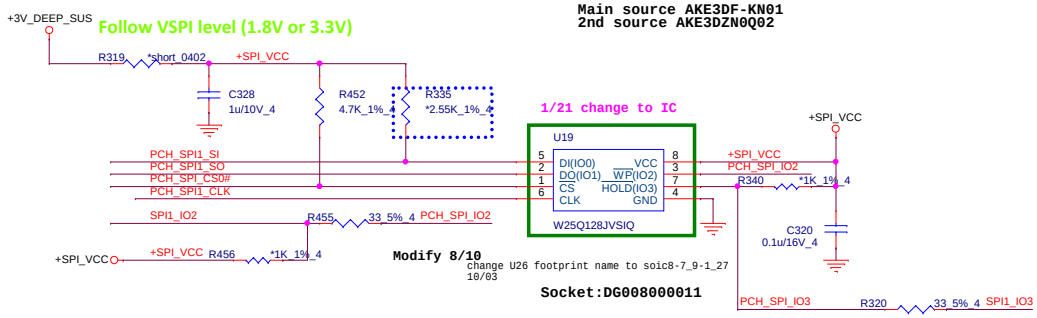
TBT_PLTRST# (RTD3)



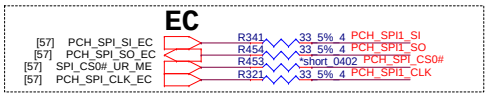
PCH SPI ROM(CLG)

PCH SOIC 208 mils 16MB
SPI ROM Socket

Main source AKE3DF-KN01
2nd source AKE3DZN0Q02



EC



Modify 8/10

Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: PCH 4/7 (GPIO/MISC)	Rev: 1A
Date: Friday, May 03, 2019	Sheet 12 of 78	

[2,9,10,11,12,14,16,39] +3V_DEEP_SUS

Boot BISO Destination: HIGH=LPC, LOW=SPI
GPP_B22 LOW

Modify 8/10

U14K

R1036 100K_1%_4 GSPI1_MOSI
[23] GPUEVENT#_PCH
[23] GC6FBEN_Q
R1094 *short_0402
[23] DGPU_PWROK_Q

[25] DGPU_PWR_EN
[21] DGPU_HOLD_RST#
TP108
modify 10/20

TP107
BBS_BIT1
GPP_C11
[54] TPD_INT#_PCH
+3V_DEEP_SUS
R1110 10K_1%_2

GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GSPI0_MOSI
DGPU_PWR_EN
DGPU_HOLD_RST#
GPP_B15
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
UART2_CTS#
UART2_RTS#
UART2_TXD
UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
I2C1_SCL
I2C1_SDA
I2C0_SCL
I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

PCH_CFL-H_874P

Modify 8/10

TBT_FORCE_PWR_R R941 *short_0402 TBT_FORCE_PWR [38]
BOARD_ID0 [32]
BOARD_ID1 [32]
BOARD_ID2
BOARD_ID3
R547 *short_0402 LCD_OD_EN# [32]
BOARD_ID4
BOARD_ID5
BOARD_ID6
BOARD_ID7
BOARD_ID8
BOARD_ID9
BOARD_ID10
BOARD_ID11
BOARD_ID12
BOARD_ID13

Add R1219 for intel#571006 10/18
+3V
GPP_H21 R895 10K_1%_4
GPP_H21 = XTAL Frequency Select

EMI RESERVE

EC6 I2C1_SCL *10P/50V/C0G_4 [38] TBT_HTPLG_NL5
R1055 *short_0402 UART2_CTS#
S_GPIO R1056 *short_0402 UART2_RTS#
UART2_TXD
UART2_RXD

TBT3
TPD
[40] I2C1_SCL
[40] I2C1_SDA
[54] I2C0_SCL
[54] I2C0_SDA

RESERVED

BOARD_ID0	BOARD_ID1	OD_EN	PWM pin	NSVR pin	Support panel
0	0	NC	Reserve	Reserve	Reserve
1	0	NC	NC	Y	NSVR
1	1	NC	Y	NC	DD/Normal
0	1	Reserve	Reserve	Reserve	Reserve

+3V_DEEP_SUS

Modify 8/10

I2C0_SCL R451 2.2K_5%_4
I2C0_SDA R438 2.2K_5%_4
I2C1_SCL R1057 2.2K_5%_4
I2C1_SDA R483 2.2K_5%_4
GPP_C11 R1059 100K_1%_4
UART2_CTS# R1048 *49.9K_1%_4
UART2_RTS# R1099 2.2K_5%_4
UART2_TXD R484 *49.9K_1%_4
UART2_RXD R1008 *49.9K_1%_4
change R331 to 2.2K and stuff it for TBT HPD 11/29

+3V

DDPC_CLK R862 *10K_1%_4
DDPC_DATA R880 *10K_1%_4
DDPB_CLK R874 *10K_1%_4
DDPB_DATA R893 *10K_1%_4
DDPD_CLK R888 *10K_1%_4
DDPD_DATA R902 *10K_1%_4
SKTOCC_N_R R900 *100K_1%_4

+3V_DEEP_SUS

modify 8/8

R1058 *100K_1%_4 BOARD_ID0 R1106 10K_1%_4
R1052 *100K_1%_4 BOARD_ID1 R1091 10K_1%_4
R970 *10K_1%_4 BOARD_ID2 R991 SUB@10K_1%_4
R487 *10K_1%_4 BOARD_ID3 R544 10K_1%_4
R1045 10K_1%_2 BOARD_ID4 R1090 *10K_1%_2
R548 i7@10K_1%_4 BOARD_ID5 R554 *i9@10K_1%_4
R497 iTPM@10K_1%_4 BOARD_ID6 R549 *dTPM@10K_1%_4
R1041 *NVL@10K_1%_4 BOARD_ID7 R1102 VL@10K_1%_4
R1051 N-Tobii@10K_1%_4 BOARD_ID8 R1101 *Tobii@10K_1%_4
R1050 *N-Macro@10K_1%_4 BOARD_ID9 R1100 Macro@10K_1%_4
R539 *10K_1%_4 BOARD_ID10 R580 10K_1%_4
R1124 *Max-Q@10K_1%_4 BOARD_ID11 R1125 Max-P@10K_1%_4
R578 *N-GS@10K_1%_4 BOARD_ID12 R581 GS@10K_1%_4
R545 *OP@10K_1%_4 BOARD_ID13 R616 DIS@10K_1%_4

Unstuff TBT_DP_HDP from ZGQ
Change to stuff by NV FAE's suggestion 0326

TBT
[23,37,38] TBT_DP_HPD
R1004 *short_0402 DDPB_HPD0
DP_HPD_PCH_R
HDMI_HPD_PCH_R
SIO_EXT_SCI#
[57] SIO_EXT_SCI#
+3V_DEEP_SUS
R907 10K_1%_2
[32] EDP_HPD_CPU
EDP_HPD_CPU

U14E

GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DDPD_HPD2/DISP_MISC2
GPP_I3/DPPE_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F23/DDPF_CTRLDATA
GPP_F22/DDPF_CTRLCLK
GPP_F14/EXT_PWR_GATE#/PS_ON#
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
5 OF 13

DDPB_CLK
DDPB_DATA
DDPC_CLK
DDPC_DATA
DDPD_CLK
DDPD_DATA
TP95
TP100
SKTOCC_N_R [2]
GPP_K21

PCH_CFL-H_874P

Modify 8/10

+3V
R1089 *1K_1%_4 EDP_HPD_CPU R1054 100K_1%_4
R1065 *10K_1%_2 DGPU_PWR_EN R1034 10K_1%_2
R1163 10K_1%_2 GC6FBEN_Q R1164 *10K_1%_2
R1062 *10K_1%_2 DGPU_HOLD_RST# R1031 10K_1%_2
R1122 10K_1%_2 DGPU_PWROK_Q R1081 *10K_1%_2

+3V
R781 1M_1%_4
[23,33] DP_HPD_PCH
R789 *100K_1%_4
DP_HPD_PCH_R
Q70A PJX138K

update BOM 10/20

+3V
R798 1M_1%_4
[23,35] HDMI_HPD_PCH
R783 *100K_1%_4
HDMI_HPD_PCH_R
Q70B PJX138K

NV GSYNG STRAP

BOOT SELECT STRAP

HIGH:LPC
LOW: SPI. (Default)
+3V_DEEP_SUS
R1105 *4.7K_1%_4
S_GPIO
R1104 *20K_1%_4

NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)
+3V
R546 4.7K_1%_4
BBS_BIT1
R536 *20K_1%_4

RESERVED

This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

Intel ME STRAP

+3V_DEEP_SUS
R856 *100K_1%_4
GPP_K21
R852 *20K_1%_4

RESERVED

ID.NO	Function	Low	High
BOARD_ID11	PCB	MAXQ	MAXP
BOARD_ID12	G-SYNC	Non-GS	GS
BOARD_ID13	VGA	Optimus	d-VGA

ID.NO	Function	Low	High
BOARD_ID8	EYE Trace	NO	YES
BOARD_ID9	Macro Key	NO	YES
BOARD_ID10	Touch Panel	YES	NO

ID.NO	Function	Low	High
BOARD_ID4	Keyboard	Metal	Plastic
BOARD_ID5	CPU	i7	i9
BOARD_ID6	TPM	iTPM	dTPM
BOARD_ID7	Battery Vin Boost	NO	YES

ID.NO	Function	Low	High
BOARD_ID0	LCD Panel	No Stuff	Default
BOARD_ID1	LCD Panel	No Stuff	Default
BOARD_ID2	Sub-Woofer	No	YES
BOARD_ID3	Power Button	Metal	Plastic

Pin Name	Strap description	Sampled	Configuration	note
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R1126 *1K_1%_4 GSPI0_MOSI R1095 *100K_1%_4
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R1096 *1K_1%_4 GSPI1_MOSI

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	PCH 5/7 (GPIO)	1A

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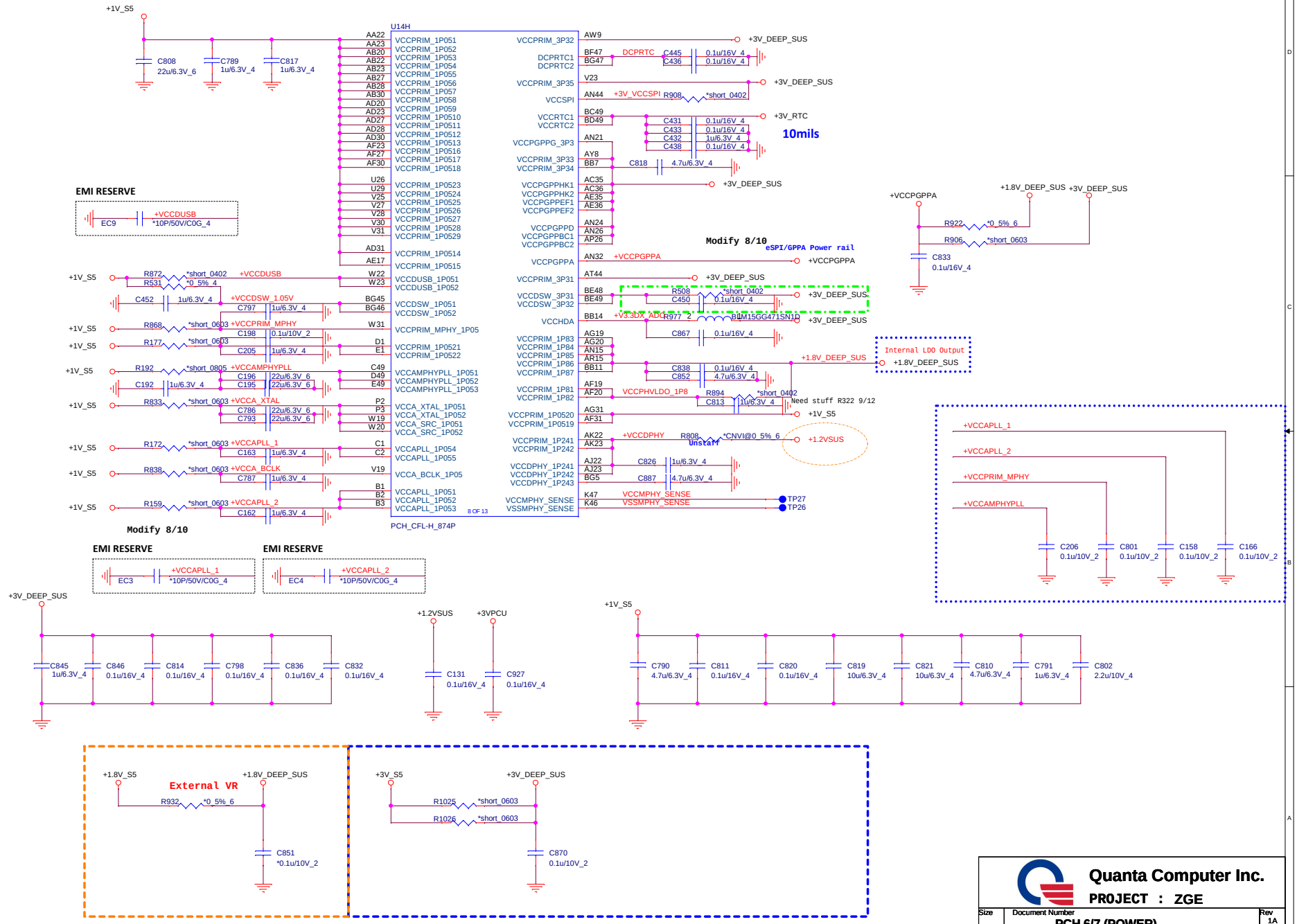
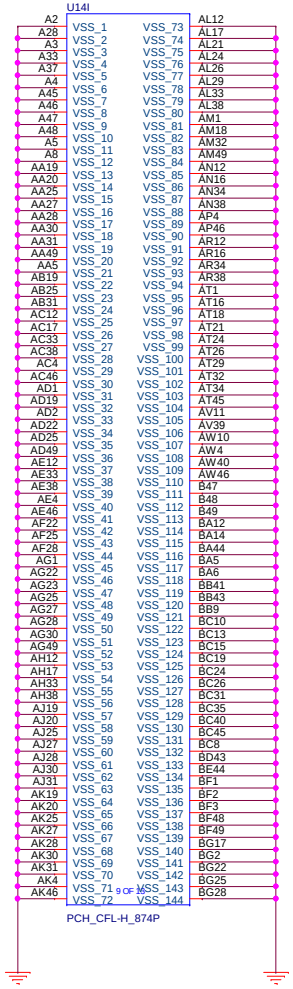
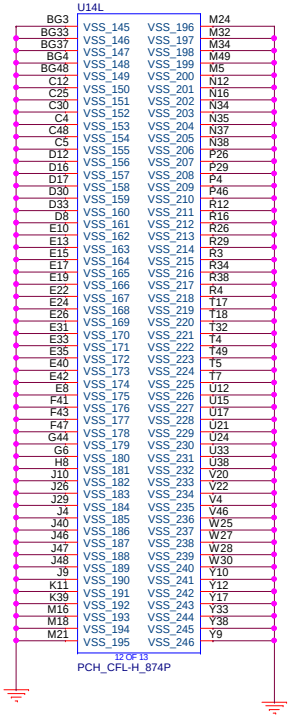
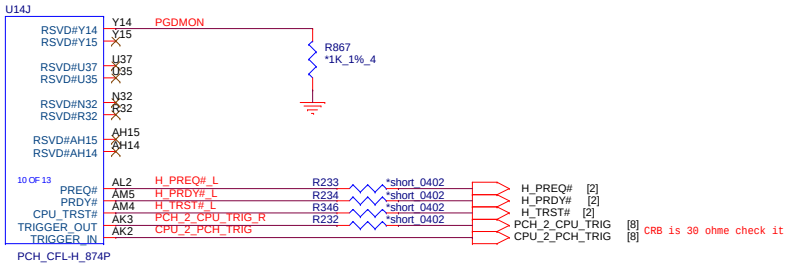
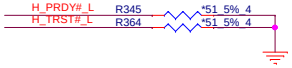


Quanta Computer Inc.			
PROJECT : ZGE			
Size	Document Number		Rev
	PCH 6/7 (POWER)		1A
Date: Friday, May 03, 2019	Sheet 14 of 78		









Quanta Computer Inc.

PROJECT : ZGE

Size	Document Number	Rev
	PCH 7/7 (GND)	1A

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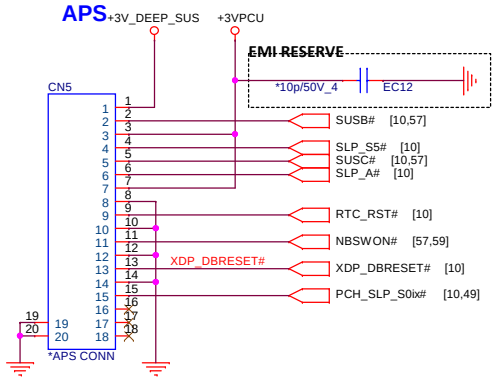
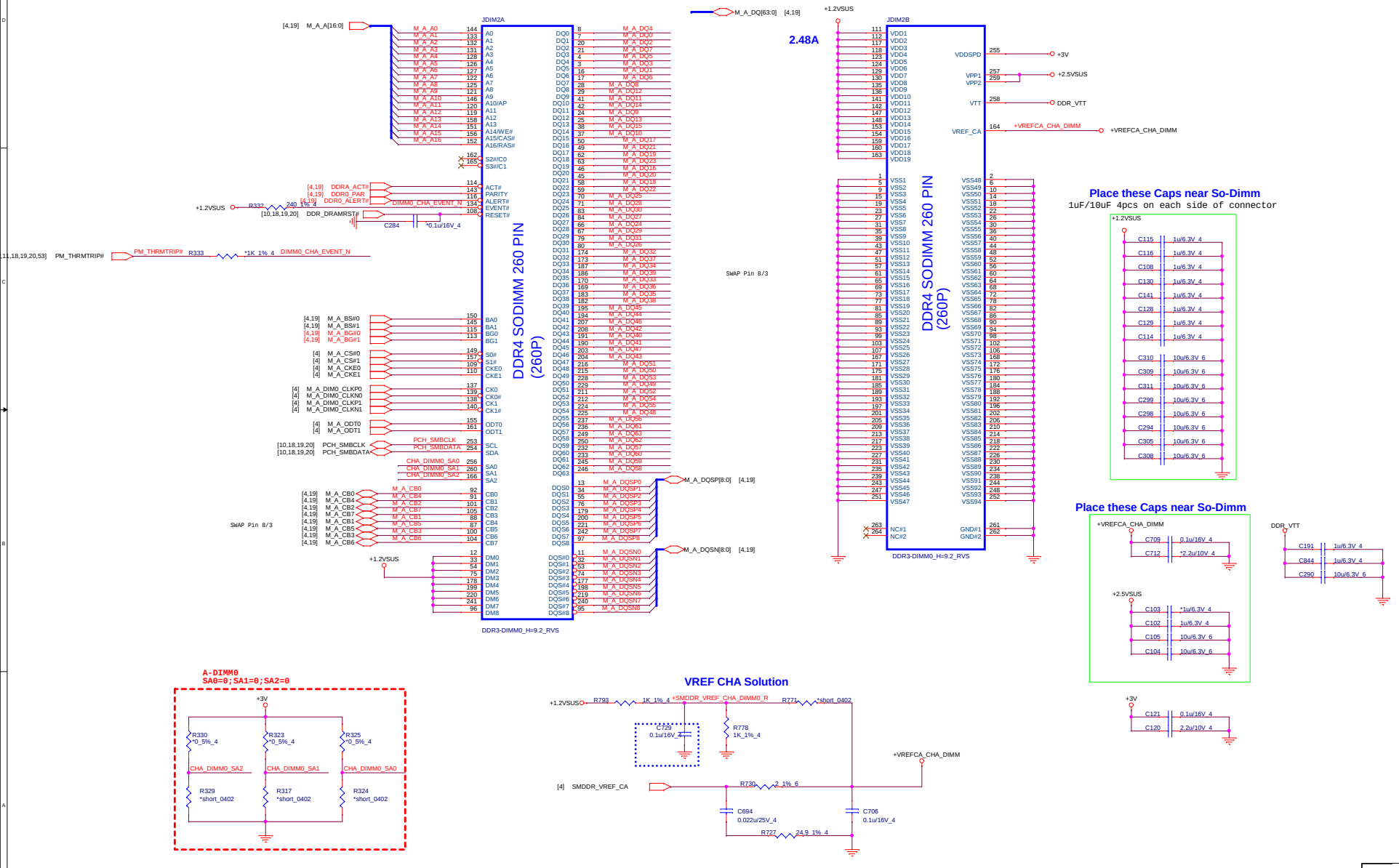


+3V_DEEP_SUS [2,9,10,11,12,13,14,39]
+3VPCU [9,10,12,14,32,37,39,40,47,54,57,59,61,62,68,70,75]

Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: XDP & APS	Rev: 1A
Date: Friday, May 03, 2019	Sheet 16 of 78	



Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	DDR4 Channel A DIMM0	1A

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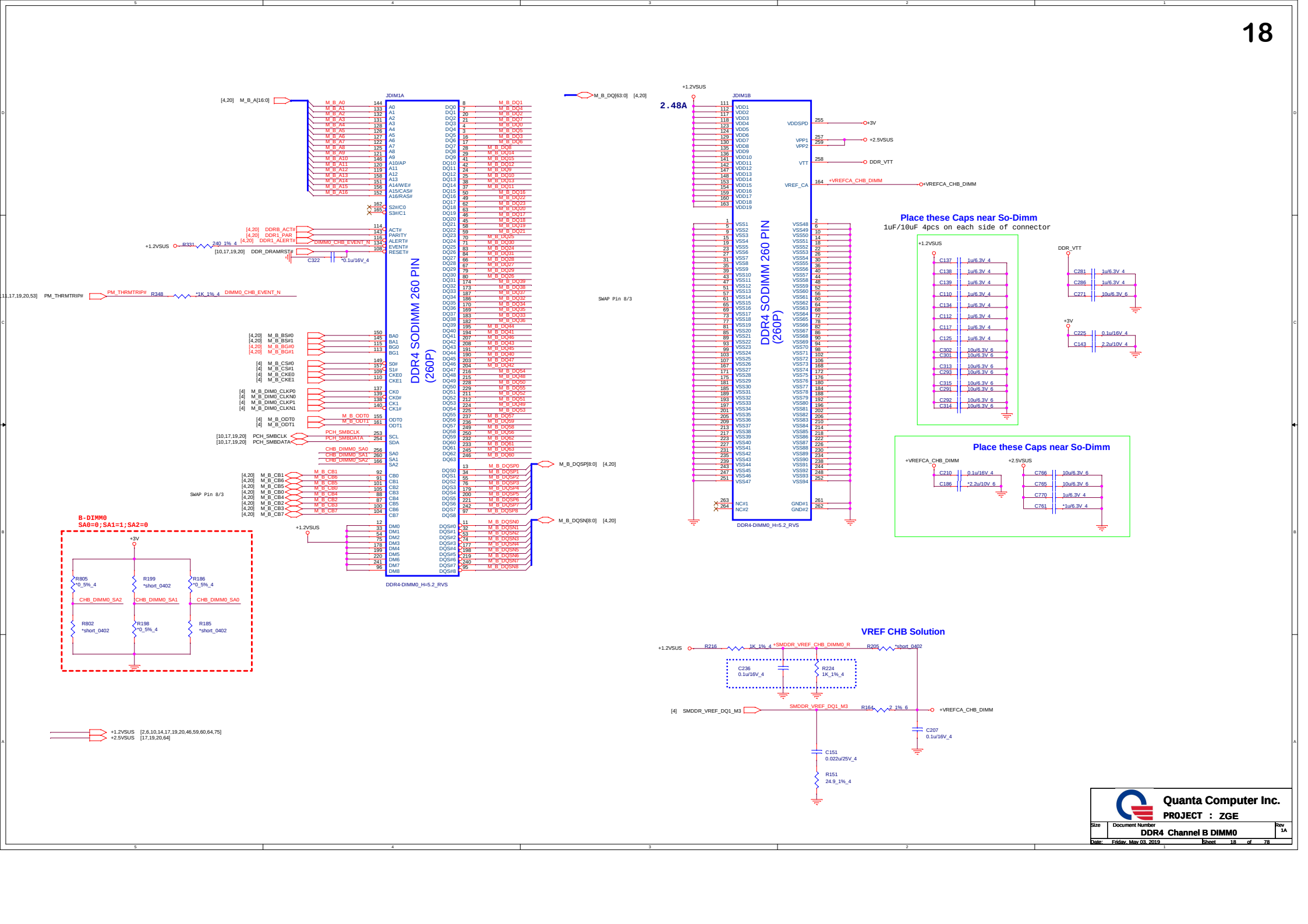
JDIM1A
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=5.2_RVS
JDIM1B
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=5.2_RVS
2.48A
SWAP Pin 8/3
B-DIMM0
SA0=0;SA1=1;SA2=0
Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector
Place these Caps near So-Dimm
VREF CHB Solution
Quanta Computer Inc.
PROJECT : ZGE
DDR4 Channel B DIMM0
Friday, May 03, 2019
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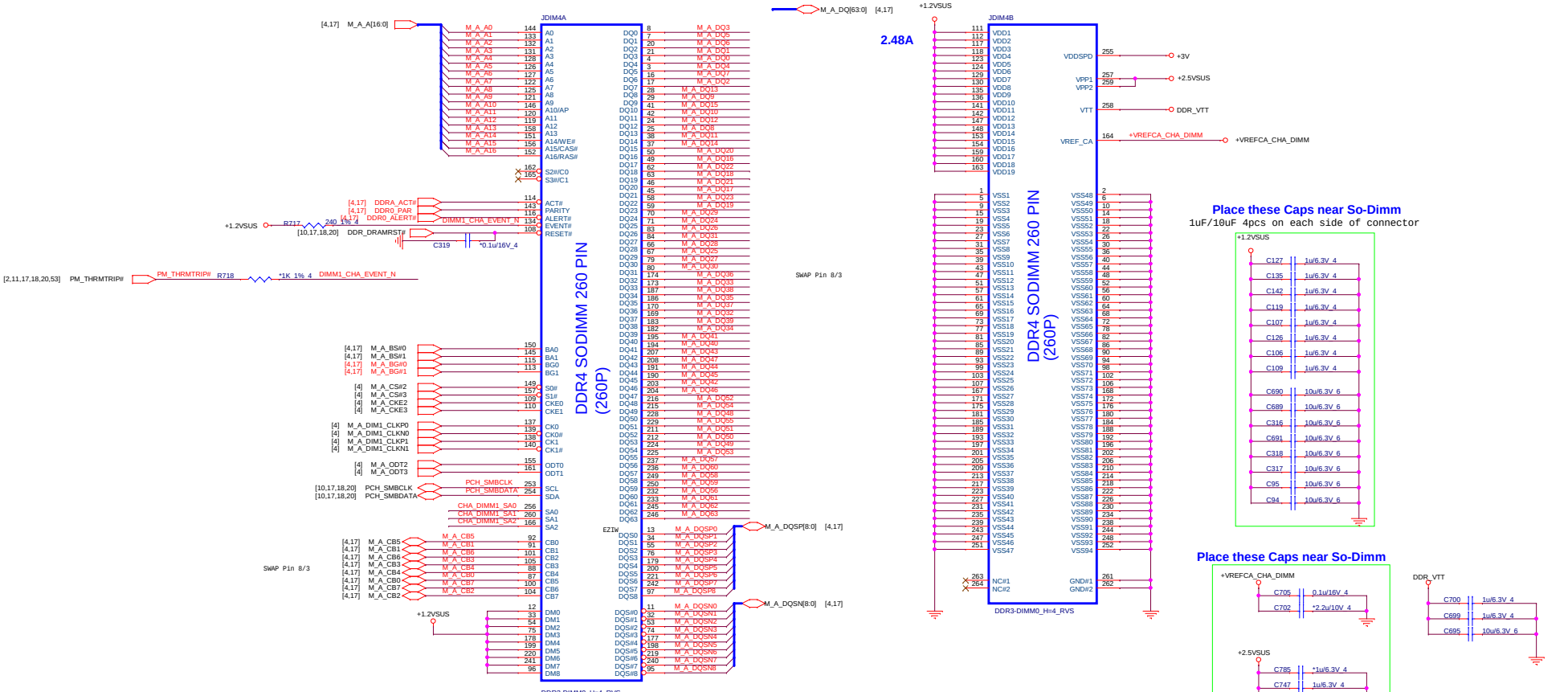
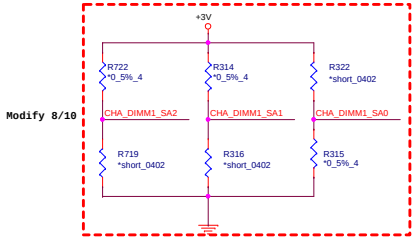
7/28 change to STD



A-DIMM1
SA0=1;SA1=0;SA2=0



Modify 8/10

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	DDR4 Channel A DIMM1	1A

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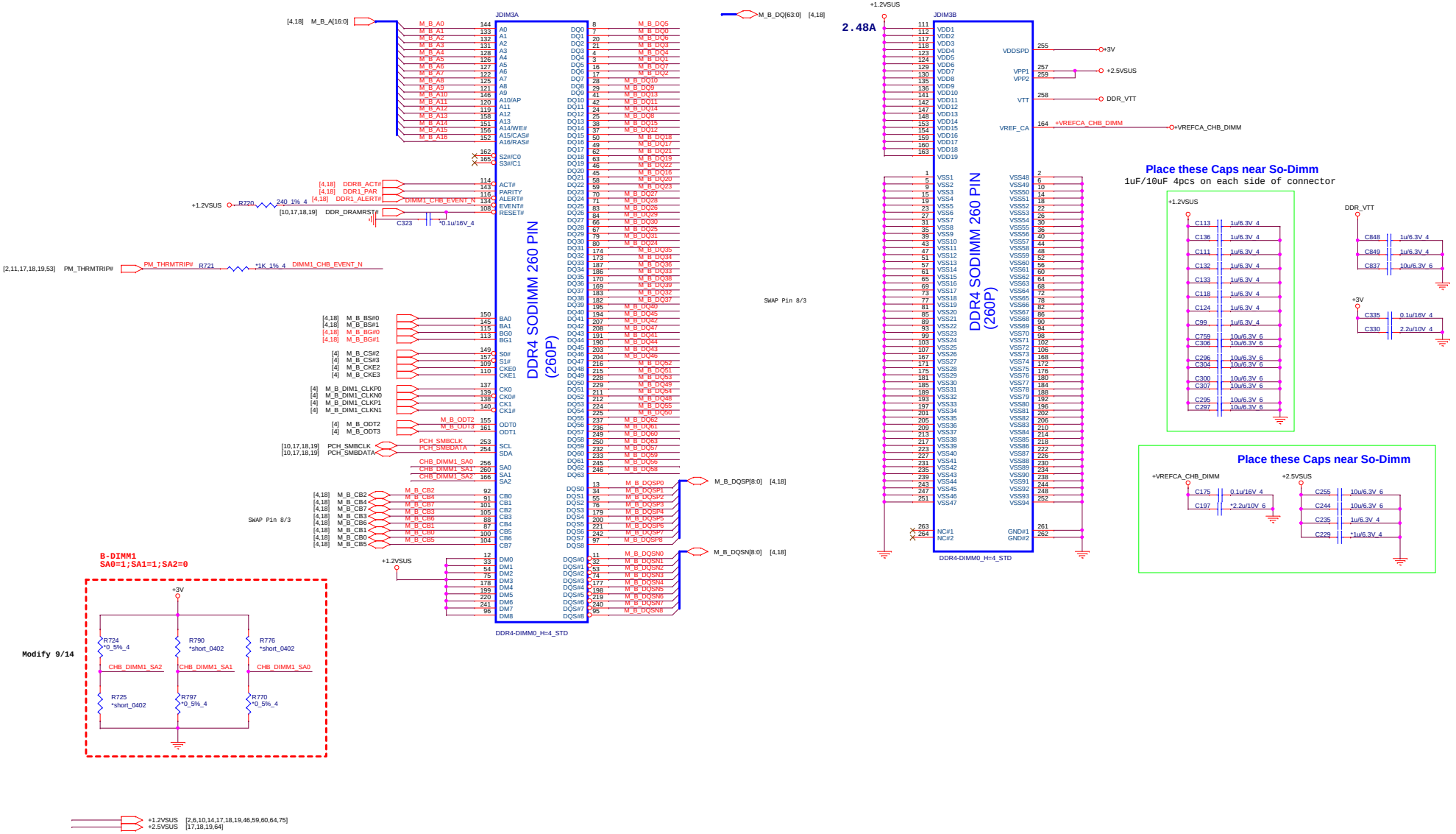
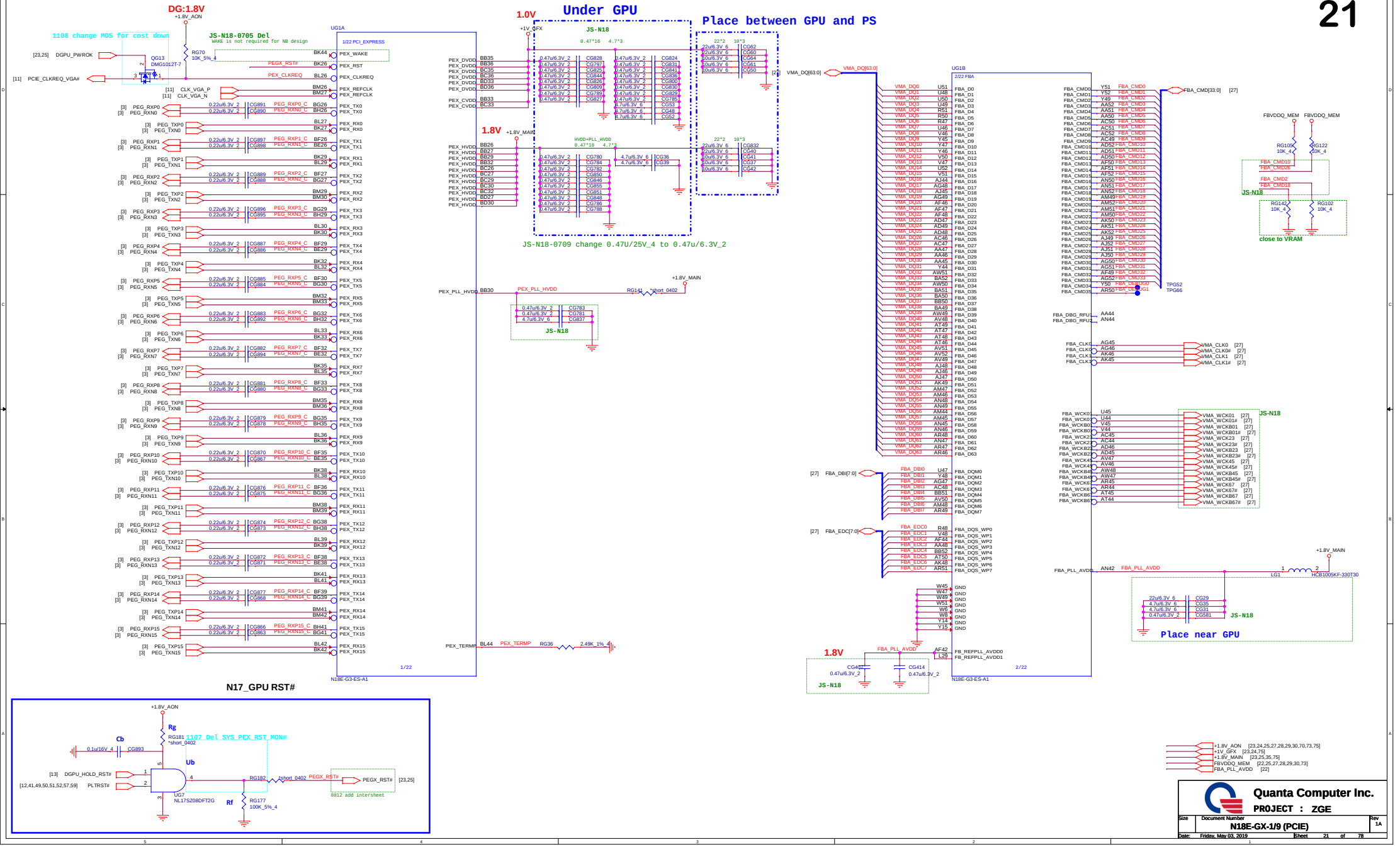
7/28 change RVS




DG:1.8V
1108 change MOS for cost down
JS-N18-0705 Del
WAKE is not required for NB design
Under GPU
Place between GPU and PS
JS-N18-0709 change 0.47U/25V_4 to 0.47u/6.3V_2
close to VRAM
Place near GPU
N17_GPU RST#
1107 Del SYS_PEX_RST_MON#
Quanta Computer Inc.
PROJECT : ZGE
N18E-GX-1/9 (PCIE)
Friday, May 03, 2019

FBVDDQ_MEM [21,25,27,28,29,30,73]
FBA_PLL_AVDD [21]

UG1C
3/22 FBB
N18E-G3-ES-A1

UG1D
4/22 FBC
N18E-G3-ES-A1

UG1E
5/22 FBD
N18E-G3-ES-A1

N18E-G3
5/22 FBD | N/A

JS-N18

close to VRAM

TBT DP/Re-Driver

JS-N18 from IFPP to IFPB

TBT DP/Re-Driver

JS-N18 from IFPP to IFPB

IFPAB

TYPE-C

PCB CO-LAYOUT

PCB CO-LAYOUT

eDP

HDMI/Re-Driver

DP

Under the GPU

Near the GPU

Close the GPU

Near the GPU

C, D share the filter

follow ZGQ

Near the GPU

E, F share the filter

follow ZGQ

For DP port, prevent backdrive leakage current into GPU

JS-N18-0702

Drax GSync SKU

Non GSync SKU

BOM:

VRAM Table for G3 GDDR6

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x1	TBD	Micron	MT61K256M32JE-14:A		AKG532BTL84	Default
0x0	TBD	Samsung	K4ZB032SBC-HC14		AKGSBG0T505	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
01010	8Gb	256-bit	Samsung
01011	8Gb	256-bit	Micron
01010	8Gb	256-bit	Hynix
01110	16Gb	256-bit	Hynix
01111	16Gb	256-bit	Samsung
01100	16Gb	256-bit	Micron

JS-N18E change to 8Mb

BOM:

	Description	Size	P/N
N18E-G3	W25QR8EWSNIG	8Mb	AKE5GGN0N02
N18E-G3	GD25LQ80CTIGR	8Mb	AKE5GF00Q01
N18E-G2	MX25UB033EM1I-12G	8Mb	AKE5GFP0Z02

JS-N18E-TBD

For ICT test

JS-N18 8706

JS-N18-0706

JS-N18 DEL

JS-N18-0705

JS-N18-0708 50ohm

JS-N18 8706

HDMI-HPD

DP HPD

eDP HPD(For G-Sync)

TBT HPD1

0712: CG106 change to 0201

0712: CG107 change to 0201

0712: CG108 change to 0201

0712: CG109 change to 0201

Throttle

Event

Overt shutdown

JS-B106 follow WBC

GP1012 AC detect
AC high
DC low

Nvidia : suggest to connect this pin to EC only

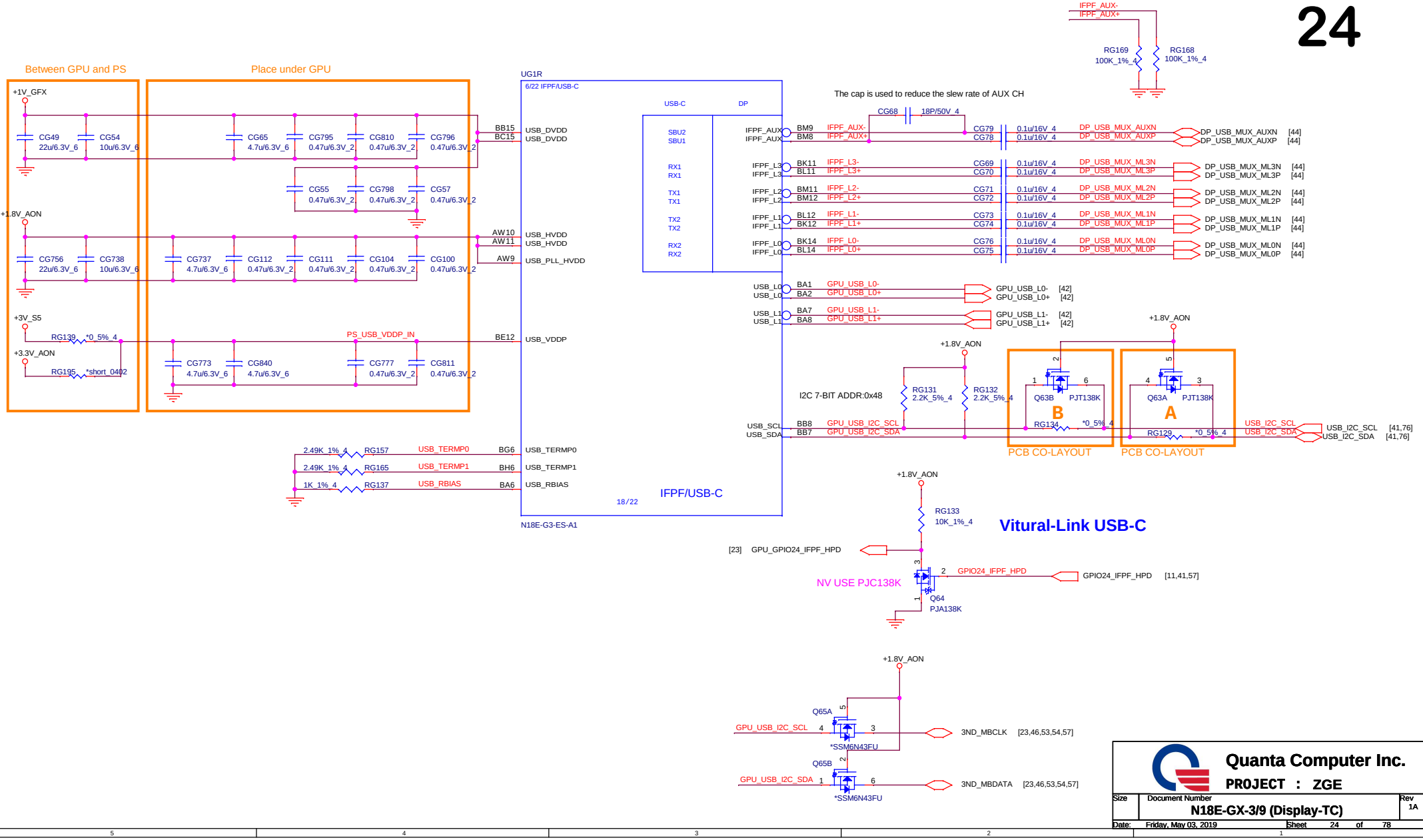
Table 14.1 GPIO Descriptions for Package GB48-256 (Continued)

GPIO Pin Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO31	LCD_BLEN		LCD Panel Backlight enable	100K Pull Down
GPIO22	DNVPROT_N			2.2K Pull Up, see circuit
GPIO23	RASTER_SYNC1			100K Pull Down
GPIO24	HPD_PPP*/GBC_HPD* or DONGLE_DET*	I	Hot plug detect for PPP or USBC	10K Pull Up to VIN, 10K ADH
GPIO25	FSYNC_PD	O		Pull up/pull down with series resistor depending on PD topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_PPC*	I	Hot plug detect for PPC	10K Pull Up to VIN_ADH
GPIO28	PAL_HT* / ADC_AUX_SEL			10K Pull Up
GPIO29	ECE_BL_SW			10K Pull Down
GPIO30	UNUSED			

Table 14.1 GPIO Descriptions for Package GB48-256 (Continued)

GPIO Pin Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO1	GC6-SCA_FB_EH	O		10K Pull Down
GPIO2	GC6-SCL_EVENT*	I		10K Pull Up
GPIO3	UNUSED	O		
GPIO4	CC6-THR_MARK_EN	O		10K Pull Up
GPIO5	FRAME_LOCK*	I	Frame lock	10K Pull UP/...
GPIO6	HIVIDEO_PD*	O	Phase Shedding per Section 10.4.3*	PU/PD with series resistor depending on PD topology
GPIO7	LCD_BL_PWM	IO	LCD Panel Backlight PWM	10K Pull Down
GPIO8	MDA_VDD_CTL	O	Memory voltage control	8/PD depending on DIO topology
GPIO9	THERM_ALERT*	OD	Active Low Thermal Alert	10 kΩ Pull Up to VIN
GPIO10	MDA_VREF_CTL	O	Memory VREF Control	10K Pull Down
GPIO11	LCD_VCC	O		10K Pull Down
GPIO12	PWR_LEVEL	I	AC power detect or low power supply overdrive input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_PPP*	I	Hot Plug Detect for PPP	10K Pull Up to VIN_ADH
GPIO15	HPD_PPPD	I	Hot Plug Detect for PPP	10K Pull Up to VIN_ADH
GPIO16	UNUSED	O		
GPIO17	UNUSED			
GPIO18	HPD_PPC*	I	Hot Plug Detect for PPC	10K Pull Up to VIN_ADH
GPIO19	HPD_PPCC	I	Hot Plug Detect for PPC	10K Pull Up to VIN_ADH
GPIO20	Reserved	O		
GPIO21	GC6-NB_FGC6			10K Pull Down

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



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PROJECT : ZGE

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	N18E-GX-3/9 (Display-TC)	1A
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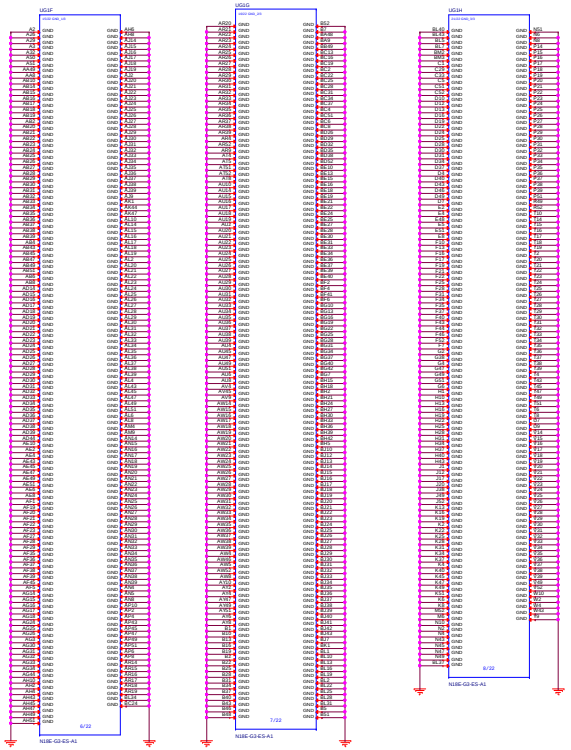
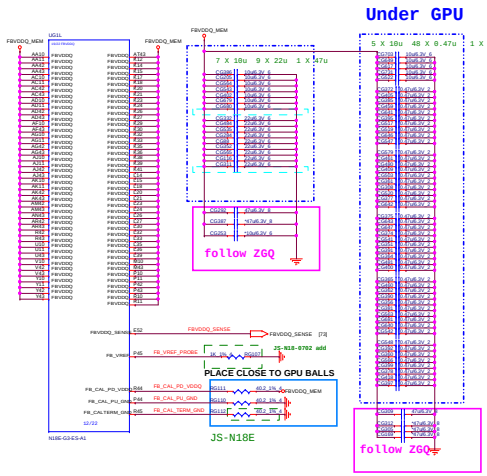
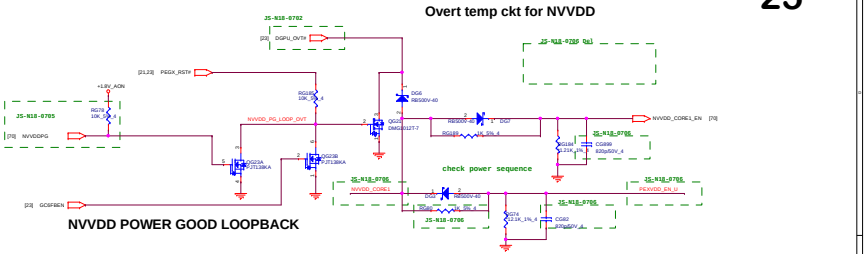
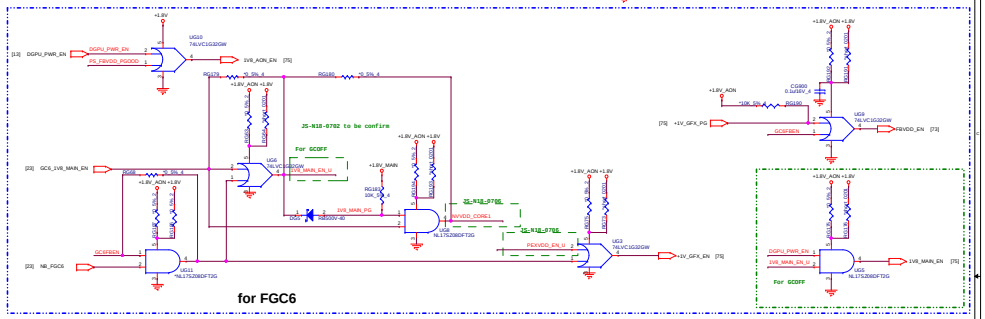
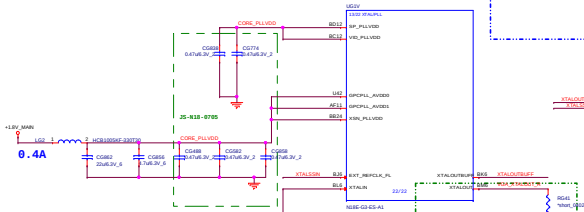


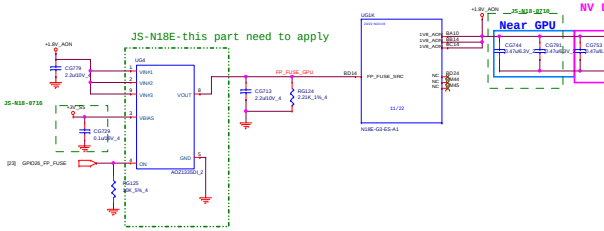


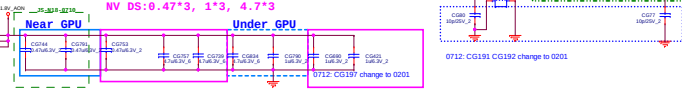


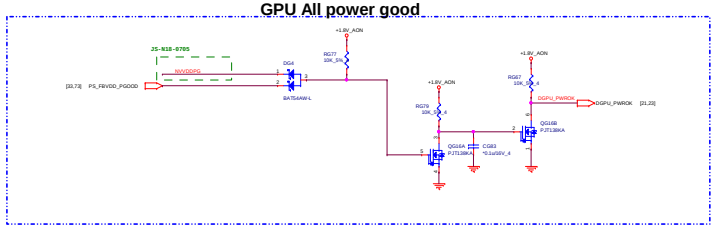


	GC6_1V8_MAIN_EN	GC6FBEN	NB_FGC6	+1.8V_AON	+1.8V_MAIN	NVVDD	+1V_GFX	FBVDDQ
POWER ON	1	0	0	ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FGC6	0	1	1	ON	ON	OFF	ON	ON









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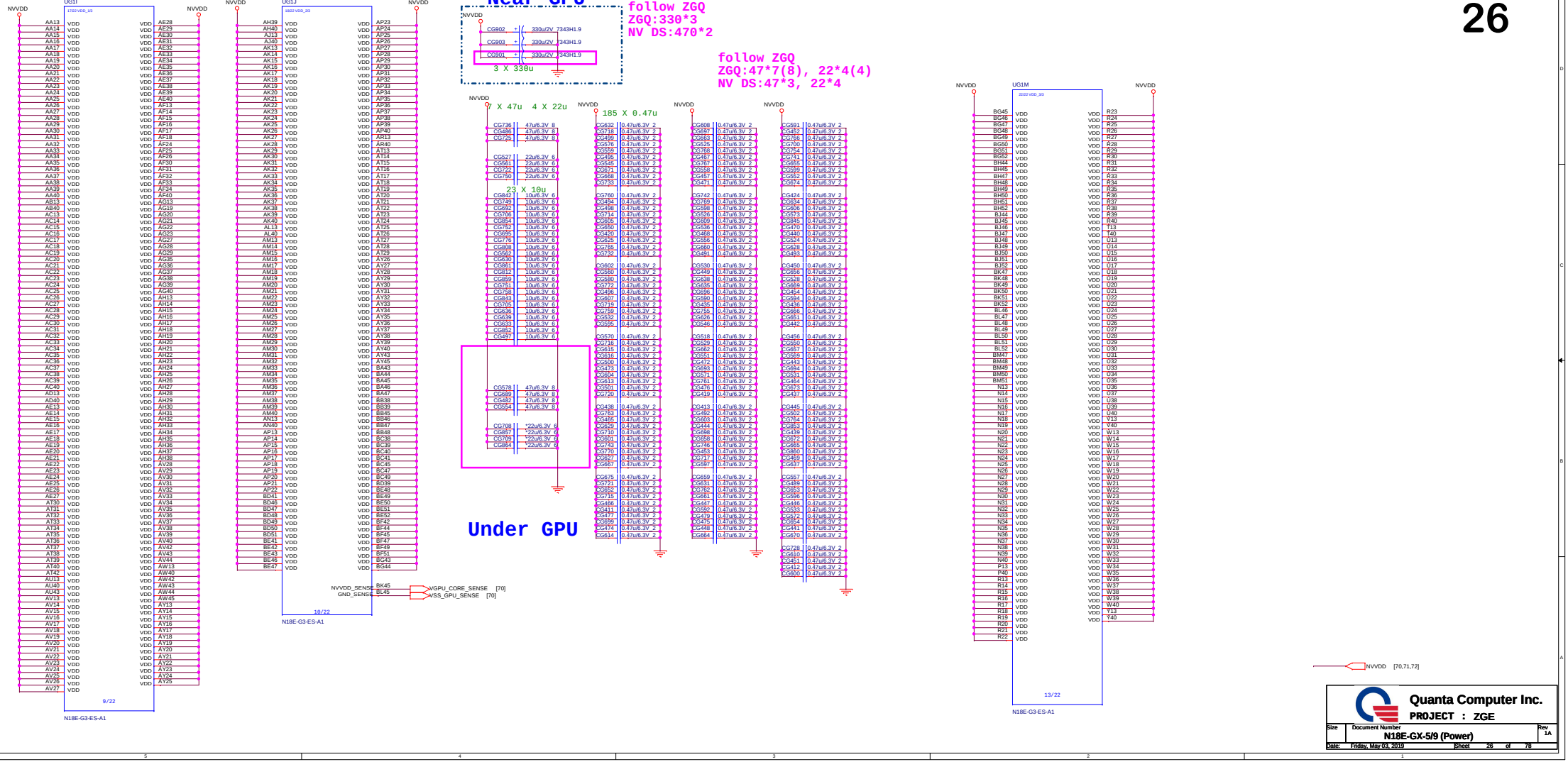
PROJECT : ZGE
N18E-GX -4/9 (MISC)



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	N18E-GX-5/9 (Power)	1A
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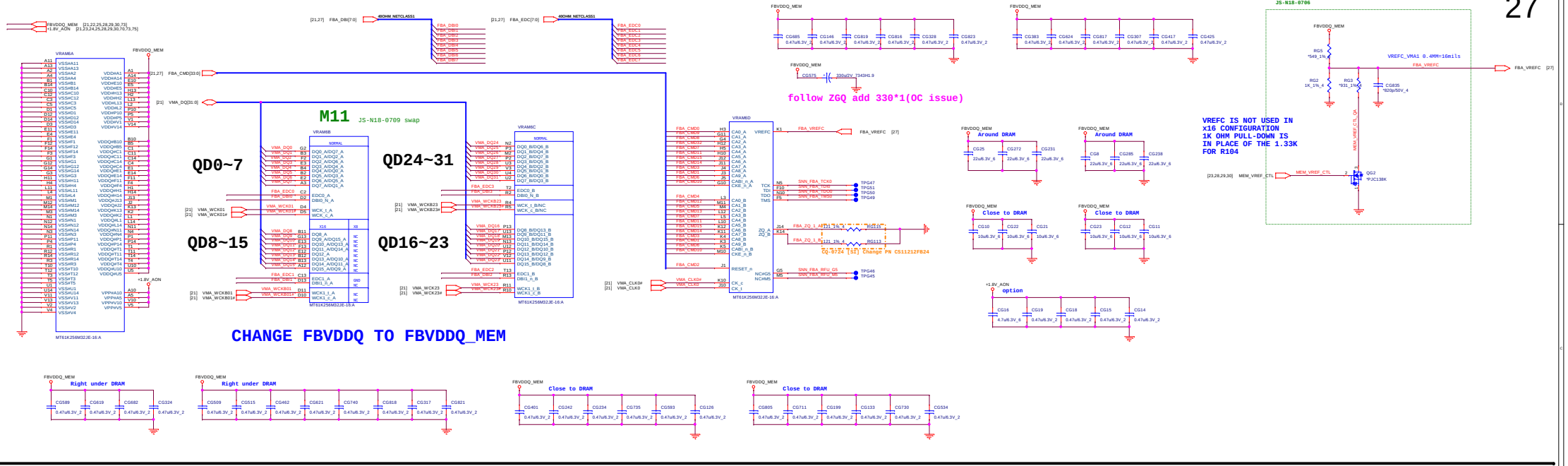
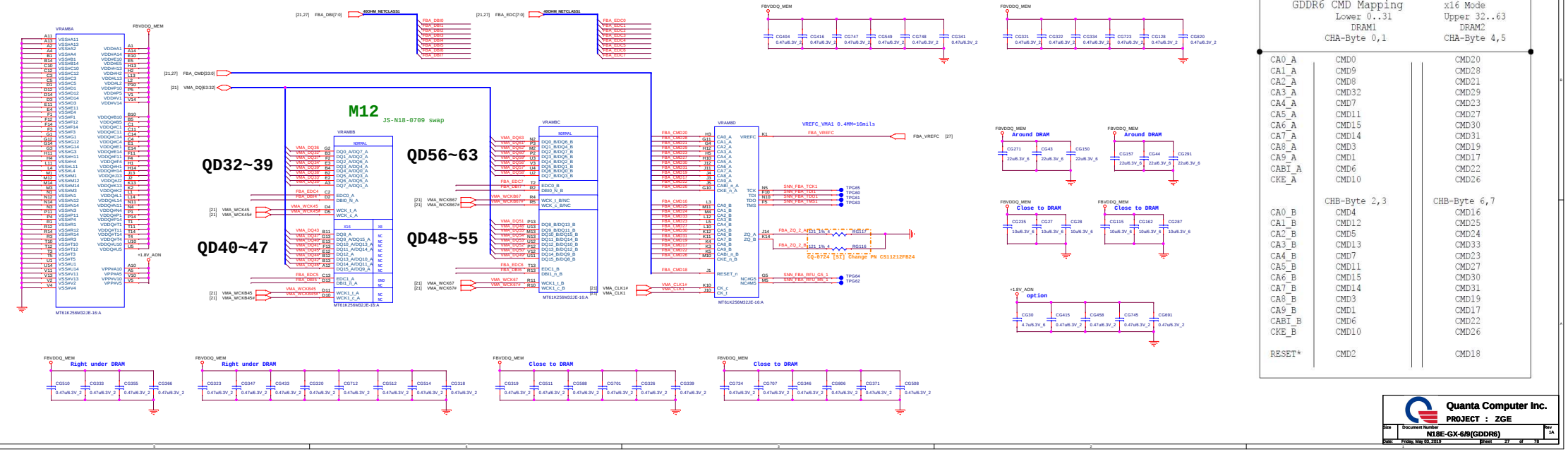
MEMORY: FBA Partition 31..0



MEMORY: FBA Partition 63..32



GDDR6 CMD Mapping		x16 Mode
	Lower 0..31	Upper 32..63
	DRAM1	DRAM2
	CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

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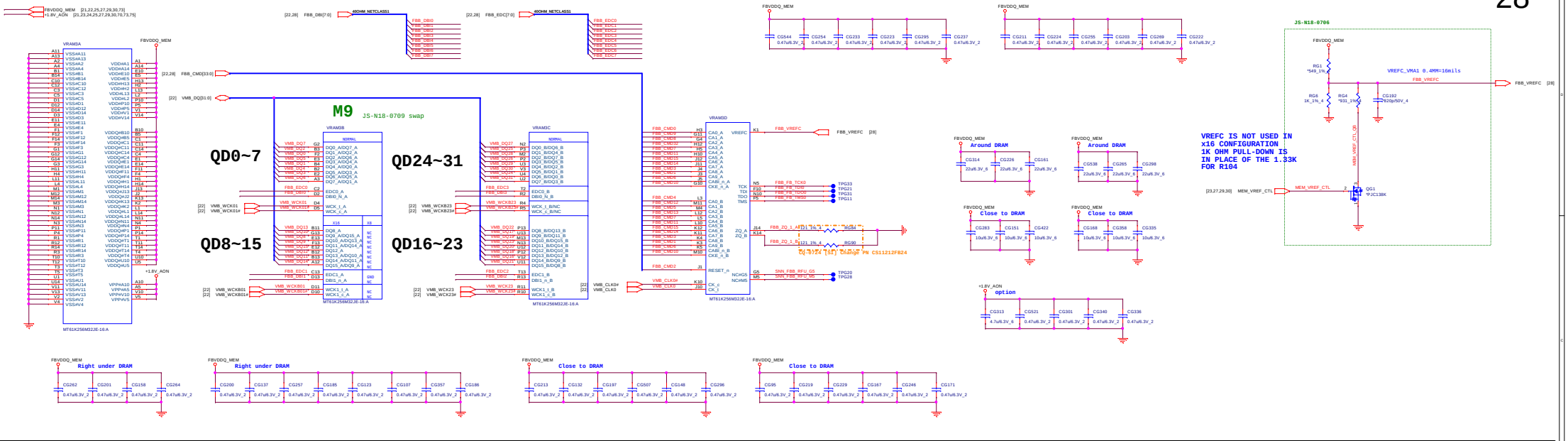
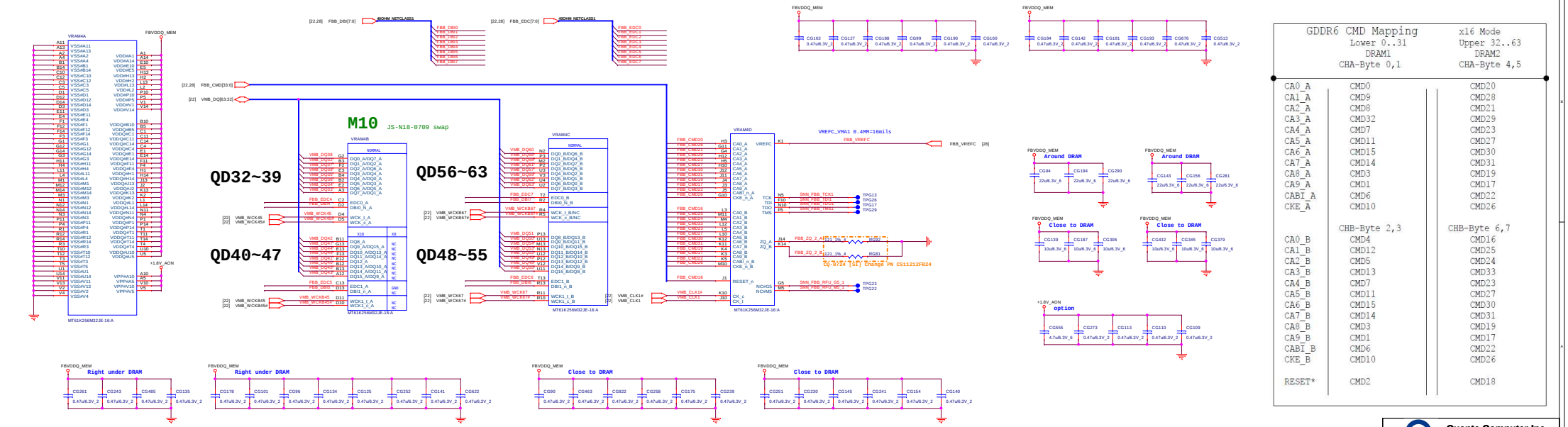
MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

Quanta Computer Inc.
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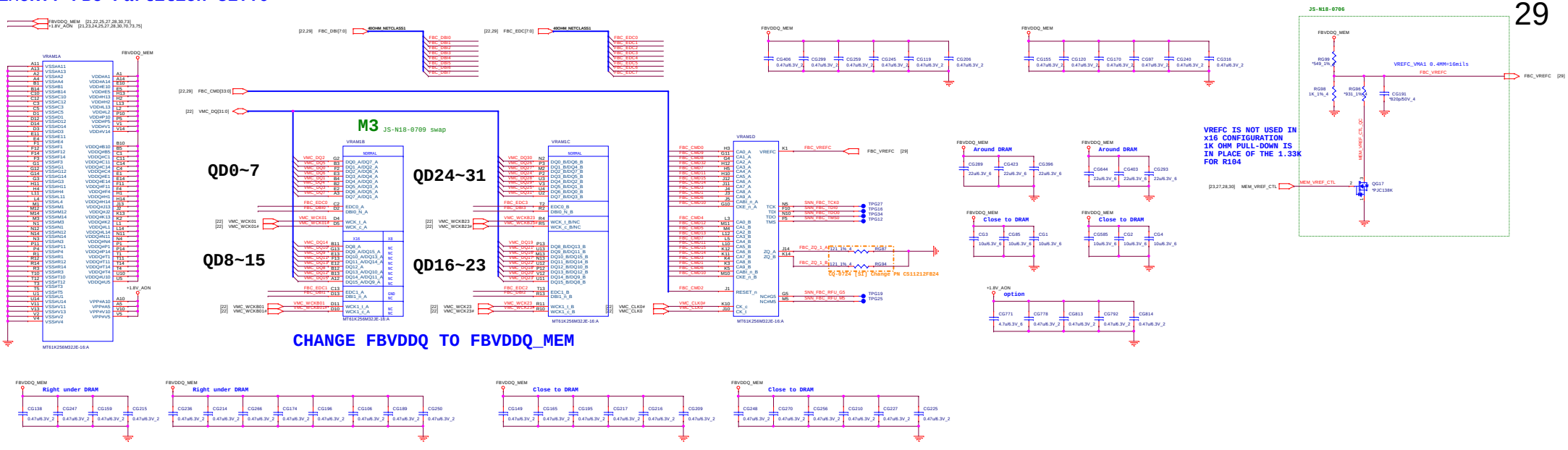
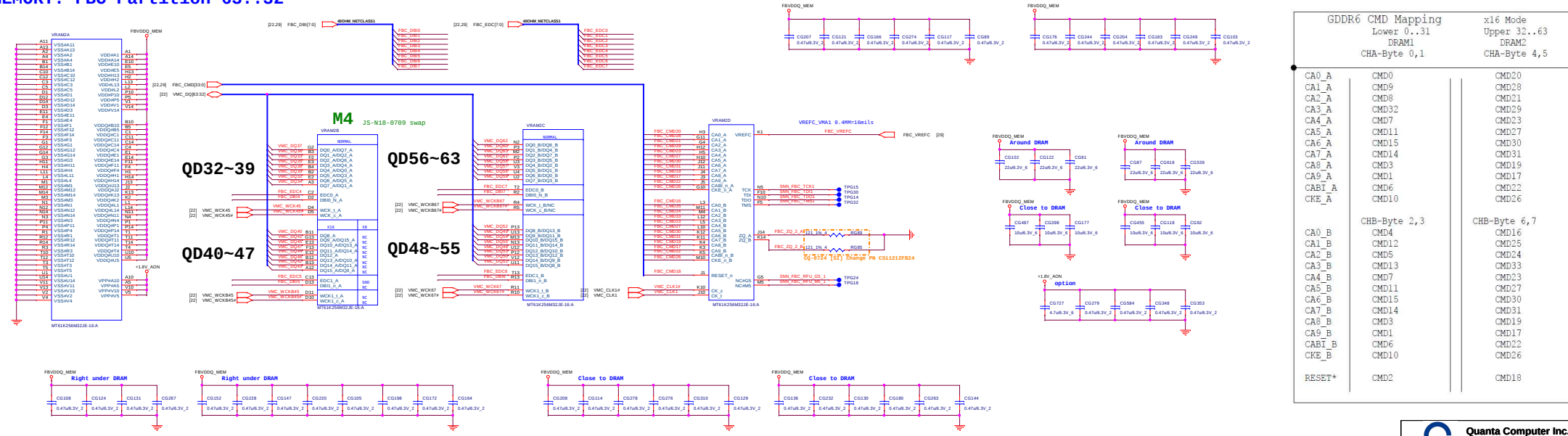
MEMORY: FBC Partition 31..0



MEMORY: FBC Partition 63..32



GDDR6 CMD Mapping	Lower 0..31 DRAM1 CHA-Byte 0,1	x16 Mode Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

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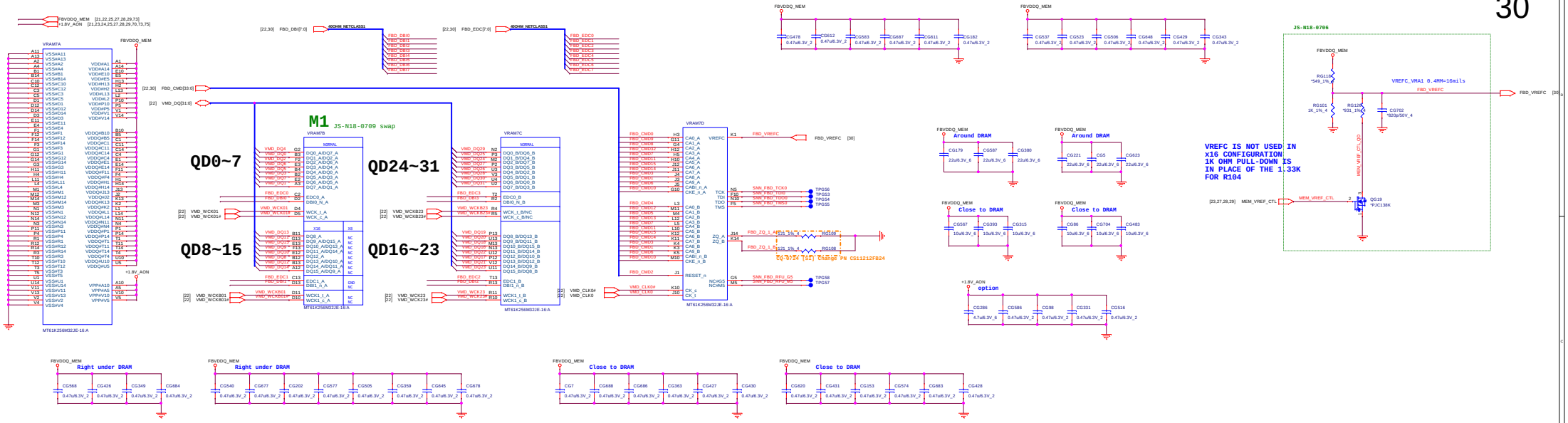
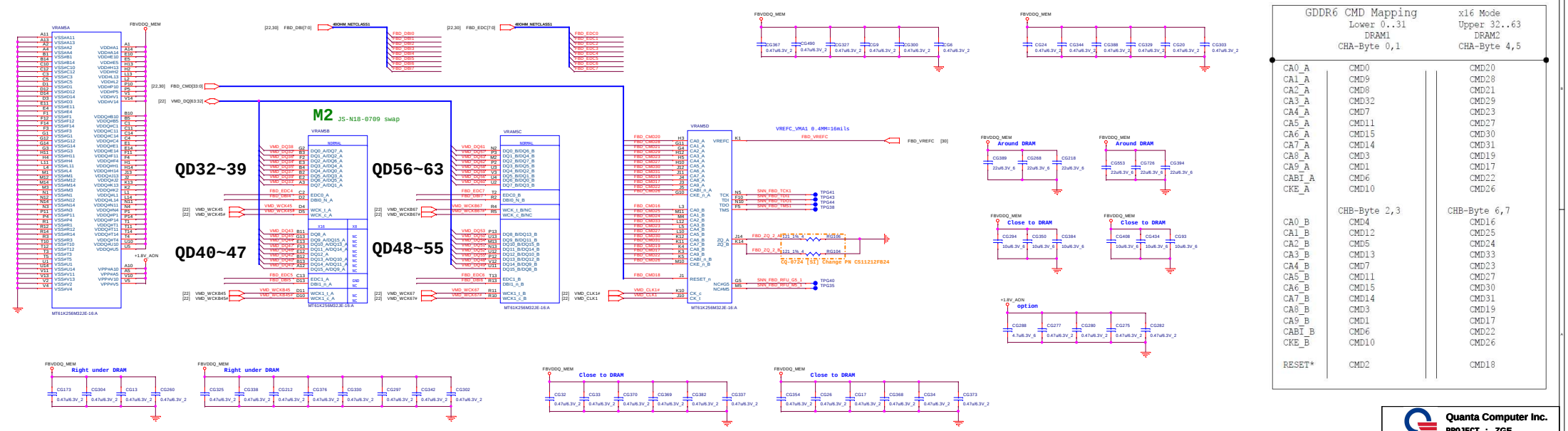
MEMORY: FBD Partition 31..0



MEMORY: FBD Partition 63..32



GDDR6 CMD Mapping	Lower 0..31 DRAM1 CHA-Byte 0,1	x16 Mode Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

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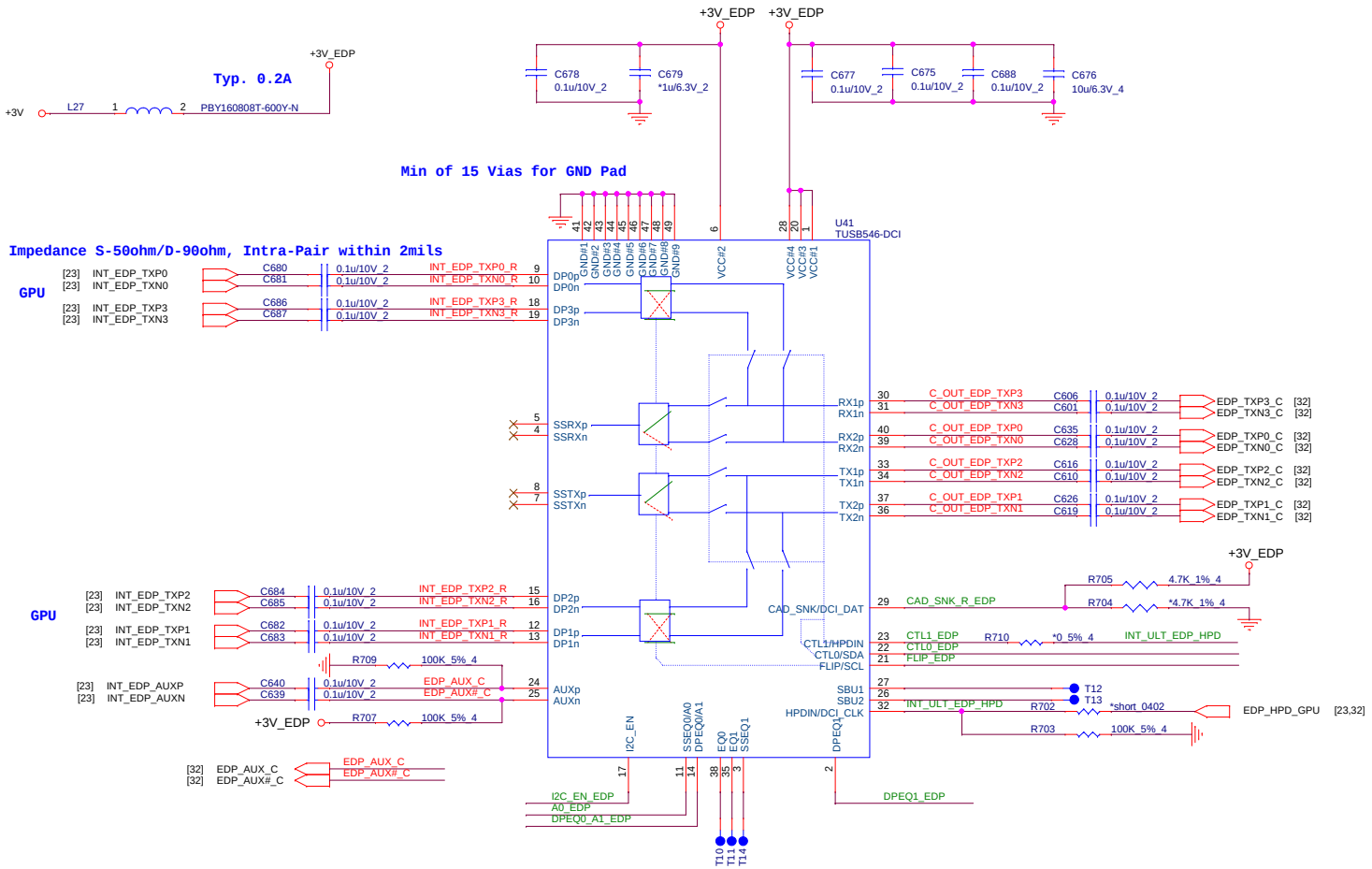
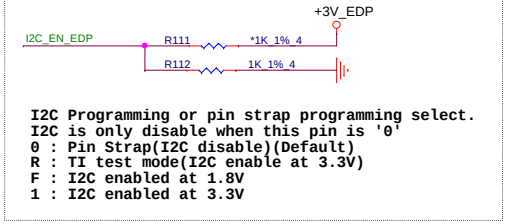
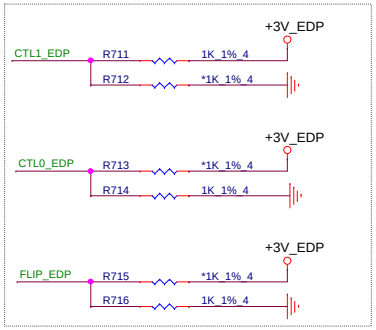
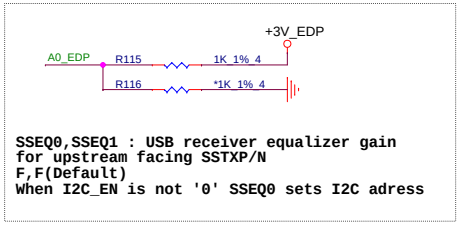
eDP Redriver



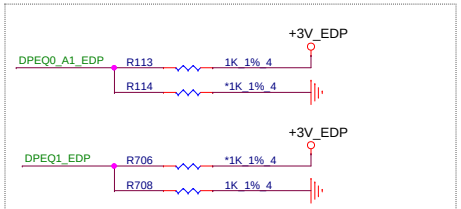


I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V





SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress



DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

Quanta Computer Inc.		
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	eDP Re-driver(TUSB546)	1A
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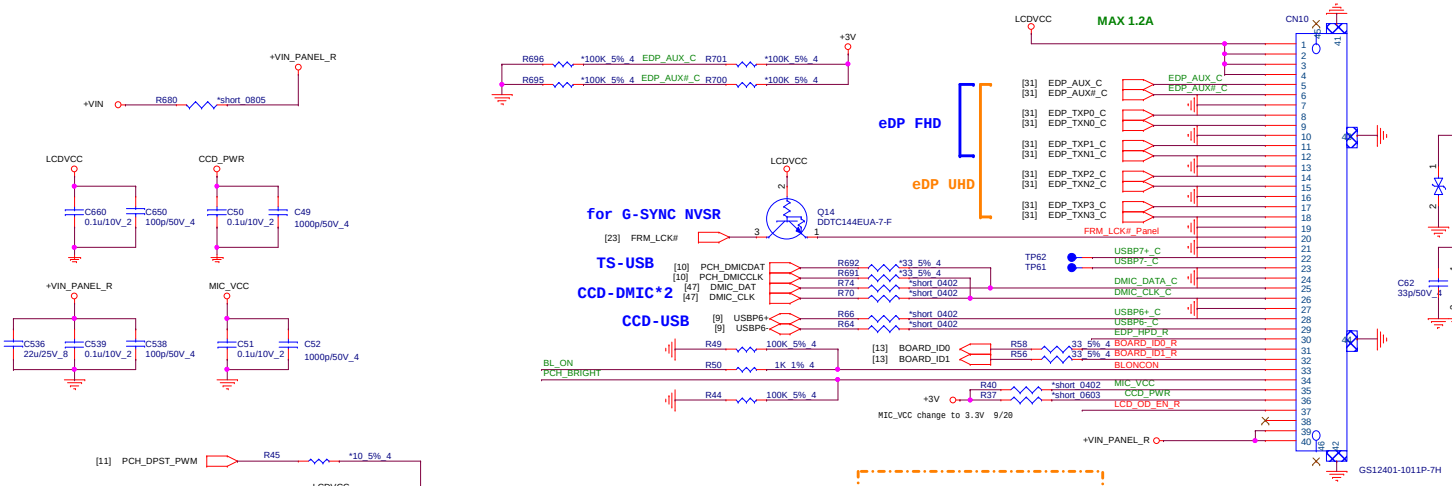
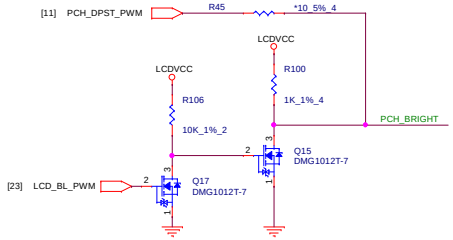
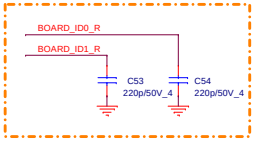
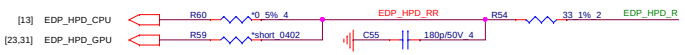
LCD CONNECTOR



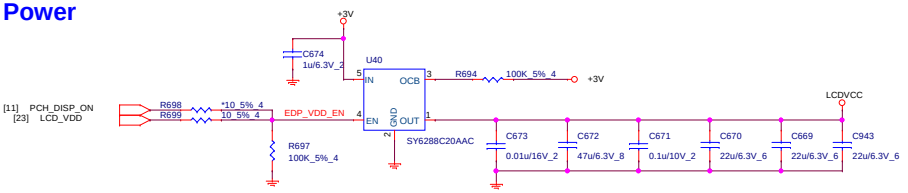




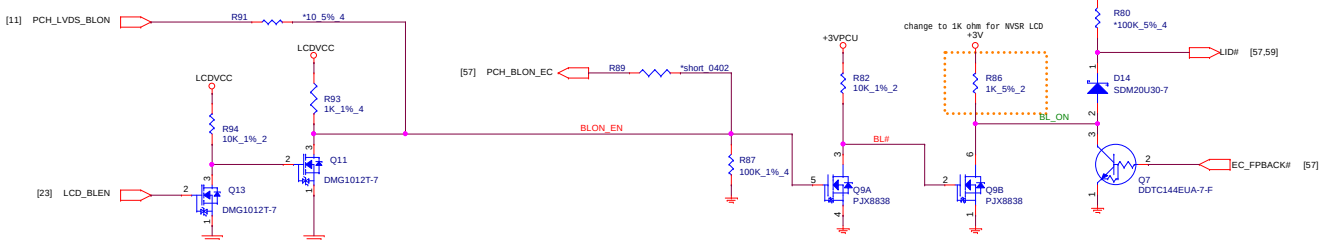
BOARD_ID0	BOARD_ID1	OD_EN	PWM pin	NSVR pin	Support panel
0	0	NC	Reserve	Reserve	Reserve
1	0	NC	NC	Y	NSVR
0	1	Y	Y	NC	DD
1	1	NC	Y	NC	Normal, DD, Freesync



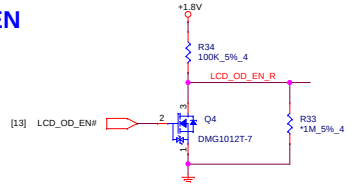
LCD Power



Backlight



LCD OD EN



Function	Enable	Disable
LCD OD_EN_R	Hi or Open	Default

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	eDP Panel/CCD/Hall Sensor	1A

Date: Friday, May 03, 2019 Sheet 32 of 78

DP Redriver

BU5 use MAINON to enable

U36
UP7553PMA5-15
change value for safety

Min of 15 Vias for GND Pad

U39
TUSB546-DCIRNQR

GPU

Impedance S-50ohm/D-90ohm, Intra-Pair within 2mils

GPU

support dual mode /0525

HDMI DAT

HDMI CLK

To support dual mode (DP++) over DisplayPort through Dongle for HDMI, the circuit shown below is required to be implemented on the motherboard.

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

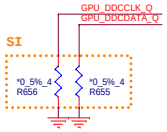
CN2
2DT1517-321211F

ESD1
*AZ1045-04F.R7G

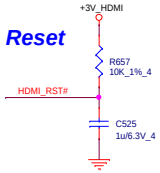
Quanta Computer Inc.			
PROJECT : ZGE			
Size	Document Number		Rev
	DP Re-driver(TUSB546)		1A
Date: Friday, May 03, 2019		Sheet 33 of 78	

HDMI Retimer(HDM)

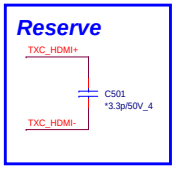
From GPU



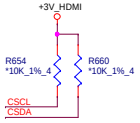
Reset

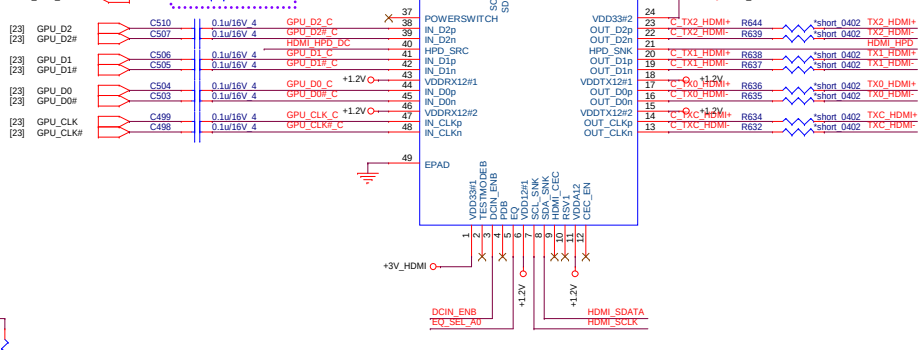


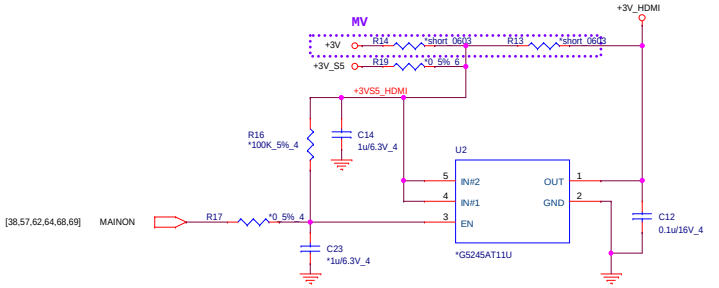
Reserve



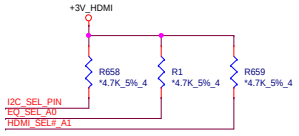
Optional

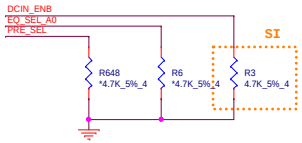






PS8409 strap pin





DCIN_ENB
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input

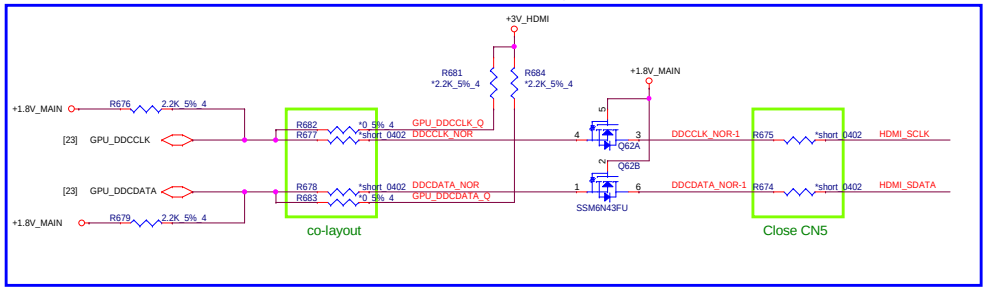
EQ_SEL_A0
Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensaton for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

PRE_SEL
Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

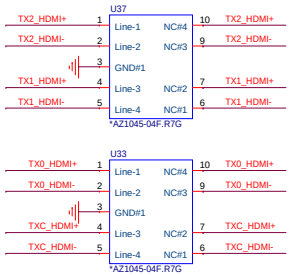
HDMI_SEL#_A1
HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

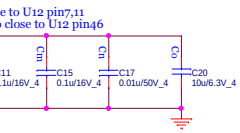
I2C_SEL_PIN
I2C Slave Address selection; Internal pull down, 3.3V I/O.
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.

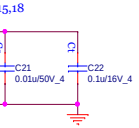
Prevent current leakage when GPU is power off
add R12317/R1231 is for HMDI verify

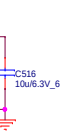


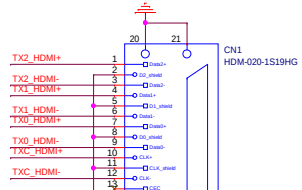
For ESD
Layout note:Place close to HDMI Conn



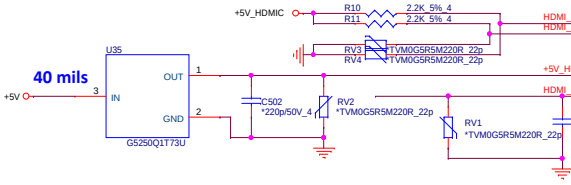








Layout note:Place close to HDMI Conn



Quanta Computer Inc.

PROJECT : ZGE

Size	Document Number	Rev
	HDMI	1A

Date: Friday, May 03, 2019 Sheet 36 of 78

Typ . 0.2A

+3V_TYPEC_DP1

+3V L31 1 2 PBY160808T-600Y-N

+3V_S5 L30 1 2 *PBY160808T-600Y-N

+3VPCU L29 1 2 *PBY160808T-600Y-N

C154 0.1u/10V_2

C155 *1u/6.3V_2

C156 0.1u/10V_2

C214 0.1u/10V_2

C211 0.1u/10V_2

C153 10u/6.3V_4

Min of 15 Vias for GND Pad

Impedance S-50ohm/D-90ohm, Intra-Pair within 2mils

[23] GPU_TBT_D0
[23] GPU_TBT_D0#
C167 0.1u/10V_2 C_GPU_TBT_D0 9
C172 0.1u/10V_2 C_GPU_TBT_D0# 10
DP0p
DP0n

[23] GPU_TBT_D3
[23] GPU_TBT_D3#
C203 0.1u/10V_2 C_GPU_TBT_D3 18
C208 0.1u/10V_2 C_GPU_TBT_D3# 19
DP3p
DP3n

5 SSRXp
4 SSRXn

8 SSTXp
7 SSTXn

[23] GPU_TBT_D2
[23] GPU_TBT_D2#
C193 0.1u/10V_2 C_GPU_TBT_D2 15
C201 0.1u/10V_2 C_GPU_TBT_D2# 16
DP2p
DP2n

[23] GPU_TBT_D1
[23] GPU_TBT_D1#
C182 0.1u/10V_2 C_GPU_TBT_D1 12
C187 0.1u/10V_2 C_GPU_TBT_D1# 13
DP1p
DP1n

[23,38] GPU_TBT_AUXP
[23,38] GPU_TBT_AUXN
C233 0.1u/10V_2 C_GPU_TBT_AUXP 24
C230 0.1u/10V_2 C_GPU_TBT_AUXN 25
AUXp
AUXn

+3V_TYPEC_DP1
R213 100K_1%_4 C_GPU_TBT_AUXN
R212 100K_1%_4 C_GPU_TBT_AUXP

GND#1 41
GND#2 42
GND#3 43
GND#4 44
GND#5 45
GND#6 46
GND#7 47
GND#8 48
GND#9 49
VCC#2 6
VCC#4 28
VCC#3 20
VCC#1 1

RX1p
RX1n
RX2p
RX2n
TX1p
TX1n
TX2p
TX2n
CAD_SNK/DCI_DAT
CTL1/HPDIN
CTL0/SDA
FLIP/SCL
SBU1
SBU2
HPDIN/DCI_CLK

I2C_EN
SSEQ0/A0
DPEQ0/A1
EQ0
EQ1
SSEQ1
DPEQ1

17 I2C_EN_TBT
11 A0_TBT
14 DPEQ0_A1_TBT
2 DPEQ1_TBT
38 T4
35 T5
3 T15

U10
TUSB546-DCIRNQR

Impedance S-50ohm/D-90ohm, Intra-Pair within 2mils

30 31 DDI1_TX3_DP/DN [38]
40 39 DDI1_TX0_DP/DN [38]
33 34 DDI1_TX2_DP/DN [38]
37 36 DDI1_TX1_DP/DN [38]

+3V_TYPEC_DP1
R818 4.7K_1%_4
R813 *4.7K_1%_4
29

23 CTL1_TBT_HPDIN
22 CTL0_TBT_SDA
21 FLIP_TBT_CLK
R211 *0_5%_4 TBT_HPD

27 T6
26 T7
32 TBT_HPD
R807 *short_0402 TBT_DP_HPD [13,23,38]

+3V_TYPEC_DP1
I2C_EN_TBT R815 *1K_1%_4
R817 1K_1%_4

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

+3V_TYPEC_DP1
CTL1_TBT_HPDIN R826 1K_1%_4
R210 *1K_1%_4

+3V_TYPEC_DP1
CTL0_TBT_SDA C782 1u/6.3V_2
R209 1K_1%_4

+3V_TYPEC_DP1
FLIP_TBT_CLK R823 *1K_1%_4
R208 1K_1%_4

+3V_TYPEC_DP1
A0_TBT R795 1K_1%_4
R794 *1K_1%_4

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

+3V_TYPEC_DP1
DPEQ0_A1_TBT R800 1K_1%_4
R806 *1K_1%_4

+3V_TYPEC_DP1
DPEQ1_TBT R788 *1K_1%_4
R792 1K_1%_4

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

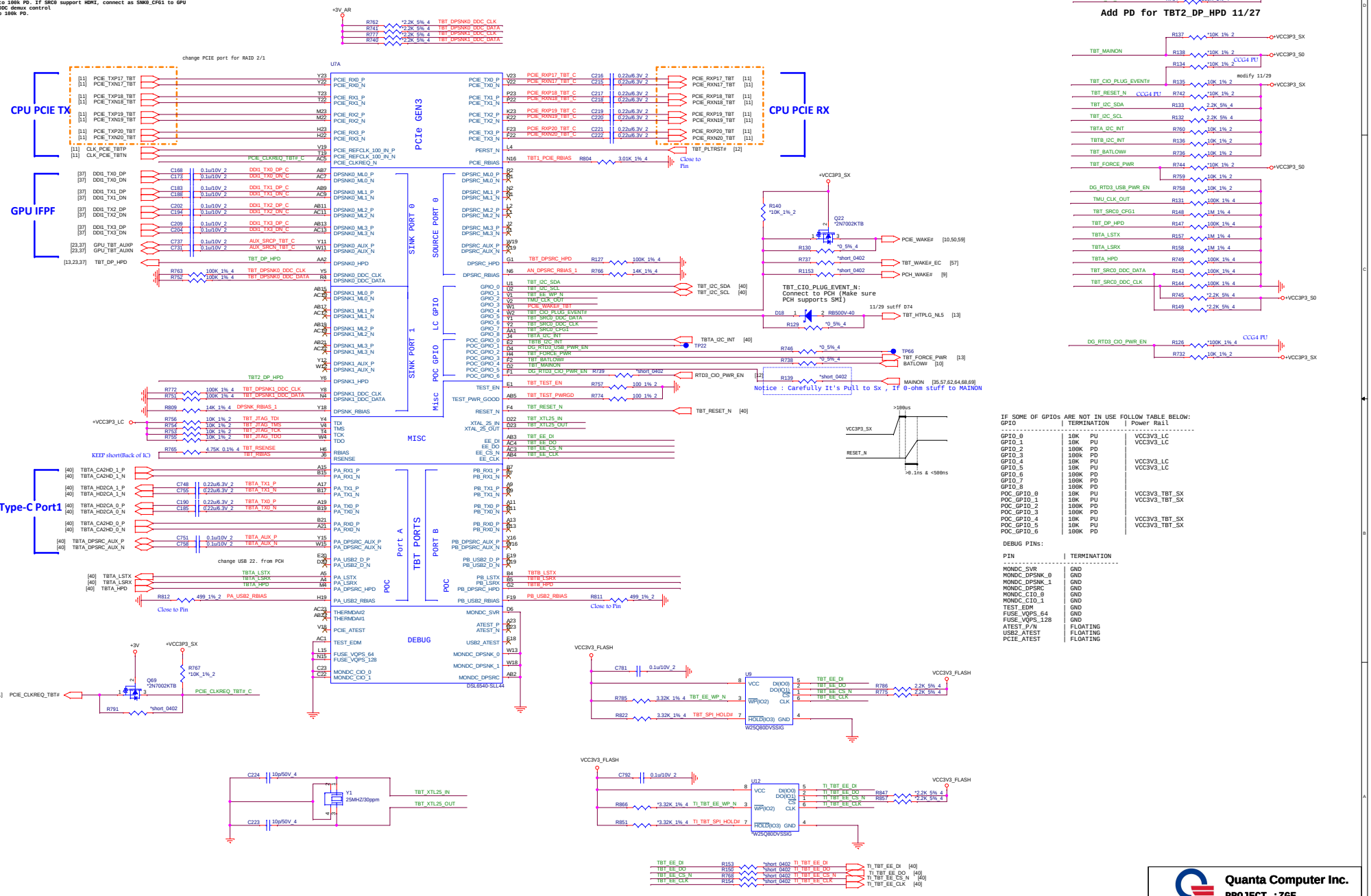
Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	Type C DP re-Driver	1A
Date: Friday, May 03, 2019	Sheet 37 of 78	

TBT(Apline Ridge)

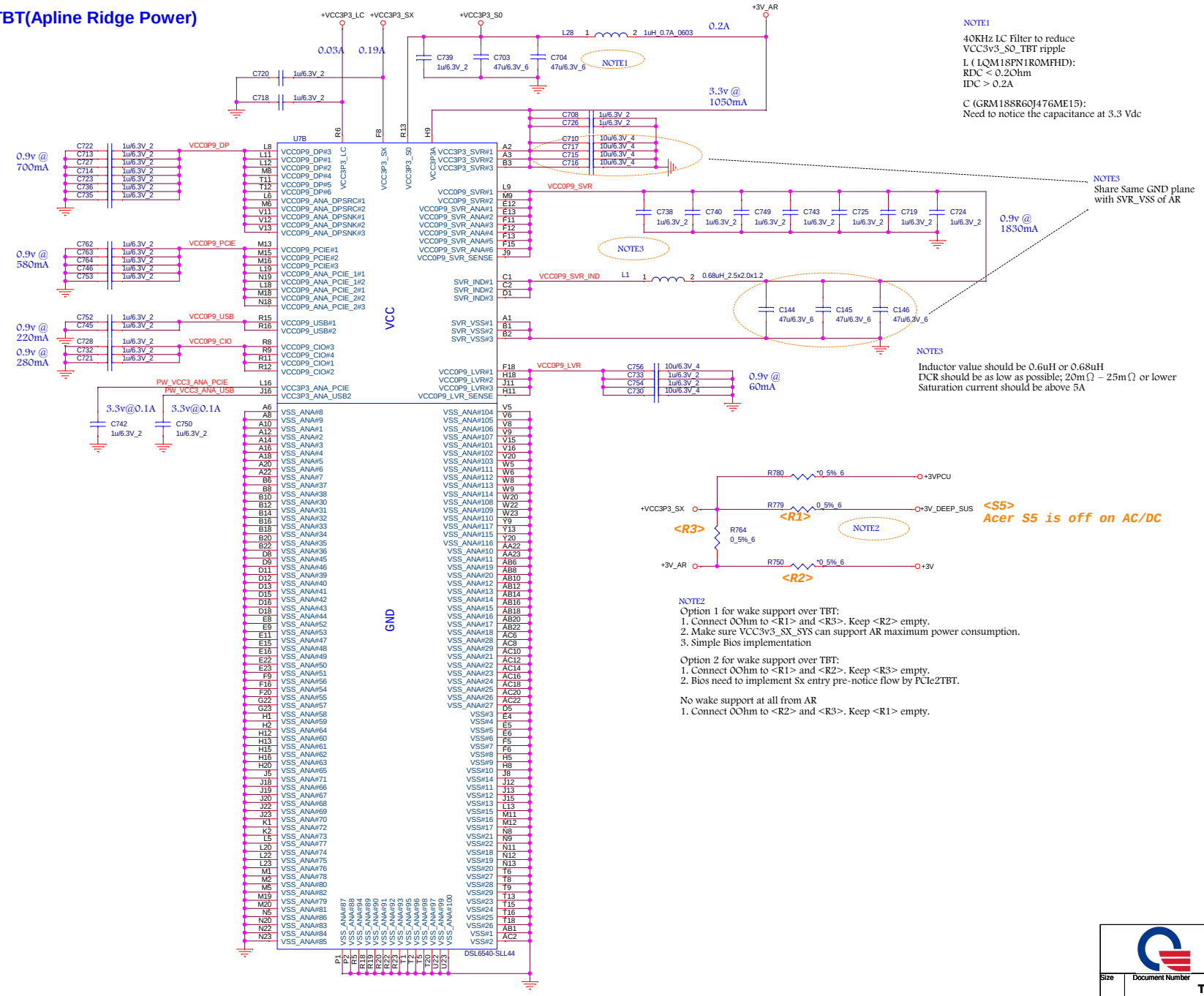
this symbol is not built by AJSLLSN0U04!!

NOTE:
SNK0_DDC_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.
SNK1_DDC_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
SNK1_DDC_clk ?connect to 100k PD.



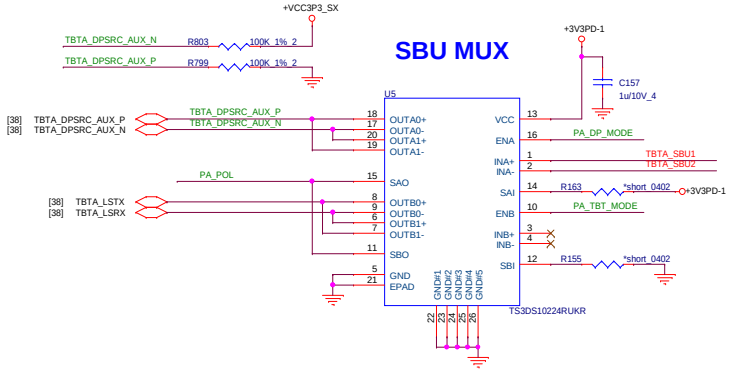
Quanta Computer Inc.	
PROJECT : ZGE	
Size	Document Number: TBT(Apline Ridge) — Rev: 1A
Date: Friday, May 03, 2019	Sheet 38 of 78

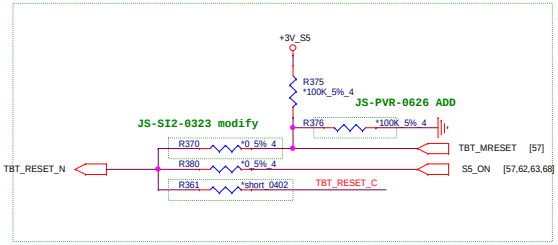
TBT(Apline Ridge Power)



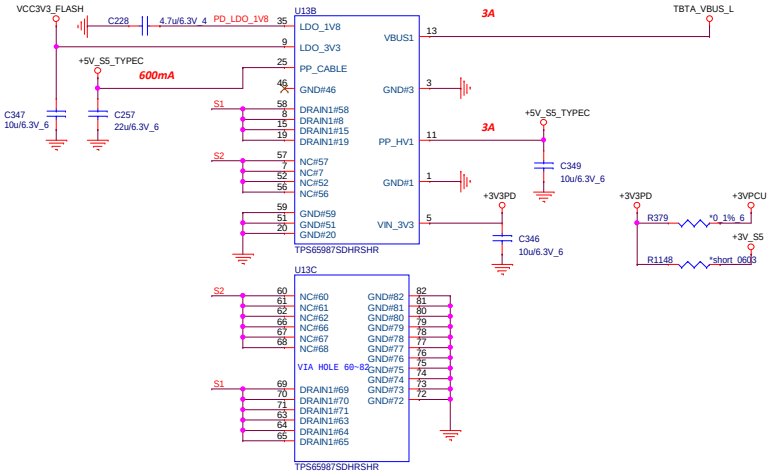
Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number	Rev 1A
	TBT(Apline Ridge Power)	
Date: Friday, May 03, 2019	Sheet 39 of 78	

SBU MUX

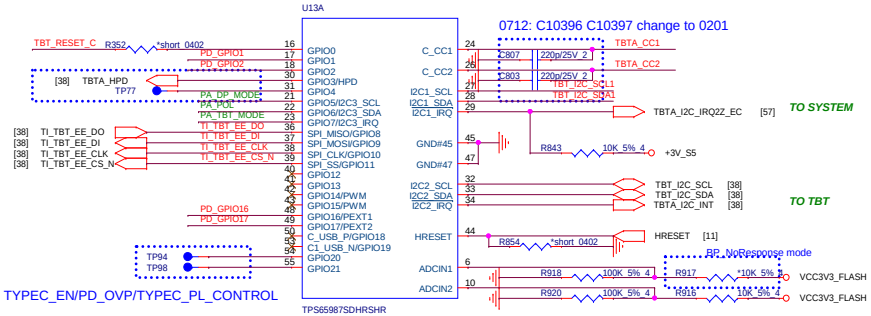




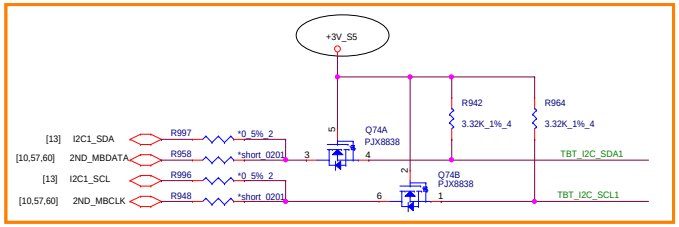
CQ-0724 [SI] Change to 988-CG (X38)



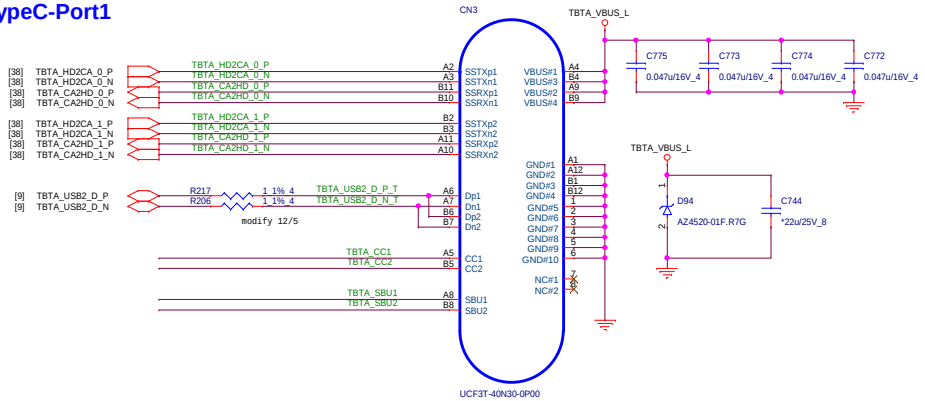
CQ-0725 [SI] Change net name



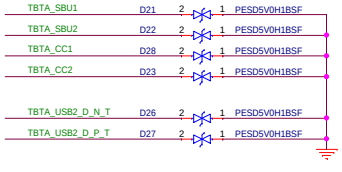
0717: Add TYPEC_EN/PD_OVP/TYPEC_PL_CONTROL

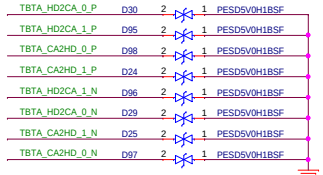


TypeC-Port1



ESD





Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	TI TPS65982	1A
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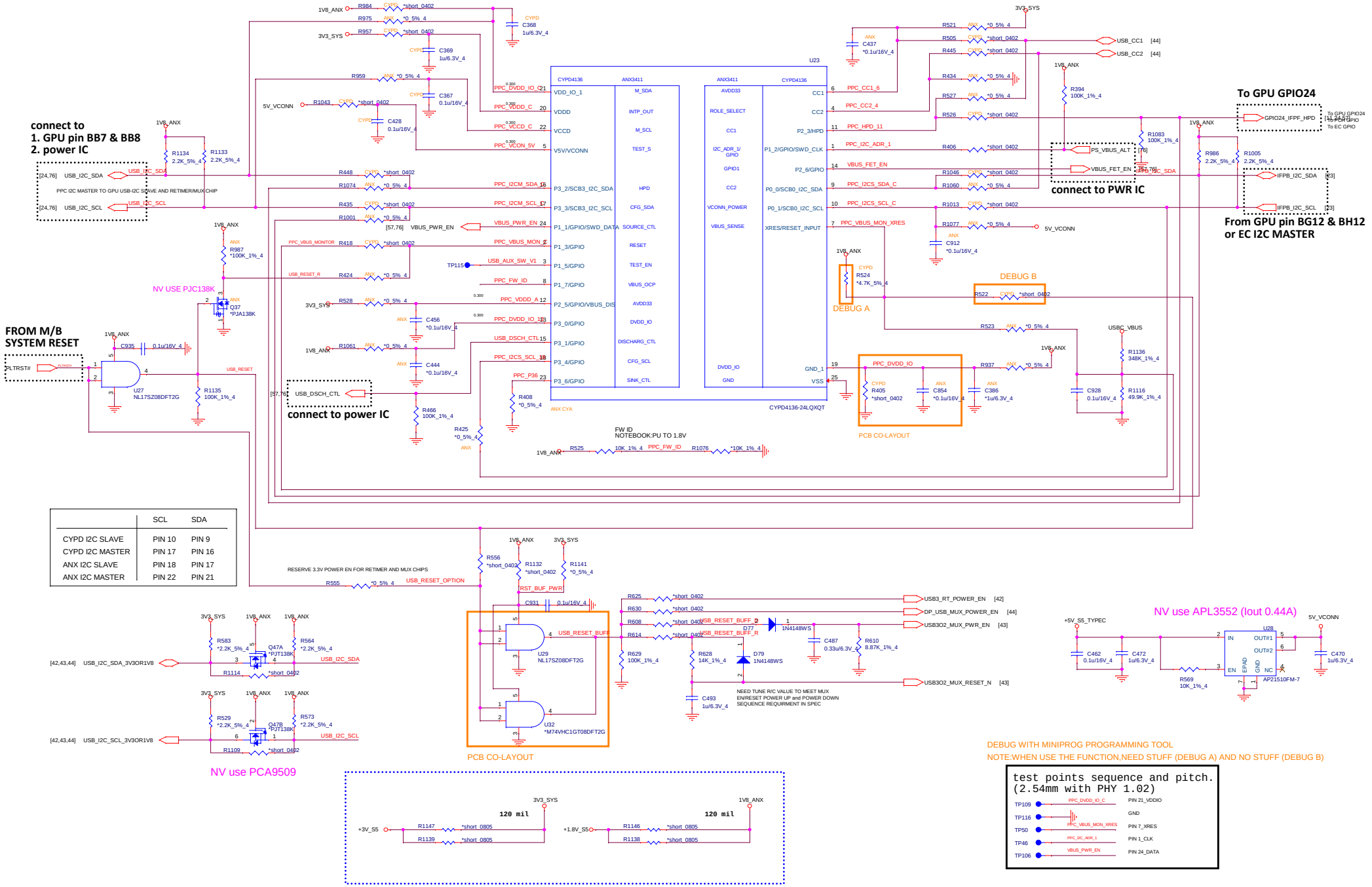
NV Type-C PPC (UTC)



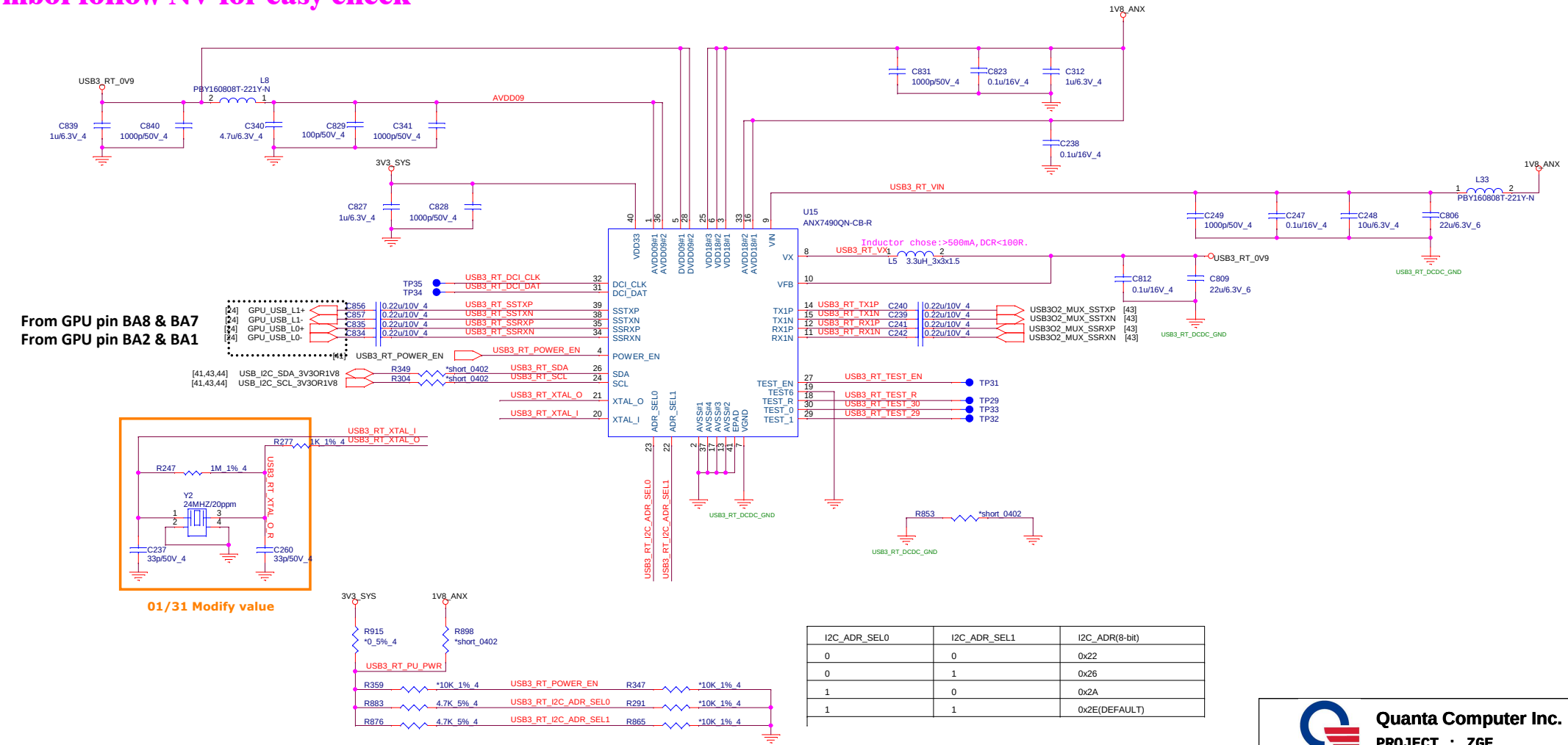
	SCL	SDA
CYPD I2C SLAVE	PIN 10	PIN 9
CYPD I2C MASTER	PIN 17	PIN 16
ANX I2C SLAVE	PIN 18	PIN 17
ANX I2C MASTER	PIN 22	PIN 21

Kyle say : 要 100% follow NV released 的 schematics

Quanta Computer Inc.	
PROJECT : ZGE	
Size	Document Number: TC2 PPC(CYPD4136) Rev: 1A
Date: Friday, May 03, 2019	Sheet 41 of 78

NV Type-C USB3 Re-Timer (UTC)

symbol follow NV for easy check



I2C_ADR_SEL0	I2C_ADR_SEL1	I2C_ADR(8-bit)
0	0	0x22
0	1	0x26
1	0	0x2A
1	1	0x2E(DEFAULT)

Quanta Computer Inc.

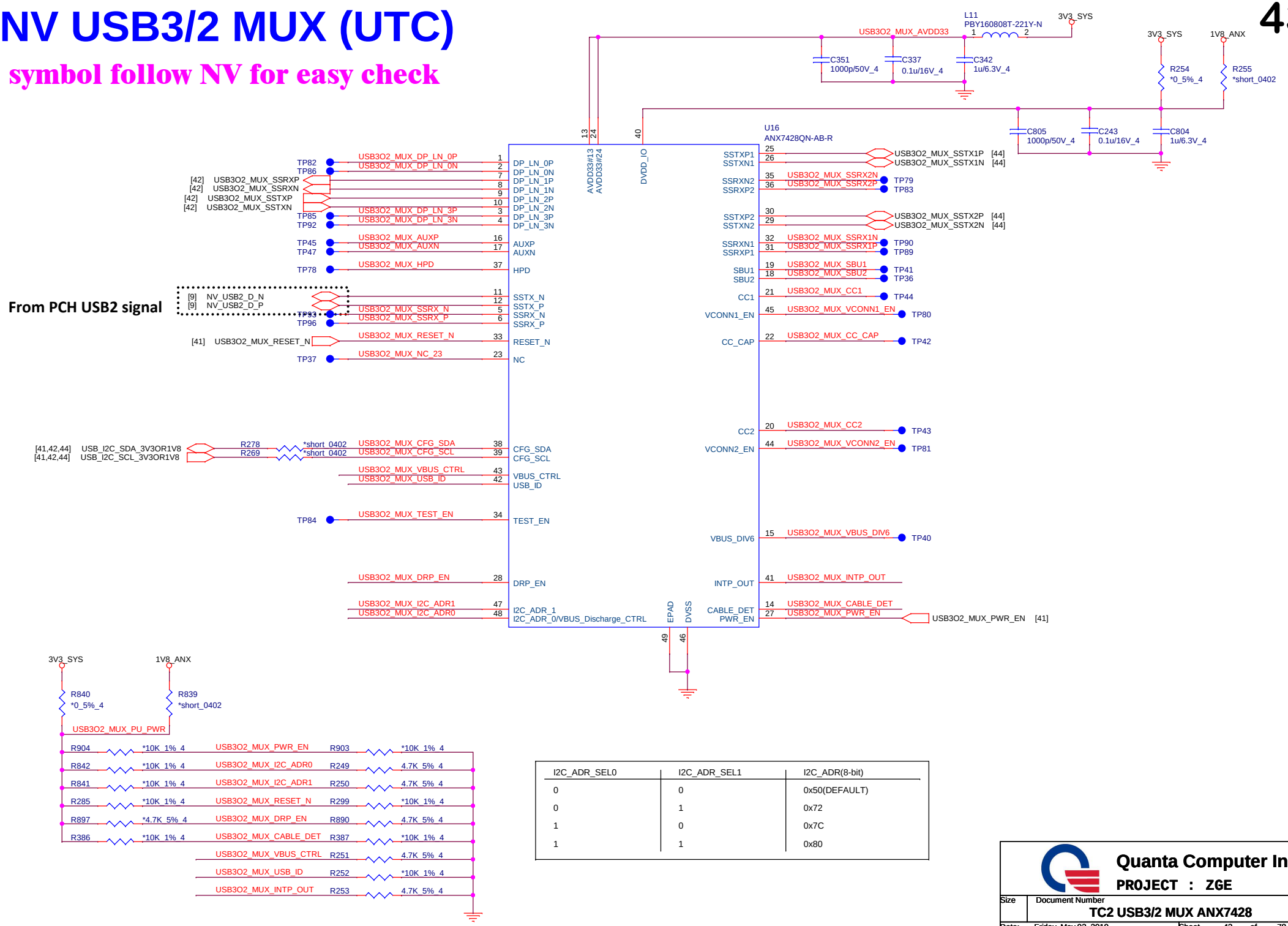
PROJECT : ZGE

Size	Document Number	Rev
	TC2 USB3 Re-Timer ANX7490	1A

Date: Friday, May 03, 2019 Sheet 42 of 78

NV USB3/2 MUX (UTC)

symbol follow NV for easy check



I2C_ADR_SEL0	I2C_ADR_SEL1	I2C_ADR(8-bit)
0	0	0x50(DEFAULT)
0	1	0x72
1	0	0x7C
1	1	0x80

Quanta Computer Inc.

PROJECT : ZGE

Size	Document Number	Rev
	TC2 USB3/2 MUX ANX7428	1A

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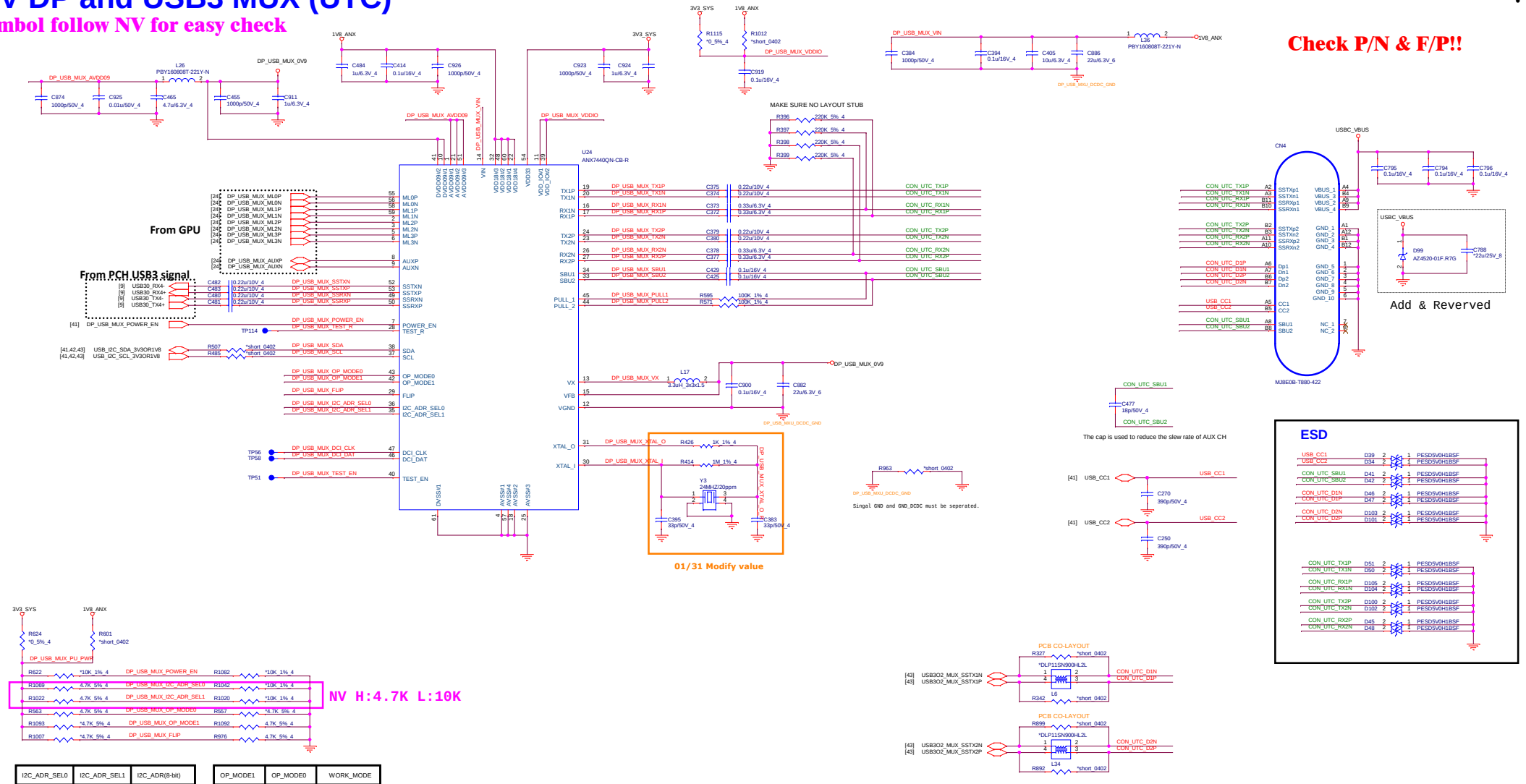
NV DP and USB3 MUX (UTC)

symbol follow NV for easy check

Check P/N & F/P!!



I2C_ADR_SEL0	I2C_ADR_SEL1	I2C_ADR(8-bit)
0	0	0x20
0	1	0x24
1	0	0x28
1	1	0x2C(DEFAULT)

OP_MODE1	OP_MODE0	WORK_MODE
0	0	CHIP DISABLED
0	1	USB3
1	0	DP2+USB3
1	1	DP4

Quanta Computer Inc.
PROJECT : ZGE

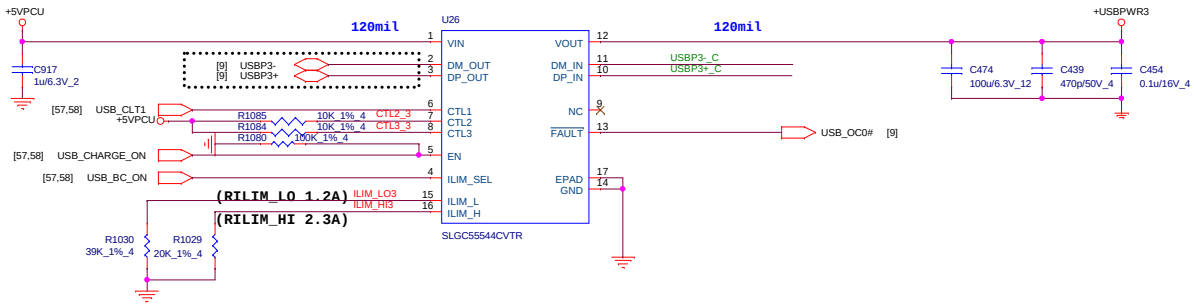
Size	Document Number	Rev
	TC2 DP/USB3 MUX ANX7440	1A

Date: Friday, May 03, 2019 Sheet 44 of 78

USB Charger (UBC)_BC 1.2

Part Number	Description
AL002544001	TPS2544RTER
AL055544001	SLGC55544CVTR

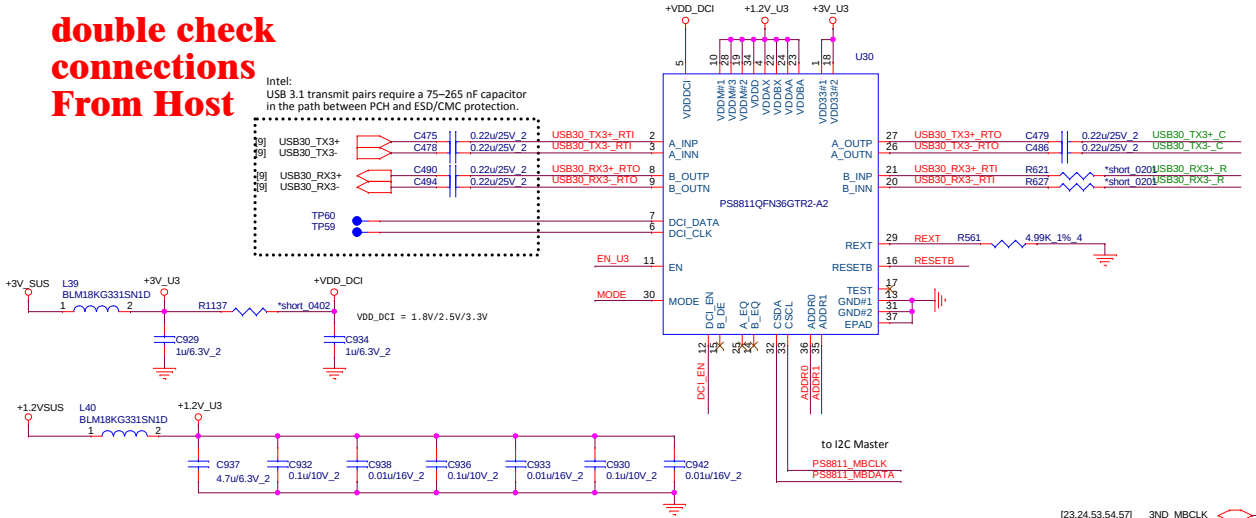
USB_BC_ON(Low)-->ILIM_L
USB_BC_ON(High)-->ILIM_H



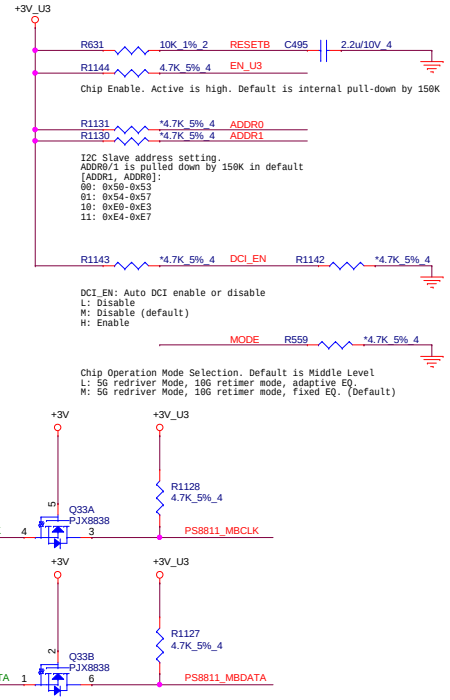
USB3.0 Retimer (UB3) Vendor suggests to use I2C mode.

double check connections From Host

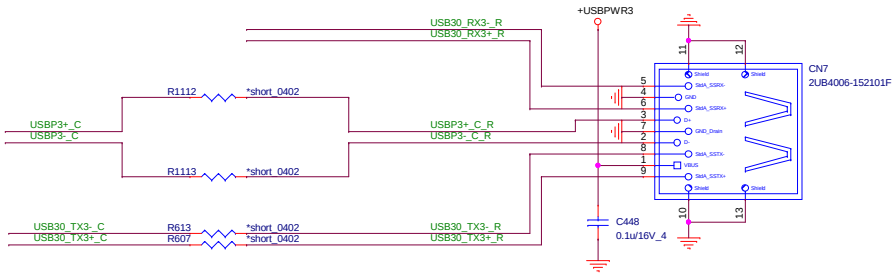
Intel:
USB 3.1 transmit pairs require a 75–265 nF capacitor in the path between PCH and ESD/CMC protection.

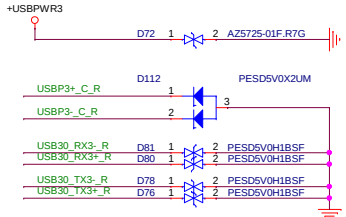


Decoupling caps need be placed as close to power pins as possible.
1.2 V power ripple requirement: < 30 mV



USB3.0 (UB3)





Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	USB2.0*1/USB3.0*3/BC1.2	1A
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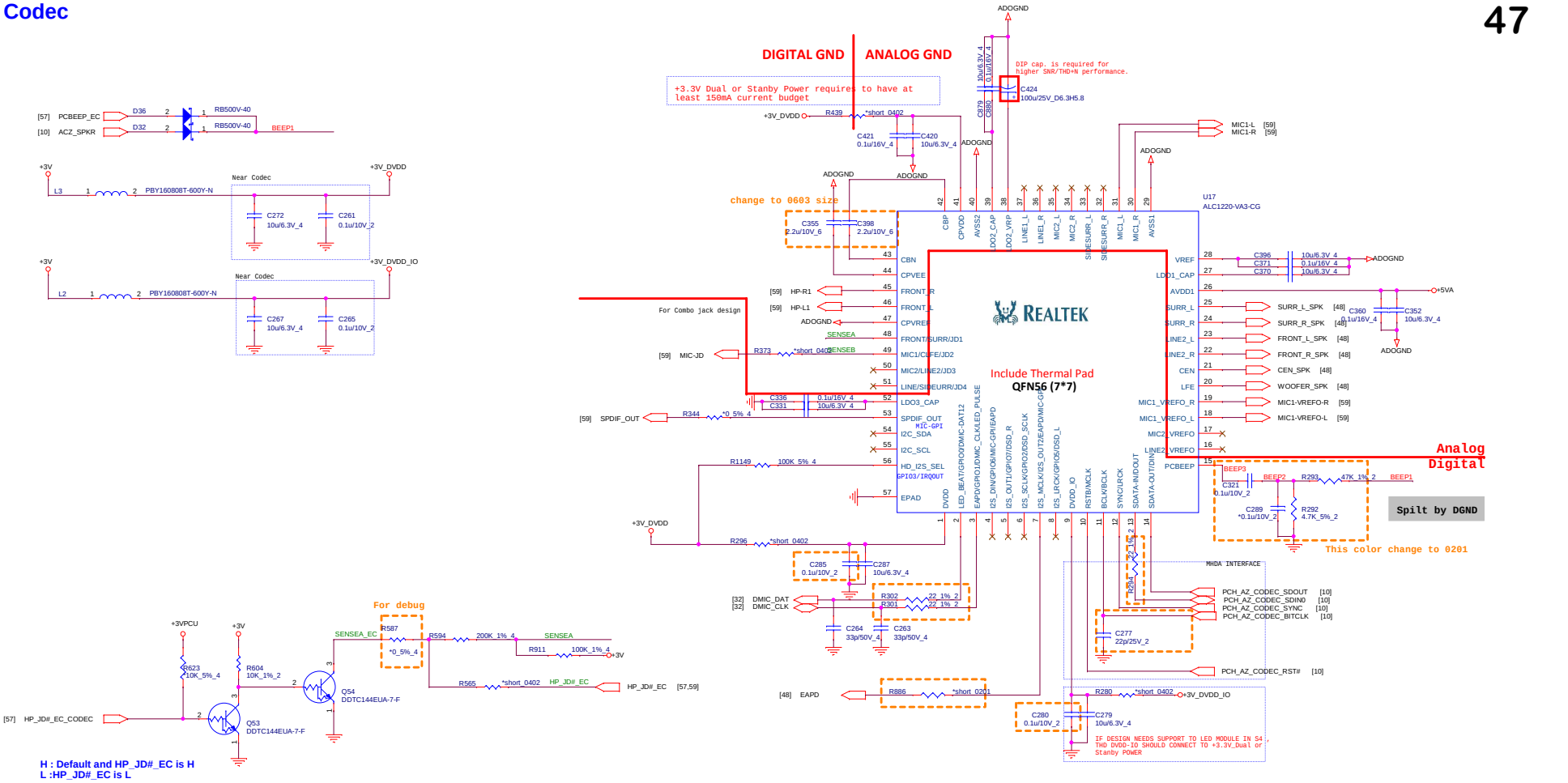
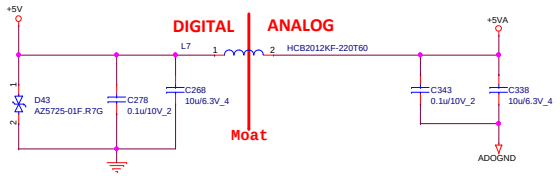
Codec



Codec PWR 5V(ADO)

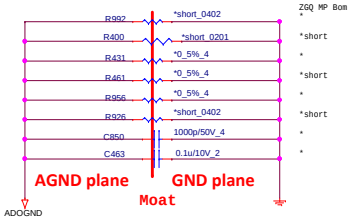


Mute(ADO)

Internal Speaker(ADO)

Bead RDC<30mohm

DC-DET circuit(ADO)



Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: Azalia ALC299-CG,S-AMP	Rev: 1A
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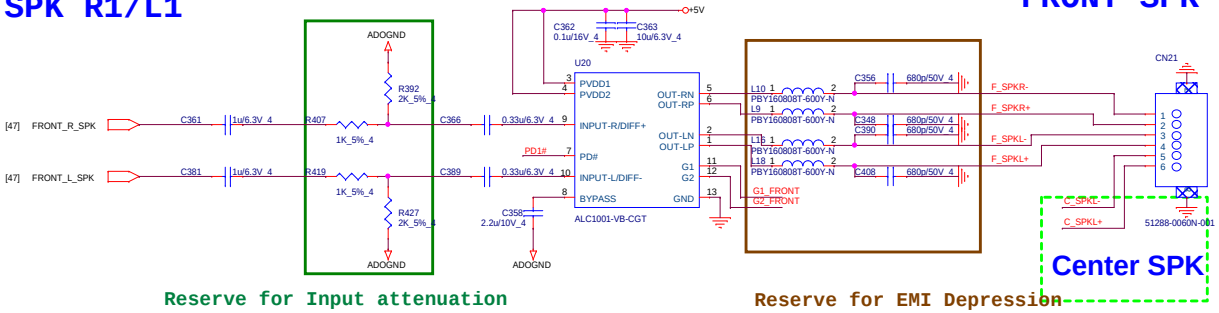
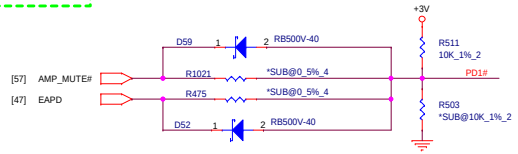
SPK R1/L1



Reserve for Input attenuation

To have optimization output power

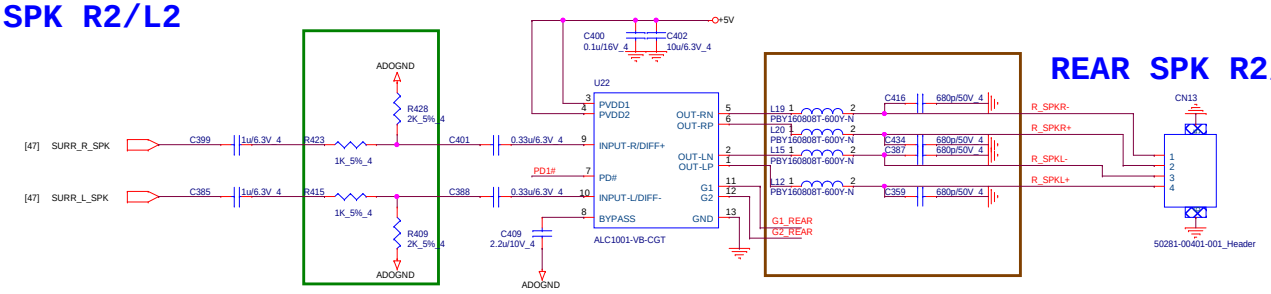
Reserve for EMI Depression
Close to IC
Speaker Loading =4Ohm +- 10%



Output Gain Table

G2	G1	SE-input Stereo-output Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

SPK R2/L2



Reserve for Input attenuation

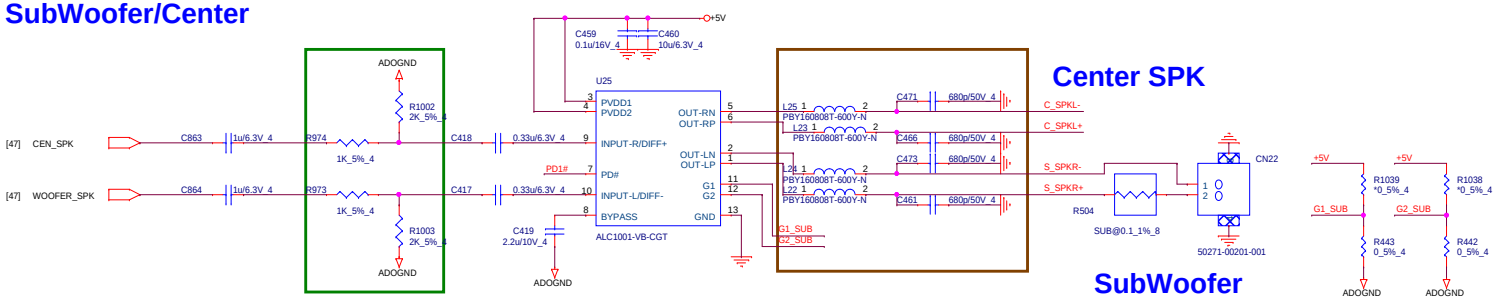
To have optimization output power

Reserve for EMI Depression
Close to IC
Speaker Loading =4Ohm +- 10%

Output Gain Table

G2	G1	SE-input Stereo-output Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

SubWoofer/Center



Reserve for Input attenuation

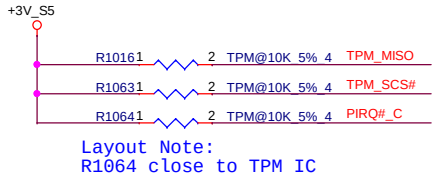
To have optimization output power

Reserve for EMI Depression
Close to IC
Speaker Loading =4Ohm +- 10%

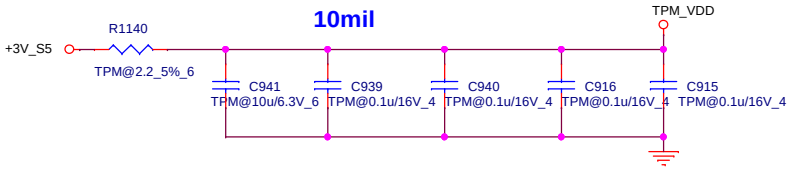
Output Gain Table

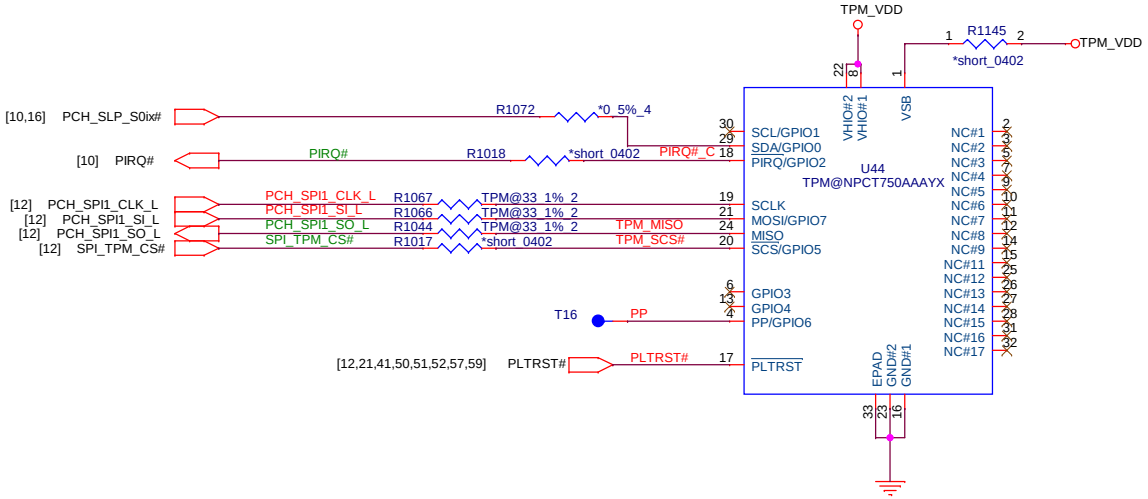
G2	G1	SE-input Stereo-output Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

TPM NPCT750



Layout Note:
R1064 close to TPM IC





NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- VHIO can be either +3.3V or +1.8V.
- It is recommended to connect VHIO to V_RUN.
- VALW can be either +3.3V or +1.8V.
- VALW power rail should be powered whenever the system is powered by any power source.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

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NGFF_M.2 WiFi & BT (NGF)

E-Key

change USB to Port 14 for CFL-H

change Footprint 11/30

update P/N and footpint 8/4

CN16
NASE0-S6701-TSH4

NGFF EKEY

1	GND#3	3.3Vaux#1	2
3	USB_D+	3.3Vaux#2	4
5	USB_D-	LED#1	6
7	GND#4	PCM_CLK	8
9	SDIO CLK(O)	PCM_SYNC	10
11	SDIO CMD(IO)	PCM_IN	12
13	SDIO DAT0(IO)	PCM_OUT	14
15	SDIO DAT1(IO)	LED#2	16
17	SDIO DAT2(IO)	GND#13	18
19	SDIO DAT3(IO)	UART Wake	20
21	SDIO Wake(I)	UART Rx	22
23	SDIO Reset		
		UART Tx	32
33	GND#5	UART RTS	34
35	PETp0	UART CTS	36
37	PETn0	Clink RESET	38
39	GND#6	CLink DATA	40
41	PERp0	CLink CLK	42
43	PERn0	COEX3	44
45	GND#7	COEX2	46
47	REFCLKP0	COEX1	48
49	REFCLKN0	SUSCLK(32KHz)	50
51	GND#8	PERST0#	52
53	CLKREQ0#	W_DISABLE2#	54
55	PEWake0#	W_DISABLE1#	56
57	GND#9	NFC_I2C_SM_DATA	58
59	PETp1	NFC_I2C_SM_CLK	60
61	PETn1	NFC_I2C_IRQ	62
63	GND#10	GPIO0_NFC_RESET#	64
65	PERp1	UIM_SWP/PERST1#	66
67	PERn1	UIM_POWER_SNK	68
69	GND#11	UIM_POWER_SRC	70
71	Reserved1	3.3Vaux#3	72
73	Reserved2	3.3Vaux#4	74
75	GND#12		
79	NC#2	GND#1	77
78	NC#1	GND#2	76

[9] USBP14+
[9] USBP14-
[11] CNV_WRXN1
[11] CNV_WRXP1
[11] CNV_WRXN0
[11] CNV_WRXP0
[11] CNV_WR_CLKN
[11] CNV_WR_CLKP
[11] PCIE_TXP15_WLAN
[11] PCIE_TXN15_WLAN
[11] PCIE_RXP15_WLAN
[11] PCIE_RXN15_WLAN
[11] CLK_PCIE_WLANP
[11] CLK_PCIE_WLANN
WLAN_CLKREQ#
WLAN_WAKE_R#
[11] CNV_WTXN1
[11] CNV_WTXP1
[11] CNV_WTXN0
[11] CNV_WTXP0
[11] CNV_WT_CLKN
[11] CNV_WT_CLKP

+WL_VDD
C159 10u/6.3V_4
C164 0.1u/10V_2
C160 0.1u/10V_2
C152 0.1u/10V_2
C815 0.1u/10V_2

WIGIG_LED
TP91
PCM_CLK [10]
CNV_RF_RESET# [10]
PCM_IN [10]
MODEM_CLKREQ [10]
modify 8/23
CNV_BRI_RSP_R R263 22_1%_4
UART_WAKE_N [10]
CNV_BRI_RSP [11]
CNV_RGI_RSP_R R215 22_1%_4
CNV_RGI_DT [11]
CNV_RGI_RSP [11]
CNV_BRI_DT [11]
TP128
TP129
TP130
Modify 8/10
CNV_PA_BLANKING [11]
CNV_MFUART2_TXD [11]
CNV_MFUART2_RXD [11]
SUSCLK [10]
WLAN_RST#
R200 *short_0402 PLTRST#
PLTRST# [12,21,41,49,51,52,57,59]
BT_EN
RF_EN
BT_EN [57]
RF_EN [57]
LPC_LAD0_C
CLK_PCI_LPC_C
LPC_LFRAME#_C
R179 *short_0402
R178 *short_0402
R176 *short_0402
LPC_LAD0 [9,57]
CLK_PCI_LPC [9]
LPC_LFRAME# [9,57]
R175 *short_0402
CLKIN_XTAL [11]
LPC_LAD1_C
LPC_LAD2_C
LPC_LAD3_C
R173 *short_0402
R168 *short_0402
R167 *short_0402
LPC_LAD1 [9,57]
LPC_LAD2 [9,57]
LPC_LAD3 [9,57]

Change 80 port pin defined 7/19

+WL_VDD
BT_EN R191 *10K_1%_4
RF_EN R184 *10K_1%_4
Add it for CNVi 9/29

Close M.2 connector

+1.8V_DEEP_SUS
CNV_RGI_DT R243 20K_1%_4
R417 *100K_1%_4
+1.8V_DEEP_SUS
CNV_BRI_DT R225 10K_1%_4
R355 *4.7K_1%_4

+WL_VDD
+WL_VDD
R220 4.7K_1%_4
WLAN_CLKREQ#
Q28
2N7002KTB
PCIE_CLKREQ_WLAN# [11]

Q31
CNV@AO3413
+3V_S5
C266 CNV@1u/6.3V_4
R282 CNV@100K_5%_4
R300
[57] WLANPWR#
CNV@10K_5%_4
C288 10u/6.3V_4
C824 0.1u/10V_2
C822 0.1u/10V_2
C169 0.1u/10V_2
+WL_VDD
+3V
+3V_S5
R362 *0_5%_6
R265 *0_5%_6
R
Add R for CNVi

+WL_VDD
+WL_VDD
R204 *4.7K_1%_4
WLAN_WAKE_R#
Q26
*2N7002KTB
PCIE_WAKE#
PCIE_WAKE# [10,38,59]

Quanta Computer Inc.		
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	NGFF WiFi & BT	1A
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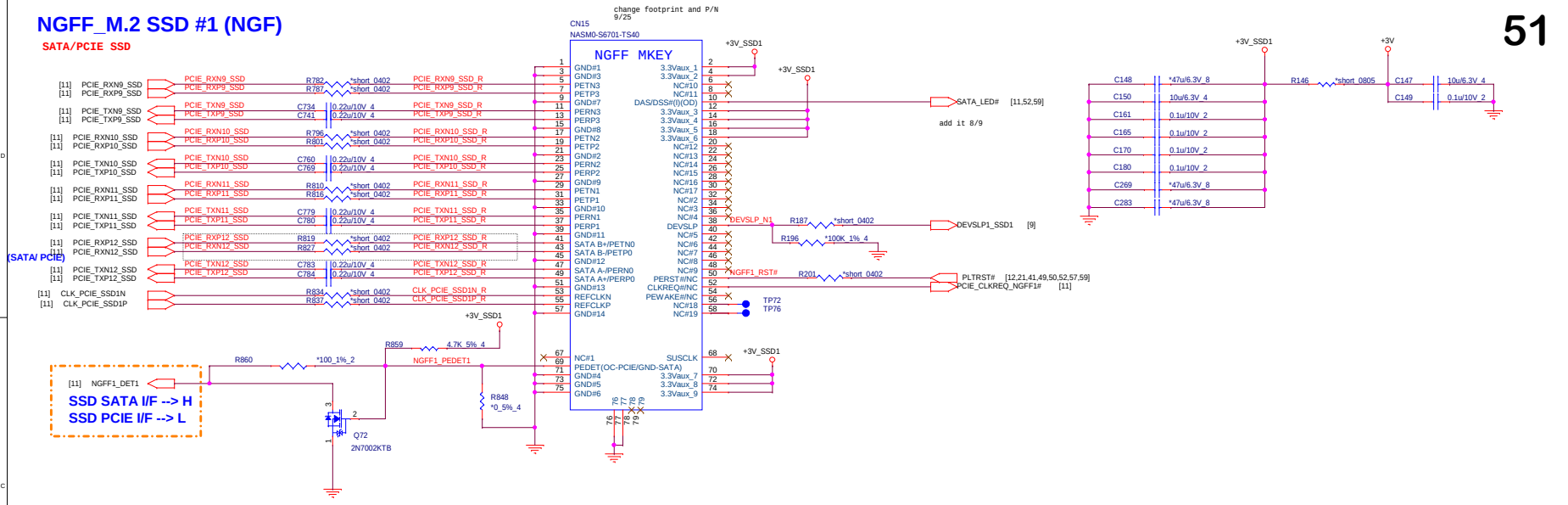
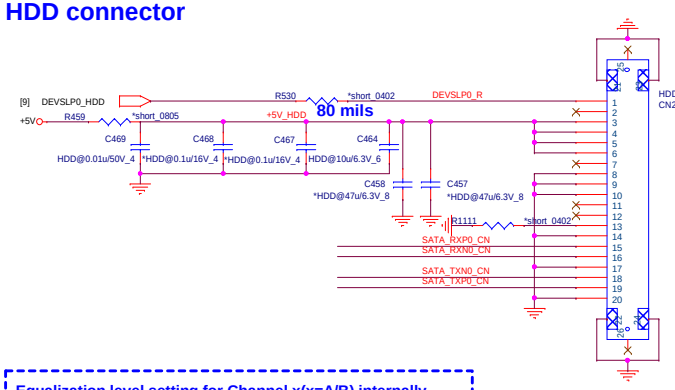
NGFF_M.2 SSD #1 (NGF)

SATA/PCIE SSD

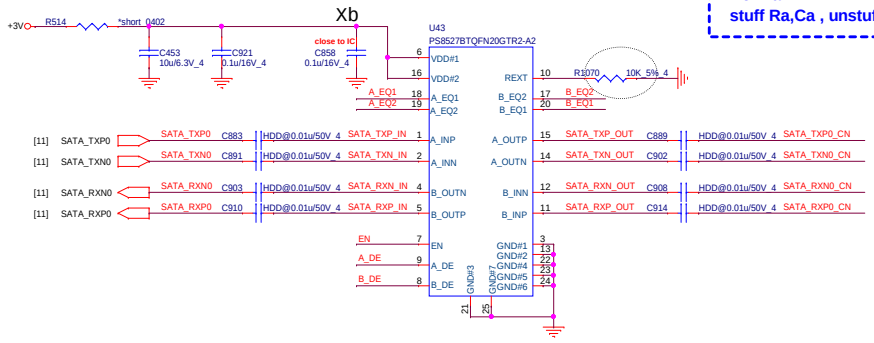


HDD

HDD connector



HDD Re-driver

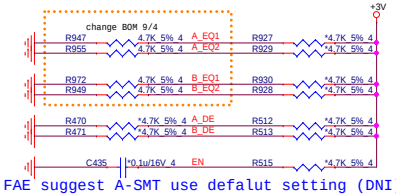


SATA re-driver IC
stuff Rb,Cb,Xb , unstuff Ra,Ca

Normal
stuff Ra,Ca , unstuff Rb,Cb

Equalization level setting for Channel x(x=A/B),internally tied to VDD/2 (default:12.2dB)
[x_EQ2, x_EQ1] ==
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)
[x_DE] ==
L: 0 dB
H: -6dB



Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	NGFF SSD #1 / HDD	1A

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NGFF_M.2 SSD #2 (NGF)

Only for PCIE SSD

change footprint and P/N
9/25

CN18
NASM0-S6701-TS40

NGFF MKEY

1	GND#1	3.3Vaux_1	2
3	GND#3	3.3Vaux_2	4
5	PETN3	NC#10	6
7	PETP3	NC#11	8
9	GND#7	DAS/DSS#(I)(OD)	10
11	PERN3	3.3Vaux_3	12
13	PERP3	3.3Vaux_4	14
15	GND#8	3.3Vaux_5	16
17	PETN2	3.3Vaux_6	18
19	PETP2	NC#12	20
21	GND#2	NC#13	22
23	PERN2	NC#14	24
25	PERP2	NC#15	26
27	GND#9	NC#16	28
29	PETN1	NC#17	30
31	PETP1	NC#2	32
33	GND#10	NC#3	34
35	PERN1	NC#4	36
37	PERP1	DEVSLP	38
39	GND#11	NC#5	40
41	SATA B+/PETN0	NC#6	42
43	SATA B-/PETP0	NC#7	44
45	GND#12	NC#8	46
47	SATA A-/PERN0	NC#9	48
49	SATA A+/PERP0	PERST#/NC	50
51	GND#13	CLKREQ#/NC	52
53	REFCLKN	PEWAKE#/NC	54
55	REFCLKP	NC#18	56
57	GND#14	NC#19	58
67	NC#1	SUSCLK	68
69	PEDET(OC-PCIE/GND-SATA)		70
71	GND#4	3.3Vaux_7	72
73	GND#5	3.3Vaux_8	74
75	GND#6	3.3Vaux_9	
76			
77			
78			
79			

+3V_SSD2
+3V_SSD2
+3V_SSD2
+3V
+3V_SSD2

[9] PCIE_RXN24_SSD → PCIE_RXN24_SSD → R933 *short_0402 → PCIE_RXN24_SSD_R
[9] PCIE_RXP24_SSD → PCIE_RXP24_SSD → R934 *short_0402 → PCIE_RXP24_SSD_R
[9] PCIE_TXN24_SSD → PCIE_TXN24_SSD → C862 0.22u/10V_4 → PCIE_TXN24_SSD_R
[9] PCIE_TXP24_SSD → PCIE_TXP24_SSD → C869 0.22u/10V_4 → PCIE_TXP24_SSD_R
[9] PCIE_RXN23_SSD → PCIE_RXN23_SSD → R950 *short_0402 → PCIE_RXN23_SSD_R
[9] PCIE_RXP23_SSD → PCIE_RXP23_SSD → R966 *short_0402 → PCIE_RXP23_SSD_R
[9] PCIE_TXN23_SSD → PCIE_TXN23_SSD → C876 0.22u/10V_4 → PCIE_TXN23_SSD_R
[9] PCIE_TXP23_SSD → PCIE_TXP23_SSD → C885 0.22u/10V_4 → PCIE_TXP23_SSD_R
[9] PCIE_RXN22_SSD → PCIE_RXN22_SSD → R985 *short_0402 → PCIE_RXN22_SSD_R
[9] PCIE_RXP22_SSD → PCIE_RXP22_SSD → R1000 *short_0402 → PCIE_RXP22_SSD_R
[9] PCIE_TXN22_SSD → PCIE_TXN22_SSD → C899 0.22u/10V_4 → PCIE_TXN22_SSD_R
[9] PCIE_TXP22_SSD → PCIE_TXP22_SSD → C904 0.22u/10V_4 → PCIE_TXP22_SSD_R
[9] PCIE_RXP21_SSD → PCIE_RXP21_SSD → R1027 *short_0402 → PCIE_RXP21_SSD_R
[9] PCIE_RXN21_SSD → PCIE_RXN21_SSD → R1028 *short_0402 → PCIE_RXN21_SSD_R
[9] PCIE_TXN21_SSD → PCIE_TXN21_SSD → C913 0.22u/10V_4 → PCIE_TXN21_SSD_R
[9] PCIE_TXP21_SSD → PCIE_TXP21_SSD → C920 0.22u/10V_4 → PCIE_TXP21_SSD_R
[11] CLK_PCIE_SSD2N → R1075 *short_0402 → CLK_PCIE_SSD2N_R
[11] CLK_PCIE_SSD2P → R1086 *short_0402 → CLK_PCIE_SSD2P_R

SATA_LED# [11,51,59]

add it 8/9

DEVSLP_N2 → R520 *short_0402 → DEVSLP4_SSD2 [9]
R501 *100K_1%_4

NGFF2_RST# → R609 *short_0402 → PLTRST# [12,21,41,49,50,51,57,59]
PCIE_CLKREQ_NGFF2# [11]

TP123
TP124

Del SSD detcet circuit for PCIE SSD RAID 2/1

C376 *47u/6.3V_8
C403 10u/6.3V_4
C412 0.1u/10V_2
C413 0.1u/10V_2
C410 0.1u/10V_2
C411 0.1u/10V_2
C485 *47u/6.3V_8
C491 *47u/6.3V_8

R391 *short_0805
C345 10u/6.3V_4
C354 0.1u/10V_2

Quanta Computer Inc.
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	NGFF SSD #2	1A
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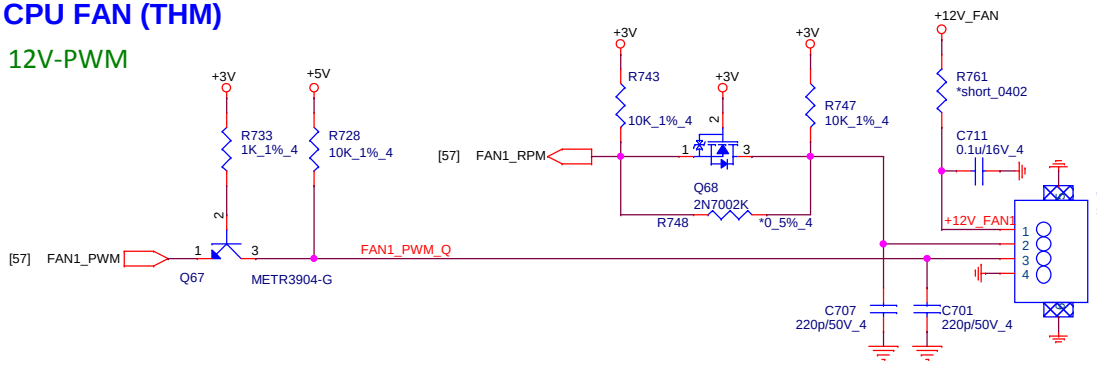
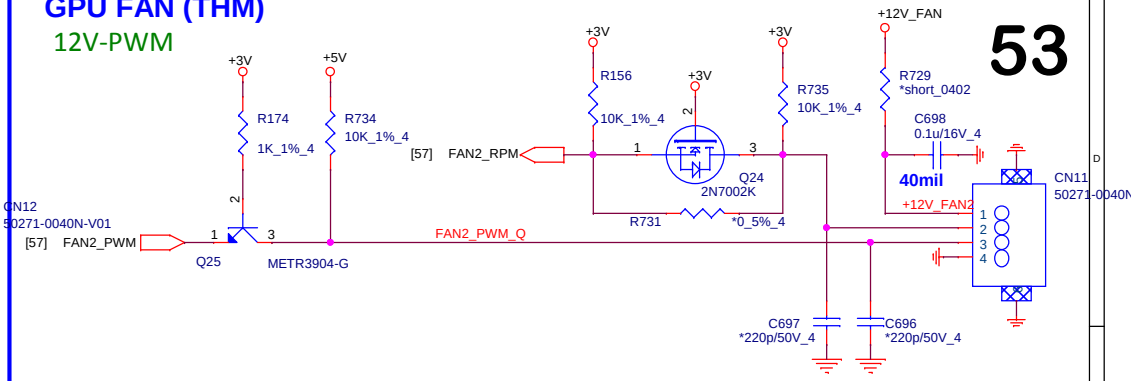
CPU FAN (THM)

12V-PWM

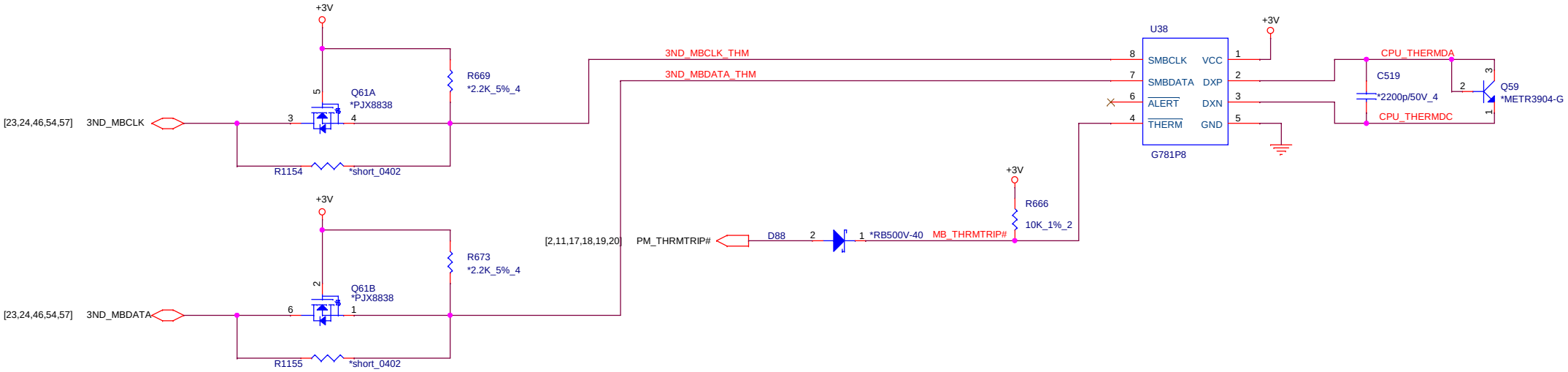


GPU FAN (THM)

12V-PWM



CPU Thermal Sensor,Local CPU Thermal Sensor



Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: FAN,Thermal,FAN LED	Rev: 1A
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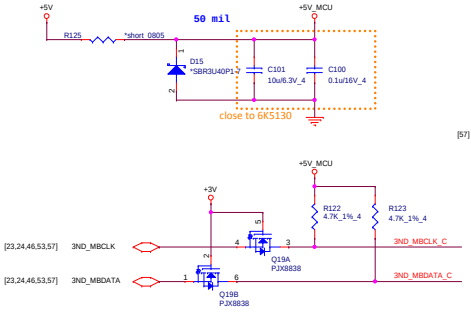
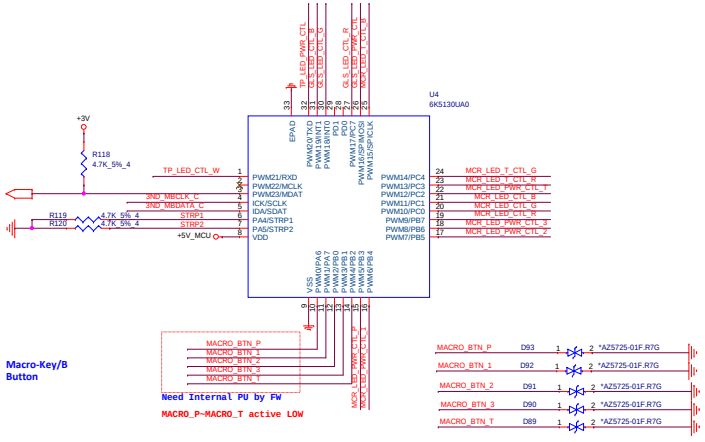
UIF Controller



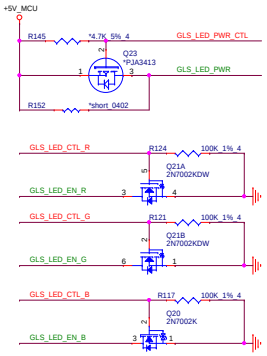


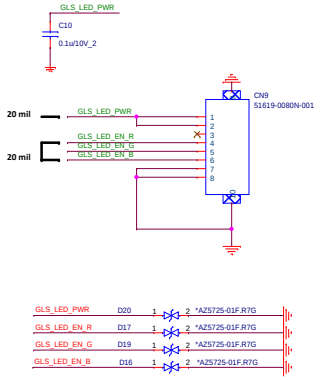
Macro-Key/B Button

Need Internal PU by FW

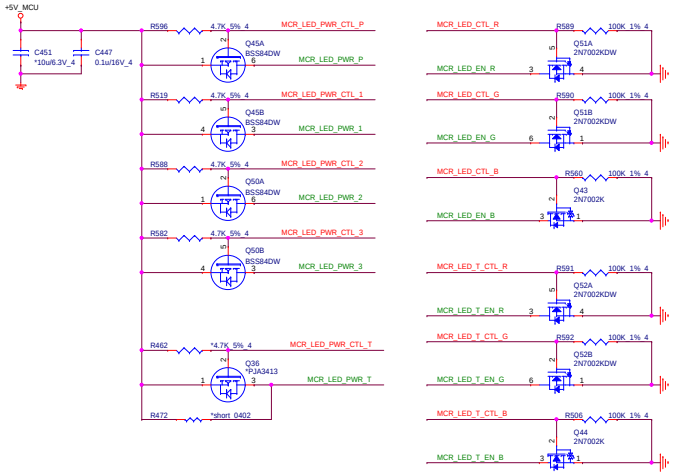
MACRO_P~MACRO_T active LOW

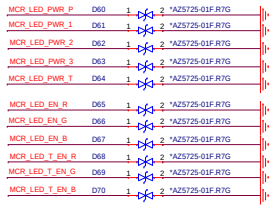
RGB CLASS



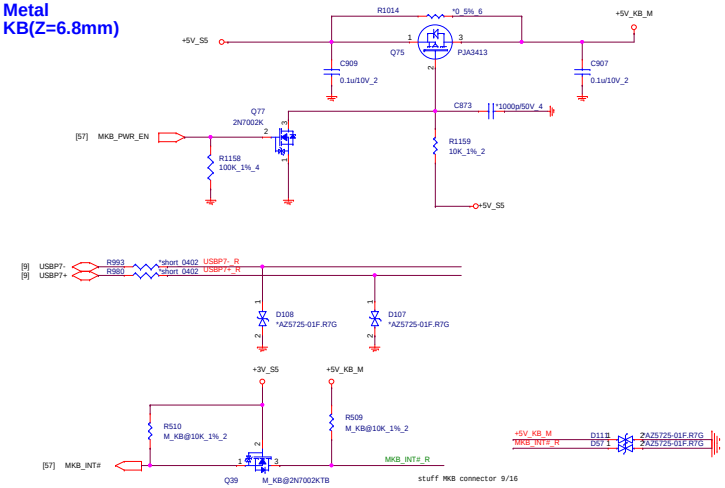


MACRO LED

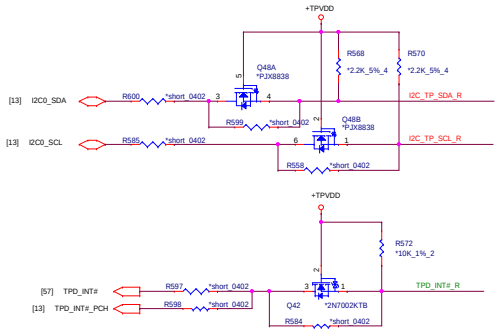


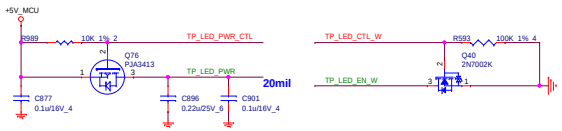


Metal KB(Z=6.8mm)



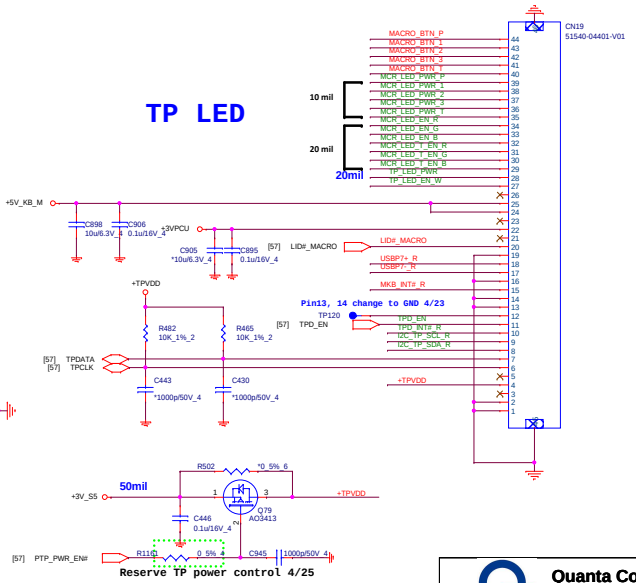
Plastic-Touch PAD





Keyboard Transfer D/B

TP LED



Quanta Computer Inc.
PROJECT : ZGE
Size | Document Number: MCU PWM/LED Driver | Rev 1A
Date: Friday, May 03, 2019 | Sheet 54 of 78

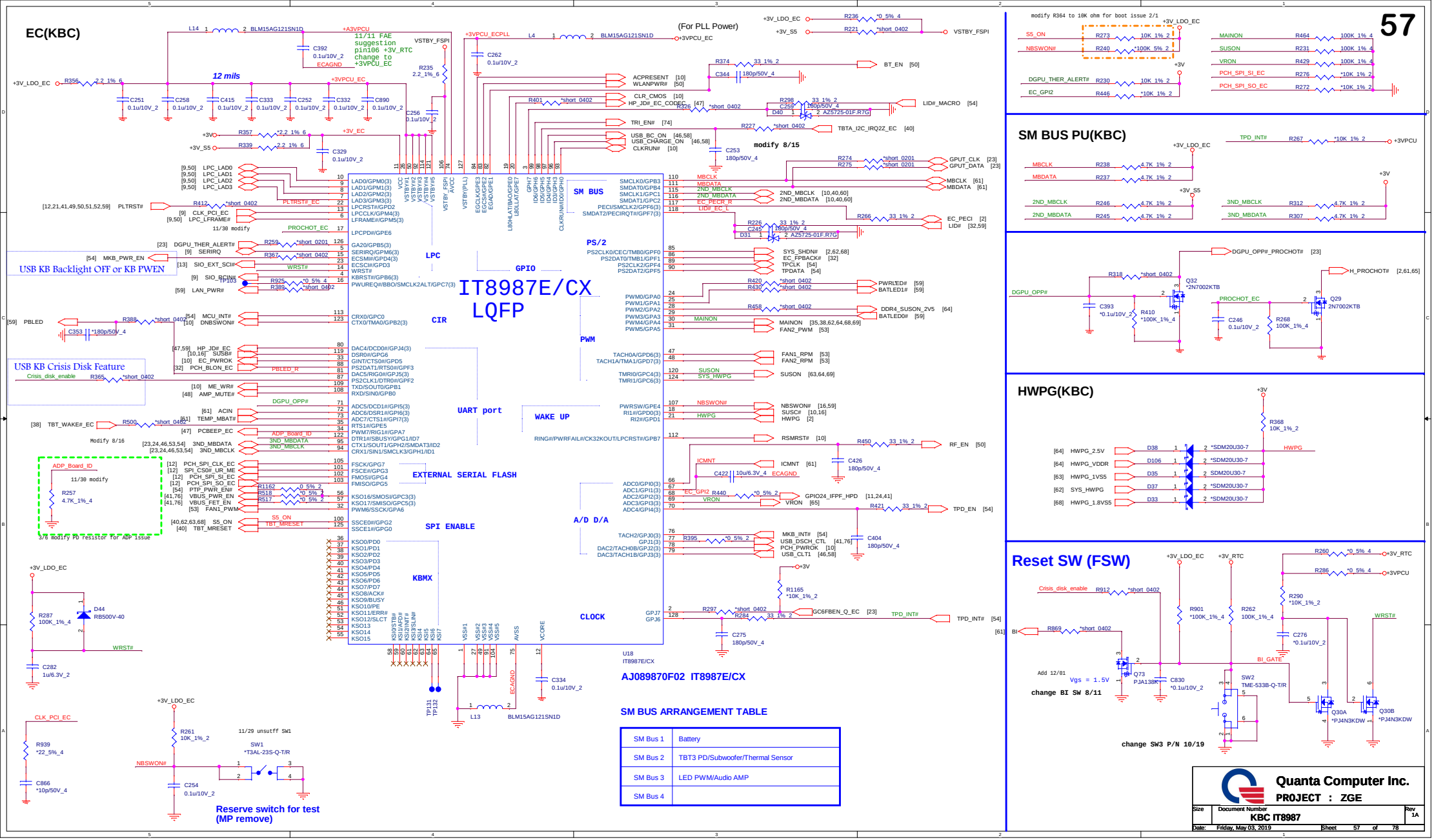
Quanta Computer Inc.

PROJECT : ZGE

Size	Document Number	Rev
	Macro key/LCD Cover/TP	1A

Date: Friday, May 03, 2019 Sheet 56 of 78

EC(KBC)



AJ089870F02 IT8987E/CX

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	TBT3 PD/Subwoofer/Thermal Sensor
SM Bus 3	LED PWM/Audio AMP
SM Bus 4	

modify R364 to 10K ohm for boot issue 2/1

57

SM BUS PU(KBC)

HWPG(KBC)

Reset SW (FSW)

change BI SW 8/11

change SW3 P/N 10/19

Add 12/01

Vgs = 1.5V

Quanta Computer Inc.

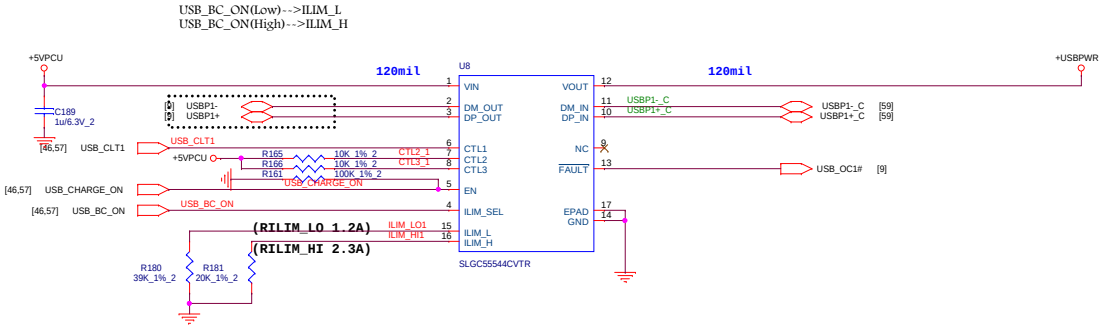
PROJECT : ZGE

Size	Document Number	Rev
	KBC IT8987	1A

Date: Friday, May 03, 2019 Sheet 57 of 78

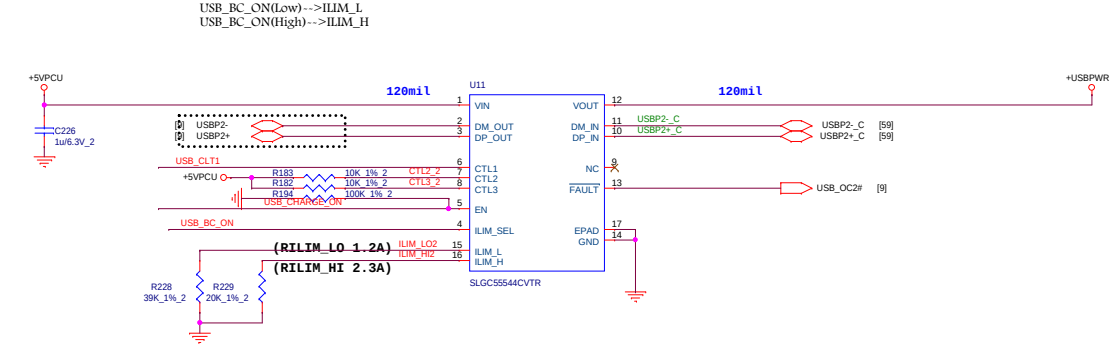
USB Charger (UBC)_BC 1.2

Part Number	Description
AL002544001	TPS2544RTER
AL055544001	SLGC55544CVTR



USB Charger (UBC)_BC 1.2

Part Number	Description
AL002544001	TPS2544RTER
AL055544001	SLGC55544CVTR



Hole

BOT side

WiFi nut

HOLE22 H-TC228BC181D130P2

BOT side

SSD CHASIS nut

HOLE25 h-tc228bc189d146p2

SSD nut

HOLE21 H-TC228BC181D138P2

HOLE27 H-TC228BC181D138P2

HOLE28 *hg-tic315bc394d118p2

HOLE1 *hg-tic315bc394d118p2

HOLE2 *hg-tic315bc394d118p2

HOLE19 *hg-tic315bc394d118p2

HOLE16 *HG-TIC315BC394D118P2

HOLE26 *HG-C276D118P2

HOLE17 *hg-c315d118p2

HOLE12 *HG-TIC315BC394D118P2

HOLE13 *hg-c315d118p2

HOLE24 *hg-c315d118p2

HOLE4 *hg-c315d118p2

HOLE5 *hg-c315d118p2

HOLE29 *hg-c315d118p2

HOLE20 *H-C315D220P2

HOLE15 *H-TIC220BC283D146P2

HOLE14 *H-TIC220BC283D146P2

HOLE6 *H-TIC220BC283D146P2

HOLE8 *H-TIC220BC283D146P2

HOLE7 *H-TIC220BC283D146P2

HOLE11 *H-TIC220BC283D146P2

HOLE30 *H-TIC220BC283D146P2

HOLE9 *H-TIC220BC283D146P2

SPAD2 *SPAD-C315

HOLE23 *H-C102D102N

HOLE10 *H-ZGE-1N

HOLE18 *H-O114X102D114X102N

2D barcode

HOLE3 *2D-BARCODE-8X8-S

2D barcode

HOLE31 *2D-BARCODE-8X8-S

VGA Shrapnel

S1 CLIP-39X35-100X18-3P

S3 CLIP-39X35-100X18-3P

S6 CLIP-39X35-100X18-3P

S7 CLIP-39X35-100X18-3P

S8 CLIP-39X35-100X18-3P

S10 CLIP-39X35-100X18-3P

S13 CLIP-39X35-100X18-3P

S15 CLIP-39X35-100X18-3P

S14 CLIP-39X35-100X18-3P

S12 CLIP-39X35-100X18-3P

S11 CLIP-39X35-100X18-3P

S9 CLIP-39X35-100X18-3P

S5 CLIP-39X35-100X18-3P

S4 CLIP-39X35-100X18-3P

S2 CLIP-39X35-100X18-3P

SPAD3 *PAD-ZGE-1

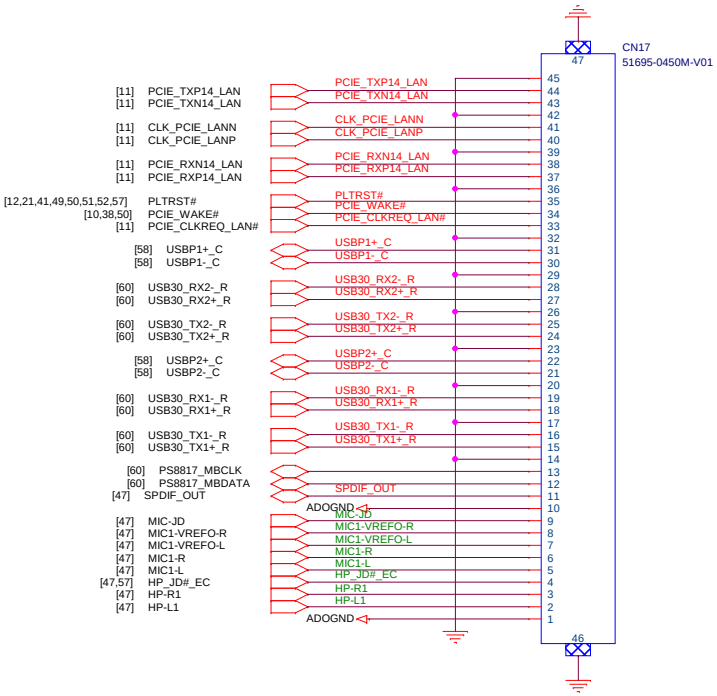
	P/N	Description
WLAN M.2 Nut	MBLI8001010	WLAN NUT LI8(MBLI8001,3A)COPPER
SSD Nut X 2	MBZHP001010	SMT NUT THERMAL ZHP(MBZHP001,3A)COPPER
SSD Nut (CHASIS)	MBZS8001010	MB STEEL NUT WIFI ZS8(MBZS8001,REV3A)

Quanta Computer Inc.

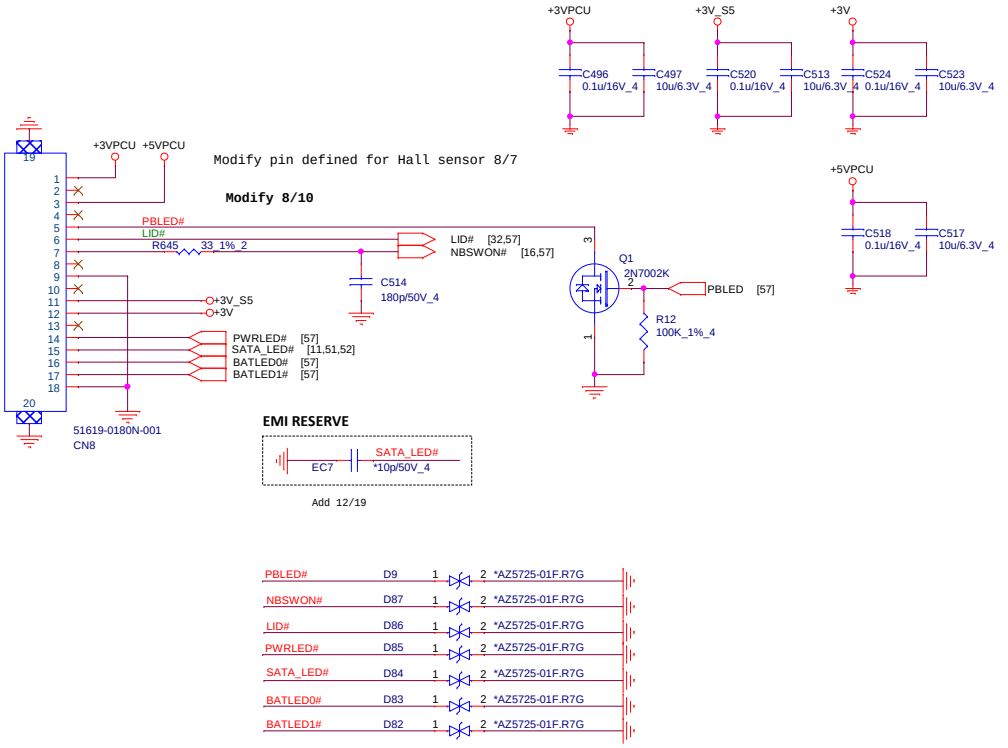
PROJECT : ZGE

Size	Document Number	Rev
	DB USB3 Charger/HOLE	1A
Date: Friday, May 03, 2019	Sheet 58 of 78	

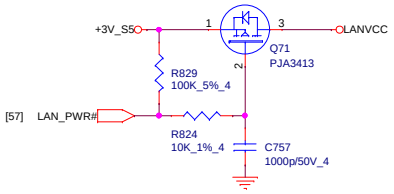
Audio/USB/LAN Board Conn

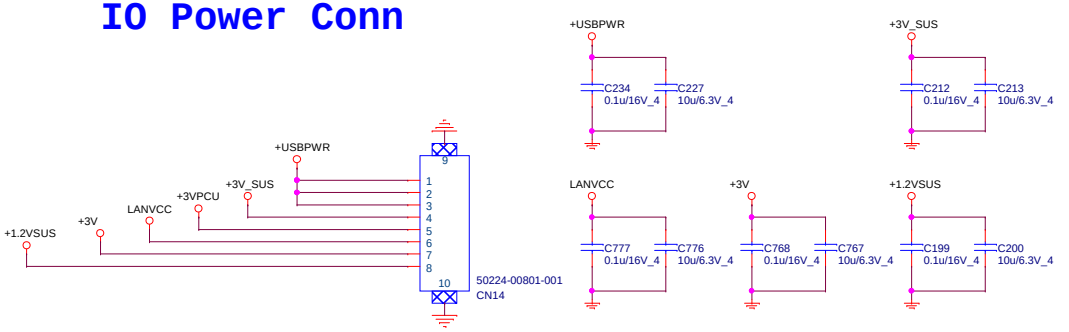


Power & LED Board Conn



IO Power Conn





+3V_SUS [46,60,62,63]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,62,63,64,65,68,70,73,75]
+3VPCU [9,10,12,14,16,32,37,39,40,47,54,57,61,62,68,70,75]
+1.2VSUS [2,6,10,14,17,18,19,20,46,60,64,75]

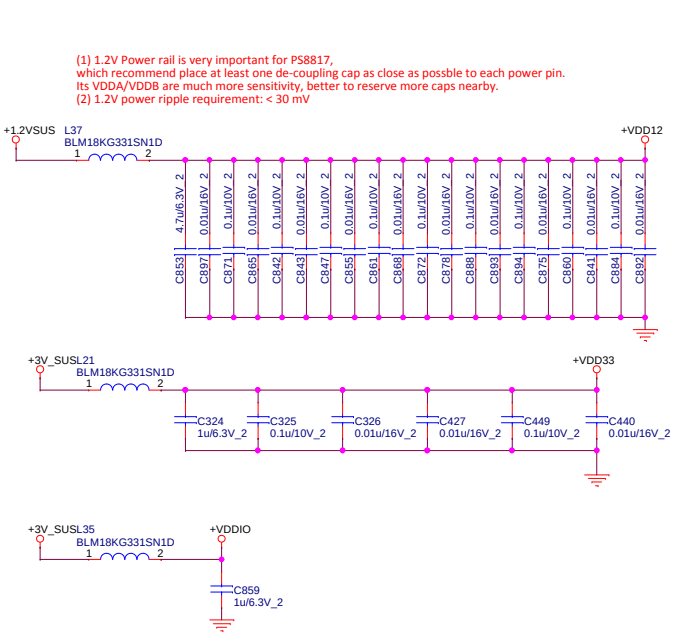
Quanta Computer Inc.
PROJECT : ZGE

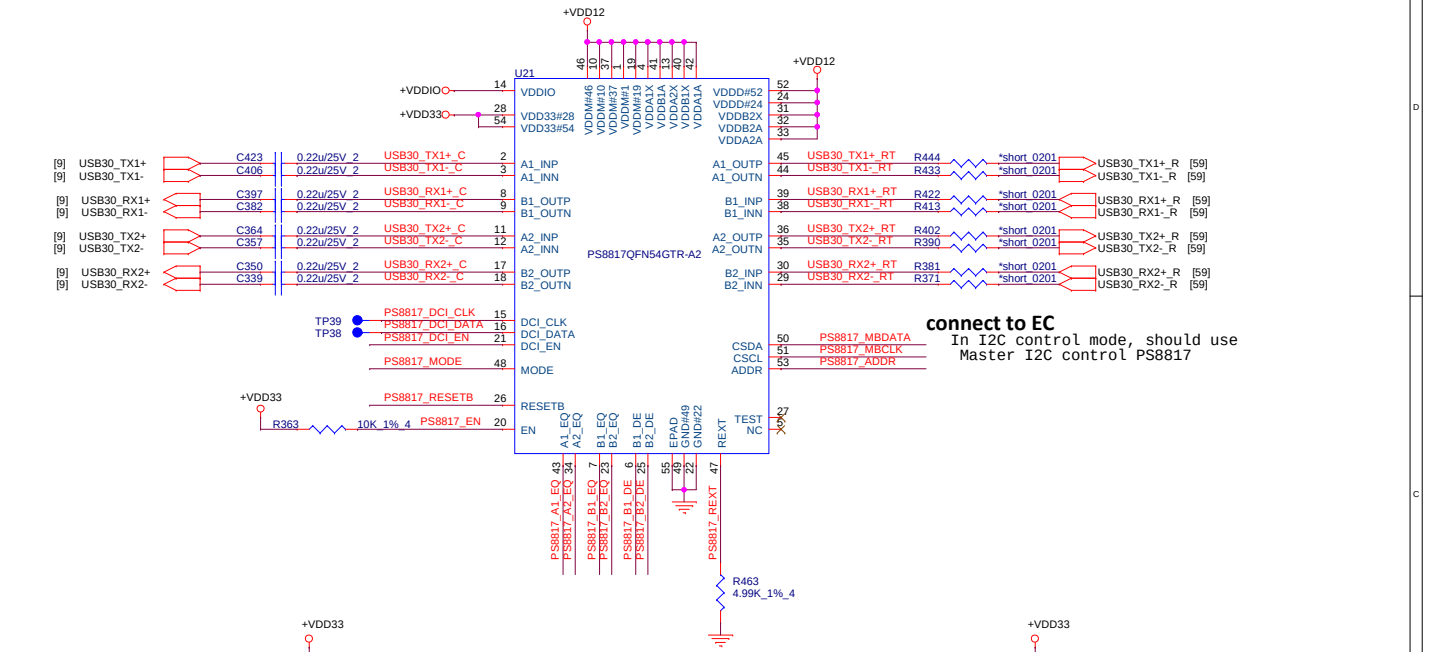
Size	Document Number	Rev
	IO/B	1A

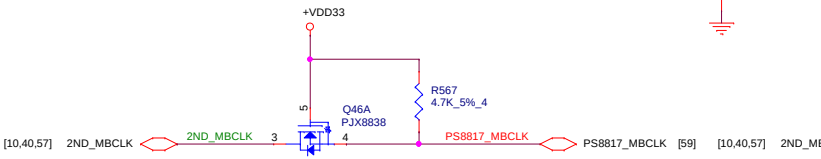
Date: Friday, May 03, 2019 Sheet 59 of 78

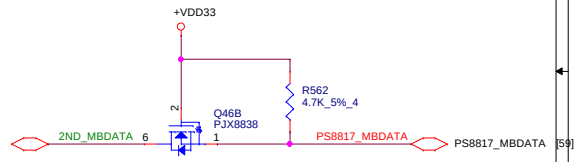
USB3 RE-TIMER FOR IO/DB

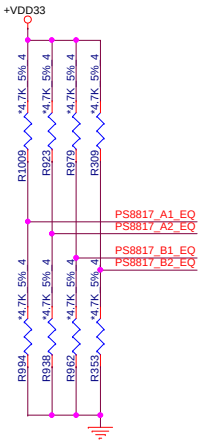
(1) 1.2V Power rail is very important for PS8817,
which recommend place at least one de-coupling cap as close as possble to each power pin.
Its VDDA/VDDB are much more sensitivity, better to reserve more caps nearby.
(2) 1.2V power ripple requirement: < 30 mV









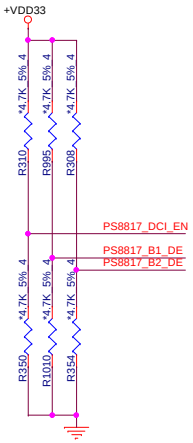


A1_EQ:USB Host facing RX channel receiver equalization setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

A2_EQ:USB Host facing RX channel receiver equalization setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

B1_EQ:USB connector facing RX channel receiver equalization setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

B2_EQ:USB connector facing RX channel receiver equalization setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

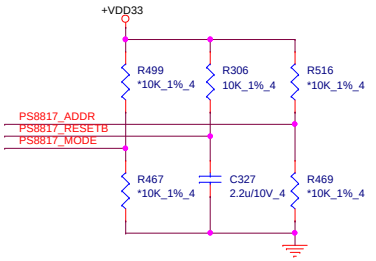


A1_DE:USB connector facing TX channel De-emphasis setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

A2_DE: USB connector facing TX channel De-emphasis setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

B1_DE:USB Host facing TX channel De-emphasis setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD

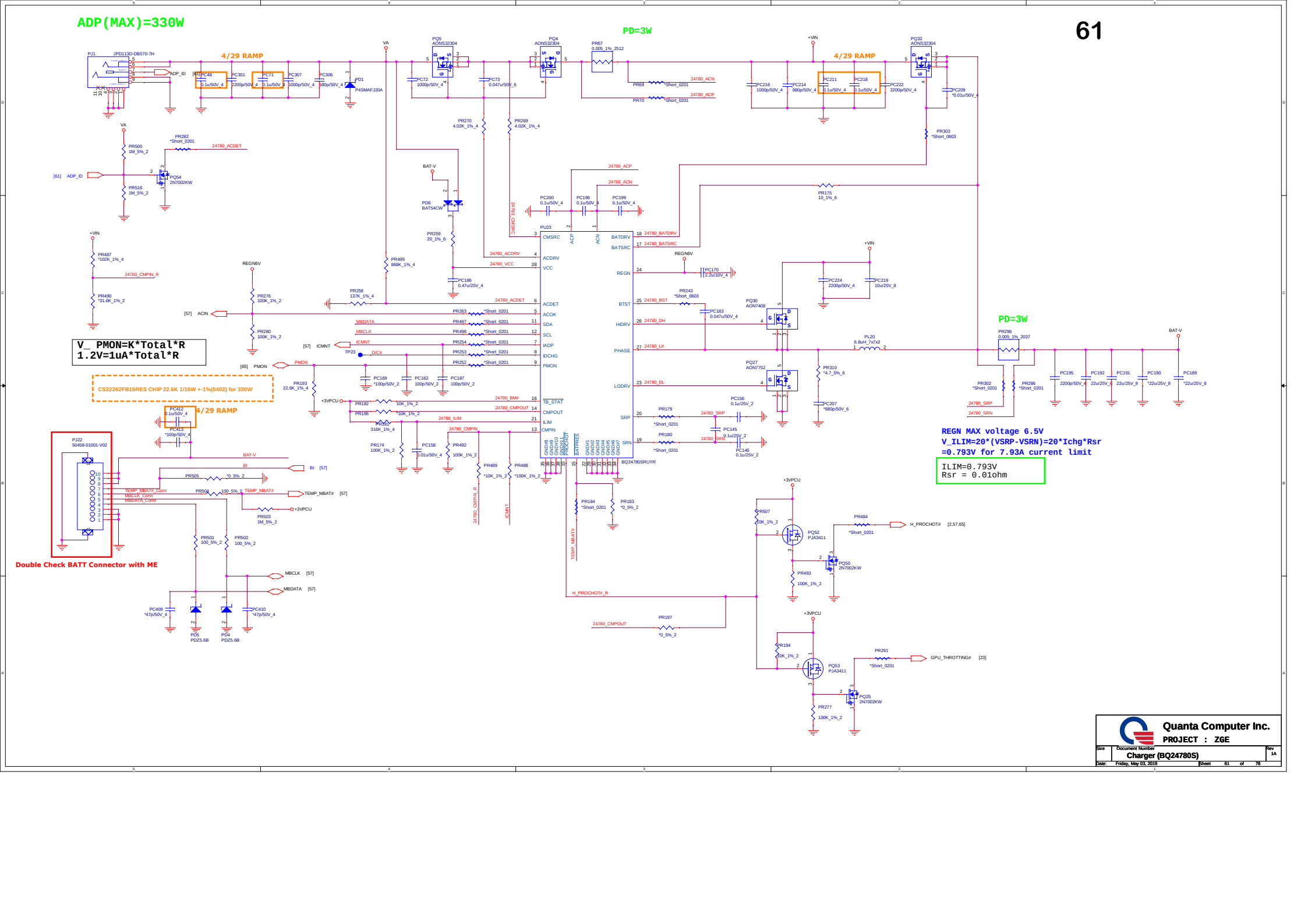
B2_DE: USB Host facing TX channel De-emphasis setting;
3-state input, internally tied to VDD33/2, 3.3V tolerance.
L: TBD
M: TBD(Default)
H: TBD



ADDR: I2C control bus address. Internally pull down at 150k次, 3.3V I/O.
L: 0x50~0x57(Default I2C slave address)
H: 0xE0~0xE7

MODE: Operation mode configuration, default is in middle level
L: 5G redriver mode, 10G retimer mode, adaptive EQ.
M: 5G redriver mode, 10G retimer mode, fix EQ (default)

Quanta Computer Inc.
PROJECT : ZGE
Size | Document Number: Power Board / UIF LED | Rev 1A
Date: Friday, May 03, 2019 | Sheet 60 of 78


ADP(MAX)=330W
PD=3W
61
4/29 RAMP
4/29 RAMP
4/29 RAMP
PD=3W
V_ PMON=K*Total*R
1.2V=1uA*Total*R
CS32262FB15RES CHIP 22.6K 1/16W +-1%(0402) for 330W
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 7.93A current limit
ILIM=0.793V
Rsr = 0.01ohm
Double Check BATT Connector with ME
Quanta Computer Inc.
PROJECT : ZGE
Charger (BQ24780S)
Friday, May 03, 2019

+VIN [32,61,63,64,65,66,67,68,69,73,75,76]
+5VPCU [46,58,59,63,75]
+3VPCU [9,10,12,14,16,32,37,39,40,47,54,57,59,61,68,70,75]
SYS_SHDN# [2,57,68]
3V_LDO [68,74]

+5VPCU
5 Volt +/- 5%
TDC : 15A
PEAK : 20.3A
OCP : 28A
Width : 720mil

Isat=27A

Rds(on)=3m ohm

OCP:28A (For BAT 4S1P)
L(ripple current)
=(12-5)*5/(2.2u*0.3M*12)
=4.419A
Iocp=28-(4.419/2)=25.79A
Vth=(25.79A*2.99mOhm)+1mV=78.113mV
R(Ilim)=(78.113mV*8)/10uA
~62.49K

Power auto recovery

+3VPCU
3.3 Volt +/- 5%
TDC : 13A
PEAK : 16A
OCP : 21A
Width : 520mil

Isat=27A

Rds(on)=4.9m ohm

OCP:21A (For BAT 4S1P)
L(ripple current)
=(12-3.3)*3.3/(1u*0.355M*12)
~3.0633A
Iocp=21-(3.0633/2)=19.468A
Vth=(19.468A*4.9mOhm)+1mV=96.393mV
R(Ilim)=(96.393mV*8)/10uA
=77.11K

+5V_S5 [54,64,65,66,67,69,70,71,72,73,75]
+5V [35,47,48,51,53,54,68,74]
+3V_S5 [14,24,25,35,37,40,41,49,50,54,57,59,64,74]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,63,64,65,68,70,73,75]

TDC : 2.2A
PEAK : 2.9A
Width : 100mil

TDC : 5.1A
PEAK : 6.8A
Width : 220mil

TDC : 3.3A
PEAK : 4.4A
Width : 140mil

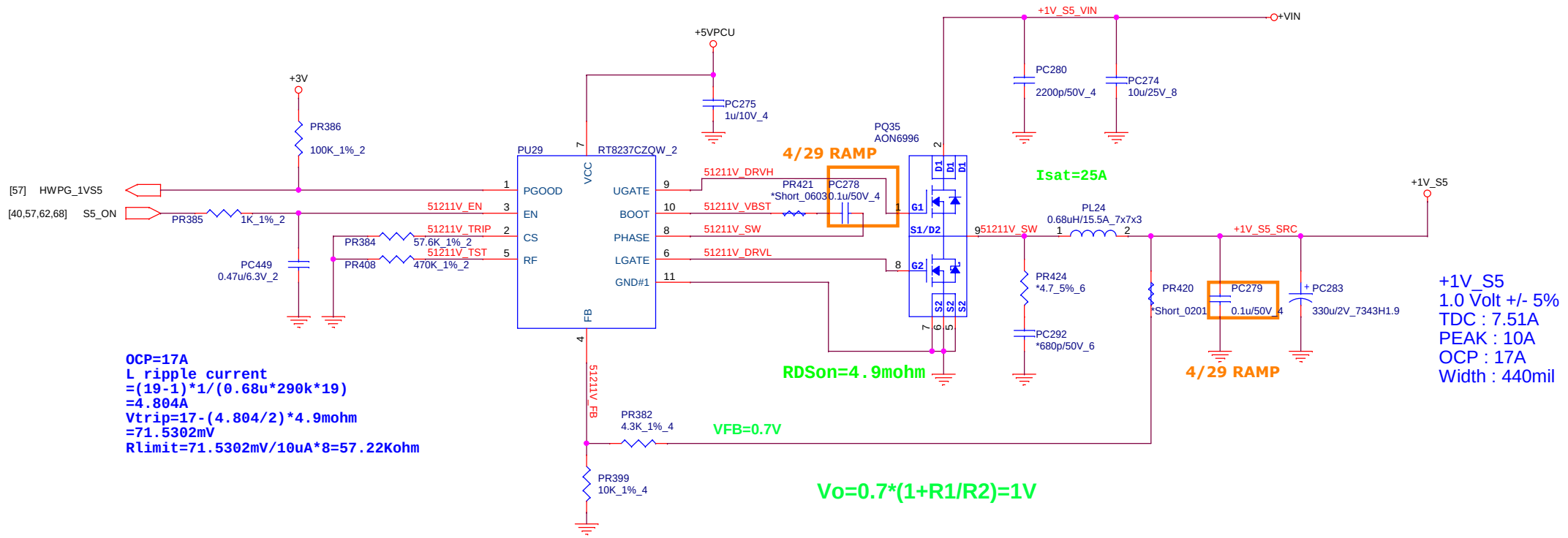
TDC : 5.62A
PEAK : 7.49A
Width : 240mil

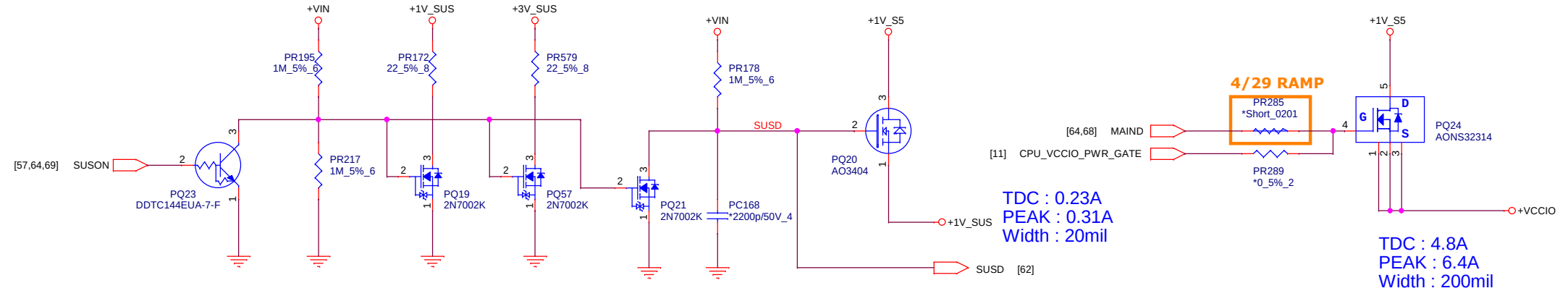
TDC :6A
PEAK : 8A
Width : 200mil

TDC : 0.11A
PEAK : 0.15A

Quanta Computer Inc.			
PROJECT : ZGE			
Size	Document Number		Rev
	SYSTEM 5V/3V (TPS51225R)		1A
Date: Friday, May 03, 2019		Sheet 62 of 78	

+VIN [32,61,62,64,65,66,67,68,69,73,75,76]
+1V_S5 [10,11,14]
+5VPCU [46,58,59,62,75]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,64,65,68,70,73,75]
+1V_SUS [6]
+VCCIO [2,3,6,65,68]

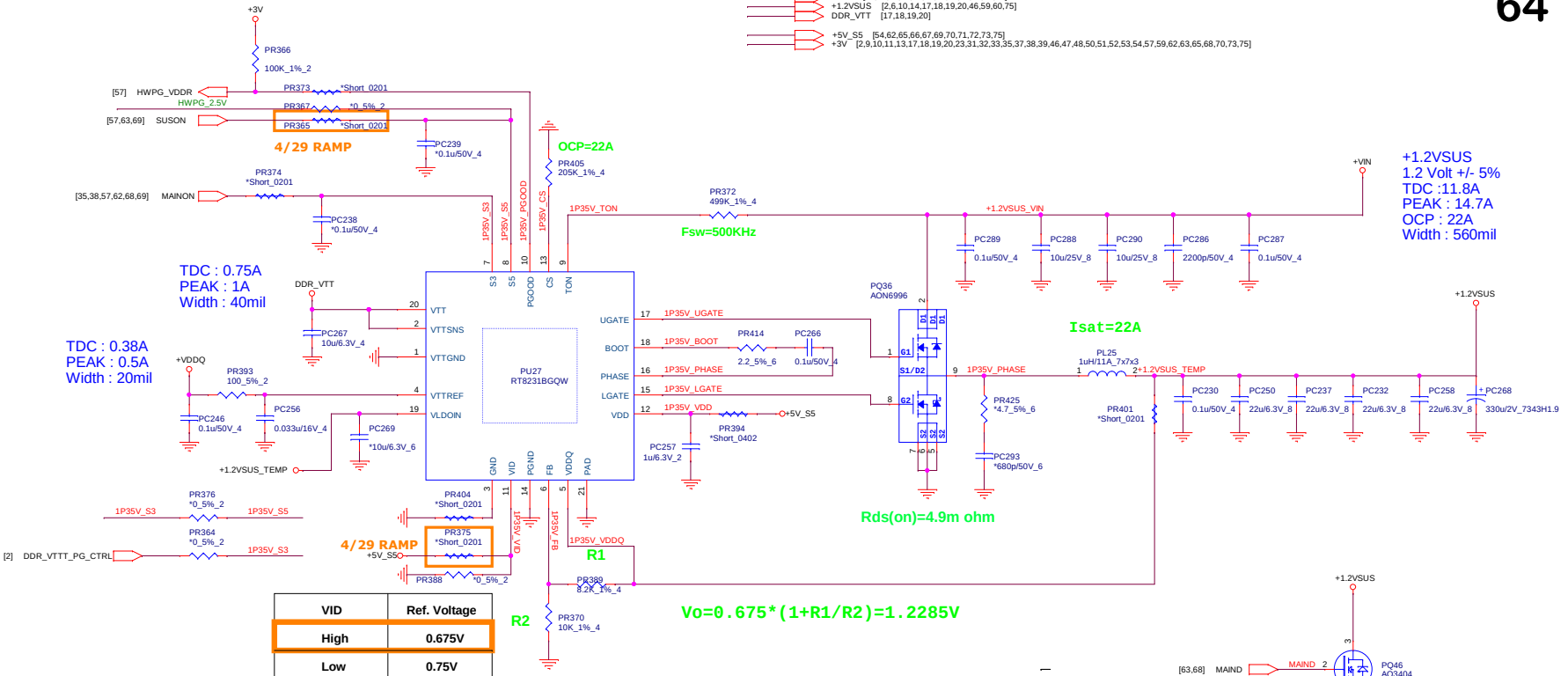




Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: +1V_S5 (RT8237CZQW_2)	Rev: 1A
Date: Friday, May 03, 2019	Sheet 63 of 78	

+VIN [32,61,62,63,65,66,67,68,69,73,75,76]
+1.2VSUS [2,6,10,14,17,18,19,20,46,59,60,75]
DDR_VTT [17,18,19,20]

+5V_S5 [54,62,65,66,67,69,70,71,72,73,75]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,63,65,68,70,73,75]



VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=22A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=22-(2.248/2)*4.9mohm
=102.291mV
Rlimit=102.291mV/5uA*10=204.58Kohm

DDR=1.2V
R1=7.87K/F_4
R2=10K/F_4

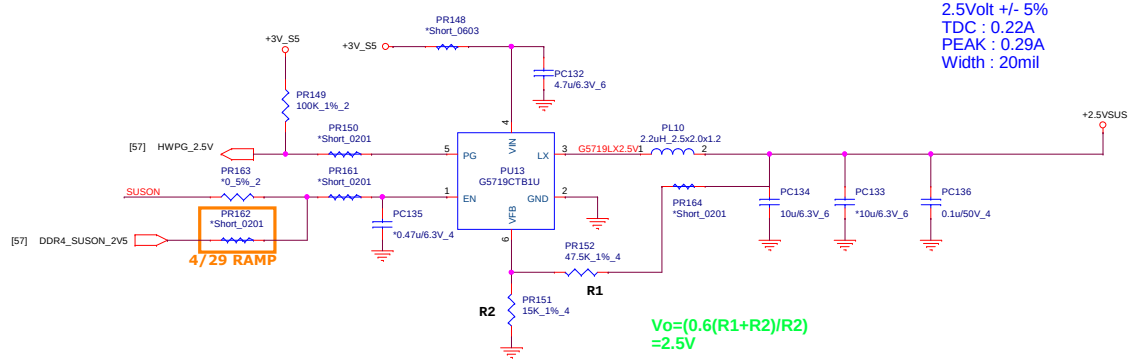
	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

TDC : 0.22A
PEAK : 0.29A

+2.5VSUS Power Rail For DDR4

+3V_S5 [14,24,25,35,37,40,41,49,50,54,57,59,62,74]
+2.5VSUS [17,18,19,20]

+2.5VSUS
2.5Volt +/- 5%
TDC : 0.22A
PEAK : 0.29A
Width : 20mil



Vo=(0.6(R1+R2)/R2)
=2.5V

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	DDR4_+1.2VSUS (RT8231BGQW)	1A

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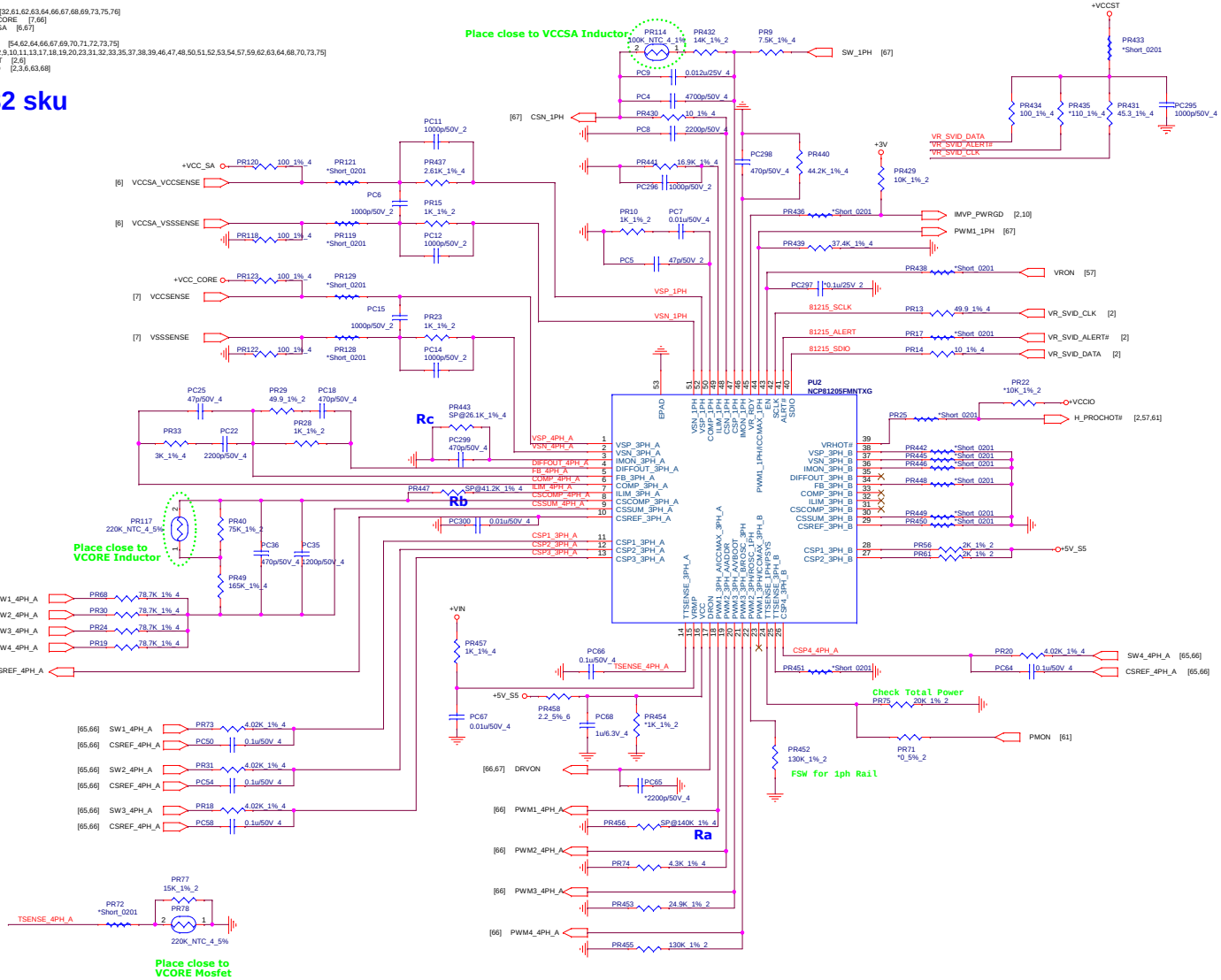
+VIN [32,61,62,63,64,66,67,68,69,73,75,76]
+VCC_CORE [7,66]
+VCC_SA [6,67]
+5V_S5 [54,62,64,66,67,69,70,71,72,73,75]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,63,64,68,70,73,75]
+VCCST [2,6]
+VCCIO [2,3,6,63,68]

For H82 sku



CFL-H82 & (K SKU= H82*1.25) (4+1 Phase)

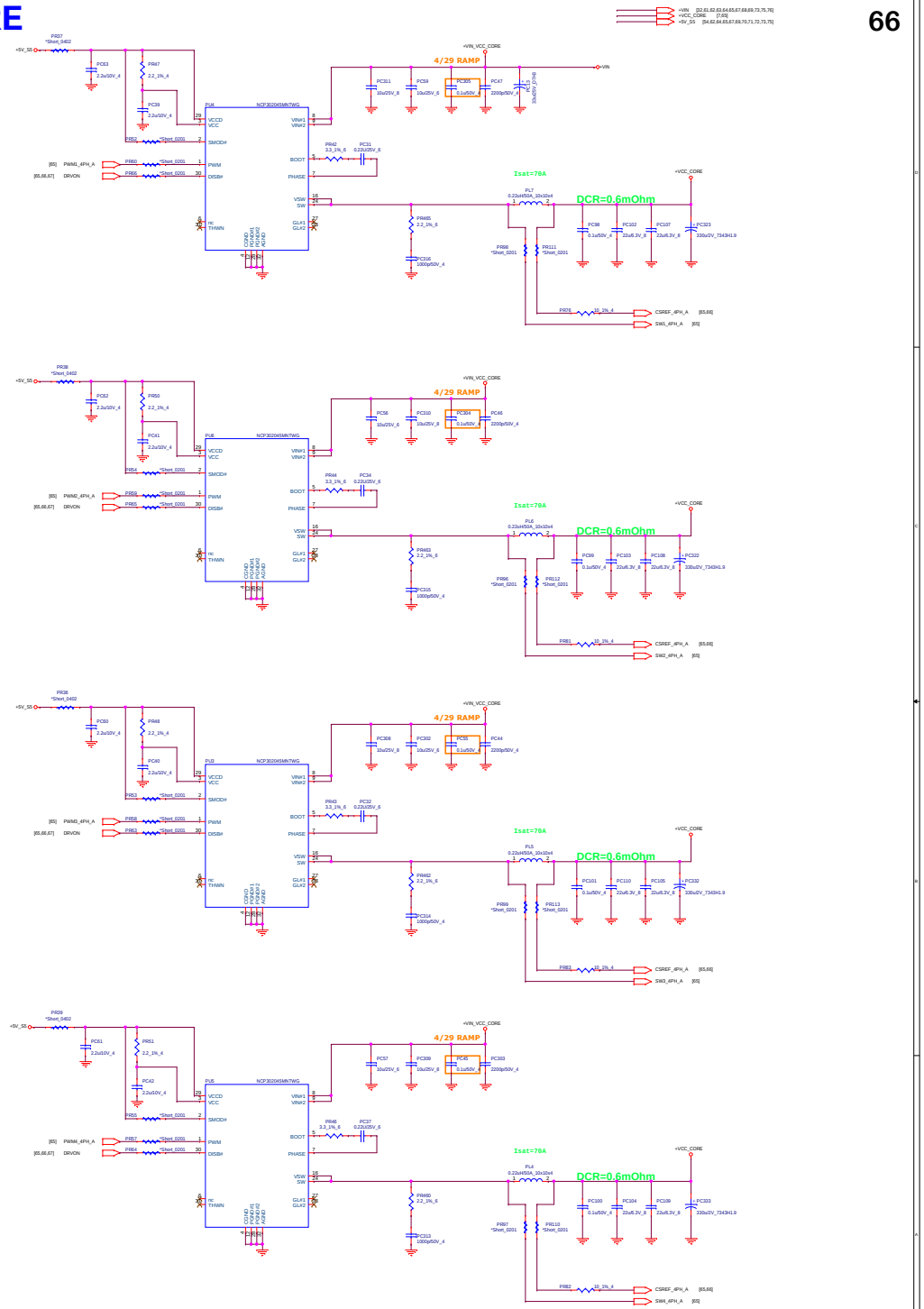
VCORE	VCCSA
Icc TDC：86A (K=108A)	Icc TDC：10A
Icc Max：140A (K=175A)	Icc Max：11.1A
OCP：185A (K=225A)	OCP：20A
VCORE L/L：	**VCORE L/L：**
R_DC_LL：1.8mV/A	R_DC_LL：10.3mV/A
R_AC_LL：1.8mV/A	R_AC_LL：10.3mV/A

Default Setting(H82 / K SKU)

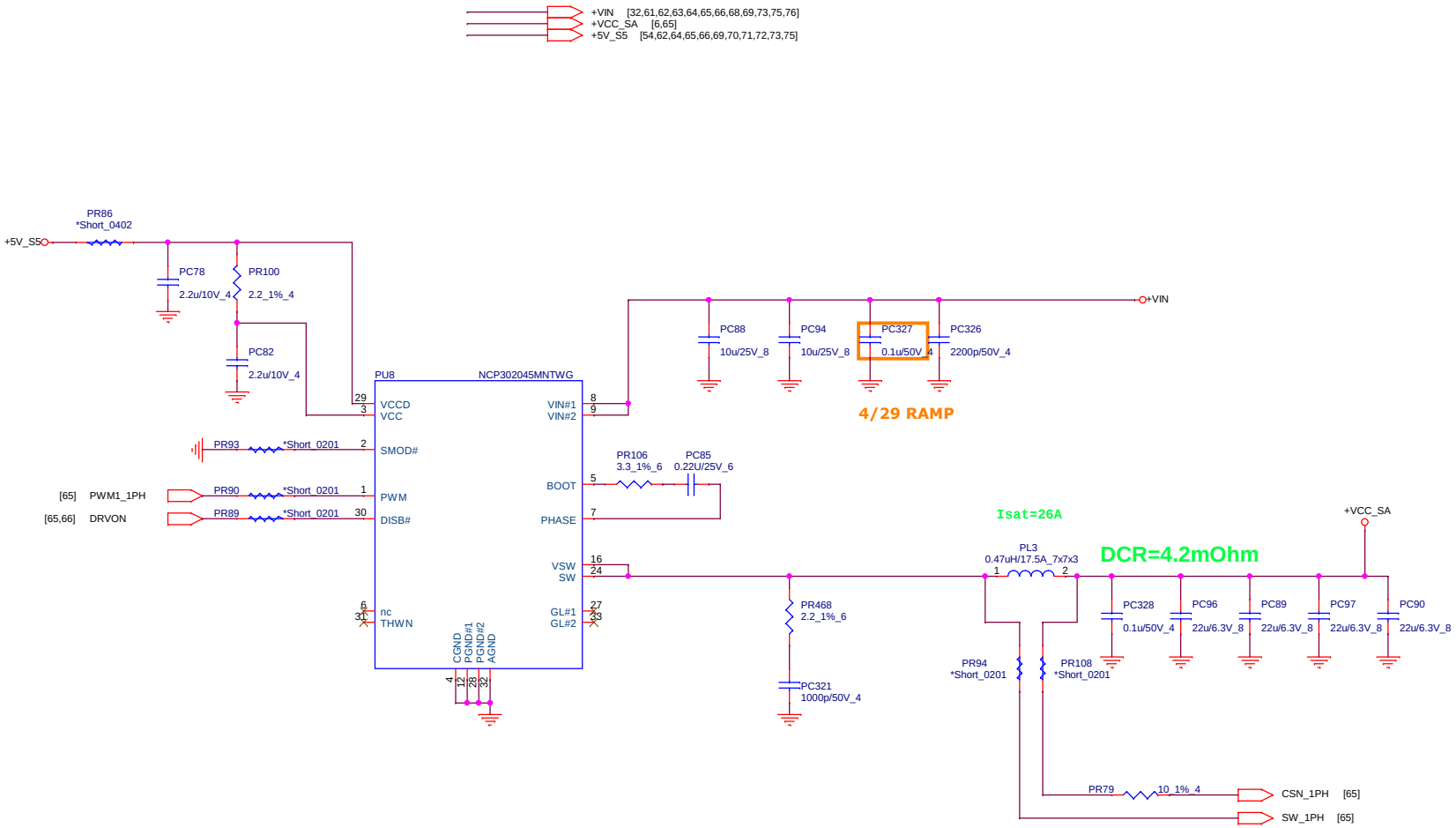
Item	Location	H82	K SKU
Ra	PR456	CS41132FB17 *113K ohm*	CS41402FB14 *140K ohm*
Rb	PR447	CS33322FB13 *33.2K ohm*	CS34122FB19 *41.2K ohm*
Rc	PR443	CS32612FB09 *26.1K ohm*	CS32612FB09 *26.1K ohm*

Quanta Computer Inc.
PROJECT : ZGE
Size | Document Number: CPU VR IC (NCP81215MNTXG) | Rev: 1A
Date: Friday, May 03, 2019 | Sheet 65 of 78

VCORE


+VIN [52,61,62,63,64,65,67,68,69,73,75,76]
+VCC_CORE [7,63]
+5V_S5 [54,62,64,65,67,69,70,71,72,73,75]
4/29 RAMP
Isat=70A
DCR=0.6mOhm
+VCC_CORE
+VIN_VCC_CORE
NCP302045MNTWG
PWM1_4PH_A
PWM2_4PH_A
PWM3_4PH_A
PWM4_4PH_A
DRVON
CSREF_4PH_A
SW1_4PH_A
SW2_4PH_A
SW3_4PH_A
SW4_4PH_A

VCCSA

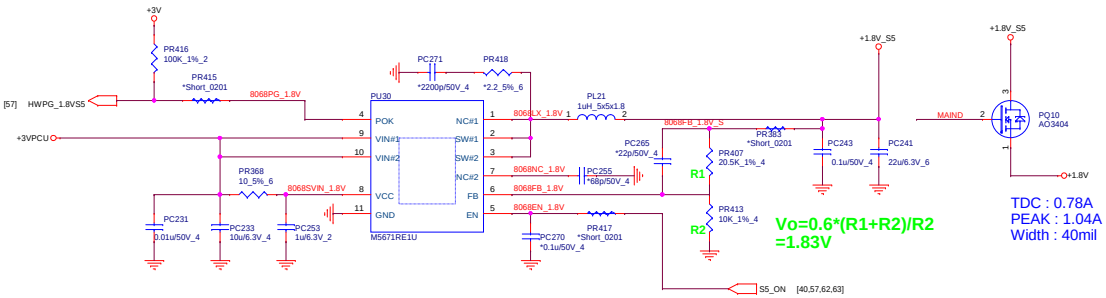


Quanta Computer Inc.		
PROJECT : ZGE		
Size	Document Number: VCCSA 1-Phase Power Stage	Rev: 1A
Date: Friday, May 03, 2019	Sheet 67 of 78	

+3VPCU [9,10,12,14,16,32,37,39,40,47,54,57,59,61,62,70,75]
+1.8V_S5 [14,41]
+1.8V [25,32]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,63,64,65,70,73,75]
3V_LDO [62,74]

+VIN [32,61,62,63,64,65,66,67,69,73,75,76]
+5V [35,47,48,51,53,54,62,74]
+VCCIO [2,3,6,63,65]

+1.8V_S5
1.8Volt +/- 5%
TDC : 1.5A
PEAK : 2A
Width : 80mil

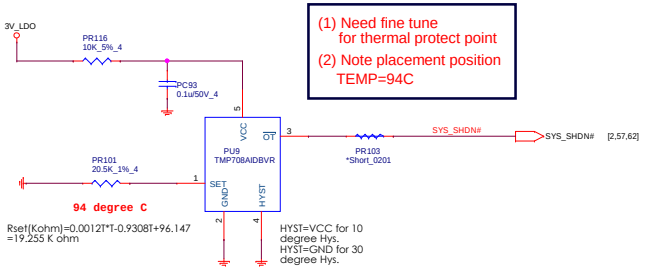


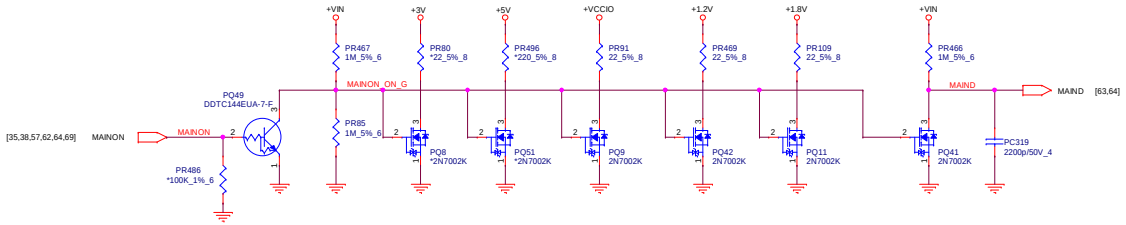
Vo=0.6*(R1+R2)/R2
=1.83V

TDC : 0.78A
PEAK : 1.04A
Width : 40mil

Thermal protection

(1) Need fine tune
for thermal protect point
(2) Note placement position
TEMP=94C





Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	+1.8V_S5/Thermal Protect	1A
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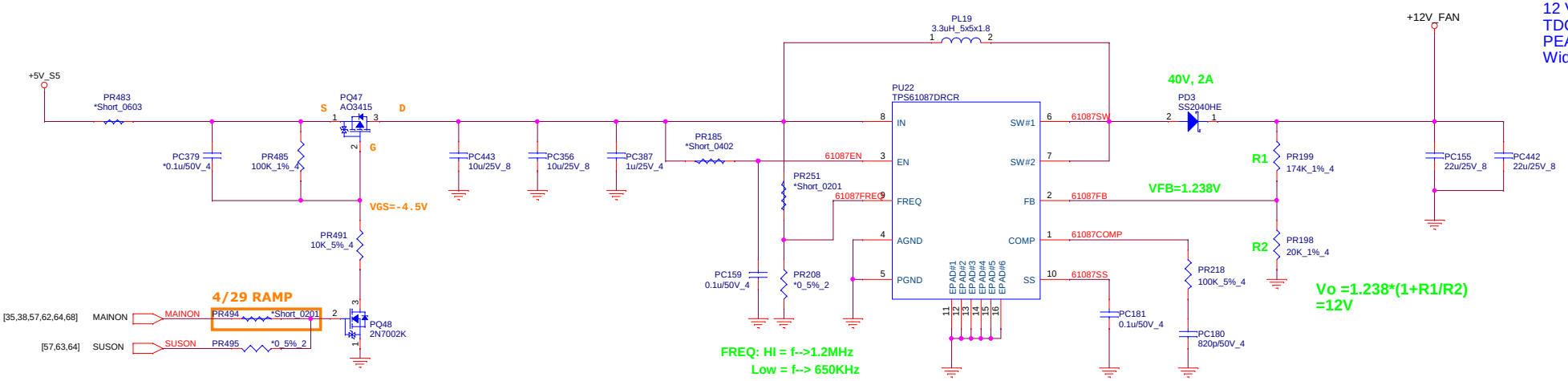
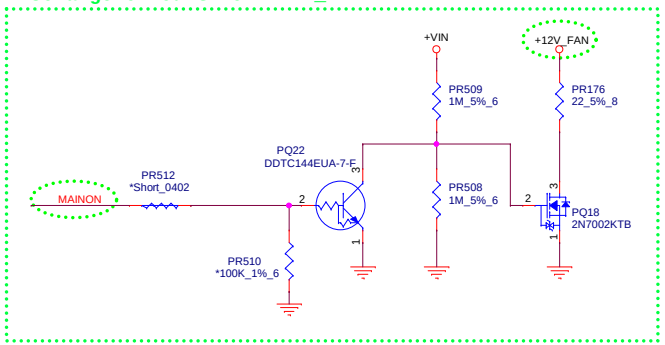
FAN POWER (TPS61087)

[54,62,64,65,66,67,70,71,72,73,75] +5V_S5
[53] +12V_FAN
[32,61,62,63,64,65,66,67,68,73,75,76] +VIN



+12V_FAN
12 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

Discharge Circuit For +12V_FAN



Quanta Computer Inc.			
PROJECT : ZGE			
Size	Document Number		Rev
	FAN POWER (TPS61087)		1A
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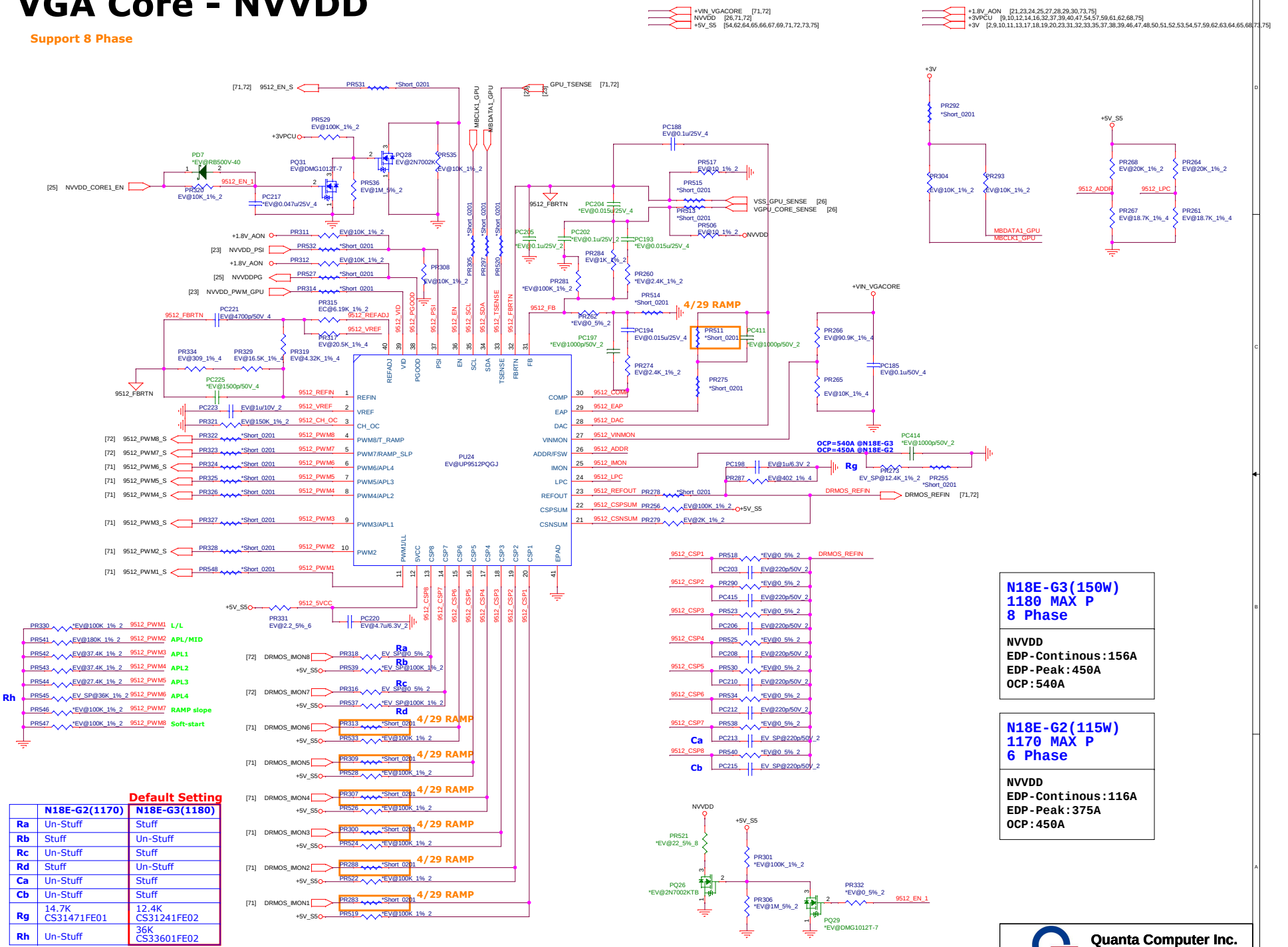
VGA Core - NVVDD

Support 8 Phase



N18E-G3(150W)
1180 MAX P
8 Phase

NVVDD
EDP-Continous:156A
EDP-Peak:450A
OCP:540A

N18E-G2(115W)
1170 MAX P
6 Phase

NVVDD
EDP-Continous:116A
EDP-Peak:375A
OCP:450A

Default Setting

	N18E-G2(1170)	N18E-G3(1180)
Ra	Un-Stuff	Stuff
Rb	Stuff	Un-Stuff
Rc	Un-Stuff	Stuff
Rd	Stuff	Un-Stuff
Ca	Un-Stuff	Stuff
Cb	Un-Stuff	Stuff
Rg	14.7K CS31471FE01	12.4K CS31241FE02
Rh	Un-Stuff	36K CS33601FE02

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	+VGPU (UP9512PQGJ)	1A

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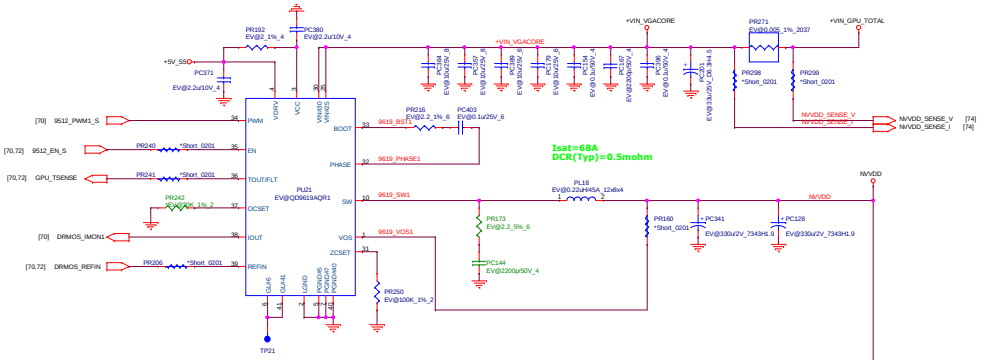
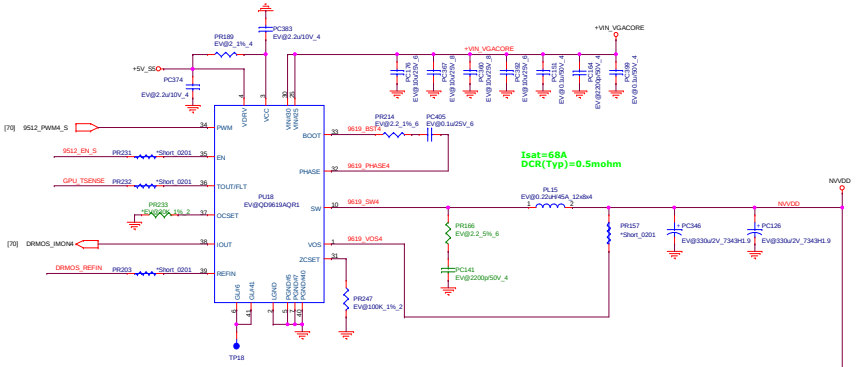
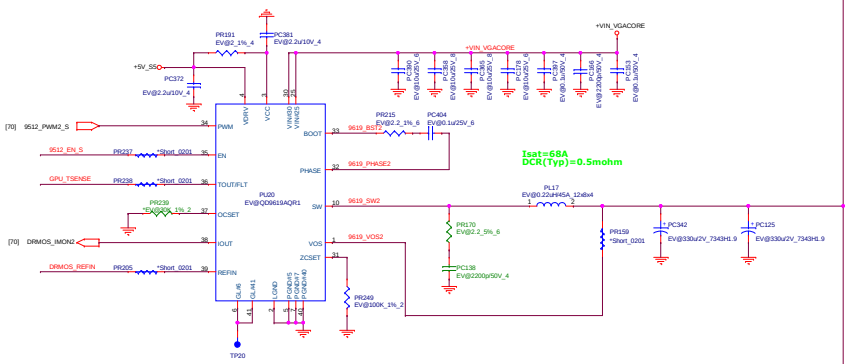
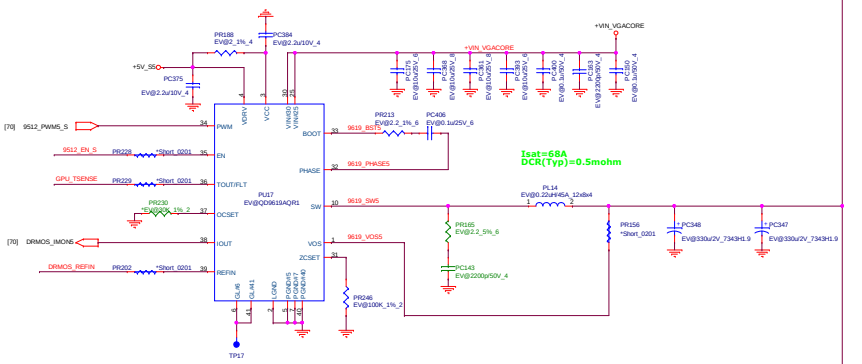
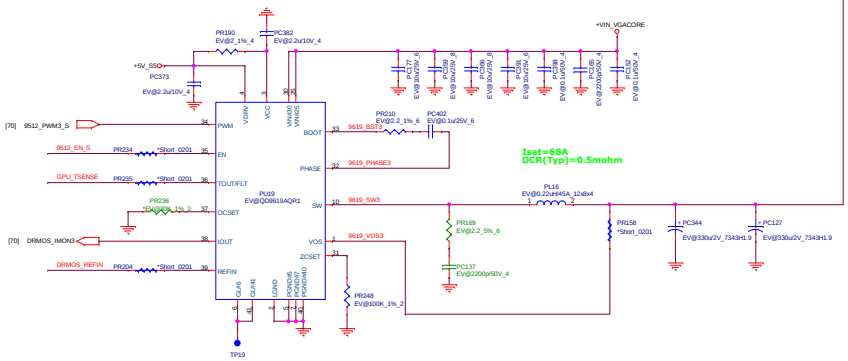
+VIN_GPU_TOTAL [73]
+VIN_VGACORE [70,72]
NVVDD [26,70,72]
+5V_S5 [54,62,64,65,66,67,69,70,72,73,75]

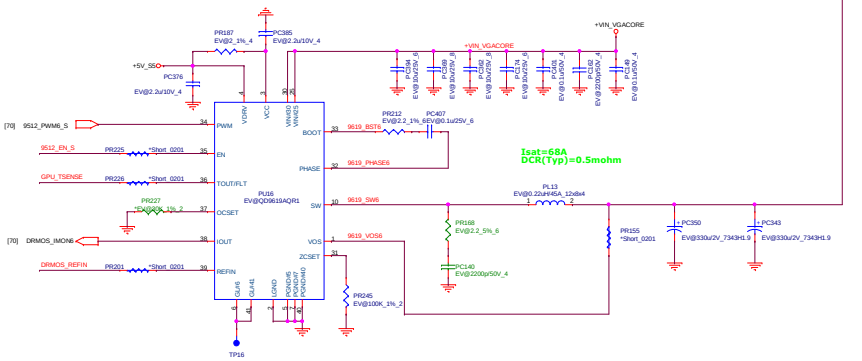












N18E-G3(150W)
1180 MAX P
8 Phase

NVVDD
EDP-Continous:156A
EDP-Peak:450A
OCP:540A

N18E-G2(115W)
1170 MAX P
6 Phase

NVVDD
EDP-Continous:116A
EDP-Peak:375A
OCP:450A

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	+VGPU (UP9512PQGJ)	1A
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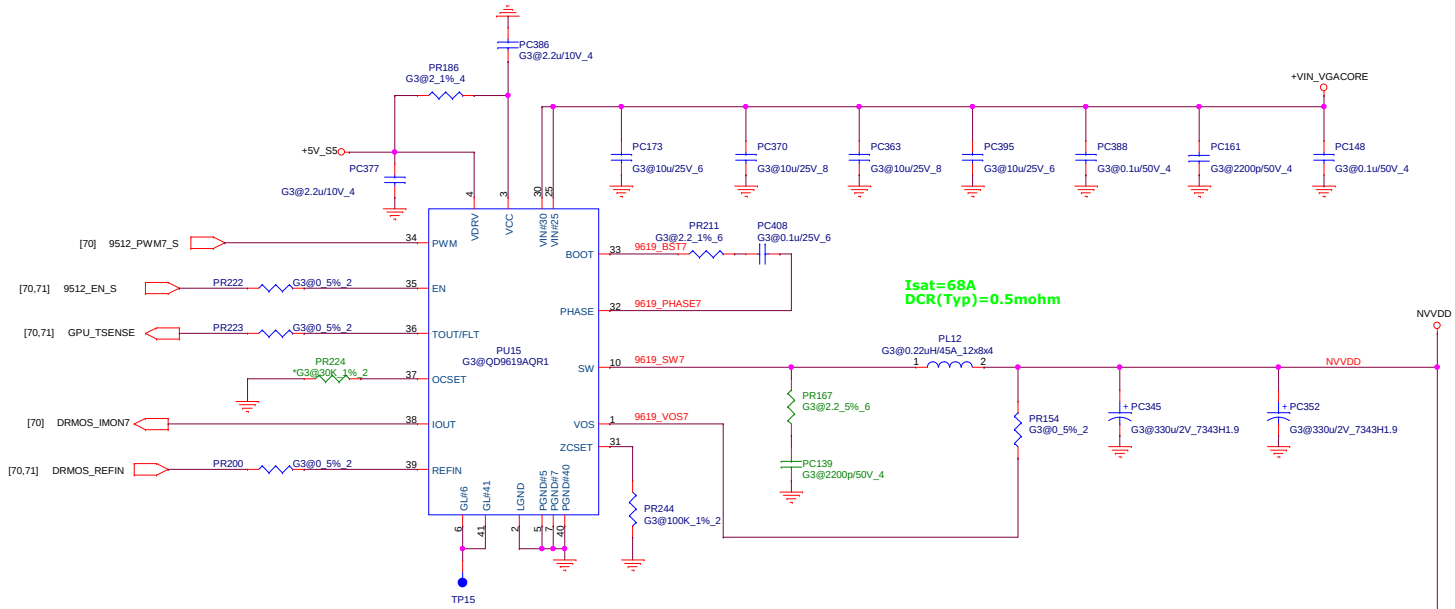
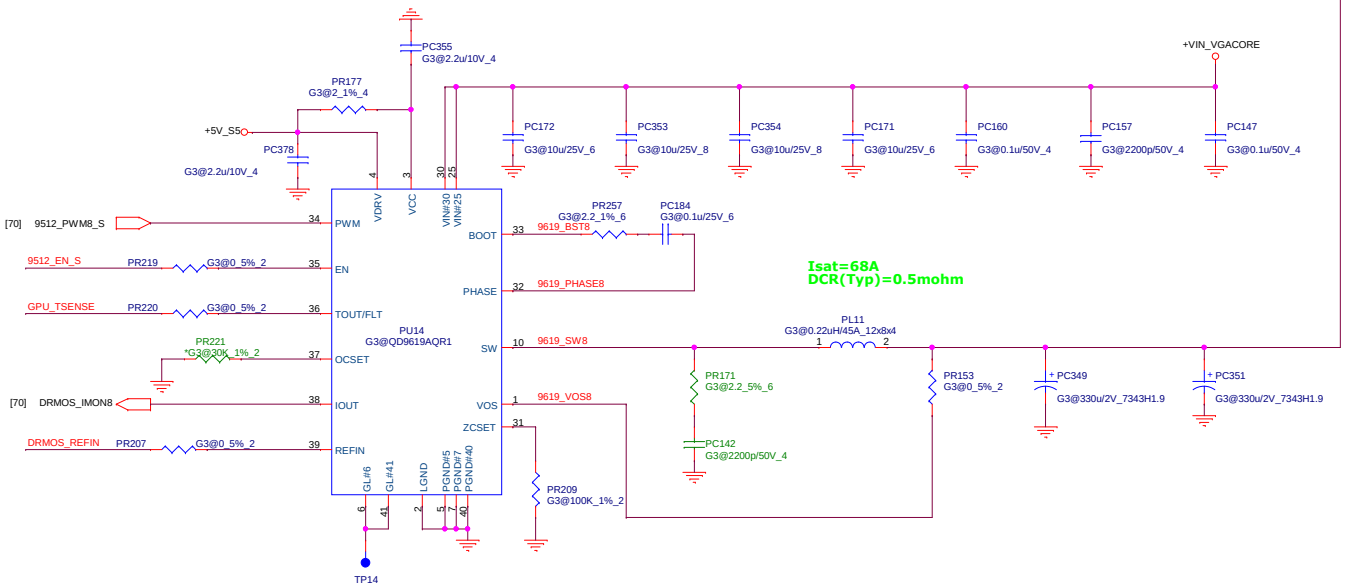
+VIN_VGACORE [70,71]
NVVDD [26,70,71]
+5V_S5 [54,62,64,65,66,67,69,70,71,73,75]





N18E-G3(150W)
1180 MAX P
8 Phase

NVVDD
EDP-Continous:156A
EDP-Peak:450A
OCP:540A

N18E-G2(115W)
1170 MAX P
6 Phase

NVVDD
EDP-Continous:116A
EDP-Peak:375A
OCP:450A

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	+VGPU (UP9512PQGJ)	1A
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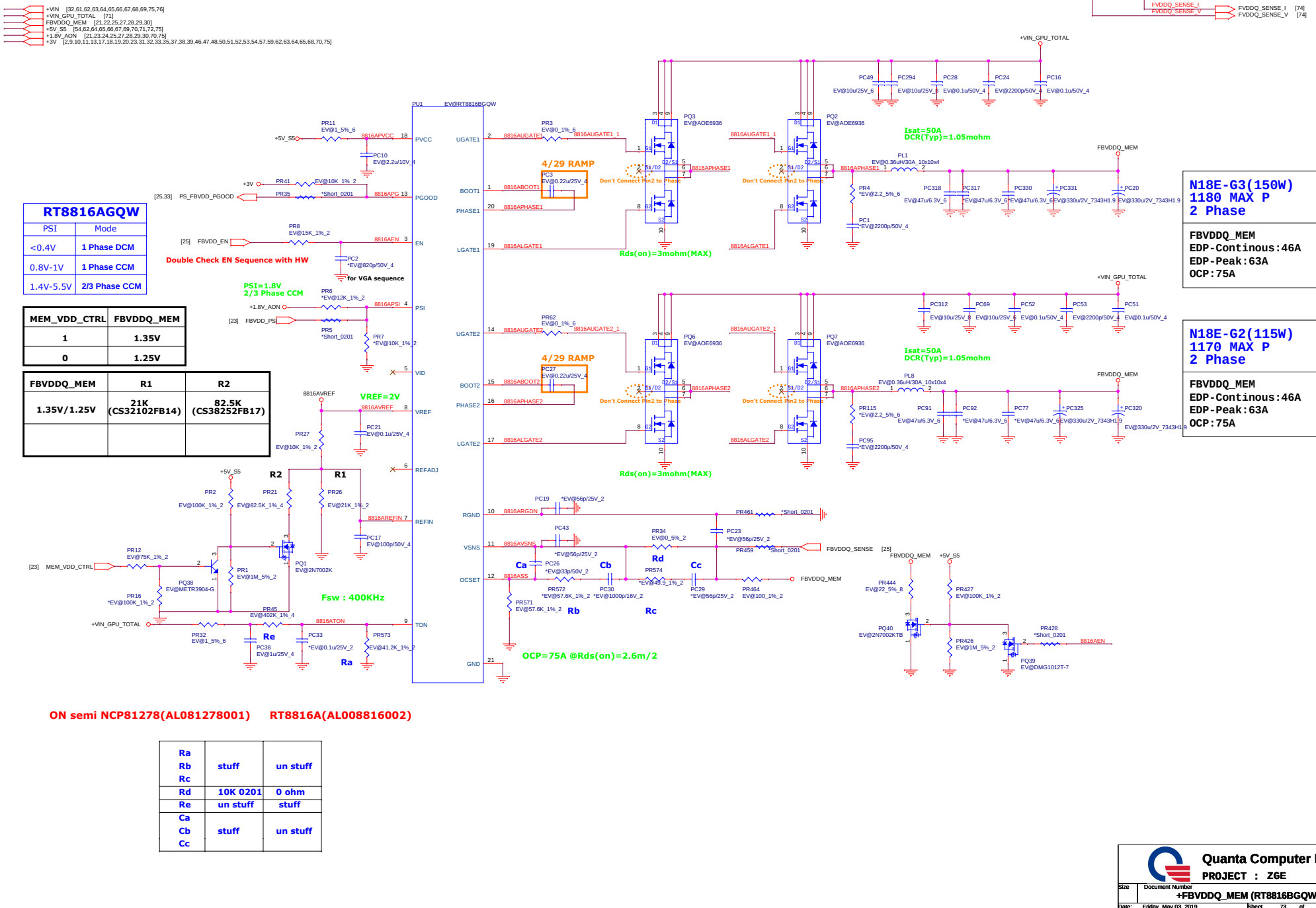
VGA Core - FBVDDQ_MEM



RT8816AGQW	
PSI	Mode
<0.4V	1 Phase DCM
0.8V-1V	1 Phase CCM
1.4V-5.5V	2/3 Phase CCM

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.35V
0	1.25V

FBVDDQ_MEM	R1	R2
1.35V/1.25V	21K (CS32102FB14)	82.5K (CS38252FB17)

N18E-G3(150W)
1180 MAX P
2 Phase

FBVDDQ_MEM
EDP-Continous:46A
EDP-Peak:63A
OCP:75A

N18E-G2(115W)
1170 MAX P
2 Phase

FBVDDQ_MEM
EDP-Continous:46A
EDP-Peak:63A
OCP:75A

ON semi NCP81278(AL081278001) **RT8816A(AL008816002)**

Ra Rb Rc	stuff	un stuff
Rd	10K 0201	0 ohm
Re	un stuff	stuff
Ca Cb Cc	stuff	un stuff

Quanta Computer Inc.
PROJECT : Z6E

Size	Document Number	Rev
	+FBVDDQ_MEM (RT8816BGQW)	1A
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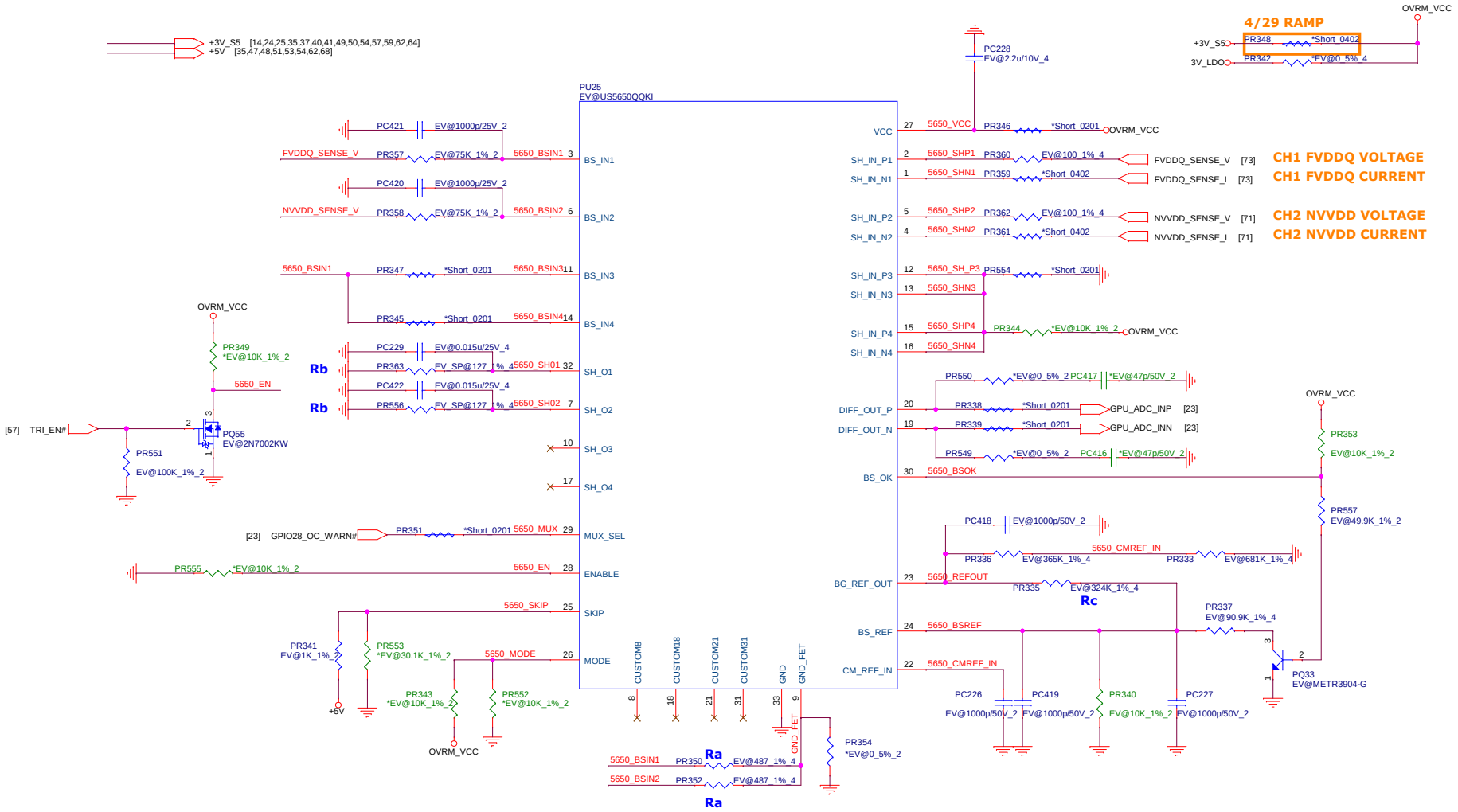
Power Monitoring with OVR-M



ON semi NCP45491 | **UPI US5650PQKI Default Setting**

	N18E-G2(1170) 115W		N18E-G3(1180) 150W		N18E-G2(1170) 115W		N18E-G3(1180) 150W	
Ra	PR350 PR352	649 Ohm	CS16492FB13	649 Ohm	CS16492FB13	PR350 PR352	487 Ohm	CS14872FB05	487 Ohm	CS14872FB05
Rb	PR363 PR556	191 Ohm	CS11912FB00	169 Ohm	CS11692FB09	PR363 PR556	143 Ohm	CS11432FB00	127 Ohm	CS11272FB21
Rc	PR335	243k Ohm	CS42432FB02	243k Ohm	CS42432FB02	PR335	324k Ohm	CS43242FB11	324k Ohm	CS43242FB11

Quanta Computer Inc.
PROJECT : ZGE
Size | Document Number: OVR-M (US5650PQKI) | Rev 1A
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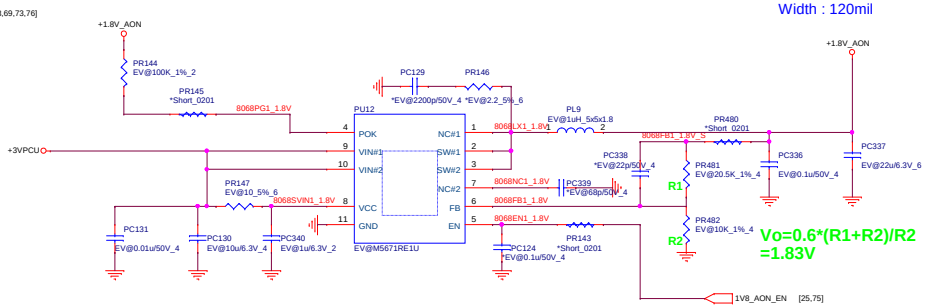
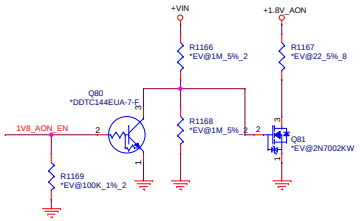
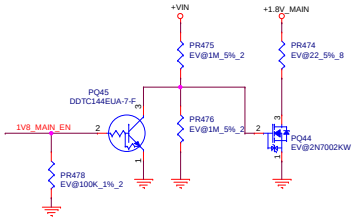
+3VPCU [9,10,12,14,16,32,37,39,40,47,54,57,59,61,62,68,70]
+1.8V_AON [21,23,24,25,27,28,29,30,70,73]
+1.8V_MAIN [21,23,25,35]
+5VPCU [46,58,59,62,63]
+VIN [32,61,62,63,64,65,66,67,68,69,73,76]

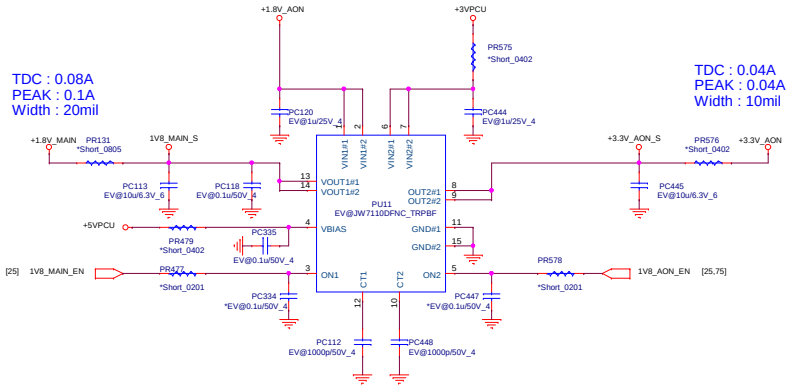
+1.8V_AON
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil





TDC : 0.08A
PEAK : 0.1A
Width : 20mil

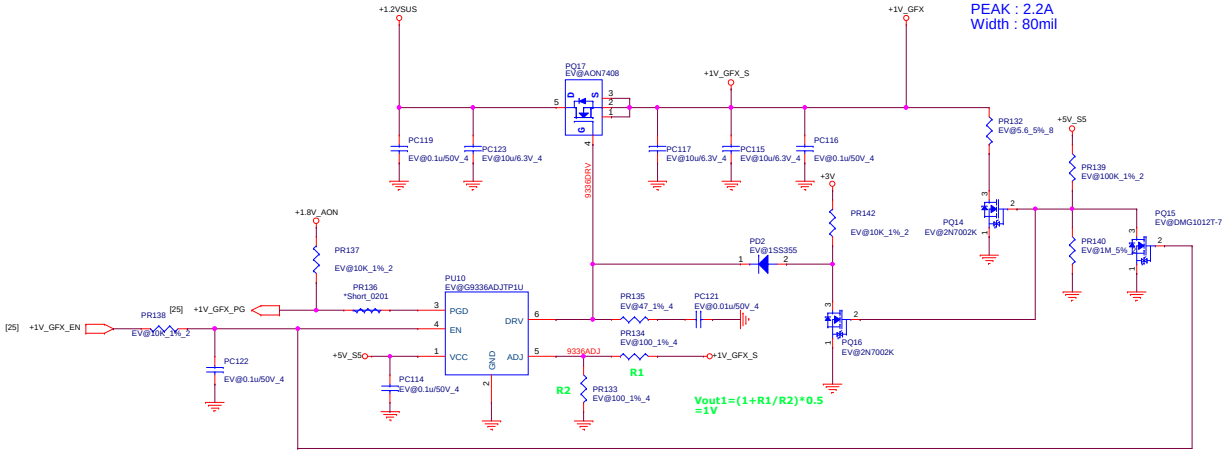




TDC : 0.04A
PEAK : 0.04A
Width : 10mil

+1.2VSUS [2,6,10,14,17,18,19,20,46,59,60,64]
+1V_GFX [21,23,24]
+5V_S5 [54,62,64,65,66,67,69,70,71,72,73]
+3V [2,9,10,11,13,17,18,19,20,23,31,32,33,35,37,38,39,46,47,48,50,51,52,53,54,57,59,62,63,64,65,68,70,73]

+1V_GFX
TDC : 1.65A
PEAK : 2.2A
Width : 80mil



Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	+1.8V_AON & +1.8V_MAIN & +1V_GFX	1A
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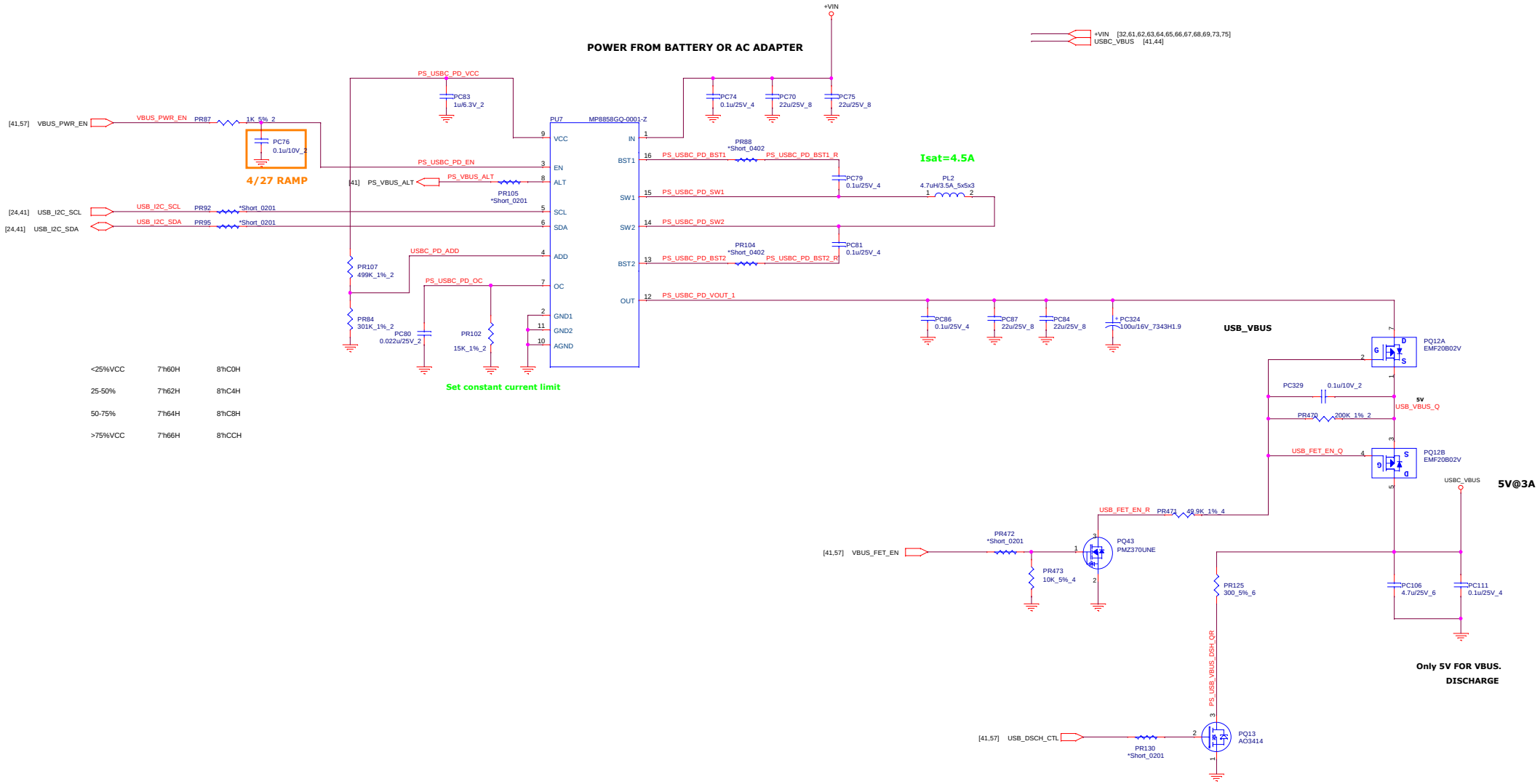
USB-C VBUS Buckboost

Adaptor : 19V
Battery : 12V (4S)



<25%VCC	7'h60H	8'hC0H
25-50%	7'h62H	8'hC4H
50-75%	7'h64H	8'hC8H
>75%VCC	7'h66H	8'hCCH

Quanta Computer Inc.
PROJECT : ZGE

Size	Document Number	Rev
	USB-C Buckboost (MP8858GQ)	1A
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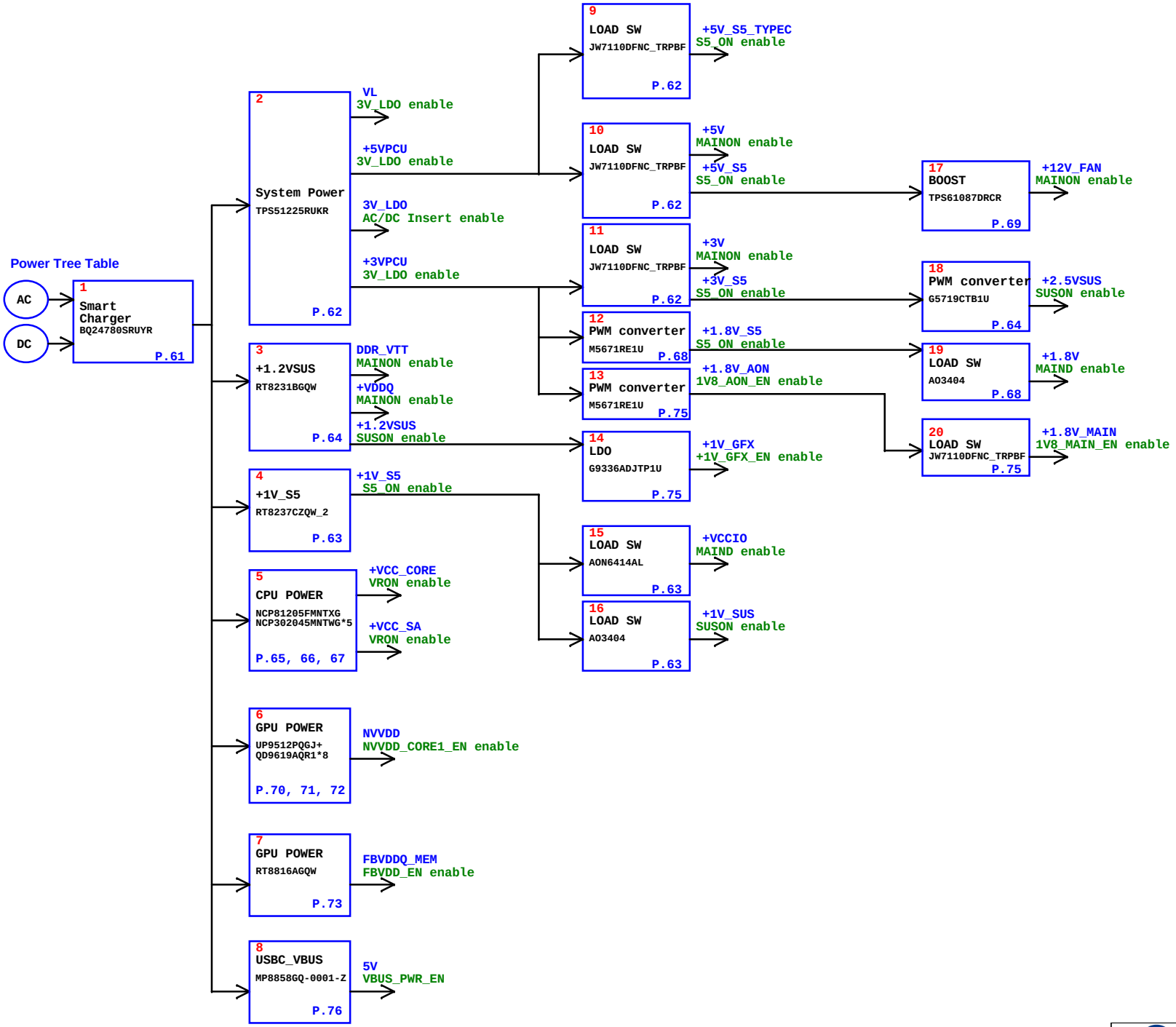
Power Tree Table



Quanta Computer Inc.
PROJECT : ZGE
POWER TREE TABLE
Size | Document Number | Rev 1A
Date: Friday, May 03, 2019 | Sheet 77 of 78