MODEL NAME : *PAP00*

PCB NO : *LA-6961P (DA**********)*

BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Huron River)

Sandy Bridge(BGA1023) + Cougar Point(SFF)

DISCRETE VGA N12P-GS(optimus)

2010-11-29

Rev: 0.4

Compal Electronics, Inc.			
Title: Cover Page			
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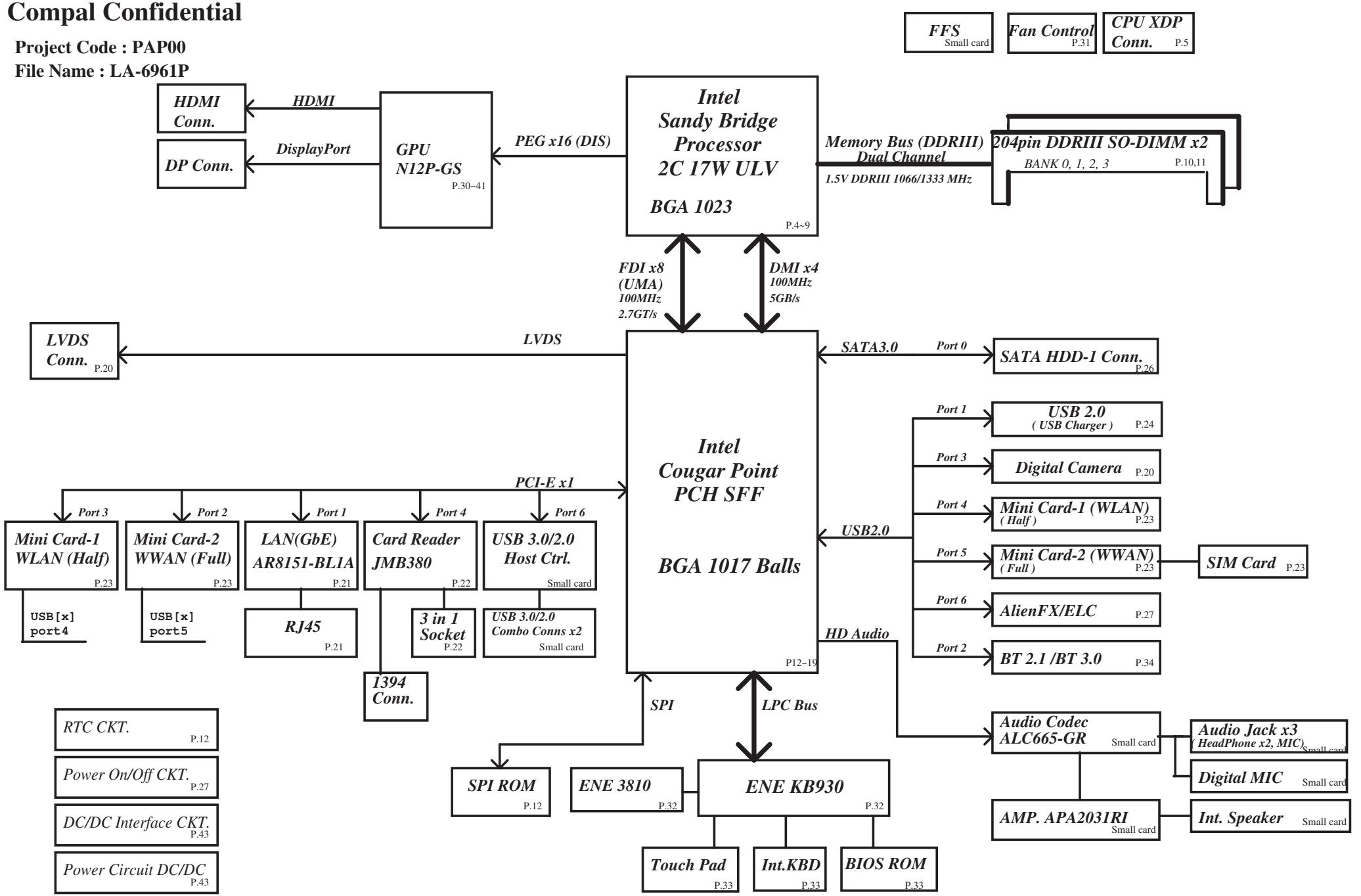
Project Code : PAP00
File Name : LA-6961P



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size	Document Number	Rev
B		0.4

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

Link

PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (Ext Left Side)
	2	Bluetooth
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN)
	6	ELC
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
	13	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Issued Date	2010/07/06	Deciphered Date	2011/07/06

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+1.05VS

RC2 24.9_0402_1%

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG_ICOMPI G3 — PEG_COMP
PEG_ICOMPO G1
PEG_RCOMPO G4

UCPU1A

DMI

14 DMI_CRX_PTX_N0	M2	DMI_RX#[0]
14 DMI_CRX_PTX_N1	P6	DMI_RX#[1]
14 DMI_CRX_PTX_N2	P1	DMI_RX#[2]
14 DMI_CRX_PTX_N3	P10	DMI_RX#[3]
14 DMI_CRX_PTX_P0	N3	DMI_RX[0]
14 DMI_CRX_PTX_P1	P7	DMI_RX[1]
14 DMI_CRX_PTX_P2	P3	DMI_RX[2]
14 DMI_CRX_PTX_P3	P11	DMI_RX[3]
14 DMI_CTX_PRX_N0	K1	DMI_TX#[0]
14 DMI_CTX_PRX_N1	M8	DMI_TX#[1]
14 DMI_CTX_PRX_N2	N4	DMI_TX#[2]
14 DMI_CTX_PRX_N3	R2	DMI_TX#[3]
14 DMI_CTX_PRX_P0	K3	DMI_TX[0]
14 DMI_CTX_PRX_P1	M7	DMI_TX[1]
14 DMI_CTX_PRX_P2	P4	DMI_TX[2]
14 DMI_CTX_PRX_P3	T3	DMI_TX[3]

Intel(R) FDI

14 FDI_CTX_PRX_N0	U7	FDI0_TX#[0]
14 FDI_CTX_PRX_N1	W11	FDI0_TX#[1]
14 FDI_CTX_PRX_N2	W1	FDI0_TX#[2]
14 FDI_CTX_PRX_N3	AA6	FDI0_TX#[3]
14 FDI_CTX_PRX_N4	W6	FDI1_TX#[0]
14 FDI_CTX_PRX_N5	V4	FDI1_TX#[1]
14 FDI_CTX_PRX_N6	Y2	FDI1_TX#[2]
14 FDI_CTX_PRX_N7	AC9	FDI1_TX#[3]
14 FDI_CTX_PRX_P0	U6	FDI0_TX[0]
14 FDI_CTX_PRX_P1	W10	FDI0_TX[1]
14 FDI_CTX_PRX_P2	W3	FDI0_TX[2]
14 FDI_CTX_PRX_P3	AA7	FDI0_TX[3]
14 FDI_CTX_PRX_P4	W7	FDI1_TX[0]
14 FDI_CTX_PRX_P5	T4	FDI1_TX[1]
14 FDI_CTX_PRX_P6	AA3	FDI1_TX[2]
14 FDI_CTX_PRX_P7	AC8	FDI1_TX[3]
14 FDI_FSYNC0	AA11	FDI0_FSYNC
14 FDI_FSYNC1	AC12	FDI1_FSYNC
14 FDI_INT	U11	FDI_INT
14 FDI_LSYNC0	AA10	FDI0_LSYNC
14 FDI_LSYNC1	AG8	FDI1_LSYNC

DP

+1.05VS — RC36 24.9_0402_1% — +EDP_COM — RC126 10K_0402_5%

AF3	eDP_COMPIO
AD2	eDP_ICOMPO
AG11	eDP_HPD
AG4	eDP_AUX#
AF4	eDP_AUX
AC3	eDP_TX#[0]
AC4	eDP_TX#[1]
AE11	eDP_TX#[2]
AE7	eDP_TX#[3]
AC1	eDP_TX[0]
AA4	eDP_TX[1]
AE10	eDP_TX[2]
AE6	eDP_TX[3]

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PCI EXPRESS -- GRAPHICS

PEG_RX#[0]	H22	PEG_GTX_C_HRX_N0	PEG_GTX_C_HRX_N0 30	
PEG_RX#[1]	J21	PEG_GTX_C_HRX_N1	PEG_GTX_C_HRX_N1 30	
PEG_RX#[2]	R22	PEG_GTX_C_HRX_N2	PEG_GTX_C_HRX_N2 30	
PEG_RX#[3]	D21	PEG_GTX_C_HRX_N3	PEG_GTX_C_HRX_N3 30	
PEG_RX#[4]	A19	PEG_GTX_C_HRX_N4	PEG_GTX_C_HRX_N4 30	
PEG_RX#[5]	D17	PEG_GTX_C_HRX_N5	PEG_GTX_C_HRX_N5 30	
PEG_RX#[6]	B14	PEG_GTX_C_HRX_N6	PEG_GTX_C_HRX_N6 30	
PEG_RX#[7]	D13	PEG_GTX_C_HRX_N7	PEG_GTX_C_HRX_N7 30	
PEG_RX#[8]	A11	PEG_GTX_C_HRX_N8	PEG_GTX_C_HRX_N8 30	
PEG_RX#[9]	B10	PEG_GTX_C_HRX_N9	PEG_GTX_C_HRX_N9 30	
PEG_RX#[10]	G8	PEG_GTX_C_HRX_N10	PEG_GTX_C_HRX_N10 30	
PEG_RX#[11]	A8	PEG_GTX_C_HRX_N11	PEG_GTX_C_HRX_N11 30	
PEG_RX#[12]	B6	PEG_GTX_C_HRX_N12	PEG_GTX_C_HRX_N12 30	
PEG_RX#[13]	H8	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N13 30	
PEG_RX#[14]	F5	PEG_GTX_C_HRX_N14	PEG_GTX_C_HRX_N14 30	
PEG_RX#[15]	K7	PEG_GTX_C_HRX_N15	PEG_GTX_C_HRX_N15 30	
PEG_RX[0]	K22	PEG_GTX_C_HRX_P0	PEG_GTX_C_HRX_P0 30	
PEG_RX[1]	K19	PEG_GTX_C_HRX_P1	PEG_GTX_C_HRX_P1 30	
PEG_RX[2]	C21	PEG_GTX_C_HRX_P2	PEG_GTX_C_HRX_P2 30	
PEG_RX[3]	D19	PEG_GTX_C_HRX_P3	PEG_GTX_C_HRX_P3 30	
PEG_RX[4]	C19	PEG_GTX_C_HRX_P4	PEG_GTX_C_HRX_P4 30	
PEG_RX[5]	D16	PEG_GTX_C_HRX_P5	PEG_GTX_C_HRX_P5 30	
PEG_RX[6]	C13	PEG_GTX_C_HRX_P6	PEG_GTX_C_HRX_P6 30	
PEG_RX[7]	D12	PEG_GTX_C_HRX_P7	PEG_GTX_C_HRX_P7 30	
PEG_RX[8]	C11	PEG_GTX_C_HRX_P8	PEG_GTX_C_HRX_P8 30	
PEG_RX[9]	C9	PEG_GTX_C_HRX_P9	PEG_GTX_C_HRX_P9 30	
PEG_RX[10]	F8	PEG_GTX_C_HRX_P10	PEG_GTX_C_HRX_P10 30	
PEG_RX[11]	C8	PEG_GTX_C_HRX_P11	PEG_GTX_C_HRX_P11 30	
PEG_RX[12]	C5	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P12 30	
PEG_RX[13]	H6	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P13 30	
PEG_RX[14]	F6	PEG_GTX_C_HRX_P14	PEG_GTX_C_HRX_P14 30	
PEG_RX[15]	K6	PEG_GTX_C_HRX_P15	PEG_GTX_C_HRX_P15 30	

PEG_TX[0]	G22	PEG_HTX_GRX_N0	CC185 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N0 30	
PEG_TX[1]	C23	PEG_HTX_GRX_N1	CC186 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N1 30	
PEG_TX[2]	D23	PEG_HTX_GRX_N2	CC187 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N2 30	
PEG_TX[3]	F21	PEG_HTX_GRX_N3	CC188 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N3 30	
PEG_TX[4]	H19	PEG_HTX_GRX_N4	CC189 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N4 30	
PEG_TX[5]	C17	PEG_HTX_GRX_N5	CC190 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N5 30	
PEG_TX[6]	K15	PEG_HTX_GRX_N6	CC191 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N6 30	
PEG_TX[7]	F17	PEG_HTX_GRX_N7	CC192 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N7 30	
PEG_TX[8]	F14	PEG_HTX_GRX_N8	CC193 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N8 30	
PEG_TX[9]	A15	PEG_HTX_GRX_N9	CC194 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N9 30	
PEG_TX[10]	J14	PEG_HTX_GRX_N10	CC195 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N10 30	
PEG_TX[11]	H13	PEG_HTX_GRX_N11	CC196 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N11 30	
PEG_TX[12]	M10	PEG_HTX_GRX_N12	CC197 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N12 30	
PEG_TX[13]	F10	PEG_HTX_GRX_N13	CC198 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N13 30	
PEG_TX[14]	D9	PEG_HTX_GRX_N14	CC199 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N14 30	
PEG_TX[15]	J4	PEG_HTX_GRX_N15	CC200 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_N15 30	
PEG_TX[0]	F22	PEG_HTX_GRX_P0	CC201 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P0 30	
PEG_TX[1]	A23	PEG_HTX_GRX_P1	CC202 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P1 30	
PEG_TX[2]	D24	PEG_HTX_GRX_P2	CC203 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P2 30	
PEG_TX[3]	F21	PEG_HTX_GRX_P3	CC204 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P3 30	
PEG_TX[4]	G19	PEG_HTX_GRX_P4	CC205 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P4 30	
PEG_TX[5]	B18	PEG_HTX_GRX_P5	CC206 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P5 30	
PEG_TX[6]	K17	PEG_HTX_GRX_P6	CC207 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P6 30	
PEG_TX[7]	G17	PEG_HTX_GRX_P7	CC208 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P7 30	
PEG_TX[8]	F14	PEG_HTX_GRX_P8	CC209 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P8 30	
PEG_TX[9]	C15	PEG_HTX_GRX_P9	CC210 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P9 30	
PEG_TX[10]	K13	PEG_HTX_GRX_P10	CC211 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P10 30	
PEG_TX[11]	G13	PEG_HTX_GRX_P11	CC212 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P11 30	
PEG_TX[12]	K10	PEG_HTX_GRX_P12	CC213 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P12 30	
PEG_TX[13]	G10	PEG_HTX_GRX_P13	CC214 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P13 30	
PEG_TX[14]	D8	PEG_HTX_GRX_P14	CC215 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P14 30	
PEG_TX[15]	K4	PEG_HTX_GRX_P15	CC216 1	2 0.1U_0402_10V7K~D	PEG_HTX_C_GRX_P15 30	

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

UCPU1I

VSS

RG17	VSS[181]	VSS[251]	M4
RG21	VSS[182]	VSS[252]	M58
RG24	VSS[183]	VSS[253]	M6
RG28	VSS[184]	VSS[254]	N1
RG37	VSS[185]	VSS[255]	N17
RG41	VSS[186]	VSS[256]	N21
RG45	VSS[187]	VSS[257]	N25
RG49	VSS[188]	VSS[258]	N28
RG53	VSS[189]	VSS[259]	N33
BG9	VSS[190]	VSS[260]	N36
C29	VSS[191]	VSS[261]	N40
C35	VSS[192]	VSS[262]	N43
C40	VSS[193]	VSS[263]	N47
D10	VSS[194]	VSS[264]	N48
D14	VSS[195]	VSS[265]	N51
D18	VSS[196]	VSS[266]	N52
D22	VSS[197]	VSS[267]	N56
D26	VSS[198]	VSS[268]	N61
D29	VSS[199]	VSS[269]	P14
D35	VSS[200]	VSS[270]	P16
D4	VSS[201]	VSS[271]	P18
D40	VSS[202]	VSS[272]	P21
D43	VSS[203]	VSS[273]	P58
D46	VSS[204]	VSS[274]	P59
D50	VSS[205]	VSS[275]	P9
D54	VSS[206]	VSS[276]	R17
D58	VSS[207]	VSS[277]	R20
D6	VSS[208]	VSS[278]	R4
E25	VSS[209]	VSS[279]	R46
E29	VSS[210]	VSS[280]	T1
E3	VSS[211]	VSS[281]	T47
E35	VSS[212]	VSS[282]	T50
E40	VSS[213]	VSS[283]	T51
F13	VSS[214]	VSS[284]	T52
F15	VSS[215]	VSS[285]	T53
F19	VSS[216]	VSS[286]	T55
F29	VSS[217]	VSS[287]	T56
F35	VSS[218]	VSS[288]	U13
F40	VSS[219]	VSS[289]	U8
F55	VSS[220]	VSS[290]	V20
G48	VSS[221]	VSS[291]	V61
G51	VSS[222]	VSS[292]	W13
G6	VSS[223]	VSS[293]	W15
G61	VSS[224]	VSS[294]	W18
H10	VSS[225]	VSS[295]	W21
H14	VSS[226]	VSS[296]	W46
H17	VSS[227]	VSS[297]	W8
H21	VSS[228]	VSS[298]	Y4
H4	VSS[229]	VSS[299]	Y47
H53	VSS[230]	VSS[300]	Y58
H58	VSS[231]	VSS[301]	Y59
J1	VSS[232]		
J49	VSS[233]		
J55	VSS[234]		
K11	VSS[235]		
K21	VSS[236]		
K51	VSS[237]	VSS_NCTF_1	A5
K8	VSS[238]	VSS_NCTF_2	A57
L16	VSS[239]	VSS_NCTF_3	BC61
L20	VSS[240]	VSS_NCTF_4	BD3
L22	VSS[241]	VSS_NCTF_5	BD59
L26	VSS[242]	VSS_NCTF_6	BE4
L30	VSS[243]	VSS_NCTF_7	BE58
L34	VSS[244]	VSS_NCTF_8	BG5
L38	VSS[245]	VSS_NCTF_9	BG57
L43	VSS[246]	VSS_NCTF_10	C3
L48	VSS[247]	VSS_NCTF_11	C58
L61	VSS[248]	VSS_NCTF_12	D59
M11	VSS[249]	VSS_NCTF_13	F1
M15	VSS[250]	VSS_NCTF_14	F61

NCTF

SANDY-BRIDGE_BGA1023~D

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Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

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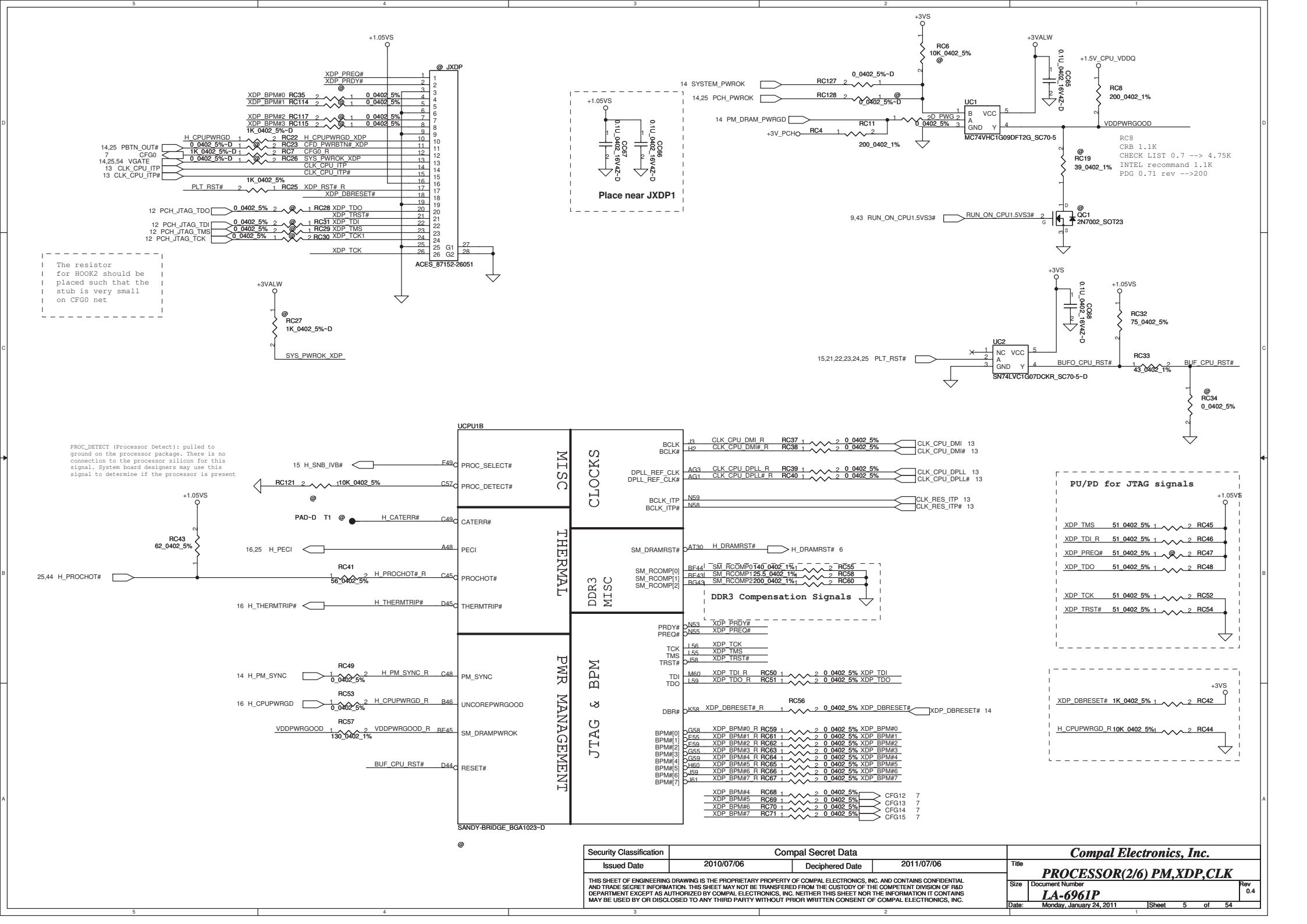

Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	PROCESSOR(2/6) PM,XDP,CLK
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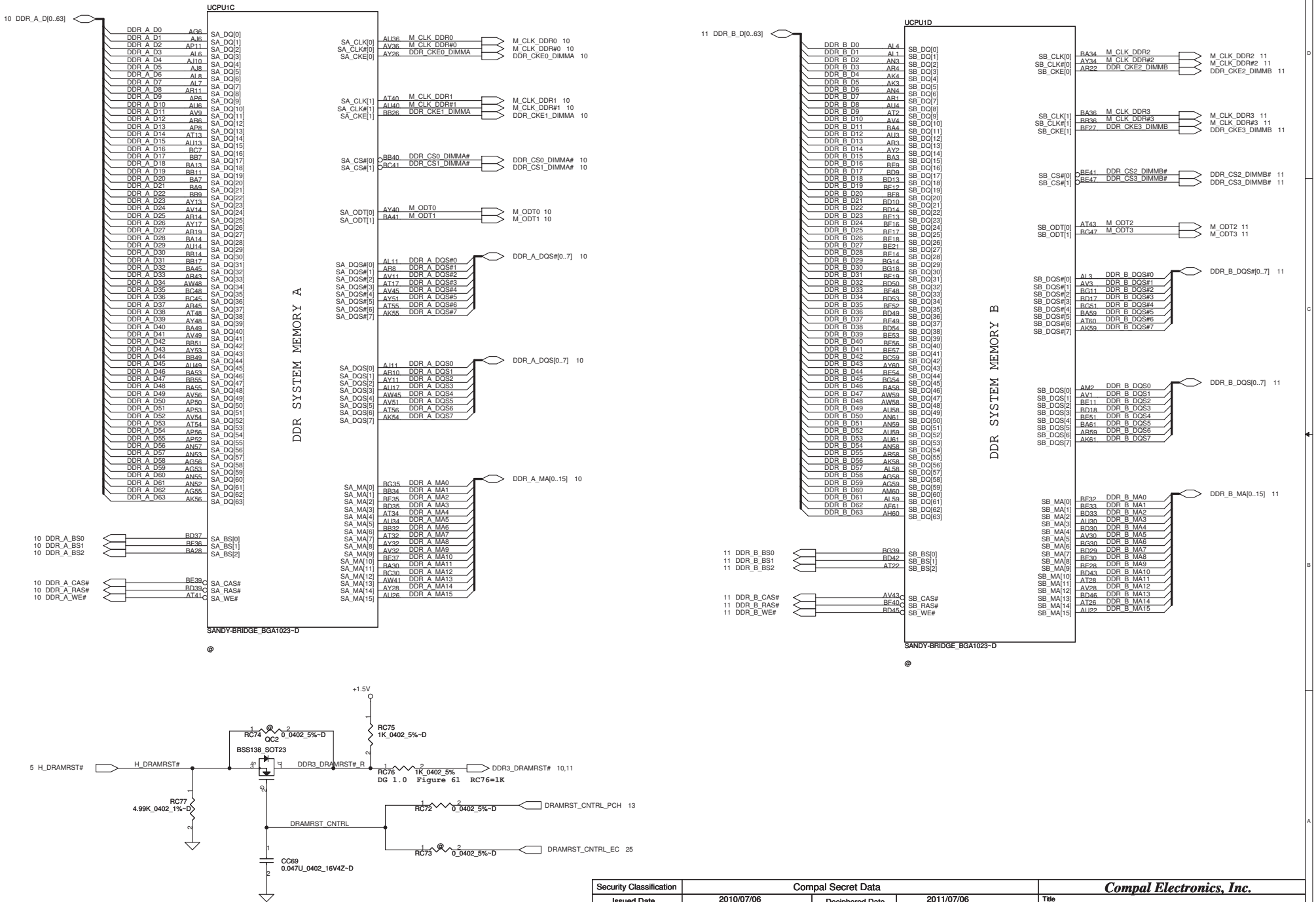

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Compal Electronics, Inc.

Title: PROCESSOR(3/6) DDRIII

Size	Document Number	Rev
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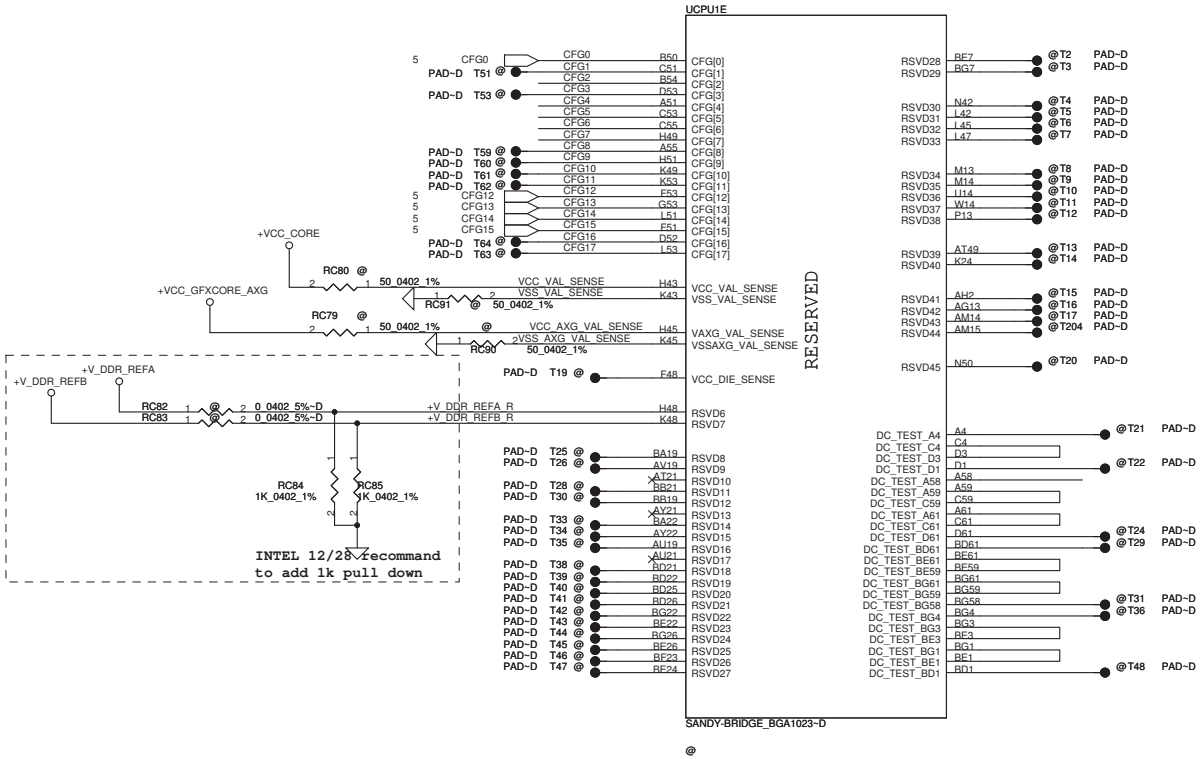
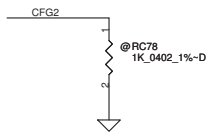
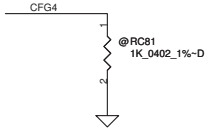


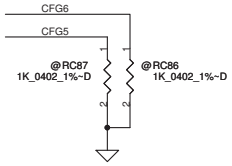
CFG Straps for Processor



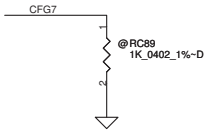
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	*1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



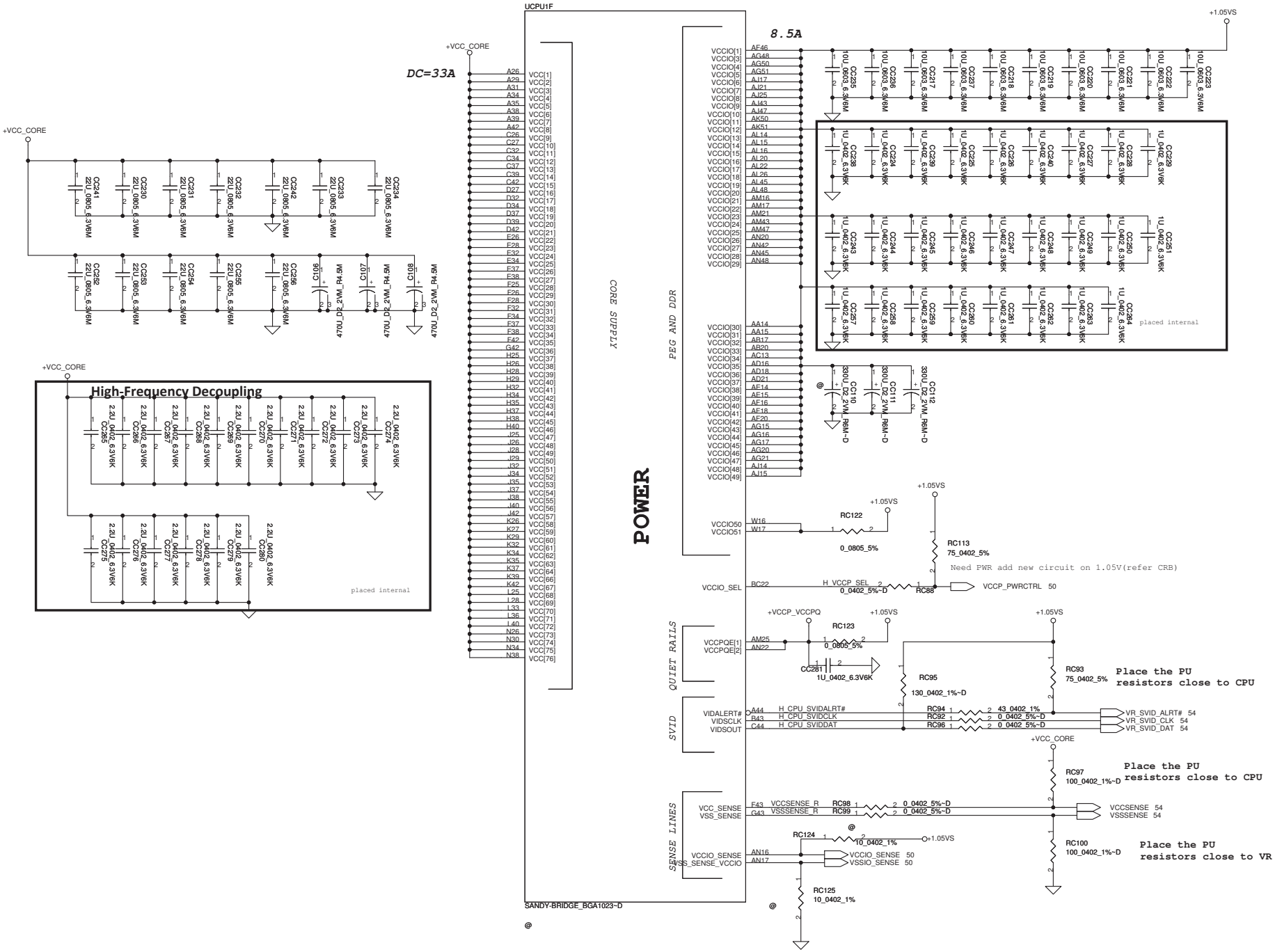
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.			
Title	PROCESSOR(4/6) RSVD,CFG		
Size	Document Number		Rev
	LA-6961P		0.4
Date:	Monday, January 24, 2011	Sheet	7 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	PROCESSOR(5/6) PWR,BYPASS
Size	Document Number: LA-6961P
Rev	0.4
Date:	Monday, January 24, 2011
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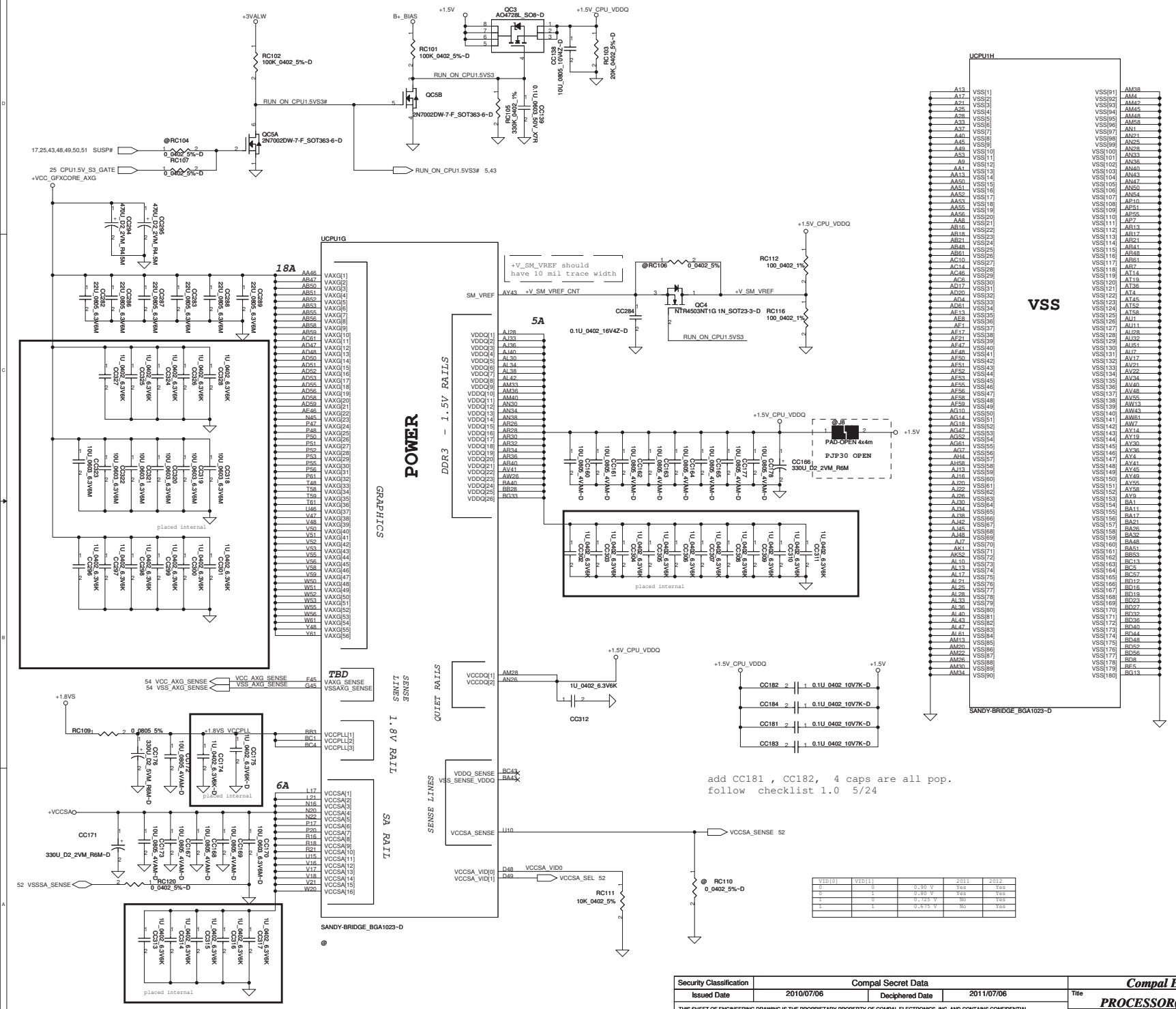
+1.5V_CPU_VDDQ Source



VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

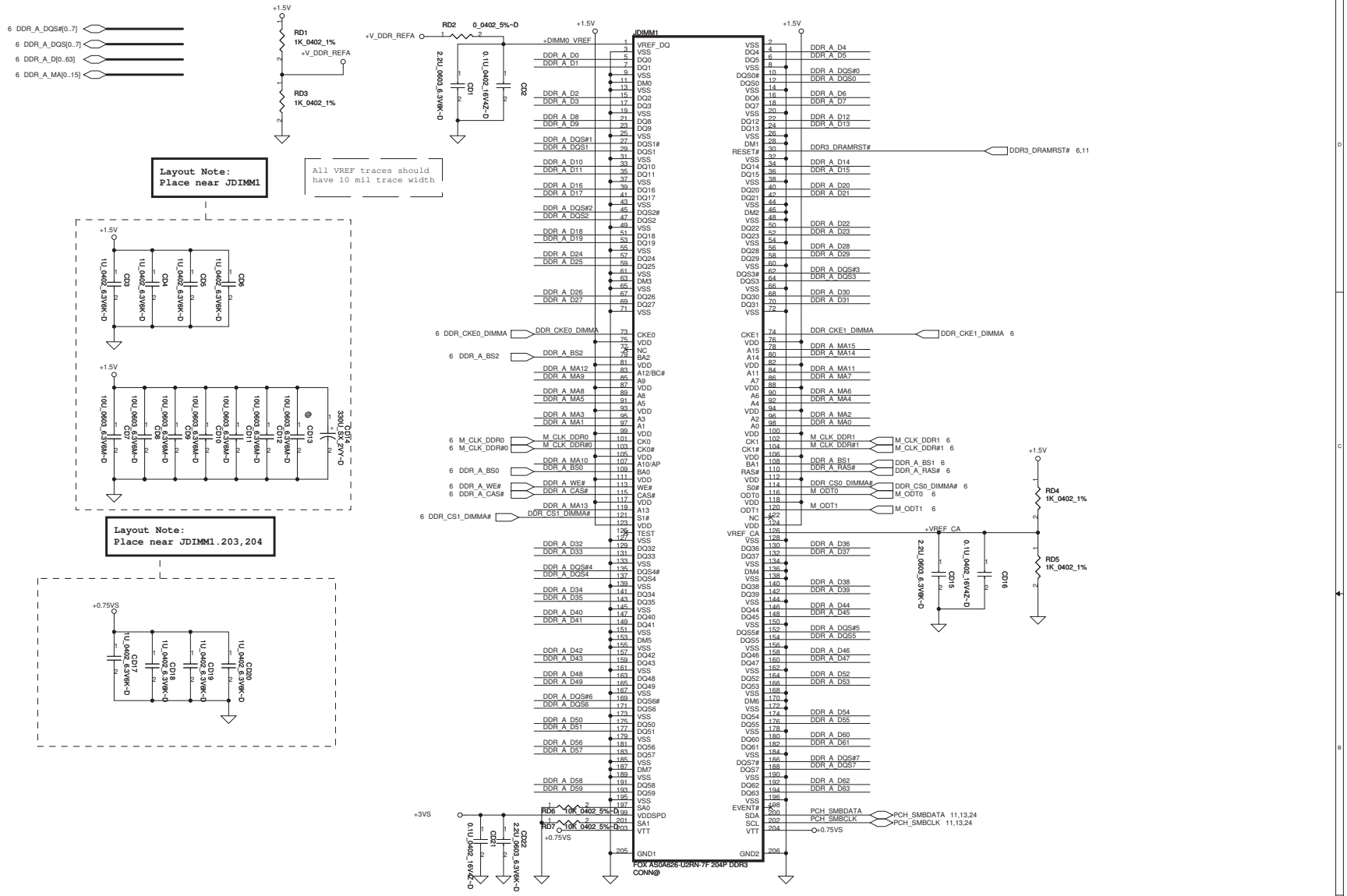
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: PROCESSOR(6/6) PWR,VSS

Size: | Document Number: LA-6961P | Rev: 0.4

Date: Monday, January 24, 2011 | Sheet 9 of 54



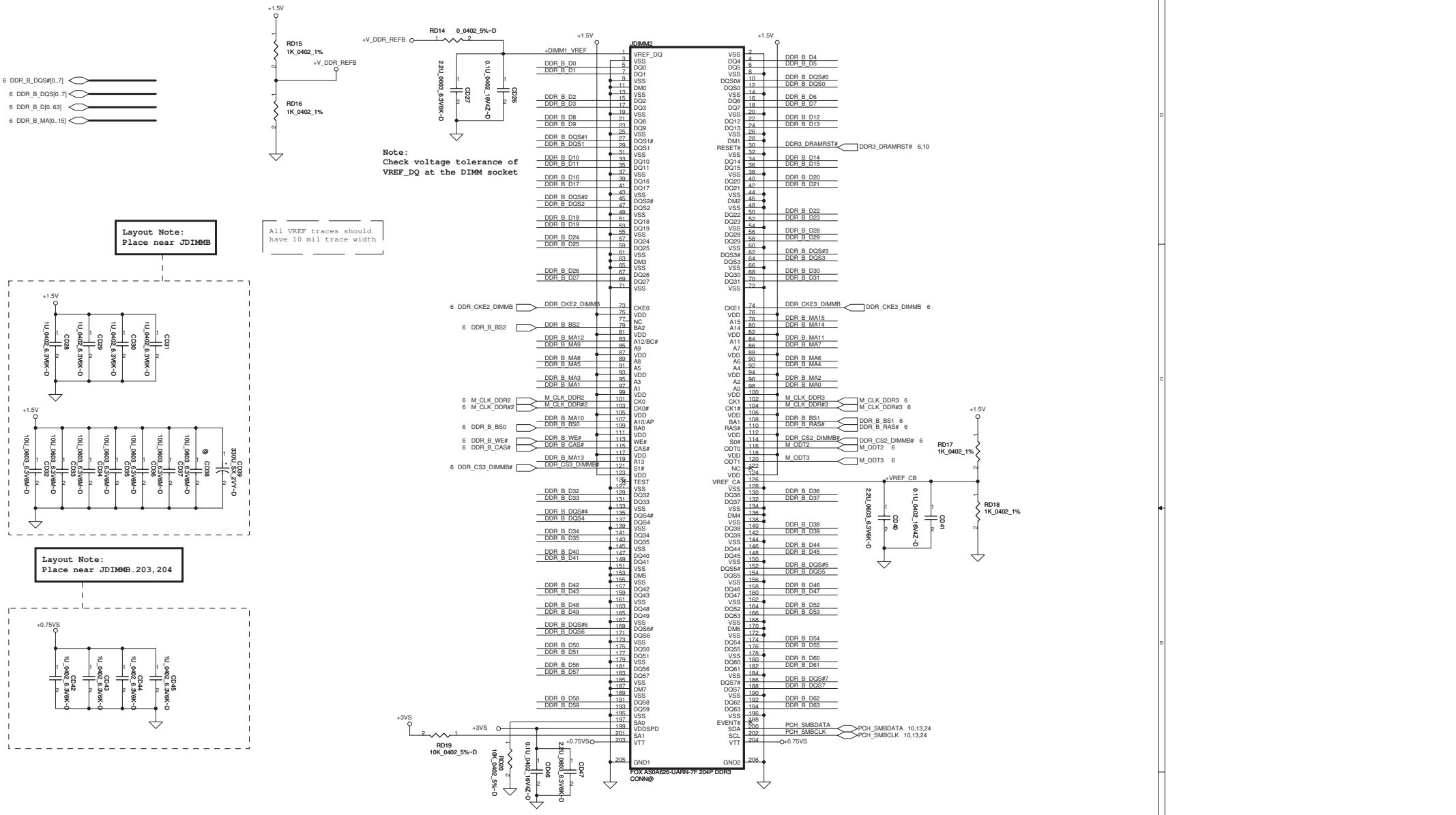
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: DDRIII DIMMA

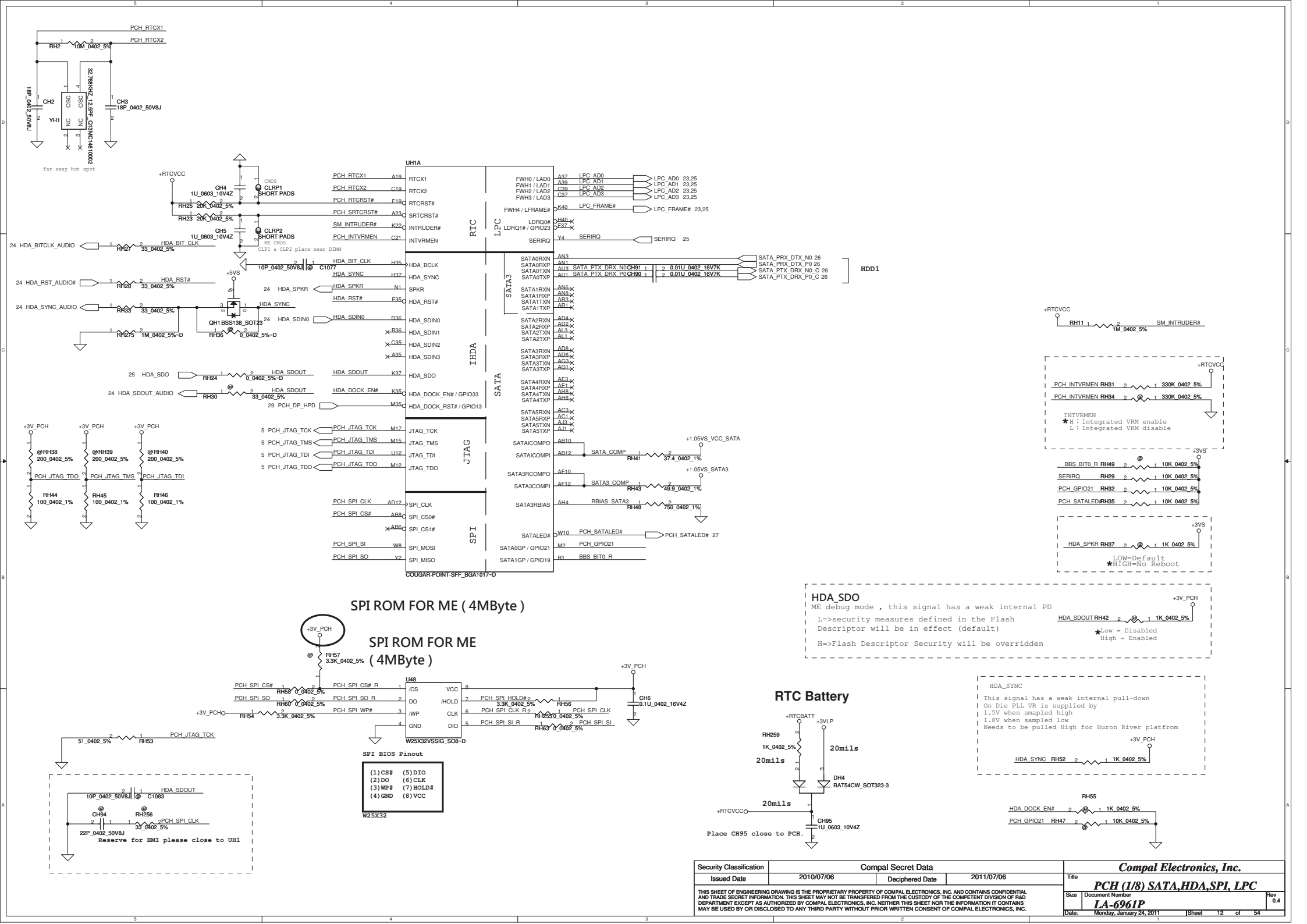
Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 Sheet 10 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	DDRIII DIMMB
Size	Document Number: LA-6961P
Rev	0.4
Date:	Monday, January 24, 2011
Sheet	11 of 54



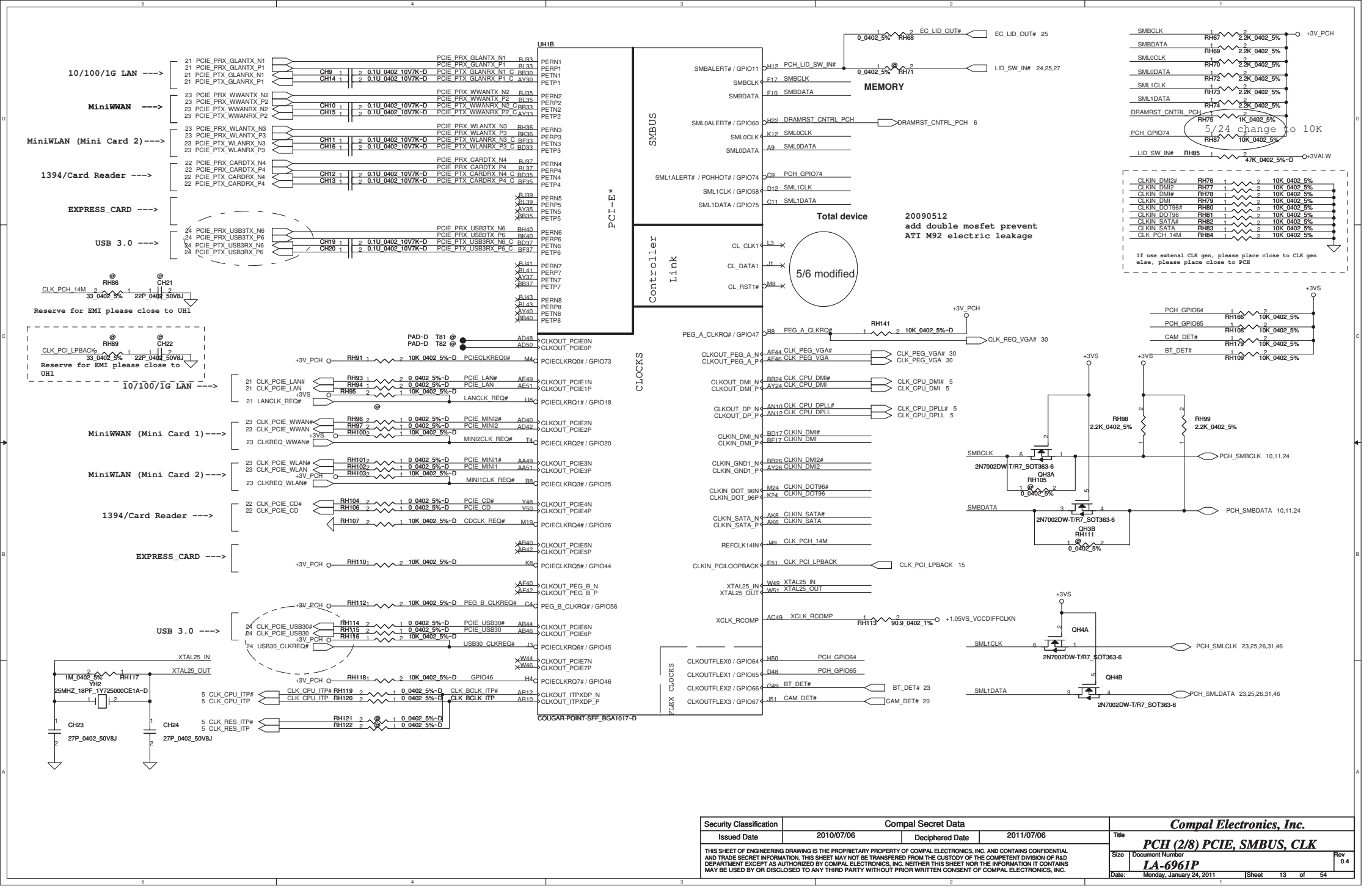
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **PCH (1/8) SATA,HDA,SPI, LPC**

Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 Sheet 12 of 54



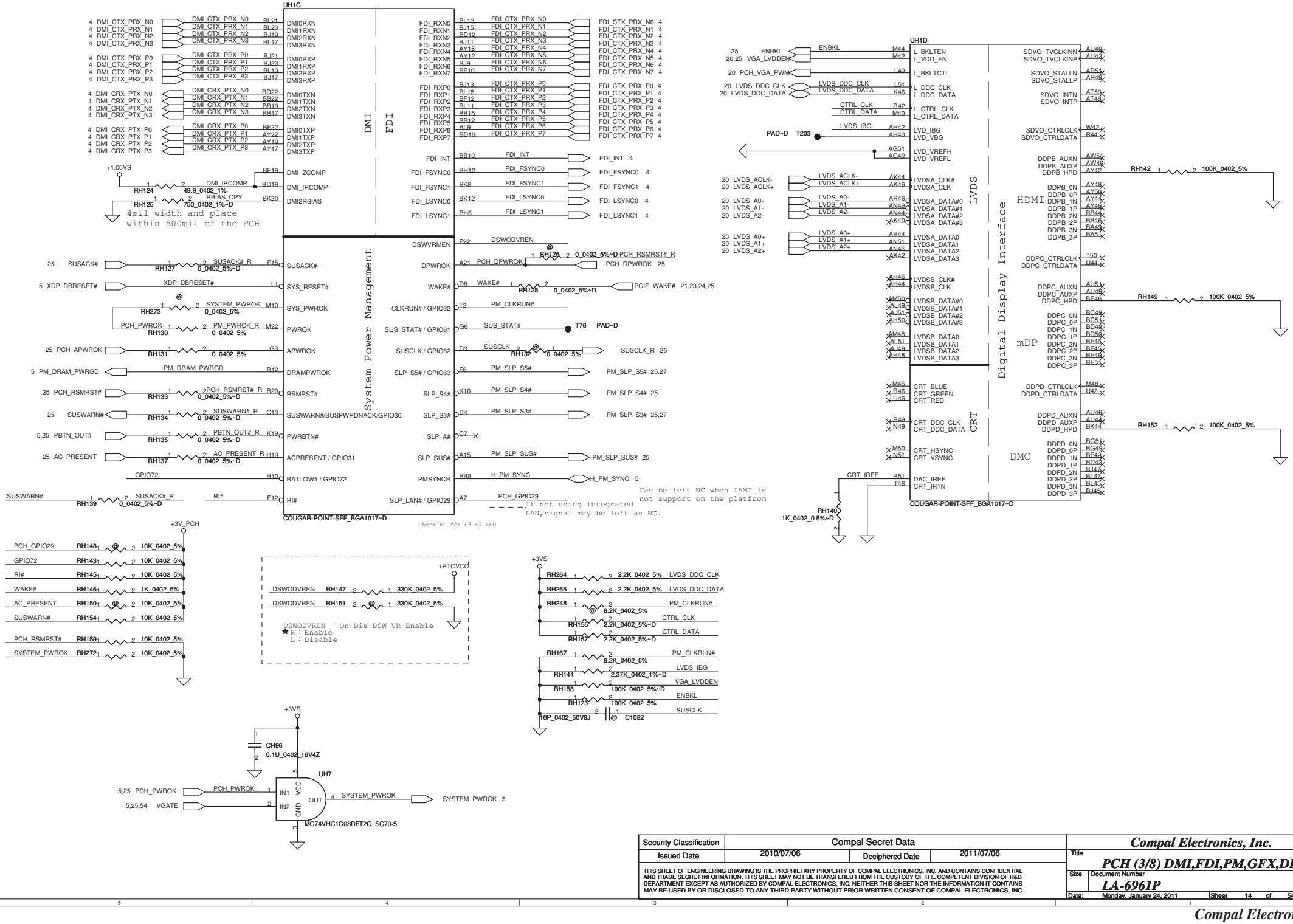
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 | Sheet 13 of 54



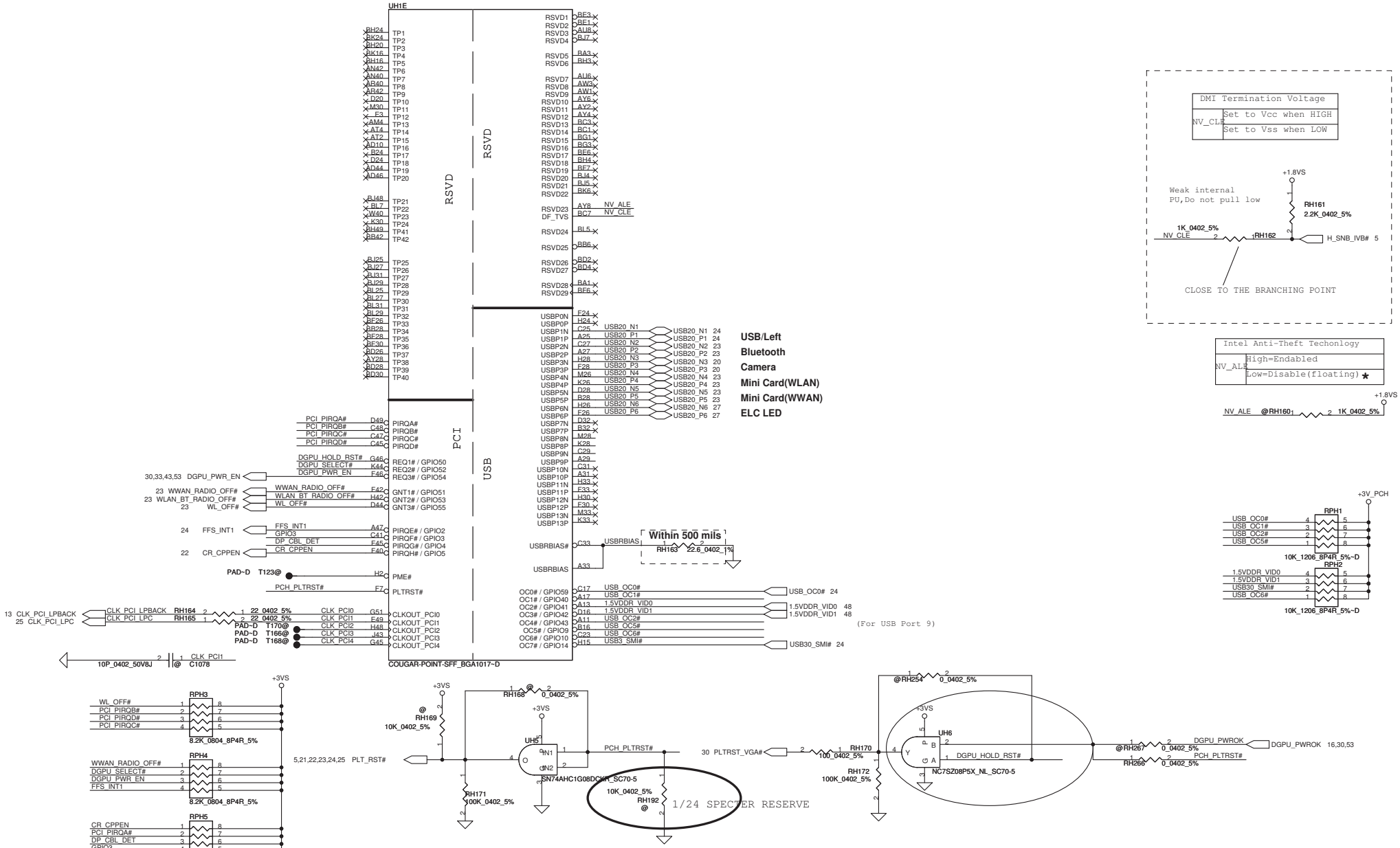
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 | Sheet 14 of 54



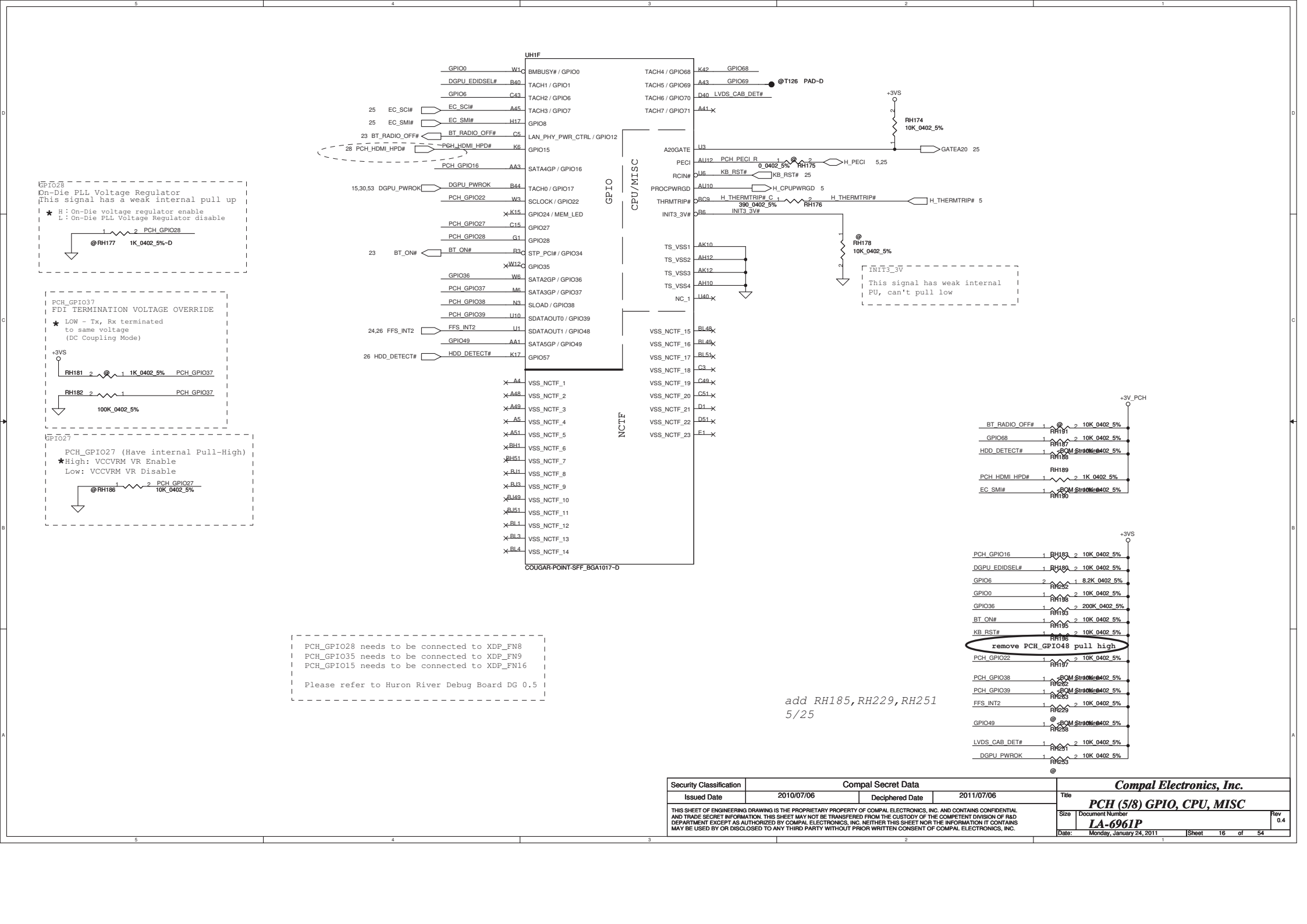
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

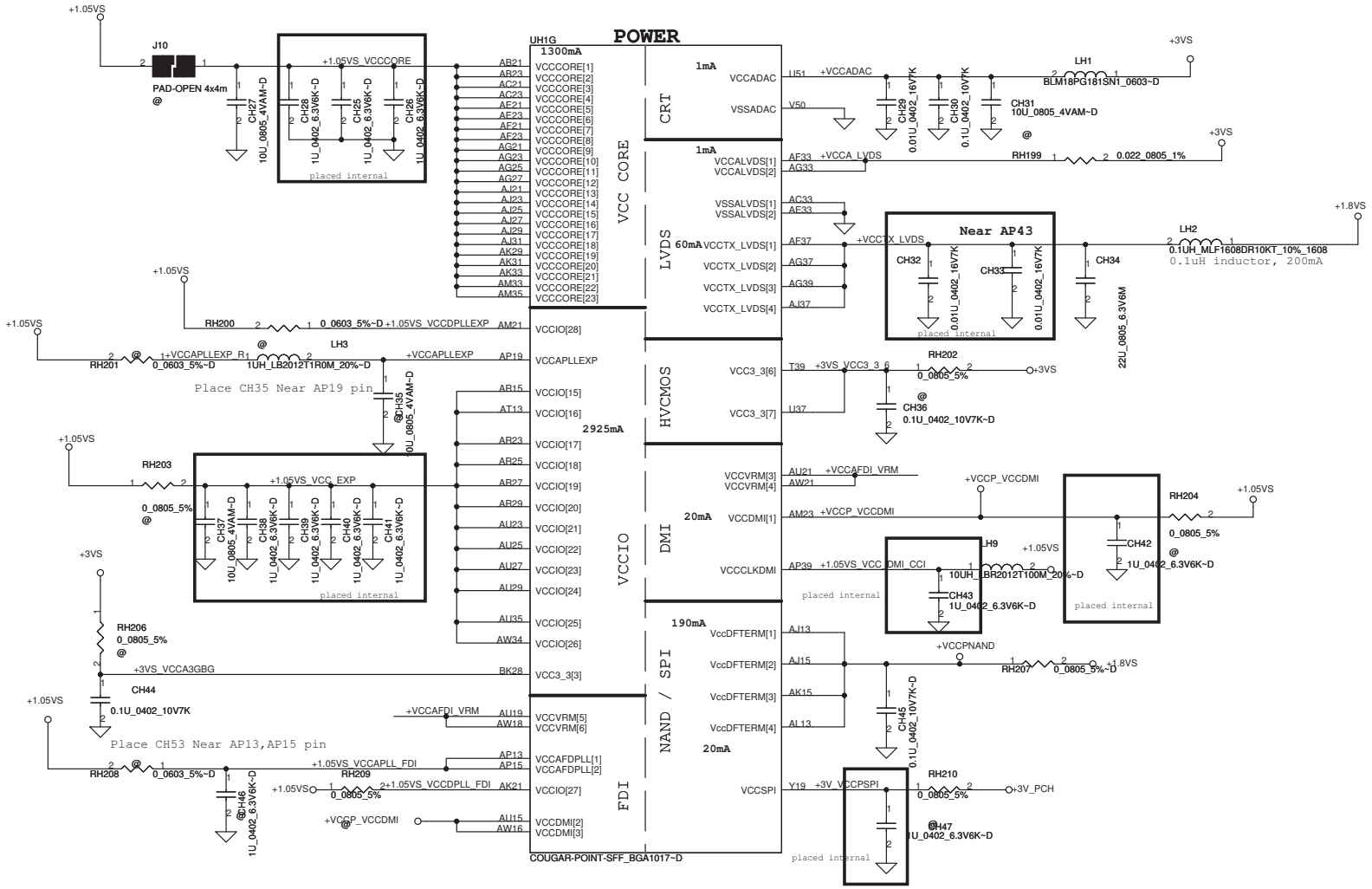
Size	Document Number	Rev
	LA-6961P	0.4

Date: Tuesday, January 25, 2011 | Sheet 15 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.			
Title	PCH (5/8) GPIO, CPU, MISC		
Size	Document Number LA-6961P		Rev 0.4
Date: Monday, January 24, 2011	Sheet 16 of 54		



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

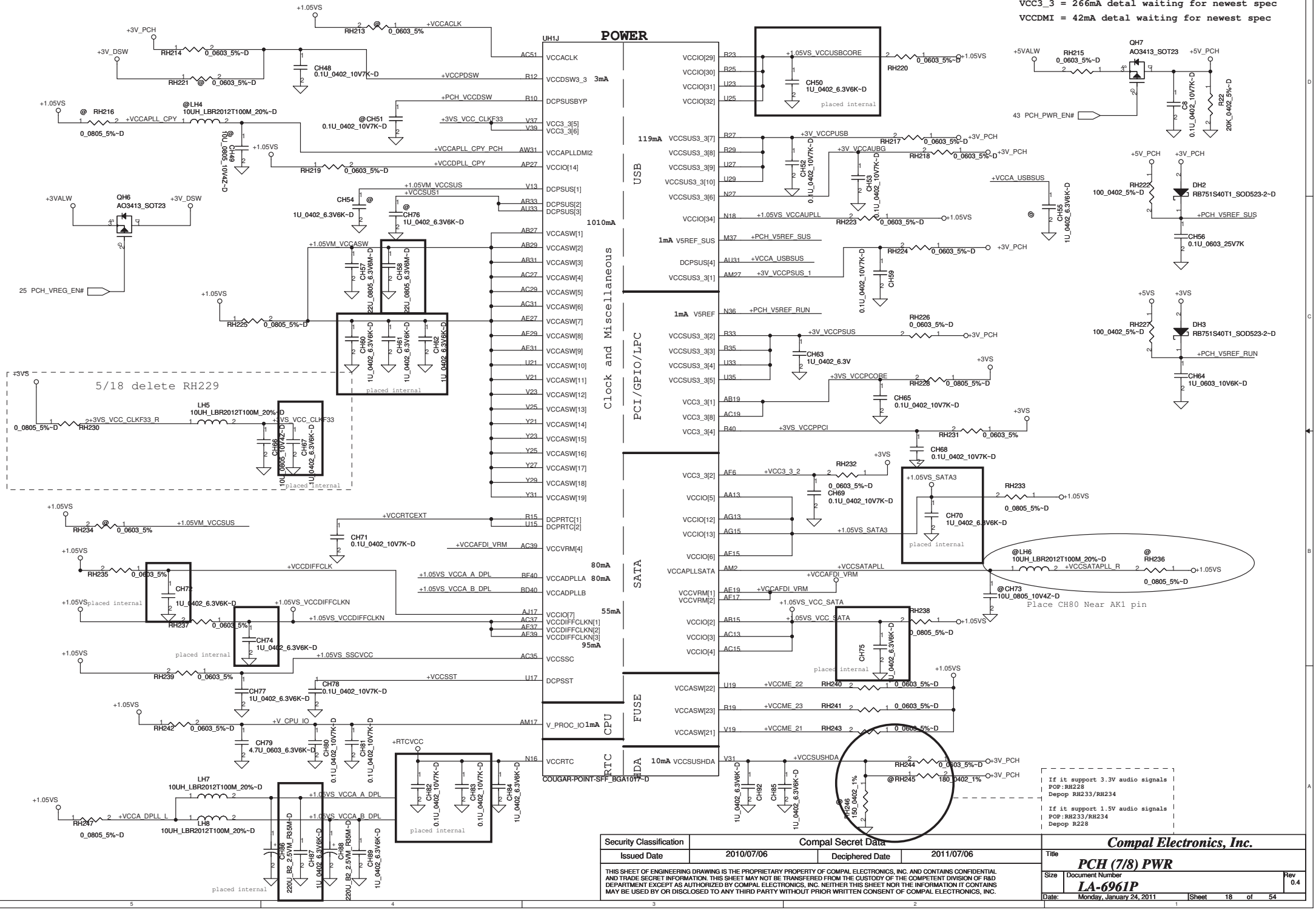
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size | Document Number: LA-6961P | Rev: 0.4

Date: Monday, January 24, 2011 | Sheet 17 of 54



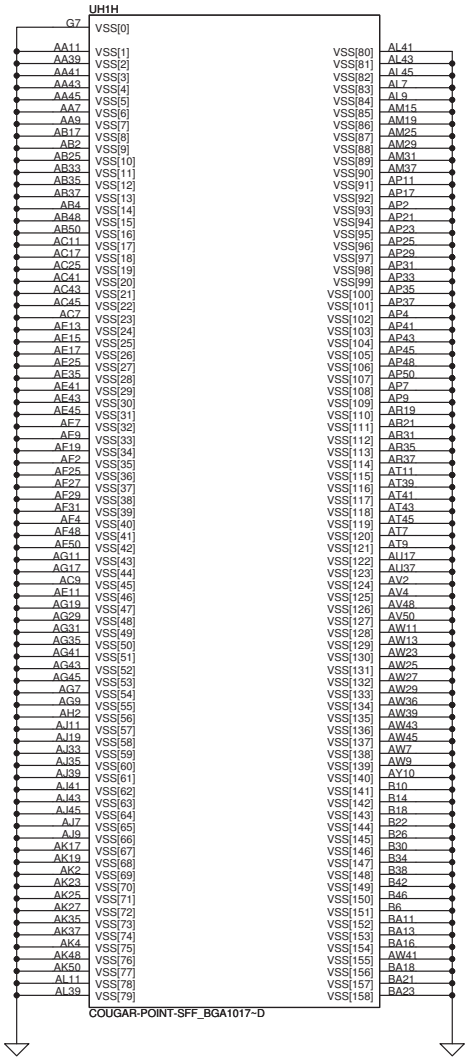
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

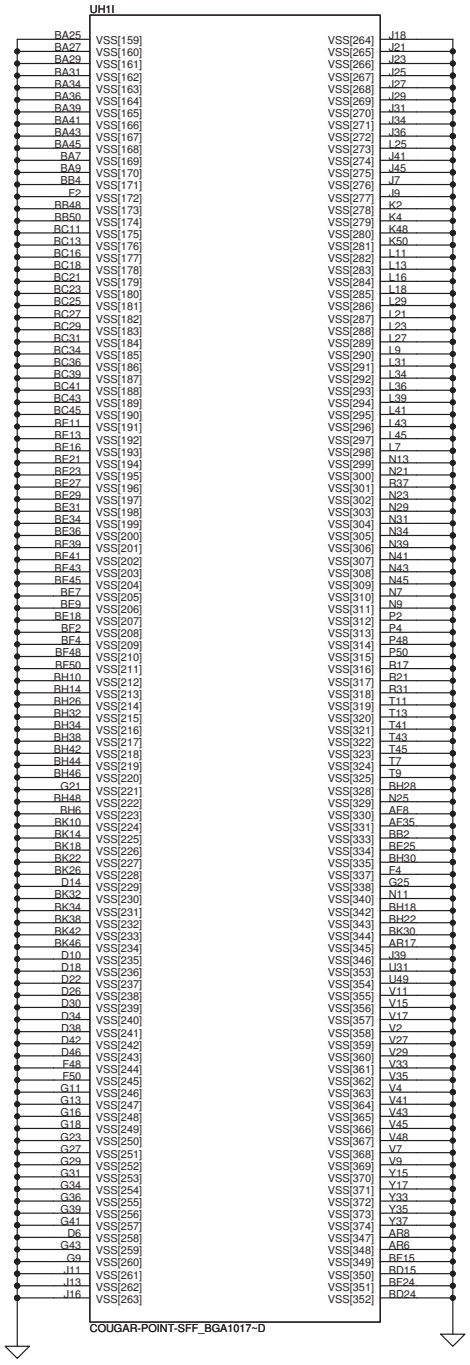
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 | Sheet 18 of 54





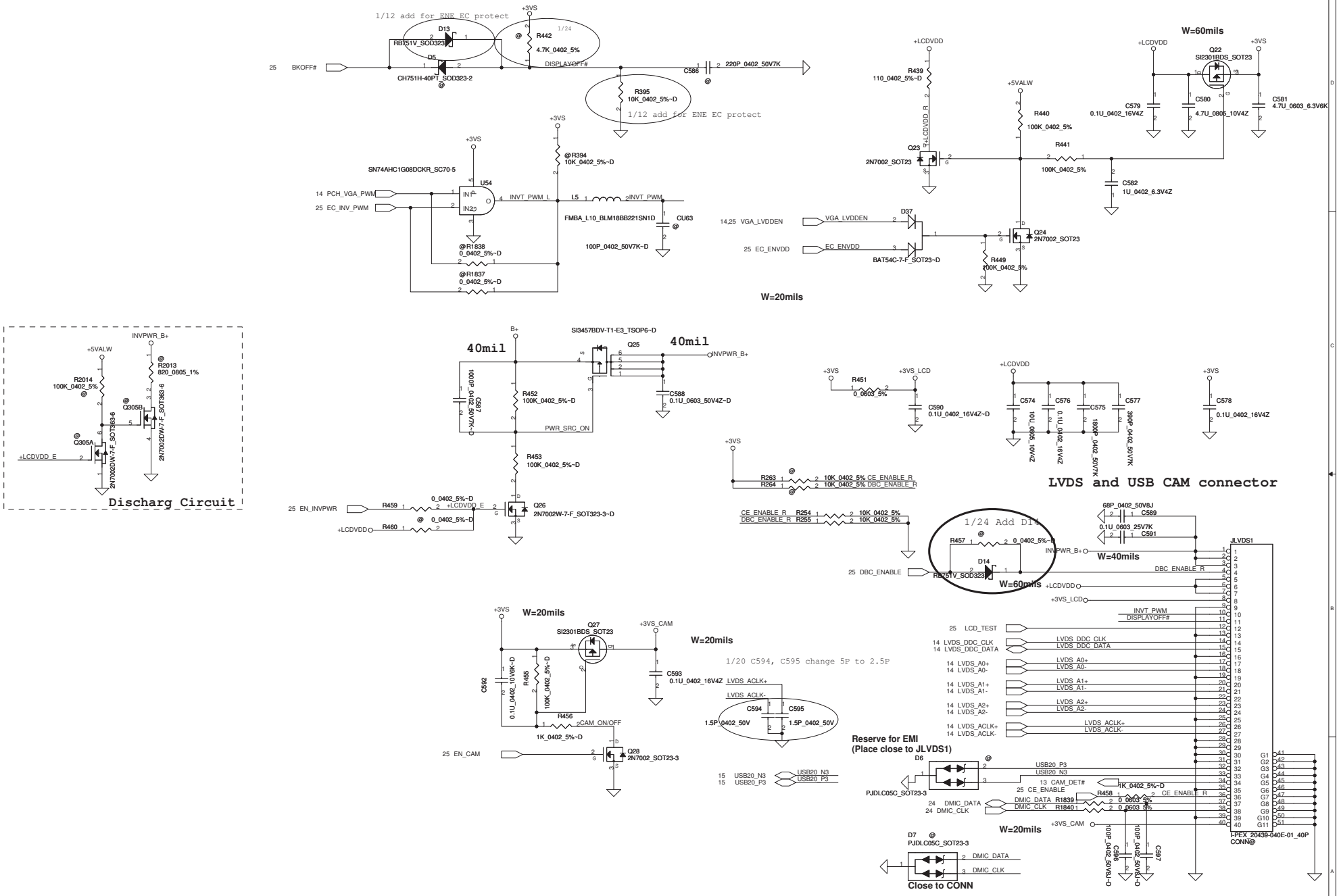
Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-6961P	0.4

Date: Monday, January 24, 2011 | Sheet 19 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **LVDS /camera conn.**

Size	Document Number	Rev
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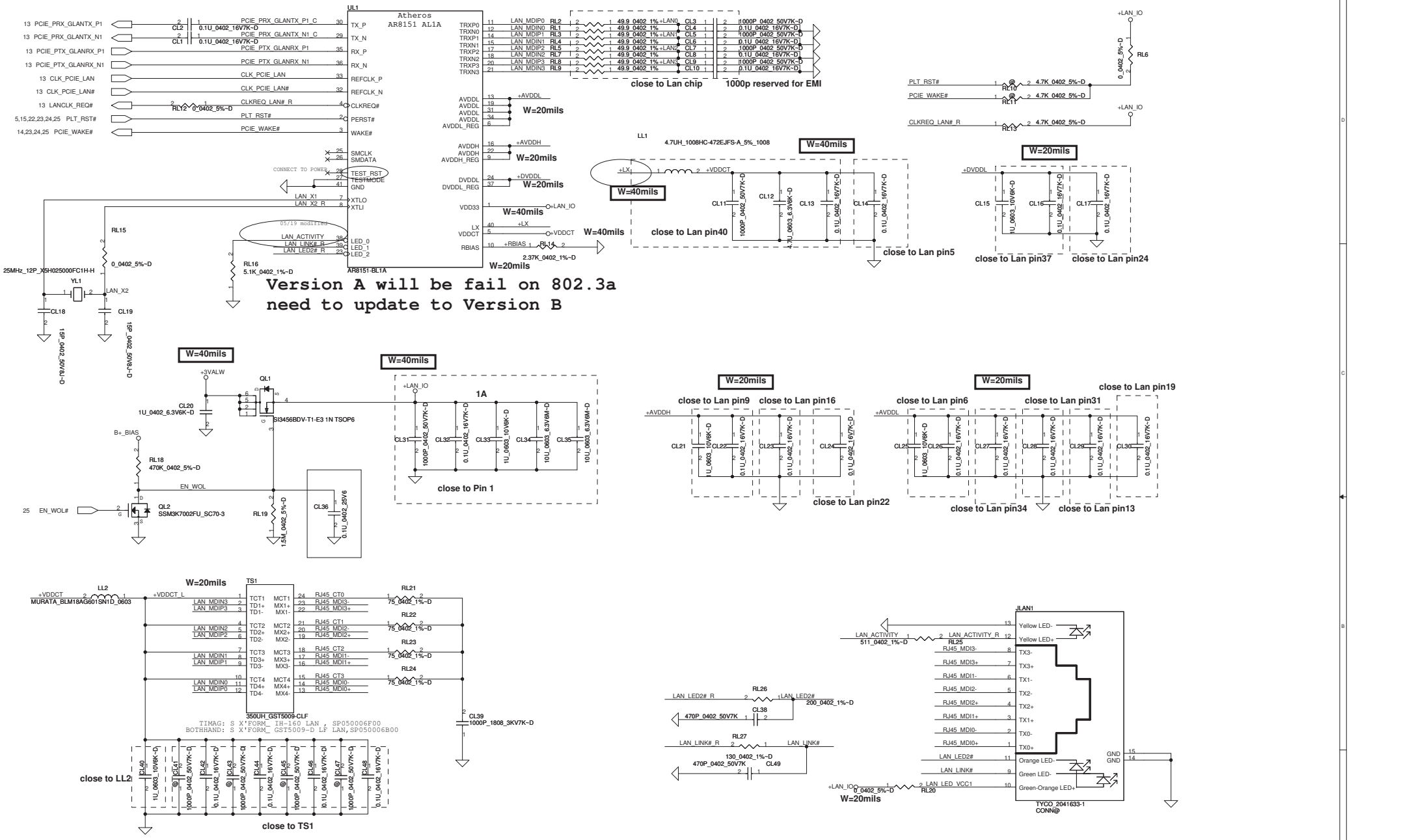
Date: Tuesday, January 25, 2011 | Sheet 20 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **GLAN AR8151 AL1A/ RJ45**

Size	Document Number	Rev
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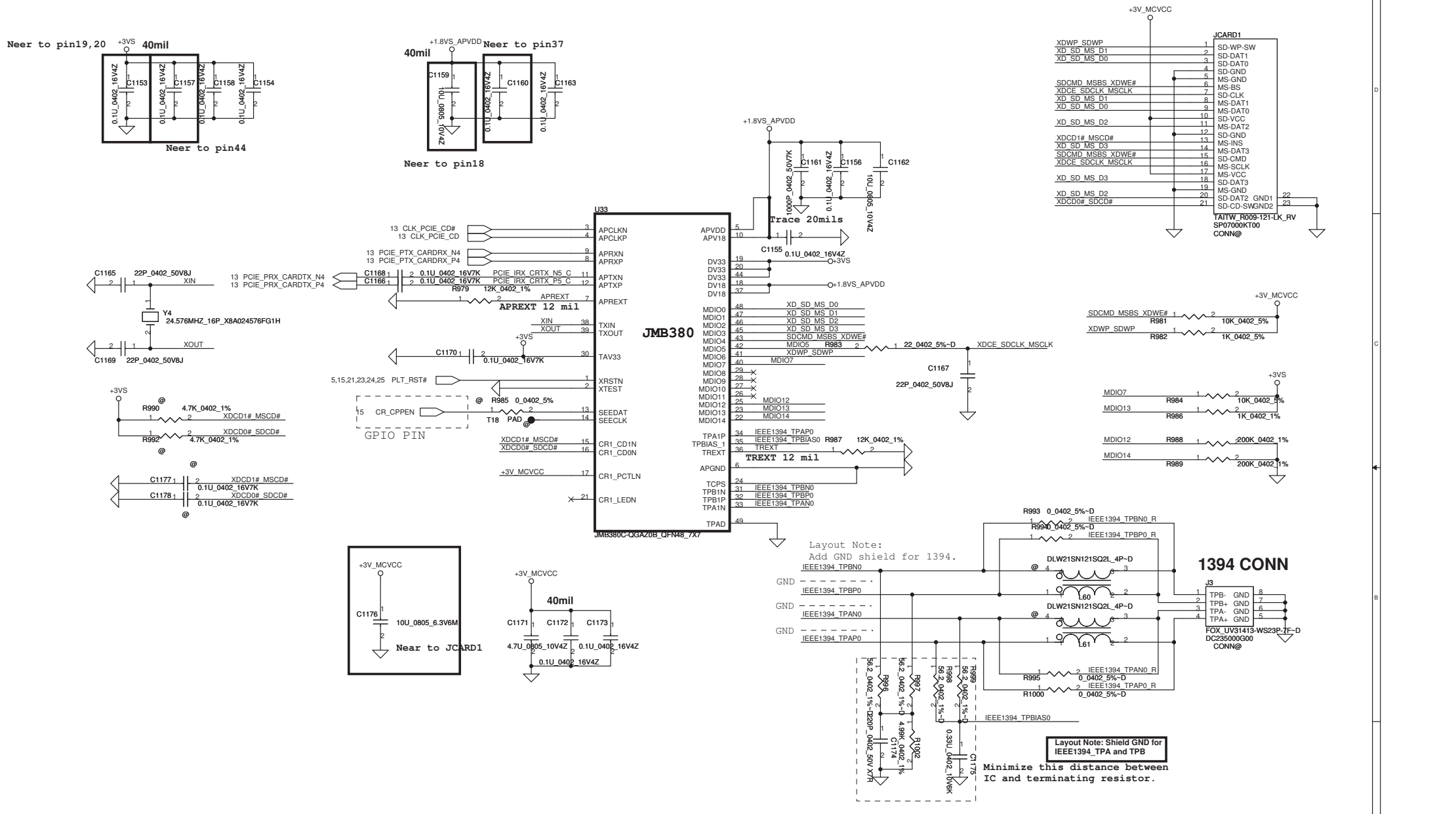
3 in 1 Card Reader CONN



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Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

Compal Electronics, Inc.	
Title	CARD READER/1394
Size: Custom	Document Number: LA-6961P
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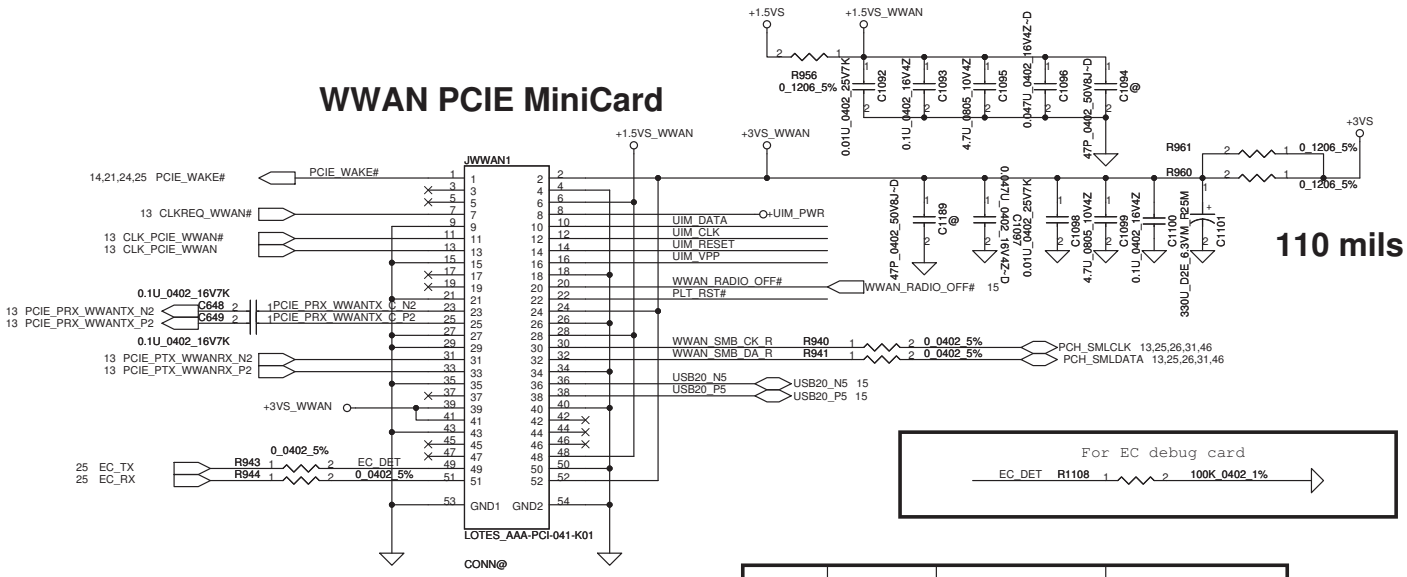
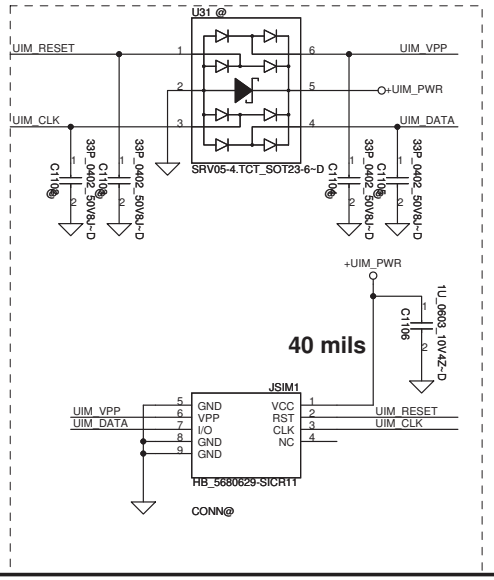
WWAN PCIE MiniCard



SIM Card

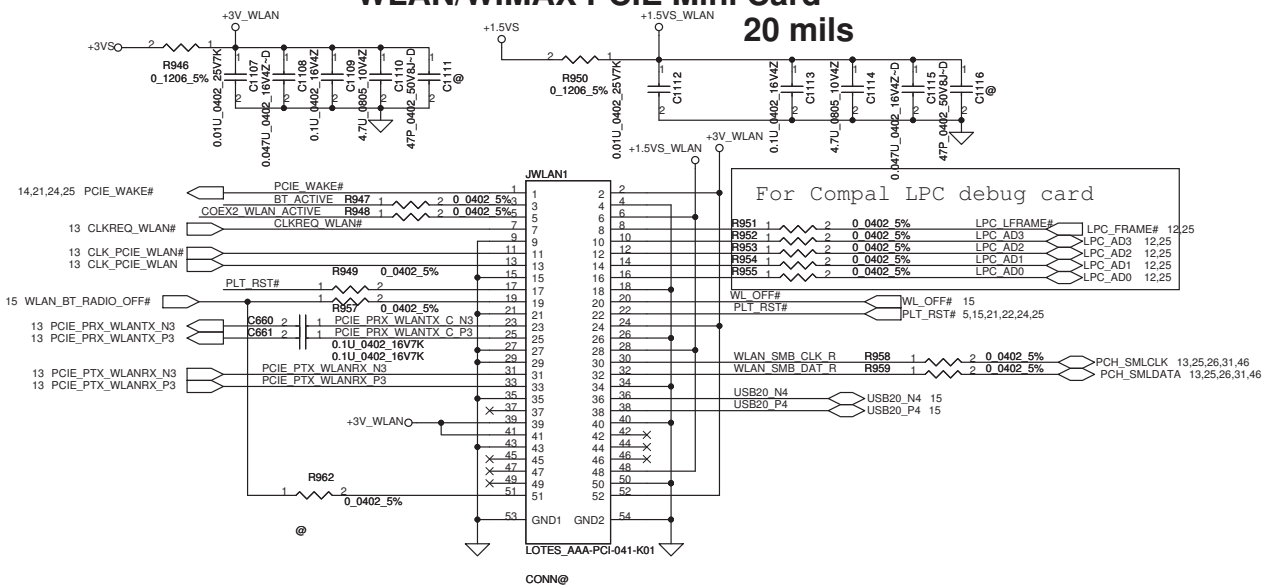


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

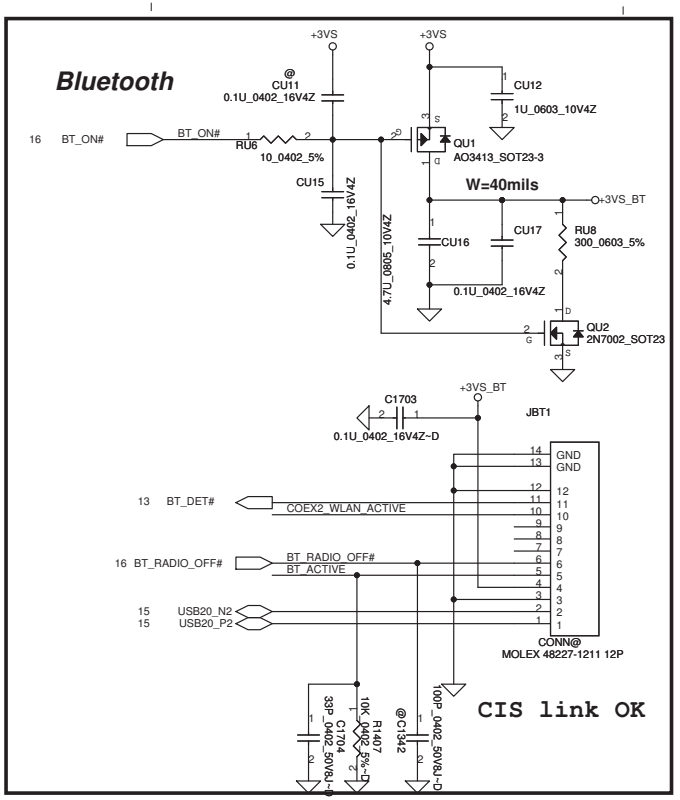
WLAN/WIMAX PCIE Mini Card

40 mils

20 mils



Bluetooth



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.			
Title: WLAN/WWAN/SIM/BT			
Size: Custom	Document Number: LA-6961P		Rev: 0.4
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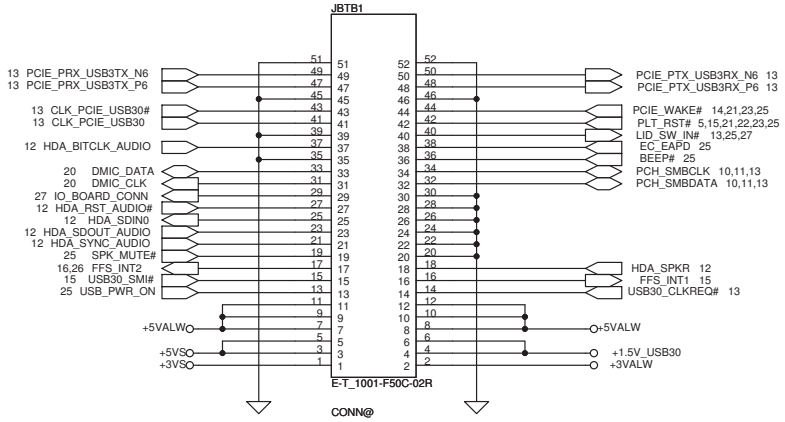
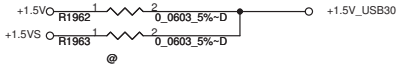
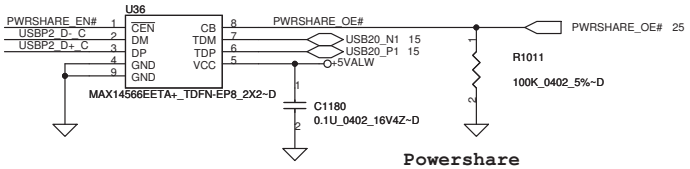
IO Board CONN

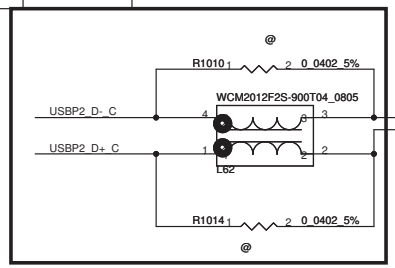


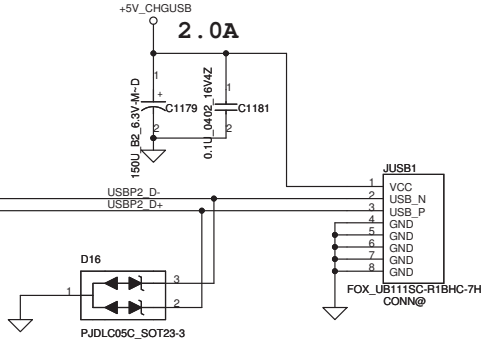




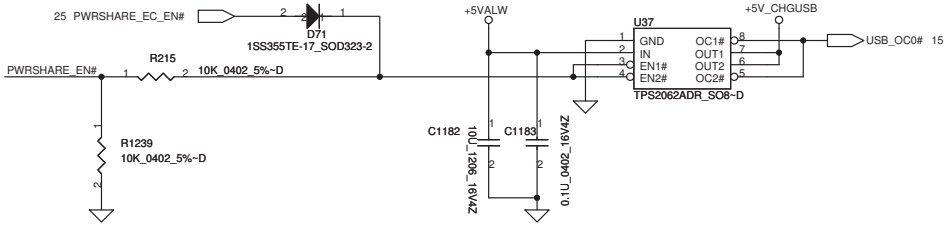
Powershare

OE#	Function
L	Dect charger
H	D=1D





2.0A



Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	USB/LID SW/IO CONN
Size: Custom	Document Number: LA-6961P
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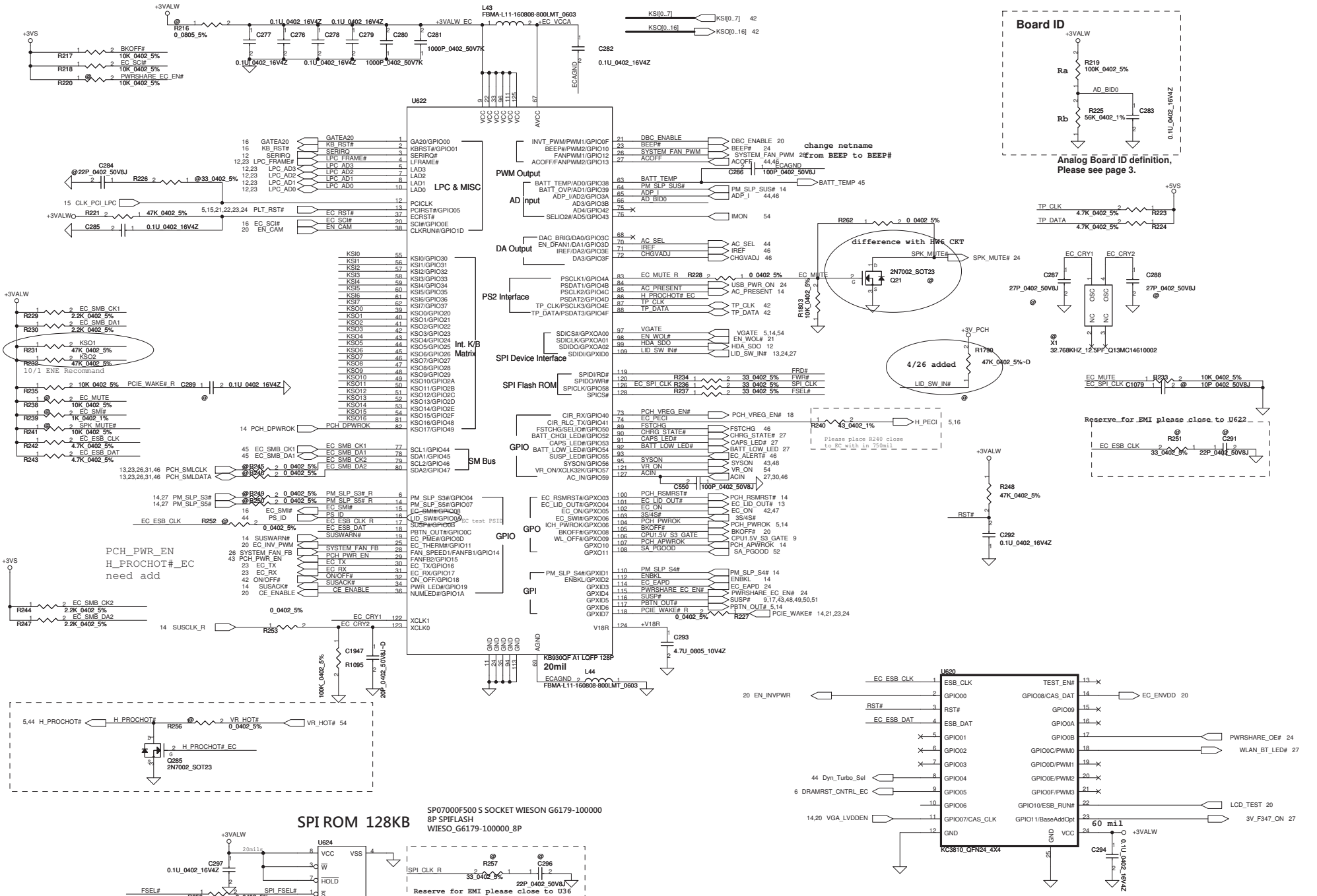
Date: Monday, January 24, 2011	Sheet 24 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/07/06

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Compal Electronics, Inc.

Title: **EC ENE-KB930/ ENE3810**

Size	Document Number	Rev
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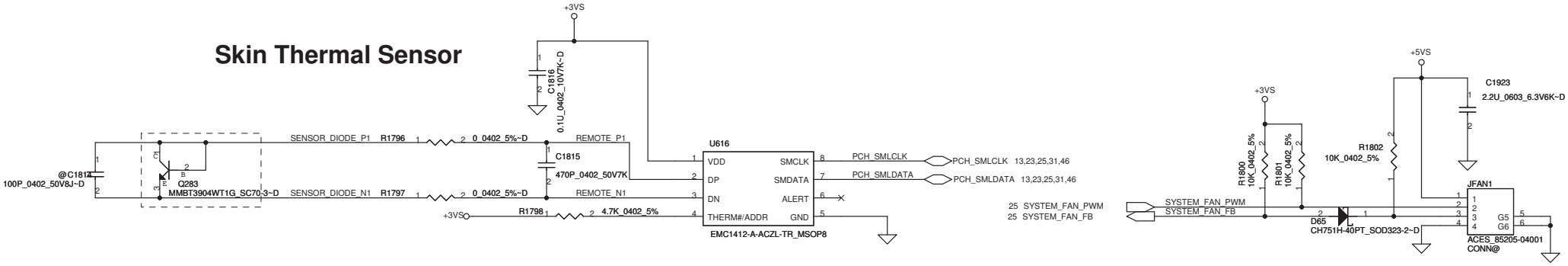
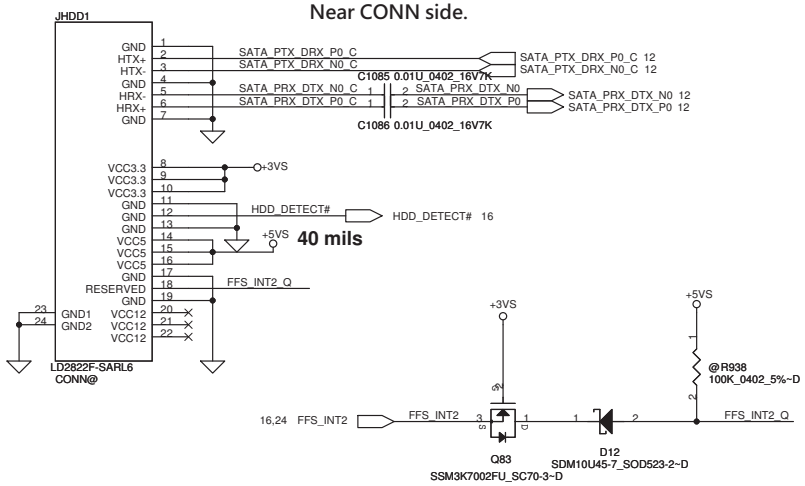
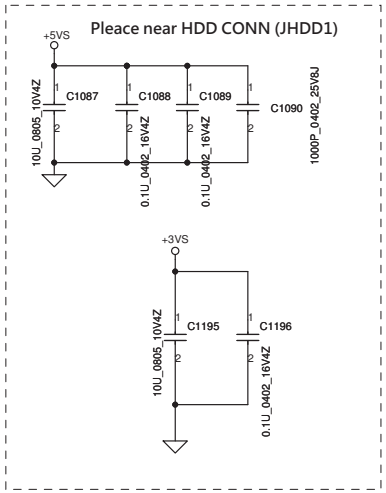
Skin Thermal Sensor



HDD Connector

Near CONN side.





Compal Electronics, Inc.

Title: FAN & Thermal Sensor

Size | Document Number: LA-6961P | Rev: 0.4

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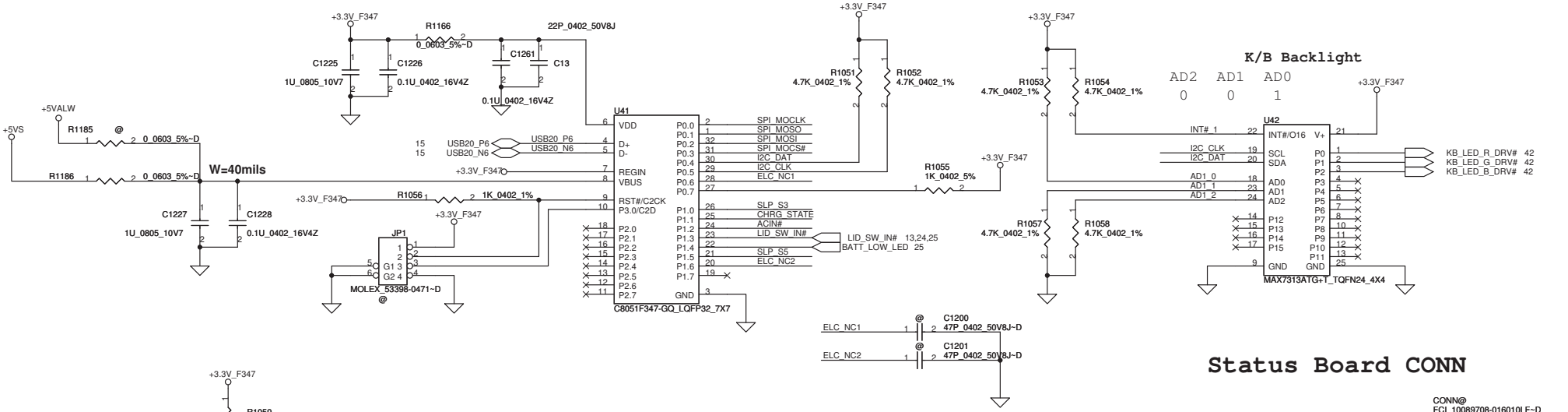
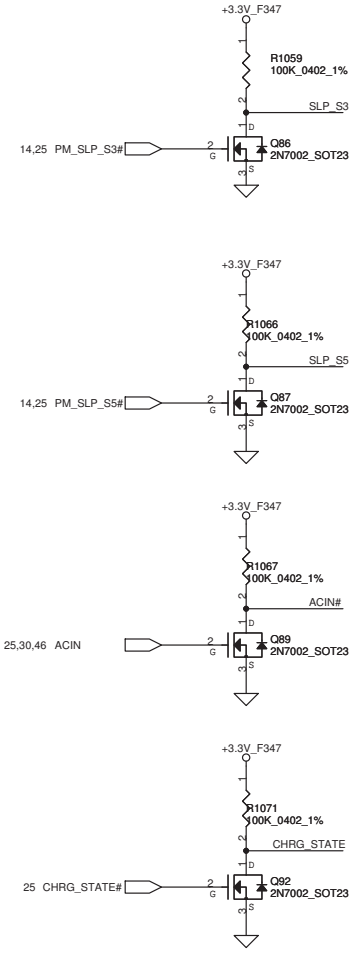
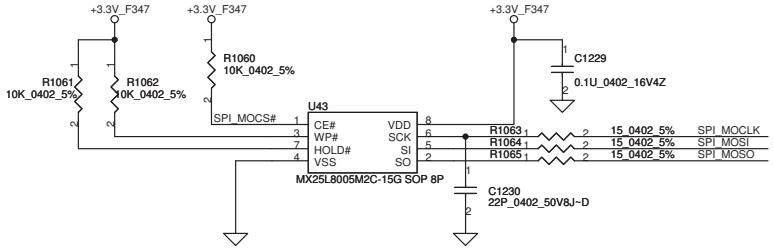
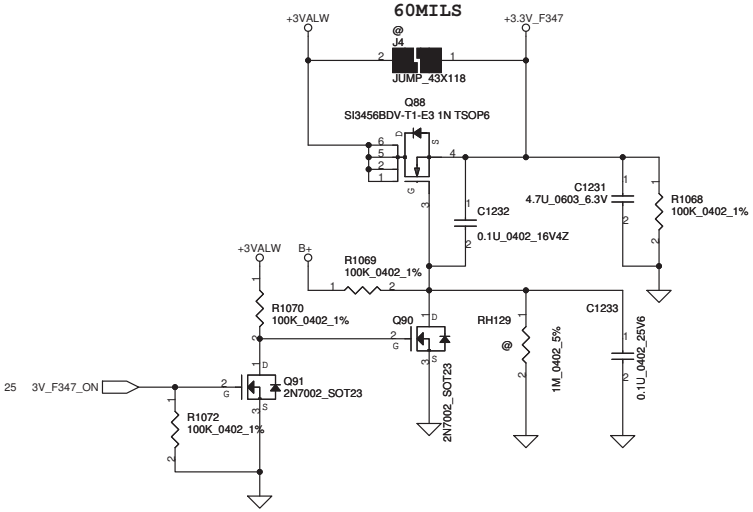
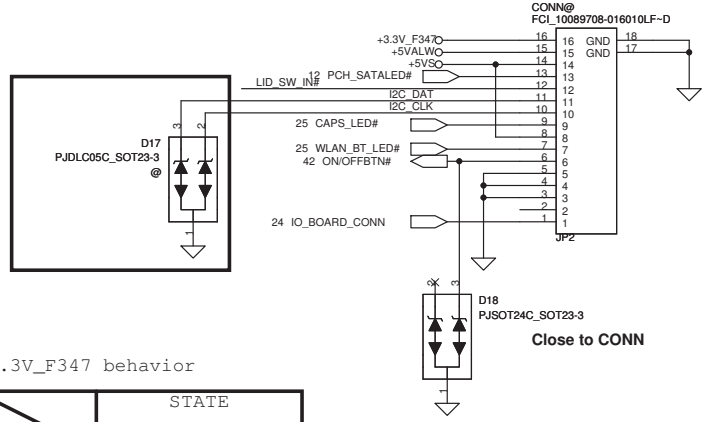


Status Board CONN









+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: ELC/STATUS CONN

Size: Custom | Document Number: LA-6961P | Rev: 0.4

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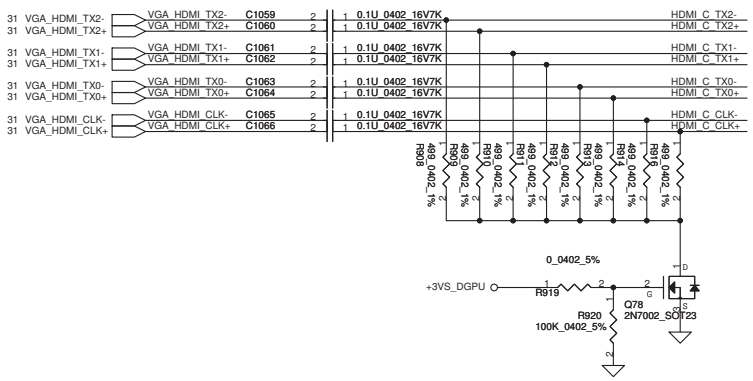
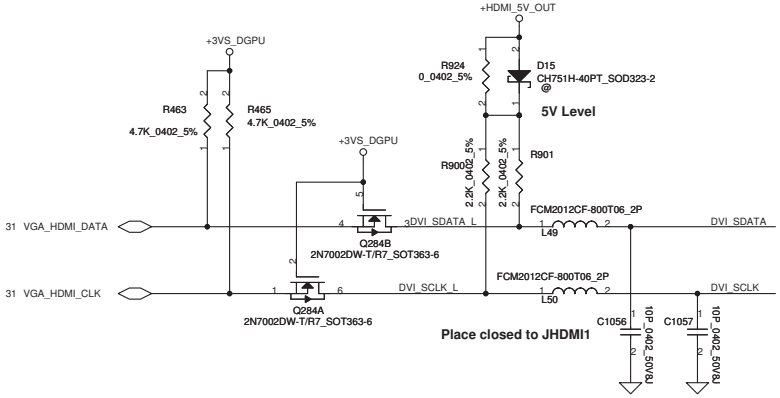
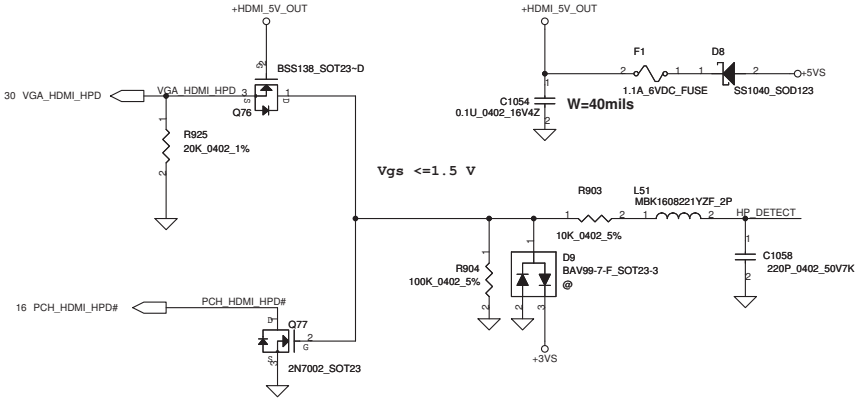
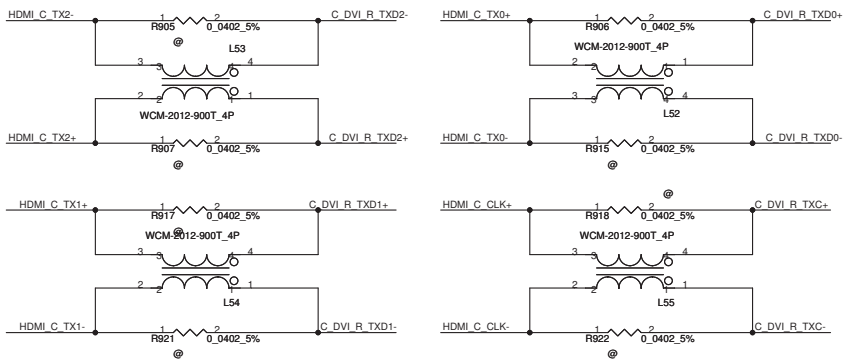
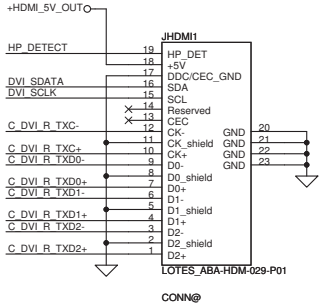








HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.			
Title: HDMI			
Size: Custom	Document Number: LA-6961P		Rev: 0.4
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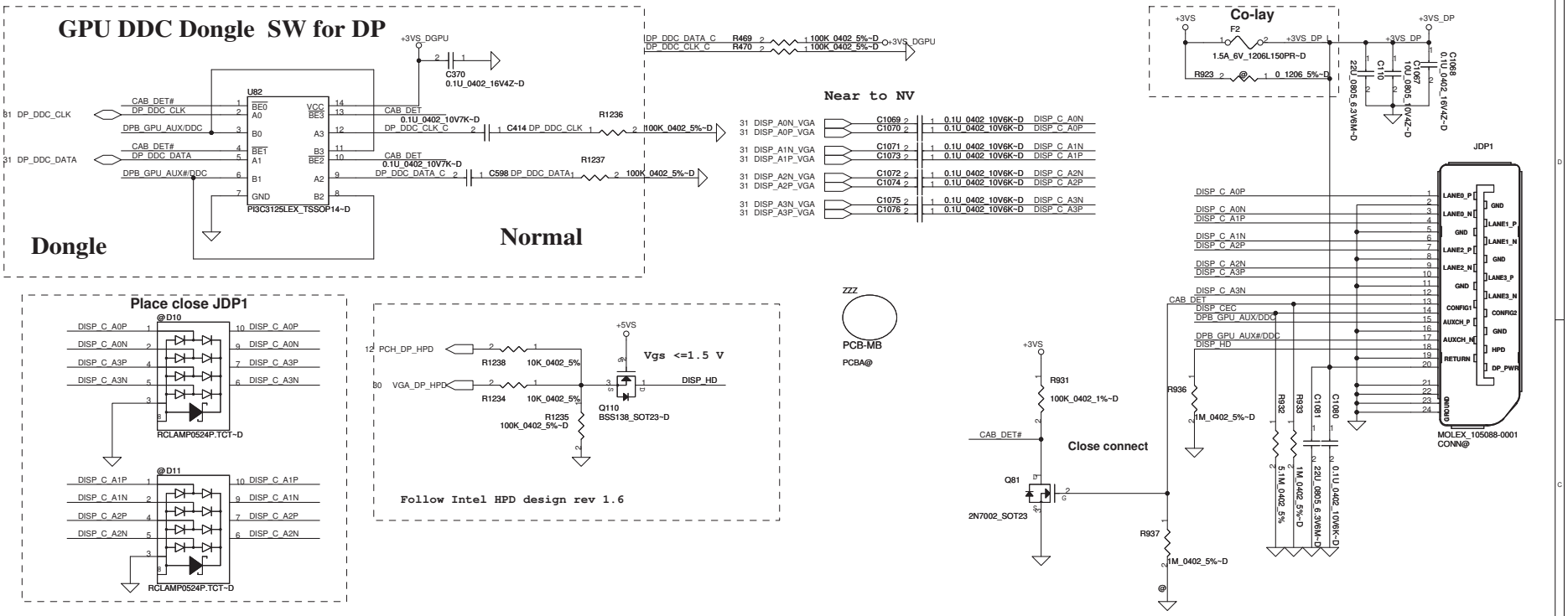

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Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

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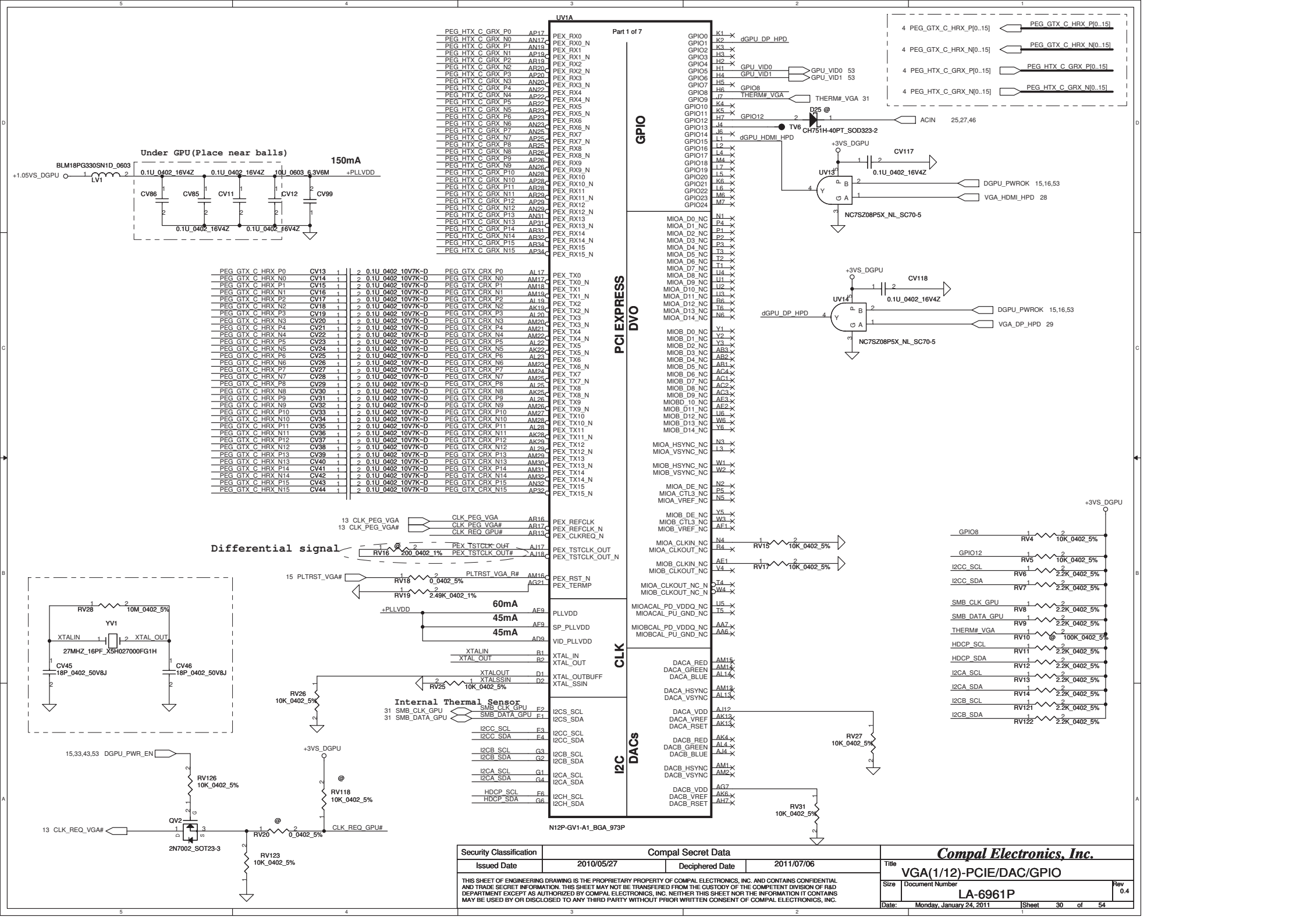
Compal Electronics, Inc.			
Title: DP/FAN/HDD			
Size: Custom	Document Number: LA-6961P		Rev: 0.4
Date: Monday, January 24, 2011	Sheet 29 of 54		



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: VGA(1/12)-PCIE/DAC/GPIO

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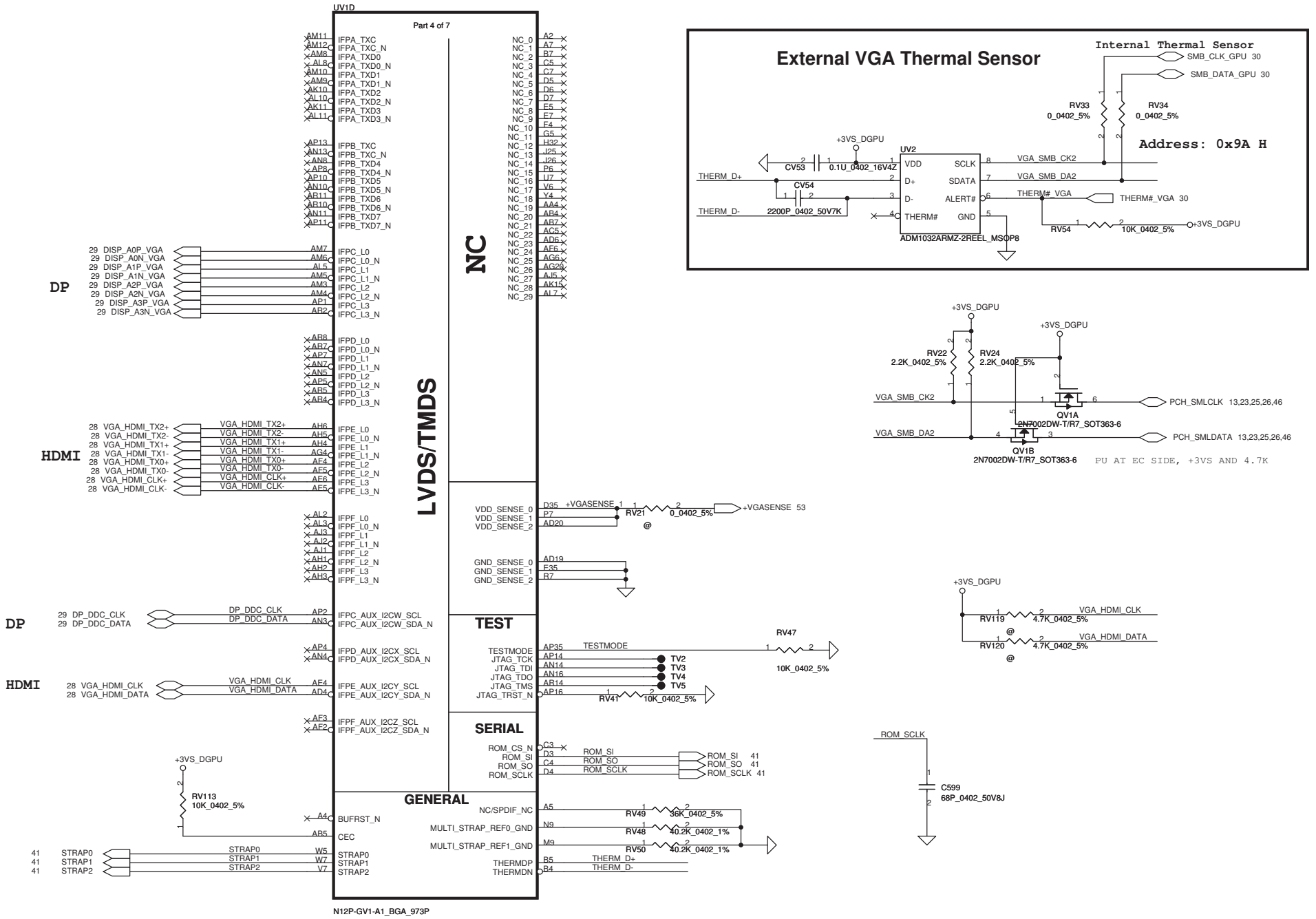

Security Classification	Compal Secret Data	X76	
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	VGA(2/12)-LVDS/HDMI/DP/THM
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+VGA_CORE — C1184 1 2 0.1U_0402_10V7K~D — +1.05VS
+VCC_GFXCORE_AXG — C1185 1 2 0.1U_0402_10V7K~D — +VCC_CORE
+VCC_GFXCORE_AXG — C1187 1 2 0.1U_0402_10V7K~D — +VCC_CORE
+VCC_GFXCORE_AXG — C1188 1 2 0.1U_0402_10V7K~D — +VCC_CORE

+VCC_CORE — C1186 1 2 0.1U_0402_10V7K~D — +1.05VS
+VCC_CORE — C1190 1 2 0.1U_0402_10V7K~D — +1.05VS

30.5A

+VGA_CORE

UV1G

Part 7 of 7

POWER

AB11	VDD_0	VDD_56	P21
AB13	VDD_1	VDD_57	P23
AB15	VDD_2	VDD_58	P25
AB17	VDD_3	VDD_59	R11
AB19	VDD_4	VDD_60	R12
AB21	VDD_5	VDD_61	R13
AB23	VDD_6	VDD_62	R14
AB25	VDD_7	VDD_63	R15
AC11	VDD_8	VDD_64	R16
AC12	VDD_9	VDD_65	R17
AC13	VDD_10	VDD_66	R18
AC14	VDD_11	VDD_67	R19
AC15	VDD_12	VDD_68	R20
AC16	VDD_13	VDD_69	R21
AC17	VDD_14	VDD_70	R22
AC18	VDD_15	VDD_71	R23
AC19	VDD_16	VDD_72	R24
AC20	VDD_17	VDD_73	R25
AC21	VDD_18	VDD_74	T12
AC22	VDD_19	VDD_75	T14
AC23	VDD_20	VDD_76	T16
AC24	VDD_21	VDD_77	T18
AC25	VDD_22	VDD_78	T20
AD12	VDD_23	VDD_79	T22
AD14	VDD_24	VDD_80	T24
AD16	VDD_25	VDD_81	V11
AD18	VDD_26	VDD_82	V13
AD22	VDD_27	VDD_83	V15
AD24	VDD_28	VDD_84	V17
L11	VDD_29	VDD_85	V19
L12	VDD_30	VDD_86	V21
L13	VDD_31	VDD_87	V23
L14	VDD_32	VDD_88	V25
L15	VDD_33	VDD_89	W11
L16	VDD_34	VDD_90	W12
L17	VDD_35	VDD_91	W13
L18	VDD_36	VDD_92	W14
L19	VDD_37	VDD_93	W15
L20	VDD_38	VDD_94	W16
L21	VDD_39	VDD_95	W17
L22	VDD_40	VDD_96	W18
L23	VDD_41	VDD_97	W19
L24	VDD_42	VDD_98	W20
L25	VDD_43	VDD_99	W21
M12	VDD_44	VDD_100	W22
M14	VDD_45	VDD_101	W23
M16	VDD_46	VDD_102	W24
M18	VDD_47	VDD_103	W25
M20	VDD_48	VDD_104	Y12
M22	VDD_49	VDD_105	Y14
M24	VDD_50	VDD_106	Y16
P11	VDD_51	VDD_107	Y18
P13	VDD_52	VDD_108	Y20
P15	VDD_53	VDD_109	Y22
P17	VDD_54	VDD_110	Y24
P19	VDD_55		

+VGA_CORE

N12P-GV1-A1_BGA_973P

Near GPU

+VGA_CORE

CV57 470U_D2_2V-M~D

CV912 47U_0805_4V6

CV318 22U_0805_6.3V6M

CV64 10U_0603_6.3V6M

CV66 10U_0603_6.3V6M

CV213 4.7U_0603_6.3V6K

Under GPU

+VGA_CORE

CV295 0.1U_0402_16V4Z

CV296 0.1U_0402_16V4Z

CV73 0.047U_0402_25V6K

CV74 0.047U_0402_25V6K

CV75 0.047U_0402_25V6K

+VGA_CORE

CV80 0.022U_0402_25V7K

CV81 0.022U_0402_25V7K

CV119 0.022U_0402_25V7K

+VGA_CORE

CV72 1U_0402_6.3V4Z

CV913 0.22U_0402_6.3V6K

CV914 0.22U_0402_6.3V6K

CV915 0.22U_0402_6.3V6K

+VGA_CORE

CV105 0.01U_0402_25V7K

CV115 0.01U_0402_25V7K

CV116 0.01U_0402_25V7K

CV120 0.01U_0402_25V7K

CV121 0.01U_0402_25V7K

CV127 0.01U_0402_25V7K

CV128 0.01U_0402_25V7K

CV130 0.01U_0402_25V7K

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

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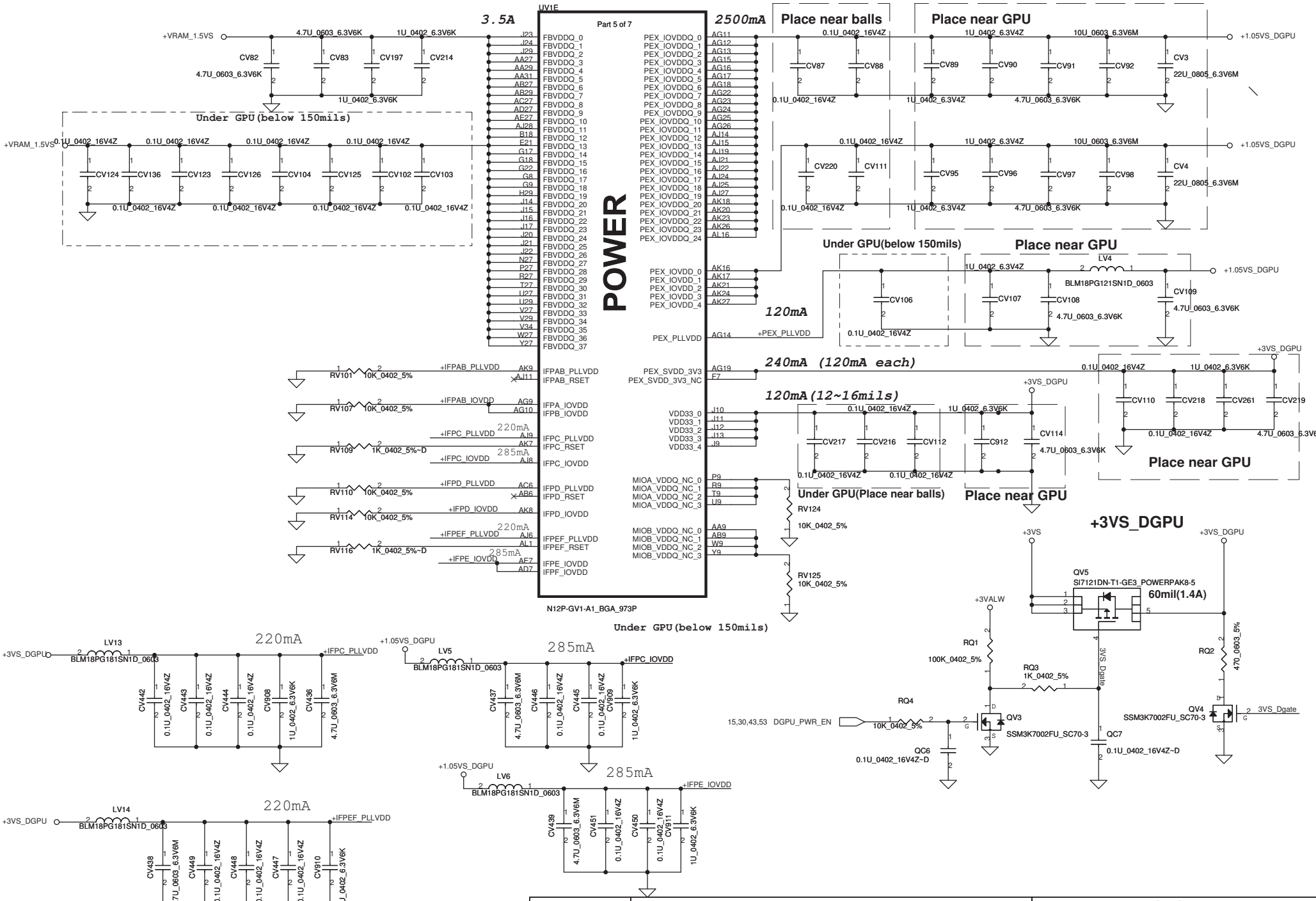

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	VGA(4/12)-POWER
Size	Document Number: LA-6961P
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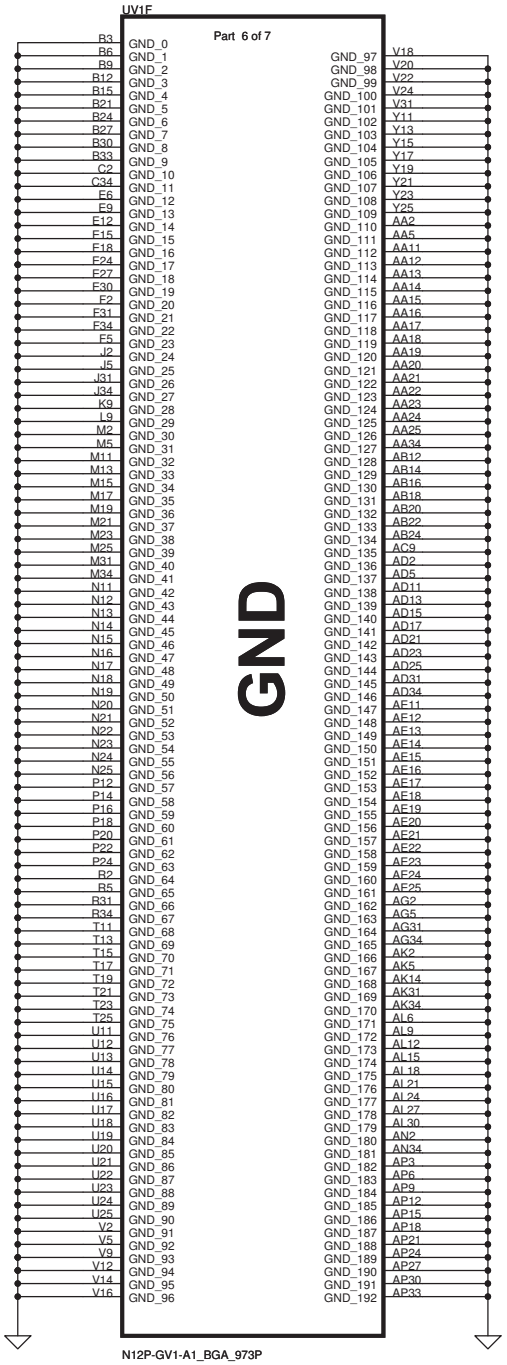

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: VGA(5/12)-GND

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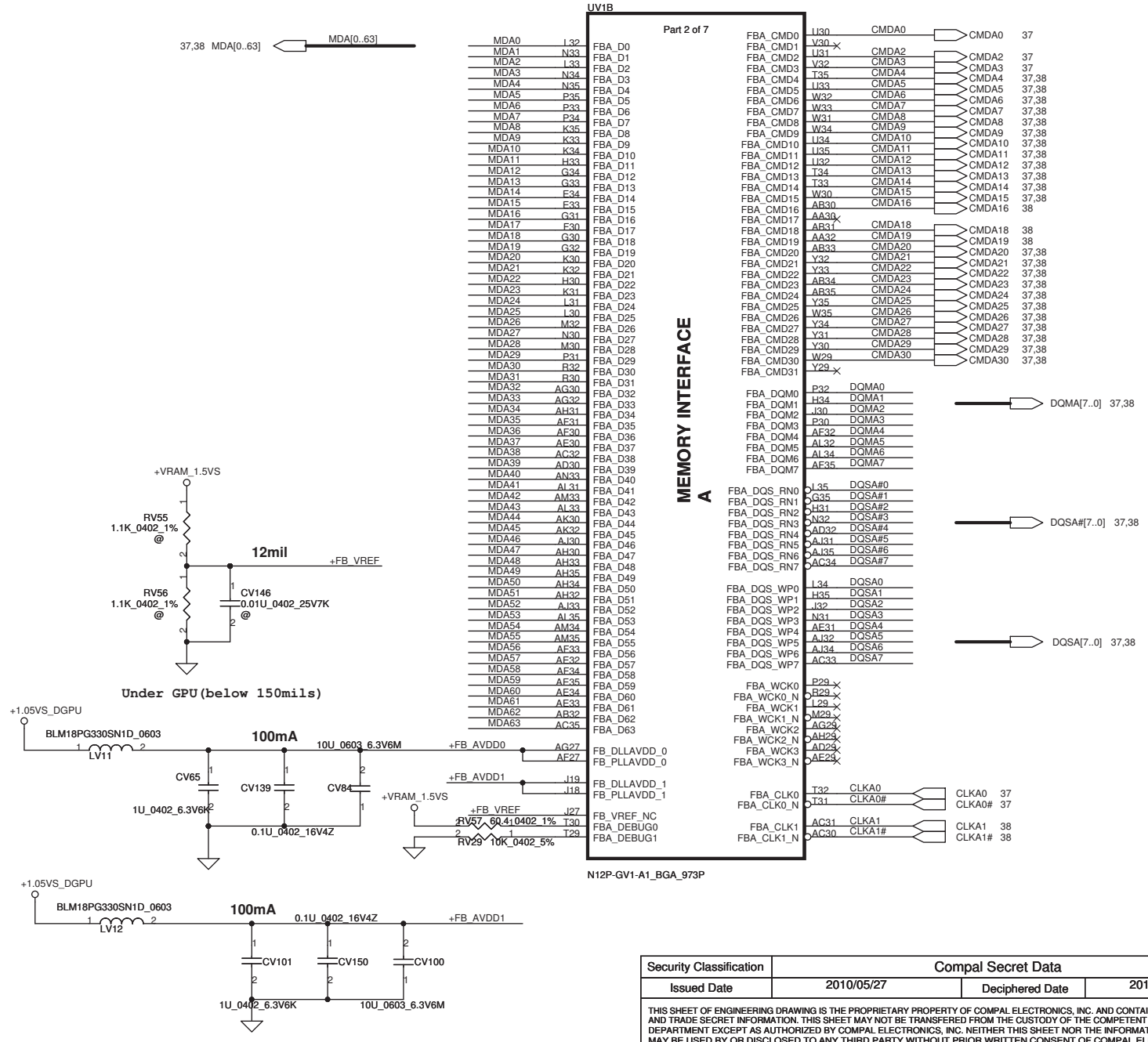


Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

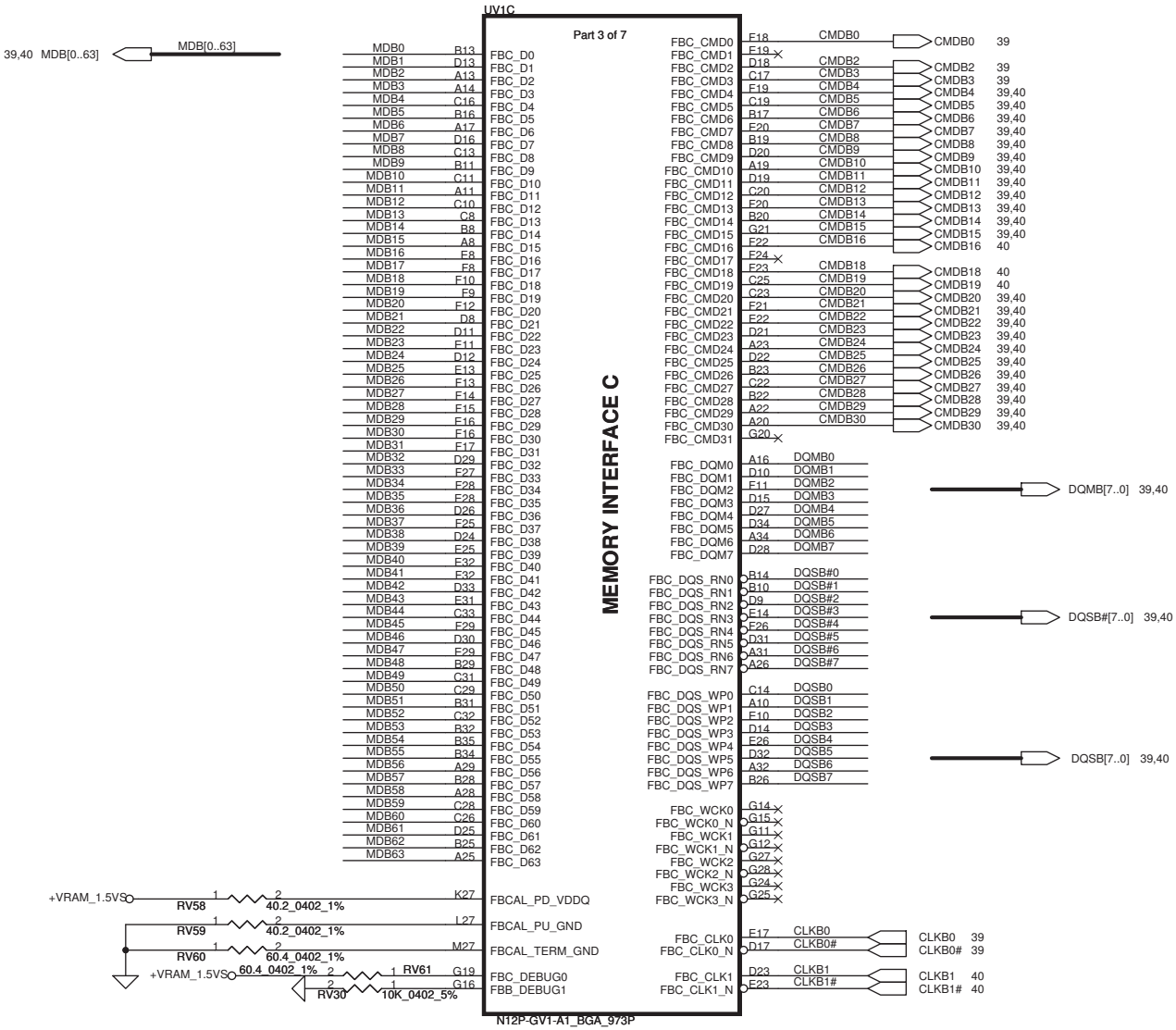
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: LA-6961P | Rev: 0.4

Date: Monday, January 24, 2011 | Sheet 35 of 54



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.
Title: VGA(7/12)-MEM Interface C
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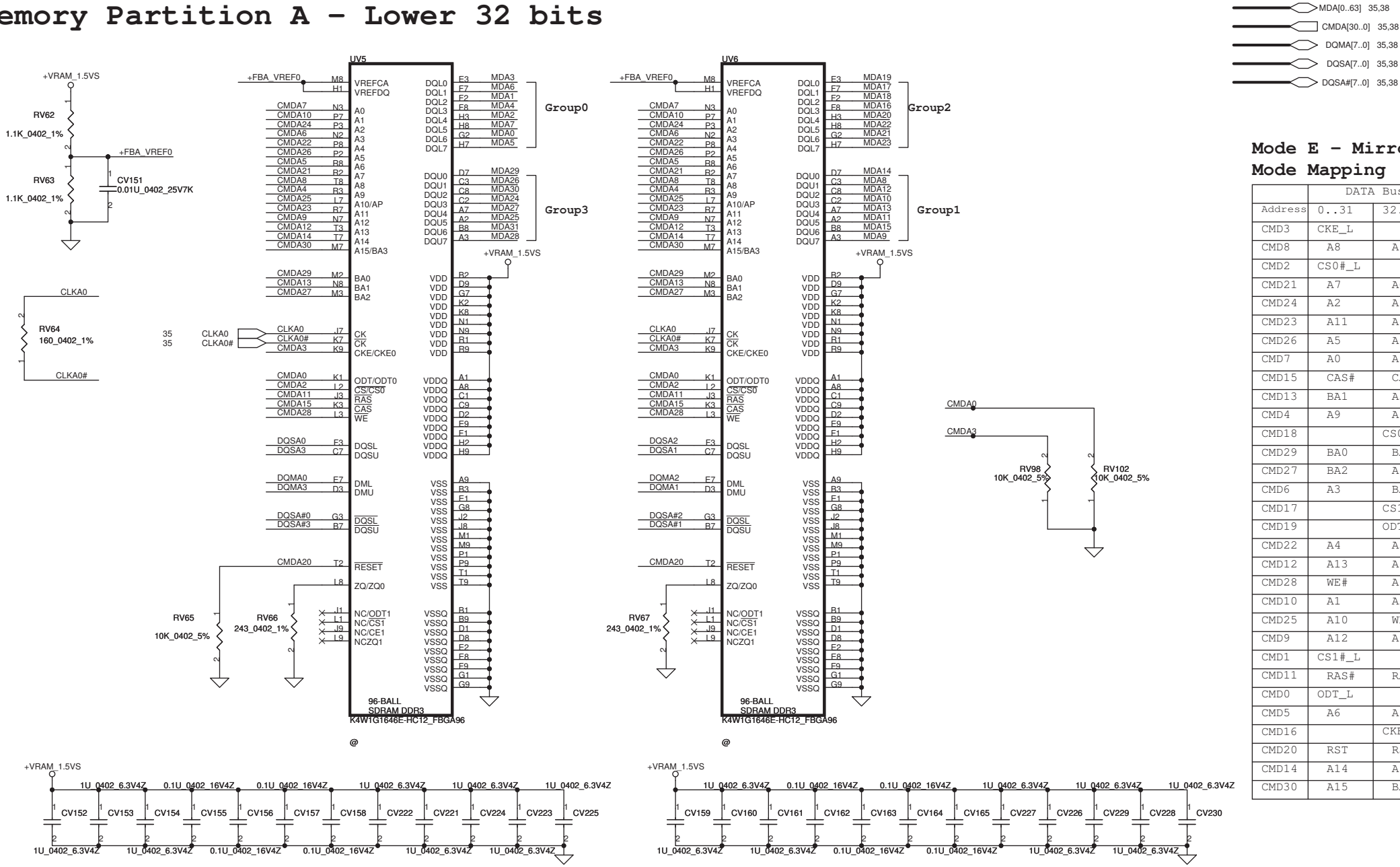
Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	VGA(8/12)-VRAM A Lower
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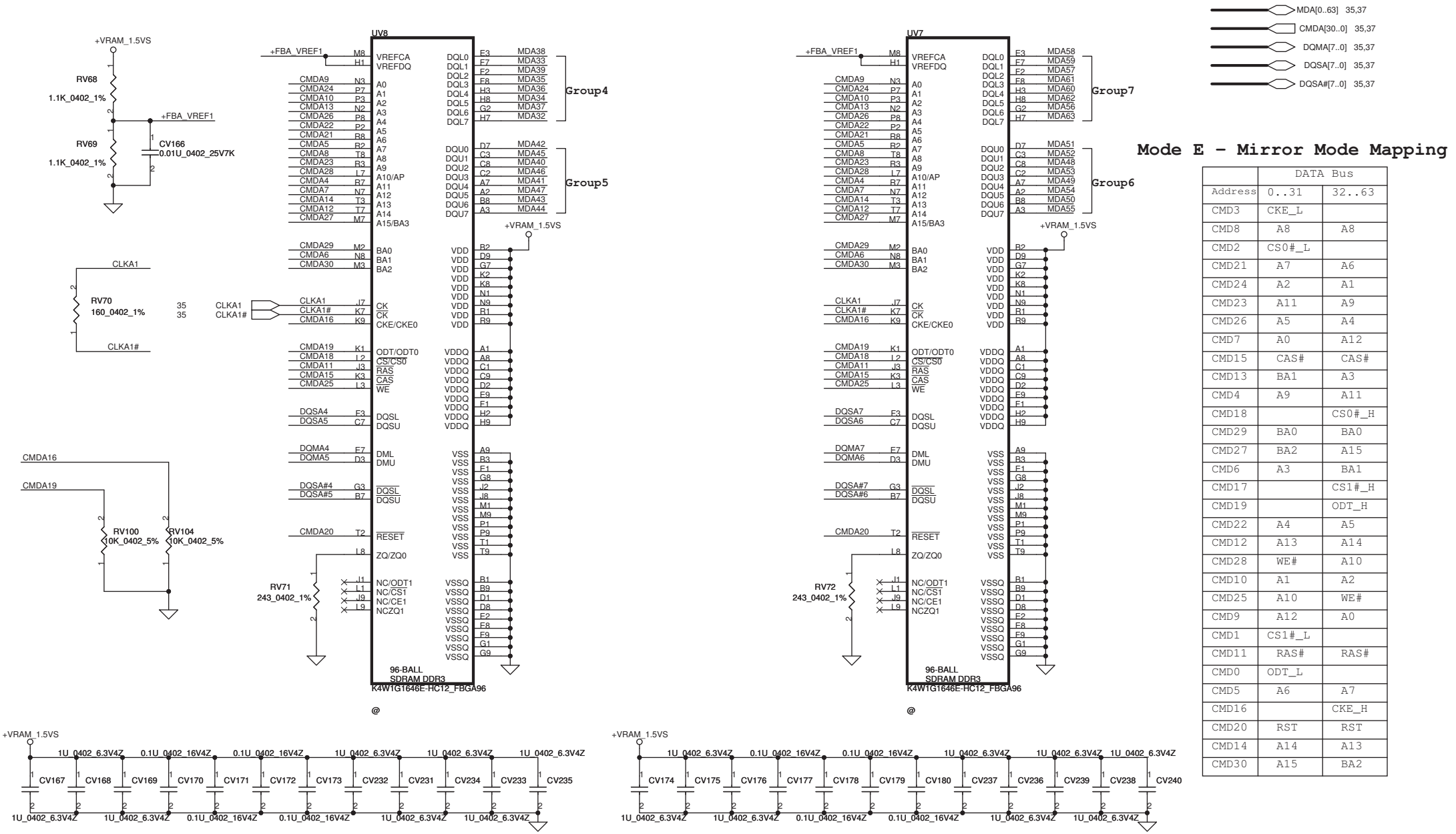
Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.			
Title	VGA(9/12)-VRAM A Upper		
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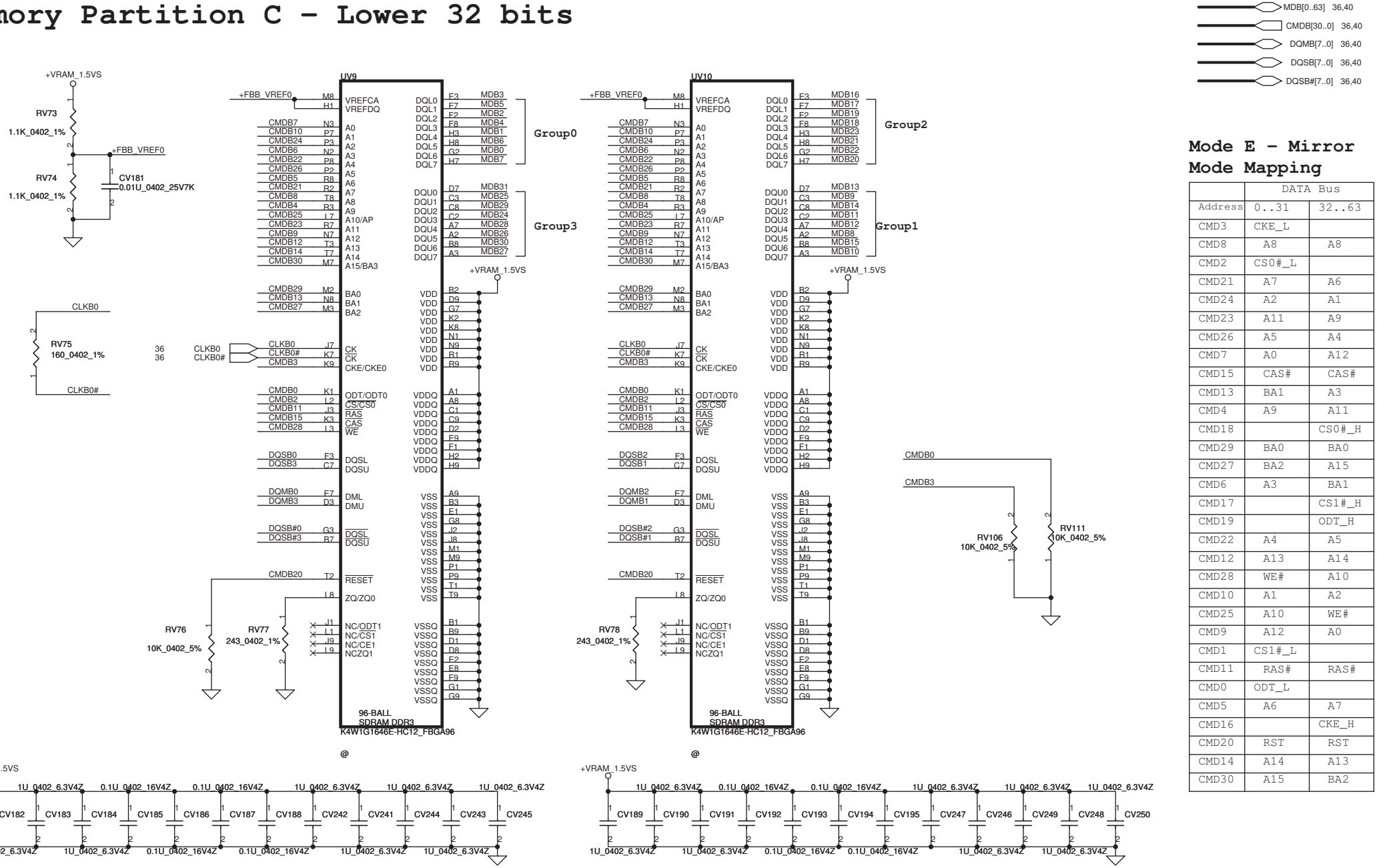
Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	VGA(10/12)-VRAM C Lower
Size: Custom	Document Number: LA-6961P
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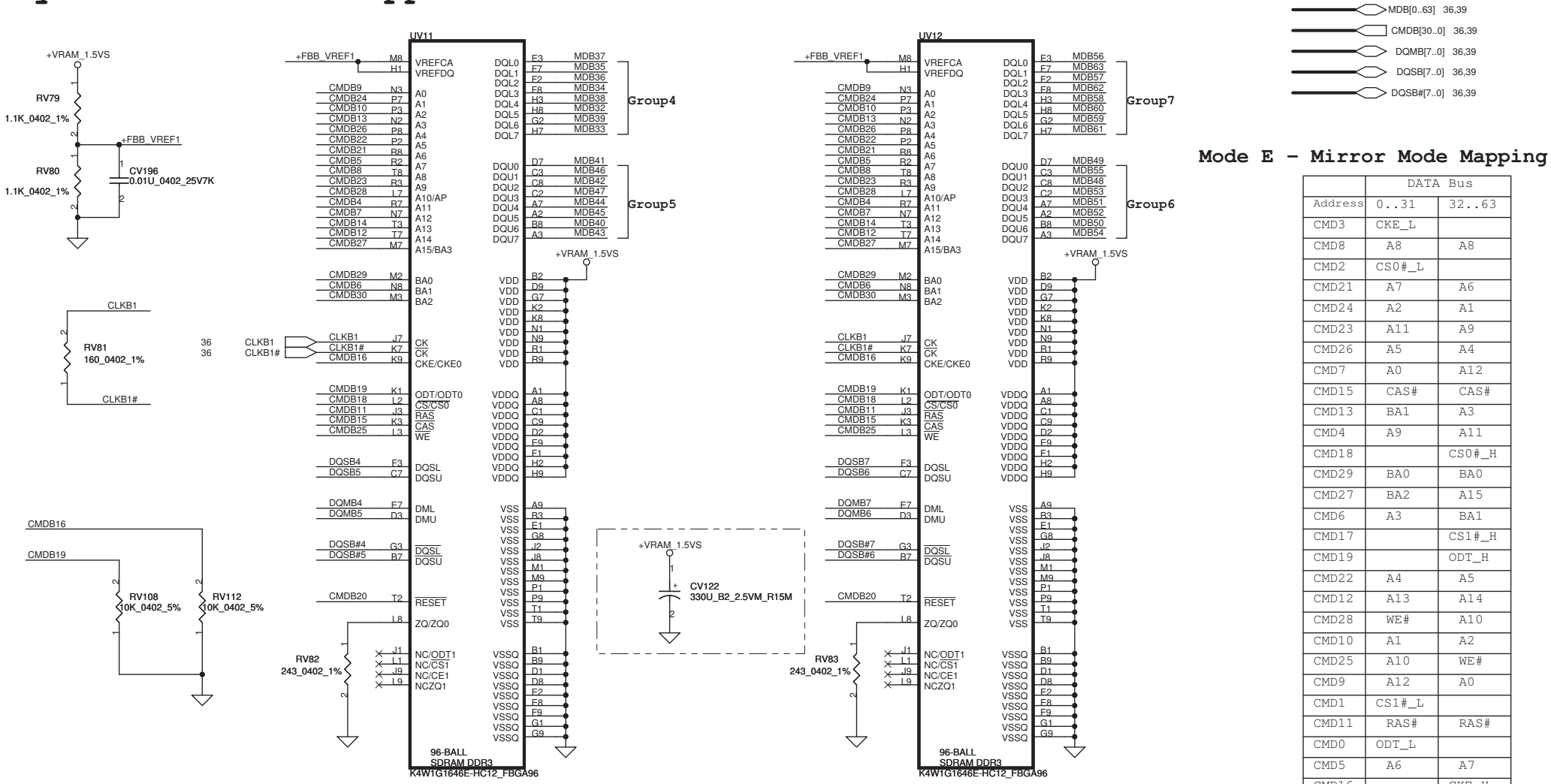
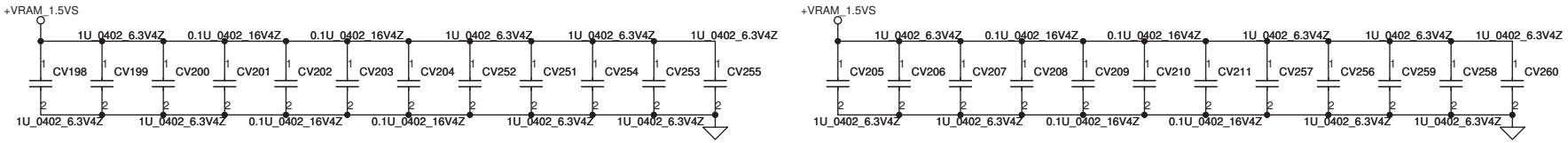
Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: VGA(11/12)-VRAM C Upper

Size	Document Number	Rev
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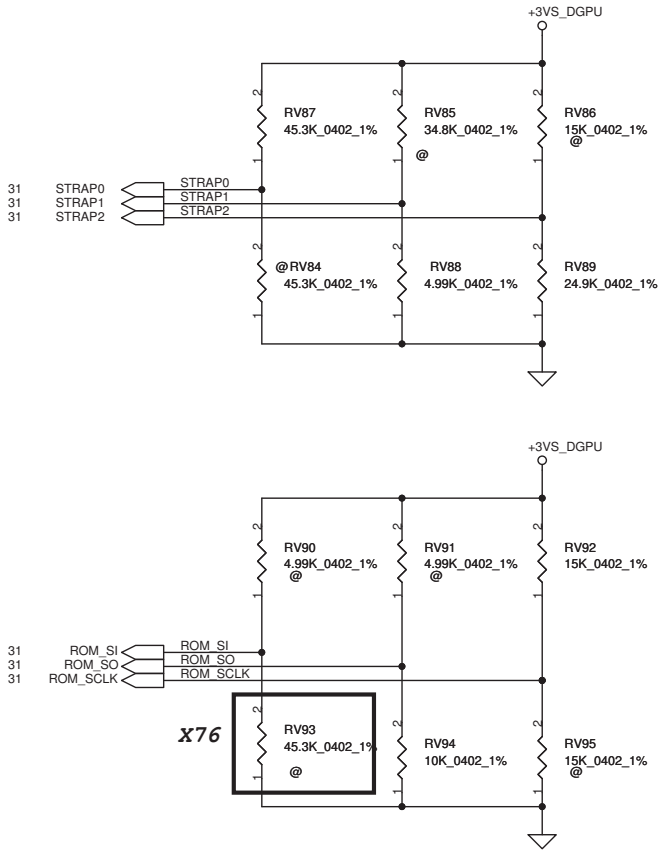


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

N12P-GS-A1 :
ROM_SO : PL-10K
ROM_CLK : PH-15K
ROM_SI : PL45.3K (Samsung 2GB)
Strap 2 : PL-5K
Strap 1 : PH-35K
Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003YO00	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/07/06

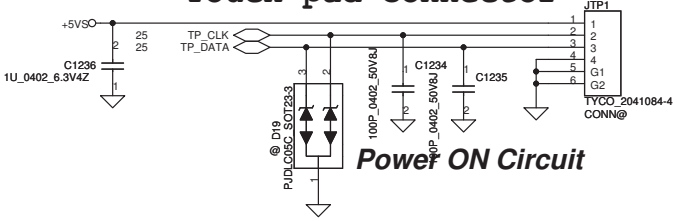
Compal Electronics, Inc.

Title: VGA(12/12)-MISC

Size: Custom | Document Number: LA-6961P | Rev: 0.4

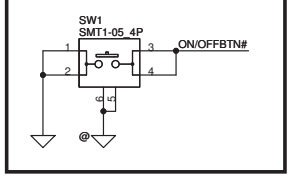
Date: Monday, January 24, 2011 | Sheet 41 of 54

Touch pad Connector

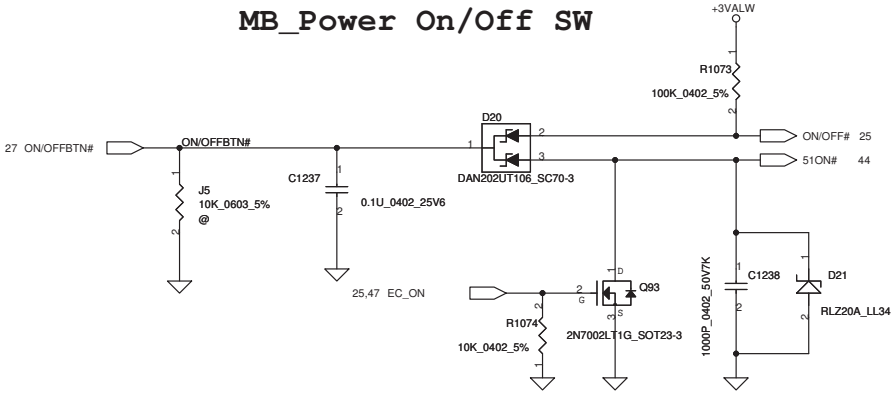


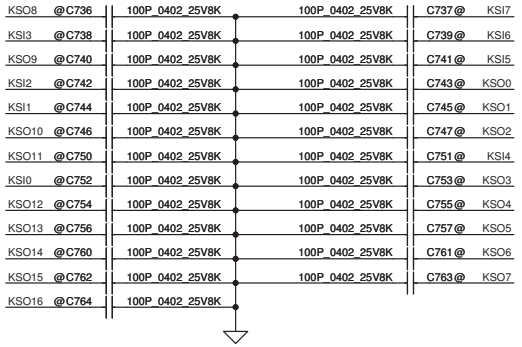
Power ON Circuit

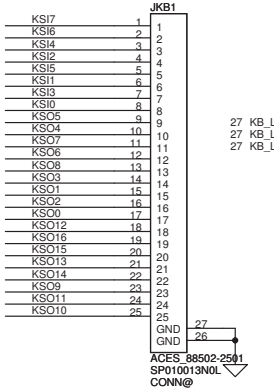
For Debug Only

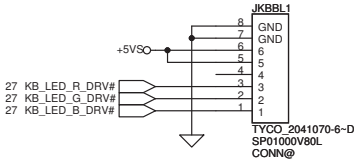


MB_Power On/Off SW



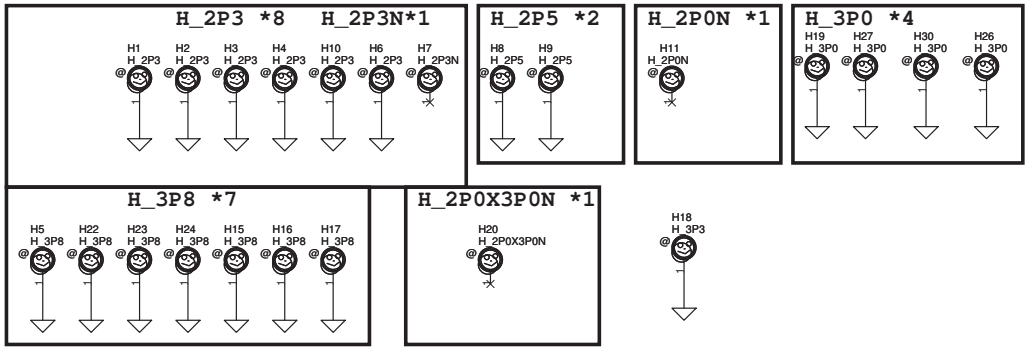






KSI[0..7] KSI[0..7] 25

KSO[0..16] KSO[0..16] 25



Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.	
Title	SW/TP/SCREW
Size: Custom	Document Number: LA-6961P
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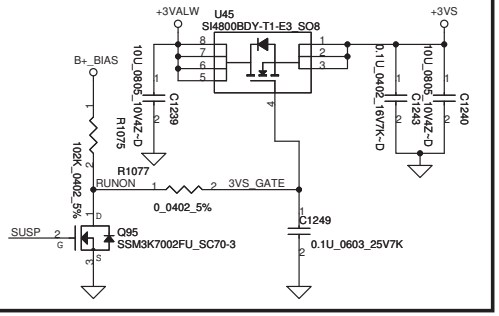
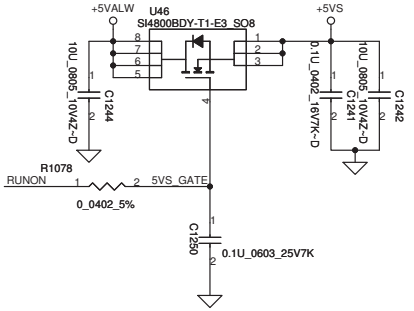
Date: Monday, January 24, 2011	Sheet 42 of 54

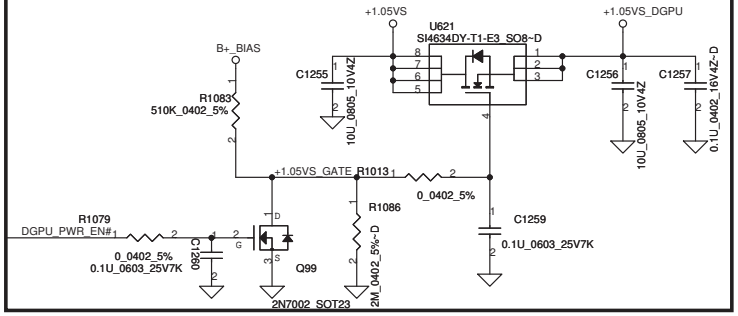
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

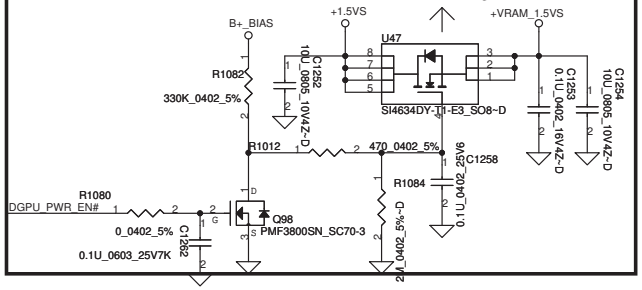


+1.05V to +1.05VS_DGPU Transfer

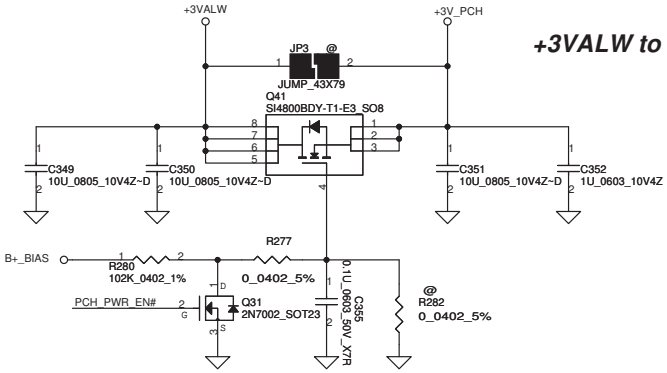


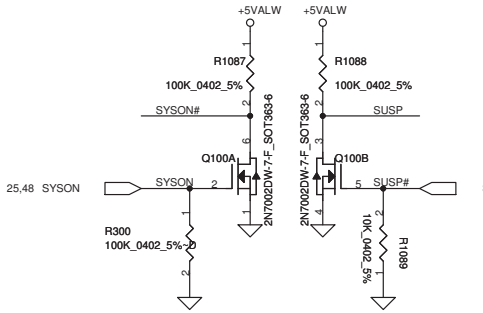
+1.5VS to +1.5VSDGPU Transfer

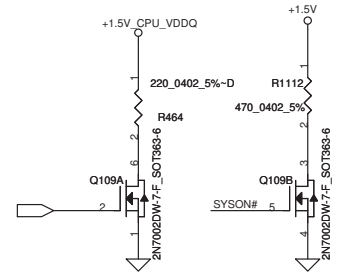
SB54392008L EOL, P/N change to SB54800038L

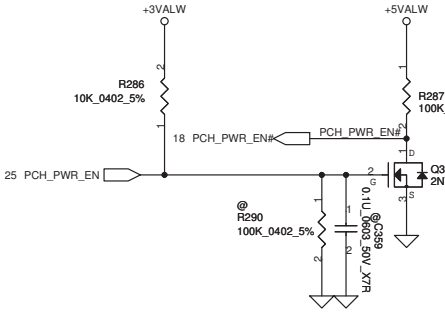


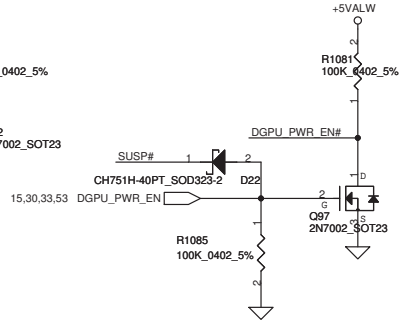
+3VALW to +3V_PCH

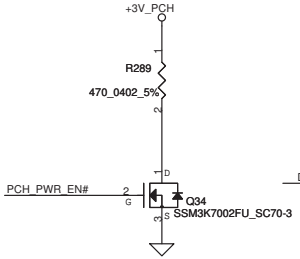


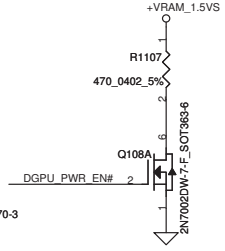


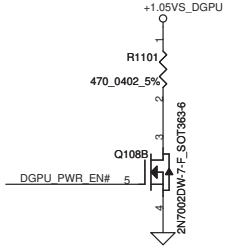


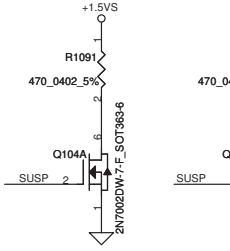


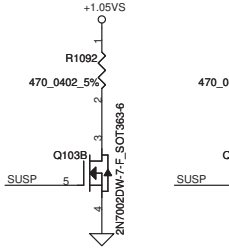


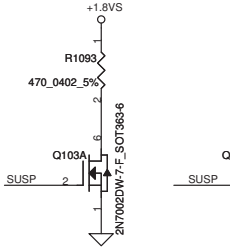


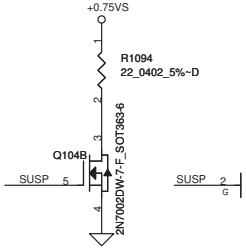


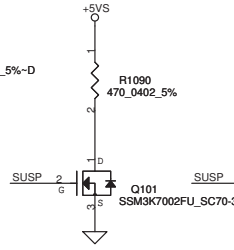


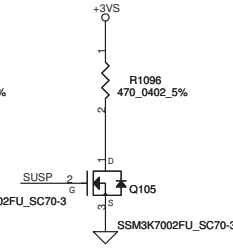












Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2011/07/06

Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

Size	Document Number	Rev
Custom	LA-6961P	0.4

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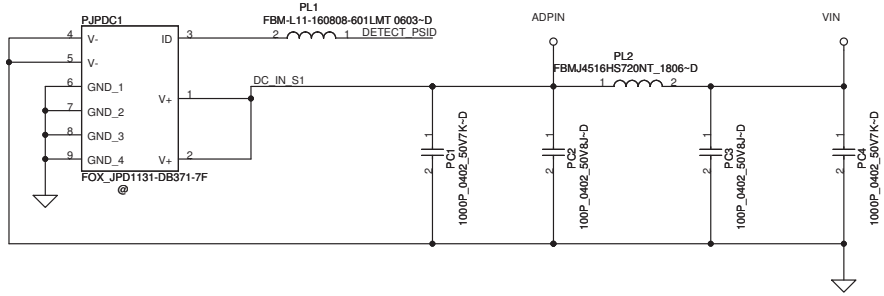
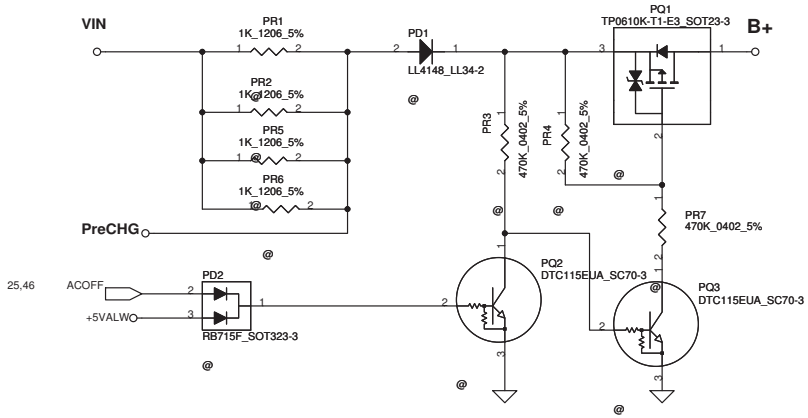
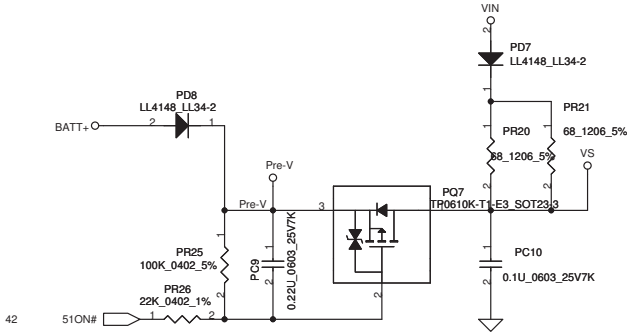
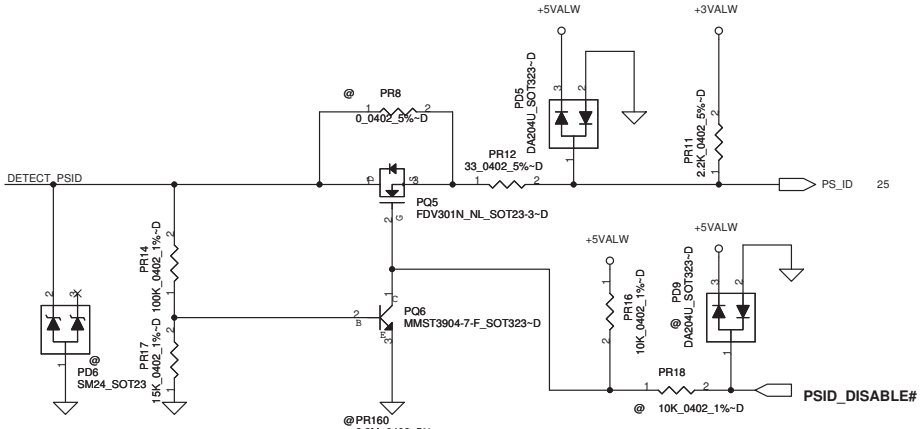
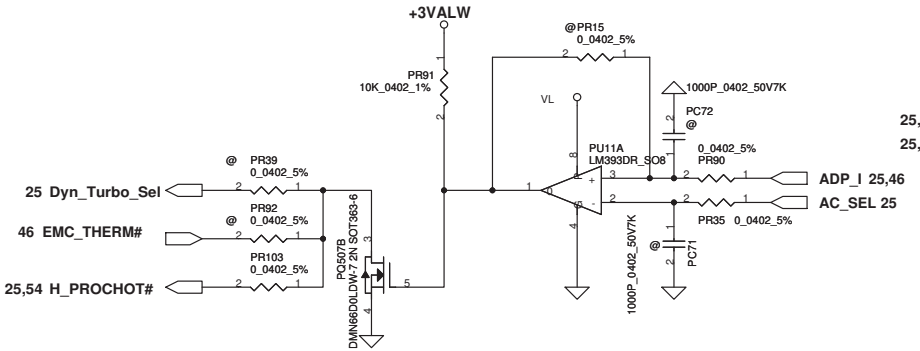
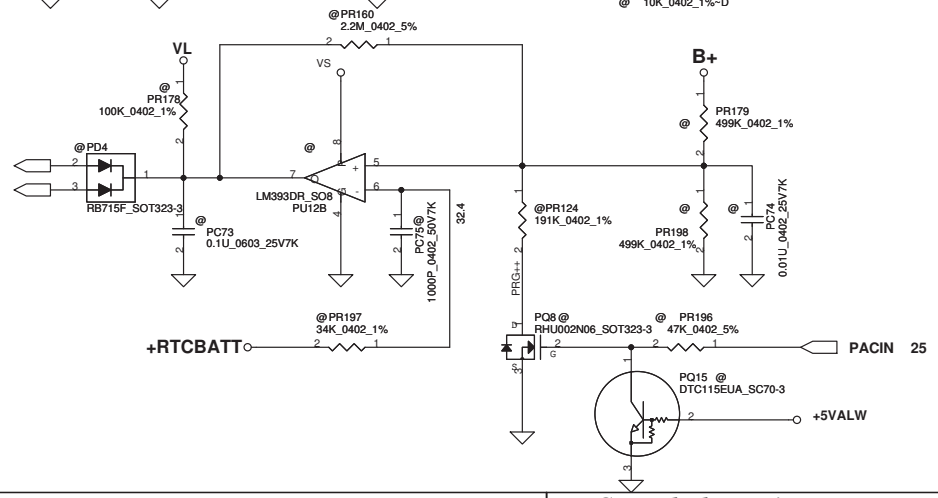






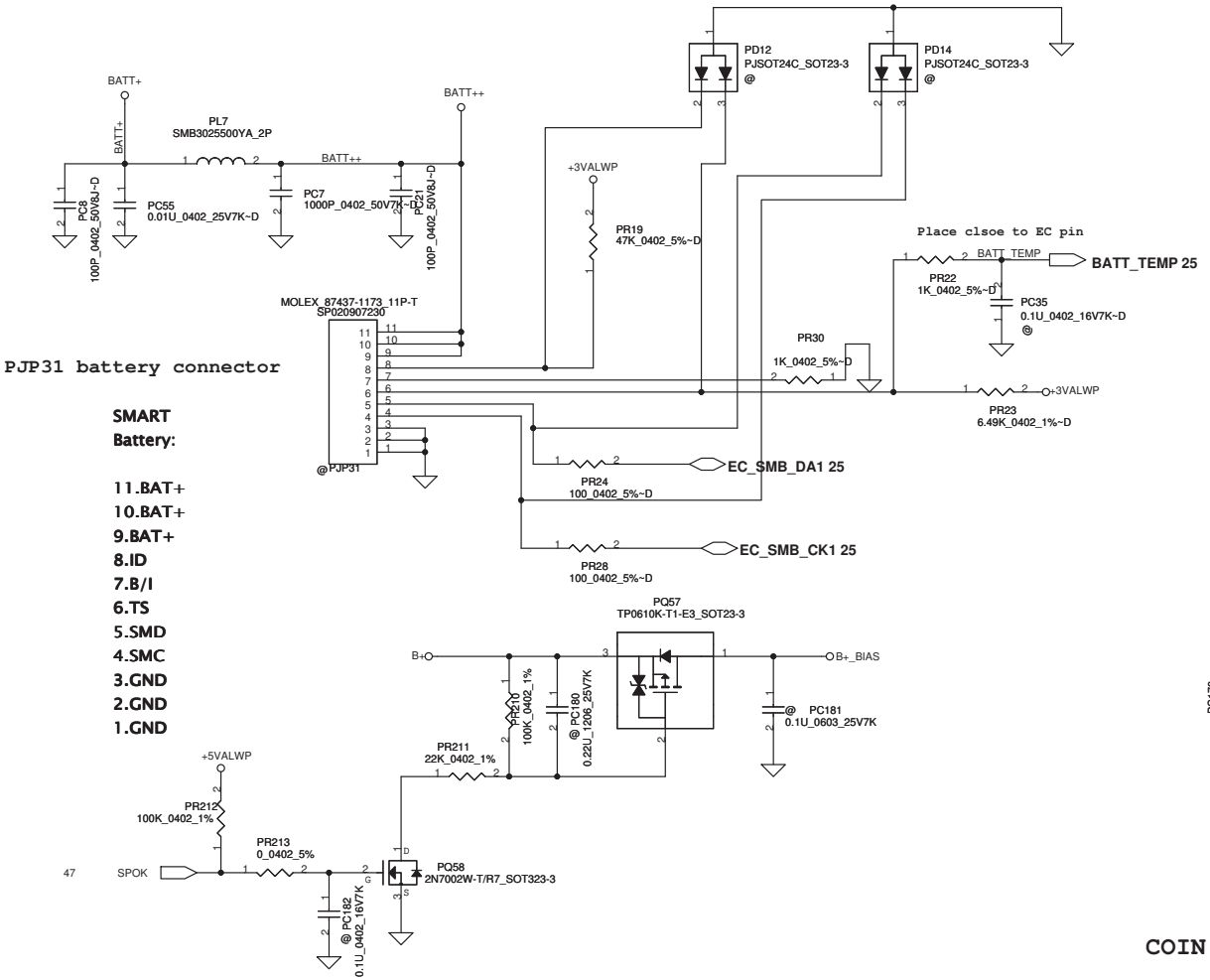






Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Compal Electronics, Inc.			
Title: PWR-DCIN / Vin Detector			
Size: Custom	Document Number: LA-6961P		Rev: 0.1
Date: Monday, January 24, 2011	Sheet 44 of 54		



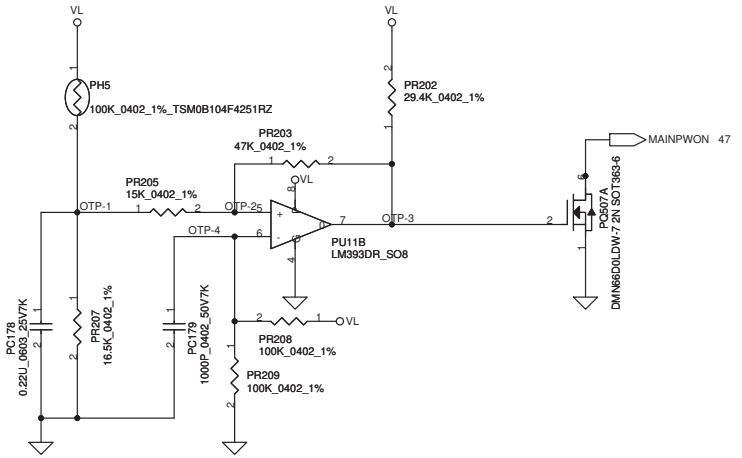
PJP31 battery connector

SMART Battery:

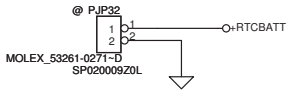
11.BAT+
10.BAT+
9.BAT+
8.ID
7.B/I
6.TS
5.SMD
4.SMC
3.GND
2.GND
1.GND

Battery Connect/OTP

PH3 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



COIN RTC Battery



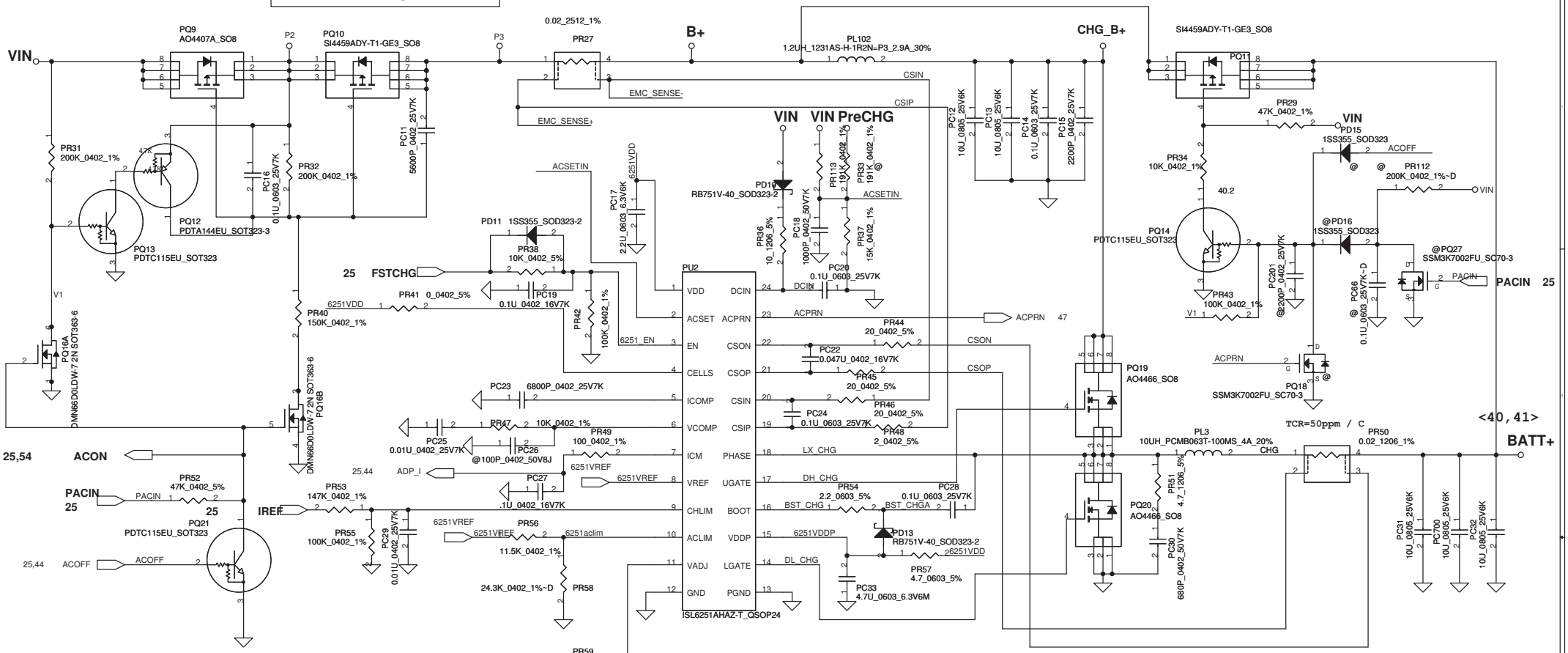
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size: Custom	Document Number: LA-6961P		Rev: 0.1
Date: Monday, January 24, 2011	Sheet 45 of 54		

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



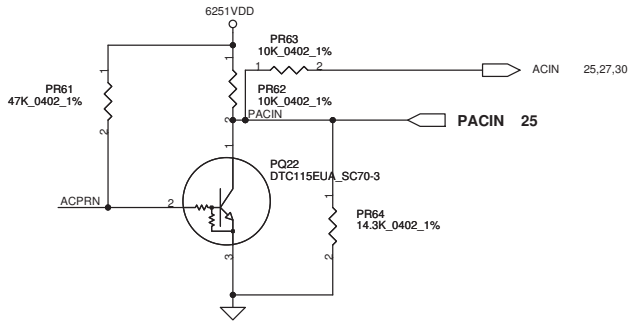
CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

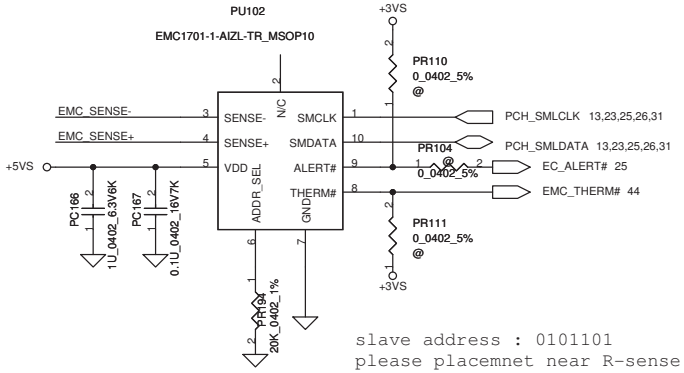
CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

add 8/17
customer request





slave address : 0101101
please placemnet near R-sense

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

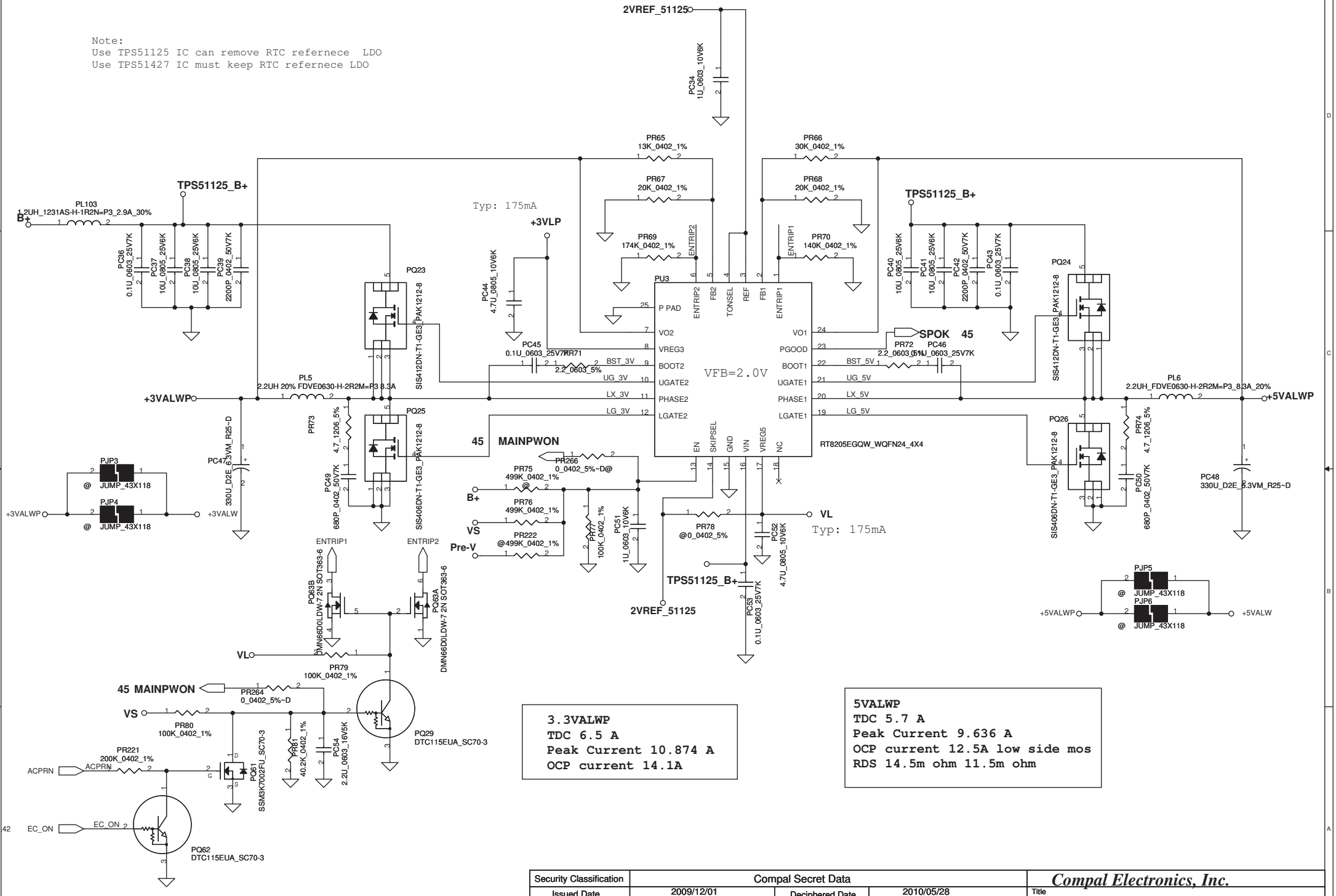
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Compal Electronics, Inc.

Title: PWR-CHARGER

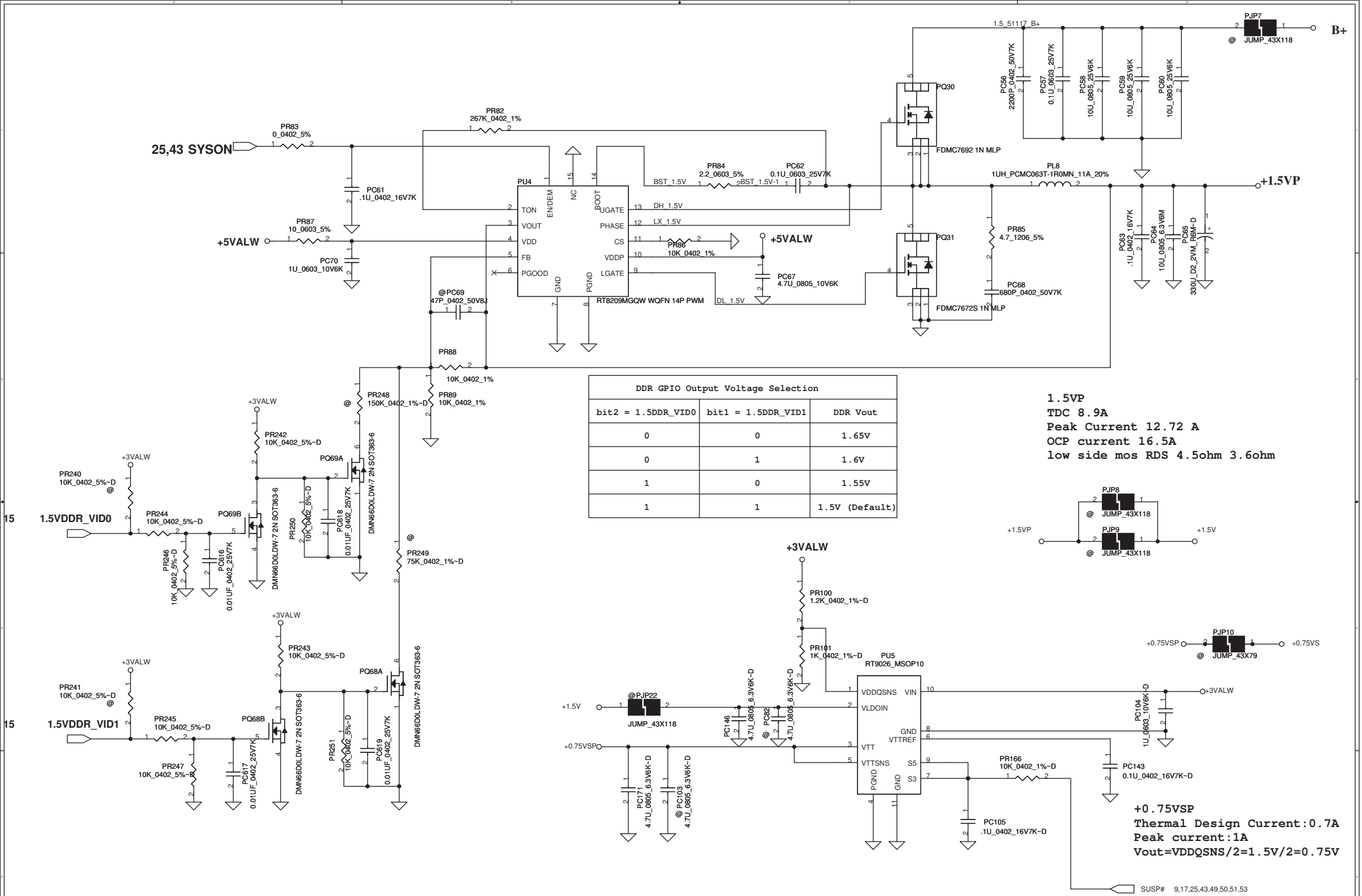
Size: Custom | Document Number: LA-6961P | Rev: 0.1

Date: Monday, January 24, 2011 | Sheet 46 of 54



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Compal Electronics, Inc.			
Title: 3VALWP/5VALWP			
Size: Custom	Document Number: LA-6961P		Rev: 0.1
Date: Monday, January 24, 2011	Sheet 47 of 54		



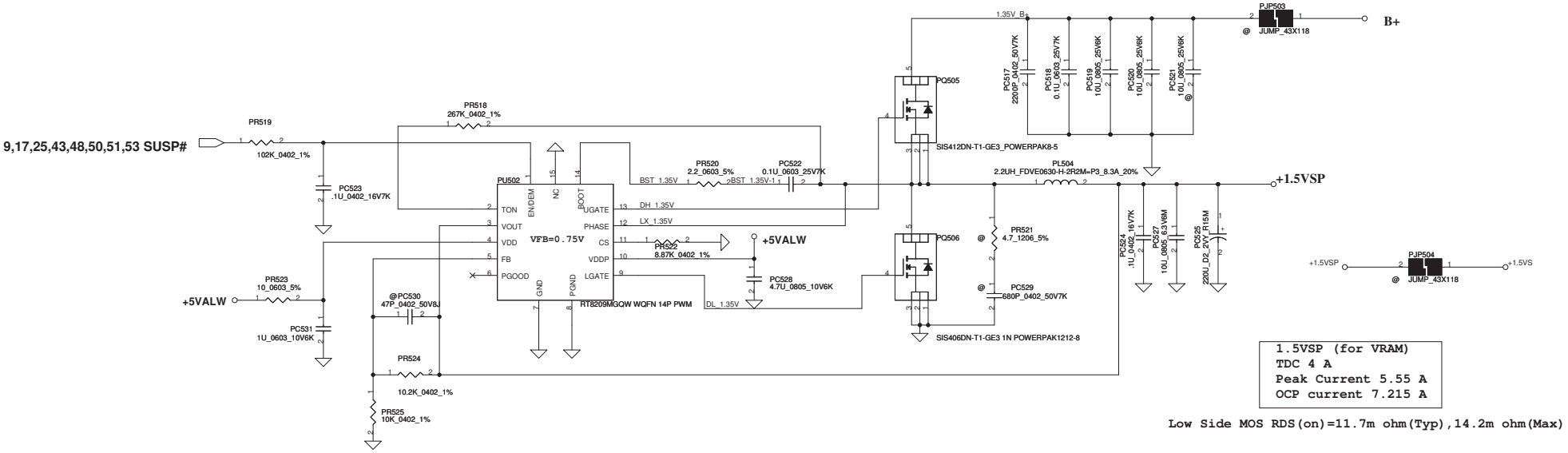
DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

1.5VP
TDC 8.9A
Peak Current 12.72 A
OCP current 16.5A
low side mos RDS 4.5ohm 3.6ohm

+0.75VSP
Thermal Design Current:0.7A
Peak current:1A
Vout=VDDQSNS/2=1.5V/2=0.75V

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Title	PWR-+1.5VP/+0.75VSP	
Size: Custom	Document Number: LA-6961P	Rev: 0.1
Date: Monday, January 24, 2011	Sheet 48 of 54	



1.5VSP (for VRAM)
TDC 4 A
Peak Current 5.55 A
OCP current 7.215 A

Low Side MOS RDS(on)=11.7m ohm(Typ),14.2m ohm(Max)

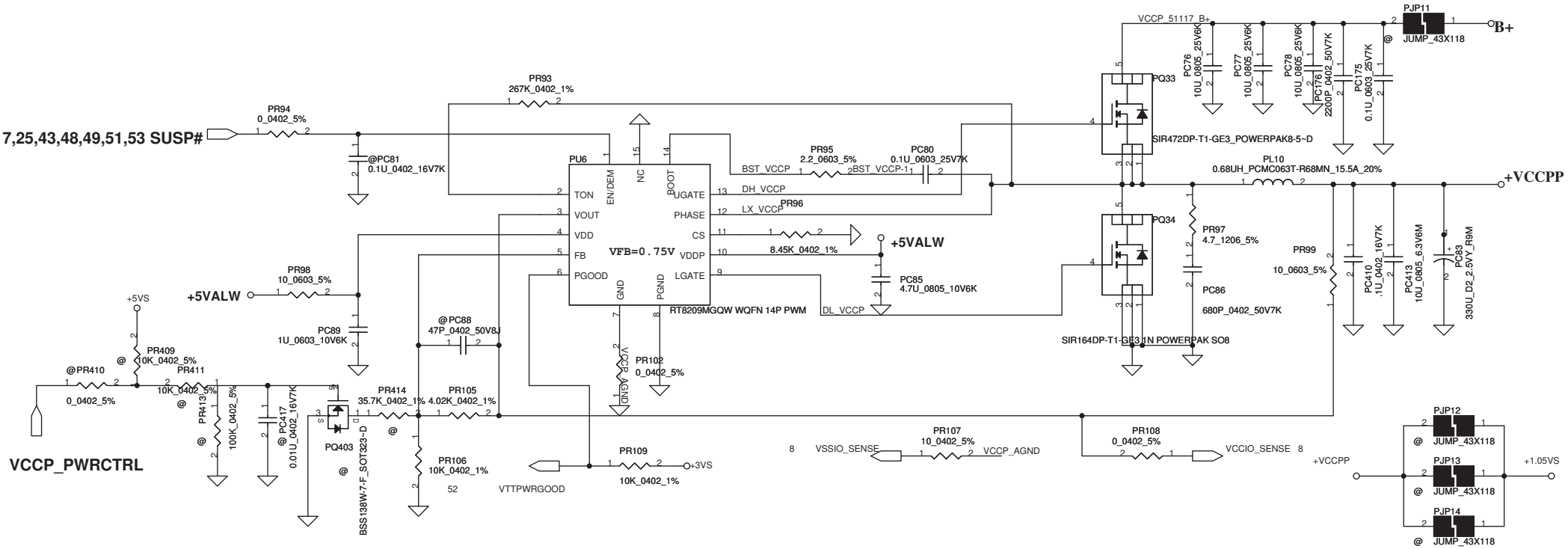
Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	2011/08/03

Compal Electronics, Inc.

Title: PWR-+VCCSAP/+1.5VSP

Size	Document Number	Rev
C	LA-6961P	0.1

Date: Monday, January 24, 2011 Sheet 49 of 54



VCCP
TDC 11.5 A
Peak Current 16.458 A
OCP 21.4 currentA
low side mos RDS 4.5 ohm(MAX)
3.6ohm(MAX)

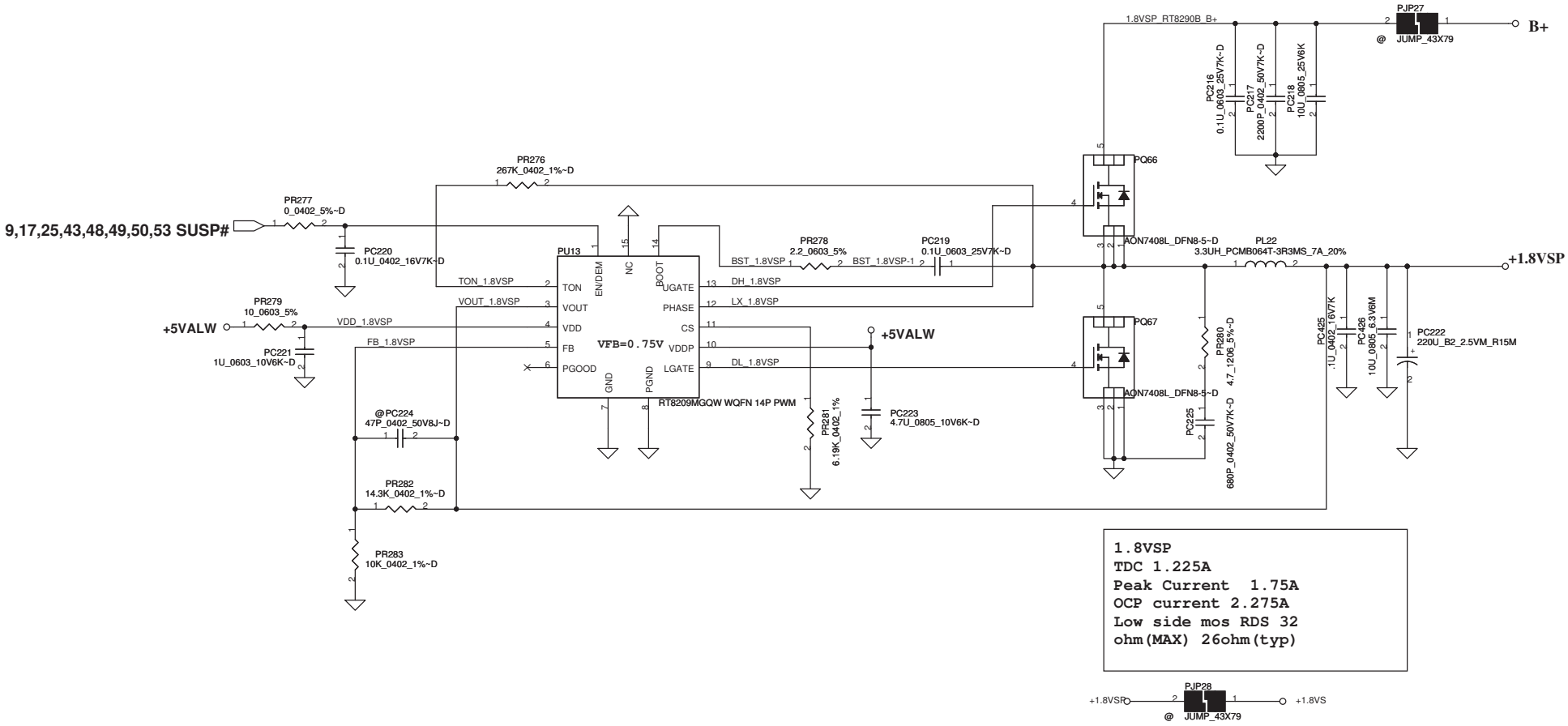
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: LA-6961P | Rev: 0.1

Date: Monday, January 24, 2011 | Sheet 50 of 54

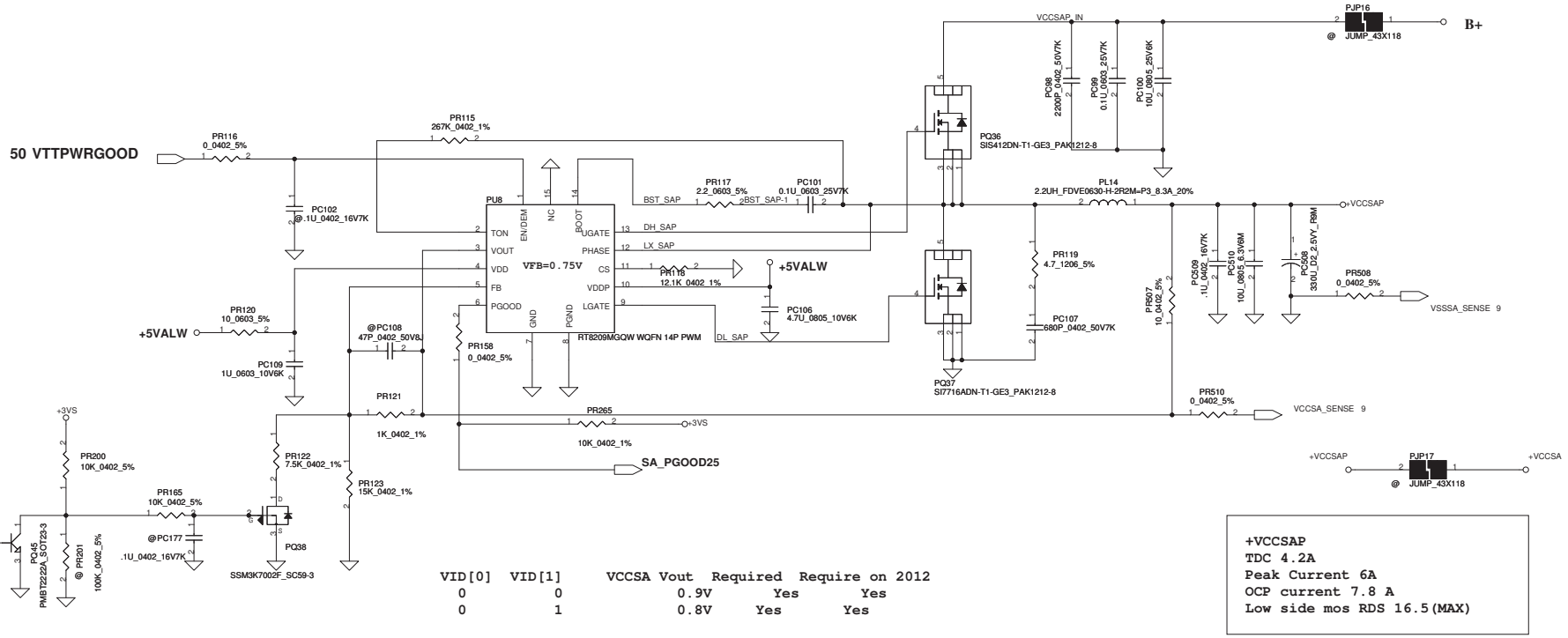


Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

Title: ***PWR-+1.8VSP***

Size	Document Number	Rev
Custom	***LA-6961P***	0.1

Date: Monday, January 24, 2011 | Sheet 51 of 54



VID[0]	VID[1]	VCCSA Vout	Required	Require on 2012
0	0	0.9V	Yes	Yes
0	1	0.8V	Yes	Yes

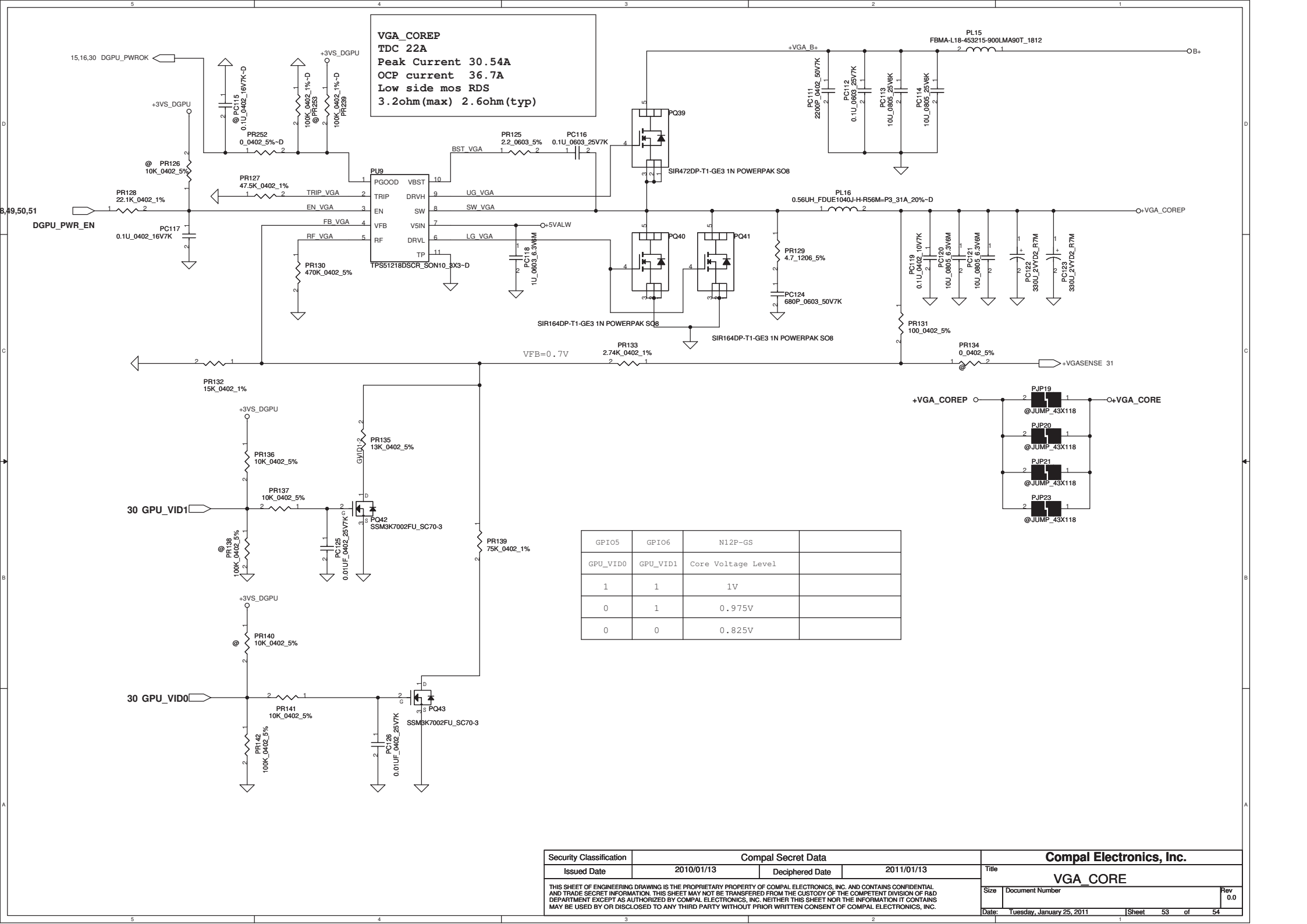
+VCCSAP
TDC 4.2A
Peak Current 6A
OCP current 7.8 A
Low side mos RDS 16.5(MAX)

Compal Electronics, Inc.

Title: PWR-VCCSA_COREP

Size	Document Number	Rev
C	LA-6761P	0.1

Date: Monday, January 24, 2011 Sheet 52 of 54



GPIO5	GPIO6	N12P-GS	
GPU_VID0	GPU_VID1	Core Voltage Level	
1	1	1V	
0	1	0.975V	
0	0	0.825V	

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: VGA_CORE

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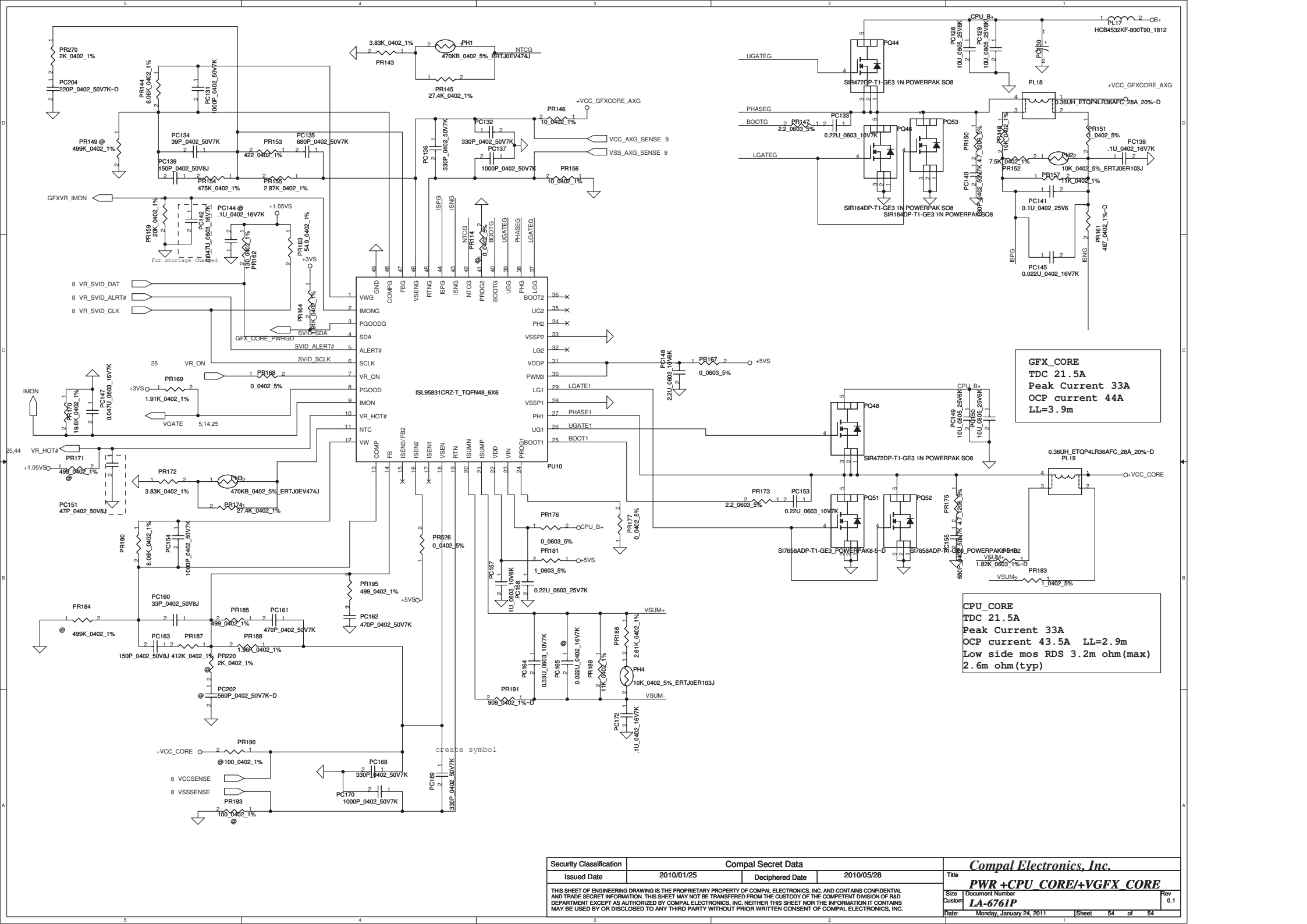

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/05/28

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

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Custom	LA-6761P	0.1

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Version change list (P.I.R. List)

EE section

Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of CL18,CL19	2010/10/15	PT
9	High pot	21	Change CL39 to SEI20102K1L	2010/10/15	PT
10	DFX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCH change version	12	Change BOM UH1 SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DG updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resister connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUO requirement	20	Add R2005,R2006 to reserve EN_INVPWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUO requirement	20	Add R2013,R2014,Q305 to reserve INVPWR_B+ Discharg Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AF1DAPA	24	Add R1962,R1963 to UPD720200AF1DAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_DGPU	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1Kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change R1095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,R1095 to 100Kohm,C287,C288, X1 resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to D7I	2010/10/26	PT
26	Intel request	12~19	Change BOM UH1 SA00004IV1L	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM C1167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SE07I200J8L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPIO14	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	1712 add D13, R395		
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Title: HW Changed-List History-1

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	LA-6961P	0.3

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