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PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2010-09-10

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: PLA00 M/B LA-6951P Schematic	Rev: 0.1
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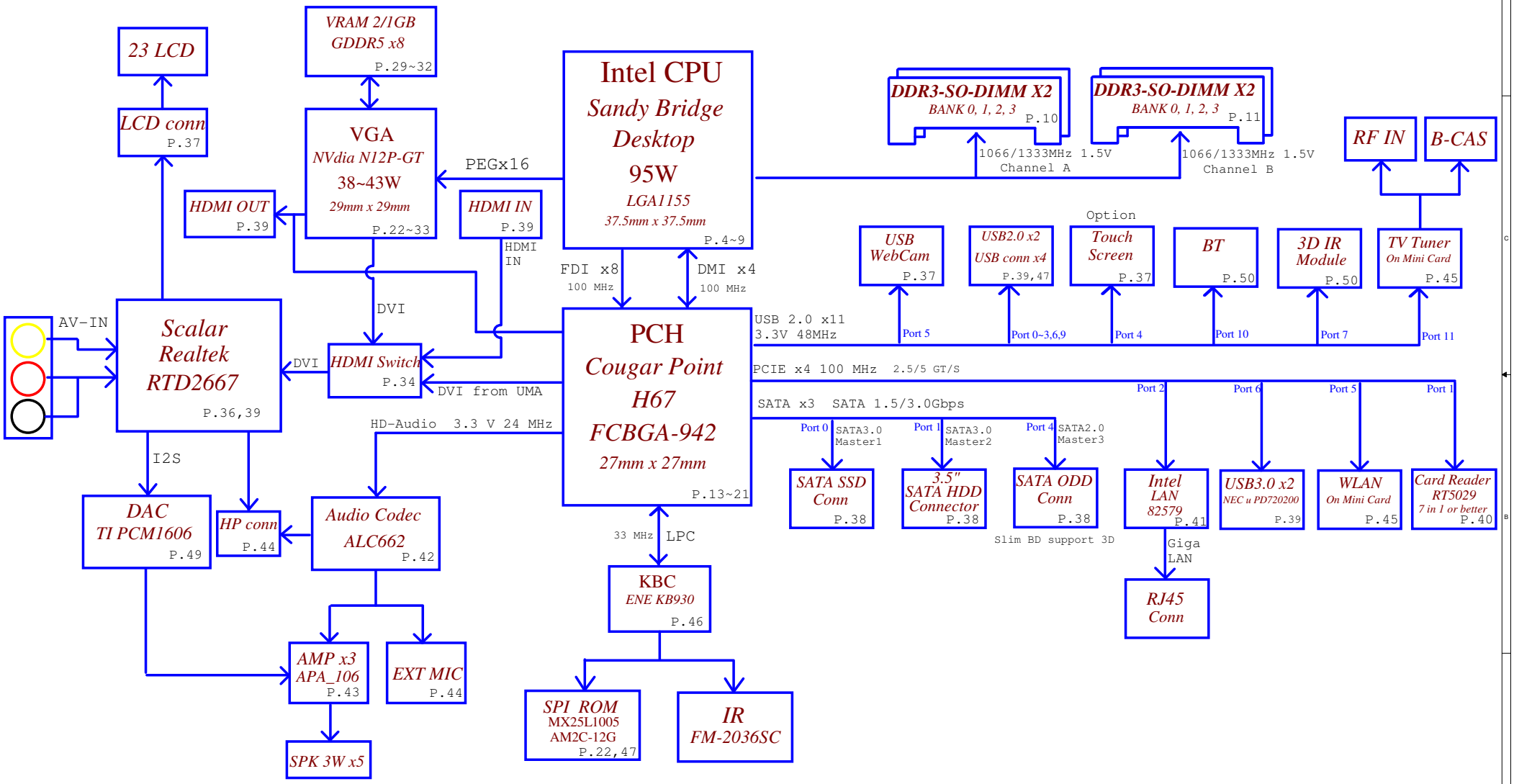
Model Name : PLA00

File Name : LA6951P



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	Block Diagrams_2D		
Size: Custom	Document Number: M/B LA-6951P Schematic		Rev: 0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	N/A	N/A	N/A
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@(VRAM:Hynix)
0	1	0	DIS@(VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
		7	3D IR
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(TV Tuner)
	UHCI6	12	Mini Car(WLAN)
		13	

BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
TAS3208	3208@
PCM1606	1606@
Samsung VRAM	X76_SAM@
Hynix VRAM	X76_HYN@
CRT	CRT@

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

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Title: Notes List

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DMI_PTX_HRX_N[0..3] <15>
DMI_PTX_HRX_P[0..3] <15>
DMI_HTX_PRX_N[0..3] <15>
DMI_HTX_PRX_P[0..3] <15>

PEG_GTX_C_HRX_P[0..15] <23>
PEG_GTX_C_HRX_N[0..15] <23>
PEG_HTX_C_GRX_P[0..15] <23>
PEG_HTX_C_GRX_N[0..15] <23>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

JCPU1C SKT_H2

<REV>

PEG

PEG_GTX_C_HRX_P15	B11	PEG_RX[0]	PEG_TX[0]	C13	PEG_HTX_GRX_P15	C1	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P15
PEG_GTX_C_HRX_N15	B12	PEG_RX#[0]	PEG_TX#[0]	C14	PEG_HTX_GRX_N15	C2	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N15
PEG_GTX_C_HRX_P14	D12	PEG_RX[1]	PEG_TX[1]	E14	PEG_HTX_GRX_P14	C3	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P14
PEG_GTX_C_HRX_N14	D11	PEG_RX#[1]	PEG_TX#[1]	E13	PEG_HTX_GRX_N14	C4	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N14
PEG_GTX_C_HRX_P13	C10	PEG_RX[2]	PEG_TX[2]	G14	PEG_HTX_GRX_P13	C5	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P13
PEG_GTX_C_HRX_N13	C9	PEG_RX#[2]	PEG_TX#[2]	G13	PEG_HTX_GRX_N13	C6	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N13
PEG_GTX_C_HRX_P12	E10	PEG_RX[3]	PEG_TX[3]	F12	PEG_HTX_GRX_P12	C7	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P12
PEG_GTX_C_HRX_N12	E9	PEG_RX#[3]	PEG_TX#[3]	F11	PEG_HTX_GRX_N12	C8	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N12
PEG_GTX_C_HRX_P11	B8	PEG_RX[4]	PEG_TX[4]	J14	PEG_HTX_GRX_P11	C9	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P11
PEG_GTX_C_HRX_N11	B7	PEG_RX#[4]	PEG_TX#[4]	J13	PEG_HTX_GRX_N11	C10	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N11
PEG_GTX_C_HRX_P10	C6	PEG_RX[5]	PEG_TX[5]	D8	PEG_HTX_GRX_P10	C11	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P10
PEG_GTX_C_HRX_N10	C5	PEG_RX#[5]	PEG_TX#[5]	D7	PEG_HTX_GRX_N10	C12	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N10
PEG_GTX_C_HRX_P9	A5	PEG_RX[6]	PEG_TX[6]	D3	PEG_HTX_GRX_P9	C13	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P9
PEG_GTX_C_HRX_N9	A6	PEG_RX#[6]	PEG_TX#[6]	C3	PEG_HTX_GRX_N9	C14	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N9
PEG_GTX_C_HRX_P8	E2	PEG_RX[7]	PEG_TX[7]	E6	PEG_HTX_GRX_P8	C15	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P8
PEG_GTX_C_HRX_N8	E1	PEG_RX#[7]	PEG_TX#[7]	E5	PEG_HTX_GRX_N8	C16	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N8
PEG_GTX_C_HRX_P7	F4	PEG_RX[8]	PEG_TX[8]	F8	PEG_HTX_GRX_P7	C17	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P7
PEG_GTX_C_HRX_N7	F3	PEG_RX#[8]	PEG_TX#[8]	F7	PEG_HTX_GRX_N7	C18	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N7
PEG_GTX_C_HRX_P6	G2	PEG_RX[9]	PEG_TX[9]	G10	PEG_HTX_GRX_P6	C19	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P6
PEG_GTX_C_HRX_N6	G1	PEG_RX#[9]	PEG_TX#[9]	G9	PEG_HTX_GRX_N6	C20	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N6
PEG_GTX_C_HRX_P5	H3	PEG_RX[10]	PEG_TX[10]	G5	PEG_HTX_GRX_P5	C21	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P5
PEG_GTX_C_HRX_N5	H4	PEG_RX#[10]	PEG_TX[11]	G6	PEG_HTX_GRX_N5	C22	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N5
PEG_GTX_C_HRX_P4	J1	PEG_RX[11]	PEG_TX#[11]	K7	PEG_HTX_GRX_P4	C23	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P4
PEG_GTX_C_HRX_N4	J2	PEG_RX#[11]	PEG_TX[12]	K8	PEG_HTX_GRX_N4	C24	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N4
PEG_GTX_C_HRX_P3	K3	PEG_RX[12]	PEG_TX#[12]	J5	PEG_HTX_GRX_P3	C25	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P3
PEG_GTX_C_HRX_N3	K4	PEG_RX#[12]	PEG_TX[13]	J6	PEG_HTX_GRX_N3	C26	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N3
PEG_GTX_C_HRX_P2	L1	PEG_RX[13]	PEG_TX#[13]	M8	PEG_HTX_GRX_P2	C27	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P2
PEG_GTX_C_HRX_N2	L2	PEG_RX#[13]	PEG_TX[14]	M7	PEG_HTX_GRX_N2	C28	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N2
PEG_GTX_C_HRX_P1	M3	PEG_RX[14]	PEG_TX#[14]	L6	PEG_HTX_GRX_P1	C29	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P1
PEG_GTX_C_HRX_N1	M4	PEG_RX#[14]	PEG_TX[15]	L5	PEG_HTX_GRX_N1	C30	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N1
PEG_GTX_C_HRX_P0	N1	PEG_RX[15]	PEG_TX#[15]	N5	PEG_HTX_GRX_P0	C31	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P0
PEG_GTX_C_HRX_N0	N2	PEG_RX#[15]		N6	PEG_HTX_GRX_N0	C32	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N0

DMI

DMI_PTX_HRX_P0	W5	DMI_RX[0]	DMI_TX[0]	V7	DMI_HTX_PRX_P0
DMI_PTX_HRX_N0	W4	DMI_RX#[0]	DMI_TX#[0]	V6	DMI_HTX_PRX_N0
DMI_PTX_HRX_P1	V3	DMI_RX[1]	DMI_TX[1]	W7	DMI_HTX_PRX_P1
DMI_PTX_HRX_N1	V4	DMI_RX#[1]	DMI_TX#[1]	W8	DMI_HTX_PRX_N1
DMI_PTX_HRX_P2	Y3	DMI_RX[2]	DMI_TX[2]	Y6	DMI_HTX_PRX_P2
DMI_PTX_HRX_N2	Y4	DMI_RX#[2]	DMI_TX#[2]	Y7	DMI_HTX_PRX_N2
DMI_PTX_HRX_P3	AA4	DMI_RX_3	DMI_TX[3]	AA7	DMI_HTX_PRX_P3
DMI_PTX_HRX_N3	AA5	DMI_RX#[3]	DMI_TX#[3]	AA8	DMI_HTX_PRX_N3

GEN

	P3	PE_RX[0]	PE_TX[0]	P8	
	P4	PE_RX#[0]	PE_TX#[0]	P7	
	R2	PE_RX[1]	PE_TX[1]	T7	
	R1	PE_RX#[1]	PE_TX#[1]	T8	
	T4	PE_RX[2]	PE_TX[2]	R6	
	T3	PE_RX#[2]	PE_TX#[2]	R5	
	U2	PE_RX[3]	PE_TX[3]	U5	
	U1	PE_RX#[3]		U6	

7/20 PE_RX[0~3]/PE_RX#[0~3] only use on Workstation.

7/20 PE_TX[0~3]/PE_TX#[0~3] only use on Workstation.

+1.05VS

24.9_0402_1% 2 1 R1 PEG_IRCOMP

B5	PEG_ICOMPO	
C4	PEG_RCOMPO	
B4	PEG_ICOMPI	

LOTES_ACAZIF096P01_SANDYBRIDGE 3 OF 11 CONN@

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)

1000P_0402_50V7K @ 2 1 C1007 H_FDI_FSYNC0
1000P_0402_50V7K @ 2 1 C1008 H_FDI_LSYNC0
1000P_0402_50V7K @ 2 1 C1009 H_FDI_FSYNC1
1000P_0402_50V7K @ 2 1 C1010 H_FDI_LSYNC1
1000P_0402_50V7K @ 2 1 C1011 H_FDI_INT

8/23 Add

H_FDI_TXN[0..7] <17>
H_FDI_TXP[0..7] <17>

JCPU1D SKT_H2

FDI_TX[0]

<17> H_FDI_FSYNC0	AC5	FDI_FSYNC_0	FDI_TX[0]	AC8	H_FDI_TXP0
<17> H_FDI_LSYNC0	AC4	FDI_LSYNC_0	FDI_TX#[0]	AC7	H_FDI_TXN0
			FDI_TX[1]	AC2	H_FDI_TXP1
			FDI_TX#[1]	AC3	H_FDI_TXN1
			FDI_TX[2]	AD2	H_FDI_TXP2
			FDI_TX#[2]	AD1	H_FDI_TXN2
			FDI_TX[3]	AD4	H_FDI_TXP3
			FDI_TX#[3]	AD3	H_FDI_TXN3
<17> H_FDI_FSYNC1	AE5	FDI_FSYNC_1	FDI_TX[4]	AD7	H_FDI_TXP4
<17> H_FDI_LSYNC1	AE4	FDI_LSYNC_1	FDI_TX#[4]	AD6	H_FDI_TXN4
			FDI_TX[5]	AE7	H_FDI_TXP5
			FDI_TX#[5]	AE8	H_FDI_TXN5
			FDI_TX[6]	AF3	H_FDI_TXP6
			FDI_TX#[6]	AF2	H_FDI_TXN6
			FDI_TX[7]	AG2	H_FDI_TXP7
			FDI_TX#[7]	AG1	H_FDI_TXN7
<17> H_FDI_INT	AG3	FDI_INT			
			FDI LINK		
+1.05VS 24.9_0402_1% 2 1 R2	AE2	FDI_ICOMP			
	AE1	FDI_COMPIO			
		FDI_ICOMPO			

LOTES_ACAZIF096P01_SANDYBRIDGE 4 OF 11 CONN@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.1

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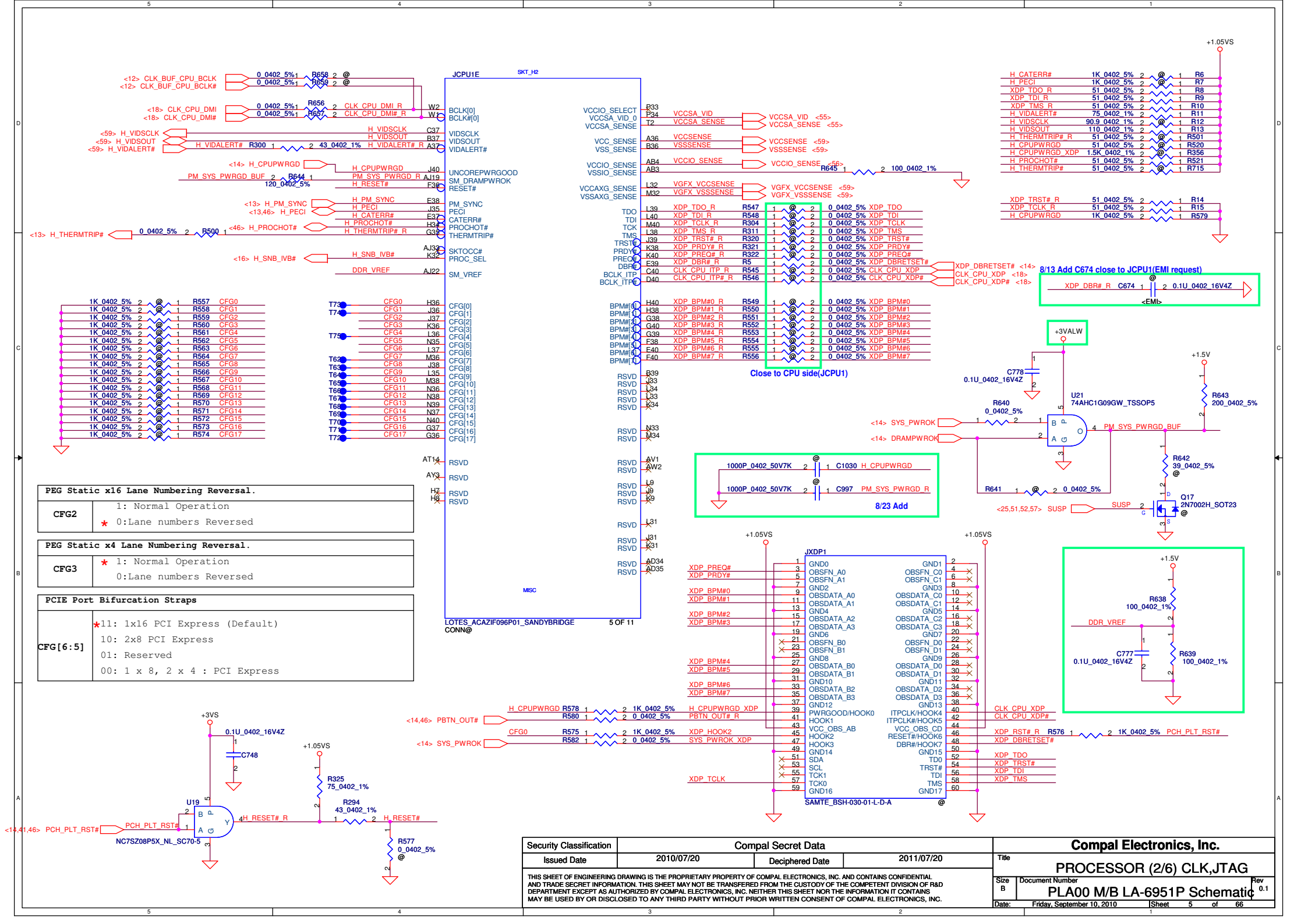

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.1

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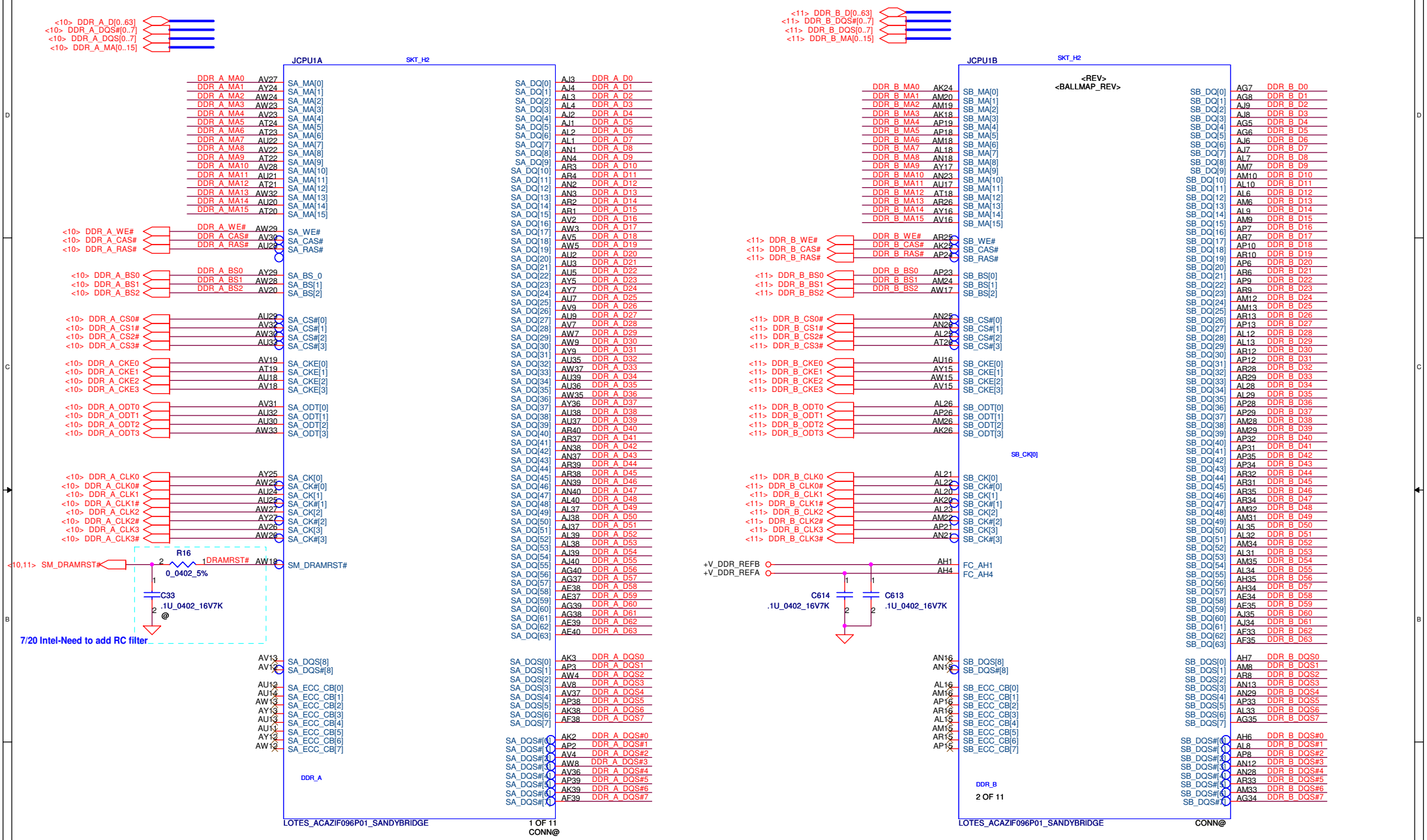

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.1

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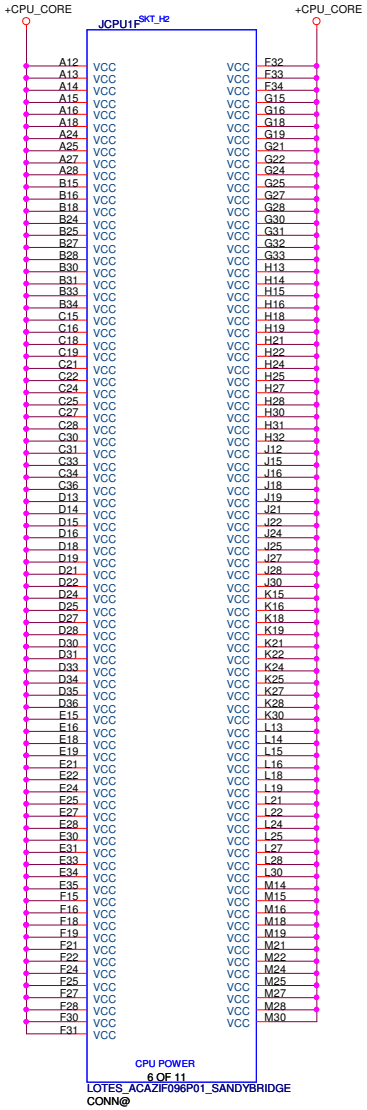
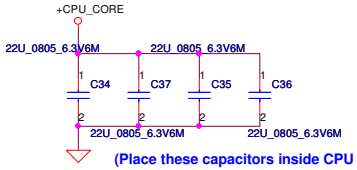
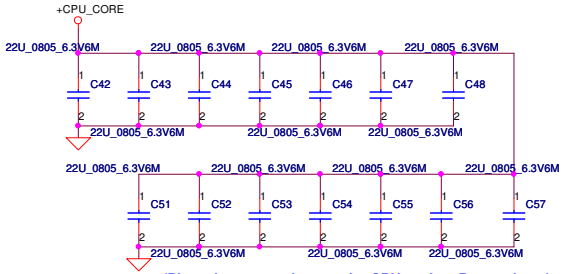
+CPU_CORE : 112A



+CPU_CORE

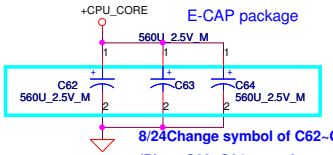


(Place these capacitors inside CPU socket cavity, top layer)



(Place these capacitors under CPU socket, Bottom layer)

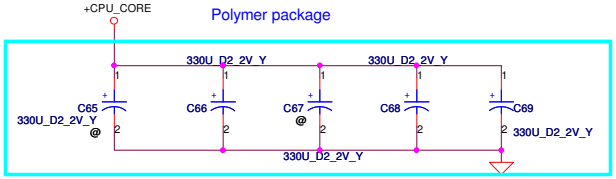
E-CAP package



8/24Change symbol of C62~C63 from SF000001P00 to SF000001K00

(Place C62~C64 capacitors under CPU socket, Top layer)

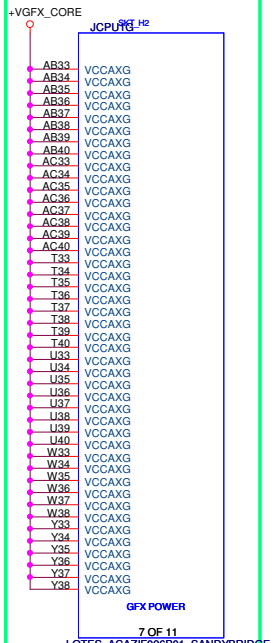
Polymer package



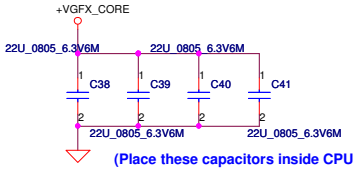
8/24Change symbol of C66~C69 from SF000002O00 to SGA20331E10
8/24Change symbol of C65 from SF000001P00 to SGA20331E10

(Place C65~C69 capacitors under CPU socket, Bottom layer)

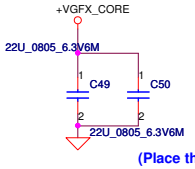
+VGFX_CORE : 35A



+VGFX_CORE

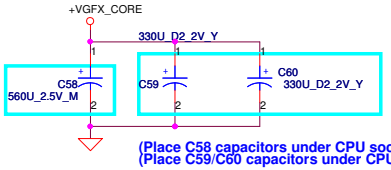


(Place these capacitors inside CPU socket cavity, top layer)



(Place these capacitors under CPU socket, Bottom layer)

E-CAP package



(Place C58 capacitors under CPU socket, Top layer)
(Place C59/C60 capacitors under CPU socket, Bottom layer)

8/24Change symbol of C58 from SF000001P00 to SF000001K00
8/24Change symbol of C59/C60 from SF000001P00 to SGA20331E10

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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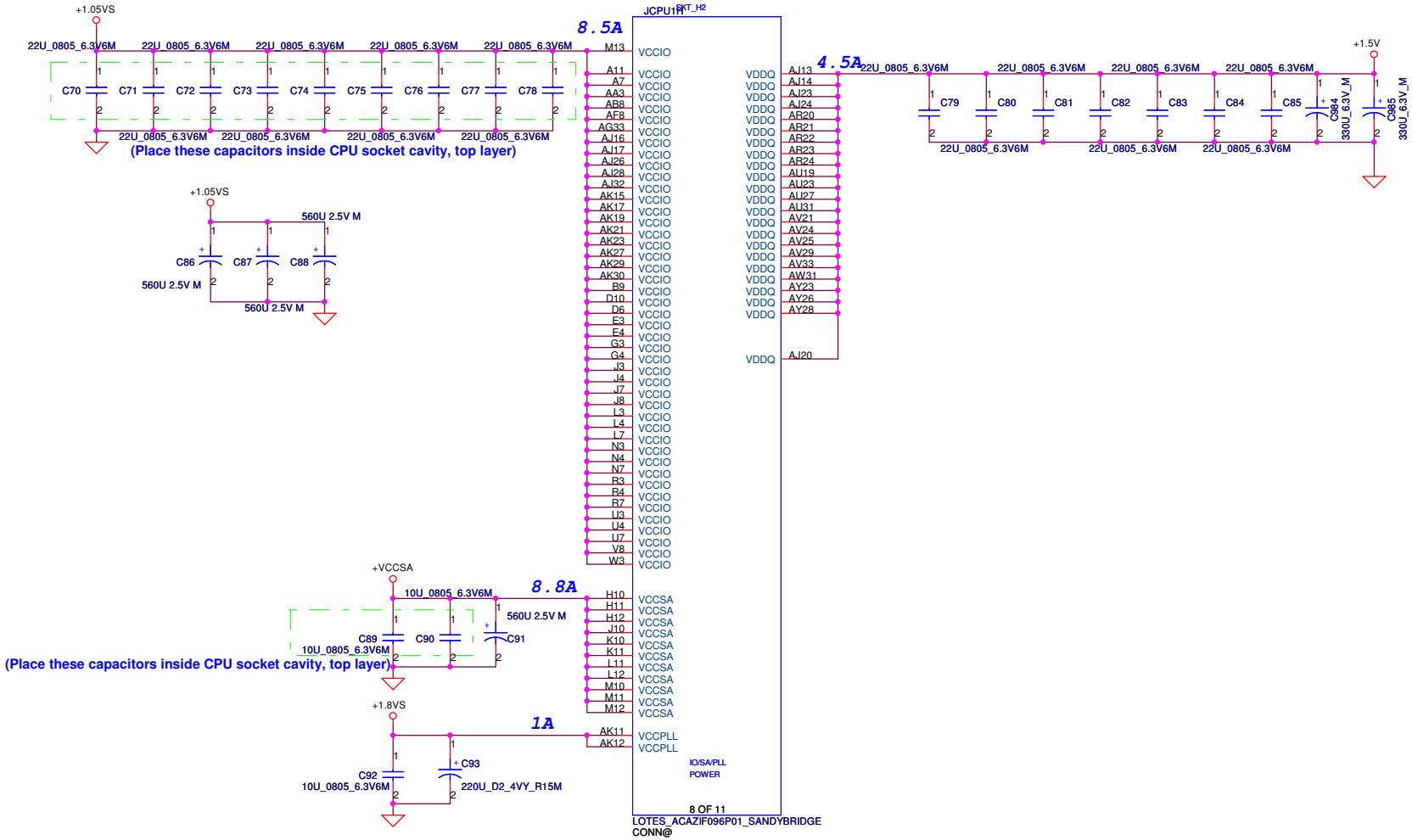


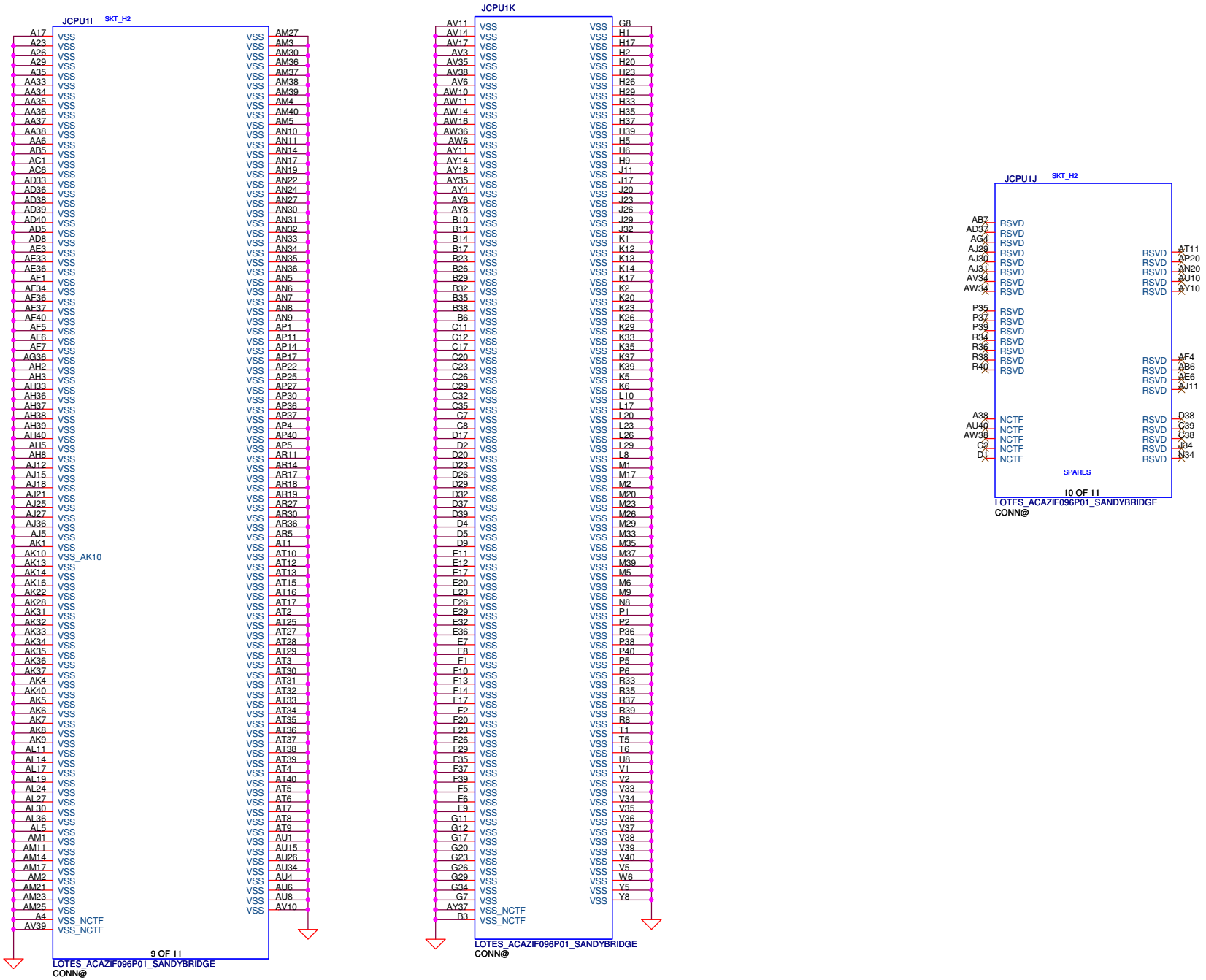
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 | Sheet 8 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 Sheet 9 of 66

Layout Note:Place C94 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMA

Layout Note: Place near JDIMMA

Layout Note:Place near JDIMM1.203/204

Layout Note:Place near JDIMM2.203/204

JDIMM1

JDIMM2

SUYIN_600023HB204G208ZL
CONN@

FOX_AS0A626-U2SN-7F
CONN@

STANDARD:9.2mm

STANDARD:5.2mm

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: DDRIII CHANNELA

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 10 of 66

Layout Note:Place C124 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMB

Layout Note: Place near JDIMMB

Layout Note:Place near JDIMM4.203/204

Layout Note:Place near JDIMM3.203/204

JDIMM4

JDIMM3

FOX_AS0A626-U2RN-7F
CONN@

FOX_AS0A626-UARN-7F
CONN@

<Address: 01>

Reverse H:5.2mm

Reverse H:9.2mm

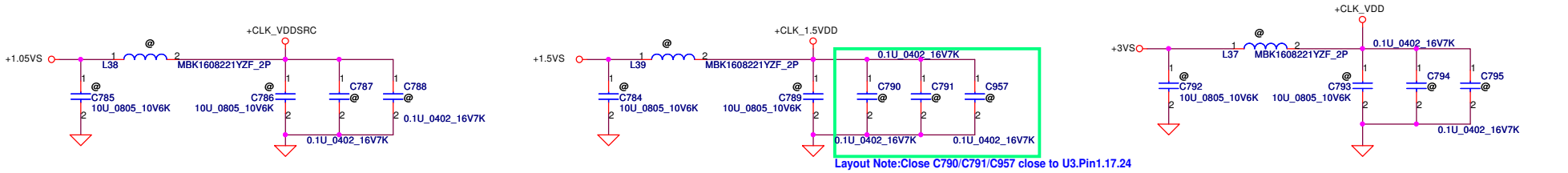
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

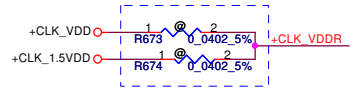
Title: DDRIII CHANNELB

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

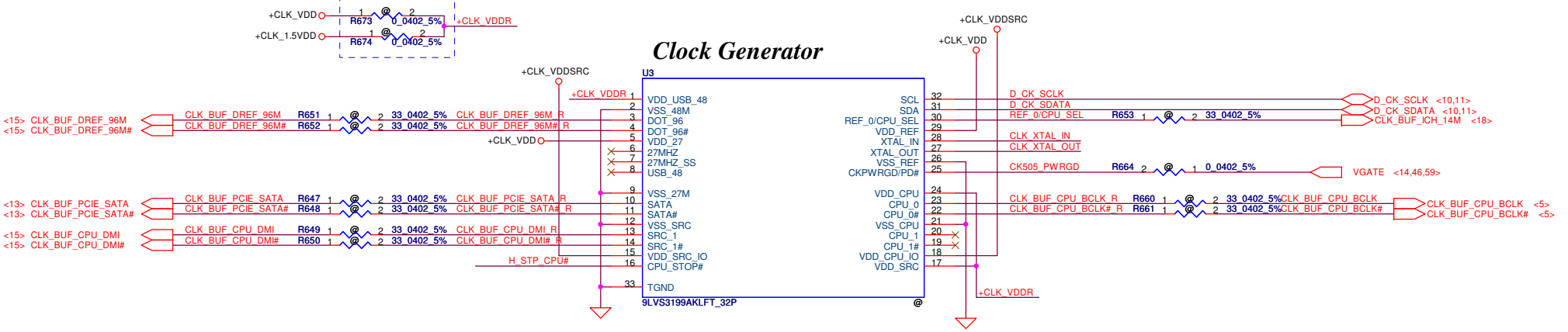
Date: Friday, September 10, 2010 | Sheet 11 of 66



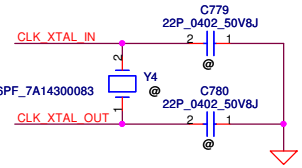
Layout Note:Close C790/C791/C957 close to U3.Pin1.17.24

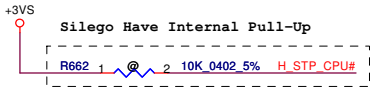


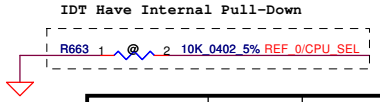
Clock Generator



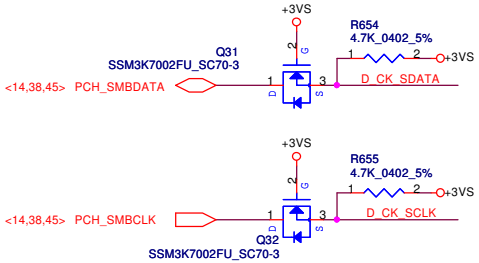
LOW Power:
Realtek: RTM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00







PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



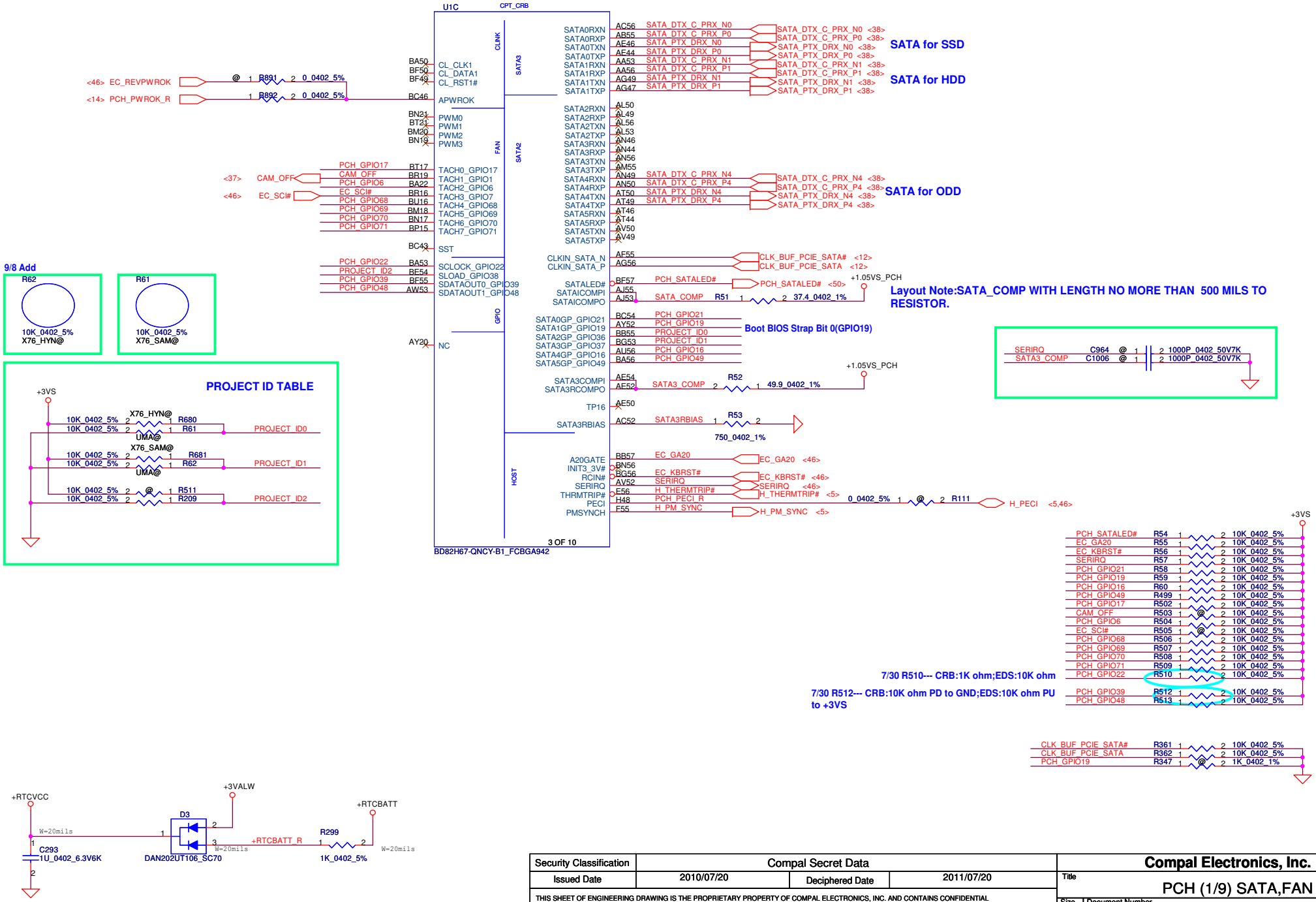
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 12 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (1/9) SATA,FAN

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 Sheet 13 of 66

HDA for AUDIO

<42> HDA_BITCLK_AUDIO — R69 33_0402_5% — HDA_BITCLK_PCH
<42> HDA_RST#_AUDIO — R72 33_0402_5% — HDA_RST#_PCH
<42> HDA_SDOUT_AUDIO — R73 33_0402_5% — HDA_SDOUT_PCH

HDA_SDO

ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC

This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
*Need to pull high for Huron River platform

+3VALW — R392 1K_0402_5% — HDA_SYNC_PCH
+3VS — Q21 BSS138_NL_SOT23-3
<42> HDA_SYNC_AUDIO — R70 33_0402_5% — HDA_SYNC_AUDIO_R
R393 0_0402_5%

PCH_RSMRST# — R303 0_0402_5% — PCH_DPWROK
Stuff R303 if do not support DeepSX state

EC_PWROK — R344 0_0402_5% — PCH_PWROK_R

<46> LPC_AD0 — LPC_AD0 — BA20
<46> LPC_AD1 — LPC_AD1 — BJ17
<46> LPC_AD2 — LPC_AD2 — BJ20
<46> LPC_AD3 — LPC_AD3 — BG20
<46> LPC_FRAME# — LPC_FRAME# — BK17 / BG17
HDA_BITCLK_PCH — BJ22
HDA_RST# PCH — BC22
<42> HDA_SDIN0 — HDA_SDIN0 — BD22
BF22
+3VALW — R338 1K_0402_1% — BK22
<46> ME_FLASH — R890 0_0402_5% — HDA_SDOUT_PCH — BJ22
HDA_SYNC_PCH — BT23
BP23

PCH_SPI_MOSI_1 — R79 0_0402_5% — PCH_SPI_MOSI — AU53
PCH_SPI_MISO_1 — R80 0_0402_5% — PCH_SPI_MISO — AT55
PCH_SPI_CS0# — R81 0_0402_5% — PCH_SPI_CS0#_R — AT57
PCH_SPI_CLK_1 — R83 0_0402_5% — PCH_SPI_CLK — AR54
AR56

+3VALW
2.2K_0402_5% — R945 — PCH_SMBCLK
2.2K_0402_5% — R946 — PCH_SMBDATA

PCH_RTCX1 — BR39
PCH_RTCX2 — BN39
PCH_RTCRST# — BT41
PCH_SRTCRST# — BN37
SM_INTRUDER# — BM38
PCH_PWROK_R — BJ38
PCH_RSMRST# — BK38
PCH_INTVRMEN — BN41
PCH_DPWROK — BT37
PCH_DSWVRMEN — BR42

PCH_GPIO11 — BN49
<12,38,45> PCH_SMBCLK — PCH_SMBCLK — BT47
<12,38,45> PCH_SMBDATA — PCH_SMBDATA — BR49
PCH_GPIO60 — BU49
<41> LAN_SMBCLK — LAN_SMBCLK — BT51
<41> LAN_SMBDATA — LAN_SMBDATA — BM50
PCH_GPIO74 — BR46
<22,43,46> EC_SMB_CK2 — EC_SMB_CK2 — R88 0_0402_5% — PCH_SML1CLK — BJ46
<22,43,46> EC_SMB_DA2 — EC_SMB_DA2 — R89 0_0402_5% — PCH_SML1DAT — BK46

C146 18P_0402_50V8J — PCH_RTCX1
X1 32.768KHZ_12.5PF_Q13MC14610002
R87 10M_0402_5%
C147 18P_0402_50V8J — PCH_RTCX2

+RTCVCC — R90 20K_0402_1% — PCH_RTCRST#
close to RAM door — J1 10K_0603_5% — C148 1U_0402_6.3V6K
RC Delay 18~25mS

+RTCVCC — R99 20K_0402_1% — PCH_SRTCRST#
close to RAM door — J2 10K_0603_5% — C149 1U_0402_6.3V6K
RC Delay 18~25mS

+RTCVCC
1M_0402_5% — R103 — SM_INTRUDER#
390K_0402_5% — R104 — PCH_DSWVRMEN
390K_0402_5% — R105 — PCH_INTVRMEN
R106 1K_0402_5%

8/20 Add
1000P_0402_50V7K — C987 — LAN_CLKREQ#
1000P_0402_50V7K — C988 — PCH_JTAG_TDO

8/19 Change footprint of U2 to WIESO_G6179-100000_8P

+3VS
R94 4.7K_0402_5% — PCH_SPI_CS0# — SPI_WP1#
R96 4.7K_0402_5% — SPI_HOLD1#

SA000041P00 4MB
U2
CS# VCC 8 — PCH_SPI_CLK_1
WP# SCLK 6 — PCH_SPI_MOSI_1
HOLD# SI 5 — PCH_SPI_MISO_1
GND SO 2
S IC FL 32M MX25L3206EM2I-12G SOP 8P
SPI ROM Footprint 200mil

R348 0_0402_5%
+3VS
U20 NC7SZ08P5X_NL_SC70-5
<5> SYS_PWROK — SYS_PWROK — EC_PWROK — EC_PWROK <46>
VGATE — VGATE <12,46,59>

R943 0_0402_5%
+3VS
U25 NC7SZ08P5X_NL_SC70-5
PCH_PLT_RST# — PLT_RST# — PLT_RST# <23,39,40,45>
R944 100K_0402_5%

SYS_PWROK_R — R349 0_0402_5% — SYS_PWROK
R350 0_0402_5% — VGATE

U1D
LDRQ1#_GPIO23 — BA20
FWH0_LAD0 — BK15
FWH1_LAD1 — BJ17
FWH2_LAD2 — BJ20
FWH3_LAD3 — BG20
LDRQ0# — BK17
FWH4_LFRAME# — BG17
HDA_BCLK — BJ22
HDA_RST# — BC22
HDA_SDIN0 — BD22
HDA_SDIN1 — BF22
HDA_SDIN2 — BK22
HDA_SDIN3 — BJ22
HDA_SDO — BT23
HDA_SYNC — BP23
SPI_MOSI — AU53
SPI_MISO — AT55
SPI_CS0# — AT57
SPI_CLK — AR54
SPI_CS1# — AR56
RTCX1 — BR39
RTCX2 — BN39
RTCRST# — BT41
SRTCRST# — BN37
INTRUDER# — BM38
PWROK — BJ38
RSMRST# — BK38
INTVRMEN — BN41
DPWROK — BT37
DSWVRMEN — BR42
SMBALERT#_GPIO11 — BN49
SMBCLK — BT47
SMBDATA — BR49
SML0ALERT#_GPIO60 — BU49
SML0CLK — BT51
SML0DATA — BM50
SML1ALERT#_PCHHOT#_GPIO74 — BR46
SML1CLK_GPIO58 — BJ46
SML1DATA_GPIO75 — BK46
4 OF 10
BD82H67-QNCY-B1_FCBGA942

BMBUSY#_GPIO0 — AW55 — PCH_GPIO0
CLKRUN#_GPIO32 — BC56 — CLKRUN# — CLKRUN# <46>
HDA_DOCK_EN#_GPIO33 — BC25 — PCH_GPIO33
STP_PCI#_GPIO34 — BL56 — PCH_GPIO34
GPIO35 — BJ57 — PCH_GPIO35
GPIO8 — BP51 — EC_SMI# — EC_SMI# <39,46>
LAN_PHY_PWR_CTRL_GPIO12 — BK50 — PM_LANPHY_ENABLE — PM_LANPHY_ENABLE <41>
HDA_DOCK_RST#_GPIO13 — BA25 — PCH_GPIO13
GPIO15 — BM55 — SMIB — SMIB <39>
GPIO24_MEM_LED — BP53 — T1
GPIO28 — BJ55 — PCH_GPIO28
SLP_LAN#_GPIO29 — BH49 — SLP_LAN# — SLP_LAN# <41>
PCIECLKRQ2#_GPIO20 — AV43 — LAN_CLKREQ# — LAN_CLKREQ# <41>
PCIECLKRQ5#_GPIO44 — BL54 — WLAN_CLKREQ# — WLAN_CLKREQ# <45>
PCIECLKRQ6#_GPIO45 — AV44 — CLKREQ_USB30# — CLKREQ_USB30# <39>
PCIECLKRQ7#_GPIO46 — BP55 — TV_CLKREQ# — TV_CLKREQ# <45>
GPIO57 — BT53 — PCH_GPIO57
SYS_PWROK — BJ53 — SYS_PWROK_R
RI# — BJ48 — EC_SWI# — EC_SWI# <46>
PLTRST# — BK48 — PCH_PLT_RST# — PCH_PLT_RST# <5,41,46>
WAKE# — BC44 — PCH_PCIE_WAKE# — R364 0_0402_5% — PCH_PCIE_WAKE# <39,45>
SLP_A# — BC41
SLP_S3# — BM53 — PM_SLP_S3# — PM_SLP_S3# <46>
SLP_S4# — BN52 — PM_SLP_S4# — PM_SLP_S4# <46>
SLP_S5#_GPIO63 — BH50 — PM_SLP_S5# — PM_SLP_S5# <46>
SUS_STAT#_GPIO61 — BN54 — T2
SUSCLK_GPIO62 — BA47 — PCH_SUSCLK_R — R363 0_0402_5% — PCH_SUSCLK <46>
BATLOW#_GPIO72 — AV46 — PCH_GPIO72
SUSACK# — BP45 — SUS_PWR_ACK_R — R365 0_0402_5% — SUS_PWR_ACK <46>
SUSWARN#-SUS_PWR_DN_ACK-GPIO30 — BU46 — SUSWARN#_R — R390 0_0402_5% — SUSWARN# <46>
DRAMPWROK — BG46 — DRAMPWROK — DRAMPWROK <5>
GPIO27 — BJ43 — PCH_GPIO27
GPIO31 — BG43 — PCH_GPIO31
SLP_SUS# — BD43 — T51
PWRBTN# — BT43 — PBTN_OUT# — PBTN_OUT# <5,46>
SYS_RESET# — BE52 — XDP_DBRETSET# — XDP_DBRETSET# <5>
SPKR — BE56 — PCH_SPKR — PCH_SPKR <42>
PROCPWRGD — D53 — H_CPUPWRGD — H_CPUPWRGD <5>
TP12 — BC49 — PCH_JTAG_RST#
JTAG_TCK — BA43 — PCH_JTAG_TCK
JTAG_TDI — BC52 — PCH_JTAG_TDI
JTAG_TDO — BF47 — PCH_JTAG_TDO
JTAG_TMS — BC50 — PCH_JTAG_TMS

+3VALW
EC_SMI# — R324 10K_0402_5%
EC_SWI# — R74 10K_0402_5%
PCH_GPIO74 — R75 10K_0402_5%
PCH_SML1CLK — R63 2.2K_0402_5%
PCH_SML1DAT — R76 2.2K_0402_5%
LAN_SMBCLK — R64 2.2K_0402_5%
LAN_SMBDATA — R65 2.2K_0402_5%
PCH_GPIO60 — R77 2.2K_0402_5%
PM_LANPHY_ENABLE — R66 10K_0402_5%
SMIB — R67 10K_0402_5%
PCH_GPIO28 — R68 1K_0402_1%
PCH_GPIO13 — R896 10K_0402_5%
SUSWARN#_R — R448 10K_0402_5%
PCH_GPIO57 — R71 10K_0402_5%
PCH_GPIO27 — R78 10K_0402_5%
WLAN_CLKREQ# — R530 10K_0402_5%
CLKREQ_USB30# — R531 10K_0402_5%
TV_CLKREQ# — R532 10K_0402_5%
DRAMPWROK — R646 200_0402_5%
PCH_GPIO31 — R675 10K_0402_5%
PCH_GPIO72 — R676 200_0402_5%
PCH_PCIE_WAKE# — R203 1K_0402_1%
PCH_GPIO11 — R716 10K_0402_5%

SUS_PWR_ACK_R — R391 0_0402_5% — SUSWARN#_R
Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit

+3VS
PCH_GPIO33 — R894 10K_0402_5%
PCH_GPIO0 — R82 10K_0402_5%
PCH_GPIO34 — R84 10K_0402_5%
LAN_CLKREQ# — R529 10K_0402_5%
XDP_DBRETSET# — R581 10K_0402_5%
PCH_SPKR — R583 1K_0402_5%
PCH_SPKR:HIGH= Enable (No Reboot);
* LOW= Disable(Default)

CLKRUN# — R926 10K_0402_5%
SLP_LAN# — R897 1K_0402_1%
PCH_GPIO33 — R895 1K_0402_1%
SYS_PWROK — R719 10K_0402_5%
PCH_GPIO35 — R85 2.2K_0402_5%
EC_SMI# — R86 1K_0402_1%
SUSWARN#_R — R207 1K_0402_1%
EC_PWROK — R718 10K_0402_5%
PCH_GPIO28 — R340 1K_0402_1%
* On-Die PLL Voltage Regulator
H: Enable
L: Disable

XDP_DBRETSET# — C676 0.1U_0402_16V4Z — <EMI>
8/13 Add C676 close to U1(EMI request)

R342 0_0402_5%
Q18 MMBT3906_SOT23-3
PCH_RSMRST# — EC_RSMRST# <46>
R717 10K_0402_5%
R319 4.7K_0402_5% — +3VALW
D38A
D38B
BAV99DW-7-F_SOT363-N
R343 2.2K_0402_5%

+3VALW
PCH_JTAG_TMS — R91 200_0402_5% — R92 100_0402_5%
PCH_JTAG_TDO — R93 200_0402_5% — R95 100_0402_5%
PCH_JTAG_TDI — R97 200_0402_5% — R98 100_0402_5%
PCH_JTAG_RST# — R100 20K_0402_5% — R101 10K_0402_5%
PCH_JTAG_TCK — R102 51_0402_5%

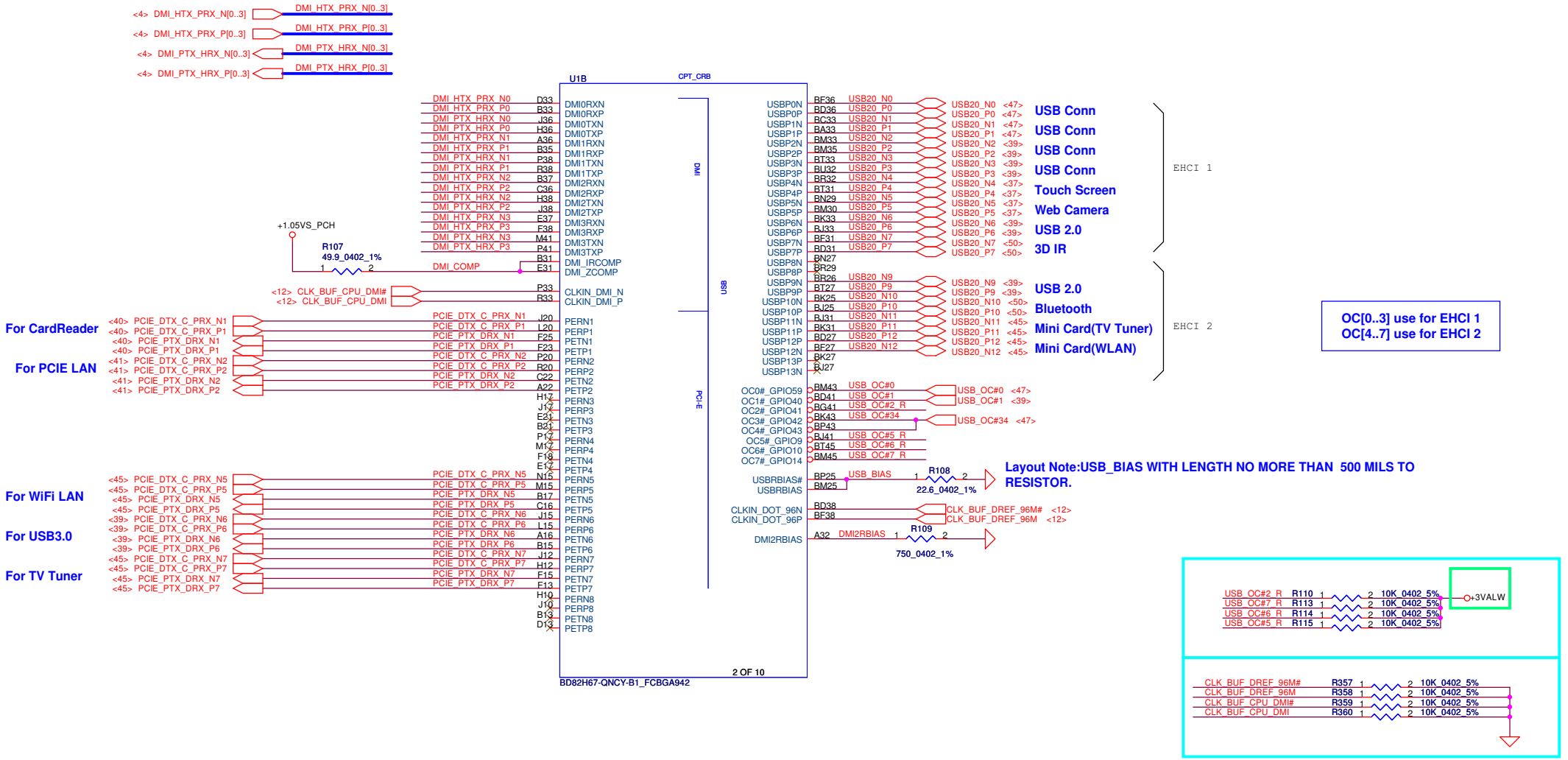
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (2/9) LPC, HDA, SMBUS

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 14 of 66



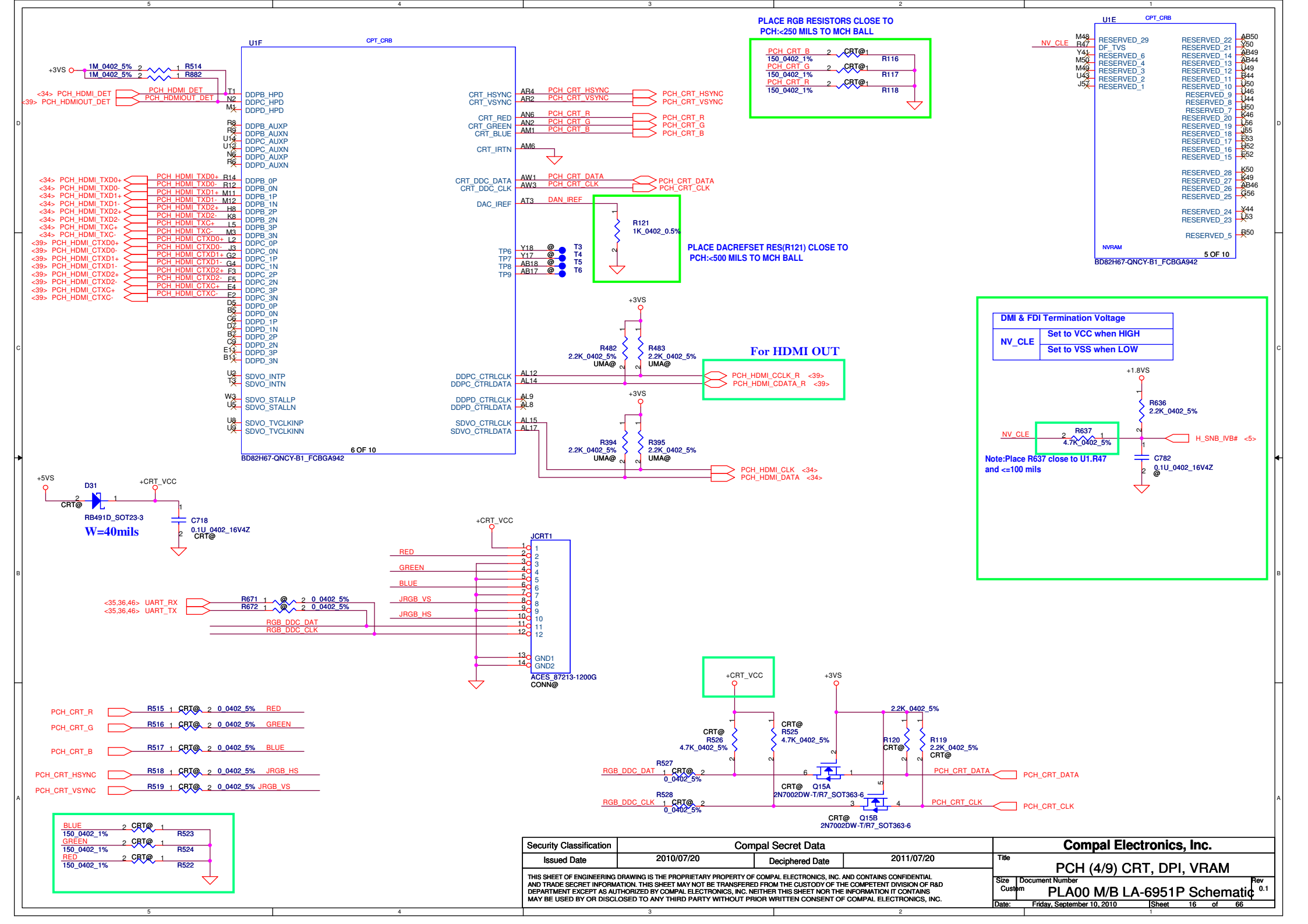
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

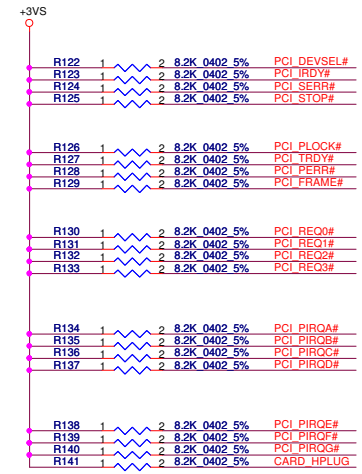
Compal Electronics, Inc.

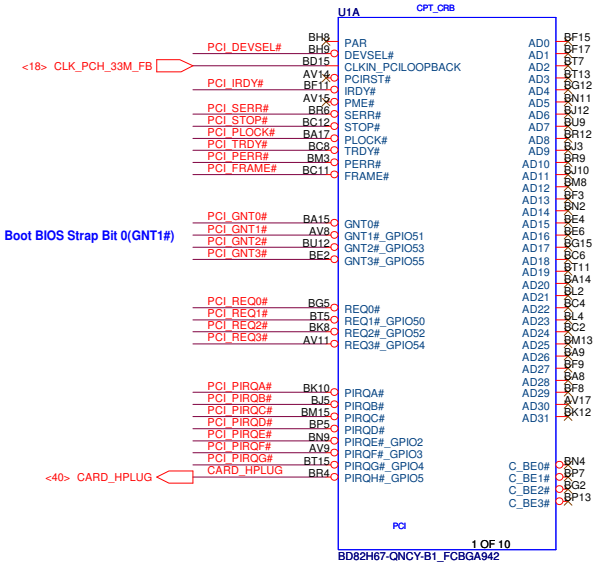
Title: PCH (3/9) DMI, USB, PCIE

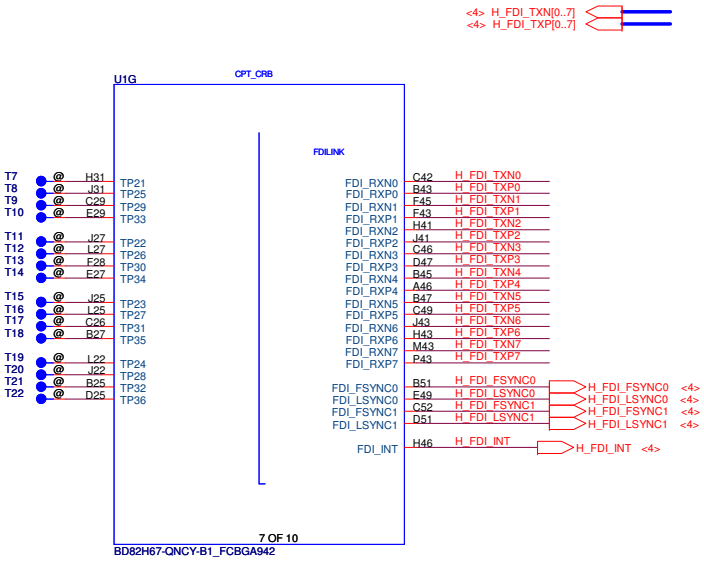
Size	Document Number	Rev
A	PLA00 M/B LA-6951P Schematic	0.1

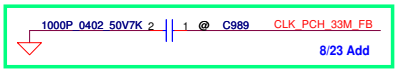
Date: Friday, September 10, 2010 Sheet 15 of 66


PLACE RGB RESISTORS CLOSE TO PCH:<250 MILS TO MCH BALL
PLACE DACREFSET RES(R121) CLOSE TO PCH:<500 MILS TO MCH BALL
For HDMI OUT
DMI & FDI Termination Voltage
NV_CLE
Set to VCC when HIGH
Set to VSS when LOW
Note:Place R637 close to U1.R47 and <=100 mils
W=40mils
U1F
CPT_CRB
6 OF 10
BD82H67-QNCY-B1_FCBGA942
U1E
5 OF 10
NVRAM
JCRT1
ACES_87213-1200G
CONN@
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
Compal Electronics, Inc.
PCH (4/9) CRT, DPI, VRAM
PLA00 M/B LA-6951P Schematic
Friday, September 10, 2010
Sheet 16 of 66

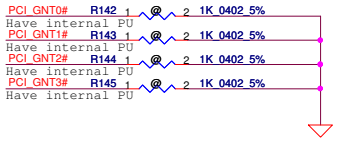








Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (5/9) PCI,FDI

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 17 of 66

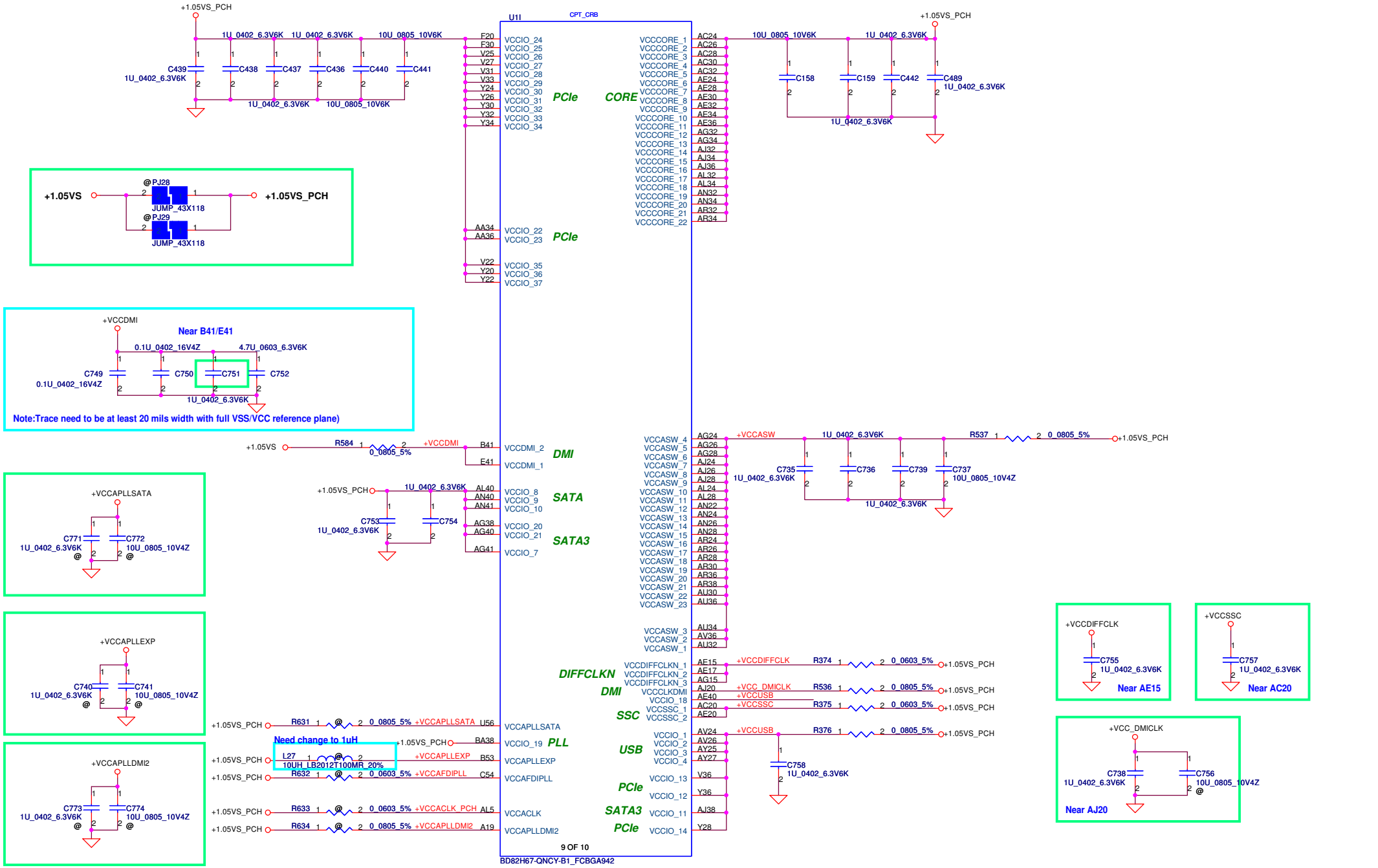
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (6/9) CLOCK

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 Sheet 18 of 66



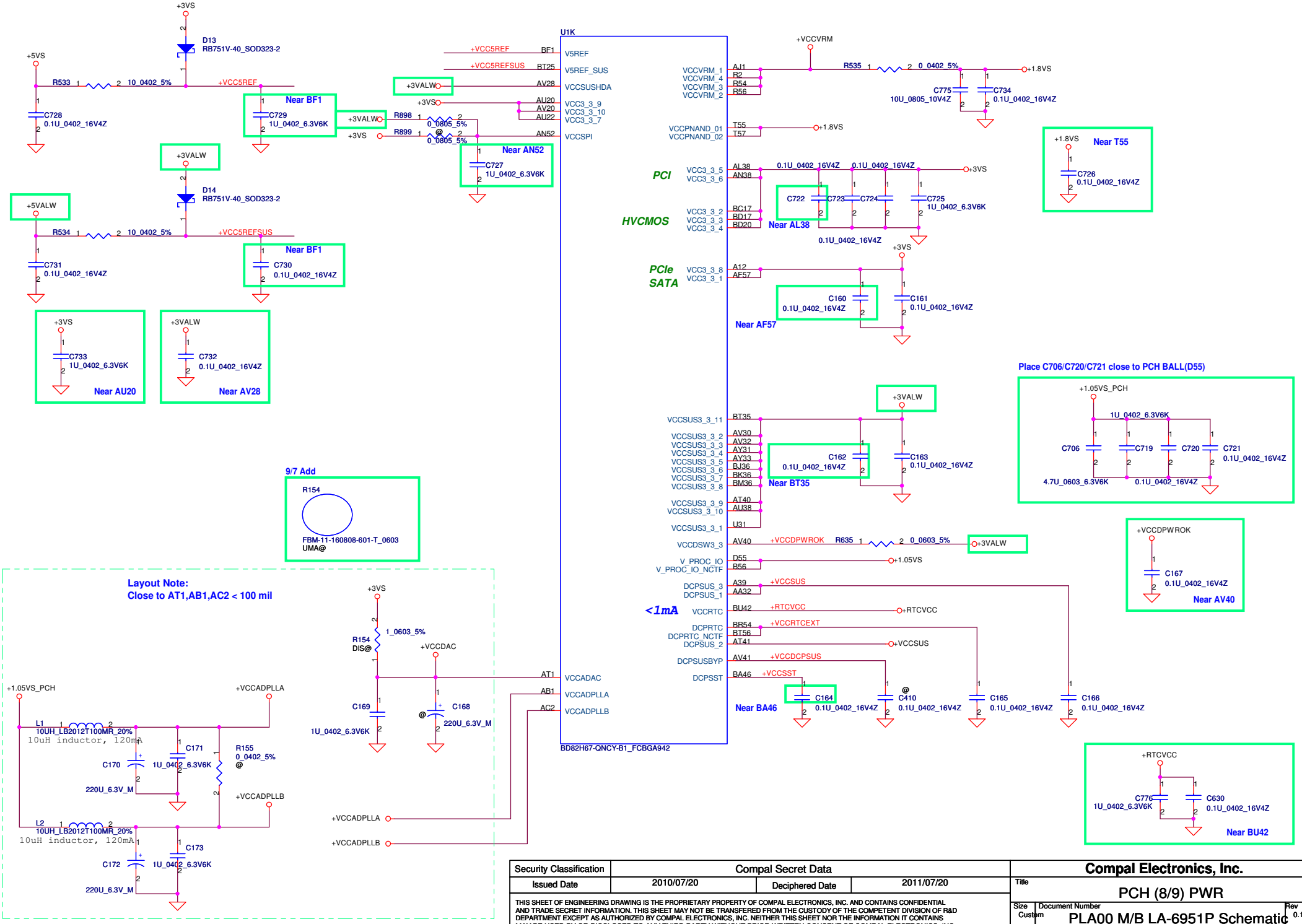
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 19 of 66



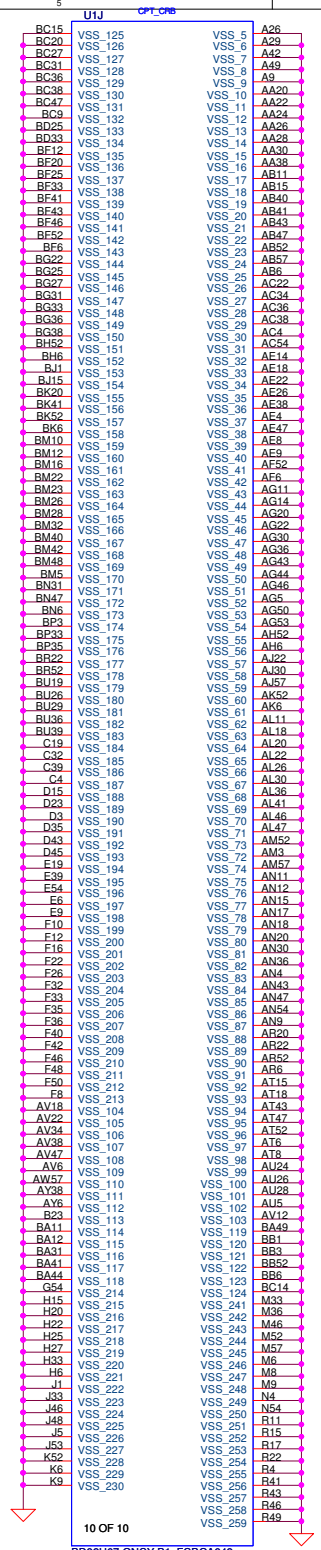
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

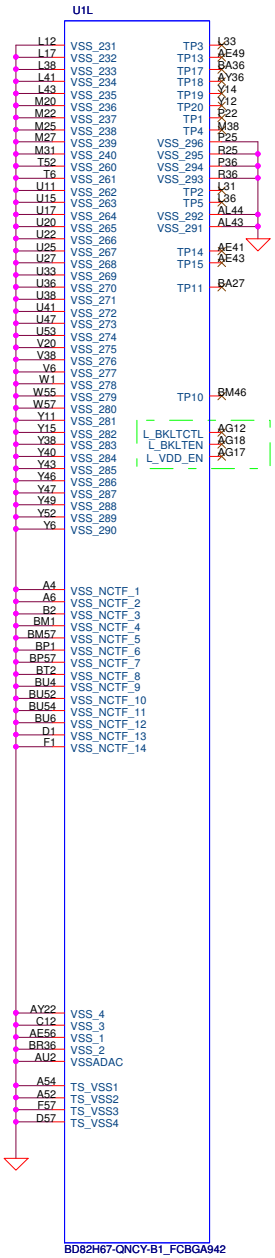
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 | Sheet 20 of 66





NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

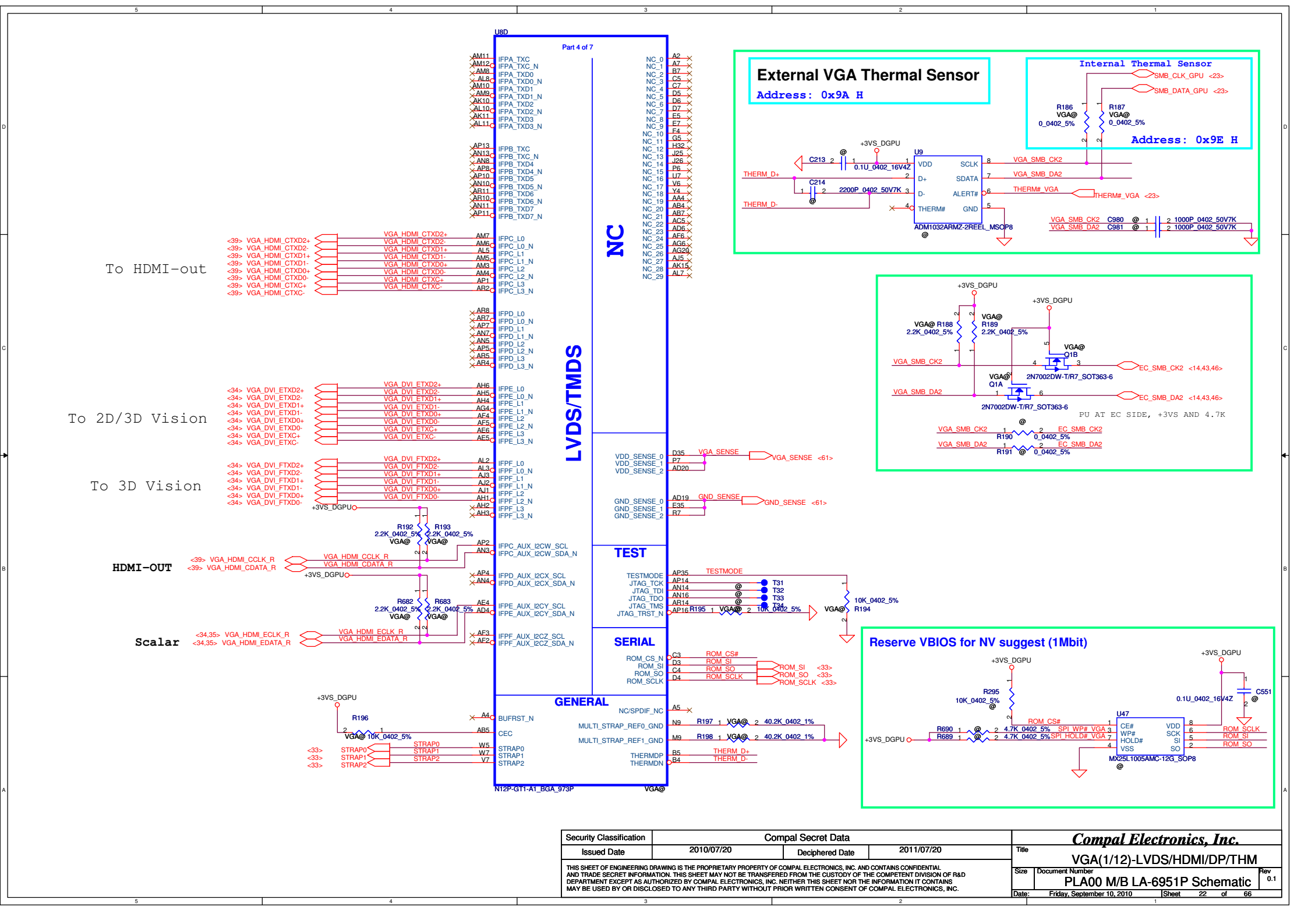
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **PCH(9/9)VSS**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 | Sheet 21 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.
Title: VGA(1/12)-LVDS/HDMI/DP/THM
Size: Document Number: PLA00 M/B LA-6951P Schematic
Rev: 0.1
Date: Friday, September 10, 2010
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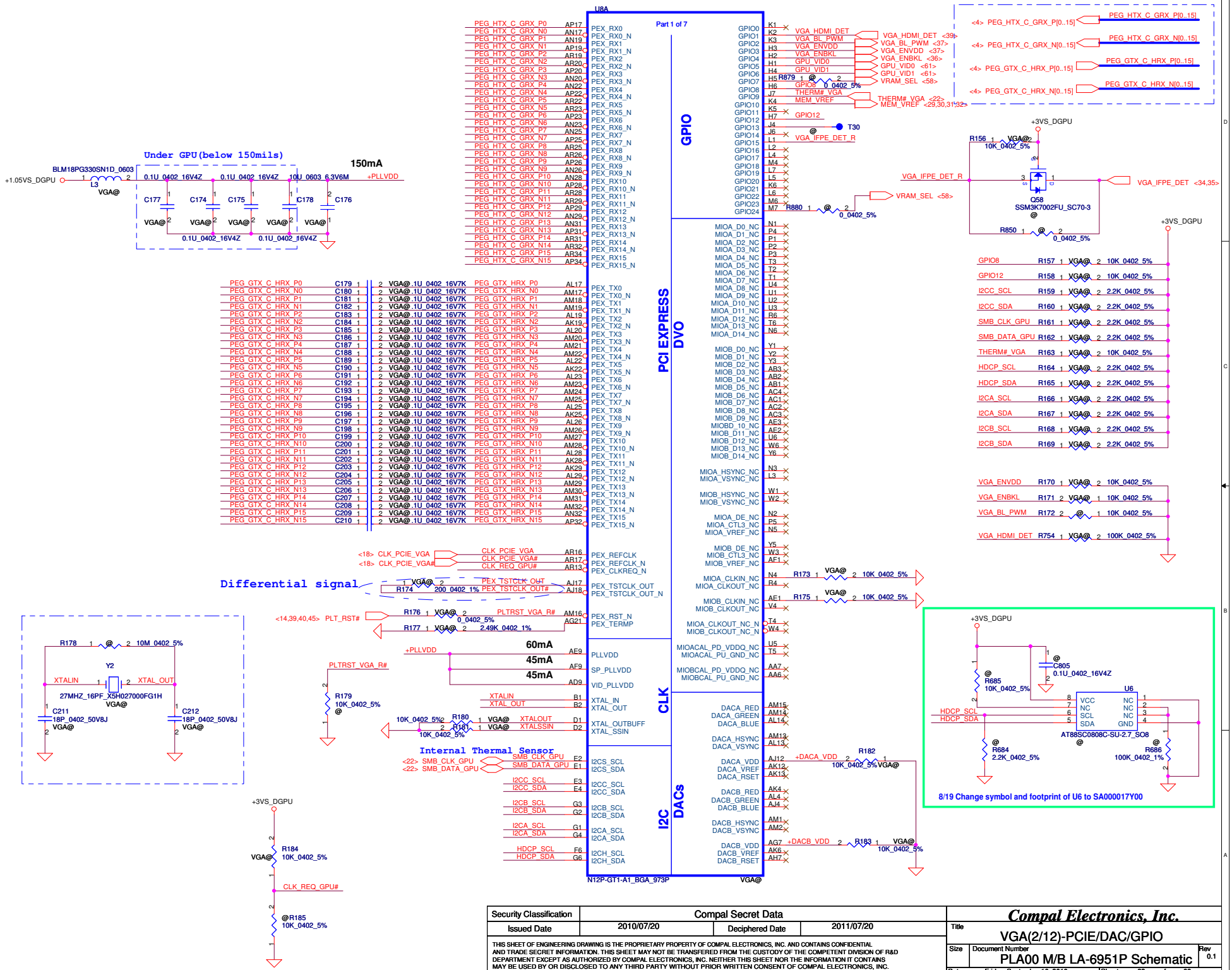


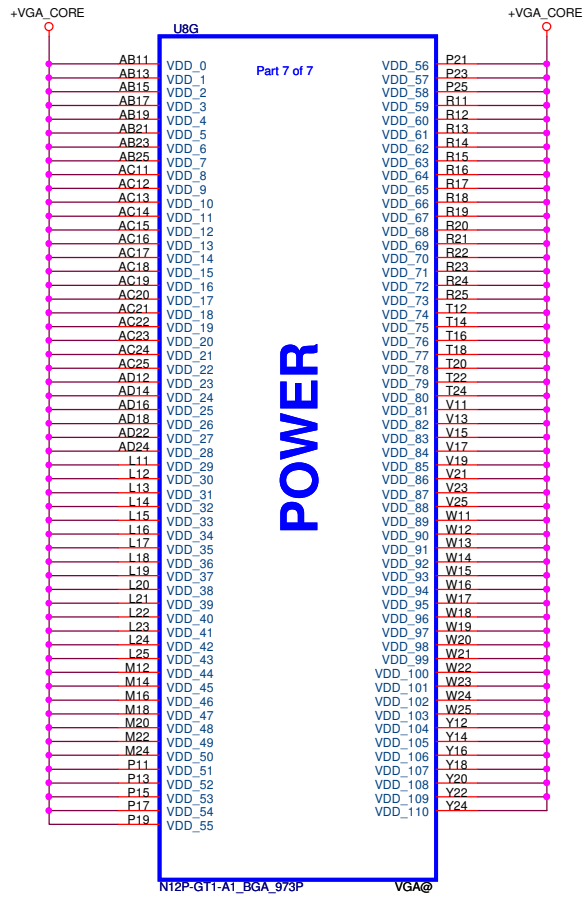
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

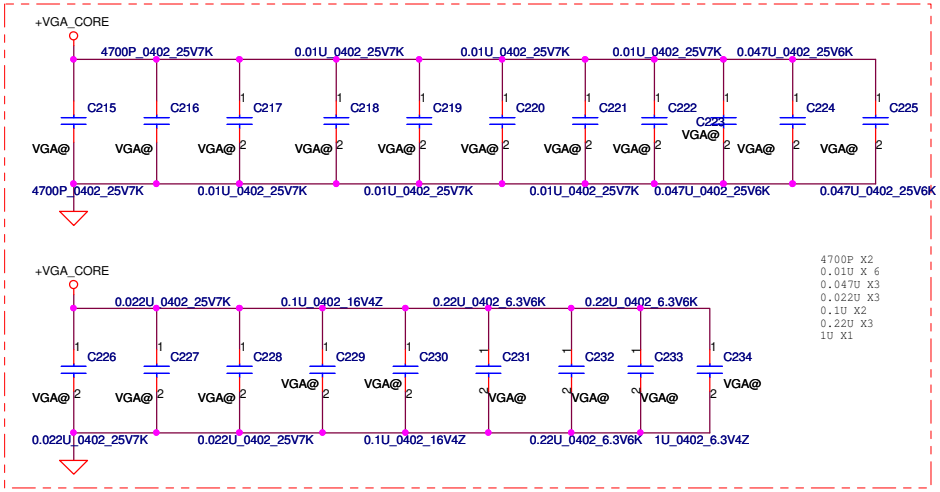
Title: VGA(2/12)-PCIE/DAC/GPIO

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

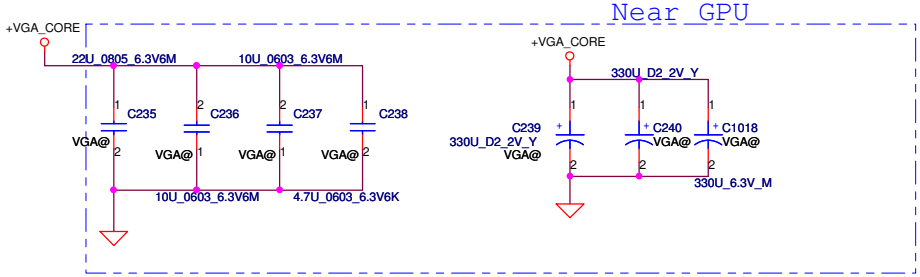
Date: Friday, September 10, 2010 | Sheet 23 of 66



Under GPU



Near GPU



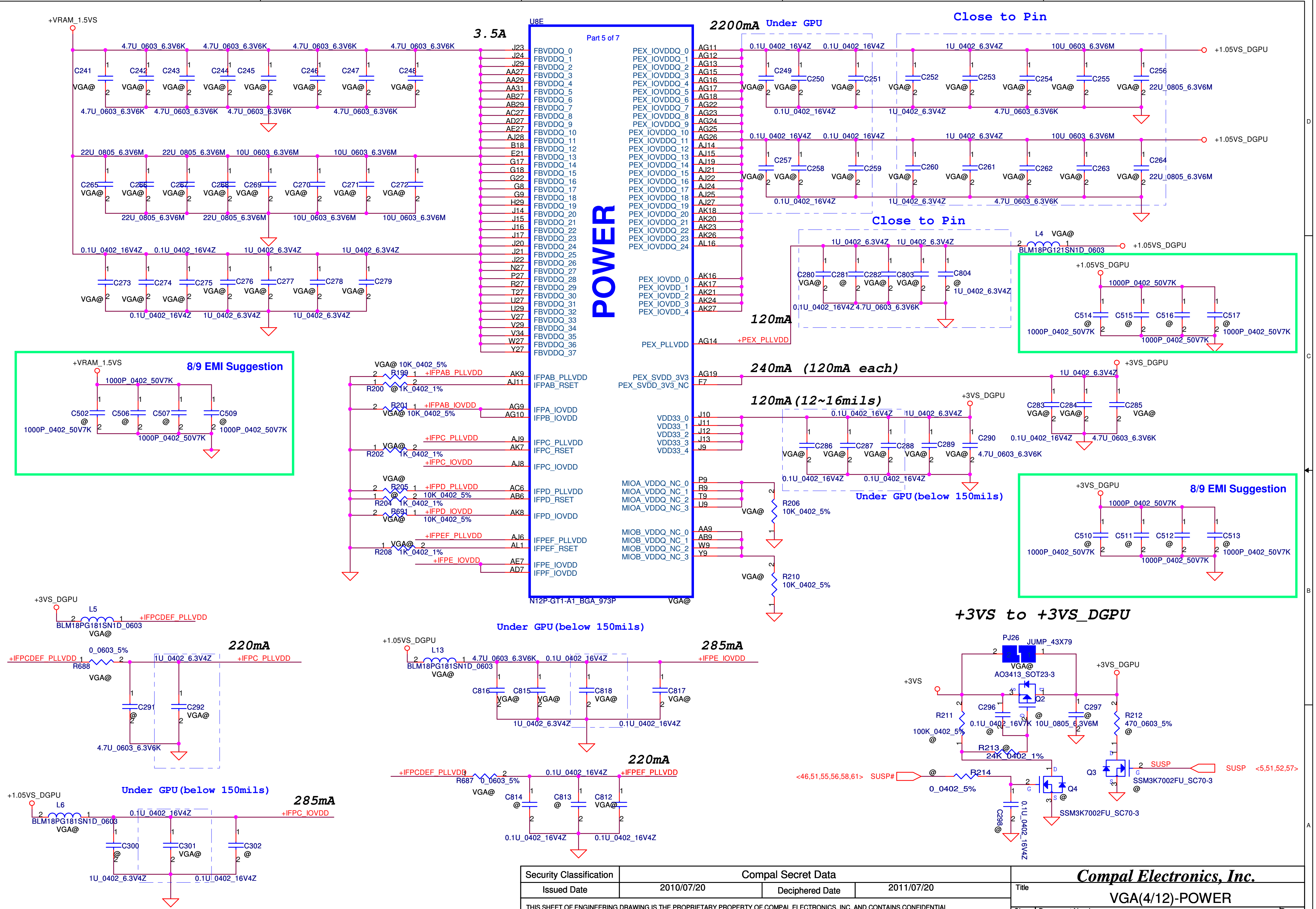
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 24 of 66



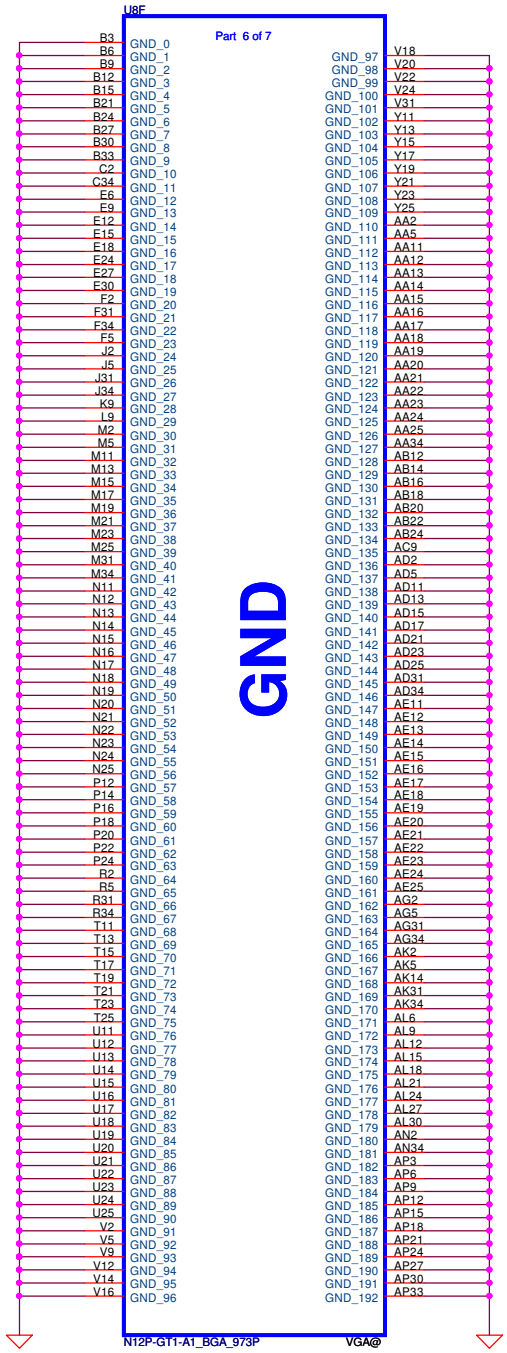
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(4/12)-POWER

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev 0.1

Date: Friday, September 10, 2010 | Sheet 25 of 66



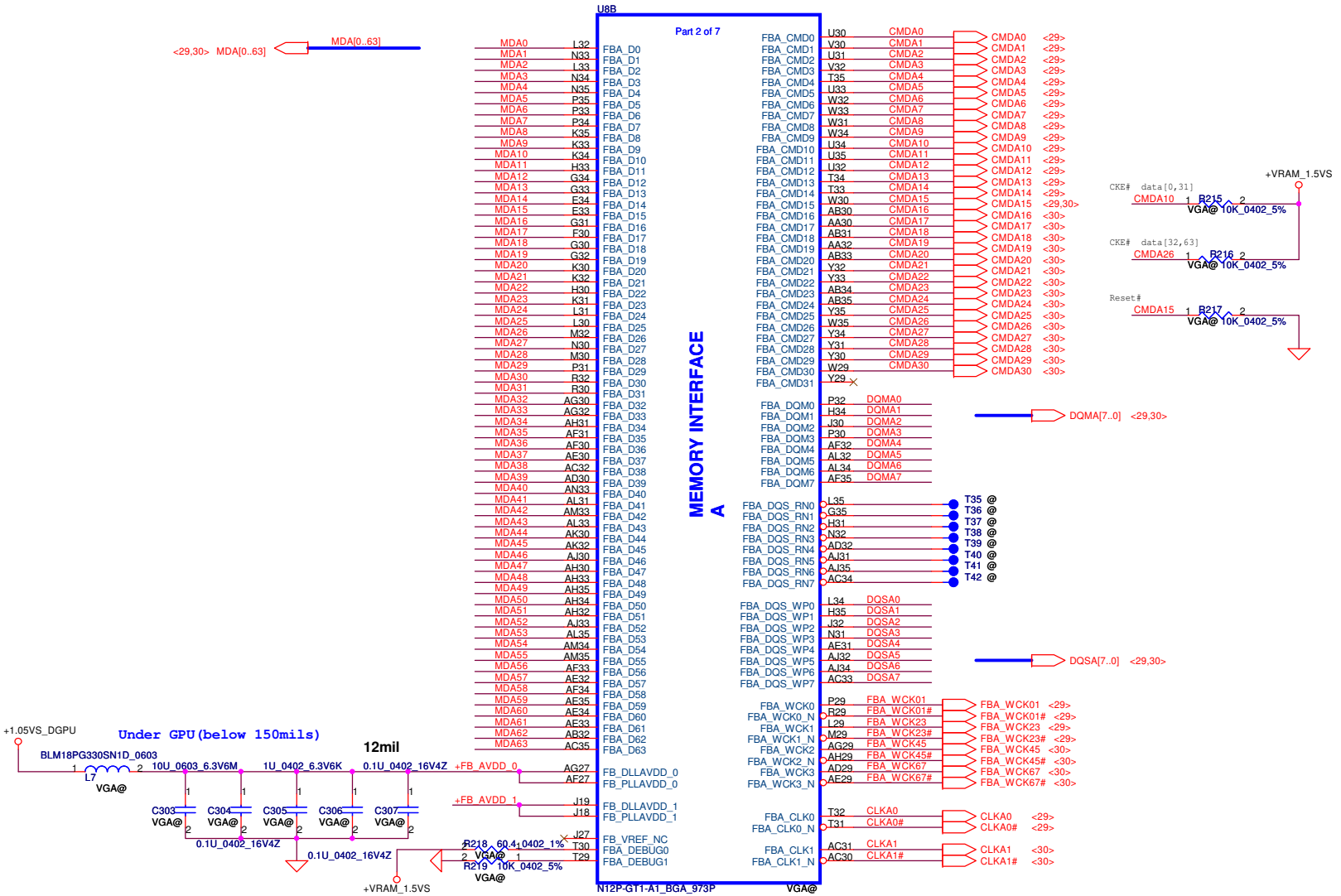
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 26 of 66



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

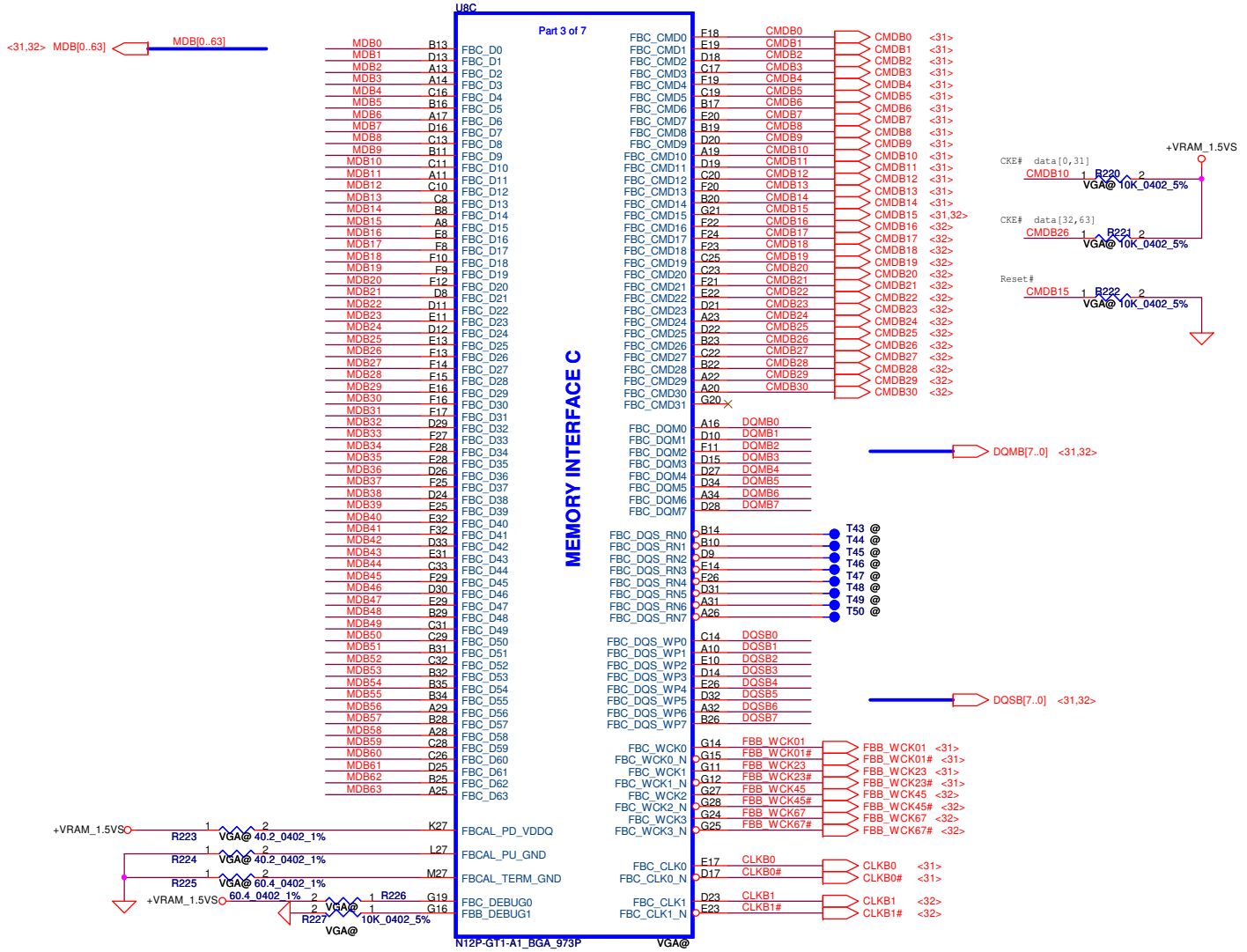
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 27 of 66



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U10

U11

170-BALL
SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

9/7 Add

U10 K4G10325FE-HC04 X76_SAM@

U11 K4G10325FE-HC04 X76_SAM@

MDA[0..63] <27,30>

DQMA[7..0] <27,30>

DQSA[7..0] <27,30>

+VRAM_1.5VS

+FBA_VREFC

+FBA_VREFD

R228 549_0402_1% VGA@

R229 549_0402_1% VGA@

R230 1.33K_0402_1% VGA@

R231 1.33K_0402_1% VGA@

C313 0.01U_0402_25V7K VGA@

C314 0.01U_0402_25V7K VGA@

R232 931_0402_1% VGA@

R233 931_0402_1% VGA@

<23,30,31,32> MEM_VREF

Q5 SSM3K7002FU_SC70-3 VGA@

R234 1K_0402_5% VGA@

R235 1K_0402_5% VGA@

R236 121_0402_1% VGA@

R237 121_0402_1% VGA@

C315 0.01U_0402_25V7K VGA@

R238 40.2_0402_1% VGA@

R239 160_0402_1%

R240 40.2_0402_1% VGA@

C316 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M

C317 C318 C319 VGA@

0.1U_0402_16V4Z

C320 C321 C322 C323 C324 C325 VGA@

1U_0402_6.3V4Z

C326 C327 C328 C329 C330 C331 C332 C333 VGA@

C742 330U_D2_2V_Y VGA@

C1017 330U_6.3V_M @

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VRAM_GDDR5 / Channel A

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U12

U13

MDA[0..63] <27,29>
DQMA[7..0] <27,29>
DQSA[7..0] <27,29>

+VRAM_1.5VS

R241 549_0402_1% VGA@
R242 549_0402_1% VGA@
R243 1.33K_0402_1% VGA@
R244 1.33K_0402_1% VGA@
16mil +FBA_VREFD_U
16mil +FBA_VREFC_U
C334 0.01U_0402_25V7K VGA@
C335 0.01U_0402_25V7K VGA@
R247 VGA@ 931_0402_1%
R248 VGA@ 931_0402_1%
<23,29,31,32> MEM_VREF
Q6 SSM3K7002FU_SC70-3 VGA@

CLKA1
R251 40.2_0402_1% VGA@
R259 @ 160_0402_1%
CLKA1#
R253 40.2_0402_1% VGA@
CLKA1_R
C337 0.01U_0402_25V7K VGA@

+VRAM_1.5VS
10U_0603_6.3V6M
C338 VGA@
C339 VGA@
C340 VGA@
10U_0603_6.3V6M

+VRAM_1.5VS
0.1U_0402_16V4Z
C341 VGA@
C342 VGA@
C343 VGA@
C344 VGA@
C345 VGA@
C346 VGA@
0.1U_0402_16V4Z

+VRAM_1.5VS
1U_0402_6.3V4Z
C347 VGA@
C348 VGA@
C349 VGA@
C350 VGA@
C351 VGA@
C352 VGA@
C353 VGA@
C354 VGA@
1U_0402_6.3V4Z

C336 0.01U_0402_25V7K VGA@

R245 1K_0402_1% VGA@
R249 121_0402_1% VGA@
R246 1K_0402_1% VGA@
R250 121_0402_1% VGA@

170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
X76_HYN@

9/7 Add
U12 K4G10325FE-HC04 X76_SAM@
U13 K4G10325FE-HC04 X76_SAM@

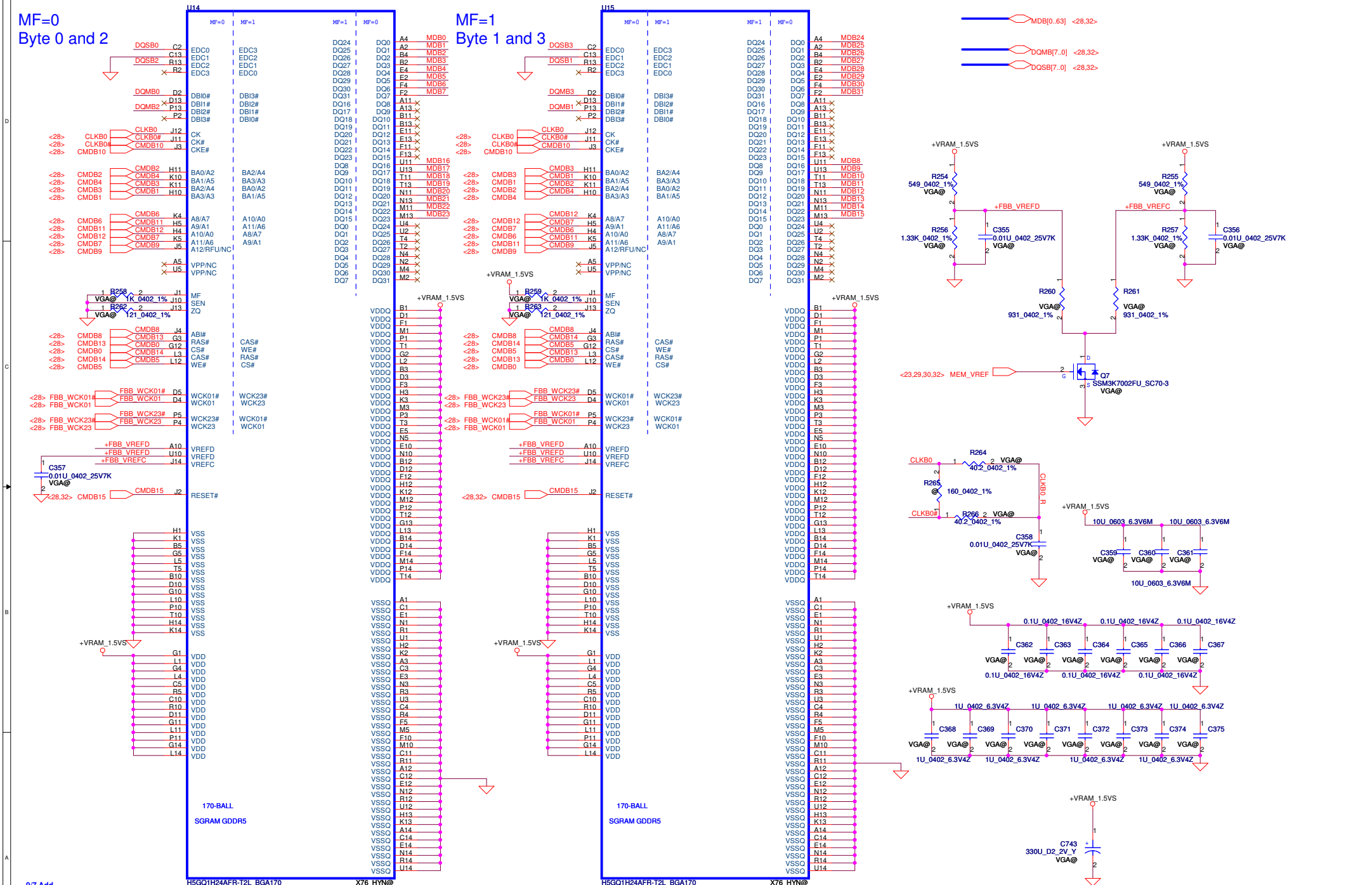
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VRAM_DDDR5 / Channel A

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 Sheet 30 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **VRAM_GDDR5 / Channel B**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

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MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U16

U17

MDB[0..63] <28,31>

DQMB[7..0] <28,31>

DQSB[7..0] <28,31>

+VRAM_1.5VS

R267 549_0402_1% VGA@

R268 549_0402_1% VGA@

16mil +FBB_VREFD_U

16mil +FBB_VREFC_U

R269 1.33K_0402_1% VGA@

C376 0.01U_0402_25V7K VGA@

R270 1.33K_0402_1% VGA@

C377 0.01U_0402_25V7K VGA@

R275 VGA@ 931_0402_1%

R276 VGA@ 931_0402_1%

<23,29,30,31> MEM_VREF

Q8 SSM3K7002FU_SC70-3 VGA@

R277 40.2_0402_1% VGA@

R278 @ 160_0402_1%

R279 40.2_0402_1% VGA@

CLKB1

CLKB1#

C379 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M

C380 VGA@

C381 VGA@

C382 VGA@

C383 VGA@

C384 VGA@

C385 VGA@

C386 VGA@

C387 VGA@

C388 VGA@

0.1U_0402_16V4Z

C389 VGA@

C390 VGA@

C391 VGA@

C392 VGA@

C393 VGA@

C394 VGA@

C395 VGA@

C396 VGA@

1U_0402_6.3V4Z

C378 0.01U_0402_25V7K VGA@

R271 1K_0402_1% VGA@

R273 121_0402_1% VGA@

R272 1K_0402_1% VGA@

R274 121_0402_1% VGA@

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

170-BALL

SGRAM GDDR5

9/7 Add

U16 K4G10325FE-HC04 X76_SAM@

U17 K4G10325FE-HC04 X76_SAM@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **VRAM_DDDR5 / Channel B**

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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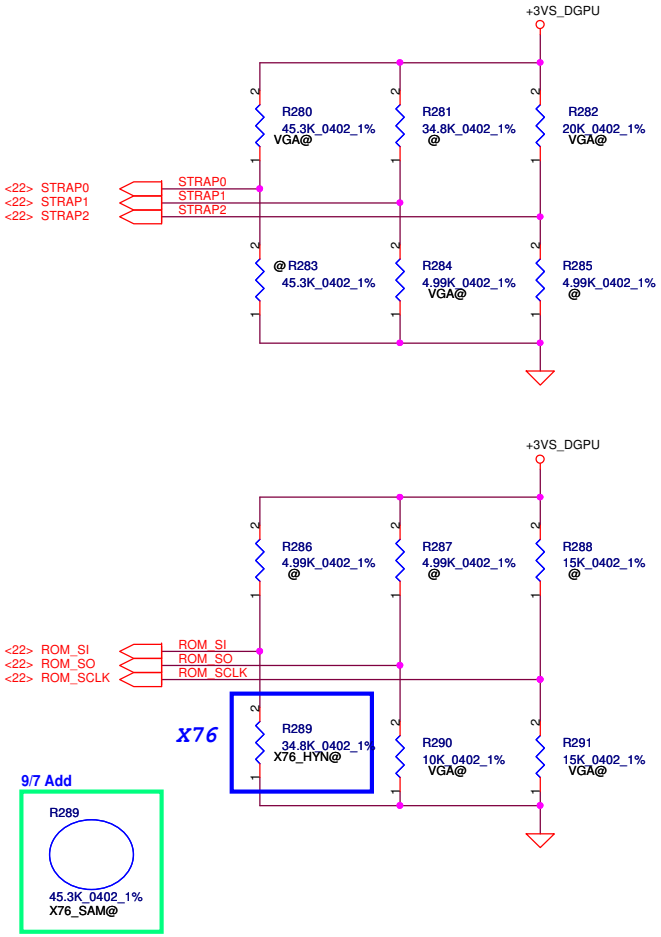

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0110	PD 34.8K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0111	PD 45.3K

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(12/12)-MISC

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

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0804 Vendor suggest close to Cap.

SEL2 (pin50)	SEL1 (pin49)	TMDS/I2C output
H	H	PORT1/SCL1/SDA1
H	L	PORT2/SCL2/SDA2

8/18 Add L56(Vendor suggest)

8/18 Add C923~C926(Vendor suggest)

8/18 Add C927(Vendor suggest)

U18

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: HDMI Switch

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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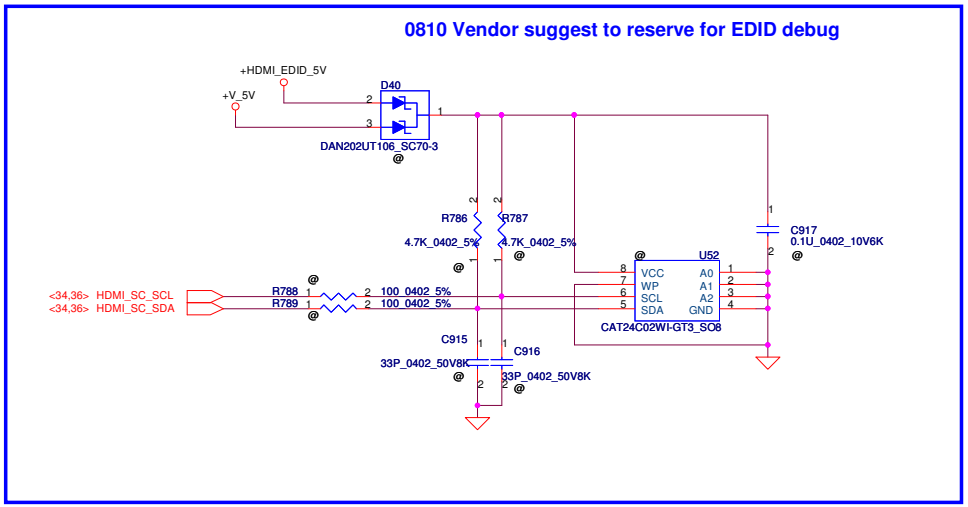
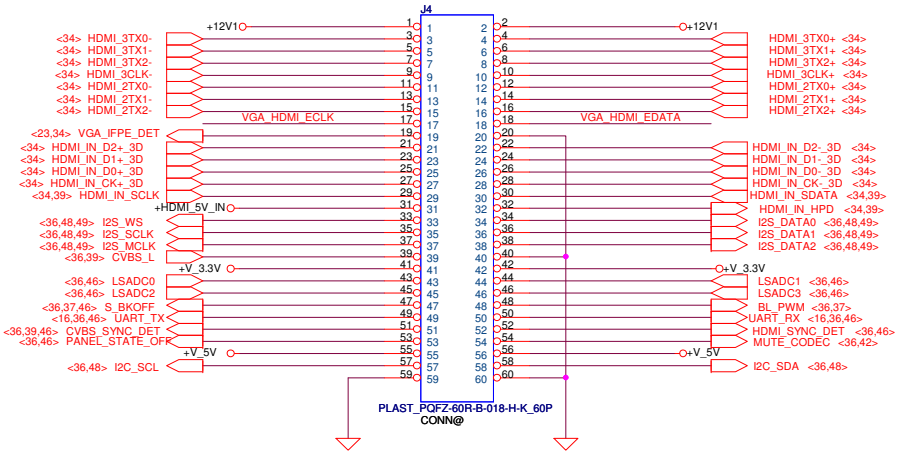
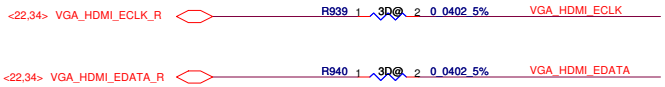
0810 Vendor suggest to reserve for EDID debug



0829 IO/B Pin define update





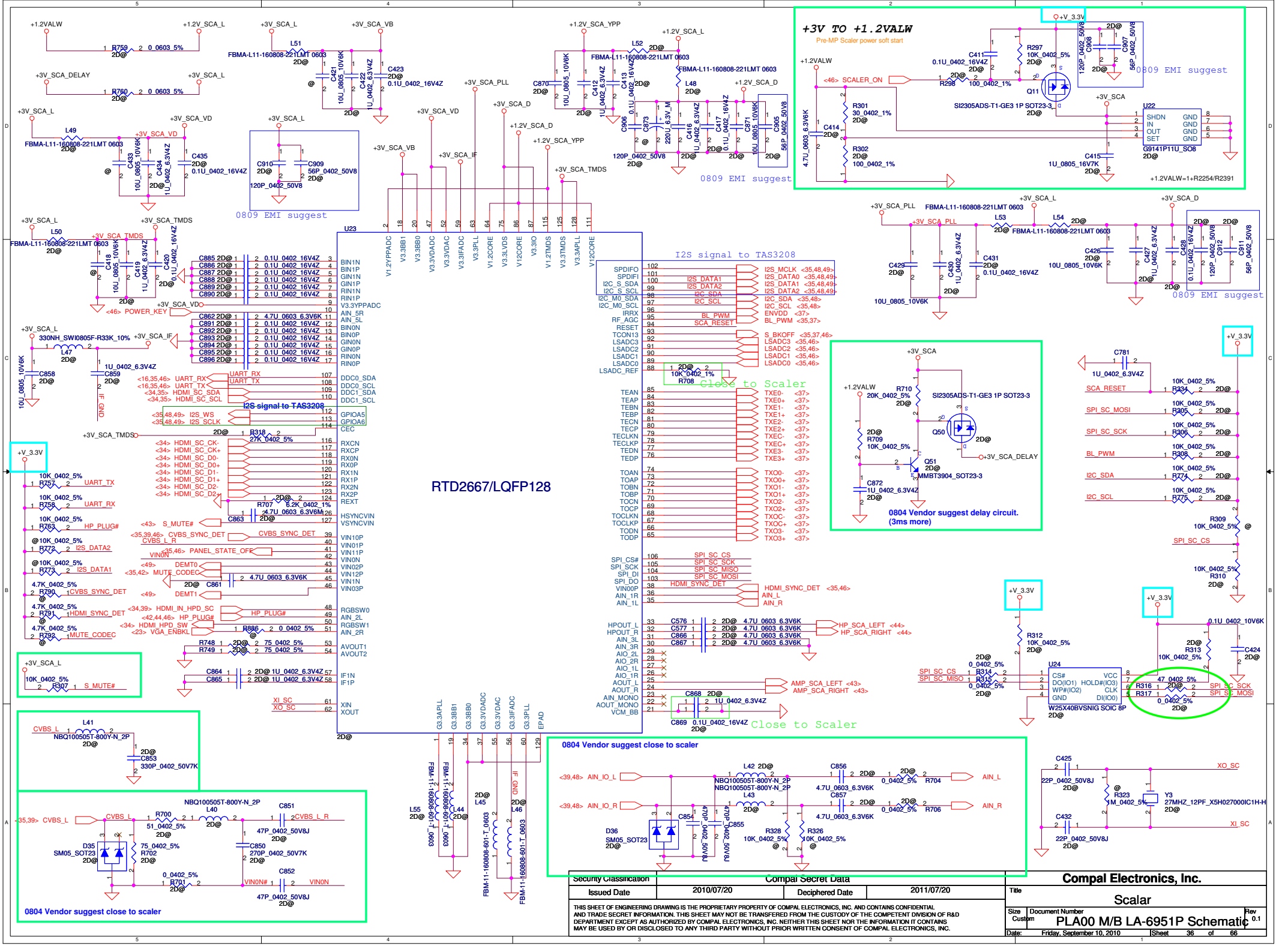
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 3D Scalar

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 35 of 66


+3V TO +1.2VALW
Pre-MP Scaler power soft start
0809 EMI suggest
I2S signal to TAS3208
Close to Scaler
0804 Vendor suggest delay circuit. (3ms more)
RTD2667/LQFP128
0804 Vendor suggest close to scaler
Compal Electronics, Inc.
Scalar
PLA00 M/B LA-6951P Schematic
Security Classification: Compal Secret Data
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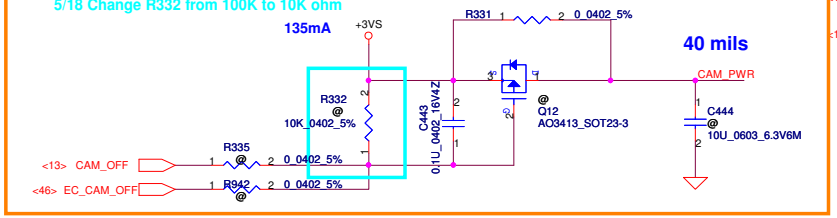
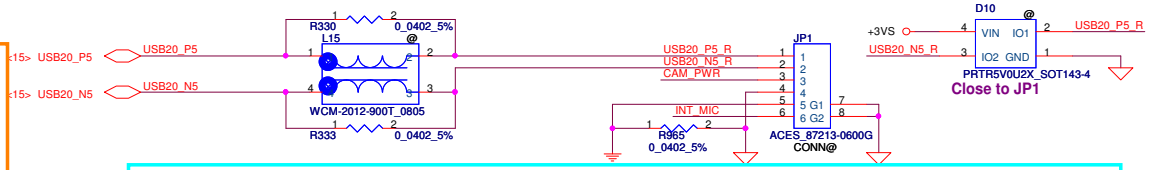
WebCam+Digital Mic

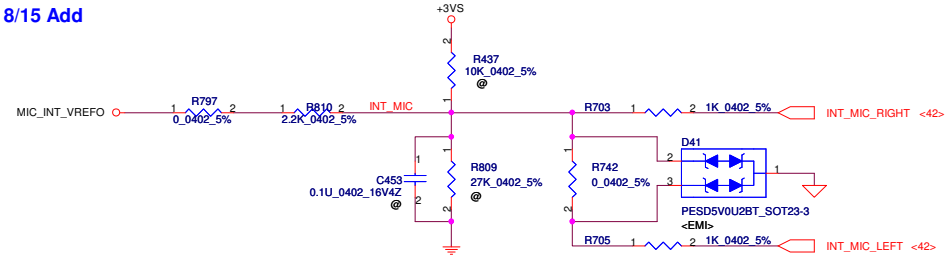
5/18 Change R332 from 100K to 10K ohm

135mA

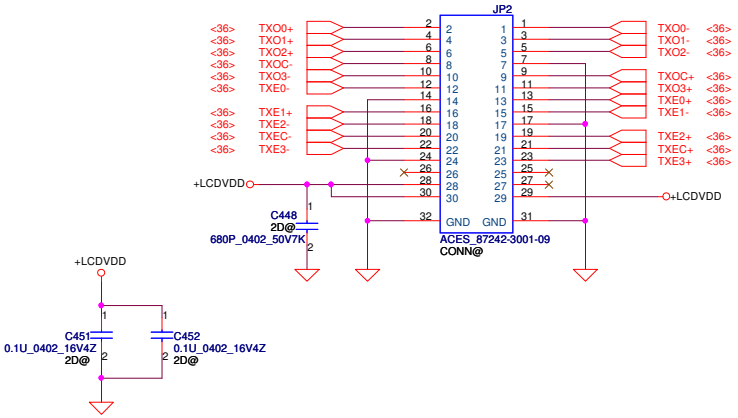




8/15 Add

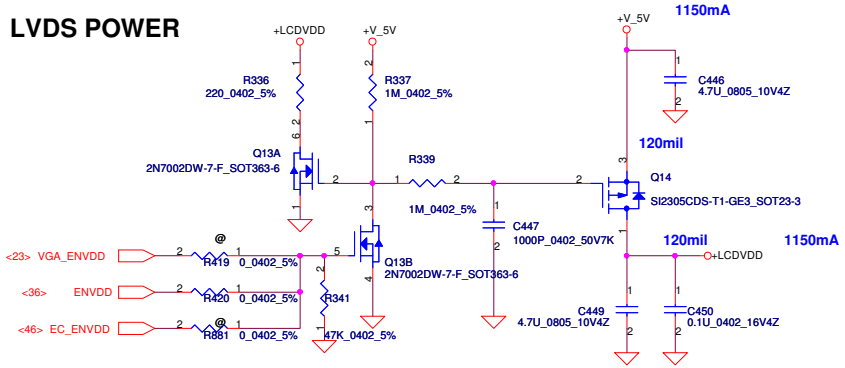


LVDS CONN



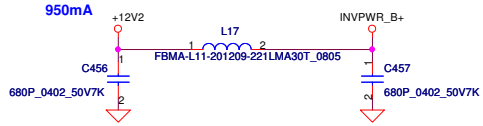
LVDS POWER

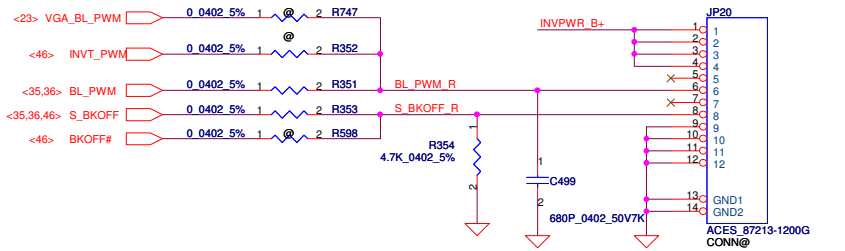
1150mA



INVERTER

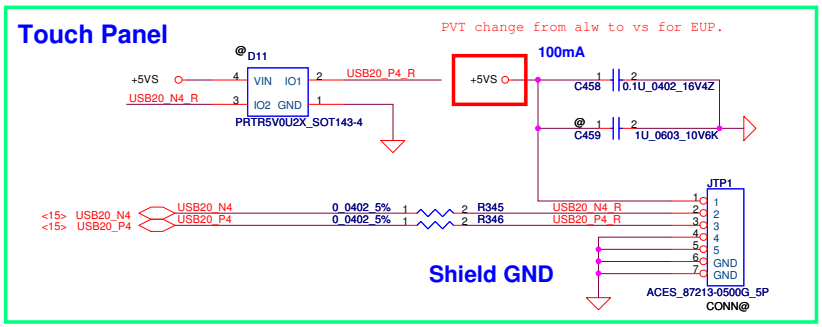
ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20





Touch Panel

PVT change from alw to vs for EUP.



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: LCD CONN. / WebCam

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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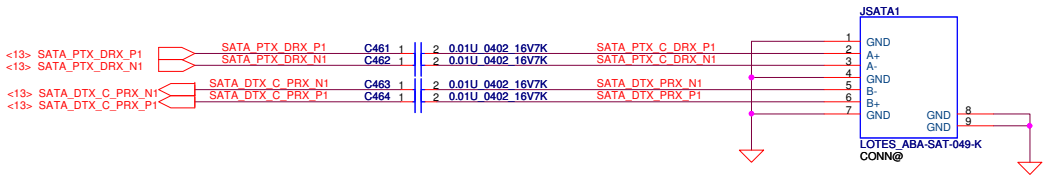
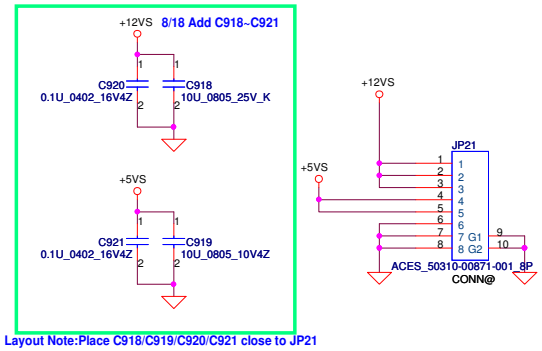
HDD

SATA HDD Conn.

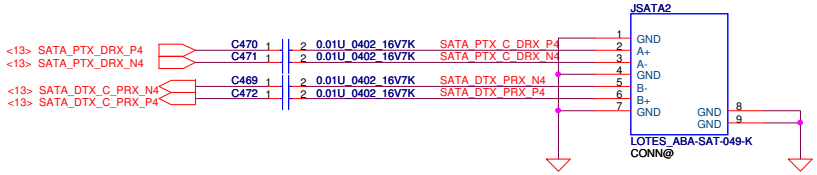


HDD/ODD POWER Conn

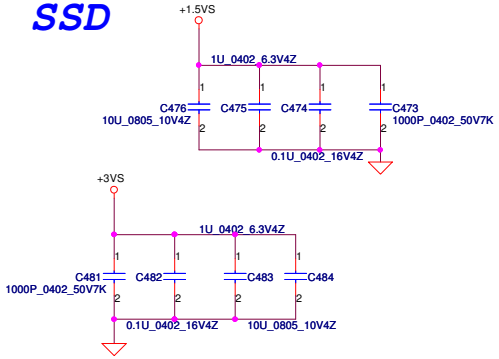


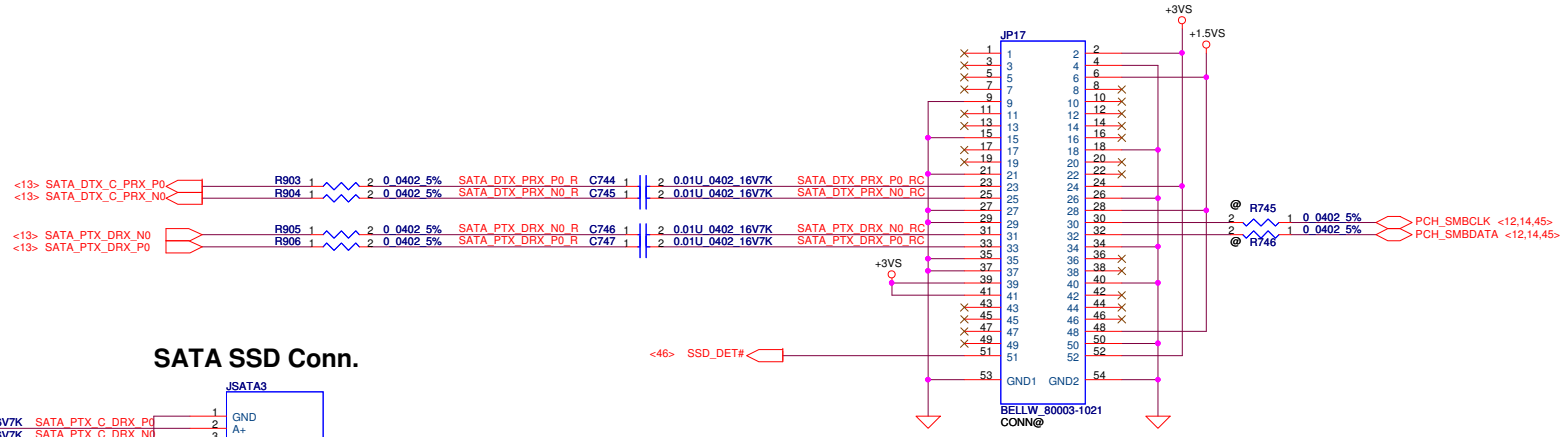
ODD

SATA ODD Conn.

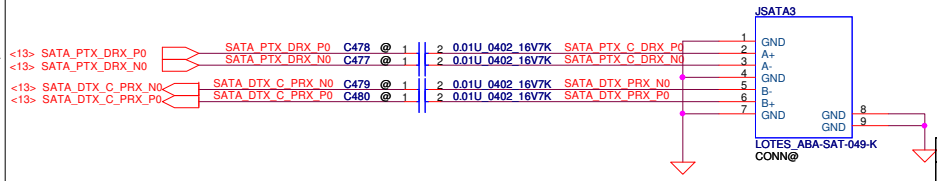


SSD





SATA SSD Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **HDD & ODD & SSD Connector**

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.1

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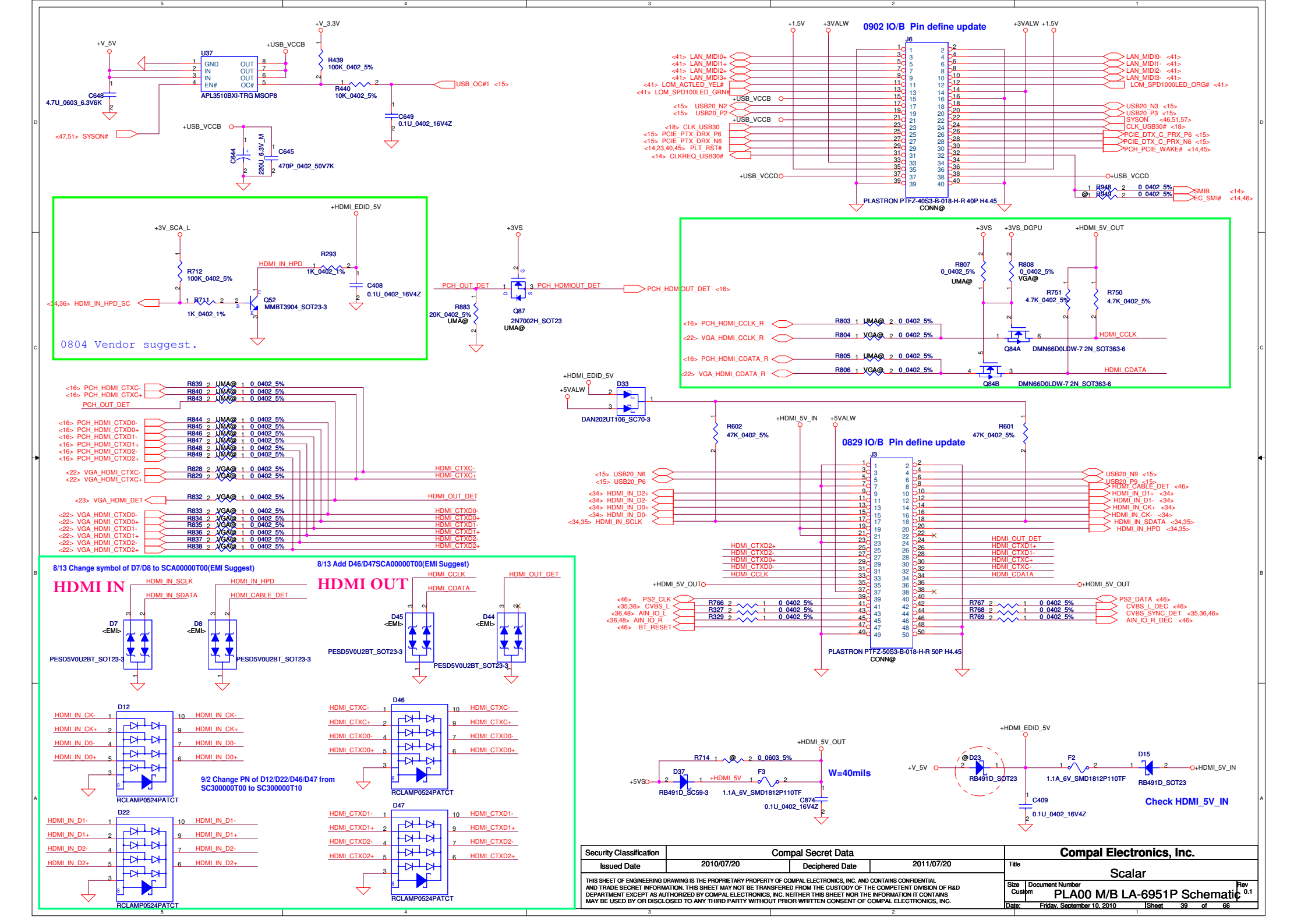
+V_5V
U37
GND
IN
IN
EN#
OUT
OUT
OUT
OC#
APL3510BXI-TRG MSOP8
+USB_VCCB
+V_3.3V
R439
100K_0402_5%
R440
10K_0402_5%
USB_OC#1 <15>
C648
4.7U_0603_6.3V6K
C649
0.1U_0402_16V4Z
<47,51> SYSON#
C644
220U_6.3V_M
C645
470P_0402_50V7K
0902 IO/B Pin define update
J6
PLASTRON PTFZ-40S3-B-018-H-R 40P H4.45
CONN@
+1.5V
+3VALW
+3VALW +1.5V
<41> LAN_MIDI0+
<41> LAN_MIDI1+
<41> LAN_MIDI2+
<41> LAN_MIDI3+
<41> LOM_ACTLED_YEL#
<41> LOM_SPD100LED_GRN#
LAN_MIDI0- <41>
LAN_MIDI1- <41>
LAN_MIDI2- <41>
LAN_MIDI3- <41>
LOM_SPD1000LED_ORG# <41>
<15> USB20_N2
<15> USB20_P2
USB20_N3 <15>
USB20_P3 <15>
SYSON <46,51,57>
<18> CLK_USB30
CLK_USB30# <18>
<15> PCIE_PTX_DRX_P6
<15> PCIE_PTX_DRX_N6
<14,23,40,45> PLT_RST#
<14> CLKREQ_USB30#
PCIE_DTX_C_PRX_P6 <15>
PCIE_DTX_C_PRX_N6 <15>
PCH_PCIE_WAKE# <14,45>
R948 0_0402_5%
R949 0_0402_5%
SMIB <14>
EC_SMI# <14,46>
+HDMI_EDID_5V
+3V_SCA_L
R712
100K_0402_5%
HDMI_IN_HPD
R293
1K_0402_1%
C408
0.1U_0402_16V4Z
<34,36> HDMI_IN_HPD_SC
R711
1K_0402_1%
Q52
MMBT3904_SOT23-3
0804 Vendor suggest.
+3VS
PCH_OUT_DET
PCH_HDMIOUT_DET
PCH_HDMIOUT_DET <16>
R883
20K_0402_5%
UMA@
Q87
2N7002H_SOT23
+3VS_DGPU
+HDMI_5V_OUT
R807
0_0402_5%
UMA@
R808
0_0402_5%
VGA@
R751
4.7K_0402_5%
R750
4.7K_0402_5%
<16> PCH_HDMI_CCLK_R
<22> VGA_HDMI_CCLK_R
<16> PCH_HDMI_CDATA_R
<22> VGA_HDMI_CDATA_R
R803 UMA@ 0_0402_5%
R804 VGA@ 0_0402_5%
R805 UMA@ 0_0402_5%
R806 VGA@ 0_0402_5%
HDMI_CCLK
HDMI_CDATA
Q84A
DMN66D0LDW-7 2N_SOT363-6
Q84B
DMN66D0LDW-7 2N_SOT363-6
<16> PCH_HDMI_CTXC-
<16> PCH_HDMI_CTXC+
R839 UMA@ 0_0402_5%
R840 UMA@ 0_0402_5%
R843 UMA@ 0_0402_5%
PCH_OUT_DET
<16> PCH_HDMI_CTXD0-
<16> PCH_HDMI_CTXD0+
<16> PCH_HDMI_CTXD1-
<16> PCH_HDMI_CTXD1+
<16> PCH_HDMI_CTXD2-
<16> PCH_HDMI_CTXD2+
R844 UMA@ 0_0402_5%
R845 UMA@ 0_0402_5%
R846 UMA@ 0_0402_5%
R847 UMA@ 0_0402_5%
R848 UMA@ 0_0402_5%
R849 UMA@ 0_0402_5%
<22> VGA_HDMI_CTXC-
<22> VGA_HDMI_CTXC+
R828 VGA@ 0_0402_5%
R829 VGA@ 0_0402_5%
HDMI_CTXC-
HDMI_CTXC+
<23> VGA_HDMI_DET
R832 VGA@ 0_0402_5%
HDMI_OUT_DET
<22> VGA_HDMI_CTXD0-
<22> VGA_HDMI_CTXD0+
<22> VGA_HDMI_CTXD1-
<22> VGA_HDMI_CTXD1+
<22> VGA_HDMI_CTXD2-
<22> VGA_HDMI_CTXD2+
R833 VGA@ 0_0402_5%
R834 VGA@ 0_0402_5%
R835 VGA@ 0_0402_5%
R836 VGA@ 0_0402_5%
R837 VGA@ 0_0402_5%
R838 VGA@ 0_0402_5%
HDMI_CTXD0-
HDMI_CTXD0+
HDMI_CTXD1-
HDMI_CTXD1+
HDMI_CTXD2-
HDMI_CTXD2+
+HDMI_EDID_5V
+5VALW
D33
DAN202UT106_SC70-3
+HDMI_5V_IN
R602
47K_0402_5%
R601
47K_0402_5%
0829 IO/B Pin define update
J3
PLASTRON PTFZ-50S3-B-018-H-R 50P H4.45
CONN@
<15> USB20_N6
<15> USB20_P6
<34> HDMI_IN_D2+
<34> HDMI_IN_D2-
<34> HDMI_IN_D0+
<34> HDMI_IN_D0-
<34,35> HDMI_IN_SCLK
USB20_N9 <15>
USB20_P9 <15>
HDMI_CABLE_DET <46>
HDMI_IN_D1+ <34>
HDMI_IN_D1- <34>
HDMI_IN_CK+ <34>
HDMI_IN_CK- <34>
HDMI_IN_SDATA <34,35>
HDMI_IN_HPD <34,35>
HDMI_CTXD2+
HDMI_CTXD2-
HDMI_CTXD0+
HDMI_CTXD0-
HDMI_CCLK
HDMI_OUT_DET
HDMI_CTXD1+
HDMI_CTXD1-
HDMI_CTXC+
HDMI_CTXC-
HDMI_CDATA
+HDMI_5V_OUT
<46> PS2_CLK
<35,36> CVBS_L
<36,48> AIN_IO_L
<36,48> AIN_IO_R
<46> BT_RESET
R766 0_0402_5%
R327 0_0402_5%
R329 0_0402_5%
R767 0_0402_5%
R768 0_0402_5%
R769 0_0402_5%
PS2_DATA <46>
CVBS_L_DEC <46>
CVBS_SYNC_DET <35,36,46>
AIN_IO_R_DEC <46>
8/13 Change symbol of D7/D8 to SCA00000T00(EMI Suggest)
HDMI IN
HDMI_IN_SCLK
HDMI_IN_SDATA
HDMI_IN_HPD
HDMI_CABLE_DET
D7
<EMI>
D8
<EMI>
PESD5V0U2BT_SOT23-3
8/13 Add D46/D47SCA00000T00(EMI Suggest)
HDMI OUT
HDMI_CCLK
HDMI_CDATA
HDMI_OUT_DET
D45
<EMI>
D44
<EMI>
PESD5V0U2BT_SOT23-3
D12
HDMI_IN_CK-
HDMI_IN_CK+
HDMI_IN_D0-
HDMI_IN_D0+
RCLAMP0524PATCT
9/2 Change PN of D12/D22/D46/D47 from SC300000T00 to SC300000T10
D46
HDMI_CTXC-
HDMI_CTXC+
HDMI_CTXD0-
HDMI_CTXD0+
D22
HDMI_IN_D1-
HDMI_IN_D1+
HDMI_IN_D2-
HDMI_IN_D2+
D47
HDMI_CTXD1-
HDMI_CTXD1+
HDMI_CTXD2-
HDMI_CTXD2+
+HDMI_5V_OUT
R714
0_0603_5%
D37
RB491D_SC59-3
F3
1.1A_6V_SMD1812P110TF
C874
0.1U_0402_16V4Z
W=40mils
+HDMI_EDID_5V
+V_5V
D23
RB491D_SOT23
F2
1.1A_6V_SMD1812P110TF
D15
RB491D_SOT23
+HDMI_5V_IN
C409
0.1U_0402_16V4Z
Check HDMI_5V_IN
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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Scalar
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
Rev
0.1
Date:
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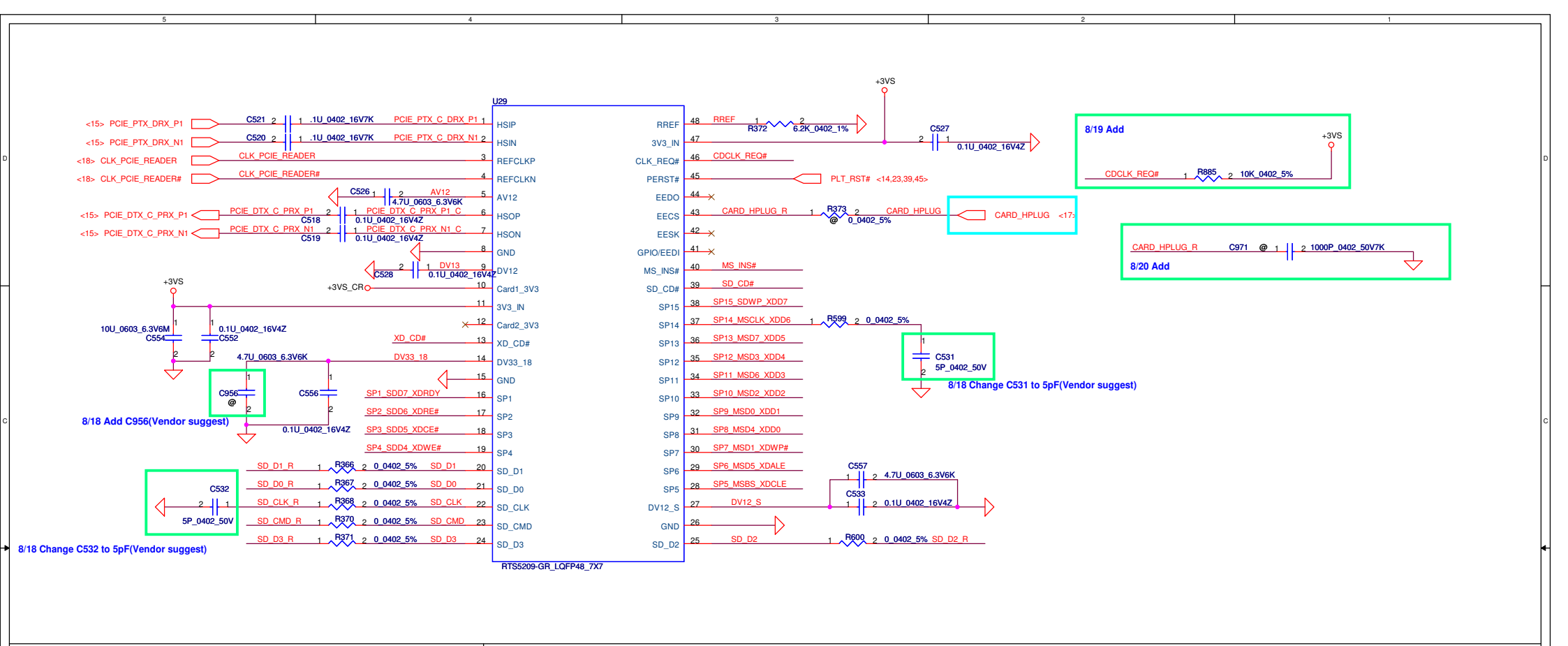
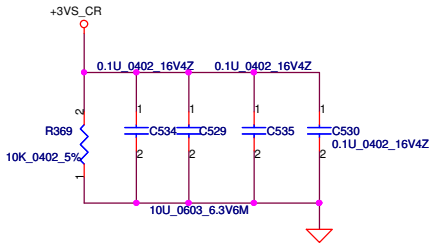
66





Place C534 close to socket pin 38

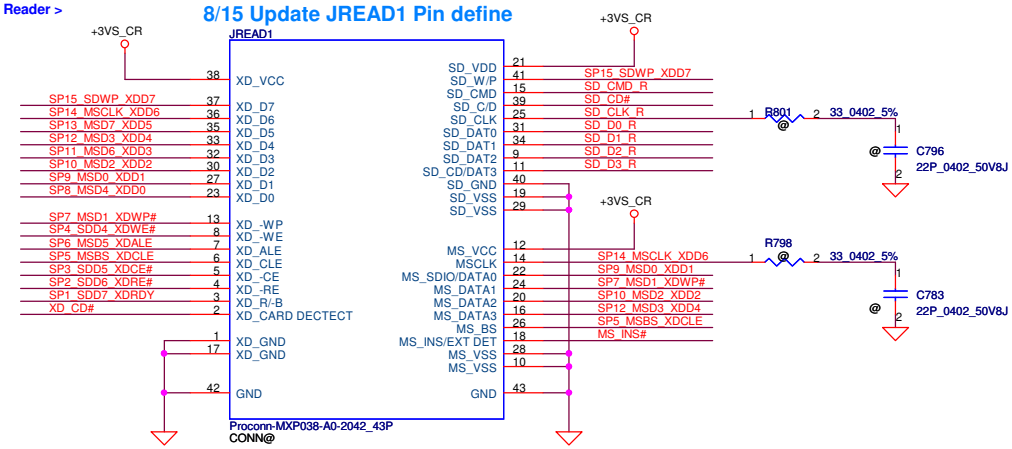
Place C529 close to socket pin 21

Place C535 close to socket pin 21

Place C530 close to socket pin 12

< 7 in 1 Card Reader >

8/15 Update JREAD1 Pin define



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Compal Electronics, Inc.

Title: PCIE-Card Reader-RTS5209

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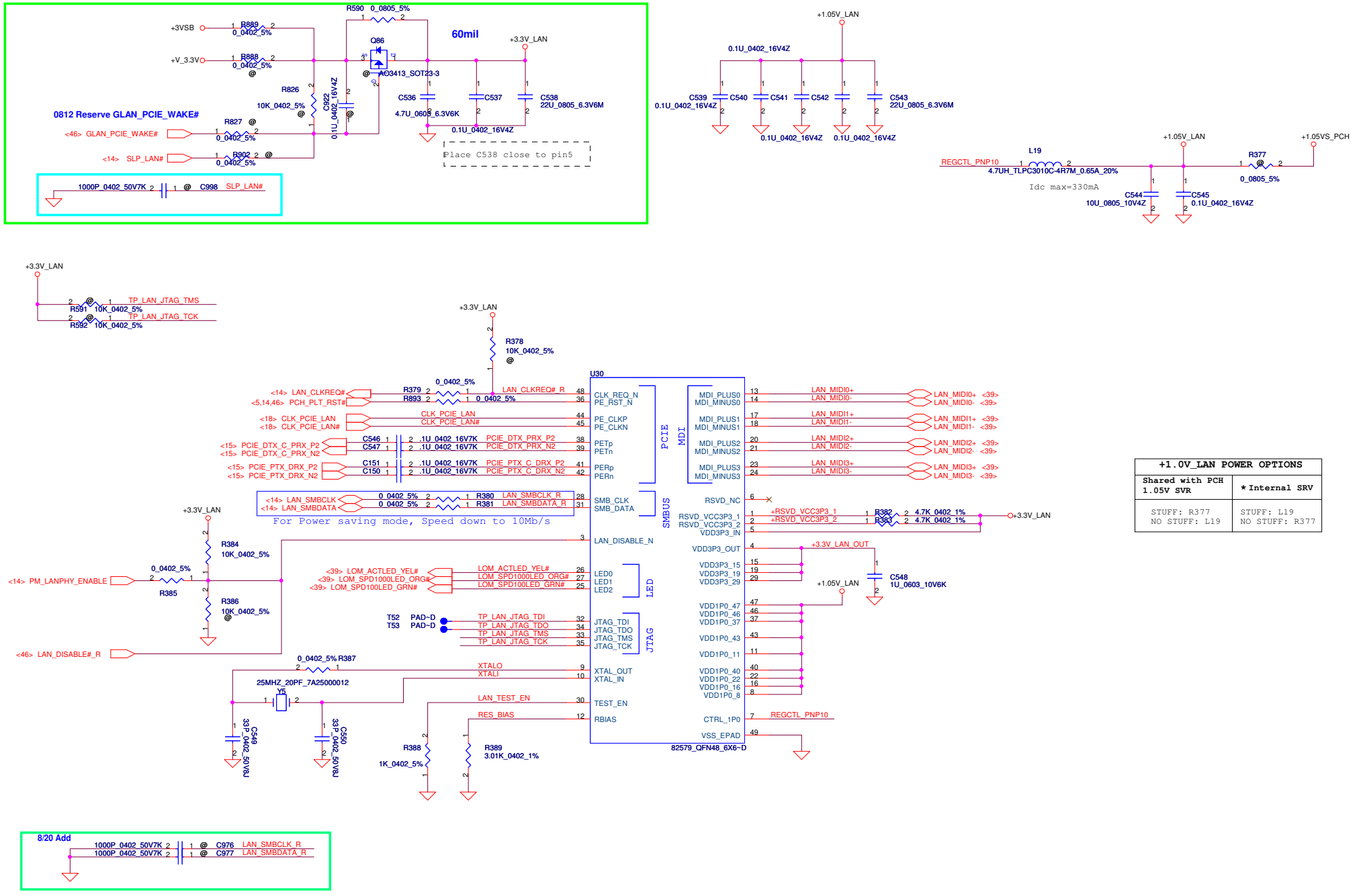

+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R377 NO STUFF: L19	STUFF: L19 NO STUFF: R377

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Intel LAN-82579

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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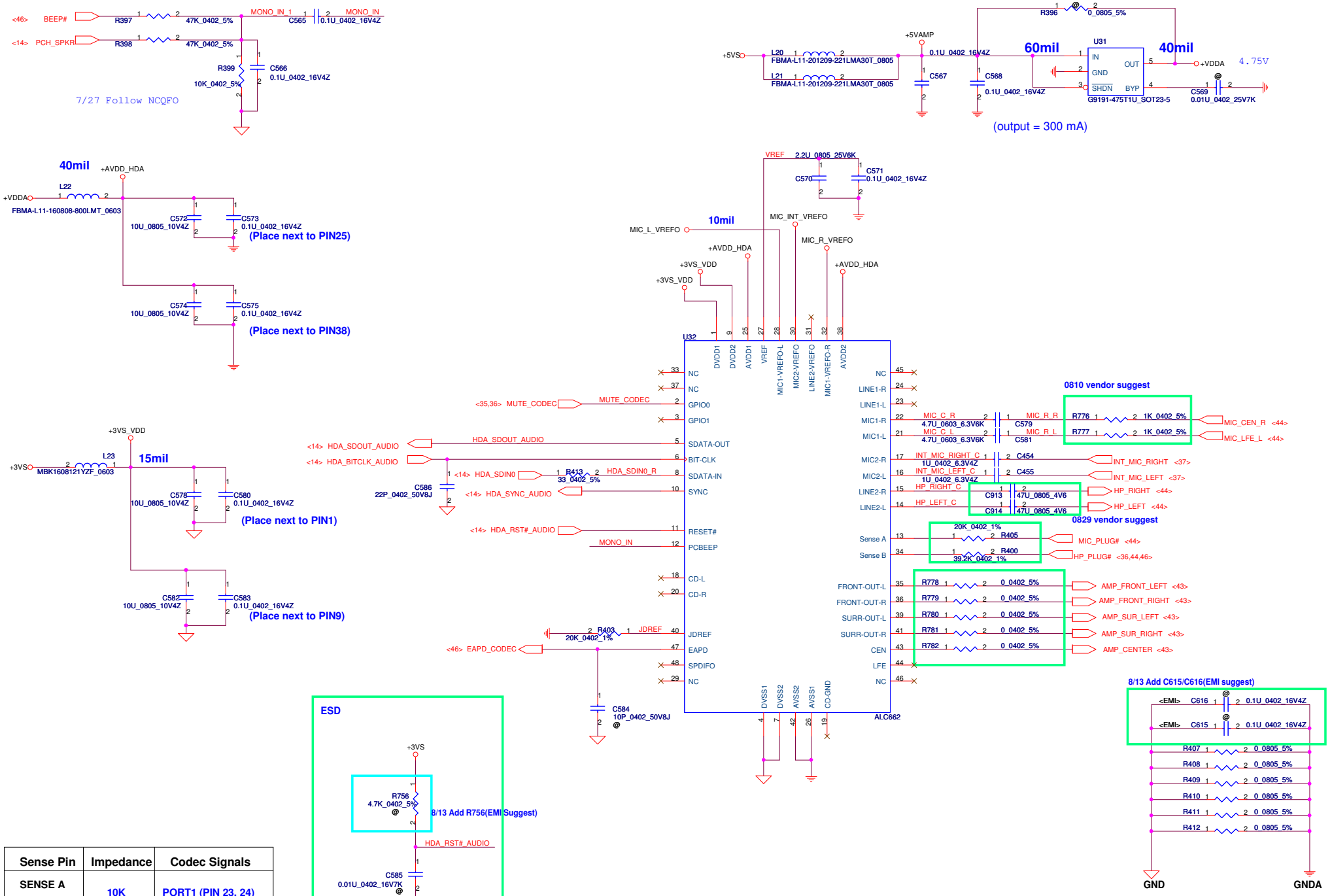

Sense Pin	Impedance	Codec Signals
SENSE A	10K	PORT1 (PIN 23, 24)
SENSE B	20K	PORT-2 (PIN 16, 17)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: HD Audio Codec ALC662

Size	Document Number	Rev
B	*PIA00 M/B LA-6951P Schematic*	0.1

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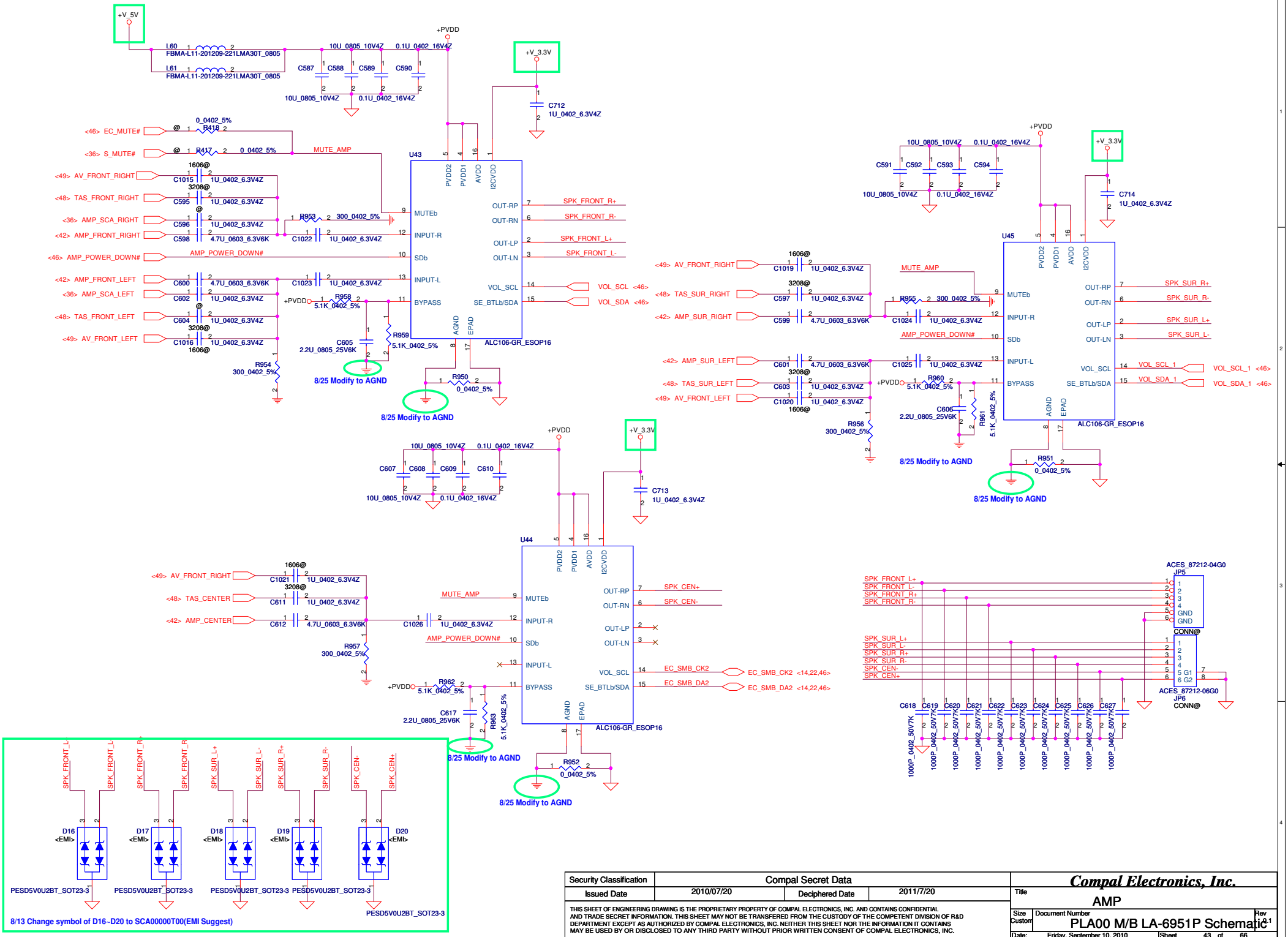


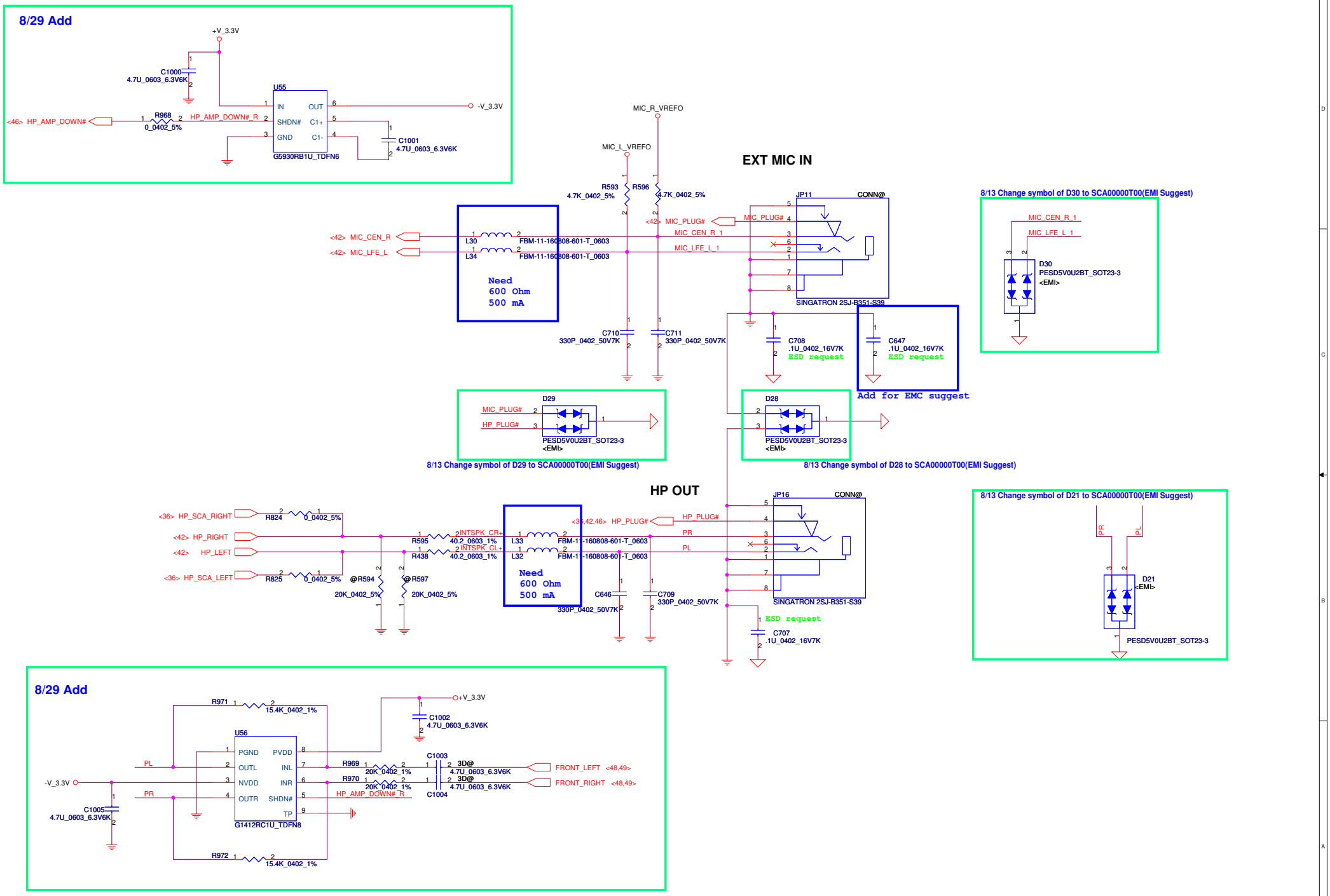
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/7/20

Compal Electronics, Inc.

Title: AMP

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 43 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Audio Jack

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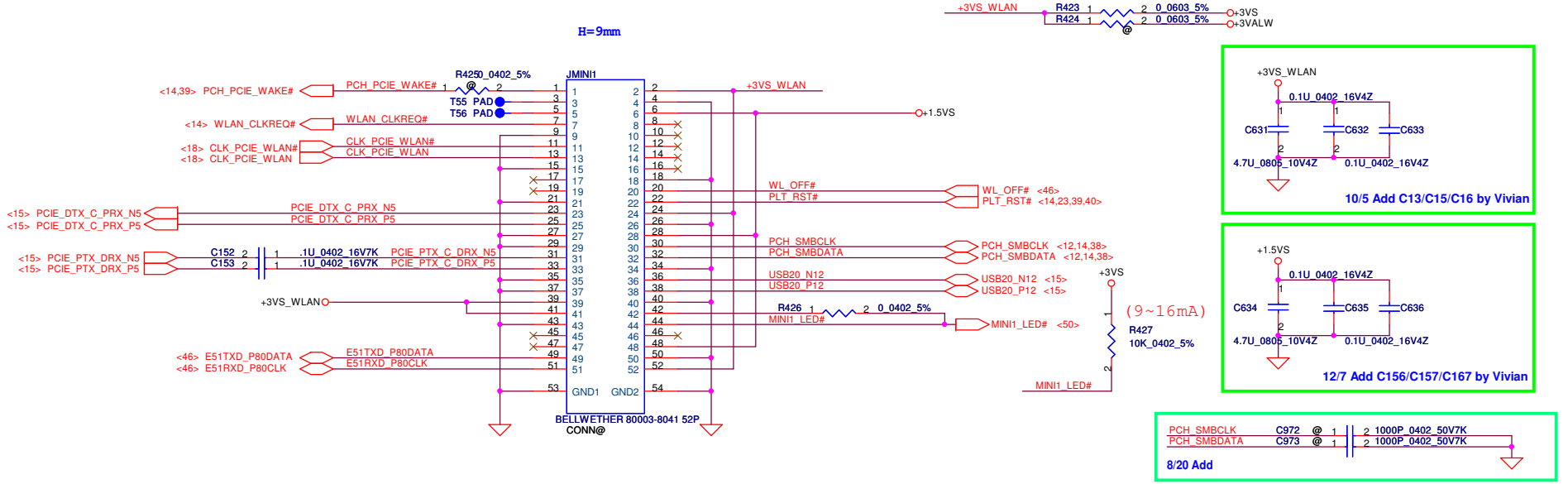
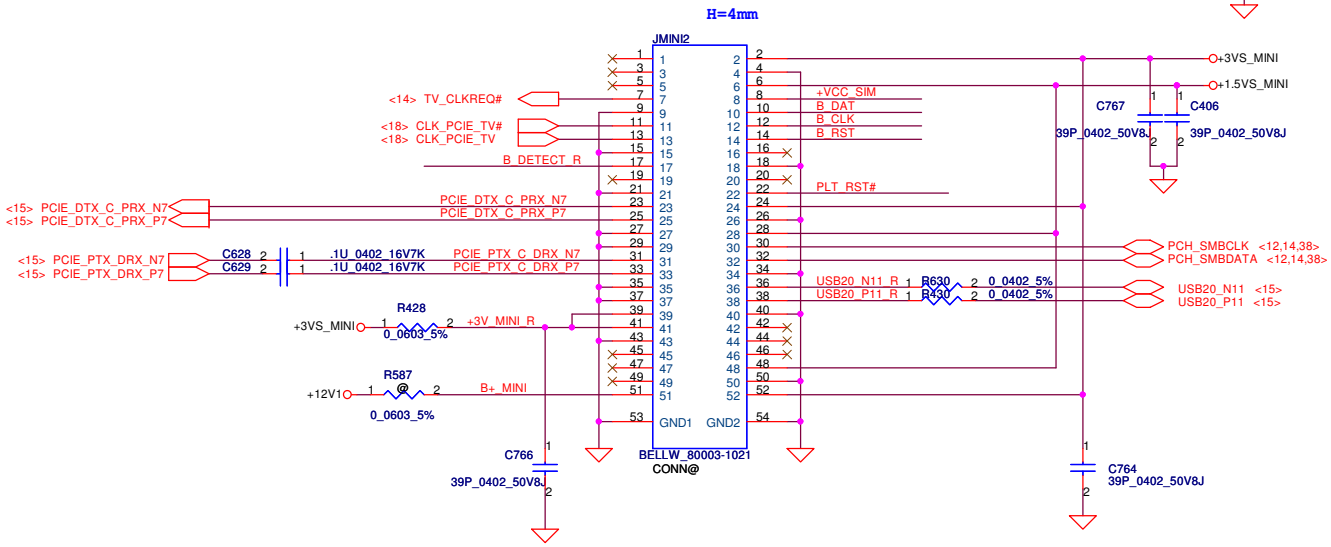
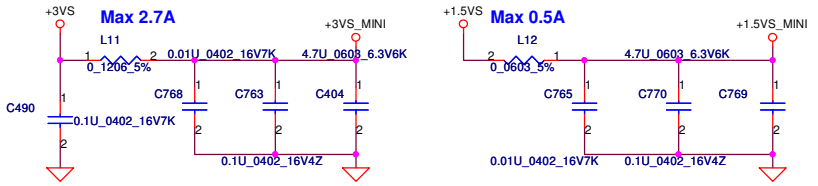
WLAN

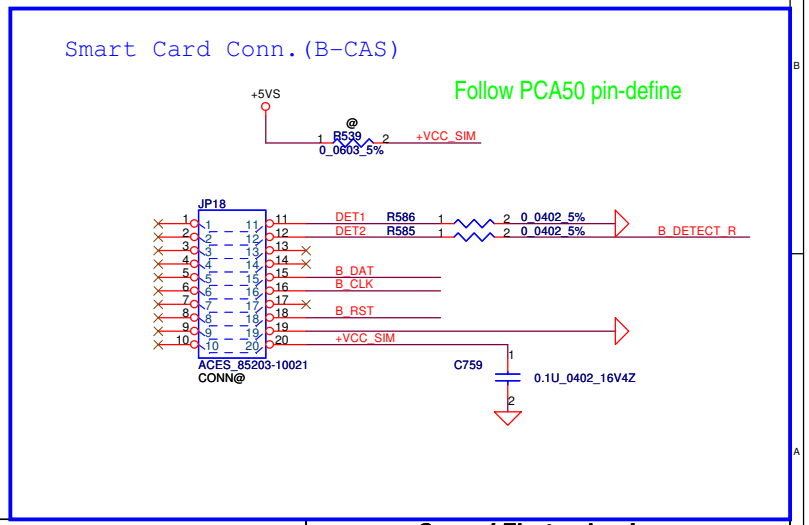


MINI

Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA







PCH_SMBCLK C974 @ 1000P_0402_50V7K
PCH_SMBDATA C975 @ 1000P_0402_50V7K
8/20 Add

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title	WLAN&MINI
Size / Document Number	Custom / PLA00 M/B LA-6951P Schematic
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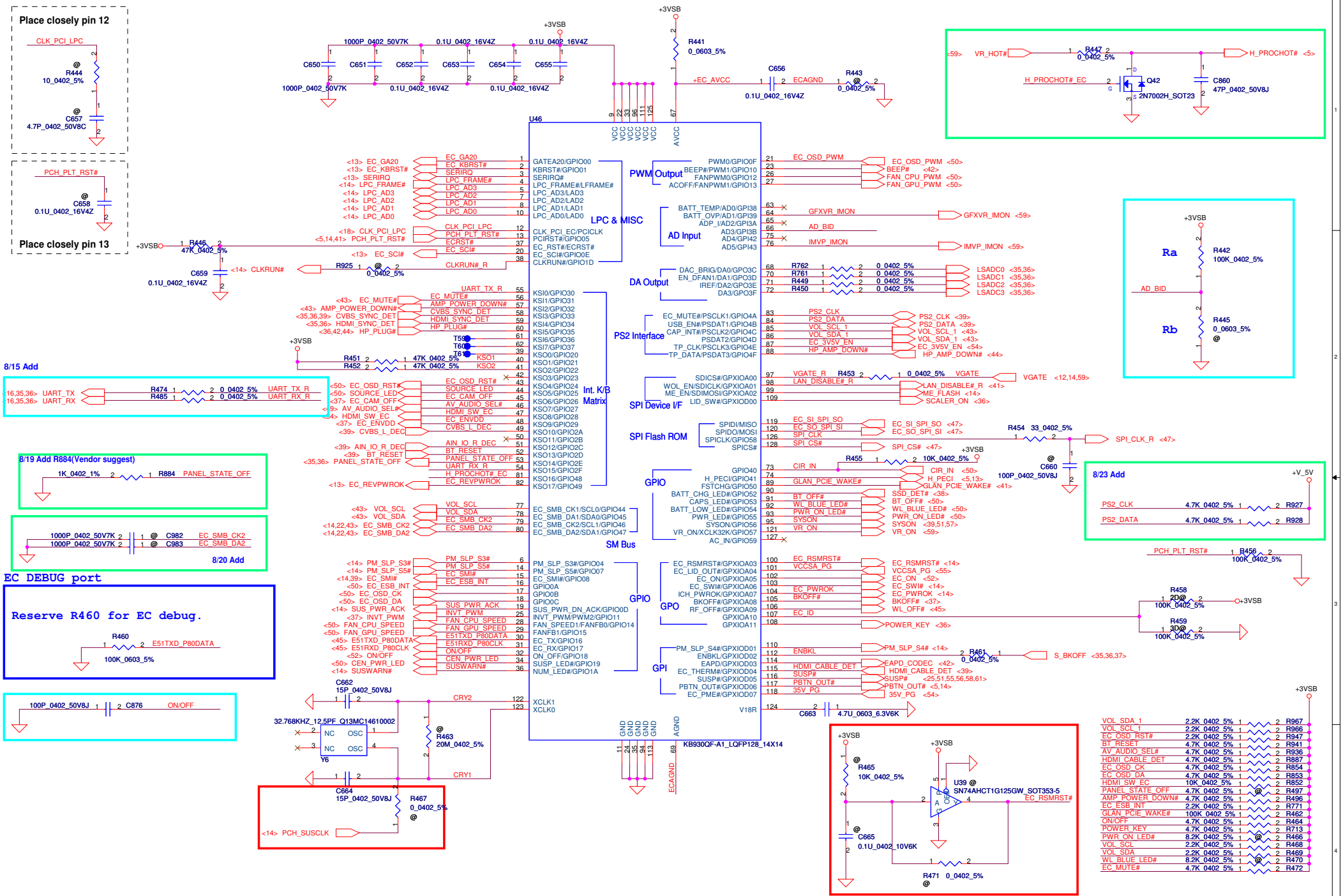

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: EC KB930/KB conn

Size	Document Number	Rev
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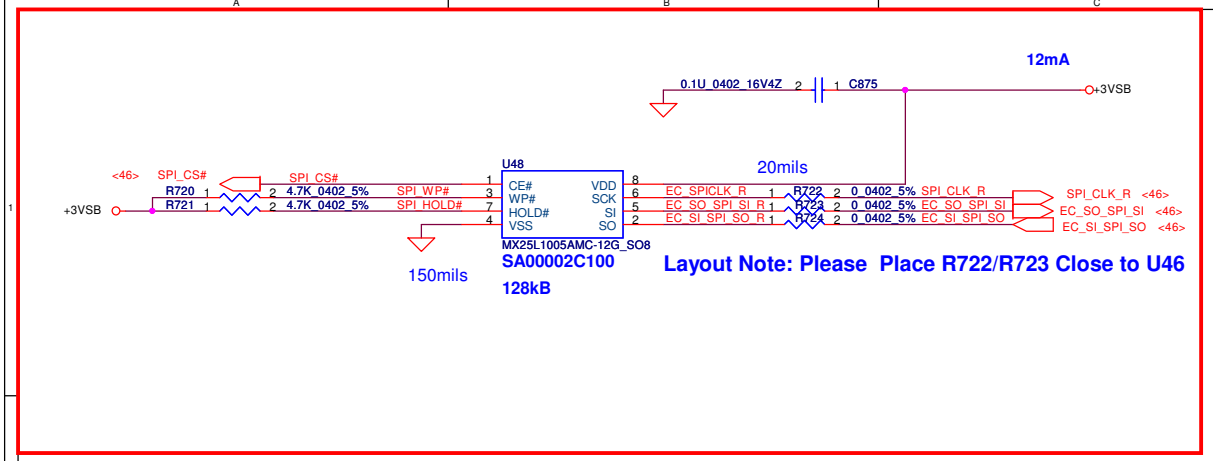
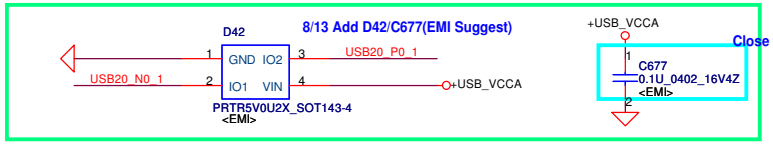
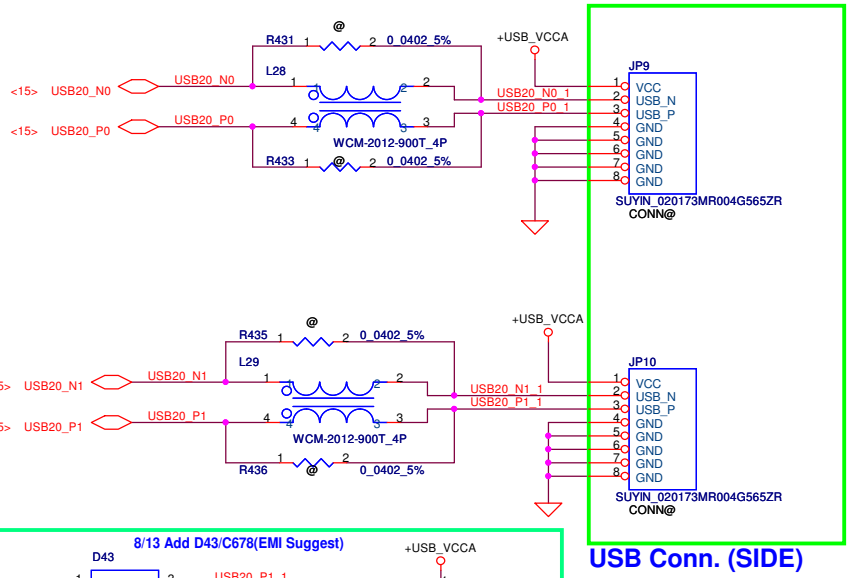
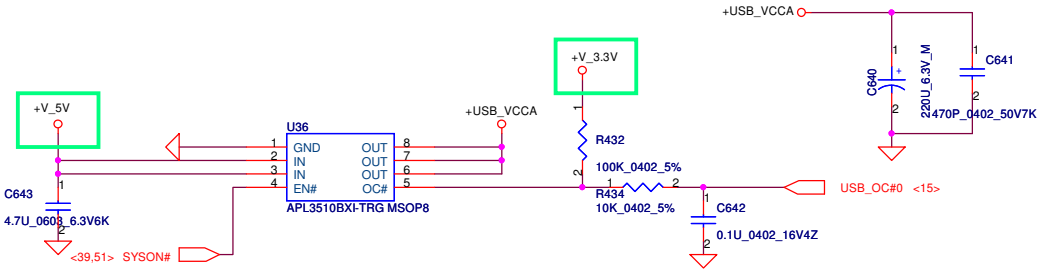
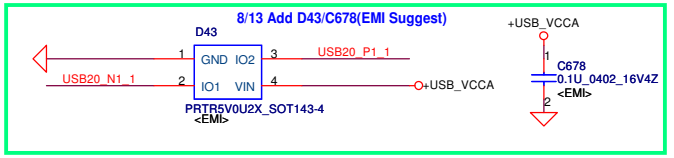
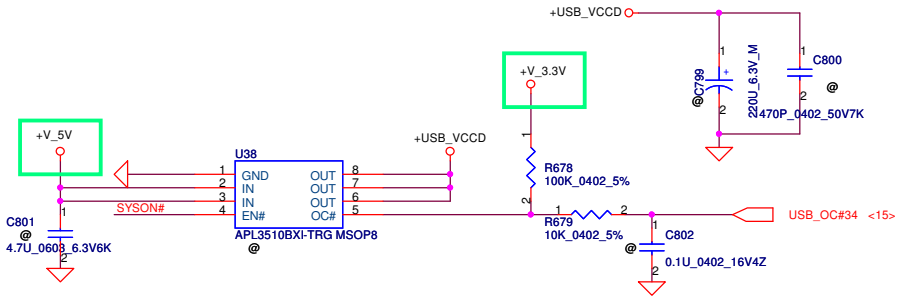












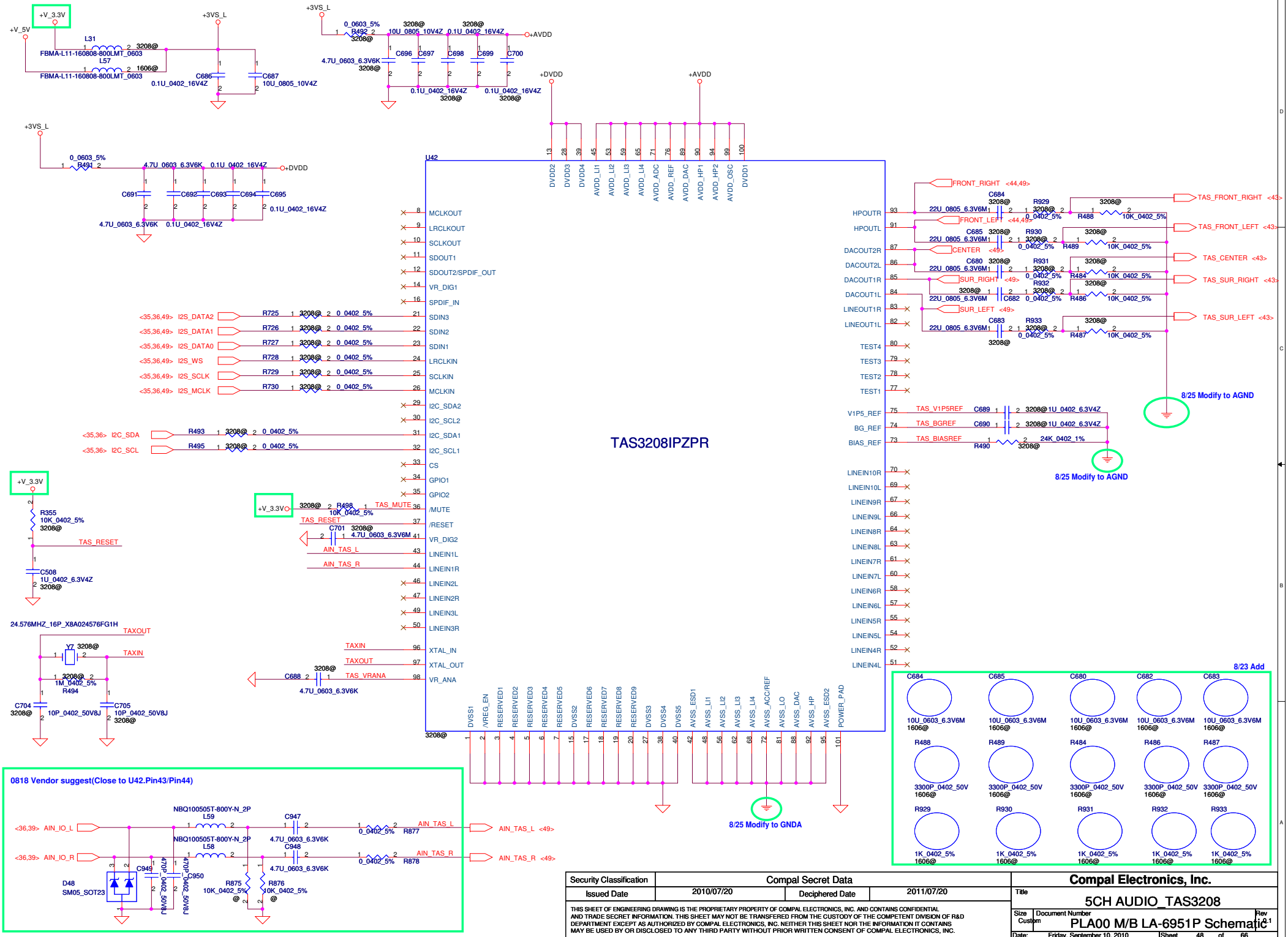
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: USB / BIOS ROM

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 Sheet 47 of 66


TAS3208IPZPR
U42
+V_3.3V
+V_5V
+3VS_L
+AVDD
+DVDD
L31
FBMA-L11-160808-800LMT_0603
L57
FBMA-L11-160808-800LMT_0603
C686 0.1U_0402_16V4Z
C687 10U_0805_10V4Z
R492 0_0603_5%
C696 C697 C698 C699 C700 4.7U_0603_6.3V6K
R491 0_0603_5%
C691 C692 C693 C694 C695 4.7U_0603_6.3V6K 0.1U_0402_16V4Z
DVDD2 DVDD3 DVDD4 AVDD_LI1 AVDD_LI2 AVDD_LI3 AVDD_LI4 AVDD_ADC AVDD_REF AVDD_DAC AVDD_HP1 AVDD_HP2 AVDD_OSC DVDD1
MCLKOUT LRCLKOUT SCLKOUT SDOUT1 SDOUT2/SPDIF_OUT VR_DIG1 SPDIF_IN
SDIN3 SDIN2 SDIN1 LRCLKIN SCLKIN MCLKIN
I2C_SDA2 I2C_SCL2 I2C_SDA1 I2C_SCL1
CS GPIO1 GPIO2 /MUTE /RESET VR_DIG2
LINEIN1L LINEIN1R LINEIN2L LINEIN2R LINEIN3L LINEIN3R
XTAL_IN XTAL_OUT VR_ANA
<35,36,49> I2S_DATA2 R725 3208@ 0_0402_5%
<35,36,49> I2S_DATA1 R726 3208@ 0_0402_5%
<35,36,49> I2S_DATA0 R727 3208@ 0_0402_5%
<35,36,49> I2S_WS R728 3208@ 0_0402_5%
<35,36,49> I2S_SCLK R729 3208@ 0_0402_5%
<35,36,49> I2S_MCLK R730 3208@ 0_0402_5%
<35,36> I2C_SDA R493 3208@ 0_0402_5%
<35,36> I2C_SCL R495 3208@ 0_0402_5%
TAS_MUTE R498 10K_0402_5%
TAS_RESET
C701 3208@ 4.7U_0603_6.3V6M
AIN_TAS_L
AIN_TAS_R
TAXIN
TAXOUT
TAS_VRANA
C688 3208@ 4.7U_0603_6.3V6K
R355 10K_0402_5%
C508 1U_0402_6.3V4Z
24.576MHZ_16P_X8A024576FG1H
Y7 3208@
R494 1M_0402_5%
C704 10P_0402_50V8J
C705 10P_0402_50V8J
DVSS1 /VREG_EN RESERVED1 RESERVED2 RESERVED3 RESERVED4 RESERVED5 DVSS2 RESERVED6 RESERVED7 RESERVED8 RESERVED9 DVSS3 DVSS4 DVSS5 AVSS_ESD1 AVSS_LI1 AVSS_LI2 AVSS_LI3 AVSS_LI4 AVSS_ACC/REF AVSS_LO AVSS_DAC AVSS_HP AVSS_ESD2 POWER_PAD
8/25 Modify to GNDA
HPOUTR HPOUTL DACOUT2R DACOUT2L DACOUT1R DACOUT1L LINEOUT1R LINEOUT1L
FRONT_RIGHT <44,49>
FRONT_LEFT <44,49>
CENTER <49>
SUR_RIGHT <49>
SUR_LEFT <49>
C684 C685 C680 C682 C683 22U_0805_6.3V6M
R929 R930 R931 R932 R933 0_0402_5%
R488 R489 R484 R486 R487 10K_0402_5%
TAS_FRONT_RIGHT <43>
TAS_FRONT_LEFT <43>
TAS_CENTER <43>
TAS_SUR_RIGHT <43>
TAS_SUR_LEFT <43>
8/25 Modify to AGND
TEST4 TEST3 TEST2 TEST1
V1P5_REF BG_REF BIAS_REF
TAS_V1P5REF C689 1U_0402_6.3V4Z
TAS_BGREF C690 1U_0402_6.3V4Z
TAS_BIASREF R490 24K_0402_1%
8/25 Modify to AGND
LINEIN10R LINEIN10L LINEIN9R LINEIN9L LINEIN8R LINEIN8L LINEIN7R LINEIN7L LINEIN6R LINEIN6L LINEIN5R LINEIN5L LINEIN4R LINEIN4L
8/23 Add
C684 C685 C680 C682 C683 10U_0603_6.3V6M 1606@
R488 R489 R484 R486 R487 3300P_0402_50V 1606@
R929 R930 R931 R932 R933 1K_0402_5% 1606@
0818 Vendor suggest(Close to U42.Pin43/Pin44)
NBQ100505T-800Y-N_2P
L59 L58
C947 C948 4.7U_0603_6.3V6K
C949 C950 470P_0402_50V8J
D48 SM05_SOT23
R875 R876 10K_0402_5%
<36,39> AIN_IO_L
<36,39> AIN_IO_R
AIN_TAS_L R877 0_0402_5%
AIN_TAS_R R878 0_0402_5%
AIN_TAS_L <49>
AIN_TAS_R <49>
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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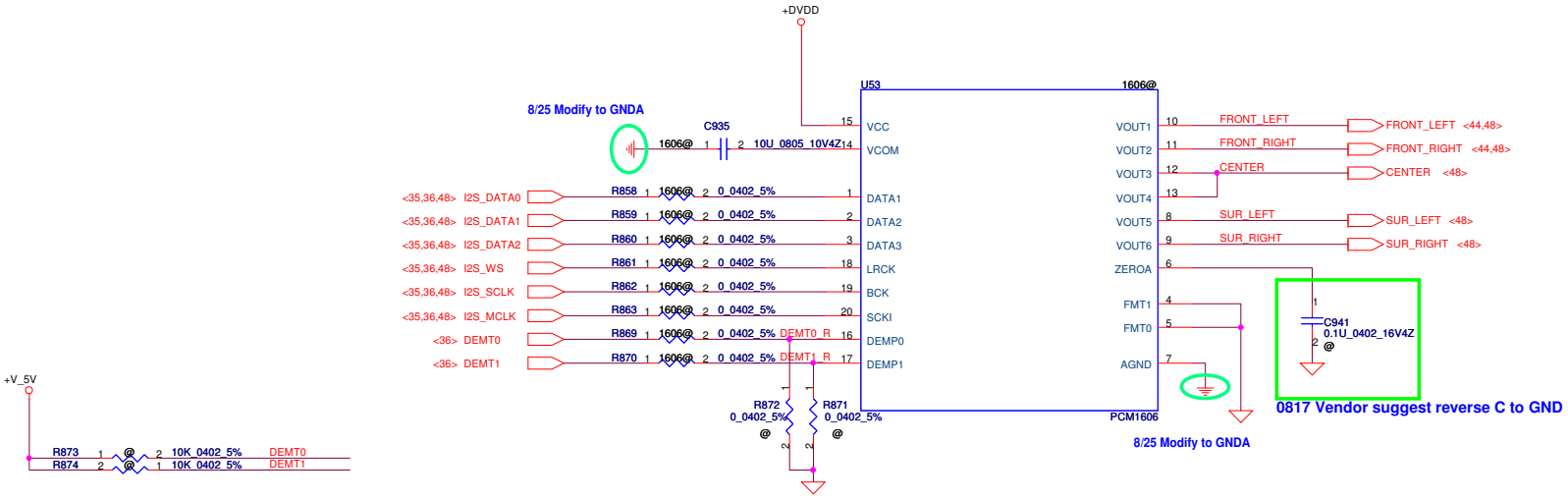
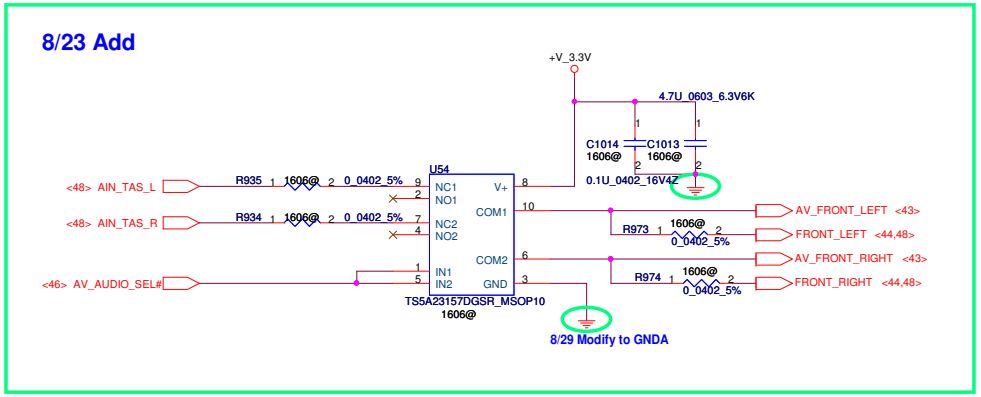
Title
5CH AUDIO_TAS3208
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
Rev
2.1
Date:
Friday, September 10, 2010
Sheet
48
of
66





De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 5CH AUDIO_PCM1606

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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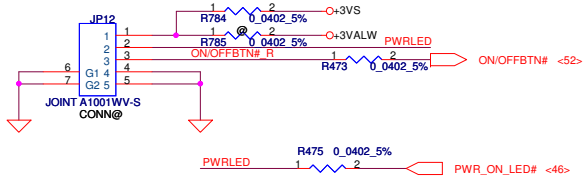
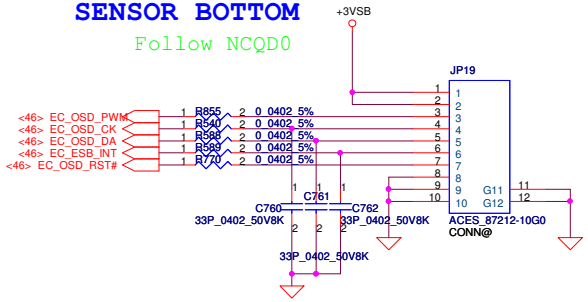
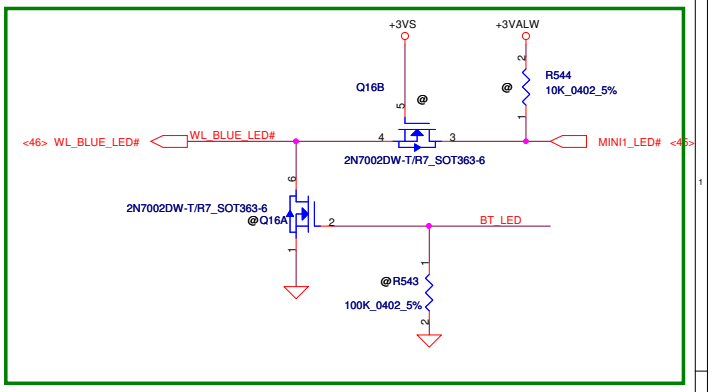
Power switch board



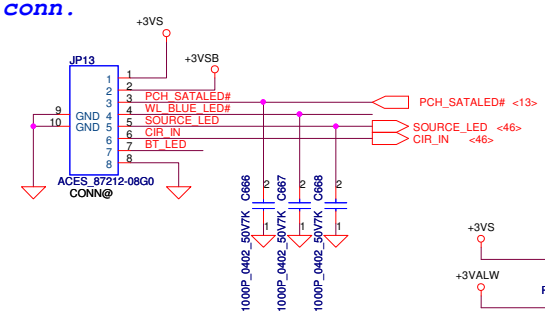
SENSOR BOTTOM

Follow NCQD0

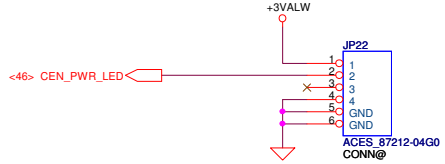


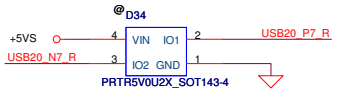


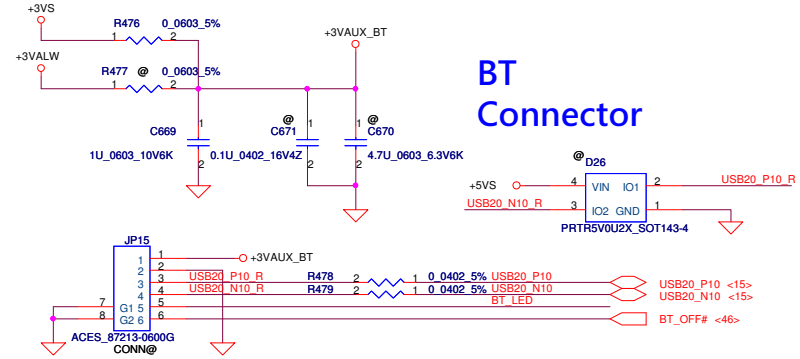
LED board conn.



DECO LED board conn.

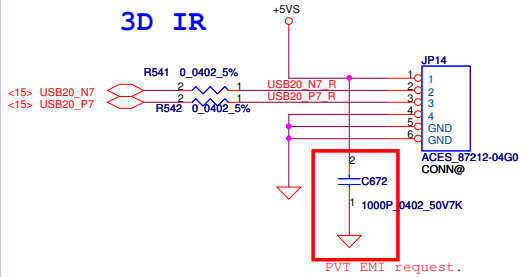


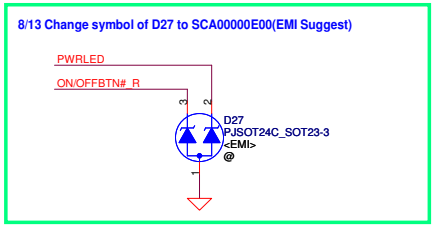




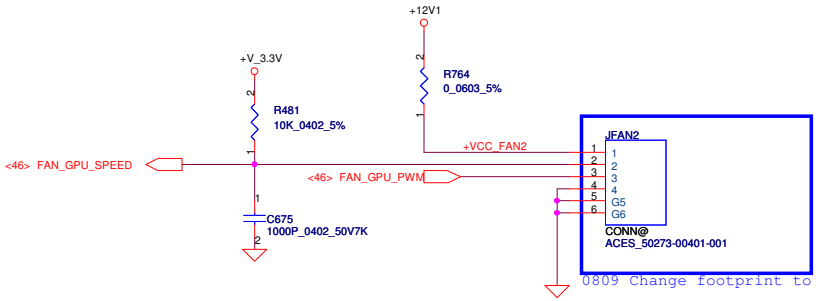
BT Connector

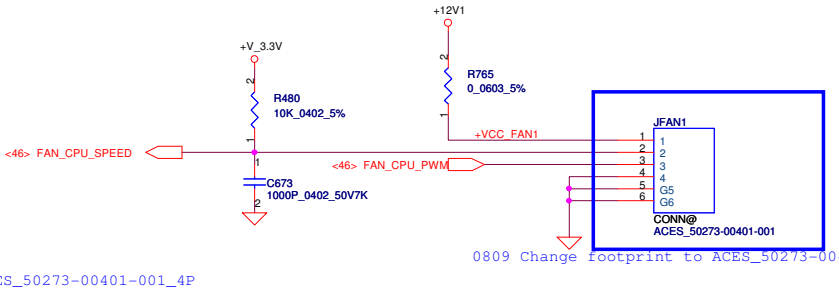
3D IR





Fan Control circuit





Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: WL/BT ON/OFF, PWR S/W, OSD

Size	Document Number	Rev
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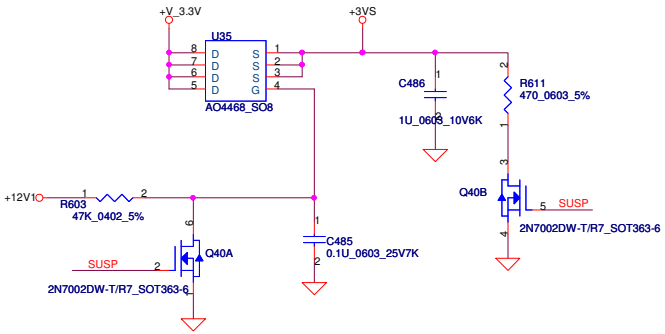
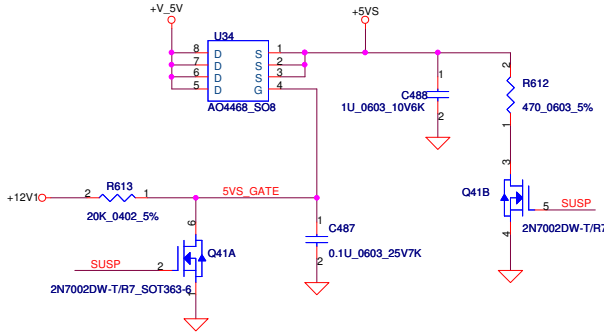
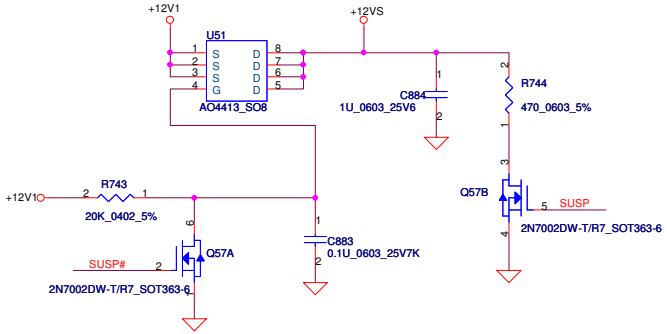
+V_3.3V TO +3VS



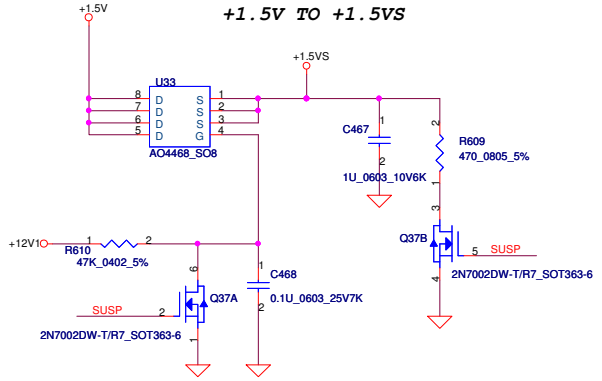
+V_5V TO +5VS

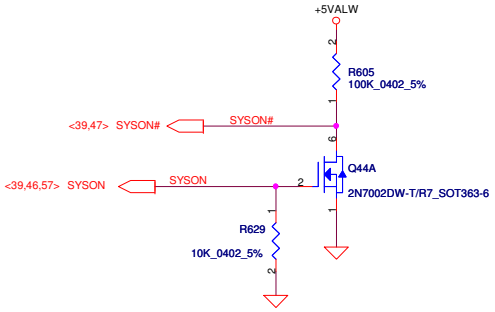


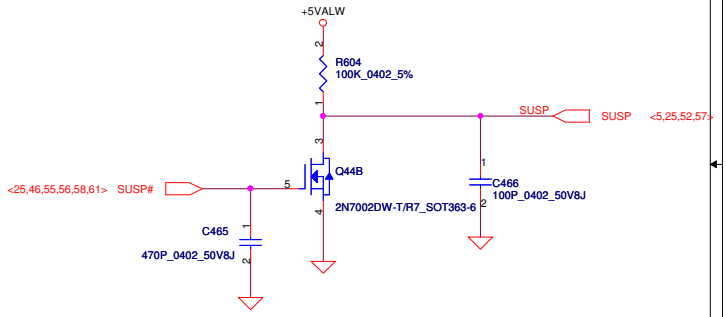
+12V1 TO +12VS



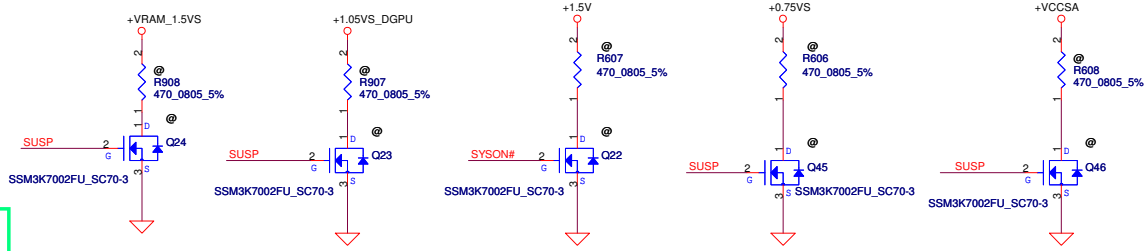
+1.5V TO +1.5VS



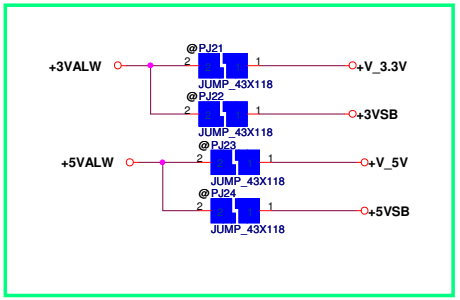




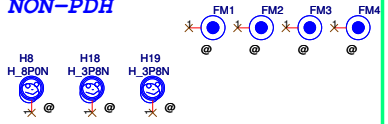
Discharge circuit



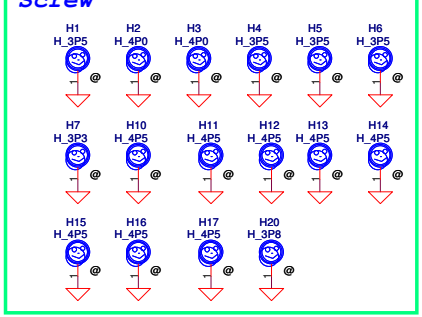
0810 Change to single channel MOS



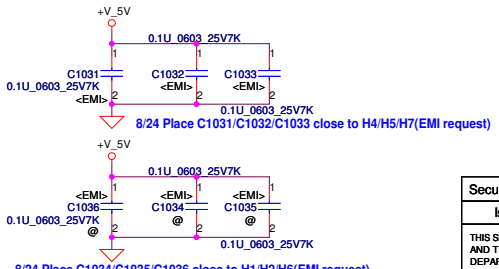
NON-PDH



Screw



8/24 Add C1031~C1036



8/24 Place C1031/C1032/C1033 close to H4/H5/H7(EMI request)

8/24 Place C1034/C1035/C1036 close to H1/H2/H6(EMI request)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: DC Interface/Screw

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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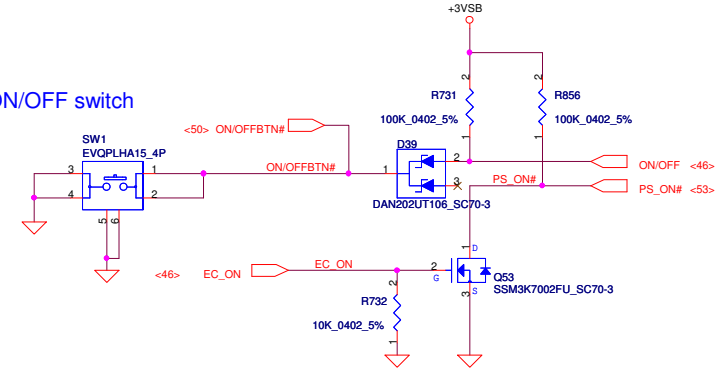
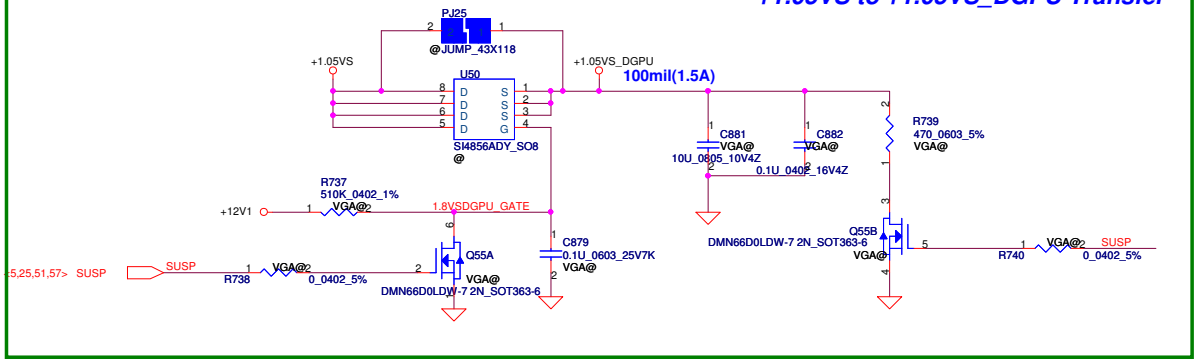
Power Button

ON/OFF switch



+1.05VS to +1.05VS_DGPU Transfer



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Power OK/PBN

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

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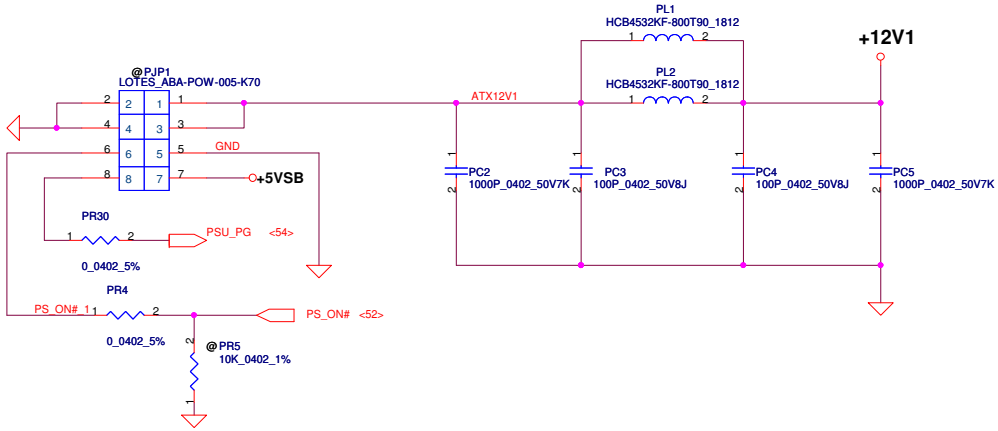
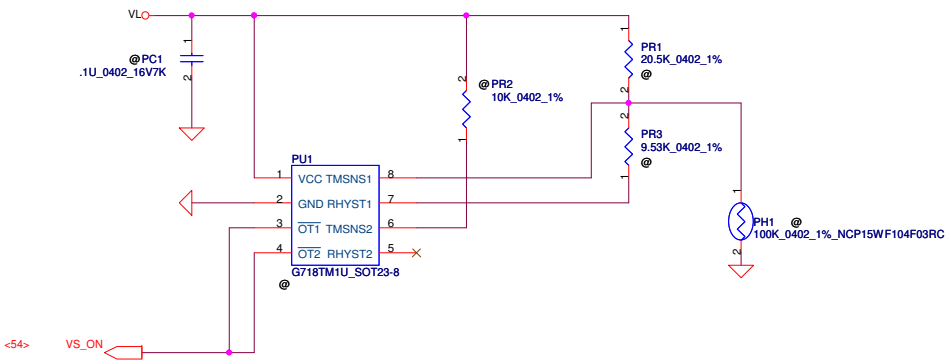
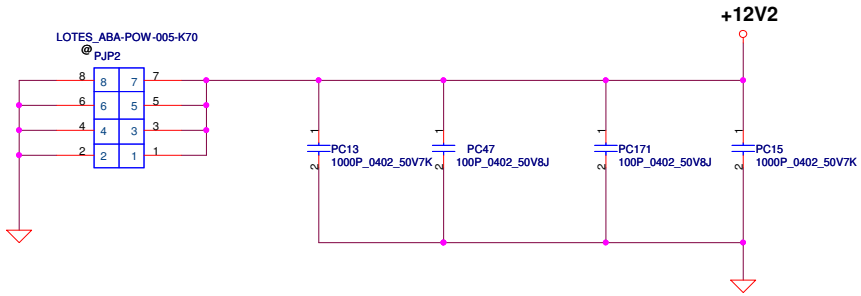
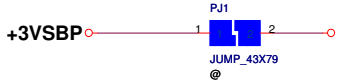
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C

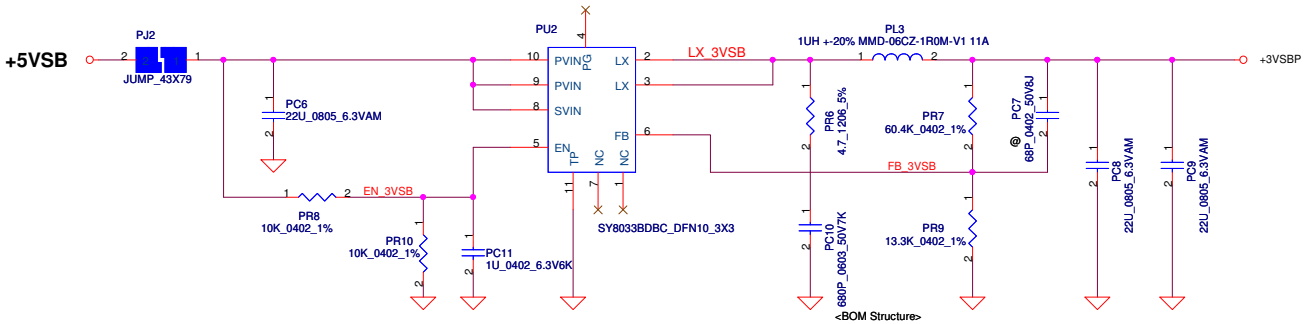








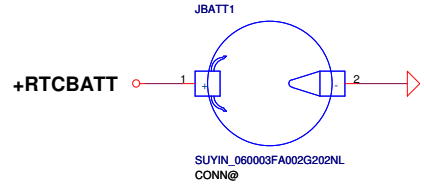
FOR EC suspend



VFB=0.6V
Vo=VFB*(1+PR7/PR9)=3.318 V

Ipeak=0.062A, Imax=0.045A

Current limit >4A



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title

Size	Document Number	Rev
Custom		0.1

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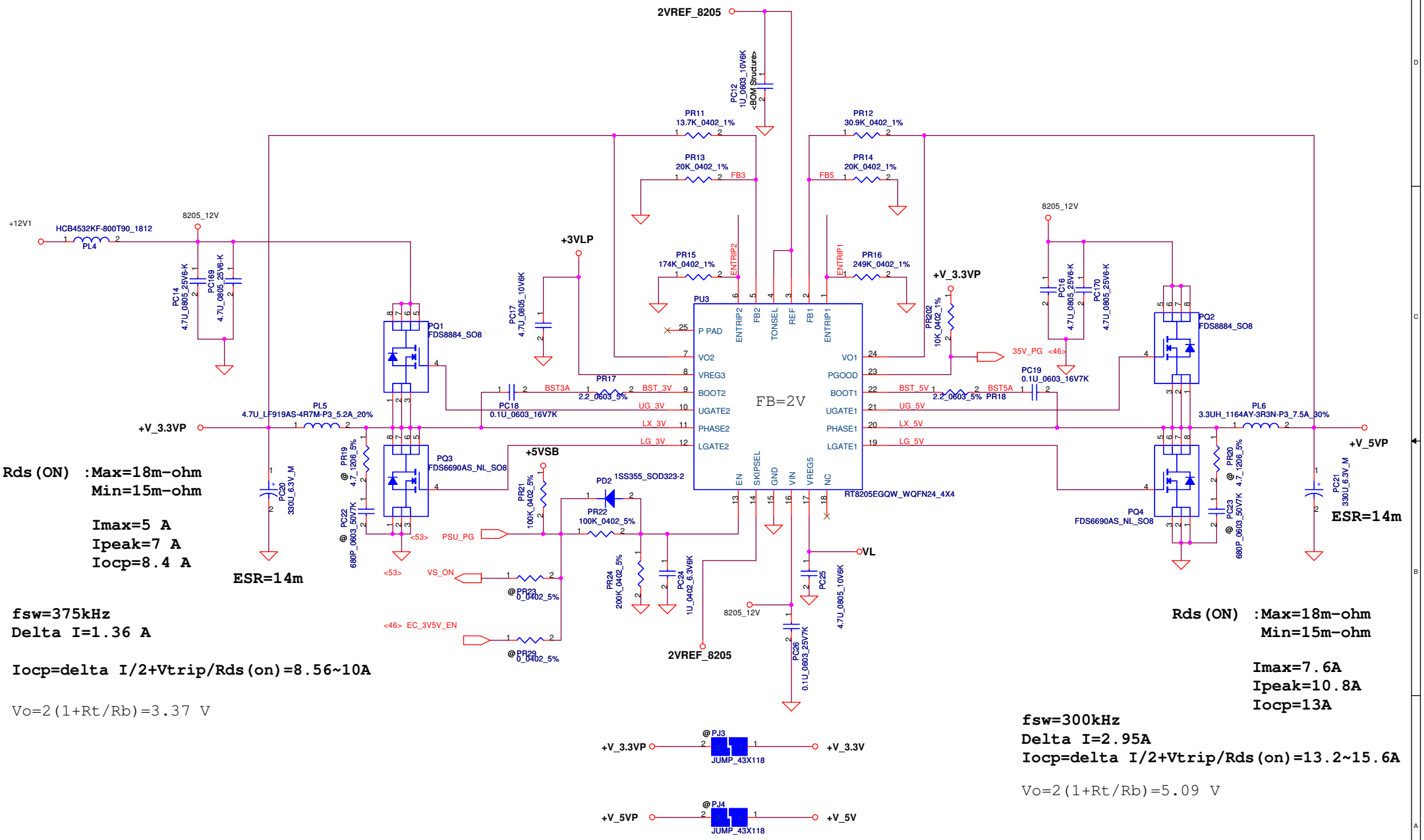


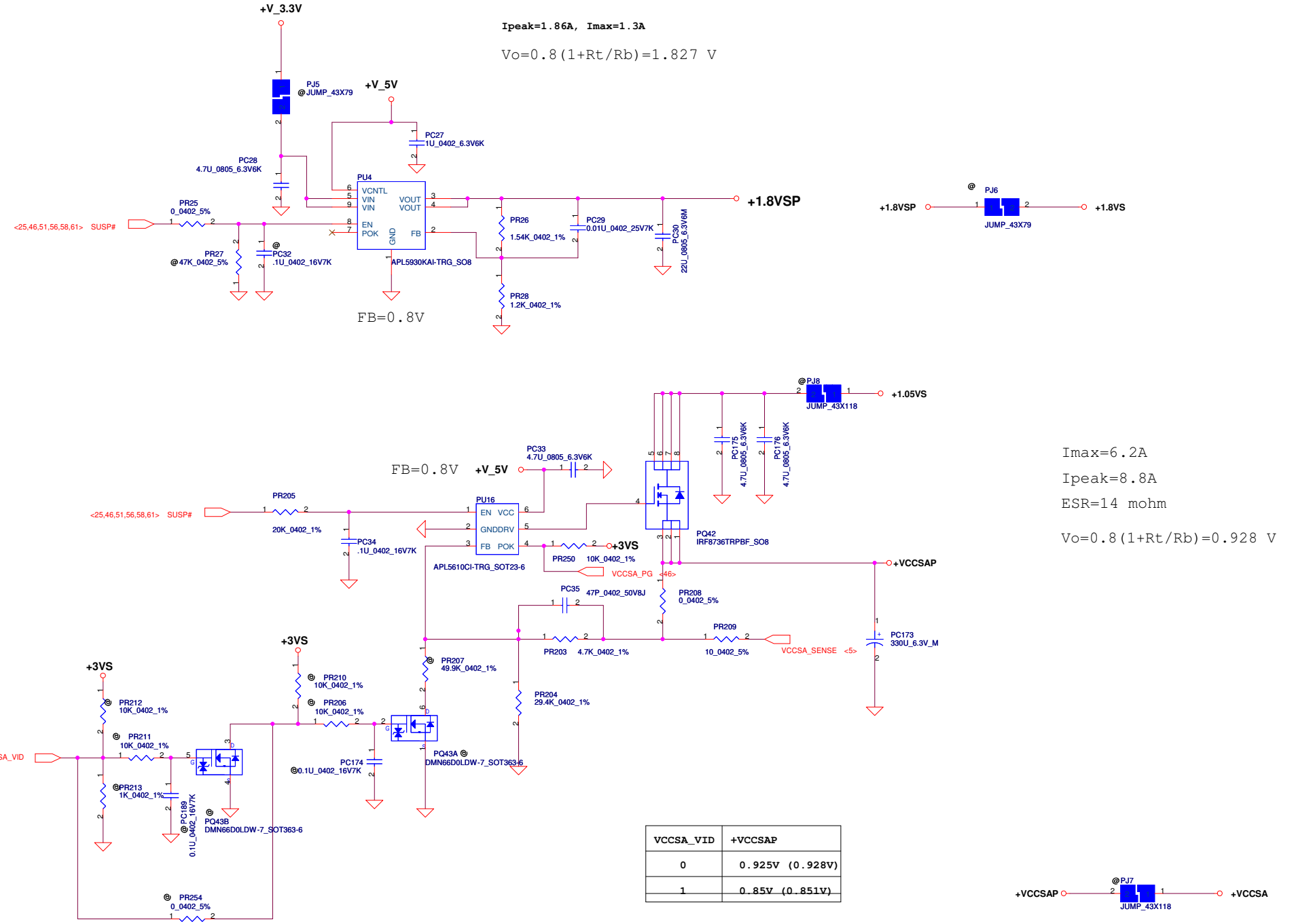
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: +V_5VP/ +V_3VP

Size: Custom | Document Number: 0.1 | Rev:

Date: Friday, September 10, 2010 | Sheet 54 of 66



VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

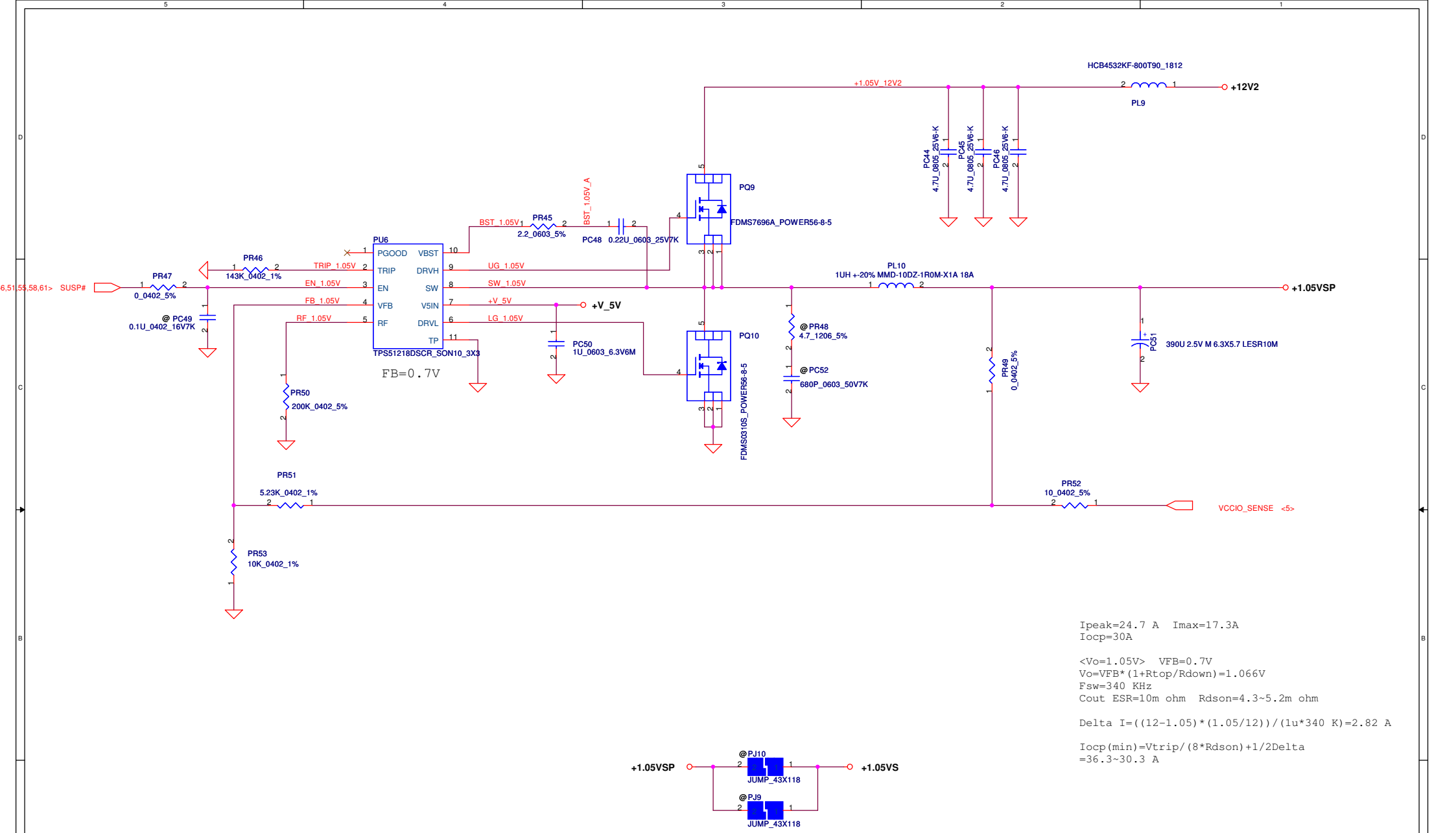
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: +VCCSA/+1.8VSP

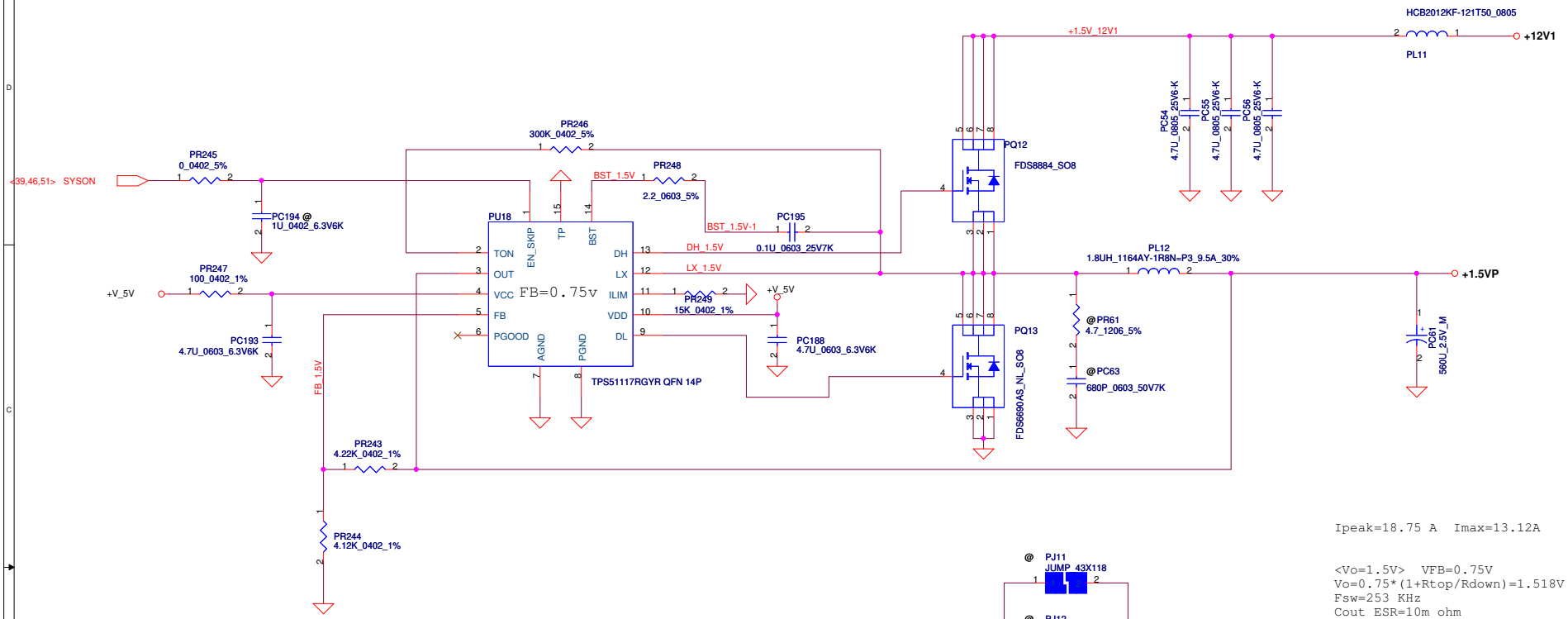
Size	Document Number	Rev
Custom		0.1

Date: Friday, September 10, 2010 | Sheet 55 of 66



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/20	Deciphered Date	2011/07/20

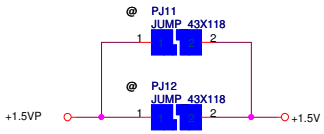
Title	+1.05VSP		
Size	Document Number		Rev
Custom			0.1
Date:	Friday, September 10, 2010	Sheet	56 of 66

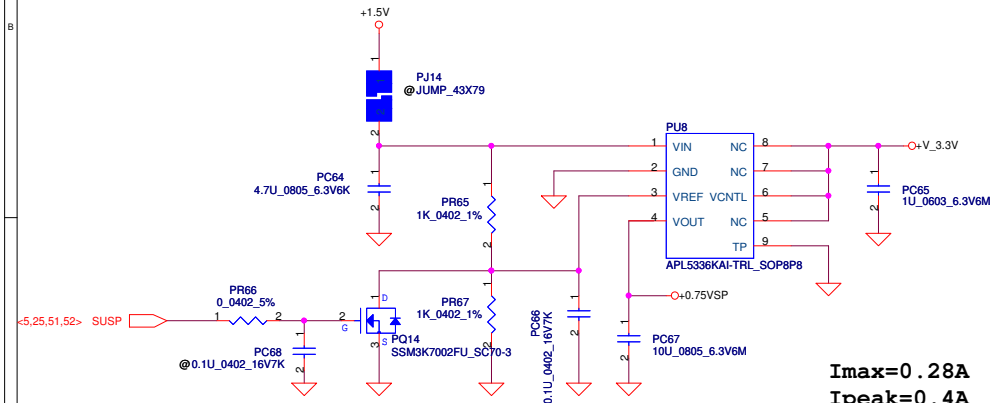


Ipeak=18.75 A Imax=13.12A

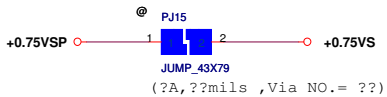
<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+Rtop/Rdown)=1.518V
Fsw=253 KHz
Cout ESR=10m ohm
Rdson=12~15 m ohm

Delta I=2.63 A
=>1/2DeltaI=1.44A
Vtrip=165 mV
Iocp=13.9~10.6 A





Imax=0.28A
Ipeak=0.4A



(?A,??mils ,Via NO.= ??)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 1.5VP/+1.2VALWP/+0.75VS

Size	Document Number	Rev
Custom		0.1

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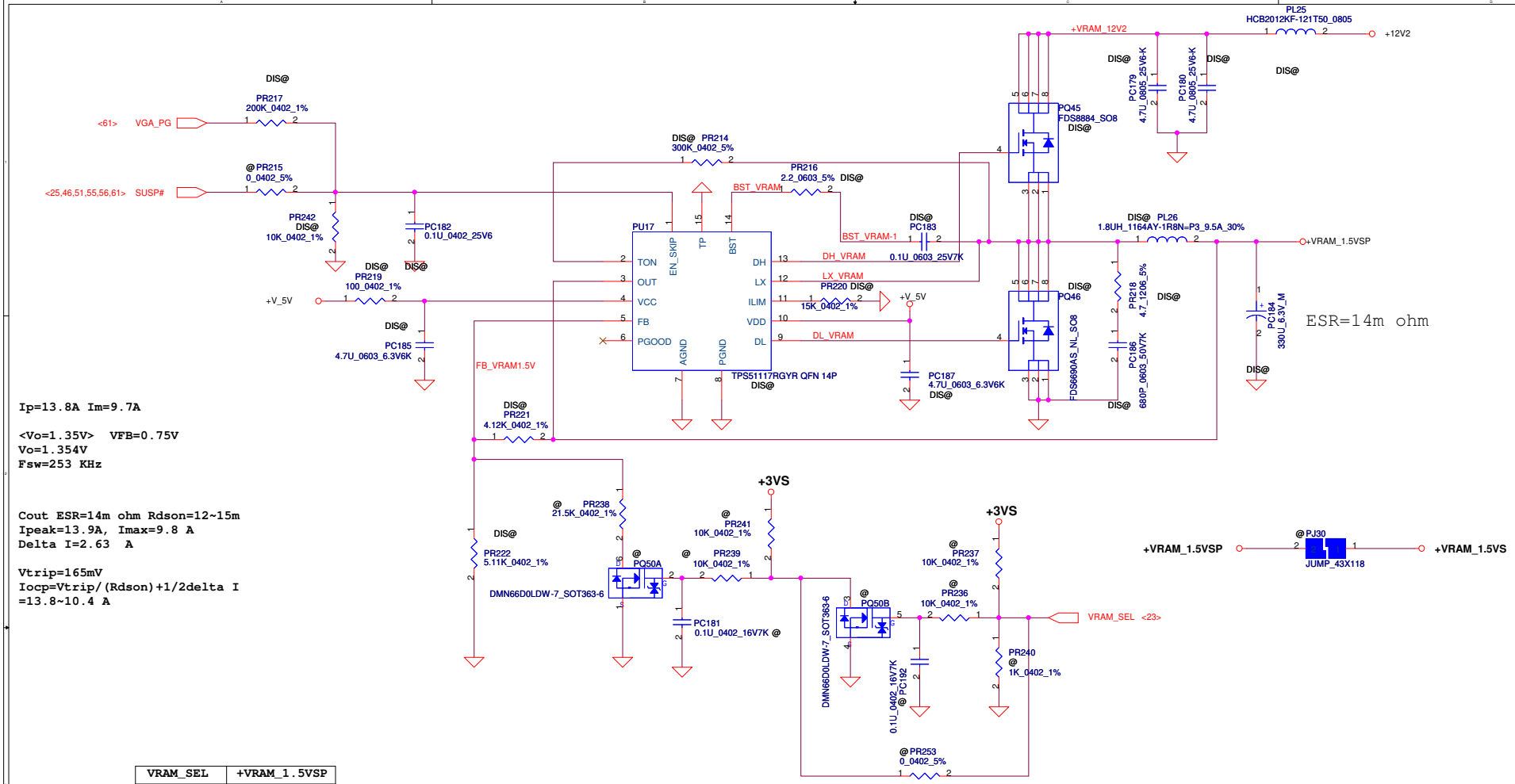
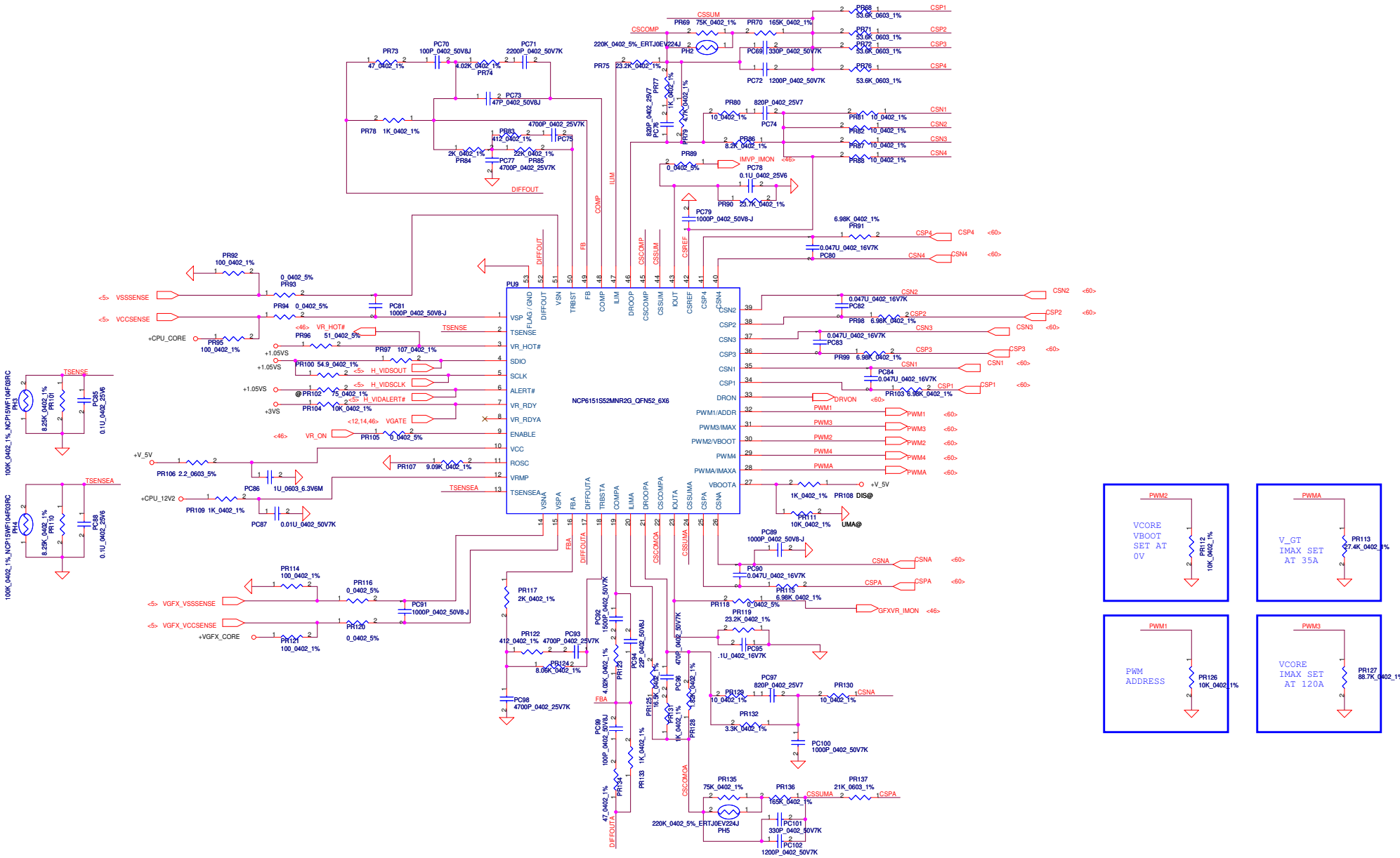


VRAM_SEL	+VRAM_1.5VSP
0	1.35V
1	1.5V

Compal Electronics, Inc.			
Title	VCCPP/1.8VP		
Size: Custom	Document Number: PLA00 M/B LA-6951P Schematic		Rev: 0.1
Date: Friday, September 10, 2010	Sheet 58 of 66		



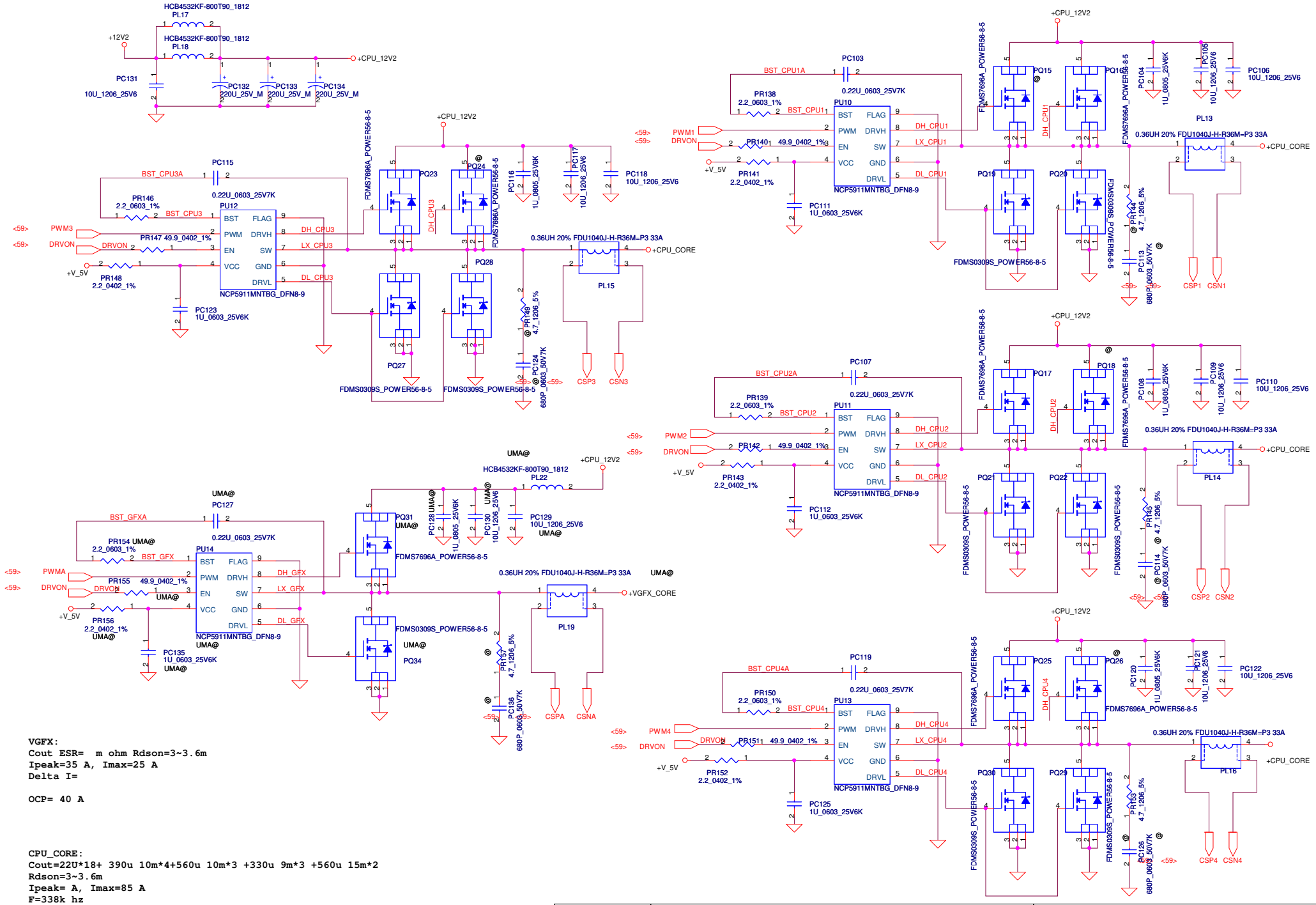
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: CPU_CORE_1

Size	Document Number	Rev
C		0.1

Date: Friday, September 10, 2010 | Sheet 59 of 66



VGFX:
Cout ESR= m ohm Rdson=3~3.6m
Ipeak=35 A, Imax=25 A
Delta I=

OCP= 40 A

CPU_CORE:
Cout=22U*18+ 390u 10m*4+560u 10m*3 +330u 9m*3 +560u 15m*2
Rdson=3~3.6m
Ipeak= A, Imax=85 A
F=338k hz
Delta I=

OCP= 135 A

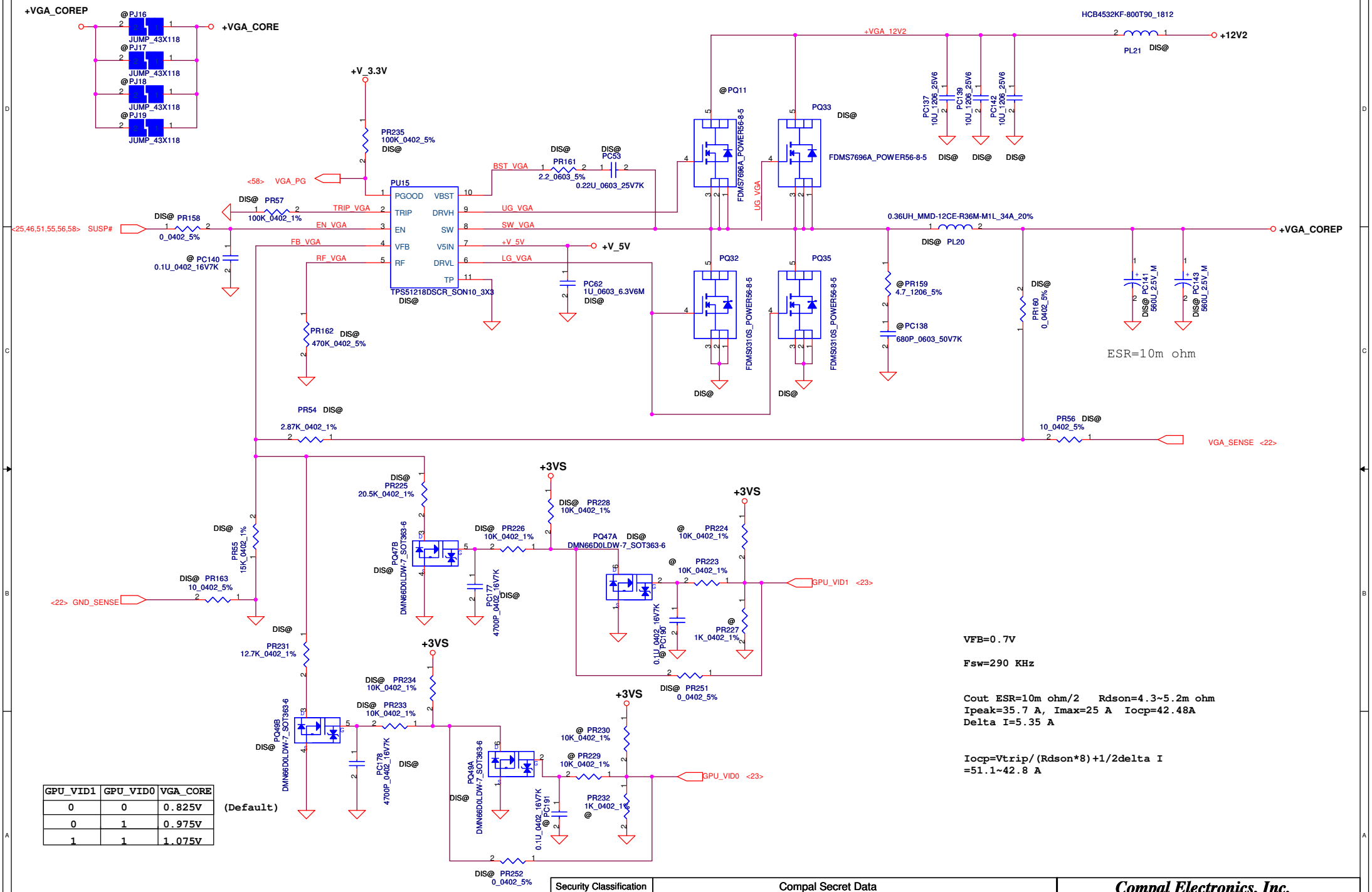
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: CPU_CORE_2

Size	Document Number	Rev
Custom		0.1

Date: Friday, September 10, 2010 | Sheet 60 of 66



GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.825V
0	1	0.975V
1	1	1.075V

(Default)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

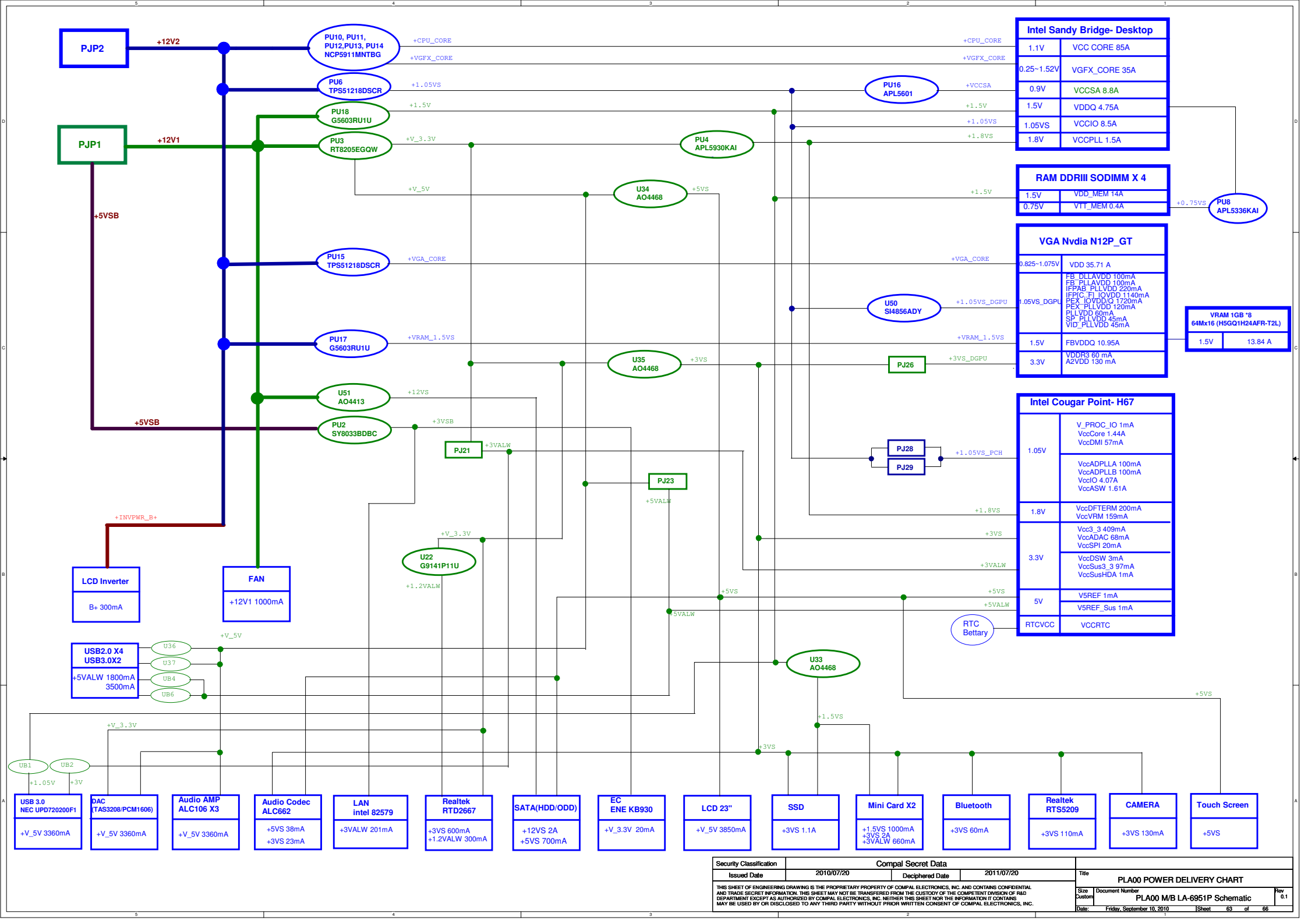
Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 61 of 66

Title	<Title>
Size: A	Document Number: PLA00 M/B LA-6951P Schematic
Rev: 0.1	
Date: Friday, September 10, 2010	Sheet 62 of 66



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

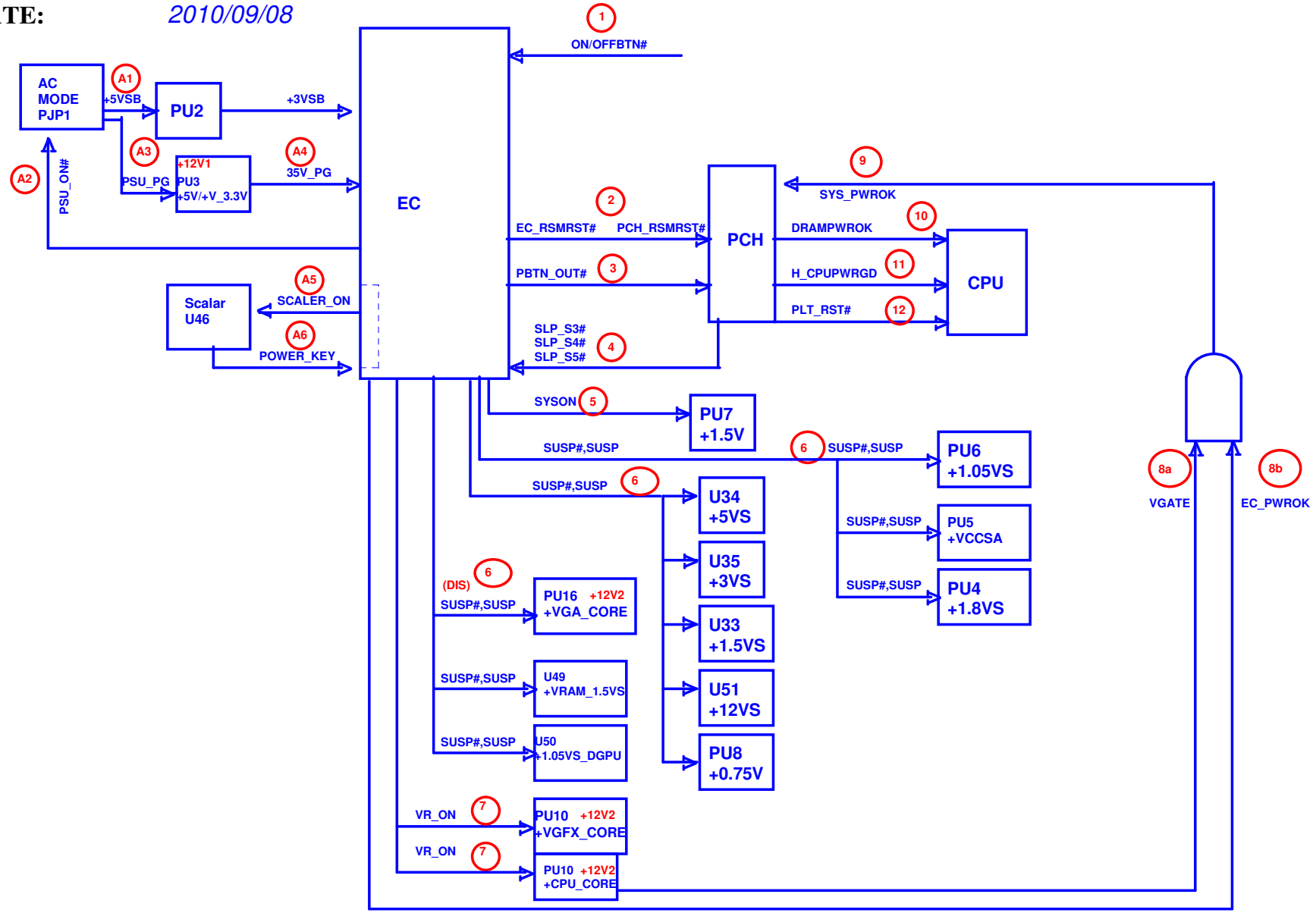
Title: PLA00 POWER DELIVERY CHART

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.1

Date: Friday, September 10, 2010 | Sheet 63 of 66

COMPAL CONFIDENTIAL

MODEL NAME: *PLA00 Power Sequence Block Diagram*
PCB NAME: *LA6951P*
REVISION: *0.1*
DATE: *2010/09/08*



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 64 of 66

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.1

Date: Friday, September 10, 2010 | Sheet 65 of 66

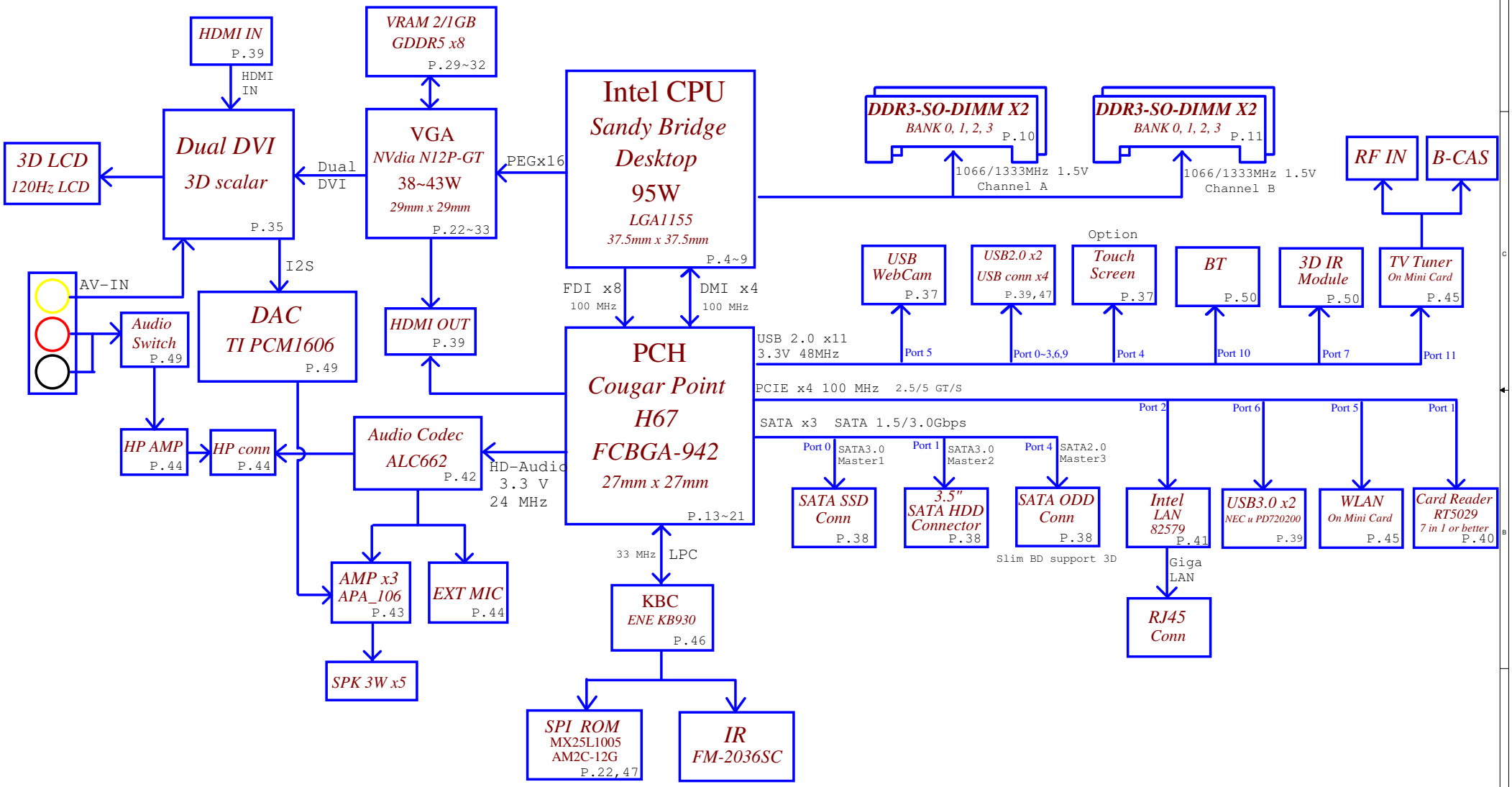
B520 (OS S5)

Power On
S5->S0

Compal Confidential

Model Name : PLA00

File Name : LA6951P



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.			
Title	Block Diagrams_3D		
Size: Custom	Document Number: M/B LA-6951P Schematic		Rev: 0.1
Date: Friday, September 10, 2010	Sheet 66 of 66		