

# MS-7511

ATX(305mm X 220mm)

## CPU:

AMD AM2/AM2+ Socket940

## System Chipset:

North Bridge --- MCP78

South Bridge --- NA

## OnBoard Chipset:

Clock Gen:NA

AZALIA Codec:ALC888

LAN Chip: REL8211BL

SIO:Fintek 71882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (MCP)

## Main Memory:

DDRII\* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 3

## PWM:

Controller:STL6740L+6741

## ACPI:

UPI solution

## Other:

FDD \*1

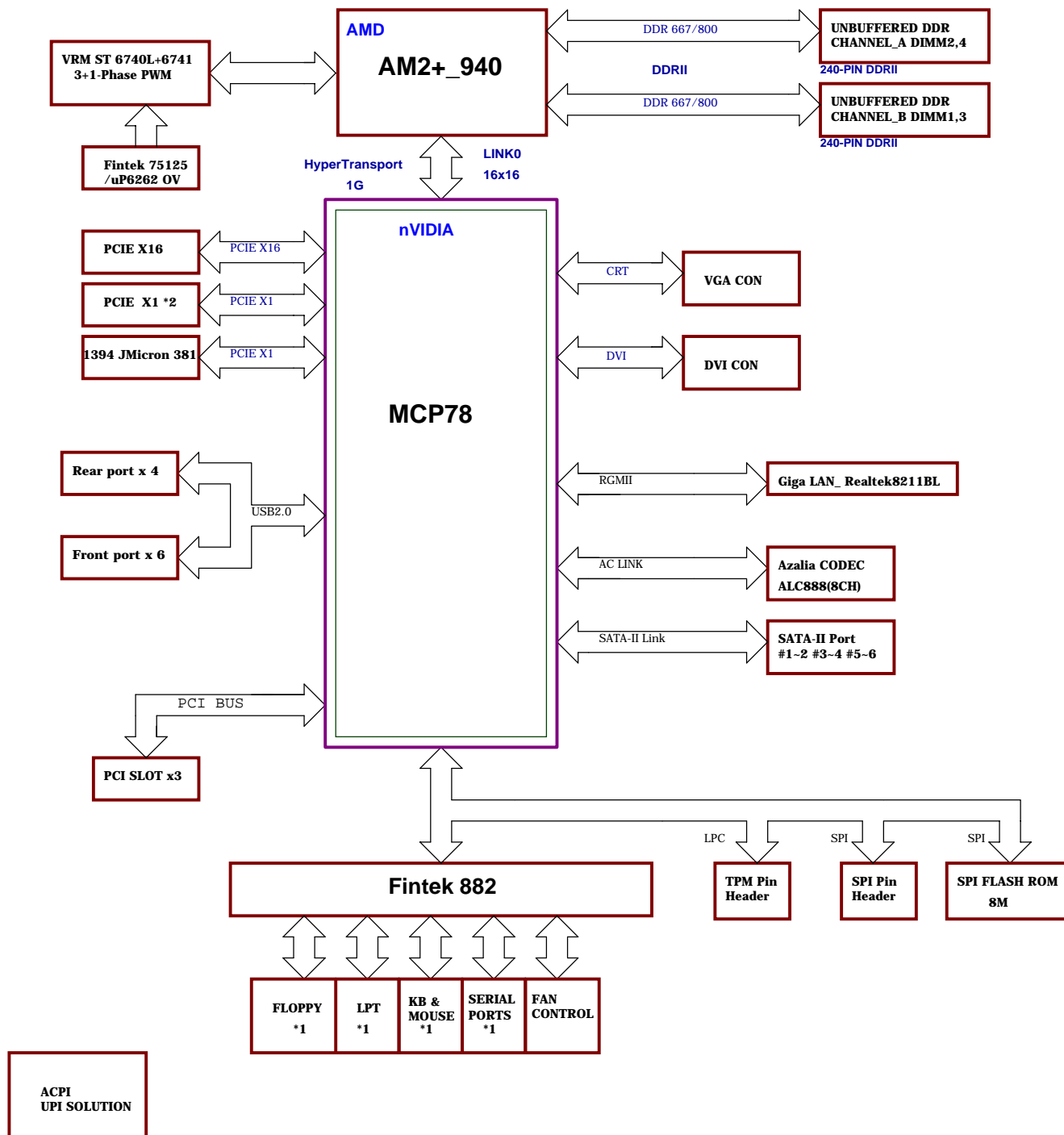
SATA(SATA2-300MB/s) \* 6

USB2.0 \*10 (Rear\*4 Front\*6)

COM PORT \*1

LPT PORT \*1

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 3 CH-A	10100010B A2H	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 2 CH-B	10100001B A4H	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	LAN_USB1	USB0- USB0+ USB1- USB1+	USB_OC0
	USB1	USB2- USB2+ USB3- USB3+	USB_OC1
Front	JUSB1	USB4- USB4+ USB5- USB5+	USB_OC3
	JUSB2	USB6- USB6+ USB7- USB7+	USB_OC4
	JUSB3	USB8- USB8+ USB9- USB9+	USB_OC5
	JUSB4	USB10- USB10+ USB11- USB11+	

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ0# PCI_GNT0#	AD21	PCI_CLKSLOT1 (PCI_CLK0)
PCI Slot 2	PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z	PCI_REQ1# PCI_GNT1#	AD22	PCI_CLKSLOT2 (PCI_CLK1)
PCI Slot 3	PCI_INT#Z PCI_INT#W PCI_INT#X PCI_INT#Y	PCI_REQ2# PCI_GNT2#	AD23	PCI_CLKSLOT3 (PCI_CLK2)
TPM				PCICLK_TPM (TPM_CLK)
Chipset				PCI_CLKIN (PCICLK4)
LPC				LPC_CLK
SIO				LPC_SIO24M

CPU VID TABLE

VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

PCI DEVICE RESET MAP

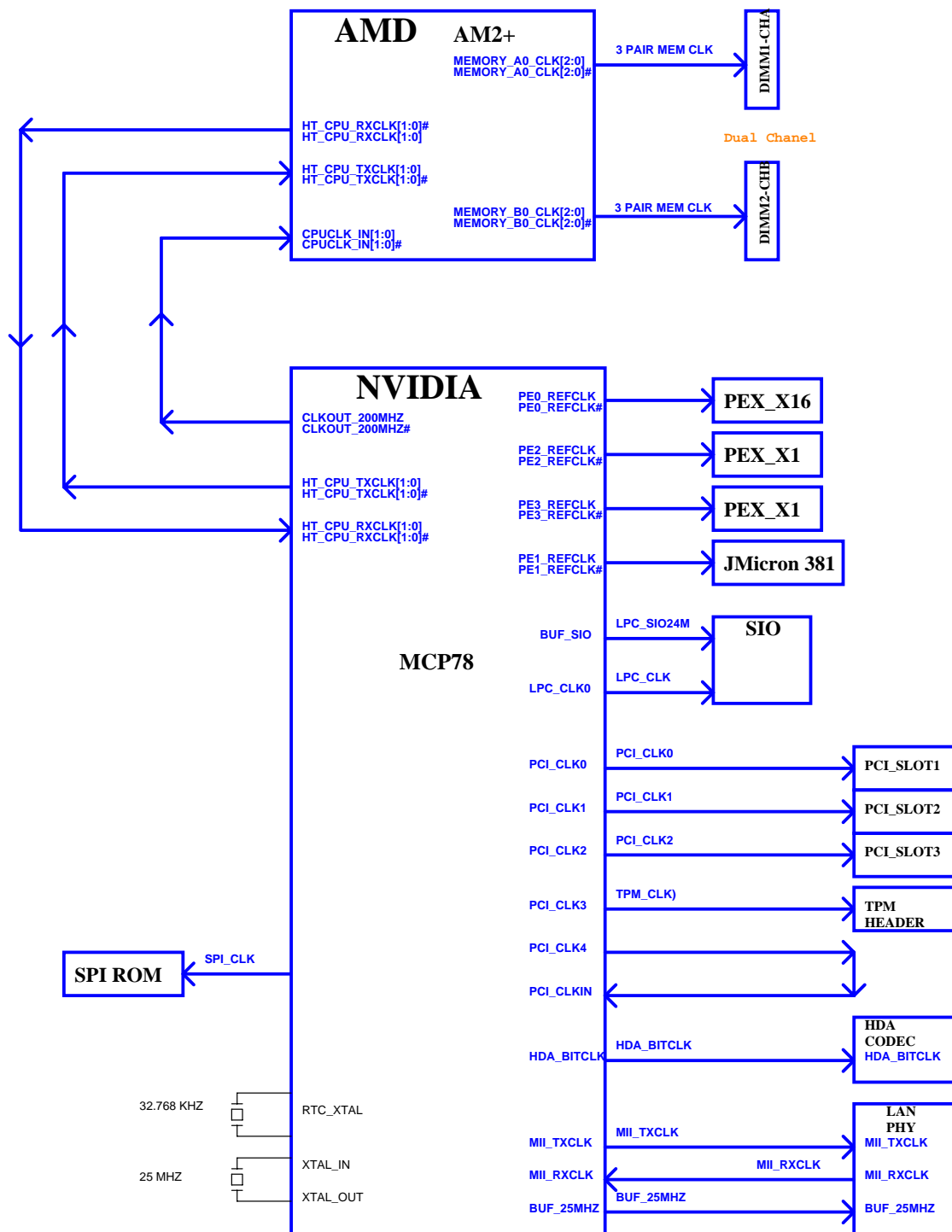
MCP78	
Signals	Target
PCI_RESET#0	PCISLOT1
PCI_RESET#1	PCISLOT2
PCI_RESET#2	PCISLOT3
LPC_RESET#	SIO/TPM
IDE_RESET#	IDE

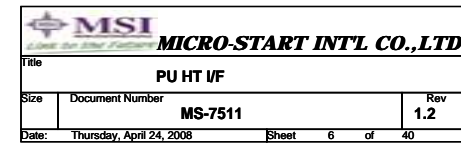
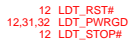
### MCP78 general purpose I/O

Name	Pin	Type	Function Description
<b>GPIO_1</b>	F2	I/O	NC
GPIO2/NMI#	F1	I/O	<b>PWR_SW_GPIO1</b>
GPIO3/SMI#	F6	I/O	<b>RST_GATE_GPIO2</b>
GPIO4/SCI_INTR#	J8	I/O	<b>USB_EN</b> Set as GPO When high turn on SVCC When low turn off SVCC
GPIO5/INIT#	G3	I/O	<b>DUAL_CTRL</b> Set as GPO When high turn on 5VDIMM in S4/S5 When low turn off 5VDIMM in S4/S5
GPIO6/FERR/SYS_SERR#	G5	I/O	NC
GPIO7/NFERR/SYS_PERR#	G6	I/O	NC
GPIO8/SPI_DI	D3	I/O	<b>SPI_DI</b>
GPIO9/SPI_DO	D4	I/O	<b>SPI_DO</b>
GPIO10/SPI_CS	E4	I/O	<b>SPI_CS#</b>
GPIO11/SPI_CLK	E3	I/O	<b>SPI_CLK</b>
MII_RESET/GPIO12#	C27	I/O	<b>MII_RESET</b>
MII_COL/GPIO13/MI2C_DATA	E24	I/O	<b>MII_COL</b>
MII_CRS/GPIO14/MI2C_CLK	F23	I/O	<b>MII_CRS</b>
LPC_DRQ1/GPIO15/FANRPM1#	B9	I/O	NC
DDC_CLK/GPIO17	B6	I/O	<b>DDC_CLK</b>
DDC_DATA/GPIO19	A6	I/O	<b>DDC_DATA</b>
PROCHOT#/GPIO20	AD8	I/O	<b>PROCHOT#</b>
PE_WAKE#/GPIO21	B22	I/O	<b>PE_WAKE#</b>
HDA_SDATA_IN0/GPIO22	A2	I/O	<b>HAD_SDATA_IN0</b>
HDA_SDATA_IN1/GPIO23	B1	I/O	NC
HDA_SDATA_IN2/GPIO24	B2	I/O	NC
USB_OC0#/GPIO25	P7	I/O	<b>USB_OC0</b>
USB_OC1#/GPIO26	P8	I/O	<b>USB_OC1</b>
USB_OC2#/GPIO27	P9	I/O	<b>USB_OC2</b>
USB_OC3#/GPIO28	P5	I/O	<b>USB_OC3</b>
USB_OC4#/GPIO29	P6	I/O	<b>USB_OC4</b>
PCI_PME#/GPIO30	E22	I/O	<b>PCI_PME#</b>
SIO_PME#/GPIO31	F4	I/O	<b>SIO_PME#</b>
EXT_SMI#/GPIO32	F3	I/O	NC
RI/GPIO33	H4	I/O	NC
SUS_CLK/GPIO34	E1	I/O	NC
MII_INTR/GPIO35	G24	I/O	<b>MII_INTR</b>
MII/RXER/GPIO36	D24	I/O	<b>MIIRXER</b>
MII_PWRDOWN/GPIO37	F24	I/O	NC
PCI_REQ3/GPIO38/RS232_CTS#	H14	I/O	<b>PCI_REQ3</b> Pull hi to VCC3
PCI_GNT3/GPIO39/RS232_RTS#	J14	I/O	<b>PCI_GNT3</b> Pull hi to VCC3
PCI_REQ2/GPIO40/RS232_DSR#	C11	I/O	<b>PCI_REQ2</b>
PCI_GNT2/GPIO41/RS232_DTR#	B10	I/O	<b>PCI_GNT2</b>
PCI_PERR/GPIO43/RS232_DCD#	G18	I/O	<b>PCI_PERR</b>
HDA_SYNC/GPIO44	B3	I/O	<b>HAD_SYNC</b>
HAD_SDATA_OUT0/GPIO45	A3	I/O	<b>HAD_SDATA_OUT0</b>
THERM_ALERT#/GPIO47	AF7	I/O	<b>CPU_THERM_ALERT#</b>
THERM_SIC/GPIO48	AH7	I/O	NC
THERM_SID/GPIO49	AF8	I/O	NC
LPC_DRQ0#/GPIO50	C9	I/O	<b>LPC_DRQ0#</b>
PCI_REQ4#/GPIO52	H14	I/O	<b>PCI_REQ4#</b> Pull hi to VCC3
PCI_GNT4#/GPIO53	D13	I/O	<b>PCI_GNT4#</b> Pull hi to VCC3
LPC_PWRDWN#/GPIO54	C8	I/O	NC
A20GATE/GPIO55	F5	I/O	<b>A20GATE</b>
KBRSTIN#/GPIO56	A4	I/O	<b>KBRST#</b>
SATA_LED#/GPIO57	A5	I/O	<b>SB_SATA_LED#</b>
THERMTRIP#/GPIO58	AE8	I/O	<b>CPU_THRIP#</b>
THERM/GPIO59	C6	I/O	<b>THERM#</b>
FANRPM0/GPIO60	E6	I/O	NC
FANCTL0/GPIO61	D6	I/O	NC
FANCTL1/GPIO62	C5	I/O	NC

### Super I/O general purpose I/O

Name	Pin	Type	Function Description
VIDOUT0/GPI00	49	I/O	GPI00_PSI
VIDOUT0/GPI01	50	I/O	GPI01_PSI
VIDOUT0/GPI02	51	I/O	GPI02_PSI
VIDOUT0/GPI03	52	I/O	GPI03_PSI
VIDOUT0/GPI04	53	I/O	Reserved for BIOS USE
VIDOUT0/GPI05/SID	54	I/O	Reserved for BIOS USE
<b>SLOT0CC#/GPI06</b>	55	I/O	Reserve pull hi to 3VUDAL
GPIO7/TURBO1#/WDTRST#	56	I/O	WDTRST# is used for over clock
GPIO10/SPI_CLK/FANIN4	59	I/O	<b>DLED1</b>
GPIO11/SPI_CS0#/FABCTL4	60	I/O	<b>DLED2</b>
GPIO12/SPI_MISO/FANCTL1_1	61	I/O	<b>DLED3</b>
PIO13/SPI_MOSI/BEEP	62	I/O	NC
GPIO14/FWH_DIS/WDTRST#/SPI_CS1#	63	I/O	<b>DLED4</b>
GPIO15/LED_VSB/ALERT#	64	I/O	<b>LED_VSB</b>
GPIO16/LED_VCC/TURBO2#	65	I/O	<b>LED_VCC</b>
GPIO17	66	I/O	<b>SPI_WP#</b>
PCIRST1#/GPIO20	74	I/O	NC
PCIRST2#/GPIO21	75	I/O	NC
PCIRST3#/GPIO22	76	I/O	NC
GPIO23/RSTCON#	77	I/O	<b>SIO_GPIO_FANTYPE</b> For CPU FAN type select: when 3pin GPIO should be low when 4pin GPIO should be high
ATXPG_IN/GPIO24	84	I/O	ATX_PWEROK
PME#/GPIO25	79	I/O	SIO_PME#
PWSIN#/GPIO26	80	I/O	PWRBUT_IN#
PWSOUT#/GPIO27	81	I/O	PWB_OUT#
S3#/GPIO31	82	I/O	<b>SLP_S3#</b>
PSON#/GPIO31	83	I/O	ATX_PSON#
PWROK/GPIO32	84		<b>PWROK</b> Set delay time as 100ms
RSMRST#/GPIO33	85		SIO_RSMRST#
IRTX/GPIO42	27		<b>IRTX</b>
IRRX/GPIO43	28		<b>IRRX</b>





9,10 MEM\_MA\_DQS\_L[7..0] >>>  
9,10 MEM\_MA\_DQS\_H[7..0] >>>  
9,10 MEM\_MA\_DM[7..0] >>>  
9,10 MEM\_MA\_DATA[63..0] >>>  
9,10,11 MEM\_MA\_ADD[15..0] >>>

9,10 MEM\_MB\_DQS\_L[7..0] >>>  
9,10 MEM\_MB\_DQS\_H[7..0] >>>  
9,10 MEM\_MB\_DM[7..0] >>>  
9,10 MEM\_MB\_DATA[63..0] >>>  
9,10,11 MEM\_MB\_ADD[15..0] >>>

U12B

9,11 MEM_MA0_CLK_H2	>>> MEM MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)	AE14	MEM MA_DATA63
9,11 MEM_MA0_CLK_L2	>>> MEM MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)	AG14	MEM MA_DATA62
9,11 MEM_MA0_CLK_H1	>>> MEM MA0_CLK_H1	AG19	MA0_CLK_H(1)	MA_DATA(61)	AG16	MEM MA_DATA61
9,11 MEM_MA0_CLK_L1	>>> MEM MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)	AD17	MEM MA_DATA60
9,11 MEM_MA0_CLK_H0	>>> MEM MA0_CLK_H0	U27	MA0_CLK_H(0)	MA_DATA(59)	AD13	MEM MA_DATA59
9,11 MEM_MA0_CLK_L0	>>> MEM MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)	AE13	MEM MA_DATA58
				MA_DATA(57)	AG15	MEM MA_DATA57
9,11 MEM_MA0_CS_L1	>>> MEM MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(56)	AE16	MEM MA_DATA56
9,11 MEM_MA0_CS_L0	>>> MEM MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(55)	AG17	MEM MA_DATA55
9,11 MEM_MA0_ODT0	>>> MEM MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(54)	AE18	MEM MA_DATA54
				MA_DATA(53)	AD21	MEM MA_DATA53
10,11 MEM_MA1_CLK_H2	>>> MEM MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(52)	AE17	MEM MA_DATA52
10,11 MEM_MA1_CLK_L2	>>> MEM MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(51)	AE17	MEM MA_DATA51
10,11 MEM_MA1_CLK_H1	>>> MEM MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(49)	AE21	MEM MA_DATA49
10,11 MEM_MA1_CLK_L1	>>> MEM MA1_CLK_L1	G21	MA1_CLK_L(1)	MA_DATA(48)	AE21	MEM MA_DATA48
10,11 MEM_MA1_CLK_H0	>>> MEM MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(47)	AE23	MEM MA_DATA47
10,11 MEM_MA1_CLK_L0	>>> MEM MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(46)	AE23	MEM MA_DATA46
				MA_DATA(45)	AJ26	MEM MA_DATA45
10,11 MEM_MA1_CS_L1	>>> MEM MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(44)	AG26	MEM MA_DATA44
10,11 MEM_MA1_CS_L0	>>> MEM MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(43)	AE22	MEM MA_DATA43
10,11 MEM_MA1_ODT0	>>> MEM MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(42)	AG23	MEM MA_DATA42
				MA_DATA(41)	AH25	MEM MA_DATA41
9,10,11 MEM_MA_CAS_L	>>> MEM MA_CAS_L	AB25	MA_CAS_L	MA_DATA(40)	AE25	MEM MA_DATA40
9,10,11 MEM_MA_WE_L	>>> MEM MA_WE_L	AB27	MA_WE_L	MA_DATA(39)	AJ28	MEM MA_DATA39
9,10,11 MEM_MA_RAS_L	>>> MEM MA_RAS_L	AA26	MA_RAS_L	MA_DATA(38)	AJ29	MEM MA_DATA38
9,10,11 MEM_MA_BANK2	>>> MEM MA_BANK2	N25	MA_BANK(2)	MA_DATA(37)	AE29	MEM MA_DATA37
9,10,11 MEM_MA_BANK1	>>> MEM MA_BANK1	Y27	MA_BANK(1)	MA_DATA(36)	AE26	MEM MA_DATA36
9,10,11 MEM_MA_BANK0	>>> MEM MA_BANK0	AA27	MA_BANK(0)	MA_DATA(35)	AJ27	MEM MA_DATA35
				MA_DATA(34)	AH27	MEM MA_DATA34
10,11 MEM_MA_CKE1	>>> MEM MA_CKE1	L27	MA_CKE(1)	MA_DATA(33)	AG29	MEM MA_DATA33
9,11 MEM_MA_CKE0	>>> MEM MA_CKE0	M25	MA_CKE(0)	MA_DATA(32)	AE27	MEM MA_DATA32
				MA_DATA(31)	E29	MEM MA_DATA31
				MA_DATA(30)	E28	MEM MA_DATA30
				MA_DATA(29)	D27	MEM MA_DATA29
				MA_DATA(28)	C27	MEM MA_DATA28
				MA_DATA(27)	G26	MEM MA_DATA27
				MA_DATA(26)	F27	MEM MA_DATA26
				MA_DATA(25)	C28	MEM MA_DATA25
				MA_DATA(24)	E27	MEM MA_DATA24
				MA_DATA(23)	F25	MEM MA_DATA23
				MA_DATA(22)	E25	MEM MA_DATA22
				MA_DATA(21)	E23	MEM MA_DATA21
				MA_DATA(20)	E26	MEM MA_DATA20
				MA_DATA(19)	C26	MEM MA_DATA19
				MA_DATA(18)	G23	MEM MA_DATA18
				MA_DATA(17)	F23	MEM MA_DATA17
				MA_DATA(16)	E22	MEM MA_DATA16
				MA_DATA(15)	E21	MEM MA_DATA15
				MA_DATA(14)	E17	MEM MA_DATA14
				MA_DATA(13)	G17	MEM MA_DATA13
				MA_DATA(12)	G22	MEM MA_DATA12
				MA_DATA(11)	F21	MEM MA_DATA11
				MA_DATA(10)	G18	MEM MA_DATA10
				MA_DATA(9)	E17	MEM MA_DATA9
				MA_DATA(8)	G16	MEM MA_DATA8
				MA_DATA(7)	E15	MEM MA_DATA7
				MA_DATA(6)	G13	MEM MA_DATA6
				MA_DATA(5)	H13	MEM MA_DATA5
				MA_DATA(4)	H17	MEM MA_DATA4
				MA_DATA(3)	E16	MEM MA_DATA3
				MA_DATA(2)	E14	MEM MA_DATA2
				MA_DATA(1)	G14	MEM MA_DATA1
				MA_DATA(0)		
				MA_DQS_H(8)	J28	X
				MA_DQS_L(8)	J27	X
				MA_DM(8)	J25	X
				MA_CHECK(7)	K25	X
				MA_CHECK(6)	J26	X
				MA_CHECK(5)	G26	X
				MA_CHECK(4)	G27	X
				MA_CHECK(3)	L24	X
				MA_CHECK(2)	K27	X
				MA_CHECK(1)	H29	X
				MA_CHECK(0)	H27	X

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U12C

9,11 MEM_MB0_CLK_H2	>>> MEM MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)	AH13	MEM MB_DATA63
9,11 MEM_MB0_CLK_L2	>>> MEM MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)	AL13	MEM MB_DATA62
9,11 MEM_MB0_CLK_H1	>>> MEM MB0_CLK_H1	AJ18	MB0_CLK_H(1)	MB_DATA(61)	AL13	MEM MB_DATA61
9,11 MEM_MB0_CLK_L1	>>> MEM MB0_CLK_L1	AJ19	MB0_CLK_L(1)	MB_DATA(60)	AJ15	MEM MB_DATA60
9,11 MEM_MB0_CLK_H0	>>> MEM MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)	AF13	MEM MB_DATA59
9,11 MEM_MB0_CLK_L0	>>> MEM MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)	AG13	MEM MB_DATA58
				MB_DATA(57)	AK15	MEM MB_DATA57
9,11 MEM_MB0_CS_L1	>>> MEM MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(56)	AL16	MEM MB_DATA56
9,11 MEM_MB0_CS_L0	>>> MEM MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(55)	AL17	MEM MB_DATA55
9,11 MEM_MB0_ODT0	>>> MEM MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(54)	AK21	MEM MB_DATA54
				MB_DATA(53)	AL15	MEM MB_DATA53
10,11 MEM_MB1_CLK_H2	>>> MEM MB1_CLK_H2	AL19	MB1_CLK_H(2)	MB_DATA(52)	AH21	MEM MB_DATA52
10,11 MEM_MB1_CLK_L2	>>> MEM MB1_CLK_L2	AL18	MB1_CLK_L(2)	MB_DATA(51)	AJ16	MEM MB_DATA51
10,11 MEM_MB1_CLK_H1	>>> MEM MB1_CLK_H1	C19	MB1_CLK_H(1)	MB_DATA(49)	AH19	MEM MB_DATA49
10,11 MEM_MB1_CLK_L1	>>> MEM MB1_CLK_L1	D19	MB1_CLK_L(1)	MB_DATA(48)	AL20	MEM MB_DATA48
10,11 MEM_MB1_CLK_H0	>>> MEM MB1_CLK_H0	W29	MB1_CLK_H(0)	MB_DATA(47)	AJ22	MEM MB_DATA47
10,11 MEM_MB1_CLK_L0	>>> MEM MB1_CLK_L0	W28	MB1_CLK_L(0)	MB_DATA(46)	AJ22	MEM MB_DATA46
				MB_DATA(45)	AK25	MEM MB_DATA45
10,11 MEM_MB1_CS_L1	>>> MEM MB1_CS_L1	AE29	MB1_CS_L(1)	MB_DATA(44)	AJ21	MEM MB_DATA44
10,11 MEM_MB1_CS_L0	>>> MEM MB1_CS_L0	AB31	MB1_CS_L(0)	MB_DATA(43)	AH21	MEM MB_DATA43
10,11 MEM_MB1_ODT0	>>> MEM MB1_ODT0	AD31	MB1_ODT(0)	MB_DATA(42)	AH23	MEM MB_DATA42
				MB_DATA(41)	AJ24	MEM MB_DATA41
9,10,11 MEM_MB_CAS_L	>>> MEM MB_CAS_L	AC29	MB_CAS_L	MB_DATA(40)	AJ24	MEM MB_DATA40
9,10,11 MEM_MB_WE_L	>>> MEM MB_WE_L	AC30	MB_WE_L	MB_DATA(39)	AK27	MEM MB_DATA39
9,10,11 MEM_MB_RAS_L	>>> MEM MB_RAS_L	AB29	MB_RAS_L	MB_DATA(38)	AH31	MEM MB_DATA38
9,10,11 MEM_MB_BANK2	>>> MEM MB_BANK2	N31	MB_BANK(2)	MB_DATA(37)	AG30	MEM MB_DATA37
9,10,11 MEM_MB_BANK1	>>> MEM MB_BANK1	AA31	MB_BANK(1)	MB_DATA(36)	AL25	MEM MB_DATA36
9,10,11 MEM_MB_BANK0	>>> MEM MB_BANK0	AA28	MB_BANK(0)	MB_DATA(35)	AL26	MEM MB_DATA35
				MB_DATA(34)	AJ30	MEM MB_DATA34
10,11 MEM_MB_CKE1	>>> MEM MB_CKE1	M31	MB_CKE(1)	MB_DATA(33)	AJ31	MEM MB_DATA33
9,11 MEM_MB_CKE0	>>> MEM MB_CKE0	M29	MB_CKE(0)	MB_DATA(32)	E31	MEM MB_DATA32
				MB_DATA(31)	E30	MEM MB_DATA31
				MB_DATA(30)	B27	MEM MB_DATA30
				MB_DATA(29)	A27	MEM MB_DATA29
				MB_DATA(28)	F29	MEM MB_DATA28
				MB_DATA(27)	F31	MEM MB_DATA27
				MB_DATA(26)	A29	MEM MB_DATA26
				MB_DATA(25)	A28	MEM MB_DATA25
				MB_DATA(24)	A25	MEM MB_DATA24
				MB_DATA(23)	A24	MEM MB_DATA23
				MB_DATA(22)	C22	MEM MB_DATA22
				MB_DATA(21)	D21	MEM MB_DATA21
				MB_DATA(20)	A26	MEM MB_DATA20
				MB_DATA(19)	B25	MEM MB_DATA19
				MB_DATA(18)	B23	MEM MB_DATA18
				MB_DATA(17)	A22	MEM MB_DATA17
				MB_DATA(16)	B21	MEM MB_DATA16
				MB_DATA(15)	A20	MEM MB_DATA15
				MB_DATA(14)	C16	MEM MB_DATA14
				MB_DATA(13)	D15	MEM MB_DATA13
				MB_DATA(12)	C21	MEM MB_DATA12
				MB_DATA(11)	A21	MEM MB_DATA11
				MB_DATA(10)	A17	MEM MB_DATA10
				MB_DATA(9)	A16	MEM MB_DATA9
				MB_DATA(8)	A15	MEM MB_DATA8
				MB_DATA(7)	A14	MEM MB_DATA7
				MB_DATA(6)	E13	MEM MB_DATA6
				MB_DATA(5)	F13	MEM MB_DATA5
				MB_DATA(4)	C15	MEM MB_DATA4
				MB_DATA(3)	A15	MEM MB_DATA3
				MB_DATA(2)	A13	MEM MB_DATA2
				MB_DATA(1)	D13	MEM MB_DATA1
				MB_DATA(0)		
				MB_DQS_H(8)	J31	X
				MB_DQS_L(8)	J30	X
				MB_DM(8)	J29	X
				MB_CHECK(7)	K29	X
				MB_CHECK(6)	K31	X
				MB_CHECK(5)	G30	X
				MB_CHECK(4)	G29	X
				MB_CHECK(3)	L29	X
				MB_CHECK(2)	L28	X
				MB_CHECK(1)	H31	X
				MB_CHECK(0)	G31	X

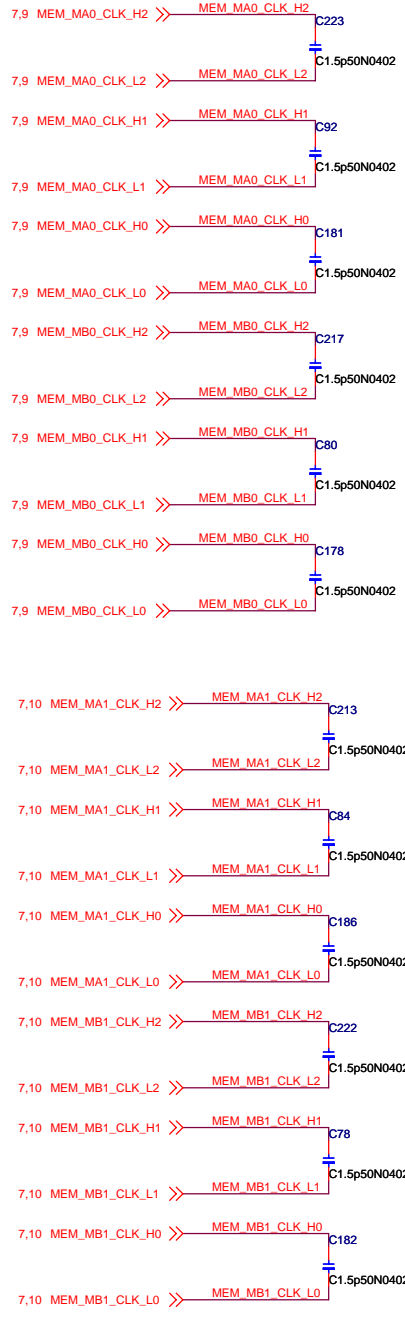
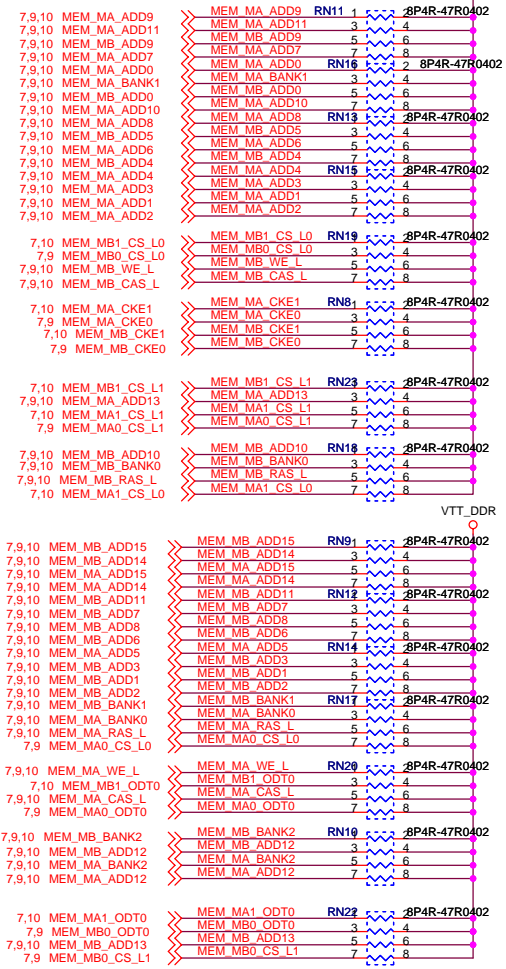
ZIF-SOCK940-RH-1



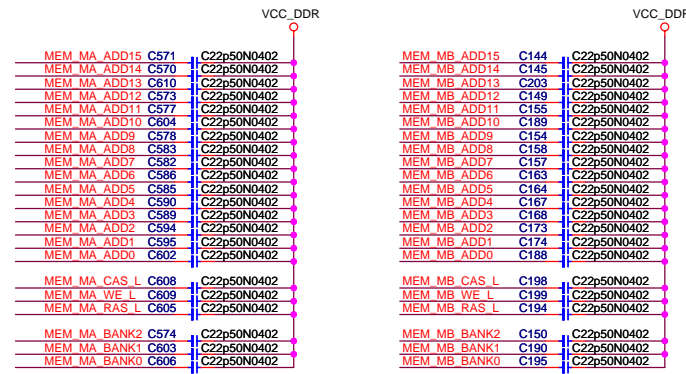




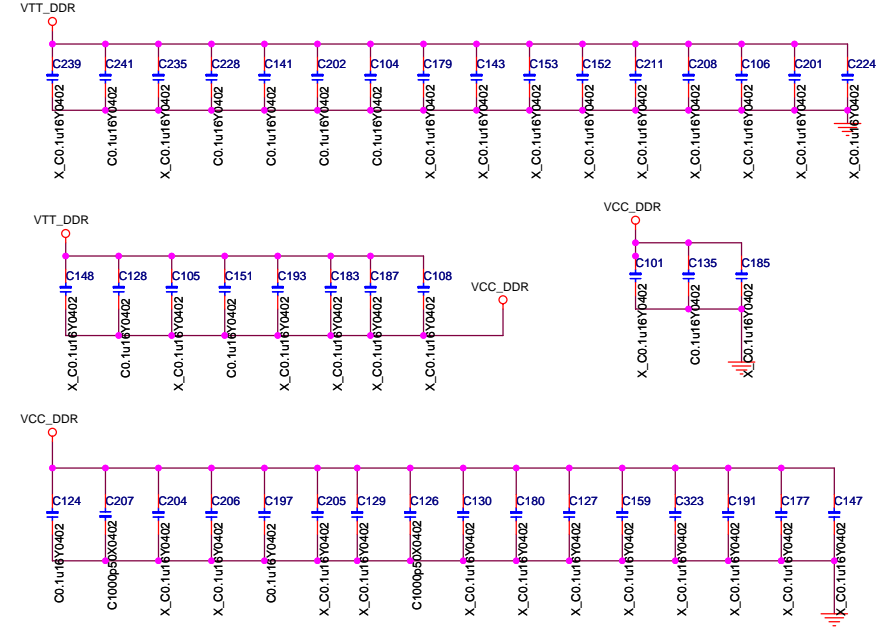
# RTT:Place Behind DIMMs



# Place Between Processor and DIMMs



# Layout: Spread out on VTT pour



# for EMI

<b>MICRO-START INT'L CO.,LTD.</b>		
Title		
DDR TERMINATOR		
Size	Document Number	Rev
	MS-7511	1.2
Date:	Monday, April 28, 2008	Sheet 11 of 40

6 HT\_CADIN\_H[15..0] >> HT\_CADIN\_H[15..0]  
6 HT\_CADIN\_L[15..0] >> HT\_CADIN\_L[15..0]  
6 HT\_CADOUT\_H[15..0] >> HT\_CADOUT\_H[15..0]  
6 HT\_CADOUT\_L[15..0] >> HT\_CADOUT\_L[15..0]

U21A

SEC 1 OF 8

HT_CADOUT_H0	AG8	HT_MCP_RXD0_P	HT_MCP_TXD0_P	AH23	HT_CADIN_H0
HT_CADOUT_H1	AG9	HT_MCP_RXD1_P	HT_MCP_TXD1_P	AH22	HT_CADIN_H1
HT_CADOUT_H2	AK9	HT_MCP_RXD2_P	HT_MCP_TXD2_P	AJ21	HT_CADIN_H2
HT_CADOUT_H3	AJ10	HT_MCP_RXD3_P	HT_MCP_TXD3_P	AH21	HT_CADIN_H3
HT_CADOUT_H4	AG12	HT_MCP_RXD4_P	HT_MCP_TXD4_P	AH19	HT_CADIN_H4
HT_CADOUT_H5	AG13	HT_MCP_RXD5_P	HT_MCP_TXD5_P	AH18	HT_CADIN_H5
HT_CADOUT_H6	AK13	HT_MCP_RXD6_P	HT_MCP_TXD6_P	AJ17	HT_CADIN_H6
HT_CADOUT_H7	AJ14	HT_MCP_RXD7_P	HT_MCP_TXD7_P	AH17	HT_CADIN_H7
HT_CADOUT_H8	AB10	HT_MCP_RXD8_P	HT_MCP_TXD8_P	AF22	HT_CADIN_H8
HT_CADOUT_H9	AD10	HT_MCP_RXD9_P	HT_MCP_TXD9_P	AB20	HT_CADIN_H9
HT_CADOUT_H10	AF10	HT_MCP_RXD10_P	HT_MCP_TXD10_P	AC20	HT_CADIN_H10
HT_CADOUT_H11	AC12	HT_MCP_RXD11_P	HT_MCP_TXD11_P	AE20	HT_CADIN_H11
HT_CADOUT_H12	AB11	HT_MCP_RXD12_P	HT_MCP_TXD12_P	AD18	HT_CADIN_H12
HT_CADOUT_H13	AB13	HT_MCP_RXD13_P	HT_MCP_TXD13_P	AF18	HT_CADIN_H13
HT_CADOUT_H14	AF14	HT_MCP_RXD14_P	HT_MCP_TXD14_P	AB17	HT_CADIN_H14
HT_CADOUT_H15	AE14	HT_MCP_RXD15_P	HT_MCP_TXD15_P	AC16	HT_CADIN_H15
HT_CADOUT_L0	AH8	HT_MCP_RXD0_N	HT_MCP_TXD0_N	AJ23	HT_CADIN_L0
HT_CADOUT_L1	AH9	HT_MCP_RXD1_N	HT_MCP_TXD1_N	AJ22	HT_CADIN_L1
HT_CADOUT_L2	AJ9	HT_MCP_RXD2_N	HT_MCP_TXD2_N	AK21	HT_CADIN_L2
HT_CADOUT_L3	AH10	HT_MCP_RXD3_N	HT_MCP_TXD3_N	AG21	HT_CADIN_L3
HT_CADOUT_L4	AH12	HT_MCP_RXD4_N	HT_MCP_TXD4_N	AJ19	HT_CADIN_L4
HT_CADOUT_L5	AH13	HT_MCP_RXD5_N	HT_MCP_TXD5_N	AJ18	HT_CADIN_L5
HT_CADOUT_L6	AJ13	HT_MCP_RXD6_N	HT_MCP_TXD6_N	AK17	HT_CADIN_L6
HT_CADOUT_L7	AH14	HT_MCP_RXD7_N	HT_MCP_TXD7_N	AG17	HT_CADIN_L7
HT_CADOUT_L8	AC10	HT_MCP_RXD8_N	HT_MCP_TXD8_N	AG22	HT_CADIN_L8
HT_CADOUT_L9	AE10	HT_MCP_RXD9_N	HT_MCP_TXD9_N	AB19	HT_CADIN_L9
HT_CADOUT_L10	AG10	HT_MCP_RXD10_N	HT_MCP_TXD10_N	AD20	HT_CADIN_L10
HT_CADOUT_L11	AD12	HT_MCP_RXD11_N	HT_MCP_TXD11_N	AE20	HT_CADIN_L11
HT_CADOUT_L12	AC11	HT_MCP_RXD12_N	HT_MCP_TXD12_N	AE18	HT_CADIN_L12
HT_CADOUT_L13	AB12	HT_MCP_RXD13_N	HT_MCP_TXD13_N	AG18	HT_CADIN_L13
HT_CADOUT_L14	AG14	HT_MCP_RXD14_N	HT_MCP_TXD14_N	AB16	HT_CADIN_L14
HT_CADOUT_L15	AD14	HT_MCP_RXD15_N	HT_MCP_TXD15_N	AD16	HT_CADIN_L15

6 HT\_CLKOUT\_H0 >> AJ11  
6 HT\_CLKOUT\_L0 >> AH11  
6 HT\_CLKOUT\_H1 >> AE12  
6 HT\_CLKOUT\_L1 >> AE12

6 HT\_CTOUT\_H0 >> AJ15  
6 HT\_CTOUT\_L0 >> AH15  
6 HT\_CTOUT\_H1 >> AB14  
6 HT\_CTOUT\_L1 >> AC14

HT\_MCP\_TX\_CLK0\_P >> HT\_CLKIN\_H0 6  
HT\_MCP\_TX\_CLK0\_N >> HT\_CLKIN\_L0 6  
HT\_MCP\_TX\_CLK1\_P >> HT\_CLKIN\_H1 6  
HT\_MCP\_TX\_CLK1\_N >> HT\_CLKIN\_L1 6

HT\_MCP\_TXCTL0\_P >> HT\_CTLIN\_H0 6  
HT\_MCP\_TXCTL0\_N >> HT\_CTLIN\_L0 6  
RESERVED35 >> HT\_CTLIN\_H1 6  
RESERVED36 >> HT\_CTLIN\_L1 6

HT\_MCP\_REQ# >> LDT\_STOP# 6  
HT\_MCP\_STOP# >> LDT\_RST# 6  
HT\_MCP\_RST# >> LDT\_PWRGD 6,31,32  
HT\_MCP\_PWRGD >> LDT\_PWRGD 6,31,32

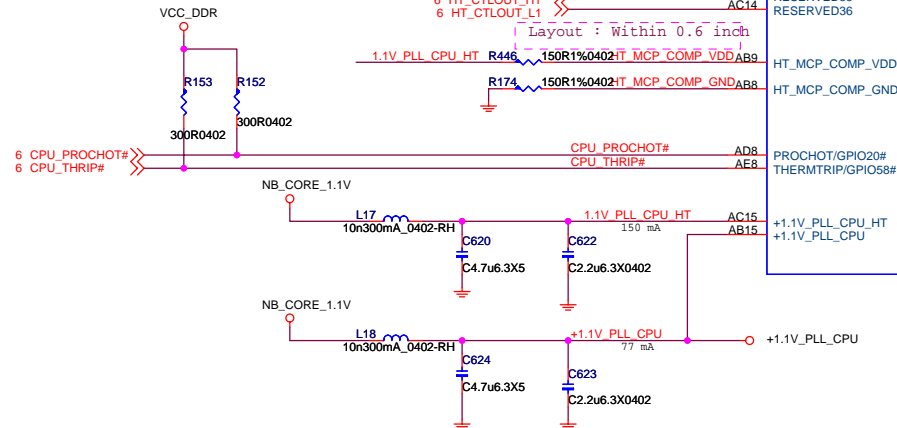
CLKOUT\_200MHZ\_P >> CPU\_CLK 6  
CLKOUT\_200MHZ\_N >> CPU\_CLK# 6

CPU\_SBVREF >> CPU\_CLK 6  
CLKOUT\_25MHZ >> CPU\_CLK# 6

CLK200\_TERM\_GND >> CPU\_CLK 6  
CLK200\_TERM\_GND >> CPU\_CLK# 6

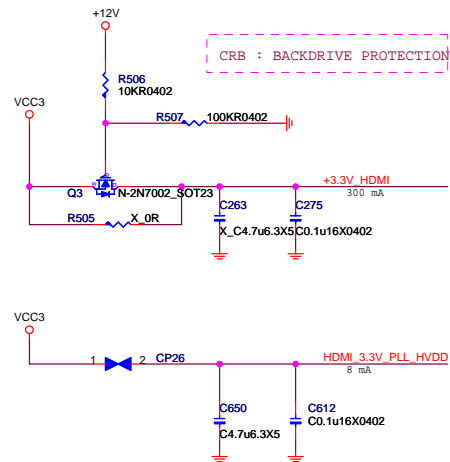
Layout : Place C301  
within 0.5 inch of MCP

Layout : Place R201  
within 1.0 inch of MCP



U21B

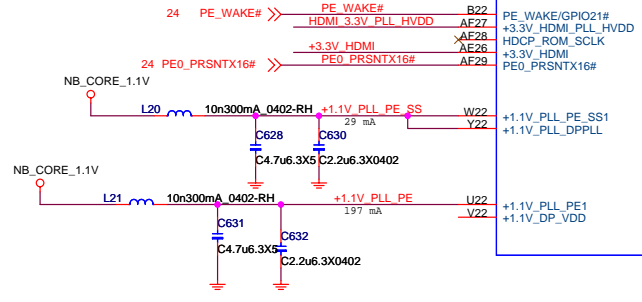
SEC 2 OF 8



24 PE0_RX0_P0	>> PE0_RX0_P0	H23
24 PE0_RX0_P1	>> PE0_RX0_P1	H25
24 PE0_RX0_P2	>> PE0_RX0_P2	K22
24 PE0_RX0_P3	>> PE0_RX0_P3	K24
24 PE0_RX0_P4	>> PE0_RX0_P4	K26
24 PE0_RX0_P5	>> PE0_RX0_P5	M22
24 PE0_RX0_P6	>> PE0_RX0_P6	M23
24 PE0_RX0_P7	>> PE0_RX0_P7	M26
24 PE0_RX0_P8	>> PE0_RX0_P8	P22
24 PE0_RX0_P9	>> PE0_RX0_P9	P26
24 PE0_RX0_P10	>> PE0_RX0_P10	P25
24 PE0_RX0_P11	>> PE0_RX0_P11	T23
24 PE0_RX0_P12	>> PE0_RX0_P12	T26
24 PE0_RX0_P13	>> PE0_RX0_P13	U23
24 PE0_RX0_P14	>> PE0_RX0_P14	V24
24 PE0_RX0_P15	>> PE0_RX0_P15	V27
24 PE0_RX0_N0	>> PE0_RX0_N0	H24
24 PE0_RX0_N1	>> PE0_RX0_N1	H26
24 PE0_RX0_N2	>> PE0_RX0_N2	K23
24 PE0_RX0_N3	>> PE0_RX0_N3	K25
24 PE0_RX0_N4	>> PE0_RX0_N4	K27
24 PE0_RX0_N5	>> PE0_RX0_N5	L22
24 PE0_RX0_N6	>> PE0_RX0_N6	M24
24 PE0_RX0_N7	>> PE0_RX0_N7	M25
24 PE0_RX0_N8	>> PE0_RX0_N8	P23
24 PE0_RX0_N9	>> PE0_RX0_N9	P27
24 PE0_RX0_N10	>> PE0_RX0_N10	P24
24 PE0_RX0_N11	>> PE0_RX0_N11	T24
24 PE0_RX0_N12	>> PE0_RX0_N12	T25
24 PE0_RX0_N13	>> PE0_RX0_N13	V23
24 PE0_RX0_N14	>> PE0_RX0_N14	V25
24 PE0_RX0_N15	>> PE0_RX0_N15	V26

PE0_RX0_P	>> PE0_RX0_P
PE0_RX1_P	>> PE0_RX1_P
PE0_RX2_P	>> PE0_RX2_P
PE0_RX3_P	>> PE0_RX3_P
PE0_RX4_P	>> PE0_RX4_P
PE0_RX5_P	>> PE0_RX5_P
PE0_RX6_P	>> PE0_RX6_P
PE0_RX7_P	>> PE0_RX7_P
PE0_RX8_P	>> PE0_RX8_P
PE0_RX9_P	>> PE0_RX9_P
PE0_RX10_P	>> PE0_RX10_P
PE0_RX11_P	>> PE0_RX11_P
PE0_RX12_P	>> PE0_RX12_P
PE0_RX13_P	>> PE0_RX13_P
PE0_RX14_P	>> PE0_RX14_P
PE0_RX15_P	>> PE0_RX15_P

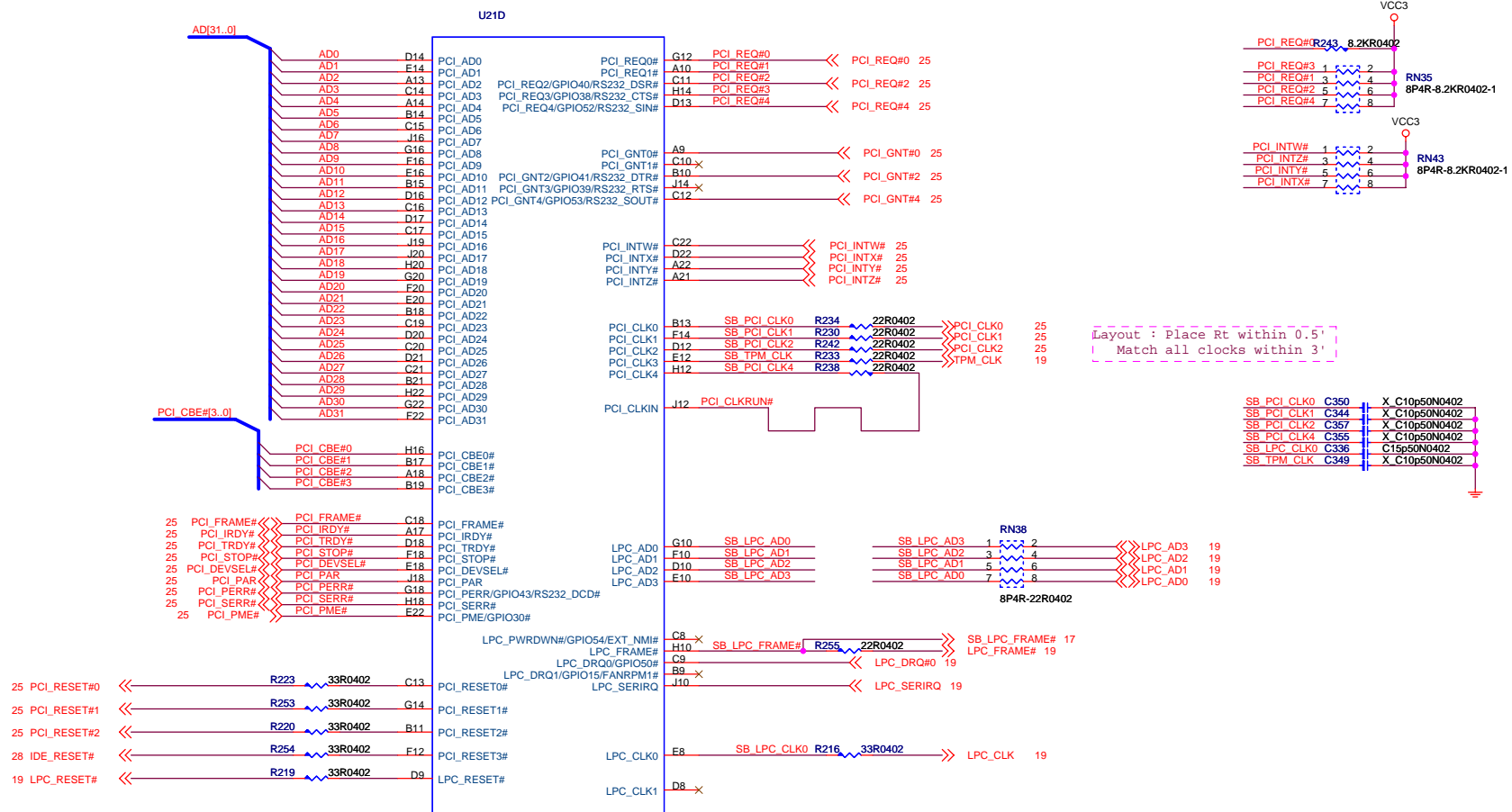
PE0_TX0_P	>> PE0_TX0_P
PE0_TX1_P	>> PE0_TX1_P
PE0_TX2_P	>> PE0_TX2_P
PE0_TX3_P	>> PE0_TX3_P
PE0_TX4_P	>> PE0_TX4_P
PE0_TX5_P	>> PE0_TX5_P
PE0_TX6_P	>> PE0_TX6_P
PE0_TX7_P	>> PE0_TX7_P
PE0_TX8_P	>> PE0_TX8_P
PE0_TX9_P	>> PE0_TX9_P
PE0_TX10_P	>> PE0_TX10_P
PE0_TX11_P	>> PE0_TX11_P
PE0_TX12_P	>> PE0_TX12_P
PE0_TX13_P	>> PE0_TX13_P
PE0_TX14_P	>> PE0_TX14_P
PE0_TX15_P	>> PE0_TX15_P
PE0_TX0_N	>> PE0_TX0_N
PE0_TX1_N	>> PE0_TX1_N
PE0_TX2_N	>> PE0_TX2_N
PE0_TX3_N	>> PE0_TX3_N
PE0_TX4_N	>> PE0_TX4_N
PE0_TX5_N	>> PE0_TX5_N
PE0_TX6_N	>> PE0_TX6_N
PE0_TX7_N	>> PE0_TX7_N
PE0_TX8_N	>> PE0_TX8_N
PE0_TX9_N	>> PE0_TX9_N
PE0_TX10_N	>> PE0_TX10_N
PE0_TX11_N	>> PE0_TX11_N
PE0_TX12_N	>> PE0_TX12_N
PE0_TX13_N	>> PE0_TX13_N
PE0_TX14_N	>> PE0_TX14_N
PE0_TX15_N	>> PE0_TX15_N

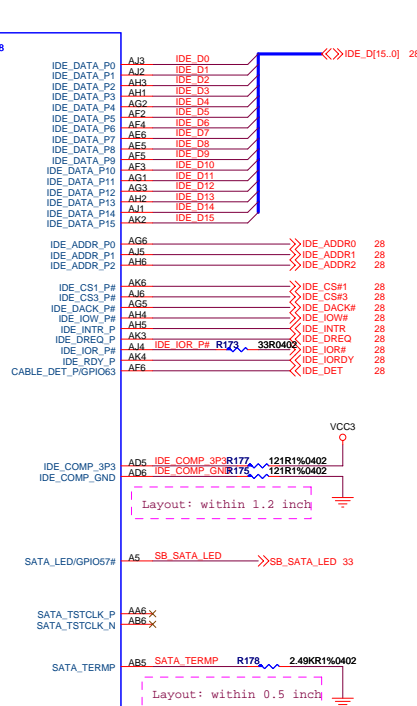
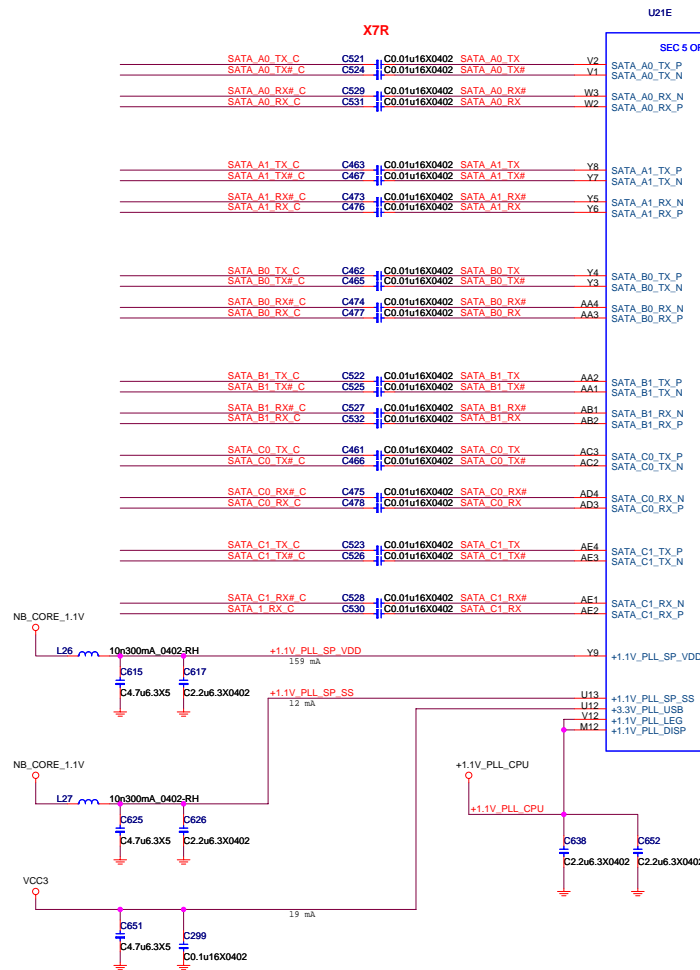
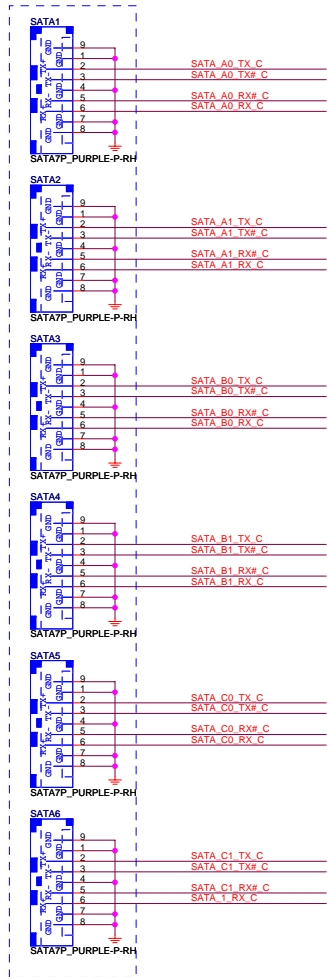


PE0_REFCLK_P	>> PE0_REFCLK_P
PE0_REFCLK_N	>> PE0_REFCLK_N
HDMI_TXD0_N	>> HDMI_TXD0_N
HDMI_TXD0_P	>> HDMI_TXD0_P
PE_RESET#	>> MCP_PE_RESET#
PE_CLK_COMP	>> PE_CLK_COMP
+3.3V_DLL_HT_RESERVED2	>> +3.3V_DLL_HT_RESERVED2



AD[31..0] <<>> AD[31..0] 25  
PCI\_CBE#[3..0] <<>> PCI\_CBE#[3..0] 25





VCC3

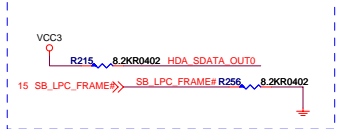
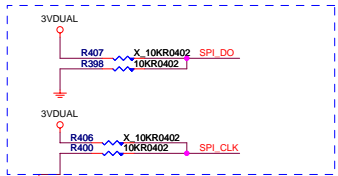
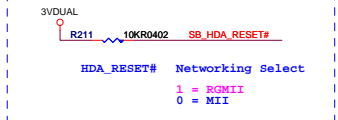
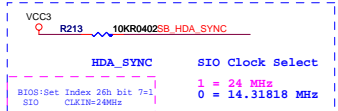
R227 X\_10KR0402

R222 1KR0402 SPEAKER

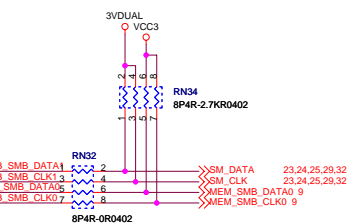
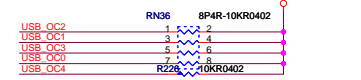
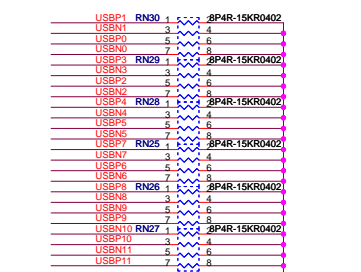
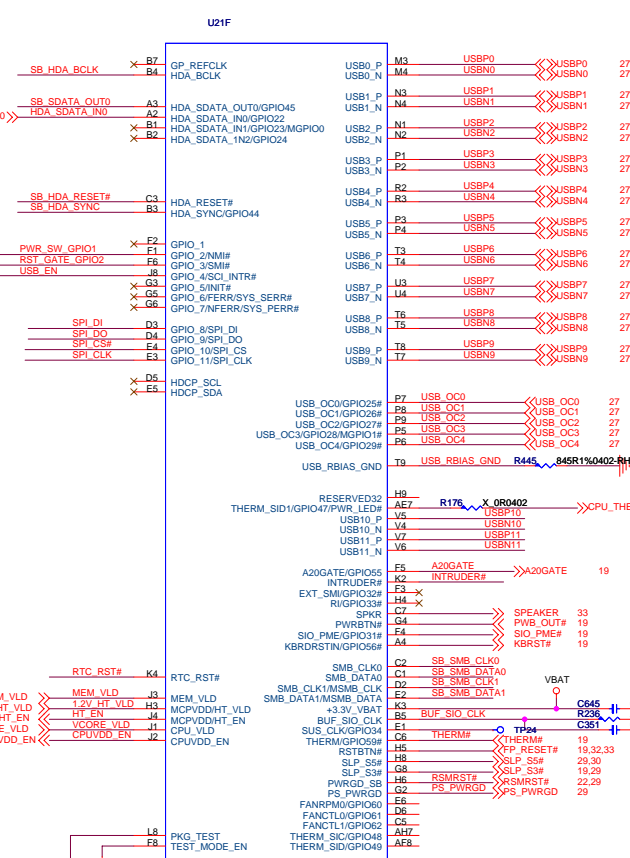
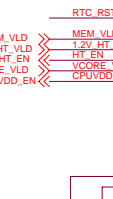
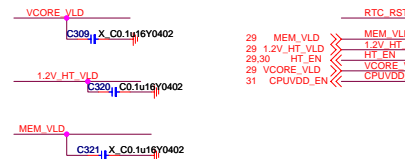
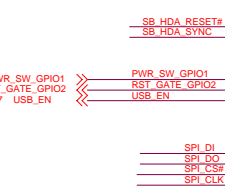
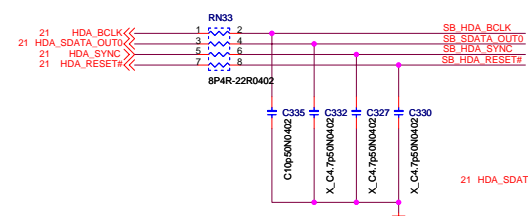
SPEAK Boot Mode Select

1 = Safe Mode Boot Init table!

0 = User Mode Boot Init table!



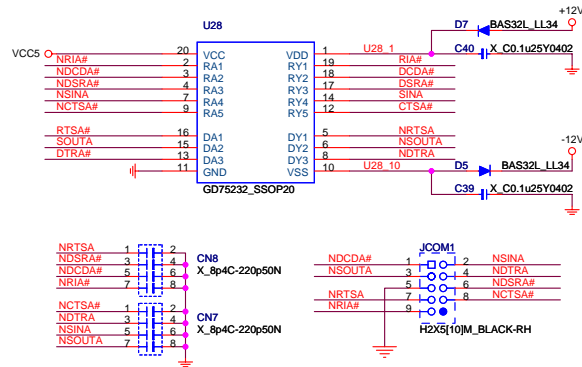
BIOS Select	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
ECT BIOS	0	1
SPT BIOS	1	0
Reserved (SPT)	1	1







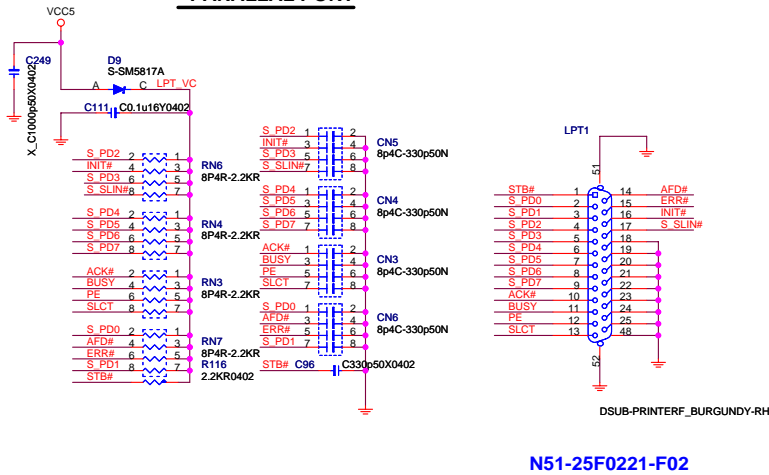
## SERIAL PORT 1



SLCT	SLCT	19
PE	PE	19
BUSY	BUSY	19
ACK#	ACK#	19
S_SLIN#	S_SLIN#	19
INIT#	INIT#	19
ERR#	ERR#	19
AFD#	AFD#	19
STB#	STB#	19
S_PD0	S_PD0	19
S_PD1	S_PD1	19
S_PD2	S_PD2	19
S_PD3	S_PD3	19
S_PD4	S_PD4	19
S_PD5	S_PD5	19
S_PD6	S_PD6	19
S_PD7	S_PD7	19

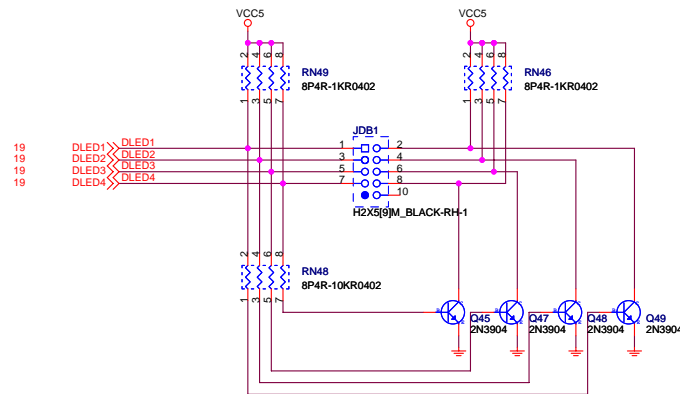
DCDA#	DCDA#	19
RIA#	RIA#	19
CTS#	CTS#	19
DTRA#	DTRA#	19
RTSA#	RTSA#	19
DSRA#	DSRA#	19
SOUTA	SOUTA	19
SINA	SINA	19

## PARALLAL PORT

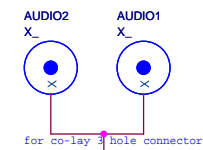


N51-25F0221-F02

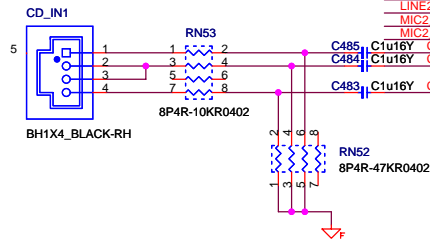
## DEBUG LED



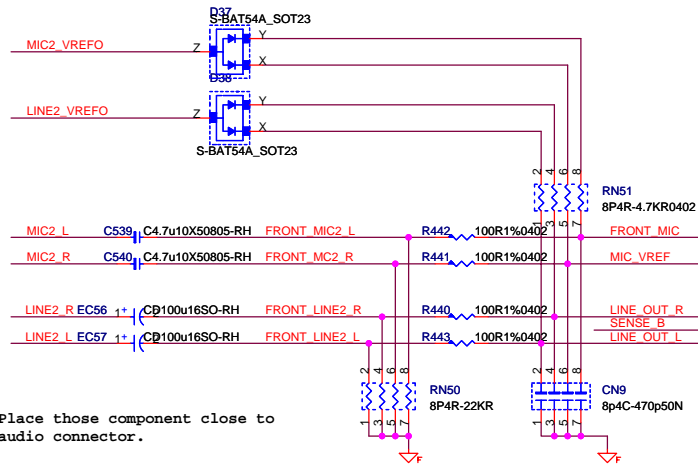
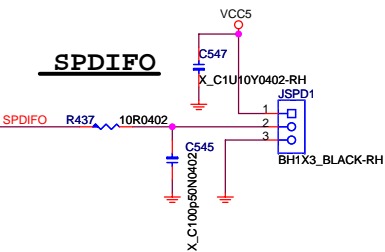
# Azalia Audio



Layout:Co-lay 3 hole connector

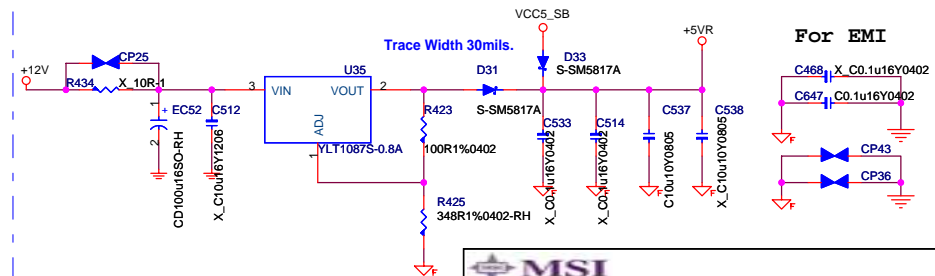
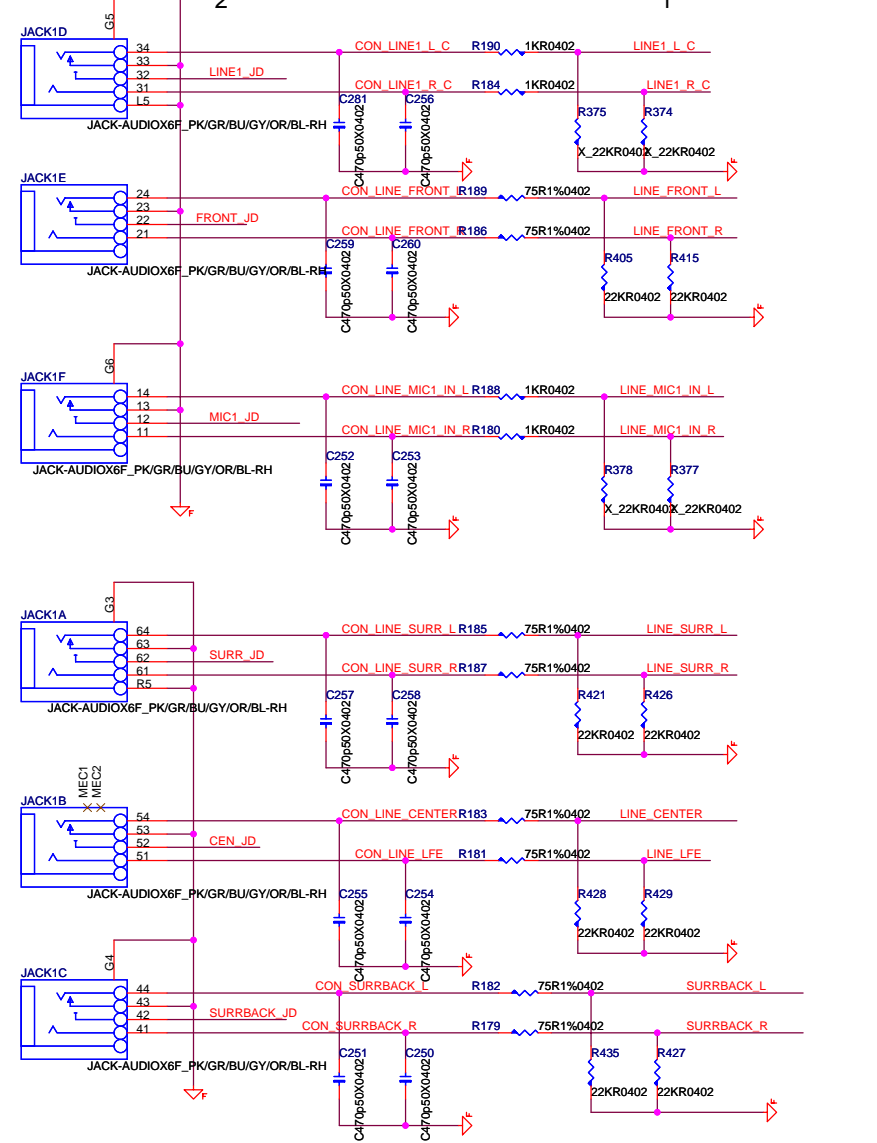
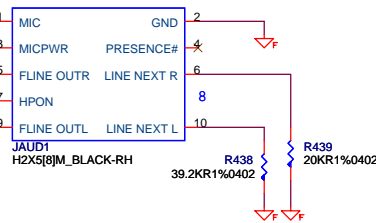
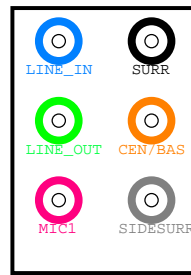
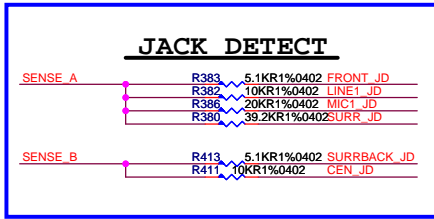
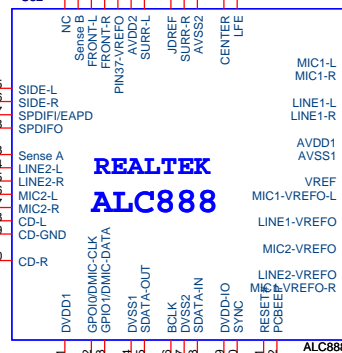


## SPDIFO



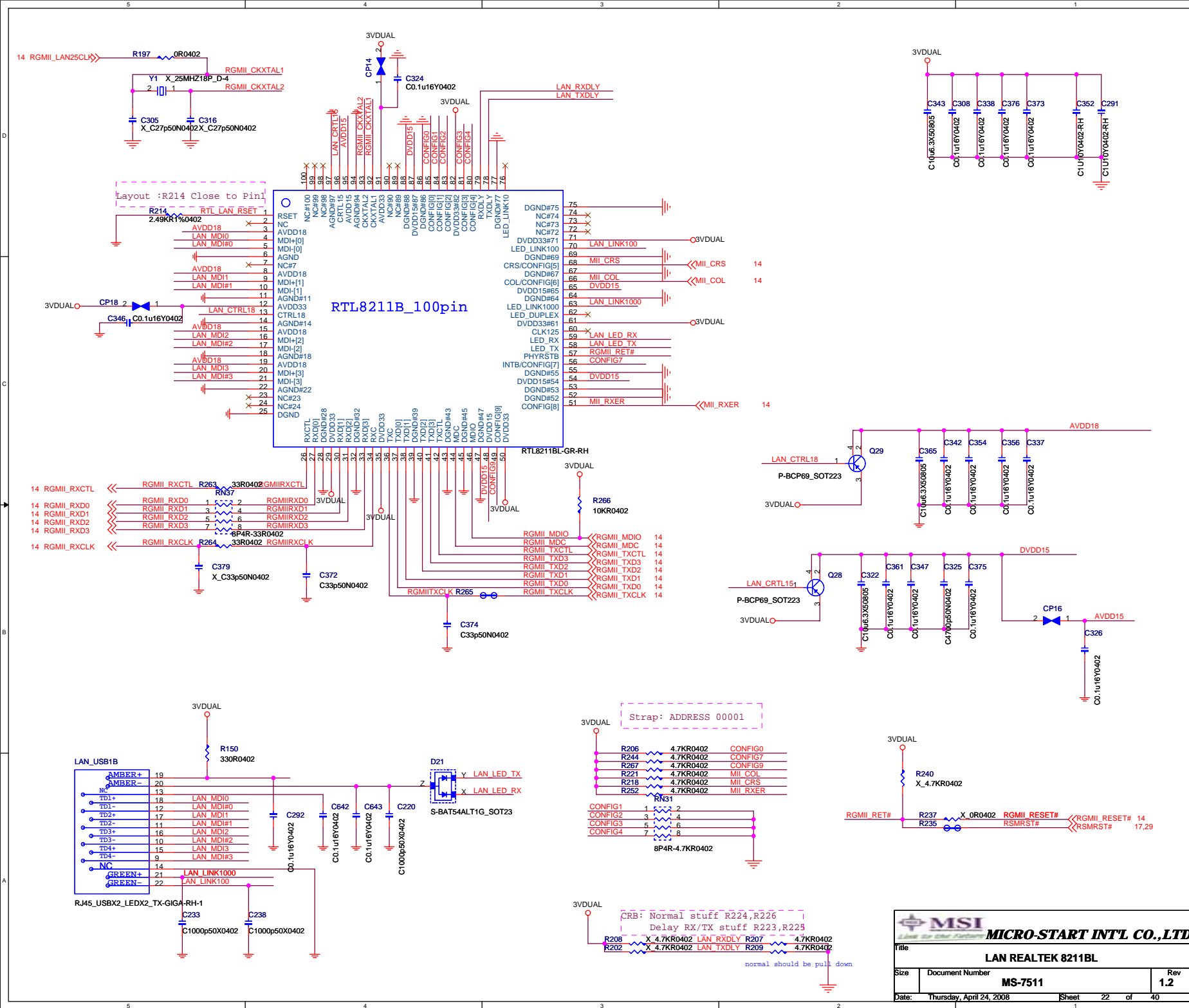
Place those component close to audio connector.

## REALTEK ALC888

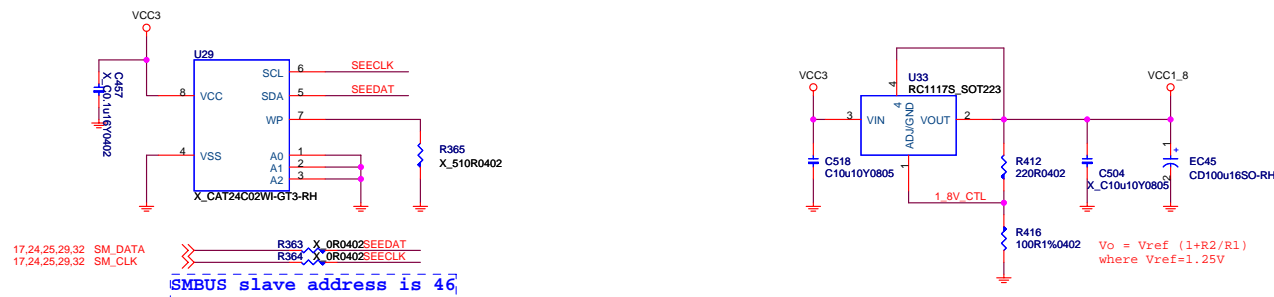
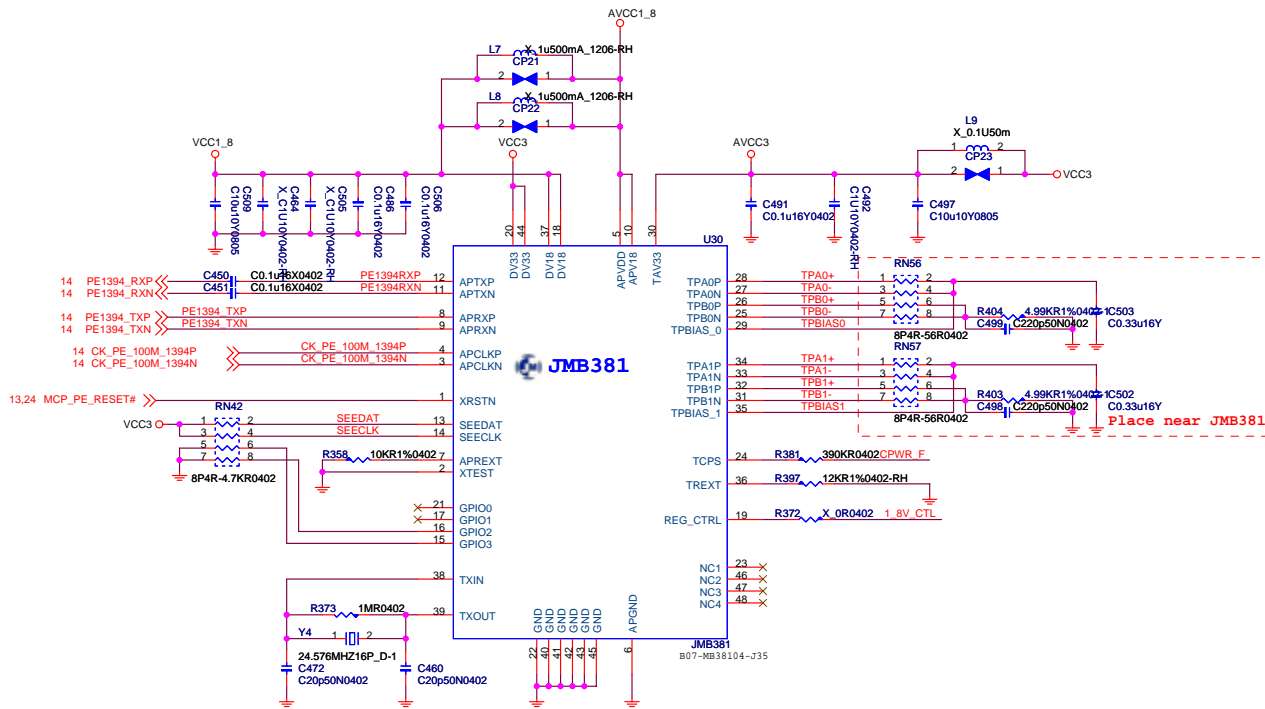


## Codec Regulator

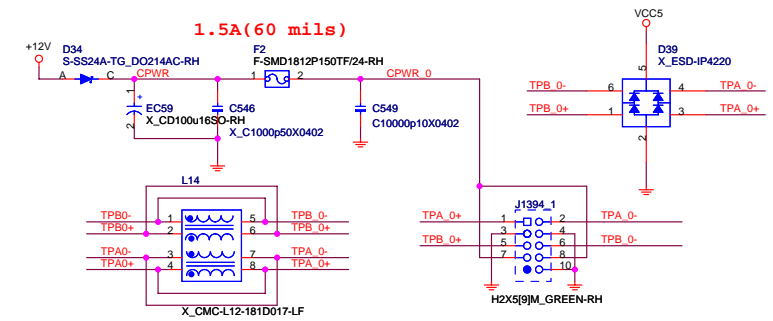
MSI		
MICRO-START INT'L CO.,LTD		
AZALIA ALC888		
Size	Document Number	Rev
	MS-7511	1.2
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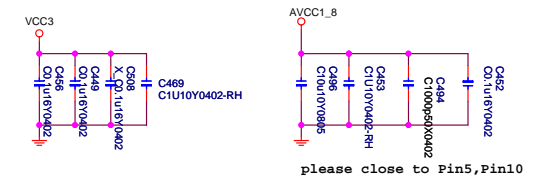
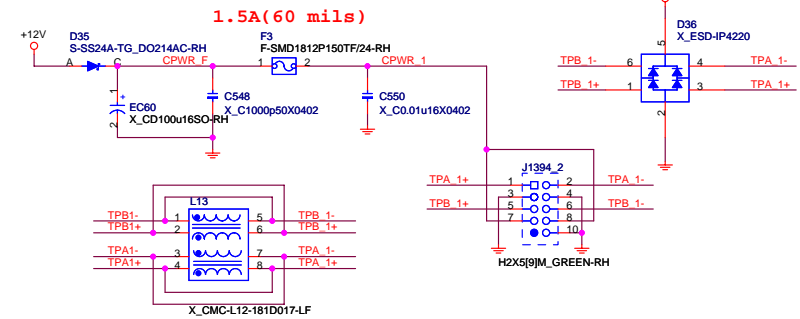
## JMICRON JMB381

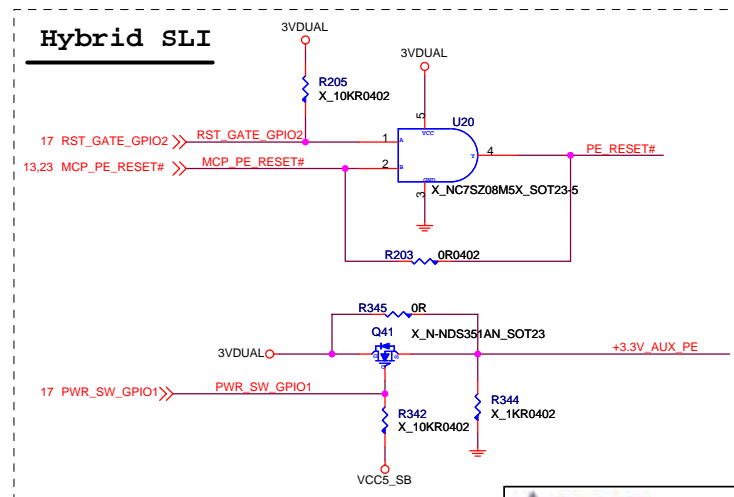
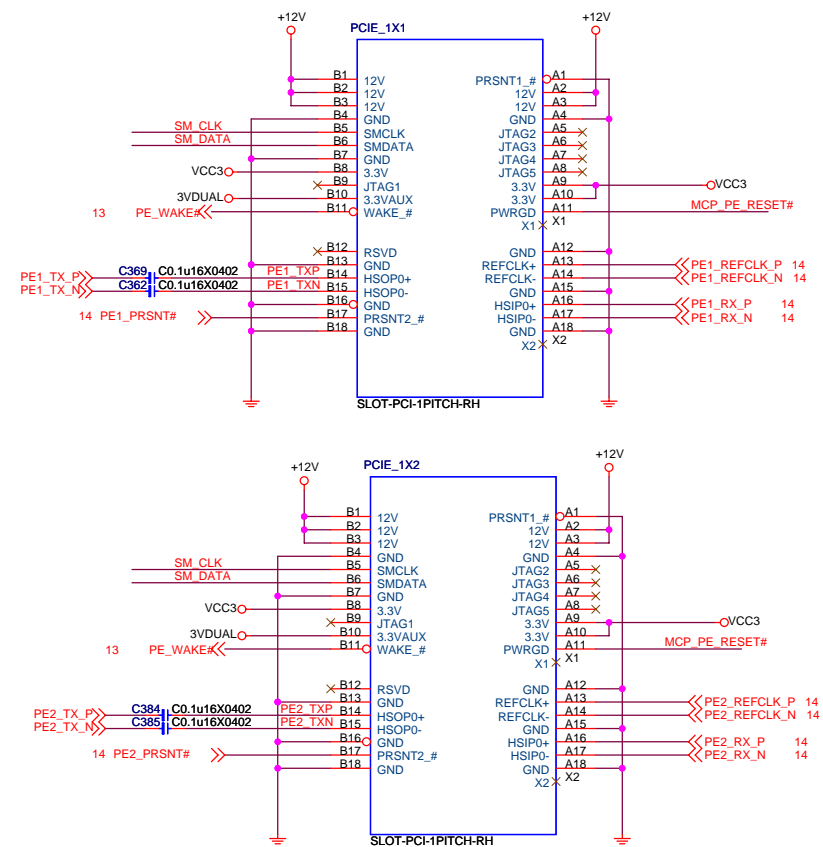
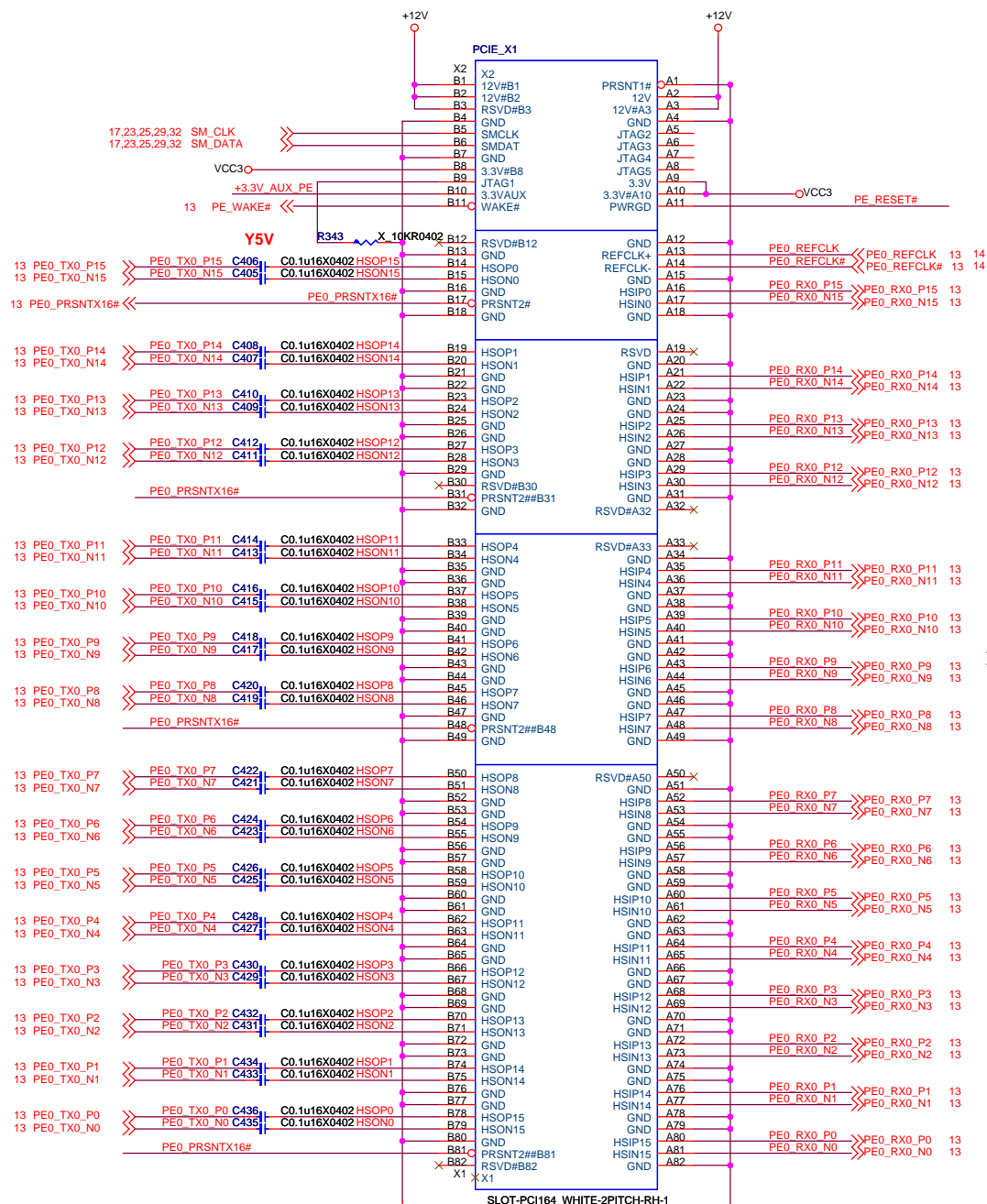


**Rear 1394 port**



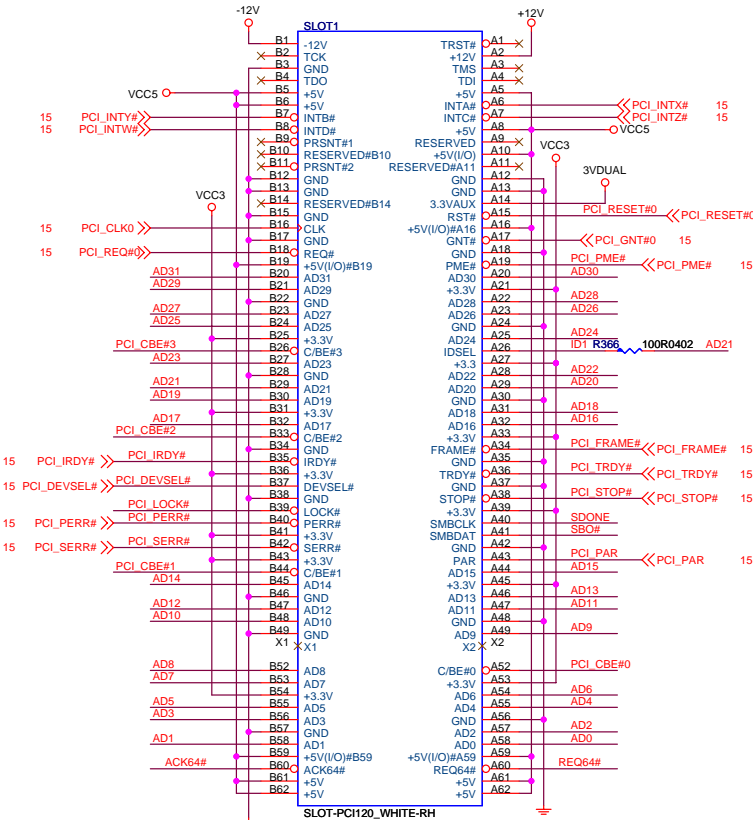
**Front 1394 pin header**





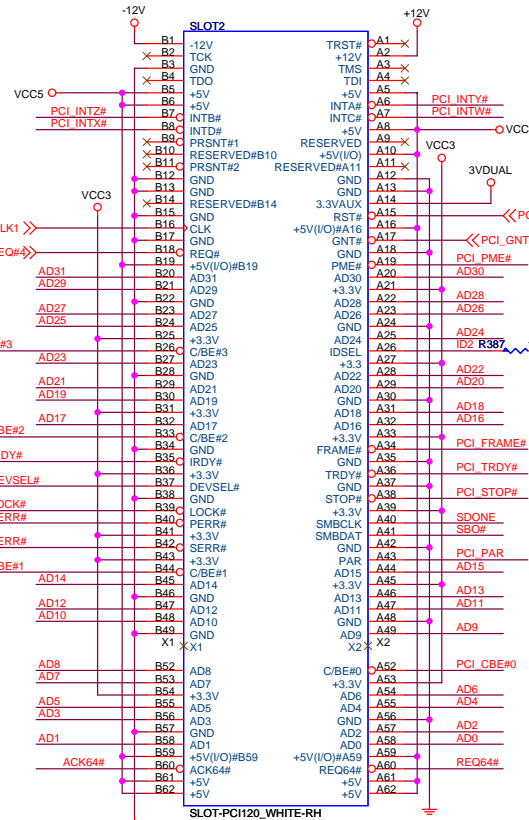
15 AD[31..0] >> AD[31..0]  
15 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

### PCI SLOT 1 (PCI VER: 2.3 COMPLY)



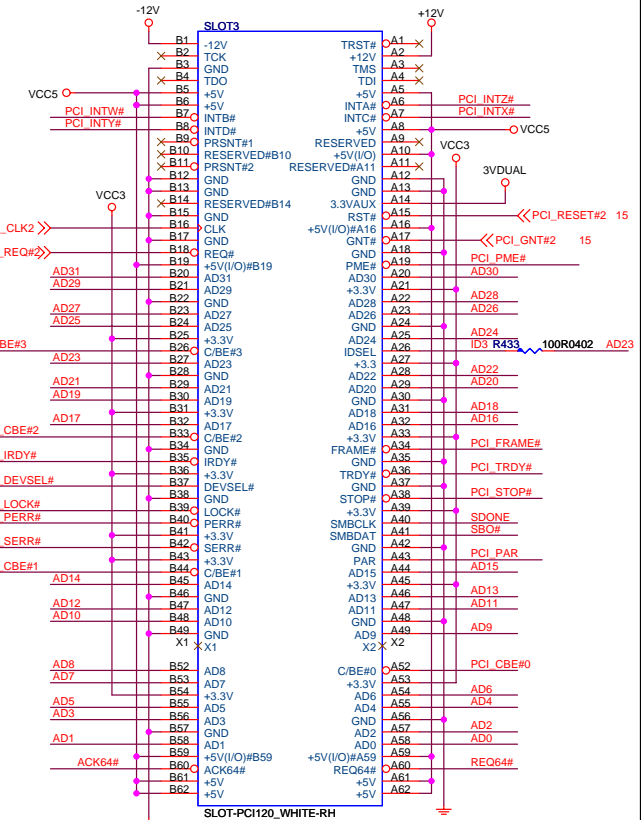
IDSEL = AD21  
MASTER = PCI\_REQ#0  
PCI\_GNT#0  
PCI\_INTX#

### PCI SLOT 2 (PCI VER: 2.3 COMPLY)



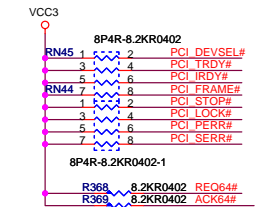
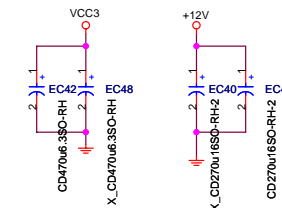
IDSEL = AD22  
MASTER = PCI\_REQ#1  
PCI\_GNT#1  
PCI\_INTY#

### PCI SLOT 2 (PCI VER: 2.3 COMPLY)



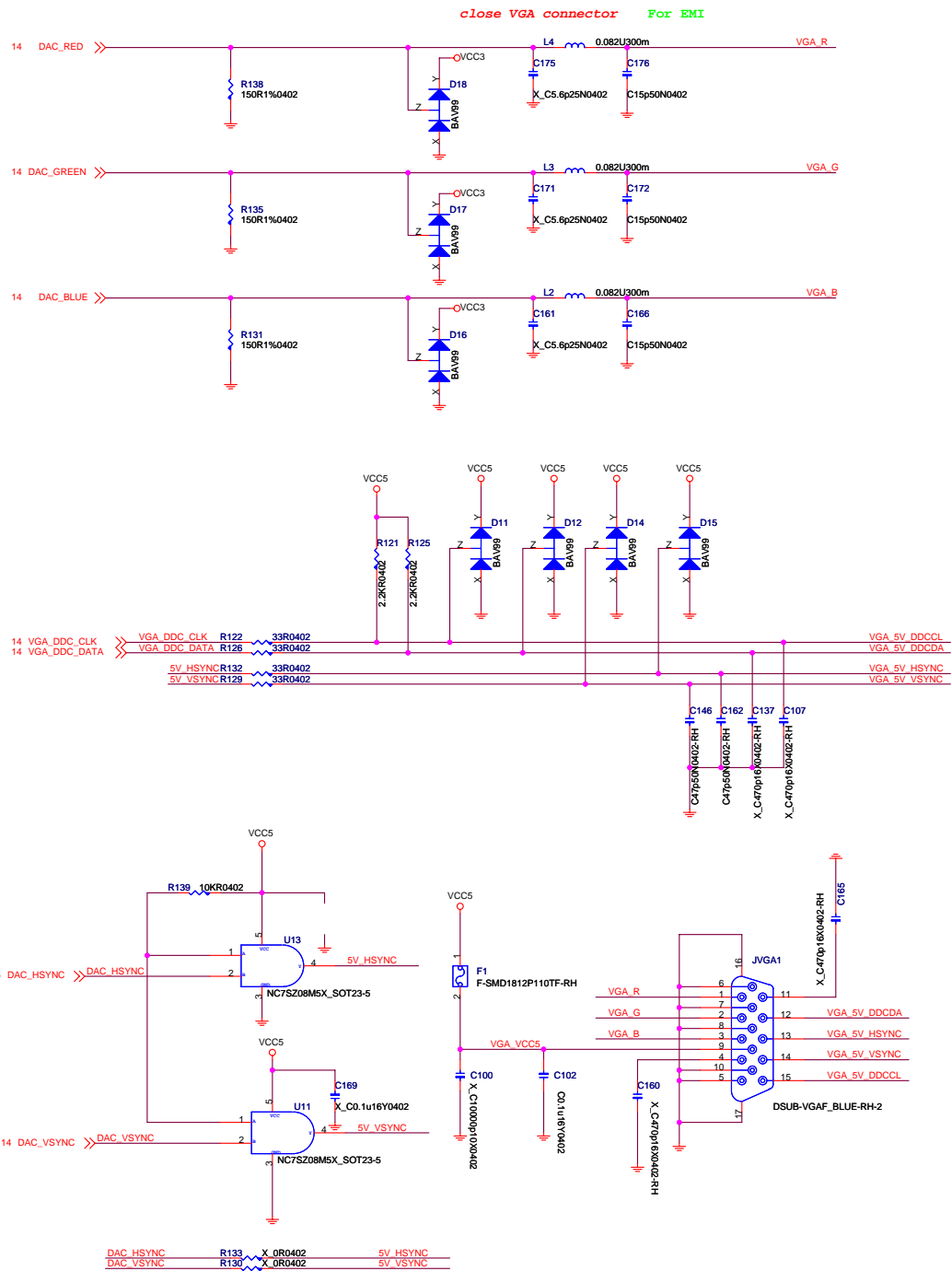
IDSEL = AD23  
MASTER = PCI\_REQ#2  
PCI\_GNT#2  
PCI\_INTZ#

### PCI PULL-UP / DOWN RESISTORS



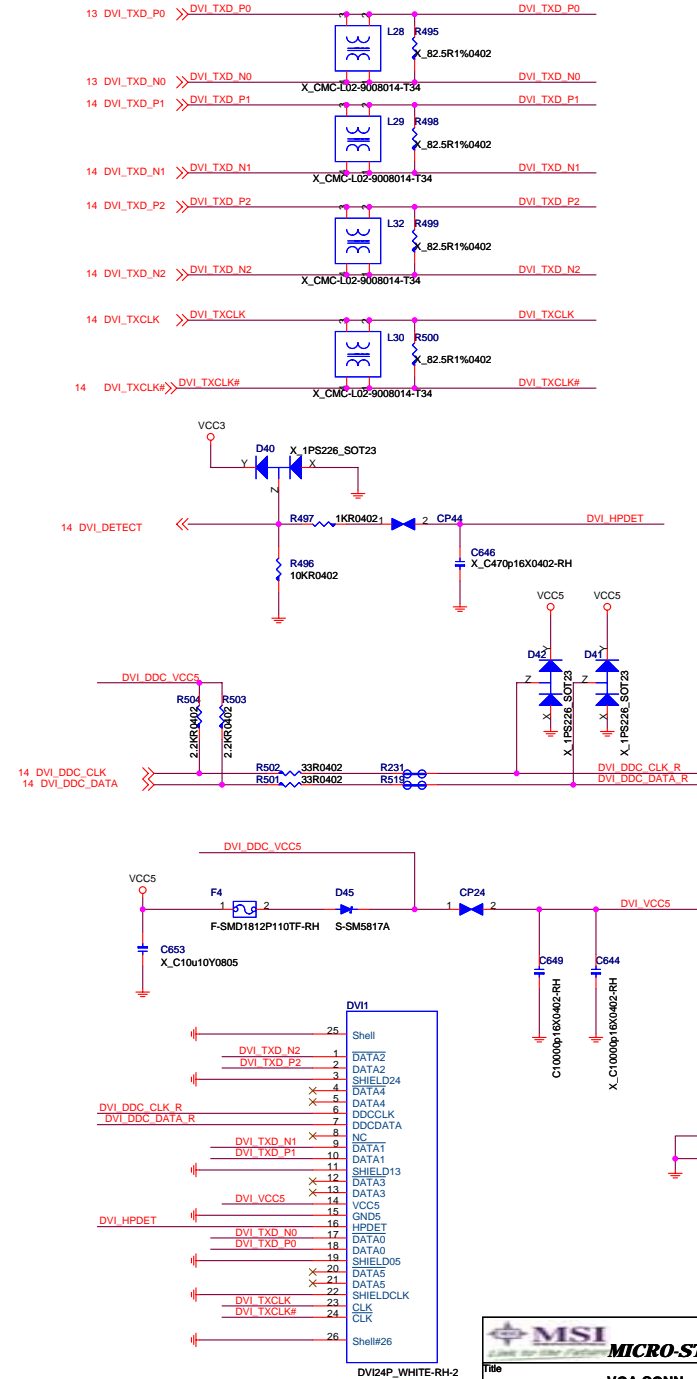
SDONE R384 X OR0402 SM\_CLK 17.23.24.29.32  
SBO# R385 X OR0402 SM\_DATA 17.23.24.29.32

### VGA CONNECTOR

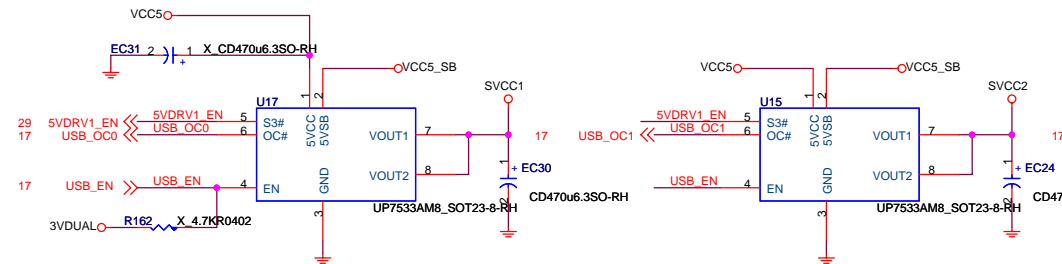


## DVI CONNECTOR

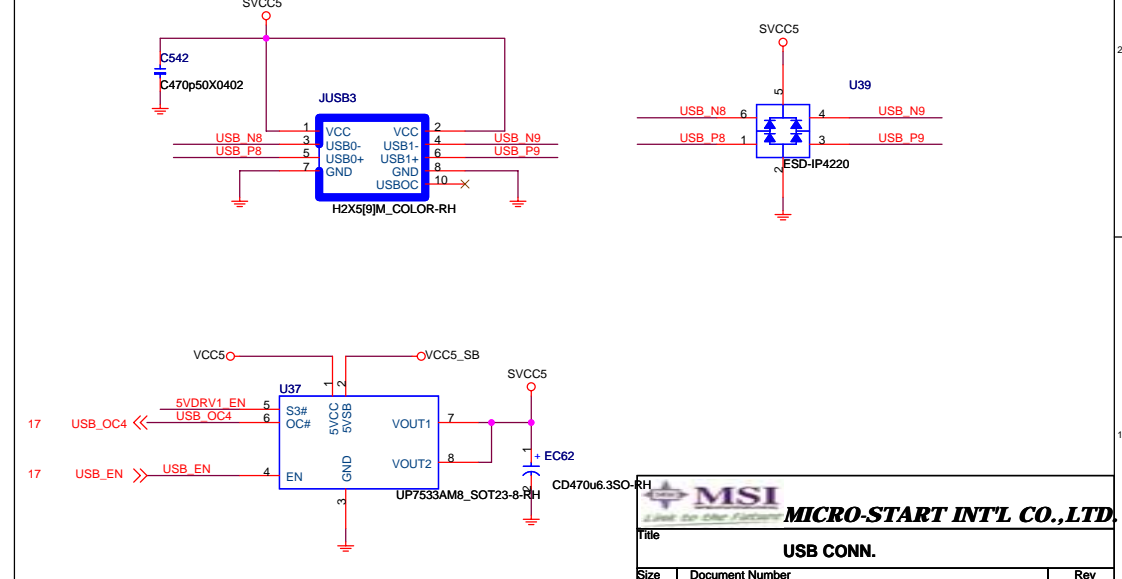
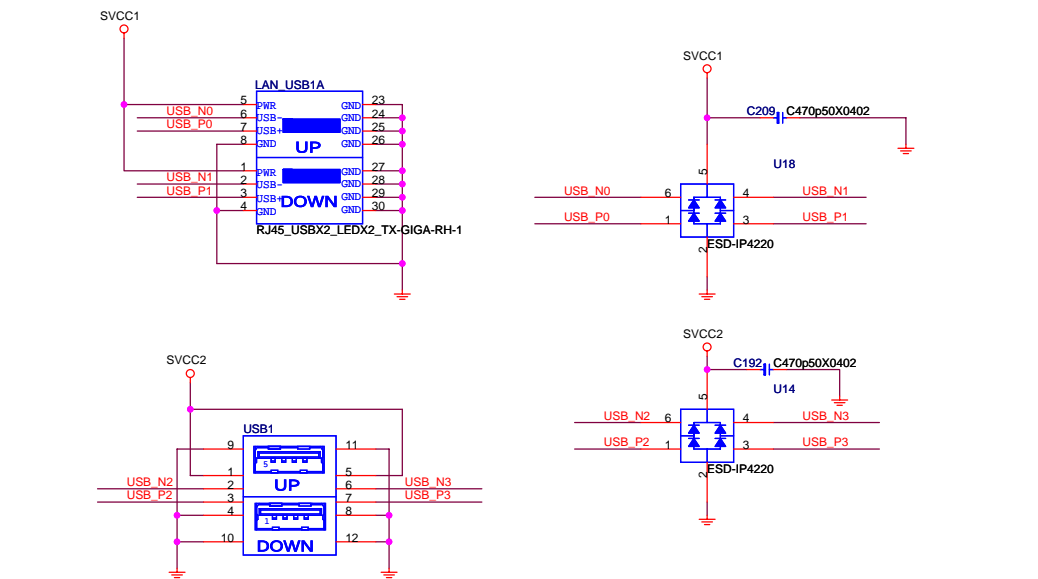
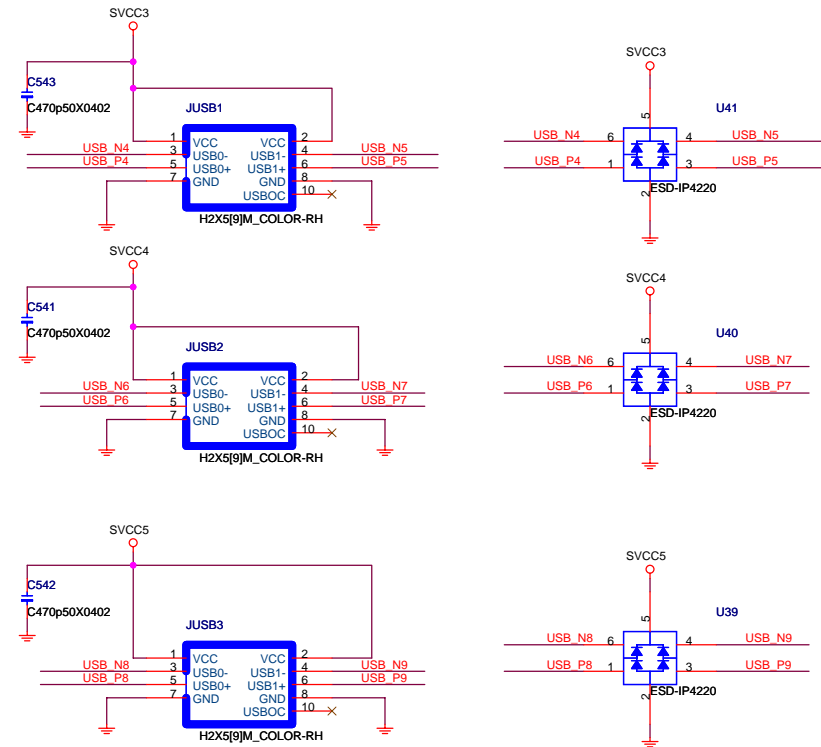
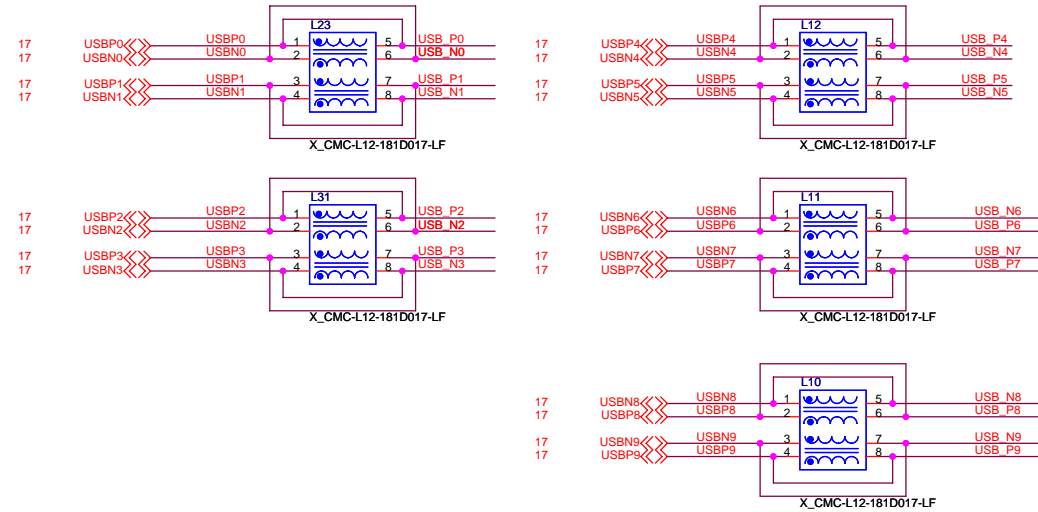
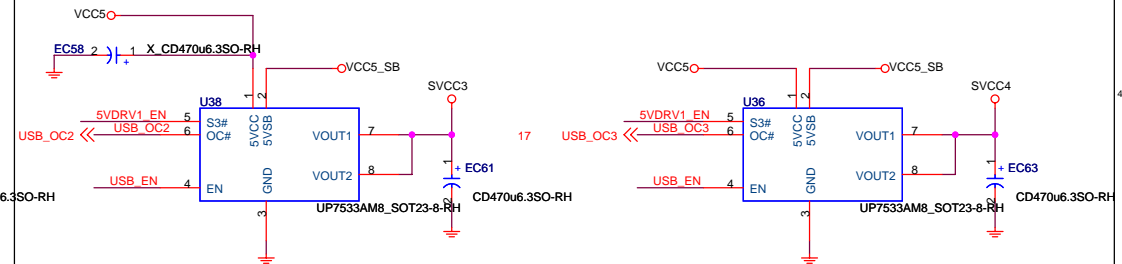
for EMI place near connector

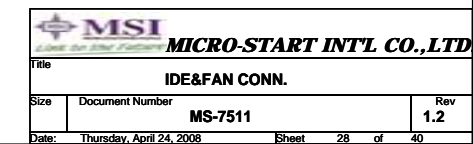
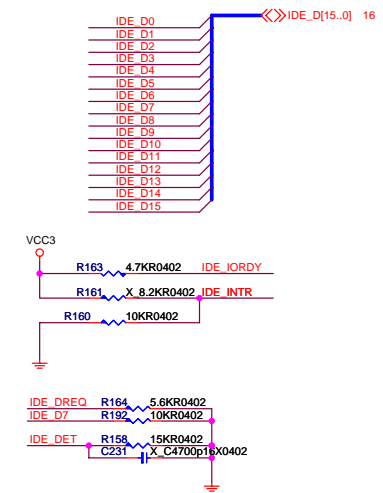


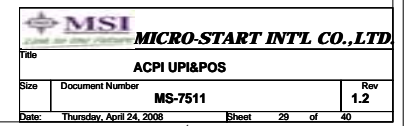
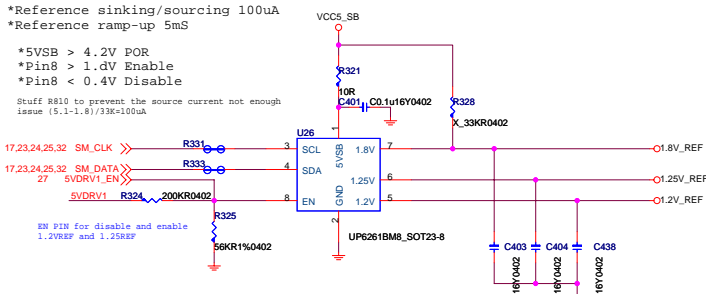
# Rear USB power



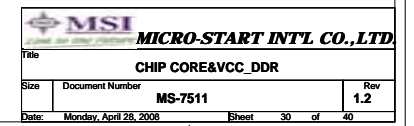
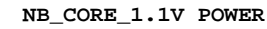
# front USB power







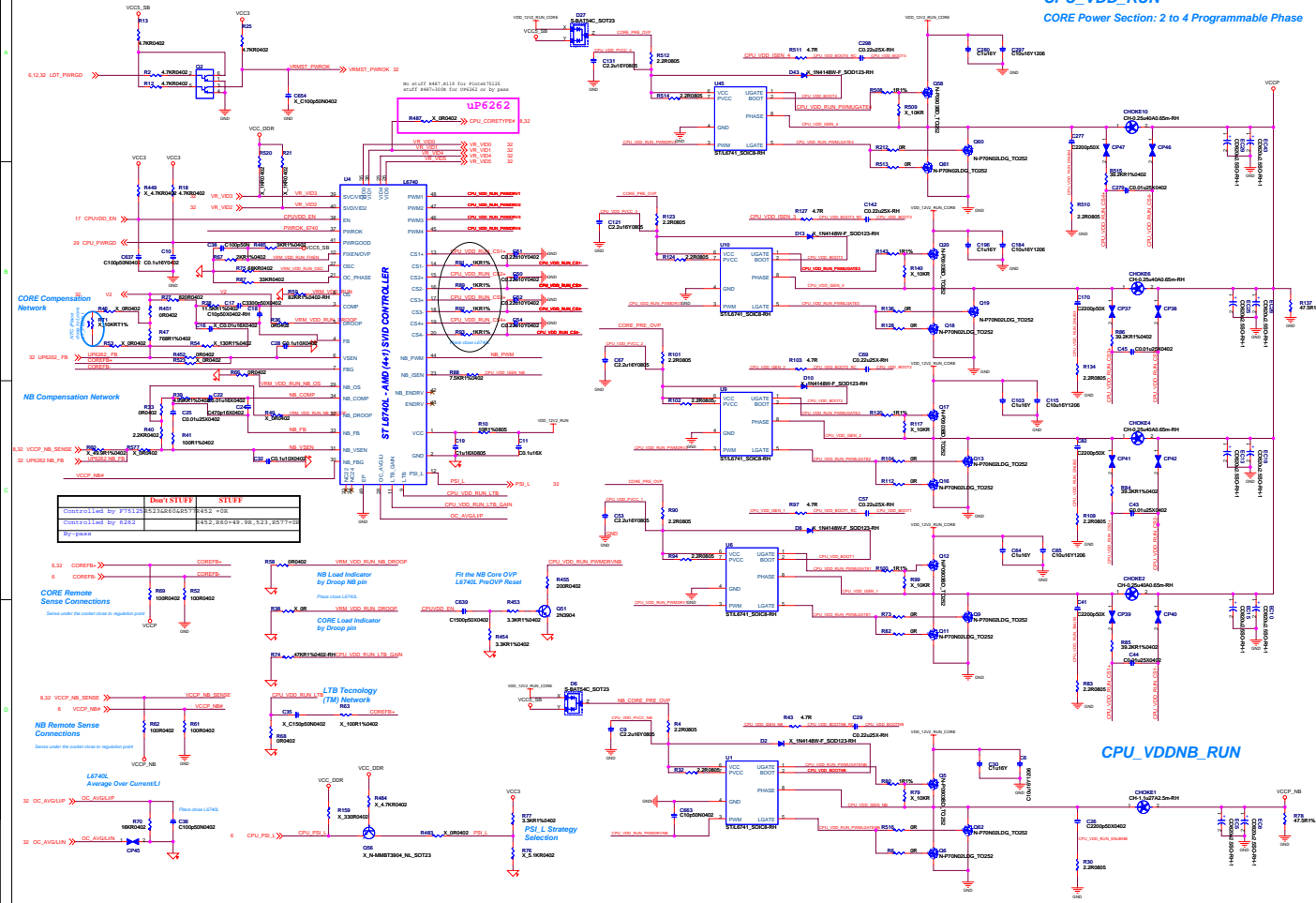
## DDR II 1.8V POWER



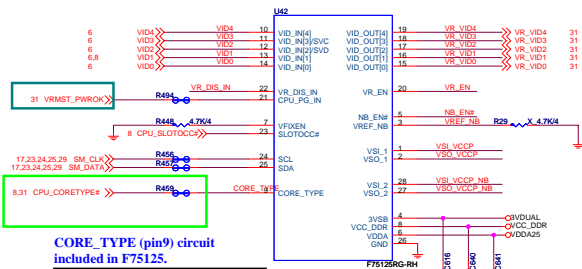
# ST6740+6741

## CPU\_VDD\_RUN

CORE Power Section: 2 to 4 Programmable Phase

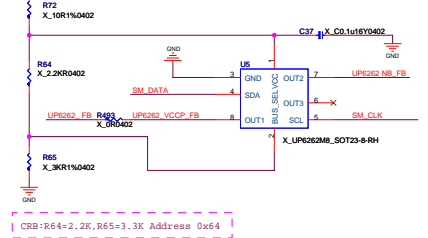


## FINTEK75125 : VCCP & VCCP\_NB OV



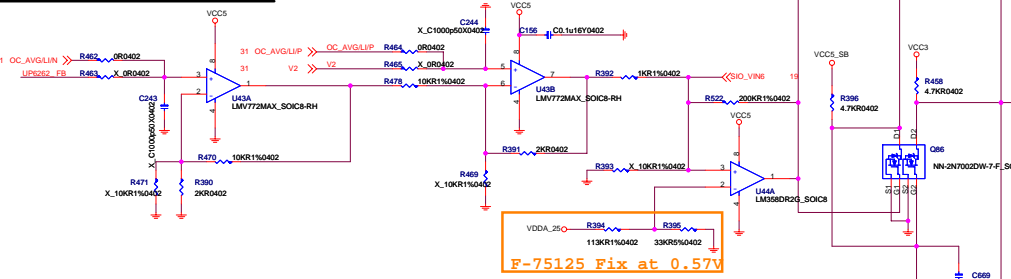
CPU\_PG\_IN enable the second level of VCORE (parallel level is different from Serial level), please refer to Fig.4

## UP6262 : VCCP & VCCP\_NB OV



CRB:R64=2.2K, R65=3.3K Address 0x64

## F-75125 PSI\_L trigger event



## Power Wattle Monitor

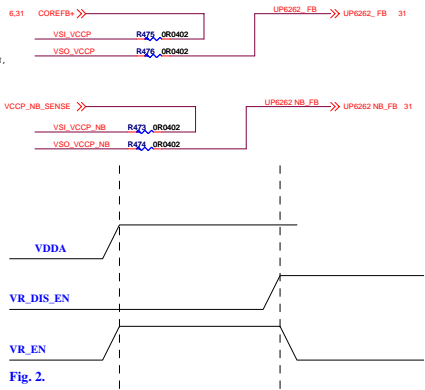
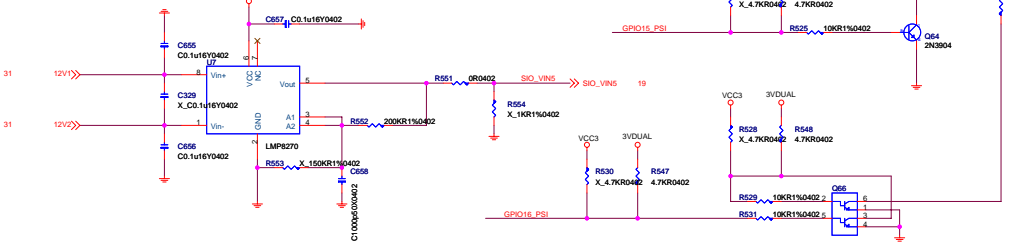


Fig. 2.

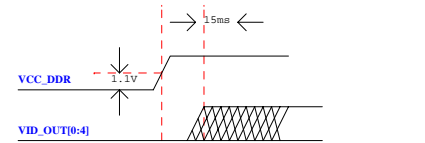


Fig. 3. Serial VID.

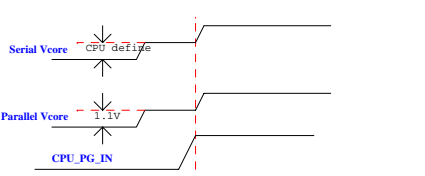


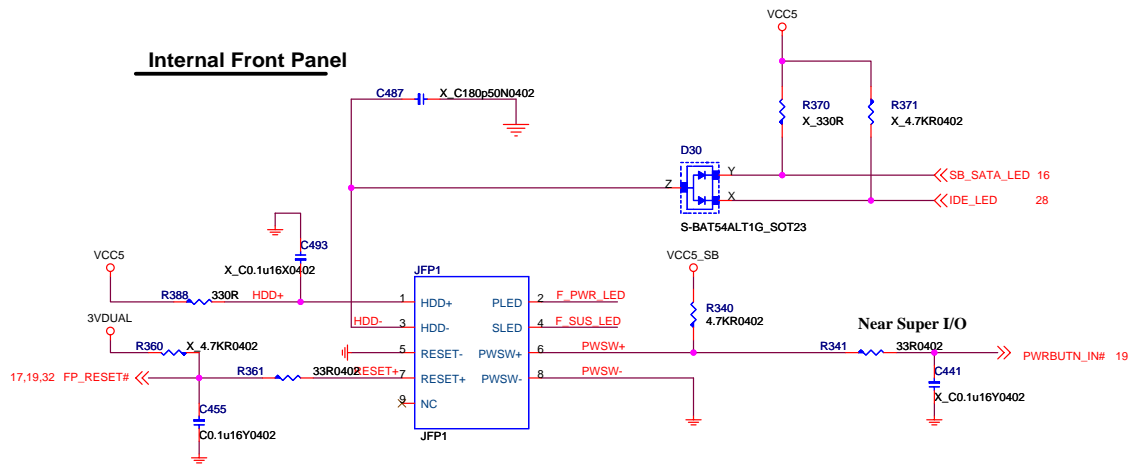
Fig. 4. Serial.

## SMBus GPIO controller

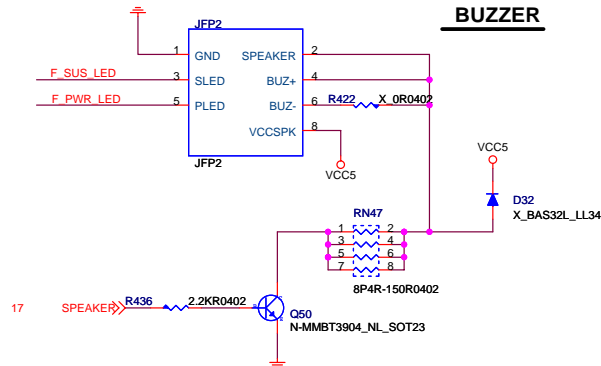
CRB:A2/A1/A0 Internal Weak PD SMBus Address 0x011 00b

MSI MICRO-START INTL CO.,LTD		
CPU POWER SEQUENCE		
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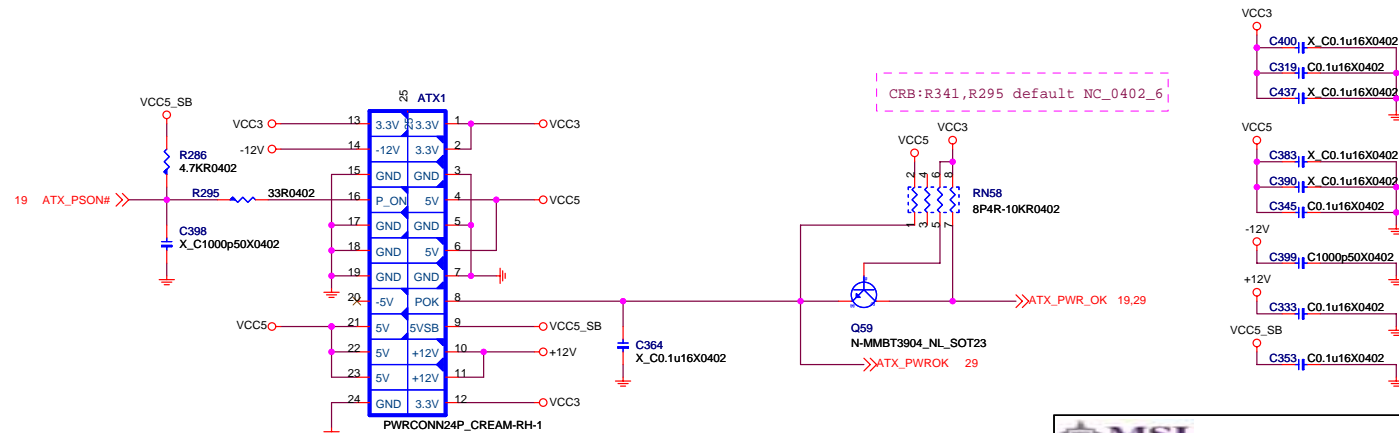
## Internal Front Panel



## BUZZER

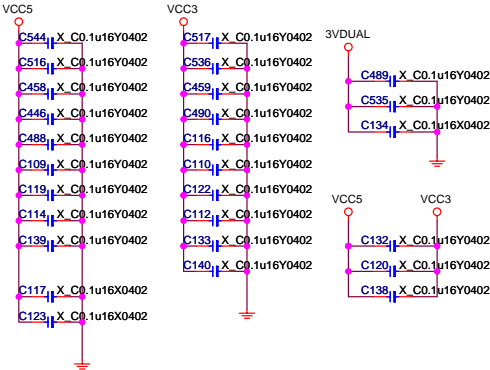


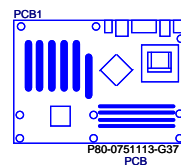
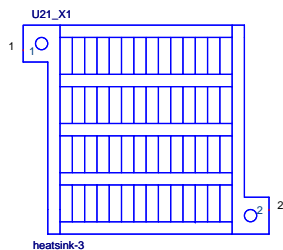
## ATX Connector



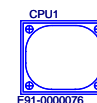
EMI solution

PCI SLOT DECOUPLING CAPACITORS



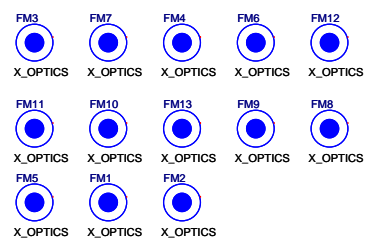


S\_BAT1\_X1  
BAT-BCR2032P-RH

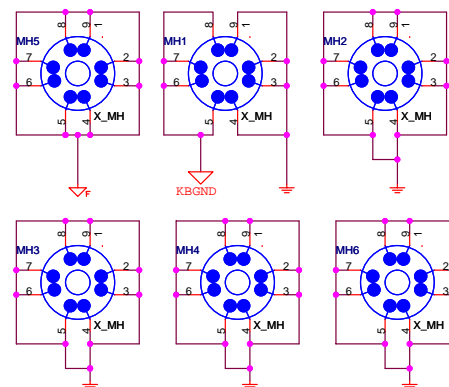


E91-0000076

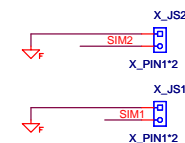
### Optics Orientation Holes



### Mounting Holes



### Simulation

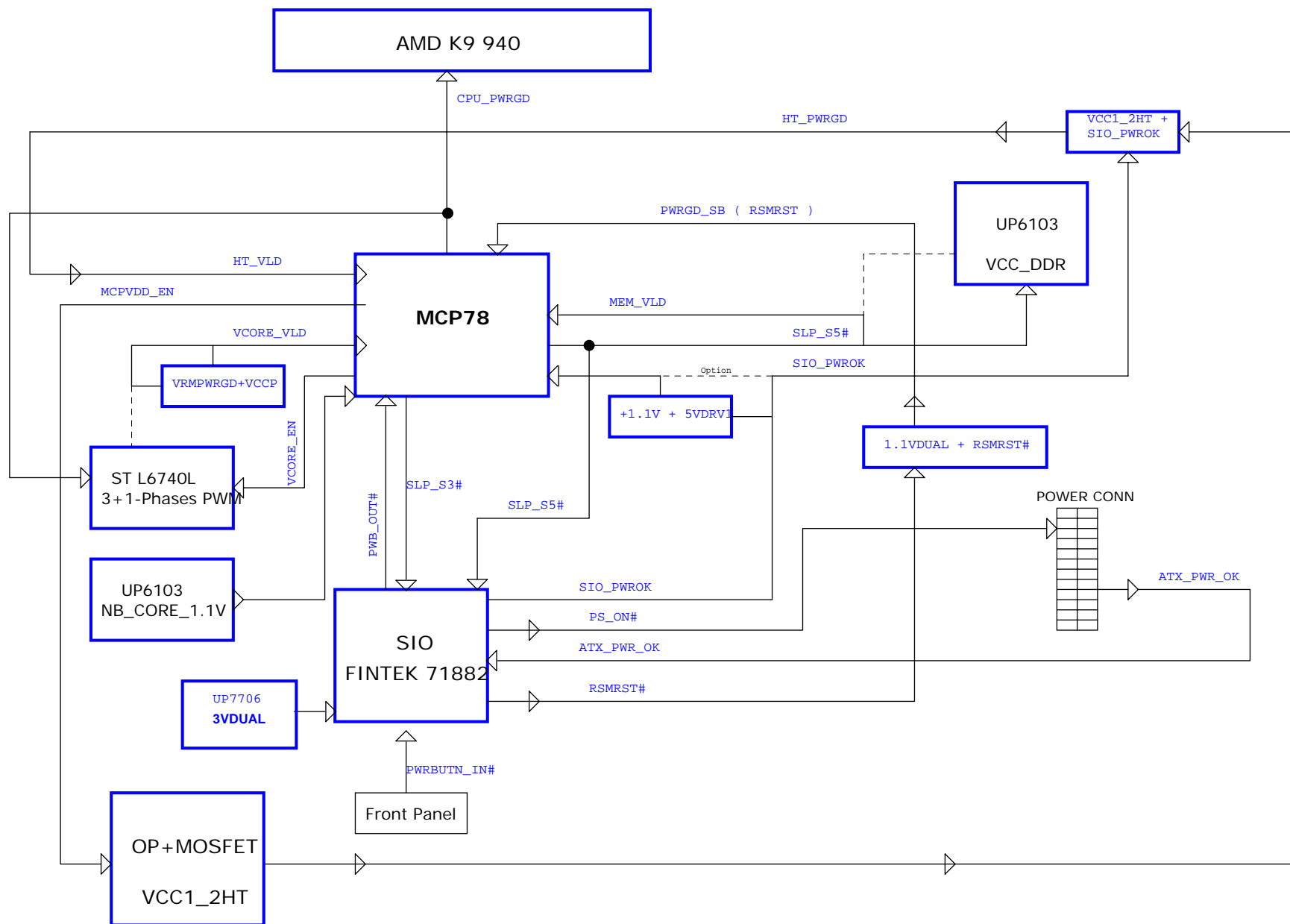


### Model option table

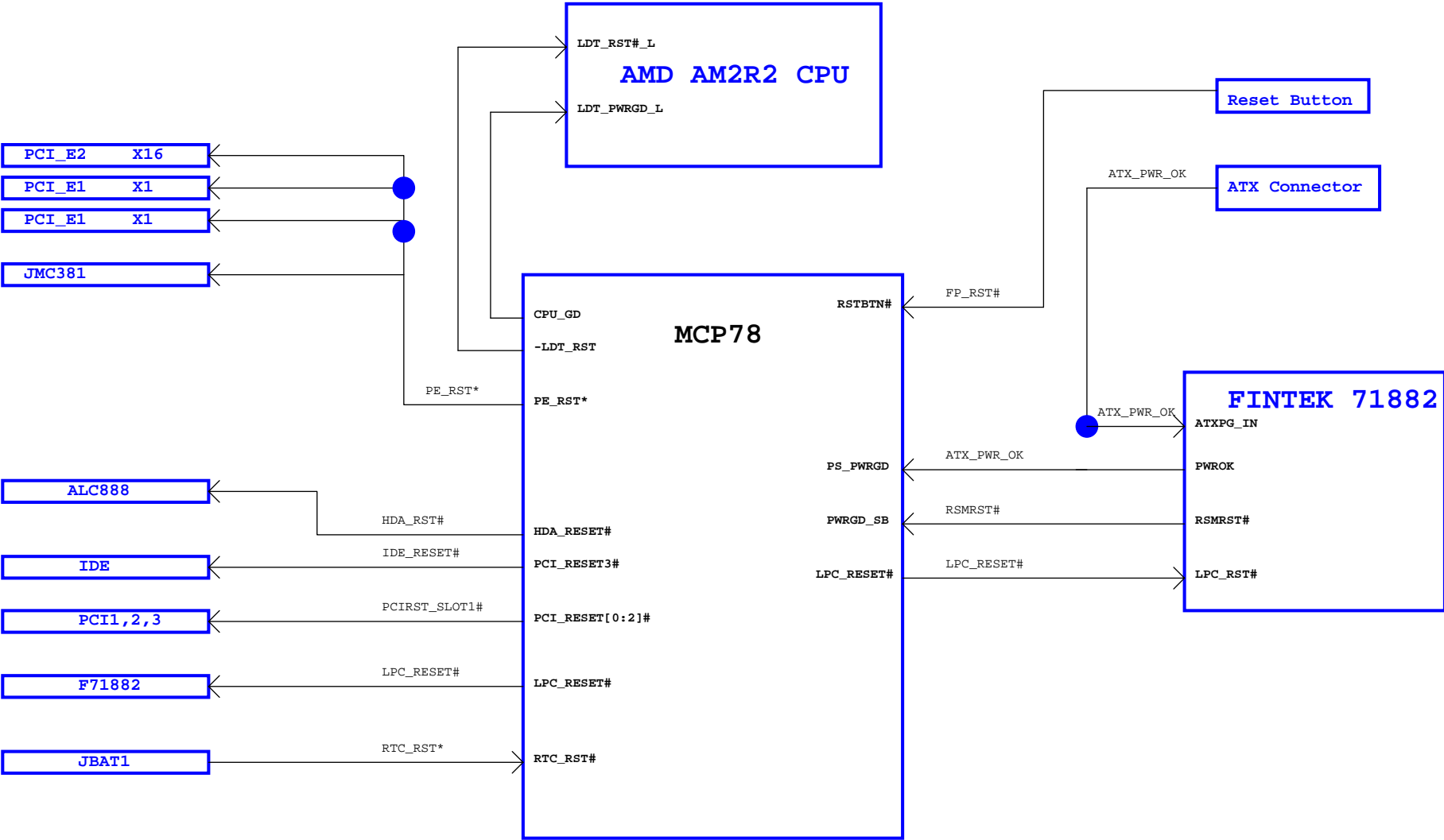
Model type	Function	BOM Config	ERP BOM No.
MS-7511	MCP78D+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+1Audio+RJ45	CFG-MCP78H	601-7511-01S
MS-7511	MCP78H/S+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+VGA+1Audio+RJ45	CFG-MCP78S	601-7511-02S



# PWROK MAP



RESET MAP





MS-7511 OA

2007/09/07

- 1.page14 Remove R53,54,55 follow EMI disain
- 2.page21 Remove reserved R200
- 3.page33 Remove reserved Q58/Remove ATX\_PWROK level shift RN58,Q59
- 4.page17,26 Modify the USB\_OC circuit
- 5.page32 R340(PWSW+) change to pull-hi to VCC5\_SB
- 6.page29 Q10 D. S reverse
- 7.page30 Reserved R7,R8
- 8.page26 L10 USB FN reversed
- 9.page8,19 Remove CPU\_SLOTOCC#
- 10.page29 R279 pull-hi to 3VDDAL
- 11.page31 power swap phasel and phase2

2007/10/19

- 1.page17 USBREBIAS R445 change to 909R1# refer to APhone
- 2.page08 C559 modify ASM C0MM to 5020
- 3.page6,29,30 For AD1Q. remove R17,R231,fit 1.1VDDAL and NB\_CORE\_1.1V to 1.1V level
- 4.page31 Remove R449
- 5.page29 Stuff C403,C404,C438 to fit the reference sawtooth; Stuff Q1,Q31 for POS
- 6.page14 stuff R260,C377 for ix the VGA fail issue
- 7.page30 Reserved R7,R8

2007/10/19

- 1.page14 Modify C370,C371 15pF to fit RTC slow issue
- 2.page17 And reserved C306,C557
- 3.page15,25 Modify PCI slot2 to PCI\_REQ#4/PCI\_GNT#4 due to PCI\_REQ#1/GNT# cannot porting right
- 4.page32 Add Fintk75125 circuit
- 5.page14,26 Instead VGA with DVI
- 6.page23 Modify the termination R to RN56,RN57 560m5#
- 7.page29,30 NB\_CORE1.1V follow the ramp up of 1.2V\_NT; Reserve ATX\_PWR\_OK as the PS\_PWRGD
- 8.page16 Swap the part reference SATA4 &SATA5
- 9.page26,30 Modify EC17,EC23,EC24,EC30,EC61,EC62,EC63 footprint to C,P3,S\_DR\_H11,5
- 10.page31 R59,R91,R92 value Add R485 3KR and modify R67 2KR to fit at 2.0V precisely; Reserve Q51 for PVI OVP trigger to prevent noboot
- 11.page21 Update Audio jack footprint to AUDIO\_JACK6\_26P\_U1
- 12.page22 Remove R159;add C359,C377 ;modify C292,C111 for EMI
- 13.page17 Reserve EC64;Add C645 close to pin U21.K3
- 14.page29 Reserve the Special PSU sequence circuit
- 15.Page26 Modify RN21,RN24 to reserved L23,L31
- 16.Page 6 Remove R17,R231;Reserve R487,R488

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2008/01/07

- 1.page 6 Add R489,R490 for Phenom noise issue Apname
- 2.page21 Modify JACK1 footprint to AUDIO\_JACK6\_26P\_U1; short AUDIO1/AUDIO2 to GNDP for 3 Hole connector
- 3.page30 Reserve R491,R492,Q57 for debug to fit VCORE\_1.1V ramp up with 1.2V\_NT controlled by HT\_EN; R232=15.8KR1#
- 4.page31 Remove R21;Modify R59 to 82KR1#;Not stuff R58 and stuff R49
- 5.page32 Reserve R493,R494 for 75125;R64=2.2K,R65=3.3K Address 0x64
- 6.page24 Separate PCIE1&X PE\_RESET# from 1X device for Hybrid SLI

MS-7511 1.2


2008/02/17

- 1.page 13,14,26 Add DVI connetotor
- 2.page14 R251,R257 modify to 1.47KR1#
- 3.page17 R245 modify to 845R1#
- 4.page19,20 Remove COM1 and modify COM2 to SIO UART A port
- 5.page21 For WQL: R425 modify to 348R1#,C613 modify to 10uXSR, R440,R441,R442,R443 modify to 100R
- 6.page31 PWR solution 4Phase 12MOS;Add Q62,D27
- 7.page12-18 Modify PLL filter follow NV Apname(DA-03779)
- 8.page27 Modify UF7533 Pin5 to 5VDRV1\_EN
- 9.page19,33 Modify SIO pin7# to ATX\_PWR\_OK;remove R231
- 10.page6,8 Modify R107,R108,R81,R96 modify to R0805 aize
- 11.page19 Modify 1.2V\_NT\_VLD circuit
- 12.page26 Add R231,R519,D45
- 13.page31,32 Add R21,R520,R17,R521;Remove R477,R249; modify NB\_EN# pull up to 3VDDAL
- 13.page17,19 RN26,RN24 swap pins
- 14.page19,31,32 Update UF75125 and PSI circuit ,and GPIO pins

MS-7511 1.3

2008/04/15

- 1.page30 Reserve R580
- 2.page31 Add ST 6740 PSI inPVI+ PREOVP Reset circuit; Add PWROK&CPUVDN\_EN sequence patch circuit
- 3.page32 Add GPIO controller W83L603G;update PSI circuit; Add 12V Power Wattage Monitor circuit
- 4.page28 Remove EC39 and reserve C670

 <b>MICRO-START INT'L CO.,LTD.</b>			
Title <b>HISTORY</b>			
Size	Document Number <b>MS-7511</b>		Rev <b>1.2</b>
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