MS-7511

ATX(305mm X 220mm)

CPU:

AMD AM2/AM2+ Socket940

System Chipset:

North Bridge --- MCP78

South Bridge --- NA

OnBoard Chipset:

Clock Gen:NA

AZALIA Codec:ALC888

LAN Chip: REL8211BL

SIO:Fintek 71882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (MCP)

Main Memory:

DDRII* 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 3

PWM:

Controller:STL6740L+6741

ACPI:

UPI solution

Other:

FDD *1
SATA(SATA2-300MB/s) * 6
USB2.0 *10 (Rear*4 Front*6)
COM PORT *1
LPT PORT *1

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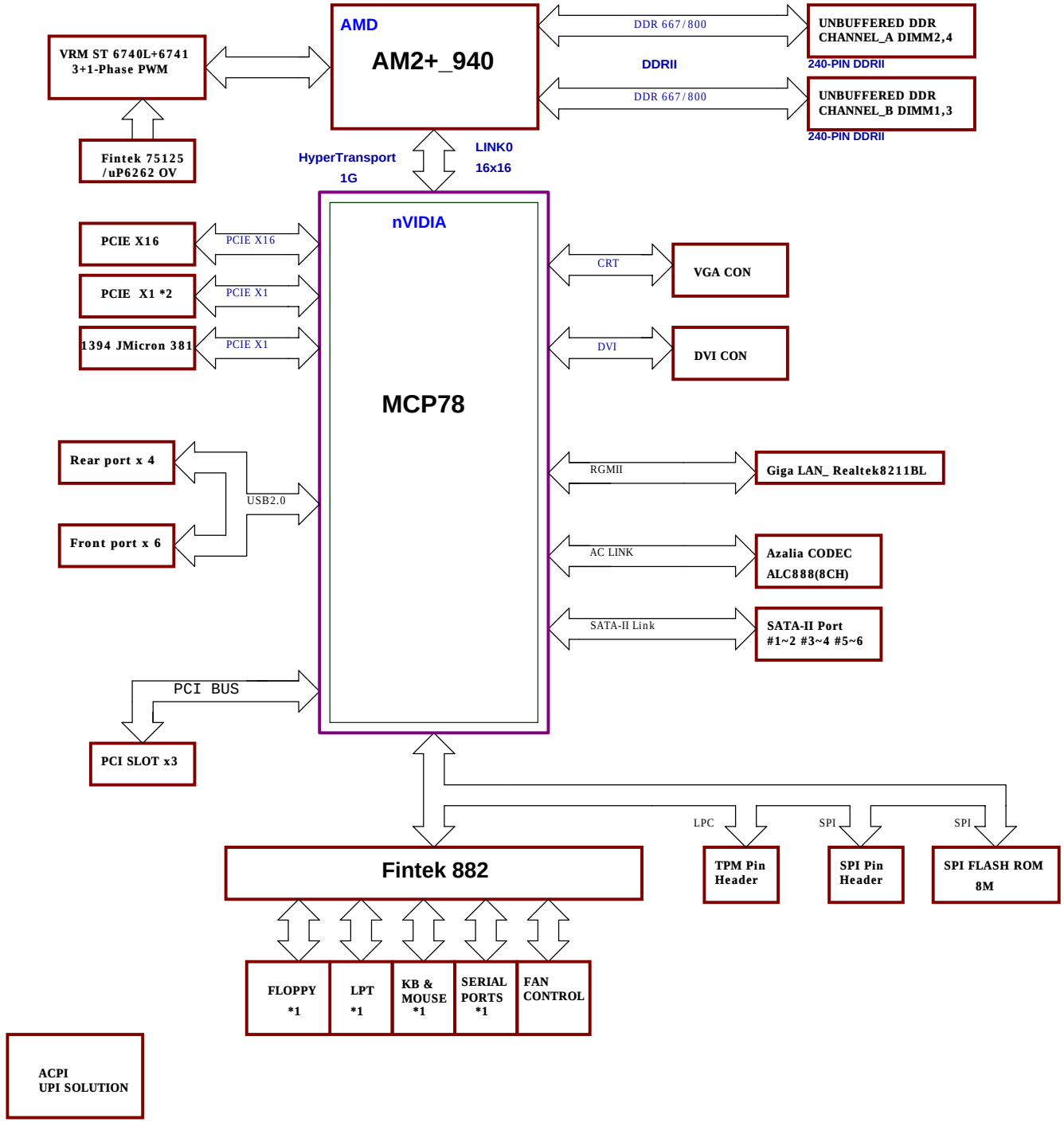

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Title	BLOCK DIAGRAM	
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA0_CLK_H0/L0 MEM_MA0_CLK_H1/L1 MEM_MA0_CLK_H2/L2
DIMM 3 CH-A	10100010B A2H	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 2 CH-B	10100001B A4H	MEM_MB0_CLK_H0/L0 MEM_MB0_CLK_H1/L1 MEM_MB0_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	LAN_USB1	USB0- USB0+ USB1- USB1+	USB_OC0
	USB1	USB2- USB2+ USB3- USB3+	USB_OC1
Front	JUSB1	USB4- USB4+ USB5- USB5+	USB_OC3
	JUSB2	USB6- USB6+ USB7- USB7+	USB_OC4
	JUSB3	USB8- USB8+ USB9- USB9+	USB_OC5
	JUSB4	USB10- USB10+ USB11- USB11+	

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ0# PCI_GNT0#	AD21	PCI_CLKSLOT1 (PCI_CLK0)
PCI Slot 2	PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z	PCI_REQ1# PCI_GNT1#	AD22	PCI_CLKSLOT2 (PCI_CLK1)
PCI Slot 3	PCI_INT#Z PCI_INT#W PCI_INT#X PCI_INT#Y	PCI_REQ2# PCI_GNT2#	AD23	PCI_CLKSLOT3 (PCI_CLK2)
TPM				PCICLK_TPM (TPM_CLK)
Chipset				PCI_CLKIN (PCICLK4)
LPC				LPC_CLK
SIO				LPC_SIO24M

PCI DEVICE RESET MAP

MCP78	
Signals	Target
PCI_RESET#0	PCISLOT1
PCI_RESET#1	PCISLOT2
PCI_RESET#2	PCISLOT3
LPC_RESET#	SIO/TPM
IDE_RESET#	IDE

CPU VID TABLE	
VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

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Title: DEVICE MAP		
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MCP78 general purpose I/O

Name	Pin	Type	Function Description
GPIO_1	F2	I/O	NC
GPIO2/NMI#	F1	I/O	**PWR_SW_GPIO1**
GPIO3/SMI#	F6	I/O	**RST_GATE_GPIO2**
GPIO4/SCI_INTR#	J8	**I/O**	**USB_EN** Set as GPO When high turn on SVCC When low turn off SVCC
GPIO5/INIT#	G3	I/O	**DUAL_CTRL** Set as GPO When high turn on 5VDIMM in S4/S5 When low turn off 5VDIMM in S4/S5
GPIO6/FERR/SYS_SERR#	G5	I/O	NC
GPIO7/NFERR/SYS_PERR#	G6	I/O	NC
GPIO8/SPI_DI	D3	I/O	**SPI_DI**
GPIO9/SPI_DO	D4	I/O	**SPI_DO**
GPIO10/SPI_CS	E4	I/O	**SPI_CS#**
GPIO11/SPI_CLK	E3	I/O	**SPI_CLK**
MII_RESET/GPIO12#	C27	I/O	MII_RESET
MII_COL/GPIO13/MI2C_DATA	E24	I/O	MII_COL
MII_CRS/GPIO14/MI2C_CLK	F23	I/O	MII_CRS
LPC_DRQ1/GPIO15/FANRPM1#	B9	I/O	NC
DDC_CLKGPIO17	B6	I/O	DDC_CLK
DDC_DATA/GPIO19	A6	I/O	DDC_DATA
PROCHOT#/GPIO20	AD8	I/O	PROCHOT#
PE_WAKE#/GPIO21	B22	I/O	PE_WAKE#
HDA_SDATA_IN0/GPIO22	A2	I/O	HAD_SDATA_IN0
HDA_SDATA_IN1/GPIO23	B1	I/O	NC
HDA_SDATA_IN2/GPIO24	B2	I/O	NC
USB_OC0#/GPIO25	P7	I/O	USB_OC0
USB_OC1#/GPIO26	P8	I/O	USB_OC1
USB_OC2#/GPIO27	P9	I/O	USB_OC2
USB_OC3#GPIO28	P5	I/O	USB_OC3
USB_OC4#/GPIO29	P6	I/O	USB_OC4
PCI_PME#/GPIO30	E22	I/O	PCI_PME#
SIO_PME#/GPIO31	F4	I/O	SIO_PME#
EXT_SMI#/GPIO32	F3	I/O	NC
RI/GPIO33	H4	I/O	NC
SUS_CLK/GPIO34	E1	I/O	NC
MII_INTR/GPIO35	G24	I/O	MII_INTR
MII/RXER/GPIO36	D24	I/O	MIIRXER
MII_PWRDOWN/GPIO37	F24	I/O	NC
PCI_REQ3/GPIO38/RS232_CTS#	H14	I/O	PCI_REQ3 Pull hi to VCC3
PCI_GNT3/GPIO39/RS232_RTS#	J14	I/O	PCI_GNT3 Pull hi to VCC3
PCI_REQ2/GPIO40/RS232_DSR#	C11	I/O	PCI_REQ2
PCI_GNT2/GPIO41/RS232_DTR#	B10	I/O	PCI_GNT2
PCI_PERR/GPIO43/RS232_DCD#	G18	I/O	PCI_PERR
HDA_SYNC/GPIO44	B3	I/O	HAD_SYNC
HAD_SDATA_OUT0/GPIO45	A3	I/O	HAD_SDATA_OUT0
THERM_ALERT#/GPIO47	AF7	I/O	CPU_THERM_ALERT#
THERM_SIC/GPIO48	AH7	I/O	NC
THERM_SID/GPIO49	AF8	I/O	NC
LPC_DRQ0#/GPIO50	C9	I/O	LPC_DRQ0#
PCI_REQ4#/GPIO52	H14	I/O	PCI_REQ4# Pull hi to VCC3
PCI_GNT4#/GPIO53	D13	I/O	PCI_GNT4# Pull hi to VCC3
LPC_PWRDWN#/GPIO54	C8	I/O	NC
A20GATE/GPIO55	F5	I/O	A20GATE
KBDRSTIN#//GPIO56	A4	I/O	KBRST#
SATA_LED#/GPIO57	A5	I/O	SB_SATA_LED#
THERMTRIP#/GPIO58	AE8	I/O	CPU_THRIP#
THERM/GPIO59	C6	I/O	THERM#
FANRPM0/GPIO60	E6	I/O	NC
FANCTL0/GPIO61	D6	I/O	NC
FANCTL1/GPIO62	C5	I/O	NC

Super I/O general purpose I/O

Name	Pin	Type	Function Description
VIDOUT0/GPIO0	49	I/O	GPIO0_PSI
VIDOUT0/GPIO1	50	I/O	GPIO1_PSI
VIDOUT0/GPIO2	51	I/O	GPIO2_PSI
VIDOUT0/GPIO3	52	I/O	GPIO3_PSI
VIDOUT0/GPIO4	53	I/O	Reserved for BIOS USE
VIDOUT0/GPIO5/SID	54	I/O	Reserved for BIOS USE
SLOTOCC#/GPIO6	55	I/O	Reserve pull hi to 3VUDAL
GPIO7/TURBO1#/WDTRST#	56	I/O	WDTRST# is used for over clock
GPIO10/SPI_CLK/FANIN4	59	I/O	**DLED1**
GPIO11/SPI_CS0#/FABCTL4	60	I/O	**DLED2**
GPIO12/SPI_MISO/FANCTL1_1	61	I/O	**DLED3**
PIO13/SPI_MOSI/BEEP	62	I/O	NC
GPIO14/FWH_DIS/WDTRST#/SPI_CS1#	63	I/O	**DLED4**
GPIO15/LED_VSB/ALERT#	64	I/O	**LED_VSB**
GPIO16/LED_VCC/TURBO2#	65	I/O	**LED_VCC**
GPIO17	66	I/O	**SPI_WP#**
PCIRST1# /GPIO20	74	I/O	NC
PCIRST2# /GPIO21	75	I/O	NC
PCIRST3# /GPIO22	76	I/O	NC
GPIO23/RSTCON#	77	I/O	**SIO_GPIO_FANTYPE** For CPU FAN type select: when 3pin GPIO should be low when 4 pin GPIO should be high
ATXPG_IN/GPIO24	84	I/O	ATX_PWEROK
PME#/GPIO25	79	I/O	SIO_PME#
PWSIN# /GPIO26	80	I/O	PWRBUT_IN#
PWSOUT#/GPIO27	81	I/O	PWB_OUT#
S3#/GPIO31	82	I/O	SLP_S3#
PSON# /GPIO31	83	I/O	ATX_PSON#
PWROK/GPIO32	84		PWROK Set delay time as 100ms
RSMRST# /GPIO33	85		SIO_RSMRST#
IRTX/GPIO42	27		**IRTX**
IRRX/GPIO43	28		**IRRX**

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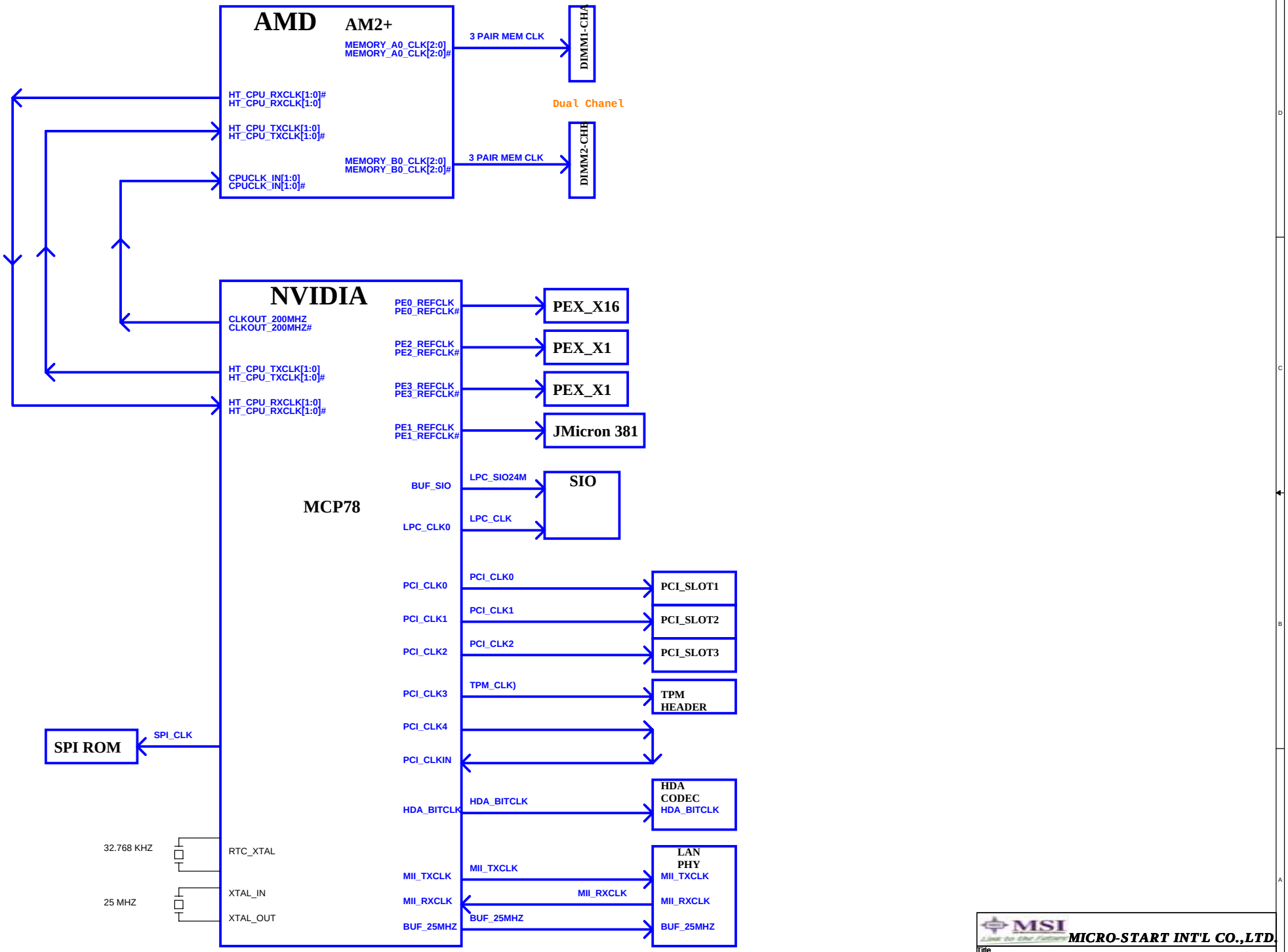

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Title	CLOCK DISTRIBUTION	
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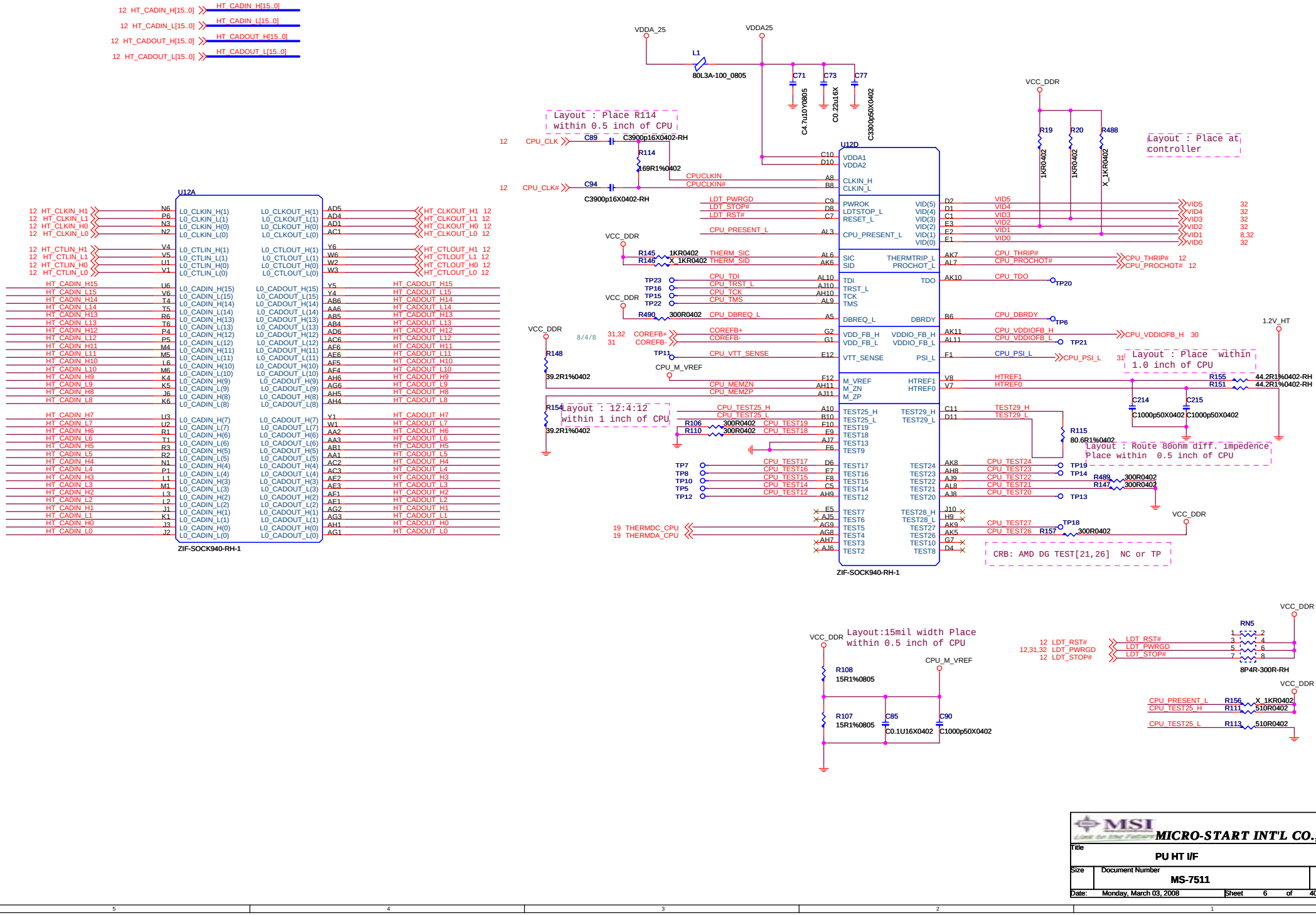

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Title	PU HT I/F	
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9,10 MEM_MA_DQS_L[7..0]
9,10 MEM_MA_DQS_H[7..0]
9,10 MEM_MA_DM[7..0]
9,10 MEM_MA_DATA[63..0]
9,10,11 MEM_MA_ADD[15..0]

9,10 MEM_MB_DQS_L[7..0]
9,10 MEM_MB_DQS_H[7..0]
9,10 MEM_MB_DM[7..0]
9,10 MEM_MB_DATA[63..0]
9,10,11 MEM_MB_ADD[15..0]

U12B

9,11 MEM_MA0_CLK_H2	MEM_MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)	AE14	MEM_MA_DATA63
9,11 MEM_MA0_CLK_L2	MEM_MA0_CLK_L2	AG20	MA0_CLK_H(1)	MA_DATA(62)	AG14	MEM_MA_DATA62
9,11 MEM_MA0_CLK_H1	MEM_MA0_CLK_H1	G19	MA0_CLK_L(1)	MA_DATA(61)	AG16	MEM_MA_DATA61
9,11 MEM_MA0_CLK_L1	MEM_MA0_CLK_L1	H19	MA0_CLK_H(0)	MA_DATA(60)	AD17	MEM_MA_DATA60
9,11 MEM_MA0_CLK_H0	MEM_MA0_CLK_H0	U27	MA0_CLK_L(0)	MA_DATA(59)	AD13	MEM_MA_DATA59
9,11 MEM_MA0_CLK_L0	MEM_MA0_CLK_L0	U26		MA_DATA(58)	AE13	MEM_MA_DATA58
				MA_DATA(57)	AG15	MEM_MA_DATA57
9,11 MEM_MA0_CS_L1	MEM_MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(56)	AE16	MEM_MA_DATA56
9,11 MEM_MA0_CS_L0	MEM_MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(55)	AG17	MEM_MA_DATA55
				MA_DATA(54)	AE18	MEM_MA_DATA54
9,11 MEM_MA0_ODT0	MEM_MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(53)	AD21	MEM_MA_DATA53
				MA_DATA(52)	AG22	MEM_MA_DATA52
10,11 MEM_MA1_CLK_H2	MEM_MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(51)	AE17	MEM_MA_DATA51
10,11 MEM_MA1_CLK_L2	MEM_MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(50)	AF17	MEM_MA_DATA50
10,11 MEM_MA1_CLK_H1	MEM_MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(49)	AF21	MEM_MA_DATA49
10,11 MEM_MA1_CLK_L1	MEM_MA1_CLK_L1	G21	MA1_CLK_L(1)	MA_DATA(48)	AE21	MEM_MA_DATA48
10,11 MEM_MA1_CLK_H0	MEM_MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(47)	AF23	MEM_MA_DATA47
10,11 MEM_MA1_CLK_L0	MEM_MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(46)	AF23	MEM_MA_DATA46
				MA_DATA(45)	AJ26	MEM_MA_DATA45
10,11 MEM_MA1_CS_L1	MEM_MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(44)	AG26	MEM_MA_DATA44
10,11 MEM_MA1_CS_L0	MEM_MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(43)	AE22	MEM_MA_DATA43
				MA_DATA(42)	AG23	MEM_MA_DATA42
10,11 MEM_MA1_ODT0	MEM_MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(41)	AH25	MEM_MA_DATA41
				MA_DATA(40)	AF25	MEM_MA_DATA40
				MA_DATA(39)	AJ28	MEM_MA_DATA39
9,10,11 MEM_MA_CAS_L	MEM_MA_CAS_L	AB25	MA_CAS_L	MA_DATA(38)	AJ29	MEM_MA_DATA38
9,10,11 MEM_MA_WE_L	MEM_MA_WE_L	AB27	MA_WE_L	MA_DATA(37)	AF29	MEM_MA_DATA37
9,10,11 MEM_MA_RAS_L	MEM_MA_RAS_L	AA26	MA_RAS_L	MA_DATA(36)	AE26	MEM_MA_DATA36
				MA_DATA(35)	AJ27	MEM_MA_DATA35
9,10,11 MEM_MA_BANK2	MEM_MA_BANK2	N25	MA_BANK(2)	MA_DATA(34)	AH27	MEM_MA_DATA34
9,10,11 MEM_MA_BANK1	MEM_MA_BANK1	Y27	MA_BANK(1)	MA_DATA(33)	AG29	MEM_MA_DATA33
9,10,11 MEM_MA_BANK0	MEM_MA_BANK0	AA27	MA_BANK(0)	MA_DATA(32)	AF27	MEM_MA_DATA32
				MA_DATA(31)	E29	MEM_MA_DATA31
10,11 MEM_MA_CKE1	MEM_MA_CKE1	L27	MA_CKE(1)	MA_DATA(30)	E28	MEM_MA_DATA30
9,11 MEM_MA_CKE0	MEM_MA_CKE0	M25	MA_CKE(0)	MA_DATA(29)	D27	MEM_MA_DATA29
				MA_DATA(28)	C27	MEM_MA_DATA28
	MEM_MA_ADD15	M27	MA_ADD(15)	MA_DATA(27)	G26	MEM_MA_DATA27
	MEM_MA_ADD14	N24	MA_ADD(14)	MA_DATA(26)	F27	MEM_MA_DATA26
	MEM_MA_ADD13	AC26	MA_ADD(13)	MA_DATA(25)	C28	MEM_MA_DATA25
	MEM_MA_ADD12	N26	MA_ADD(12)	MA_DATA(24)	E27	MEM_MA_DATA24
	MEM_MA_ADD11	P25	MA_ADD(11)	MA_DATA(23)	F25	MEM_MA_DATA23
	MEM_MA_ADD10	Y25	MA_ADD(10)	MA_DATA(22)	E25	MEM_MA_DATA22
	MEM_MA_ADD9	N27	MA_ADD(9)	MA_DATA(21)	E23	MEM_MA_DATA21
	MEM_MA_ADD8	R24	MA_ADD(8)	MA_DATA(20)	D23	MEM_MA_DATA20
	MEM_MA_ADD7	P27	MA_ADD(7)	MA_DATA(19)	E26	MEM_MA_DATA19
	MEM_MA_ADD6	R25	MA_ADD(6)	MA_DATA(18)	C26	MEM_MA_DATA18
	MEM_MA_ADD5	R26	MA_ADD(5)	MA_DATA(17)	G23	MEM_MA_DATA17
	MEM_MA_ADD4	R27	MA_ADD(4)	MA_DATA(16)	F23	MEM_MA_DATA16
	MEM_MA_ADD3	T25	MA_ADD(3)	MA_DATA(15)	E22	MEM_MA_DATA15
	MEM_MA_ADD2	U25	MA_ADD(2)	MA_DATA(14)	E21	MEM_MA_DATA14
	MEM_MA_ADD1	T27	MA_ADD(1)	MA_DATA(13)	E17	MEM_MA_DATA13
	MEM_MA_ADD0	W24	MA_ADD(0)	MA_DATA(12)	G17	MEM_MA_DATA12
				MA_DATA(11)	G22	MEM_MA_DATA11
	MEM_MA_DQS_H7	AD15	MA_DQS_H(7)	MA_DATA(10)	F21	MEM_MA_DATA10
	MEM_MA_DQS_L7	AE15	MA_DQS_L(7)	MA_DATA(9)	G18	MEM_MA_DATA9
	MEM_MA_DQS_H6	AG18	MA_DQS_H(6)	MA_DATA(8)	E17	MEM_MA_DATA8
	MEM_MA_DQS_L6	AG19	MA_DQS_L(6)	MA_DATA(7)	G16	MEM_MA_DATA7
	MEM_MA_DQS_H5	AG24	MA_DQS_H(5)	MA_DATA(6)	E15	MEM_MA_DATA6
	MEM_MA_DQS_L5	AG25	MA_DQS_L(5)	MA_DATA(5)	G13	MEM_MA_DATA5
	MEM_MA_DQS_H4	AG27	MA_DQS_H(4)	MA_DATA(4)	H13	MEM_MA_DATA4
	MEM_MA_DQS_L4	AG28	MA_DQS_L(4)	MA_DATA(3)	H17	MEM_MA_DATA3
	MEM_MA_DQS_H3	D29	MA_DQS_H(3)	MA_DATA(2)	E16	MEM_MA_DATA2
	MEM_MA_DQS_L3	C29	MA_DQS_L(3)	MA_DATA(1)	E14	MEM_MA_DATA1
	MEM_MA_DQS_H2	C25	MA_DQS_H(2)	MA_DATA(0)	G14	MEM_MA_DATA0
	MEM_MA_DQS_L2	D25	MA_DQS_L(2)			
	MEM_MA_DQS_H1	E19	MA_DQS_H(1)	MA_DQS_H(8)	J28	
	MEM_MA_DQS_L1	F19	MA_DQS_L(1)	MA_DQS_L(8)	J27	
	MEM_MA_DQS_H0	F15	MA_DQS_H(0)			
	MEM_MA_DQS_L0	G15	MA_DQS_L(0)	MA_DM(8)	J25	
	MEM_MA_DM7	AF15	MA_DM(7)	MA_CHECK(7)	K25	
	MEM_MA_DM6	AF19	MA_DM(6)	MA_CHECK(6)	J26	
	MEM_MA_DM5	AJ25	MA_DM(5)	MA_CHECK(5)	G28	
	MEM_MA_DM4	AH29	MA_DM(4)	MA_CHECK(4)	G27	
	MEM_MA_DM3	B29	MA_DM(3)	MA_CHECK(3)	L24	
	MEM_MA_DM2	E24	MA_DM(2)	MA_CHECK(2)	K27	
	MEM_MA_DM1	E18	MA_DM(1)	MA_CHECK(1)	H29	
	MEM_MA_DM0	H15	MA_DM(0)	MA_CHECK(0)	H27	

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U12C

9,11 MEM_MB0_CLK_H2	MEM_MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)	AH13	MEM_MB_DATA63
9,11 MEM_MB0_CLK_L2	MEM_MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)	AL13	MEM_MB_DATA62
9,11 MEM_MB0_CLK_H1	MEM_MB0_CLK_H1	A18	MB0_CLK_H(1)	MB_DATA(61)	AL15	MEM_MB_DATA61
9,11 MEM_MB0_CLK_L1	MEM_MB0_CLK_L1	A19	MB0_CLK_L(1)	MB_DATA(60)	AJ15	MEM_MB_DATA60
9,11 MEM_MB0_CLK_H0	MEM_MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)	AE13	MEM_MB_DATA59
9,11 MEM_MB0_CLK_L0	MEM_MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)	AG13	MEM_MB_DATA58
				MB_DATA(57)	AL14	MEM_MB_DATA57
9,11 MEM_MB0_CS_L1	MEM_MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(56)	AK15	MEM_MB_DATA56
9,11 MEM_MB0_CS_L0	MEM_MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(55)	AL16	MEM_MB_DATA55
				MB_DATA(54)	AL17	MEM_MB_DATA54
9,11 MEM_MB0_ODT0	MEM_MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(53)	AK21	MEM_MB_DATA53
				MB_DATA(52)	AL21	MEM_MB_DATA52
10,11 MEM_MB1_CLK_H2	MEM_MB1_CLK_H2	AL19	MB1_CLK_H(2)	MB_DATA(51)	AH15	MEM_MB_DATA51
10,11 MEM_MB1_CLK_L2	MEM_MB1_CLK_L2	AL18	MB1_CLK_L(2)	MB_DATA(50)	AJ16	MEM_MB_DATA50
10,11 MEM_MB1_CLK_H1	MEM_MB1_CLK_H1	C19	MB1_CLK_H(1)	MB_DATA(49)	AH19	MEM_MB_DATA49
10,11 MEM_MB1_CLK_L1	MEM_MB1_CLK_L1	D19	MB1_CLK_L(1)	MB_DATA(48)	AL20	MEM_MB_DATA48
10,11 MEM_MB1_CLK_H0	MEM_MB1_CLK_H0	W29	MB1_CLK_H(0)	MB_DATA(47)	AJ22	MEM_MB_DATA47
10,11 MEM_MB1_CLK_L0	MEM_MB1_CLK_L0	W28	MB1_CLK_L(0)	MB_DATA(46)	AL22	MEM_MB_DATA46
				MB_DATA(45)	AL24	MEM_MB_DATA45
10,11 MEM_MB1_CS_L1	MEM_MB1_CS_L1	AE29	MB1_CS_L(1)	MB_DATA(44)	AK25	MEM_MB_DATA44
10,11 MEM_MB1_CS_L0	MEM_MB1_CS_L0	AB31	MB1_CS_L(0)	MB_DATA(43)	AJ21	MEM_MB_DATA43
				MB_DATA(42)	AH21	MEM_MB_DATA42
10,11 MEM_MB1_ODT0	MEM_MB1_ODT0	AD31	MB1_ODT(0)	MB_DATA(41)	AH23	MEM_MB_DATA41
				MB_DATA(40)	AJ24	MEM_MB_DATA40
				MB_DATA(39)	AL27	MEM_MB_DATA39
9,10,11 MEM_MB_CAS_L	MEM_MB_CAS_L	AC29	MB_CAS_L	MB_DATA(38)	AK27	MEM_MB_DATA38
9,10,11 MEM_MB_WE_L	MEM_MB_WE_L	AC30	MB_WE_L	MB_DATA(37)	AH31	MEM_MB_DATA37
9,10,11 MEM_MB_RAS_L	MEM_MB_RAS_L	AB29	MB_RAS_L	MB_DATA(36)	AG30	MEM_MB_DATA36
				MB_DATA(35)	AL25	MEM_MB_DATA35
9,10,11 MEM_MB_BANK2	MEM_MB_BANK2	N31	MB_BANK(2)	MB_DATA(34)	AL26	MEM_MB_DATA34
9,10,11 MEM_MB_BANK1	MEM_MB_BANK1	AA31	MB_BANK(1)	MB_DATA(33)	AJ30	MEM_MB_DATA33
9,10,11 MEM_MB_BANK0	MEM_MB_BANK0	AA28	MB_BANK(0)	MB_DATA(32)	AJ31	MEM_MB_DATA32
				MB_DATA(31)	E31	MEM_MB_DATA31
10,11 MEM_MB_CKE1	MEM_MB_CKE1	M31	MB_CKE(1)	MB_DATA(30)	E30	MEM_MB_DATA30
9,11 MEM_MB_CKE0	MEM_MB_CKE0	M29	MB_CKE(0)	MB_DATA(29)	B27	MEM_MB_DATA29
				MB_DATA(28)	A27	MEM_MB_DATA28
	MEM_MB_ADD15	N28	MB_ADD(15)	MB_DATA(27)	F29	MEM_MB_DATA27
	MEM_MB_ADD14	N29	MB_ADD(14)	MB_DATA(26)	F31	MEM_MB_DATA26
	MEM_MB_ADD13	AE31	MB_ADD(13)	MB_DATA(25)	A29	MEM_MB_DATA25
	MEM_MB_ADD12	N30	MB_ADD(12)	MB_DATA(24)	A28	MEM_MB_DATA24
	MEM_MB_ADD11	P29	MB_ADD(11)	MB_DATA(23)	A25	MEM_MB_DATA23
	MEM_MB_ADD10	AA29	MB_ADD(10)	MB_DATA(22)	A24	MEM_MB_DATA22
	MEM_MB_ADD9	P31	MB_ADD(9)	MB_DATA(21)	C22	MEM_MB_DATA21
	MEM_MB_ADD8	R29	MB_ADD(8)	MB_DATA(20)	D21	MEM_MB_DATA20
	MEM_MB_ADD7	R28	MB_ADD(7)	MB_DATA(19)	A26	MEM_MB_DATA19
	MEM_MB_ADD6	R31	MB_ADD(6)	MB_DATA(18)	B25	MEM_MB_DATA18
	MEM_MB_ADD5	R30	MB_ADD(5)	MB_DATA(17)	B23	MEM_MB_DATA17
	MEM_MB_ADD4	T31	MB_ADD(4)	MB_DATA(16)	A22	MEM_MB_DATA16
	MEM_MB_ADD3	T29	MB_ADD(3)	MB_DATA(15)	B21	MEM_MB_DATA15
	MEM_MB_ADD2	U29	MB_ADD(2)	MB_DATA(14)	A20	MEM_MB_DATA14
	MEM_MB_ADD1	U28	MB_ADD(1)	MB_DATA(13)	C16	MEM_MB_DATA13
	MEM_MB_ADD0	AA30	MB_ADD(0)	MB_DATA(12)	D15	MEM_MB_DATA12
				MB_DATA(11)	C21	MEM_MB_DATA11
	MEM_MB_DQS_H7	AK13	MB_DQS_H(7)	MB_DATA(10)	A21	MEM_MB_DATA10
	MEM_MB_DQS_L7	AJ13	MB_DQS_L(7)	MB_DATA(9)	A17	MEM_MB_DATA9
	MEM_MB_DQS_H6	AK17	MB_DQS_H(6)	MB_DATA(8)	A16	MEM_MB_DATA8
	MEM_MB_DQS_L6	AJ17	MB_DQS_L(6)	MB_DATA(7)	B15	MEM_MB_DATA7
	MEM_MB_DQS_H5	AK23	MB_DQS_H(5)	MB_DATA(6)	A14	MEM_MB_DATA6
	MEM_MB_DQS_L5	AL23	MB_DQS_L(5)	MB_DATA(5)	E13	MEM_MB_DATA5
	MEM_MB_DQS_H4	AL28	MB_DQS_H(4)	MB_DATA(4)	F13	MEM_MB_DATA4
	MEM_MB_DQS_L4	AL29	MB_DQS_L(4)	MB_DATA(3)	C15	MEM_MB_DATA3
	MEM_MB_DQS_H3	D31	MB_DQS_H(3)	MB_DATA(2)	A15	MEM_MB_DATA2
	MEM_MB_DQS_L3	C31	MB_DQS_L(3)	MB_DATA(1)	A13	MEM_MB_DATA1
	MEM_MB_DQS_H2	C24	MB_DQS_H(2)	MB_DATA(0)	D13	MEM_MB_DATA0
	MEM_MB_DQS_L2	C23	MB_DQS_L(2)			
	MEM_MB_DQS_H1	D17	MB_DQS_H(1)	MB_DQS_H(8)	J31	
	MEM_MB_DQS_L1	C17	MB_DQS_L(1)	MB_DQS_L(8)	J30	
	MEM_MB_DQS_H0	C14	MB_DQS_H(0)			
	MEM_MB_DQS_L0	C13	MB_DQS_L(0)	MB_DM(8)	J29	
	MEM_MB_DM7	AJ14	MB_DM(7)	MB_CHECK(7)	K29	
	MEM_MB_DM6	AH17	MB_DM(6)	MB_CHECK(6)	K31	
	MEM_MB_DM5	AJ23	MB_DM(5)	MB_CHECK(5)	G30	
	MEM_MB_DM4	AK29	MB_DM(4)	MB_CHECK(4)	G29	
	MEM_MB_DM3	C30	MB_DM(3)	MB_CHECK(3)	L29	
	MEM_MB_DM2	A23	MB_DM(2)	MB_CHECK(2)	L28	
	MEM_MB_DM1	B17	MB_DM(1)	MB_CHECK(1)	H31	
	MEM_MB_DM0	B13	MB_DM(0)	MB_CHECK(0)	G31	

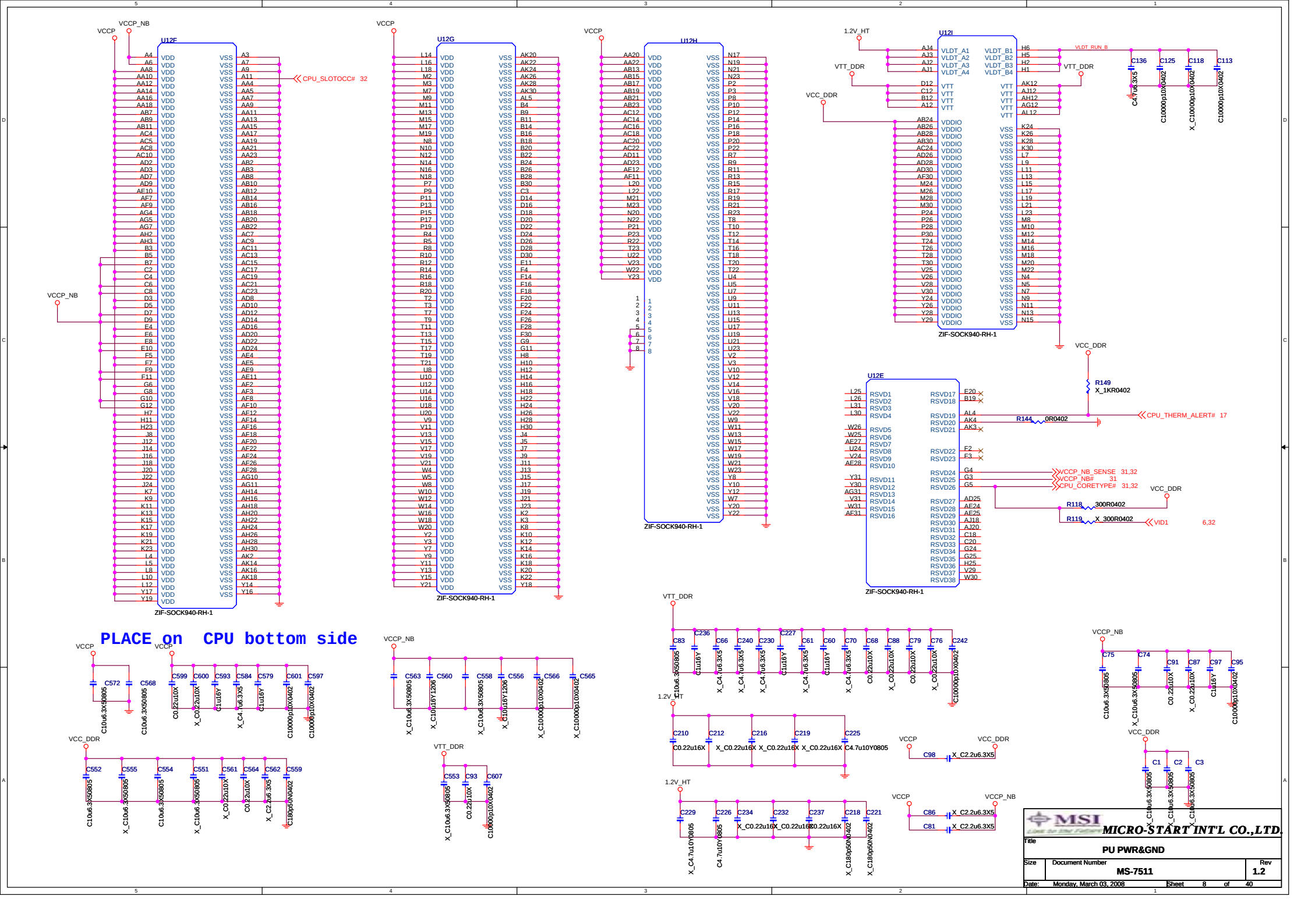
ZIF-SOCK940-RH-1

MICRO-START INT'L CO.,LTD.

Title: PU MEM I/F

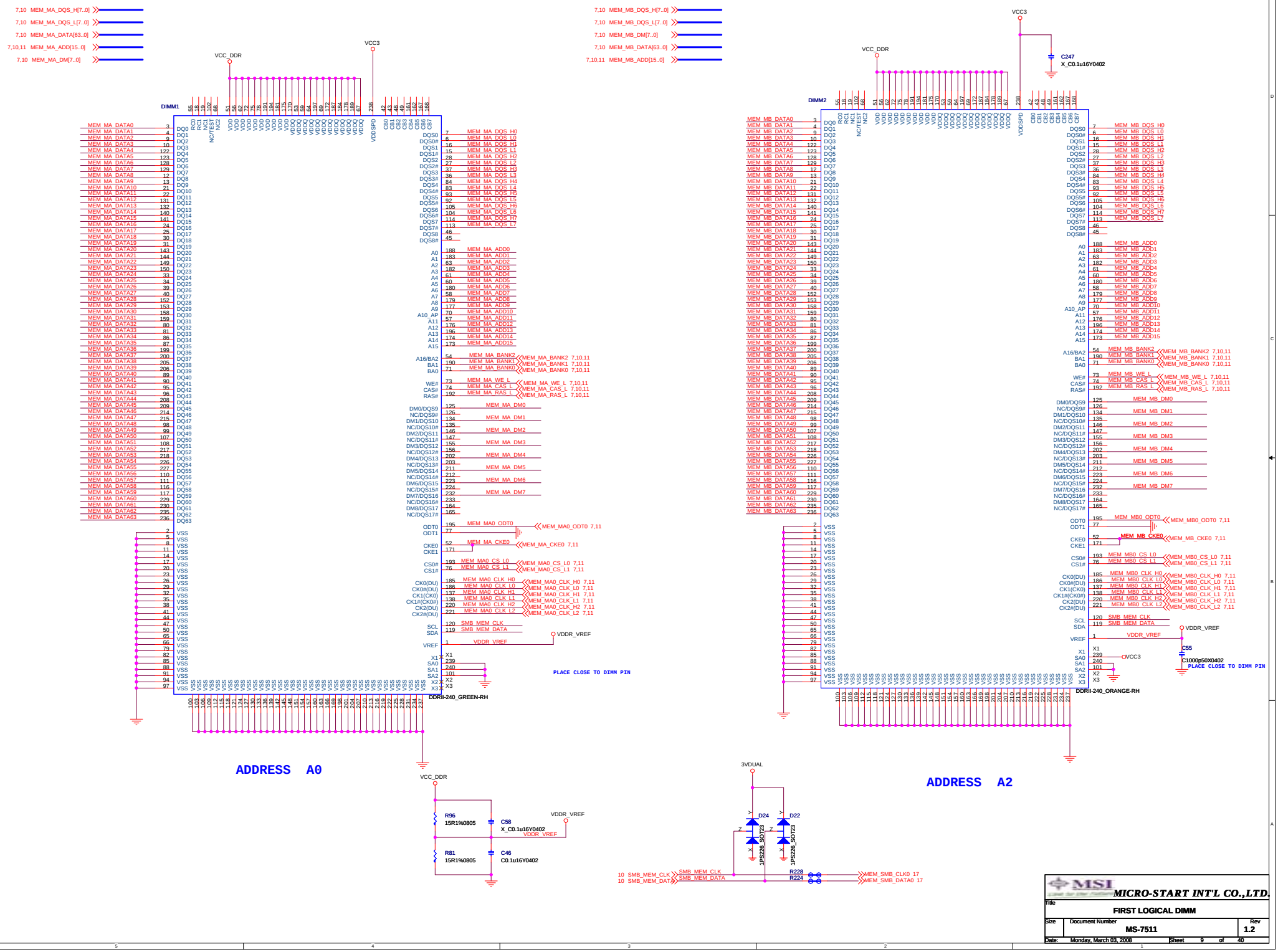
Size | Document Number: MS-7511 | Rev: 1.2

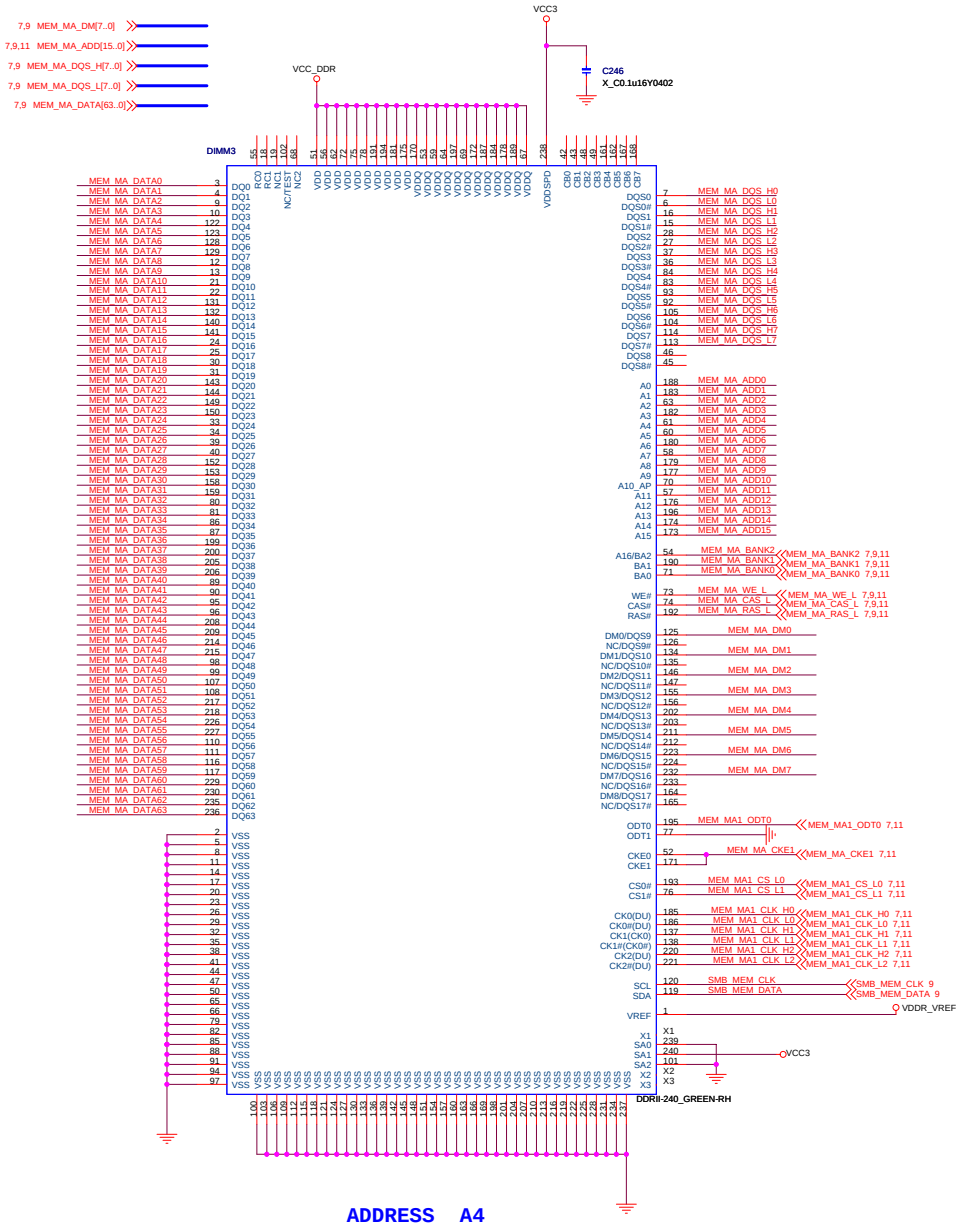
Date: Monday, March 03, 2008 | Sheet 7 of 40

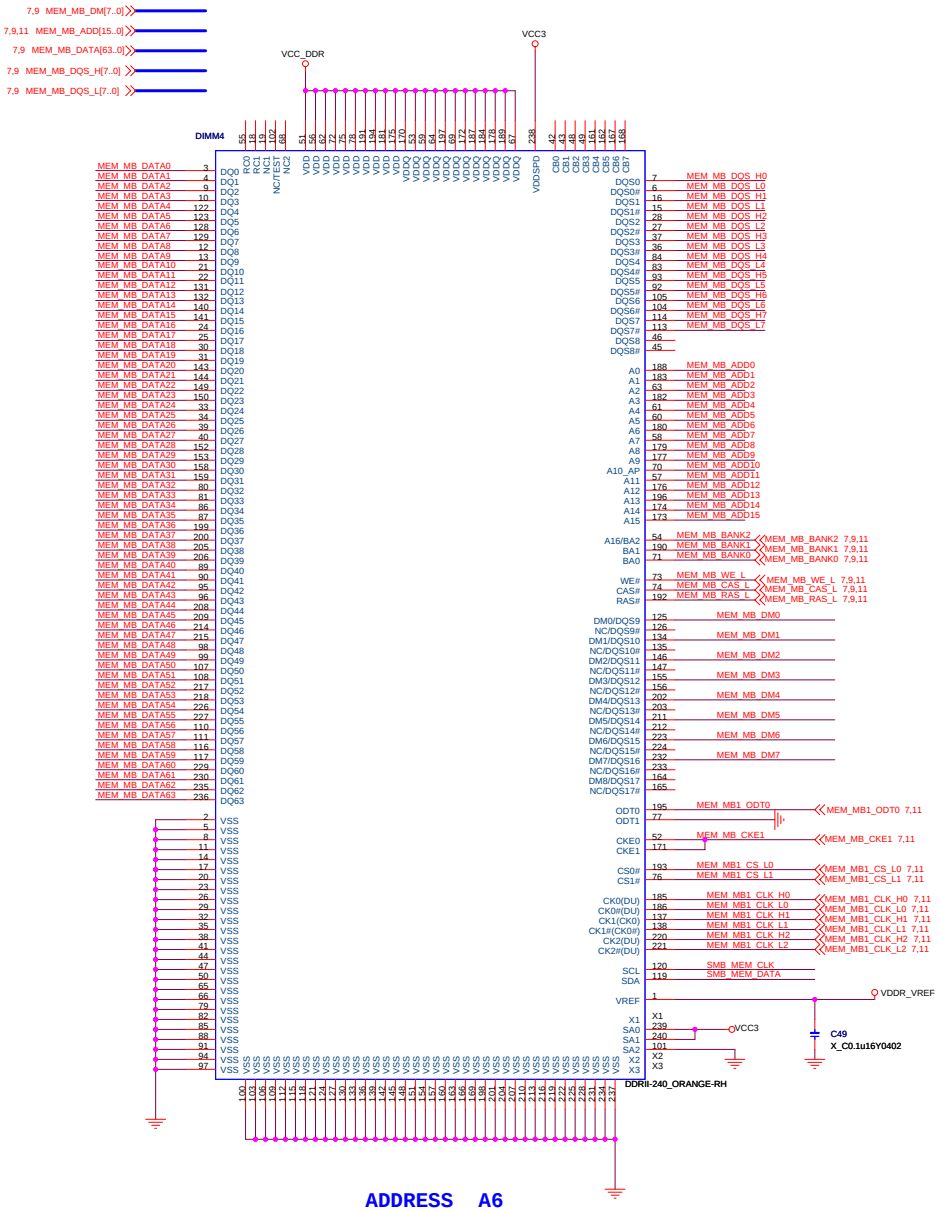


MICRO-START INT'L CO.,LTD.

Title	PU PWR&GND	
Size	Document Number: MS-7511	Rev: 1.2
Date: Monday, March 03, 2008	Sheet 8 of 40	

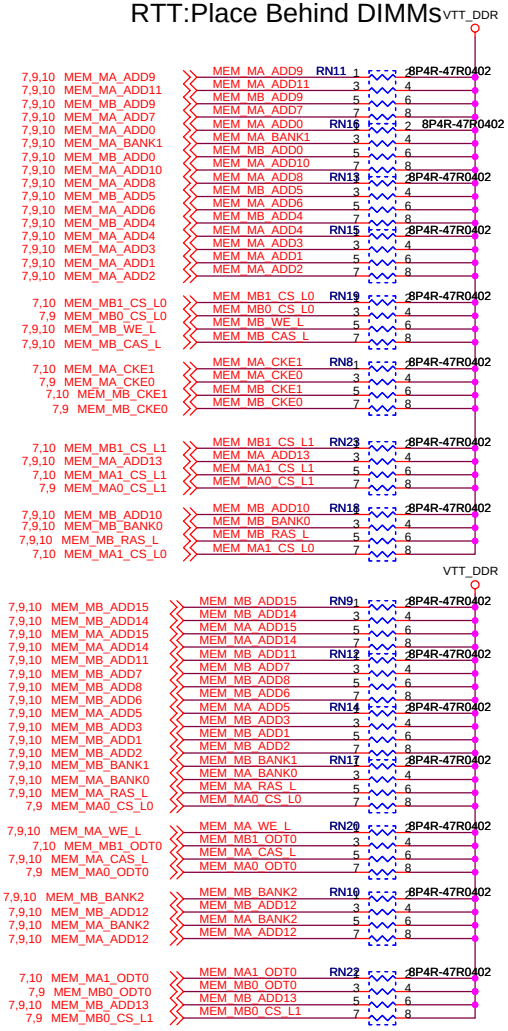

7,10 MEM_MA_DQS_H[7..0]
7,10 MEM_MA_DQS_L[7..0]
7,10 MEM_MA_DATA[63..0]
7,10,11 MEM_MA_ADD[15..0]
7,10 MEM_MA_DM[7..0]
7,10 MEM_MB_DQS_H[7..0]
7,10 MEM_MB_DQS_L[7..0]
7,10 MEM_MB_DM[7..0]
7,10 MEM_MB_DATA[63..0]
7,10,11 MEM_MB_ADD[15..0]
VCC_DDR
VCC3
DIMM1
DIMM2
DDRII-240_GREEN-RH
DDRII-240_ORANGE-RH
PLACE CLOSE TO DIMM PIN
ADDRESS A0
ADDRESS A2
C247
X_C0.1u16Y0402
C55
C1000p50X0402
R96
15R1%0805
C58
X_C0.1u16Y0402
R81
15R1%0805
C46
C0.1u16Y0402
3VDUAL
D24
D22
1PS226_SOT23
R228
R224
10 SMB_MEM_CLK
10 SMB_MEM_DAT
MEM_SMB_CLK0 17
MEM_SMB_DATA0 17
MICRO-START INT'L CO.,LTD.
FIRST LOGICAL DIMM
MS-7511
1.2
Monday, March 03, 2008
Sheet 9 of 40

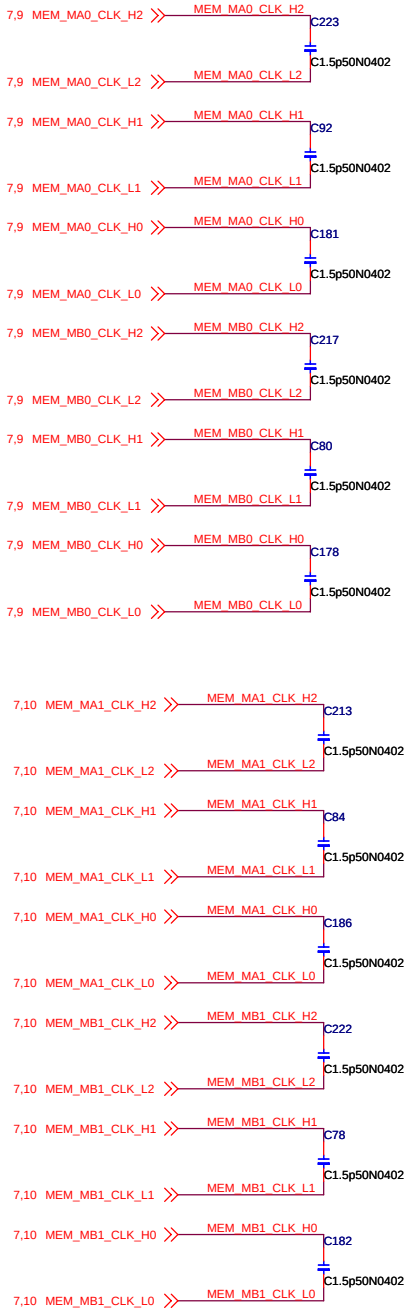




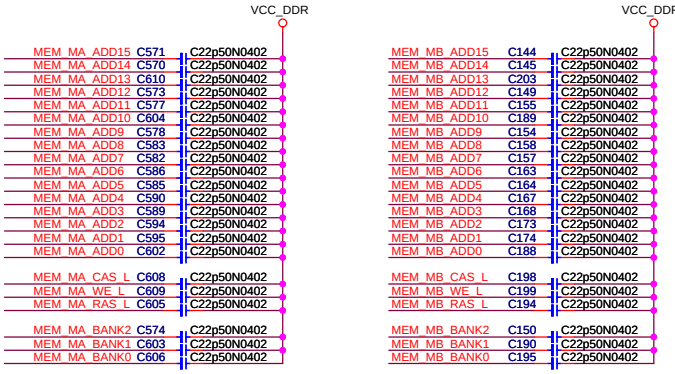
MSI	MICRO-START INT'L CO.,LTD.		
Title	SECOND LOGICAL DIMM		
Size	Document Number	MS-7511	Rev 1.2
Date:	Monday, March 03, 2008	Sheet 10 of 40	

RTT:Place Behind DIMMs

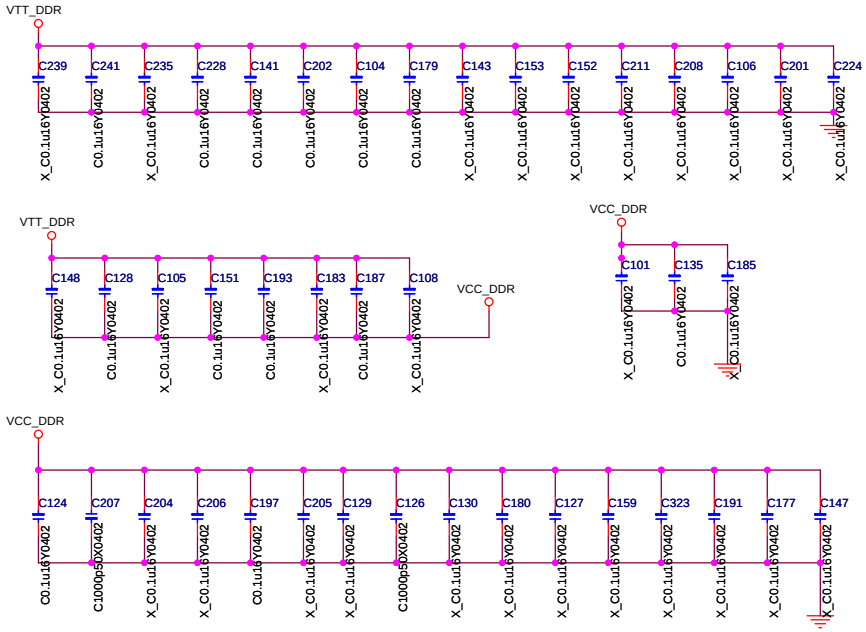




Place Between Processor and DIMMs



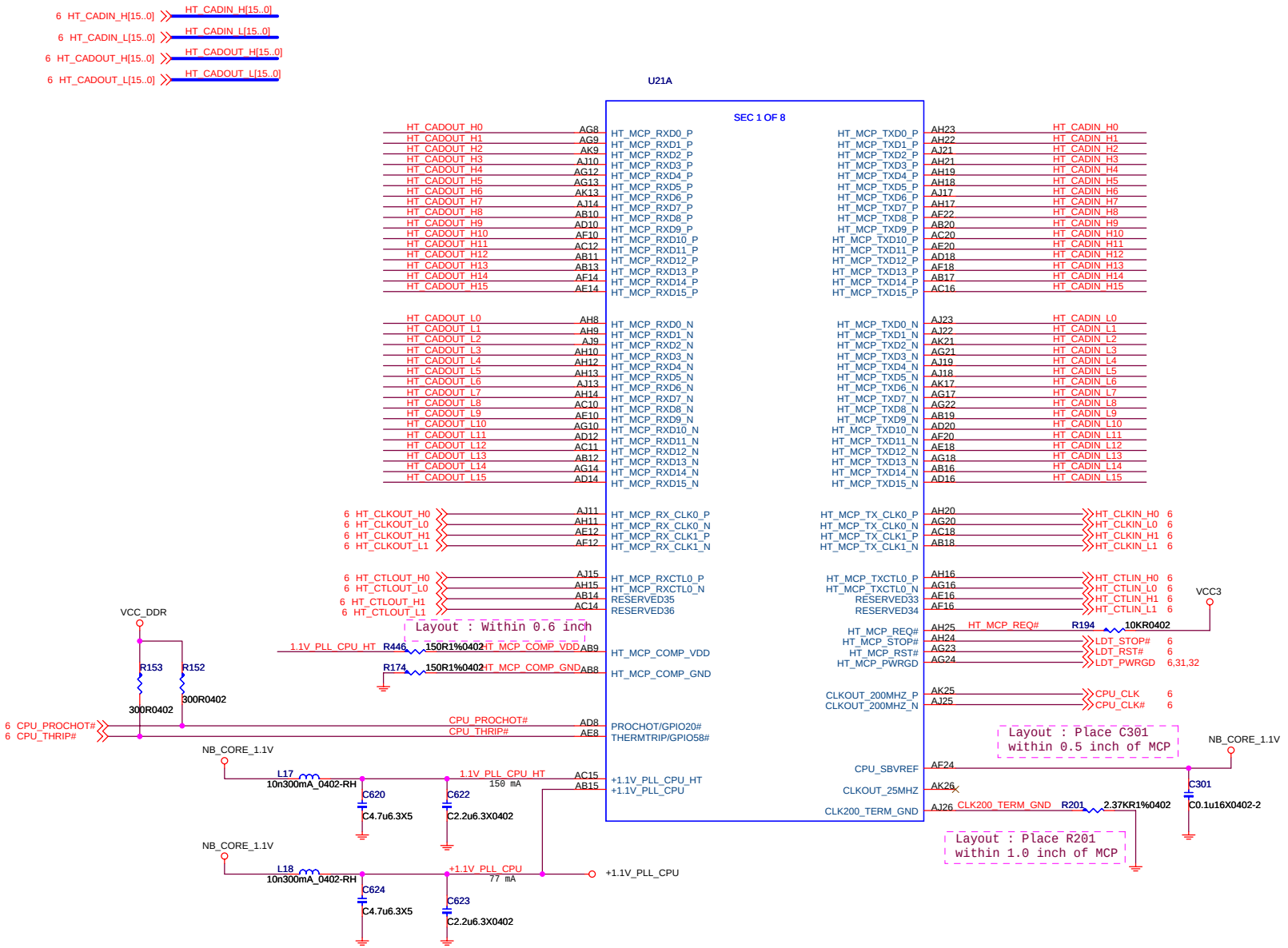
Layout: Spread out on VTT pour



for EMI

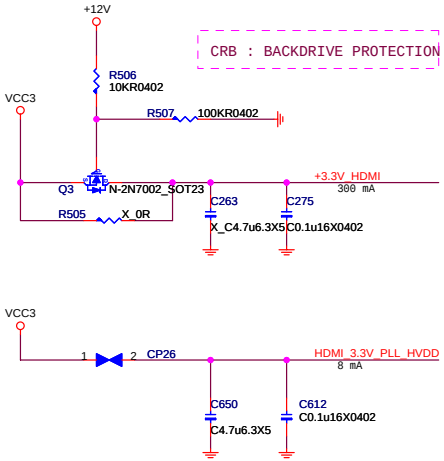
MICRO-START INT'L CO.,LTD.

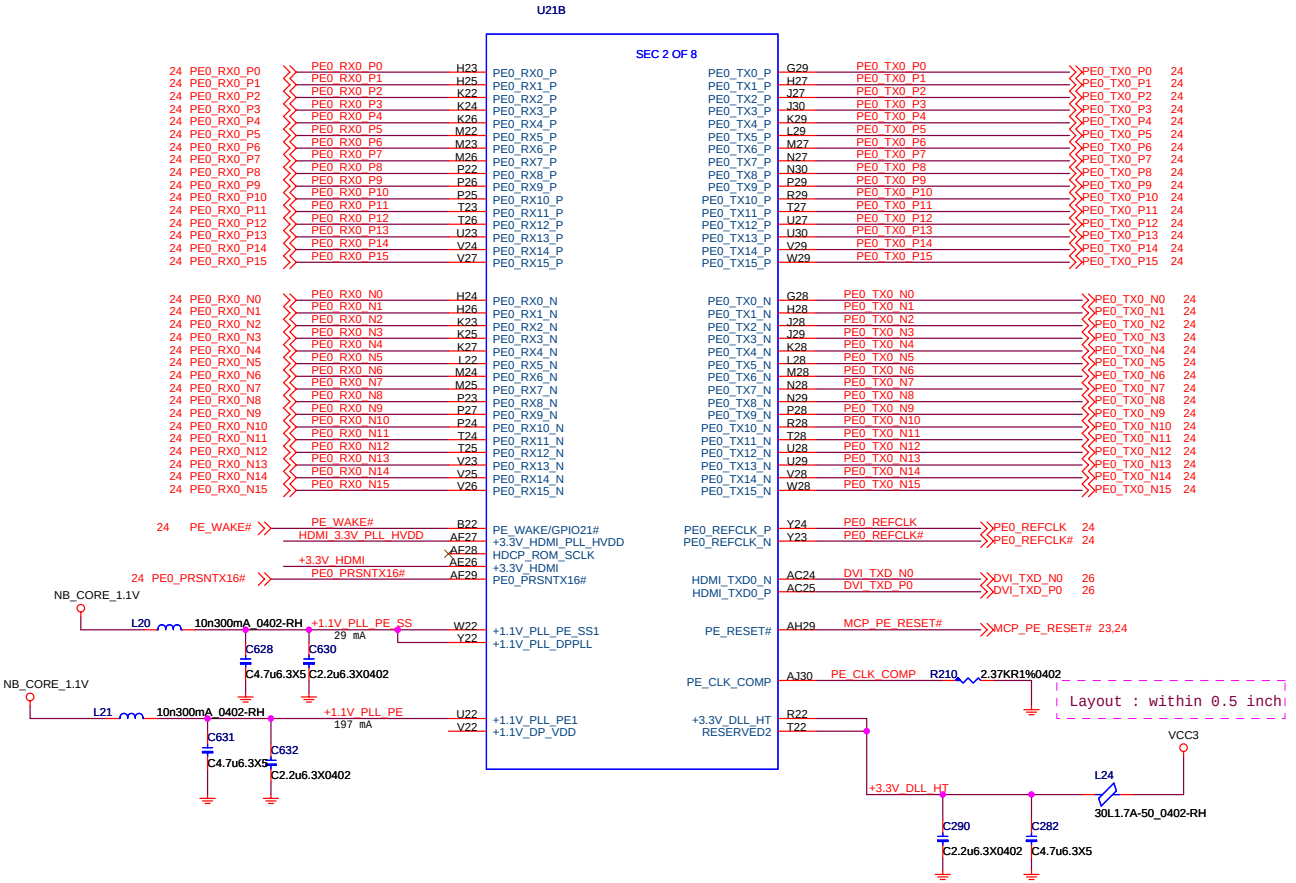
Title	DDR TERMINATOR	
Size	Document Number MS-7511	Rev 1.2
Date: Monday, March 03, 2008	Sheet 11 of 40	



MICRO-START INT'L CO.,LTD.

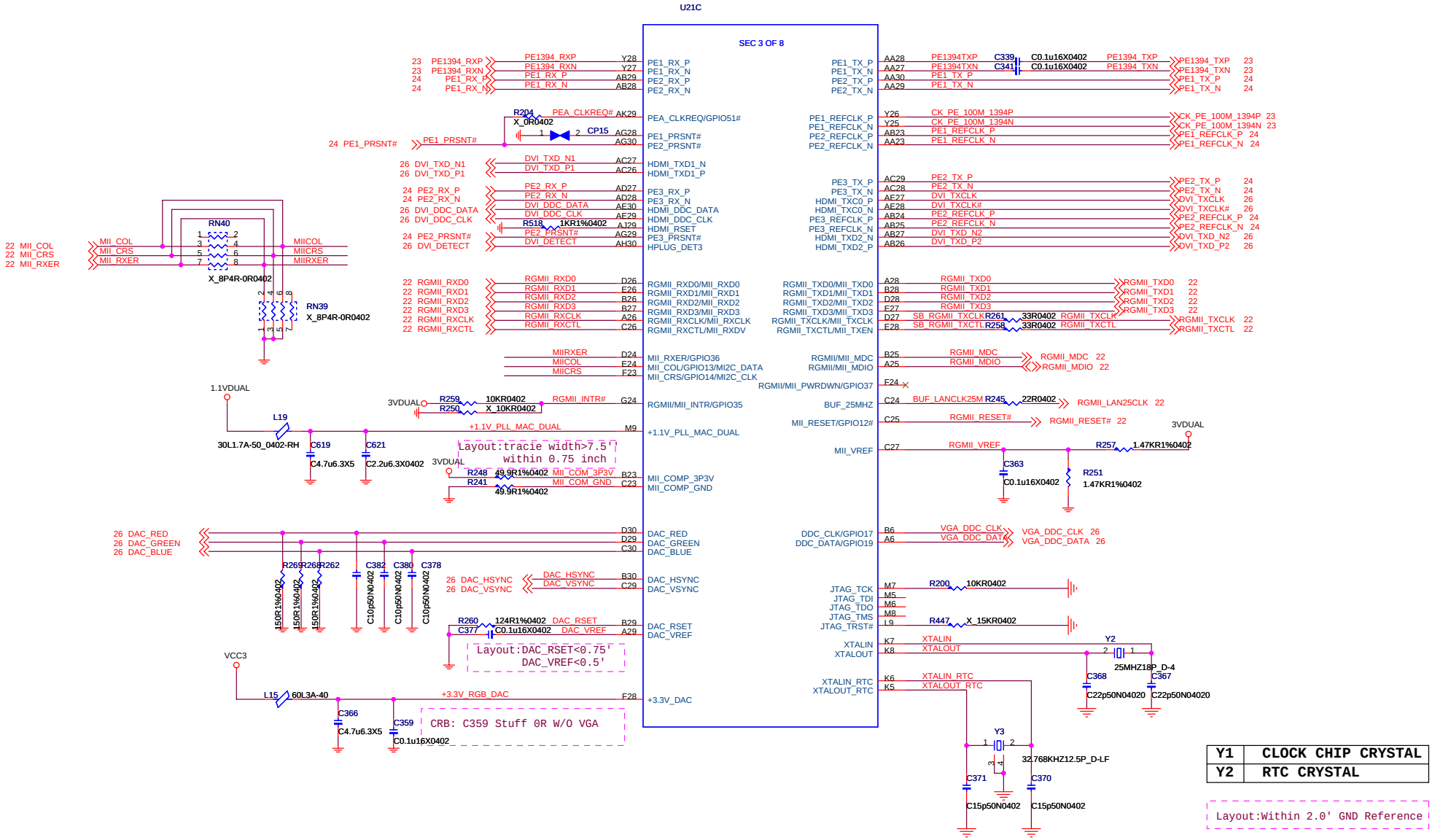
Title	MCP HT I/F	
Size	Document Number MS-7511	Rev 1.2
Date: Monday, March 03, 2008	Sheet 12 of 40	





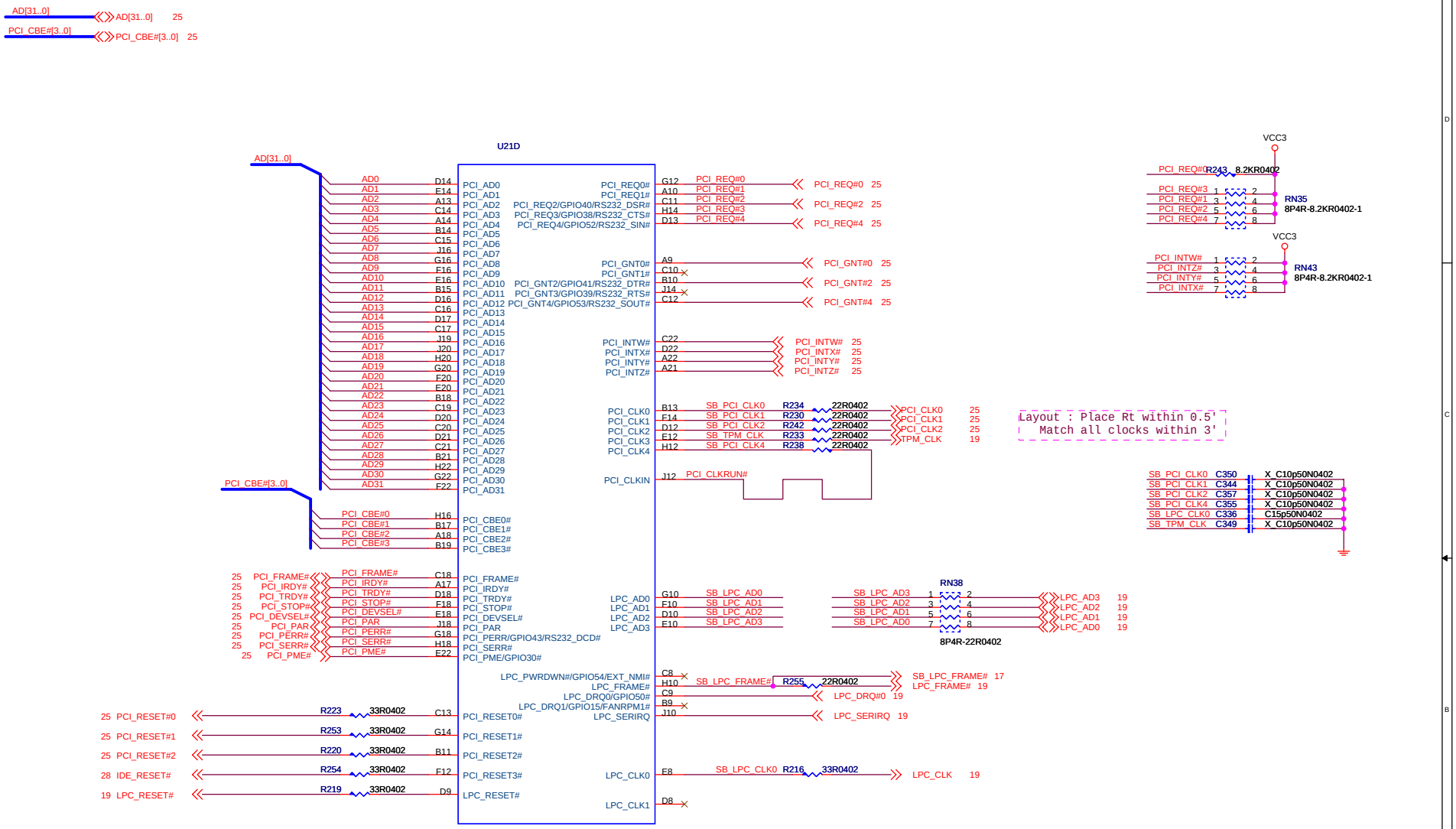
MICRO-START INT'L CO.,LTD.

Title	MCP PCIE I/F	
Size	Document Number: MS-7511	Rev: 1.2
Date: Monday, March 03, 2008	Sheet 13 of 40	

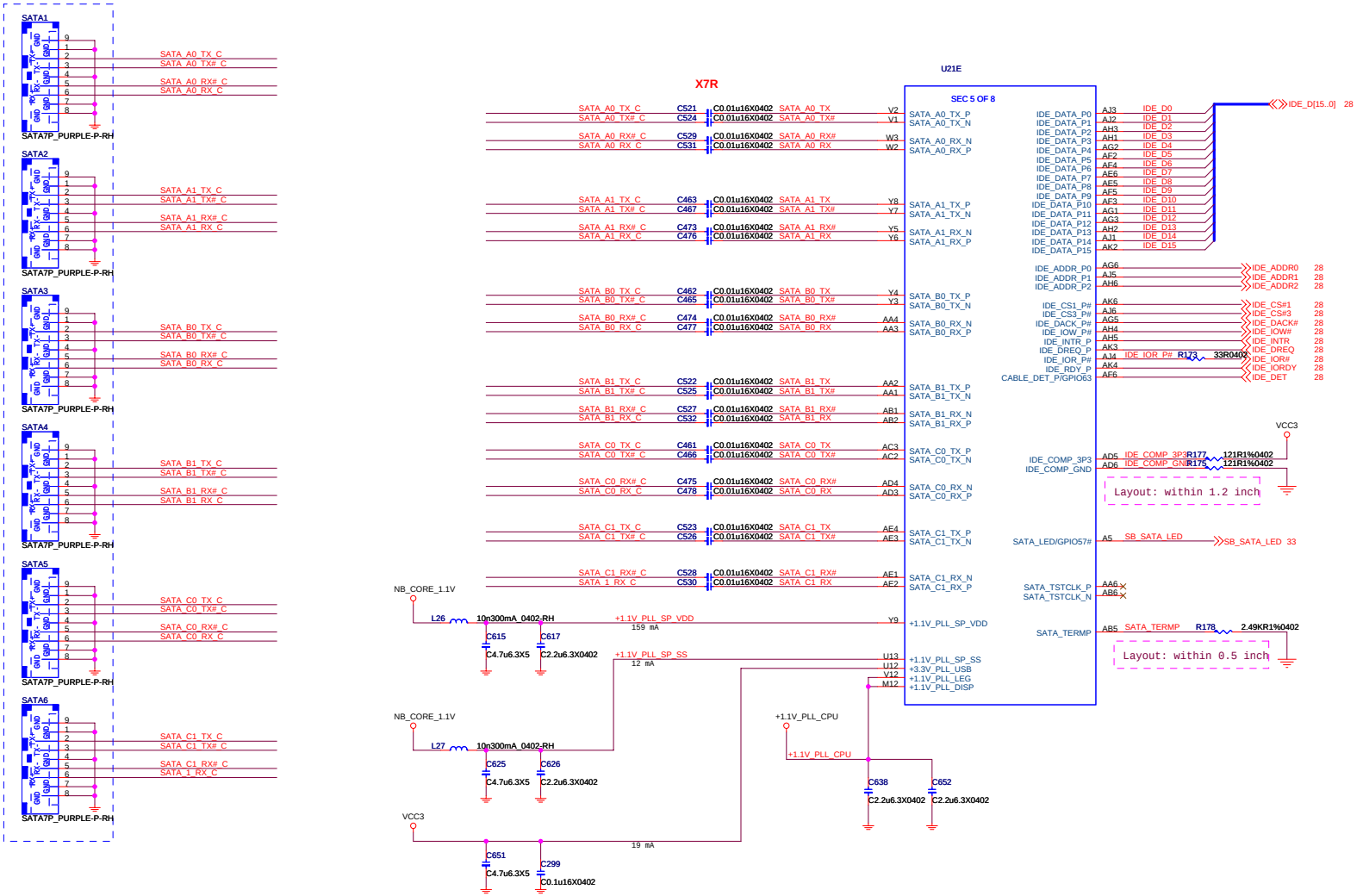


MSI MICRO-START INT'L CO.,LTD.

Title	MCP RGMII&DAC	
Size	Document Number MS-7511	Rev 1.2
Date: Monday, March 03, 2008	Sheet 14 of 40	



MICRO-START INT'L CO.,LTD.		
Title: MCP PCI&LPC		
Size	Document Number: MS-7511	Rev: 1.2
Date: Monday, March 03, 2008	Sheet 15 of 40	



MSI	MICRO-START INT'L CO.,LTD.	
Title	MCP SATA&IDE	
Size	Document Number MS-7511	Rev 1.2
Date: Monday, March 03, 2008	Sheet 16 of 40	

STRAPPING PIN

VCC3 — R227 X_10KR0402 — R222 1KR0402 — SPEAKER

SPEAK Boot Mode Select

1 = Safe Mode Boot Init table
0 = User Mode Boot Init table

VCC3 — R213 10KR0402 — SB_HDA_SYNC

HDA_SYNC SIO Clock Select

BIOS:Set Index 26h bit 7=1 SIO CLKIN=24MHz

1 = 24 MHz
0 = 14.31818 MHz

3VDUAL — R211 10KR0402 — SB_HDA_RESET#

HDA_RESET# Networking Select

1 = RGMII
0 = MII

3VDUAL — R407 10KR0402 — SPI_DO
3VDUAL — R406 X_10KR0402 — R400 10KR0402 — SPI_CLK

SPI Clock Freq. Select	SPI_DO/GPIO9	SPI_CLK/GPIO11
31 MHz	0	0
Reserved	0	1
25 MHz	1	0
1 MHz	1	1

VCC3 — R215 8.2KR0402 — HDA_SDATA_OUT0
15 SB_LPC_FRAME# — SB_LPC_FRAME# R256 8.2KR0402

BIOS Select	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS	1	0
Reserved (SPI)	1	1

RN33 8P4R-22R0402
21 HDA_BCLK — SB_HDA_BCLK
21 HDA_SDATA_OUT0 — SB_SDATA_OUT0
21 HDA_SYNC — SB_HDA_SYNC
21 HDA_RESET# — SB_HDA_RESET#

C335 C10p50N0402 — C332 X_C4.7p50N0402 — C327 X_C4.7p50N0402 — C330 X_C4.7p50N0402

U21F

SB_HDA_BCLK — B7 GP_REFCLK / B4 HDA_BCLK
SB_SDATA_OUT0 — A3 HDA_SDATA_OUT0/GPIO45
21 HDA_SDATA_IN0 — A2 HDA_SDATA_IN0/GPIO22 / B1 HDA_SDATA_IN1/GPIO23/MGPIO0 / B2 HDA_SDATA_1N2/GPIO24
SB_HDA_RESET# — C3 HDA_RESET#
SB_HDA_SYNC — B3 HDA_SYNC/GPIO44
24 PWR_SW_GPIO1 — F2 GPIO_1
24 RST_GATE_GPIO2 — F1 GPIO_2/NMI#
27 USB_EN — F6 GPIO_3/SMI# / J8 GPIO_4/SCI_INTR# / G3 GPIO_5/INIT# / G5 GPIO_6/FERR/SYS_SERR# / G6 GPIO_7/NFERR/SYS_PERR#
SPI_DI — D3 GPIO_8/SPI_DI
SPI_DO — D4 GPIO_9/SPI_DO
SPI_CS# — E4 GPIO_10/SPI_CS
SPI_CLK — E3 GPIO_11/SPI_CLK
D5 HDCP_SCL / E5 HDCP_SDA

USB0_P M3 — USBP0 — USBP0 27
USB0_N M4 — USBN0 — USBN0 27
USB1_P N3 — USBP1 — USBP1 27
USB1_N N4 — USBN1 — USBN1 27
USB2_P N1 — USBP2 — USBP2 27
USB2_N N2 — USBN2 — USBN2 27
USB3_P P1 — USBP3 — USBP3 27
USB3_N P2 — USBN3 — USBN3 27
USB4_P R2 — USBP4 — USBP4 27
USB4_N R3 — USBN4 — USBN4 27
USB5_P P3 — USBP5 — USBP5 27
USB5_N P4 — USBN5 — USBN5 27
USB6_P T3 — USBP6 — USBP6 27
USB6_N T4 — USBN6 — USBN6 27
USB7_P U3 — USBP7 — USBP7 27
USB7_N U4 — USBN7 — USBN7 27
USB8_P T6 — USBP8 — USBP8 27
USB8_N T5 — USBN8 — USBN8 27
USB9_P T8 — USBP9 — USBP9 27
USB9_N T7 — USBN9 — USBN9 27

USB_OC0/GPIO25# P7 — USB_OC0 — USB_OC0 27
USB_OC1/GPIO26# P8 — USB_OC1 — USB_OC1 27
USB_OC2/GPIO27# P9 — USB_OC2 — USB_OC2 27
USB_OC3/GPIO28/MGPIO1# P5 — USB_OC3 — USB_OC3 27
USB_OC4/GPIO29# P6 — USB_OC4 — USB_OC4 27

USB_RBIAS_GND T9 — USB_RBIAS_GND — R445 845R1%0402-RH

Layout : within 2.0 inch

RESERVED32 H9
THERM_SID1/GPIO47/PWR_LED# AE7 — R176 X_0R0402 — CPU_THERM_ALERT# 8
USB10_P V5 — USBP10
USB10_N V4 — USBN10
USB11_P V7 — USBP11
USB11_N V6 — USBN11

A20GATE/GPIO55 F5 — A20GATE — A20GATE 19
INTRUDER# K2 — INTRUDER#
EXT_SMI/GPIO32# F3 X
RI/GPIO33# H4 X
SPKR C7 — SPEAKER 33
PWRBTN# G4 — PWB_OUT# 19
SIO_PME/GPIO31# F4 — SIO_PME# 19
KBRDRSTIN/GPIO56# A4 — KBRST# 19

SMB_CLK0 C2 — SB_SMB_CLK0
SMB_DATA0 C1 — SB_SMB_DATA0
SMB_CLK1/MSMB_CLK D2 — SB_SMB_CLK1
SMB_DATA1/MSMB_DATA E2 — SB_SMB_DATA1
+3.3V_VBAT K3
BUF_SIO_CLK B5 — BUF_SIO_CLK
SUS_CLK/GPIO34 E1 — TP24
THERM/GPIO59# C6 — THERM# — THERM# 19
RSTBTN# H5 — FP_RESET# 19,33
SLP_S5# H8 — SLP_S5# 29,30
SLP_S3# G8 — SLP_S3# 19,29
PWRGD_SB H6 — RSMRST# — RSMRST# 22,29
PS_PWRGD G2 — PS_PWRGD 29
FANRPM0/GPIO60 E6
FANCTL0/GPIO61 D6
FANCTL1/GPIO62 C5
THERM_SIC/GPIO48 AH7
THERM_SID/GPIO49 AF8

VBAT — C645 C0.1u25Y0402 — R236 22R0402 — C351 C15p50N0402 — LPC_SIO24M 19

RTC_RST# K4 — RTC_RST#
MEM_VLD J3 — MEM_VLD
HT_EN J4 — MCPVDD/HT_VLD
VCORE_VLD J1 — MCPVDD/HT_EN
CPUVDD_EN J2 — CPU_VLD / CPUVDD_EN
PKG_TEST L8
TEST_MODE_EN F8

VCORE_VLD — C309 X_C0.1u16Y0402
1.2V_HT_VLD — C320 C0.1u16Y0402
MEM_VLD — C321 X_C0.1u16Y0402

29 MEM_VLD — MEM_VLD
29 1.2V_HT_VLD — 1.2V_HT_VLD
29,30 HT_EN — HT_EN
29 VCORE_VLD — VCORE_VLD
31 CPUVDD_EN — CPUVDD_EN

R229 1KR0402

USBP1 RN30 8P4R-15KR0402
USBN1 3 4
USBP0 5 6
USBN0 7 8
USBP3 RN29 8P4R-15KR0402
USBN3 3 4
USBP2 5 6
USBN2 7 8
USBP4 RN28 8P4R-15KR0402
USBN4 3 4
USBP5 5 6
USBN5 7 8
USBP7 RN25 8P4R-15KR0402
USBN7 3 4
USBP6 5 6
USBN6 7 8
USBP8 RN26 8P4R-15KR0402
USBN8 3 4
USBN9 5 6
USBP9 7 8
USBN10 RN27 8P4R-15KR0402
USBP10 3 4
USBN11 5 6
USBP11 7 8

3VDUAL
RN36 8P4R-10KR0402
USB_OC2 1 2
USB_OC1 3 4
USB_OC3 5 6
USB_OC0 7 8
USB_OC4 R226 10KR0402

3VDUAL VCC3
RN34 8P4R-2.7KR0402
SB_SMB_DATA1 — SM_DATA 23,24,25,29,32
SB_SMB_CLK1 — SM_CLK 23,24,25,29,32
SB_SMB_DATA0 — MEM_SMB_DATA0 9
SB_SMB_CLK0 — MEM_SMB_CLK0 9
RN32 8P4R-0R0402

SPI BIOS ROM & DEBUG PORT

3VDUAL — R362 10KR0402 — R367 X_10KR0402
SPI_CS# — SPI_DI
U31 W25X80VSSIG-RH: CS / DO / WP / GND / VCC / HOLD / CLK / DIO
SPI_HOLD# — SPI_CLK — SPI_DO
19 SPI_WP# — R359 X_0R0402
C306 X_C10u6.3X5R0805 — C557 X_C0.1u25Y0402
R399 10KR0402
JSPI1 H2X5(1)M-2PITCH_BLACK-RH

VBAT

3VDUAL — R354 X_1KR0402 — Q43 X_P-SI2305DS-T1-E3_SOT23-LF (S, D, BAT3)
R353 X_4.7KR0402
D28 S-BAT54C_SOT23 (X, Y, Z)
S_BAT1 — BAT2P_BLACK-RH-1 — R355 1KR0402 — R357 0R
EC64 X_CD100u16SCI-RH — C442 C4.7u10Y0805 — C443 X_C0.1u25Y0402 — C447 X_C0.1u25Y0402
20mil
VBAT — R356 49.9KR1%0402
C448 X_C1U10Y0402-RH — C445 X_C0.1u16Y0402
RTC_RST# — JVBAT1 N31-1030151+N33-1020271-RH

Normal --> 1-2
Clear CMOS -->2-3

Chassis instruction

VBAT — R346 49.9KR1%0402 — INTRUDER# — JCI1 H1X2M_BLACK-RH

MSI MICRO-START INT'L CO.,LTD.

Title		
MCP AUDIO&USB&MISC		
Size	Document Number	Rev
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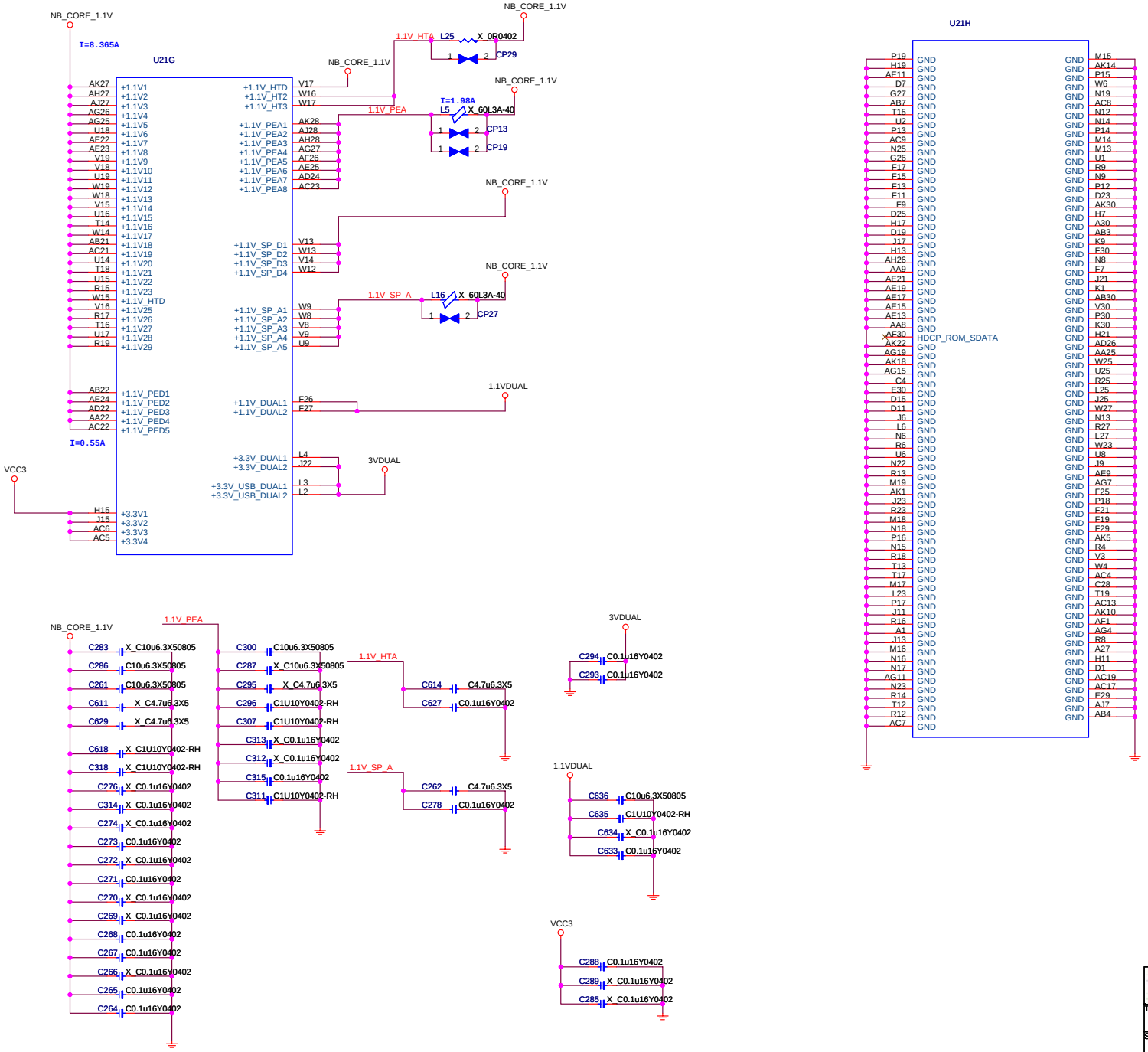

MICRO-START INT'L CO.,LTD.

Title: MCP PWR&GND

Size | Document Number: MS-7511 | Rev: 1.2

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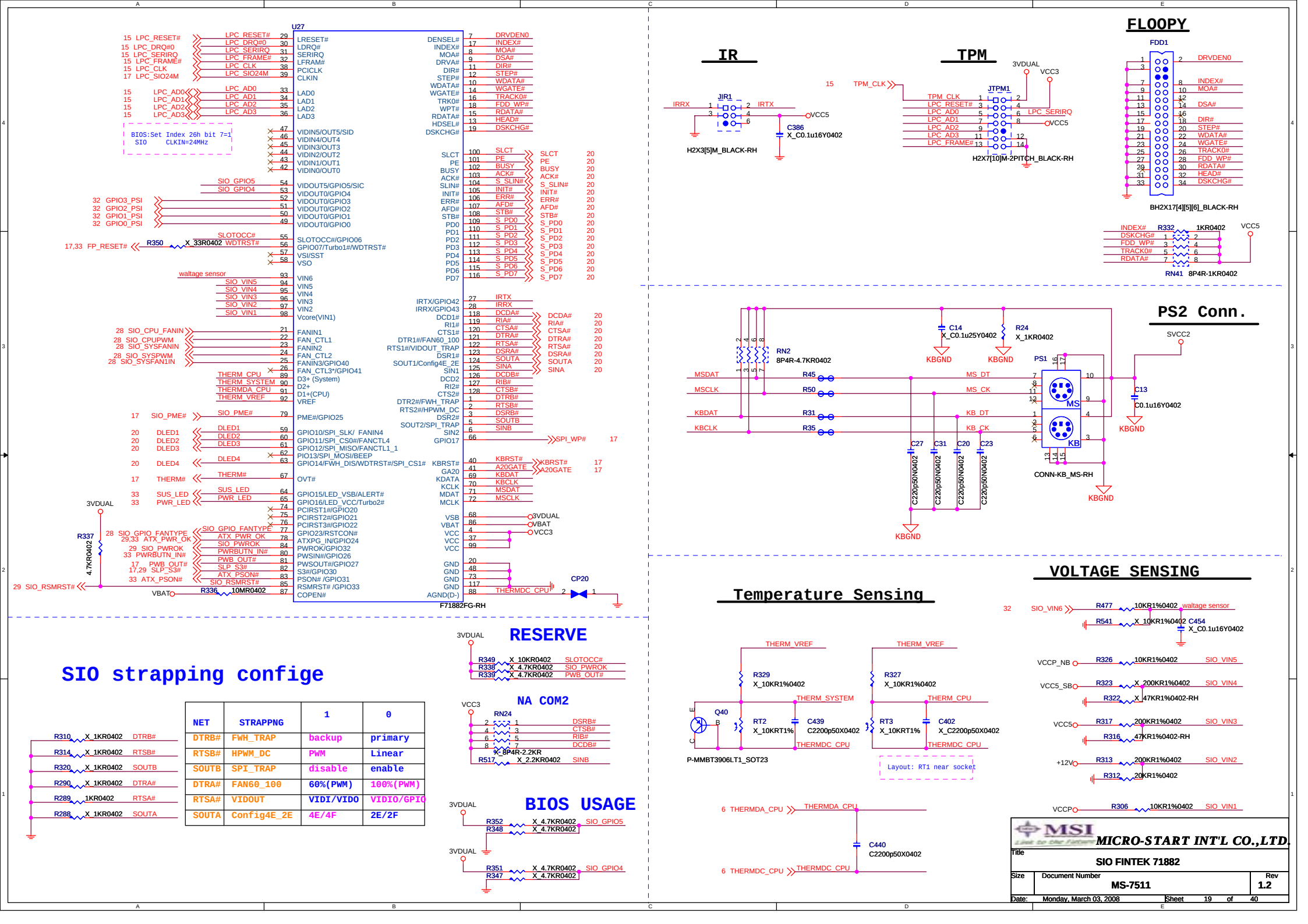
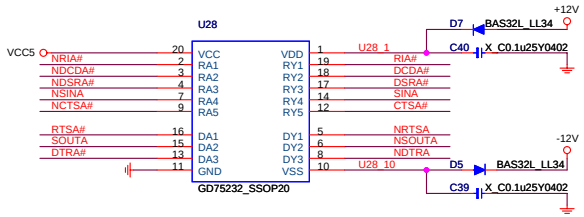
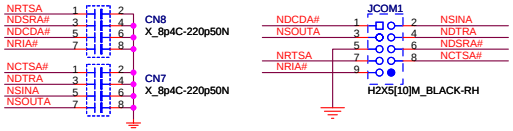


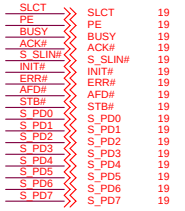
SIO strapping confige

NET	STRAPPNG	1	0
DTRB#	FWH_TRAP	backup	primary
RTSB#	HPWM_DC	PWM	Linear
SOUTB	SPI_TRAP	disable	enable
DTRA#	FAN60_100	60%(PWM)	100%(PWM)
RTSA#	VIDOUT	VIDI/VIDO	VIDIO/GPIO
SOUTA	Config4E_2E	4E/4F	2E/2F

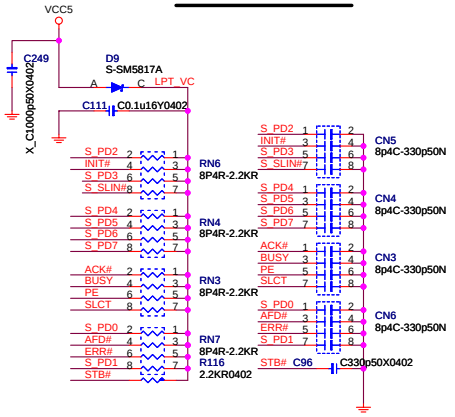
SERIAL PORT 1

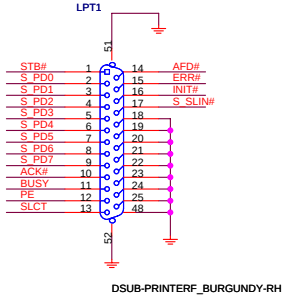






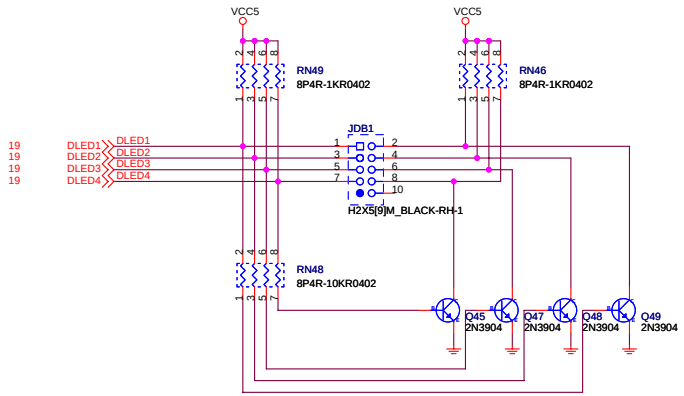
PARALLAL PORT





N51-25F0221-F02

DEBUG LED



MICRO-START INT'L CO.,LTD.

Title	SERIAL/PARALLEL PORT/DLED	
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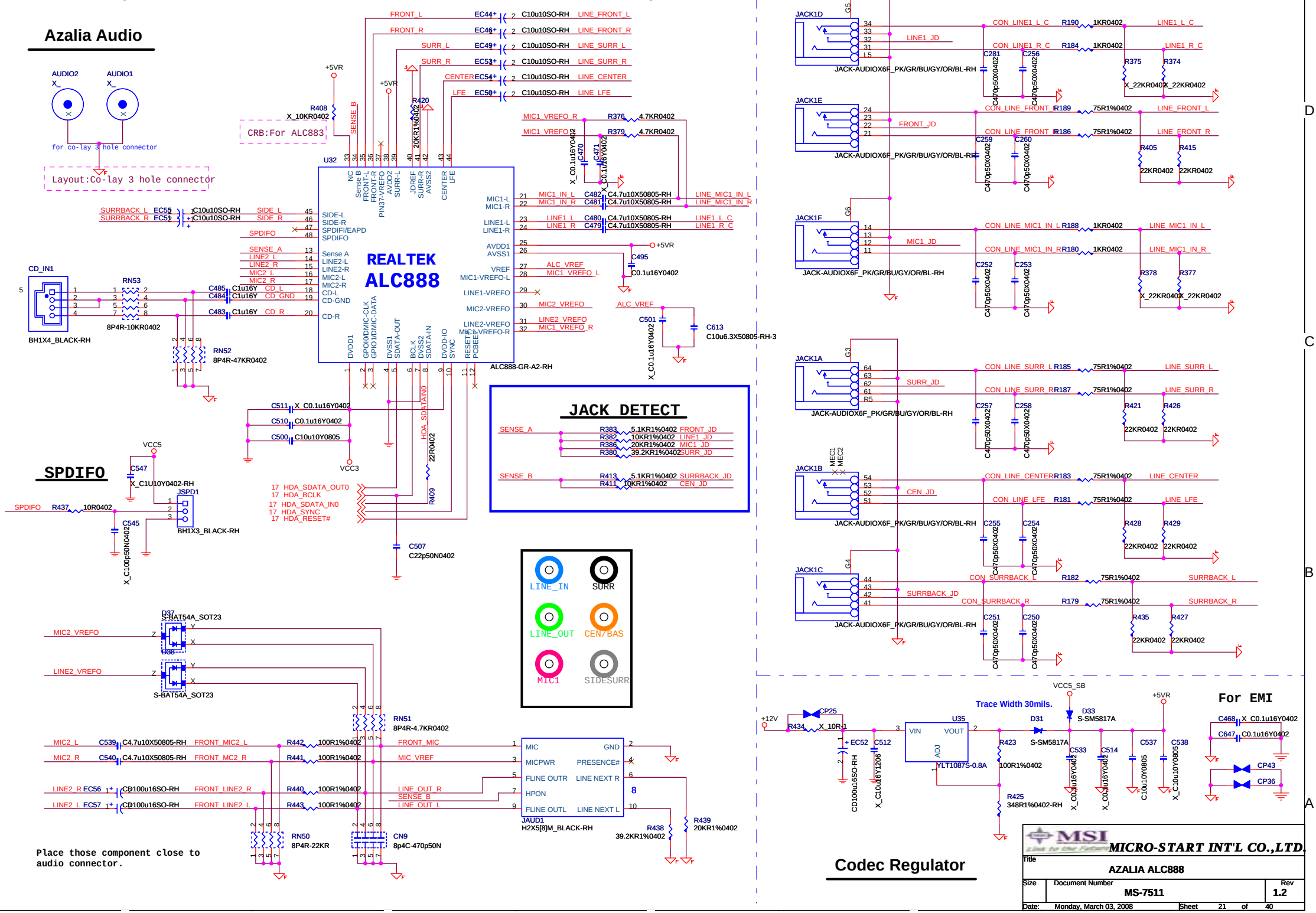
Azalia Audio



Title	AZALIA ALC888
Size	
Document Number	MS-7511
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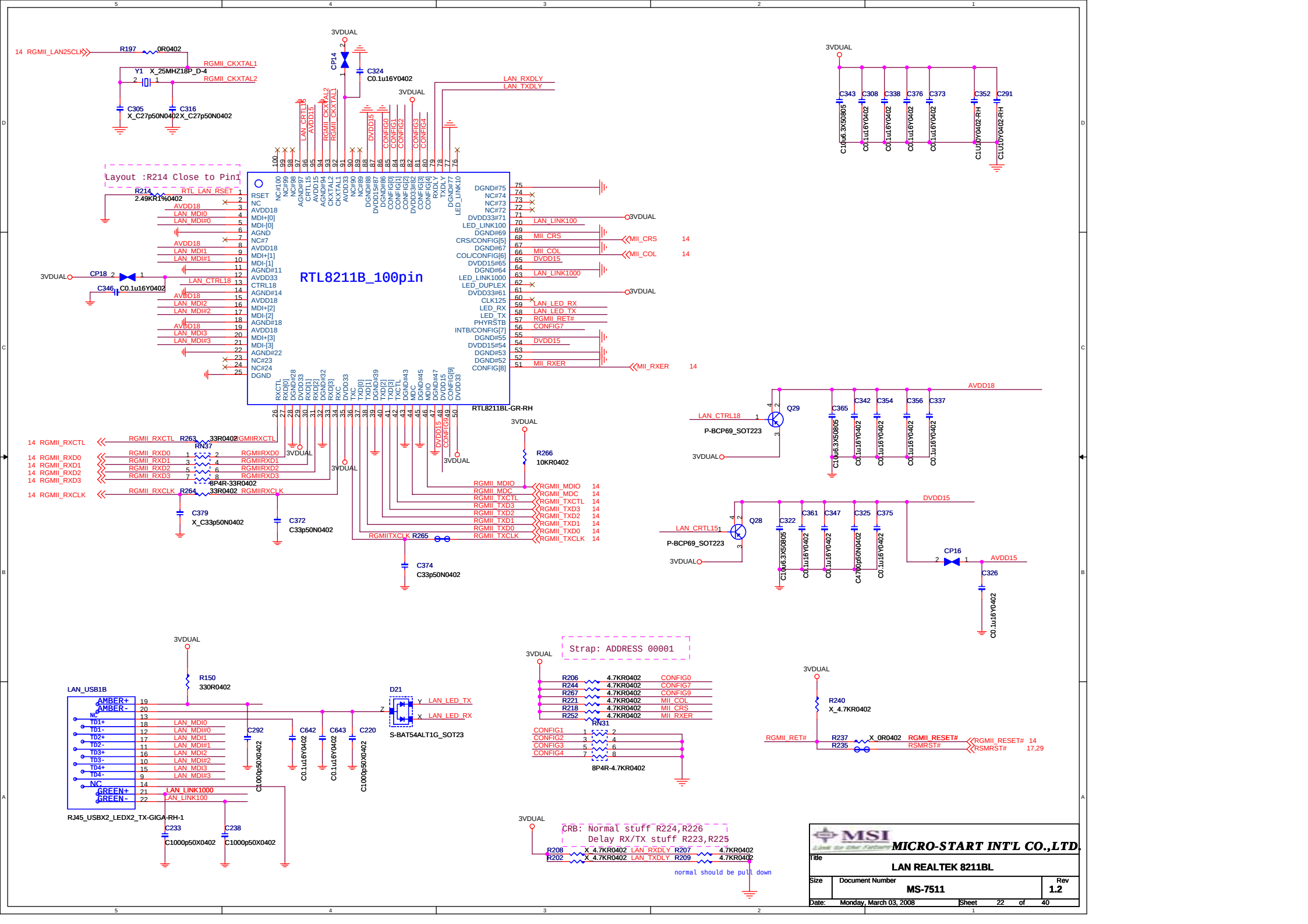
MSI MICRO-START INT'L CO.,LTD.


RTL8211B_100pin
RTL8211BL-GR-RH
Layout :R214 Close to Pin1
Strap: ADDRESS 00001
CRB: Normal stuff R224,R226
Delay RX/TX stuff R223,R225
normal should be pull down
LAN_USB1B
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
S-BAT54ALT1G_SOT23
P-BCP69_SOT223
8P4R-33R0402
8P4R-4.7KR0402
MICRO-START INT'L CO.,LTD.
LAN REALTEK 8211BL
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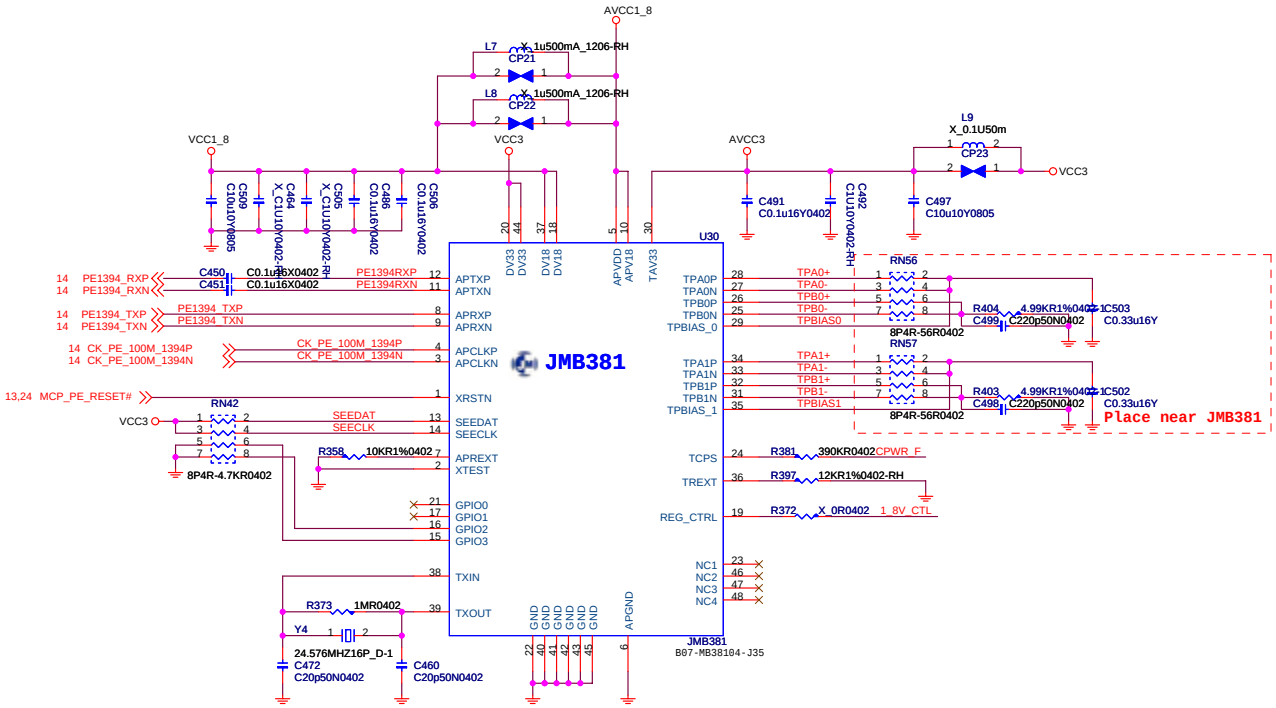
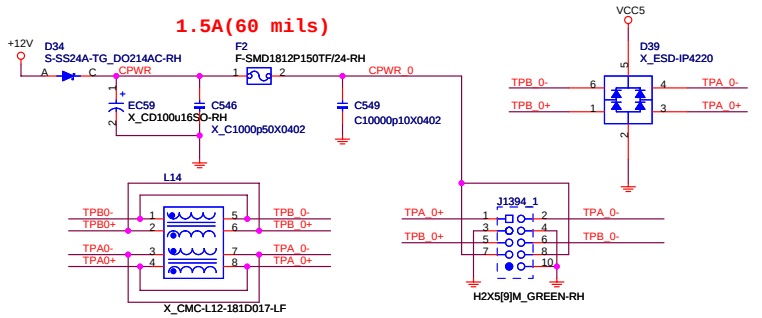
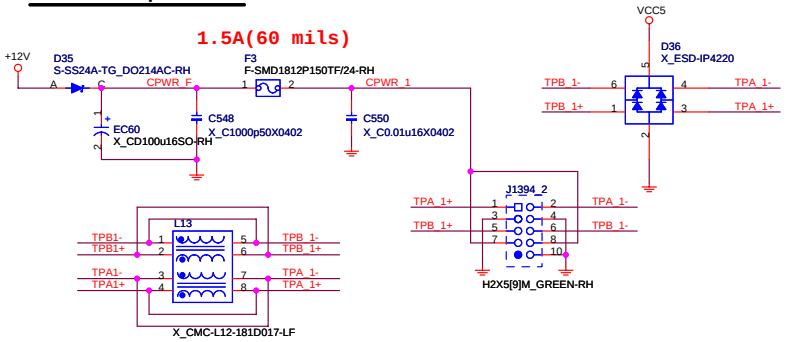
JMICRON JMB381

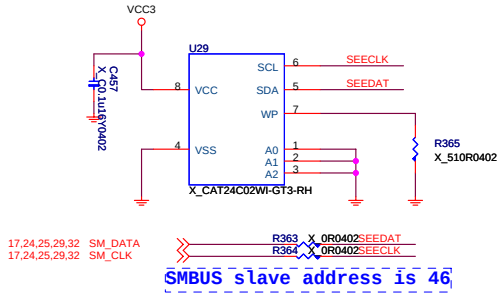


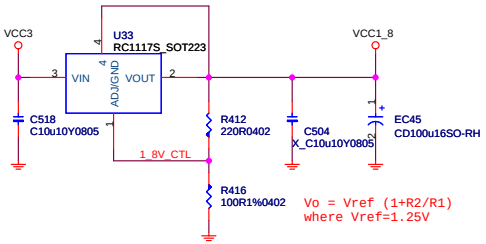
Rear 1394 port

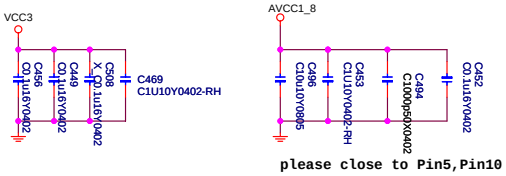


Front 1394 pin header









MSI MICRO-START INT'L CO.,LTD.

Title	1394 JIMICRON 381	
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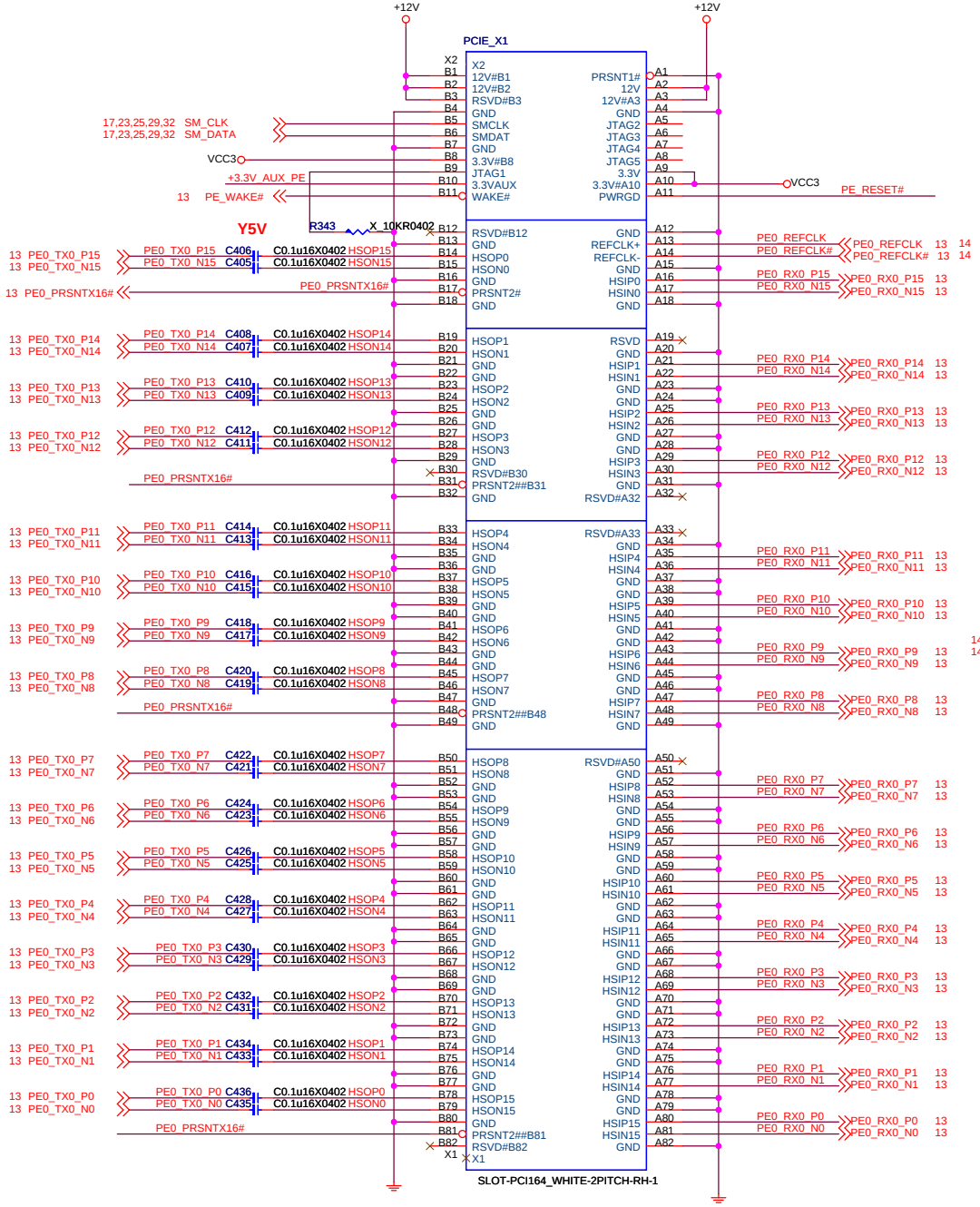

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	PCIE 16X &1X	
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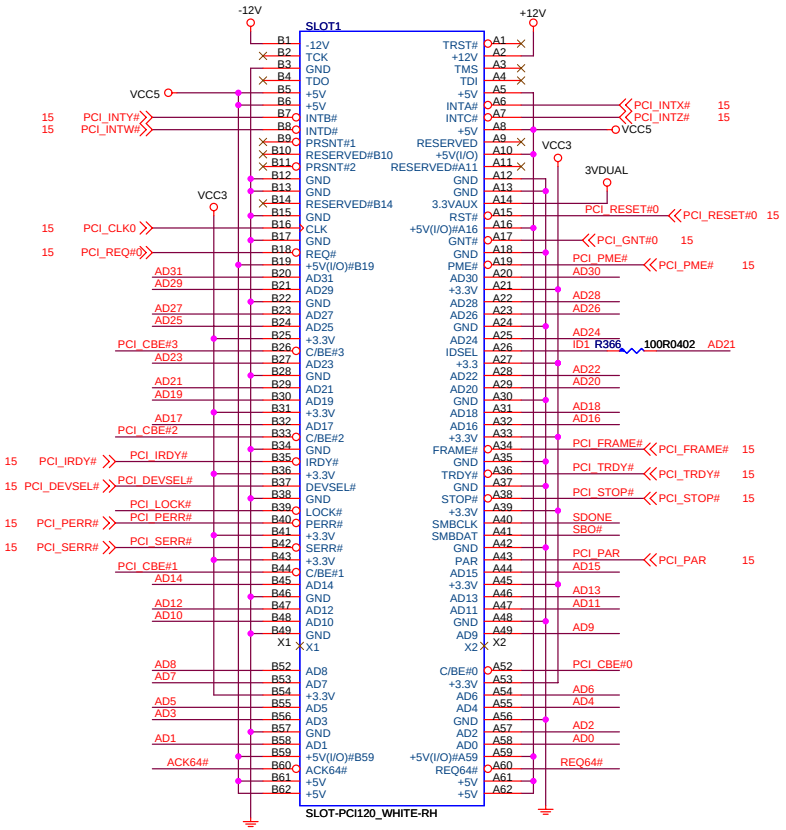
15 AD[31..0] AD[31..0]

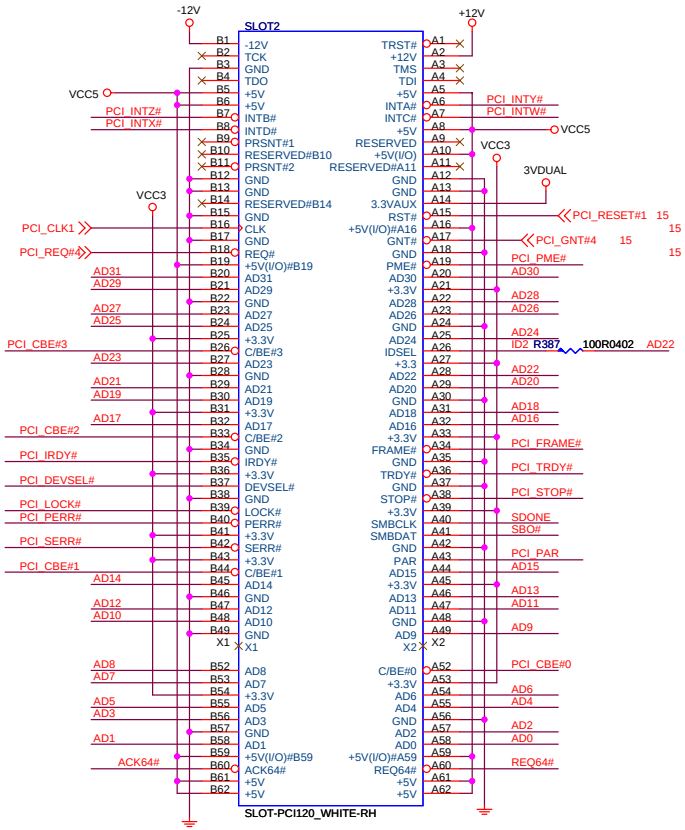
15 PCI_CBE#[3..0] PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.3 COMPLY)



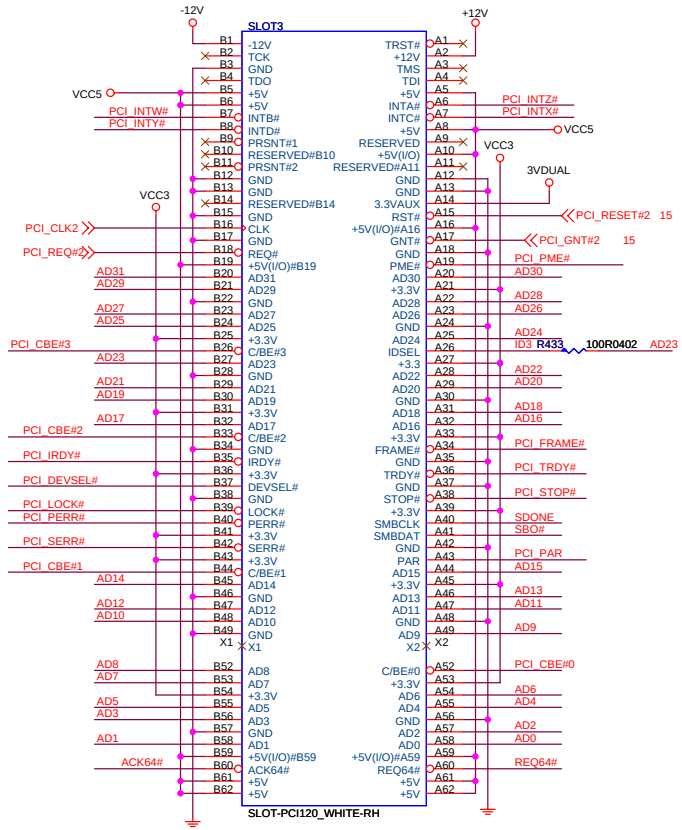
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0
PCI_INTX#

PCI SLOT 2 (PCI VER: 2.3 COMPLY)



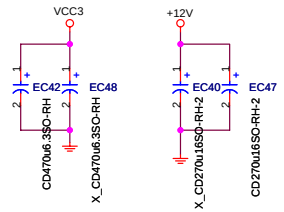
IDSEL = AD22
MASTER = PCI_REQ#1
PCI_GNT#1
PCI_INTY#

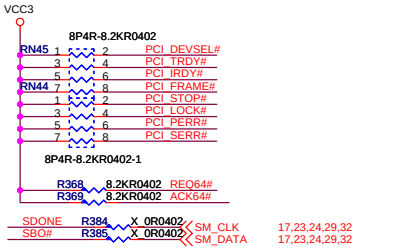
PCI SLOT 2 (PCI VER: 2.3 COMPLY)



IDSEL = AD23
MASTER = PCI_REQ#2
PCI_GNT#2
PCI_INTZ#

PCI PULL-UP / DOWN RESISTORS





MICRO-START INT'L CO.,LTD.

Title	PCI SLOT	
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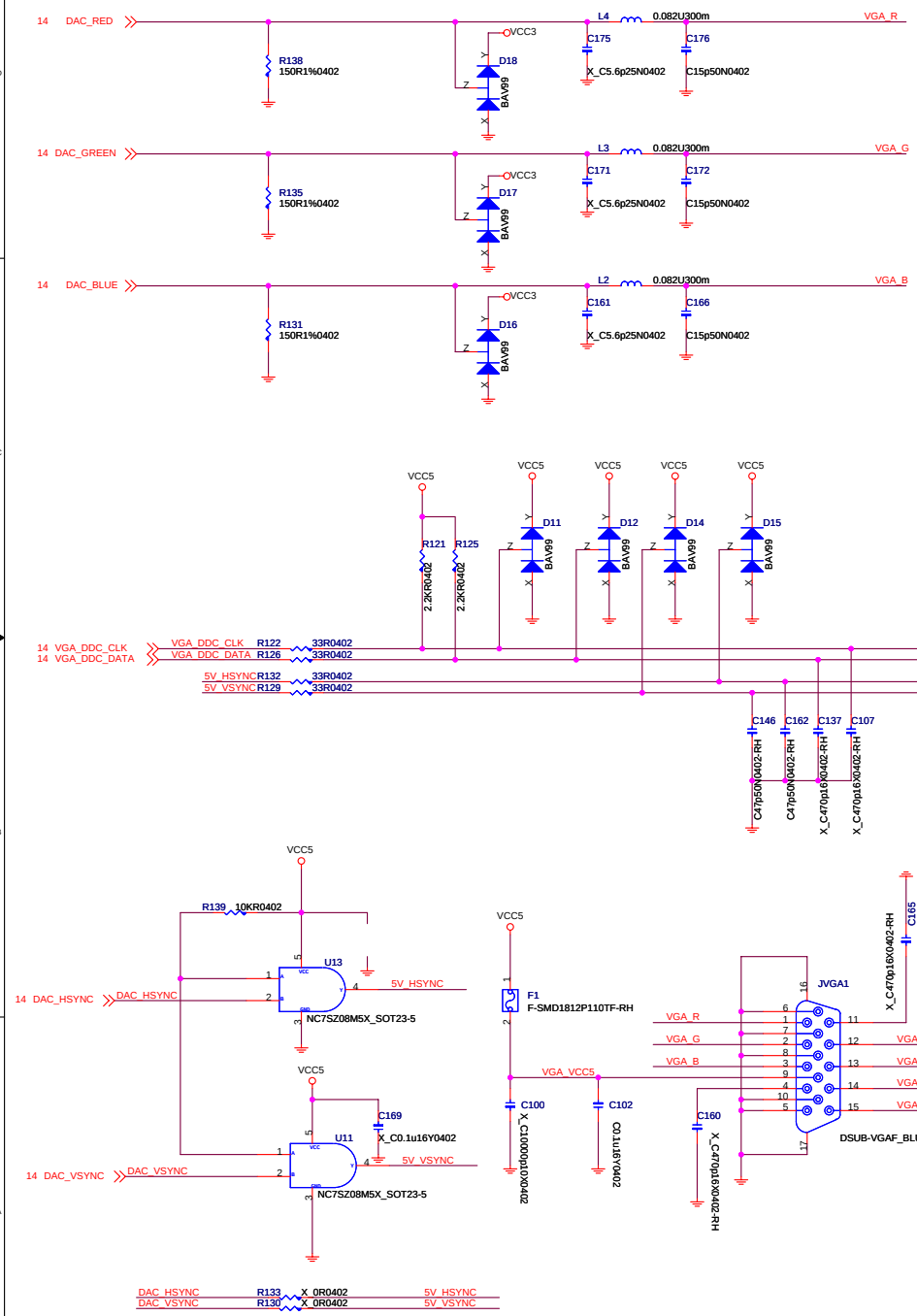
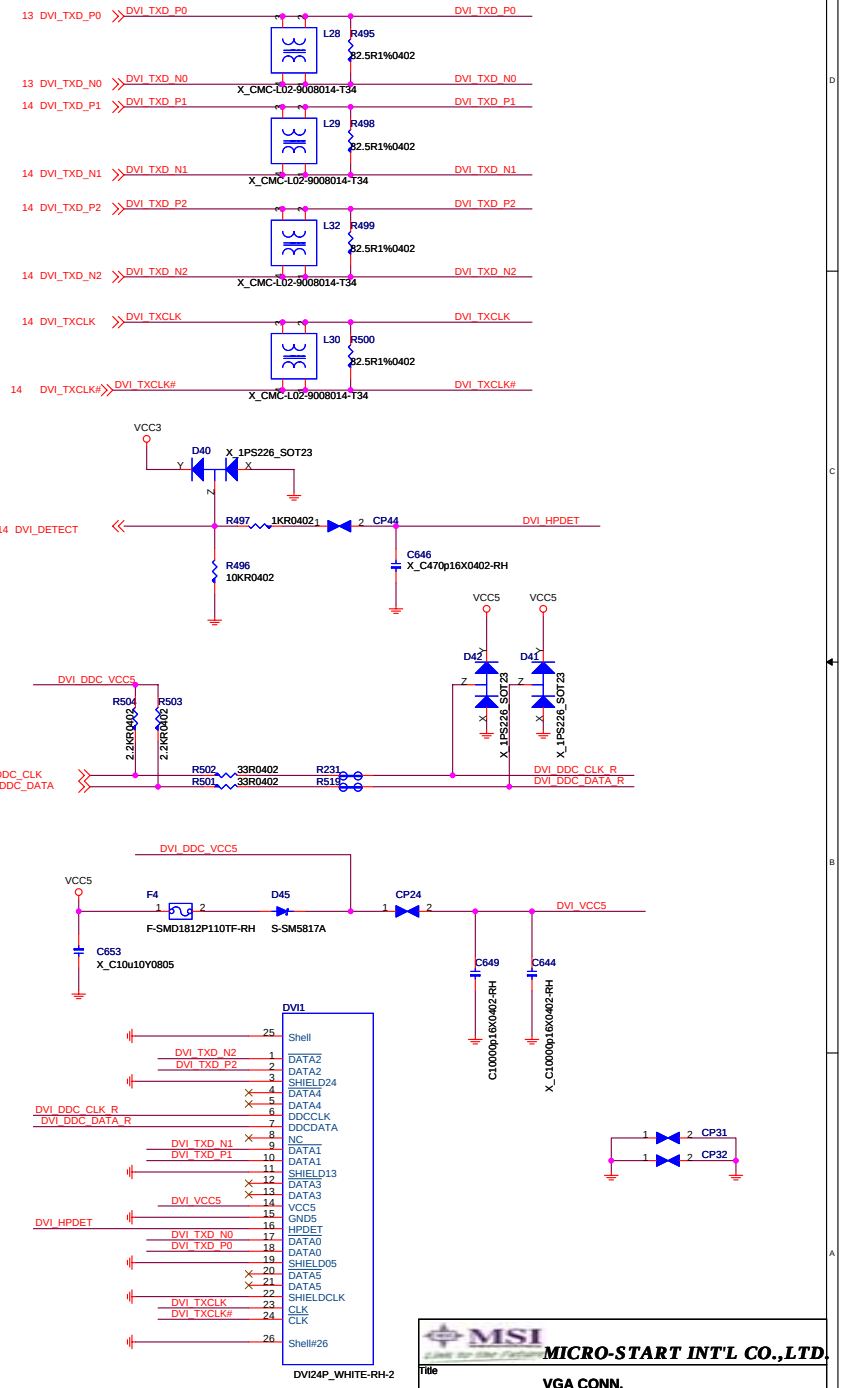
VGA CONNECTOR

close VGA connector For EMI



DVI CONNECTOR

for EMI place near connector



MICRO-START INT'L CO.,LTD.			
Title: VGA CONN.			
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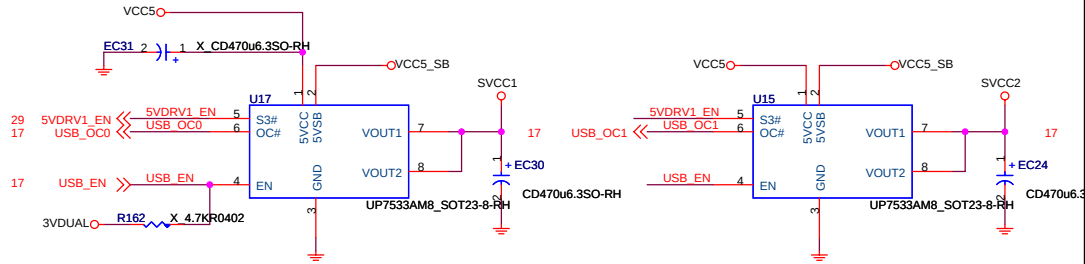
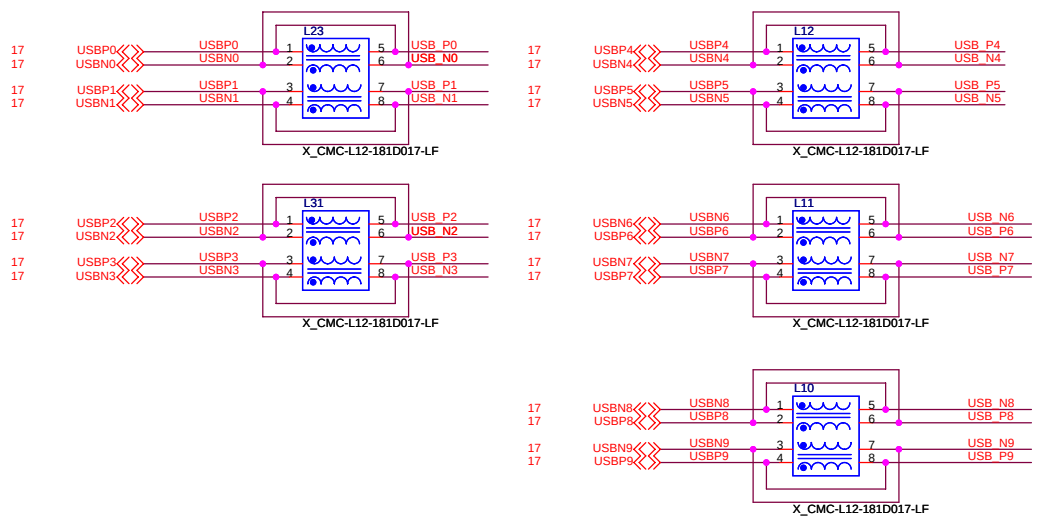
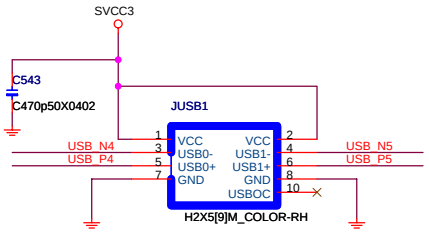
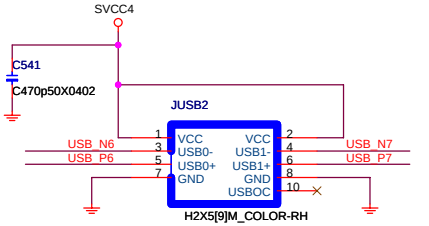
Rear USB power

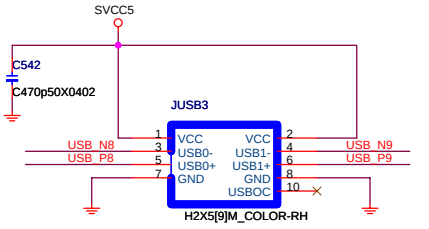


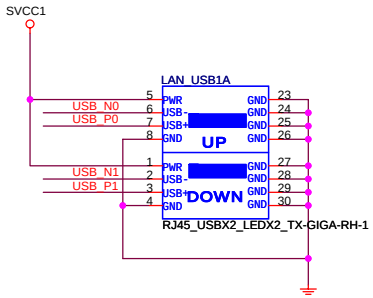
front USB power

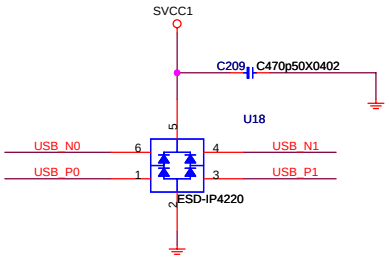


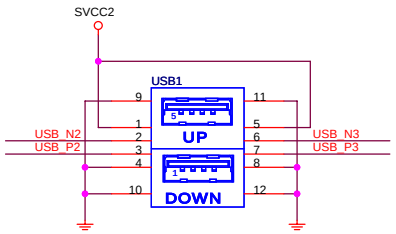


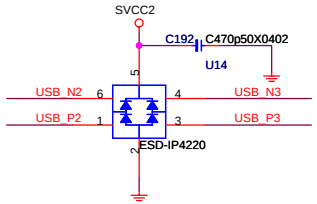


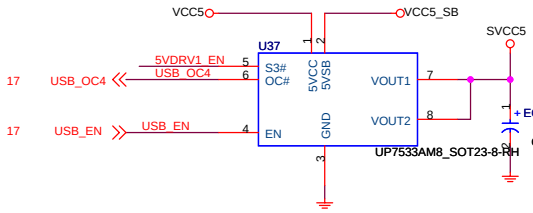












MICRO-START INT'L CO.,LTD.

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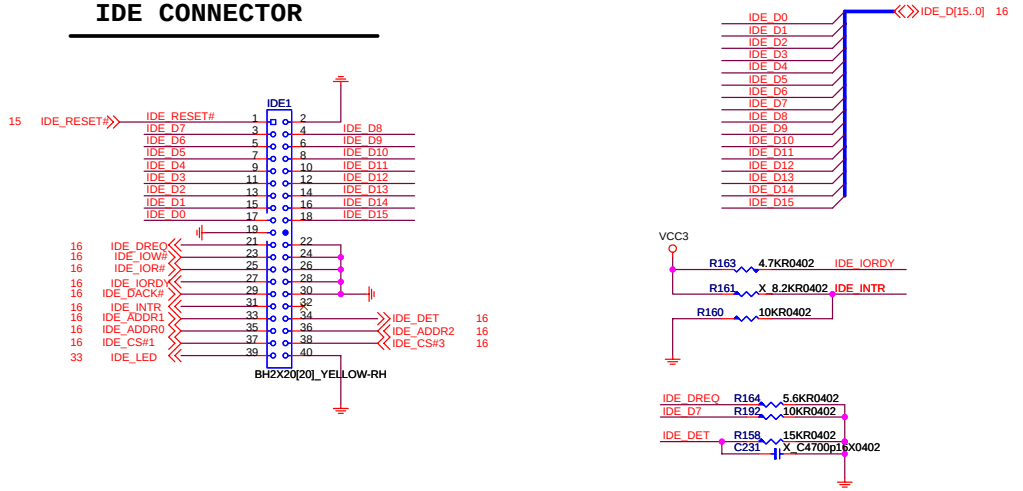
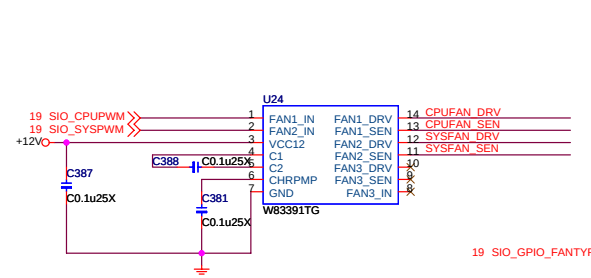
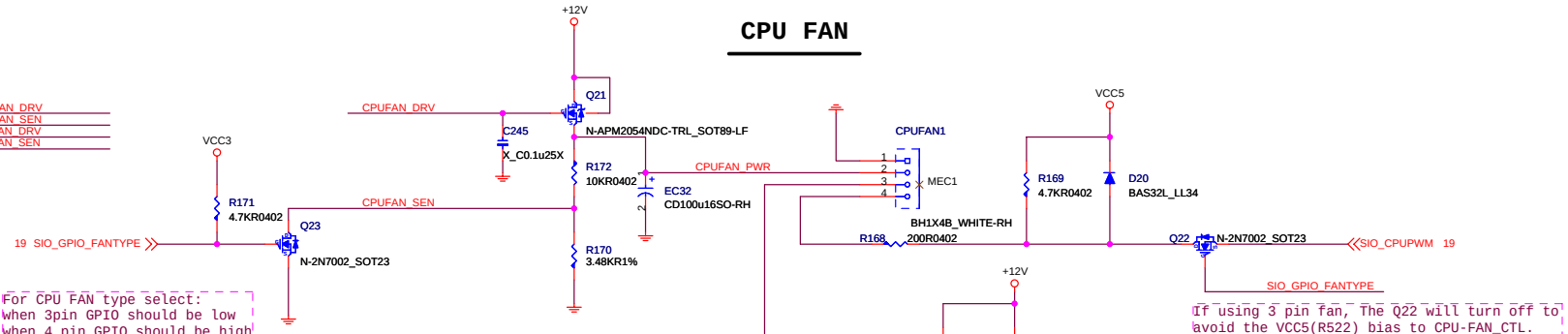
IDE CONNECTOR



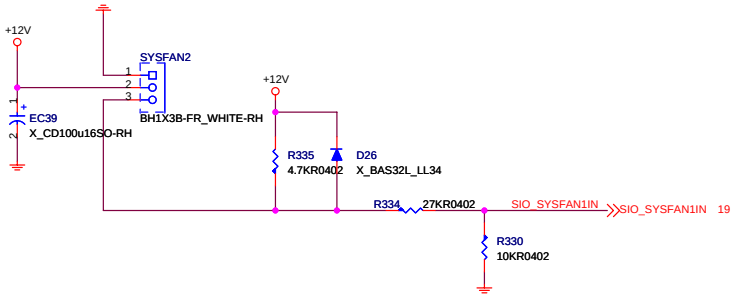
FAN CONNECTOR



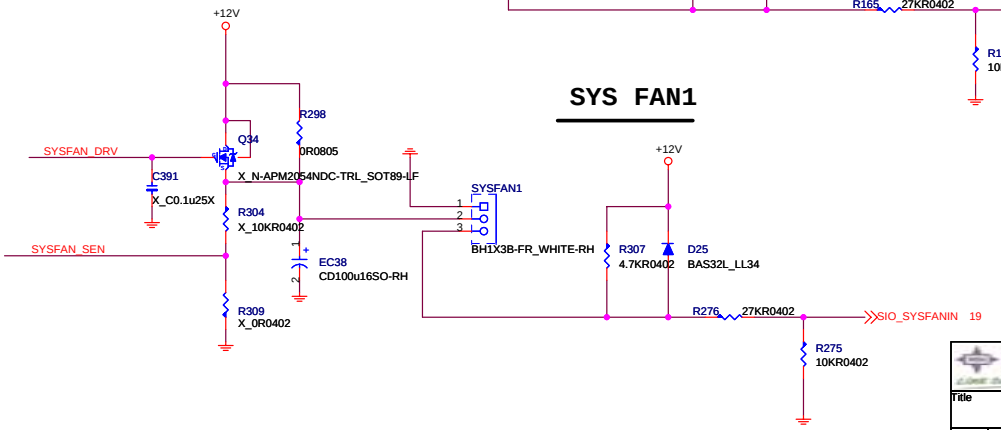
CPU FAN



SYS FAN2



SYS FAN1



MICRO-START INT'L CO.,LTD.		
Title: IDE&FAN CONN.		
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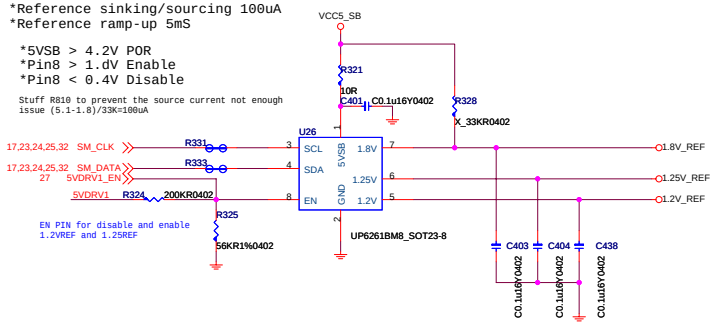
REFERENCE VOLTAGE

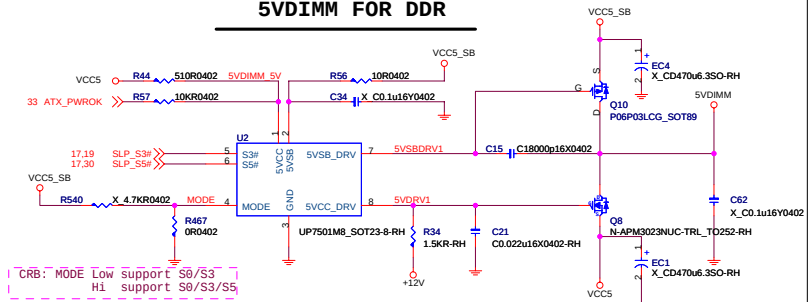
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS

*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable

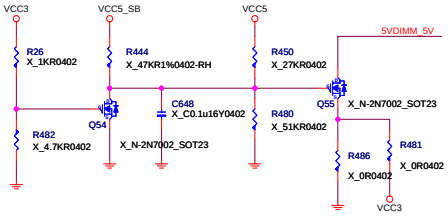
Stuff R810 to prevent the source current not enough issue (5.1-1.8)/33K=100uA



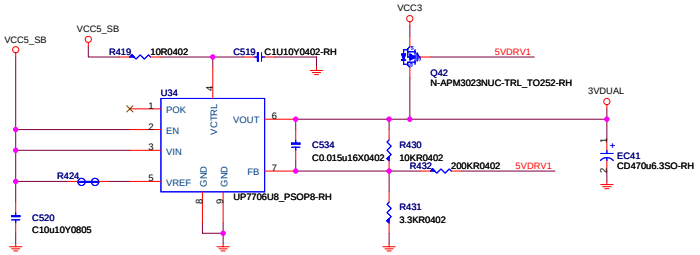
5VDIMM FOR DDR



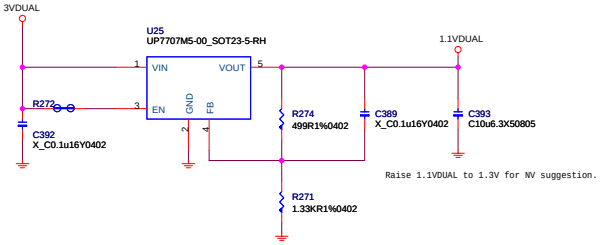
For special PSU sequence



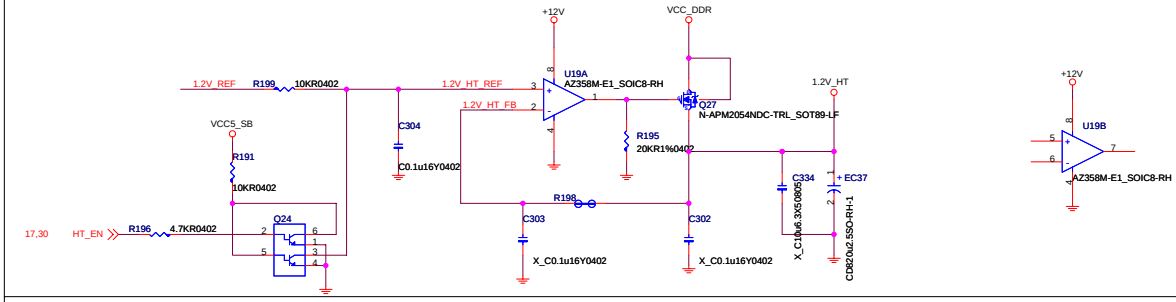
3VDUAL POWER



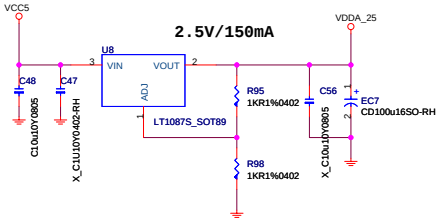
1.1DUAL POWER



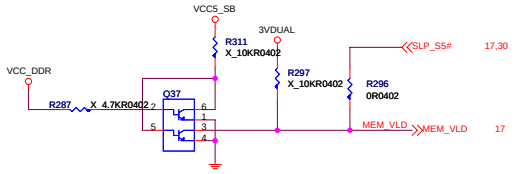
1.2V_HT POWER



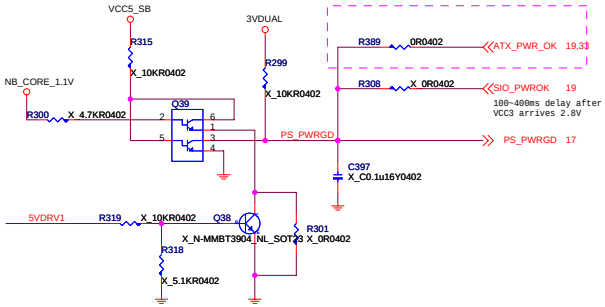
VDDA_25 POWER



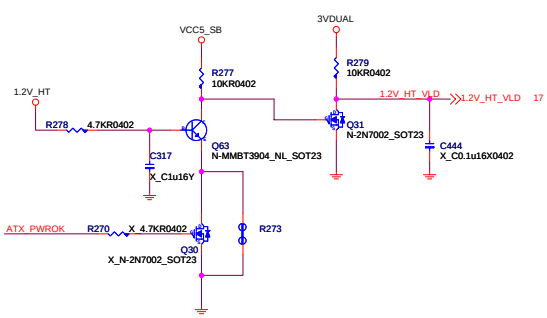
MEM_VLD CIRCUIT



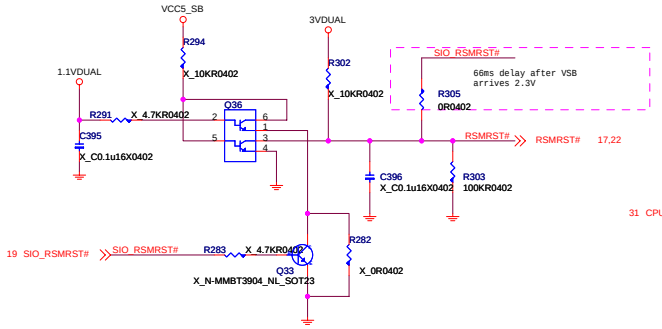
PS_PWRGD CIRCUIT



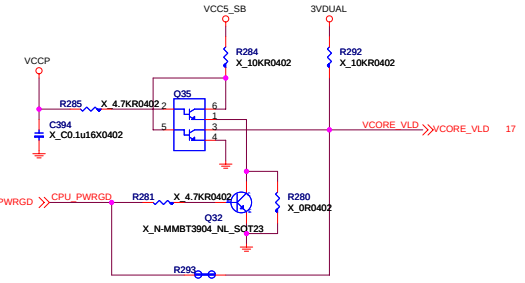
1.2V_HT_VLD CIRCUIT



PWRGD_SB CIRCUIT



VCORE_VLD CIRCUIT



MSI MICRO-START INT'L CO.,LTD.

Title	ACPI UPI&POS	
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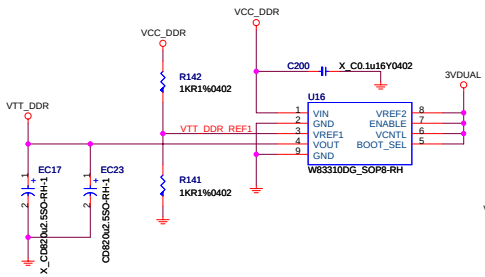
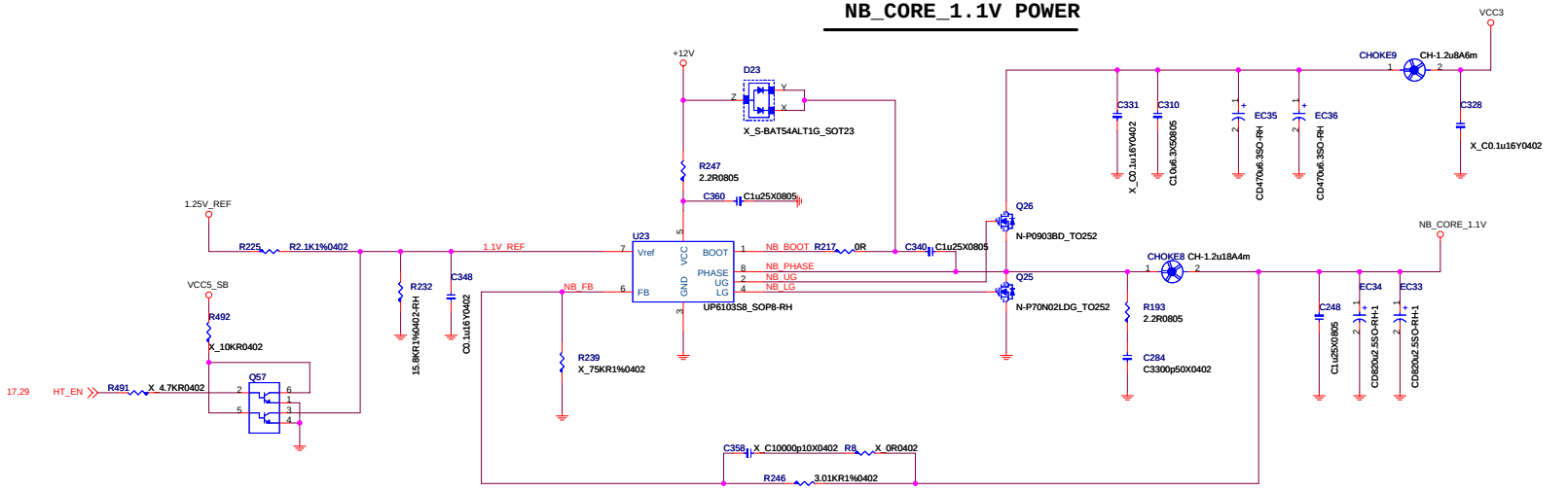
VTT_DDR POWER



DDR II 1.8V POWER

NB_CORE_1.1V POWER



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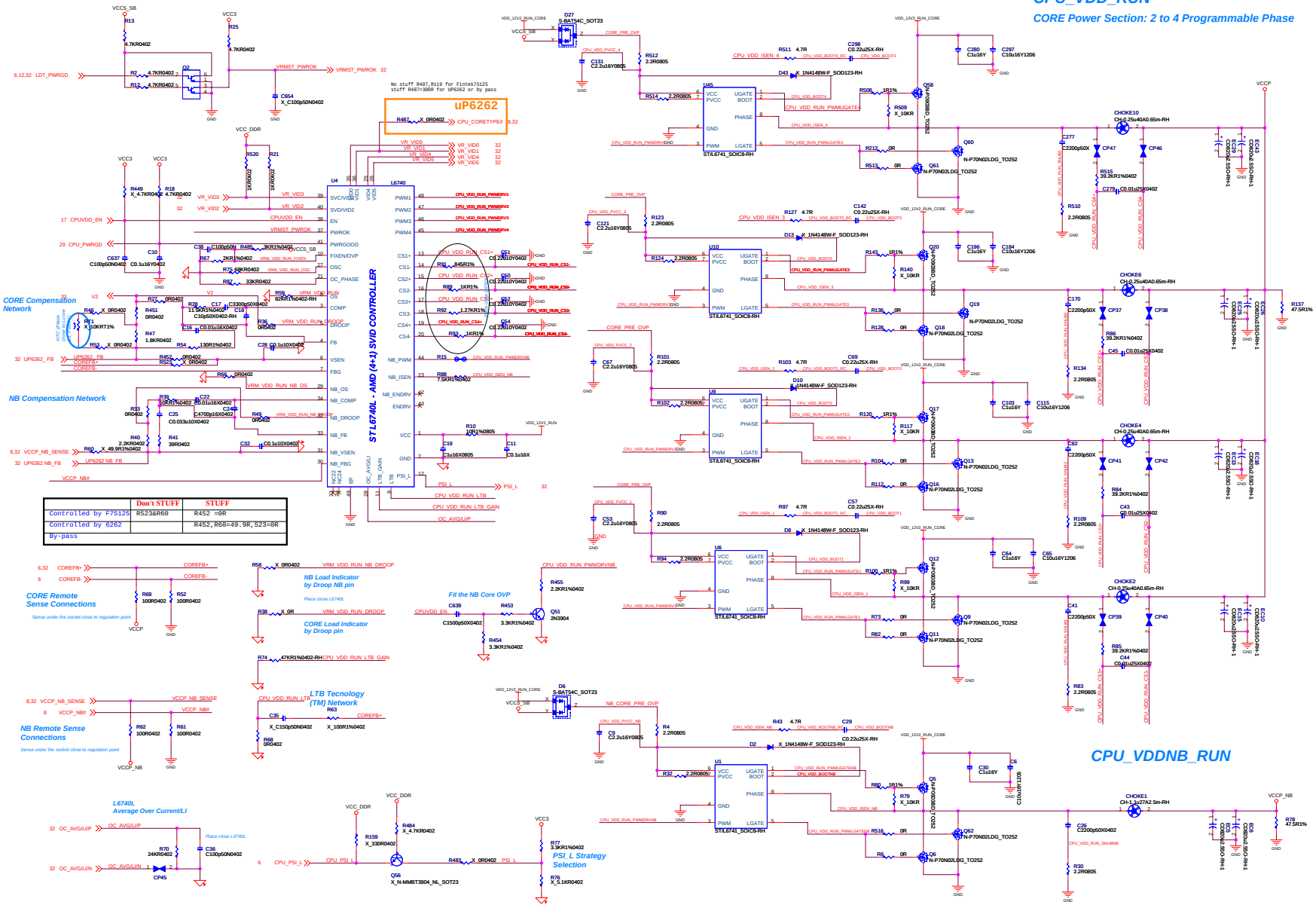
ST6740+6741

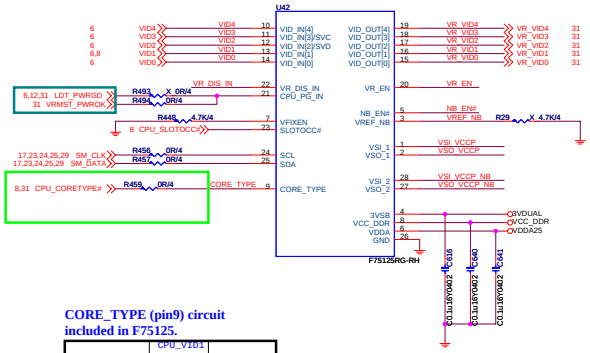
CPU_VDD_RUN

CORE Power Section: 2 to 4 Programmable Phase



CPU_VDDNB_RUN

FINTEK75125 : VCCP & VCCP_NB OV

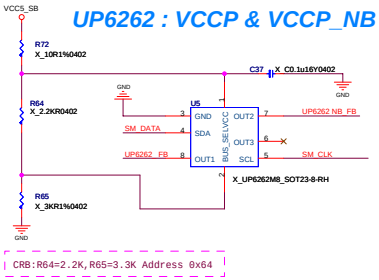


CORE_TYPE (pin9) circuit included in F75125.

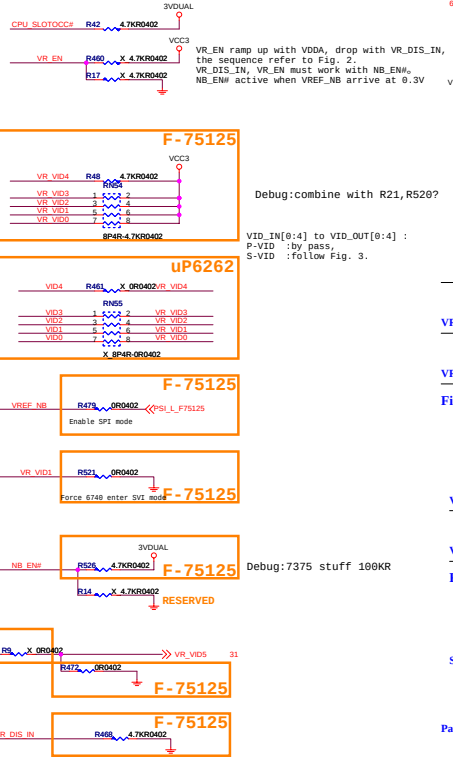
	CPU_VID1	
Parallel VID	Hi	
Serial VID	Low	

CPU_PG_IN enalble the second level of VCORE (parellel level is different from Serial level),please refer to Fig.4

UP6262 : VCCP & VCCP_NB OV



CRB:R64=2.2K,R65=3.3K Address 0x64

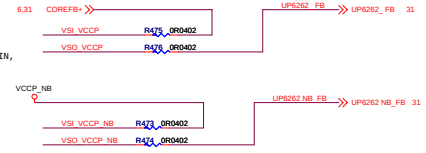


VR_EN ramp up with VDDA, drop with VR_DIS_IN, the sequence refer to Fig. 2.
VR_DIS_IN, VR_EN must work with NB_EN#。
NB_EN# active when VREF_NB arrive at 0.3V

Debug:combine with R21,R520?

VID_IN[0:4] to VID_OUT[0:4] :
P-VID :by pass,
S-VID :follow Fig. 3.

Debug:7375 stuff 100KR



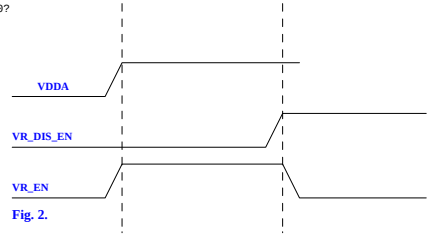


Fig. 2.

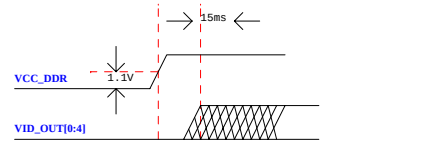


Fig. 3. Serila VID.

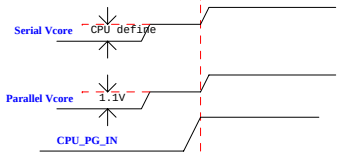
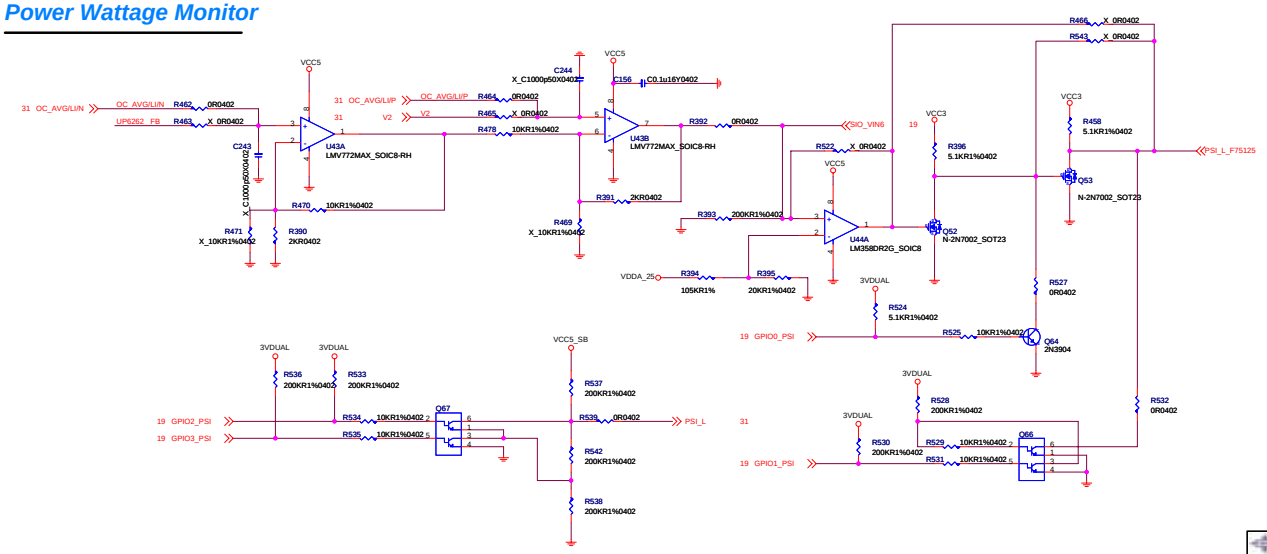


Fig. 4. serial.

Power Wattage Monitor



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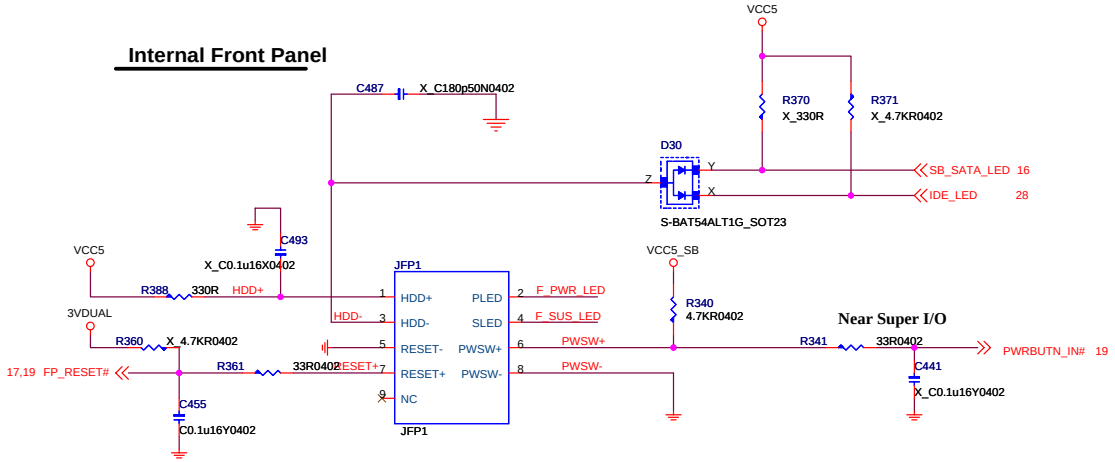
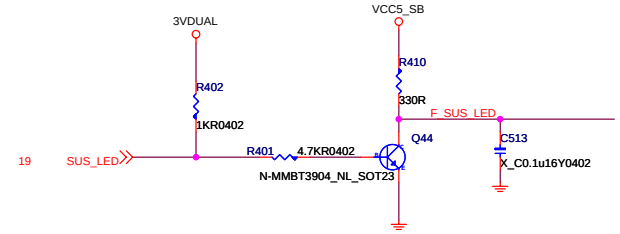
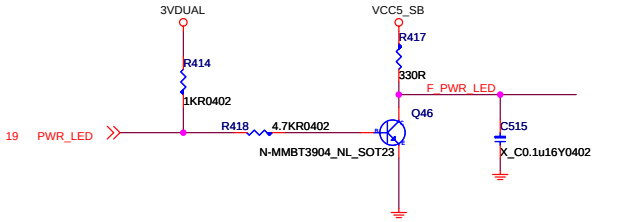
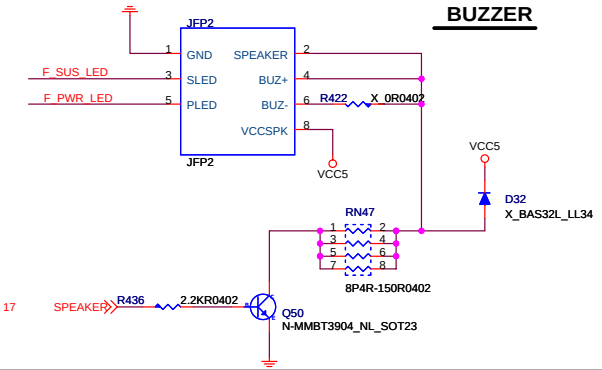
Internal Front Panel



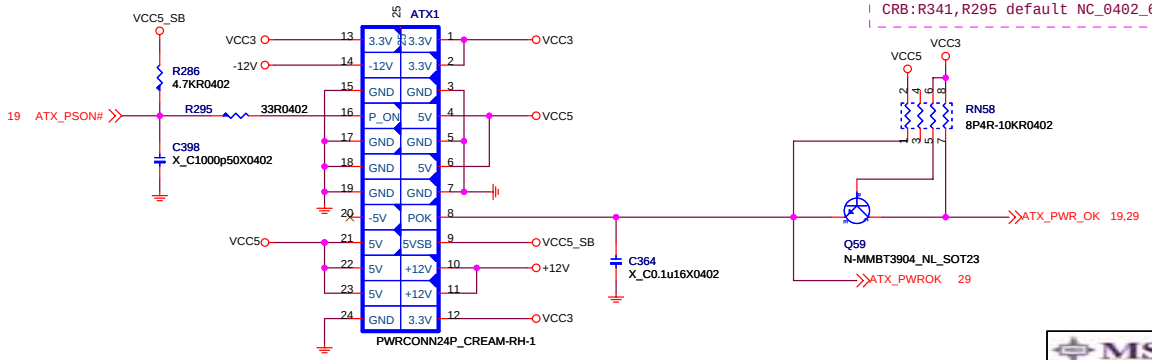


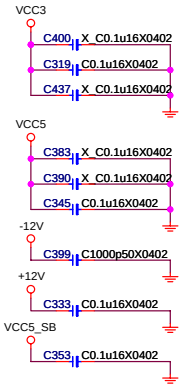


BUZZER



ATX Connector





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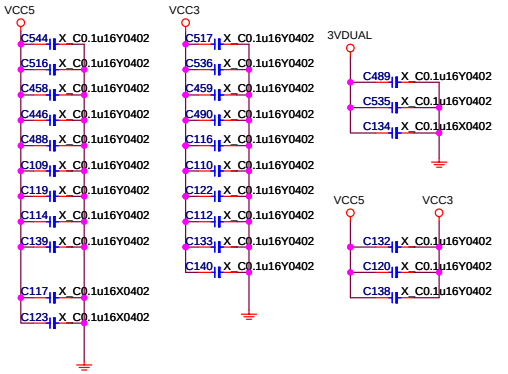
EMI solution

PCI SLOT DECOUPLING CAPACITORS



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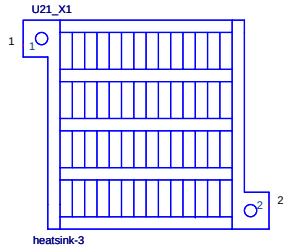
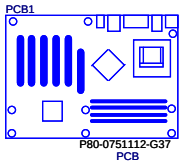
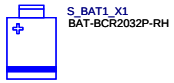
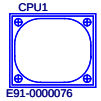
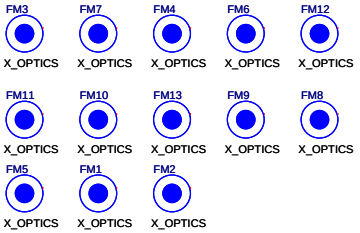




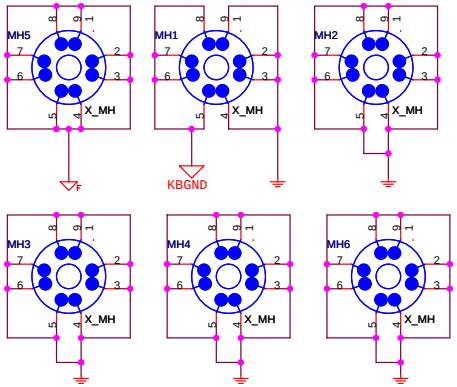




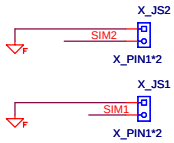
Optics Orientation Holes



Mounting Holes



Simulation



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7511	MCP78D+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+1Audio+RJ45	CFG-MCP78H	601-7511-01S
MS-7511	MCP78H/S+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+VGA+1Audio+RJ45	CFG-MCP78S	601-7511-02S

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MANUAL PARTS		
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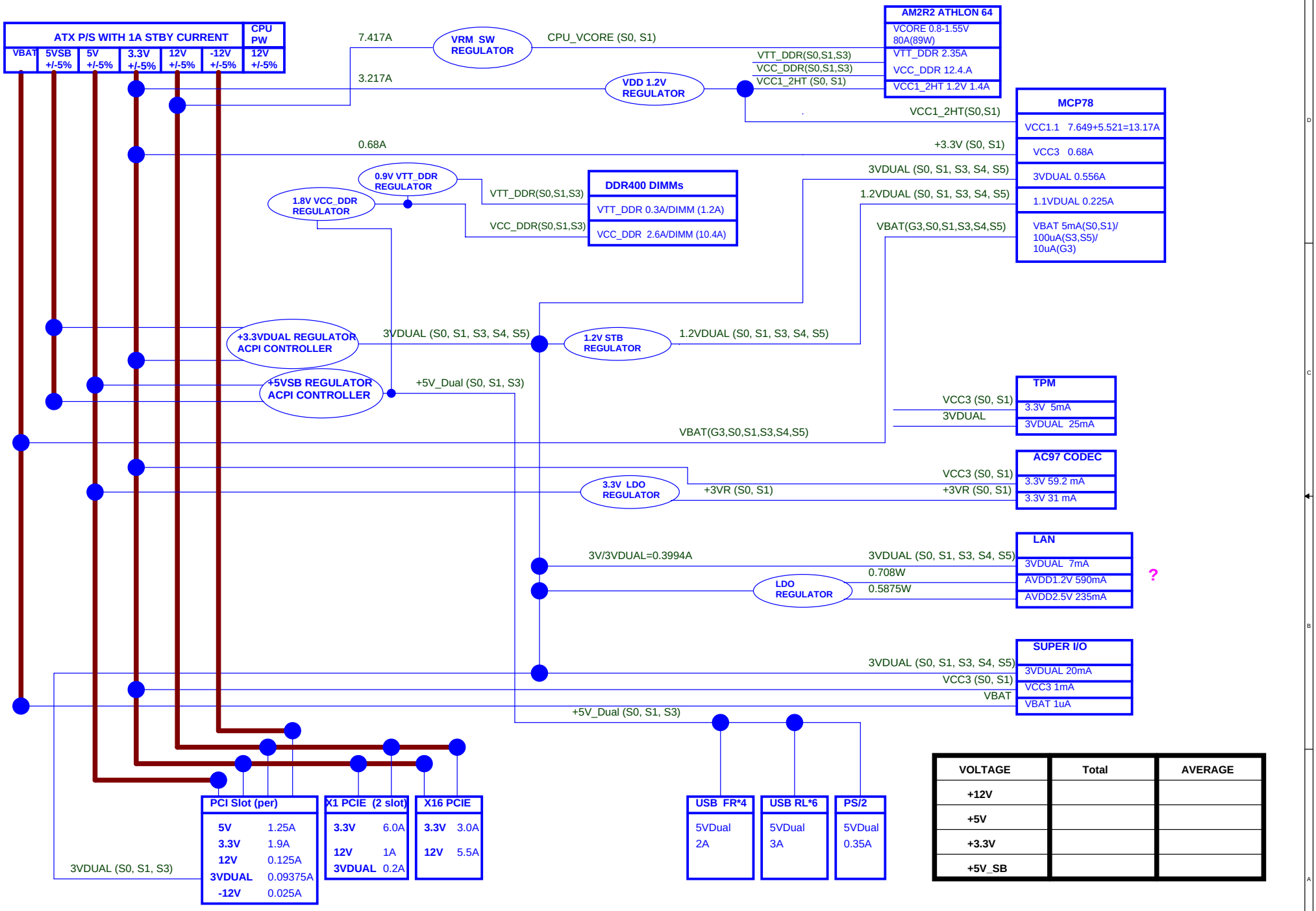

VOLTAGE	Total	AVERAGE
+12V		
+5V		
+3.3V		
+5V_SB		

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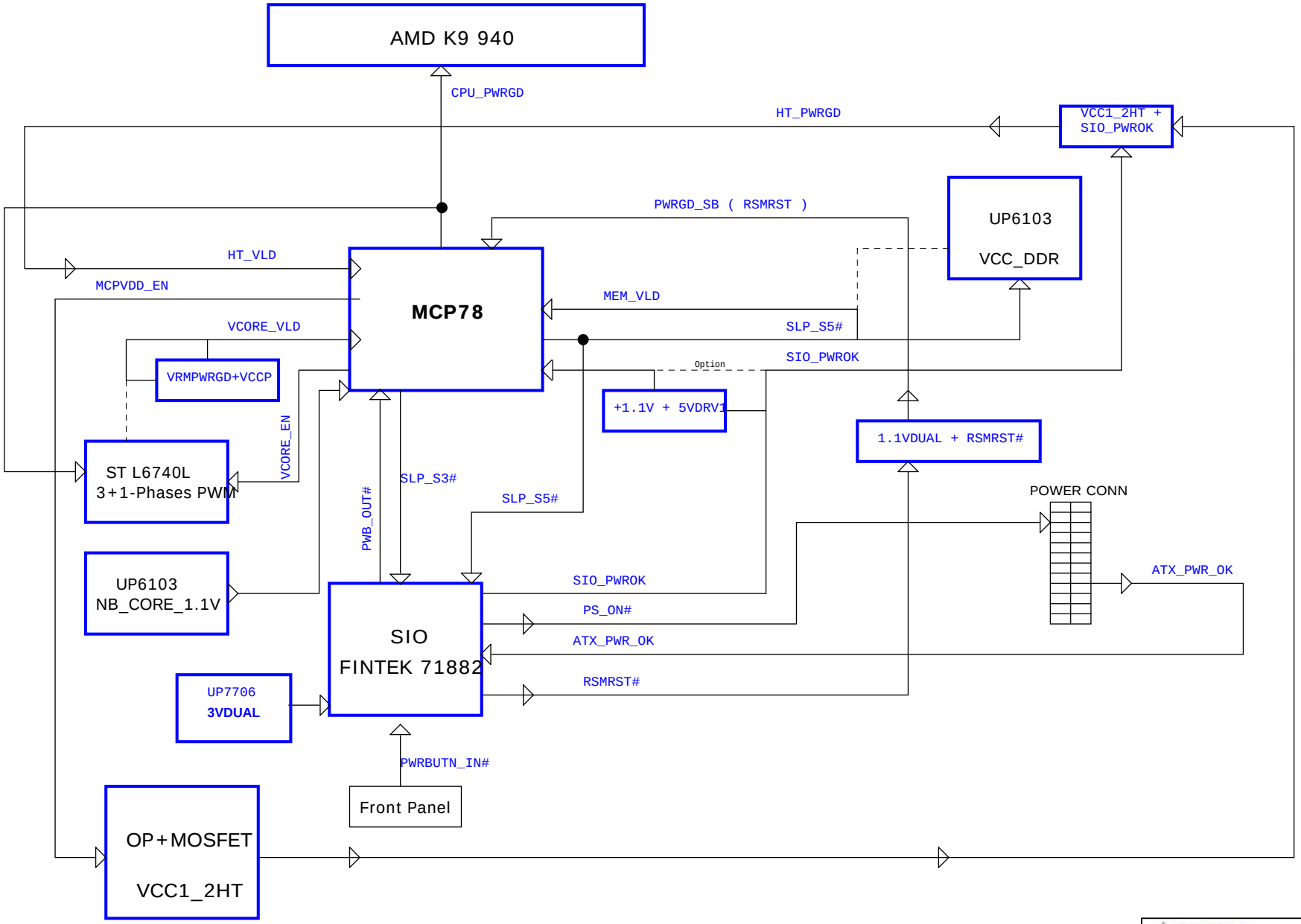
PWROK MAP



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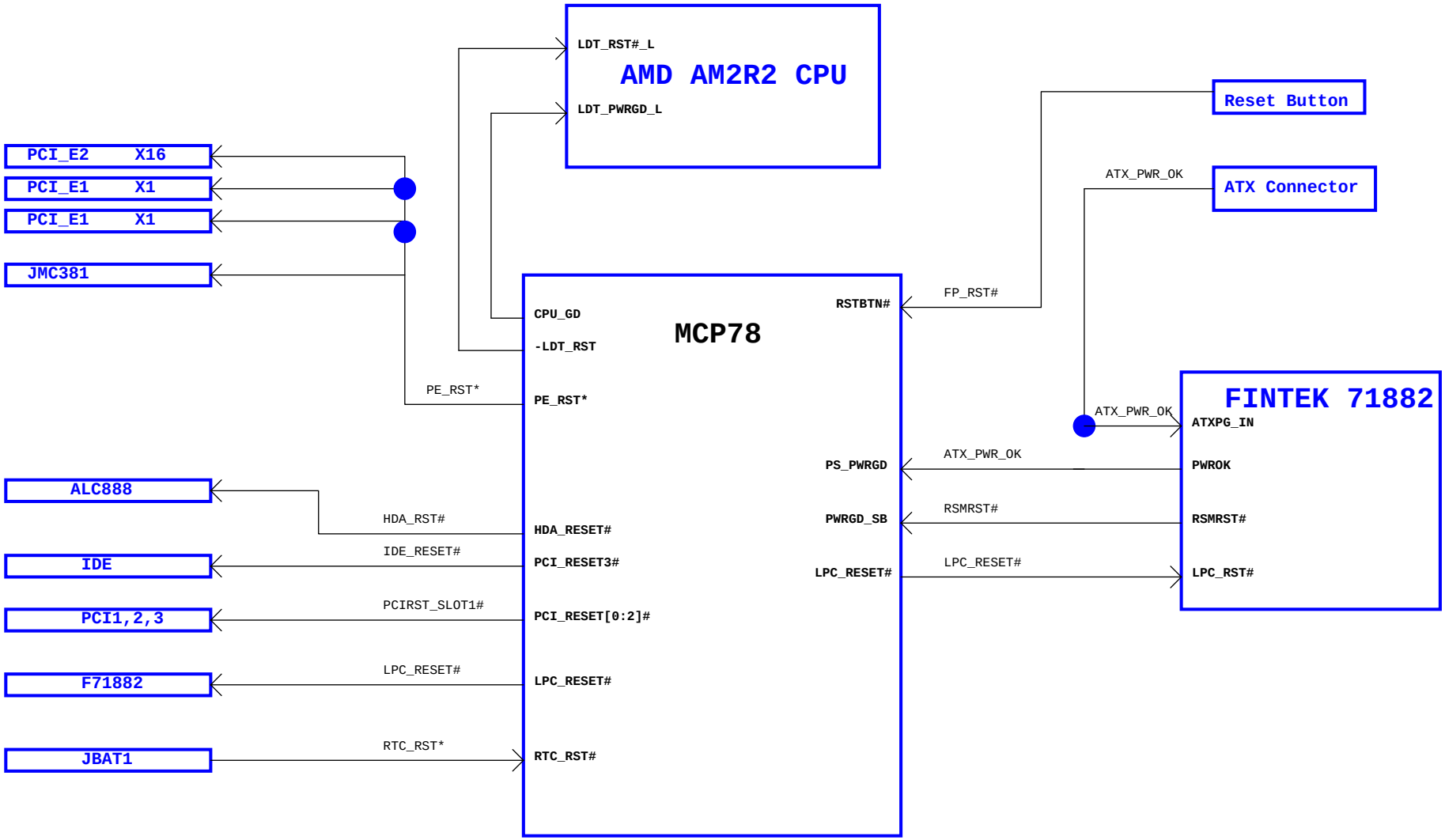
RESET MAP



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Title: MB POWER SEQUENCE

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MS-7511 0A

2007/09/07

1.page14 Remove R53,54,55 follow EMI disign
2.page21 Remove reserved R200
3.page33 Remove reserved Q58;Remove ATX_PWROK level shift RN58,Q59
4.page17,26 Modify the USB_OC circuit
5.page32 R340(PWSW+) change to pull-hi to VCC5_SB
6.page29 Q10 D, S reverse
7.page30 Reserved R7,R8
8.page26 L10 USB PN reversed
9.page8,19 Remove CPU_SLOTOCC#
10.page29 R279 pull-hi to 3VDUAL
11.page31 power swap phase1 and phase2

2007/10/19

1.page17 USBRBIAS R445 change to 909R1% refer to APnote
2.page08 C559 modify ASM COMM to 5020
3.page6,29,30 For A01Q, remove R17,R231,fit 1.1VUDAL
and NB_CORE_1.1V to 1.1V level
4.page31 Remove R449
5.page29 Stuff C403,C404,C438 to fit the reference sawtooth;
Stuff Q1,Q31 for POS
6.page14 stuff R260,C377 for ix the VGA fail issue
7.page30 Reserved R7,R8

2007/10/19

1.page14 Modify C370,C371 15pF to fit RTC slow issue
2.page17 And reserved C306,C557
3.page15,25 Modify PCI slot2 to PCI_REQ#4/PCI_GNT#4
due to PCI_REQ#1/GNT# cannot porting right
4.page32 Add Fintk75125 circuit
5.page14,26 Instead VGA with DVI
6.page23 Modify the termination R to RN56,RN57 56ohm5%
7.page29,30 NB_CORE1.1V follow the ramp up of 1.2V_HT;
Reserve ATX_PWR_OK as the PS_PWRGD
8.page16 Swap the part reference SATA4 &SATA5
9.page26,30 Modify EC17,EC23,EC24,EC30,EC61,EC62,EC63
footprint to C_P3_5_D8_H11_5
10.page31 R59,R91,R92 value
Add R485 3KR and modify R67 2KR to fit at 2.0V precisely;
Reserve Q51 for PVI OVP trigger to prevent noboot
11.page21 Update Audio jack footprint to AUDIO_JACK6_26P_U1_1
12.page22 Remove R159;add C359,C377 ;modify C292,C111 for EMI
13.page17 Reserve EC64;Add C645 close to pin U21.K3
14.page29 Reserver the Special PSU sequence cicrcuit
15.Page26 Modify RN21,RN24 to reserved L23,L31
16.Page 6 Remove R17,R231;Reserve R487,R488

MS-7511 1.1

2008/01/07

1.page 6 Add R489,R490 for Phenom noise issue Apnote
2.page21 Modify JACK1 footprint to AUDIO_JACK6_26P_U1;
short AUDIO1/AUDIO2 to GNDF for 3 Hole connector
3.page30 Reserve R491,R492,Q57 for debug to fit VCORE_1.1V
ramp up with 1.2V_HT controlled by HT_EN;
R232=15.8KR1%
4.page31 Remove R21;Modify R59 to 82KR1%;Not stuff R58 and stuff R49
5.page32 Reserve R493,R494 for 75125;R64=2.2K,R65=3.3K Address 0x64
6.page24 Separate PCIE16X PE_RESET# from 1X device for Hybrid SLI

MS-7511 1.2

2008/02/17

1.page 13,14,26 Add DVI connetctor
2.page14 R251,R257 modify to 1.47KR1%
3.page17 R245 modify to 845R1%
4.page19,20 Remove COM1 and modify COM2 to SIO UART A port
5.page21 For WHQL: R425 modify to 348R1%,C613 modify to 10uX5R,
R440,R441,R442,R443 modify to 100R
6.page31 PWR solution 4Phase 12MOS;Add Q62,D27
7.page12~18 Modify PLL filter follow NV APnote(DA-03779)
8.page27 Modify UP7533 Pin5 to 5VDRV1_EN
9.page19,33 Modify SIO pin78 to ATX_PWR_OK;remove R231
10.page6,8 Modify R107,R108,R81,R96 modify to R0805 size
11.page19 Modify 1.2V_HT_VLD circuit
12.page26 Add R231,R519,D45
13.page31,32 Add R21,R520,R17,R521;Remove R477,R249;
modify NB_EN# pull up to 3VDUAL
13.page17,19 RN26,RN24 swap pins
14.page19,31,32 Update UP75125 and PSI circuit ,and GPIO pins

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