

# MS-7511

ATX(305mm X 210mm)

## CPU:

AMD AM2+ Socket940

## System Chipset:

North Bridge --- MCP78

South Bridge --- NA

## OnBoard Chipset:

Clock Gen:NA

AZALIA Codec:ALC888

LAN Chip: REL8211BL

SIO:Fintek 882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (MCP)

## Main Memory:

DDRII\* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 3

## PWM:

Controller:STL6740L+6741

## ACPI:

UPI solution

## Other:

FDD \*1

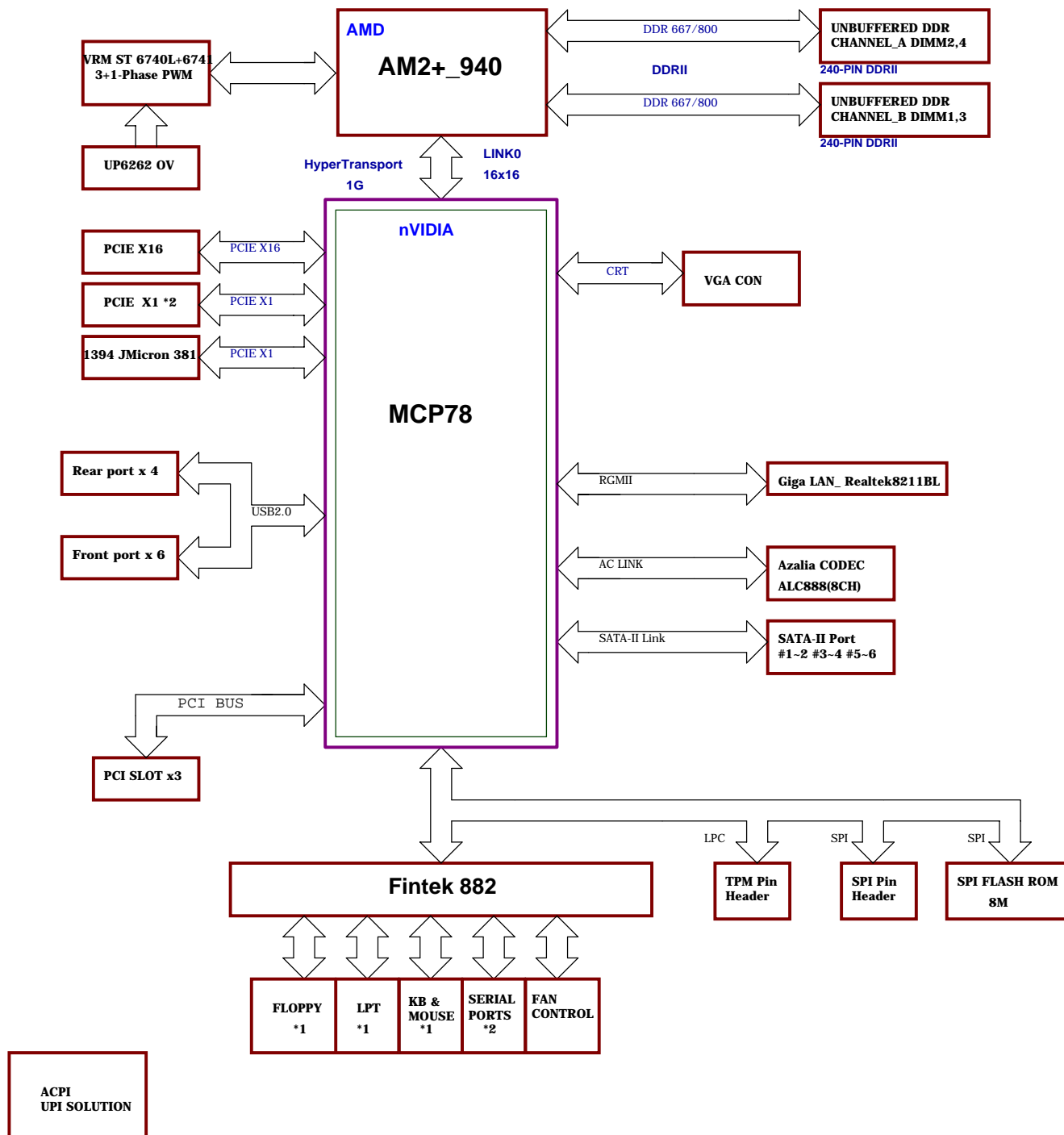
SATA(SATA2-300MB/s) \* 6

USB2.0 \*10 (Rear\*4 Front\*6)

COM PORT \*2

LPT PORT \*1

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 3 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 2 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 4 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	LAN_USB1	USB0- USB0+ USB1- USB1+	USB_OC0
	USB1	USB2- USB2+ USB3- USB3+	USB_OC1
Front	JUSB1	USB4- USB4+ USB5- USB5+	USB_OC3
	JUSB2	USB6- USB6+ USB7- USB7+	USB_OC4
	JUSB3	USB8- USB8+ USB9- USB9+	USB_OC5
	JUSB4	USB10- USB10+ USB11- USB11+	

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ0# PCI_GNT0#	AD21	PCI_CLKSLOT1 (PCI_CLK0)
PCI Slot 2	PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z	PCI_REQ1# PCI_GNT1#	AD22	PCI_CLKSLOT2 (PCI_CLK1)
PCI Slot 3	PCI_INT#Z PCI_INT#W PCI_INT#X PCI_INT#Y	PCI_REQ2# PCI_GNT2#	AD23	PCI_CLKSLOT3 (PCI_CLK2)
TPM				PCICLK_TPM (TPM_CLK)
Chipset				PCI_CLKIN (PCICLK4)
LPC				LPC_CLK
SIO				LPC_SIO24M

CPU VID TABLE	
VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

PCI DEVICE RESET MAP


MCP78	
Signals	Target
PCI_RESET#0	PCISLOT1
PCI_RESET#1	PCISLOT2
PCI_RESET#2	PCISLOT3
LPC_RESET#	SIO/TPM
IDE_RESET#	IDE

### MCP78 general purpose I/O

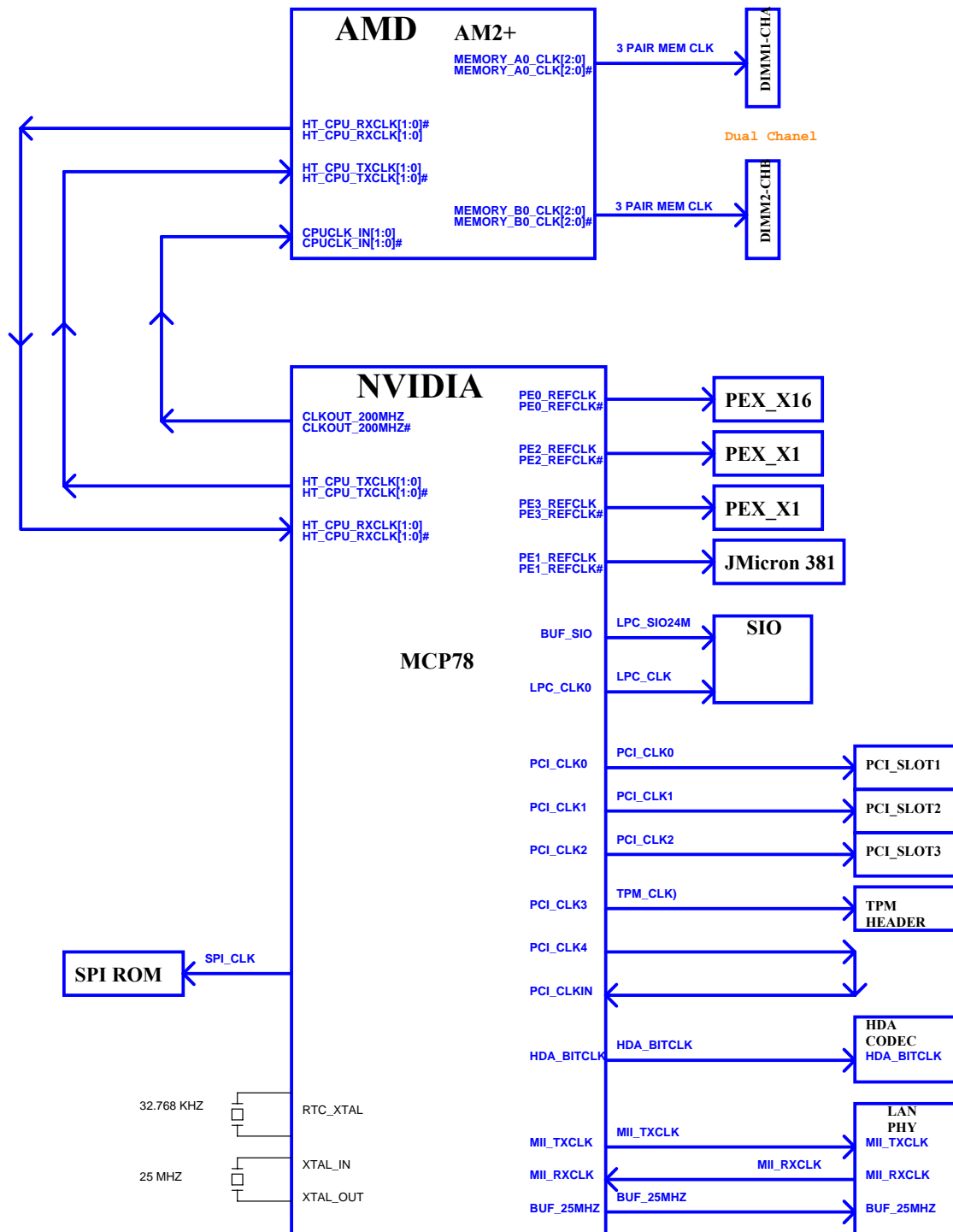
Name	Pin	Type	Function Description
<b>GPIO_1</b>	F2	I/O	NC
GPIO2/NMI#	F1	I/O	<b>PWR_SW_GPIO1</b>
GPIO3/SMI#	F6	I/O	<b>RST_GATE_GPIO2</b>
GPIO4/SCI_INTR#	J8	I/O	<b>USB_EN</b> Set as GPO When high turn on SVCC When low turn off SVCC
GPIO5/INIT#	G3	I/O	<b>DUAL_CTRL</b> Set as GPO When high turn on 5VDIMM in S4/S5 When low turn off 5VDIMM in S4/S5
GPIO6/FERR/SYS_SERR#	G5	I/O	NC
GPIO7/NFERR/SYS_PERR#	G6	I/O	NC
GPIO8/SPI_DI	D3	I/O	<b>SPI_DI</b>
GPIO9/SPI_DO	D4	I/O	<b>SPI_DO</b>
GPIO10/SPI_CS	E4	I/O	<b>SPI_CS#</b>
GPIO11/SPI_CLK	E3	I/O	<b>SPI_CLK</b>
MII_RESET/GPIO12#	C27	I/O	<b>MII_RESET</b>
MII_COL/GPIO13/MI2C_DATA	E24	I/O	<b>MII_COL</b>
MII_CRS/GPIO14/MI2C_CLK	F23	I/O	<b>MII_CRS</b>
LPC_DRQ1/GPIO15/FANRPM1#	B9	I/O	NC
DDC_CLK/GPIO17	B6	I/O	<b>DDC_CLK</b>
DDC_DATA/GPIO19	A6	I/O	<b>DDC_DATA</b>
PROCHOT#/GPIO20	AD8	I/O	<b>PROCHOT#</b>
PE_WAKE#/GPIO21	B22	I/O	<b>PE_WAKE#</b>
HDA_SDATA_IN0/GPIO22	A2	I/O	<b>HAD_SDATA_IN0</b>
HDA_SDATA_IN1/GPIO23	B1	I/O	NC
HDA_SDATA_IN2/GPIO24	B2	I/O	NC
USB_OC0#/GPIO25	P7	I/O	<b>USB_OC0</b>
USB_OC1#/GPIO26	P8	I/O	<b>USB_OC1</b>
USB_OC2#/GPIO27	P9	I/O	<b>USB_OC2</b>
USB_OC3#/GPIO28	P5	I/O	<b>USB_OC3</b>
USB_OC4#/GPIO29	P6	I/O	<b>USB_OC4</b>
PCI_PME#/GPIO30	E22	I/O	<b>PCI_PME#</b>
SIO_PME#/GPIO31	F4	I/O	<b>SIO_PME#</b>
EXT_SMI#/GPIO32	F3	I/O	NC
RI/GPIO33	H4	I/O	NC
SUS_CLK/GPIO34	E1	I/O	NC
MII_INTR/GPIO35	G24	I/O	<b>MII_INTR</b>
MII/RXER/GPIO36	D24	I/O	<b>MIIRXER</b>
MII_PWRDOWN/GPIO37	F24	I/O	NC
PCI_REQ3/GPIO38/RS232_CTS#	H14	I/O	<b>PCI_REQ3</b> Pull hi to VCC3
PCI_GNT3/GPIO39/RS232_RTS#	J14	I/O	<b>PCI_GNT3</b> Pull hi to VCC3
PCI_REQ2/GPIO40/RS232_DSR#	C11	I/O	<b>PCI_REQ2</b>
PCI_GNT2/GPIO41/RS232_DTR#	B10	I/O	<b>PCI_GNT2</b>
PCI_PERR/GPIO43/RS232_DCD#	G18	I/O	<b>PCI_PERR</b>
HDA_SYNC/GPIO44	B3	I/O	<b>HAD_SYNC</b>
HAD_SDATA_OUT0/GPIO45	A3	I/O	<b>HAD_SDATA_OUT0</b>
THERM_ALERT#/GPIO47	AF7	I/O	<b>CPU_THERM_ALERT#</b>
THERM_SIC/GPIO48	AH7	I/O	NC
THERM_SID/GPIO49	AF8	I/O	NC
LPC_DRQ0#/GPIO50	C9	I/O	<b>LPC_DRQ0#</b>
PCI_REQ4#/GPIO52	H14	I/O	<b>PCI_REQ4#</b> Pull hi to VCC3
PCI_GNT4#/GPIO53	D13	I/O	<b>PCI_GNT4#</b> Pull hi to VCC3
LPC_PWRDWN#/GPIO54	C8	I/O	NC
A20GATE/GPIO55	F5	I/O	<b>A20GATE</b>
KBRSTIN#/GPIO56	A4	I/O	<b>KBRST#</b>
SATA_LED#/GPIO57	A5	I/O	<b>SB_SATA_LED#</b>
THERMTRIP#/GPIO58	AE8	I/O	<b>CPU_THRIP#</b>
THERM/GPIO59	C6	I/O	<b>THERM#</b>
FANRPM0/GPIO60	E6	I/O	NC
FANCTL0/GPIO61	D6	I/O	NC
FANCTL1/GPIO62	C5	I/O	NC

### Super I/O general purpose I/O

Name	Pin	Type	Function Description
VIDOUT0/GPIO0	50	I/O	NC
VIDOUT0/GPIO1	51	I/O	NC
VIDOUT0/GPIO3	52	I/O	NC
VIDOUT0/GPIO4	53	I/O	Reserved for BIOS USE
VIDOUT0/GPIO5/SID	54	I/O	Reserved for BIOS USE
<b>SLOT0CC#/GPIO6</b>	55	I/O	Reserve pull hi to 3VUDAL
GPIO7/TURBO1#/WDTRST#	56	I/O	<b>WDTRST#</b> is used for over clock
GPIO10/SPI_CLK/FANIN4	59	I/O	<b>DLED1</b>
GPIO11/SPI_CS0#/FABCTL4	60	I/O	<b>DLED2</b>
GPIO12/SPI_MISO/FANCTL1_1	61	I/O	<b>DLED3</b>
PIO13/SPI_MOSI/BEEP	62	I/O	NC
GPIO14/FWH_DIS/WDTRST#/SPI_CS1#	63	I/O	<b>DLED4</b>
GPIO15/LED_VSB/ALERT#	64	I/O	<b>LED_VSB</b>
GPIO16/LED_VCC/TURBO2#	65	I/O	<b>LED_VCC</b>
GPIO17	66	I/O	<b>SPI_WP#</b>
PCIRST1#/GPIO20	74	I/O	NC
PCIRST2#/GPIO21	75	I/O	NC
PCIRST3#/GPIO22	76	I/O	NC
GPIO23/RSTCON#	77	I/O	<b>SIO_GPIO_FANTYPE</b> For CPU FAN type select: when 3pin GPIO should be low when 4pin GPIO should be high
ATXPG_IN/GPIO24	84	I/O	ATX_PWEROK
PME#/GPIO25	79	I/O	SIO_PME#
PWSIN#/GPIO26	80	I/O	PWRBUT_IN#
PWSOUT#/GPIO27	81	I/O	PWB_OUT#
S3#/GPIO31	82	I/O	<b>SLP_S3#</b>
PSON#/GPIO31	83	I/O	ATX_PSON#
PWROK/GPIO32	84		<b>PWROK</b> Set delay time as 100ms
RSMRST#/GPIO33	85		SIO_RSMRST#
IRTX/GPIO42	27		<b>IRTX</b>
IRRX/GPIO43	28		<b>IRRX</b>


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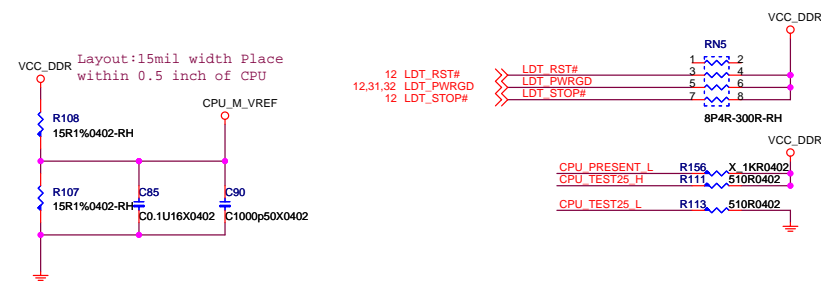
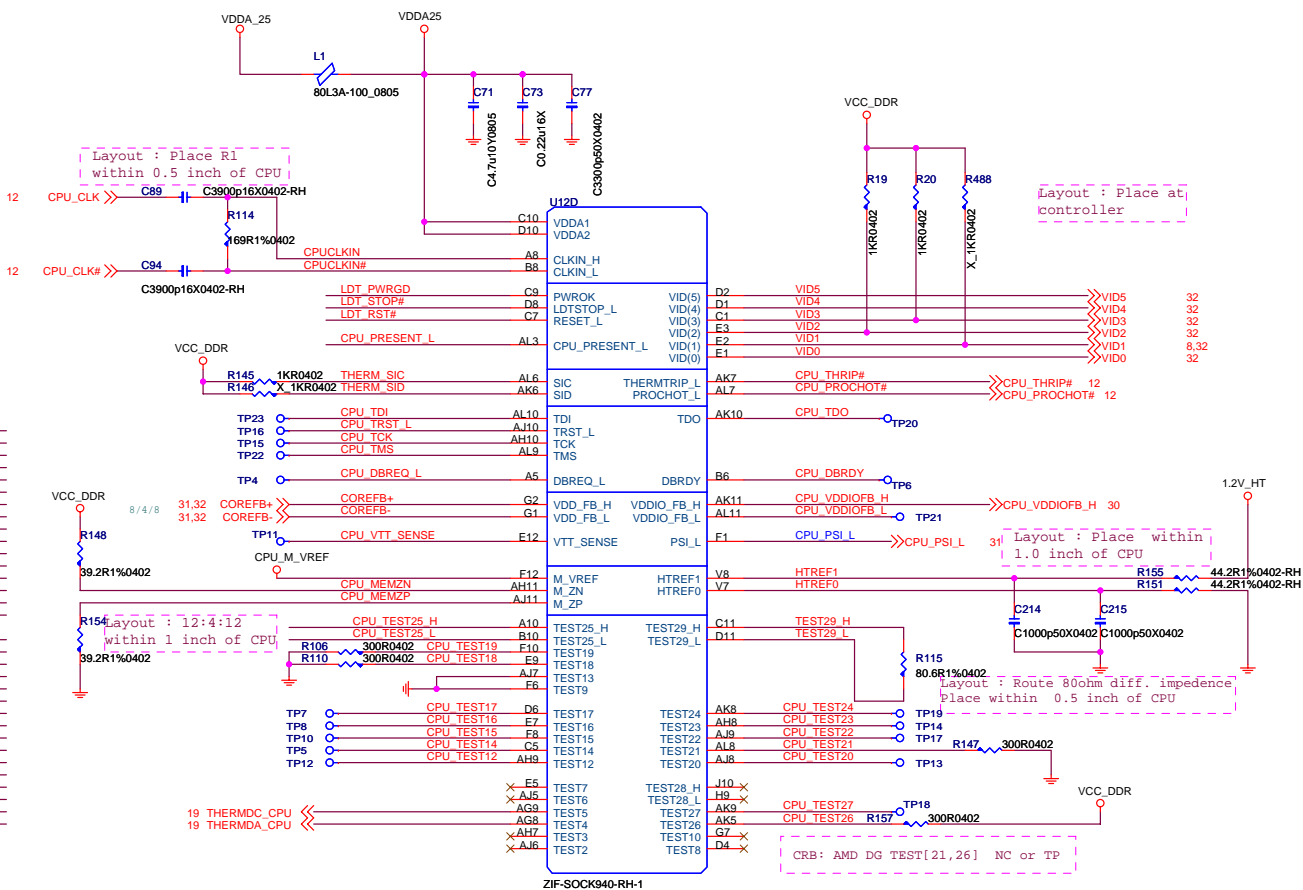
Title <b>GPIO TABLE</b>		
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Date	Wednesday, December 12, 2007	Sheet 4 of 40



12 HT\_CADIN\_H[15..0] >> HT\_CADIN\_H[15..0]  
12 HT\_CADIN\_L[15..0] >> HT\_CADIN\_L[15..0]  
12 HT\_CADOUT\_H[15..0] >> HT\_CADOUT\_H[15..0]  
12 HT\_CADOUT\_L[15..0] >> HT\_CADOUT\_L[15..0]

12 HT_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	HT_CLKOUT_H1	12
12 HT_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	HT_CLKOUT_L1	12
12 HT_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	HT_CLKOUT_H0	12
12 HT_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	HT_CLKOUT_L0	12
12 HT_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	HT_CTLOUT_H1	12
12 HT_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	HT_CTLOUT_L1	12
12 HT_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	HT_CTLOUT_H0	12
12 HT_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	HT_CTLOUT_L0	12
HT_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	HT_CADOUT_H15	
HT_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	HT_CADOUT_L15	
HT_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	HT_CADOUT_H14	
HT_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AB5	HT_CADOUT_L14	
HT_CADIN_H13	T6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB4	HT_CADOUT_H13	
HT_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	HT_CADOUT_L13	
HT_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	HT_CADOUT_H12	
HT_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	HT_CADOUT_L12	
HT_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	HT_CADOUT_H11	
HT_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	HT_CADOUT_L11	
HT_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF6	HT_CADOUT_H10	
HT_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AE4	HT_CADOUT_L10	
HT_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	HT_CADOUT_H9	
HT_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	HT_CADOUT_L9	
HT_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	HT_CADOUT_H8	
HT_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	HT_CADOUT_L8	
HT_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	HT_CADOUT_H7	
HT_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	HT_CADOUT_L7	
HT_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	HT_CADOUT_H6	
HT_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	HT_CADOUT_L6	
HT_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	HT_CADOUT_H5	
HT_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	HT_CADOUT_L5	
HT_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	HT_CADOUT_H4	
HT_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	HT_CADOUT_L4	
HT_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	HT_CADOUT_H3	
HT_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	HT_CADOUT_L3	
HT_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	HT_CADOUT_H2	
HT_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	HT_CADOUT_L2	
HT_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	HT_CADOUT_H1	
HT_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	HT_CADOUT_L1	
HT_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	HT_CADOUT_H0	
HT_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	HT_CADOUT_L0	

ZIF-SOCK940-RH-1



9,10 MEM\_MA\_DQS\_L[7..0] >>  
9,10 MEM\_MA\_DQS\_H[7..0] >>  
9,10 MEM\_MA\_DM[7..0] >>  
9,10 MEM\_MA\_DATA[63..0] >>  
9,10,11 MEM\_MA\_ADD[15..0] >>

9,10 MEM\_MB\_DQS\_L[7..0] >>  
9,10 MEM\_MB\_DQS\_H[7..0] >>  
9,10 MEM\_MB\_DM[7..0] >>  
9,10 MEM\_MB\_DATA[63..0] >>  
9,10,11 MEM\_MB\_ADD[15..0] >>

U12B

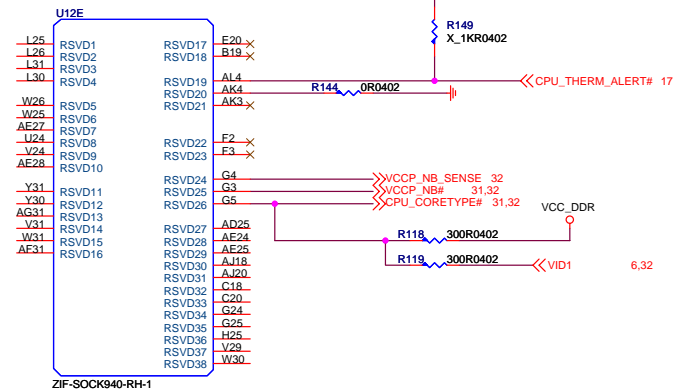
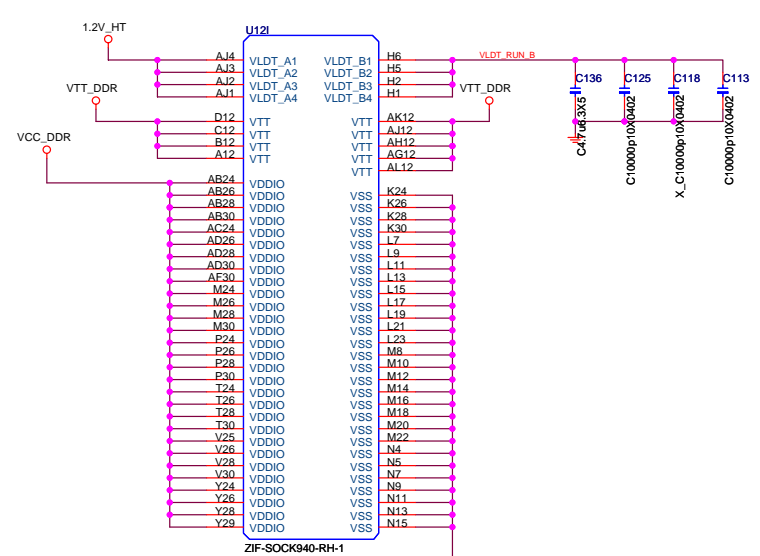
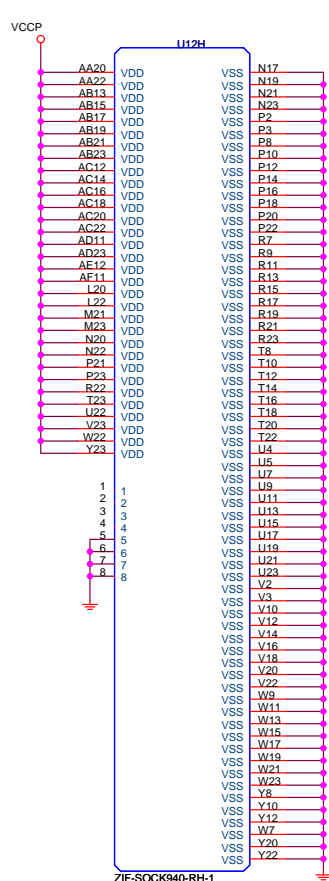
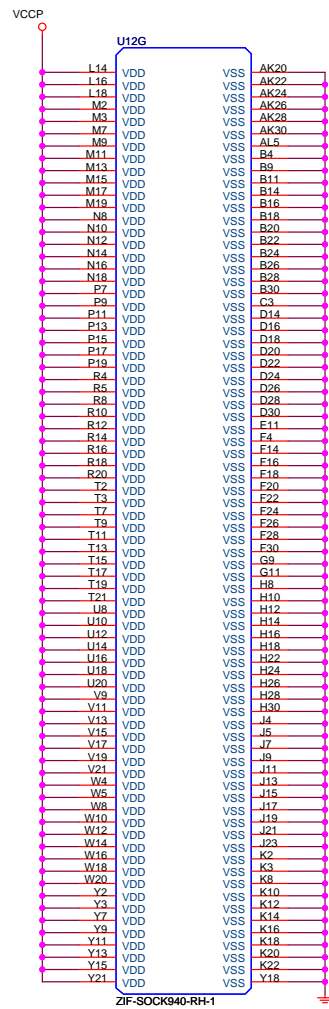
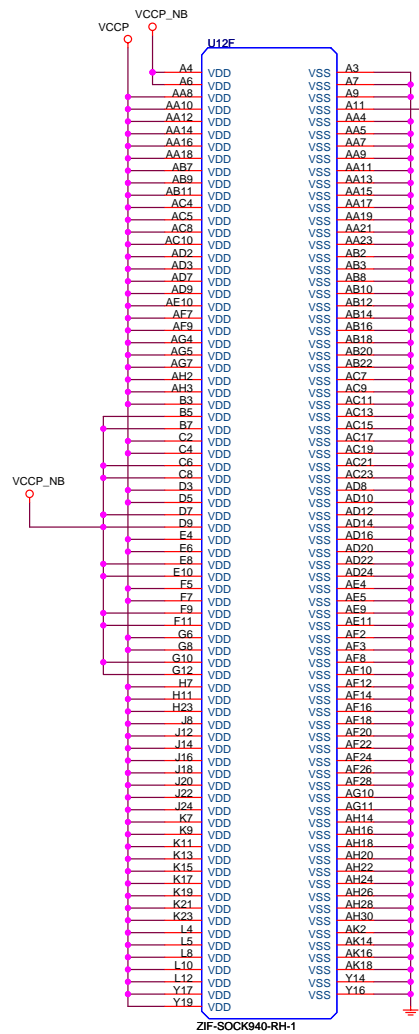
9,11 MEM_MA0_CLK_H2	>> MEM MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)	AE14	MEM MA DATA63
9,11 MEM_MA0_CLK_L2	>> MEM MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)	AG14	MEM MA DATA62
9,11 MEM_MA0_CLK_H1	>> MEM MA0_CLK_H1	AG19	MA0_CLK_H(1)	MA_DATA(61)	AG16	MEM MA DATA61
9,11 MEM_MA0_CLK_L1	>> MEM MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)	AD17	MEM MA DATA60
9,11 MEM_MA0_CLK_H0	>> MEM MA0_CLK_H0	U27	MA0_CLK_H(0)	MA_DATA(59)	AD13	MEM MA DATA59
9,11 MEM_MA0_CLK_L0	>> MEM MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)	AE13	MEM MA DATA58
				MA_DATA(57)	AG15	MEM MA DATA57
9,11 MEM_MA0_CS_L1	>> MEM MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(56)	AE16	MEM MA DATA56
9,11 MEM_MA0_CS_L0	>> MEM MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(55)	AG17	MEM MA DATA55
9,11 MEM_MA0_ODT0	>> MEM MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(54)	AE18	MEM MA DATA54
				MA_DATA(53)	AD21	MEM MA DATA53
10,11 MEM_MA1_CLK_H2	>> MEM MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(52)	AE17	MEM MA DATA52
10,11 MEM_MA1_CLK_L2	>> MEM MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(51)	AE17	MEM MA DATA51
10,11 MEM_MA1_CLK_H1	>> MEM MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(49)	AE21	MEM MA DATA49
10,11 MEM_MA1_CLK_L1	>> MEM MA1_CLK_L1	G21	MA1_CLK_L(1)	MA_DATA(48)	AE21	MEM MA DATA48
10,11 MEM_MA1_CLK_H0	>> MEM MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(47)	AE23	MEM MA DATA47
10,11 MEM_MA1_CLK_L0	>> MEM MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(46)	AE23	MEM MA DATA46
				MA_DATA(45)	AJ26	MEM MA DATA45
10,11 MEM_MA1_CS_L1	>> MEM MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(44)	AG26	MEM MA DATA44
10,11 MEM_MA1_CS_L0	>> MEM MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(43)	AE22	MEM MA DATA43
10,11 MEM_MA1_ODT0	>> MEM MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(42)	AG23	MEM MA DATA42
				MA_DATA(41)	AH25	MEM MA DATA41
9,10,11 MEM_MA_CAS_L	>> MEM MA_CAS_L	AB25	MA_CAS_L	MA_DATA(40)	AE25	MEM MA DATA40
9,10,11 MEM_MA_WE_L	>> MEM MA_WE_L	AB27	MA_WE_L	MA_DATA(39)	AJ28	MEM MA DATA39
9,10,11 MEM_MA_RAS_L	>> MEM MA_RAS_L	AA26	MA_RAS_L	MA_DATA(38)	AJ29	MEM MA DATA38
9,10,11 MEM_MA_BANK2	>> MEM MA_BANK2	N25	MA_BANK(2)	MA_DATA(37)	AE29	MEM MA DATA37
9,10,11 MEM_MA_BANK1	>> MEM MA_BANK1	Y27	MA_BANK(1)	MA_DATA(36)	AE26	MEM MA DATA36
9,10,11 MEM_MA_BANK0	>> MEM MA_BANK0	AA27	MA_BANK(0)	MA_DATA(35)	AJ27	MEM MA DATA35
				MA_DATA(34)	AG29	MEM MA DATA34
10,11 MEM_MA_CKE1	>> MEM MA_CKE1	L27	MA_CKE(1)	MA_DATA(33)	AE27	MEM MA DATA33
9,11 MEM_MA_CKE0	>> MEM MA_CKE0	M25	MA_CKE(0)	MA_DATA(32)	E29	MEM MA DATA32
				MA_DATA(31)	E28	MEM MA DATA31
				MA_DATA(30)	D27	MEM MA DATA30
				MA_DATA(29)	C27	MEM MA DATA29
				MA_DATA(28)	G26	MEM MA DATA28
				MA_DATA(27)	F27	MEM MA DATA27
				MA_DATA(26)	C28	MEM MA DATA26
				MA_DATA(25)	E27	MEM MA DATA25
				MA_DATA(24)	F25	MEM MA DATA24
				MA_DATA(23)	E25	MEM MA DATA23
				MA_DATA(22)	E23	MEM MA DATA22
				MA_DATA(21)	E23	MEM MA DATA21
				MA_DATA(20)	E26	MEM MA DATA20
				MA_DATA(19)	C26	MEM MA DATA19
				MA_DATA(18)	G23	MEM MA DATA18
				MA_DATA(17)	F23	MEM MA DATA17
				MA_DATA(16)	E22	MEM MA DATA16
				MA_DATA(15)	E21	MEM MA DATA15
				MA_DATA(14)	E17	MEM MA DATA14
				MA_DATA(13)	G17	MEM MA DATA13
				MA_DATA(12)	G22	MEM MA DATA12
				MA_DATA(11)	F21	MEM MA DATA11
				MA_DATA(10)	G18	MEM MA DATA10
				MA_DATA(9)	E17	MEM MA DATA9
				MA_DATA(8)	G16	MEM MA DATA8
				MA_DATA(7)	E15	MEM MA DATA7
				MA_DATA(6)	G13	MEM MA DATA6
				MA_DATA(5)	H13	MEM MA DATA5
				MA_DATA(4)	H17	MEM MA DATA4
				MA_DATA(3)	E16	MEM MA DATA3
				MA_DATA(2)	E14	MEM MA DATA2
				MA_DATA(1)	G14	MEM MA DATA1
				MA_DATA(0)		
				MA_DQS_H(8)	J28	X
				MA_DQS_L(8)	J27	X
				MA_DM(8)	J25	X
				MA_CHECK(7)	K25	X
				MA_CHECK(6)	J26	X
				MA_CHECK(5)	G26	X
				MA_CHECK(4)	G27	X
				MA_CHECK(3)	L24	X
				MA_CHECK(2)	K27	X
				MA_CHECK(1)	H29	X
				MA_CHECK(0)	H27	X

ZIF-SOCK940-RH-1

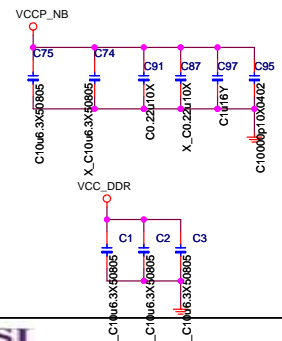
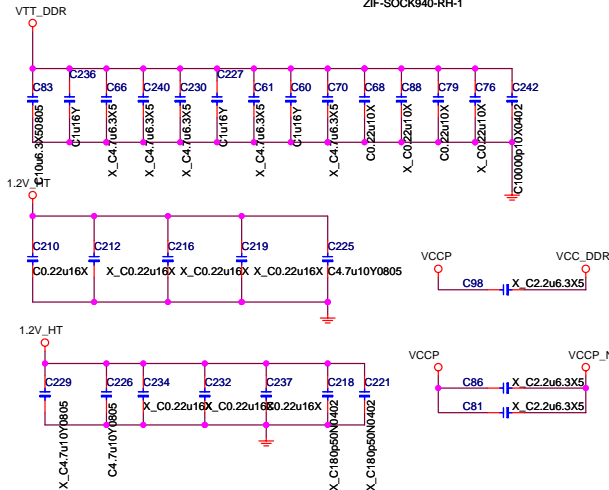
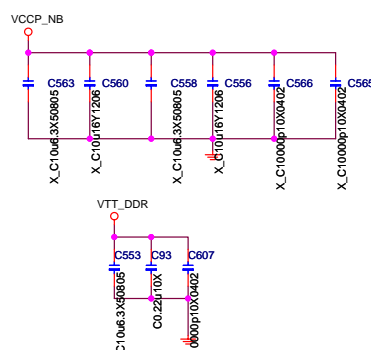
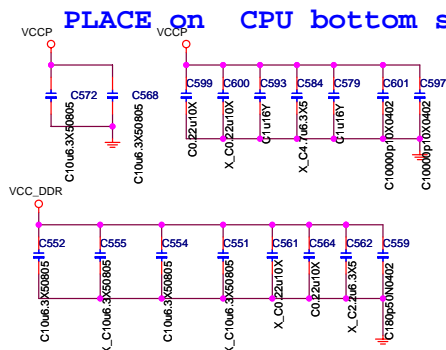
U12C

9,11 MEM_MB0_CLK_H2	>> MEM MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)	AH13	MEM MB DATA63
9,11 MEM_MB0_CLK_L2	>> MEM MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)	AL13	MEM MB DATA62
9,11 MEM_MB0_CLK_H1	>> MEM MB0_CLK_H1	AJ18	MB0_CLK_H(1)	MB_DATA(61)	AL13	MEM MB DATA61
9,11 MEM_MB0_CLK_L1	>> MEM MB0_CLK_L1	AJ19	MB0_CLK_L(1)	MB_DATA(60)	AJ15	MEM MB DATA60
9,11 MEM_MB0_CLK_H0	>> MEM MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)	AF13	MEM MB DATA59
9,11 MEM_MB0_CLK_L0	>> MEM MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)	AG13	MEM MB DATA58
				MB_DATA(57)	AK15	MEM MB DATA57
				MB_DATA(56)	AL16	MEM MB DATA56
				MB_DATA(55)	AL17	MEM MB DATA55
				MB_DATA(54)	AK21	MEM MB DATA54
				MB_DATA(53)	AL11	MEM MB DATA53
				MB_DATA(52)	AH15	MEM MB DATA52
				MB_DATA(51)	AJ16	MEM MB DATA51
				MB_DATA(50)	AH19	MEM MB DATA50
				MB_DATA(49)	AL20	MEM MB DATA49
				MB_DATA(48)	AJ22	MEM MB DATA48
				MB_DATA(47)	AJ22	MEM MB DATA47
				MB_DATA(46)	AK25	MEM MB DATA46
				MB_DATA(45)	AL24	MEM MB DATA45
				MB_DATA(44)	AJ21	MEM MB DATA44
				MB_DATA(43)	AH21	MEM MB DATA43
				MB_DATA(42)	AH23	MEM MB DATA42
				MB_DATA(41)	AJ24	MEM MB DATA41
				MB_DATA(40)	AL27	MEM MB DATA40
				MB_DATA(39)	AK27	MEM MB DATA39
				MB_DATA(38)	AH31	MEM MB DATA38
				MB_DATA(37)	AG30	MEM MB DATA37
				MB_DATA(36)	AL25	MEM MB DATA36
				MB_DATA(35)	AL26	MEM MB DATA35
				MB_DATA(34)	AJ30	MEM MB DATA34
				MB_DATA(33)	AJ31	MEM MB DATA33
				MB_DATA(32)	E31	MEM MB DATA32
				MB_DATA(31)	F30	MEM MB DATA31
				MB_DATA(30)	B27	MEM MB DATA30
				MB_DATA(29)	A27	MEM MB DATA29
				MB_DATA(28)	F29	MEM MB DATA28
				MB_DATA(27)	F31	MEM MB DATA27
				MB_DATA(26)	A29	MEM MB DATA26
				MB_DATA(25)	A28	MEM MB DATA25
				MB_DATA(24)	A25	MEM MB DATA24
				MB_DATA(23)	A24	MEM MB DATA23
				MB_DATA(22)	C24	MEM MB DATA22
				MB_DATA(21)	D21	MEM MB DATA21
				MB_DATA(20)	B25	MEM MB DATA20
				MB_DATA(19)	B23	MEM MB DATA19
				MB_DATA(18)	A26	MEM MB DATA18
				MB_DATA(17)	B21	MEM MB DATA17
				MB_DATA(16)	A20	MEM MB DATA16
				MB_DATA(15)	C16	MEM MB DATA15
				MB_DATA(14)	D15	MEM MB DATA14
				MB_DATA(13)	C21	MEM MB DATA13
				MB_DATA(12)	A21	MEM MB DATA12
				MB_DATA(11)	A17	MEM MB DATA11
				MB_DATA(10)	A16	MEM MB DATA10
				MB_DATA(9)	A16	MEM MB DATA9
				MB_DATA(8)	A14	MEM MB DATA8
				MB_DATA(7)	E13	MEM MB DATA7
				MB_DATA(6)	F13	MEM MB DATA6
				MB_DATA(5)	C15	MEM MB DATA5
				MB_DATA(4)	A15	MEM MB DATA4
				MB_DATA(3)	A13	MEM MB DATA3
				MB_DATA(2)	D13	MEM MB DATA2
				MB_DATA(1)		
				MB_DATA(0)		
				MB_DQS_H(7)	J31	X
				MB_DQS_L(7)	J30	X
				MB_DQS_H(6)	J29	X
				MB_DQS_L(6)		
				MB_DQS_H(5)		
				MB_DQS_L(5)		
				MB_DQS_H(4)		
				MB_DQS_L(4)		
				MB_DQS_H(3)		
				MB_DQS_L(3)		
				MB_DQS_H(2)		
				MB_DQS_L(2)		
				MB_DQS_H(1)		
				MB_DQS_L(1)		
				MB_DQS_H(0)		
				MB_DQS_L(0)		
				MB_DM(7)	K29	X
				MB_DM(6)	K31	X
				MB_DM(5)	G30	X
				MB_DM(4)	G29	X
				MB_DM(3)	L29	X
				MB_DM(2)	L28	X
				MB_DM(1)	H31	X
				MB_DM(0)	G31	X

ZIF-SOCK940-RH-1

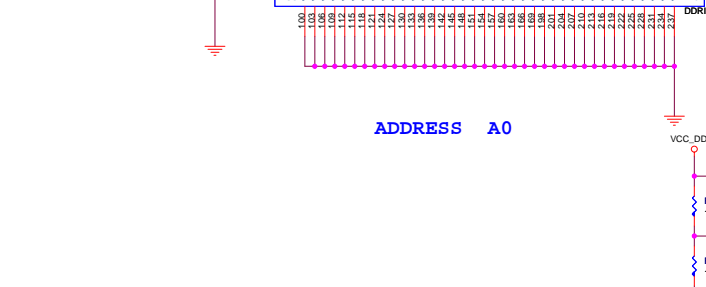
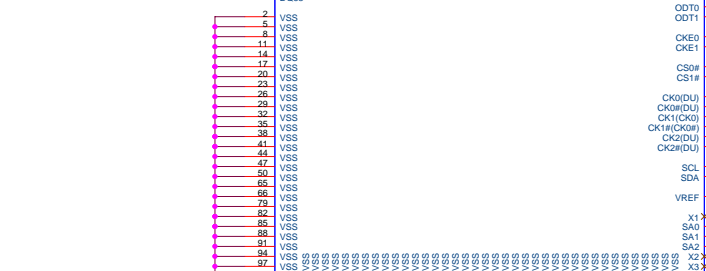
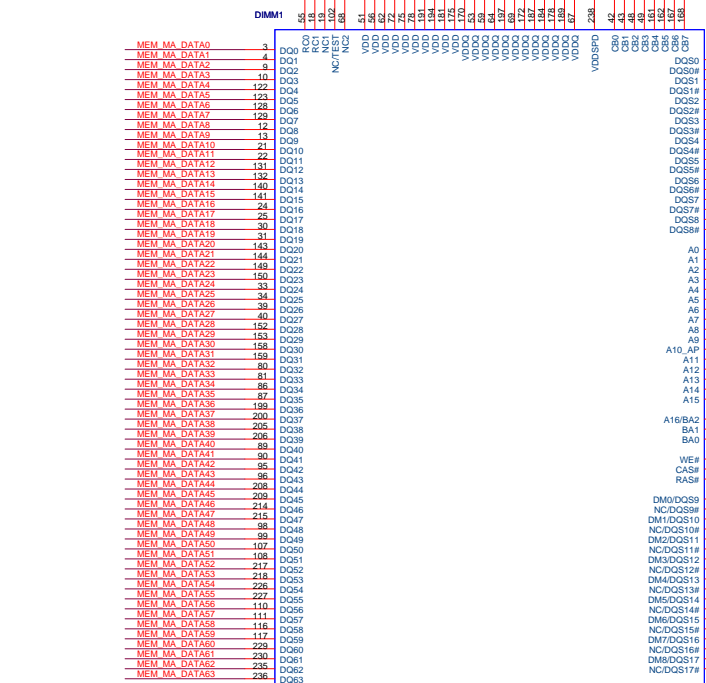


PLACE on CPU bottom side

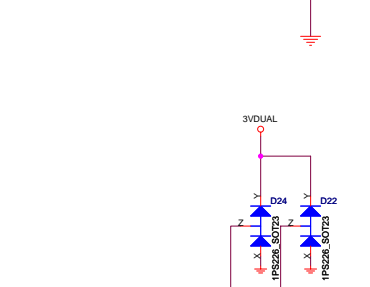
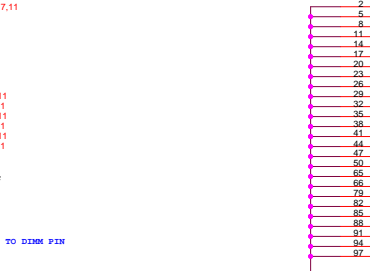
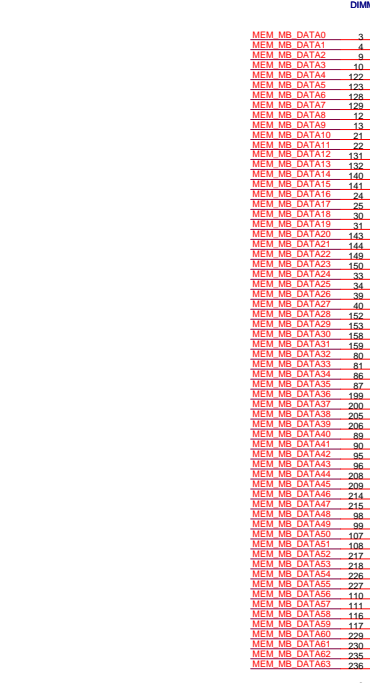




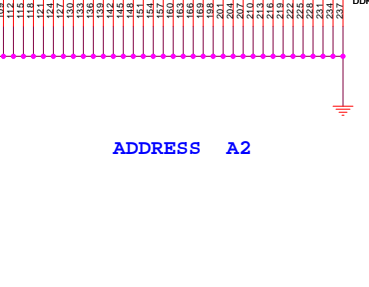
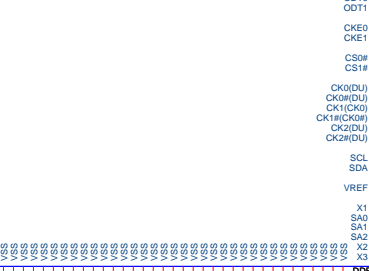
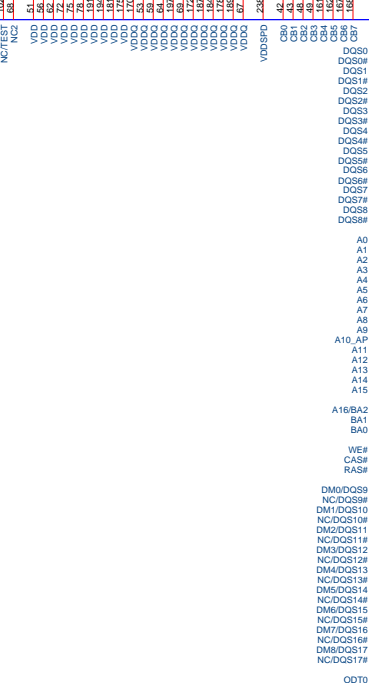
7,10 MEM\_MA\_DQS\_H[7..0] >>  
7,10 MEM\_MA\_DQS\_L[7..0] >>  
7,10 MEM\_MA\_DATA[63..0] >>  
7,10,11 MEM\_MA\_ADD[15..0] >>  
7,10 MEM\_MA\_DM[7..0] >>



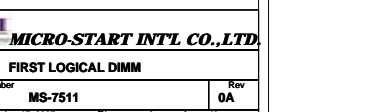
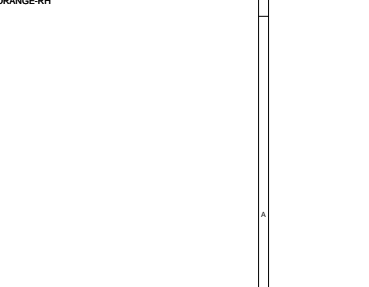
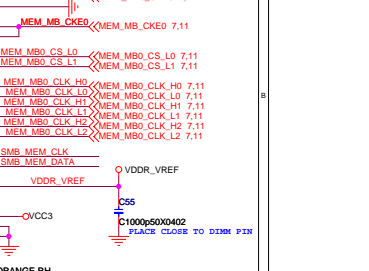
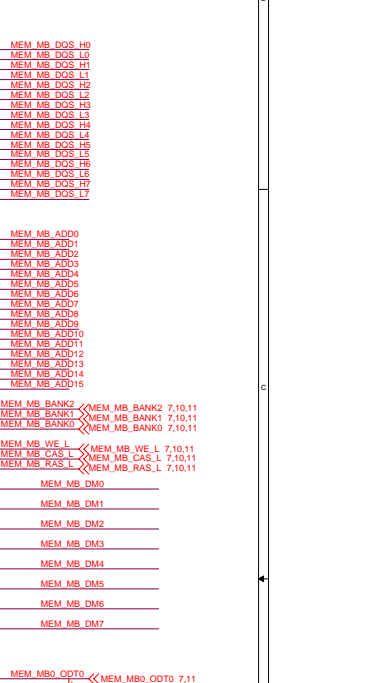
7,10 MEM\_MB\_DQS\_H[7..0] >>  
7,10 MEM\_MB\_DQS\_L[7..0] >>  
7,10 MEM\_MB\_DM[7..0] >>  
7,10 MEM\_MB\_DATA[63..0] >>  
7,10,11 MEM\_MB\_ADD[15..0] >>



7,10 MEM\_MB\_DQS\_H[7..0] >>  
7,10 MEM\_MB\_DQS\_L[7..0] >>  
7,10 MEM\_MB\_DM[7..0] >>  
7,10 MEM\_MB\_DATA[63..0] >>  
7,10,11 MEM\_MB\_ADD[15..0] >>

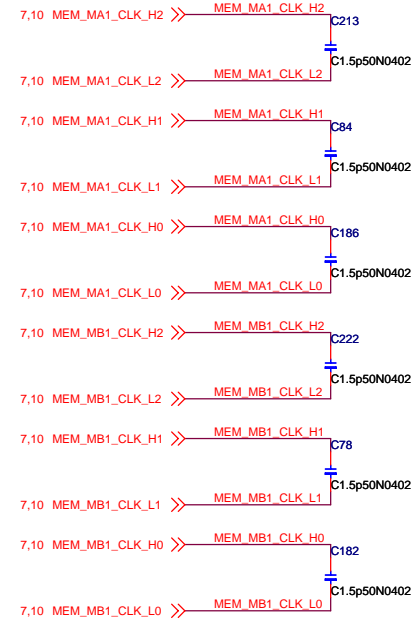
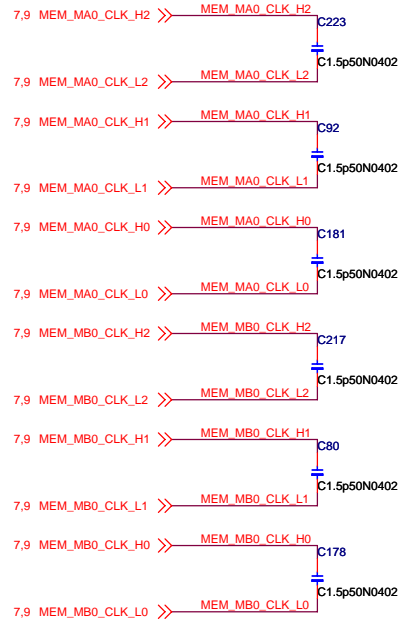
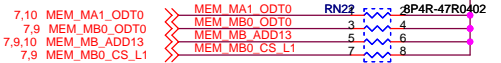
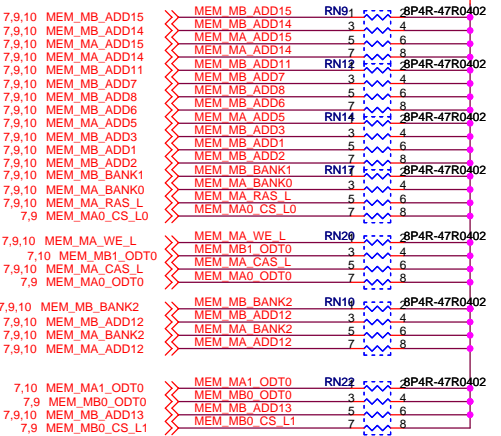
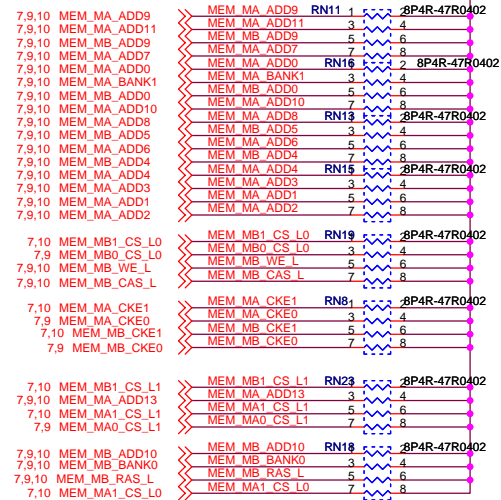


7,10 MEM\_MB\_DQS\_H[7..0] >>  
7,10 MEM\_MB\_DQS\_L[7..0] >>  
7,10 MEM\_MB\_DM[7..0] >>  
7,10 MEM\_MB\_DATA[63..0] >>  
7,10,11 MEM\_MB\_ADD[15..0] >>

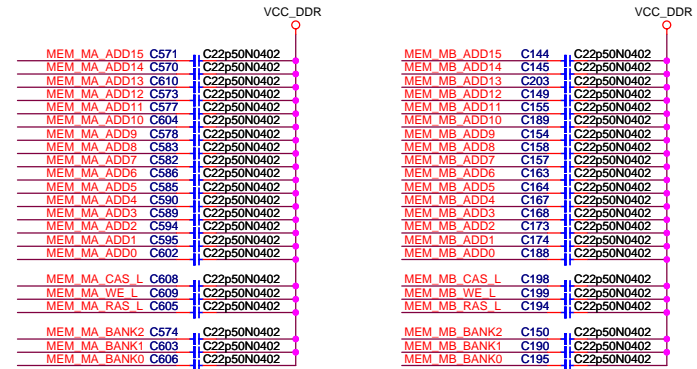




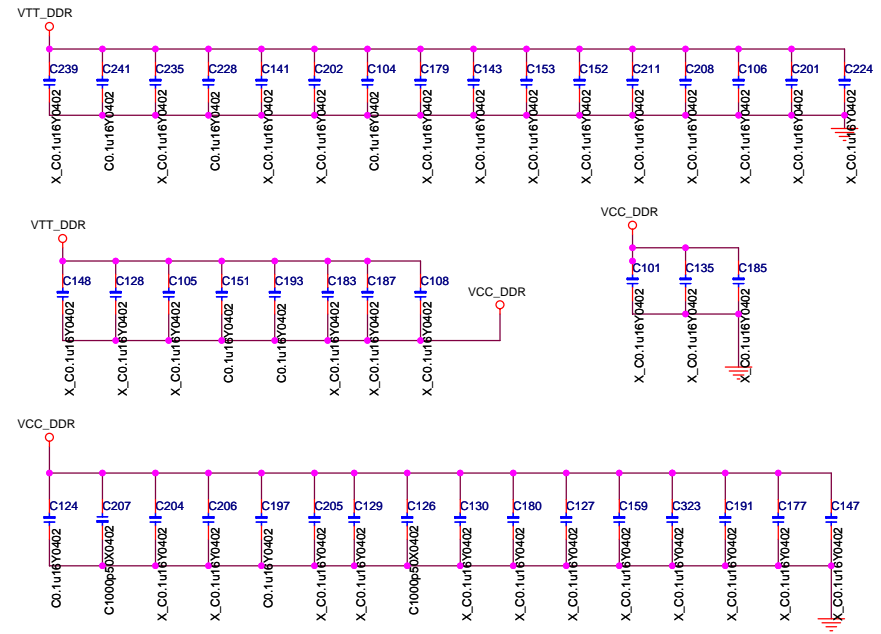
## RTT:Place Behind DIMMs<sup>VTT\_DDR</sup>




## Place Between Processor and DIMMs



Layout: Spread out on VTT pour



for EMI

 <b>MICRO-START INT'L CO.,LTD.</b>			
Title			
DDR TERMINATOR			
Size	Document Number	Rev	
	MS-5711	0A	
Date:	Monday, December 17, 2007	Sheet	11 of 40

6 HT\_CADIN\_H[15..0] >> HT\_CADIN\_H[15..0]  
6 HT\_CADIN\_L[15..0] >> HT\_CADIN\_L[15..0]  
6 HT\_CADOUT\_H[15..0] >> HT\_CADOUT\_H[15..0]  
6 HT\_CADOUT\_L[15..0] >> HT\_CADOUT\_L[15..0]

U21A

SEC 1 OF 8

HT_CADOUT_H0	AG8	HT_MCP_RXD0_P	HT_MCP_TXD0_P	AH23	HT_CADIN_H0
HT_CADOUT_H1	AG9	HT_MCP_RXD1_P	HT_MCP_TXD1_P	AH22	HT_CADIN_H1
HT_CADOUT_H2	AK9	HT_MCP_RXD2_P	HT_MCP_TXD2_P	AJ21	HT_CADIN_H2
HT_CADOUT_H3	AJ10	HT_MCP_RXD3_P	HT_MCP_TXD3_P	AH21	HT_CADIN_H3
HT_CADOUT_H4	AG12	HT_MCP_RXD4_P	HT_MCP_TXD4_P	AH19	HT_CADIN_H4
HT_CADOUT_H5	AG13	HT_MCP_RXD5_P	HT_MCP_TXD5_P	AH18	HT_CADIN_H5
HT_CADOUT_H6	AK13	HT_MCP_RXD6_P	HT_MCP_TXD6_P	AJ17	HT_CADIN_H6
HT_CADOUT_H7	AJ14	HT_MCP_RXD7_P	HT_MCP_TXD7_P	AH17	HT_CADIN_H7
HT_CADOUT_H8	AB10	HT_MCP_RXD8_P	HT_MCP_TXD8_P	AF22	HT_CADIN_H8
HT_CADOUT_H9	AD10	HT_MCP_RXD9_P	HT_MCP_TXD9_P	AB20	HT_CADIN_H9
HT_CADOUT_H10	AF10	HT_MCP_RXD10_P	HT_MCP_TXD10_P	AC20	HT_CADIN_H10
HT_CADOUT_H11	AC12	HT_MCP_RXD11_P	HT_MCP_TXD11_P	AE20	HT_CADIN_H11
HT_CADOUT_H12	AB11	HT_MCP_RXD12_P	HT_MCP_TXD12_P	AD18	HT_CADIN_H12
HT_CADOUT_H13	AB13	HT_MCP_RXD13_P	HT_MCP_TXD13_P	AF18	HT_CADIN_H13
HT_CADOUT_H14	AF14	HT_MCP_RXD14_P	HT_MCP_TXD14_P	AB17	HT_CADIN_H14
HT_CADOUT_H15	AE14	HT_MCP_RXD15_P	HT_MCP_TXD15_P	AC16	HT_CADIN_H15
HT_CADOUT_L0	AH8	HT_MCP_RXD0_N	HT_MCP_TXD0_N	AJ23	HT_CADIN_L0
HT_CADOUT_L1	AH9	HT_MCP_RXD1_N	HT_MCP_TXD1_N	AJ22	HT_CADIN_L1
HT_CADOUT_L2	AJ9	HT_MCP_RXD2_N	HT_MCP_TXD2_N	AK21	HT_CADIN_L2
HT_CADOUT_L3	AH10	HT_MCP_RXD3_N	HT_MCP_TXD3_N	AG21	HT_CADIN_L3
HT_CADOUT_L4	AH12	HT_MCP_RXD4_N	HT_MCP_TXD4_N	AJ19	HT_CADIN_L4
HT_CADOUT_L5	AH13	HT_MCP_RXD5_N	HT_MCP_TXD5_N	AJ18	HT_CADIN_L5
HT_CADOUT_L6	AJ13	HT_MCP_RXD6_N	HT_MCP_TXD6_N	AK17	HT_CADIN_L6
HT_CADOUT_L7	AH14	HT_MCP_RXD7_N	HT_MCP_TXD7_N	AG17	HT_CADIN_L7
HT_CADOUT_L8	AC10	HT_MCP_RXD8_N	HT_MCP_TXD8_N	AG22	HT_CADIN_L8
HT_CADOUT_L9	AE10	HT_MCP_RXD9_N	HT_MCP_TXD9_N	AB19	HT_CADIN_L9
HT_CADOUT_L10	AG10	HT_MCP_RXD10_N	HT_MCP_TXD10_N	AD20	HT_CADIN_L10
HT_CADOUT_L11	AD12	HT_MCP_RXD11_N	HT_MCP_TXD11_N	AE20	HT_CADIN_L11
HT_CADOUT_L12	AC11	HT_MCP_RXD12_N	HT_MCP_TXD12_N	AE18	HT_CADIN_L12
HT_CADOUT_L13	AB12	HT_MCP_RXD13_N	HT_MCP_TXD13_N	AG18	HT_CADIN_L13
HT_CADOUT_L14	AG14	HT_MCP_RXD14_N	HT_MCP_TXD14_N	AB16	HT_CADIN_L14
HT_CADOUT_L15	AD14	HT_MCP_RXD15_N	HT_MCP_TXD15_N	AD16	HT_CADIN_L15

6 HT\_CLKOUT\_H0 >> AJ11 HT\_MCP\_RX\_CLK0\_P  
6 HT\_CLKOUT\_L0 >> AH11 HT\_MCP\_RX\_CLK0\_N  
6 HT\_CLKOUT\_H1 >> AE12 HT\_MCP\_RX\_CLK1\_P  
6 HT\_CLKOUT\_L1 >> AE12 HT\_MCP\_RX\_CLK1\_N

6 HT\_CTOUT\_H0 >> AJ15 HT\_MCP\_RXCTL0\_P  
6 HT\_CTOUT\_L0 >> AH15 HT\_MCP\_RXCTL0\_N  
6 HT\_CTOUT\_H1 >> AB14 RESERVED35  
6 HT\_CTOUT\_L1 >> AC14 RESERVED36

HT\_MCP\_TX\_CLK0\_P >> AH20 HT\_CLKIN\_H0 6  
HT\_MCP\_TX\_CLK0\_N >> AG20 HT\_CLKIN\_L0 6  
HT\_MCP\_TX\_CLK1\_P >> AC18 HT\_CLKIN\_H1 6  
HT\_MCP\_TX\_CLK1\_N >> AB18 HT\_CLKIN\_L1 6

HT\_MCP\_TXCTL0\_P >> AH16 HT\_CTLIN\_H0 6  
HT\_MCP\_TXCTL0\_N >> AG16 HT\_CTLIN\_L0 6  
RESERVED35 >> AE16 HT\_CTLIN\_H1 6  
RESERVED36 >> AF16 HT\_CTLIN\_L1 6

HT\_MCP\_REQ# >> AH25 HT\_MCP\_REQ# R194 10KR0402  
HT\_MCP\_STOP# >> AH24 >> LDT\_STOP# 6  
HT\_MCP\_RST# >> AG23 >> LDT\_RST# 6  
HT\_MCP\_PWRGD >> AG24 >> LDT\_PWRGD 6,31,32

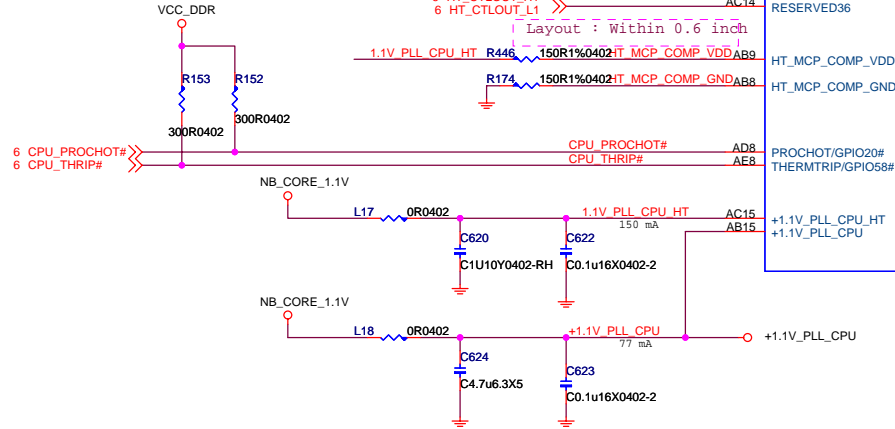
CLKOUT\_200MHZ\_P >> AK25 >> CPU\_CLK 6  
CLKOUT\_200MHZ\_N >> AJ25 >> CPU\_CLK# 6

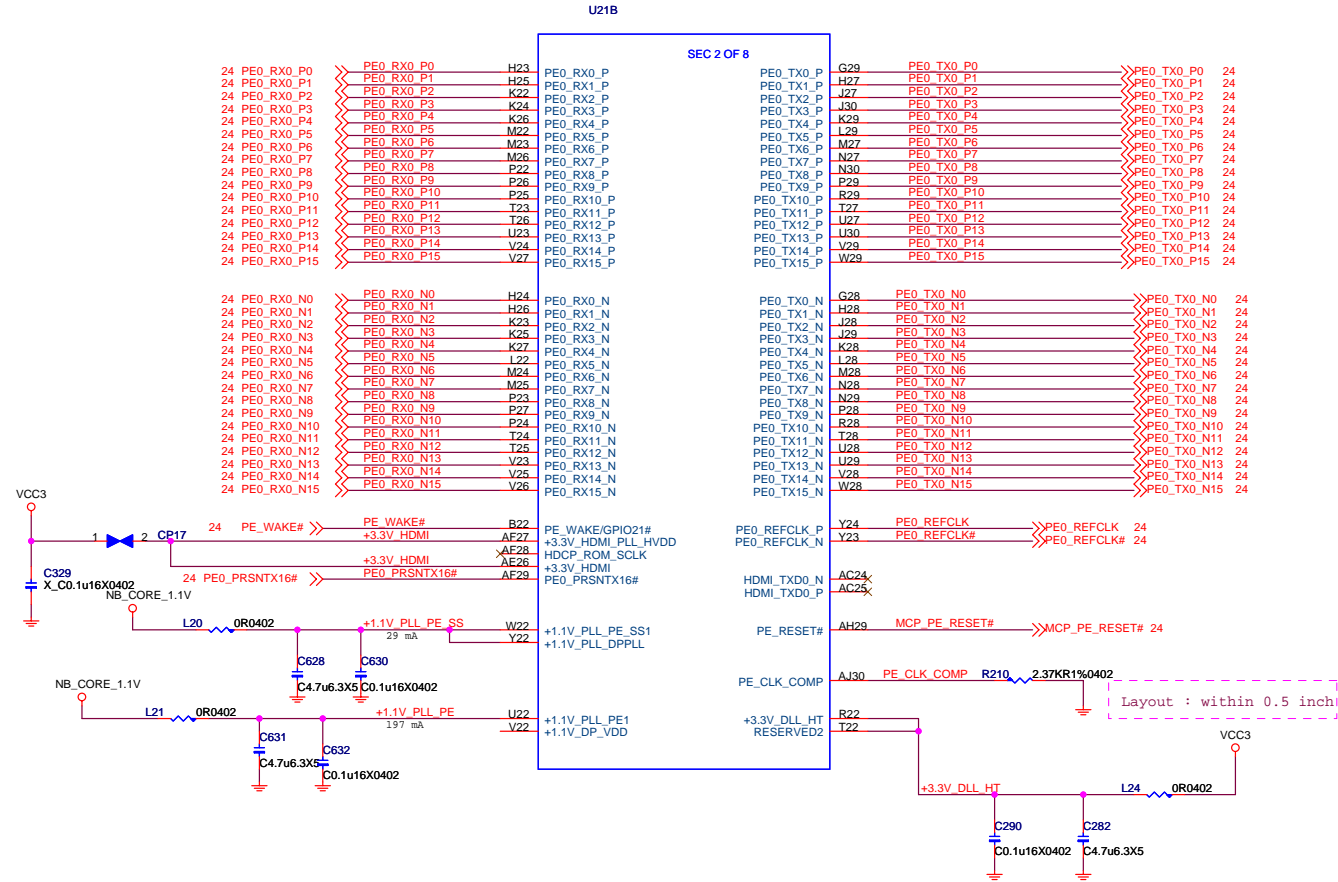
CPU\_SBVREF >> AF24  
CLKOUT\_25MHZ >> AK28  
CLK200\_TERM\_GND >> AJ26 CLK200\_TERM\_GNDR201 2.37KR1%0402

VCC3

NB\_CORE\_1.1V

C301  
C0.1u16X0402-2

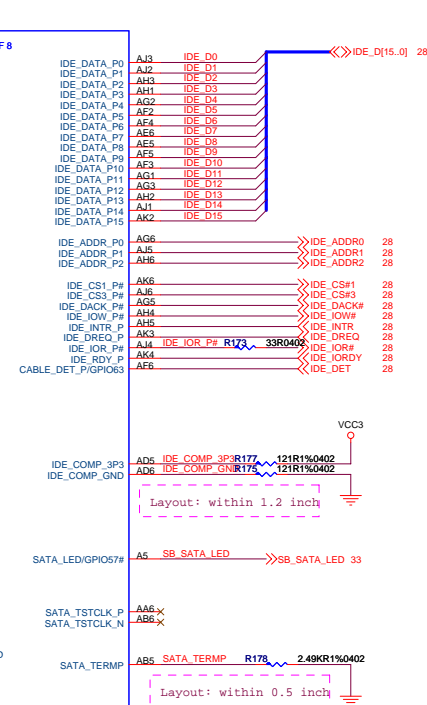
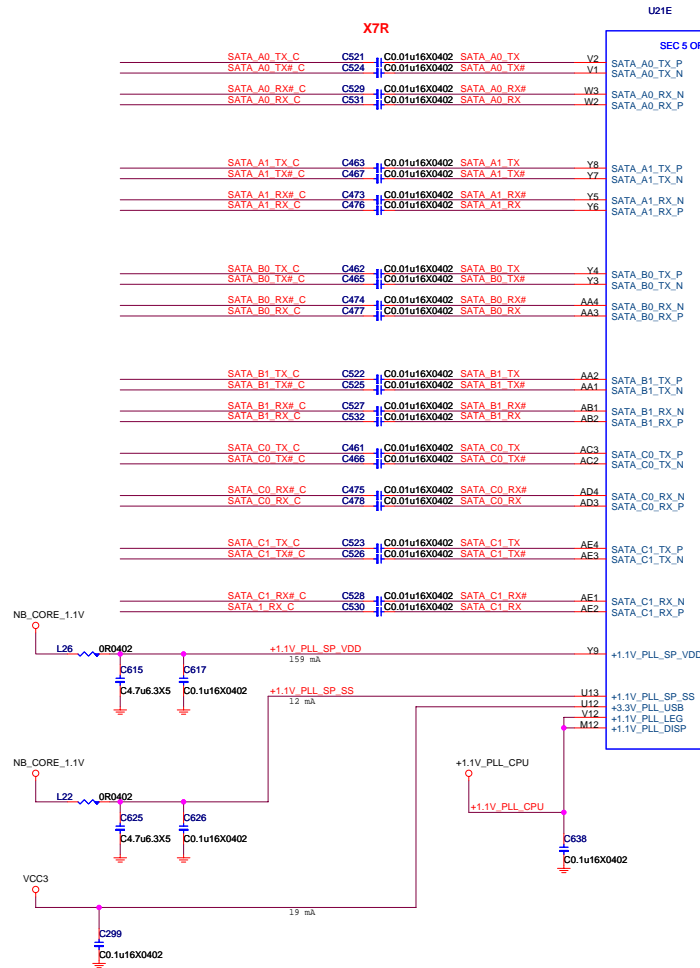
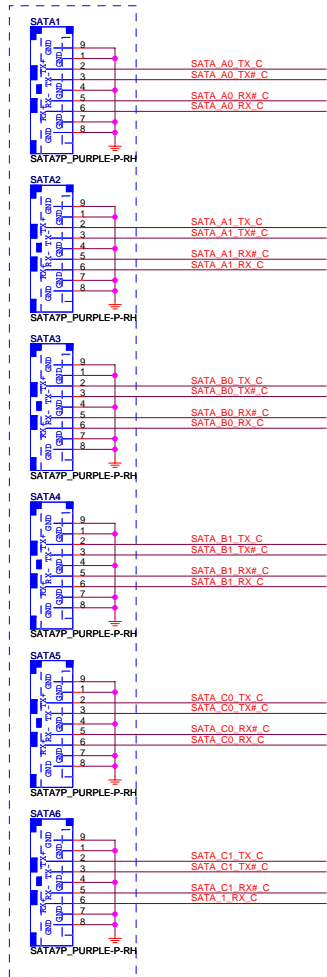






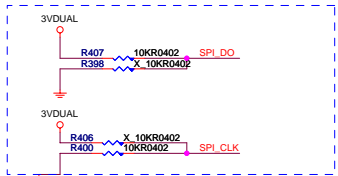
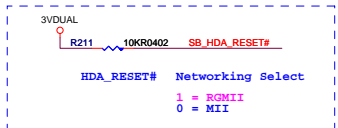
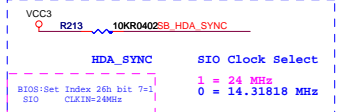
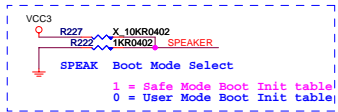




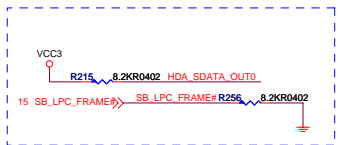




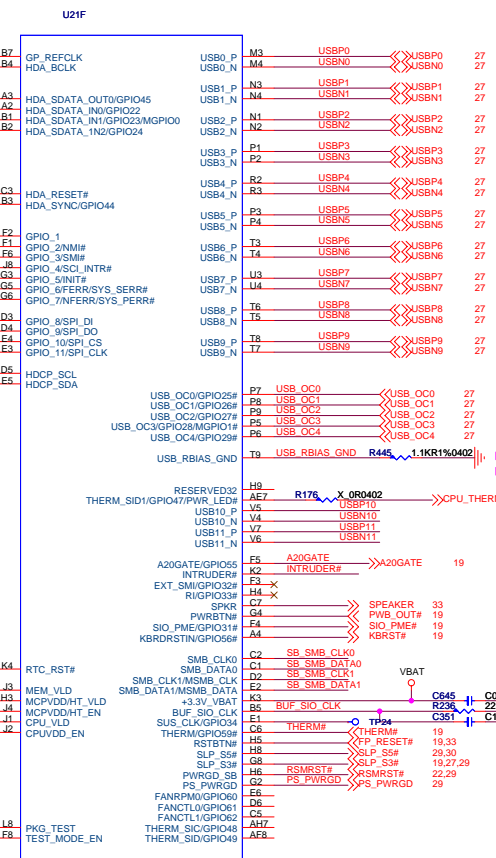
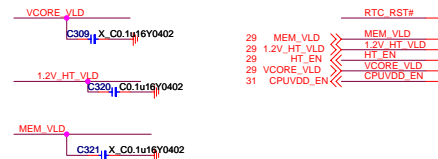
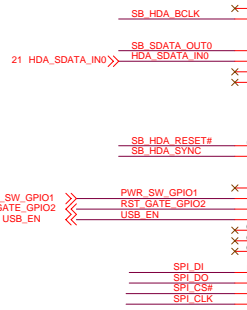
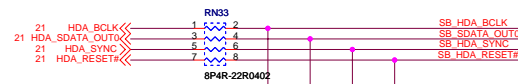
## STRAPPING PIN

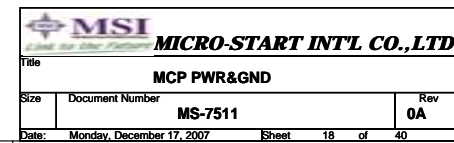
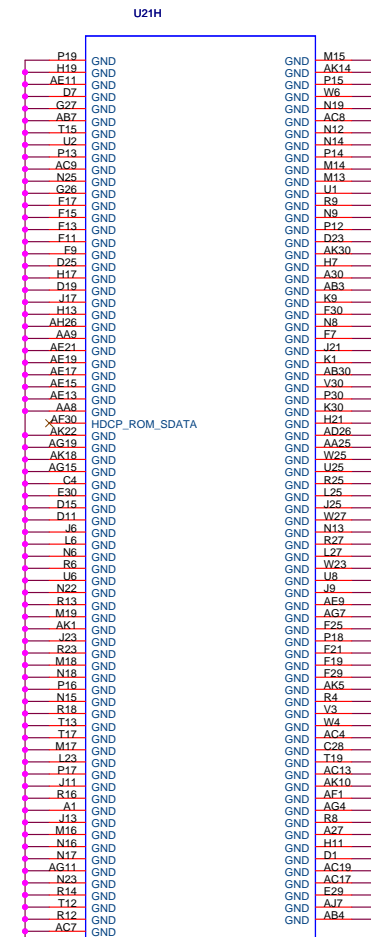


SPI Clock Freq. Select	SPI_DO/GPIO9	SPI_CLK/GPIO11
31 MHz	0	0
Reserved	0	1
25 MHz	1	0
1 MHz	1	1

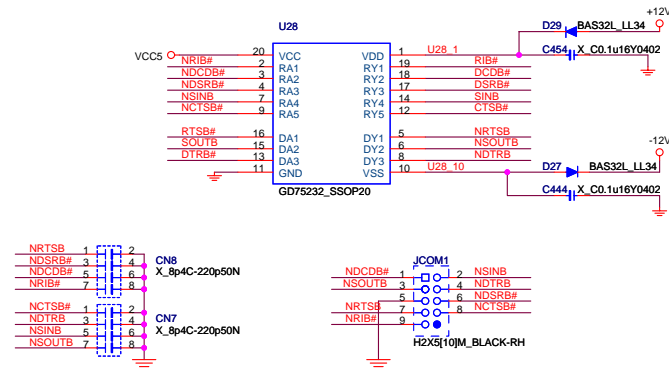
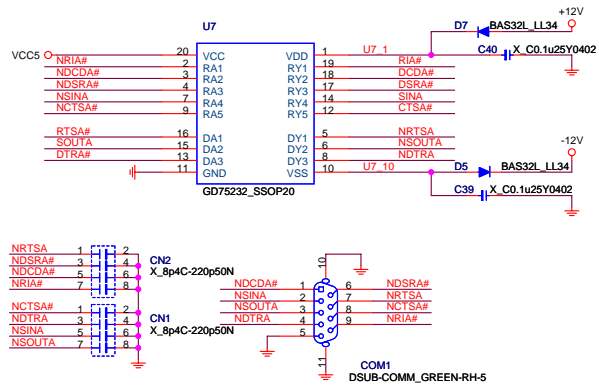


BIOS Select	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS	1	0
Reserved (SPI)	1	1

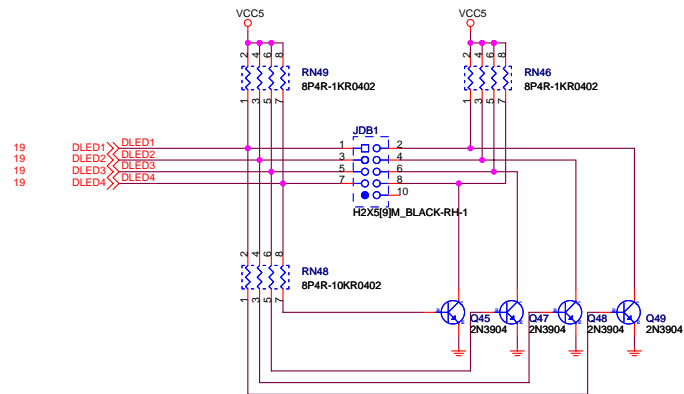
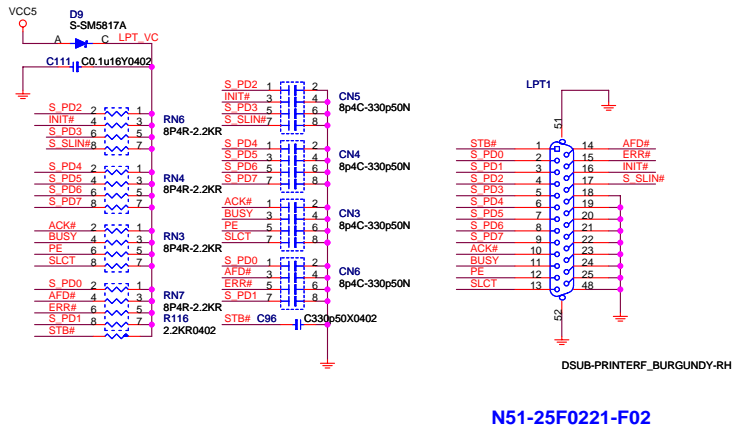




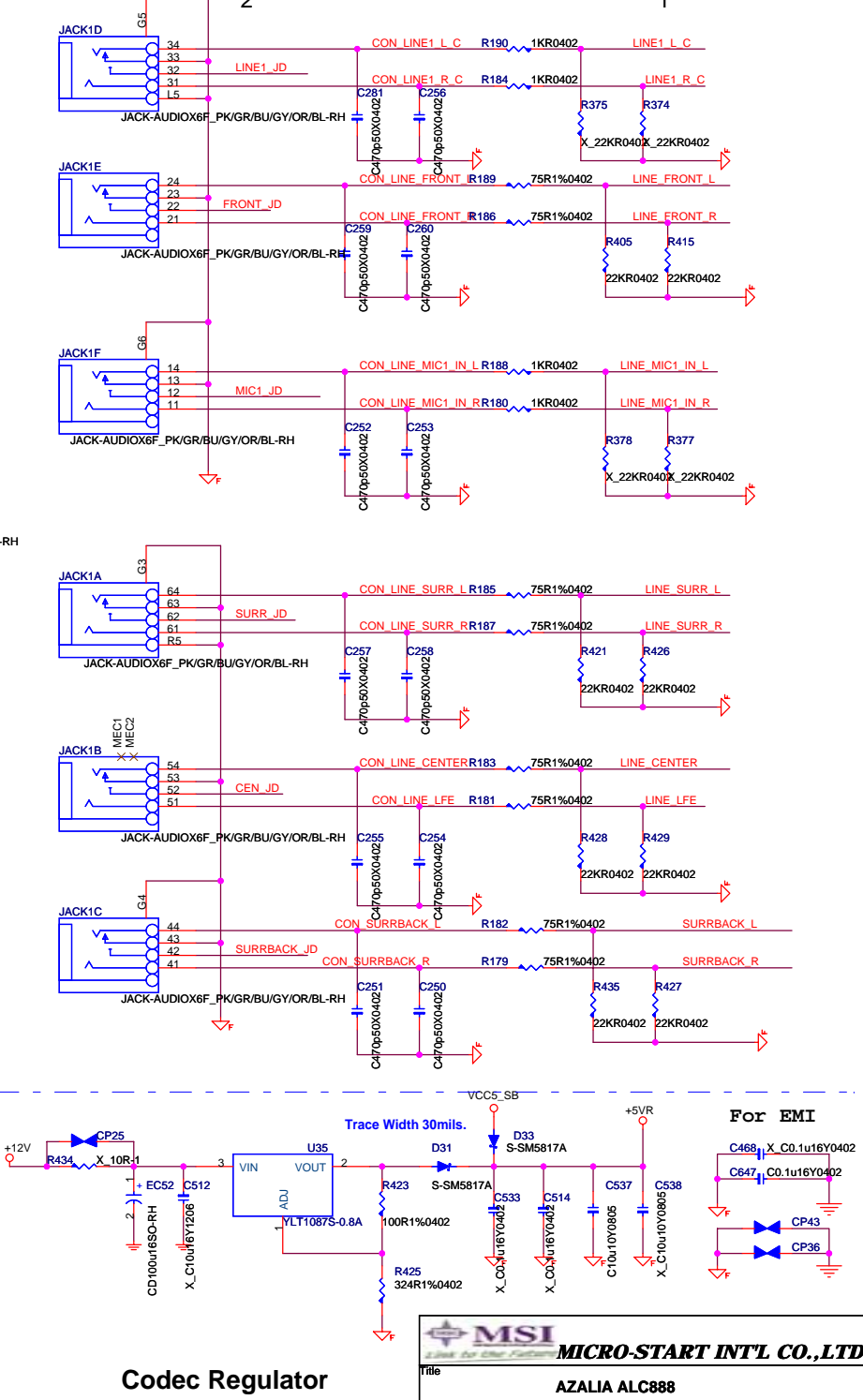
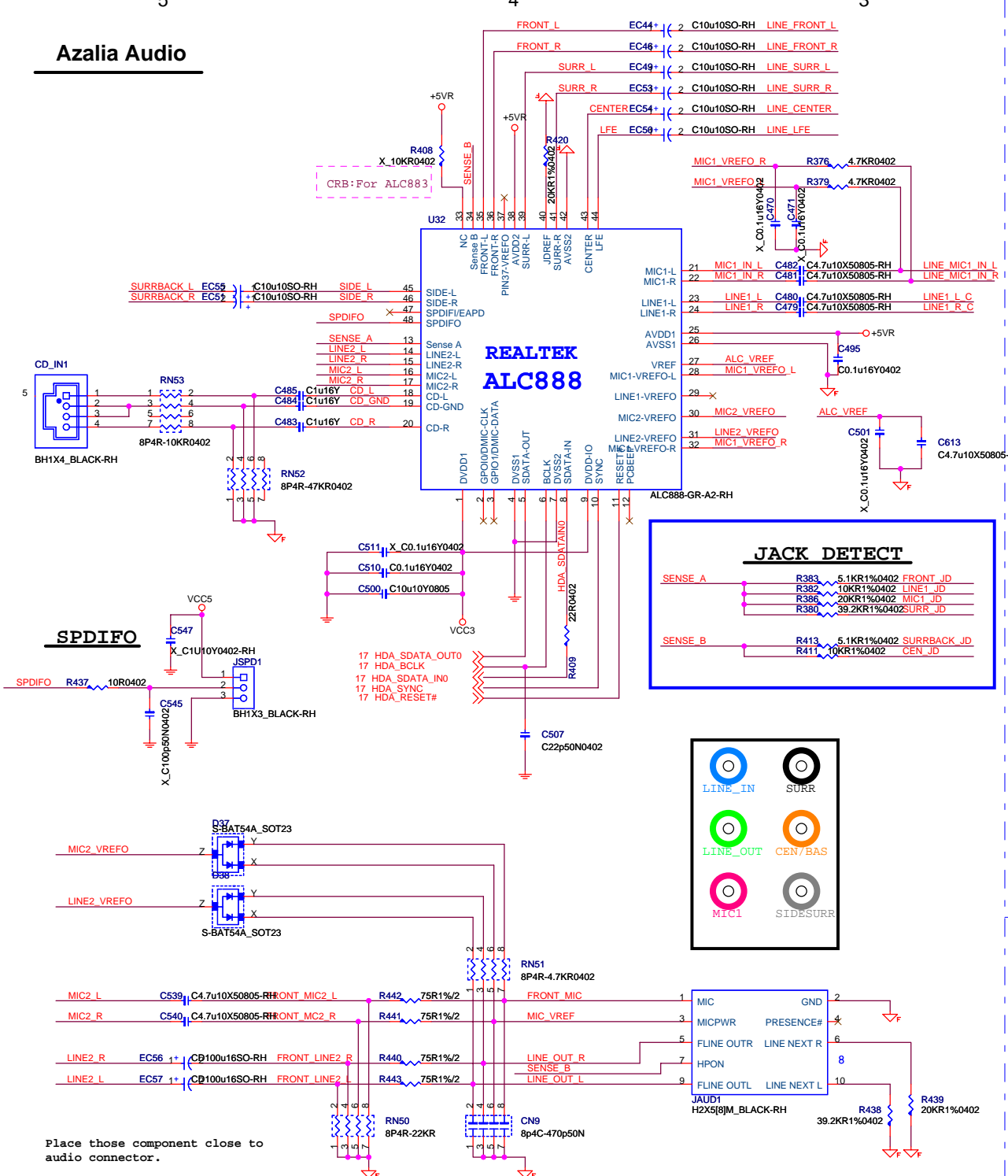


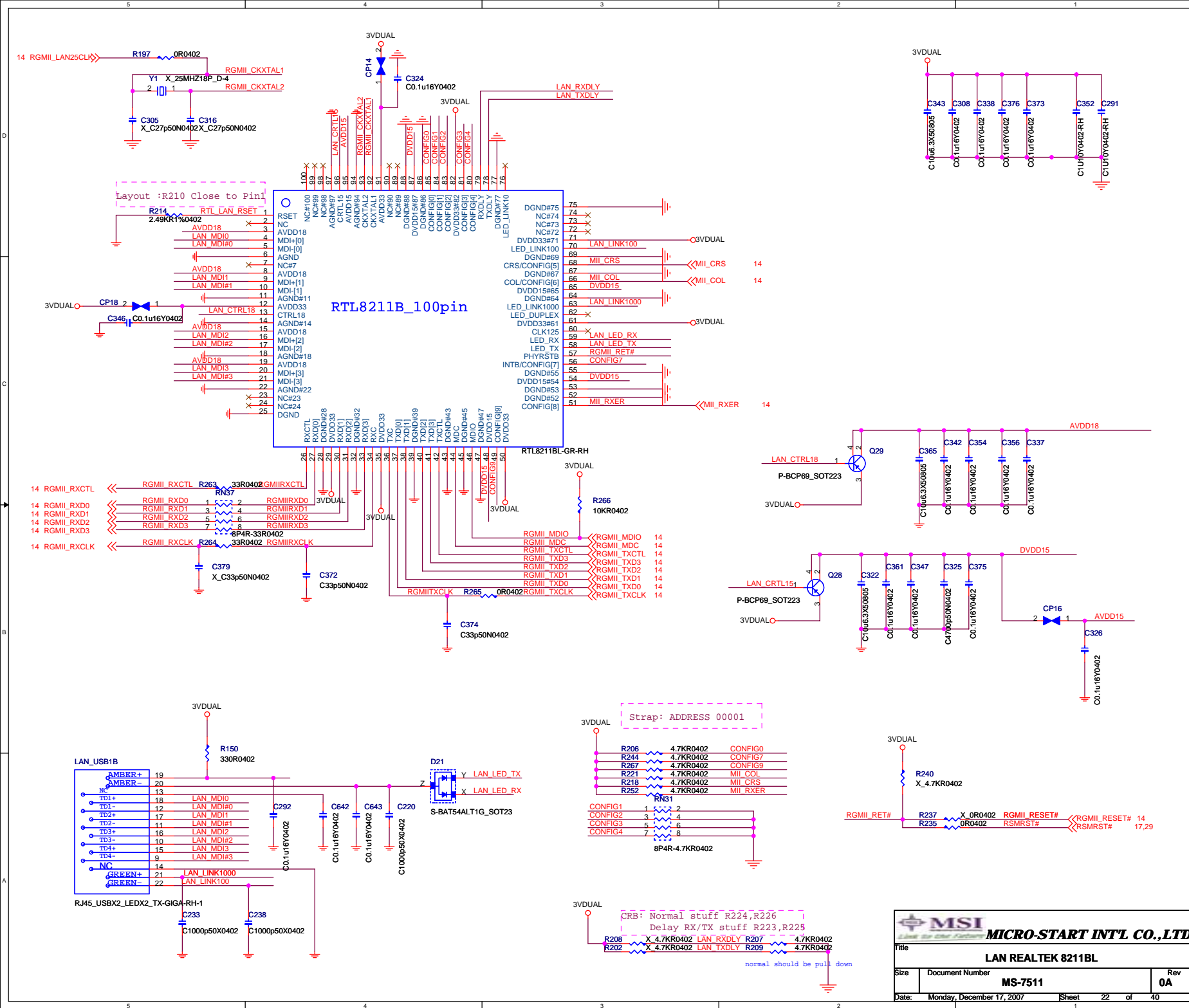


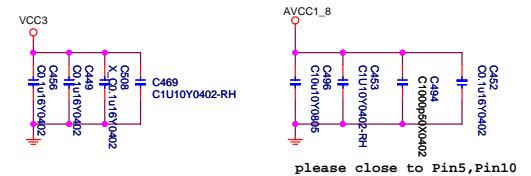
SLCT	SLCT	19
BUSY	BUSY	19
ACK#	ACK#	19
S_SLN#	S_SLN#	19
INT#	INT#	19
ERR#	ERR#	19
AFD#	AFD#	19
STB#	STB#	19
S_PD0	S_PD0	19
S_PD1	S_PD1	19
S_PD2	S_PD2	19
S_PD3	S_PD3	19
S_PD4	S_PD4	19
S_PD5	S_PD5	19
S_PD6	S_PD6	19
S_PD7	S_PD7	19
DCDA#	DCDA#	19
RIA#	RIA#	19
CTSA#	CTSA#	19
DTRA#	DTRA#	19
RTSA#	RTSA#	19
DSRA#	DSRA#	19
SOUTA	SOUTA	19
SINA	SINA	19
DCDB#	DCDB#	19
RIB#	RIB#	19
CTSB#	CTSB#	19
DTRB#	DTRB#	19
RTSB#	RTSB#	19
DSRB#	DSRB#	19
SOUTB	SOUTB	19
SINB	SINB	19



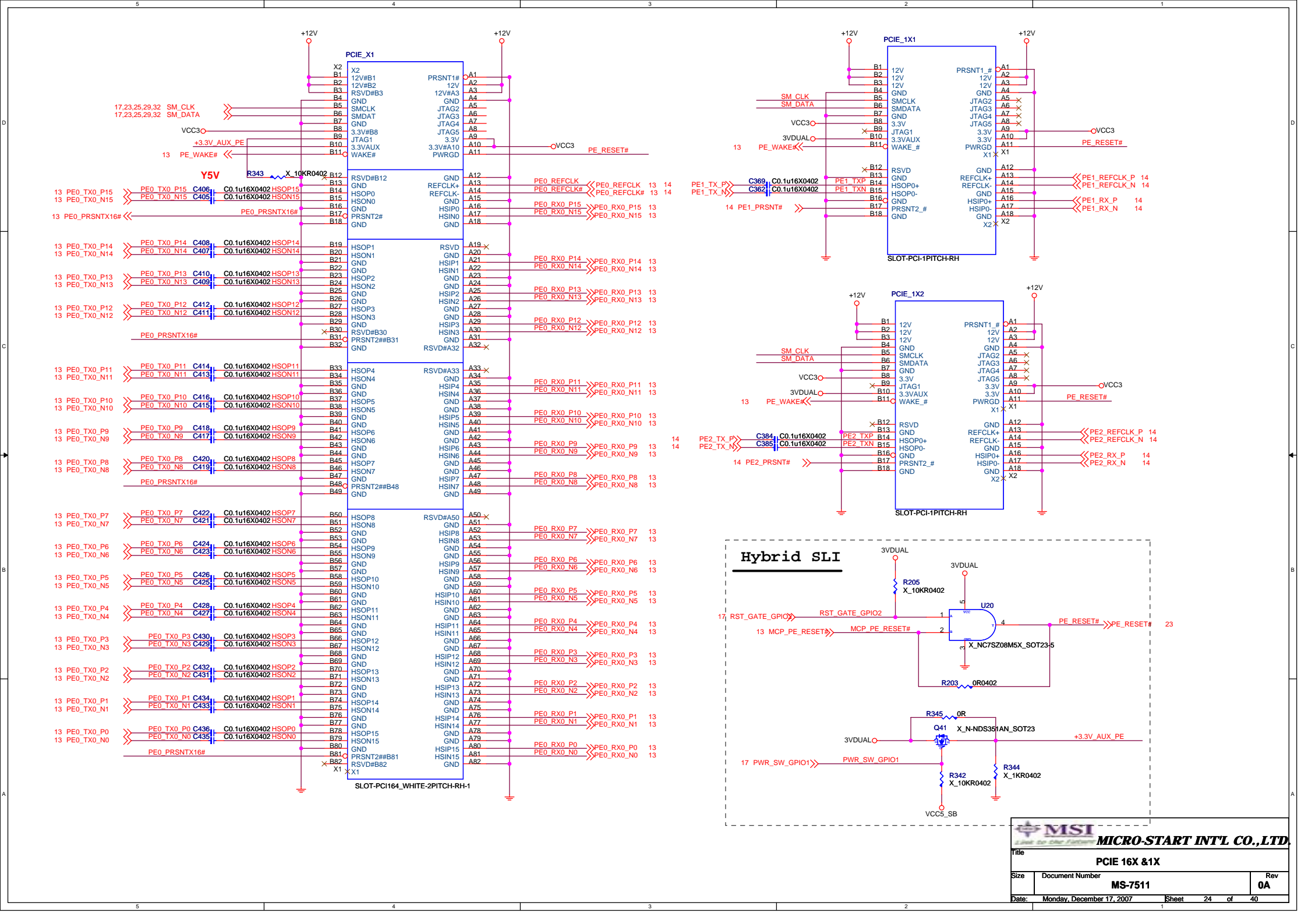
# Azalia Audio





[illegible][illegible]

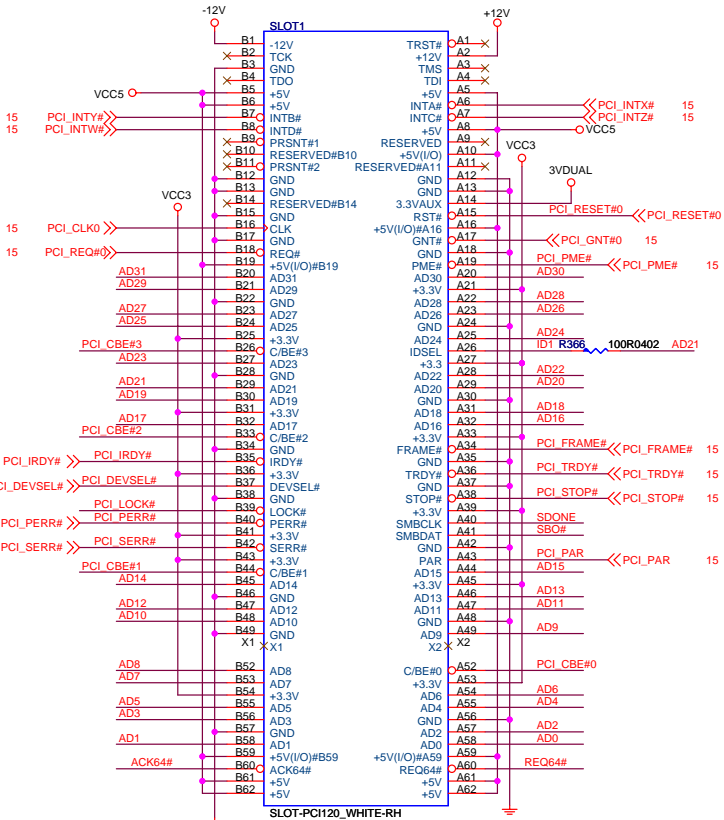






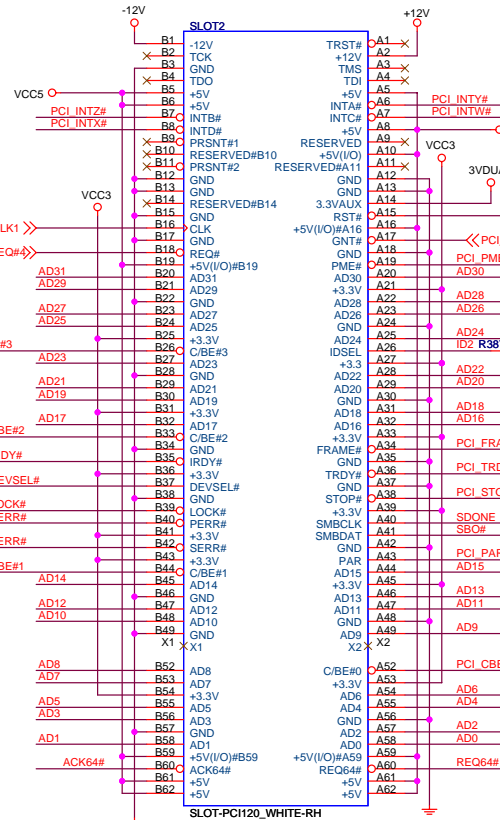
15 AD[31..0] >> AD[31..0]  
15 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

### PCI SLOT 1 (PCI VER: 2.3 COMPLY)



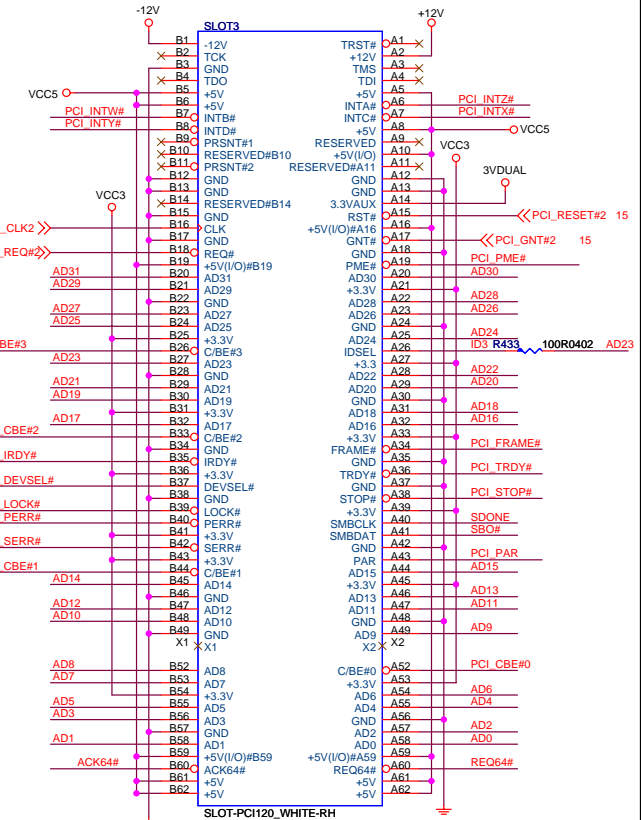
IDSEL = AD21  
MASTER = PCI\_REQ#0  
PCI\_GNT#0  
PCI\_INTX#

### PCI SLOT 2 (PCI VER: 2.3 COMPLY)



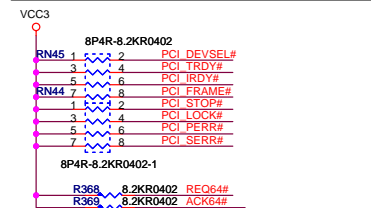
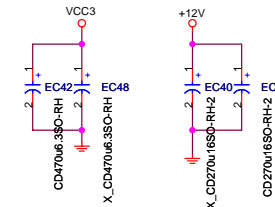
IDSEL = AD22  
MASTER = PCI\_REQ#1  
PCI\_GNT#1  
PCI\_INTY#

### PCI SLOT 2 (PCI VER: 2.3 COMPLY)



IDSEL = AD23  
MASTER = PCI\_REQ#2  
PCI\_GNT#2  
PCI\_INTZ#

### PCI PULL-UP / DOWN RESISTORS



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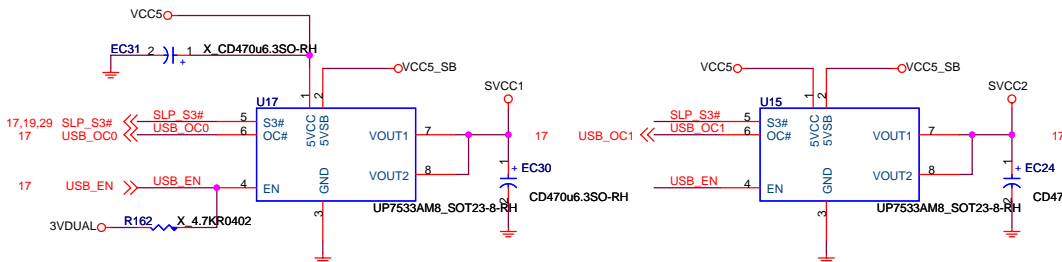
Title: **PCI SLOT**

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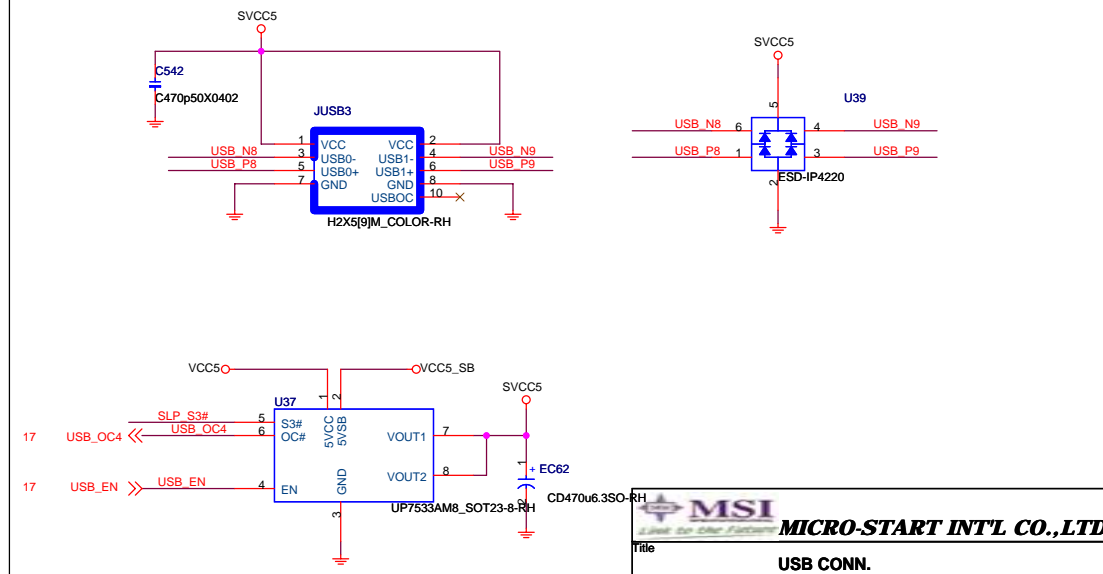
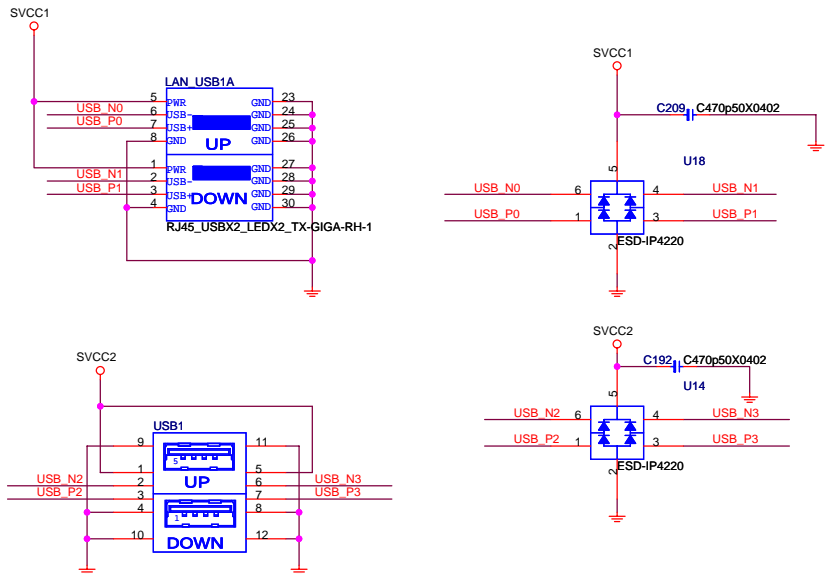
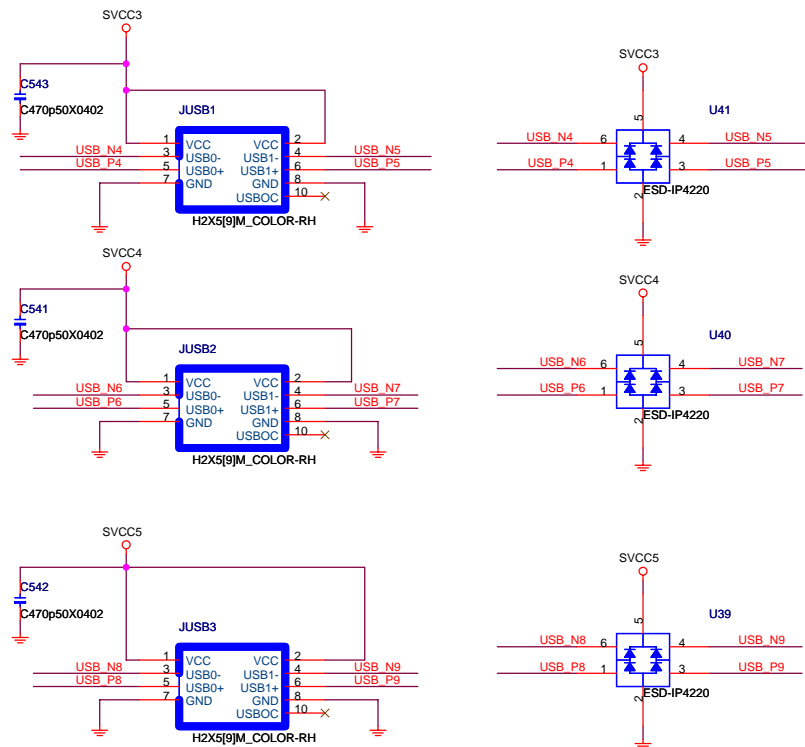
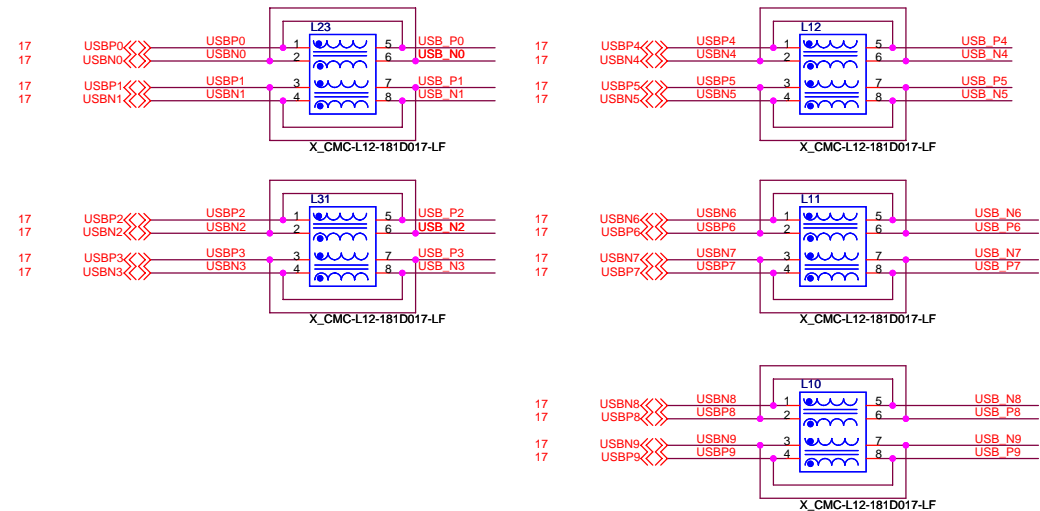
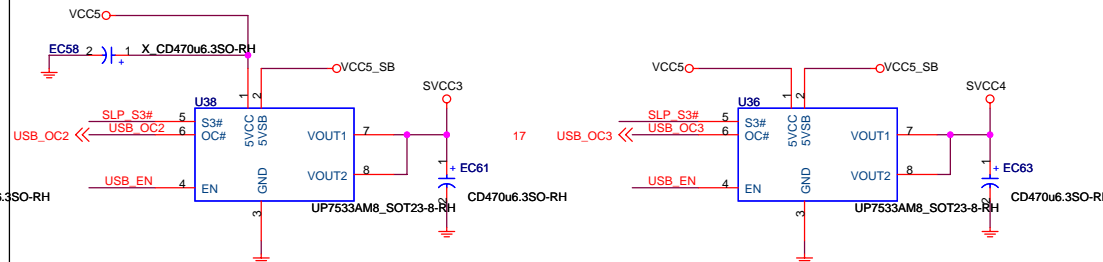
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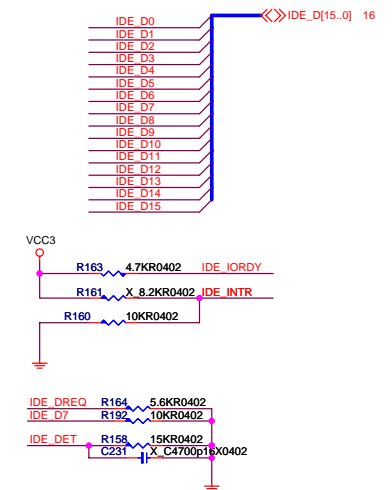
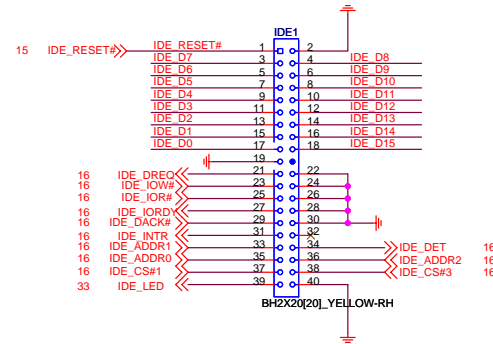
# Rear USB power



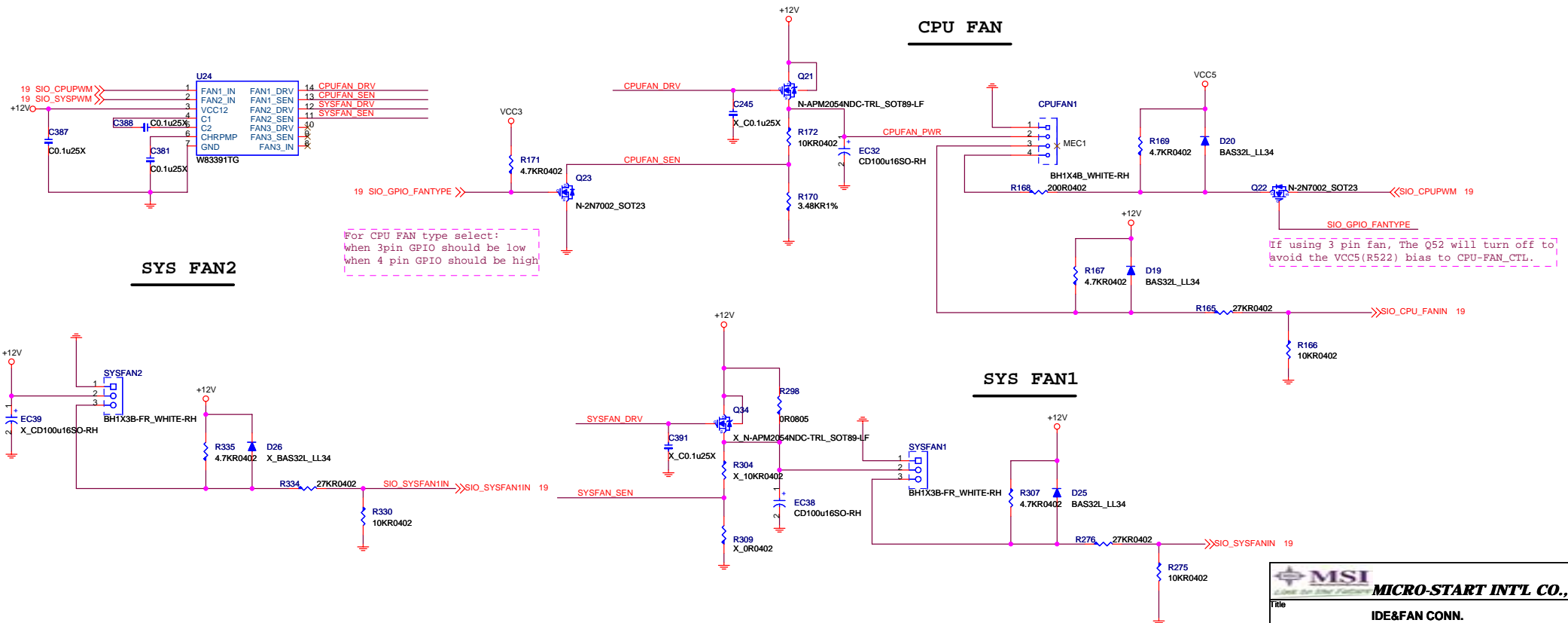
# front USB power



## IDE CONNECTOR

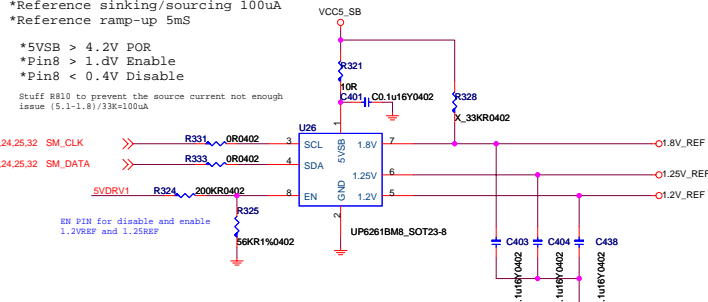


## FAN CONNECTOR

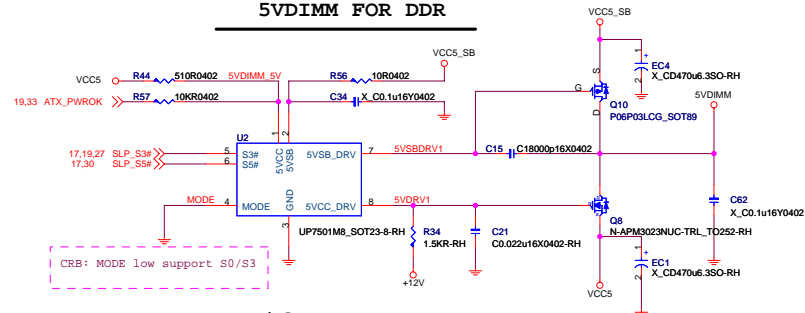


## REFERENCE VOLTAGE

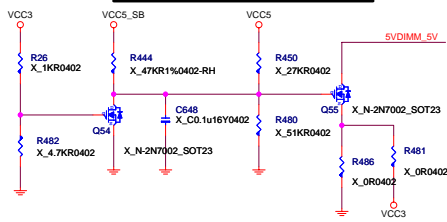
\*Reference sinking/sourcing 100uA  
 \*Reference ramp-up 5mS  
 \*5VSB > 4.2V POR  
 \*Pin8 > 1.0V Enable  
 \*Pin8 < 0.4V Disable  
 Stuff R810 to prevent the source current not enough issue (5.1-1.8)/33K=100uA



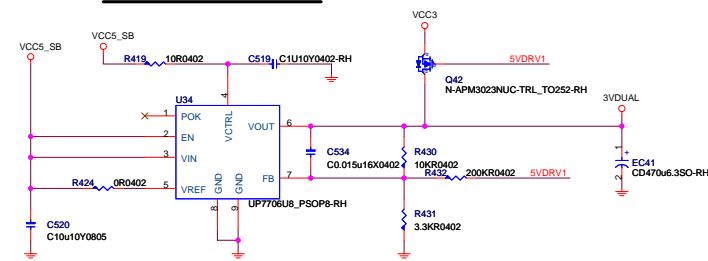
## 5VDIMM FOR DDR



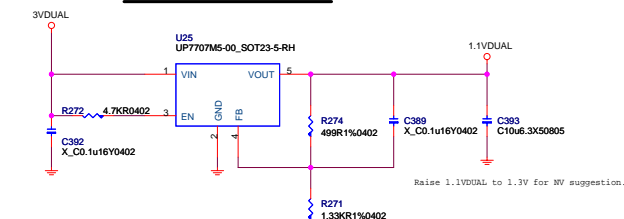
## For special PSU sequence



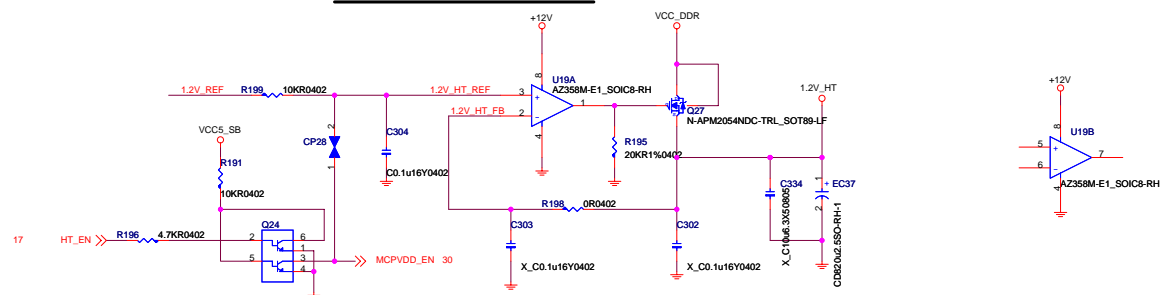
## 3VDUAL POWER



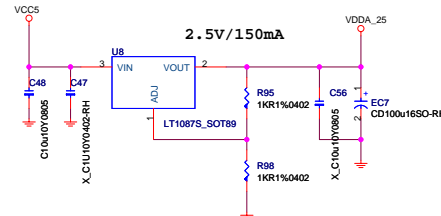
## 1.1DUAL POWER



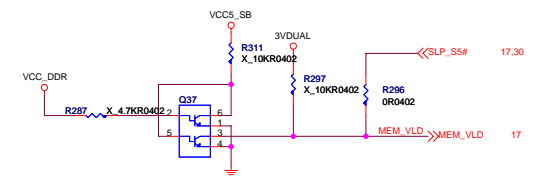
## 1.2V\_HT POWER



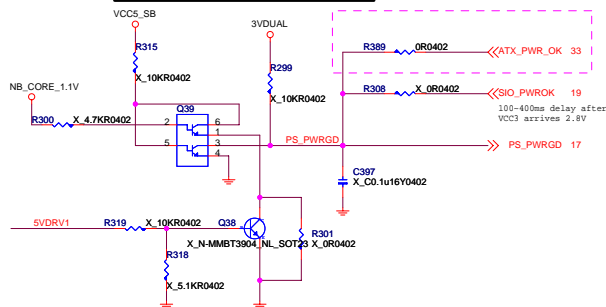
## VDDA\_25 POWER



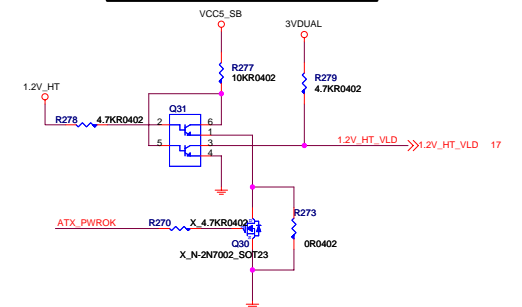
## MEM\_VLD CIRCUIT



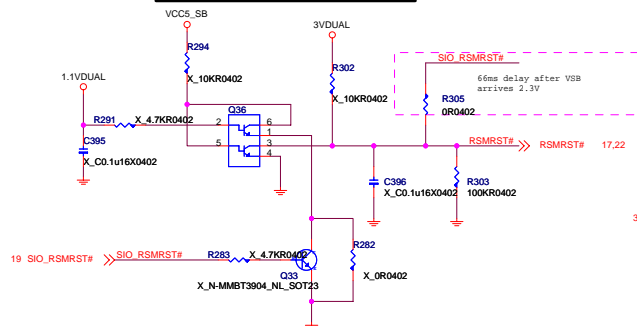
## PS\_PWRGD CIRCUIT



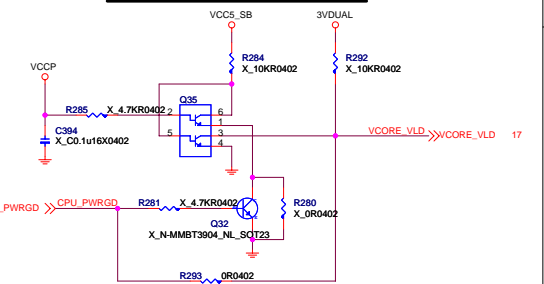
## 1.2V\_HT\_VLD CIRCUIT



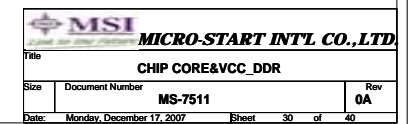
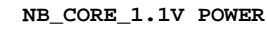
## PWRGD\_SB CIRCUIT

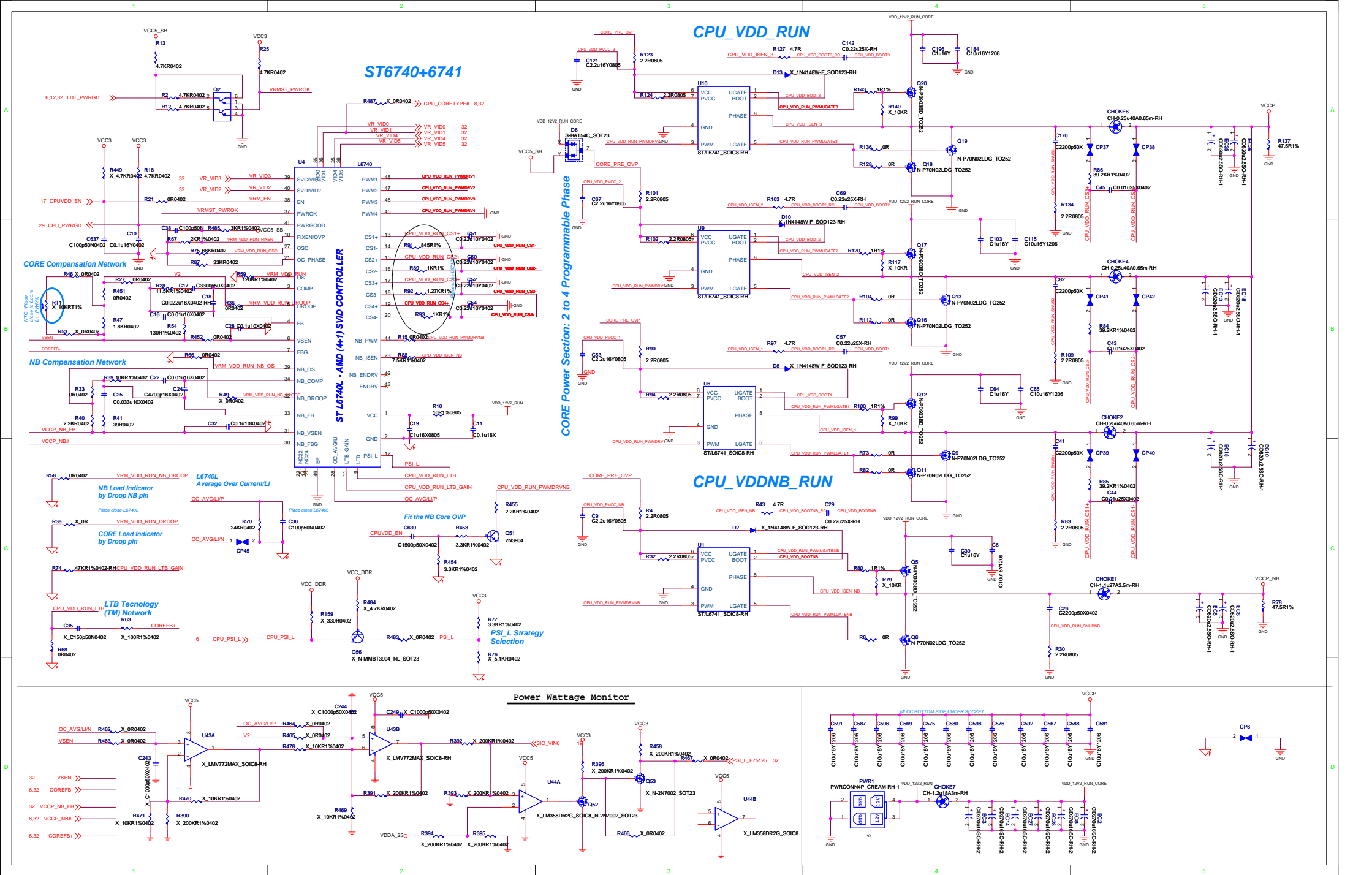


## VCORE\_VLD CIRCUIT

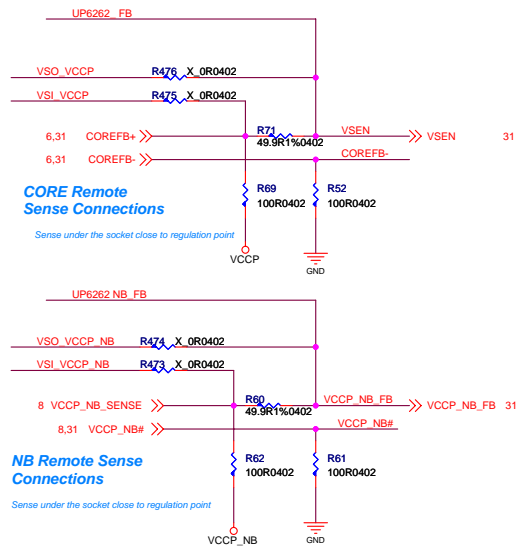
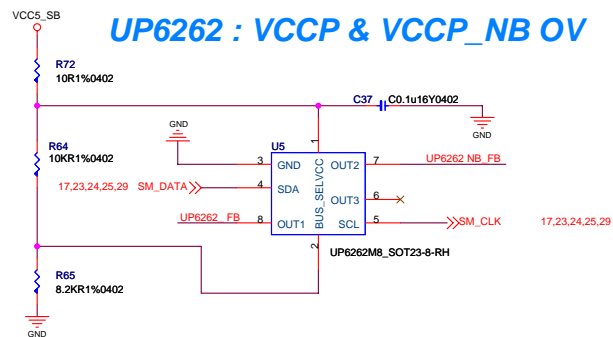


## DDR II 1.8V POWER

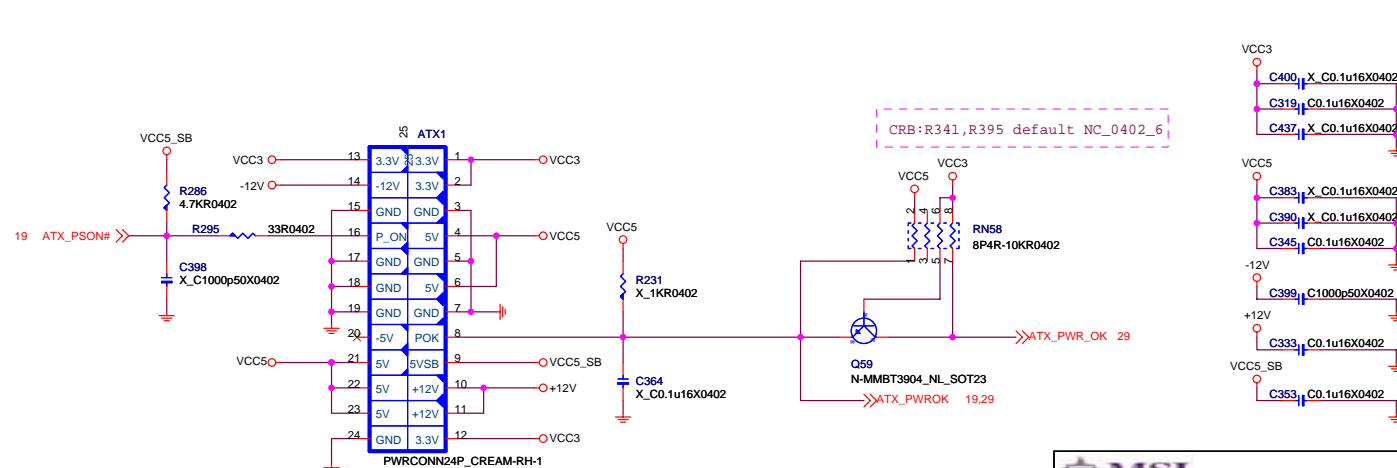
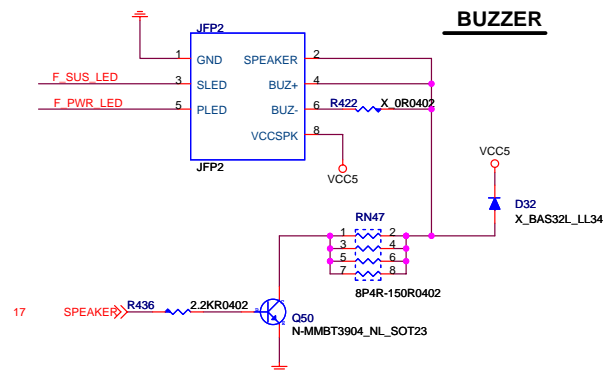
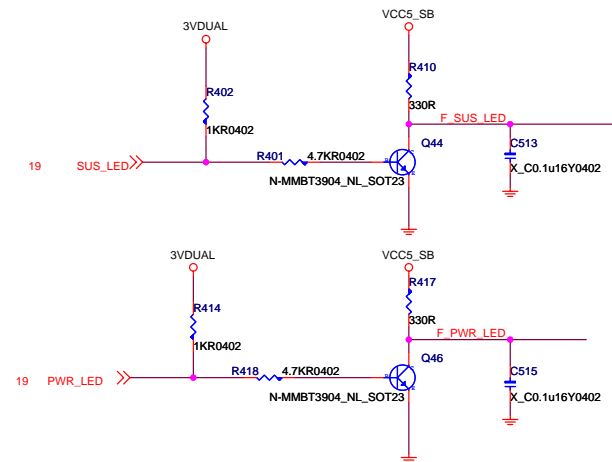
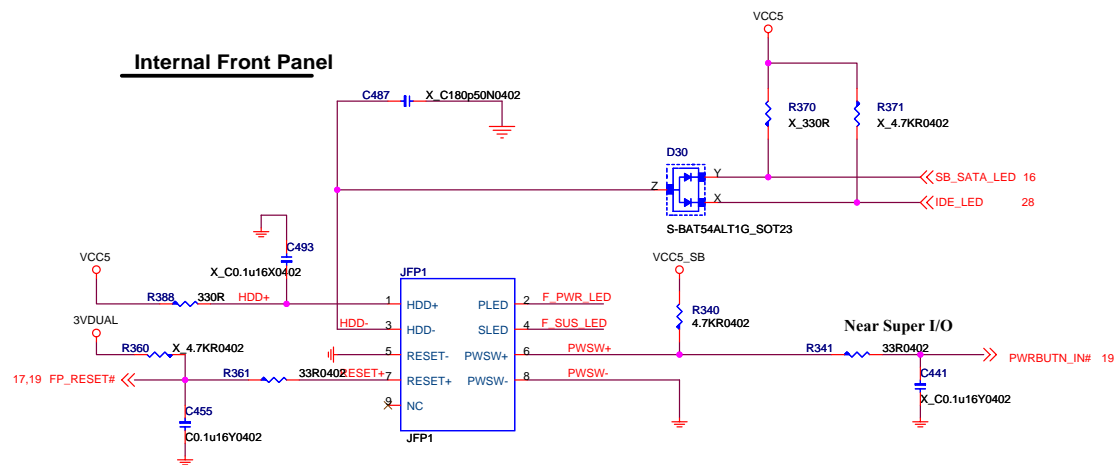




## UP6262 : VCCP & VCCP\_NB OV

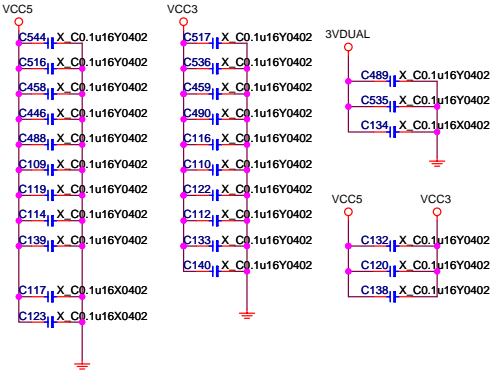


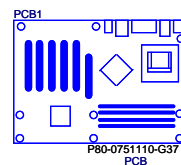
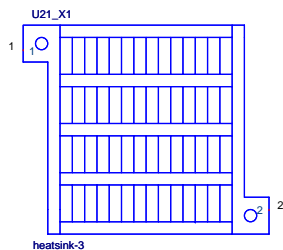




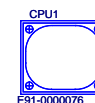
EMI solution

PCI SLOT DECOUPLING CAPACITORS

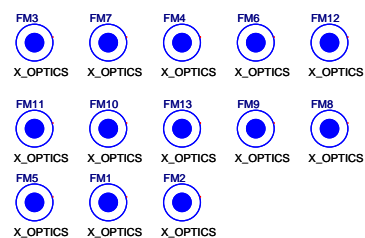




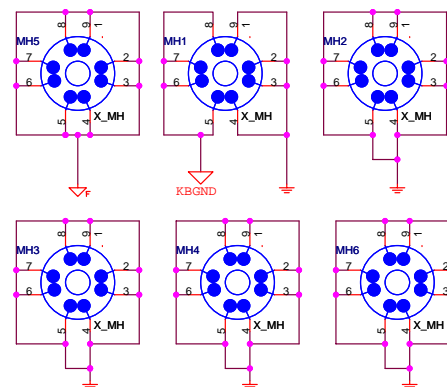
S. BAT1\_X1  
BAT-BCR2032P-RH



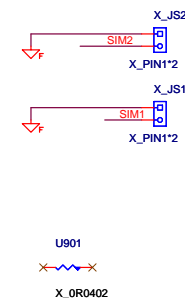
### Optics Orientation Holes



### Mounting Holes



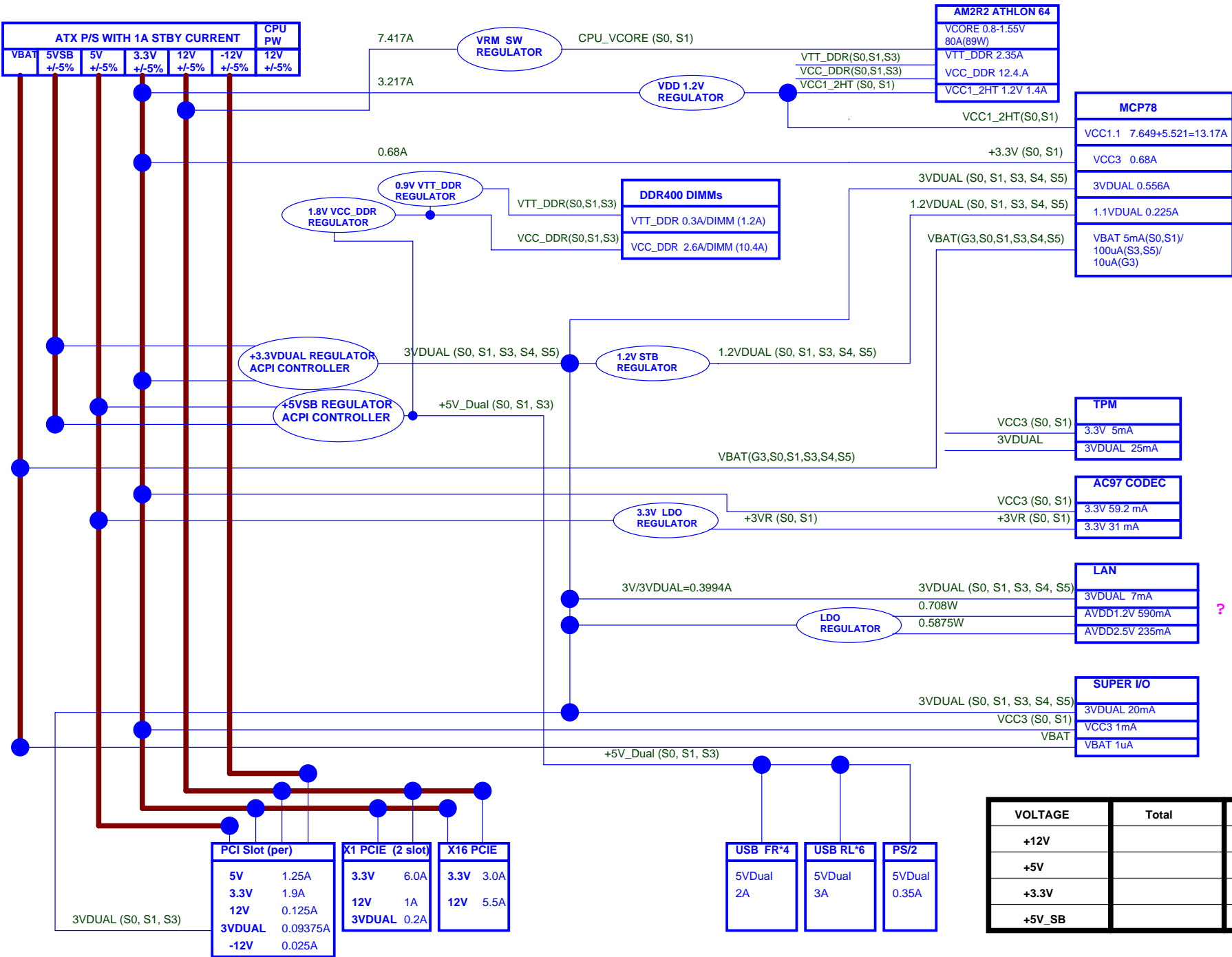
### Simulation



### Model option table

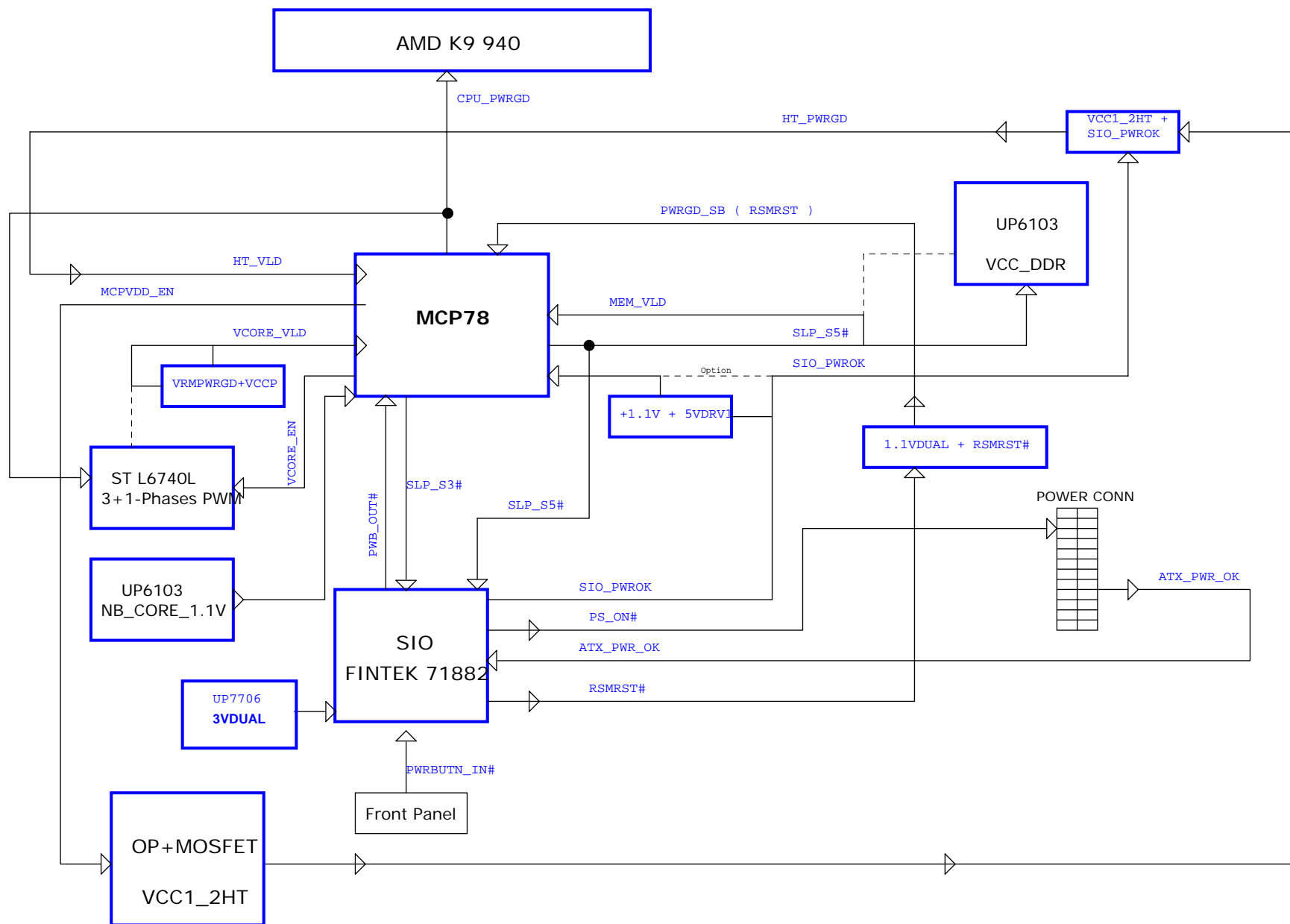
Model type	Function	BOM Config	ERP BOM No.
MS-7511	MCP78D+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+1Audio+RJ45	CFG-MCP78D	601-7511-01S
MS-7511	MCP78H/S+RTL8211BL+ALC888+3PCI+1PCIEX16+2PCIEX1 +PS2+10USB+2COM+VGA+1Audio+RJ45	CFG-MCP78H	601-7511-02S

ATX P/S WITH 1A STBY CURRENT						CPU PW
VBA1	5VSB	5V	3.3V	12V	-12V	12V
	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

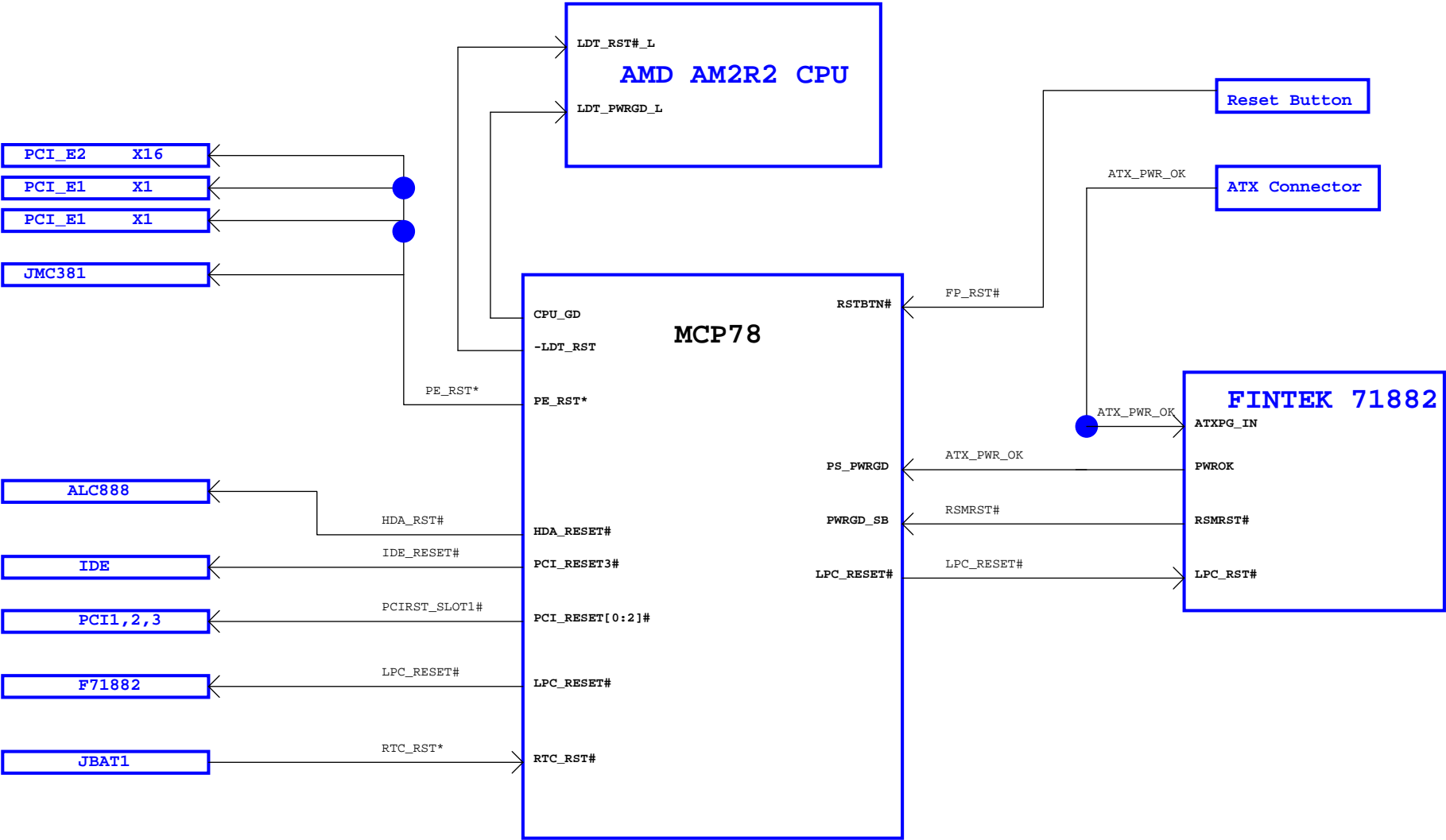


VOLTAGE	Total	AVERAGE
+12V		
+5V		
+3.3V		
+5V_SB		

# PWROK MAP



RESET MAP



5

(c)

3

A



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2007/09/07


- 1.page14 Remove R53,54,55 follow EMI disign
- 2.page21 Remove reserved R200
- 3.page13 Remove reserved Q58/Remove ATX\_PWROK level shift RN58,Q59
- 4.page17,26 Modify the USB\_OC circuit
- 5.page32 R340(PWSW+) change to pull-hi to VCC5\_SB
- 6.page29 Q10 D, S reverse
- 7.page10 Reserved R7,R8
- 8.page26 L10 USB PN reversed
- 9.page8,19 Remove CPU\_SLOT0CC#
- 10.page29 R279 pull-hi to 3VDDAL
- 11.page31 power swap phasel and phase2

2007/10/19

- 1.page17 USBREBIAS R445 change to 909R1# refer to APhote
- 2.page08 C559 modify ASM C0MM to 5020
- 3.page6,29,30 For AD1Q, remove R17,R231,fit 1.1VDDAL and RB\_CORE\_1.1V to 1.1V level
- 4.page31 Remove R449
- 5.page29 Stuff C403,C404,C438 to fit the reference sawtooth; Stuff Q1,Q31 for POS
- 6.page14 stuff R260,C377 for ix the VGA fail issue
- 7.page30 Reserved R7,R8

2007/10/19

- 1.page14 Modify C370,C371 15pF to fit RTC slow issue
- 2.page17 And reserved C306,C557
- 3.page15,25 Modify PCI slot2 to PCI\_REQ#4/PCI\_GNT#4 due to PCI\_REQ#1/GNT# cannot porting right
- 4.page32 Add Fintk75125 circuit
- 5.page14,26 Instead VGA with DVI
- 6.page23 Modify the termination R to RN56,RN57 560hm5#
- 7.page29,30 WB\_CORE1.1V follow the ramp up of 1.2V\_NT7; Reserve ATX\_PWR\_OK as the PS\_PWRGD
- 8.page16 Swap the part reference SATA4 &SATA5
- 9.page26,30 Modify EC17,EC23,EC24,EC30,EC61,EC62,EC63 footprint to C\_P1\_5\_DR\_H11\_5
- 10.page31 R59,R91,R92 value Add R485 3KR and modify R67 2KR to fit at 2.0V precisely; Reserve Q51 for PVI OVP trigger to prevent noboot
- 11.page21 Update Audio jack footprint to AUDIO\_JACK6\_26P\_U1\_1
- 12.page22 Remove R159;add C359,C377 ;modify C292,C111 for EMI
- 13.page17 Reserve EC64;Add C645 close to pin U21.K3
- 14.page29 Reserver the Special PSU sequence circuit
- 15.Page26 Modify RN21,RN24 to reserved L23,L31
- 16.Page 6 Remove R17,R231;Reserve R487,R488



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