GA-990FXA-D3

Revision : 1.01

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDR3 MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDR3 CHANNEL A
09	DDR3 CHANNEL B
10	RD990 HT-LINK I/F, PCIE I/F
11	RD990 SYSTEM I/F, STRAPS
12	RD990 POWER & GND
13	ICS9LPRS477
14	ATI SB950 PCIE/PCI/CPU/LPC
15	ATI SB950 ACPI/USB/GPIO/AUDIO
16	ATI SB950 SATA/SPI/IDE/HWM
17	ATI SB950 POWER & GND
18	PCI EXPRESS x16 ,x1
19	PCI EXPRESS x16 ,X4
20	PCI SLOT , PCIEx4
21	IT8720 LPC, KB/MS, TPM
22	F_USB, IPWR
23	ALC889
24	AUDIO JACK
25	FAN/HWMO/COM

PAGE	TITLE
26	ATX, FRONT PANEL
27	POWER SECQUENCE
28	5V_DUAL, DDR15V, DDRVTT, EUP
29	VCORE (PWM ISL6329)
30	NB/SB POWER, VCC12HT, VDDA25
31	REALTK RTL8111E
32	EJ168 R_USB30

GIGABYTE

Title: COVER SHEET		
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 1 of 32	

Model Name:GA-990FXA-D3

AM2-->AM3 Different: AE9-->AE7, H22-->H20. Extra pin:B2 AM3 socket is 938 pins. Only shift 2 pins.

Component value change history

Version: 1.01

4 Layer, 4mil 50ohm +/- 15% B

P-Code: U98145-0

Date	Version		Change Items
2011.03.17	0.1 New BOM Release.	PCB:0.1	Modify from 9M990FXA5-00-01
2011.04.13	1.0A BOM Release.	PCB:1.0	Add AMD Validation parts ,Add Thermal-Die schematic
2011.04.13	1.0A BOM Release.	PCB:1.0	Modify from 9M990FXA3-00-10A
2011.05.06	1.0B BOM Release.	PCB:1.01	Remove PCB silkscreen SLI logo

Circuit or PCB layout change for next version

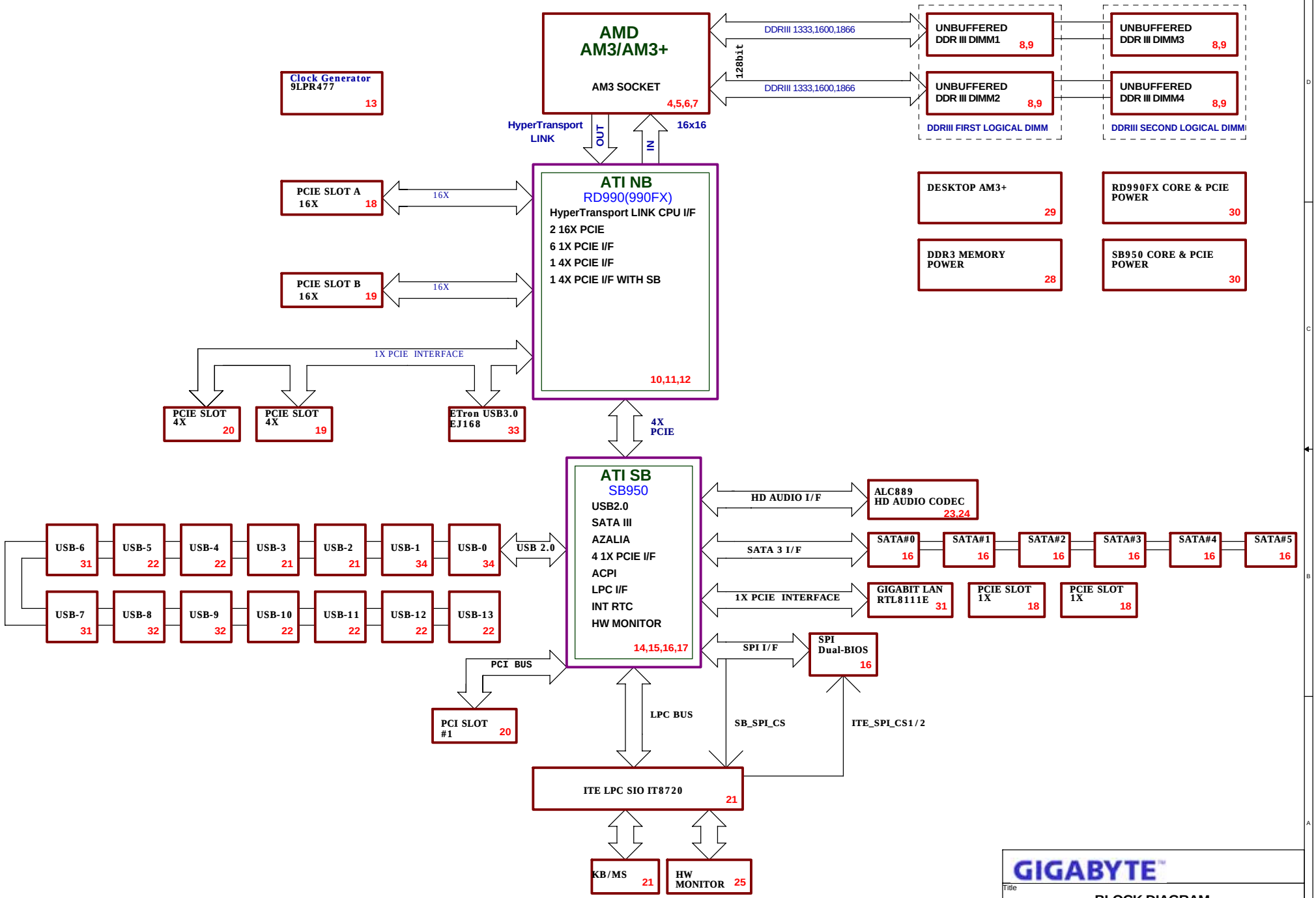
Date	Version	Reason
2011.03.16	0.1 Gerber-out	Modify from GA-990FXA-UD5 Rev 0.1
2011.04.12	1.0 Gerber-out	Add AMD Validation parts ,Add Thermal-Die schematic
2011.04.12	1.0 Gerber-out	Modify from GA-990FXA-UD3 Rev 1.0
2011.05.05	1.01 Gerber-out	Remove PCB silkscreen SLI logo

GIGABYTE

Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-990FXA-D3 | Rev: 1.01

Date: Thursday, May 05, 2011 | Sheet 2 of 32



GIGABYTE

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 3 of 32	

L0_CADIN_L[0..15]
L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AF2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

VCORE
AC1 100P/4/NPO/50V/J/X
AC2 100P/4/NPO/50V/J/X
AC3 100P/4/NPO/50V/J/X
HT_BUS Vcore use

MH3 MH9 MH8
MH1 MH2 MH4
MH7 MH5 MH6
HOLE_3/X

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

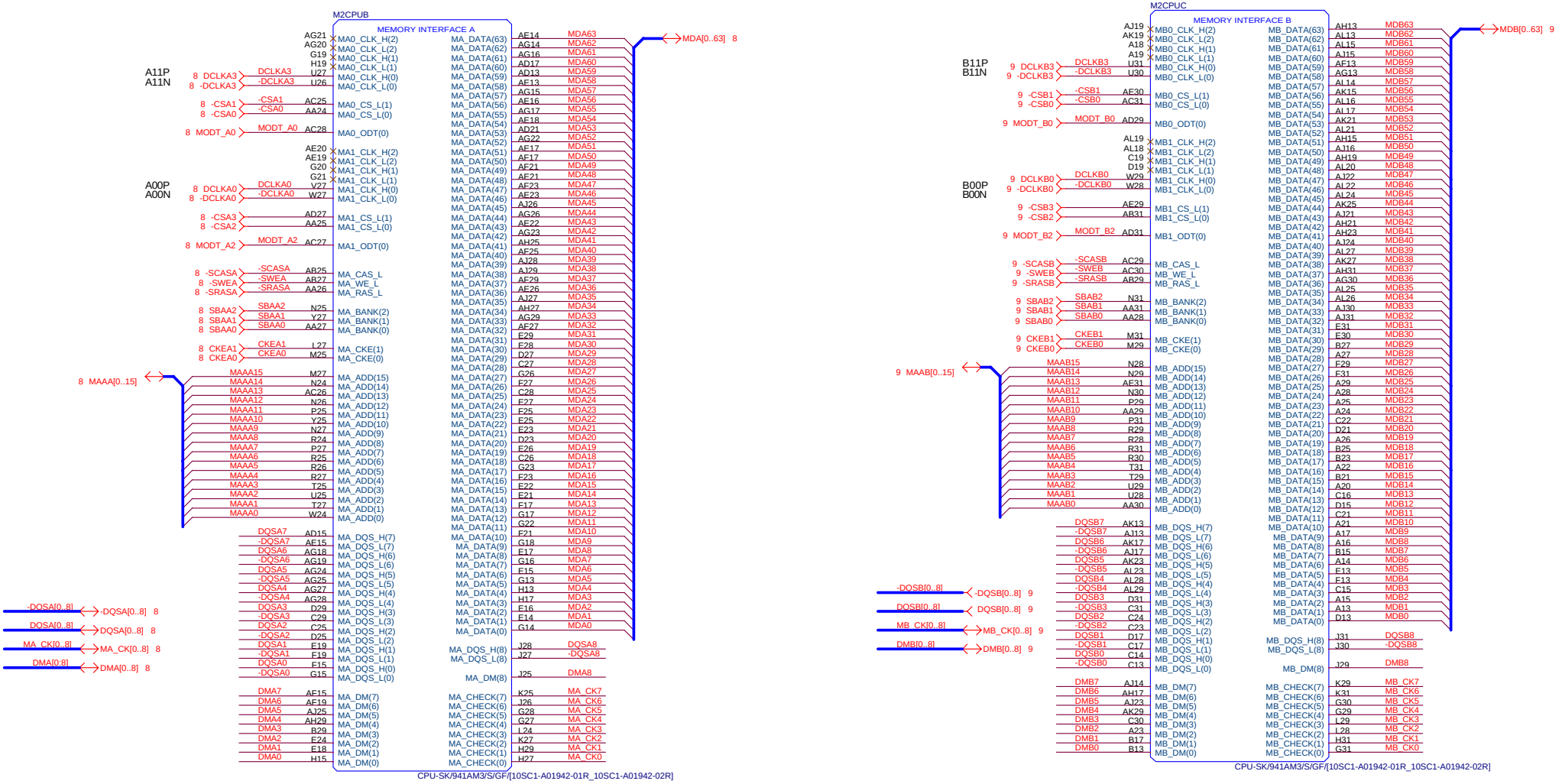
K1 K2 K3 K4 K5 K6
K1_ICT/X

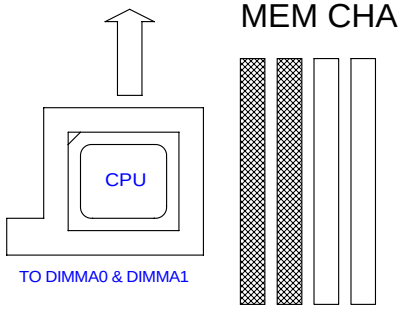
M2CPU

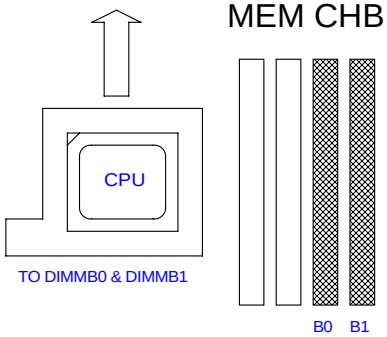
AM3RM/SC/BL/MB/[12KRC-04K812-31R]

GIGABYTE

Title: COVER SHEET		
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 4 of 32	

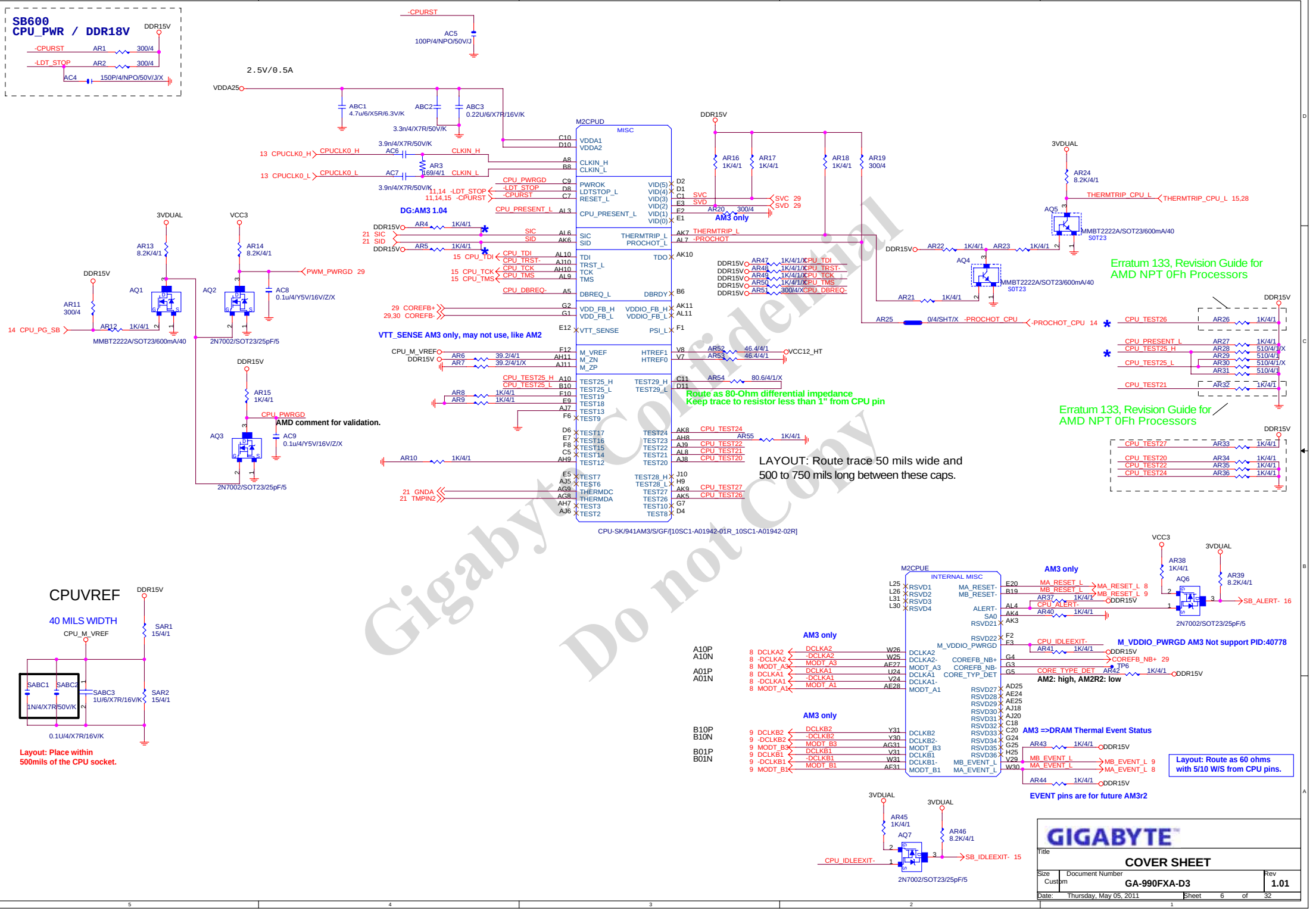


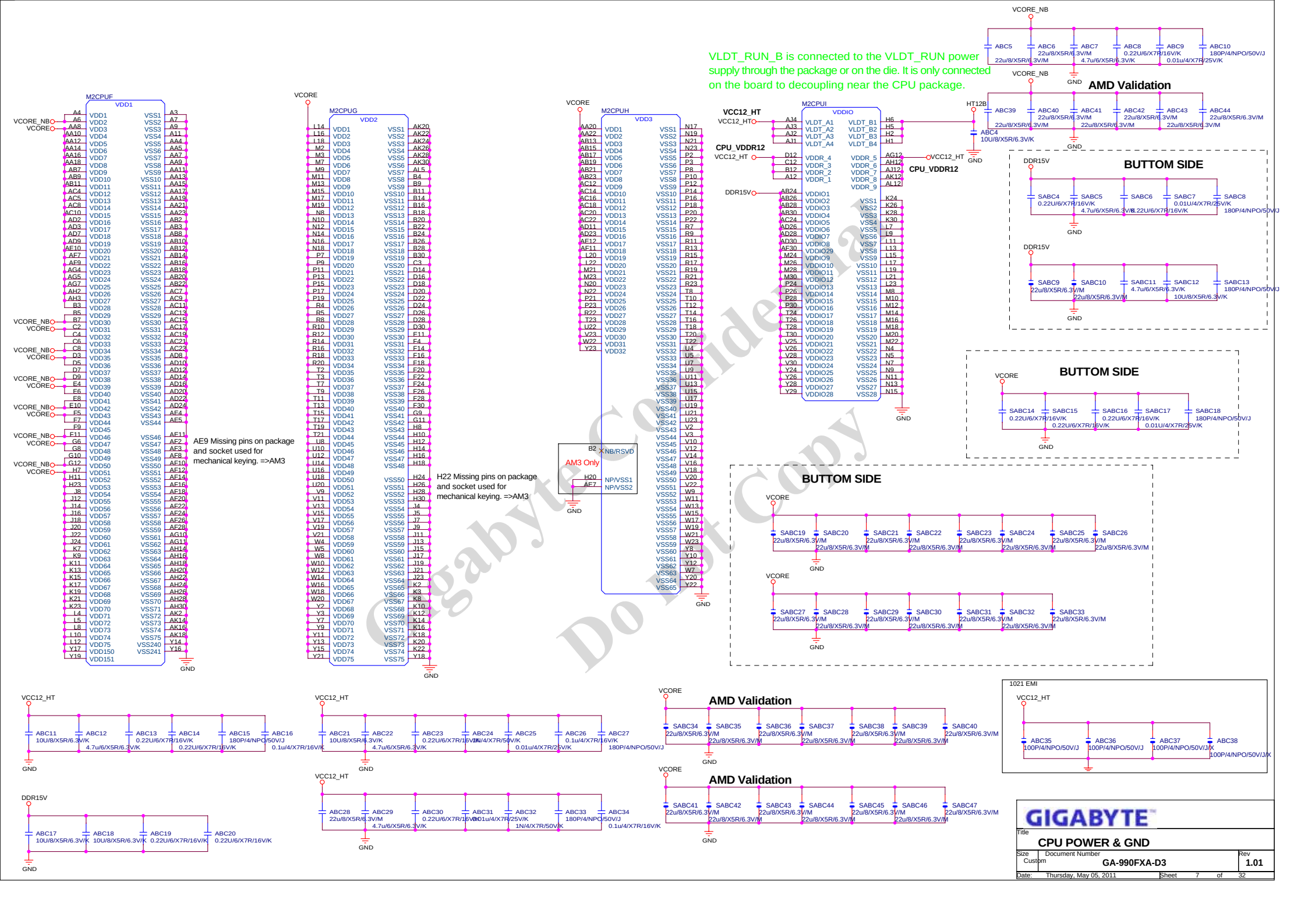




GIGABYTE

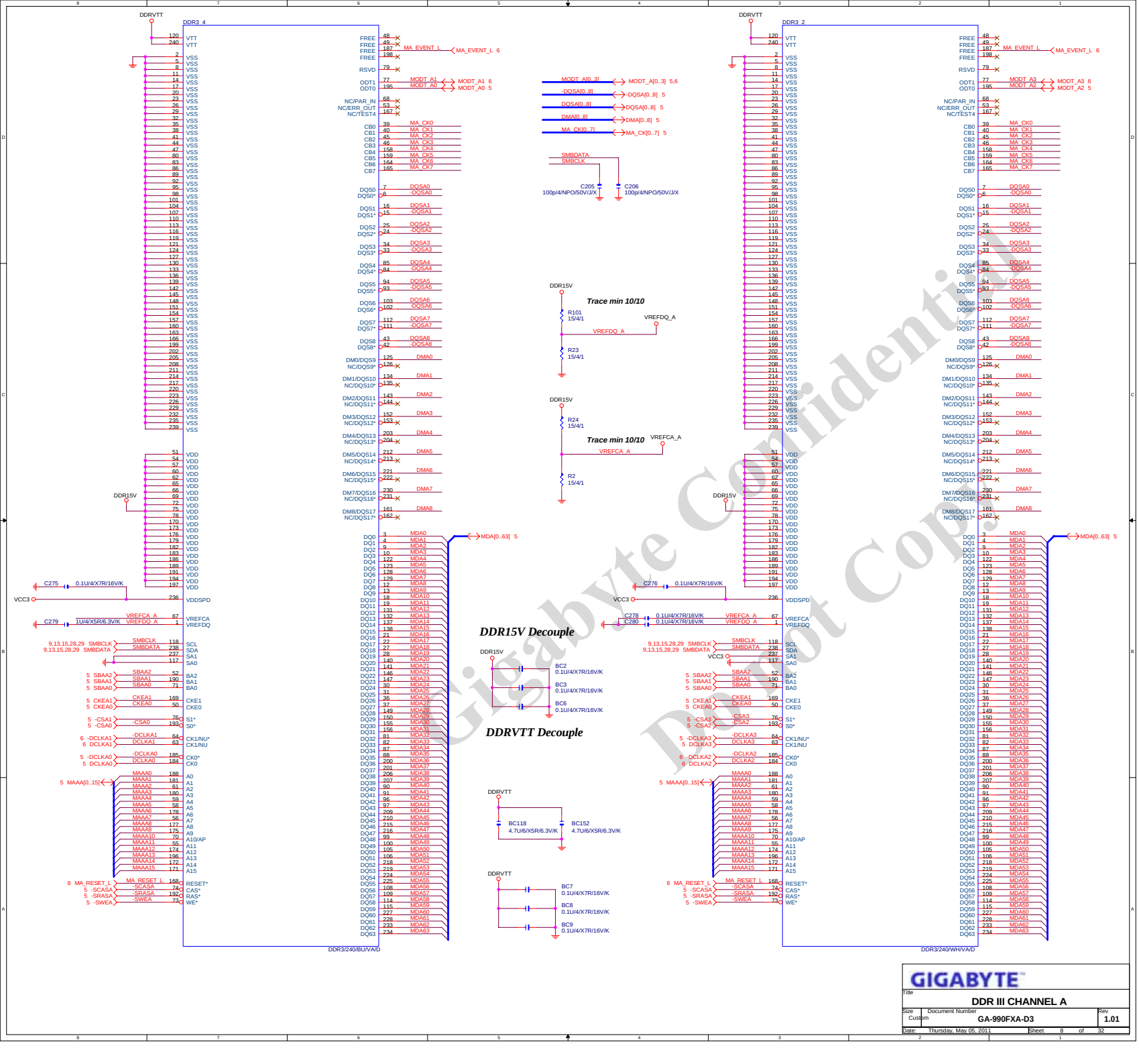
Title: COVER SHEET		
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 5 of 32	


SB600
CPU_PWR / DDR18V
DDR15V
-CPURST
AR1
300/4
-LDT_STOP
AR2
300/4
AC4
150P/4/NPO/50V/J/X
AC5
100P/4/NPO/50V/J
2.5V/0.5A
VDDA25
ABC1
4.7u/6/X5R/6.3V/K
ABC2
3.3n/4/X7R/50V/K
ABC3
0.22U/6/X7R/16V/K
M2CPUD
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
13 CPUCLK0_H
CPUCLK0_H
AC6
3.9n/4/X7R/50V/K
AR3
169/4/1
13 CPUCLK0_L
CPUCLK0_L
AC7
3.9n/4/X7R/50V/K
CPU_PWRGD
-LDT_STOP
-CPURST
11,14 -LDT_STOP
11,14,15 -CPURST
DG:AM3 1.04
CPU_PRESENT_L
AR16
1K/4/1
AR17
1K/4/1
AR18
1K/4/1
AR19
300/4
SVC
SVD
SVC 29
SVD 29
AR20
300/4
AM3 only
3VDUAL
AR24
8.2K/4/1
THERMTRIP_CPU_L
THERMTRIP_CPU_L 15,28
AQ5
MMBT2222A/SOT23/600mA/40
S0T23
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
DDR15V
AR4
1K/4/1
AR5
1K/4/1
21 SIC
21 SID
SIC
SID
15 CPU_TDI
CPU_TDI
CPU_TRST-
CPU_TCK
CPU_TMS
CPU_DBREQ-
TDI
TRST_L
TCK
TMS
DBREQ_L
TDO
DBRDY
THERMTRIP_L
-PROCHOT
AR22
1K/4/1
AR23
1K/4/1
AQ4
MMBT2222A/SOT23/600mA/40
S0T23
AR21
1K/4/1
AR25
0/4/SHT/X
-PROCHOT_CPU
-PROCHOT_CPU 14
AR47
AR48
AR49
AR50
AR51
300/4/X
CPU_TDI
CPU_TRST-
CPU_TCK
CPU_TMS
CPU_DBREQ-
3VDUAL
VCC3
AR13
8.2K/4/1
AR14
8.2K/4/1
PWM_PWRGD 29
AR11
300/4
AR12
1K/4/1
14 CPU_PG_SB
AQ1
AQ2
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
AC8
0.1u/4/Y5V/16V/Z/X
29 COREFB+
29,30 COREFB-
VTT_SENSE AM3 only, may not use, like AM2
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
VTT_SENSE
PSI_L
CPU_M_VREF
AR6
39.2/4/1
AR7
39.2/4/1/X
AR52
46.4/4/1
AR53
46.4/4/1
VCC12_HT
CPU_TEST25_H
CPU_TEST25_L
AR8
1K/4/1
AR9
1K/4/1
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
AR54
80.6/4/1/X
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
AR10
1K/4/1
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST21
CPU_TEST20
AR55
1K/4/1
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
21 GNDA
21 TMPIN2
CPU_TEST27
CPU_TEST26
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]
AR15
1K/4/1
CPU_PWRGD
AMD comment for validation.
AQ3
AC9
0.1u/4/Y5V/16V/Z/X
2N7002/SOT23/25pF/5
CPU_TEST26
CPU_PRESENT_L
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST21
AR26
AR27
AR28
AR29
AR30
AR31
AR32
1K/4/1
510/4/1/X
510/4/1
CPU_TEST27
CPU_TEST20
CPU_TEST22
CPU_TEST24
AR33
AR34
AR35
AR36
M2CPUE
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
ALERT-
SA0
RSVD21
RSVD22
M_VDDIO_PWRGD
COREFB_NB+
COREFB_NB-
CORE_TYP_DET
MA_RESET-
MB_RESET-
MA_RESET_L
MB_RESET_L
CPU_ALERT-
CPU_IDLEEXIT-
CORE_TYPE_DET
AM3 only
MA_RESET_L 8
MB_RESET_L 9
DDR15V
M_VDDIO_PWRGD AM3 Not support PID:40778
COREFB_NB+ 29
TP6
AM2: high, AM2R2: low
AR38
1K/4/1
AR39
8.2K/4/1
AQ6
2N7002/SOT23/25pF/5
SB_ALERT- 16
A10P
A10N
A01P
A01N
B10P
B10N
B01P
B01N
DCLKA2
-DCLKA2
MODT_A3
DCLKA1
-DCLKA1
MODT_A1
DCLKB2
-DCLKB2
MODT_B3
DCLKB1
-DCLKB1
MODT_B1
MB_EVENT_L
MA_EVENT_L
AM3 =>DRAM Thermal Event Status
MB_EVENT_L 9
MA_EVENT_L 8
Layout: Route as 60 ohms
with 5/10 W/S from CPU pins.
EVENT pins are for future AM3r2
AR43
AR44
AR45
1K/4/1
AQ7
AR46
8.2K/4/1
SB_IDLEEXIT- 15
CPUVREF
40 MILS WIDTH
CPU_M_VREF
SAR1
15/4/1
SAR2
15/4/1
SABC1
SABC2
1N/4/X7R/50V/K
SABC3
1U/6/X7R/16V/K
0.1U/4/X7R/16V/K
Layout: Place within
500mils of the CPU socket.
Gigabyte Confidential
Do not Copy
GIGABYTE
Title
COVER SHEET
Size
Custom
Document Number
GA-990FXA-D3
Rev
1.01
Date: Thursday, May 05, 2011
Sheet 6 of 32



GIGABYTE

Title	CPU POWER & GND
Size: Custom	Document Number: GA-990FXA-D3
Rev	1.01
Date: Thursday, May 05, 2011	Sheet 7 of 32

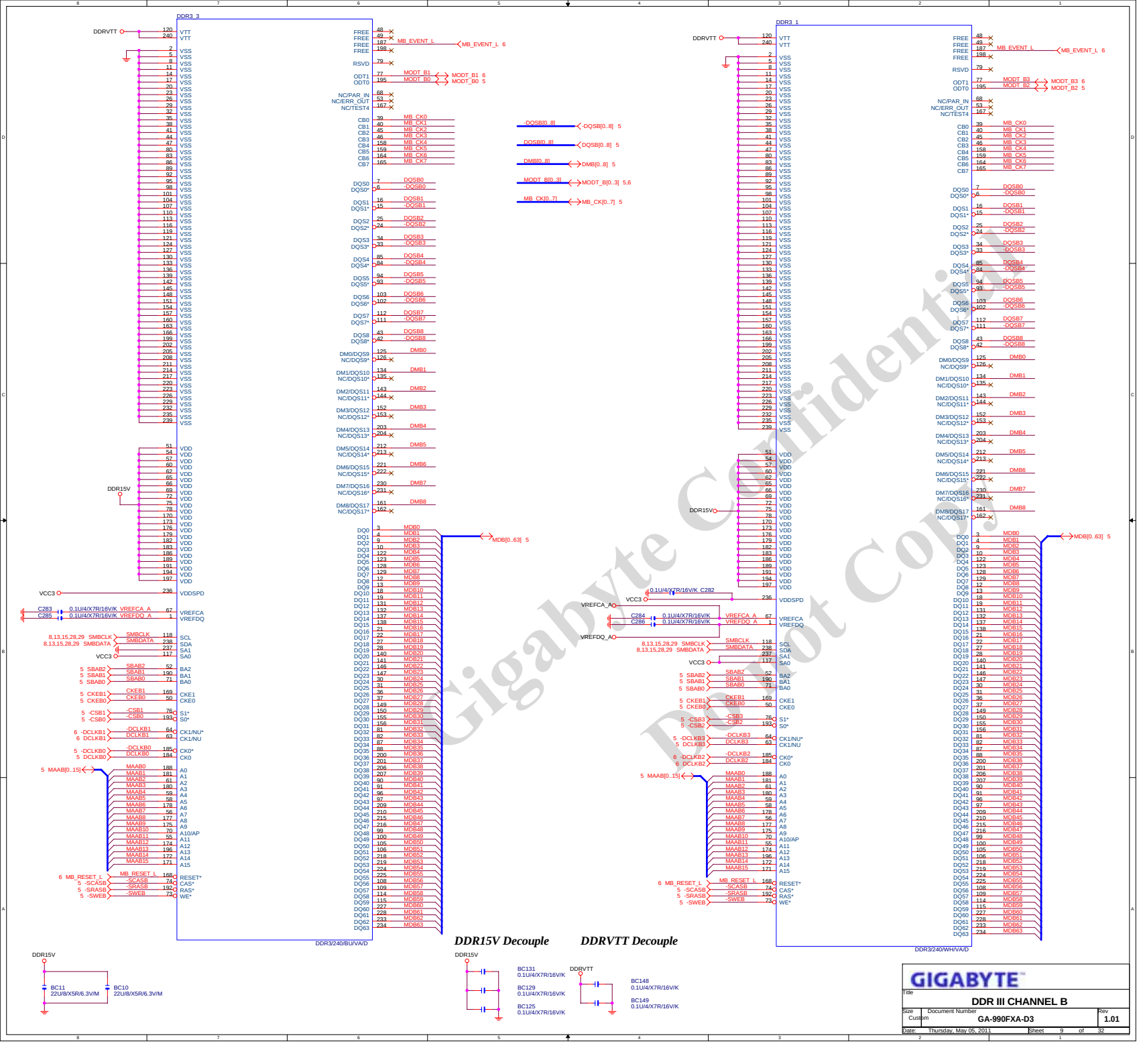


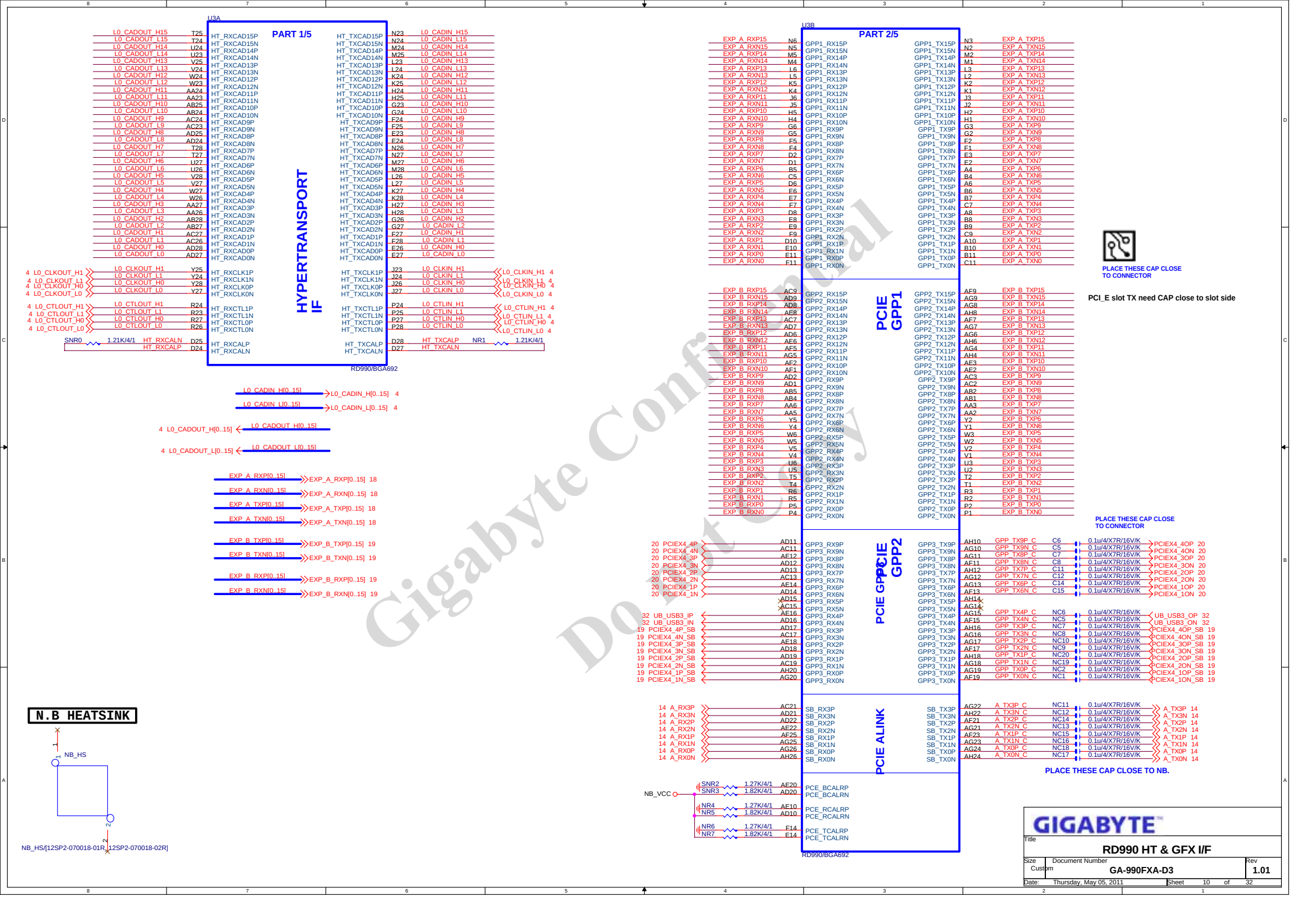
GIGABYTE

Title: DDR III CHANNEL A

Size	Document Number	Rev
Custom	GA-990FXA-D3	1.01

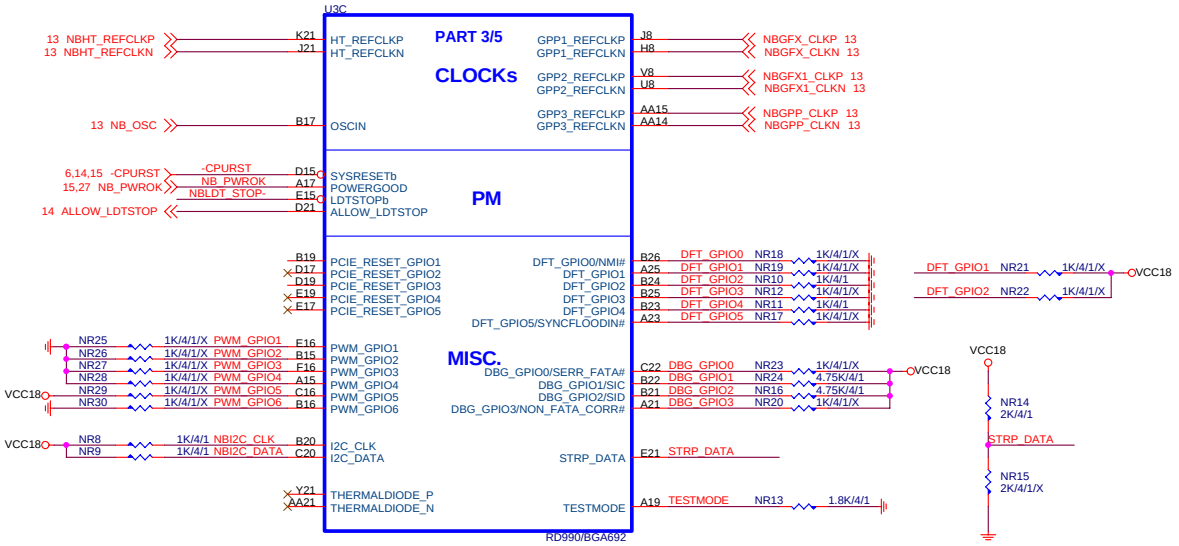
Date: Thursday, May 05, 2011 Sheet 8 of 32

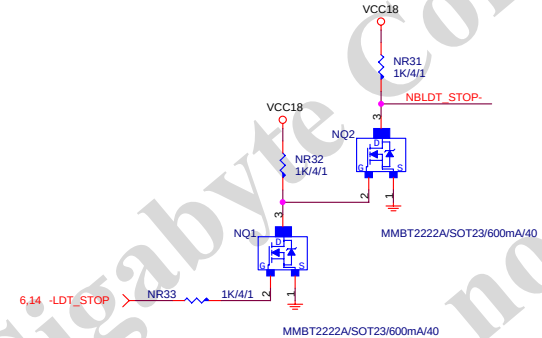




GIGABYTE

Title	RD990 HT & GFX I/F	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 10 of 32	





DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

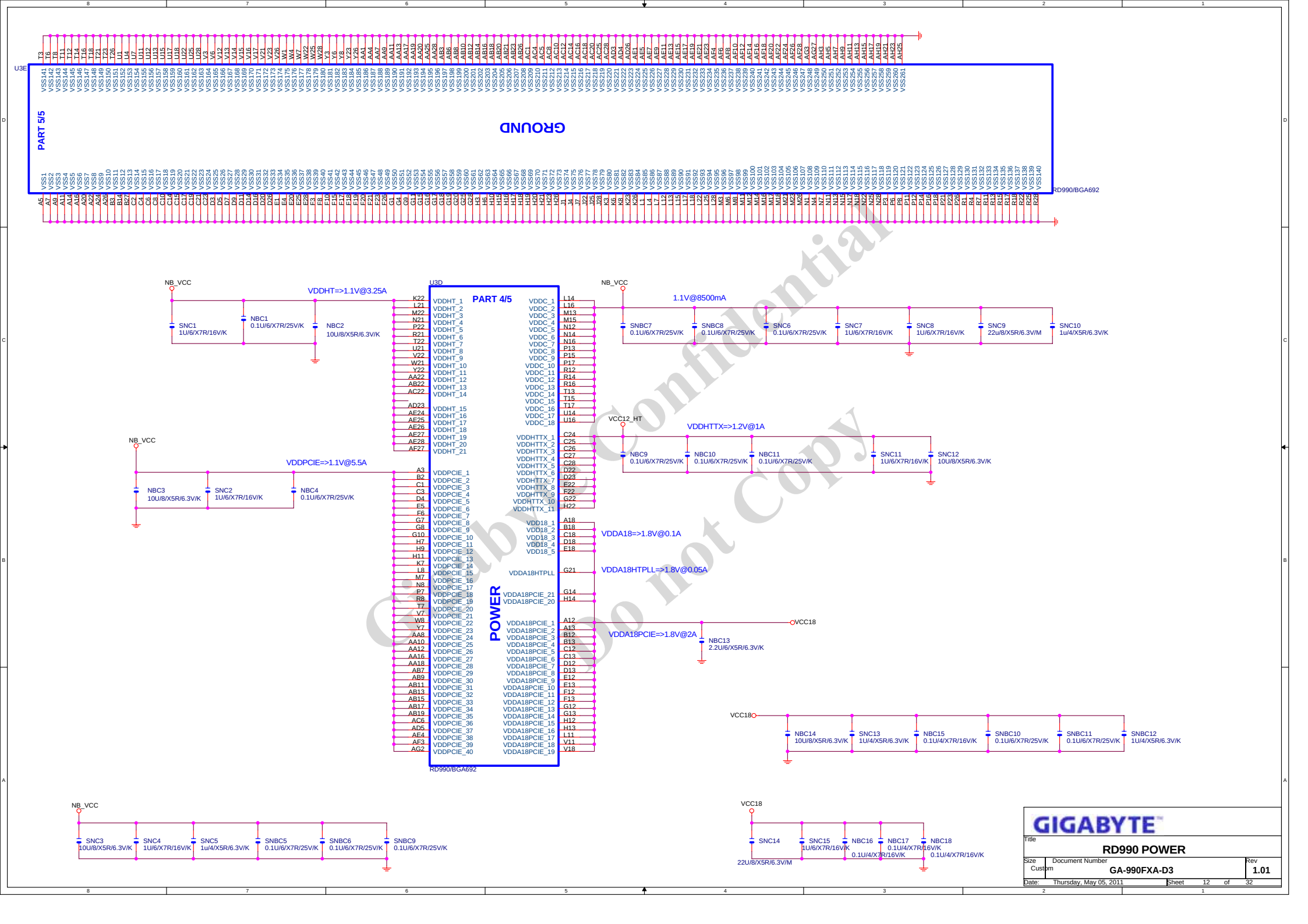
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE

Title	RD990 CLOCK & SYSB I/F	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 11 of 32	

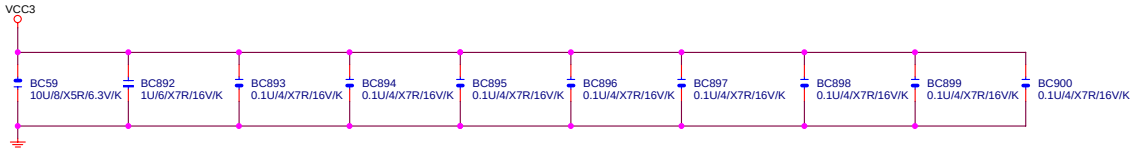


GIGABYTE

Title: RD990 POWER

Size: Custom | Document Number: GA-990FXA-D3 | Rev: 1.01

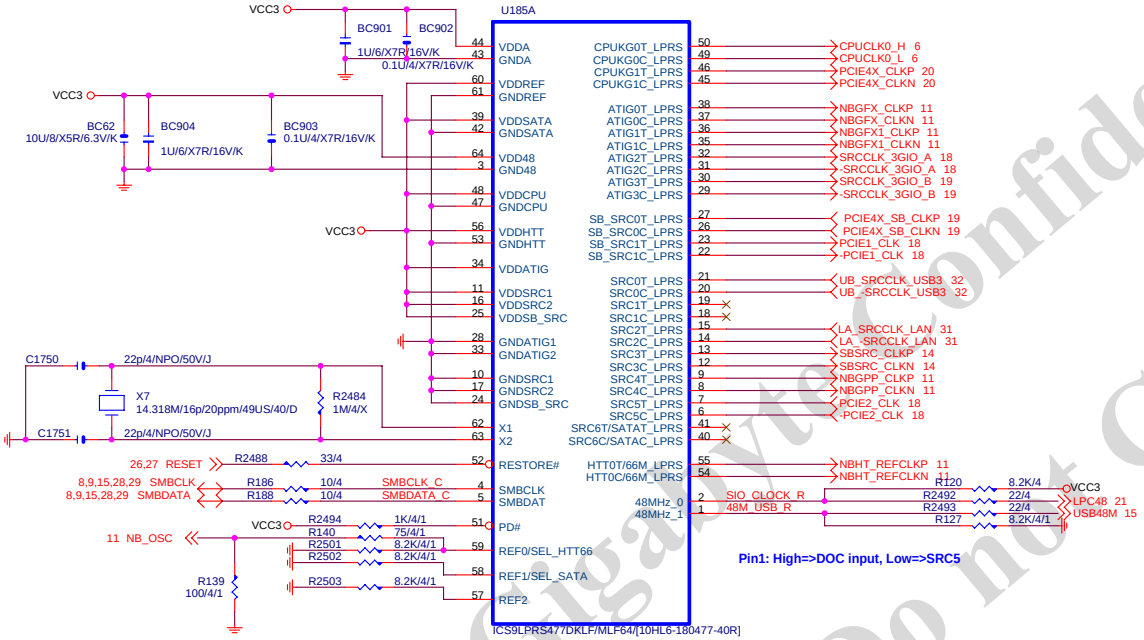
Date: Thursday, May 05, 2011 | Sheet 12 of 32



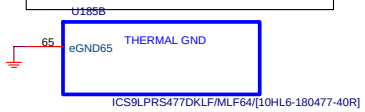
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

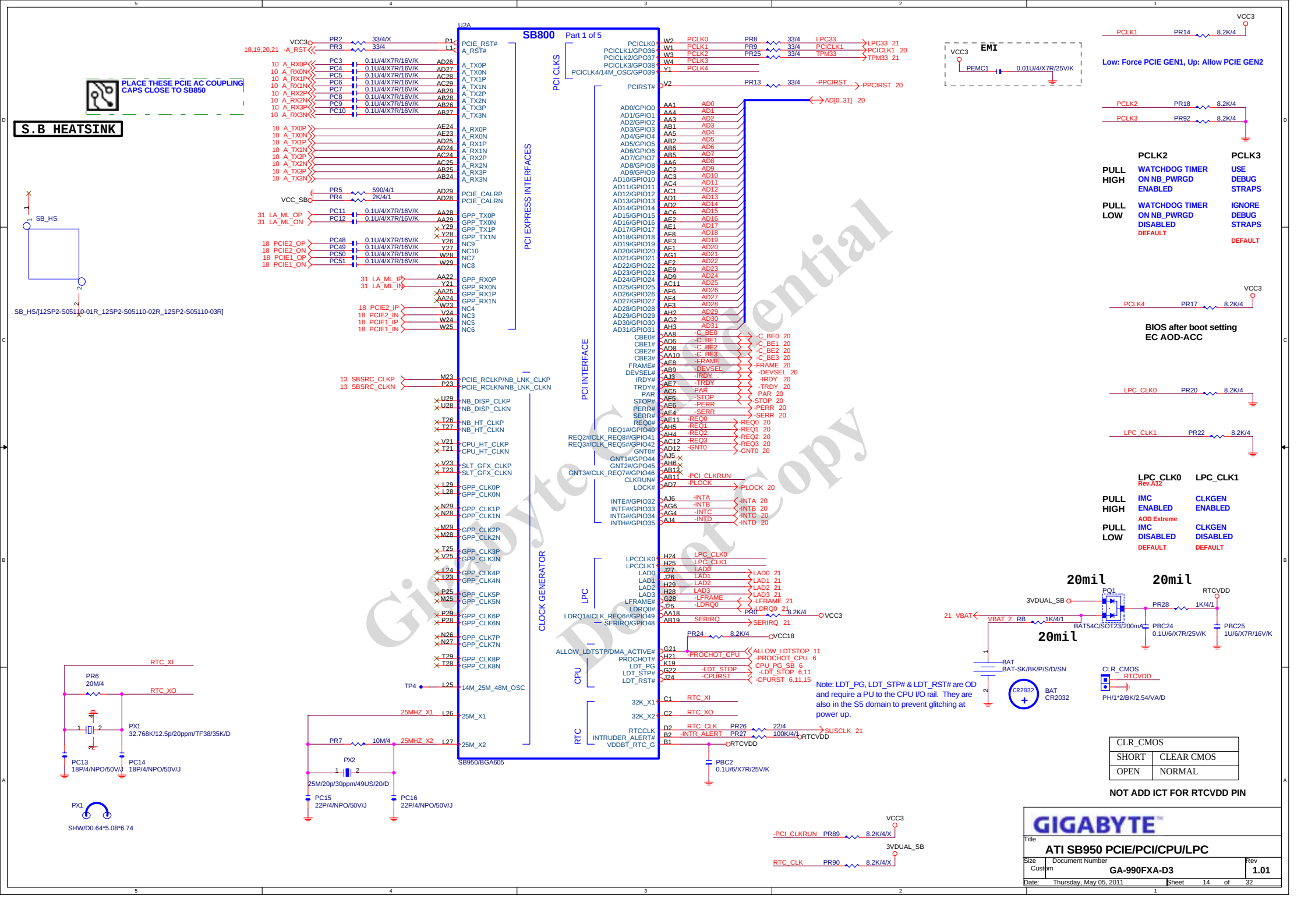
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE

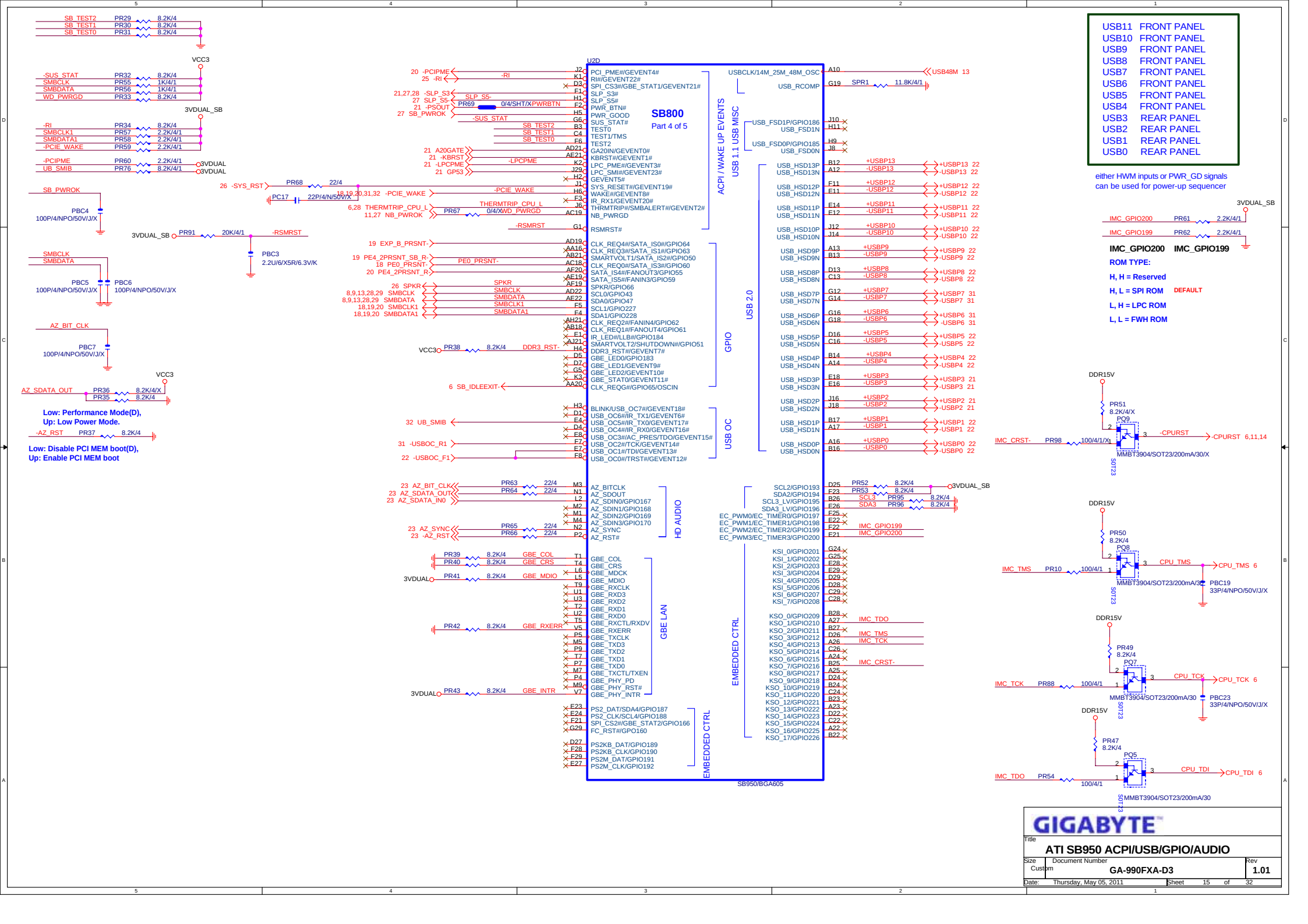
Title: ICS9LPRS477

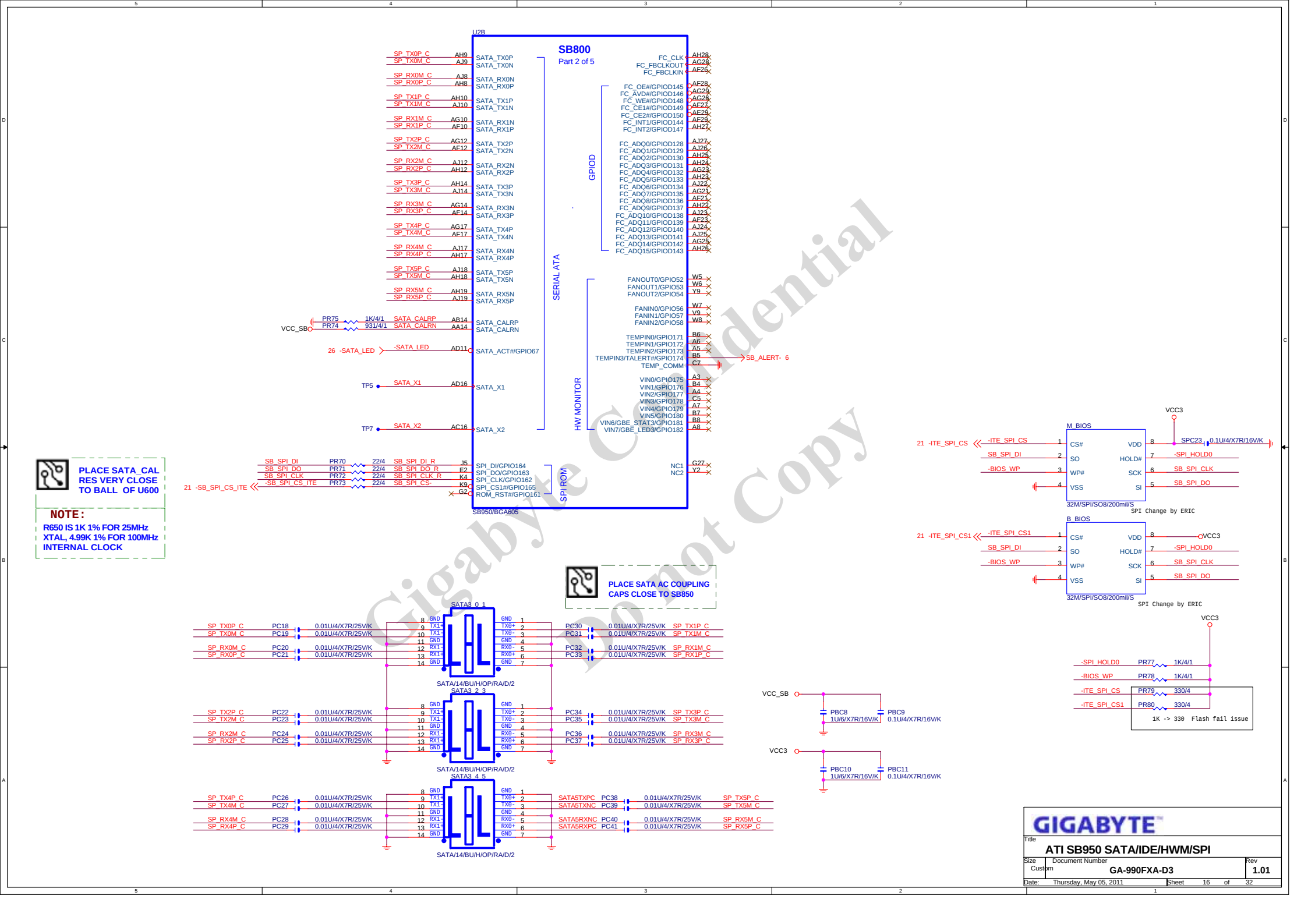
Size: Custom | Document Number: GA-990FXA-D3 | Rev: 1.01

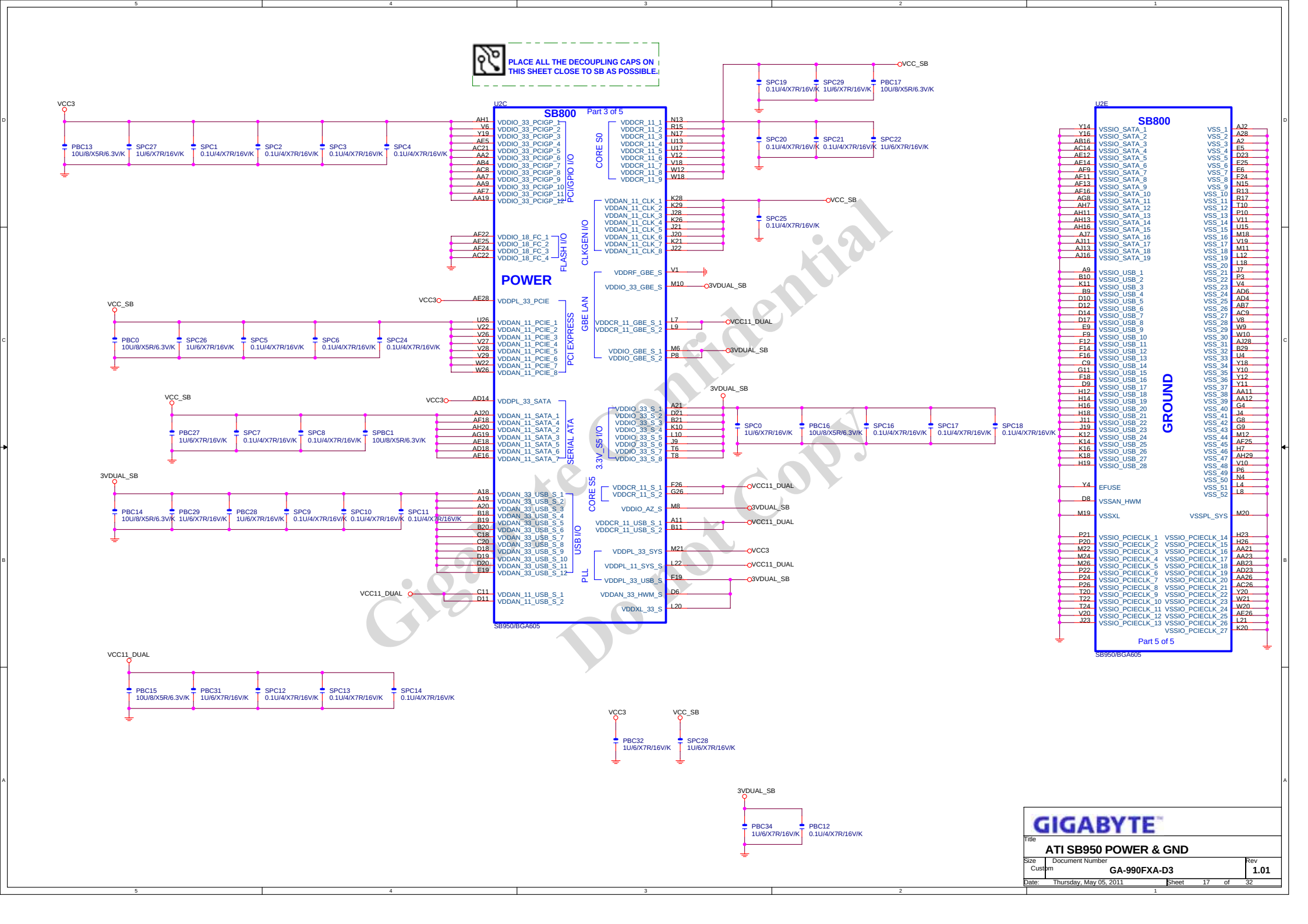
Date: Thursday, May 05, 2011 | Sheet 13 of 32

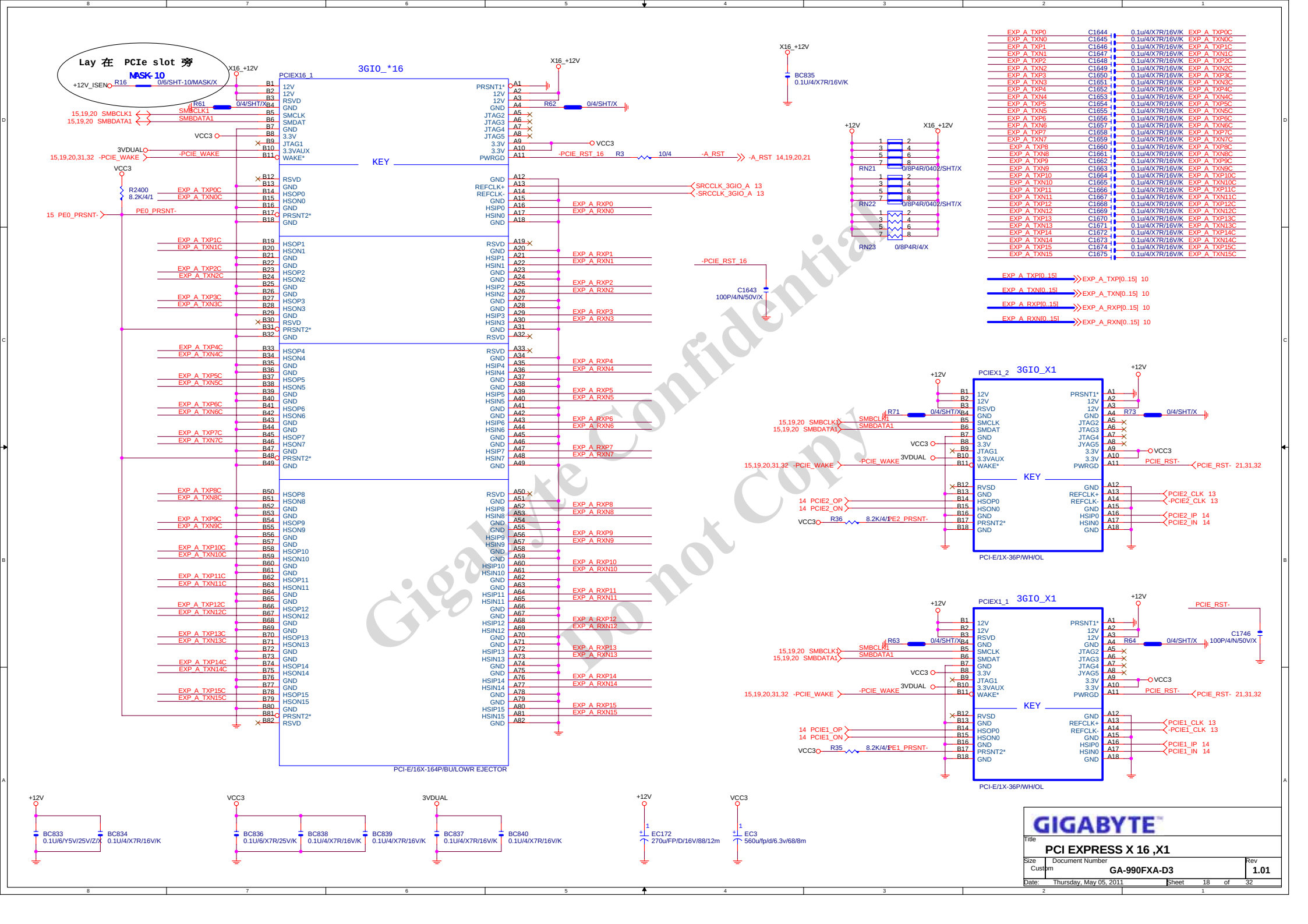


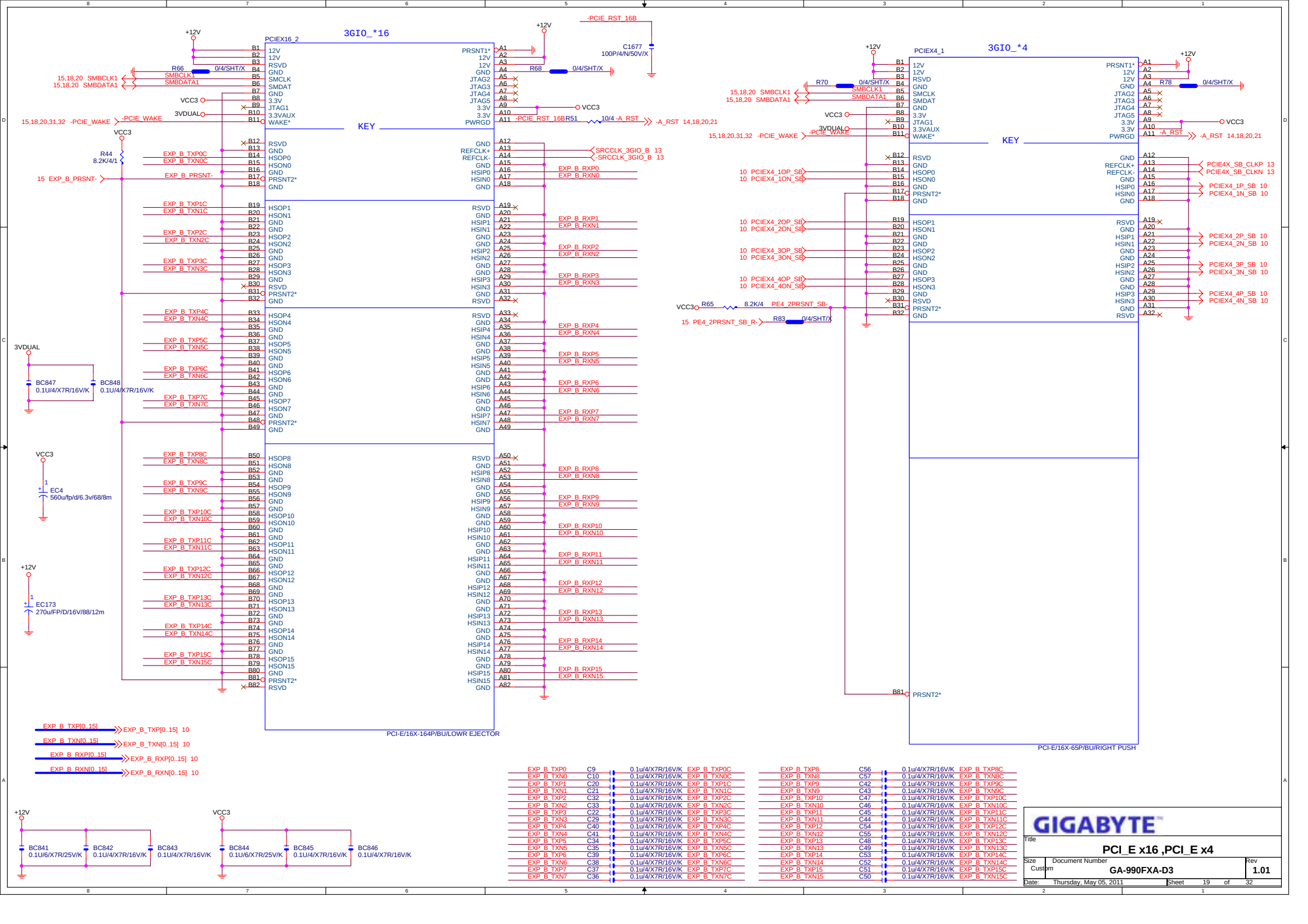
Title	ATI SB950 PCIE/PCI/CPU/LPC
Size	Custom
Document Number	GA-990FXA-D3
Rev	1.01
Date:	Thursday, May 05, 2011
Sheet	14 of 32

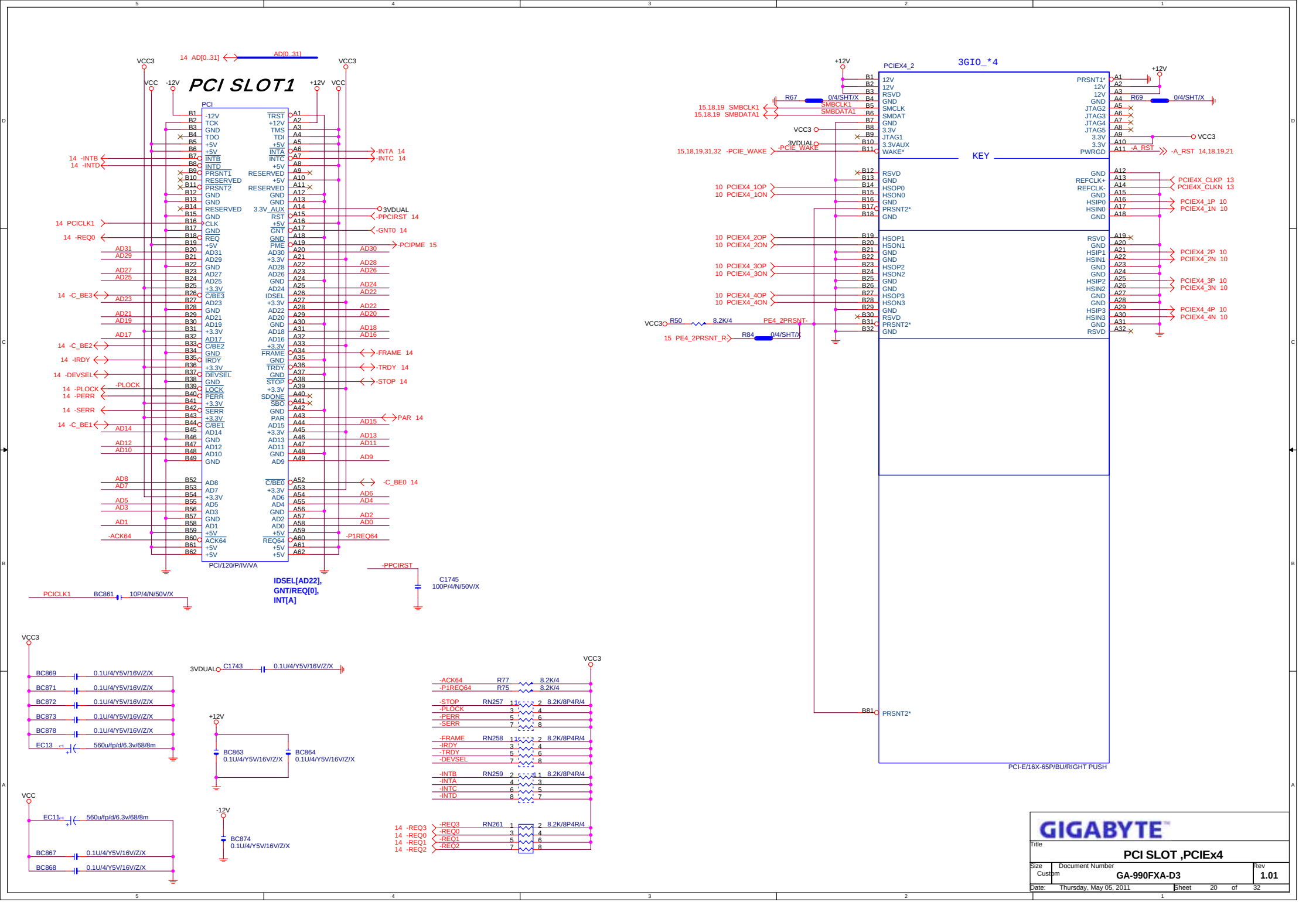

SB800
Part 4 of 5
SB950/BGA605
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
IMC_GPIO200 IMC_GPIO199
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
Low: Performance Mode(D), Up: Low Power Mode.
Low: Disable PCI MEM boot(D), Up: Enable PCI MEM boot
GIGABYTE
ATI SB950 ACPI/USB/GPIO/AUDIO
GA-990FXA-D3
1.01
Thursday, May 05, 2011
Sheet 15 of 32

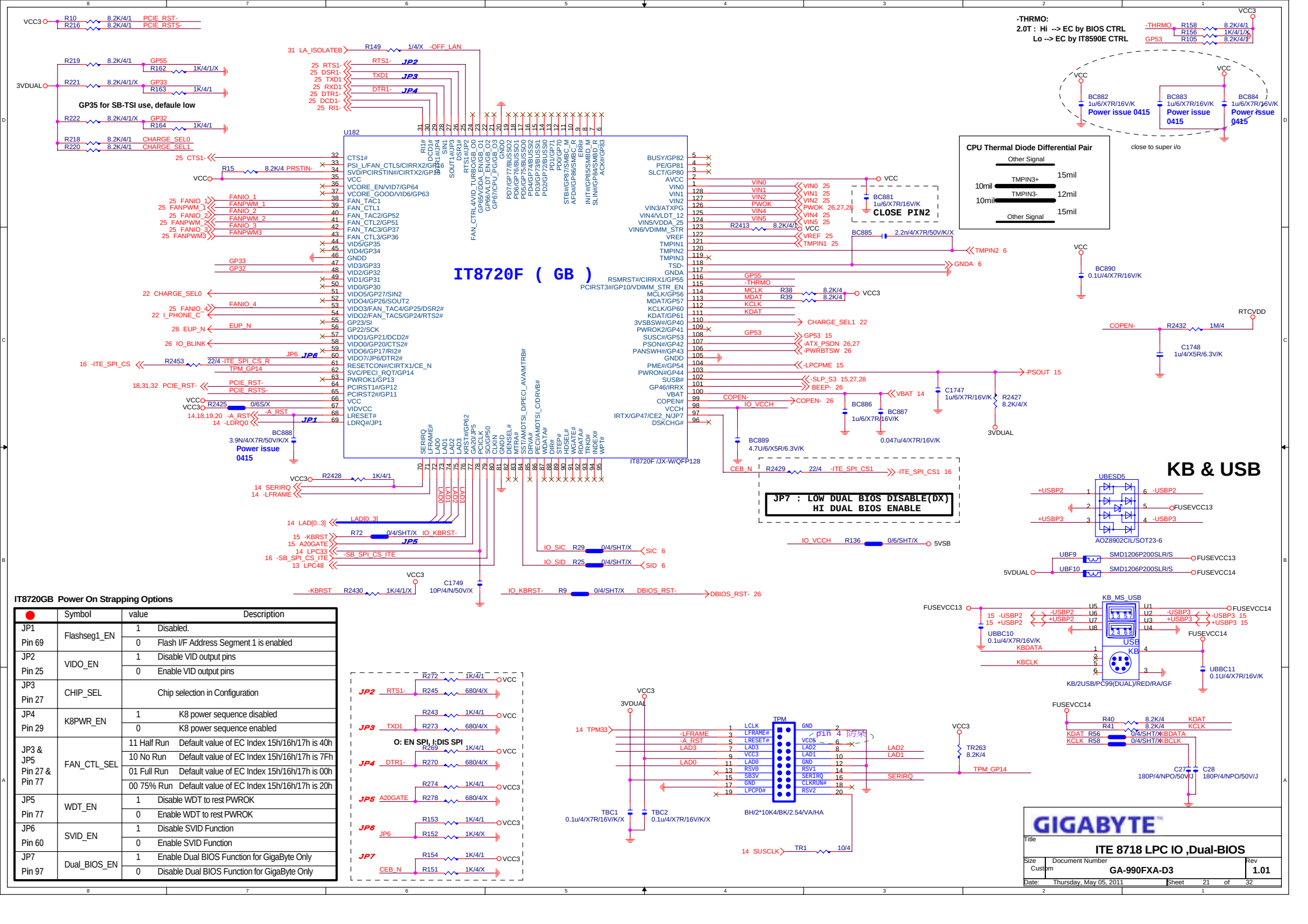

U2B
SB800
Part 2 of 5
SERIAL ATA
GPIOD
HW MONITOR
SPI ROM
SB950/BGA605
SATA_X1
SATA_X2
SATA_CALRP
SATA_CALRN
SATA_ACT#/GPIO67
-SATA_LED
-SB_SPI_CS_ITE
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600
NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK
PLACE SATA AC COUPLING CAPS CLOSE TO SB850
SATA3_0_1
SATA3_2_3
SATA3_4_5
SATA/14/BU/H/OP/RA/D/2
M_BIOS
B_BIOS
32M/SPI/SO8/200mil/S
SPI Change by ERIC
1K -> 330 Flash fail issue
GIGABYTE
ATI SB950 SATA/IDE/HWM/SPI
GA-990FXA-D3
1.01
Thursday, May 05, 2011
Sheet 16 of 32
Gigabyte Confidential
Do not Copy


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
SB800
Part 3 of 5
POWER
SB950/BGA605
SB800
GROUND
Part 5 of 5
SB950/BGA605
Gigabyte Confidential
Do not Copy
GIGABYTE
Title
ATI SB950 POWER & GND
Size
Custom
Document Number
GA-990FXA-D3
Rev
1.01
Date: Thursday, May 05, 2011
Sheet 17 of 32


Lay 在 PCIe slot 旁
MASK 10
PCIEX16_1
3GIO_*16
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
PCIEX1_2
3GIO_X1
PCI-E/1X-36P/WH/OL
PCIEX1_1
3GIO_X1
PCI-E/1X-36P/WH/OL
Gigabyte Confidential
Do not Copy
GIGABYTE
PCI EXPRESS X 16 ,X1
GA-990FXA-D3
1.01
Thursday, May 05, 2011
Sheet 18 of 32


3GIO_*16
PCIEX16_2
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
3GIO_*4
PCIEX4_1
KEY
PCI-E/16X-65P/BU/RIGHT PUSH
GIGABYTE
Title
PCI_E x16 ,PCI_E x4
Size
Custom
Document Number
GA-990FXA-D3
Rev
1.01
Date: Thursday, May 05, 2011
Sheet 19 of 32


PCI SLOT1
PCI
PCI/120/P/IV/VA
IDSEL[AD22],
GNT/REQ[0],
INT[A]
PCIEX4_2
3GIO_*4
KEY
PCI-E/16X-65P/BU/RIGHT PUSH
GIGABYTE
PCI SLOT ,PCIEx4
GA-990FXA-D3
1.01
Thursday, May 05, 2011

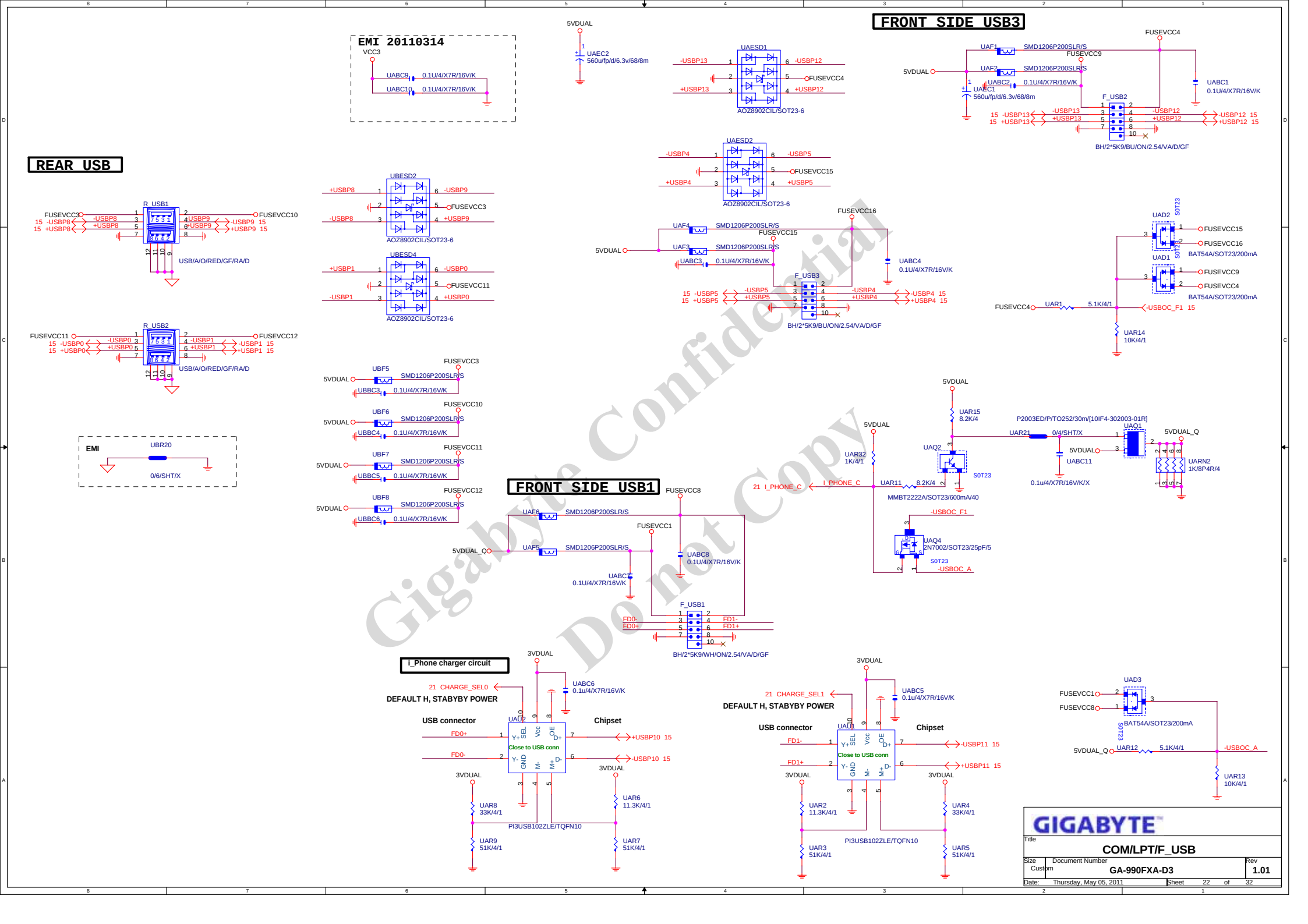


IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	CHIP_SEL		Chip selection in Configuration
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

GIGABYTE

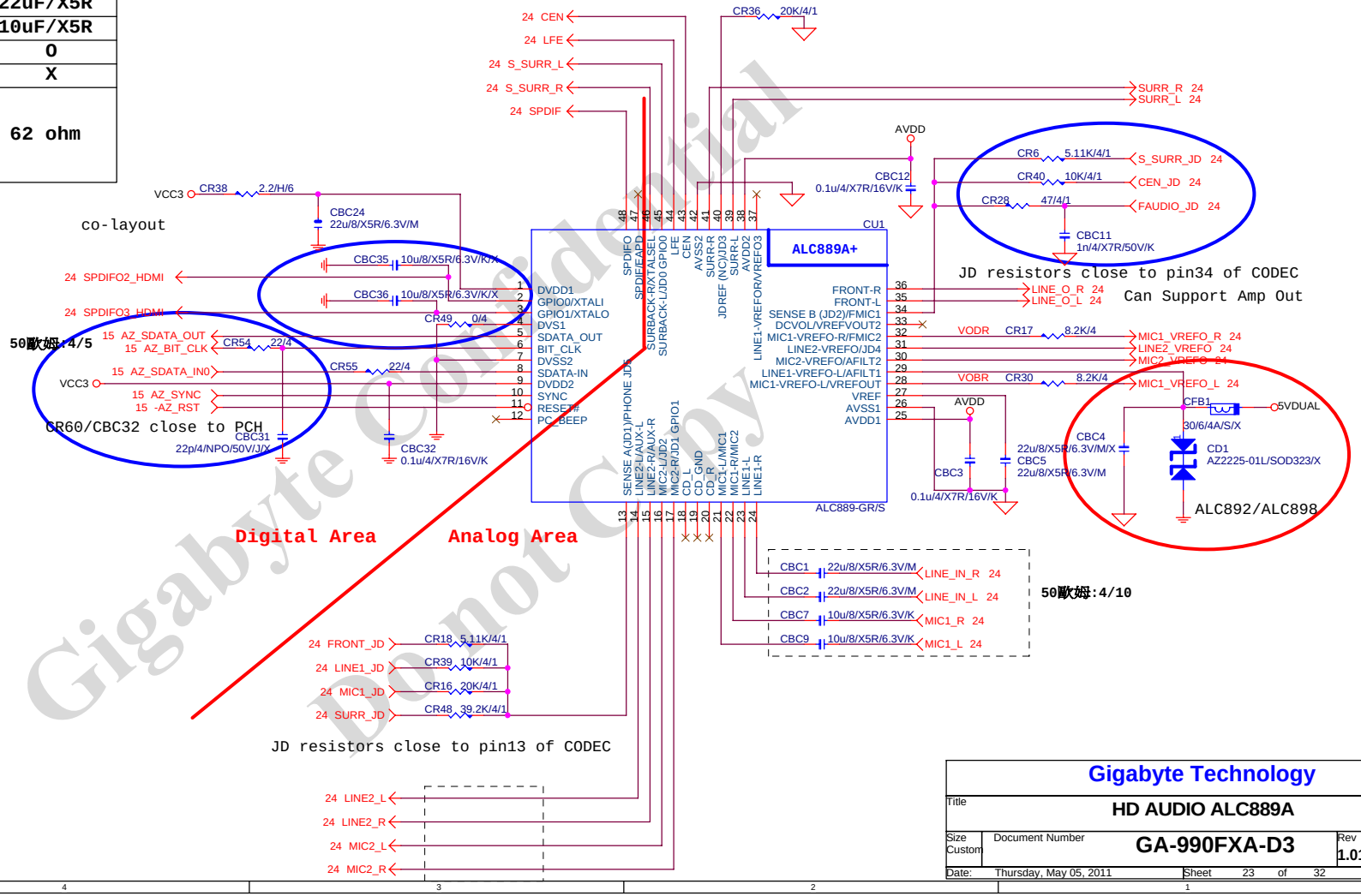
Title	ITE 8718 LPC IO ,Dual-BIOS	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 21 of 32	


FRONT SIDE USB3
REAR USB
FRONT SIDE USB1
EMI 20110314
VCC3
UABC9 0.1U/4/X7R/16V/K
UABC10 0.1U/4/X7R/16V/K
5VDUAL
UAEC2 560u/fp/d/6.3v/68/8m
UAESD1
AOZ8902CIL/SOT23-6
FUSEVCC4
UAF1 SMD1206P200SLR/S
FUSEVCC9
UAF2 SMD1206P200SLR/S
UABC2 0.1U/4/X7R/16V/K
UABC1 560u/fp/d/6.3v/68/8m
UABC1 0.1U/4/X7R/16V/K
F_USB2
BH/2*5K9/BU/ON/2.54/VA/D/GF
UAESD2
AOZ8902CIL/SOT23-6
FUSEVCC15
FUSEVCC16
UAF4 SMD1206P200SLR/S
UAF3 SMD1206P200SLR/S
UABC3 0.1U/4/X7R/16V/K
UABC4 0.1U/4/X7R/16V/K
F_USB3
BH/2*5K9/BU/ON/2.54/VA/D/GF
R_USB1
USB/A/O/RED/GF/RA/D
R_USB2
USB/A/O/RED/GF/RA/D
UBESD2
AOZ8902CIL/SOT23-6
UBESD4
AOZ8902CIL/SOT23-6
UAD2 BAT54A/SOT23/200mA
UAD1 BAT54A/SOT23/200mA
UAR1 5.1K/4/1
UAR14 10K/4/1
UBF5 SMD1206P200SLR/S
UBBC3 0.1U/4/X7R/16V/K
UBF6 SMD1206P200SLR/S
UBBC4 0.1U/4/X7R/16V/K
UBF7 SMD1206P200SLR/S
UBBC5 0.1U/4/X7R/16V/K
UBF8 SMD1206P200SLR/S
UBBC6 0.1U/4/X7R/16V/K
EMI
UBR20
0/6/SHT/X
UAR15 8.2K/4
P2003ED/P/TO252/30m/[10IF4-302003-01R]
UAR21 0/4/SHT/X
UAQ1
UARN2 1K/8P4R/4
UAR32 1K/4/1
UAR11 8.2K/4
MMBT2222A/SOT23/600mA/40
UABC11 0.1u/4/X7R/16V/K/X
UAQ2
UAQ4 2N7002/SOT23/25pF/5
UAF6 SMD1206P200SLR/S
UAF5 SMD1206P200SLR/S
UABC8 0.1U/4/X7R/16V/K
UABC7 0.1U/4/X7R/16V/K
F_USB1
BH/2*5K9/WH/ON/2.54/VA/D/GF
i_Phone charger circuit
DEFAULT H, STABYBY POWER
USB connector
Chipset
Close to USB conn
UAQ0
UABC6 0.1u/4/X7R/16V/K
UAR8 33K/4/1
UAR6 11.3K/4/1
UAR9 51K/4/1
UAR7 51K/4/1
PI3USB102ZLE/TQFN10
UAQ1
UABC5 0.1u/4/X7R/16V/K
UAR2 11.3K/4/1
UAR4 33K/4/1
UAR3 51K/4/1
UAR5 51K/4/1
UAD3 BAT54A/SOT23/200mA
UAR12 5.1K/4/1
UAR13 10K/4/1
GIGABYTE
COM/LPT/F_USB
GA-990FXA-D3
1.01
Thursday, May 05, 2011
22 of 32
Gigabyte Confidential
Do not Copy

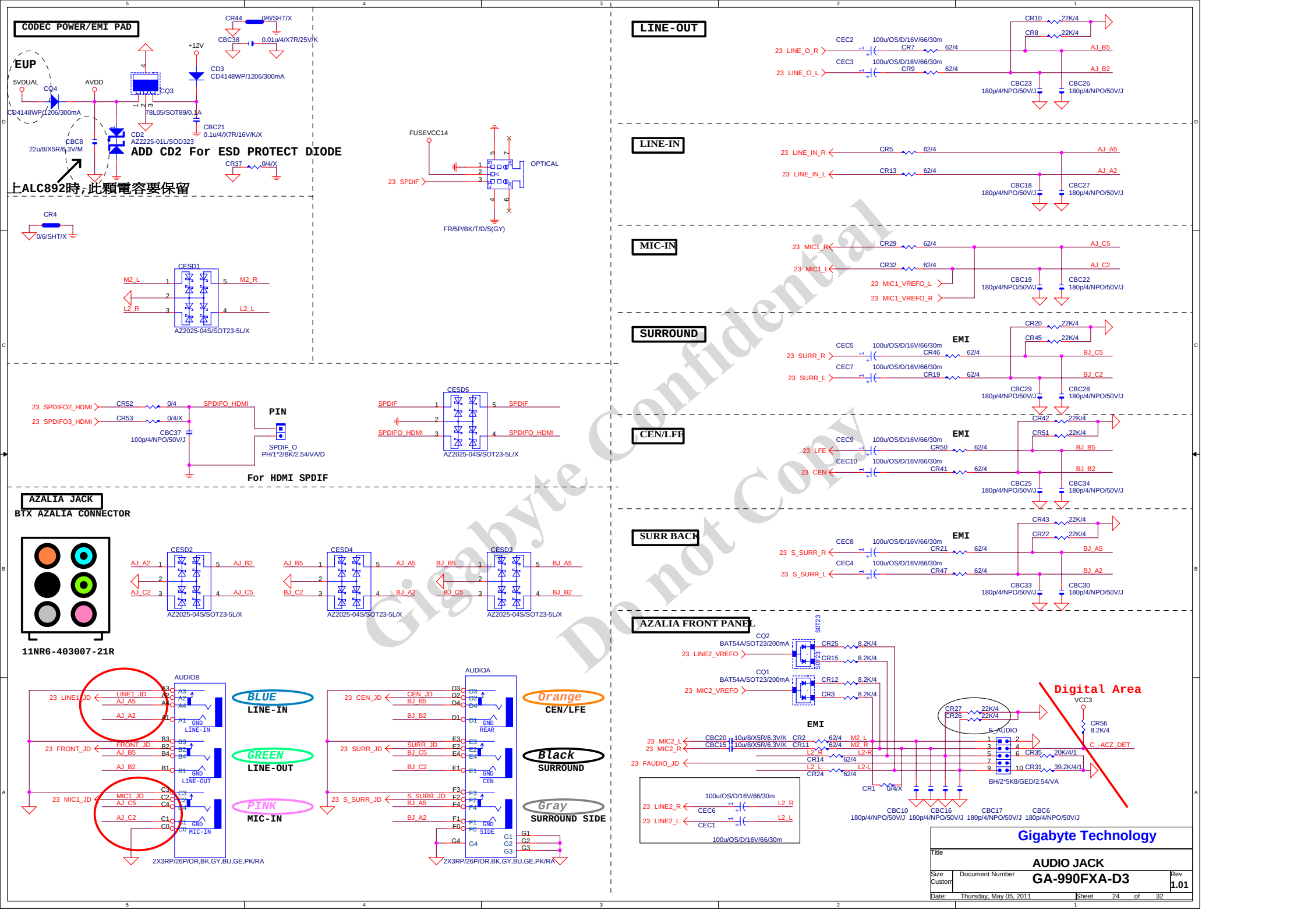
AZALIA CODEC

ALC889/ALC889B/ALC892/ALC898 Colay

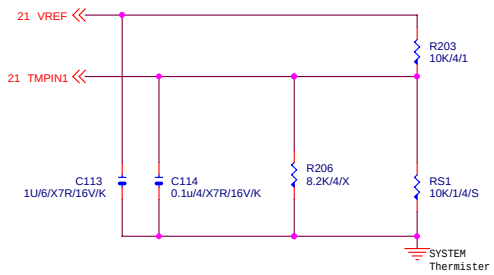
	ALC889	ALC889B	ALC898/ALC892
CR65	0	0	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	0	X	0
CR66	X	0	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	0
CD2/CD3/CQ3/CQ5	0	0	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm

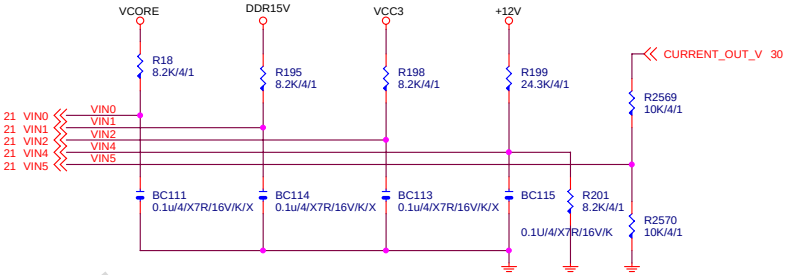


Gigabyte Technology	
Title	HD AUDIO ALC889A
Size: Custom	Document Number: GA-990FXA-D3
Rev	1.01
Date: Thursday, May 05, 2011	Sheet 23 of 32

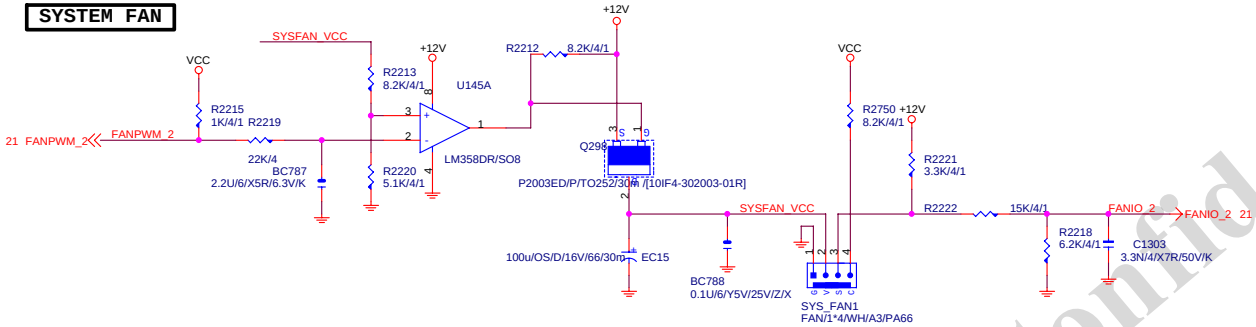

CODEC POWER/EMI PAD
EUP
5VDUAL
AVDD
CD4
CD4148WP/1206/300mA
CR44 0/6/SHT/X
CBC38 0.01u/4/X7R/25V/K
+12V
CD3
CD4148WP/1206/300mA
CQ3
78L05/SOT89/0.1A
CBC21
0.1u/4/X7R/16V/K/X
CBC8
22u/8/X5R/6.3V/M
CD2
AZ2225-01L/SOD323
ADD CD2 For ESD PROTECT DIODE
CR37 0/4/X
上ALC892時,此顆電容要保留
CR4
0/6/SHT/X
FUSEVCC14
23 SPDIF
OPTICAL
FR/5P/BK/T/D/S(GY)
CESD1
M2_L
L2_R
M2_R
L2_L
AZ2025-04S/SOT23-5L/X
23 SPDIFO2_HDMI
23 SPDIFO3_HDMI
CR52 0/4
CR53 0/4/X
CBC37
100p/4/NPO/50V/J
SPDIFO_HDMI
PIN
SPDIF_O
PH/1*2/BK/2.54/VA/D
For HDMI SPDIF
CESD5
SPDIF
SPDIFO_HDMI
AZ2025-04S/SOT23-5L/X
AZALIA JACK
BTX AZALIA CONNECTOR
11NR6-403007-21R
CESD2
CESD4
CESD3
AJ_A2
AJ_C2
AJ_B2
AJ_B5
AJ_A5
AJ_C5
BJ_B5
BJ_C2
BJ_A2
BJ_C5
BJ_A5
BJ_B2
AUDIOB
AUDIOA
23 LINE1_JD
23 FRONT_JD
23 MIC1_JD
23 CEN_JD
23 SURR_JD
23 S_SURR_JD
BLUE
LINE-IN
GREEN
LINE-OUT
PINK
MIC-IN
Orange
CEN/LFE
Black
SURROUND
Gray
SURROUND SIDE
2X3RP/26P/OR,BK,GY,BU,GE,PK/RA
LINE-OUT
23 LINE_O_R
23 LINE_O_L
CEC2
CEC3
100u/OS/D/16V/66/30m
CR7 62/4
CR9 62/4
CR10 22K/4
CR8 22K/4
AJ_B5
AJ_B2
CBC23
CBC26
180p/4/NPO/50V/J
LINE-IN
23 LINE_IN_R
23 LINE_IN_L
CR5 62/4
CR13 62/4
AJ_A5
AJ_A2
CBC18
CBC27
MIC-IN
23 MIC1_R
23 MIC1_L
CR29 62/4
CR32 62/4
23 MIC1_VREFO_L
23 MIC1_VREFO_R
AJ_C5
AJ_C2
CBC19
CBC22
SURROUND
EMI
23 SURR_R
23 SURR_L
CEC5
CEC7
CR46 62/4
CR19 62/4
CR20 22K/4
CR45 22K/4
BJ_C5
BJ_C2
CBC29
CBC28
CEN/LFE
23 LFE
23 CEN
CEC9
CEC10
CR50 62/4
CR41 62/4
CR42 22K/4
CR51 22K/4
BJ_B5
BJ_B2
CBC25
CBC34
SURR BACK
23 S_SURR_R
23 S_SURR_L
CEC8
CEC4
CR21 62/4
CR47 62/4
CR43 22K/4
CR22 22K/4
BJ_A5
BJ_A2
CBC33
CBC30
AZALIA FRONT PANEL
CQ2
CQ1
BAT54A/SOT23/200mA
SOT23
23 LINE2_VREFO
23 MIC2_VREFO
CR25 8.2K/4
CR15 8.2K/4
CR12 8.2K/4
CR3 8.2K/4
EMI
23 MIC2_L
23 MIC2_R
23 FAUDIO_JD
CBC20
CBC15
10u/8/X5R/6.3V/K
CR2
CR11
CR14
CR24
62/4
M2_L
M2_R
L2_R
L2_L
CR1 0/4/X
F_AUDIO
BH/2*5K8/GED/2.54/VA
Digital Area
VCC3
CR56 8.2K/4
C_-ACZ_DET
CR35 20K/4/1
CR31 39.2K/4/1
CR27 22K/4
CR26 22K/4
23 LINE2_R
23 LINE2_L
CEC6
CEC1
CBC10
CBC16
CBC17
CBC6
180p/4/NPO/50V/J
Gigabyte Confidential
Do not Copy
Gigabyte Technology
Title
AUDIO JACK
Size Custom
Document Number
GA-990FXA-D3
Rev 1.01
Date: Thursday, May 05, 2011
Sheet 24 of 32

Hardware Monitor circuits

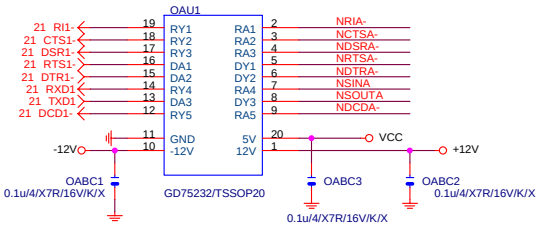




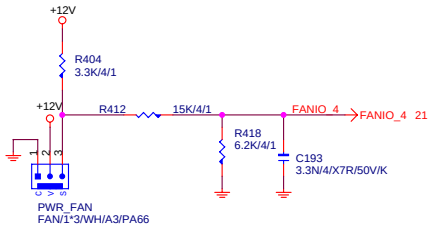
SYSTEM FAN



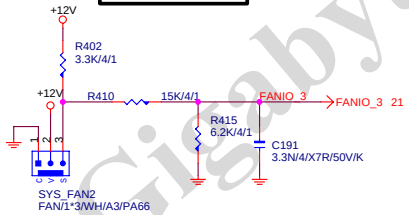
COMA



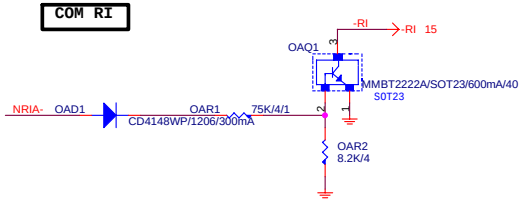
POWER FAN

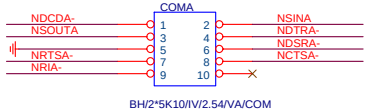


SYSTEM FAN2



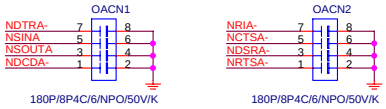
COM RI





BH/2*5K10/IV/2.54/VA/COM

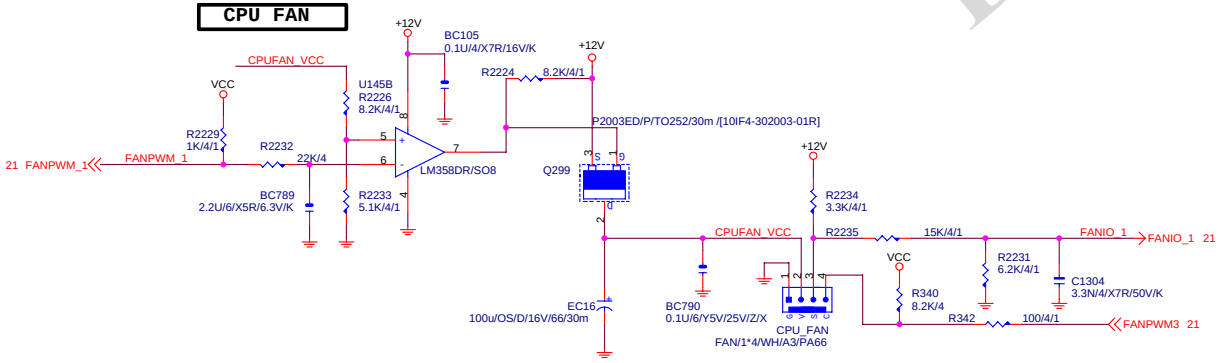
11NH3-000205-Y1R/Y2R



180P/8P4C/6/NPO/50V/K

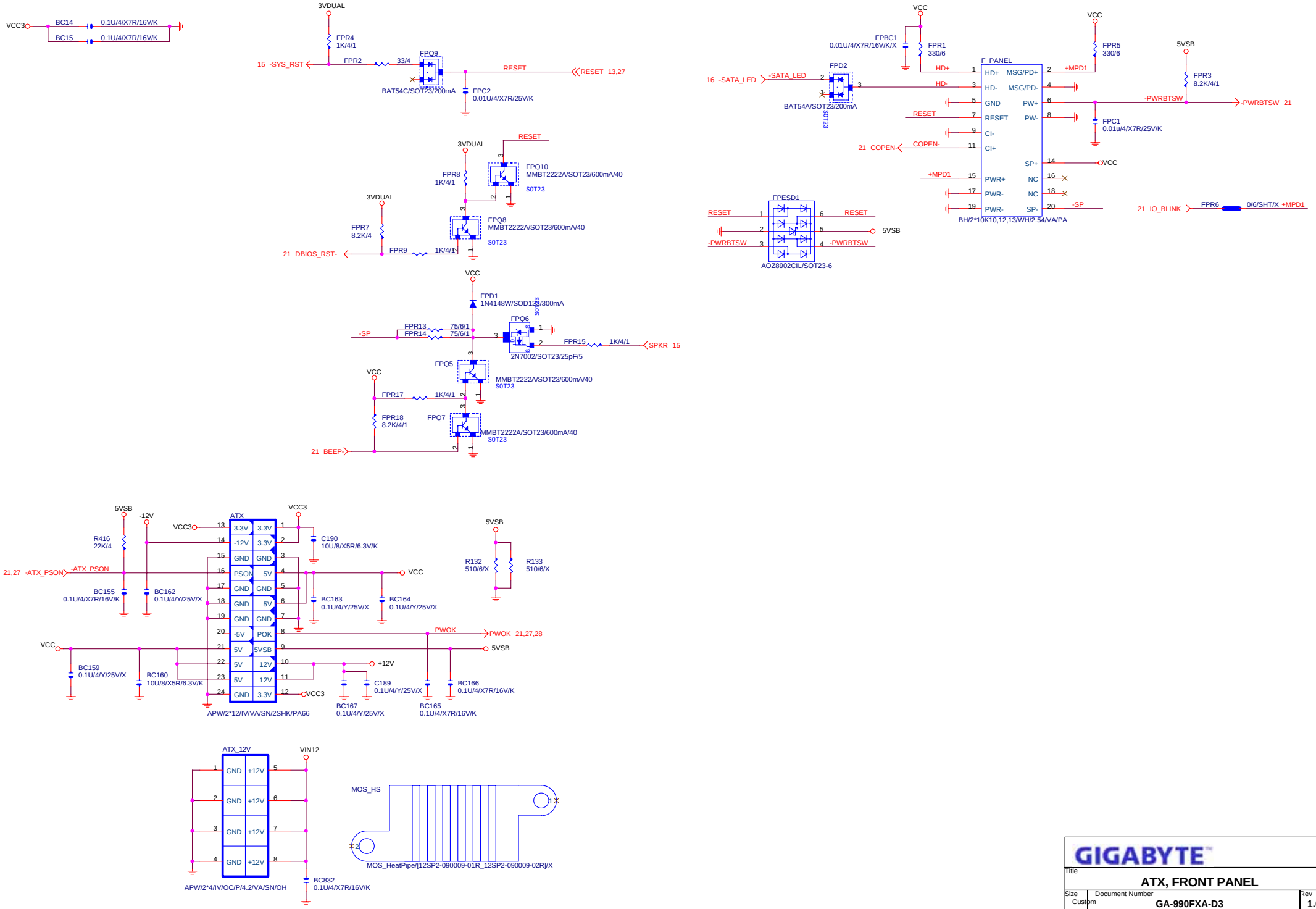
180P/8P4C/6/NPO/50V/K

CPU FAN



GIGABYTE

Title	FAN/HWMO/COM	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 25 of 32	

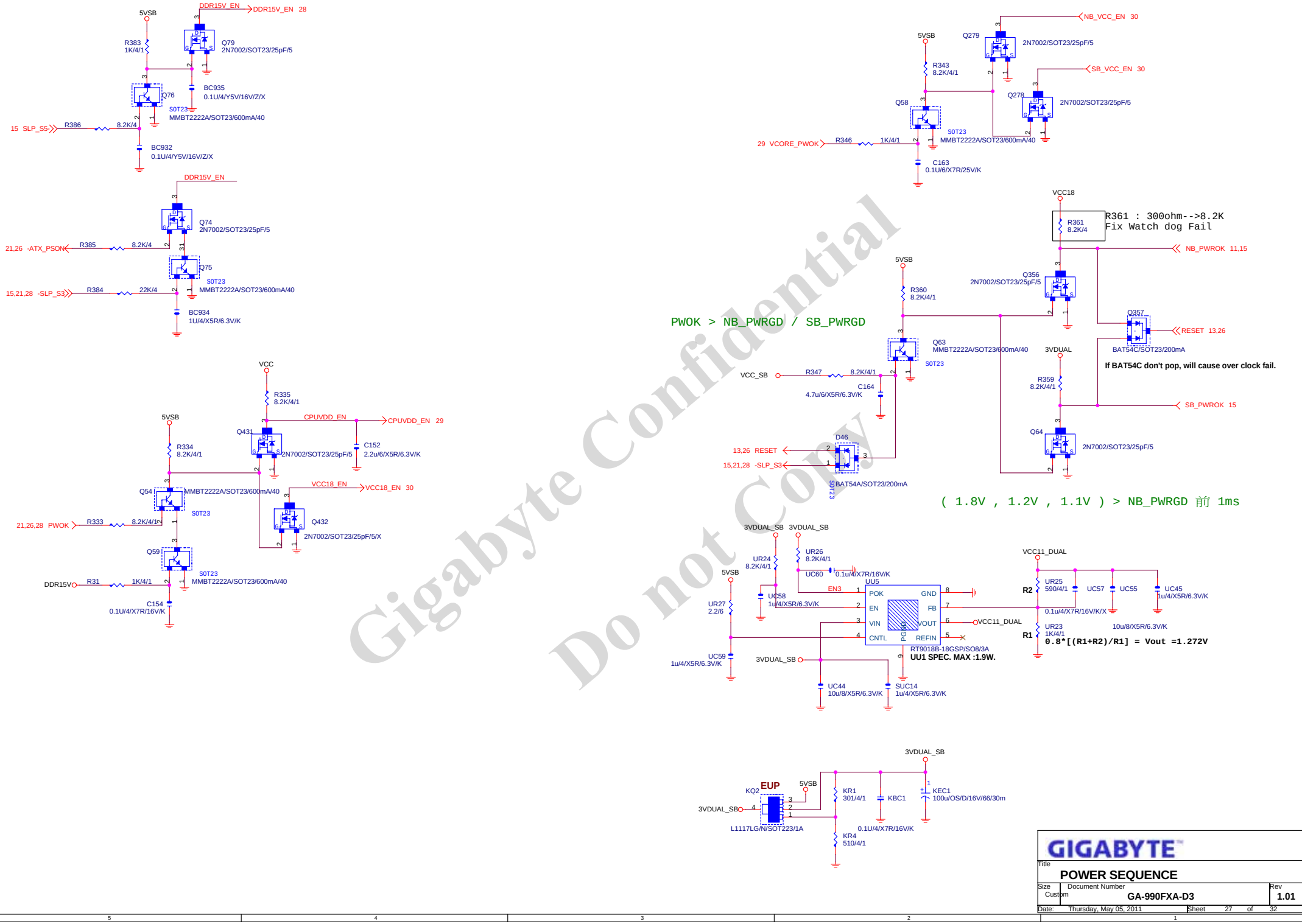


GIGABYTE

Title: ATX, FRONT PANEL

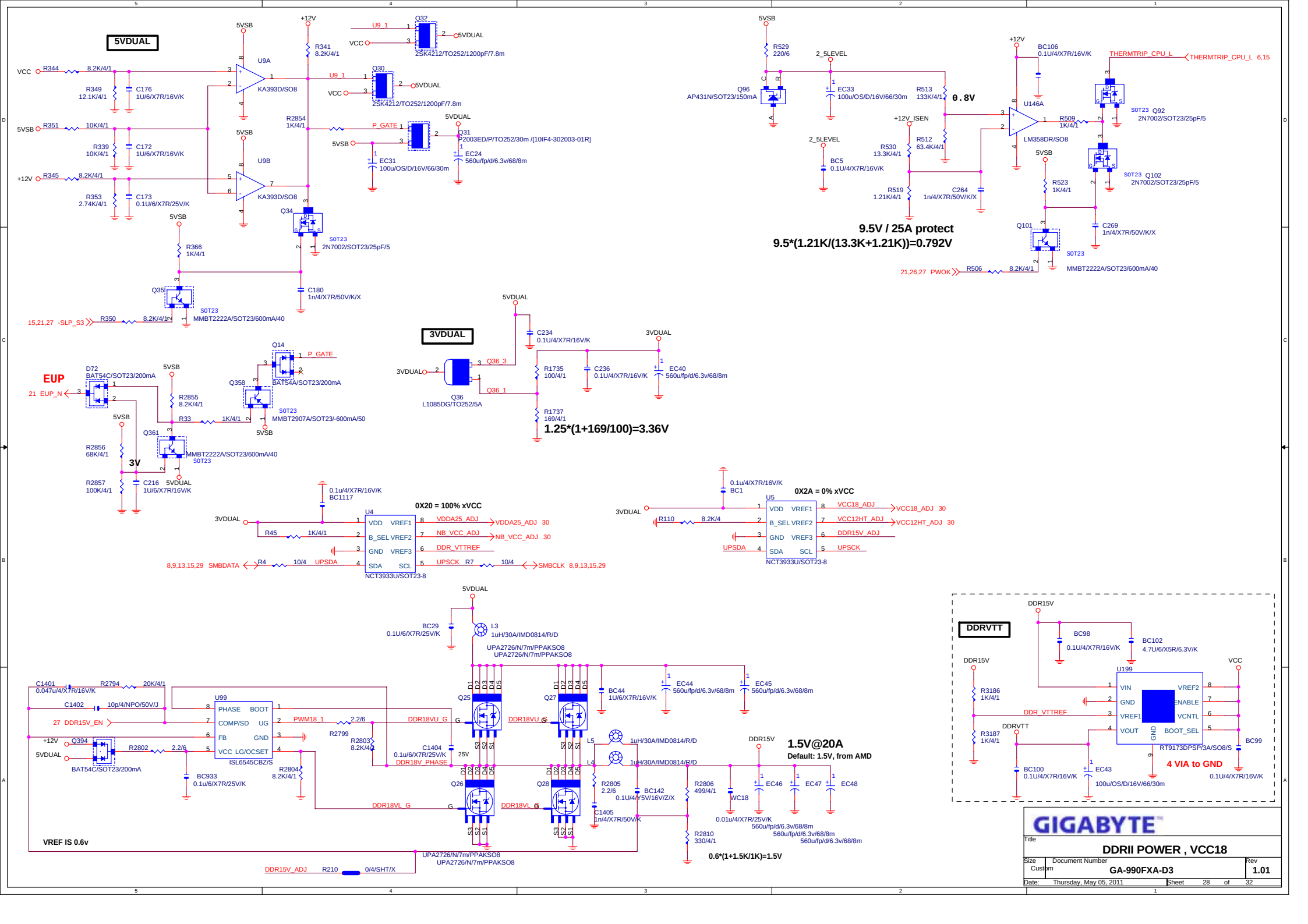
Size	Document Number	Rev
Custom	GA-990FXA-D3	1.01

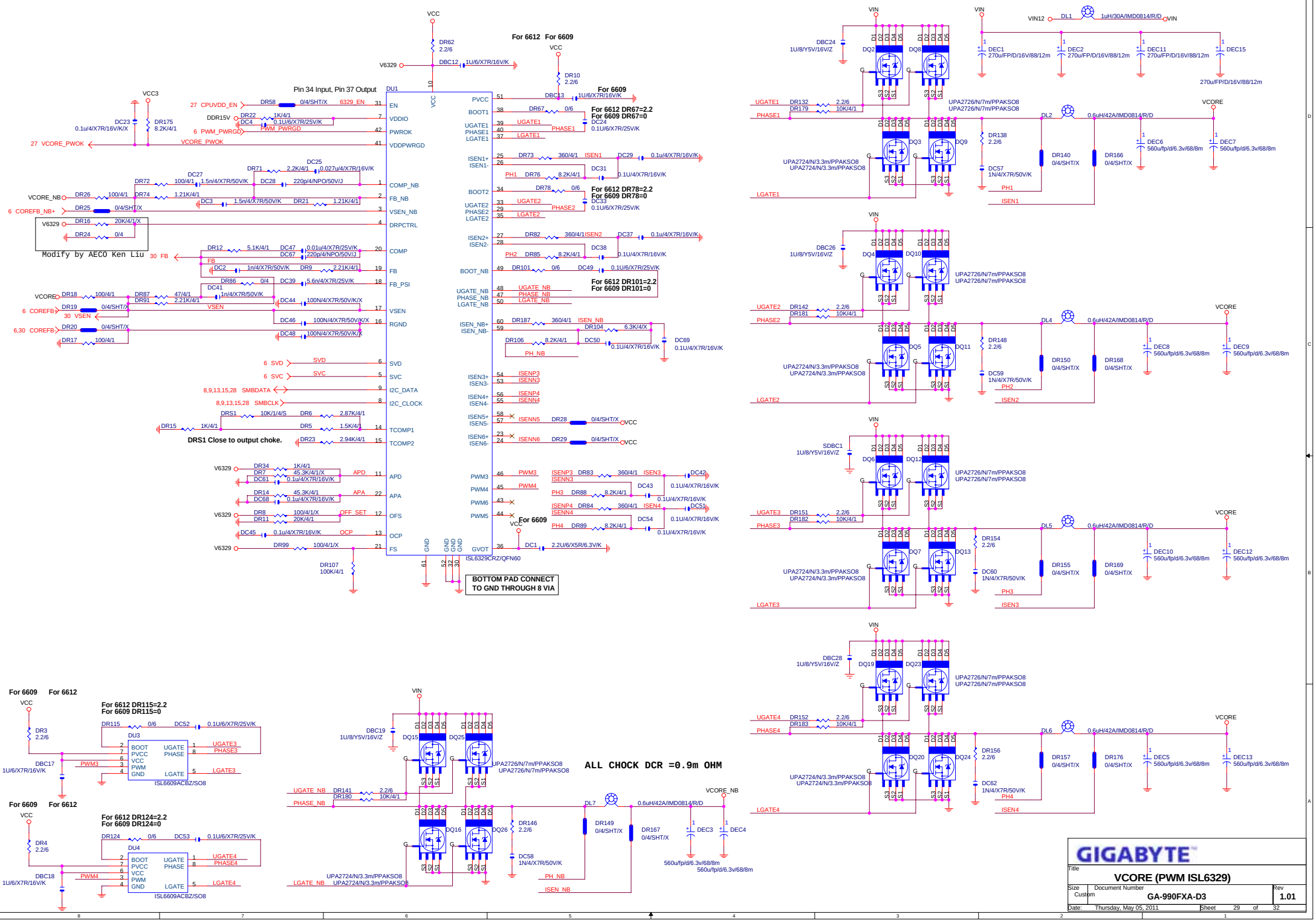
Date: Thursday, May 05, 2011 Sheet 26 of 32

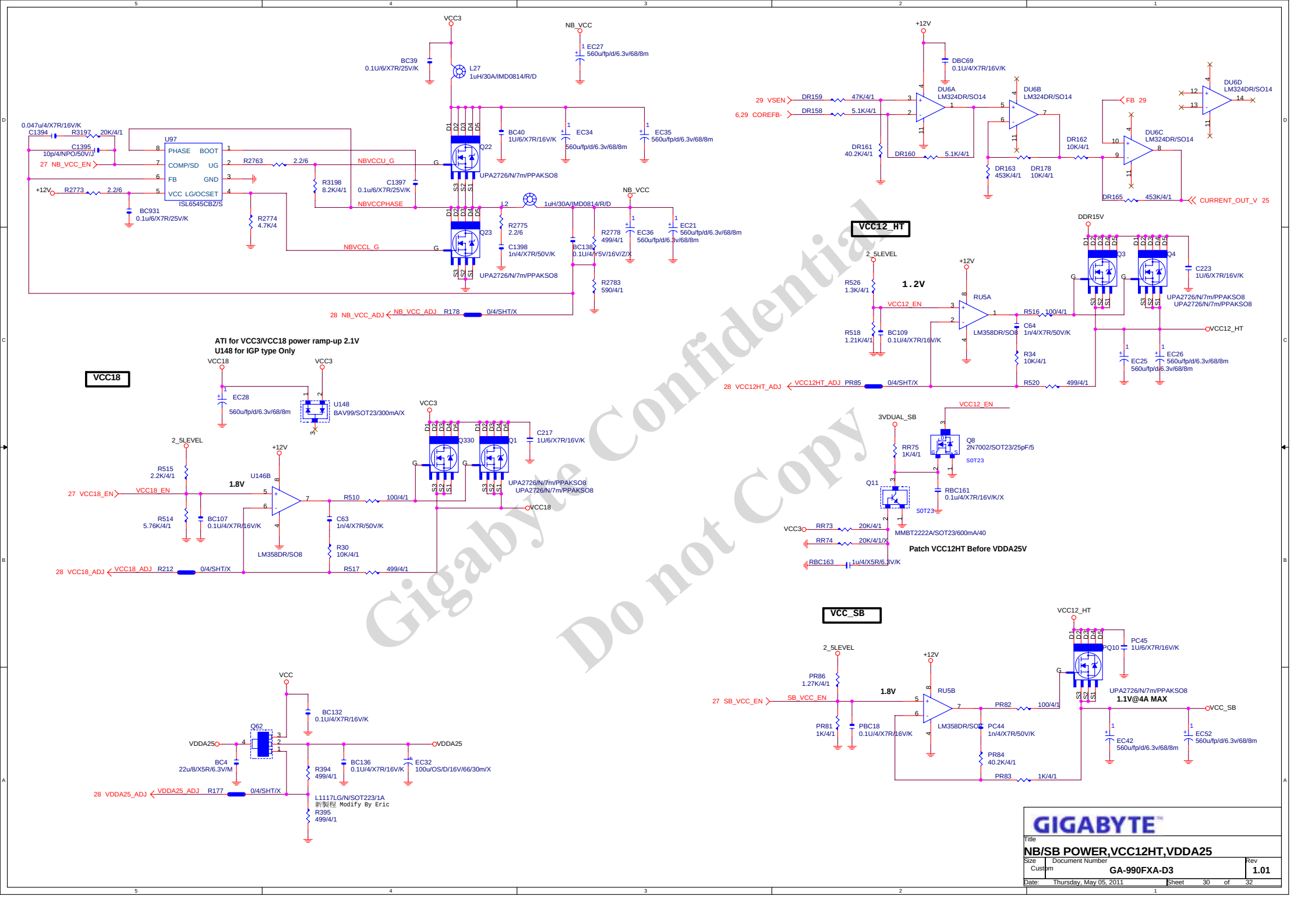


GIGABYTE

Title: POWER SEQUENCE		
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 27 of 32	


5VDUAL
U9A
KA393D/SO8
U9B
KA393D/SO8
Q32
2SK4212/TO252/1200pF/7.8m
Q30
2SK4212/TO252/1200pF/7.8m
Q31
P2003ED/P/TO252/30m /[10IF4-302003-01R]
Q34
S0T23
2N7002/SOT23/25pF/5
Q35
S0T23
MMBT2222A/SOT23/600mA/40
EC31
100u/OS/D/16V/66/30m
EC24
560u/fp/d/6.3v/68/8m
3VDUAL
Q36
L1085DG/TO252/5A
1.25*(1+169/100)=3.36V
EUP
Q14
BAT54A/SOT23/200mA
Q358
S0T23
MMBT2907A/SOT23/-600mA/50
Q361
S0T23
MMBT2222A/SOT23/600mA/40
3V
0X20 = 100% xVCC
U4
NCT3933U/SOT23-8
0X2A = 0% xVCC
U5
NCT3933U/SOT23-8
9.5V / 25A protect
9.5*(1.21K/(13.3K+1.21K))=0.792V
U146A
LM358DR/SO8
Q101
S0T23
MMBT2222A/SOT23/600mA/40
U99
ISL6545CBZ/S
Q394
BAT54C/SOT23/200mA
Q25
Q26
Q27
Q28
1.5V@20A
Default: 1.5V, from AMD
VREF IS 0.6v
0.6*(1+1.5K/1K)=1.5V
DDRVTT
U199
RT9173DPSP/3A/SO8/S
4 VIA to GND
GIGABYTE
DDRII POWER , VCC18
GA-990FXA-D3
1.01
Thursday, May 05, 2011
Sheet 28 of 32


For 6612 For 6609
Pin 34 Input, Pin 37 Output
Modify by AECO Ken Liu
DRS1 Close to output choke.
For 6612 DR67=2.2
For 6609 DR67=0
For 6612 DR78=2.2
For 6609 DR78=0
For 6612 DR101=2.2
For 6609 DR101=0
BOTTOM PAD CONNECT
TO GND THROUGH 8 VIA
ISL6329CRZ/QFN60
For 6612 DR115=2.2
For 6609 DR115=0
For 6612 DR124=2.2
For 6609 DR124=0
ISL6609ACBZ/SO8
ALL CHOCK DCR =0.9m OHM
VCORE (PWM ISL6329)
GA-990FXA-D3
1.01
Thursday, May 05, 2011
29 of 32



PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

FOR DSM MODE
(DEEP SLUMBER MODE)

ENABLE SW

Dual Color LED
D4 D3 Green
D4 D3 Orange

Single Color LED
D2 D1 Yellow

P35-152-19W9

(CLOSE LU1)

(PIN3,6,9,13,29,41,45)

CLOSE LL2

(PIN21)

離IC近越好

USB_LAN

USB 3.0 ESD protect.

USB3.0/2.0

Close to USB30_LAN

Close to USB30_LAN

90歐姆:[20/4.5/7.5/4.5/20]

UP

DOWN

USB+LAN/1G/GO,Y/OS/RA/D/1/RED

EMI

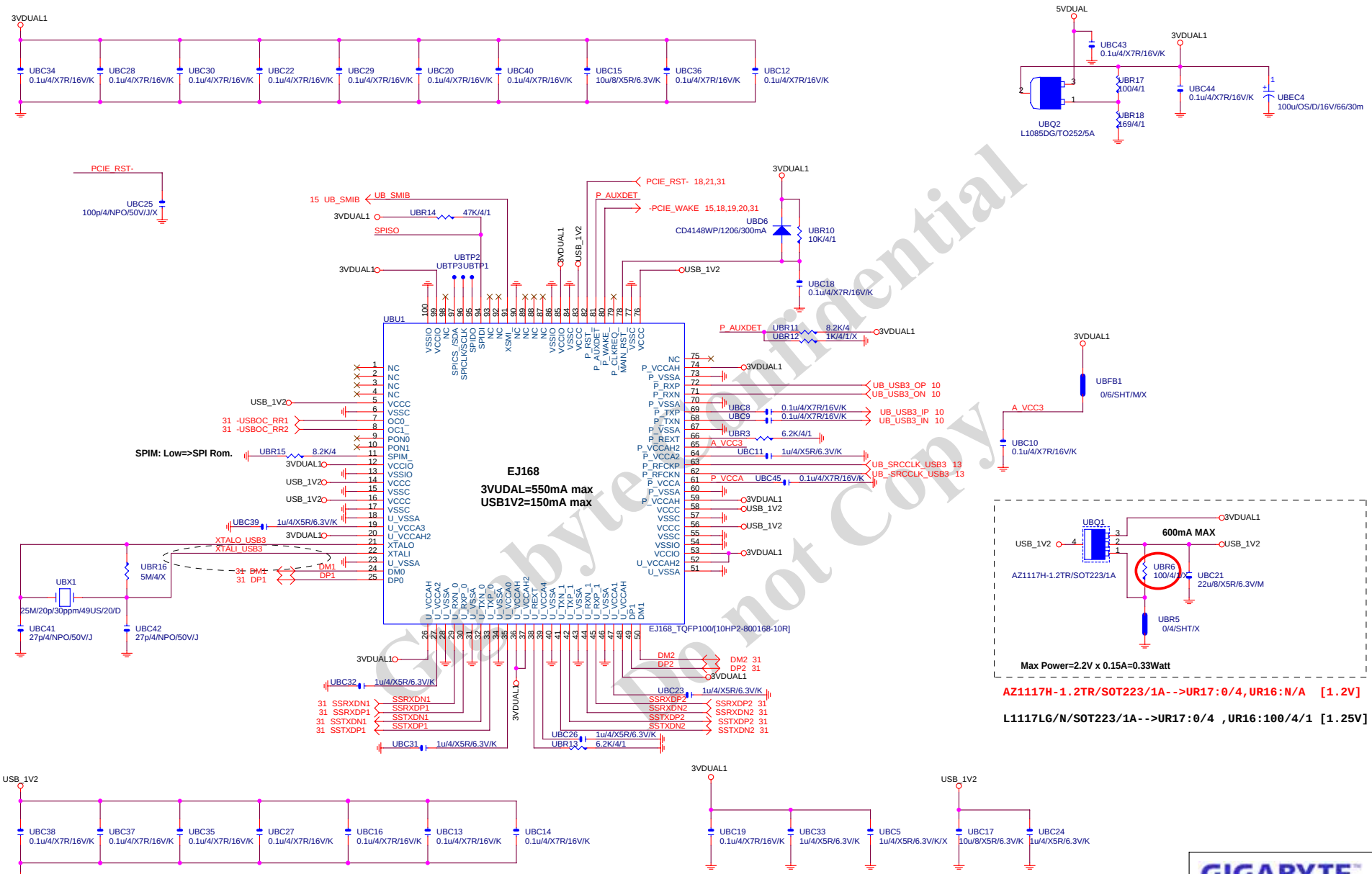
USB/18P/BU/OS/RA/D/2/SB

GIGABYTE

Title: REALTK RTL8111C/8101E

Size: Custom | Document Number: GA-990FXA-D3 | Rev: 1.01

Date: Thursday, May 05, 2011 | Sheet 31 of 32



GIGABYTE

Title	EJ168 R_USB30	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.01
Date: Thursday, May 05, 2011	Sheet 32 of 32	