GA-990FXA-D3

Revision : 1.0

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Model Name:GA-990FXA-D3

Component value change history

Version: 1.0

4 Layer, 4mil 50ohm +/- 15% B

P-Code: U98145-0

Date	Version		Change Items
2011.03.17	0.1 New BOM Release.	PCB:0.1	Modify from 9M990FXA5-00-01
2011.04.13	1.0A BOM Release.	PCB:1.0	Add AMD Validation parts ,Add Thermal-Die schematic
2011.04.13	1.0A BOM Release.	PCB:1.0	Modify from 9M990FXA3-00-10A
2011.05.06	1.0B BOM Release.	PCB:1.01	Remove PCB silkscreen SLI logo
2011.05.27	1.0C BOM Release.	PCB:1.0	Change PCB to 1.0 (W/SLI LOGO) & add 依利安達 ISL6545 for DDR power VCC pin BC933 0.1u change to 1uF/X7R

Circuit or PCB layout change for next version

AM2-->AM3 Different: AE9-->AE7, H22-->H20. Extra pin:B2 AM3 socket is 938 pins. Only shift 2 pins.

Date	Version	Reason
2011.03.16	0.1 Gerber-out	Modify from GA-990FXA-UD5 Rev 0.1
2011.04.12	1.0 Gerber-out	Add AMD Validation parts ,Add Thermal-Die schematic
2011.04.12	1.0 Gerber-out	Modify from GA-990FXA-UD3 Rev 1.0
2011.05.05	1.01 Gerber-out	Remove PCB silkscreen SLI logo

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Title: BOM & PCB HISTORY

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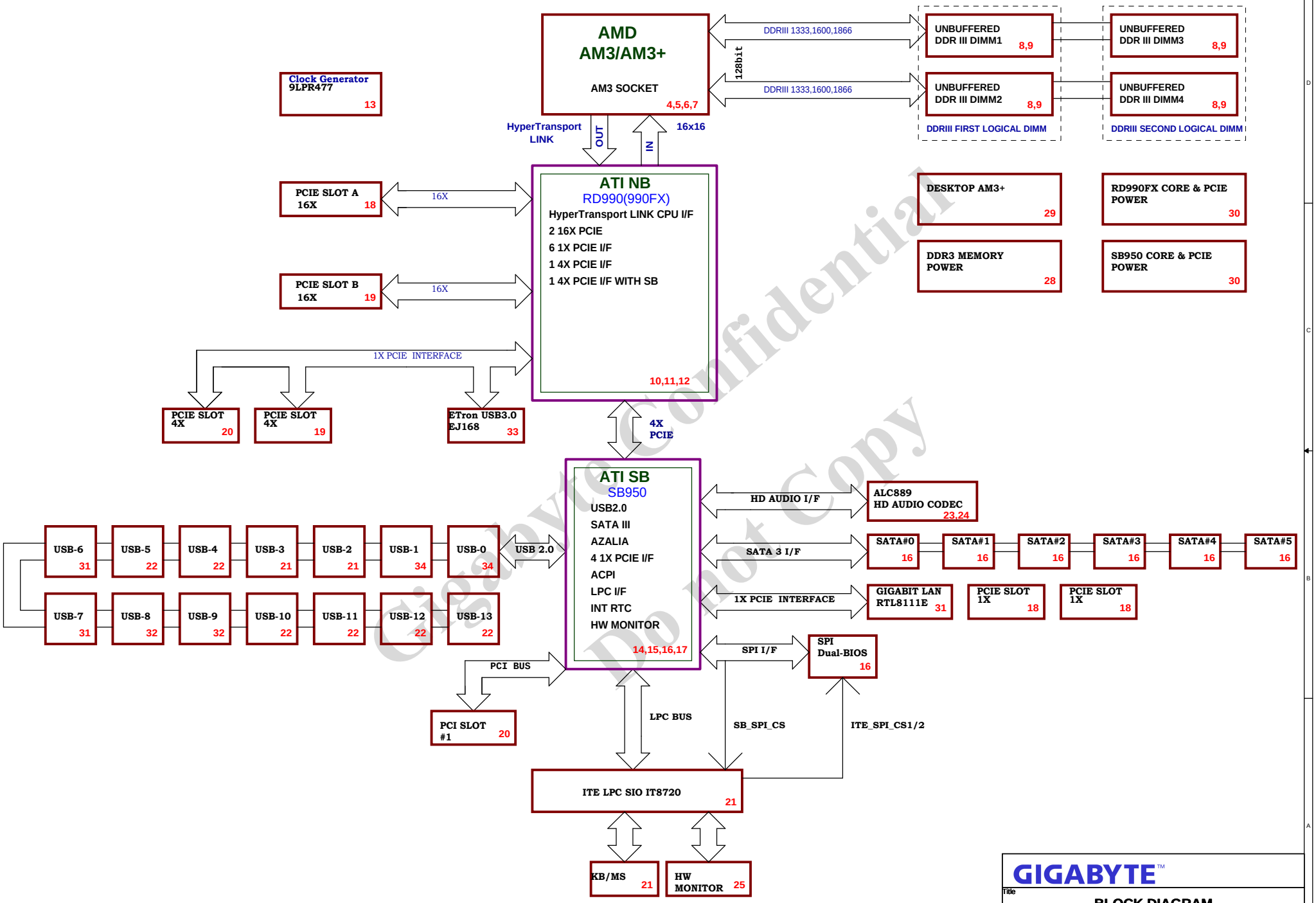

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Title	BLOCK DIAGRAM	
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L0_CADIN_L[0..15]
L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

VCORE
AC1 100P/4/NPO/50V/J/X
AC2 100P/4/NPO/50V/J/X
AC3 100P/4/NPO/50V/J/X
HT_BUS Vcore use

MH3 HOLE_3/X
MH9 HOLE_3/X
MH8 HOLE_3/X
MH1 HOLE_3/X
MH2 HOLE_3/X
MH4 HOLE_3/X
MH7 HOLE_3/X
MH5 HOLE_3/X
MH6 HOLE_3/X

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

K1 K1_ICT/X
K2 K1_ICT/X
K3 K1_ICT/X
K4 K1_ICT/X
K5 K1_ICT/X
K6 K1_ICT/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

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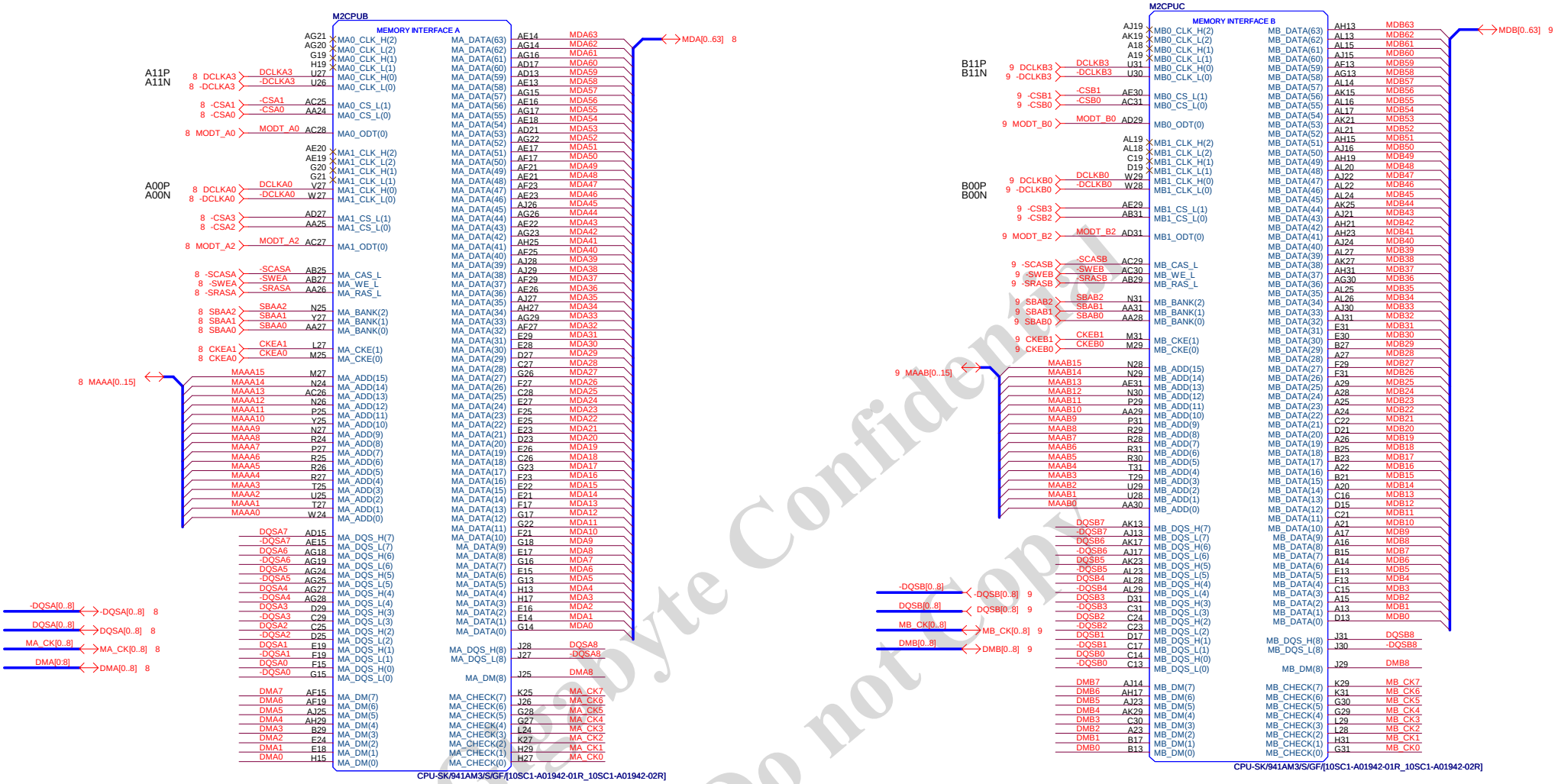

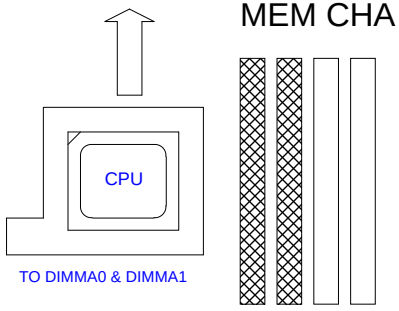

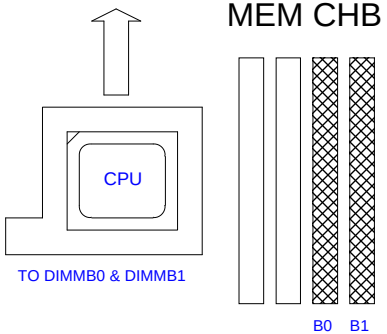

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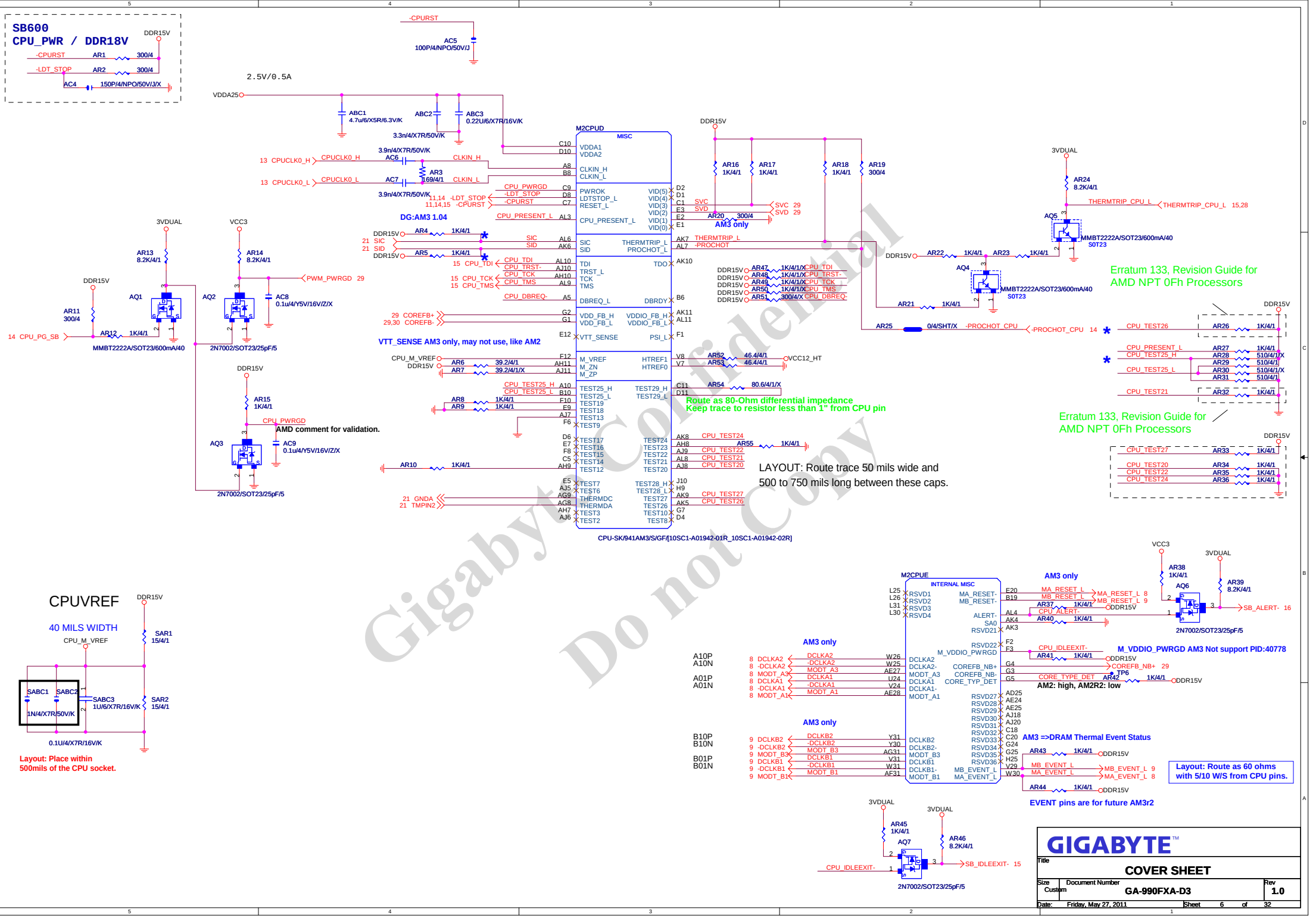

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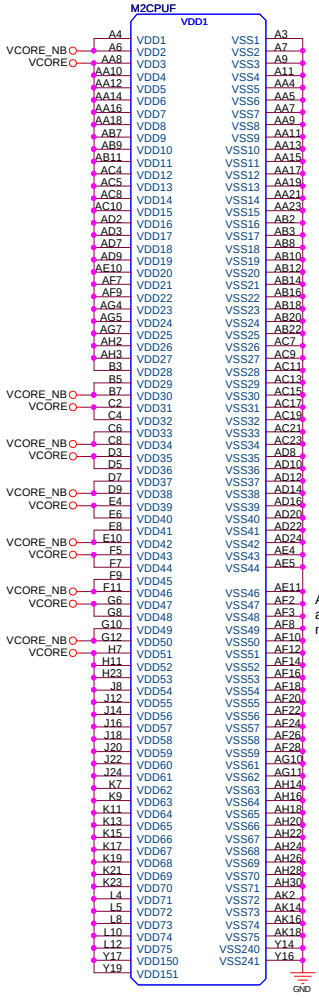
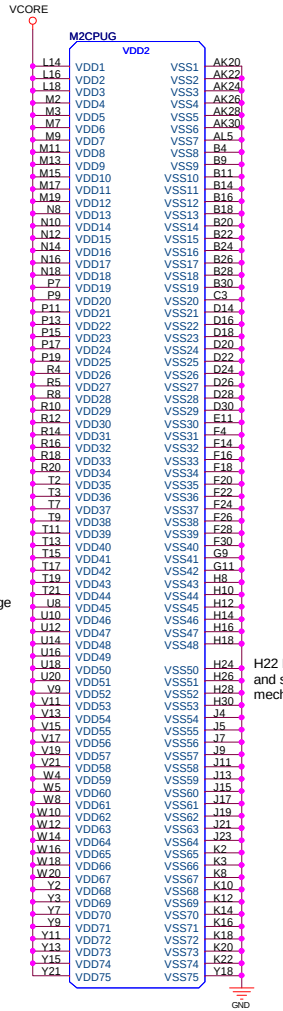
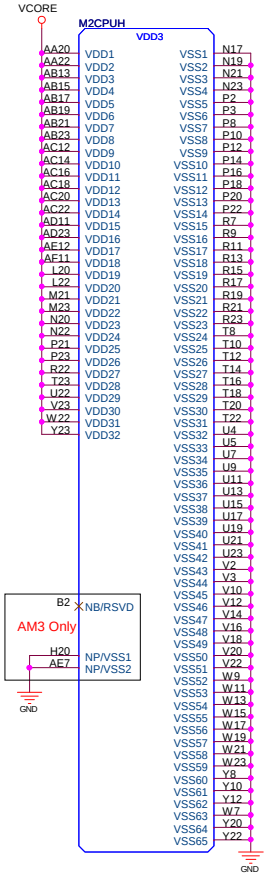
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

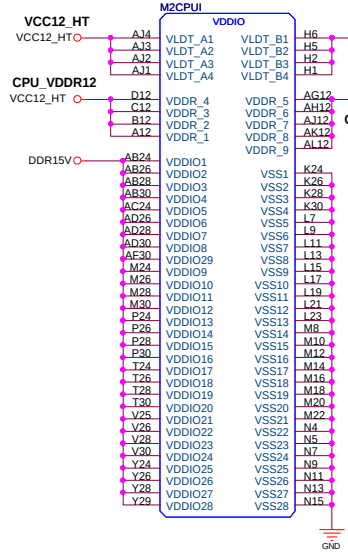


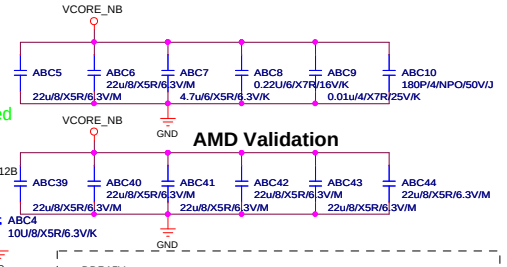
AE9 Missing pins on package and socket used for mechanical keying. =>AM3

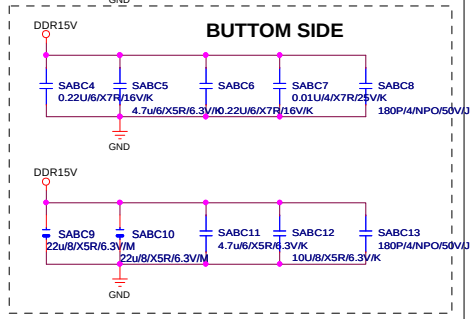


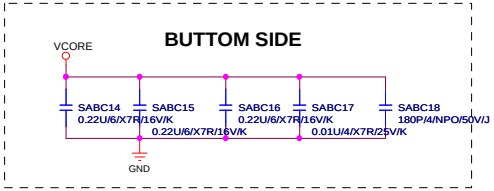


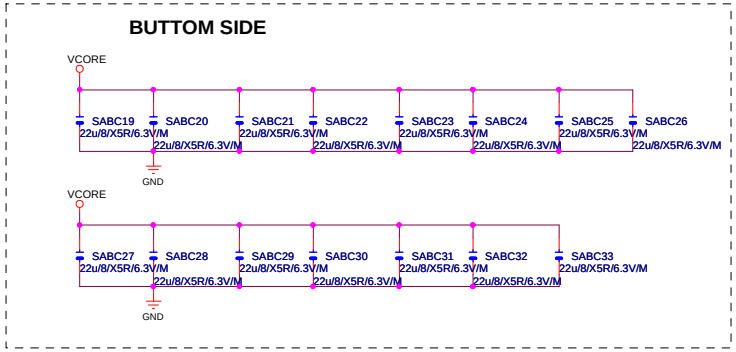
H22 Missing pins on package and socket used for mechanical keying. =>AM3

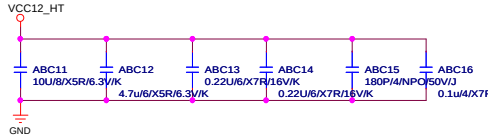


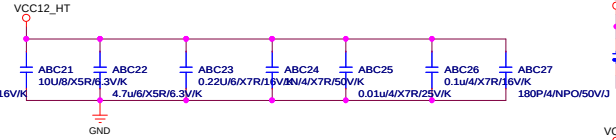


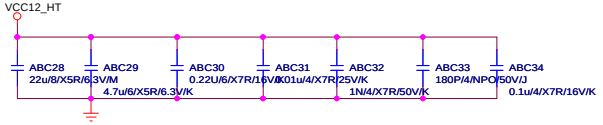


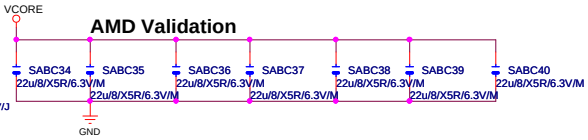


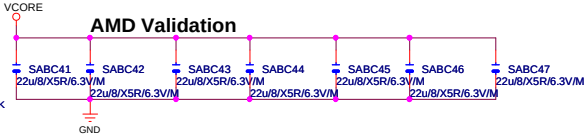


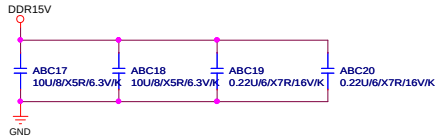


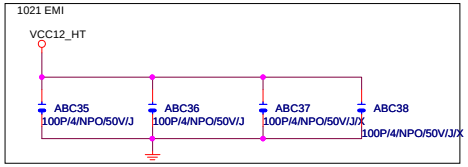












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Title	CPU POWER & GND	
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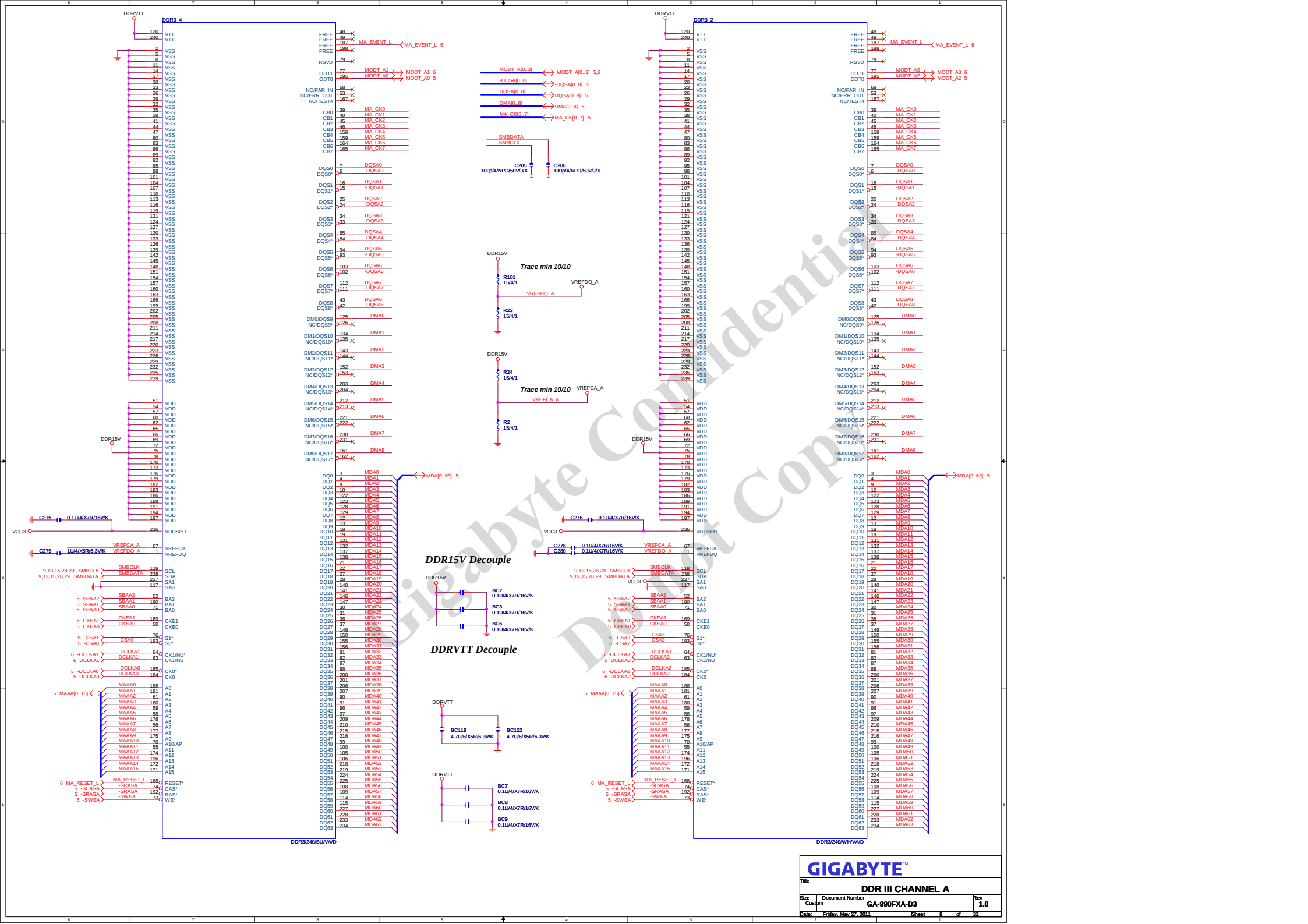

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Title: DDR III CHANNEL A

Size	Document Number	Rev
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DDR3_3
DDR3/240/BU/VA/D
DDR3_1
DDR3/240/W/H/VA/D
DDRVTT
DDR15V
VCC3
VREFCA_A
VREFDQ_A
VREFCA
VREFDQ
VDDSPD
SCL
SDA
SA0
SA1
BA0
BA1
BA2
CKE0
CKE1
S0*
CK0
CK1/NU
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
RESET*
CAS*
RAS*
WE*
MB_EVENT_L
MODT_B1
MODT_B0
MODT_B3
MODT_B2
MB_CK0
MB_CK1
MB_CK2
MB_CK3
MB_CK4
MB_CK5
MB_CK6
MB_CK7
DQSB0
DQSB1
DQSB2
DQSB3
DQSB4
DQSB5
DQSB6
DQSB7
DQSB8
DMB0
DMB1
DMB2
DMB3
DMB4
DMB5
DMB6
DMB7
DMB8
MDB[0..63]
MAAB[0..15]
-DQSB[0..8]
DQSB[0..8]
DMB[0..8]
MODT_B[0..3]
MB_CK[0..7]
DDR15V Decouple
DDRVTT Decouple
BC131 0.1U/4/X7R/16V/K
BC129 0.1U/4/X7R/16V/K
BC125 0.1U/4/X7R/16V/K
BC148 0.1U/4/X7R/16V/K
BC149 0.1U/4/X7R/16V/K
BC11 22U/8/X5R/6.3V/M
BC10 22U/8/X5R/6.3V/M
C283 0.1U/4/X7R/16V/K
C285 0.1U/4/X7R/16V/K
C284 0.1U/4/X7R/16V/K
C286 0.1U/4/X7R/16V/K
GIGABYTE
Title
DDR III CHANNEL B
Size
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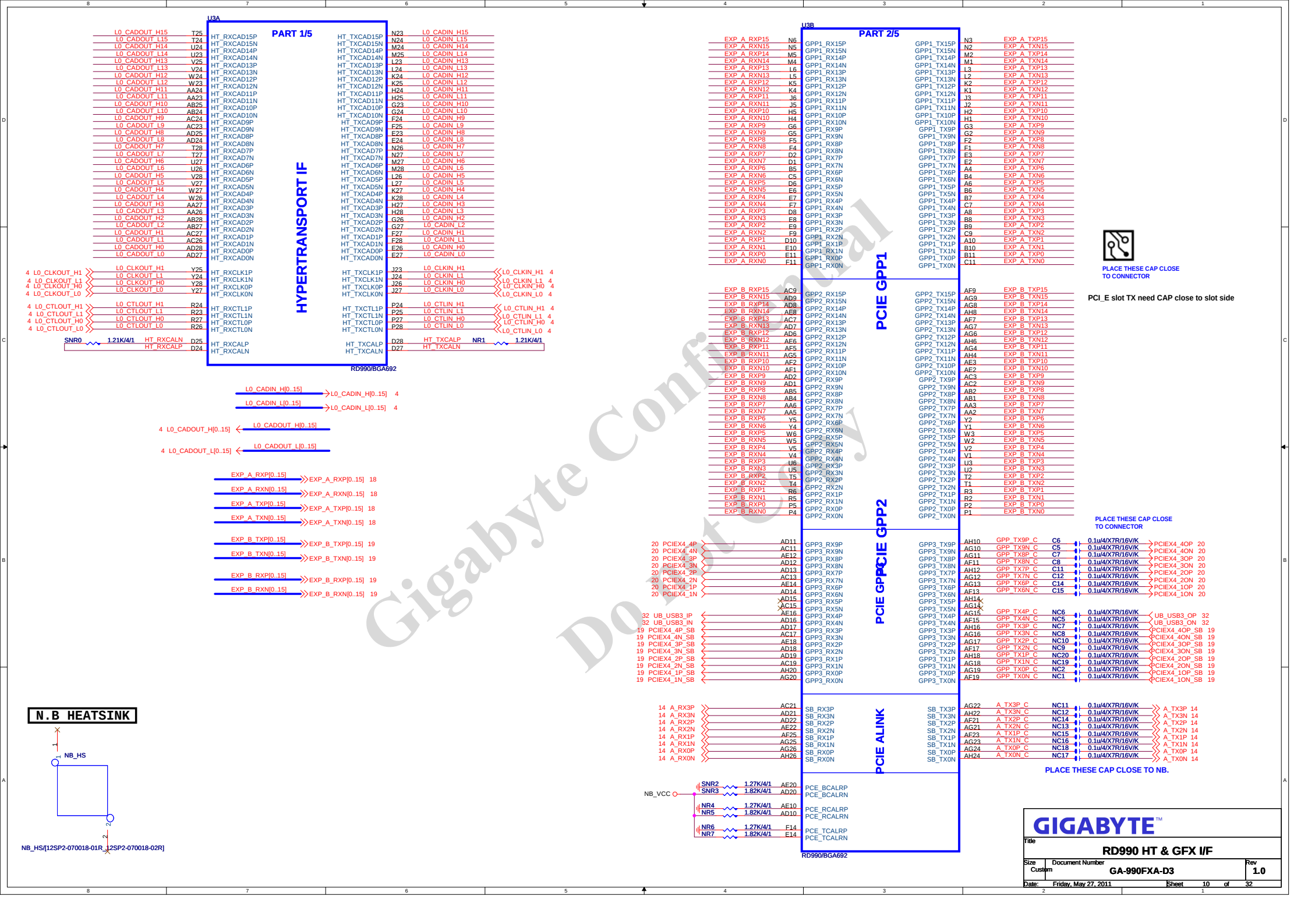
U3A
PART 1/5
HYPERTRANSPORT IF
RD990/BGA692
U3B
PART 2/5
PCIE GPP1
PCIE GPP2
PCIE GPP3
PCIE ALINK
RD990/BGA692
N.B HEATSINK
NB_HS
NB_HS/[12SP2-070018-01R_12SP2-070018-02R]
PLACE THESE CAP CLOSE TO CONNECTOR
PCI_E slot TX need CAP close to slot side
PLACE THESE CAP CLOSE TO NB.
GIGABYTE
RD990 HT & GFX I/F
GA-990FXA-D3
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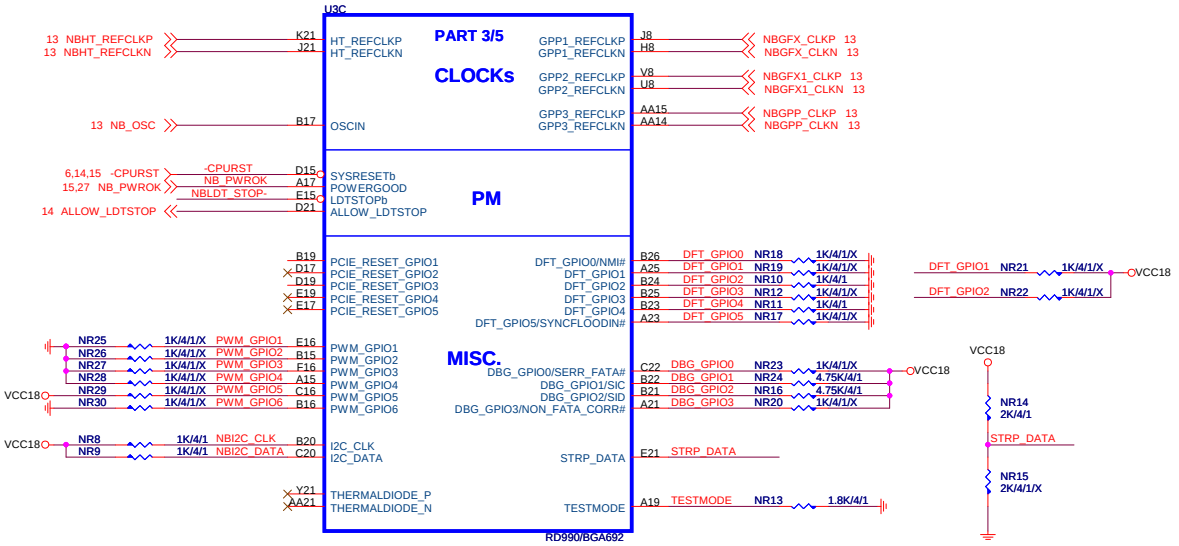
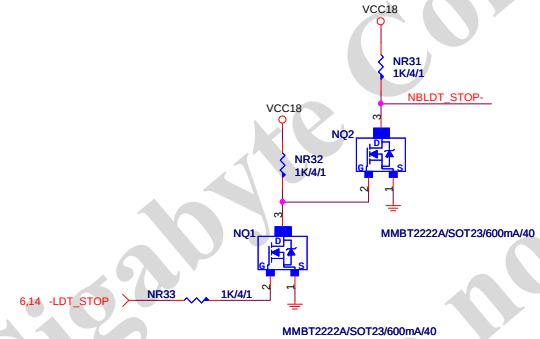
Do Not Copy





DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

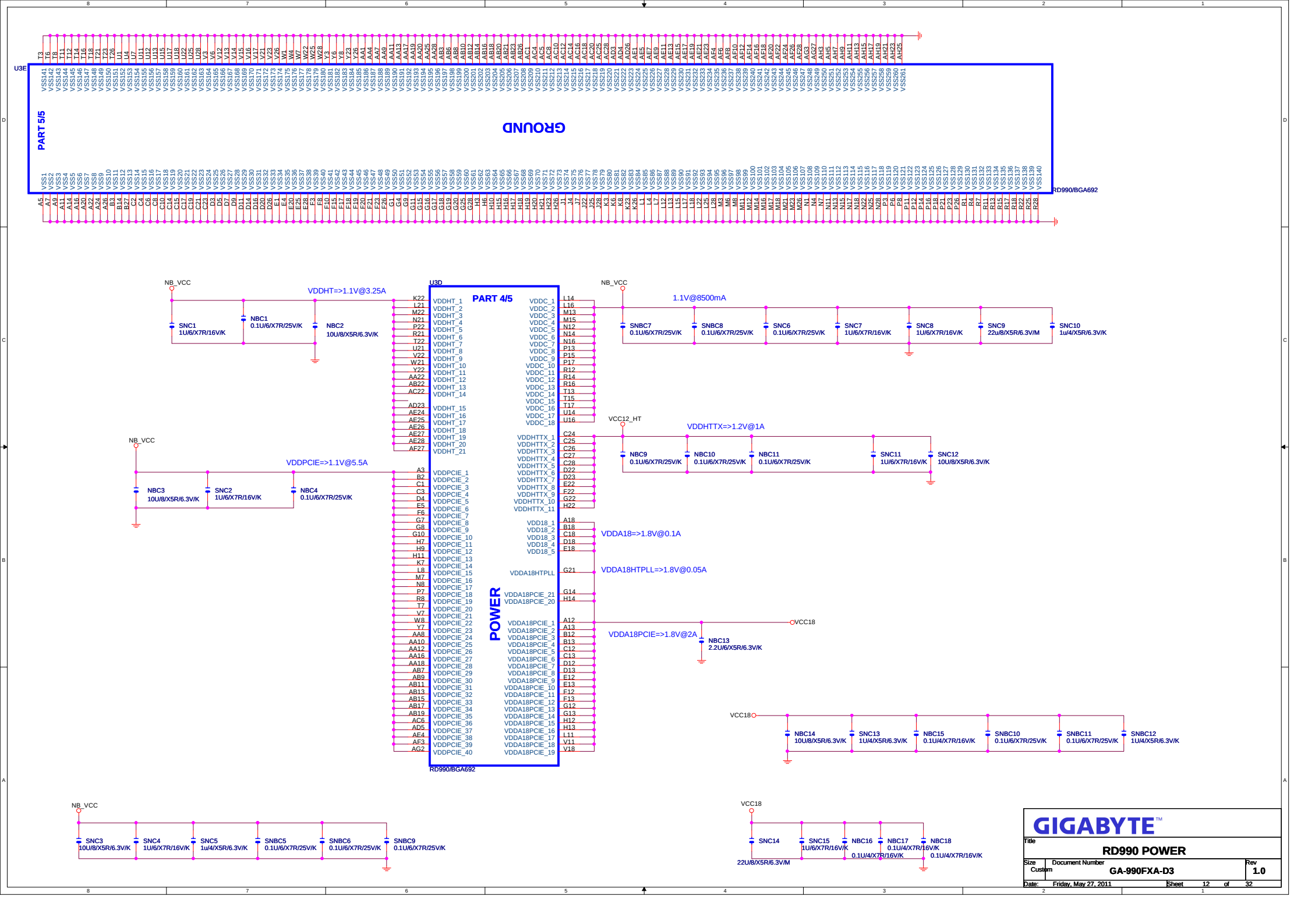
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

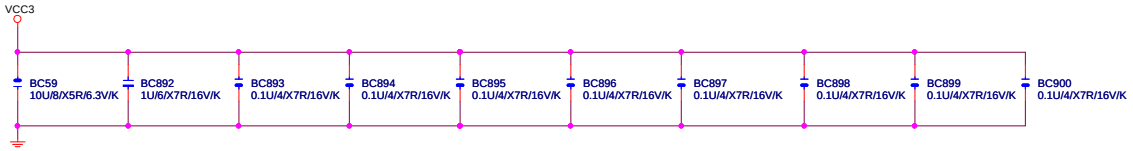
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE™

Title	RD990 CLOCK & SYSB I/F	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.0
Date: Friday, May 27, 2011	Sheet 11 of 32	

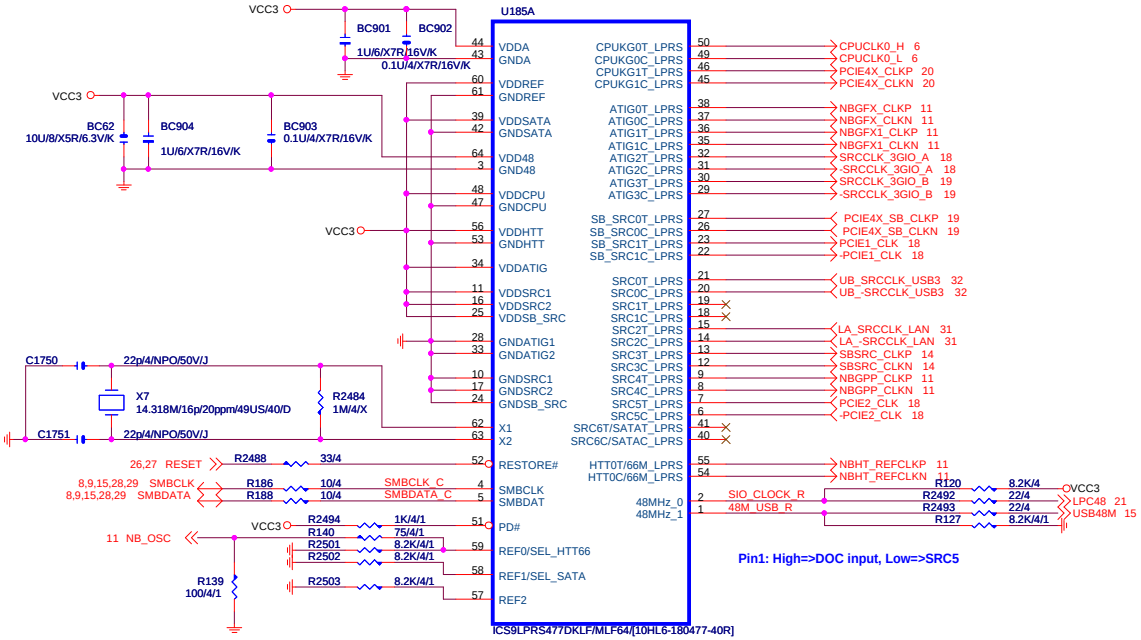

U3E
PART 5/5
GROUND
RD990/BGA692
U3D
PART 4/5
POWER
RD990/BGA692
NB_VCC
VDDHT=>1.1V@3.25A
SNC1 1U/6/X7R/16V/K
NBC1 0.1U/6/X7R/25V/K
NBC2 10U/8/X5R/6.3V/K
1.1V@8500mA
SNBC7 0.1U/6/X7R/25V/K
SNBC8 0.1U/6/X7R/25V/K
SNC6 0.1U/6/X7R/25V/K
SNC7 1U/6/X7R/16V/K
SNC8 1U/6/X7R/16V/K
SNC9 22u/8/X5R/6.3V/M
SNC10 1u/4/X5R/6.3V/K
VCC12_HT
VDDHTTX=>1.2V@1A
NBC9 0.1U/6/X7R/25V/K
NBC10 0.1U/6/X7R/25V/K
NBC11 0.1U/6/X7R/25V/K
SNC11 1U/6/X7R/16V/K
SNC12 10U/8/X5R/6.3V/K
VDDPCIE=>1.1V@5.5A
NBC3 10U/8/X5R/6.3V/K
SNC2 1U/6/X7R/16V/K
NBC4 0.1U/6/X7R/25V/K
VDDA18=>1.8V@0.1A
VDDA18HTPLL=>1.8V@0.05A
VCC18
VDDA18PCIE=>1.8V@2A
NBC13 2.2U/6/X5R/6.3V/K
NBC14 10U/8/X5R/6.3V/K
SNC13 1U/4/X5R/6.3V/K
NBC15 0.1U/4/X7R/16V/K
SNBC10 0.1U/6/X7R/25V/K
SNBC11 0.1U/6/X7R/25V/K
SNBC12 1U/4/X5R/6.3V/K
SNC3 10U/8/X5R/6.3V/K
SNC4 1U/6/X7R/16V/K
SNC5 1u/4/X5R/6.3V/K
SNBC5 0.1U/6/X7R/25V/K
SNBC6 0.1U/6/X7R/25V/K
SNBC9 0.1U/6/X7R/25V/K
SNC14 22U/8/X5R/6.3V/M
SNC15 1U/6/X7R/16V/K
NBC16 0.1U/4/X7R/16V/K
NBC17 0.1U/4/X7R/16V/K
NBC18 0.1U/4/X7R/16V/K
GIGABYTE
Title
RD990 POWER
Size
Custom
Document Number
GA-990FXA-D3
Rev
1.0
Date: Friday, May 27, 2011
Sheet 12 of 32



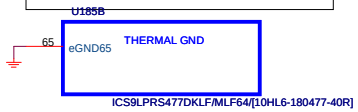
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

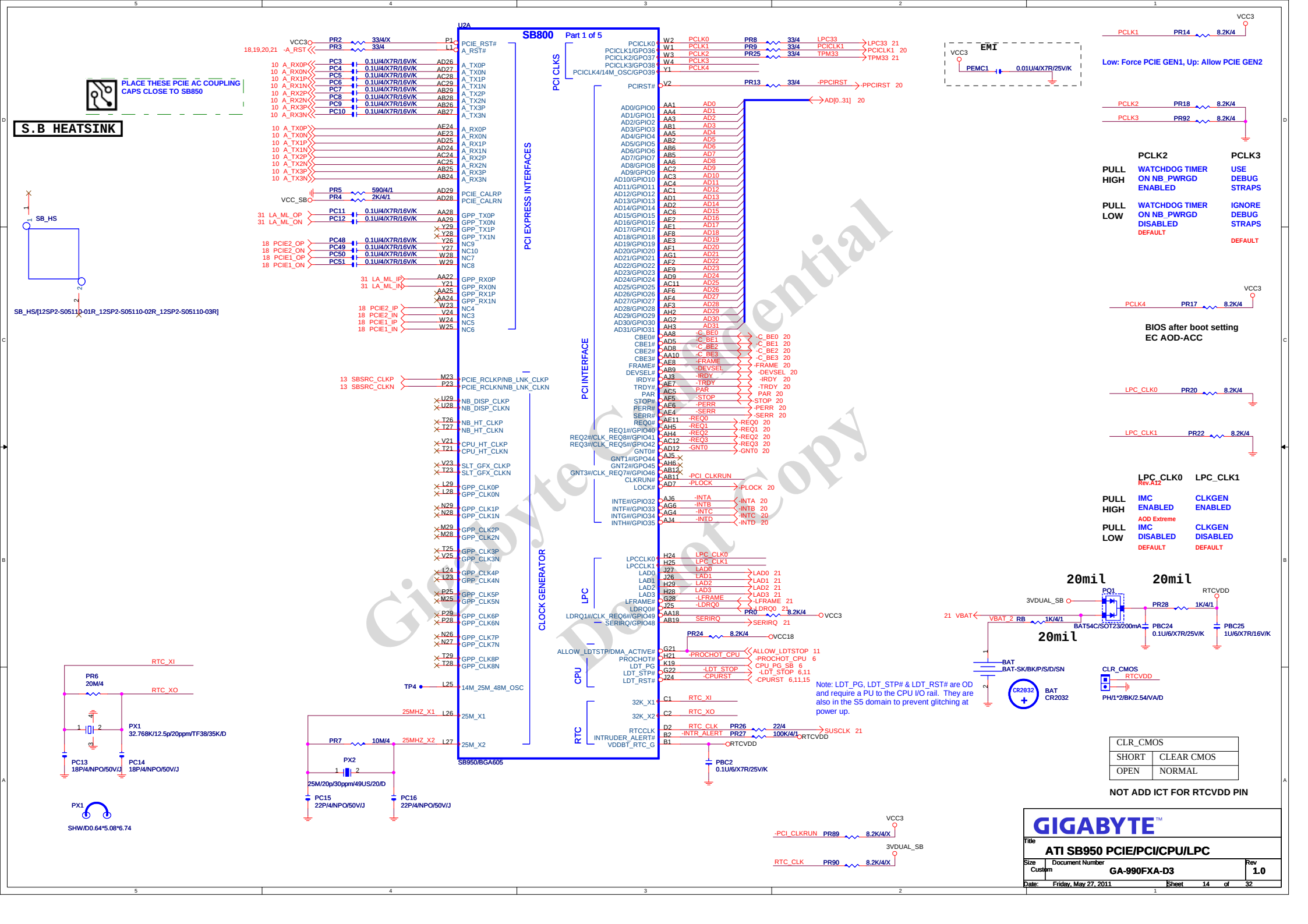
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

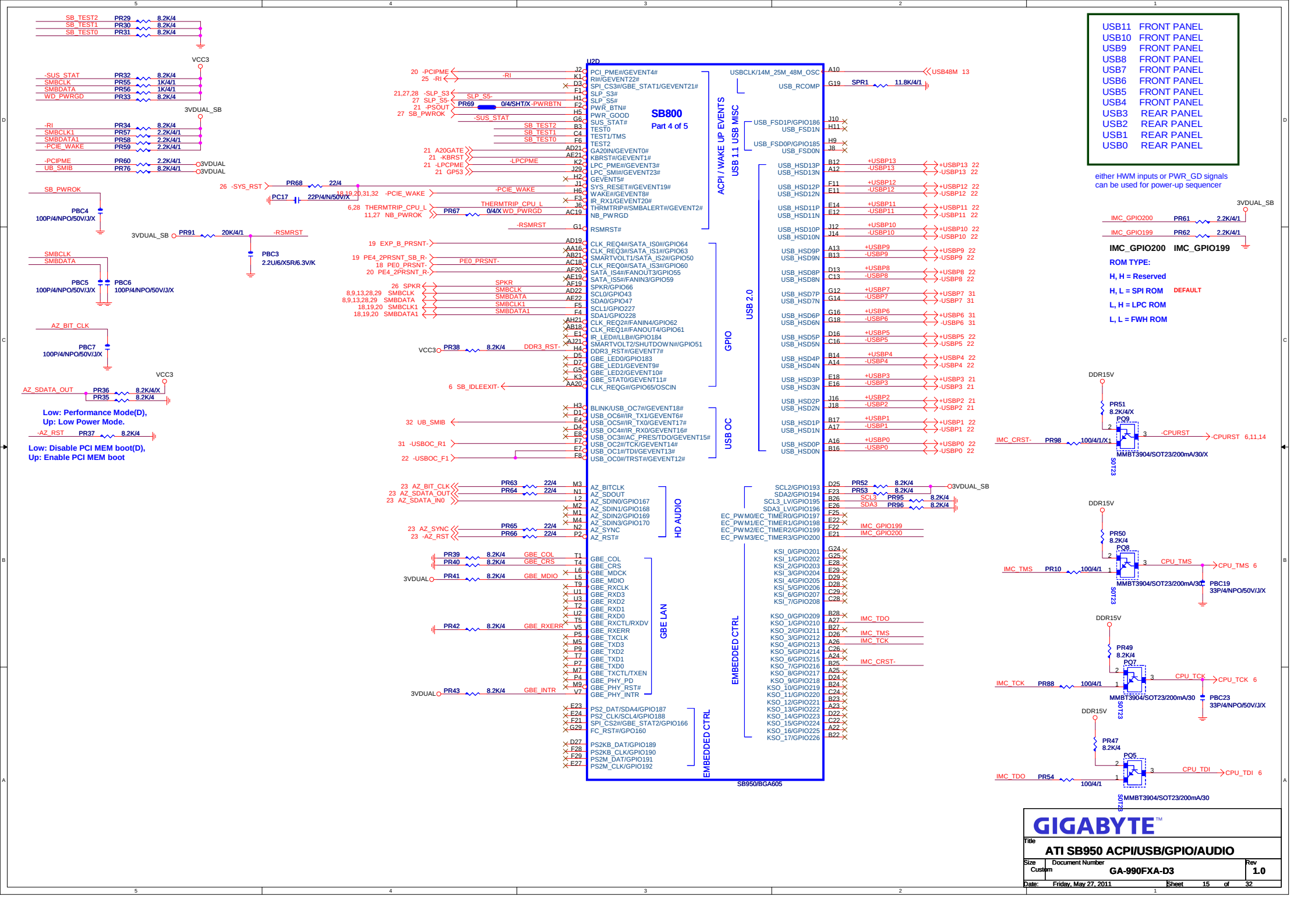
GIGABYTE™

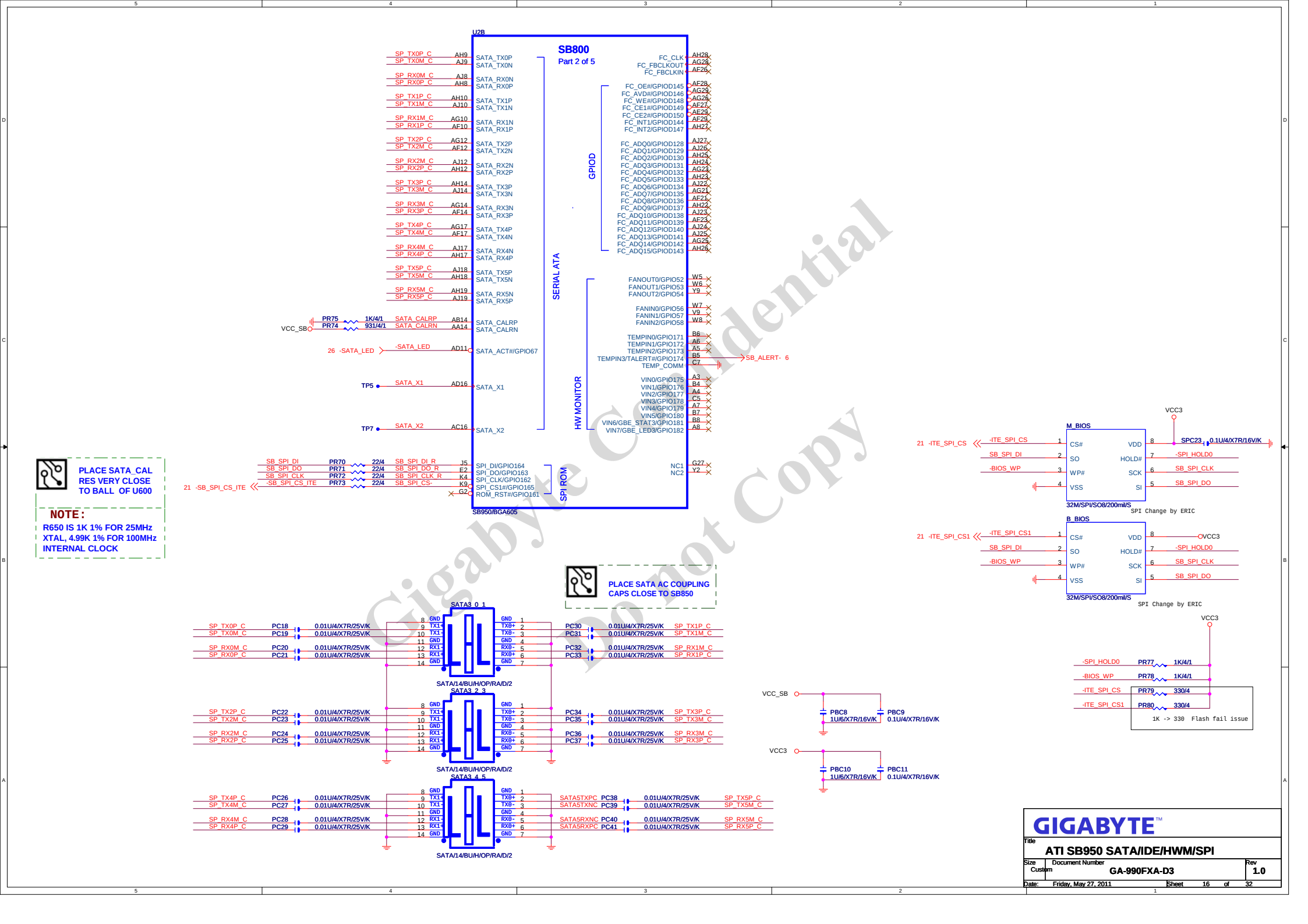
Title: ICS9LPRS477

Size: Custom | Document Number: GA-990FXA-D3 | Rev: 1.0

Date: Friday, May 27, 2011 | Sheet 13 of 32




SB800
Part 4 of 5
SB950/BGA605
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
IMC_GPIO200 IMC_GPIO199
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
Low: Performance Mode(D), Up: Low Power Mode.
Low: Disable PCI MEM boot(D), Up: Enable PCI MEM boot
GIGABYTE
ATI SB950 ACPI/USB/GPIO/AUDIO
GA-990FXA-D3
1.0
Friday, May 27, 2011
Sheet 15 of 32


U2B
SB800
Part 2 of 5
SERIAL ATA
GPIOD
HW MONITOR
SPI ROM
SB950/BGA605
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600
NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK
PLACE SATA AC COUPLING CAPS CLOSE TO SB850
SATA3_0_1
SATA3_2_3
SATA3_4_5
SATA/14/BU/H/OP/RA/D/2
M_BIOS
B_BIOS
32M/SPI/SO8/200mil/S
SPI Change by ERIC
1K -> 330 Flash fail issue
GIGABYTE
ATI SB950 SATA/IDE/HWM/SPI
GA-990FXA-D3
Rev 1.0
Friday, May 27, 2011
Sheet 16 of 32
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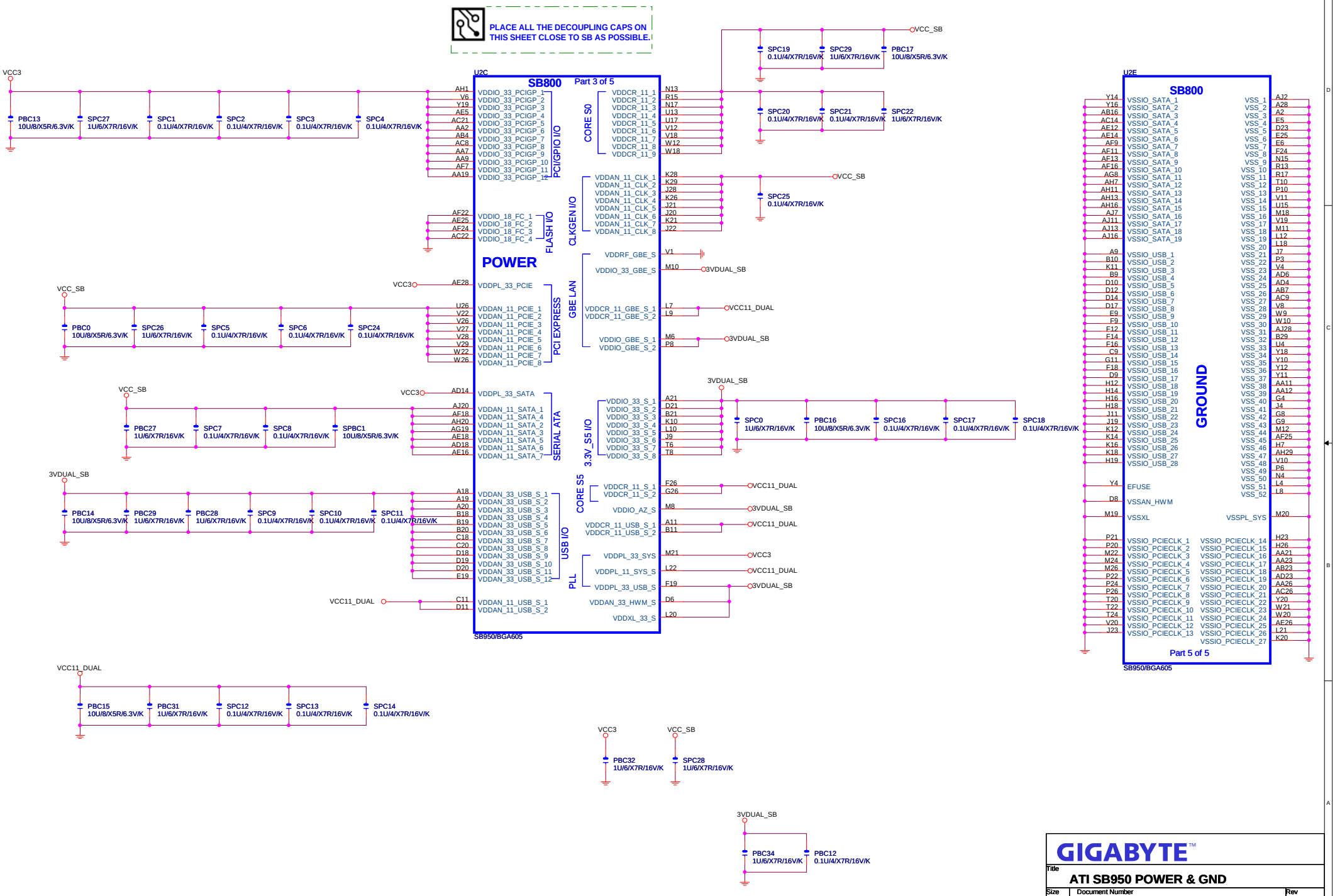
Do not Copy

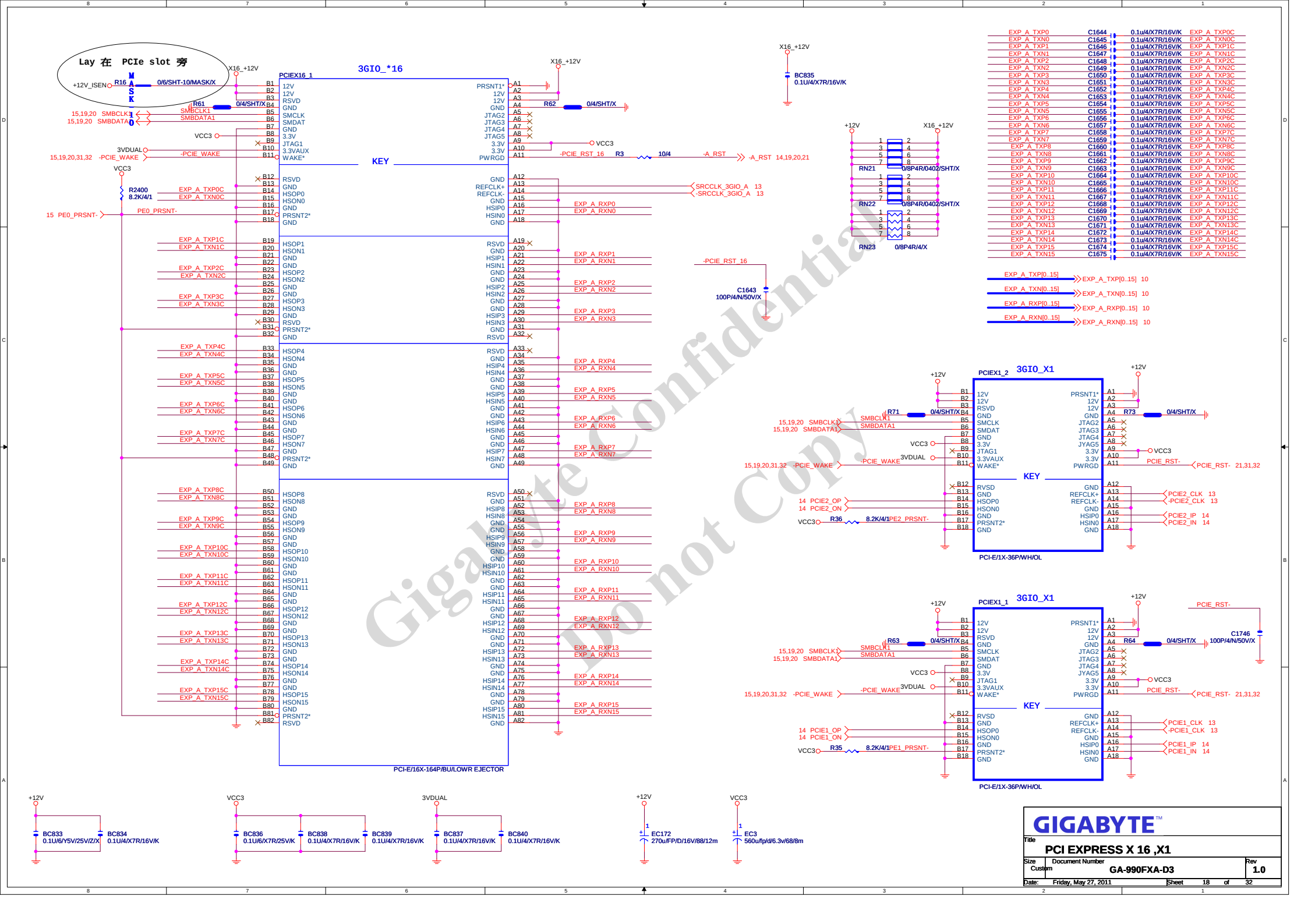


GIGABYTE™

Title: ATI SB950 POWER & GND

Size	Document Number	Rev
Custom	GA-990FXA-D3	1.0

Date: Friday, May 27, 2011 Sheet 17 of 32


Lay 在 PCIe slot 旁
PCIEX16_1
3GIO_*16
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
PCIEX1_2
3GIO_X1
PCI-E/1X-36P/WH/OL
PCIEX1_1
3GIO_X1
PCI-E/1X-36P/WH/OL
GIGABYTE
PCI EXPRESS X 16 ,X1
GA-990FXA-D3
1.0
Friday, May 27, 2011
Sheet 18 of 32
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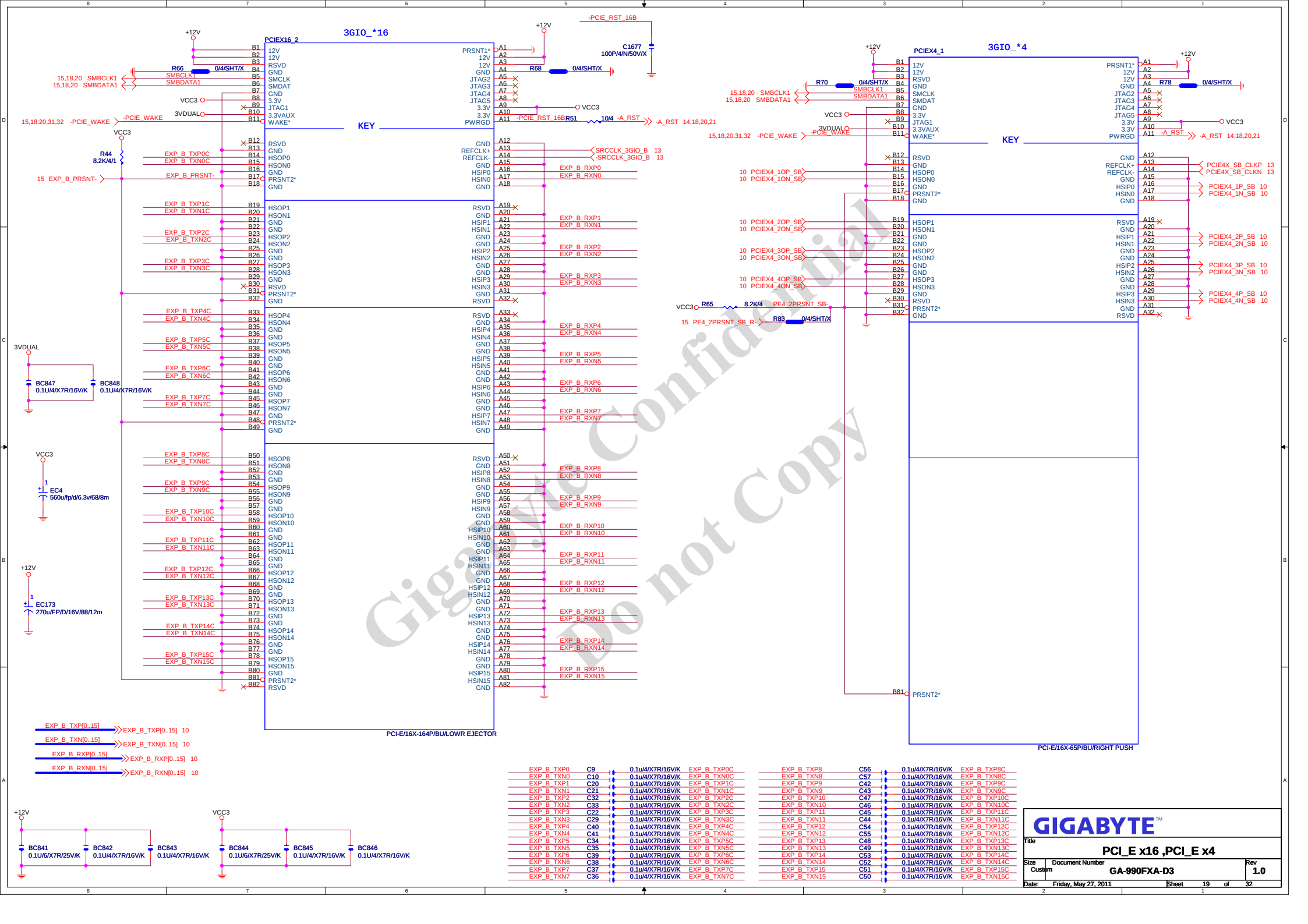
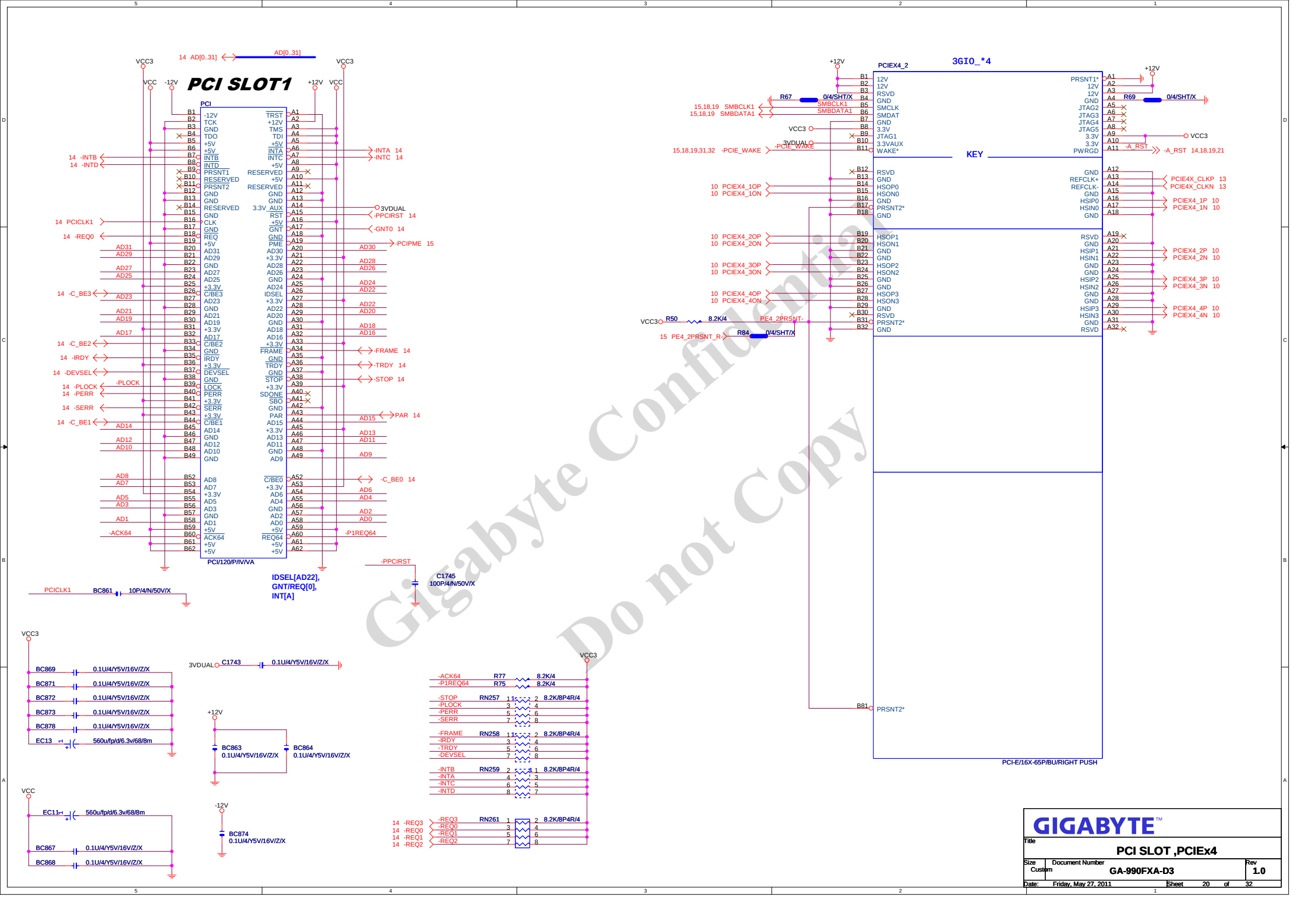
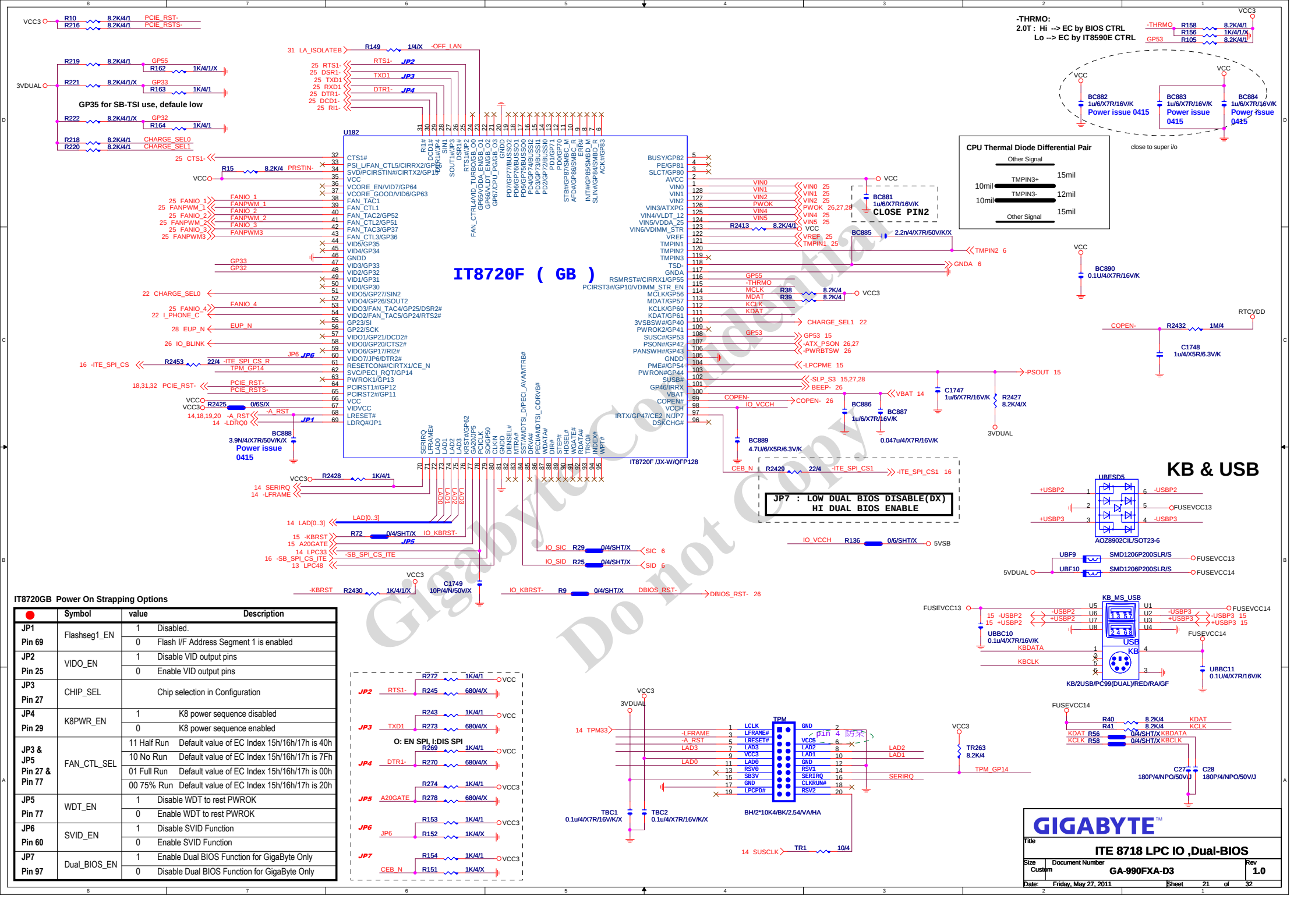
Do not Copy


3GIO_*16
PCIEX16_2
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
3GIO_*4
PCIEX4_1
KEY
PCI-E/16X-65P/BU/RIGHT PUSH
-PCIE_RST_16B
C1677
100P/4/N/50V/X
R66 0/4/SHT/X
R68 0/4/SHT/X
R70 0/4/SHT/X
R78 0/4/SHT/X
R51 10/4
-A_RST
-A_RST 14,18,20,21
15,18,20 SMBCLK1
15,18,20 SMBDATA1
15,18,20,31,32 -PCIE_WAKE
R44 8.2K/4/1
15 EXP_B_PRSNT-
R65 8.2K/4
PE4_2PRSNT_SB-
15 PE4_2PRSNT_SB_R-
R83 0/4/SHT/X
SRCCLK_3GIO_B 13
-SRCCLK_3GIO_B 13
10 PCIEX4_1OP_SB
10 PCIEX4_1ON_SB
10 PCIEX4_2OP_SB
10 PCIEX4_2ON_SB
10 PCIEX4_3OP_SB
10 PCIEX4_3ON_SB
10 PCIEX4_4OP_SB
10 PCIEX4_4ON_SB
PCIEX4_1P_SB 10
PCIEX4_1N_SB 10
PCIEX4_2P_SB 10
PCIEX4_2N_SB 10
PCIEX4_3P_SB 10
PCIEX4_3N_SB 10
PCIEX4_4P_SB 10
PCIEX4_4N_SB 10
PCIE4X_SB_CLKP 13
PCIE4X_SB_CLKN 13
EXP_B_TXP[0..15]
EXP_B_TXN[0..15]
EXP_B_RXP[0..15]
EXP_B_RXN[0..15]
EC4 560u/fp/d/6.3v/68/8m
EC173 270u/FP/D/16V/88/12m
BC847 0.1U/4/X7R/16V/K
BC848 0.1U/4/X7R/16V/K
BC841 0.1U/6/X7R/25V/K
BC842 0.1U/4/X7R/16V/K
BC843 0.1U/4/X7R/16V/K
BC844 0.1U/6/X7R/25V/K
BC845 0.1U/4/X7R/16V/K
BC846 0.1U/4/X7R/16V/K
C9 C10 C20 C21 C32 C33 C22 C29 C40 C41 C34 C35 C39 C38 C37 C36
C56 C57 C42 C43 C47 C46 C45 C44 C54 C55 C48 C49 C53 C52 C51 C50
0.1u/4/X7R/16V/K
GIGABYTE
Title
PCI_E x16 ,PCI_E x4
Size Custom
Document Number GA-990FXA-D3
Rev 1.0
Date: Friday, May 27, 2011
Sheet 19 of 32
Gigabyte Confidential
Do not Copy





IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	CHIP_SEL		Chip selection in Configuration
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

Title	ITE 8718 LPC IO ,Dual-BIOS
Size / Document Number	Custom / GA-990FXA-D3
Rev	1.0
Date:	Friday, May 27, 2011
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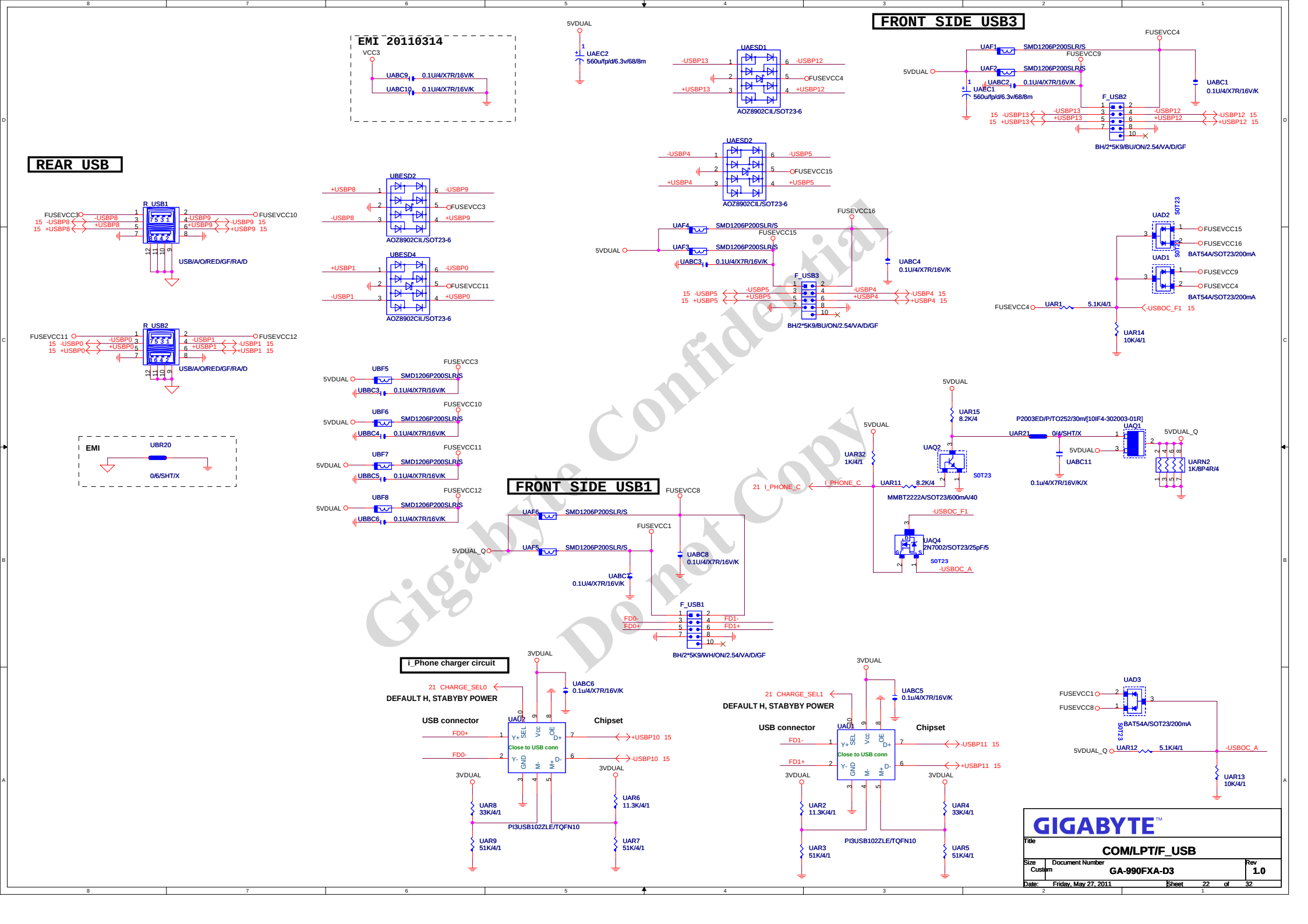
FRONT SIDE USB3
REAR USB
FRONT SIDE USB1
EMI 20110314
VCC3
UABC9 0.1U/4/X7R/16V/K
UABC10 0.1U/4/X7R/16V/K
5VDUAL
UAEC2 560u/fp/d/6.3v/68/8m
UAESD1
AOZ8902CIL/SOT23-6
FUSEVCC4
UAF1 SMD1206P200SLR/S
FUSEVCC9
UAF2 SMD1206P200SLR/S
UABC2 0.1U/4/X7R/16V/K
UAEC1 560u/fp/d/6.3v/68/8m
UABC1 0.1U/4/X7R/16V/K
F_USB2
BH/2*5K9/BU/ON/2.54/VA/D/GF
UAESD2
AOZ8902CIL/SOT23-6
FUSEVCC15
UAF4 SMD1206P200SLR/S
UAF3 SMD1206P200SLR/S
UABC3 0.1U/4/X7R/16V/K
UABC4 0.1U/4/X7R/16V/K
F_USB3
BH/2*5K9/BU/ON/2.54/VA/D/GF
FUSEVCC16
R_USB1
USB/A/O/RED/GF/RA/D
R_USB2
USB/A/O/RED/GF/RA/D
UBESD2
AOZ8902CIL/SOT23-6
UBESD4
AOZ8902CIL/SOT23-6
UBF5 SMD1206P200SLR/S
UBBC3 0.1U/4/X7R/16V/K
UBF6 SMD1206P200SLR/S
UBBC4 0.1U/4/X7R/16V/K
UBF7 SMD1206P200SLR/S
UBBC5 0.1U/4/X7R/16V/K
UBF8 SMD1206P200SLR/S
UBBC6 0.1U/4/X7R/16V/K
EMI
UBR20
0/6/SHT/X
UAD2
UAD1
BAT54A/SOT23/200mA
UAR1 5.1K/4/1
UAR14 10K/4/1
UAR15 8.2K/4
UAR32 1K/4/1
UAR11 8.2K/4
UAQ2
MMBT2222A/SOT23/600mA/40
P2003ED/P/TO252/30m/[10IF4-302003-01R]
UAR21 0/4/SHT/X
UABC11 0.1u/4/X7R/16V/K/X
UAQ1
UARN2 1K/8P4R/4
UAQ4 2N7002/SOT23/25pF/5
UABC8 0.1U/4/X7R/16V/K
UABC7 0.1U/4/X7R/16V/K
F_USB1
BH/2*5K9/WH/ON/2.54/VA/D/GF
i_Phone charger circuit
DEFAULT H, STABYBY POWER
USB connector
Chipset
Close to USB conn
PI3USB102ZLE/TQFN10
UAR8 33K/4/1
UAR9 51K/4/1
UAR6 11.3K/4/1
UAR7 51K/4/1
UABC6 0.1u/4/X7R/16V/K
UABC5 0.1u/4/X7R/16V/K
UAR2 11.3K/4/1
UAR3 51K/4/1
UAR4 33K/4/1
UAR5 51K/4/1
UAD3
UAR12 5.1K/4/1
UAR13 10K/4/1
GIGABYTE
COM/LPT/F_USB
GA-990FXA-D3
1.0
Friday, May 27, 2011
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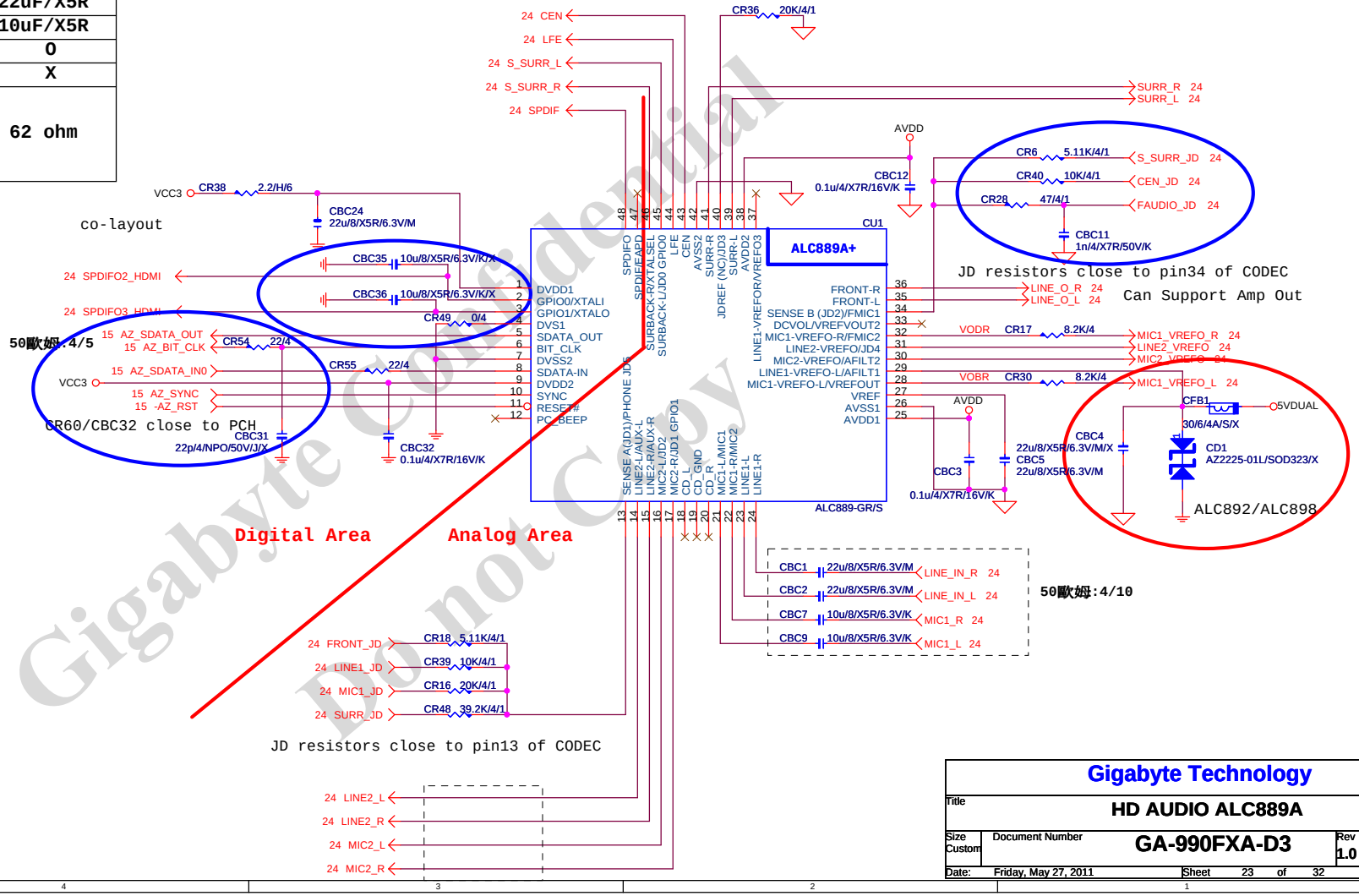
AZALIA CODEC *ALC889/ALC889B/ALC892/ALC898 Colay*

	ALC889	ALC889B	ALC898/ALC892
CR65	0	0	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	0	X	0
CR66	X	0	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	0
CD2/CD3/CQ3/CQ5	0	0	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm



Gigabyte Technology		
Title	HD AUDIO ALC889A	
Size: Custom	Document Number: GA-990FXA-D3	Rev: 1.0
Date: Friday, May 27, 2011	Sheet 23 of 32	

CODEC POWER/EMI PAD

EUP

5VDUAL CR44 0/6/SHT/X

CBC38 0.01u/4/X7R/25V/K

+12V CD3 CD4148WP/1206/300mA

CQ3 78L05/SOT89/0.1A

CD4148WP/1206/300mA CBC21 0.1u/4/X7R/16V/K/X

AVDD CD2 AZ2225-01L/SOD323

CBC8 22u/8/X5R/6.3V/M

ADD CD2 For ESD PROTECT DIODE

CR37 0/4/X

上ALC892時,此顆電容要保留

CR4 0/6/SHT/X

FUSEVCC14

23 SPDIF

OPTICAL

FR/5P/BK/T/D/S(GY)

CESD1

M2_L M2_R L2_R L2_L

AZ2025-04S/SOT23-5L/X

23 SPDIFO2_HDMI CR52 0/4 SPDIFO_HDMI

23 SPDIFO3_HDMI CR53 0/4/X

CBC37 100p/4/NPO/50V/J

PIN

SPDIF_O PH/1*2/BK/2.54/VA/D

For HDMI SPDIF

CESD5

SPDIF SPDIFO_HDMI

AZ2025-04S/SOT23-5L/X

AZALIA JACK

BTX AZALIA CONNECTOR

11NR6-403007-21R

CESD2 AJ_A2 AJ_B2 AJ_C2 AJ_C5

CESD4 AJ_B5 AJ_A5 BJ_C2 BJ_A2

CESD3 BJ_B5 BJ_A5 BJ_C5 BJ_B2

AZ2025-04S/SOT23-5L/X

AUDIOB

23 LINE1_JD LINE1_JD AJ_A5 AJ_A2 GND LINE-IN

BLUE LINE-IN

23 FRONT_JD FRONT_JD AJ_B5 AJ_B2 GND LINE-OUT

GREEN LINE-OUT

23 MIC1_JD MIC1_JD AJ_C5 AJ_C2 GND MIC-IN

PINK MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

AUDIOA

23 CEN_JD CEN_JD BJ_B5 BJ_B2 GND REAR

Orange CEN/LFE

23 SURR_JD SURR_JD BJ_C5 BJ_C2 GND CEN

Black SURROUND

23 S_SURR_JD S_SURR_JD BJ_A5 BJ_A2 GND SIDE

Gray SURROUND SIDE

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

LINE-OUT

23 LINE_O_R CEC2 100u/OS/D/16V/66/30m CR7 62/4 AJ_B5

23 LINE_O_L CEC3 100u/OS/D/16V/66/30m CR9 62/4 AJ_B2

CR10 22K/4 CR8 22K/4

CBC23 180p/4/NPO/50V/J CBC26 180p/4/NPO/50V/J

LINE-IN

23 LINE_IN_R CR5 62/4 AJ_A5

23 LINE_IN_L CR13 62/4 AJ_A2

CBC18 180p/4/NPO/50V/J CBC27 180p/4/NPO/50V/J

MIC-IN

23 MIC1_R CR29 62/4 AJ_C5

23 MIC1_L CR32 62/4 AJ_C2

23 MIC1_VREFO_L

23 MIC1_VREFO_R

CBC19 180p/4/NPO/50V/J CBC22 180p/4/NPO/50V/J

SURROUND

EMI

23 SURR_R CEC5 100u/OS/D/16V/66/30m CR46 62/4 BJ_C5

23 SURR_L CEC7 100u/OS/D/16V/66/30m CR19 62/4 BJ_C2

CR20 22K/4 CR45 22K/4

CBC29 180p/4/NPO/50V/J CBC28 180p/4/NPO/50V/J

CEN/LFE

EMI

23 LFE CEC9 100u/OS/D/16V/66/30m CR50 62/4 BJ_B5

23 CEN CEC10 100u/OS/D/16V/66/30m CR41 62/4 BJ_B2

CR42 22K/4 CR51 22K/4

CBC25 180p/4/NPO/50V/J CBC34 180p/4/NPO/50V/J

SURR BACK

EMI

23 S_SURR_R CEC8 100u/OS/D/16V/66/30m CR21 62/4 BJ_A5

23 S_SURR_L CEC4 100u/OS/D/16V/66/30m CR47 62/4 BJ_A2

CR43 22K/4 CR22 22K/4

CBC33 180p/4/NPO/50V/J CBC30 180p/4/NPO/50V/J

AZALIA FRONT PANEL

CQ2 BAT54A/SOT23/200mA SOT23

23 LINE2_VREFO CR25 8.2K/4 CR15 8.2K/4

CQ1 BAT54A/SOT23/200mA

23 MIC2_VREFO CR12 8.2K/4 CR3 8.2K/4

EMI

23 MIC2_L CBC20 10u/8/X5R/6.3V/K CR2 62/4 M2_L

23 MIC2_R CBC15 10u/8/X5R/6.3V/K CR11 62/4 M2_R

23 FAUDIO_JD CR14 62/4 L2_R

L2_L CR24 62/4 L2_L

CR1 0/4/X

F_AUDIO

CR27 22K/4 CR26 22K/4

CR35 20K/4/1 CR31 39.2K/4/1

BH/2*5K8/GED/2.54/VA

Digital Area

VCC3 CR56 8.2K/4

C_ACZ_DET

100u/OS/D/16V/66/30m

23 LINE2_R CEC6 L2_R

23 LINE2_L CEC1 L2_L

100u/OS/D/16V/66/30m

CBC10 180p/4/NPO/50V/J CBC16 180p/4/NPO/50V/J CBC17 180p/4/NPO/50V/J CBC6 180p/4/NPO/50V/J

Gigabyte Technology

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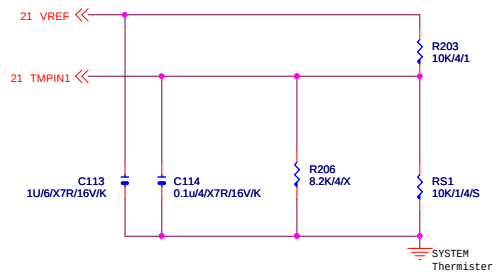
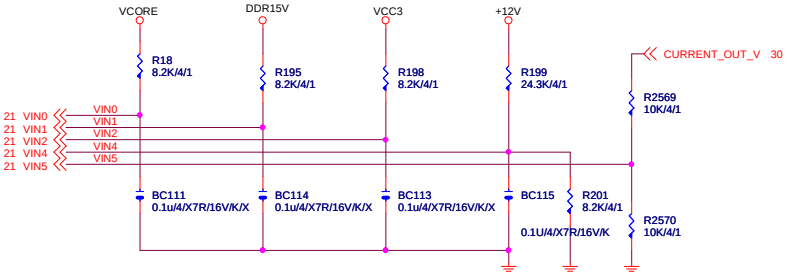
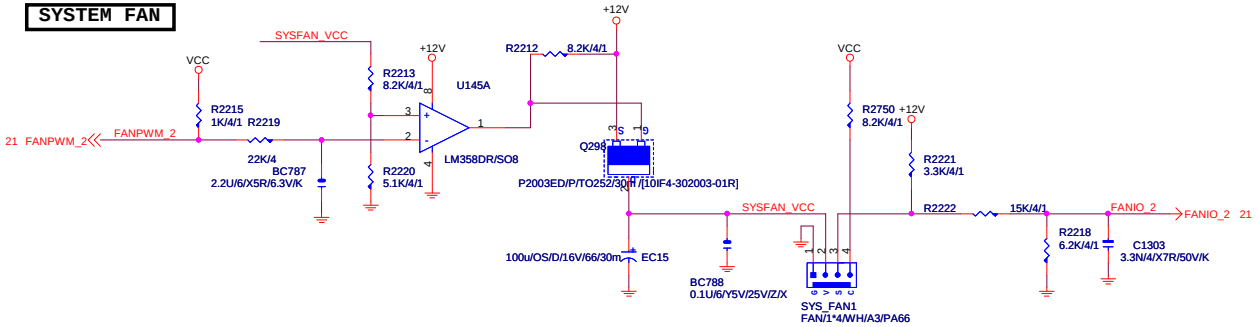
Hardware Monitor circuits

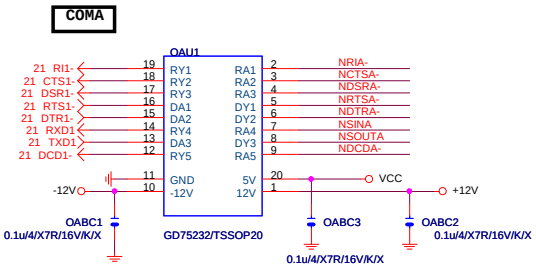




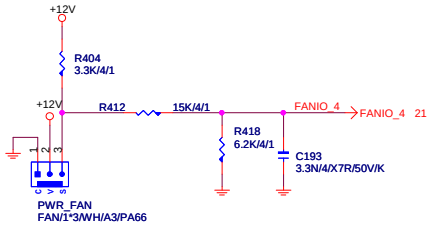
SYSTEM FAN



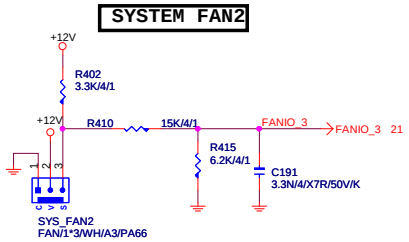
COMA



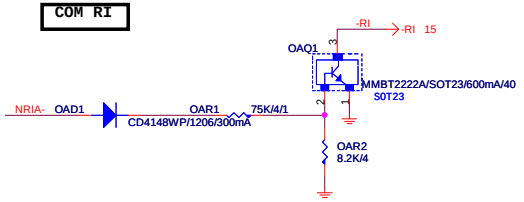
POWER FAN

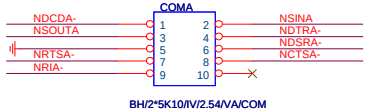


SYSTEM FAN2

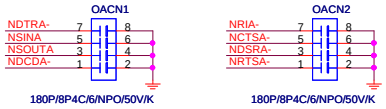


COM RI

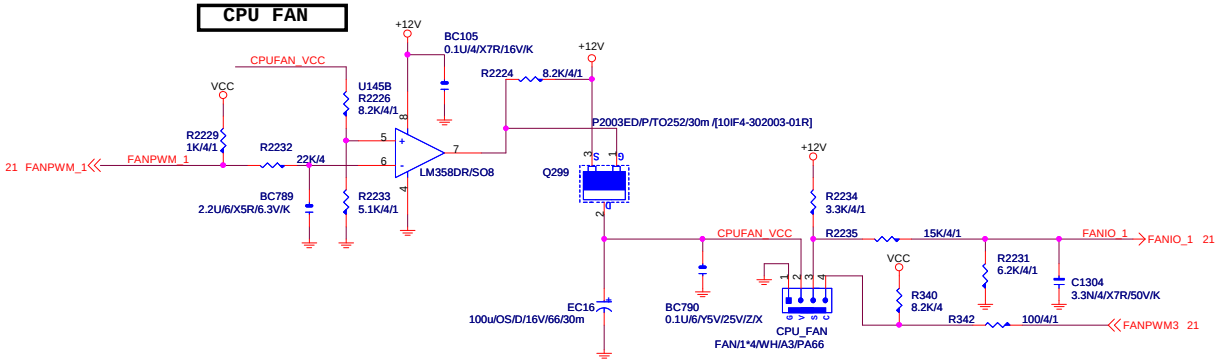




11NH3-000205-Y1R/Y2R



CPU FAN



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Title	FAN/HWMO/COM	
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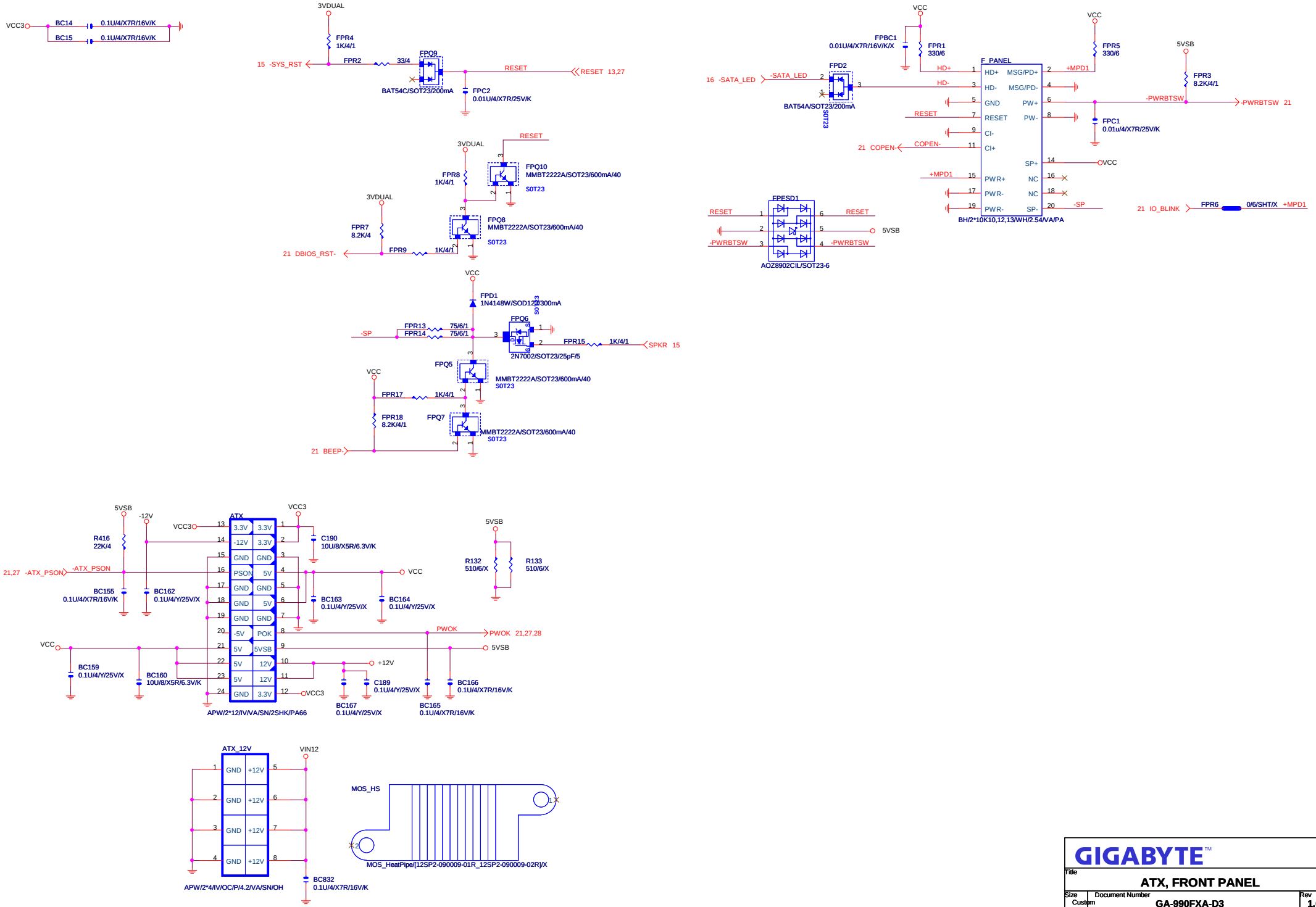

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Title	ATX, FRONT PANEL	
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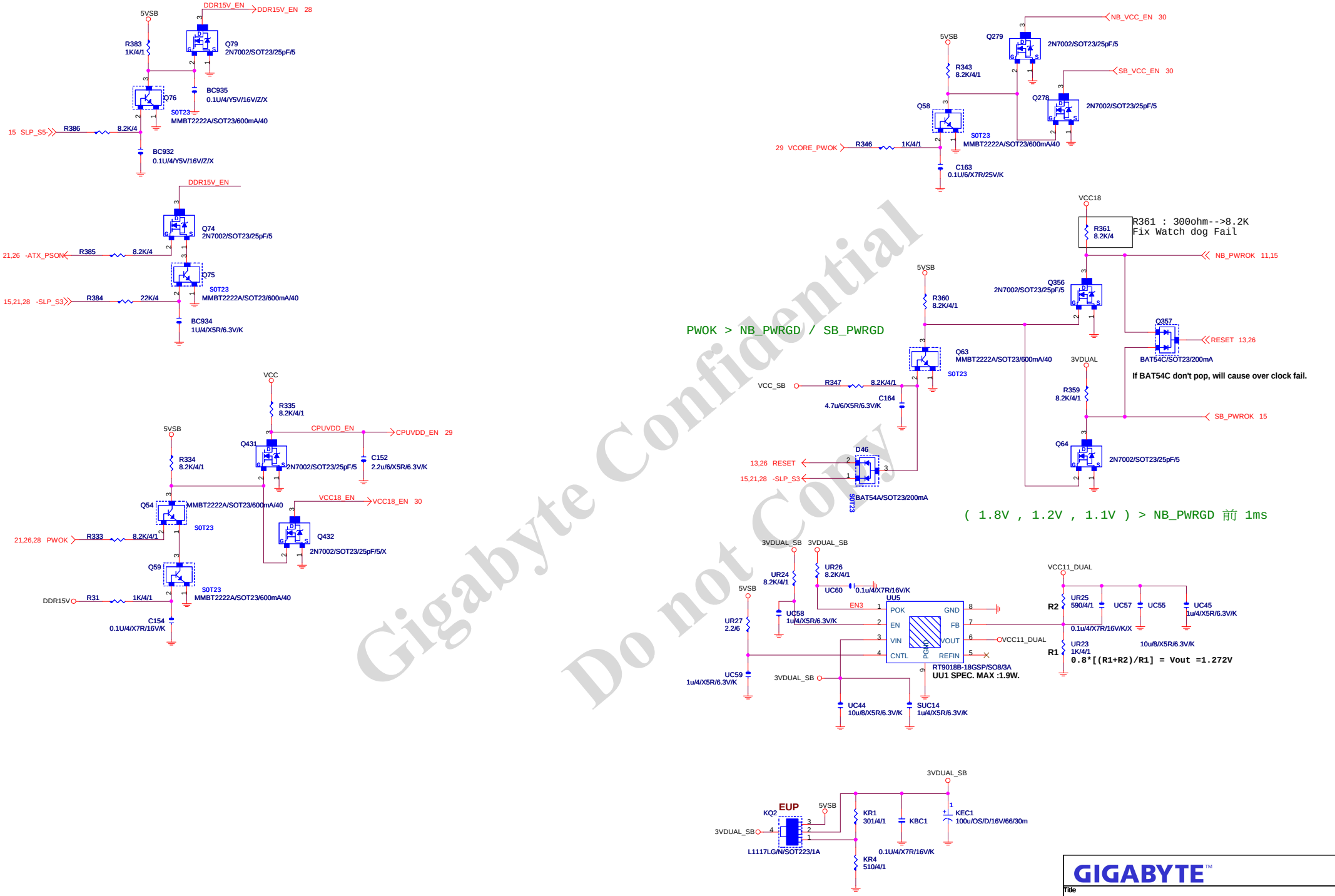

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Title: POWER SEQUENCE		
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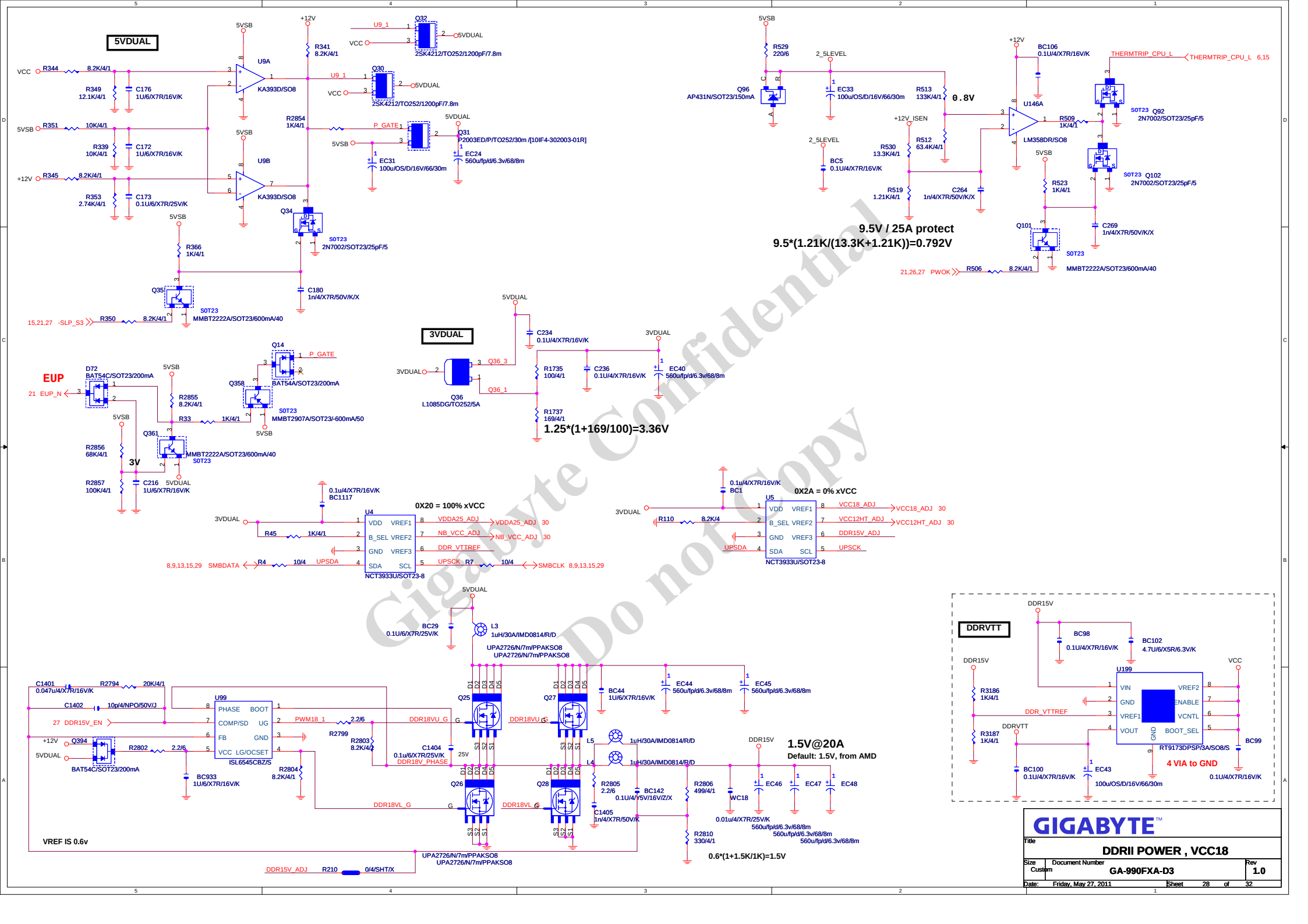

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Title	DDRII POWER , VCC18	
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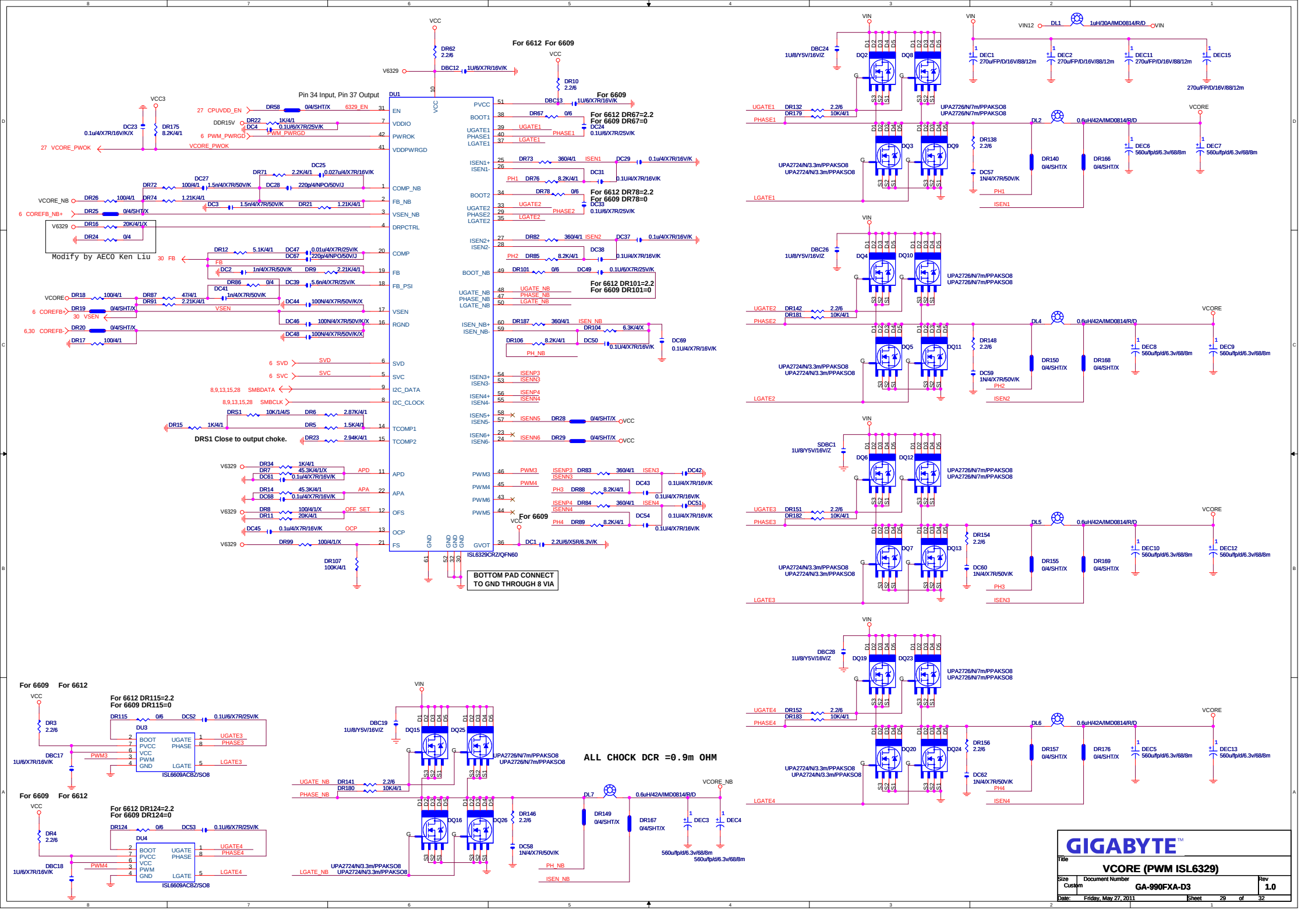
For 6612 For 6609
Pin 34 Input, Pin 37 Output
Modify by AECO Ken Liu
DRS1 Close to output choke.
ISL6329CRZ/QFN60
BOTTOM PAD CONNECT TO GND THROUGH 8 VIA
For 6612 DR67=2.2
For 6609 DR67=0
For 6612 DR78=2.2
For 6609 DR78=0
For 6612 DR101=2.2
For 6609 DR101=0
For 6609 For 6612
For 6612 DR115=2.2
For 6609 DR115=0
For 6609 For 6612
For 6612 DR124=2.2
For 6609 DR124=0
ISL6609ACBZ/SO8
ALL CHOCK DCR =0.9m OHM
UPA2726/N/7m/PPAKSO8
UPA2724/N/3.3m/PPAKSO8
0.6uH/42A/IMD0814/R/D
GIGABYTE
VCORE (PWM ISL6329)
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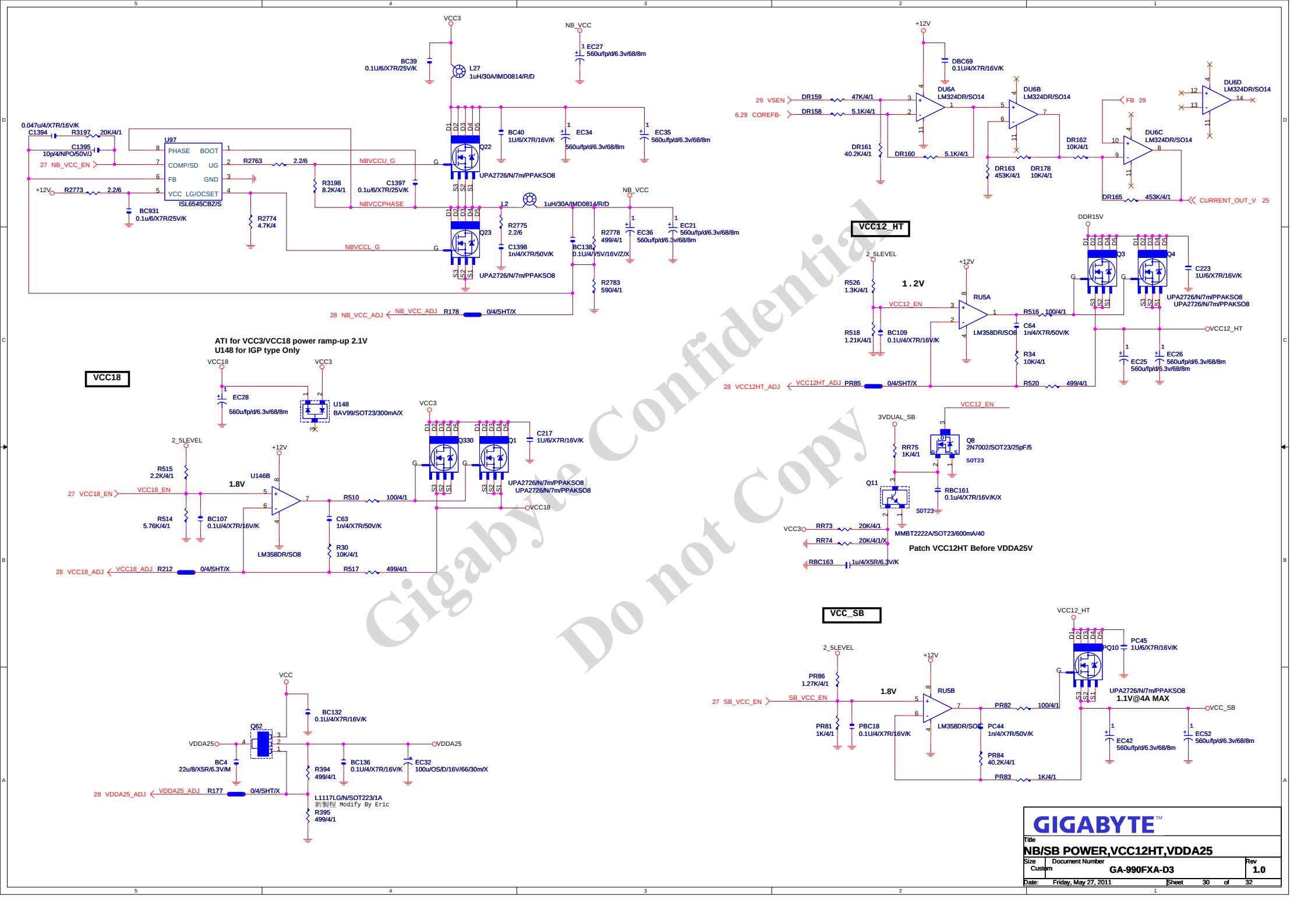
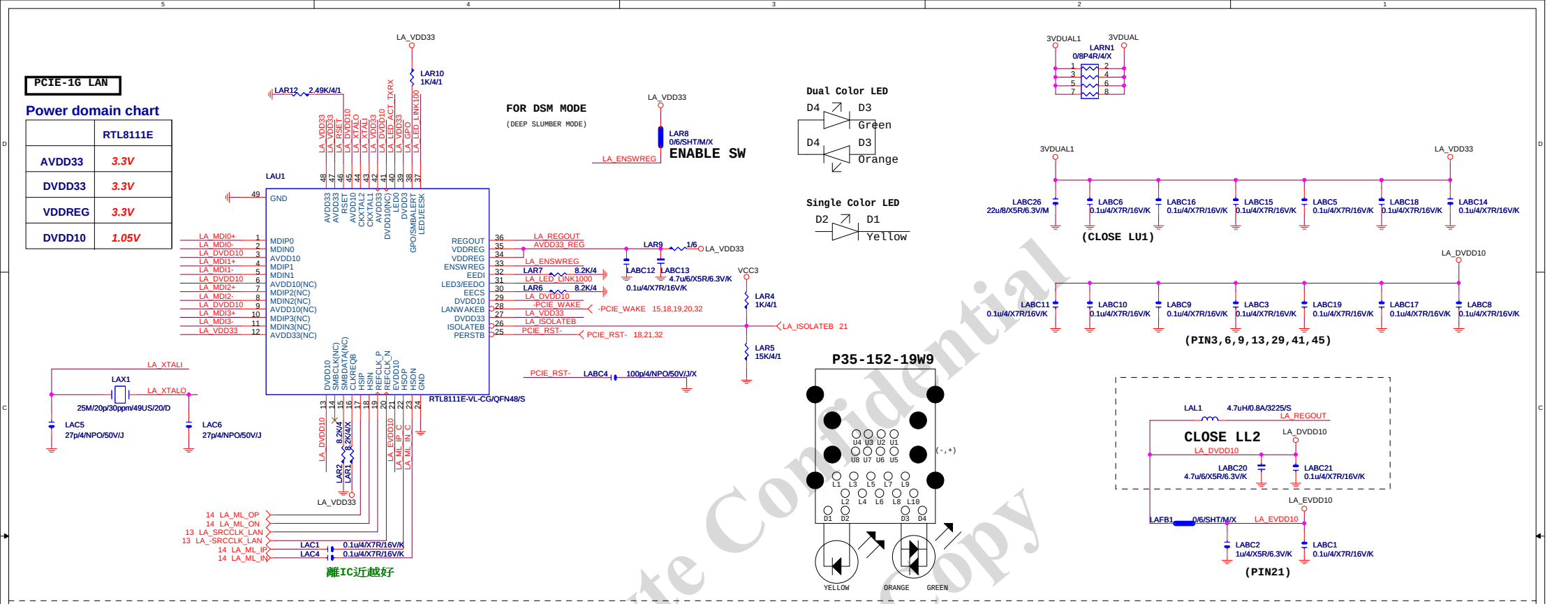


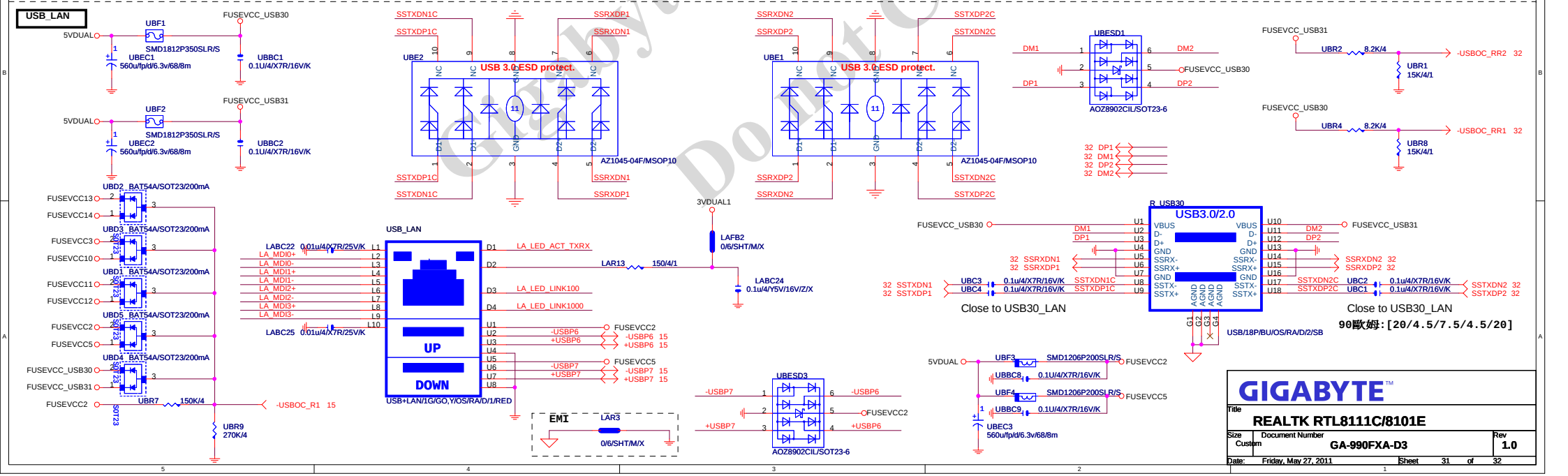
PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB_LAN



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Title: REALTK RTL8111C/8101E

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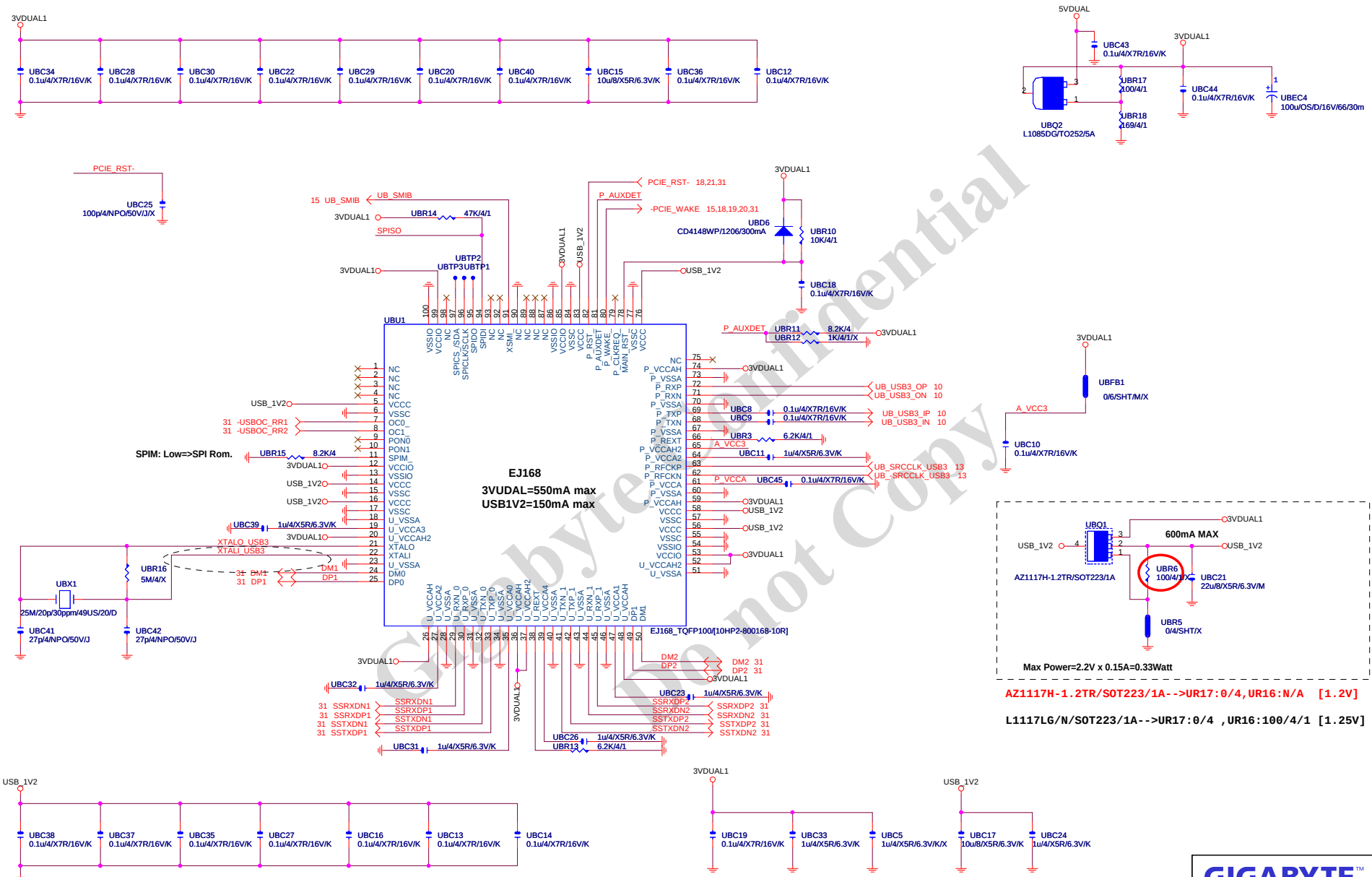

Title	EJ168 R_USB30
Size	Custom
Document Number	GA-990FXA-D3
Rev	1.0
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