Model : J10IL1

Intel Diamondville CPU +Intel 945GSE+ Intel ICH7-M

MB	Revision History	
A	03/31/08	Initial REV.A
B	05/23/08	Release REV.B
C	??/??/08	Release REV.C

J10IL1 REV.C P/N LIST

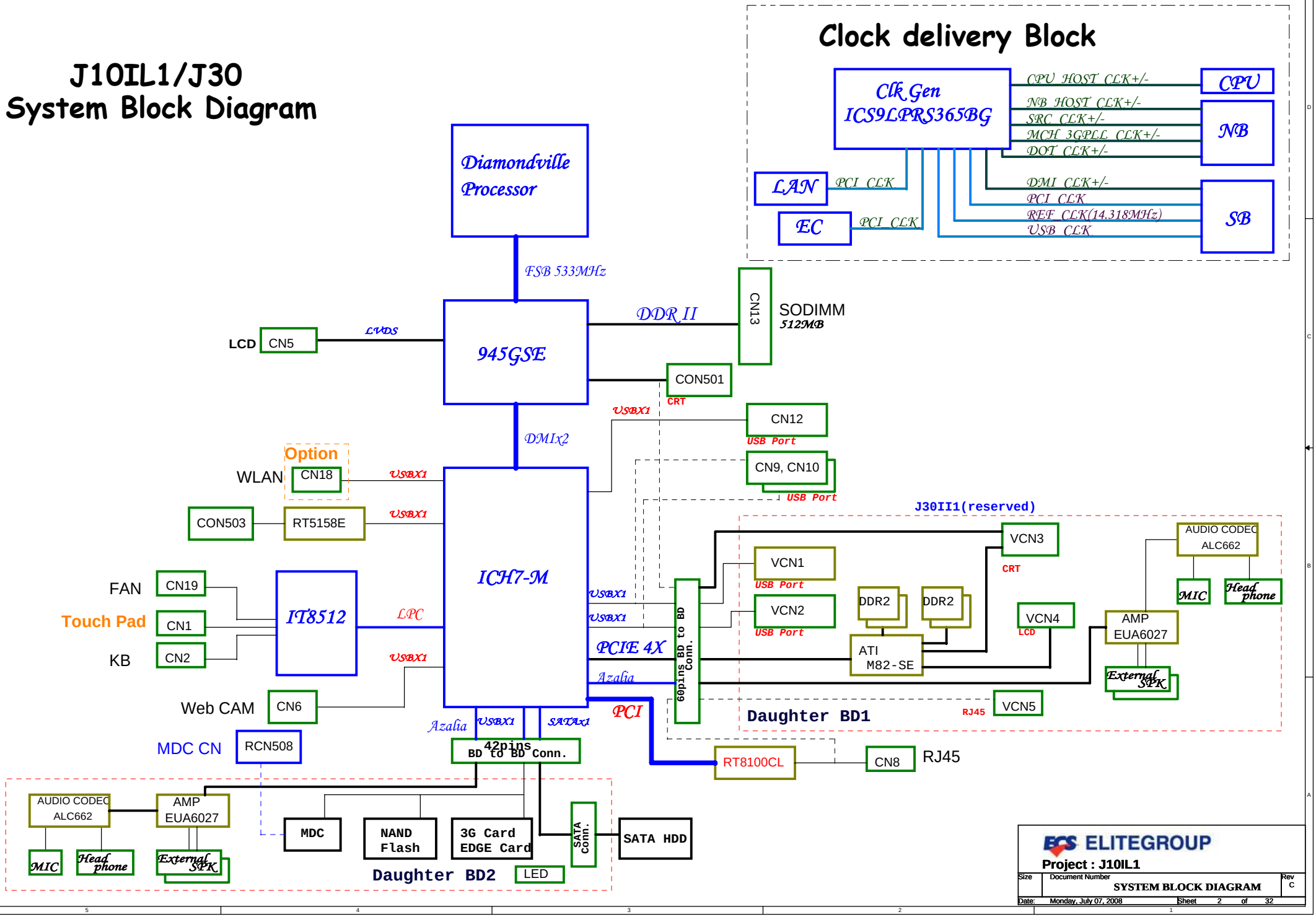
	PCB P/N	PCB ASSY P/N
Initial REV.A		
MB BD	37GJ10000-A0	82GJ10000-A0
Function BD	35GWJ1000-A0	80GWJ1000-A0
Release REV.B		
MB BD	37GJ10000-B0	82GJ10000-B0
Function BD	35GWJ1000-B0	80GWJ1000-B0
RJ11 BD	35G9J1000-A0	80G9J1000-A0
Release REV.C		
MB BD	37GJ10000-C0	
Function BD	35GWJ1000-C0	
RJ11 BD	35G9J1000-B0	

ECS ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS COVER PAGE	C
Date:	Monday, July 07, 2008	Sheet 1 of 32

J10IL1/J30
System Block Diagram



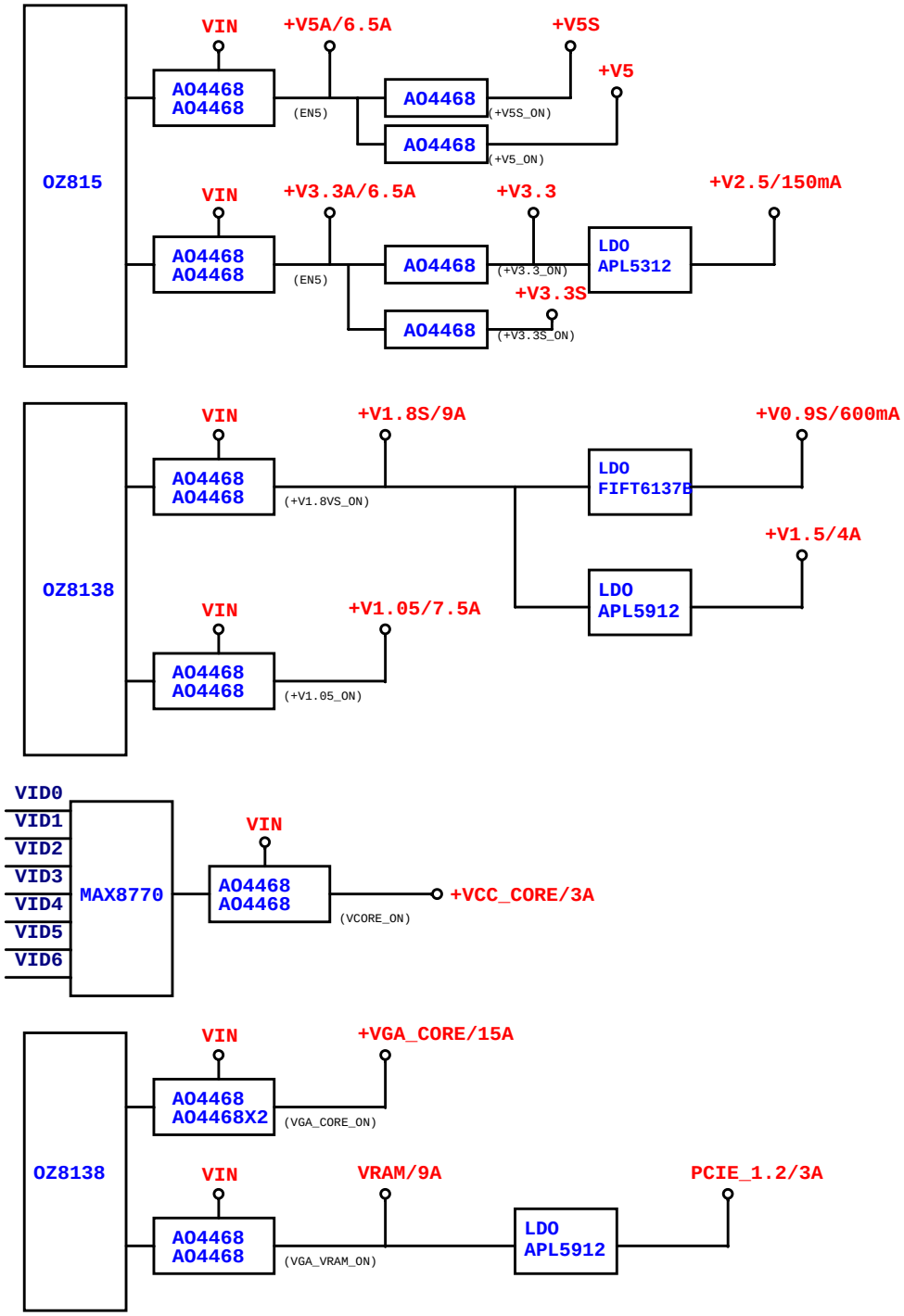
ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SYSTEM BLOCK DIAGRAM	C

Date: Monday, July 07, 2008 Sheet 2 of 32

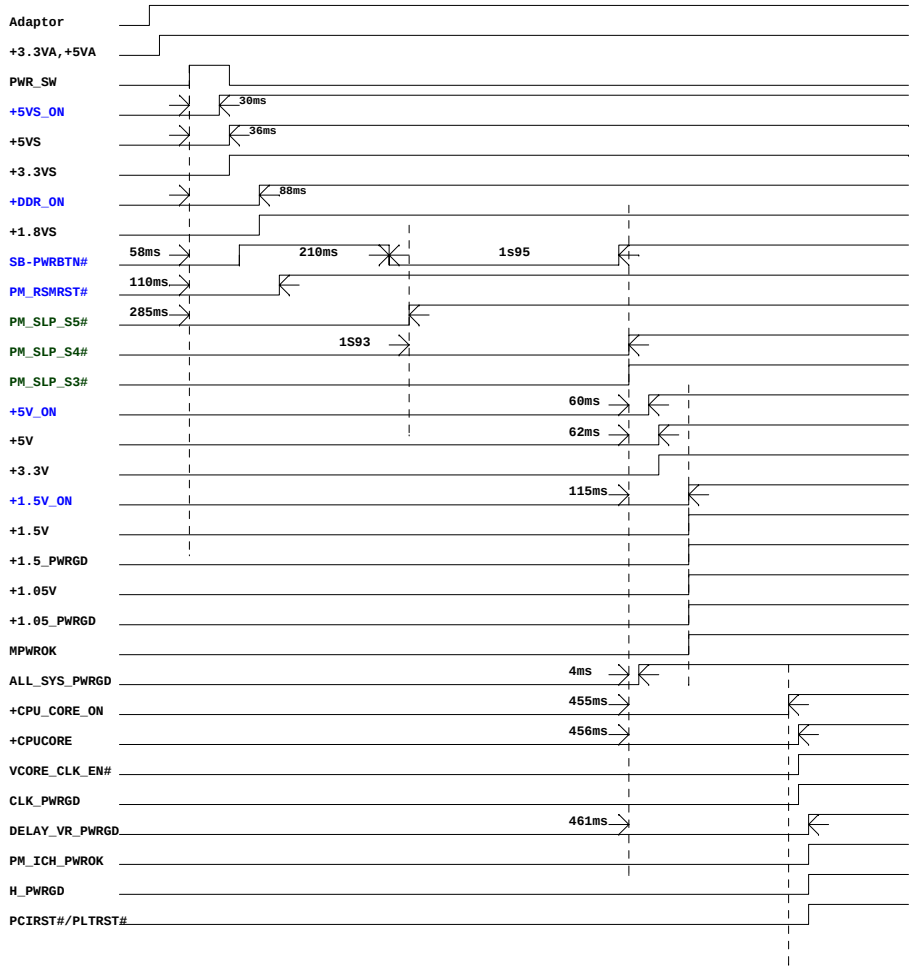
POWER BLOCK DIAGRAM



J10IL1 M/B Power Rail State :

	+*V_LDO	+*VA	+*VS	+*V	CLK
AC/DC S0/Moff (Full On)	ON	ON	ON	ON	ON
AC/DC S3/Moff (STR)	ON	ON	ON	OFF	Only MCH BCLK
AC/DC S4/Moff (STD)	ON	ON	OFF	OFF	OFF
AC S5/Moff (Soft Off)	ON	ON	OFF	OFF	OFF
DC S5/Moff (Soft Off)	ON	OFF	OFF	OFF	OFF

Poewr On Sequence



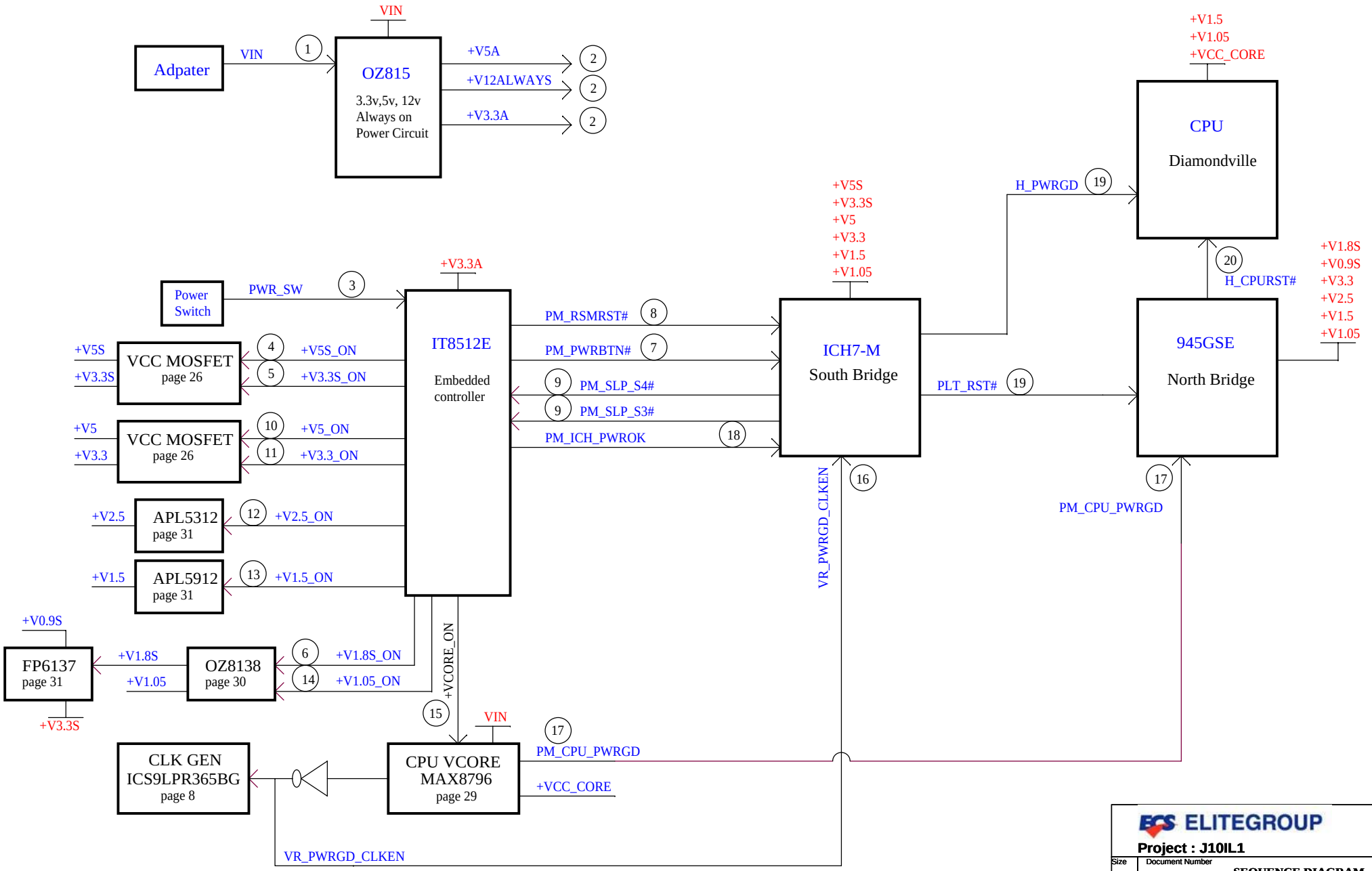
ELITEGROUP

Project : J10IL1

Size | Document Number: POWER DIAGRAM & SEQUENCE | Rev: C

Date: Monday, July 07, 2008 | Sheet 3 of 32

J10IL1 Power on Sequence Diagram



ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SEQUENCE DIAGRAM	C
Date: Monday, July 07, 2008	Sheet 4 of 32	

ICH-7M GPIO

GPIO0	PM_BMBUSY#
GPIO1	PCI_REQ#5
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	N.C
GPIO7	EC_SCI#
GPIO8	EC_EXTSMI#
GPIO9	PNLSW2
GPIO10	PNLSW1
GPIO11	SMB_ALERT#
GPIO12	PNLSW0
GPIO13	SMC_WAKE_SCI#_R
GPIO14	N.C
GPIO15	N.C
GPIO16	PM_DPRSLPVR_R
GPIO17	PCI_GNT#5
GPIO18	PM_STPPCI#
GPIO19	SATA0_R1
GPIO20	PM_STPCPU#
GPIO21	SATA0_R0
GPIO22	ICH_GPIO22
GPIO23	N.C
GPIO24	N.C
GPIO25	N.C
GPIO26	N.C
GPIO27	PM_S3HOT#_R
GPIO28	N.C
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN#
GPIO34	N.C
GPIO35	N.C
GPIO36	SATA0_R2
GPIO37	SATA0_R3
GPIO38	N.C
GPIO39	N.C
GPIO40	N.C
GPIO41	N.C
GPIO42	N.C
GPIO43	N.C
GPIO44	N.C
GPIO45	N.C
GPIO46	N.C
GPIO47	N.C
GPIO48	N.C
GPIO49	N.C
GPIO50	N.C
GPIO51	N.C
GPIO52	N.C
GPIO53	N.C
GPIO54	N.C
GPIO55	N.C
GPIO56	N.C
GPIO57	N.C
GPIO58	N.C
GPIO59	N.C
GPIO60	N.C

ITE8512E GPIO Pin Definition list

GPA0	BTL_BEEP
GPA1	BRIGHTNESS_R
GPA2	PWR_LED
GPA3	BUTTON_LED
GPA4	CHG_R_LED
GPA5	CHG_G_LED
GPA6	X
GPA7	**X**
GPB0	**VGA_CORE_ON**
GPB1	VGA_VRAM_ON
GPB2	VGA_VDDR3_ON
GPB3	SMB_CLK_GEN
GPB4	SMB_DATA_GEN
GPB5	X
GPB6	X
GPB7	PWR_KEEP
GPC0	X
GPC1	SMB_CLK_BAT
GPC2	SMB_DATA_BAT
GPC3	**X**
GPC4	X
GPC5	+V2.5_ON
GPC6	X
GPC7	+V5S_ON
GPD0	AC_IN
GPD1	WEBCAM_EN
GPD2	PLT_RST#_EC
GPD3	EC_EXTSCI#_R
GPD4	EC_EXTSMI#_R
GPD5	PM_THROTTING#
GPD6	***FAN_SPEED#***
GPD7	PM_PWRBTN#
GPE0	BKL_EC
GPE1	MUTE_AMP#
GPE2	PM_RSMRST#
GPE3	***PM_SYSRST#***
GPE4	PWR_SW
GPE5	PM_SLP_S3#
GPE6	PM_SLP_S4#
GPE7	
GPF0	RF_LED
GPF1	RF_OFF#
GPF2	X
GPF3	X
GPF4	PS2_CLK_TP
GPF5	PS2_DATA_TP
GPF6	SMB_CLK_VGA
GPF7	SMB_DATA_VGA
GPH0	VCC_MCH_VRPWRGD
GPH1	VCORE_ON
GPH2	**+V5_ON**
GPH3	+V3.3_ON
GPH4	+V3.3S_ON
GPH5	X
GPH6	+V1.05_ON
GPG1	+V1.8S_ON
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	THERM#_VGA
ADC5/GPI5	EC_PROCHOT
ADC6/GPI6	X
ADC7/GPI7	PM_SLP_S5#

ITE8512E GPIO Pin Definition list

DAC0/GPJ0	***EC_BL_PWM***
DAC0/GPJ1	CHG_I
DAC0/GPJ2	FAN_CTRL0
DAC0/GPJ3	SENBAT_V
DAC0/GPJ4	CHG_V
DAC0/GPJ5	CHG_ON

ITE8512E KB Matrlk interface

KSI0/STB#	KB_SIN0
KSI1/AFD#	KB_SIN1
KSI0/STB#	KB_SIN2
KSI3SLIN#	KB_SIN3
KSI4	KB_SIN4
KSI5	KB_SIN5
KSI6	KB_SIN6
KSI7	KB_SIN7
KSO0/PD0	KB_SOUT0
KSO1/PD1	KB_SOUT1
KSO2/PD2	KB_SOUT2
KSO2/PD3	KB_SOUT3
KSO2/PD4	KB_SOUT4
KSO2/PD5	KB_SOUT5
KSO2/PD6	KB_SOUT6
KSO2/PD7	KB_SOUT7
KSO8/ACK#	KB_SOUT8
KSO9/BUSY	KB_SOUT9
KSO10/PE	KB_SOUT10
KSO11/ERR#	KB_SOUT11
KSO12/SLCT	KB_SOUT12
KSO13	KB_SOUT13
KSO14	KB_SOUT14
KSO15	KB_SOUT15

ITE8512E SPI Flash ROM interface

FLFRAME#/GPG2	FLFRAME#
FLAD0/SCE#	SPI_CE#
FLAD1/S1	SPI_DIN
FLAD2/S2	SPI_DOUT
FLAD3/GPG6	LID#
FLCLK/SCK	SPI_CLK
FLRST#/WU17 /GPG0/TM	BKL_EC

ITE8512E System & LPC Bus

LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCCLK	CLK_PCI_LPC
WRST#	LRST#

ITE8512E Clock

CK32K	EC32KI
CK32KE	EC32KO

ITE8512E Power

VSTBY0	+3.3VA
VSTBY1	+3.3VA
VSTBY2	+3.3VA
VSTBY3	+3.3VA
VSTBY4	+3.3VA
VSTBY5	+3.3VA
VBAT	+3.3VA
AVCC	+3.3VA
VCC	+3.3V

945GSE

	CPU Socket P	GMCH GFX Freq/Core Volt	Memory	TDP
945GSE	Diamondville FSB 533 MHz	533MHZ/+V1.05	DDR2 400/533 MHz	3.5~5.5W

Diamondville CPU

Freg.(GHz)	CPU CORE(V)	ICC(A)	TDP(W)	TjMAX( )
1.6	VID fixed at 1.1V	2.2	2.5	90

ITE8512E GND

AVSS	EC-AVSS-75
VSS0	GND
VSS1	GND
VSS2	GND
VSS3	GND
VSS4	GND
VSS5	GND
VSS6	GND

945GMS GPIO

CFG_0	MCH_BSEL0
CFG_1	MCH_BSEL1
CFG_2	MCH_BSEL2
CFG_3	N.C
CFG_4	N.C
CFG_5	MCH_CFG_5
CFG_6	N.C
CFG_7	MCH_CFG_7
CFG_8	N.C
CFG_9	MCH_CFG_9
CFG_10	MCH_CFG_10
CFG_11	N.C
CFG_12	MCH_CFG_12
CFG_13	MCH_CFG_13
CFG_14	N.C
CFG_15	N.C
CFG_16	MCH_CFG_16
CFG_17	N.C
CFG_18	N.C
CFG_19	MCH_CFG_19
CFG_20	MCH_CFG_20

945GSE

VCC	ICC(mA)	mW	TEMP( )
+V1.05	3720	3906	105
+V1.5	2034	3051	
+V3.3	160	528	
+V1.8S	1752	3154	
+V0.9S	0.02	0.02	
+V2.5	142	355	

ICH7-M

VCC	ICC(mA)	mW	TEMP( )
+5V	6	30	70
+5VS	10	50	
+V3.3	366	1207	
+V3.3S	55	182	
+V1.5	1629	2444	
+V1.05	1001	1050	

ITE8512E

VCC	ICC(mA)	mW	TEMP( )
+V3.3A	300	990	70

ICS 9LPR310

VCC	ICC(mA)	mW	TEMP( )
+V3.3	450	1485	70

RTL8100CL

VCC	ICC(mA)	mW	TEMP( )
+V3.3S	80	264	70
+V2.5	40	100	

RTS5158E

VCC	ICC(mA)	mW	TEMP( )
+V3.3	250	825	70

ALC662

VCC	ICC(mA)	mW	TEMP( )
+5V	55	275	70
+V3.3	35	116	

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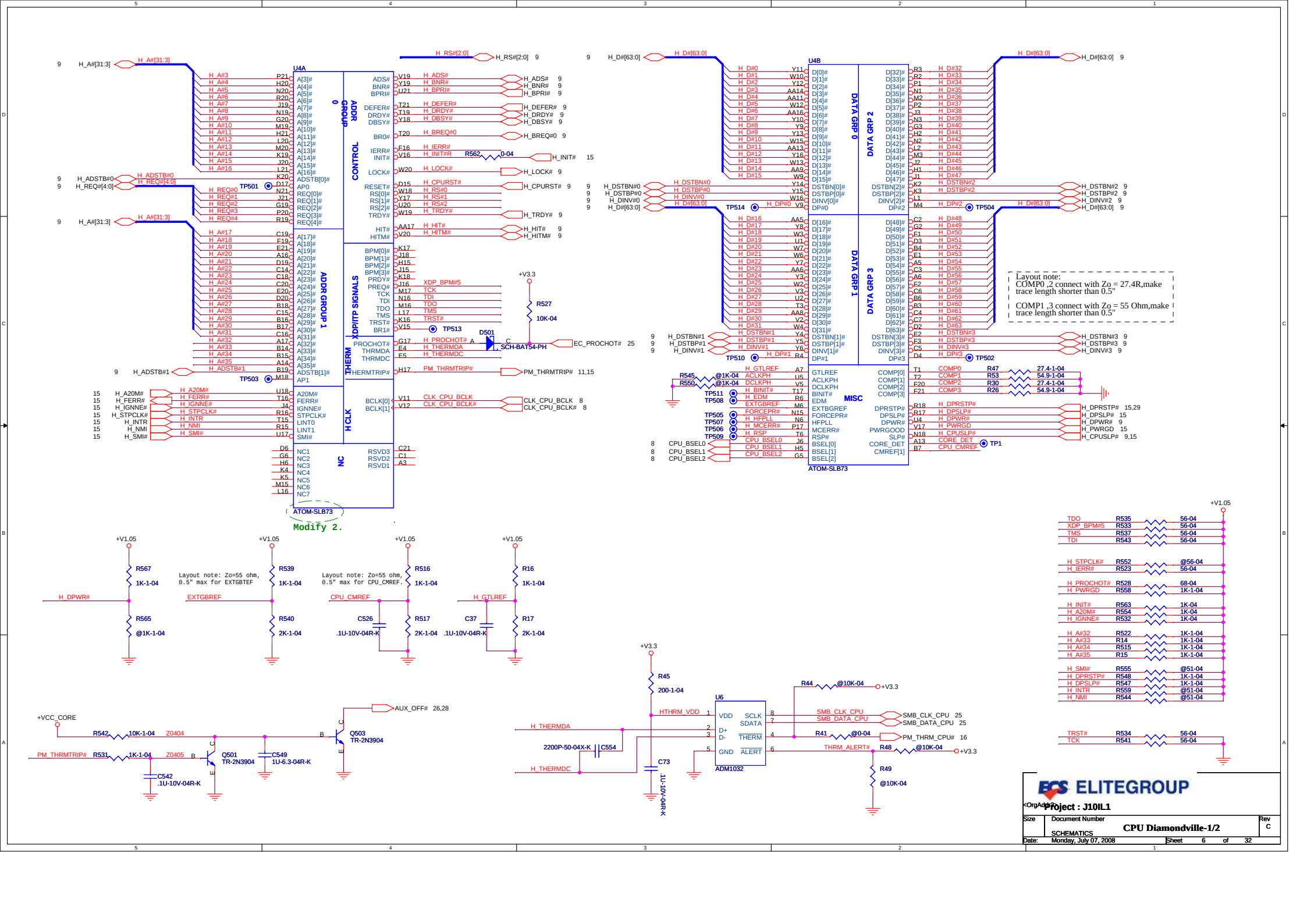
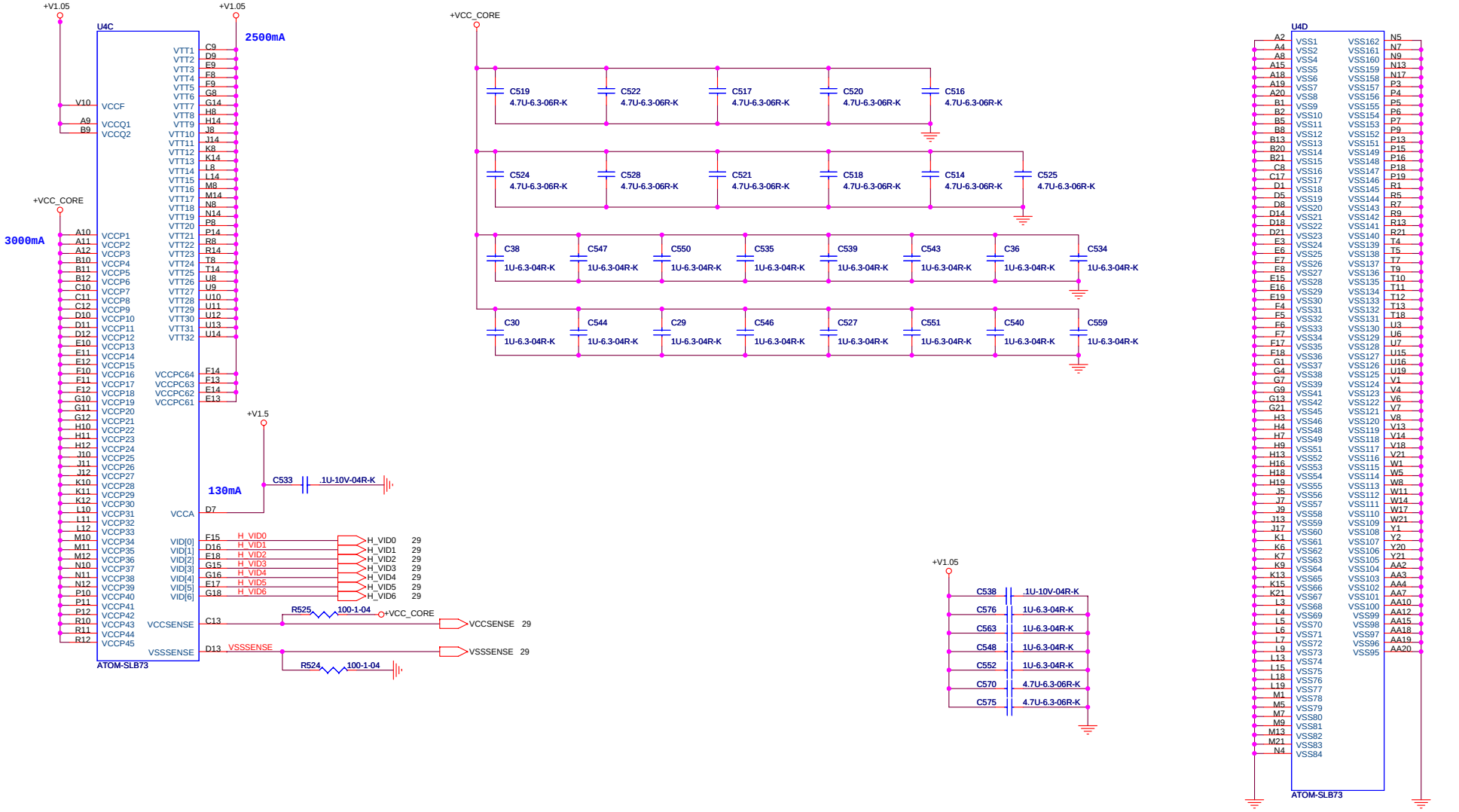
Project : J10IL1

Size	Document Number	Rev
	GPIO & POWER CONSUMPTION	C

Date: Monday, July 07, 2008 Sheet 5 of 32

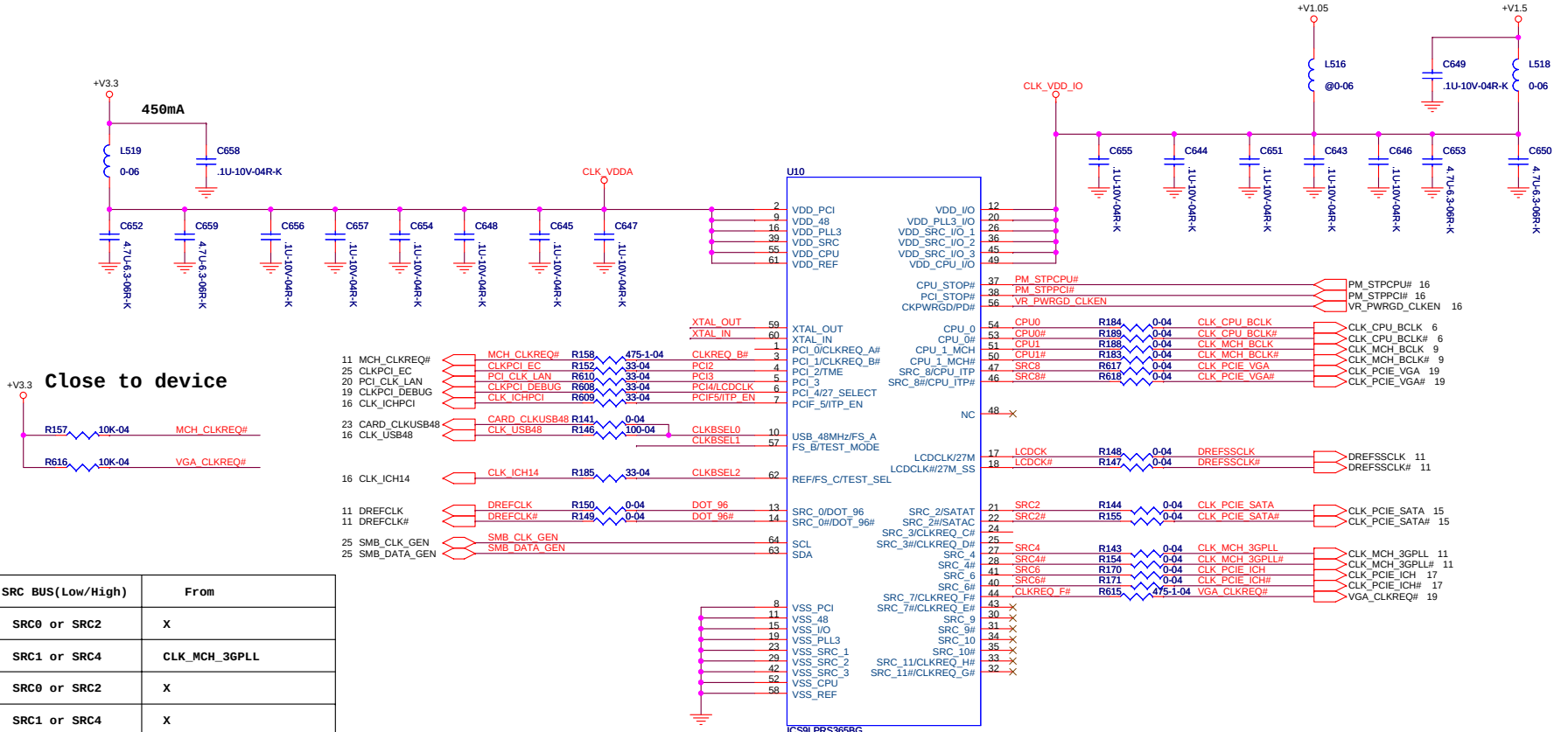

U4A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
NC
ATOM-SLB73
Modify 2.
U4B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
ATOM-SLB73
Layout note:
COMP0 ,2 connect with Zo = 27.4R,make trace length shorter than 0.5"
COMP1 ,3 connect with Zo = 55 Ohm,make trace length shorter than 0.5"
Layout note: Zo=55 ohm, 0.5" max for EXTGBTEF
Layout note: Zo=55 ohm, 0.5" max for CPU_CMREF.
U6
ADM1032
ELITEGROUP
Project : J10IL1
CPU Diamondville-1/2
SCHEMATICS
Monday, July 07, 2008
Sheet 6 of 32



ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	CPU Diamondville-2/2	C
Date: Monday, July 07, 2008	Sheet 7 of 32	



CLK REQ	Pin number	SRC BUS(Low/High)	From
A	Pin 1	SRC0 or SRC2	X
B	Pin 3	SRC1 or SRC4	CLK_MCH_3GPLL
C	Pin 24	SRC0 or SRC2	X
D	Pin 25	SRC1 or SRC4	X
E	Pin 43	SRC7 or SRC6	X
F	Pin 44	SRC7 or SRC8	CLK_PCIE_VGA
G	Pin 32	SRC11 or SRC9	X
H	Pin 33	SRC11 or SRC10	X

	BSEL2	BSEL1	BSEL0	MHZ
FSB533	0	0	1	133

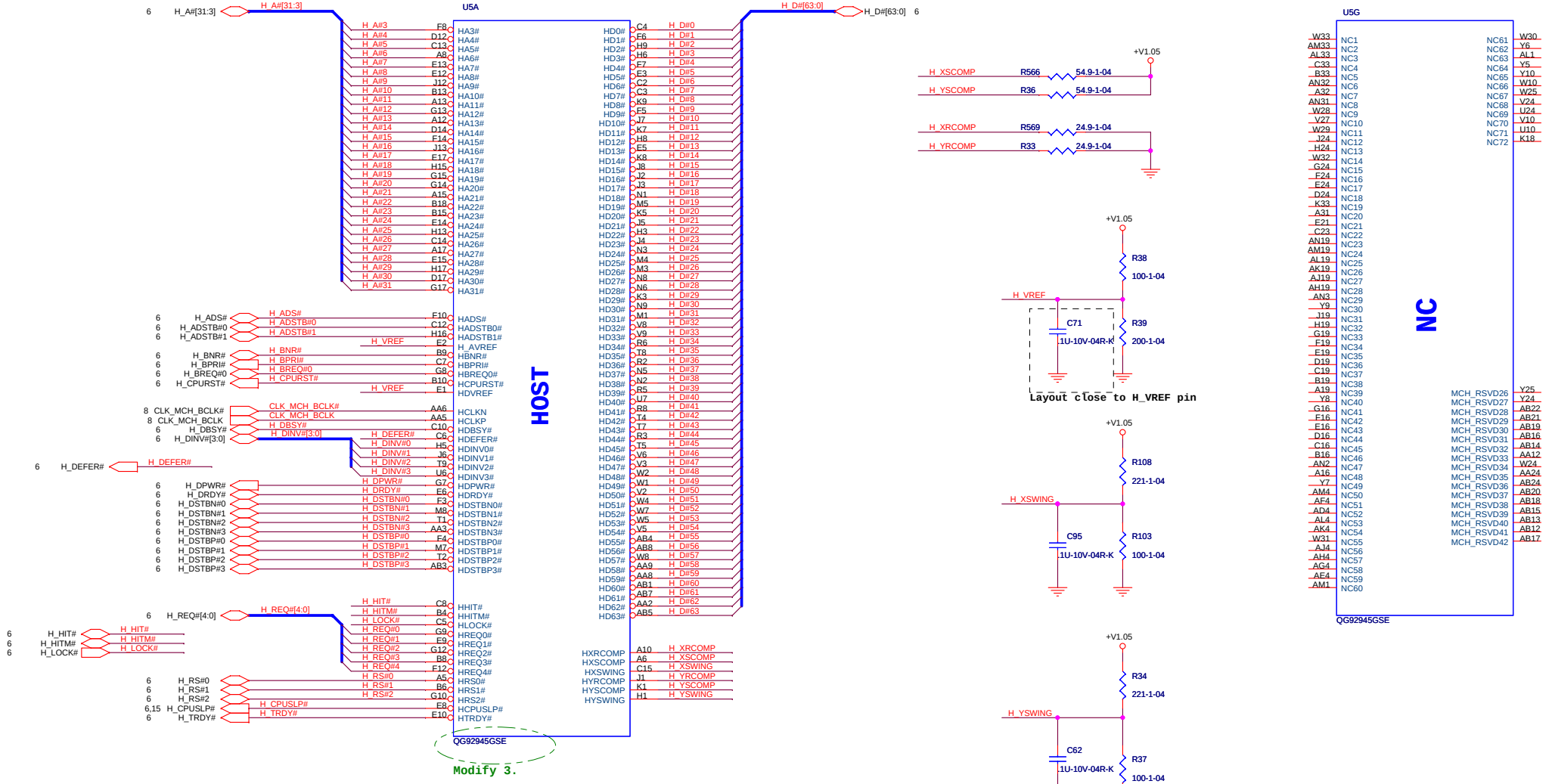
Ce = 2*CL - (Cs + Ci)
CL = Crystal Load Cap = 20P
Ci = IC internal Cap = 5P
Cs = 2P
Ce = Crystal external Cap = 33P

ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS CLOCK GENERATOR	C

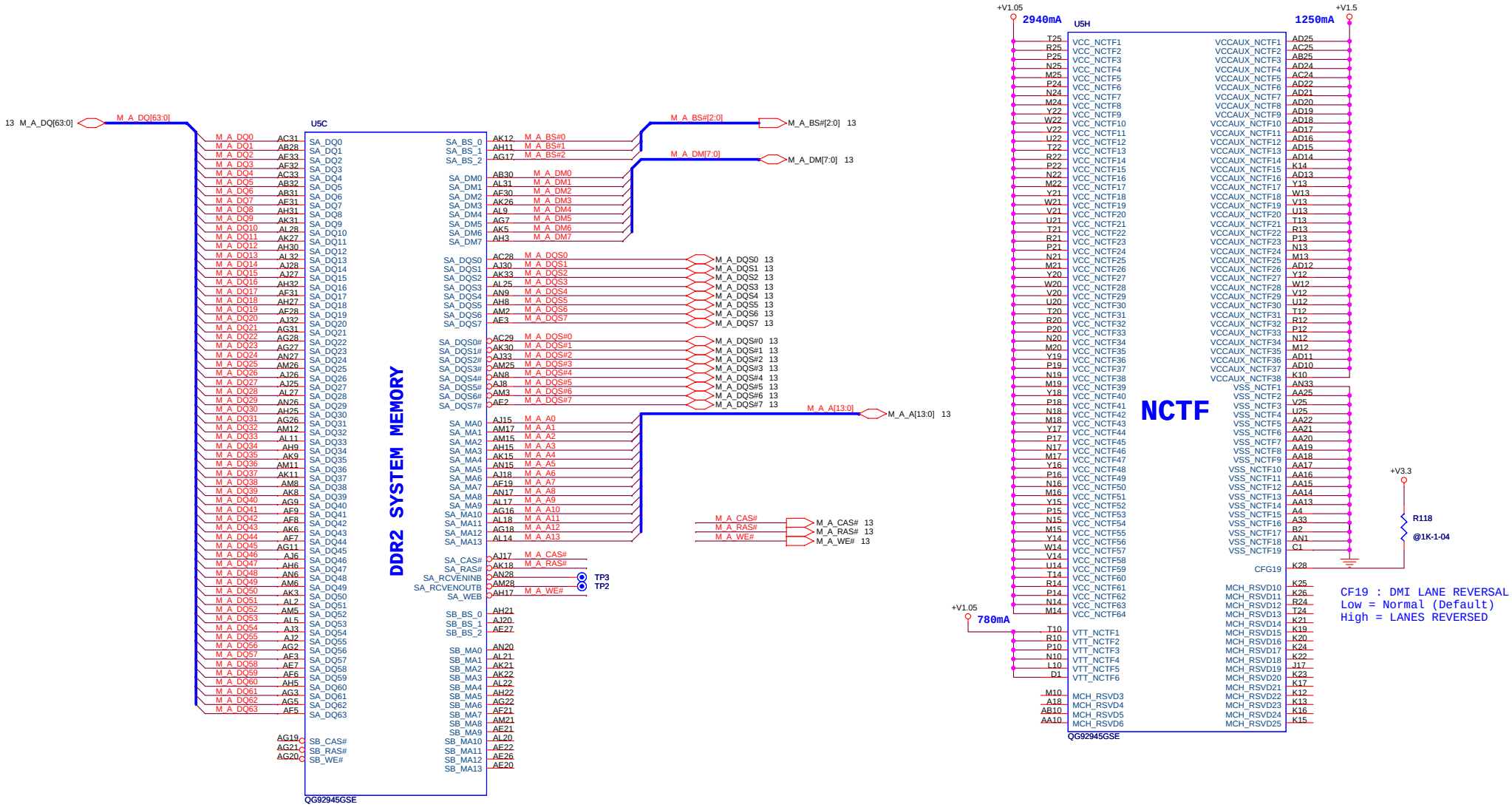
Date: Monday, July 07, 2008 Sheet 8 of 32



ELITEGROUP

Project : J10IL1

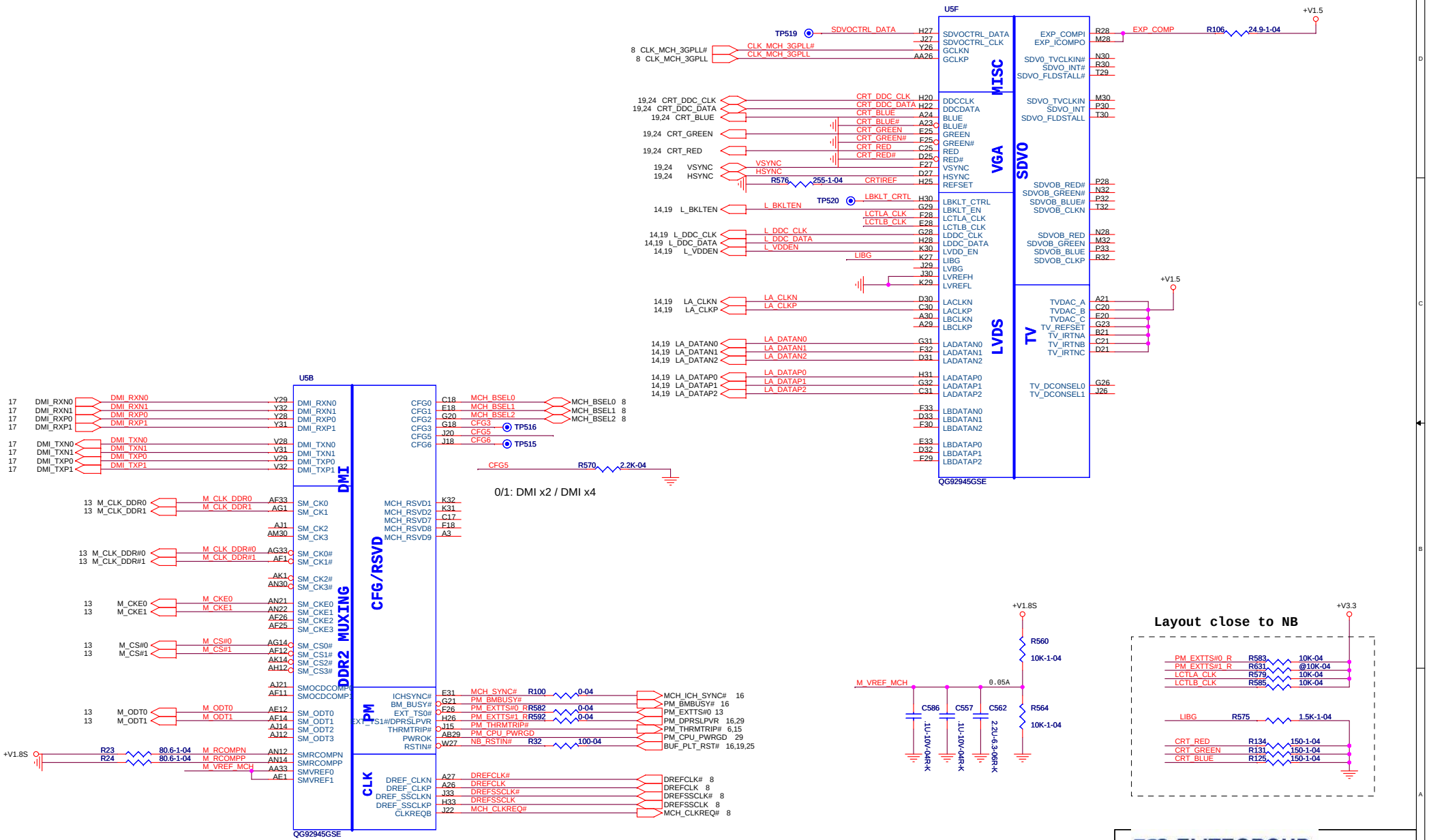
Size	Document Number	Rev
	SCHEMATICS 945GSE- Host(1/4)	C
Date: Monday, July 07, 2008	Sheet 9 of 32	



ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS 945GSE- DDR(2/4)	C
Date: Monday, July 07, 2008	Sheet 10 of 32	


U5F
MISC
VGA
SDVO
LVDS
TV
QG92945GSE
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET
LBKLT_CTRL
LBKLT_EN
LCTLA_CLK
LCTLB_CLK
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL
LACLKN
LACLKP
LBCLKN
LBCLKP
LADATAN0
LADATAN1
LADATAN2
LADATAP0
LADATAP1
LADATAP2
LBDATAN0
LBDATAN1
LBDATAN2
LBDATAP0
LBDATAP1
LBDATAP2
EXP_COMPI
EXP_ICOMPO
SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#
SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL
SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV_DCONSEL0
TV_DCONSEL1
TP519
TP520
R576 255-1-04 CRTIREF
R106 24.9-1-04 EXP_COMP
+V1.5
U5B
DMI
DDR2 MUXING
CFG/RSVD
PM
CLK
QG92945GSE
DMI_RXN0
DMI_RXN1
DMI_RXP0
DMI_RXP1
DMI_TXN0
DMI_TXN1
DMI_TXP0
DMI_TXP1
SM_CK0
SM_CK1
SM_CK2
SM_CK3
SM_CK0#
SM_CK1#
SM_CK2#
SM_CK3#
SM_CKE0
SM_CKE1
SM_CKE2
SM_CKE3
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
SMOCDCOMP0
SMOCDCOMP1
SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3
SMRCOMPN
SMRCOMPP
SMVREF0
SMVREF1
CFG0
CFG1
CFG2
CFG3
CFG5
CFG6
MCH_RSVD1
MCH_RSVD2
MCH_RSVD7
MCH_RSVD8
MCH_RSVD9
ICHSYNC#
BM_BUSY#
EXT_TS0#
EXT_TS1#/DPRSLPVR
THRMTRIP#
PWROK
RSTIN#
DREF_CLKN
DREF_CLKP
DREF_SSCLKN
DREF_SSCLKP
CLKREQB
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
TP516
TP515
R570 2.2K-04
0/1: DMI x2 / DMI x4
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR#0
M_CLK_DDR#1
M_CKE0
M_CKE1
M_CS#0
M_CS#1
M_ODT0
M_ODT1
M_RCOMPN
M_RCOMPP
M_VREF_MCH
R23 80.6-1-04
R24 80.6-1-04
MCH_SYNC# R100 0-04
PM_BMBUSY# R582 0-04
PM_EXTTS#1 R592 0-04
PM_THRMTRIP#
PM_CPU_PWRGD
NB_RSTIN# R32 100-04
DREFCLK#
DREFCLK
DREFSSCLK#
DREFSSCLK
MCH_CLKREQ#
+V1.8S
R560 10K-1-04
R564 10K-1-04
0.05A
C586 .1U-10V-04R-K
C557 .1U-10V-04R-K
C562 2.2U-6.3-06R-K
Layout close to NB
+V3.3
PM_EXTTS#0_R R583 10K-04
PM_EXTTS#1_R R631 @10K-04
LCTLA_CLK R579 10K-04
LCTLB_CLK R585 10K-04
LIBG R575 1.5K-1-04
CRT_RED R134 150-1-04
CRT_GREEN R131 150-1-04
CRT_BLUE R125 150-1-04
ELITEGROUP
<OrgAddr2>
Project : J10IL1
Size
Document Number
SCHEMATICS
945GSE- DMI & VGA(3/4)
Rev C
Date: Monday, July 07, 2008
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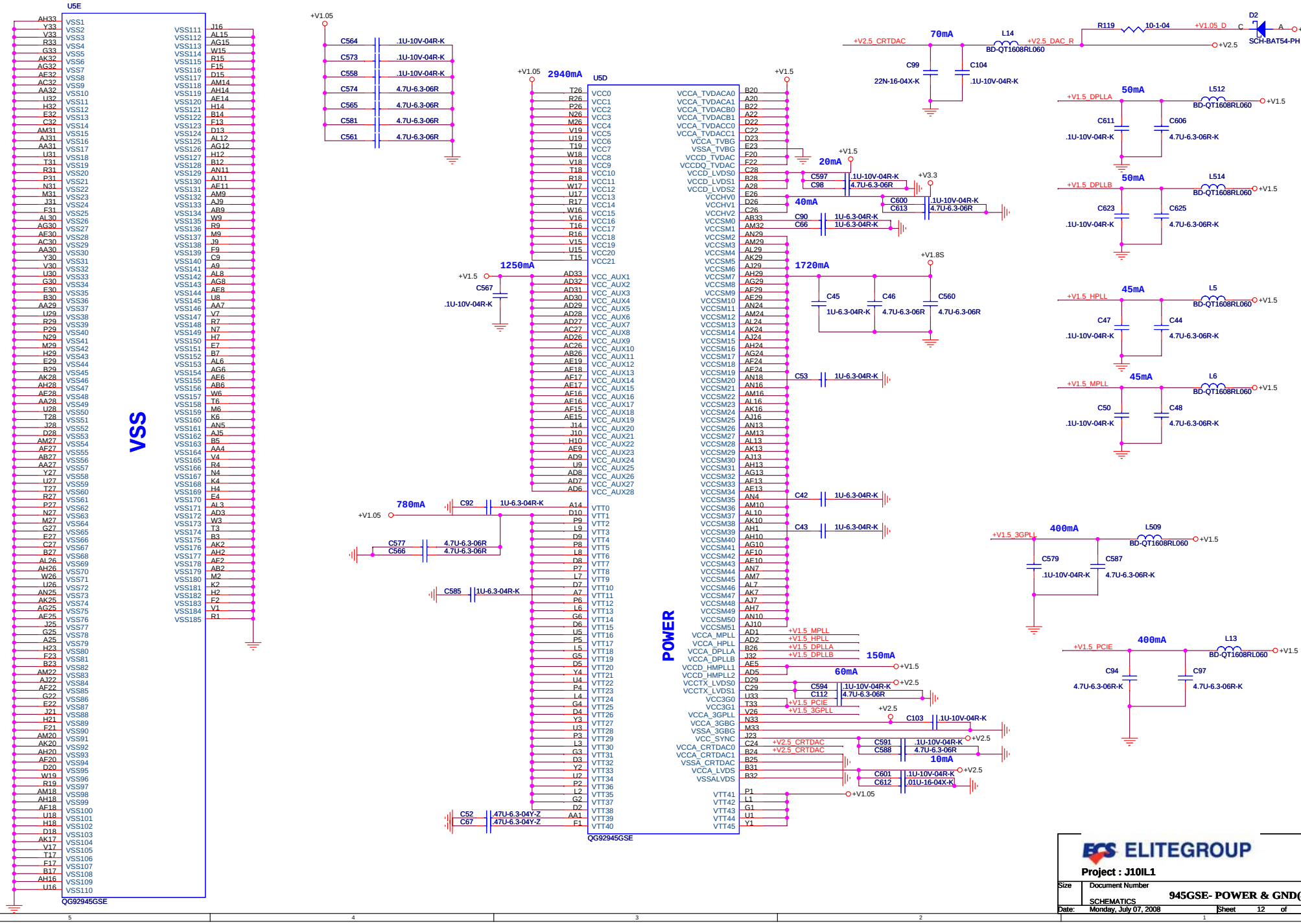
U5E
VSS
QG92945GSE
U5D
POWER
QG92945GSE
2940mA
1250mA
780mA
70mA
20mA
40mA
1720mA
60mA
150mA
10mA
50mA
45mA
400mA
L14
BD-QT1608RL060
SCH-BAT54-PH
ELITEGROUP
Project : J10IL1
945GSE- POWER & GND(4/4)
SCHEMATICS
Rev C
Date: Monday, July 07, 2008
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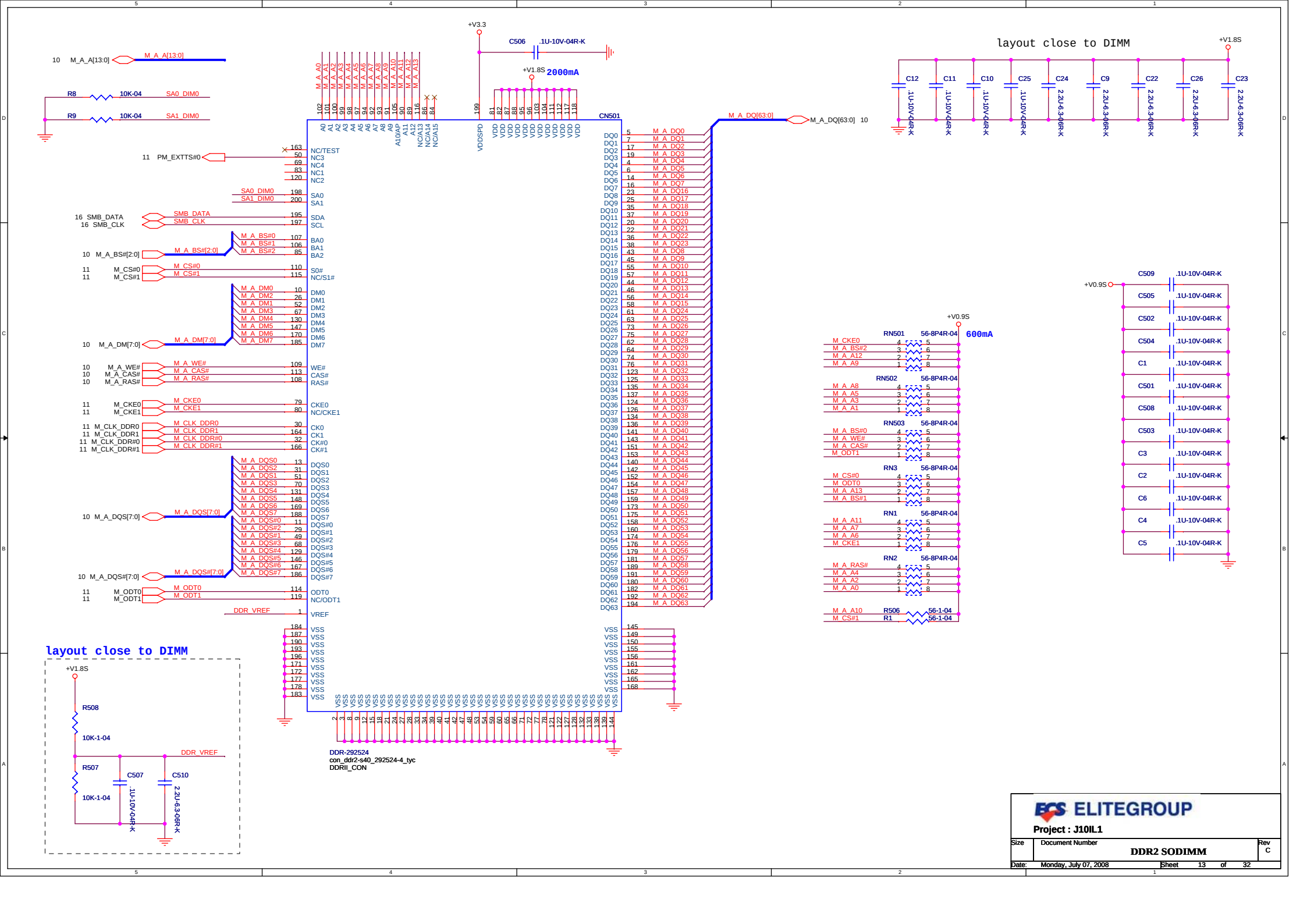
layout close to DIMM
+V1.8S
C12 .1U-10V-04R-K
C11 .1U-10V-04R-K
C10 .1U-10V-04R-K
C25 .1U-10V-04R-K
C24 2.2U-6.3-06R-K
C9 2.2U-6.3-06R-K
C22 2.2U-6.3-06R-K
C26 2.2U-6.3-06R-K
C23 2.2U-6.3-06R-K
+V3.3
C506 .1U-10V-04R-K
+V1.8S 2000mA
CN501
M_A_DQ[63:0]
10 M_A_A[13:0]
M_A_A[13:0]
R8 10K-04 SA0_DIM0
R9 10K-04 SA1_DIM0
11 PM_EXTTS#0
SA0_DIM0
SA1_DIM0
16 SMB_DATA
16 SMB_CLK
SMB_DATA
SMB_CLK
M_A_BS#0
M_A_BS#1
M_A_BS#2
10 M_A_BS#[2:0]
11 M_CS#0
11 M_CS#1
M_CS#0
M_CS#1
M_A_DM0
M_A_DM2
M_A_DM1
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
10 M_A_DM[7:0]
10 M_A_WE#
10 M_A_CAS#
10 M_A_RAS#
M_A_WE#
M_A_CAS#
M_A_RAS#
11 M_CKE0
11 M_CKE1
M_CKE0
M_CKE1
11 M_CLK_DDR0
11 M_CLK_DDR1
11 M_CLK_DDR#0
11 M_CLK_DDR#1
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR#0
M_CLK_DDR#1
M_A_DQS0
M_A_DQS2
M_A_DQS1
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
10 M_A_DQS[7:0]
M_A_DQS#0
M_A_DQS#2
M_A_DQS#1
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7
10 M_A_DQS#[7:0]
11 M_ODT0
11 M_ODT1
M_ODT0
M_ODT1
DDR_VREF
NC/TEST
NC3
NC4
NC1
NC2
SA0
SA1
SDA
SCL
BA0
BA1
BA2
S0#
NC/S1#
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
WE#
CAS#
RAS#
CKE0
NC/CKE1
CK0
CK1
CK#0
CK#1
DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7
DQS#0
DQS#1
DQS#2
DQS#3
DQS#4
DQS#5
DQS#6
DQS#7
ODT0
NC/ODT1
VREF
VSS
VDDSPD
VDD
DQ0
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M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
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M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
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M_A_DQ27
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M_A_DQ36
M_A_DQ37
M_A_DQ38
M_A_DQ39
M_A_DQ40
M_A_DQ41
M_A_DQ42
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M_A_DQ46
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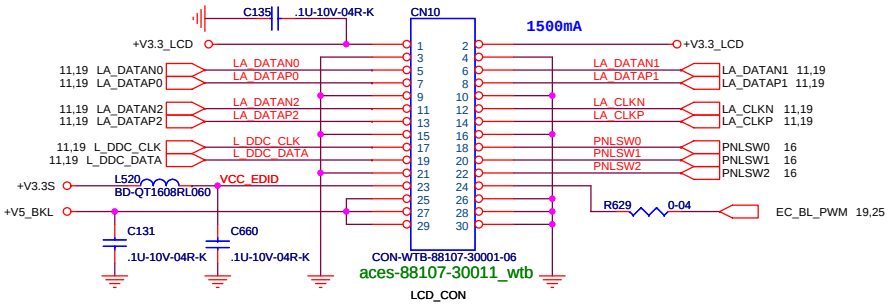
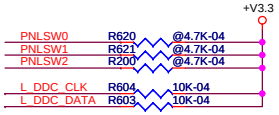
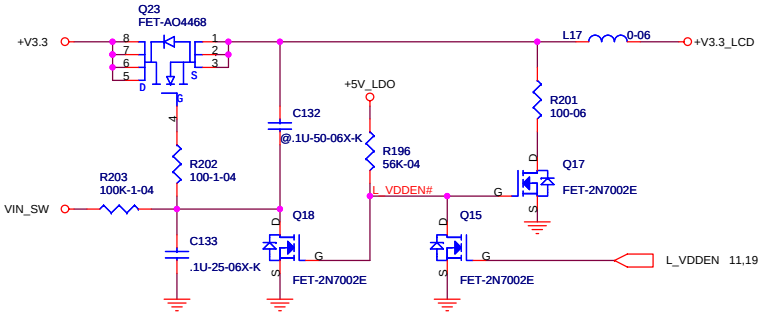
M_A_DQ51
M_A_DQ52
M_A_DQ53
M_A_DQ54
M_A_DQ55
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
DDR-292524
con_ddr2-s40_292524-4_tyc
DDRII_CON
+V0.9S
600mA
RN501 56-8P4R-04
M_CKE0
M_A_BS#2
M_A_A12
M_A_A9
RN502 56-8P4R-04
M_A_A8
M_A_A5
M_A_A3
M_A_A1
RN503 56-8P4R-04
M_A_BS#0
M_A_WE#
M_A_CAS#
M_ODT1
RN3 56-8P4R-04
M_CS#0
M_ODT0
M_A_A13
M_A_BS#1
RN1 56-8P4R-04
M_A_A11
M_A_A7
M_A_A6
M_CKE1
RN2 56-8P4R-04
M_A_RAS#
M_A_A4
M_A_A2
M_A_A0
M_A_A10 R506 56-1-04
M_CS#1 R1 56-1-04
+V0.9S
C509 .1U-10V-04R-K
C505 .1U-10V-04R-K
C502 .1U-10V-04R-K
C504 .1U-10V-04R-K
C1 .1U-10V-04R-K
C501 .1U-10V-04R-K
C508 .1U-10V-04R-K
C503 .1U-10V-04R-K
C3 .1U-10V-04R-K
C2 .1U-10V-04R-K
C6 .1U-10V-04R-K
C4 .1U-10V-04R-K
C5 .1U-10V-04R-K
layout close to DIMM
+V1.8S
R508 10K-1-04
DDR_VREF
R507 10K-1-04
C507 .1U-10V-04R-K
C510 2.2U-6.3-06R-K
ELITEGROUP
Project : J10IL1
Size
Document Number
DDR2 SODIMM
Rev C
Date: Monday, July 07, 2008
Sheet 13 of 32

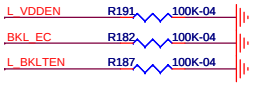
LCD PANEL ID SELECT

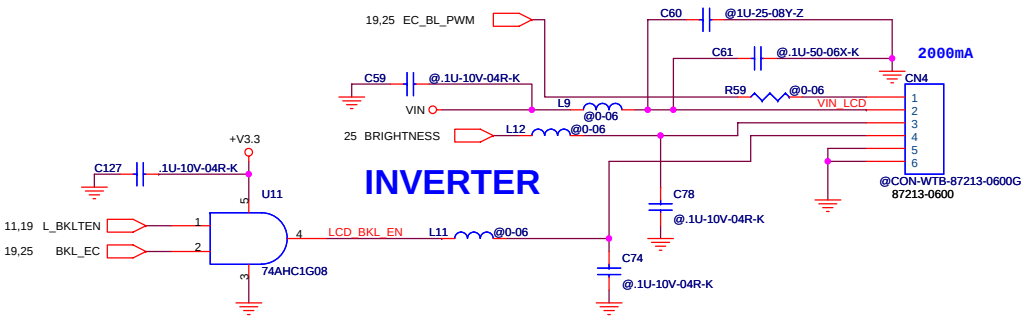
PNLSW2	PNLSW1	PNLSW0	Panel type
L	L	L	Reserved
H	H	H	800X480 (CPT 7") old
H	H	L	800X480 (TPO 7")
H	L	H	800X480 (Samsung 7")
H	L	L	800X480 (CPT 7") new
L	H	H	800X480 (CPT 9")
L	H	L	1024X600 (AUO 8.9")

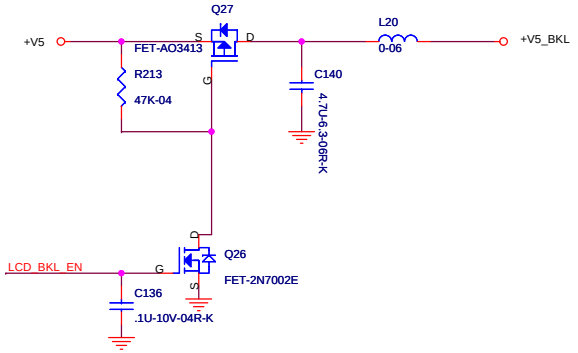








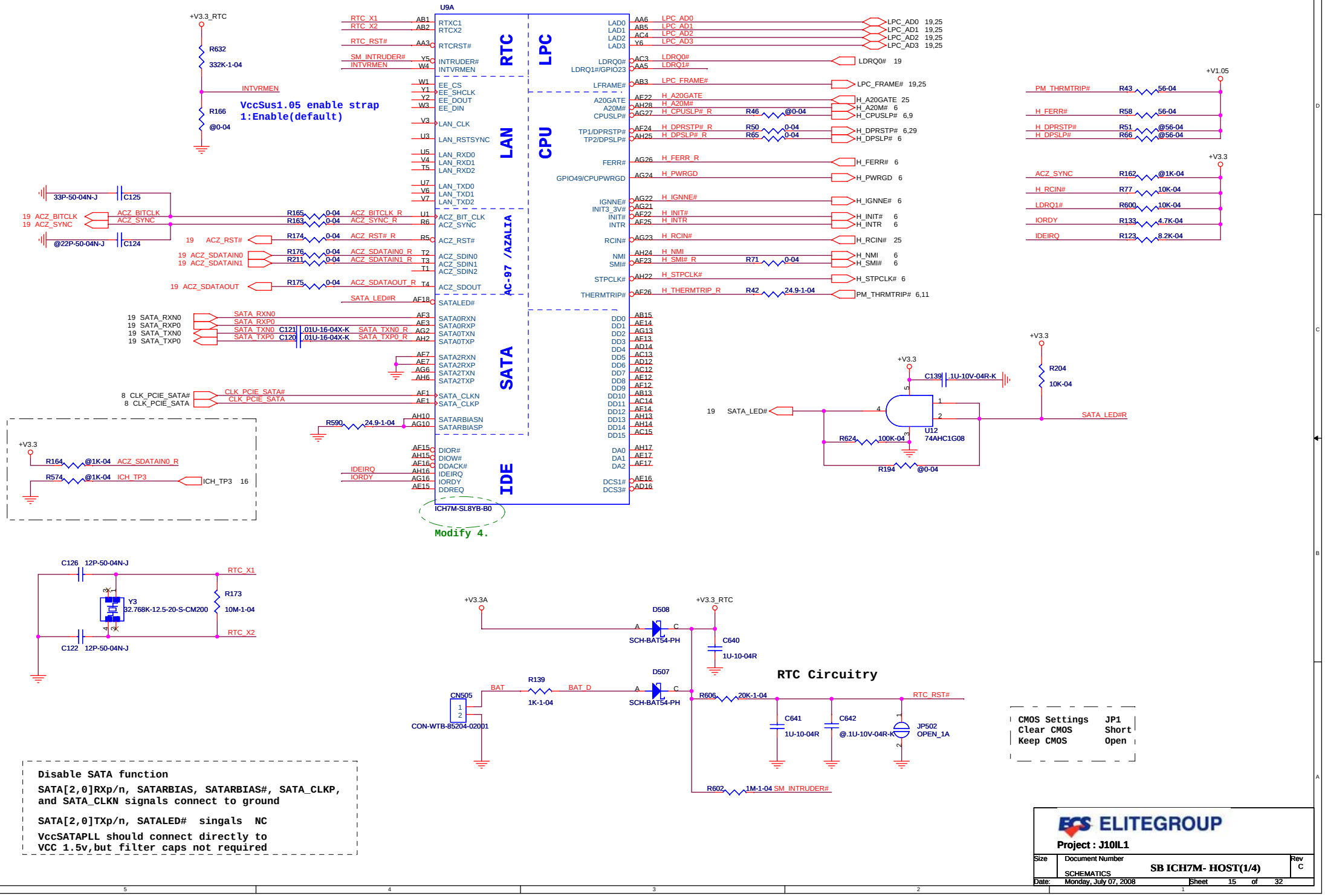




ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS LCD	C
Date: Monday, July 07, 2008	Sheet 14 of 32	


U9A
RTC
LPC
LAN
CPU
AC-97 /AZALIA
SATA
IDE
ICH7M-SL8YB-B0
+V3.3_RTC
R632
332K-1-04
INTVRMEN
R166
@0-04
VccSus1.05 enable strap
1:Enable(default)
RTC_X1
RTC_X2
RTC_RST#
SM_INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LDRQ0#
LPC_FRAME#
H_A20GATE
H_A20M#
H_CPUSLP#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
H_RCIN#
H_NMI
H_SMI#
H_STPCLK#
PM_THRMTRIP#
R46
R50
R65
R71
R42
R43
R58
R51
R66
+V1.05
+V3.3
ACZ_SYNC
H_RCIN#
LDRQ1#
IORDY
IDEIRQ
R162
R77
R600
R133
R123
33P-50-04N-J
C125
@22P-50-04N-J
C124
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDATAOUT
R165
R163
R174
R176
R211
R175
ACZ_BITCLK_R
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0_R
ACZ_SDATAIN1_R
ACZ_SDATAOUT_R
SATA_LED#R
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
C121
C120
.01U-16-04X-K
SATA_TXN0_R
SATA_TXP0_R
CLK_PCIE_SATA#
CLK_PCIE_SATA
R590
24.9-1-04
C139
.1U-10V-04R-K
R204
10K-04
U12
74AHC1G08
R624
100K-04
R194
@0-04
R164
@1K-04
R574
ICH_TP3
C126
C122
12P-50-04N-J
Y3
32.768K-12.5-20-S-CM200
R173
10M-1-04
D508
D507
SCH-BAT54-PH
C640
1U-10-04R
R139
1K-1-04
CN505
CON-WTB-85204-02001
R606
20K-1-04
C641
C642
@.1U-10V-04R-K
JP502
OPEN_1A
R602
1M-1-04
RTC Circuitry
CMOS Settings
Clear CMOS
Keep CMOS
JP1
Short
Open
Modify 4.
Disable SATA function
SATA[2,0]RXp/n, SATARBIAS, SATARBIAS#, SATA_CLKP, and SATA_CLKN signals connect to ground
SATA[2,0]TXp/n, SATALED# singals NC
VccSATAPLL should connect directly to VCC 1.5v,but filter caps not required
ELITEGROUP
Project : J10IL1
Size
Document Number
SB ICH7M- HOST(1/4)
Rev C
SCHEMATICS
Date: Monday, July 07, 2008
Sheet 15 of 32

Layout Note: Place stuffing option minimize stubs

for Singal cross power plane compensate

U9B

PCI

INTERRUPT I/F

MISC

ICH7M-SL8YB-B0

U9C

SMB

SATA GPIO

CLOCKS

SYS-GPIO

Power MGT

GPIO

ICH7M-SL8YB-B0

GNT#5 GNT#4
0 1 = SPI
1 0 = PCI
1 1 = LPC (Defult)

C56 .1U-10V-04R-K

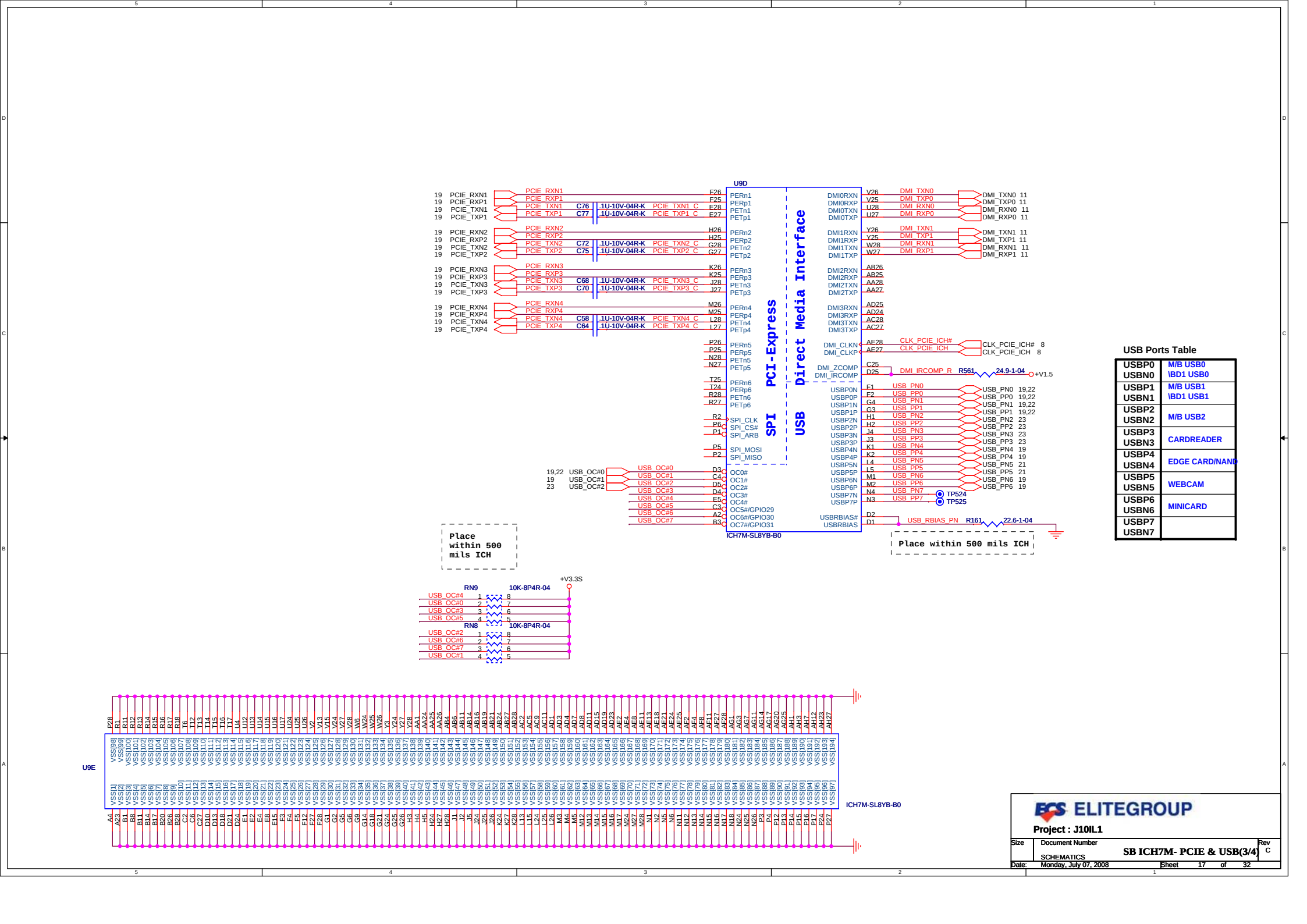
U3 74AHC1G08

Q504 FET-2N7002E

ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS SB ICH7M- PCI & GPIO(2/4)	C
Date: Monday, July 07, 2008	Sheet 16 of 32	



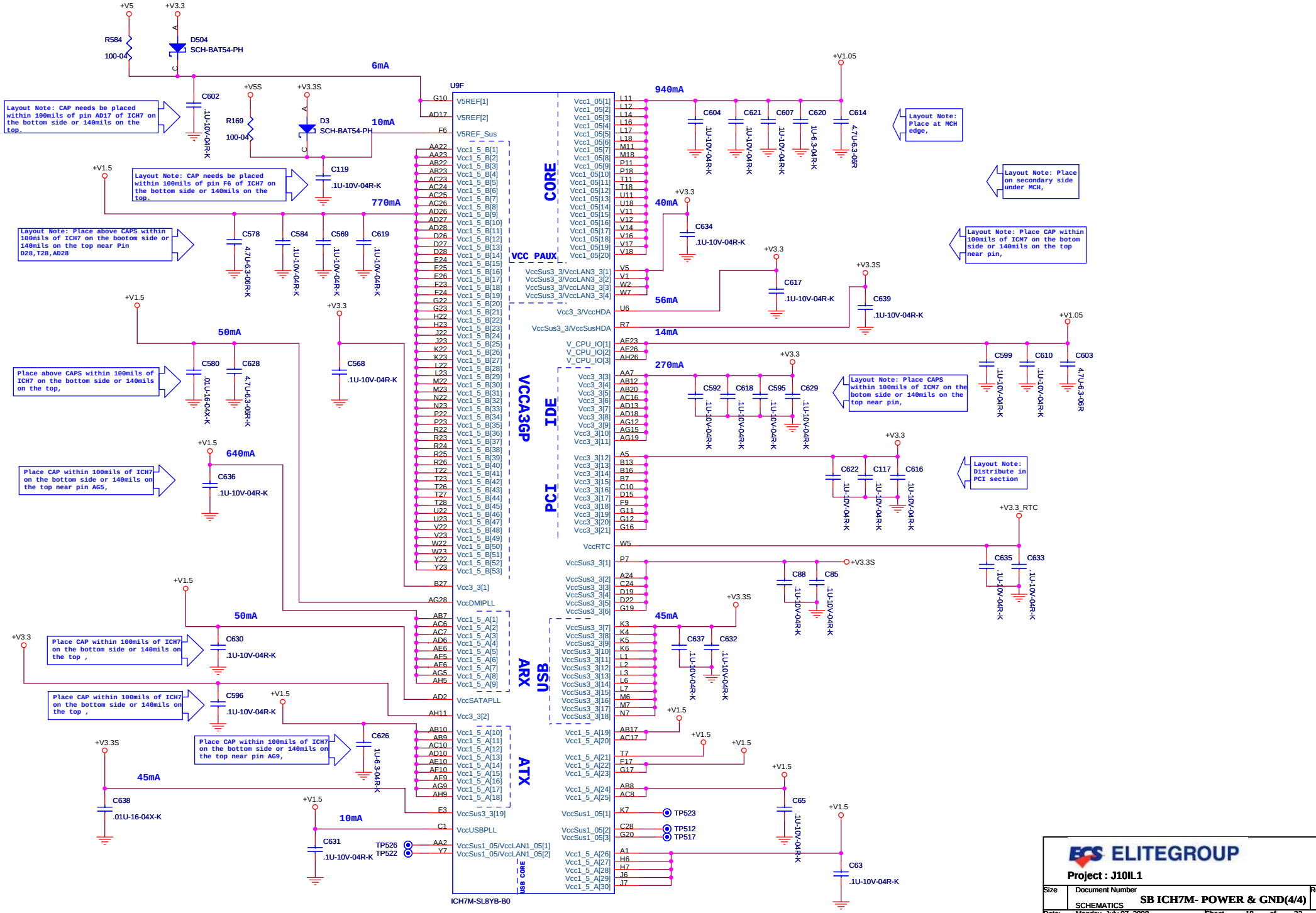
USB Ports Table

USBP0 USBN0	M/B USB0 \BD1 USB0
USBP1 USBN1	M/B USB1 \BD1 USB1
USBP2 USBN2	M/B USB2
USBP3 USBN3	CARDREADER
USBP4 USBN4	EDGE CARD/NAND
USBP5 USBN5	WEBCAM
USBP6 USBN6	MINICARD
USBP7 USBN7	

ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS SB ICH7M- PCIE & USB(3/4)	C
Date: Monday, July 07, 2008	Sheet 17 of 32	

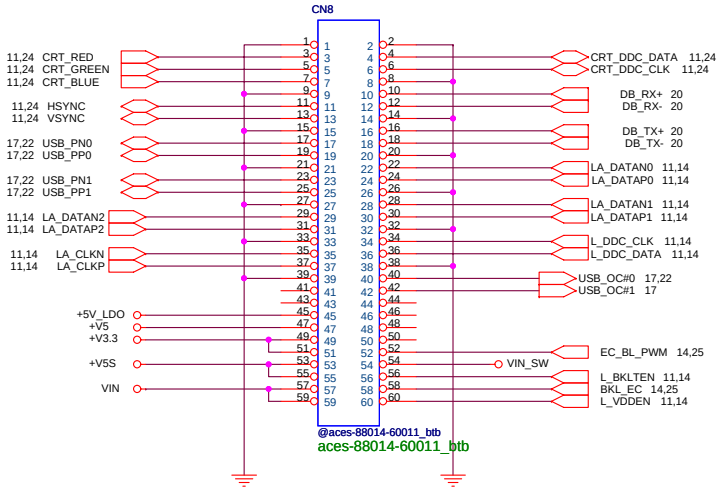


ELITEGROUP

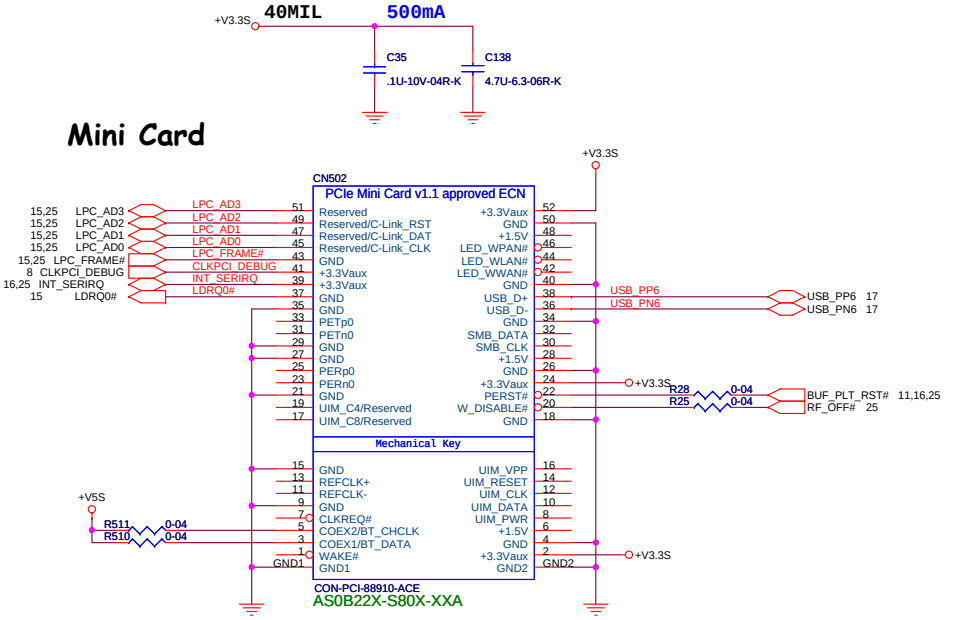
Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS SB ICH7M- POWER & GND(4/4)	C
Date: Monday, July 07, 2008	Sheet 18 of 32	

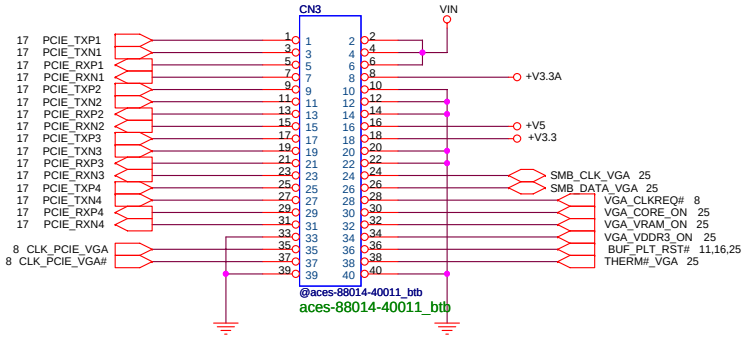
Daughter BD1 Connector



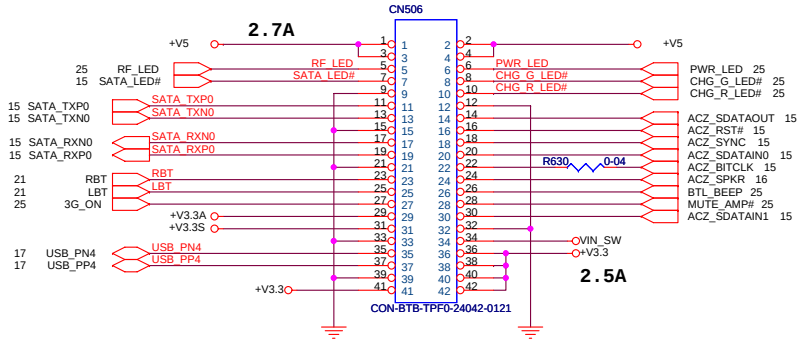
Mini Card



Daughter BD1 Connector



BD2 Connector

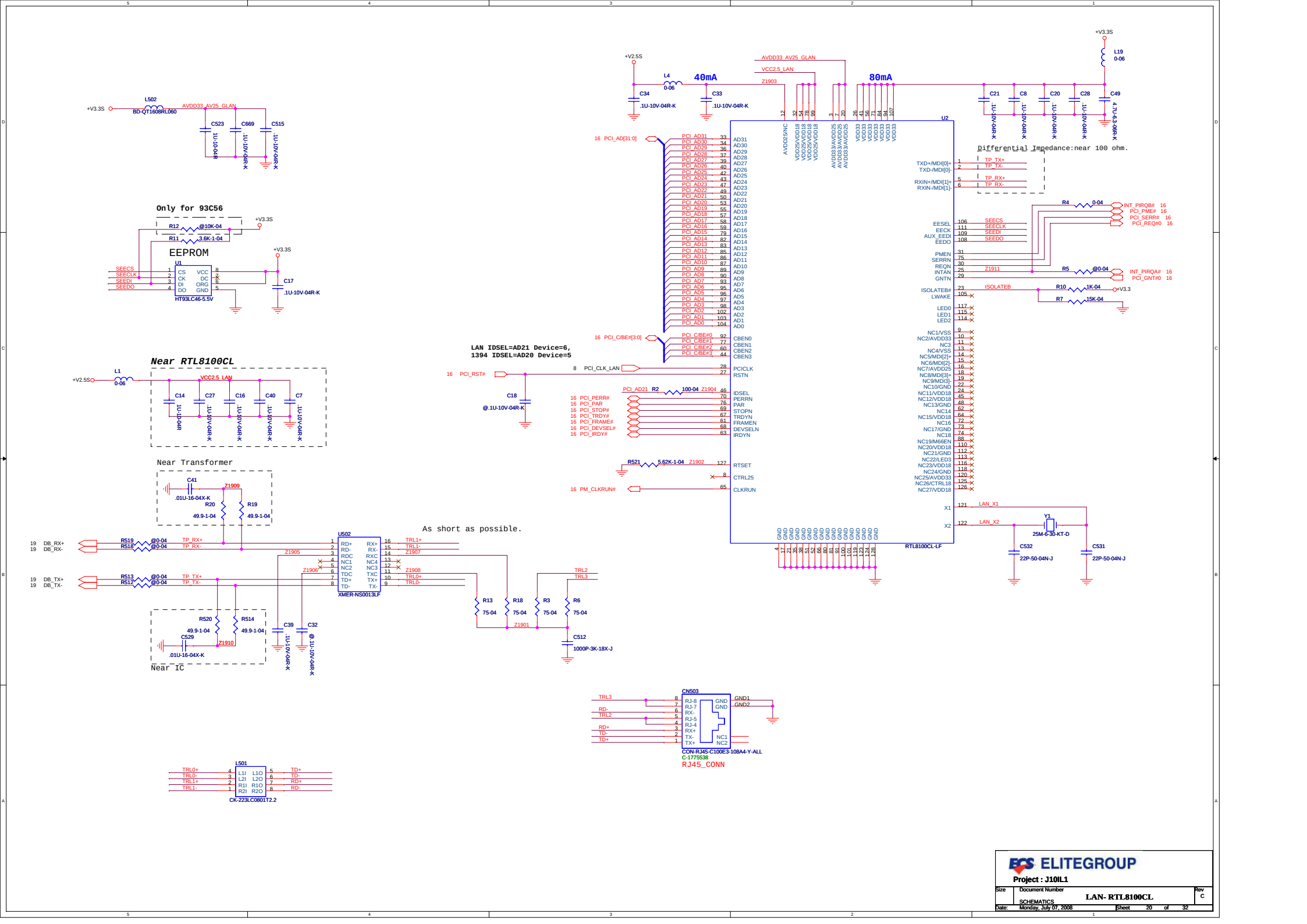


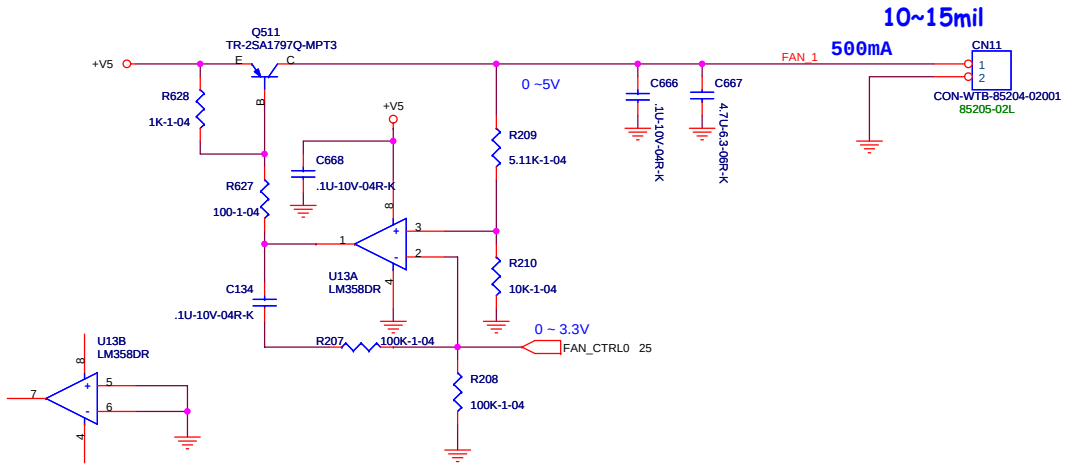
con_bb_42V127_TPF0240420121_cen

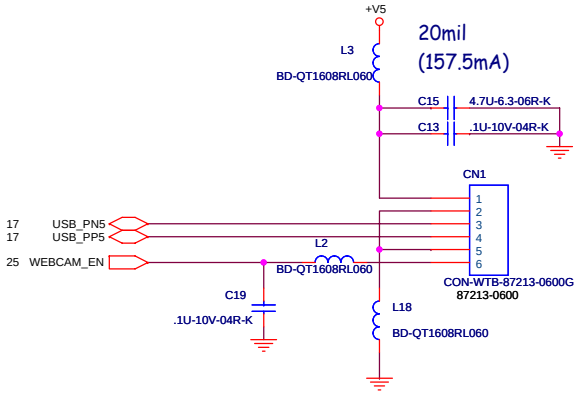
ECS ELITEGROUP

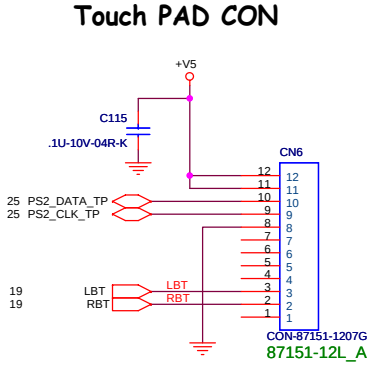
Project : J10IL1

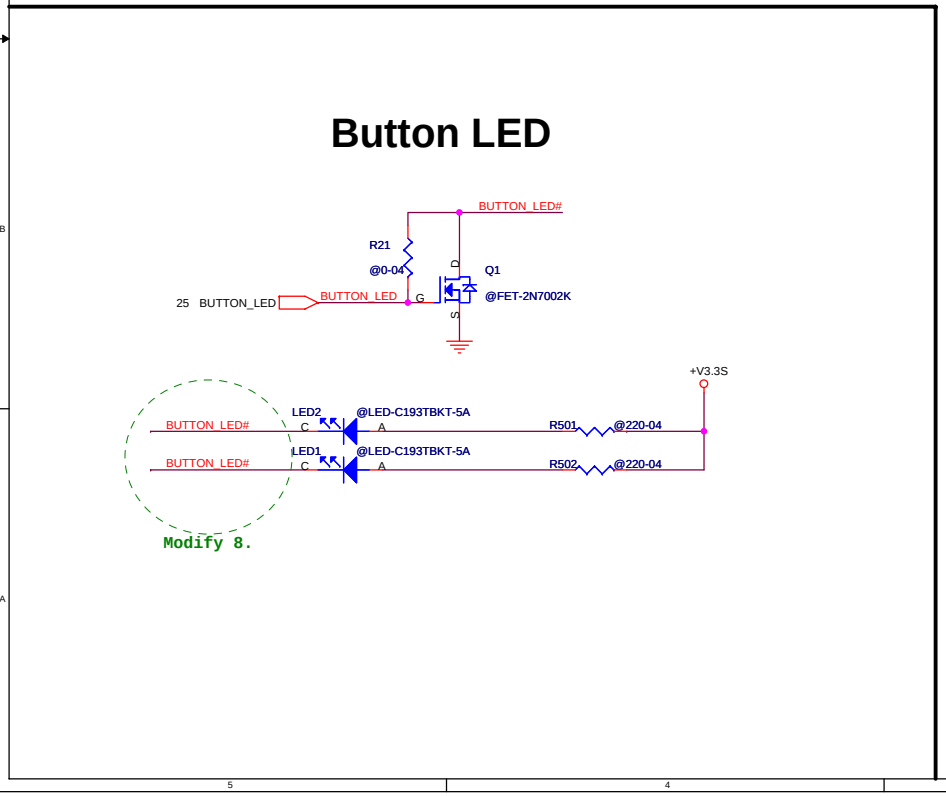
Size	Document Number	Rev
	MINICARD/BD1/BD2	C
	SCHEMATICS	
Date: Monday, July 07, 2008	Sheet 19 of 32	

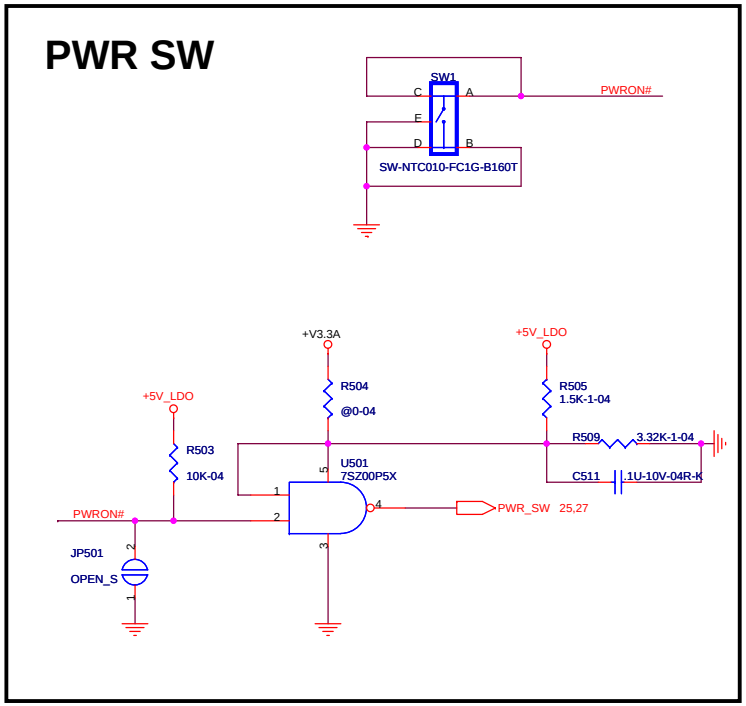

Only for 93C56
EEPROM
HT93LC46-5.5V
Near RTL8100CL
Near Transformer
Near IC
As short as possible.
LAN IDSEL=AD21 Device=6,
1394 IDSEL=AD20 Device=5
Differential Impedance:near 100 ohm.
RTL8100CL-LF
XMER-NS0013LF
CK-223LC0801T2.2
CON-RJ45-C100E3-108A4-Y-ALL
C-1775538
RJ45_CONN
ELITEGROUP
Project : J10IL1
LAN- RTL8100CL
SCHEMATICS
Monday, July 07, 2008











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Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS WEBCAM/TOUCH PAD/FAN/PW	C
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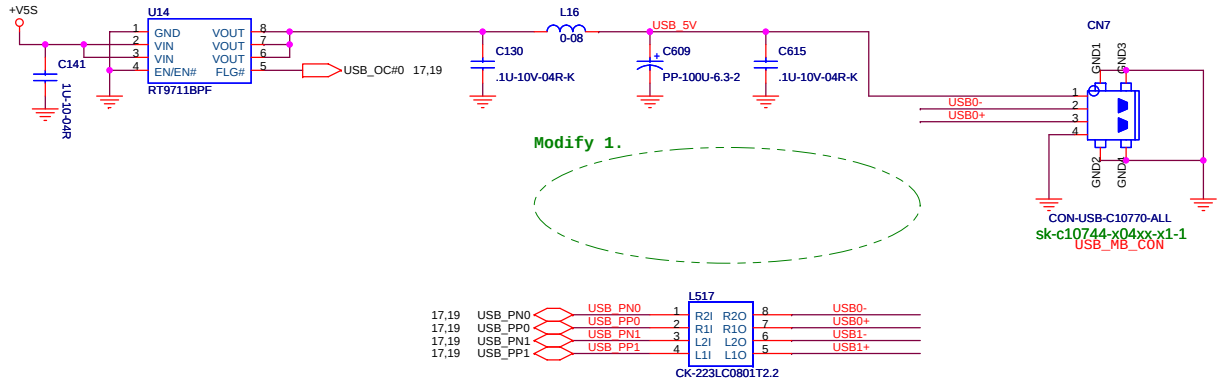
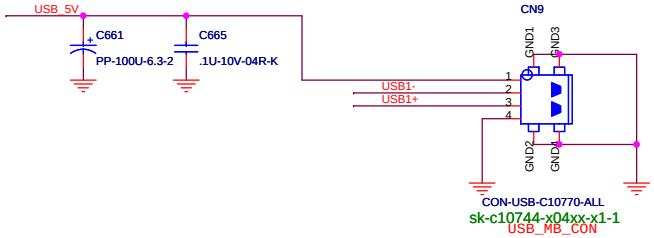
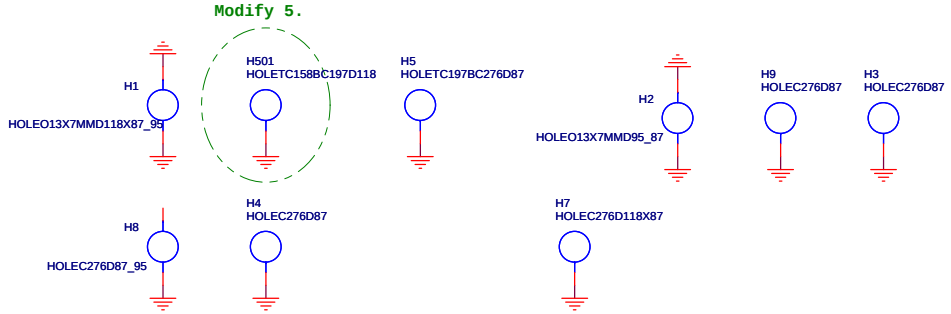


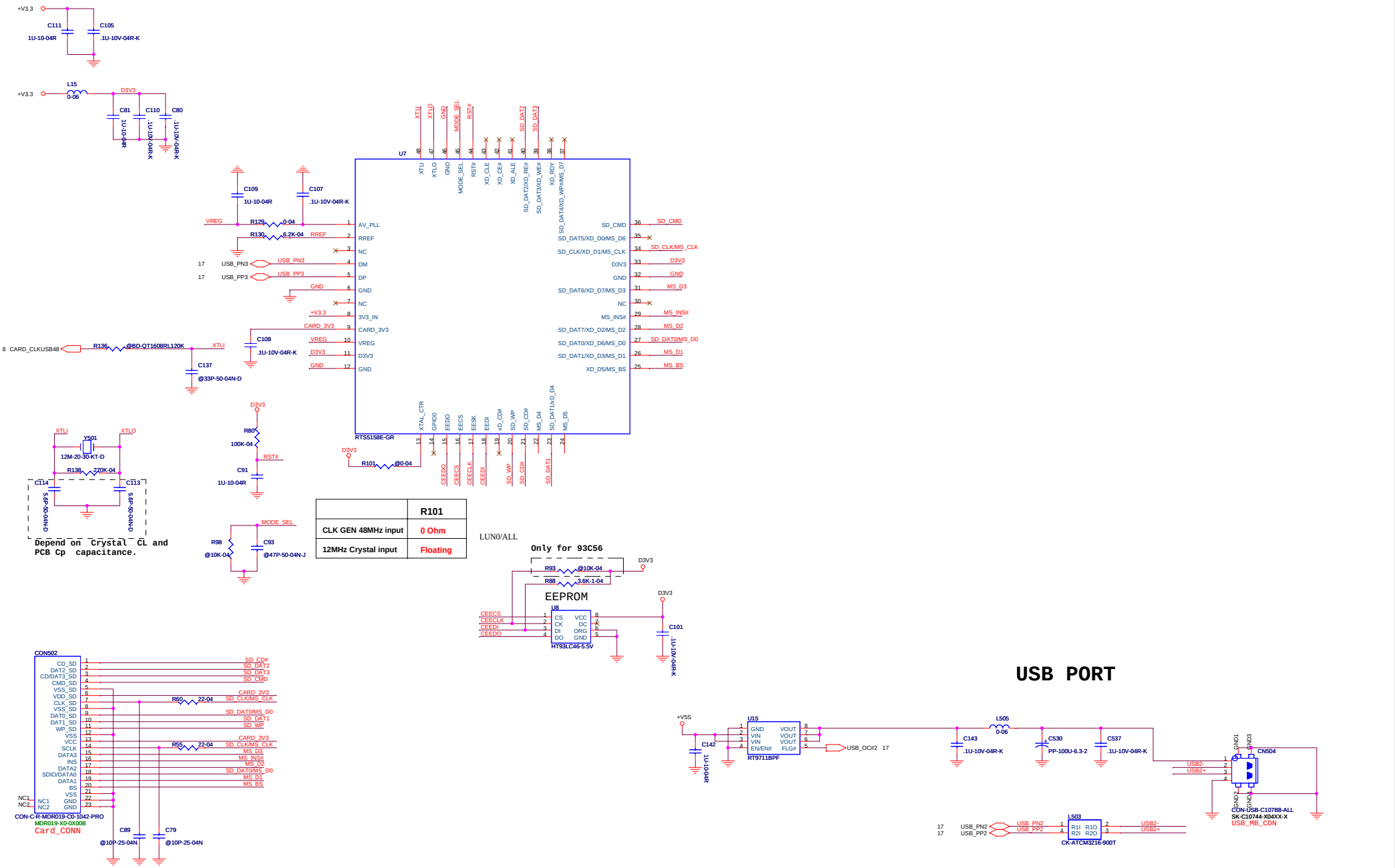




ELITEGROUP

Project : J10IL1

Size	Document Number	Rev
	SCHEMATICS USB CONN	C
Date: Monday, July 07, 2008	Sheet 22 of 32	



	R101
CLK GEN 48MHz input	0 Ohm
12MHz Crystal input	Floating

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Project : J10IL1

Size	Document Number	Rev
	CARD/USB CON	C
	SCHEMATICS	

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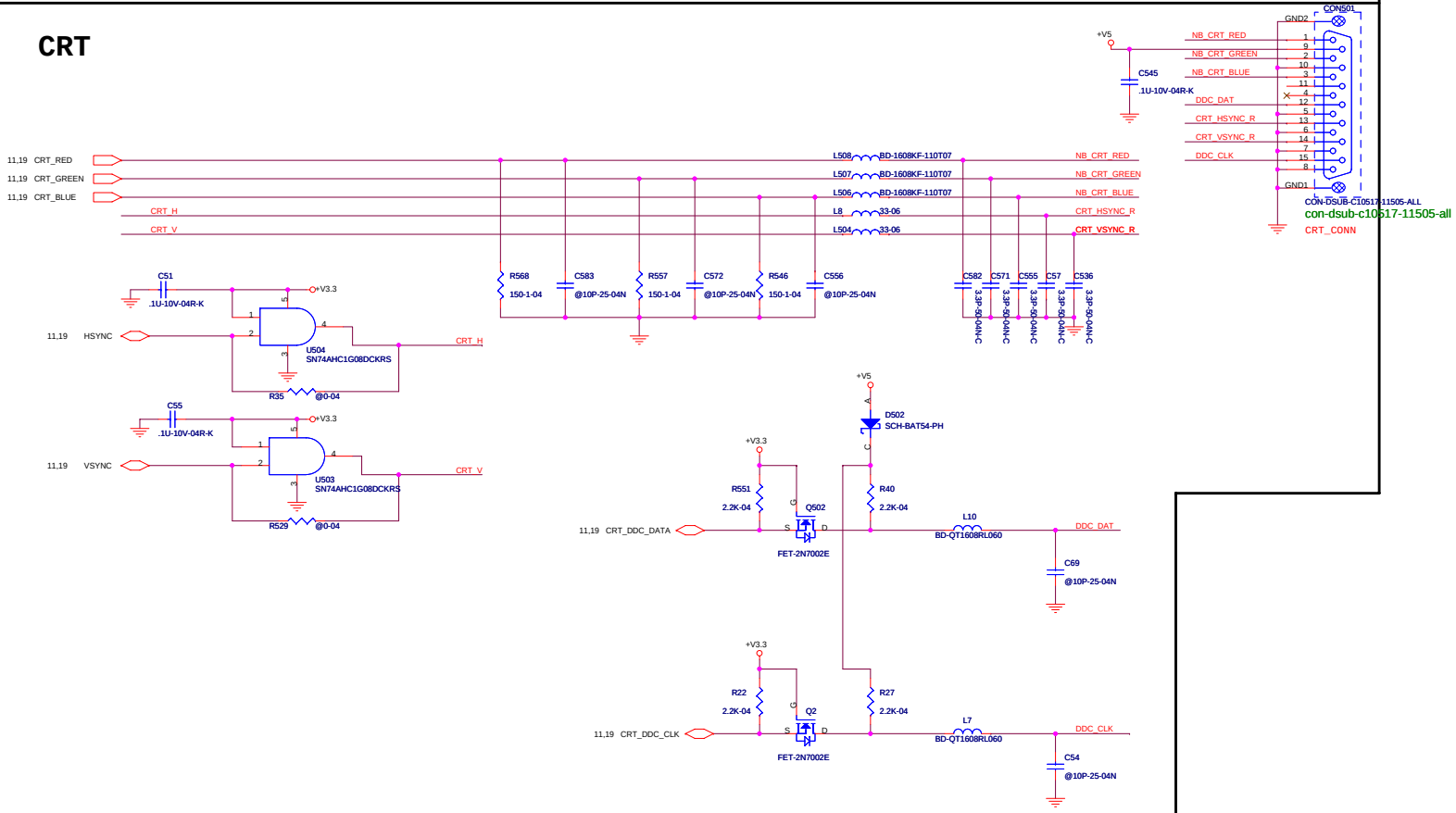
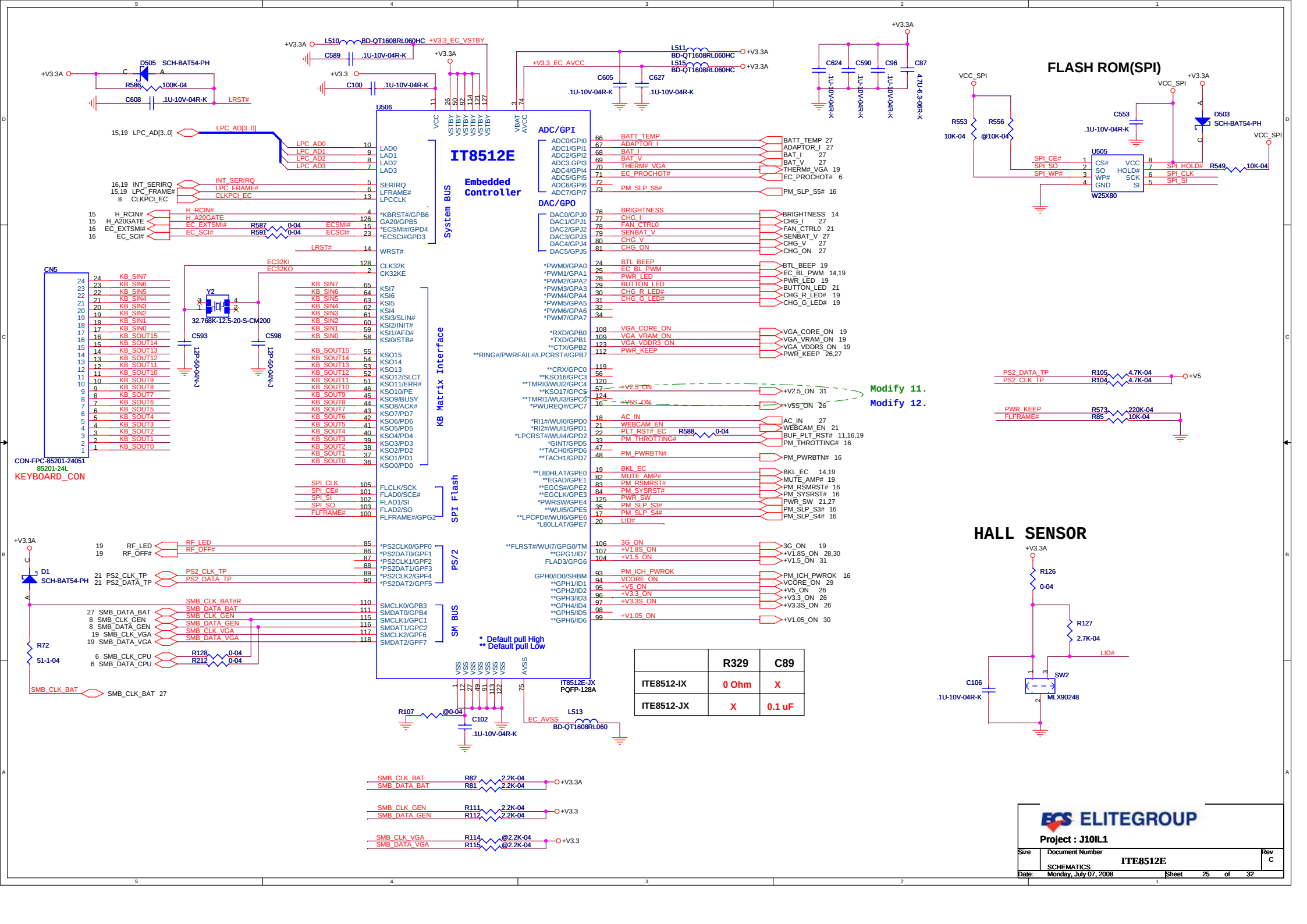
CRT



ECS ELITEGROUP		
Project : J10IL1		
Size	Document Number: CRT	Rev: C
	SCHEMATICS	
Date: Monday, July 07, 2008	Sheet 24 of 32	


IT8512E
Embedded Controller
U506
System BUS
KB Matrix Interface
SPI Flash
PS/2
SM BUS
ADC/GPI
DAC/GPO
* Default pull High
** Default pull Low
IT8512E-JX
PQFP-128A
FLASH ROM(SPI)
W25X80
HALL SENSOR
KEYBOARD_CON
CON-FPC-85201-24051
85201-24L
Modify 11.
Modify 12.
ITE8512-IX | R329 0 Ohm | C89 X
ITE8512-JX | R329 X | C89 0.1 uF
Project : J10IL1
ELITEGROUP
Size: Document Number: ITE8512E
Rev: C
SCHEMATICS
Date: Monday, July 07, 2008
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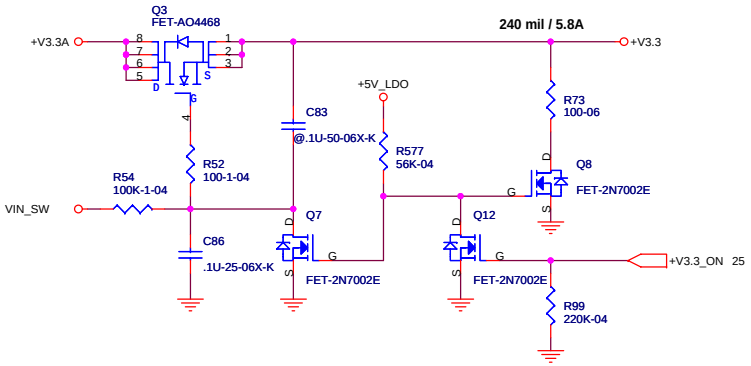

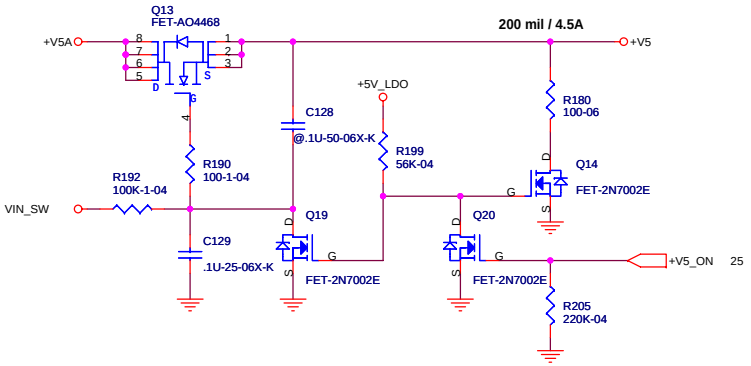

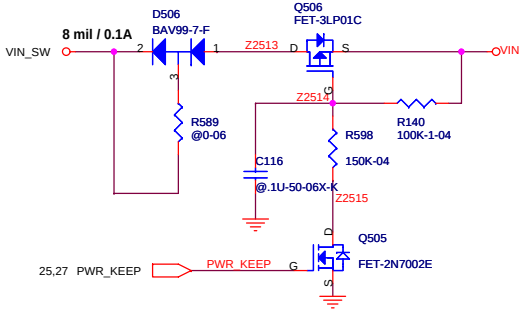

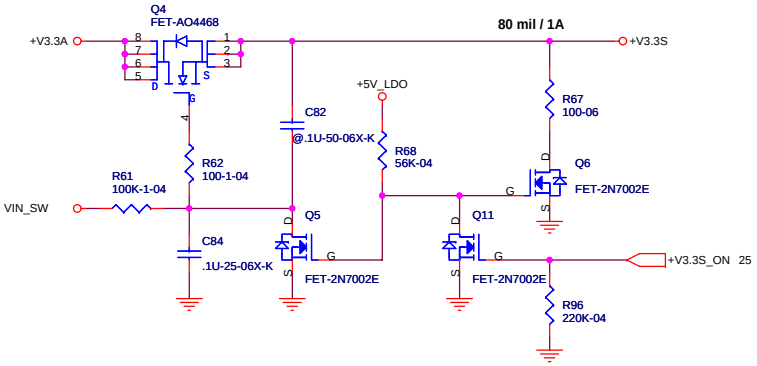

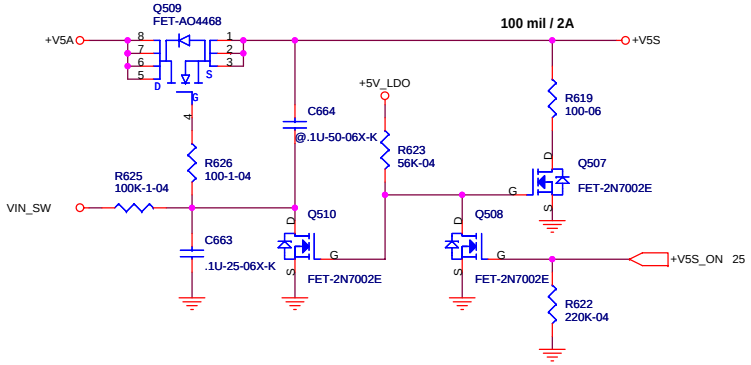

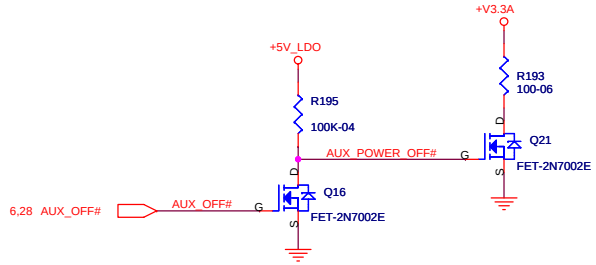

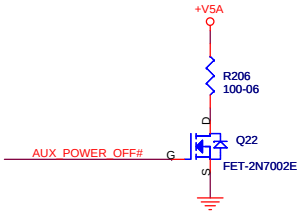

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	POWER SWITCH	C
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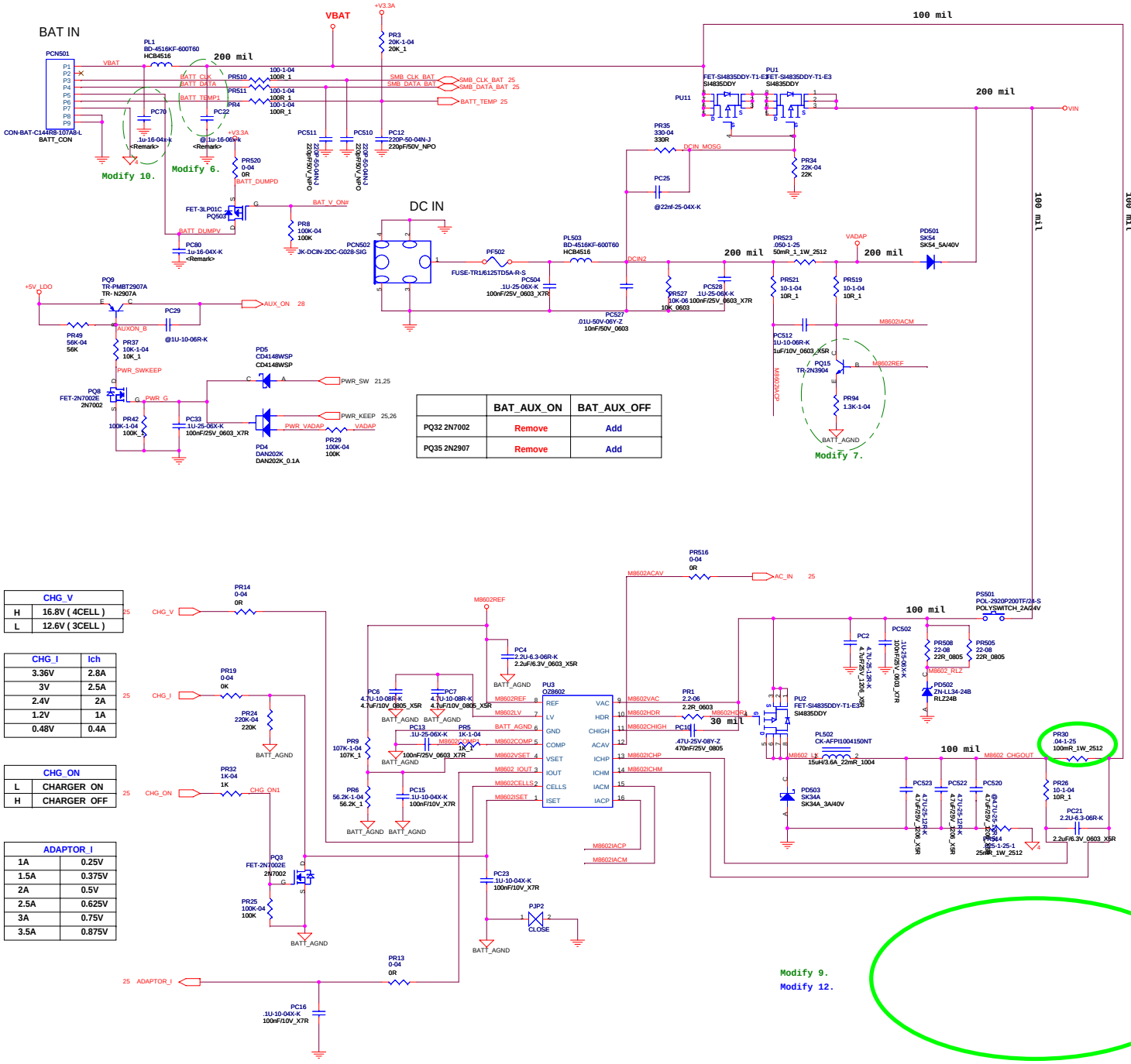


	BAT_AUX_ON	BAT_AUX_OFF
PQ32 2N7002	Remove	Add
PQ35 2N2907	Remove	Add

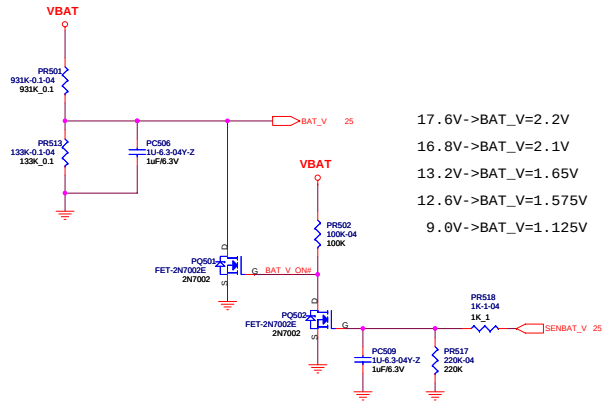
CHG_V	
H	16.8V (4CELL)
L	12.6V (3CELL)

CHG_I	Ich
3.36V	2.8A
3V	2.5A
2.4V	2A
1.2V	1A
0.48V	0.4A

CHG_ON	
L	CHARGER ON
H	CHARGER OFF

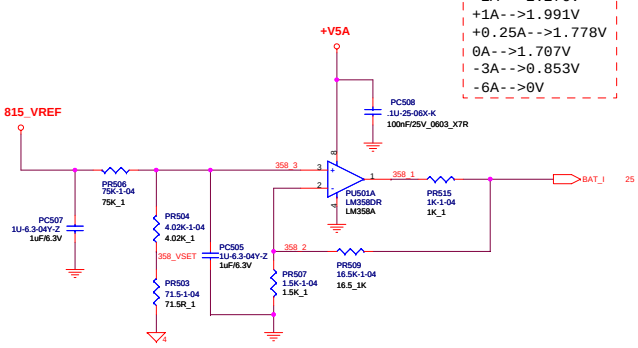
ADAPTOR_I	
1A	0.25V
1.5A	0.375V
2A	0.5V
2.5A	0.625V
3A	0.75V
3.5A	0.875V

Battery Voltage Detect



17.6V->BAT_V=2.2V
16.8V->BAT_V=2.1V
13.2V->BAT_V=1.65V
12.6V->BAT_V=1.575V
9.0V->BAT_V=1.125V

Charge / Discharge Detect



+3A-->2.56V
+2A-->2.276V
+1A-->1.991V
+0.25A-->1.778V
0A-->1.707V
-3A-->0.853V
-6A-->0V

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	DC IN/BATT IN/Charger	C
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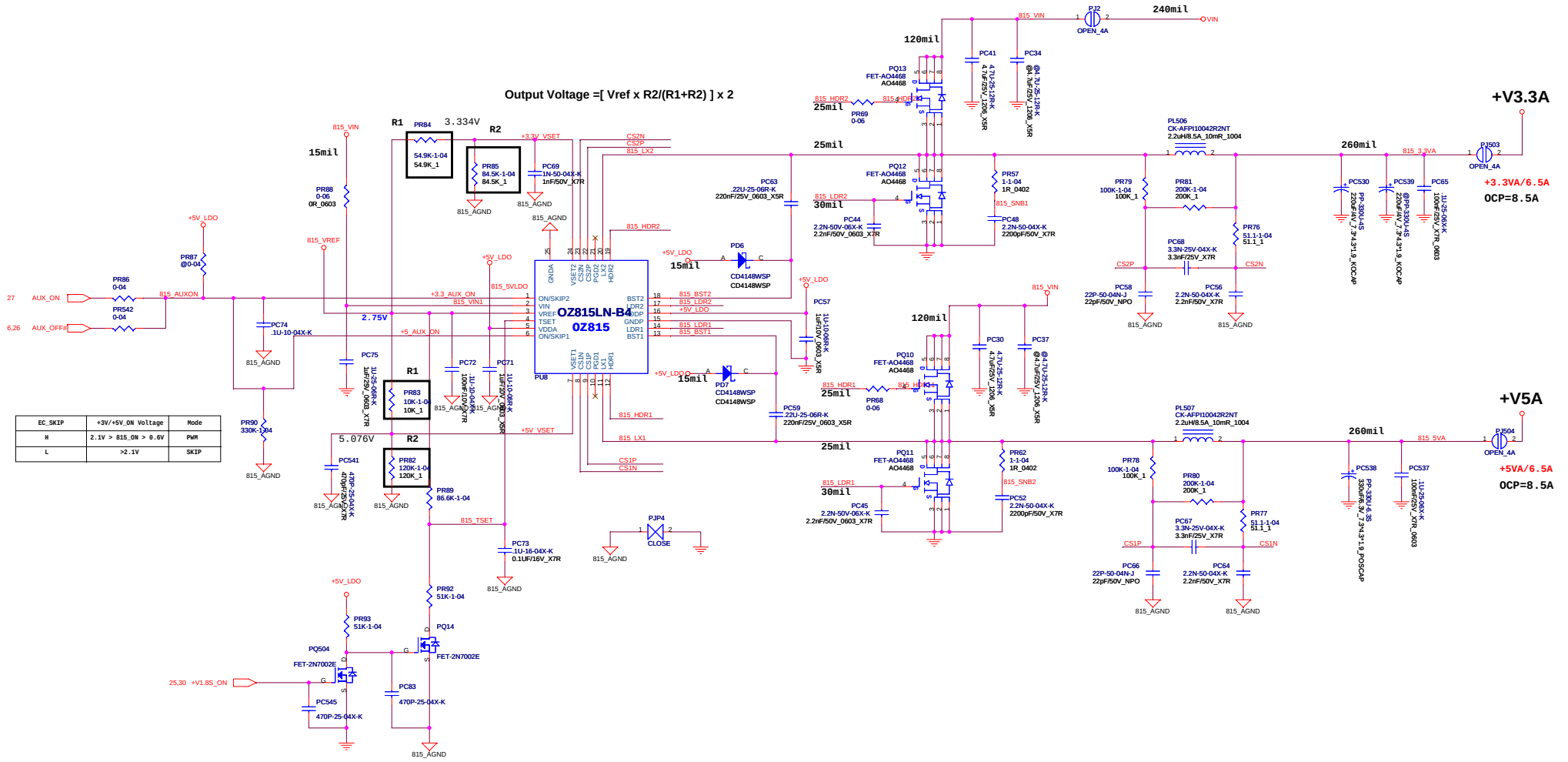
Output Voltage =[Vref x R2/(R1+R2)] x 2
+V3.3A
+3.3VA/6.5A
OCP=8.5A
+V5A
+5VA/6.5A
OCP=8.5A
OZ815LN-B4
OZ815
PU8
EC_SKIP | +3V/+5V_ON Voltage | Mode
H | 2.1V > 815_ON > 0.6V | PWM
L | >2.1V | SKIP
Project : J10IL1
+V3.3A/+V5A(OZ815)
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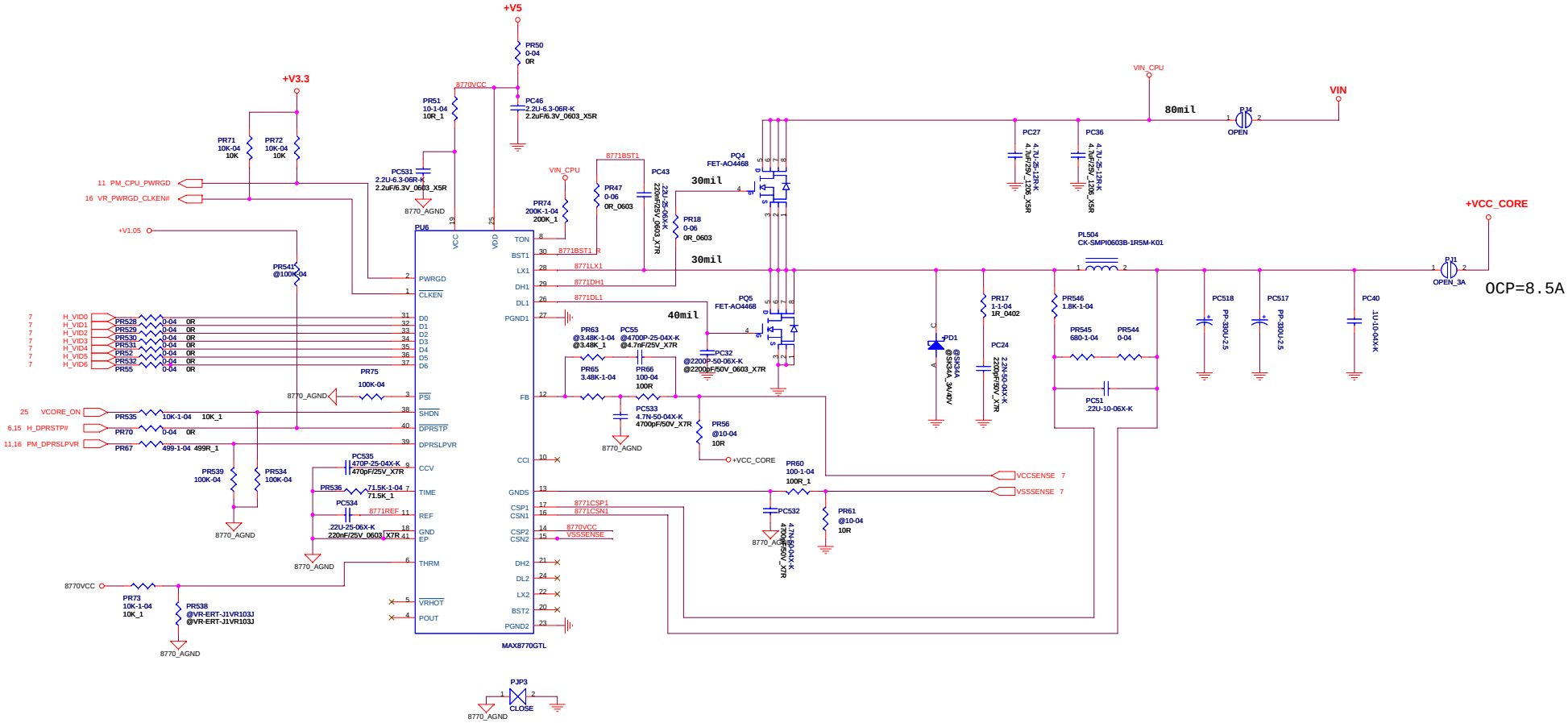

ECS COMPUTER CORP.	
Title	CPU_CORE (MAX8770)
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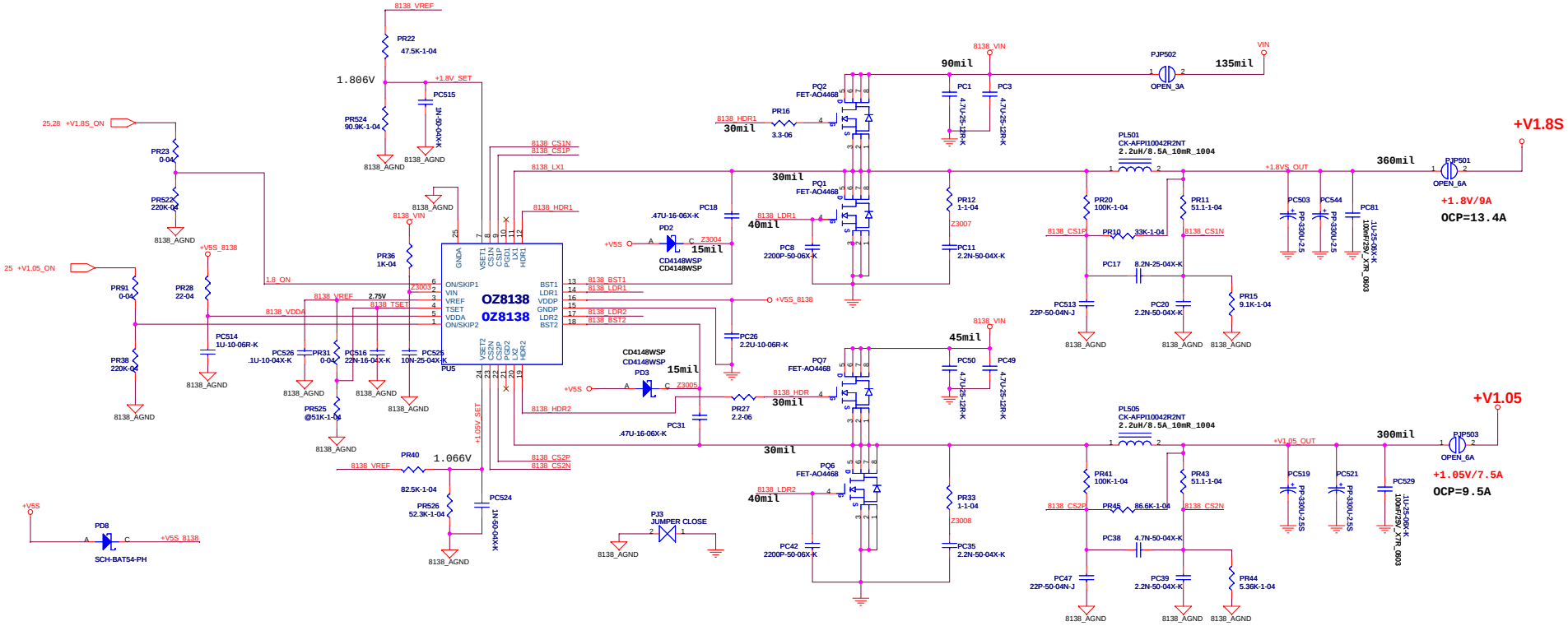

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	+V1.8S/+V1.05 (OZ8138)	C
	SCHEMATICS	

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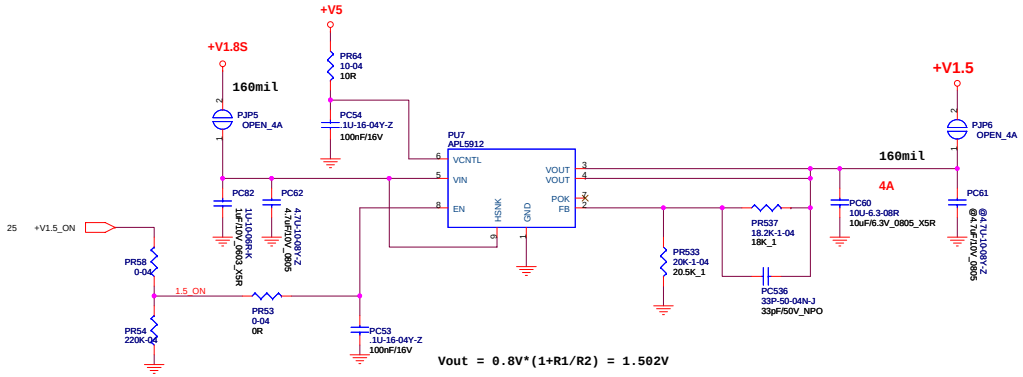

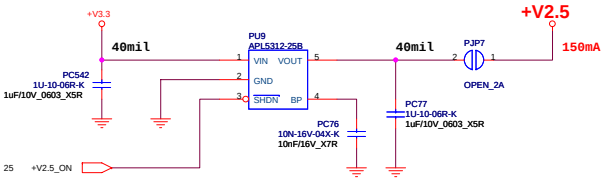

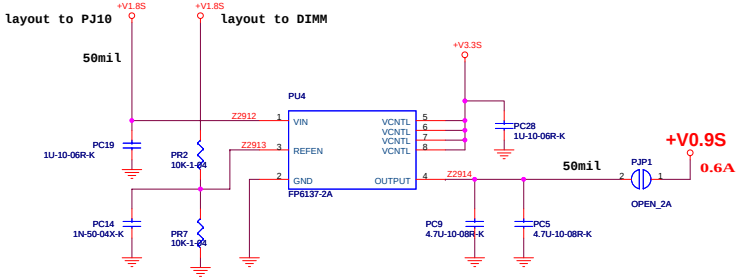

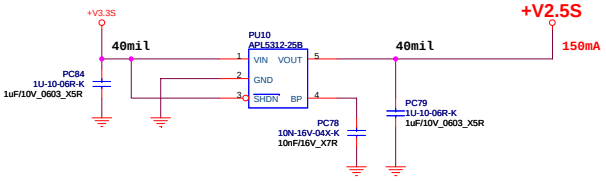

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	+V1.5/+V0.9S/+V2.5	C
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J10IL1 C-Phase Change Notes :

20080626 modify item :
Page 22 modify list :
1. Del R611,R612,R613,R614 location -> EMI don't need choke colay circuit
Page 6 modify list :
2. U4 value change to ''ATOM-SLB73'' with P/N ''01G0175K0-10'' -> C-phase request
Page 9 modify list :
3. U5 value change to ''QG92945GSE'' with P/N ''02G929450-10'' -> C-phase request
Page 15 modify list :
4. U9 value change to ''ICH7M-SL8YB-B0'' with P/N ''02G700000-G0'' -> C-phase request

20080630 modify item :
Page 22 modify list :
5. Change H6 location name to H501 -> the stand-off need on bottom side

20080702 power modify item :
Page 27 modify list :
6. remove pc22 ->for EMI solution
7. add PQ15 TR-2N3904 PR94 1.3K-1-04 ->for apc circuit

20080702 modify item :
Page 21 modify list :
8. Modify net BOTTON_LED# to BUTTON_LED# with LED1,LED2 pin C -> net name error

20080704 power modify item :
Page 27 modify list :
9. add @pq514,@pr21,@pq505,@pr39 ->battery can't pre-charge 100ma circuit
10. change pc70 to .1u-16-04x-k & add pc22 change to reserve ->EMI solution

20080704 modify item :
Page 25 modify list :
11.U506 pin 124 connect to PRE_CHARGE -> pre-charge circuit

20080707 modify item :
Page 25 & Page 27 modify list :
12.Del modify 9 , modify 11 -> layout not enough space

Power modify item :

2008???? power modify item :
Page ?? modify list :
1.

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