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MS-7512 ATX Version: 1.1

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Eaglelake - G/P (G, P3North Bridge)
Intel ICH9/10 (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS113
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111C (PCIE)
HD Audio Codec -- RTL888/888T
1394 Controller -- JMB381
PCIE to PATA/SATA Bridge -- JMB-363 e-SATA X2/ IDE X1
PCIE to PATA/SATA Bridge -- Marvell 88SE6111 SATA X1

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1 ─┐ Alternative
PCI EXPRESS X8 SLOT *1 ─┘
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 2

PWM: ISL6336+Dr.Mos

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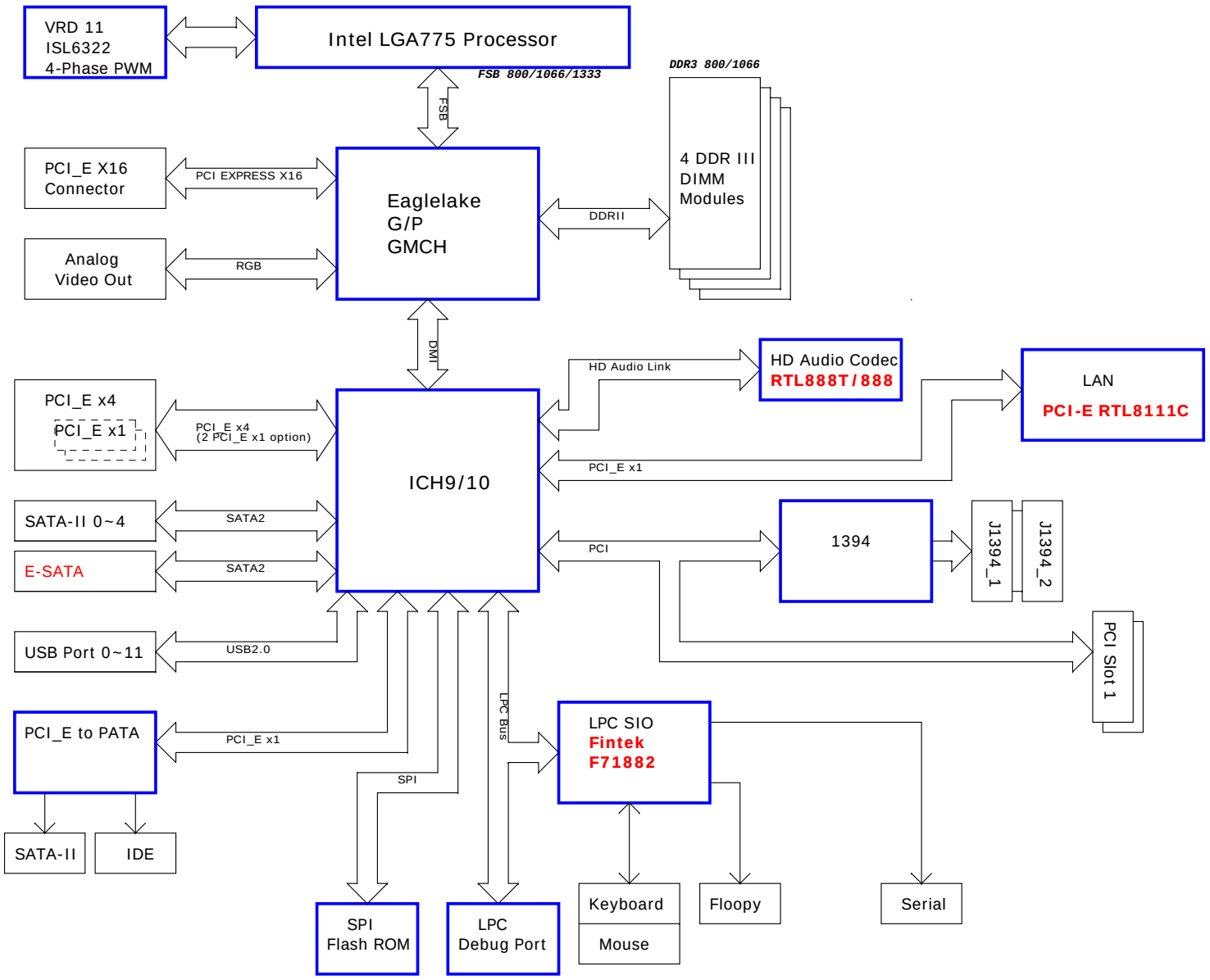
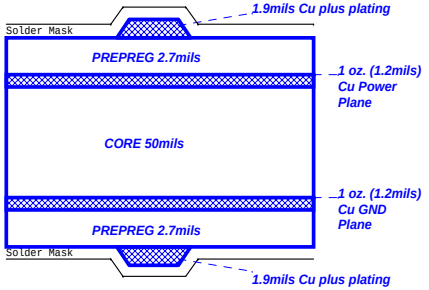
Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7512	
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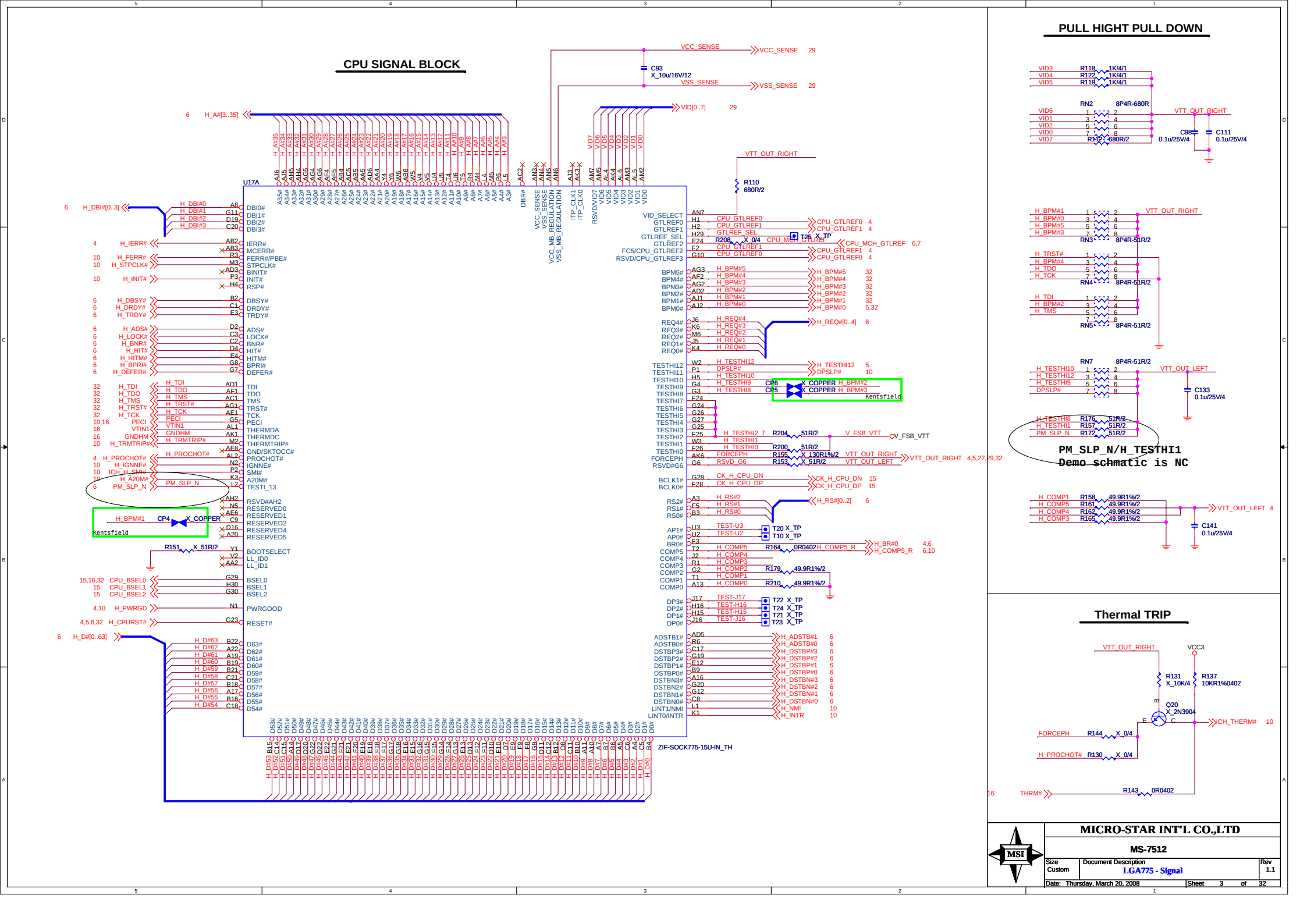
CPU SIGNAL BLOCK
U17A
ZIF-SOCK775-15U-IN_TH
PULL HIGHT PULL DOWN
PM_SLP_N/H_TESTHI1
Demo schmatic is NC
Thermal TRIP
MICRO-STAR INT'L CO.,LTD
MS-7512
LGA775 - Signal
Date: Thursday, March 20, 2008
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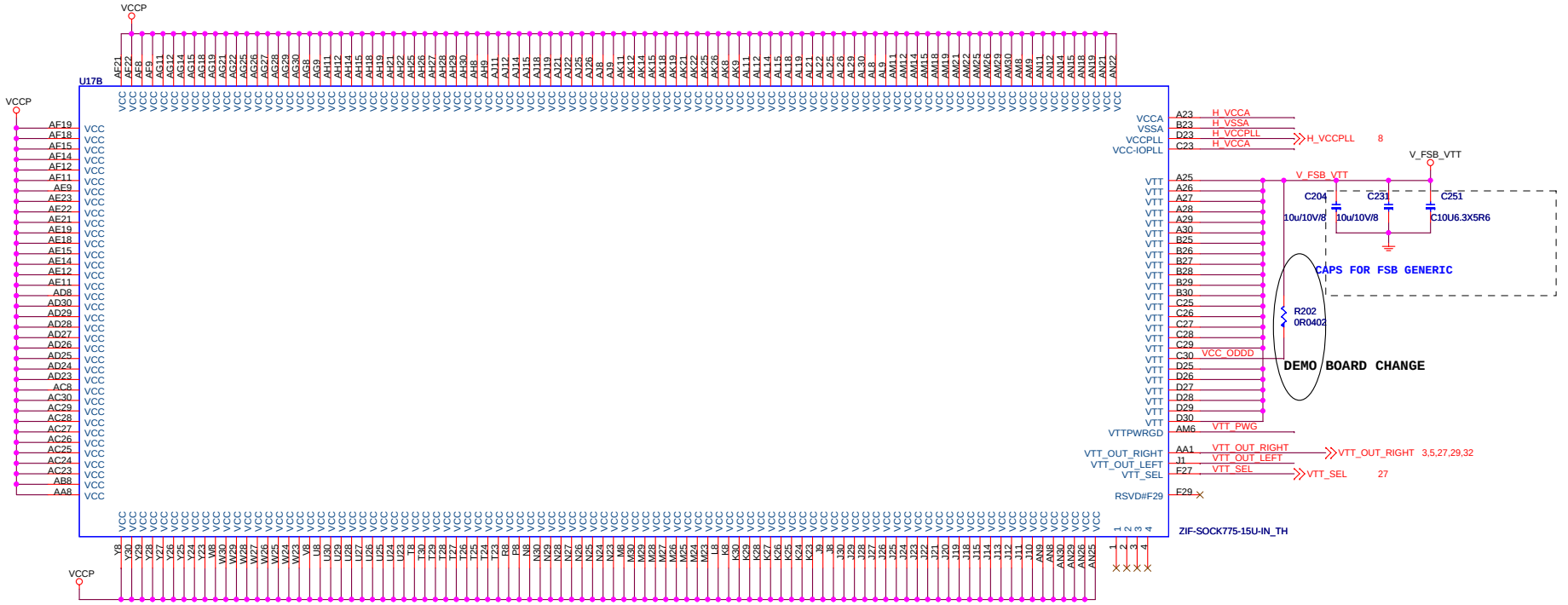
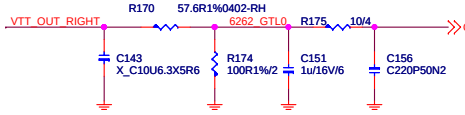
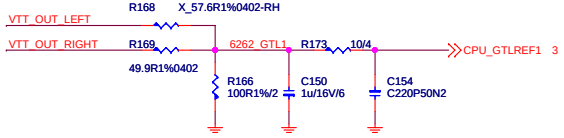


*GTLREF VOLTAGE SHOULD BE
0.635 * VTT = 0.735V (At VTT=1.2V)
0.635 * VTT = 0.7V (At VTT=1.1V)

UPI VOLTAGE CONSOLE

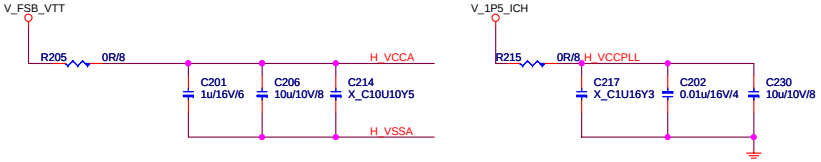


UPI VOLTAGE CONSOLE

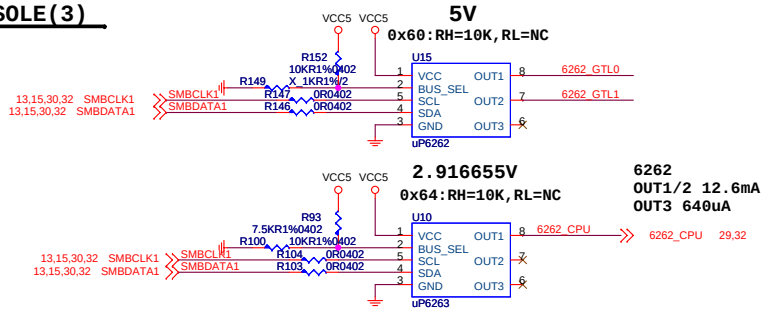


DEMO BOARD CHANGE
(GTLREF0+3/GTLREF1+2)

*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



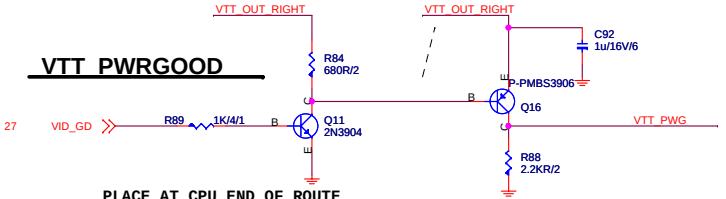
UPI VOLTAGE CONSOLE(3)



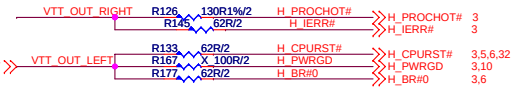
6262
OUT1/2 12.6mA
OUT3 640uA

VTT_PWRGOOD

1.2V VTT_PWRGOOD



PLACE AT CPU END OF ROUTE



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

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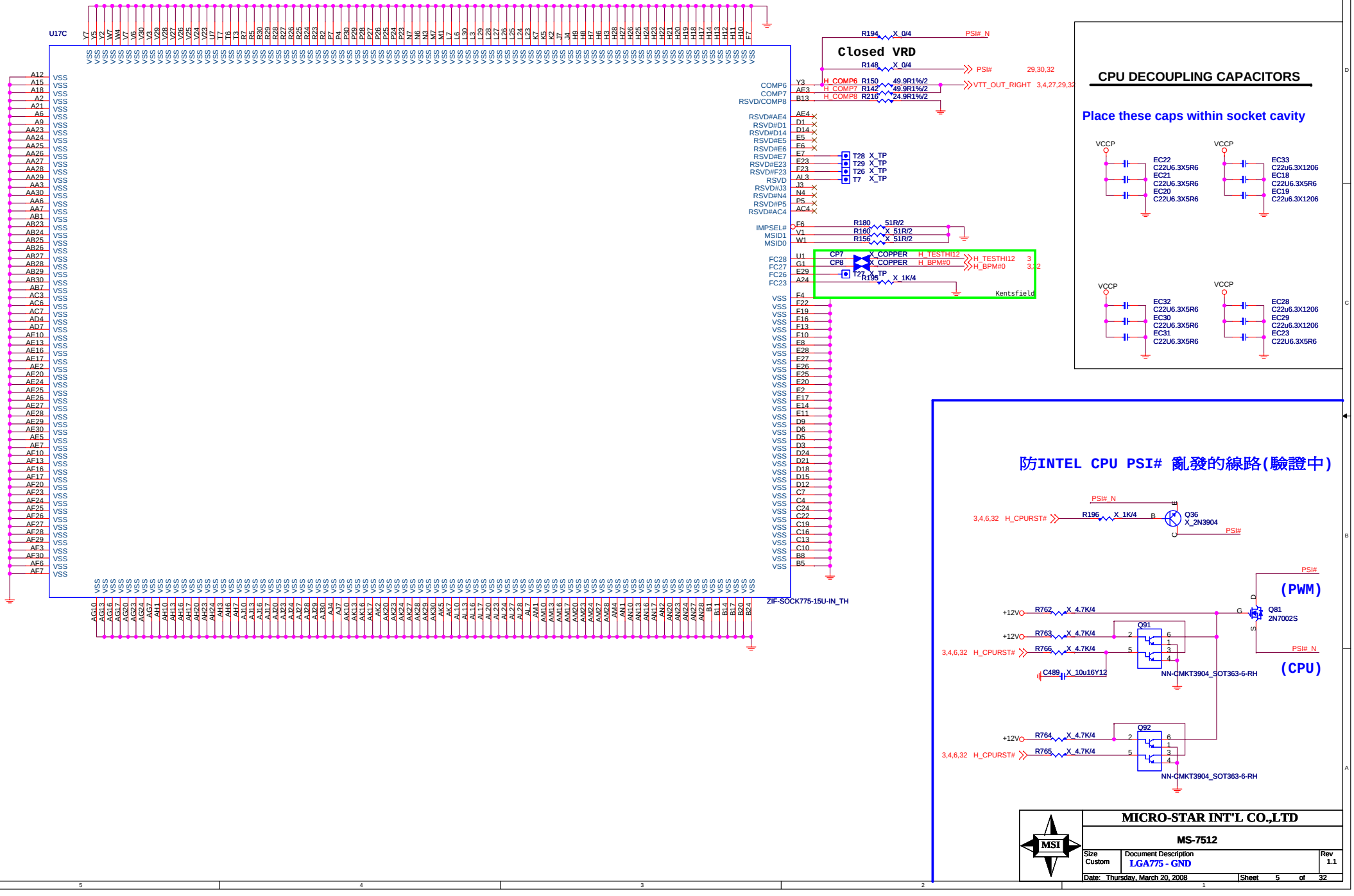

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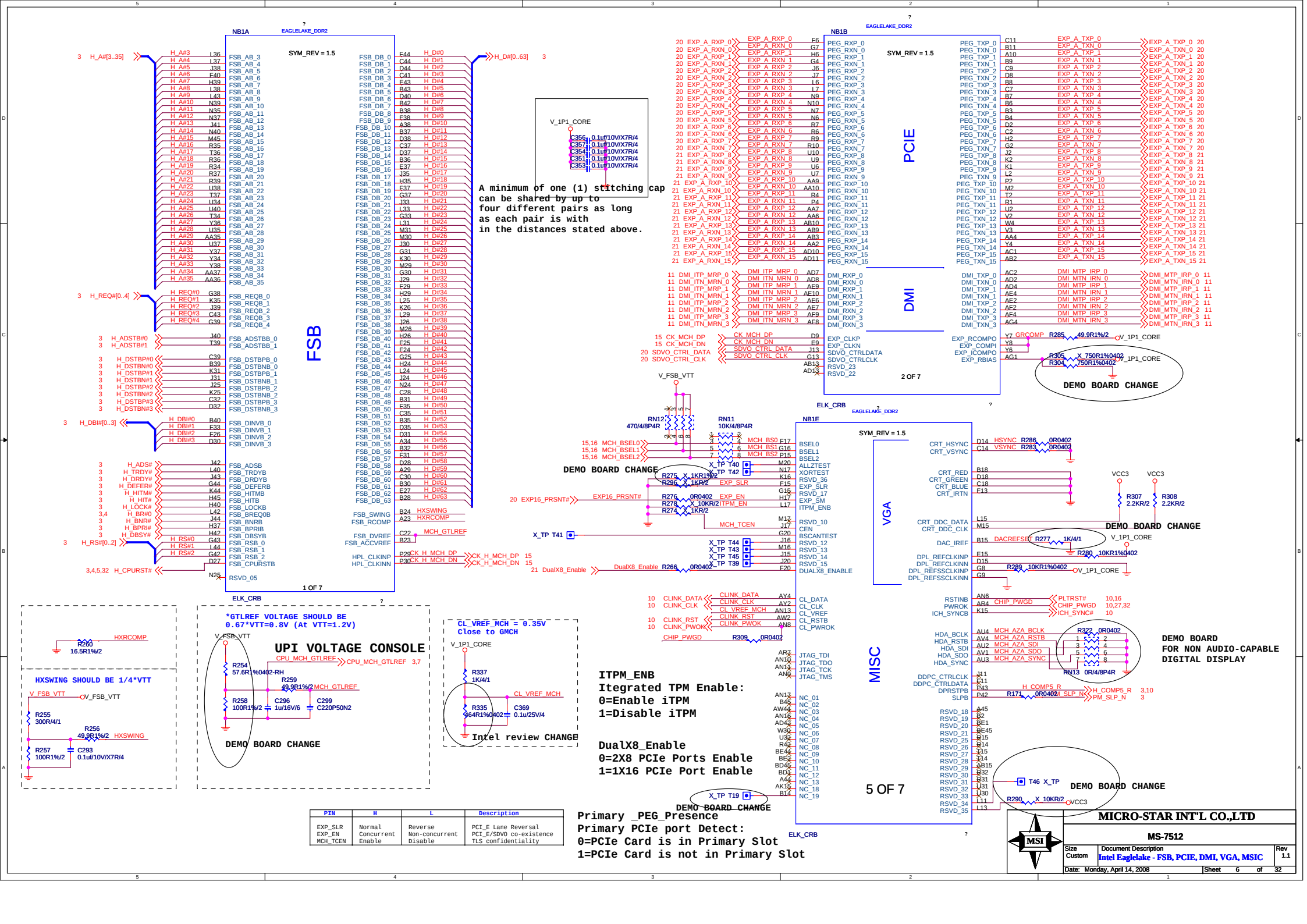
MS-7512		
Size: Custom	Document Description: LGA775 - GND	Rev: 1.1
Date: Thursday, March 20, 2008	Sheet 5 of 32	



PIN	H	L	Description
EXP_SLR EXP_EN MCH_TCEN	Normal Concurrent Enable	Reverse Non-concurrent Disable	PCI_E Lane Reversal PCI_E/SDVO co-existence TLS confidentiality

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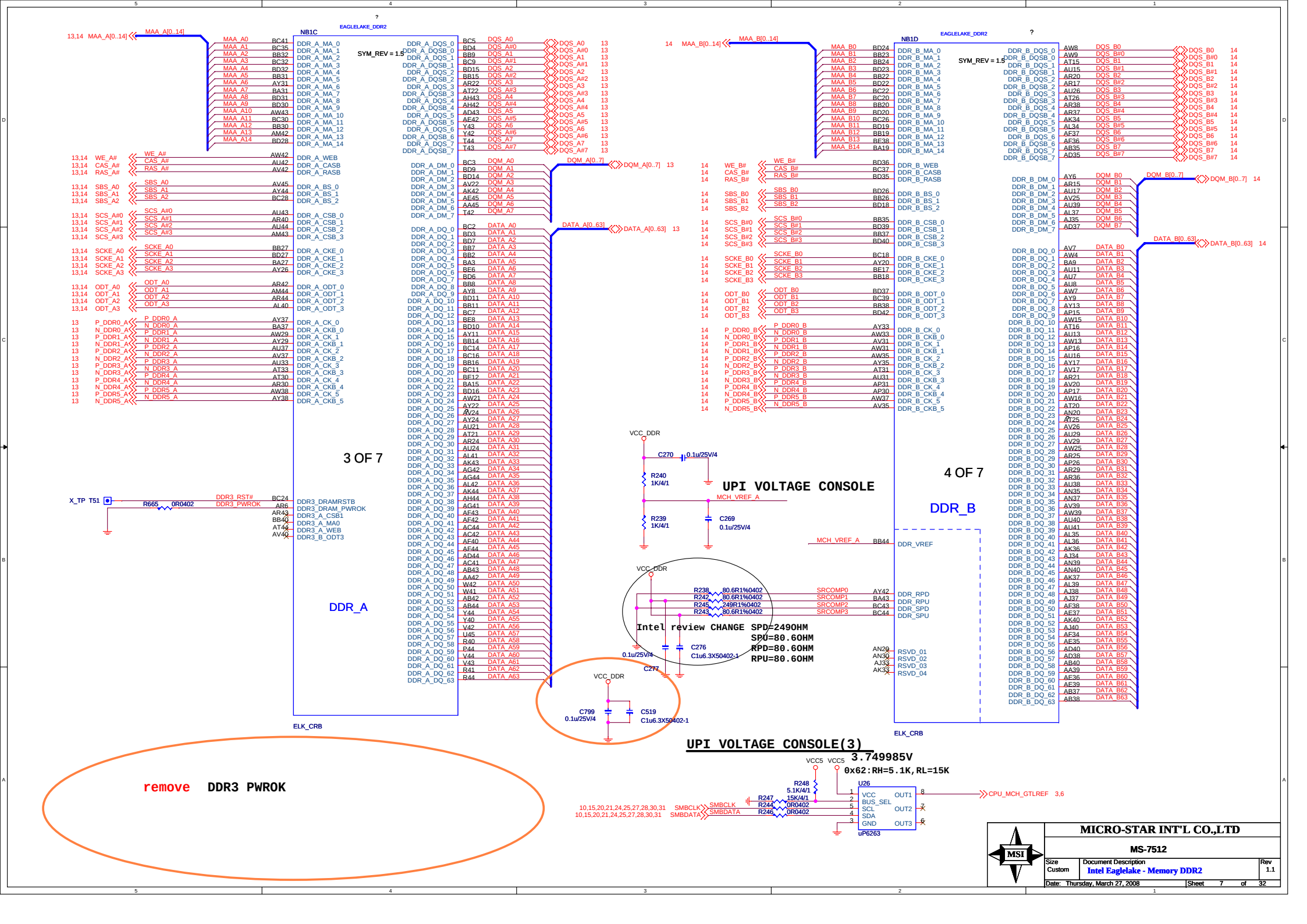
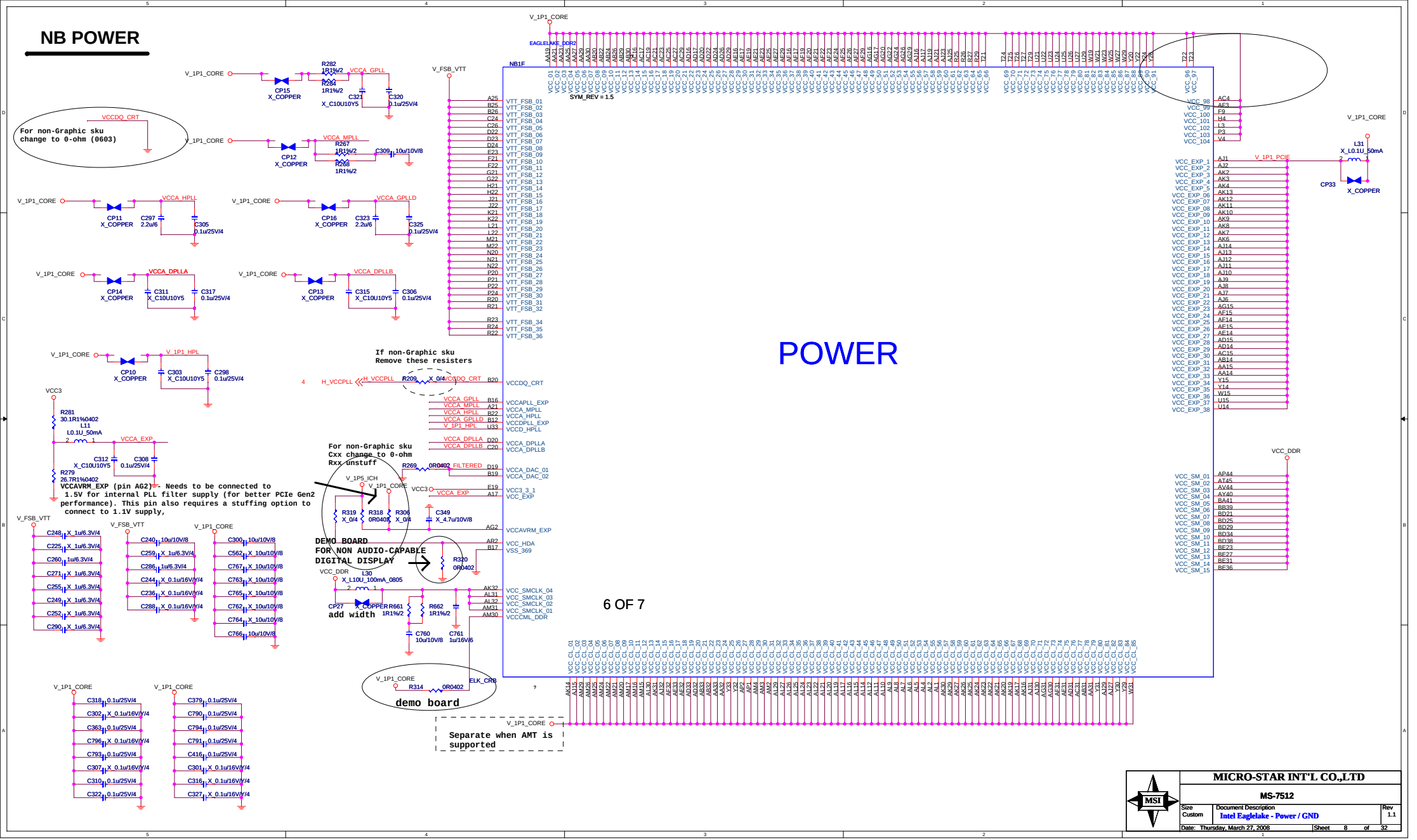
MS-7512

Size	Document Description	Rev
Custom	Intel Eaglelake - FSB, PCIE, DMI, VGA, MSIC	1.1
Date: Monday, April 14, 2008	Sheet 6 of 32	


NB1C
EAGLELAKE_DDR2
SYM_REV = 1.5
3 OF 7
DDR_A
ELK_CRB
NB1D
4 OF 7
DDR_B
UPI VOLTAGE CONSOLE
Intel review CHANGE SPD=249OHM
SPU=80.6OHM
RPD=80.6OHM
RPU=80.6OHM
UPI VOLTAGE CONSOLE(3)
3.749985V
0x62:RH=5.1K,RL=15K
uP6263
remove DDR3 PWROK
MICRO-STAR INT'L CO.,LTD
MS-7512
Intel Eaglelake - Memory DDR2
Thursday, March 27, 2008

NB POWER



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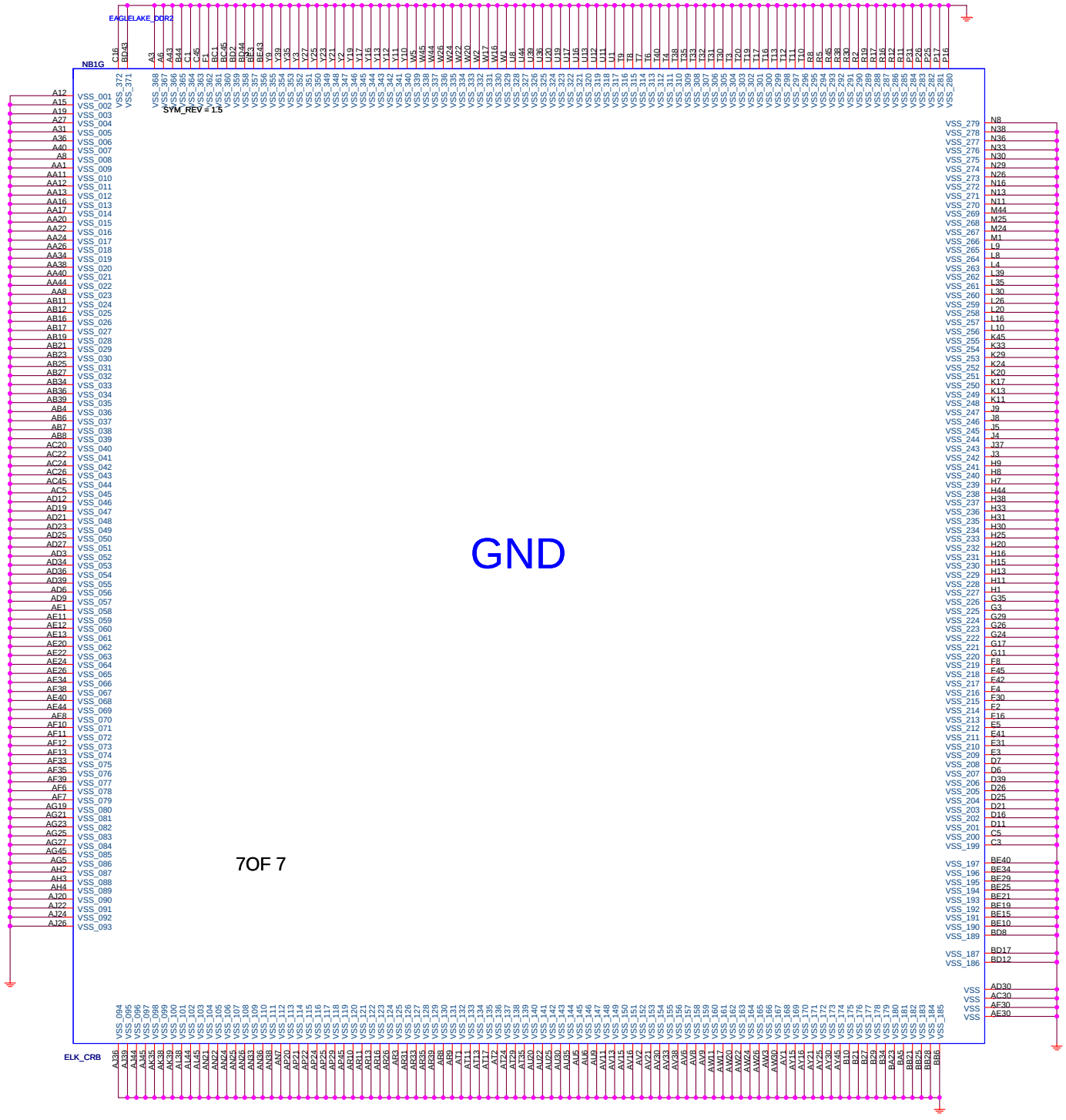
Size	Document Description	Rev
Custom	Intel Eaglelake - Power / GND	1.1

Date: Thursday, March 27, 2008 Sheet 8 of 32



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: EagleLake-GND
Rev: 1.1	
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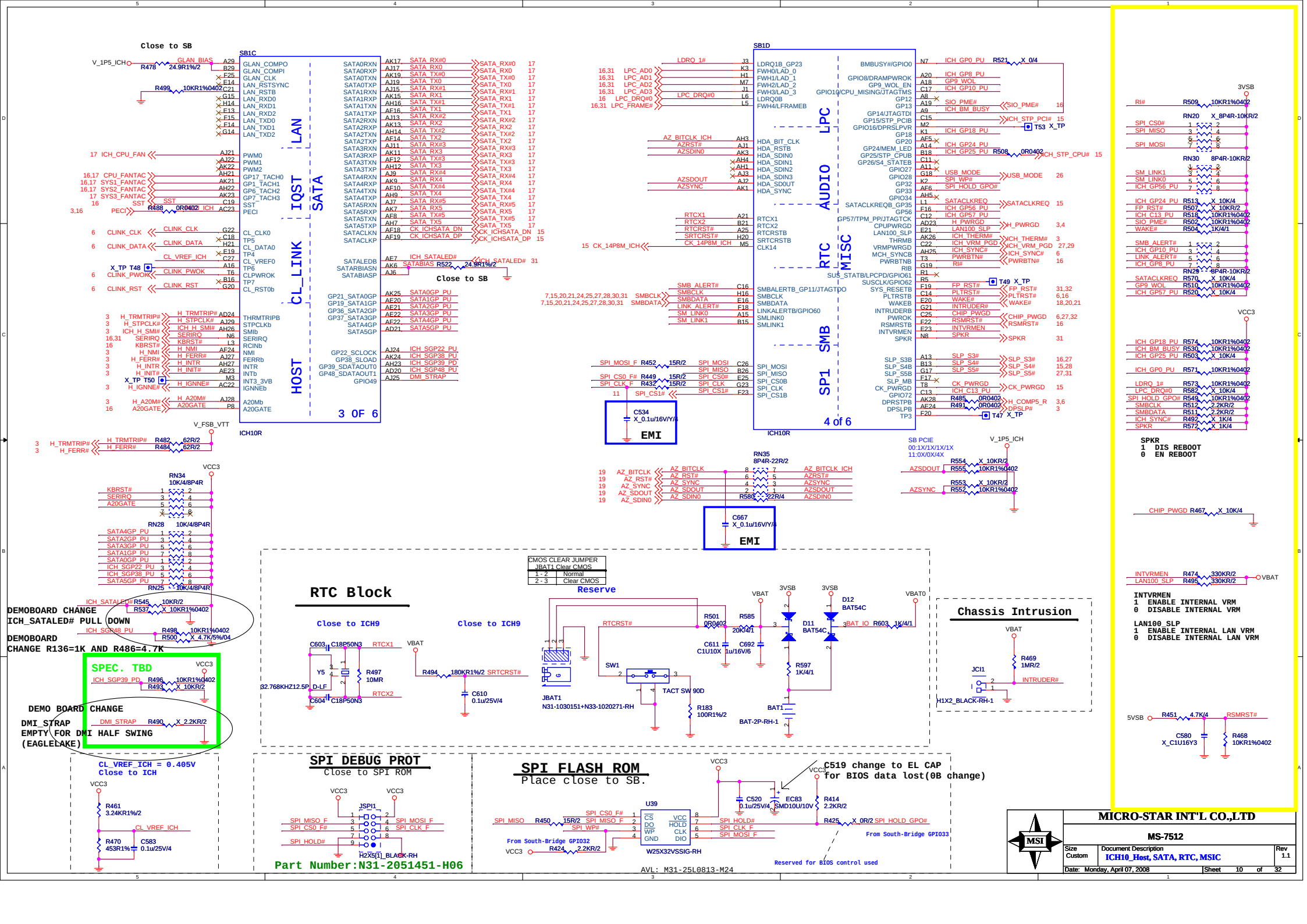
Close to SB
SB1C
LAN
IQST
SATA
CL_LINK
HOST
3 OF 6
ICH10R
SB1D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
EMI
RTC Block
Close to ICH9
Reserve
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
Chassis Intrusion
DEMOBOARD CHANGE
ICH_SATALED# PULL DOWN
DEMOBOARD
CHANGE R136=1K AND R486=4.7K
SPEC. TBD
DEMO BOARD CHANGE
DMI_STRAP
EMPTY FOR DMI HALF SWING
(EAGLELAKE)
CL_VREF_ICH = 0.405V
Close to ICH
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
SPI FLASH ROM
Place close to SB.
C519 change to EL CAP
for BIOS data lost(0B change)
From South-Bridge GPIO32
From South-Bridge GPIO33
Reserved for BIOS control used
AVL: M31-25L0813-M24
SPKR
1 DIS REBOOT
0 EN REBOOT
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
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MS-7512
ICH10_Host, SATA, RTC, MSIC
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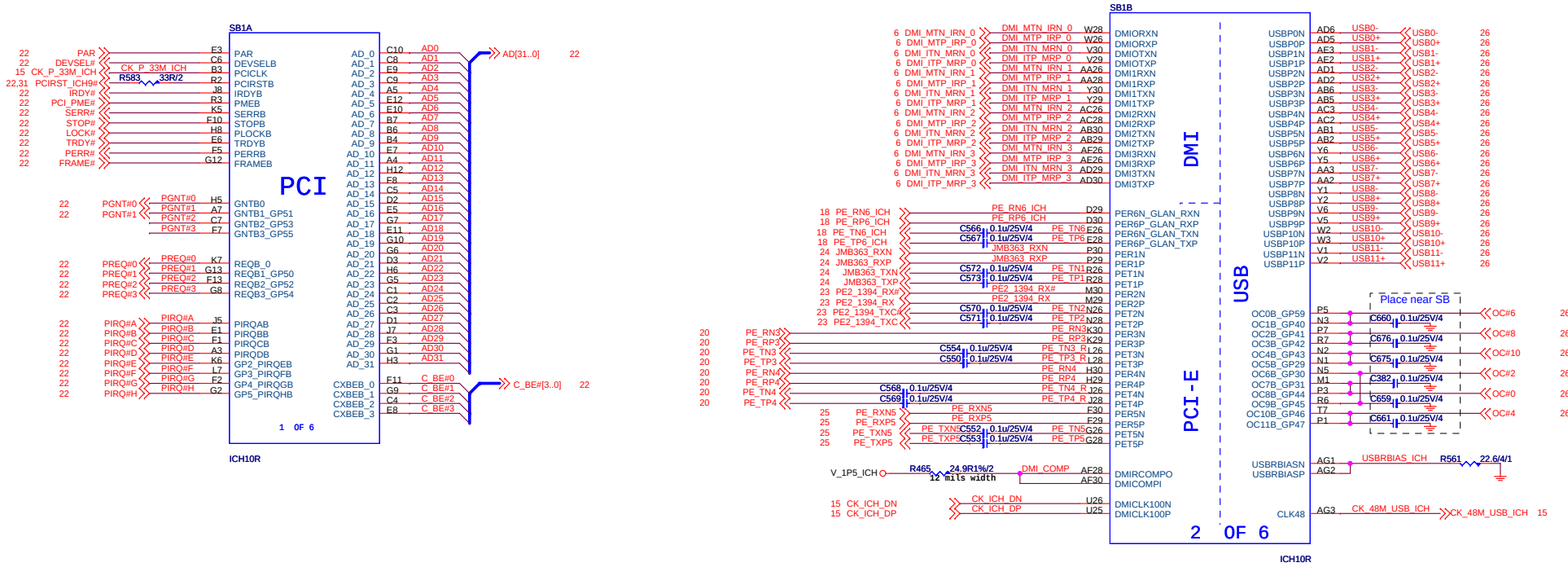
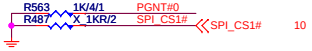
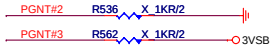


SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

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Size: Custom	Document Description: ICH10_PCI, USB, DMI, PCIEx1	Rev: 1.1
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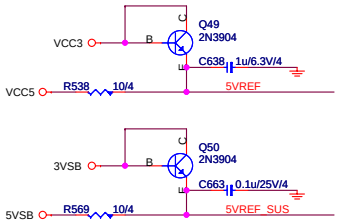
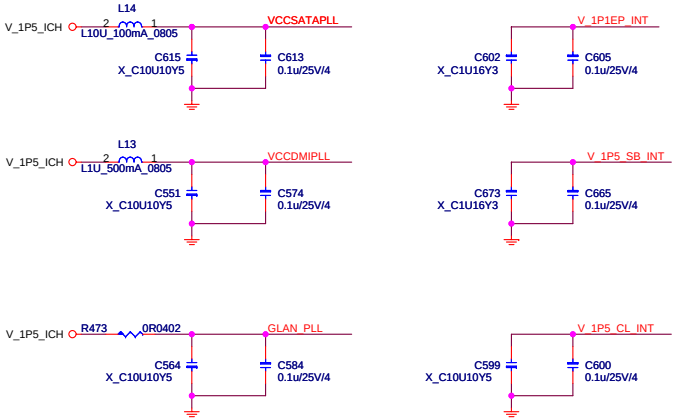
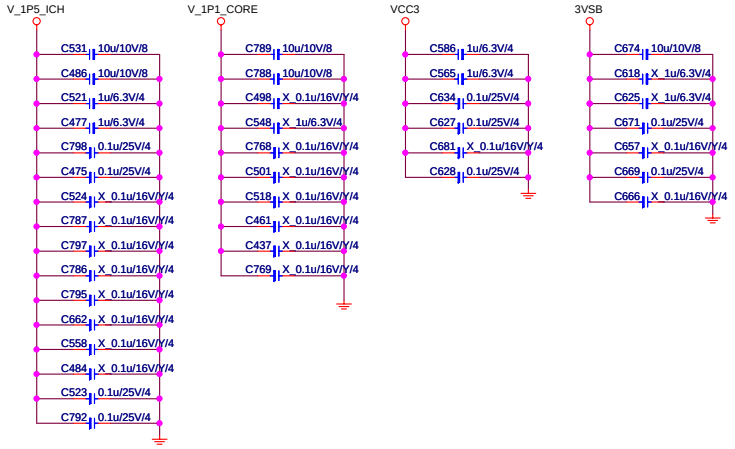
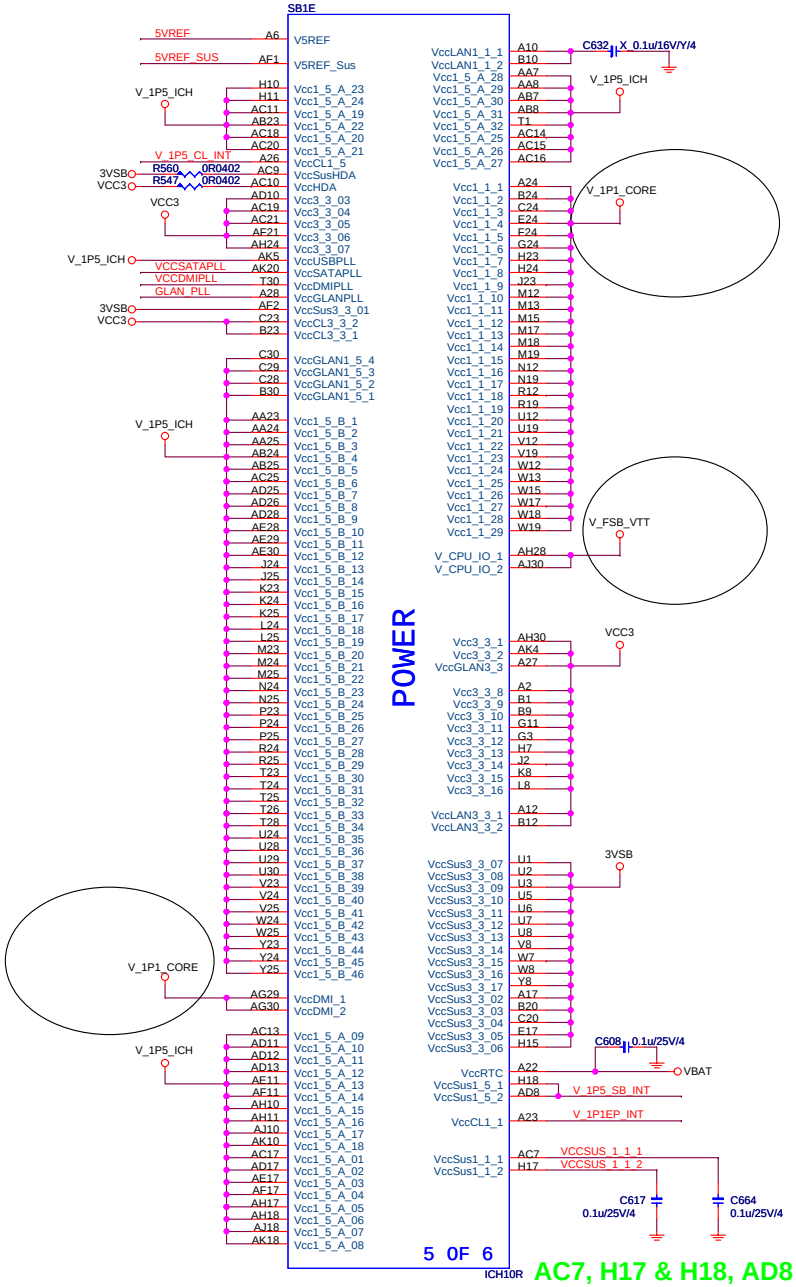
5VREF & 5VREF_SUS Sequencing Circuit

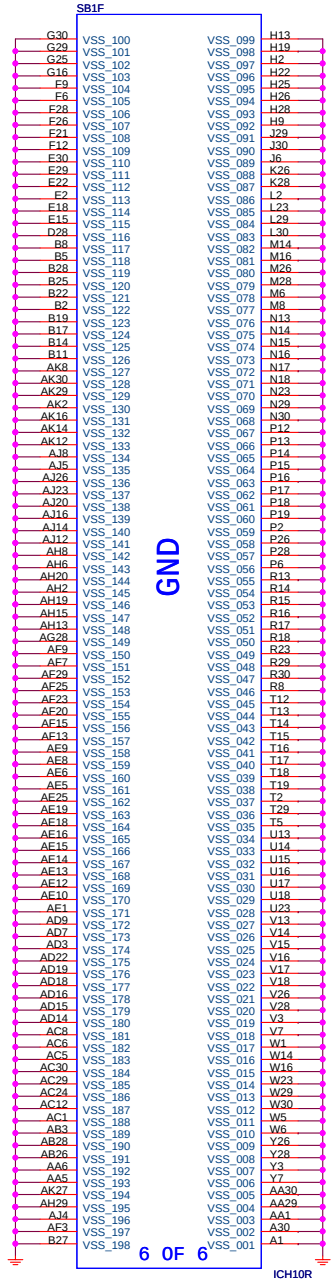


SB POWER









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Size: Custom	Document Description: ICH9/10 - Power, GND
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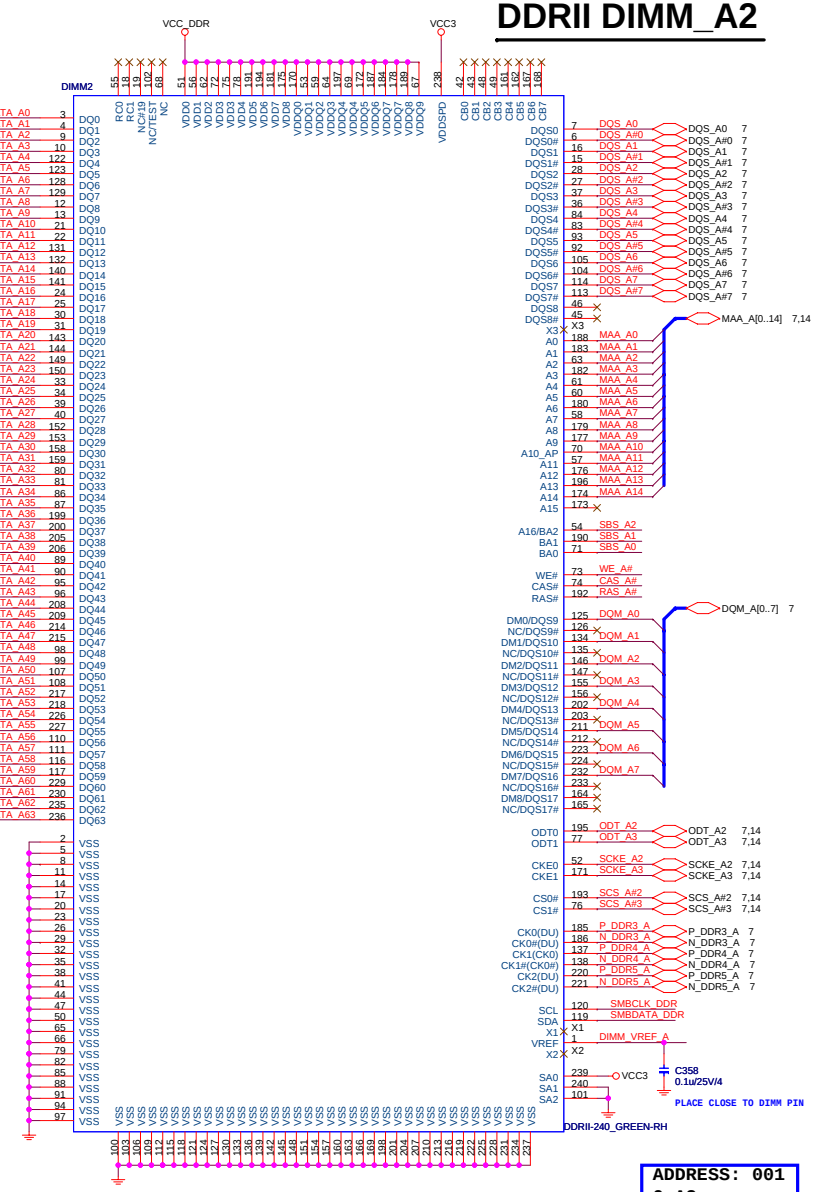
DDRII DIMM_A1

ADDRESS: 000
0xA0

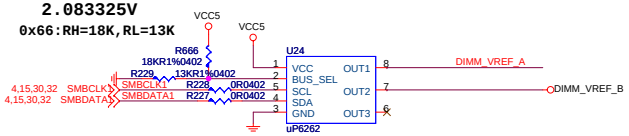
DDRII DIMM_A2

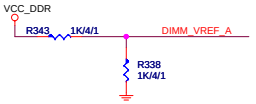


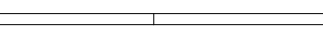
ADDRESS: 001
0xA2

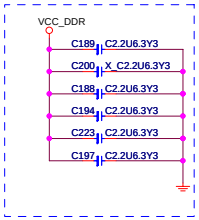
UPI VOLTAGE CONSOLE(3+1)

2.083325V
0x66:RH=18K,RL=13K









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Size: Custom	Document Description: DDR2 Chanel-A / Chanel-B	Rev: 1.1
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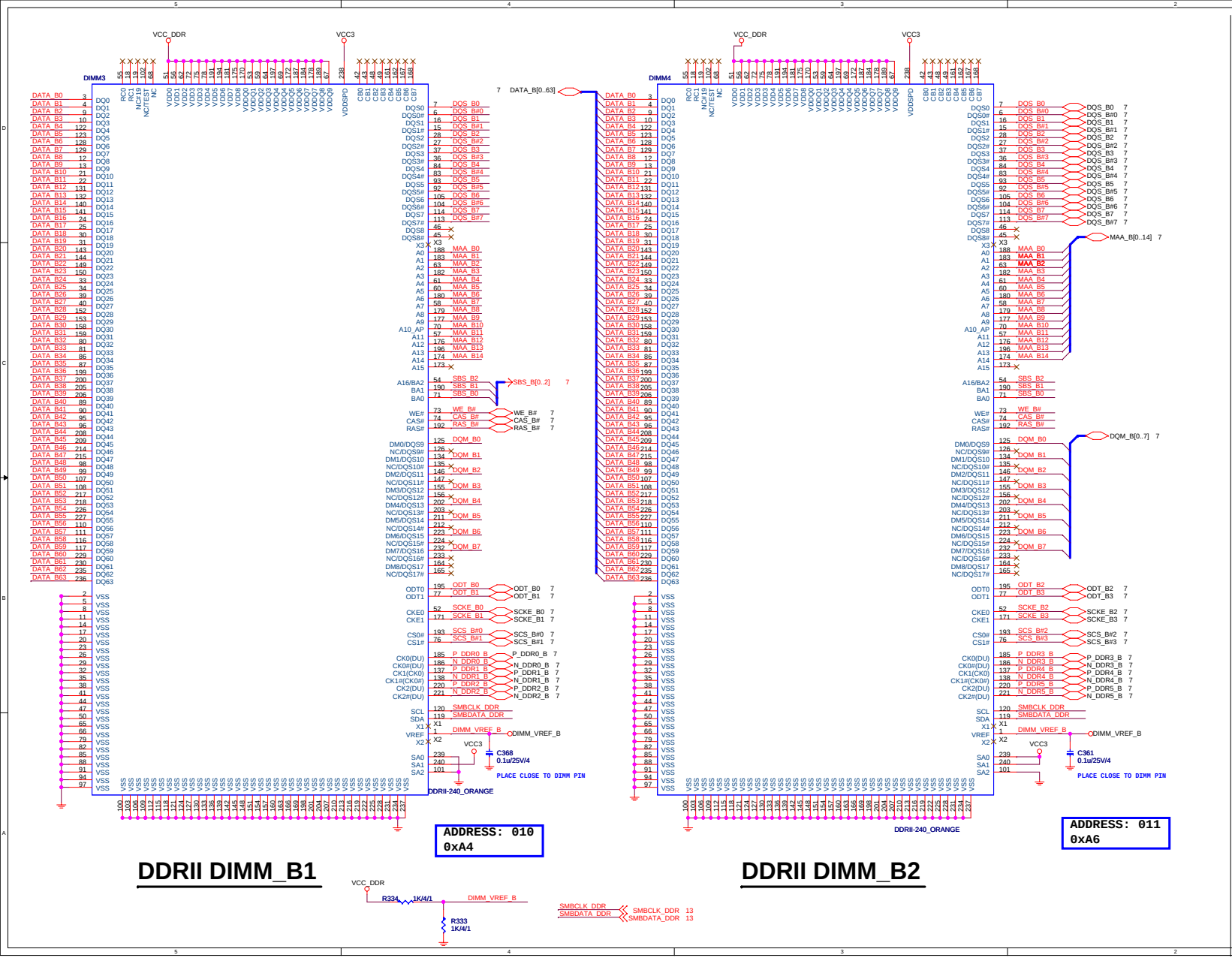
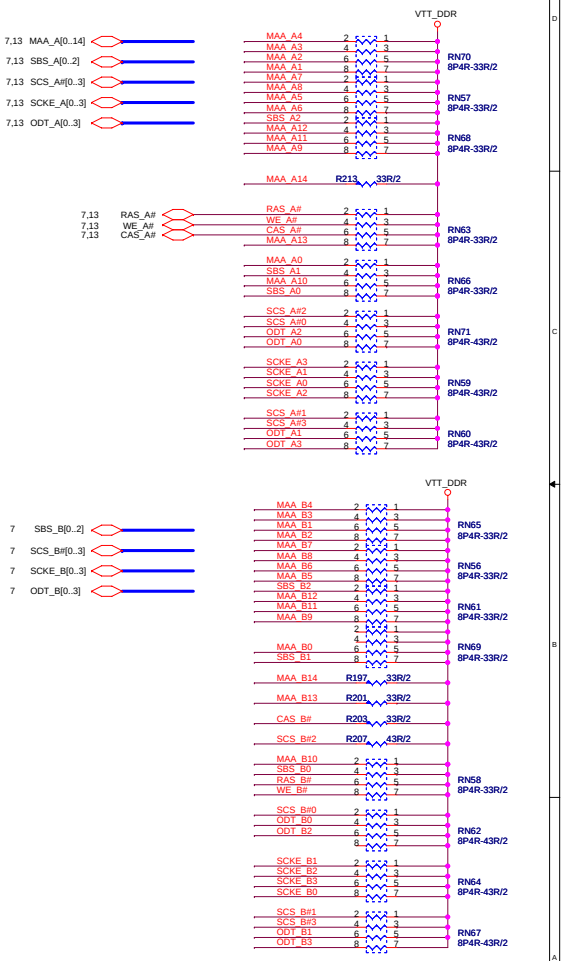
DDR II Termination

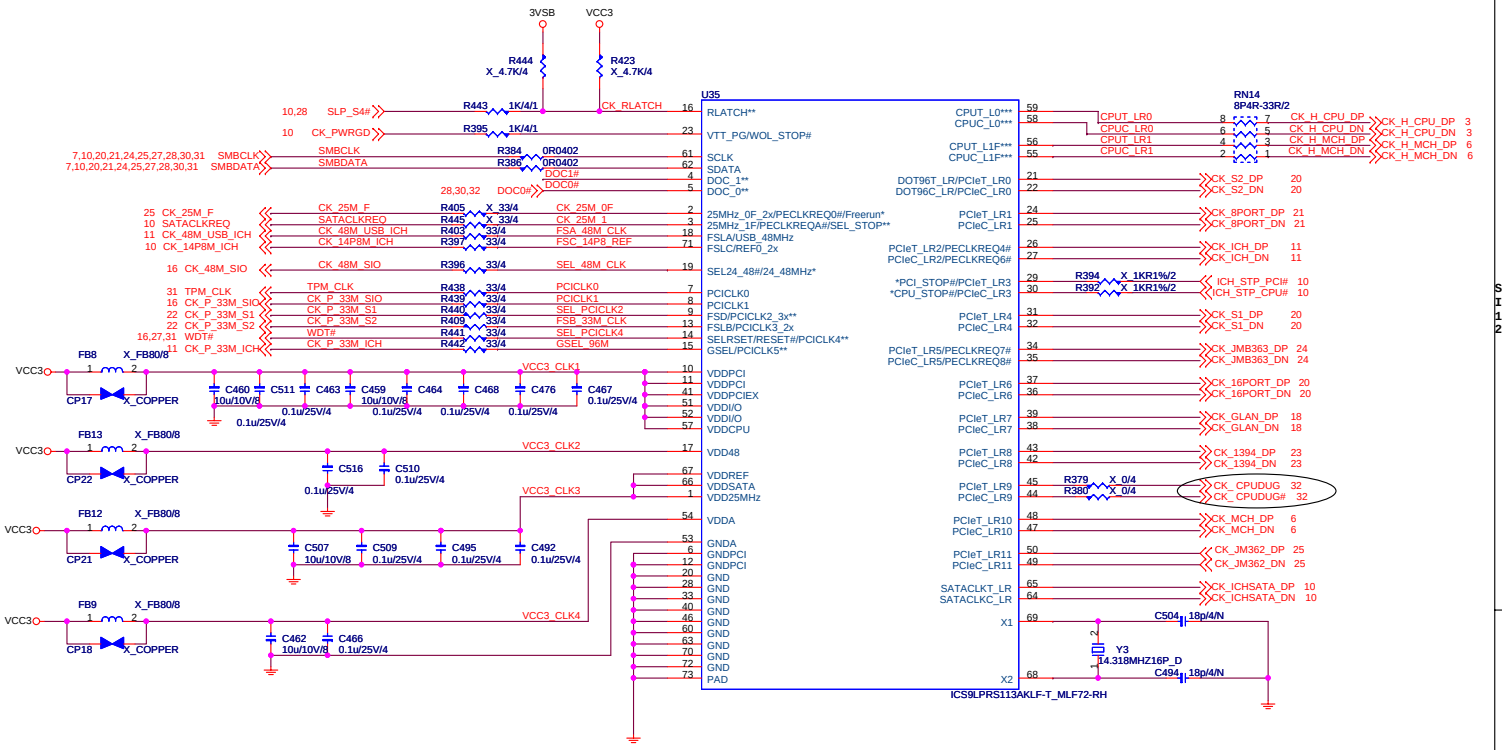


DDRII DIMM_B1

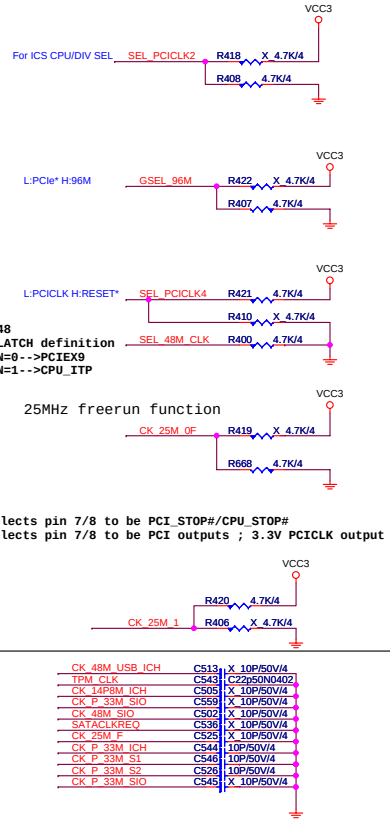
DDRII DIMM_B2



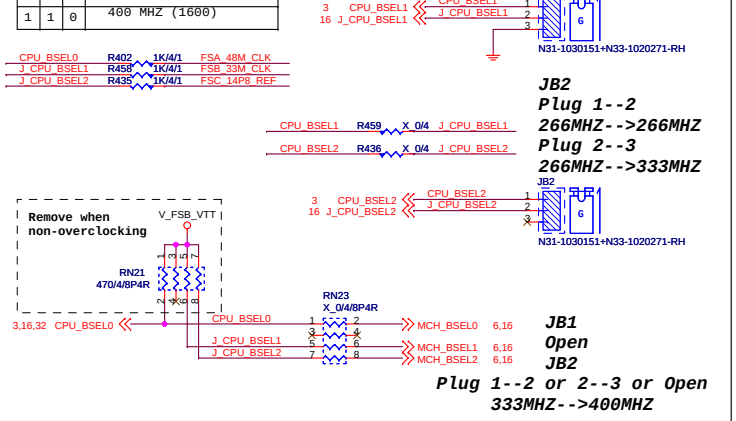
MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: DDR2 Chanel-A / Chanel-B	Rev: 1.1
Date: Thursday, March 20, 2008	Sheet 14 of 32	

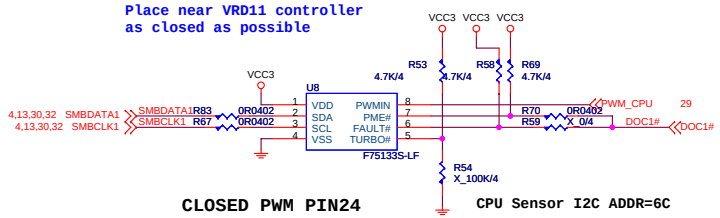


CLOCK GEN STRAPING



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
1	0	0	333 MHZ (1333)
0	1	0	200 MHZ (800)
1	1	0	400 MHZ (1600)





EASY DOT FUNCTION

DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

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Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS110	1.1

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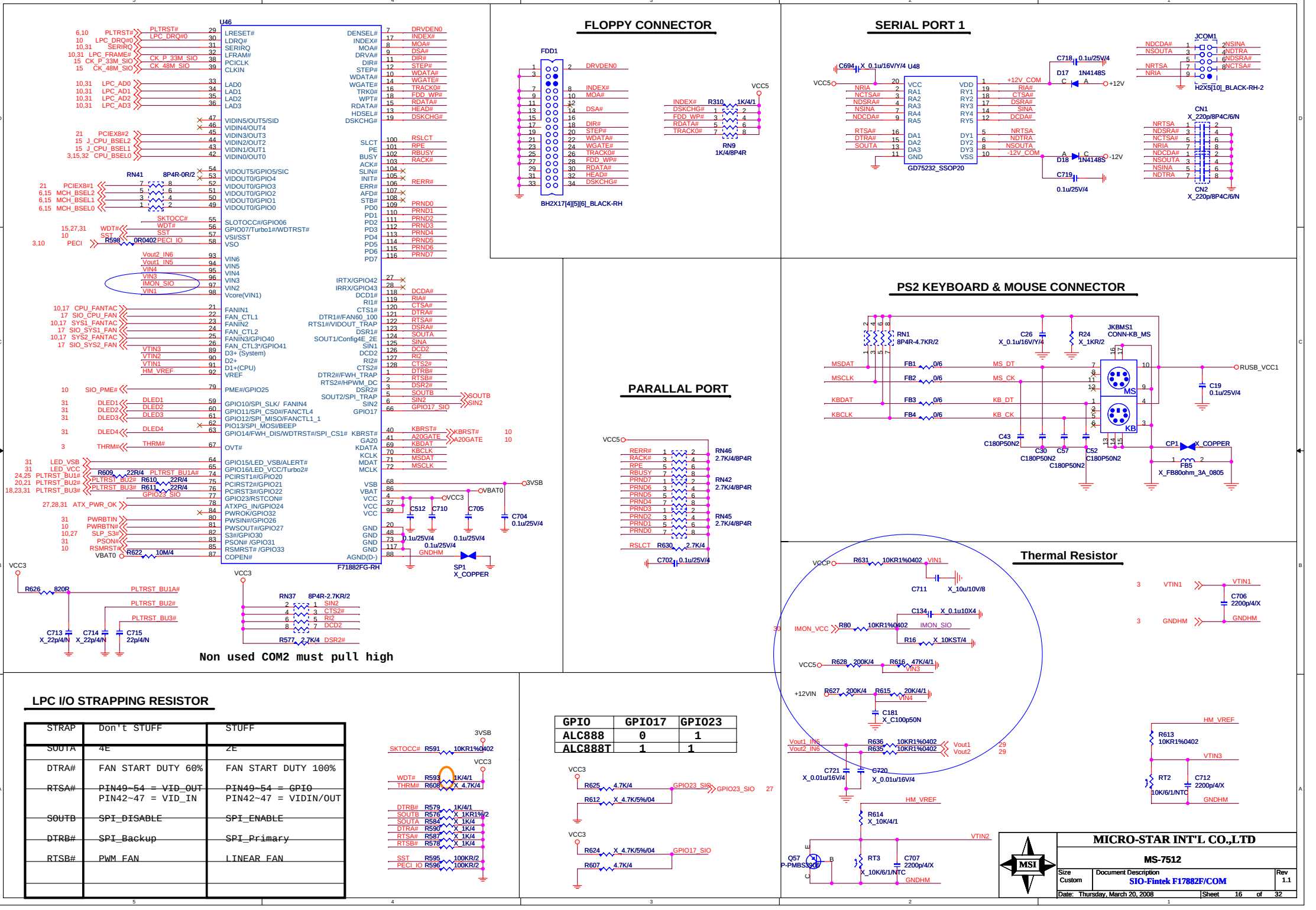
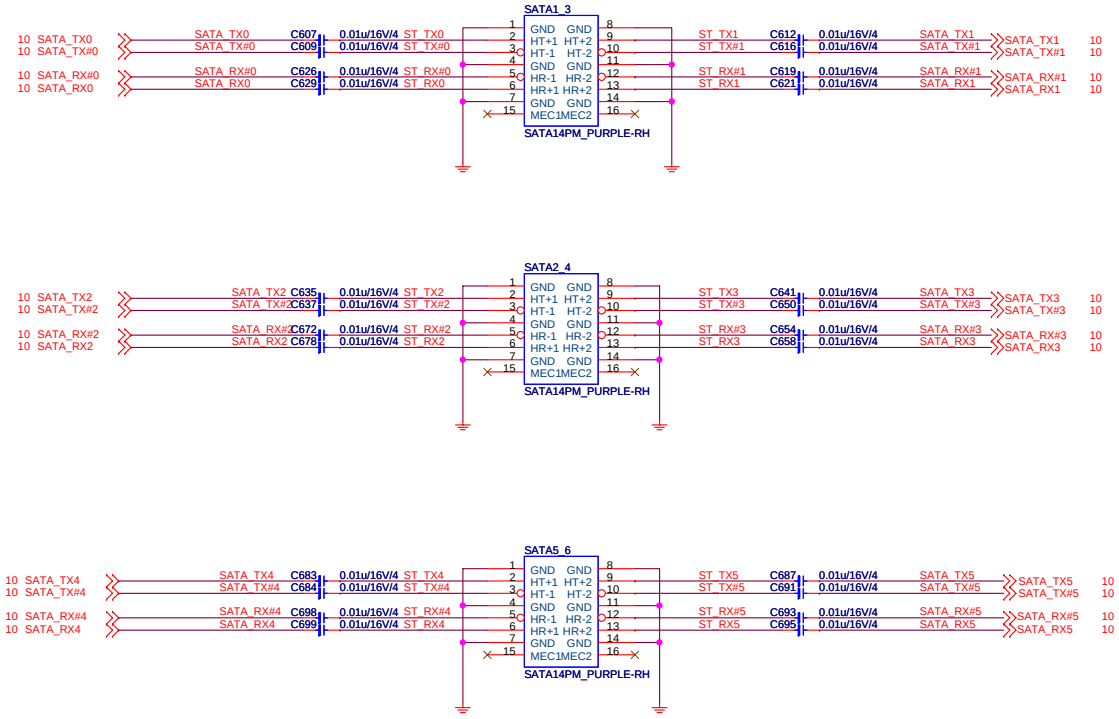
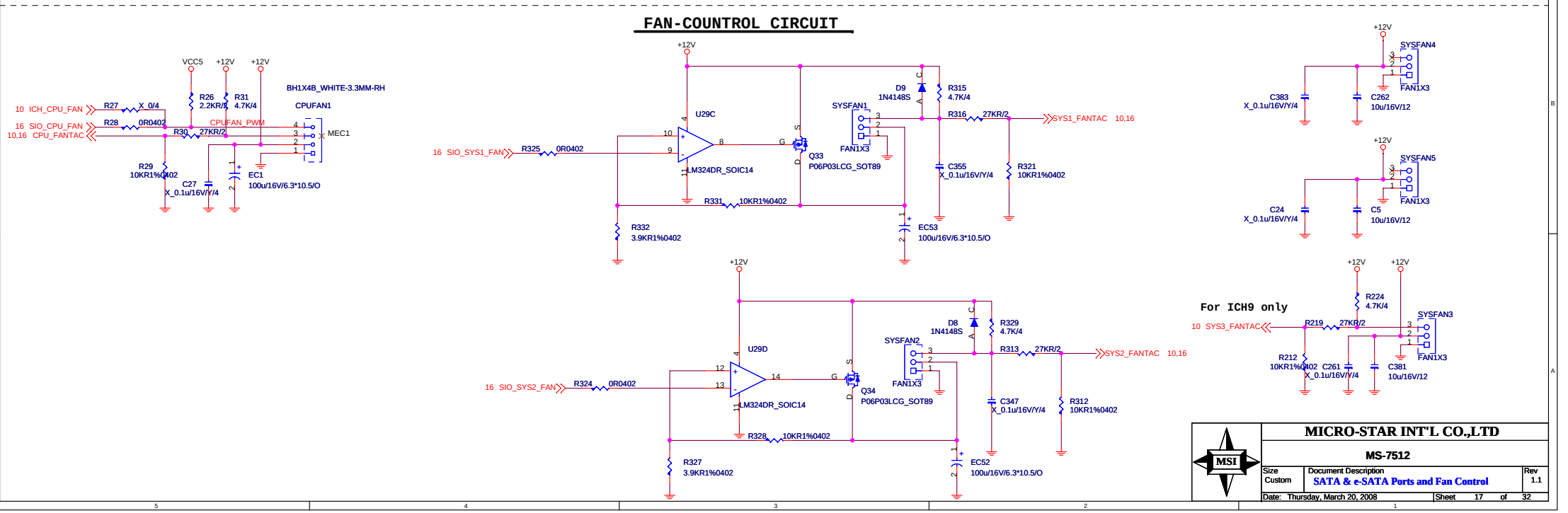


STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
RTSA#	PIN49~54 = VID_OUT PIN42~47 = VID_IN	PIN49~54 = GPIO PIN42~47 = VIDIN/OUT
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRB#	SPI_Backup	SPI_Primary
RTSB#	PWM_FAN	LINEAR_FAN

GPIO	GPIO17	GPIO23
ALC888	0	1
ALC888T	1	1


SATA1_3
SATA14PM_PURPLE-RH
SATA2_4
SATA14PM_PURPLE-RH
SATA5_6
SATA14PM_PURPLE-RH


FAN-COUNTROL CIRCUIT
BH1X4B_WHITE-3.3MM-RH
CPUFAN1
LM324DR_SOIC14
Q33
P06P03LCG_SOT89
FAN1X3
LM324DR_SOIC14
Q34
P06P03LCG_SOT89
FAN1X3
For ICH9 only
MICRO-STAR INT'L CO.,LTD
MS-7512
SATA & e-SATA Ports and Fan Control
Rev 1.1
Thursday, March 20, 2008
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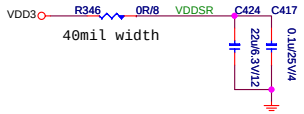
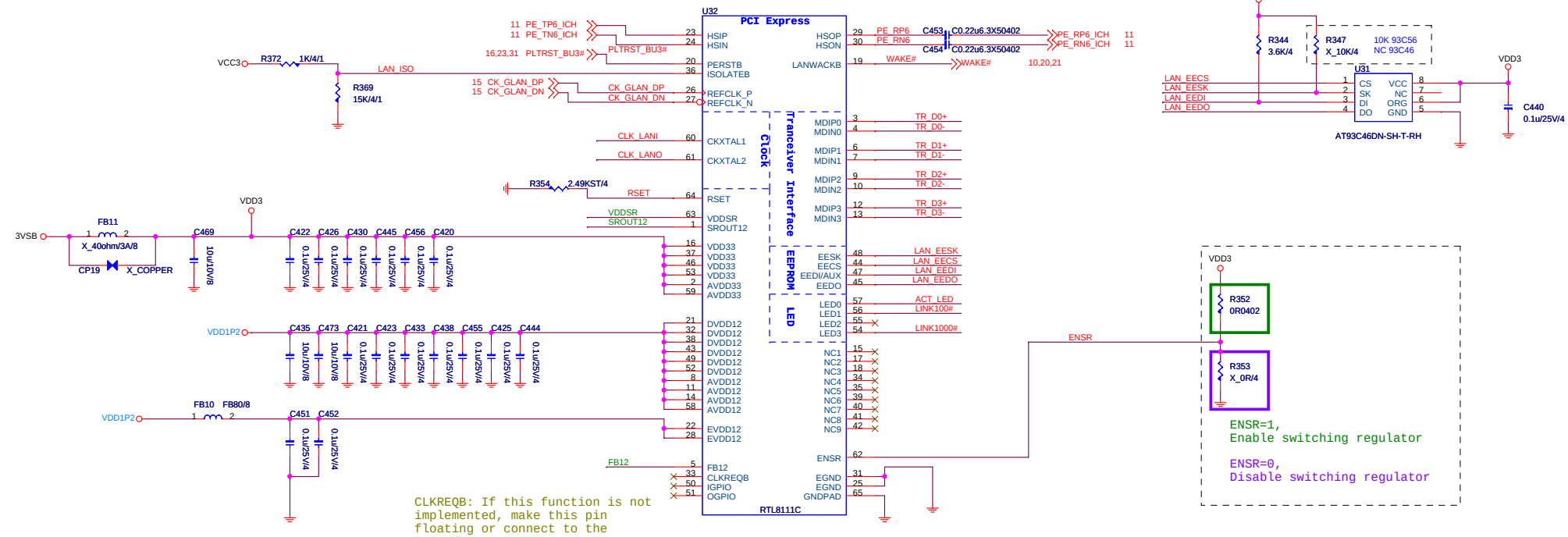
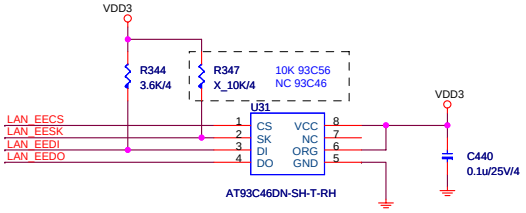
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21,D3

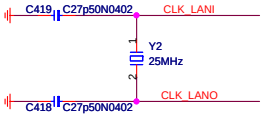


C657 C346 near Pin63 200mil,C346 must be nearly Pin63

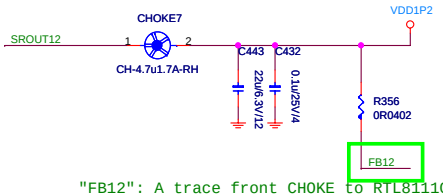


CLKREQB: If this function is not implemented, make this pin floating or connect to the ground.

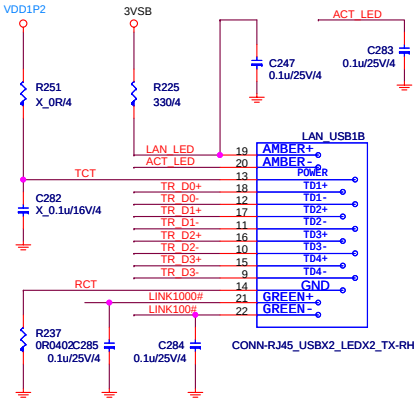




Choke C656 C345 near Pin1 200mil



"FB12": A trace front CHOKE to RTL8111C pin5



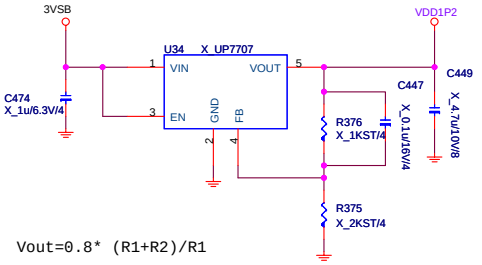
Giga-Lan
N58-22F0181-S42

Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

19 — 20 Yellow

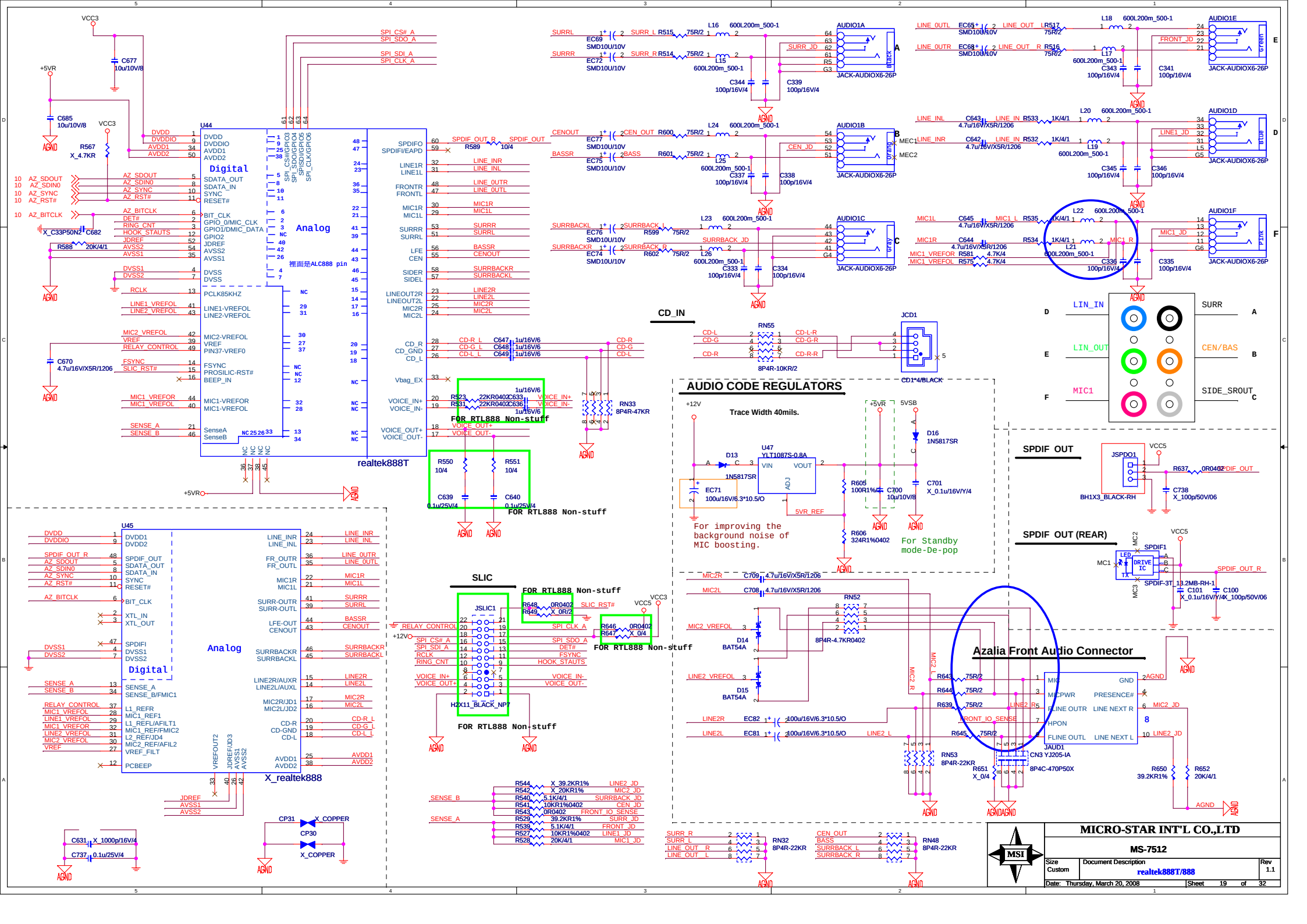
21 — 22 Orange Green

8111C switching regulator disabled

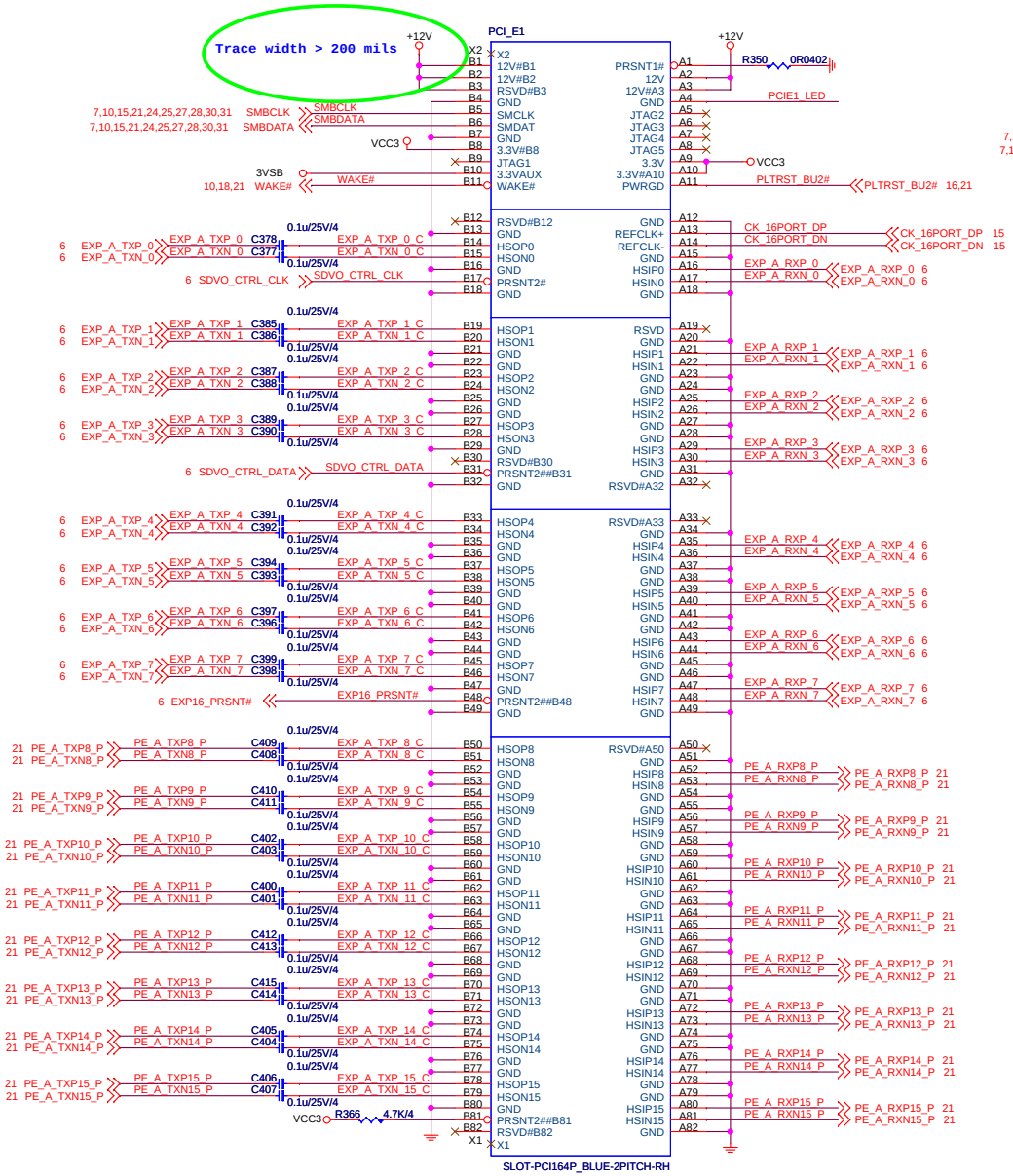


Vout=0.8* (R1+R2)/R1

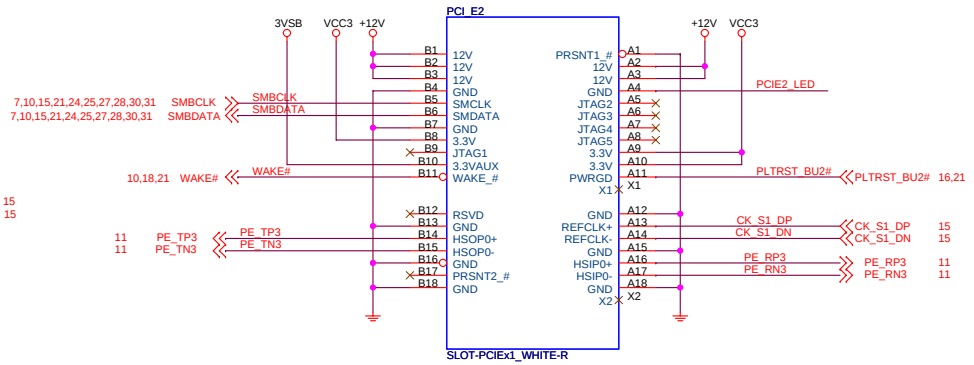
MICRO-STAR INT'L CO.,LTD			
MS-7512			
Size: Custom	Document Description: LAN Realtek RTL8111C(PCIE)		Rev: 1.1
Date: Thursday, March 20, 2008		Sheet 18 of 32	


realtek888T
X_realtek888
AUDIO CODE REGULATORS
Trace Width 40mils.
For improving the background noise of MIC boosting.
For Standby mode-De-pop
SLIC
FOR RTL888 Non-stuff
CD_IN
SPDIF OUT
SPDIF OUT (REAR)
Azalia Front Audio Connector
MICRO-STAR INT'L CO.,LTD
MS-7512
realtek888T/888
Size Custom
Document Description
Rev 1.1
Date: Thursday, March 20, 2008
Sheet 19 of 32

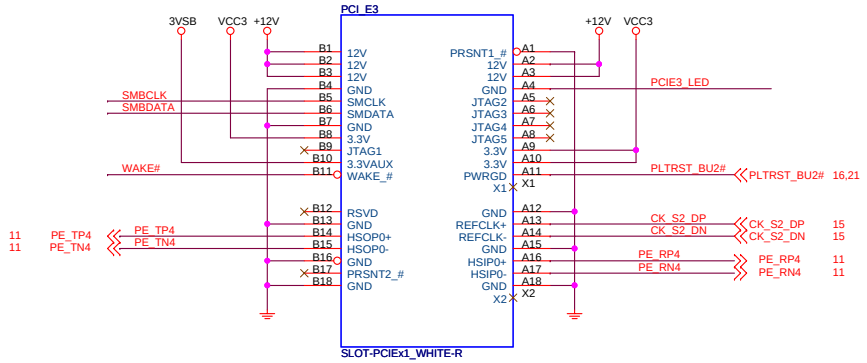
PCI_Express X16 Slot

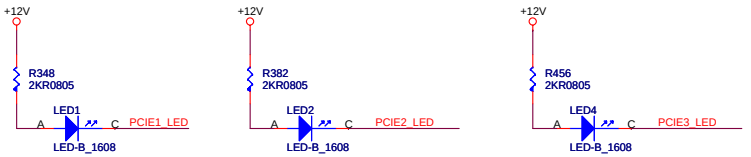


PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT





MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: PCIE x16, x1	Rev: 1.1
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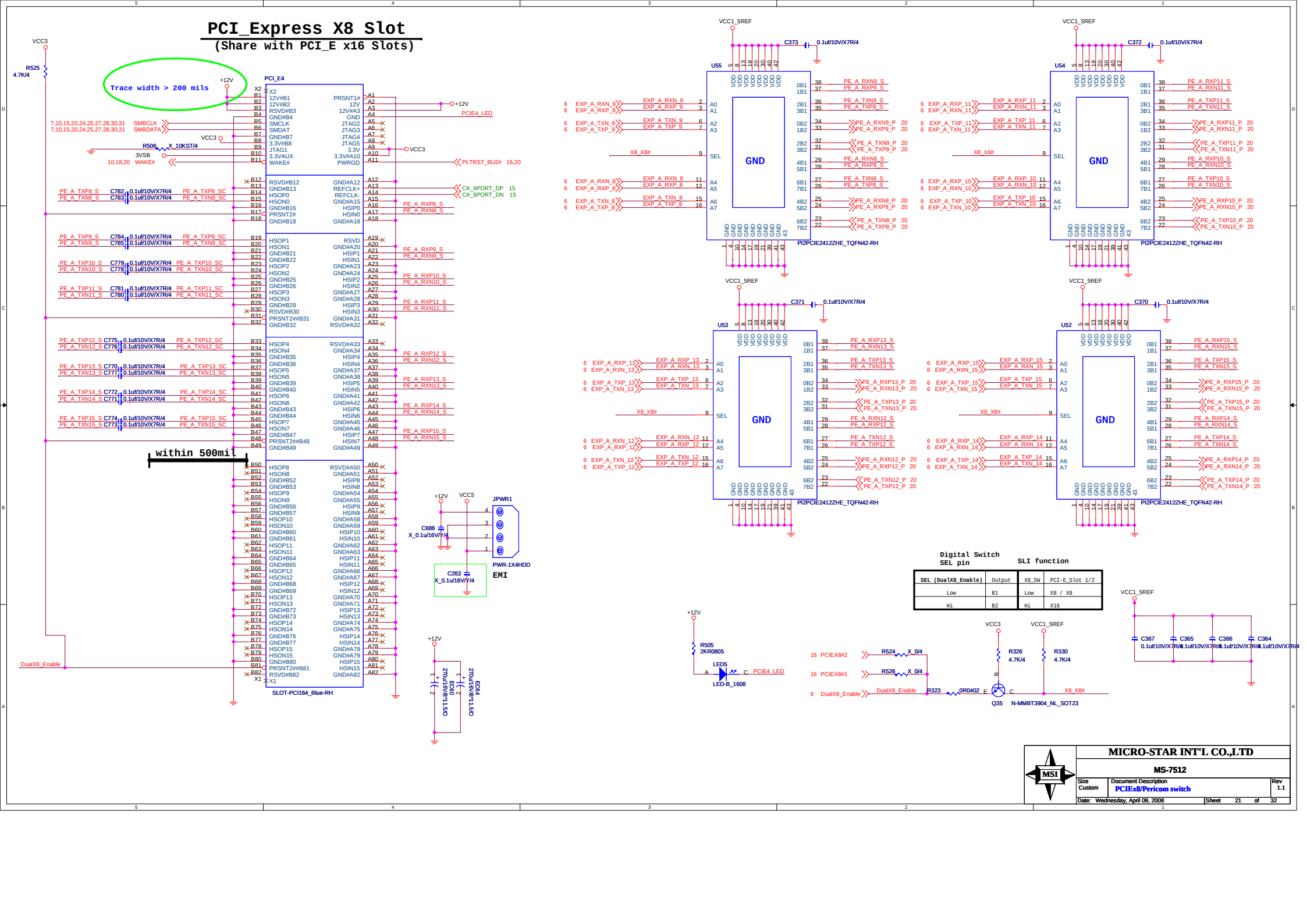
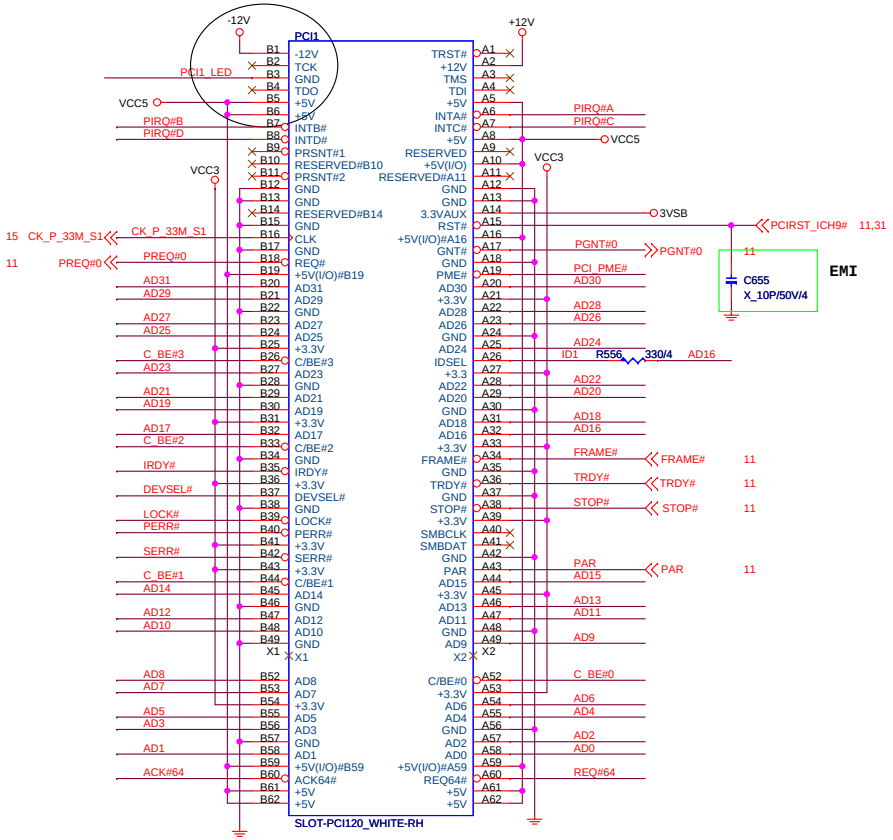
PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



Digital Switch SEL pin — SLI function

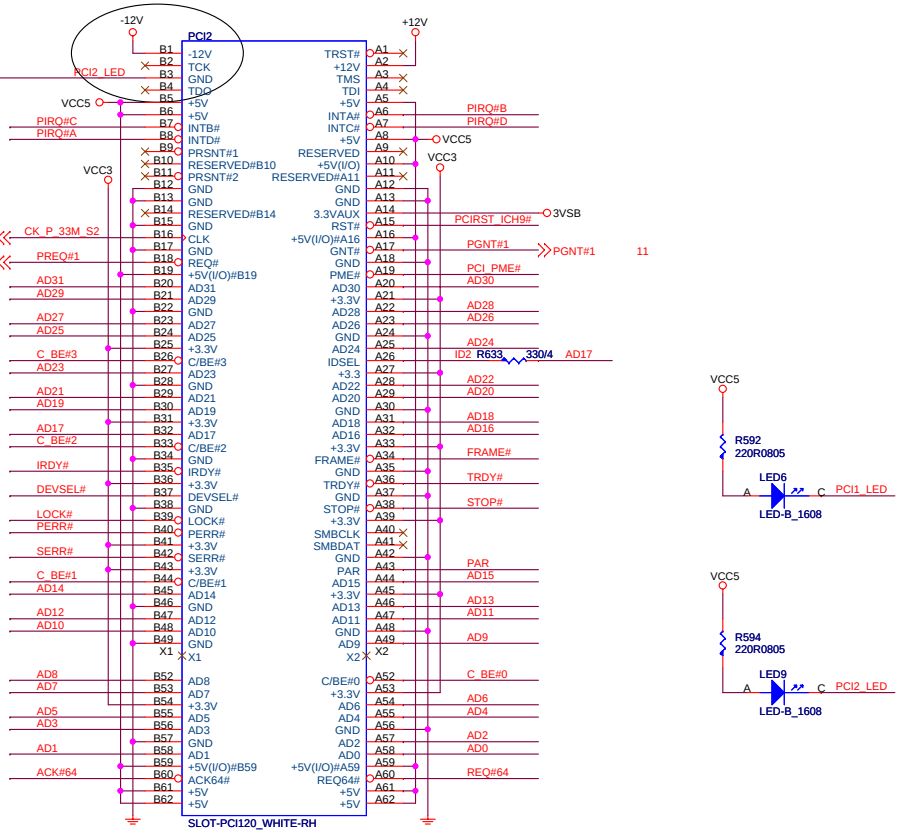
SEL (DualX8_Enable)	Output	X8_SW	PCI-E_Slot 1/2
Low	B1	Low	X8 / X8
Hi	B2	Hi	X16

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



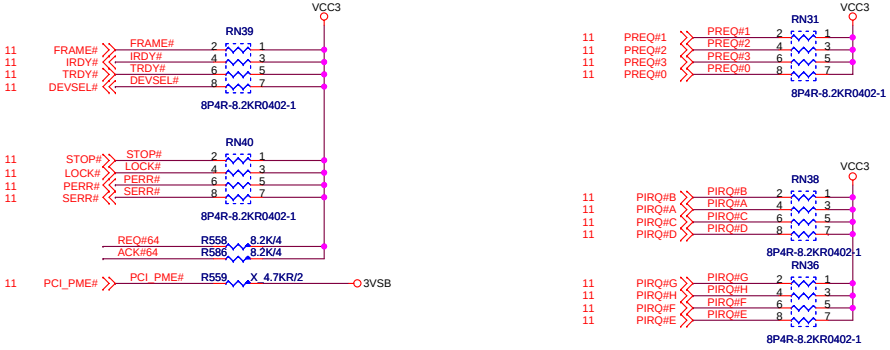
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

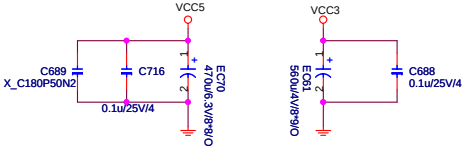


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 1.1
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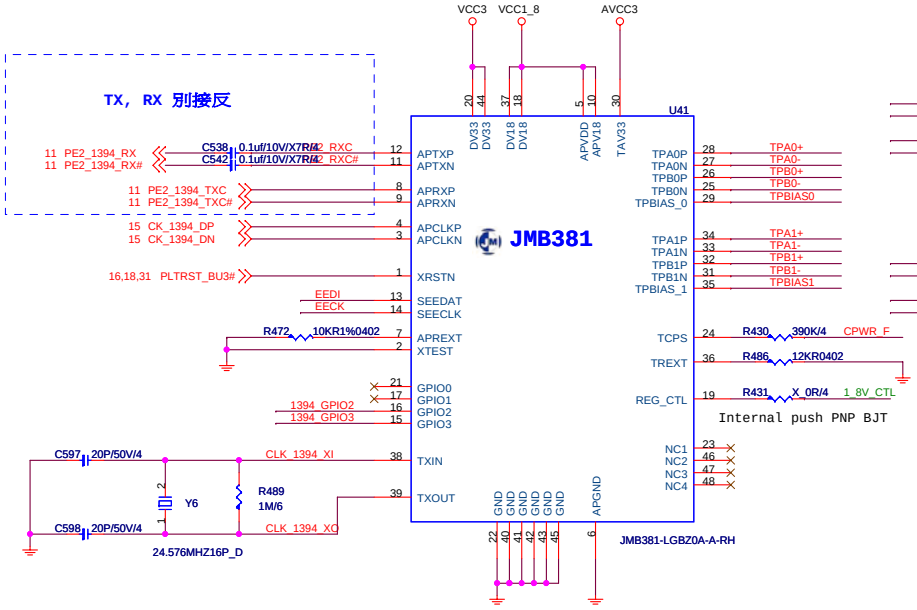
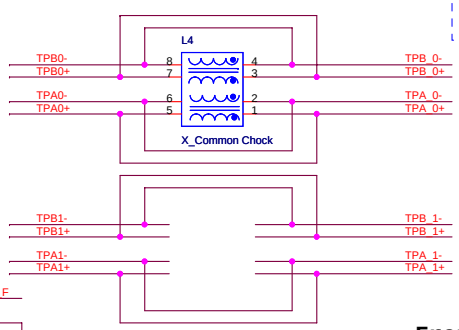
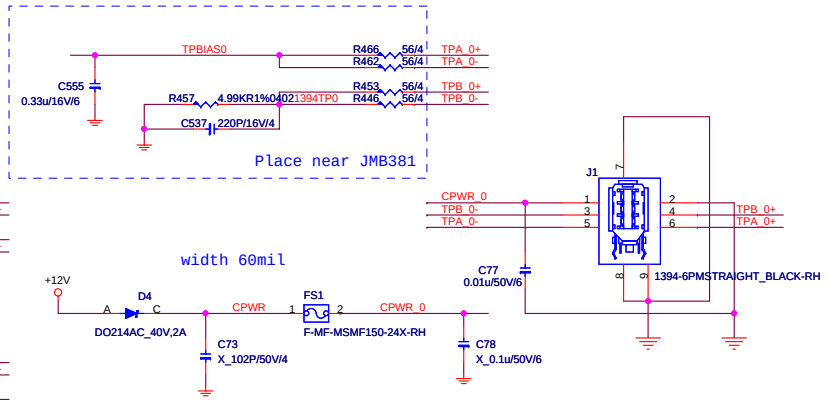
1394 CONTROLLER

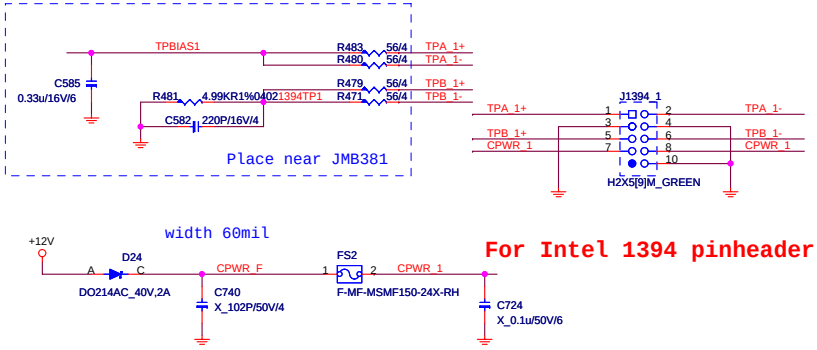


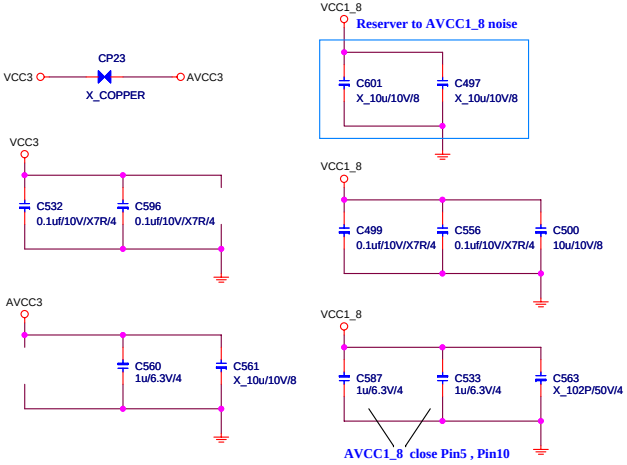


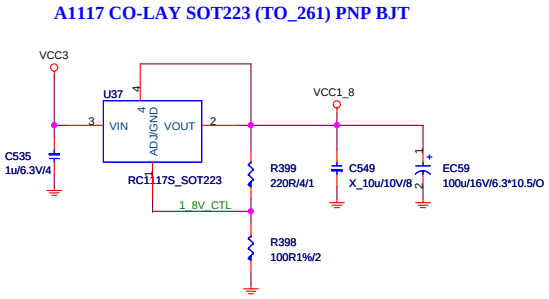
Rear 1394 port

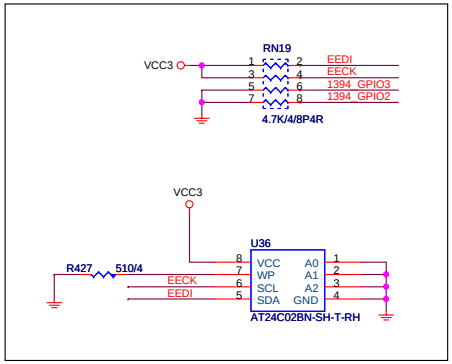


Front 1394 pin header

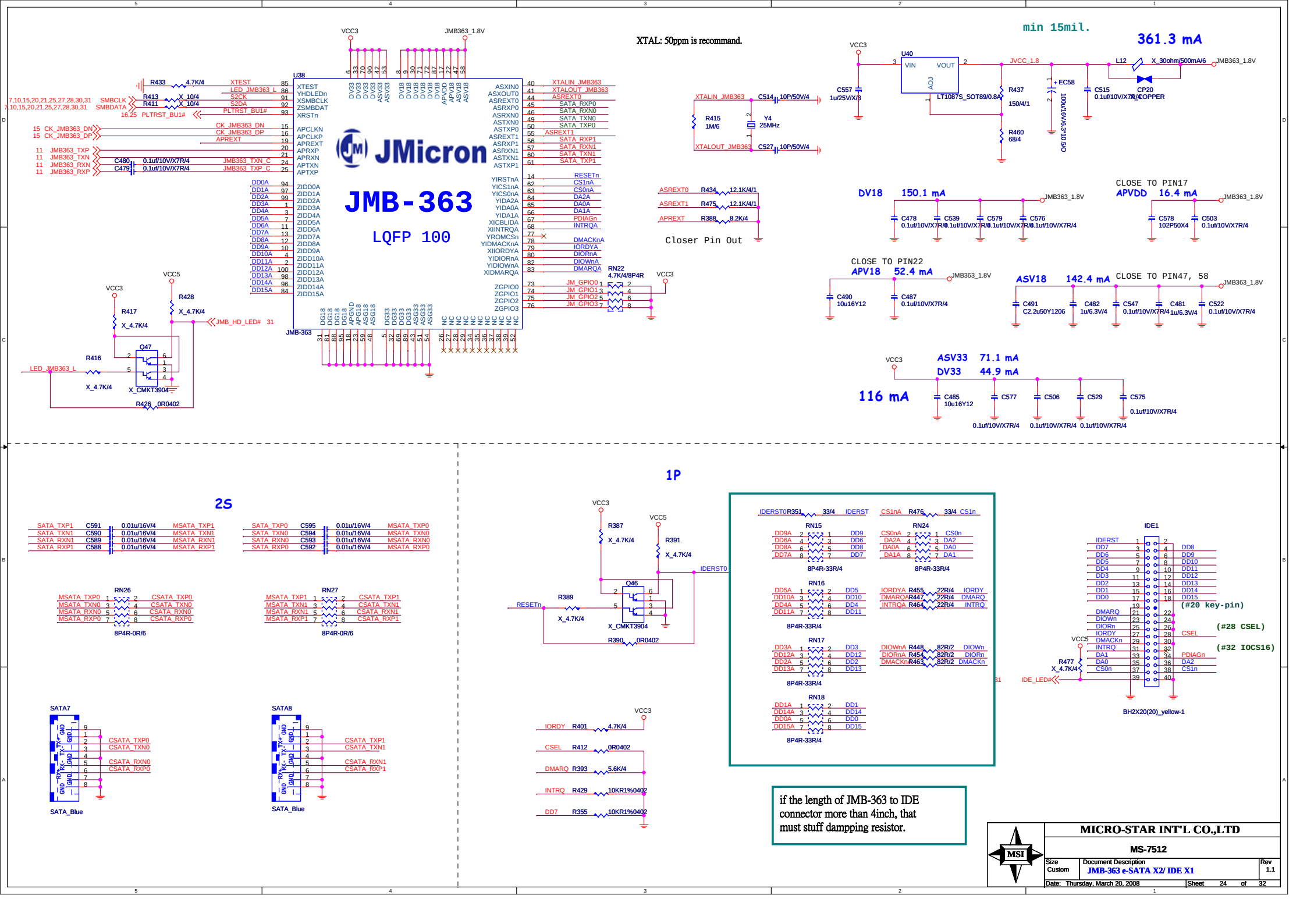








MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: 1394 Controller - JMB381	Rev: 1.1
Date: Monday, March 24, 2008	Sheet 23 of 32	


JMB-363
LQFP 100
JMicron
XTAL: 50ppm is recommand.
min 15mil.
361.3 mA
Closer Pin Out
CLOSE TO PIN17
CLOSE TO PIN22
CLOSE TO PIN47, 58
DV18 150.1 mA
APVDD 16.4 mA
APV18 52.4 mA
ASV18 142.4 mA
ASV33 71.1 mA
DV33 44.9 mA
116 mA
2S
1P
SATA7
SATA8
SATA_Blue
IDE1
BH2X20(20)_yellow-1
(#20 key-pin)
(#28 CSEL)
(#32 IOCS16)
if the length of JMB-363 to IDE connector more than 4inch, that must stuff dampping resistor.
MICRO-STAR INT'L CO.,LTD
MS-7512
JMB-363 e-SATA X2/ IDE X1
Size Custom
Rev 1.1
Date: Thursday, March 20, 2008
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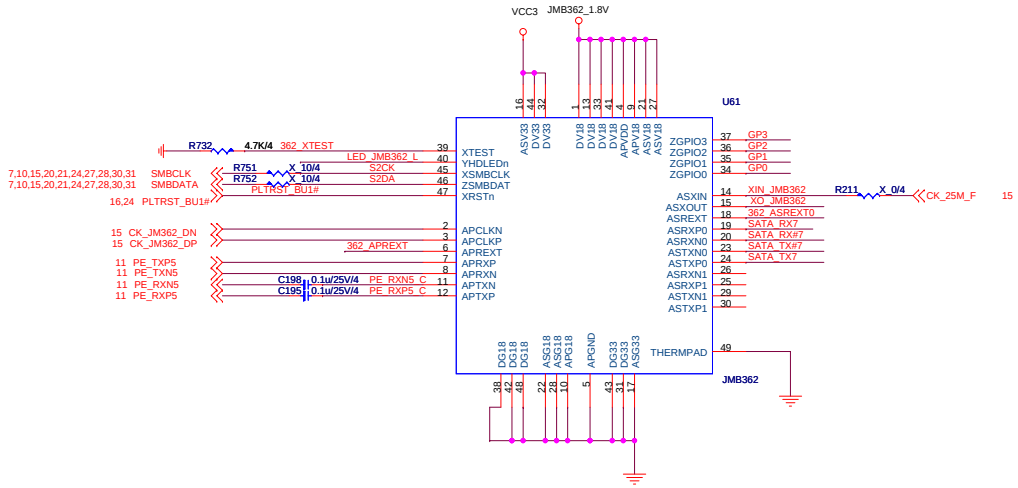
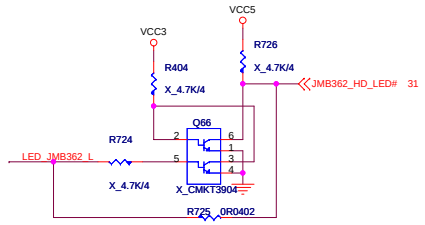
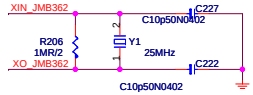
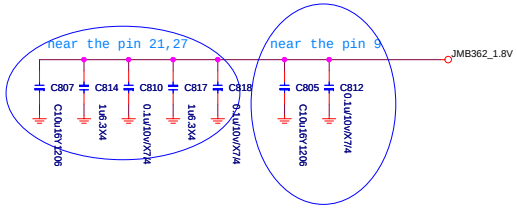
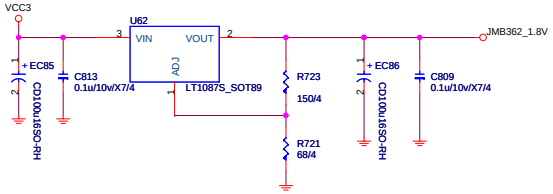
Hi-Speed PCIE to SATA/PATA Bridge

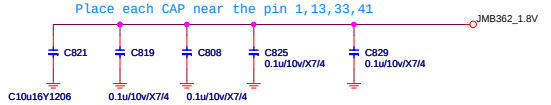


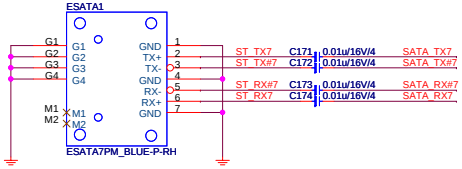


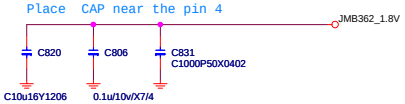


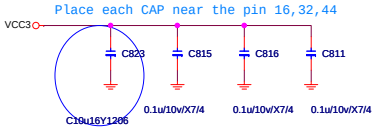












MICRO-STAR INT'L CO.,LTD		
MS-7512		
Size: Custom	Document Description: Marvell 88SE6111 PCIE to PATA/SATA	Rev: 1.1
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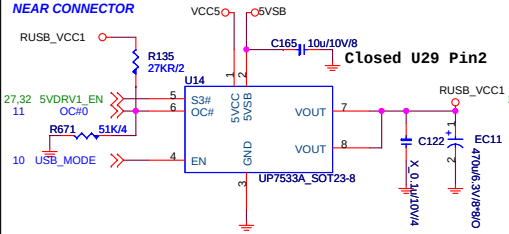
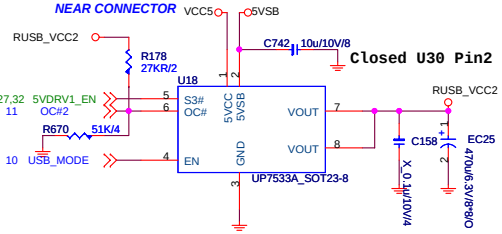
Rear USB Connector

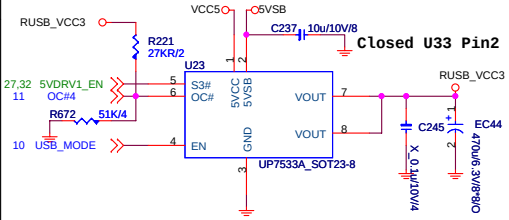
USB POWER FOR PORT 6,7



USB POWER FOR PORT 8,9



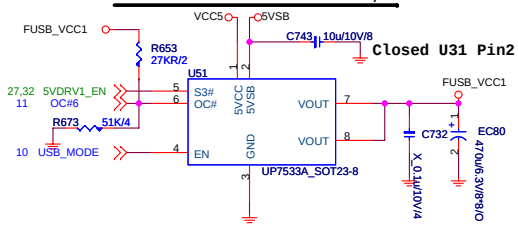
USB POWER FOR PORT 10,11



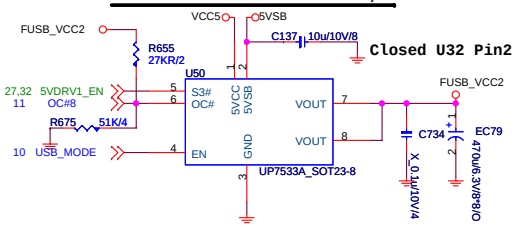
GPIO for USB voltage
H:Follow 5VSB
L:Always off

Front USB Connector

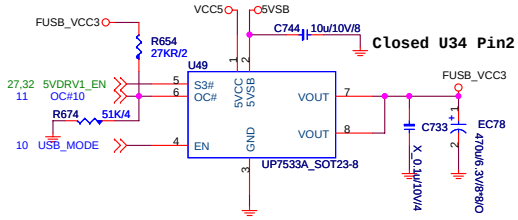
USB POWER FOR PORT 0,1



USB POWER FOR PORT 2,3

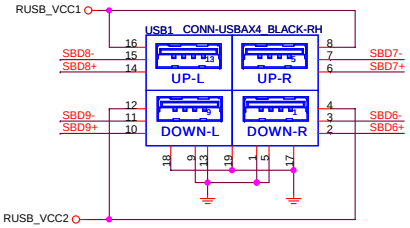


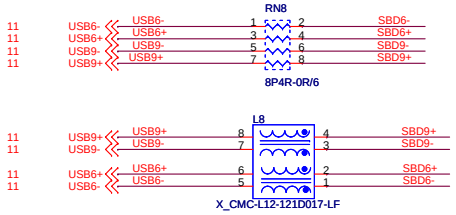
USB POWER FOR PORT 4,5

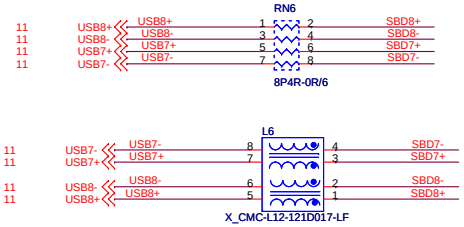


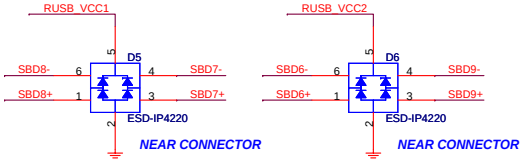
GPIO for USB voltage
H:Follow 5VSB
L:Always off

REAR USB PORT 6,7,8,9 (2x2)

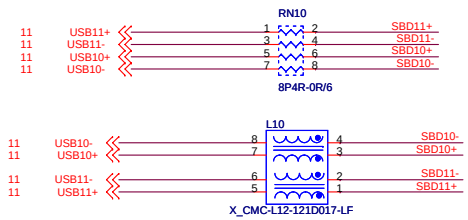


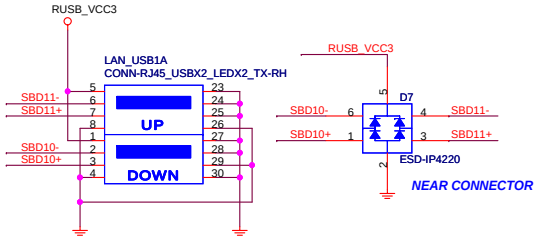




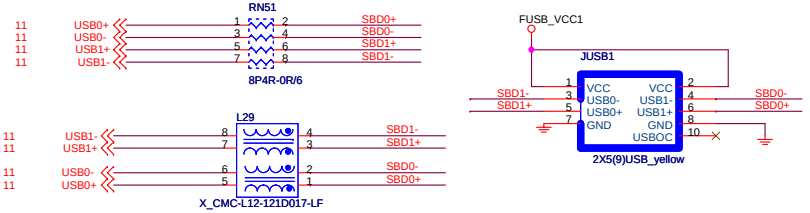


REAR USB PORT 10,11 (With LAN)

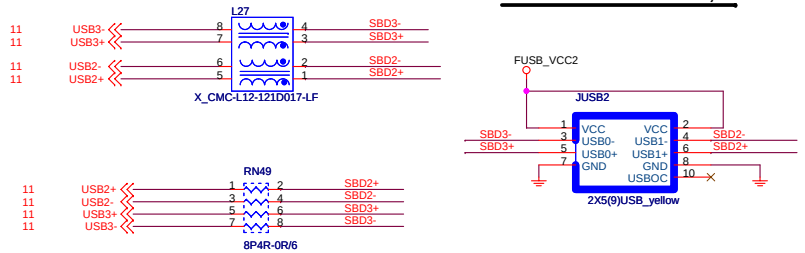




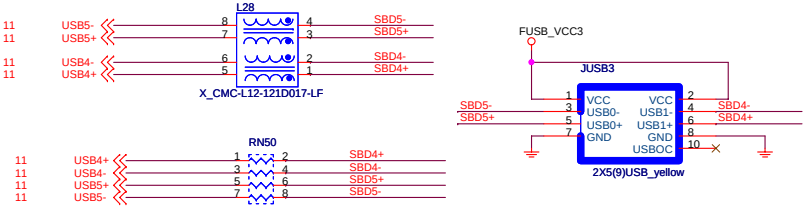
FRONT USB PORT 0,1



FRONT USB PORT 2,3



FRONT USB PORT 4,5



MICRO-STAR INT'L CO.,LTD

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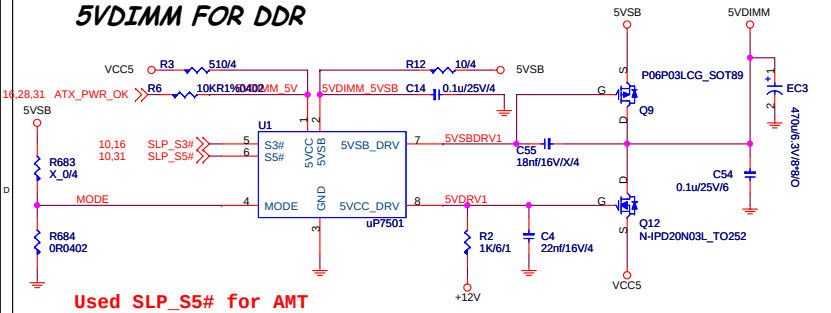
Size	Document Description	Rev
Custom	USB Connectors	1.1

Date: Thursday, March 20, 2008 Sheet 26 of 32

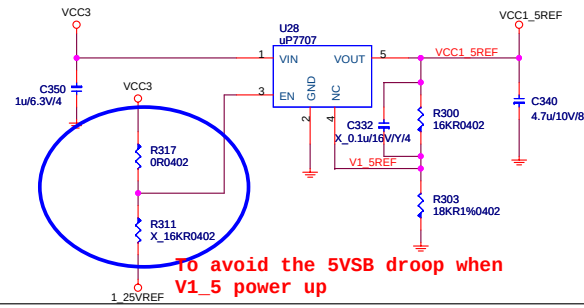
5VDIMM FOR DDR



Used SLP_S5# for AMT

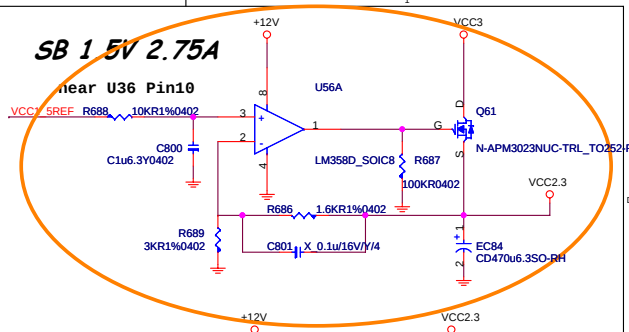
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_5REF

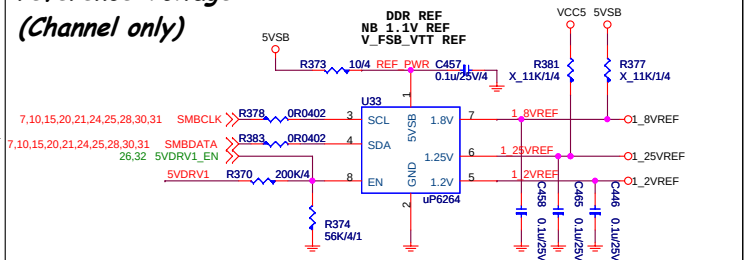


To avoid the 5VSB droop when V1_5 power up

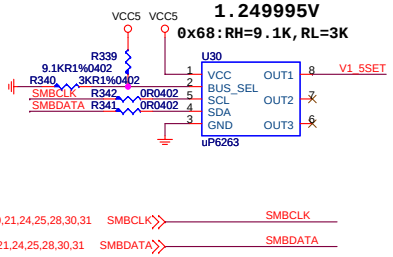
SB 1.5V 2.75A



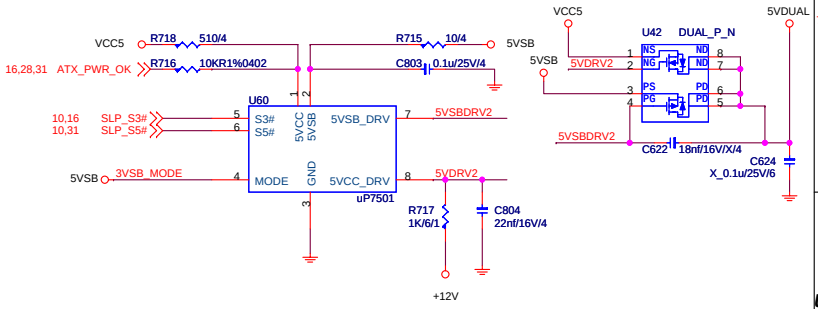
reference Voltage (Channel only)



UPI VOLTAGE CONSOLE(3)

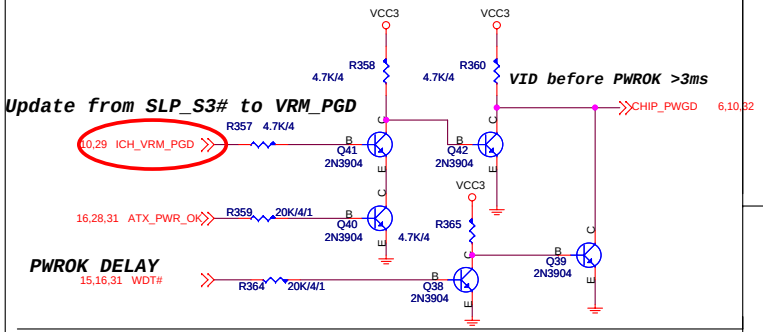


3VSB



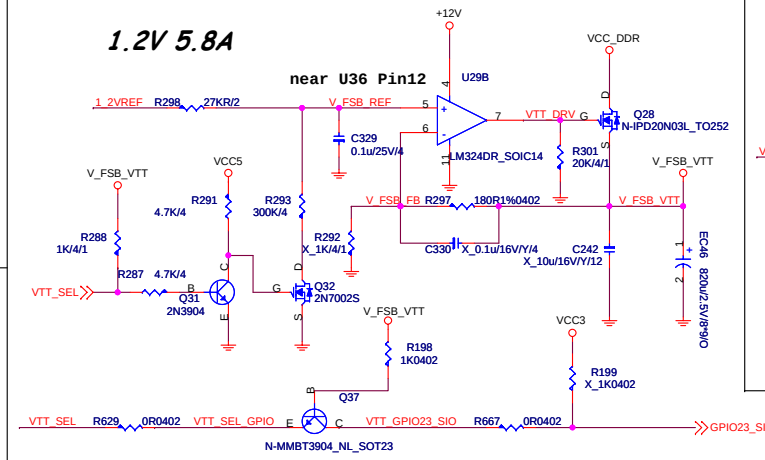
Update from SLP_S3# to VRM_PGD

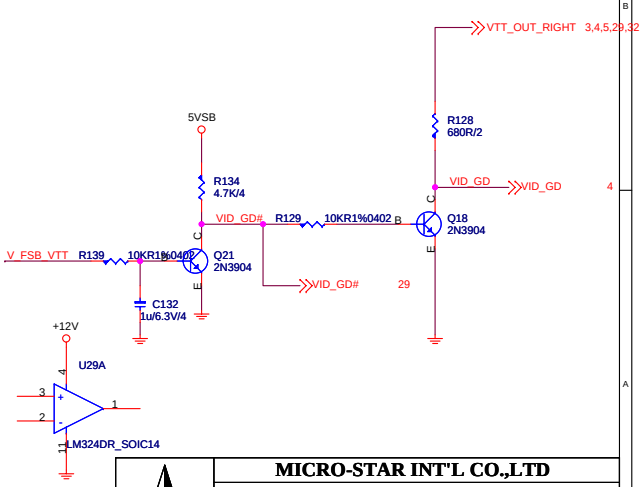
VID before PWROK >3ms

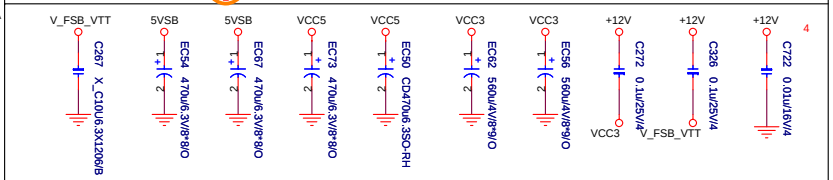


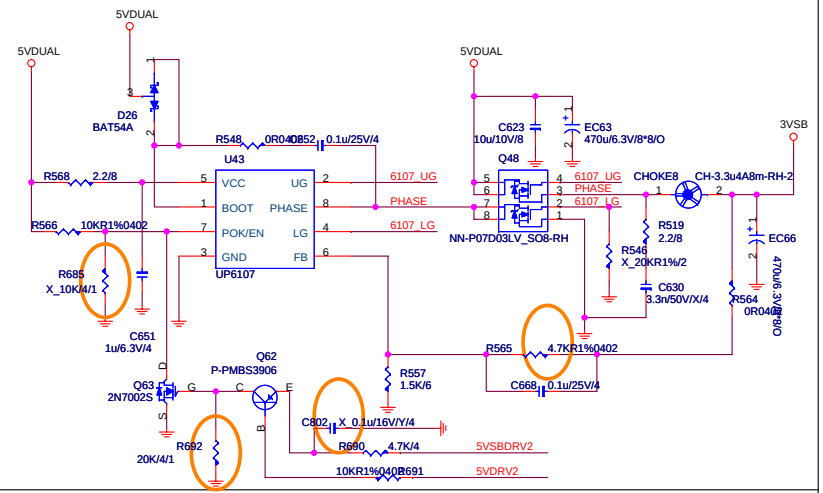
1.2V 5.8A

near U36 Pin12









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R506 CHANGE R CAN CHANGE FREQUENCY (33K=300KHZ)

DDR II 1.8V POWER

7.2A+0.75A+3A+?A=18A
(DDRIII+V_SM_VTT+NB_VCC_CL+NB_V_SM)

Iripple=18*0.6*0.8/1=8.64A
5.7*2*1=11.4A>8.64A

1.442V*(3K+12.1K)/12.1K=1.8V

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

de- VCC_DDR high frequency noise.

NB 1.1V POWER

Iripple=24.2*0.49*0.878/1=10.4A
5.7*2*1=11.4A>10.4A

NB_V1_1

For channel DOT3 used.

Place near DDR VRM controller as closed as possible

CLOSED DDR POWER PIN4

DDR Sensor I2C ADDR=66

30A

Irms(MAX) of VCC1_1=30A
(30A-4.6A-1.2A=24.2A)
(Imax-V_FSB_VTT(CPU)-V_FSB_VTT(NB)-24.2A)

CHANNEL B V_SM_VTT DECOULPING CAPS

CHANNEL A V_SM_VTT DECOULPING CAPS

EMI

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ISL6336CR VRD11.1 POWER CKT

TABLE 1. PHASE DROPPING BEHAVIOR

	PS#	FS	SS
Non-CI or (n-1)-CI Drops to 1-Phase	0	0	0
Non-CI or (n-2)-CI Drops to 2-Phase	0	0	1
2-Phase CI Drops to 1-Phase	0	1	0
2-Phase CI Drops to 2-Phase	0	1	1
Normal	1	x	x

POWER WATTAGE MONITOR

V1, V2 trace length不可拉太長,
LMV772MAX放在near PWM IC

VRMPWRGD LEVEL SHIFT

For Intel Bearlake Design Guide.
VRM must need level shift

For Power team test only

CLOSED PWM PIN24
4.3V

0.5V~1.6V/110A

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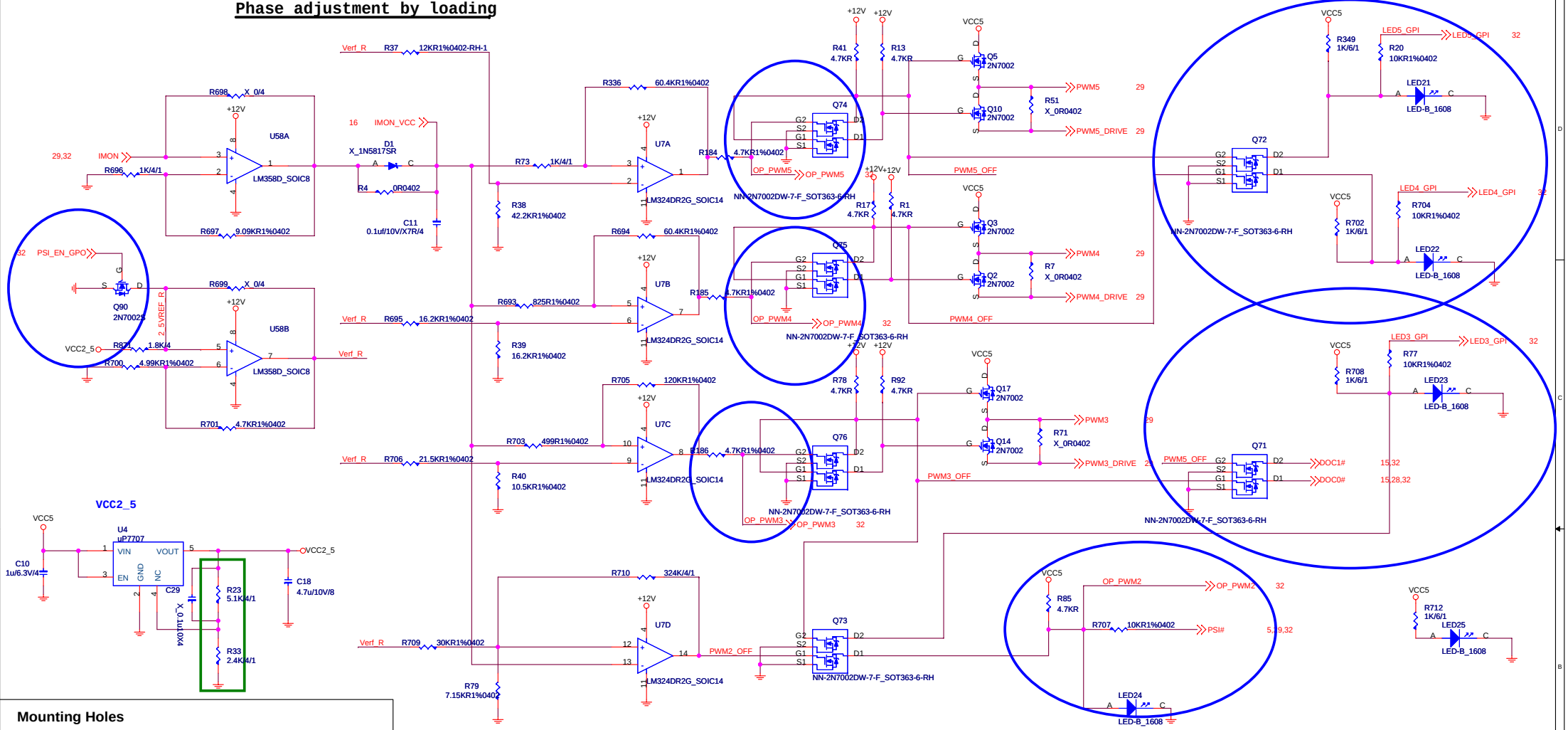
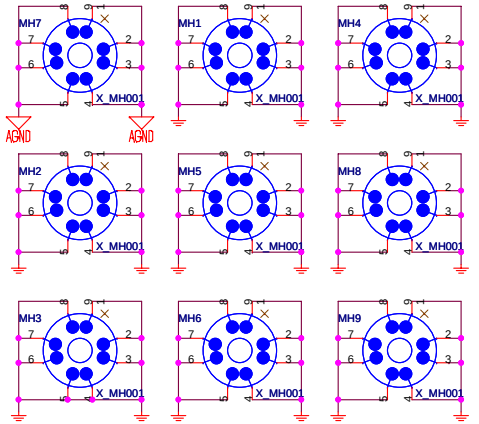
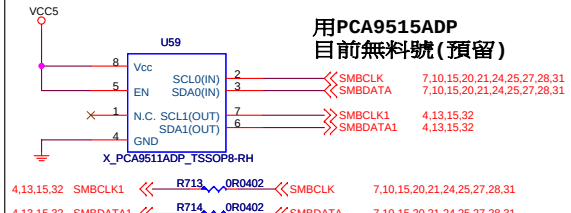
Phase adjustment by loading



Mounting Holes



用PCA9515ADP 目前無料號(預留)



Simulation

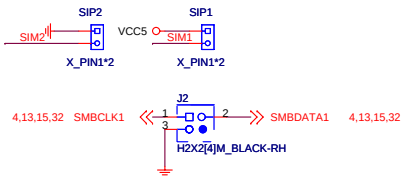
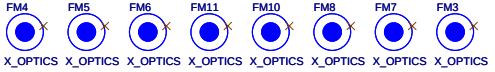


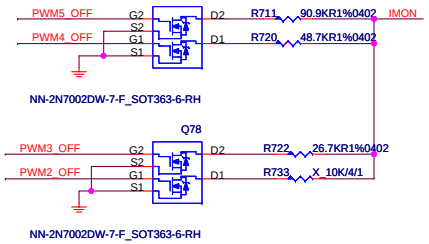
TABLE 1. PHASE DROPPING BEHAVIOR

	PSI#	FS	SS
Non-CI or (n-1)-CI Drops to 1-Phase	0	0	0
Non-CI or (n-2)-CI Drops to 2-Phase	0	0	1
2-Phase CI Drops to 1-Phase	0	1	0
2-Phase CI Drops to 2-Phase	0	1	1
Normal	1	x	x

Optical Fiducial Marks-120

Optical Fiducial Marks-100





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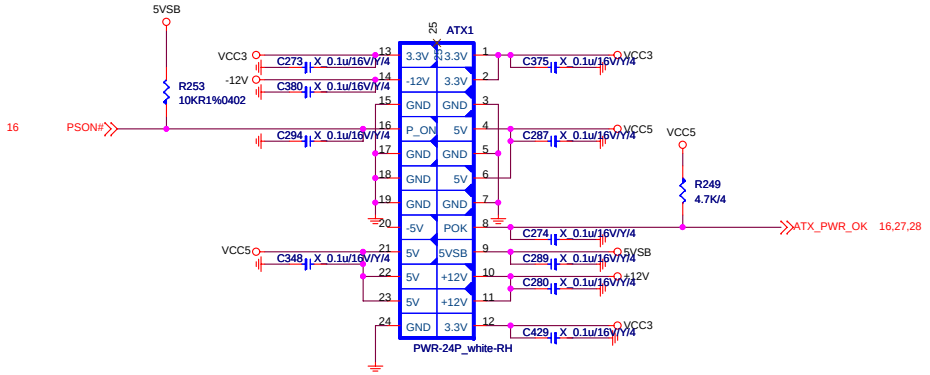
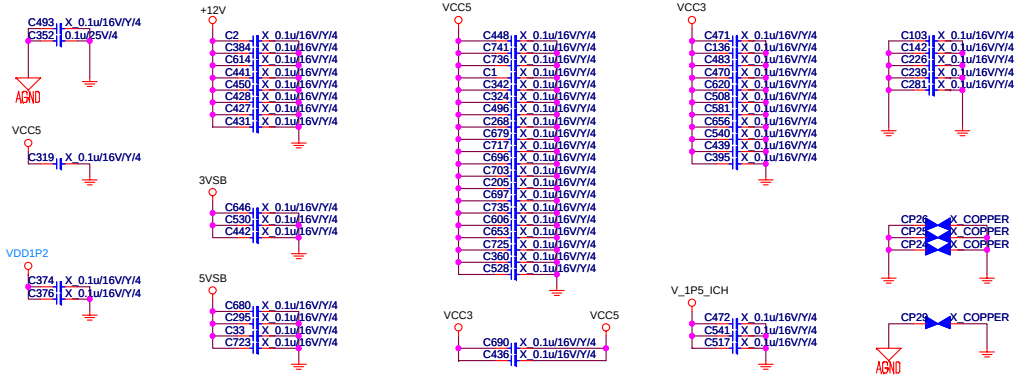
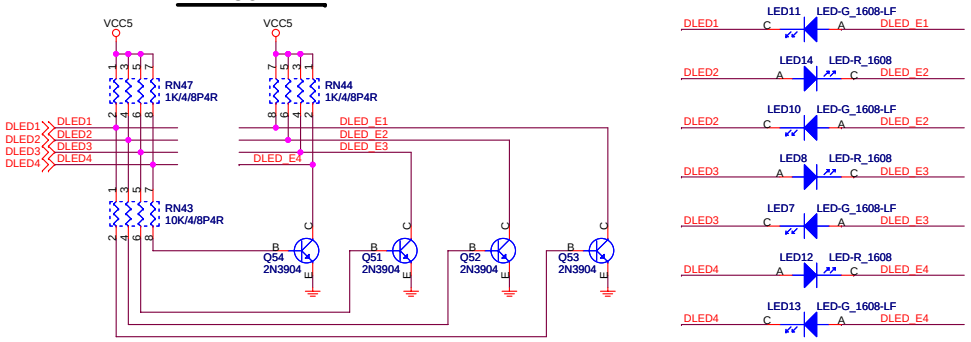
ATX POWER CONNECTOR

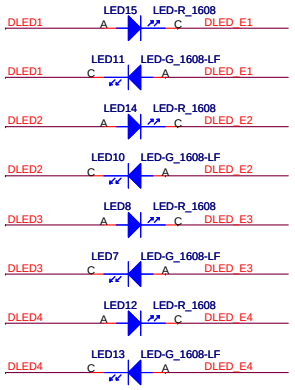


Cap. for EMI & Power

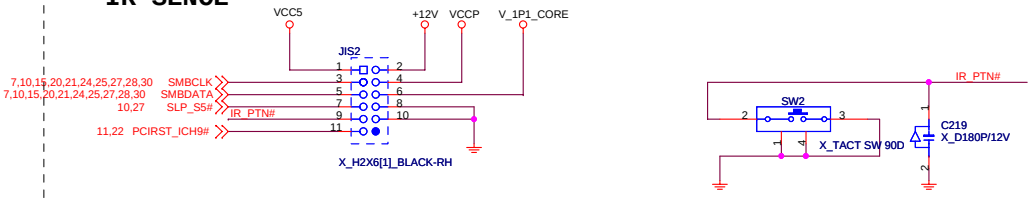


DEBUG LED

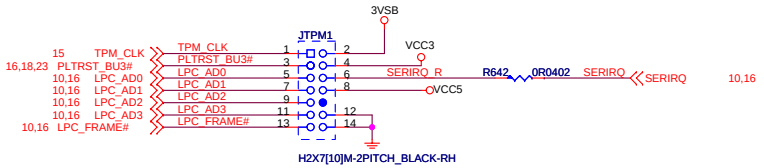




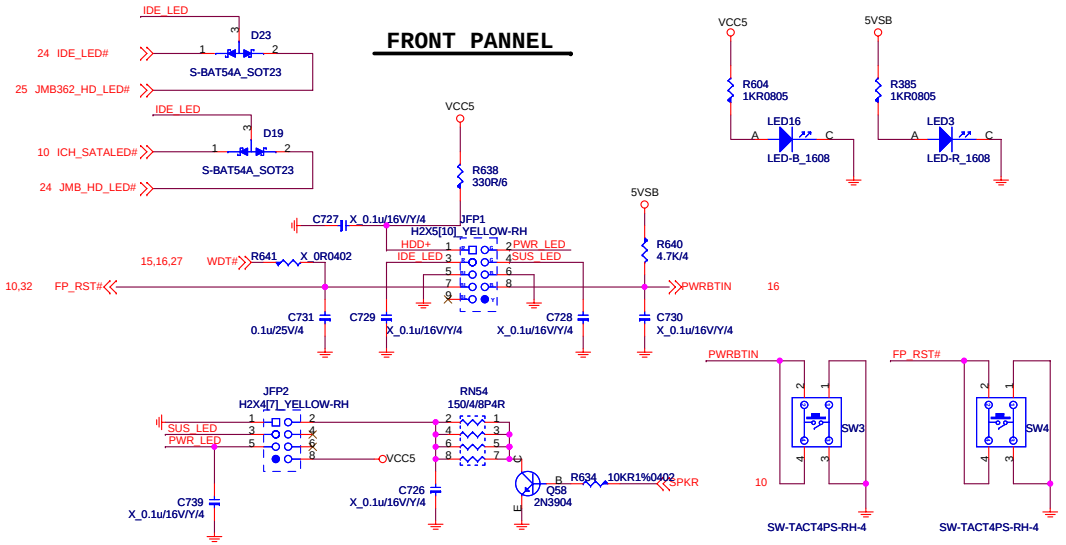
IR SENCE



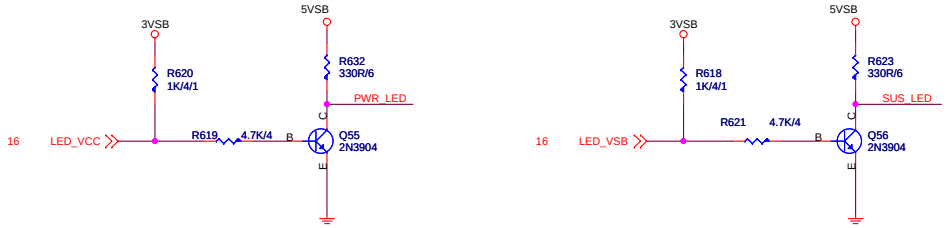
TPM



FRONT PANNEL



LED (for Fintek 71882)



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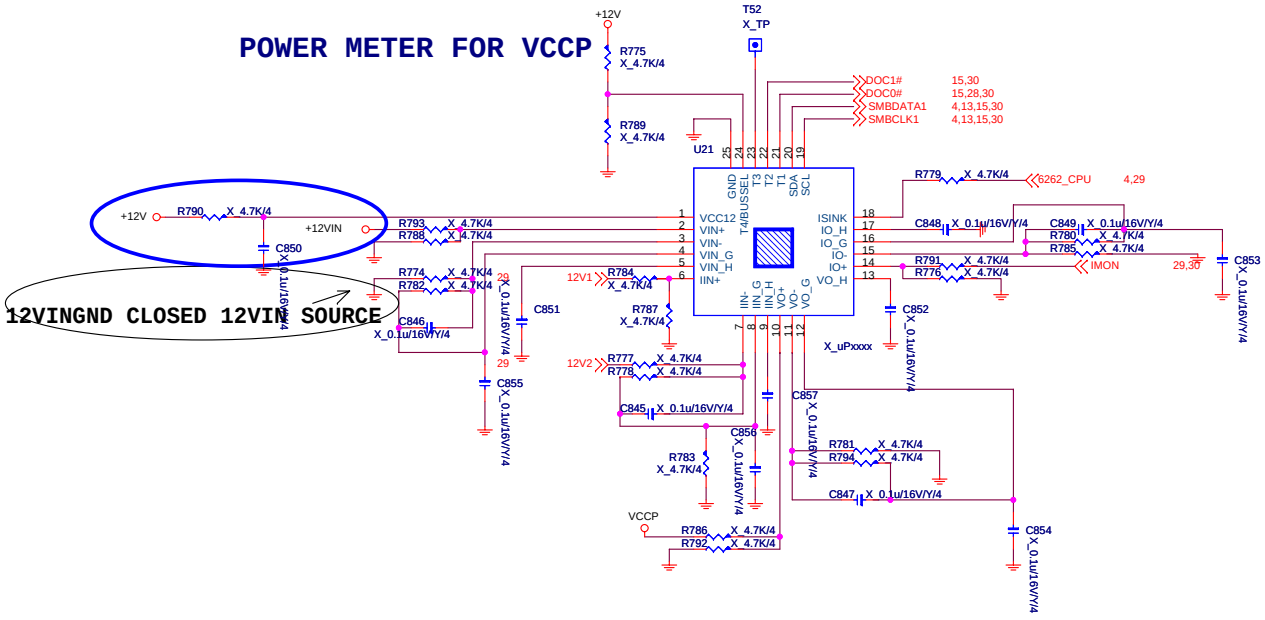
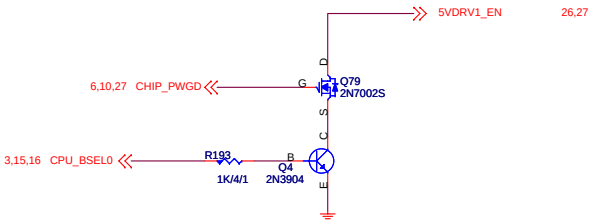
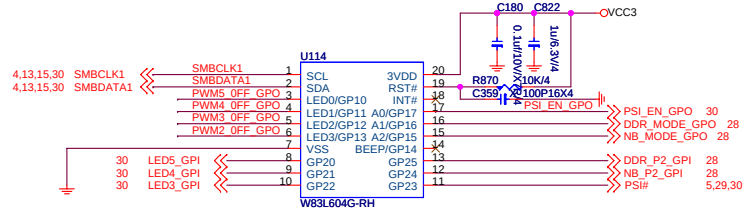
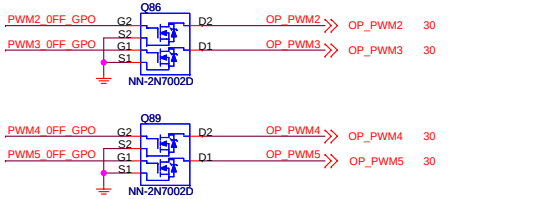
POWER METER FOR VCCP

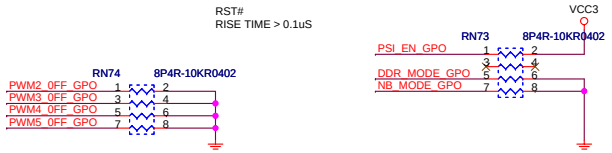


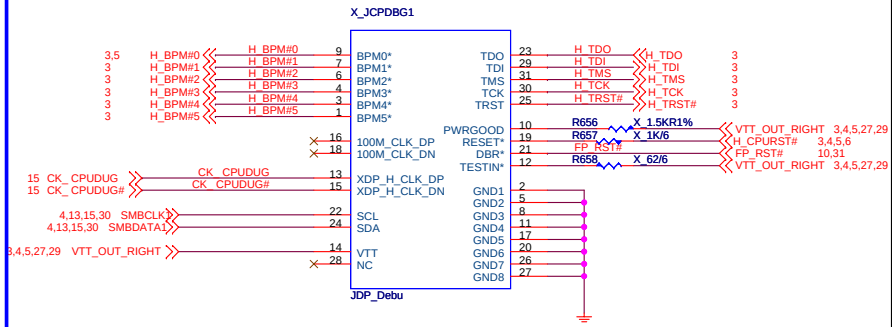
防測試線路











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