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Intel LGA775 CPU - Power	4
Intel LGA775 CPU - GND	5
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ICH8	10-12
DDR2 DIMM 1 , 2 , 3 & 4	13~15
Clock Gen ICS9LPRS512	16
W83627DHG / LPC	17
PS2 / LPT / COM Port	18
SATA / RTC / FAN Control	19
LAN - INTEL 82562V	20
Azalia Codec (ALC888)	21
PCIE X16 & X1 SLOT	22
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MS-7315 P1 uATX Version: 0.A (Dalas)

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

System Chipset:

Intel Broadwater-P (North Bridge)
Intel ICH8DH (South Bridge)

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC888
LPC Super I/O -- W83627DHG /EHG(Ver:H)
LAN -- INTEL 82562V (10/100)
CLOCK Gen -- ICS 9LPRS512 (56pin)
1394 Controller -- VT6307 / VT6308 (2-port)
Hi-USB to PATA Bridge -- CY7C68300C-56PVXC (SSOP-56)

Main Memory:

Dual-channel DDR-II * 4 (Max 4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)
Driver: Intersil ISL6612

			BOM
A	BW-965P/ICH8DH/W83627EHG/ALC888/82562V/USB to IDE	cfg-A	

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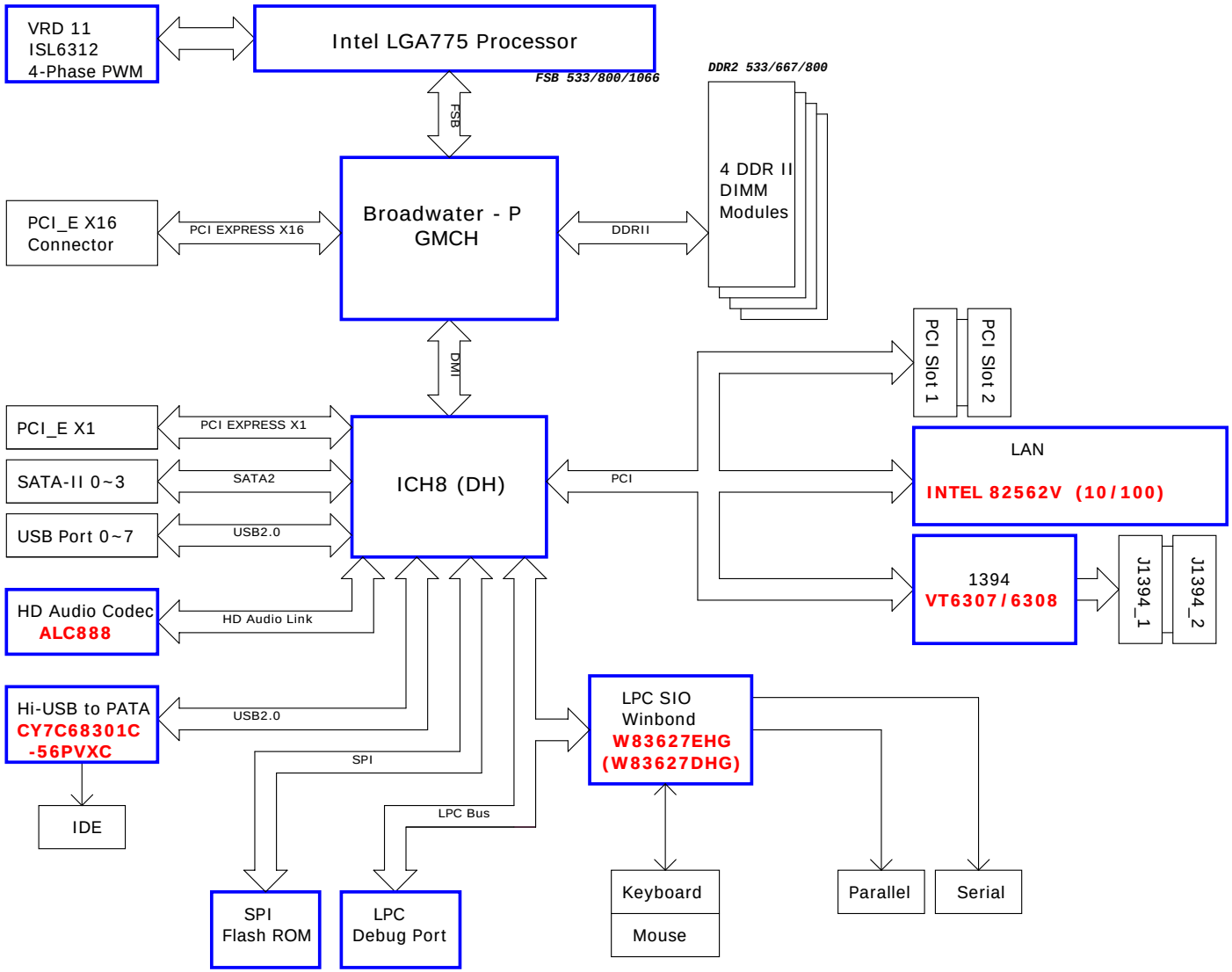
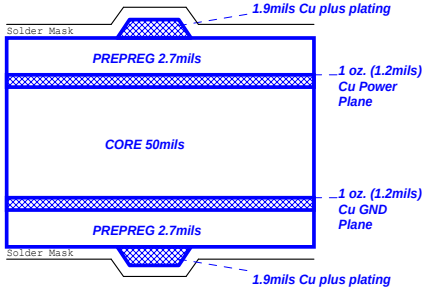
Block Diagram



Board Stack-up

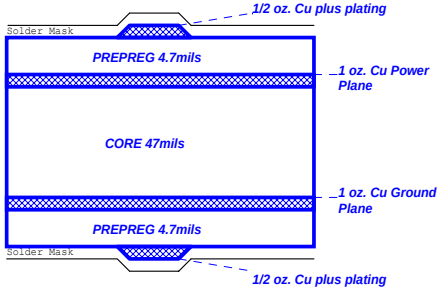
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
IEEE1394 - 110ohm Top : 5/7/5
PCIE, LAN, SATA - 100ohm Top : 5/6/5
USB2.0 - 90ohm Top : 7.5/7.5/7.5

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	MS-7315	
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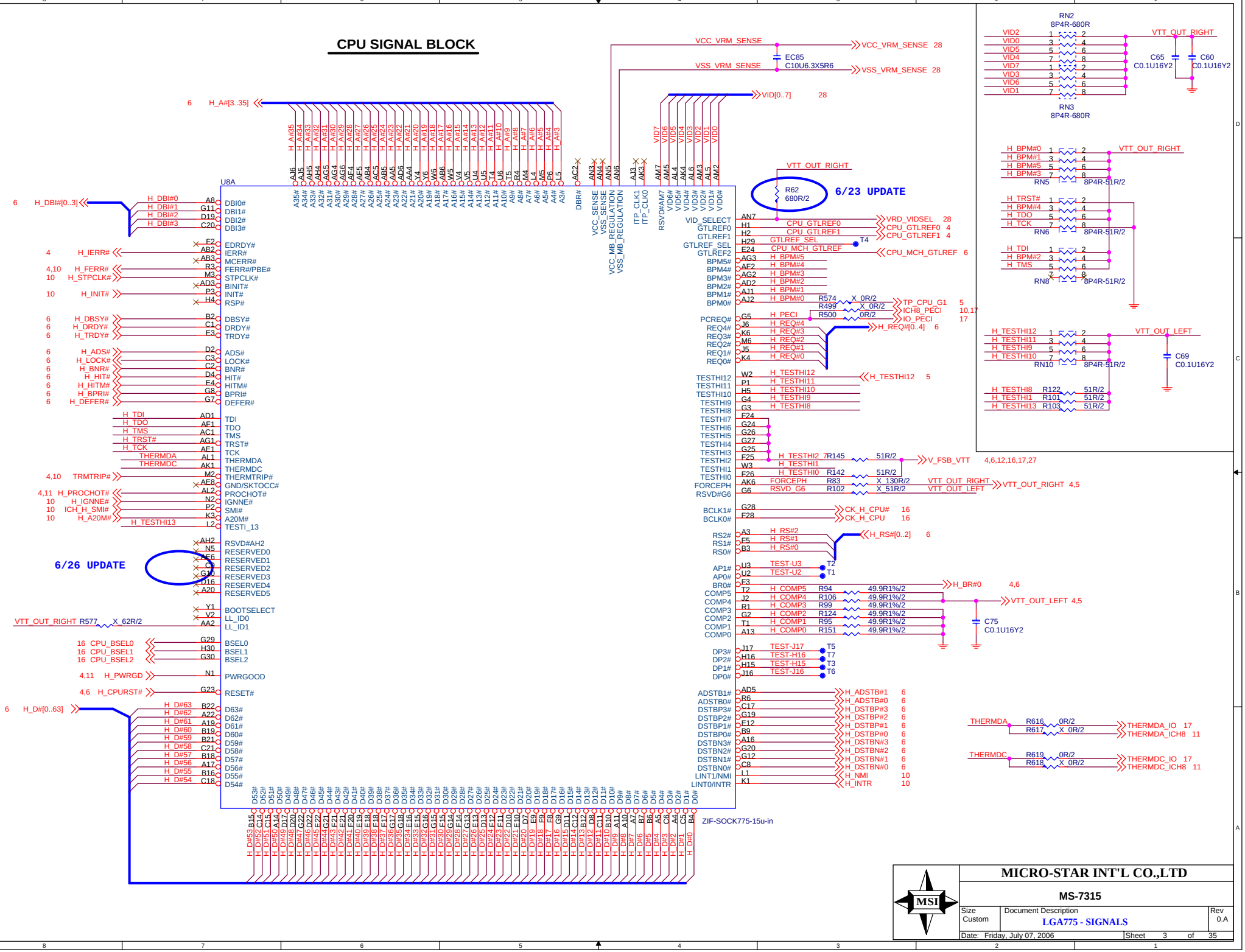
CPU SIGNAL BLOCK



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Custom	LGA775 - SIGNALS	0.A

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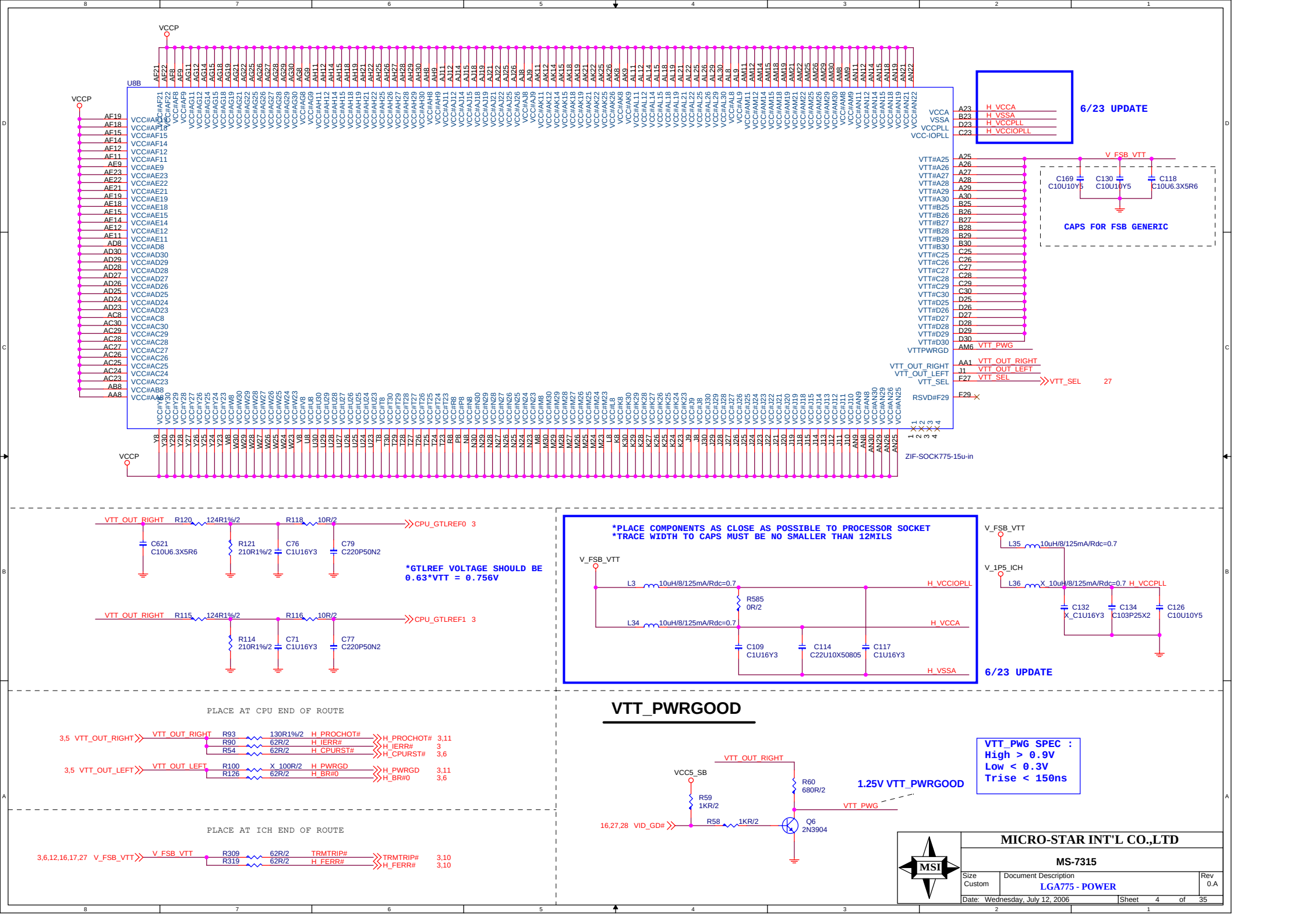
VCCP
U8B
ZIF-SOCK775-15u-in
6/23 UPDATE
H_VCCA
H_VSSA
H_VCCPLL
H_VCCIOPLL
V_FSB_VTT
C169 C10U10Y5
C130 C10U10Y5
C118 C10U6.3X5R6
CAPS FOR FSB GENERIC
VTT_PWG
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
RSVD#F29
VTT_SEL 27
VTT_OUT_RIGHT R120 124R1%/2 R118 10R/2 CPU_GTLREF0 3
C621 C10U6.3X5R6
R121 210R1%/2
C76 C1U16Y3
C79 C220P50N2
*GTLREF VOLTAGE SHOULD BE 0.63*VTT = 0.756V
VTT_OUT_RIGHT R115 124R1%/2 R116 10R/2 CPU_GTLREF1 3
R114 210R1%/2
C71 C1U16Y3
C77 C220P50N2
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
V_FSB_VTT
L3 10uH/8/125mA/Rdc=0.7
H_VCCIOPLL
R585 0R/2
L34 10uH/8/125mA/Rdc=0.7
H_VCCA
C109 C1U16Y3
C114 C22U10X50805
C117 C1U16Y3
H_VSSA
V_FSB_VTT
L35 10uH/8/125mA/Rdc=0.7
V_1P5_ICH
L36 X_10uH/8/125mA/Rdc=0.7
H_VCCPLL
C132 X_C1U16Y3
C134 C103P25X2
C126 C10U10Y5
6/23 UPDATE
PLACE AT CPU END OF ROUTE
3,5 VTT_OUT_RIGHT
VTT_OUT_RIGHT R93 130R1%/2 H_PROCHOT# H_PROCHOT# 3,11
R90 62R/2 H_IERR# H_IERR# 3
R54 62R/2 H_CPURST# H_CPURST# 3,6
3,5 VTT_OUT_LEFT
VTT_OUT_LEFT R100 X_100R/2 H_PWRGD H_PWRGD 3,11
R126 62R/2 H_BR#0 H_BR#0 3,6
PLACE AT ICH END OF ROUTE
3,6,12,16,17,27 V_FSB_VTT
V_FSB_VTT R309 62R/2 TRMTRIP# TRMTRIP# 3,10
R319 62R/2 H_FERR# H_FERR# 3,10
VTT_PWRGOOD
VTT_OUT_RIGHT
VCC5_SB
R59 1KR/2
R60 680R/2
1.25V VTT_PWRGOOD
VTT_PWG
16,27,28 VID_GD#
R58 1KR/2
Q6 2N3904
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
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Document Description
LGA775 - POWER
Rev 0.A
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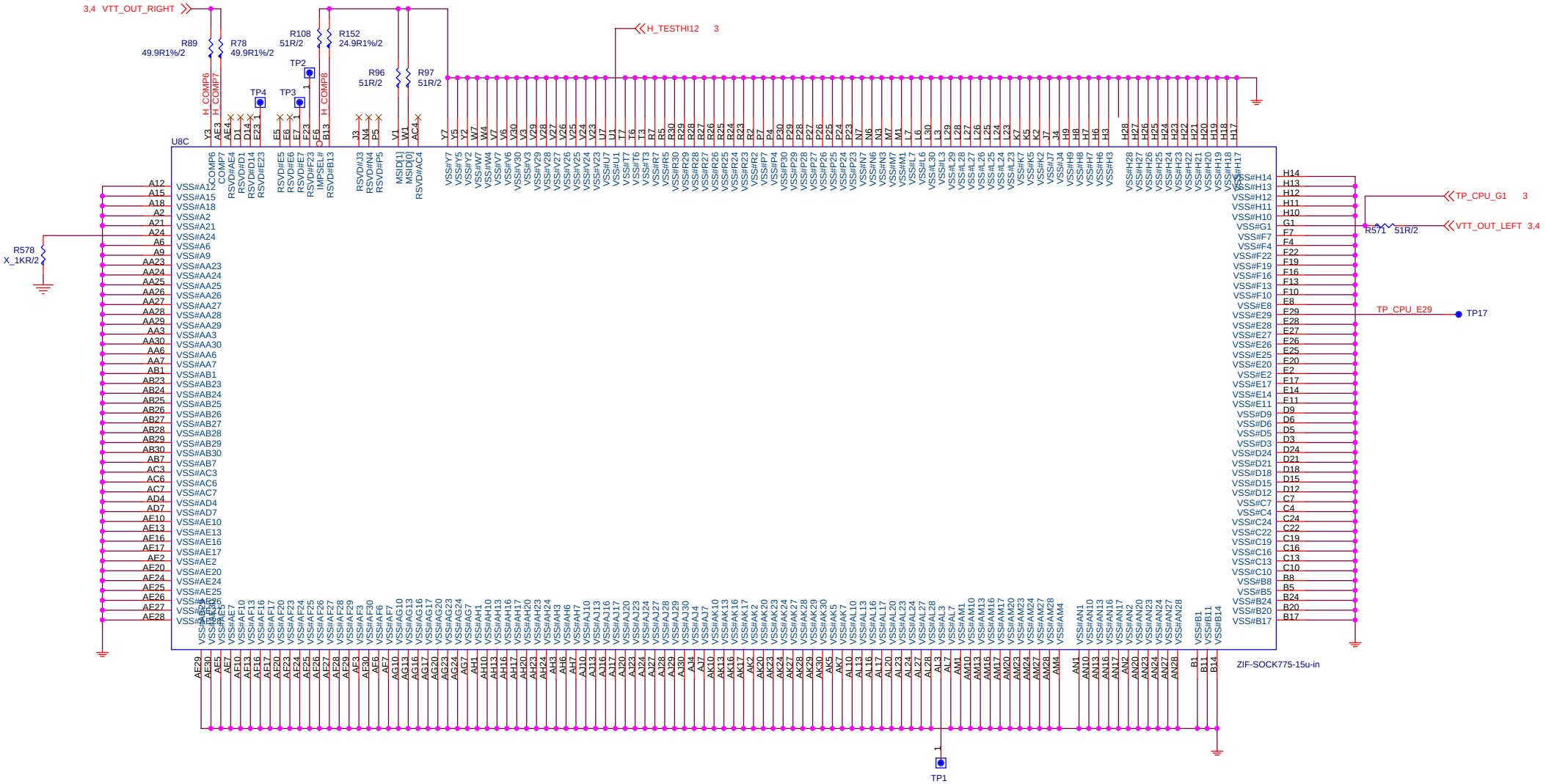
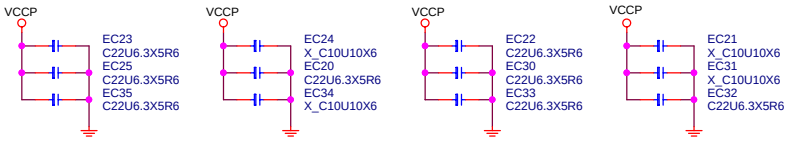


CPU DECOUPLING CAPACITORS



Place these caps within socket cavity

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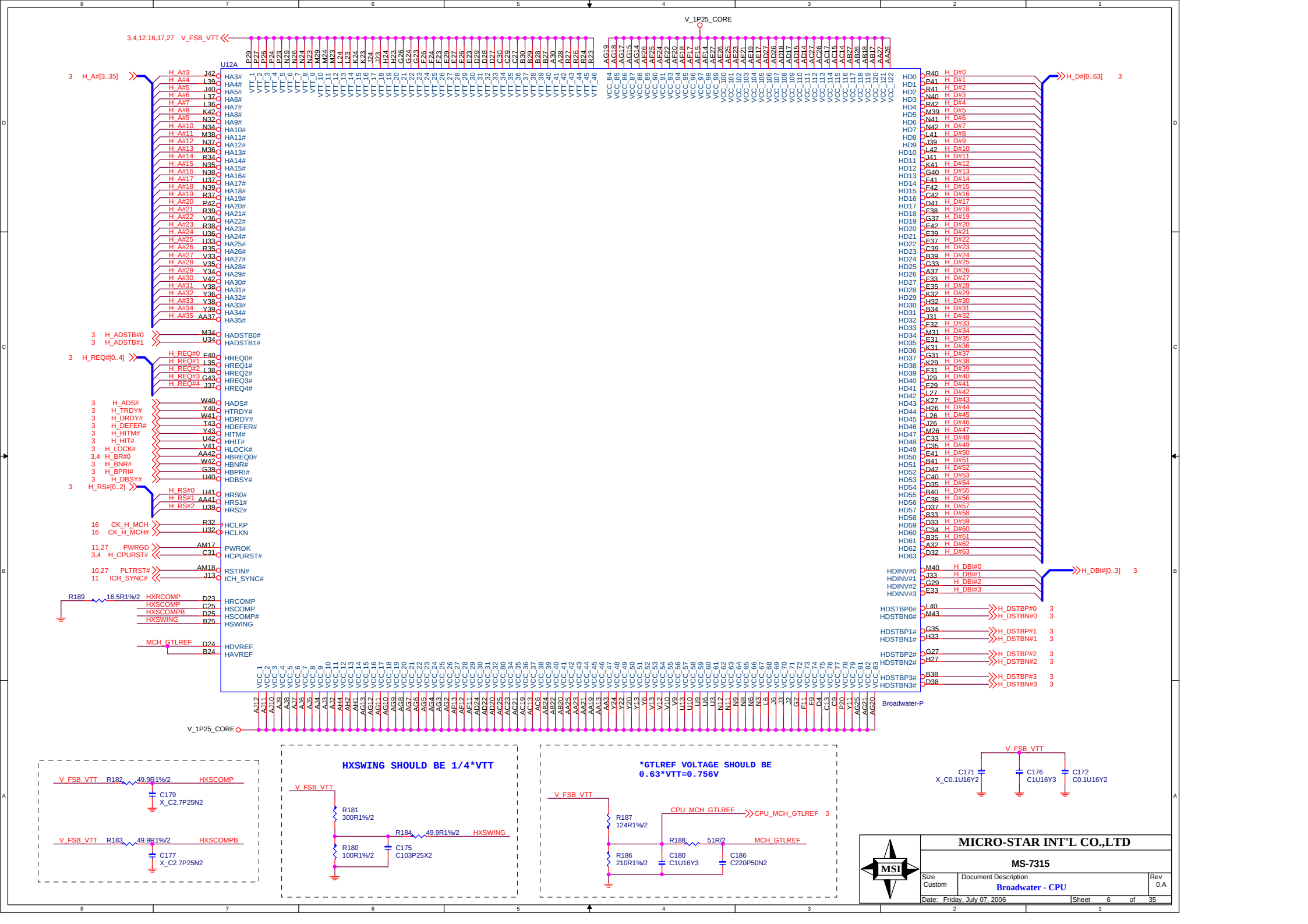
V_1P25_CORE
3,4,12,16,17,27 V_FSB_VTT
U12A
3 H_A#[3..35]
H_A#3 J42
H_A#4 L39
H_A#5 J40
H_A#6 L37
H_A#7 L36
H_A#8 K42
H_A#9 N32
H_A#10 N34
H_A#11 M38
H_A#12 N37
H_A#13 M36
H_A#14 R34
H_A#15 N35
H_A#16 N38
H_A#17 U37
H_A#18 N39
H_A#19 R37
H_A#20 P42
H_A#21 R39
H_A#22 V36
H_A#23 R38
H_A#24 U36
H_A#25 U33
H_A#26 R35
H_A#27 V33
H_A#28 V35
H_A#29 Y34
H_A#30 V42
H_A#31 V38
H_A#32 Y36
H_A#33 Y38
H_A#34 Y39
H_A#35 AA37
HA3# HA4# HA5# HA6# HA7# HA8# HA9# HA10# HA11# HA12# HA13# HA14# HA15# HA16# HA17# HA18# HA19# HA20# HA21# HA22# HA23# HA24# HA25# HA26# HA27# HA28# HA29# HA30# HA31# HA32# HA33# HA34# HA35#
3 H_ADSTB#0 M34 HADSTB0#
3 H_ADSTB#1 U34 HADSTB1#
3 H_REQ#[0..4]
H_REQ#0 F40 HREQ0#
H_REQ#1 L35 HREQ1#
H_REQ#2 L38 HREQ2#
H_REQ#3 G43 HREQ3#
H_REQ#4 J37 HREQ4#
3 H_ADS# W40 HADS#
3 H_TRDY# Y40 HTRDY#
3 H_DRDY# W41 HDRDY#
3 H_DEFER# T43 HDEFER#
3 H_HITM# Y43 HITM#
3 H_HIT# U42 HHIT#
3 H_LOCK# V41 HLOCK#
3,4 H_BR#0 AA42 HBREQ0#
3 H_BNR# W42 HBNR#
3 H_BPRI# G39 HBPRI#
3 H_DBSY# U40 HDBSY#
3 H_RS#[0..2]
H_RS#0 U41 HRS0#
H_RS#1 AA41 HRS1#
H_RS#2 U39 HRS2#
16 CK_H_MCH R32 HCLKP
16 CK_H_MCH# U32 HCLKN
11,27 PWRGD AM17 PWROK
3,4 H_CPURST# C31 HCPURST#
10,27 PLTRST# AM18 RSTIN#
11 ICH_SYNC# J13 ICH_SYNC#
R189 16.5R1%/2 HXRCOMP D23 HRCOMP
HXSCOMP C25 HSCOMP
HXSCOMPB D25 HSCOMP#
HXSWING B25 HSWING
MCH_GTLREF D24 HDVREF
B24 HAVREF
V_1P25_CORE
HD0 R40 H_D#0
HD1 P41 H_D#1
HD2 R41 H_D#2
HD3 N40 H_D#3
HD4 R42 H_D#4
HD5 M39 H_D#5
HD6 N41 H_D#6
HD7 N42 H_D#7
HD8 L41 H_D#8
HD9 J39 H_D#9
HD10 L42 H_D#10
HD11 J41 H_D#11
HD12 K41 H_D#12
HD13 G40 H_D#13
HD14 F41 H_D#14
HD15 F42 H_D#15
HD16 C42 H_D#16
HD17 D41 H_D#17
HD18 E38 H_D#18
HD19 G37 H_D#19
HD20 E42 H_D#20
HD21 E39 H_D#21
HD22 E37 H_D#22
HD23 C39 H_D#23
HD24 B39 H_D#24
HD25 G33 H_D#25
HD26 A37 H_D#26
HD27 E33 H_D#27
HD28 E35 H_D#28
HD29 K32 H_D#29
HD30 H32 H_D#30
HD31 B34 H_D#31
HD32 J31 H_D#32
HD33 F32 H_D#33
HD34 M31 H_D#34
HD35 E31 H_D#35
HD36 K31 H_D#36
HD37 G31 H_D#37
HD38 K29 H_D#38
HD39 E31 H_D#39
HD40 J29 H_D#40
HD41 F29 H_D#41
HD42 L27 H_D#42
HD43 K27 H_D#43
HD44 H26 H_D#44
HD45 L26 H_D#45
HD46 J26 H_D#46
HD47 M26 H_D#47
HD48 C33 H_D#48
HD49 C35 H_D#49
HD50 E41 H_D#50
HD51 B41 H_D#51
HD52 D42 H_D#52
HD53 C40 H_D#53
HD54 D35 H_D#54
HD55 B40 H_D#55
HD56 C38 H_D#56
HD57 D37 H_D#57
HD58 B33 H_D#58
HD59 D33 H_D#59
HD60 C34 H_D#60
HD61 B35 H_D#61
HD62 A32 H_D#62
HD63 D32 H_D#63
H_D#[0..63] 3
HDINV#0 M40 H_DBI#0
HDINV#1 J33 H_DBI#1
HDINV#2 G29 H_DBI#2
HDINV#3 E33 H_DBI#3
H_DBI#[0..3] 3
HDSTBP0# L40 H_DSTBP#0 3
HDSTBN0# M43 H_DSTBN#0 3
HDSTBP1# G35 H_DSTBP#1 3
HDSTBN1# H33 H_DSTBN#1 3
HDSTBP2# G27 H_DSTBP#2 3
HDSTBN2# H27 H_DSTBN#2 3
HDSTBP3# B38 H_DSTBP#3 3
HDSTBN3# D38 H_DSTBN#3 3
Broadwater-P
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_80 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_81 VCC_82 VCC_83
V_1P25_CORE
V_FSB_VTT R182 49.9R1%/2 HXSCOMP
C179 X_C2.7P25N2
V_FSB_VTT R183 49.9R1%/2 HXSCOMPB
C177 X_C2.7P25N2
HXSWING SHOULD BE 1/4*VTT
V_FSB_VTT
R181 300R1%/2
R184 49.9R1%/2 HXSWING
R180 100R1%/2
C175 C103P25X2
*GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
V_FSB_VTT
R187 124R1%/2
CPU_MCH_GTLREF
CPU_MCH_GTLREF 3
R188 51R/2 MCH_GTLREF
R186 210R1%/2
C180 C1U16Y3
C186 C220P50N2
V_FSB_VTT
C171 X_C0.1U16Y2
C176 C1U16Y3
C172 C0.1U16Y2
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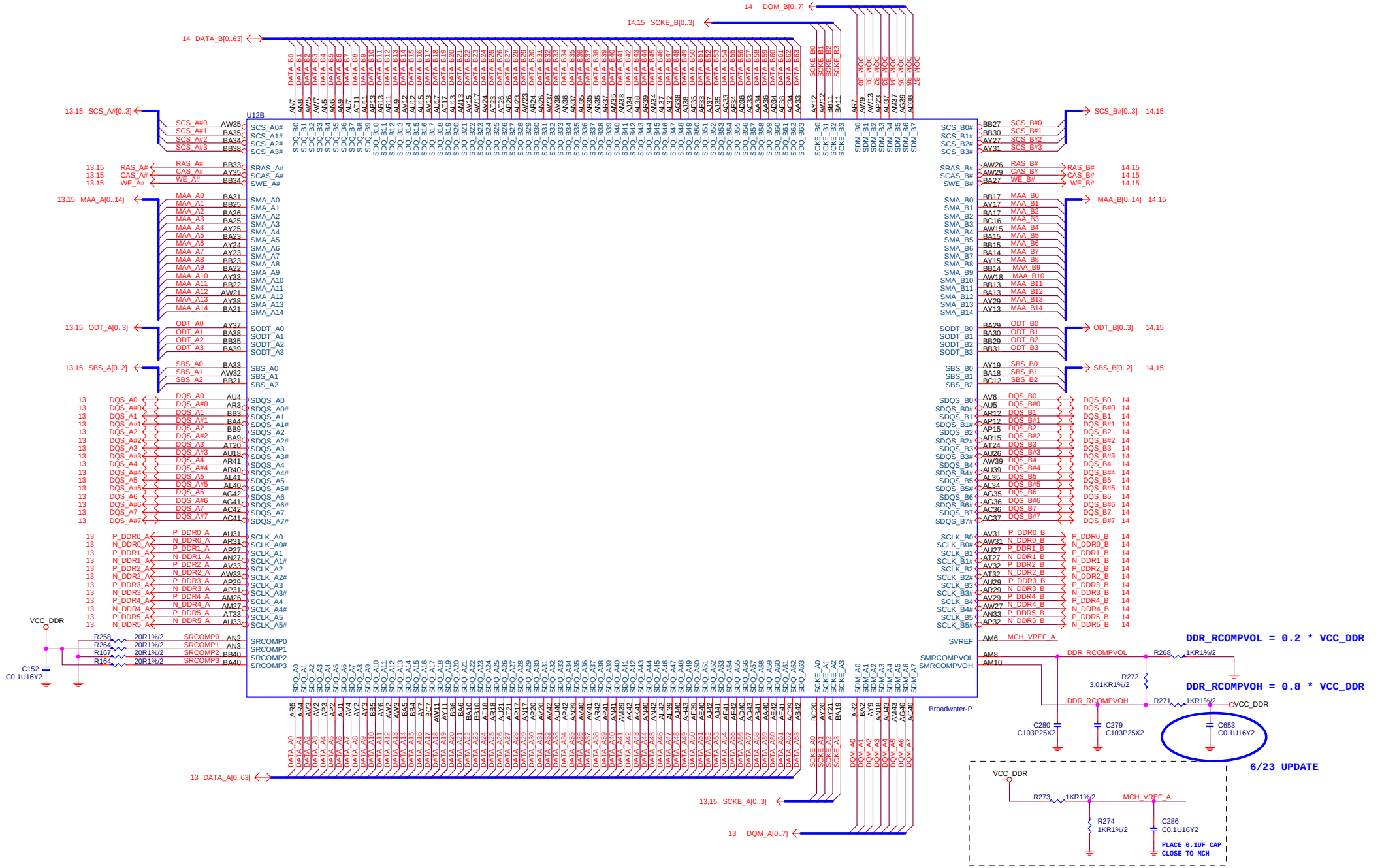

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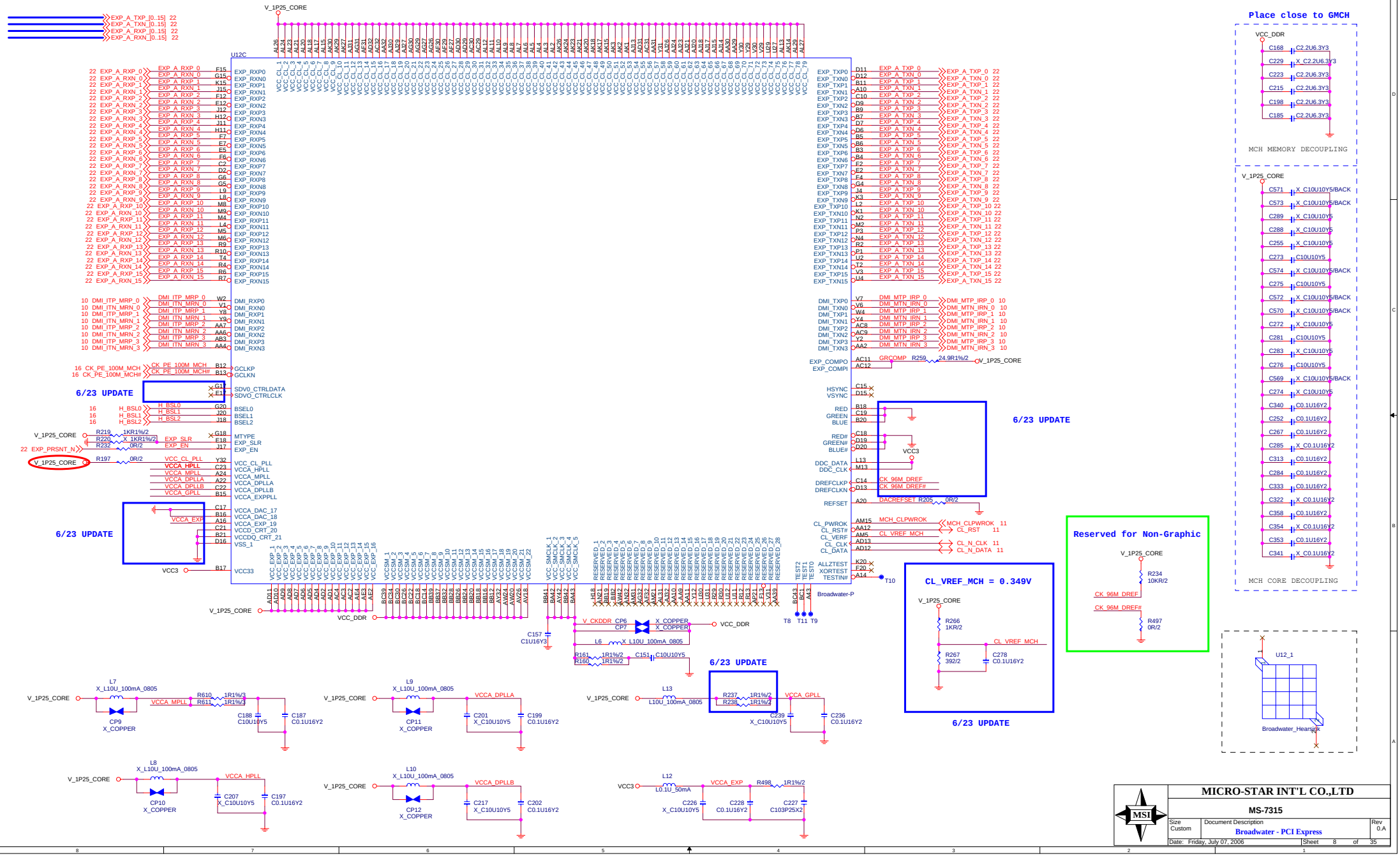
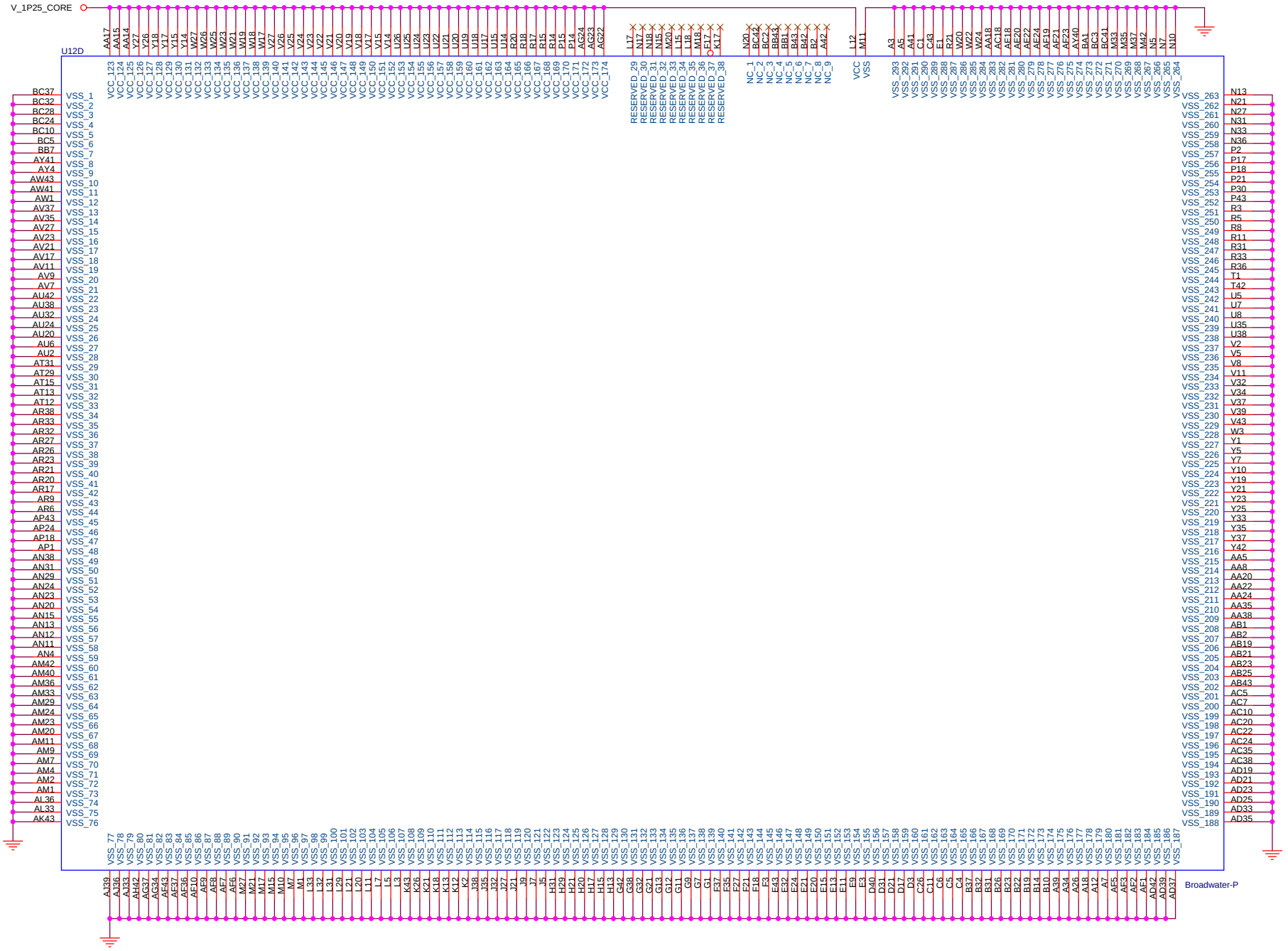

U12C
V_1P25_CORE
EXP_A_TXP_[0..15] 22
EXP_A_TXN_[0..15] 22
EXP_A_RXP_[0..15] 22
EXP_A_RXN_[0..15] 22
6/23 UPDATE
6/23 UPDATE
6/23 UPDATE
6/23 UPDATE
6/23 UPDATE
CL_VREF_MCH = 0.349V
Reserved for Non-Graphic
Place close to GMCH
MCH MEMORY DECOUPLING
MCH CORE DECOUPLING
MICRO-STAR INT'L CO.,LTD
MS-7315
Broadwater - PCI Express
Broadwater_Heatsink



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ICH8 H/W STRAPS

SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERIDE
INTVRMEN/ LAN100_SLP	EN	DIS	INT VRM (VccSus1_05,1_5,VccCL1_5) (VccLAN1_05,VccCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

PGNT#3 R390 X_1KR/2 VCC3_SB

11 ACSDOUT ACSDOUT R384 X_1KR/2

11 ACSYNC ACSYNC R385 X_1KR/2

11,24 SPKR R394 X_1KR/2 VCC3

VCC3 RN42 SATA4GP A20GATE KBRST# SATA5GP 8P4R-10KR/2 SATA4GP 11 SATA5GP 11

BOOT SELECT STRAPS

BOOT DEVICE	GNT0	SPI_CS1#	JBOOT1
FWH	1	1	1-2
SPI	0	X	2-3(Default)
PCI	1	0	1-2 & R380

R343 1KR/2 PGNT#0

R380 X_1KR/2 SPI_CS1#

SPI DEBUG PROT

Place close to SPI ROM

VCC3_SB JSPI1 SPI_MISO_F SPI_CS0_F# SPI_HOLD# SPI_MOSI_F SPI_CLK_F H2X5(10)_black-RH

Part Number : N31-2051451-H06

U24A

23,26 AD[31..0] AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

23,26 C_BE#[3..0] C_BE#0 C_BE#1 C_BE#2 C_BE#3

23,26 DEVSEL# FRAME# IRDY# TRDY# STOP# PAR LOCK# SERR# PERR# PME#

16 ICH_PCLK

23,26 PCIRST_ICH8# R408 33R/2

23 PREQ#0 PREQ#1 PREQ#2 PREQ#3

23,26 PREQ#3

23 PGNT#0 PGNT#1

26 PGNT#3

23 PIRQ#A PIRQ#B PIRQ#C PIRQ#D PIRQ#E PIRQ#F PIRQ#G PIRQ#H

23,26 PIRQ#D

17 SERIRQ

SPI_MOSI_F R344 15R/2 SPI_MOSI

SPI_MISO SPI_CS0#

SPI_CS0_F# R345 15R/2 SPI_CS0#

SPI_CLK_F R379 15R/2 SPI_CLK SPI_CS1#

PCI INTERFACE

ICH 8

PART 1/3

INTERRUPT SPI

CPU

A20M# CPUSLP# FERR# IGNNE# INIT# INIT3_3V# INTR NMI SMI# STPCLK# RCIN# A20GATE THRMTRIP# PECI ICH8_PECI

PLTRST# PLTRST_L R342 33R/2

PCI EXPRESS

PERN_1 PERP_1 PETN_1 PETP_1 PE_RXN1 PE_RXP1 PE_TXN1_C C382 C0.1U16V2 PE_TXP1_C C390 C0.1U16V2

PERN_2 PERP_2 PETN_2 PETP_2

PERN_3 PERP_3 PETN_3 PETP_3

PERN_4 PERP_4 PETN_4 PETP_4

PERN_5 PERP_5 PETN_5 PETP_5

PERN_6/GLAN_RXN PERP_6/GLAN_RXP PETN_6/GLAN_TXN PETP_6/GLAN_TXP

DIRECT MEDIA

DMI_0RXN DMI_0RXP DMI_0TXN DMI_0TXP

DMI_1RXN DMI_1RXP DMI_1TXN DMI_1TXP

DMI_2RXN DMI_2RXP DMI_2TXN DMI_2TXP

DMI_3RXN DMI_3RXP DMI_3TXN DMI_3TXP

DMI_CLKN DMI_CLKP

DMICOMPI DMI_IRCOMP

DMI_BIAS R313 24.9R1%/2

<200mils

V_1P5_ICH

LAN

GLAN_CLK LAN_RSTSYNC LAN_RST# LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2

ELAN_CLK ELAN_SYNC LAN_PWROK ELAN_RXD0 ELAN_RXD1 ELAN_RXD2 ELAN_TXD0 ELAN_TXD1 ELAN_TXD2

RN35 VCC3_SB SPI_CS0# SPI_MISO SPI_MOSI X_8P4R-10KR/2

VSS A5 A24 A28 B2 B8 B14 B17 B20 B24 C2 C22 C27 C28 D2 D6 D12 D16 D19 D22 D25 D29 E1 E21 E24 E27 E28 F2 F7 F15 F23 F24 F25 F26 G1 G4 G6 G10 G13 G18

ICH8-DH

LAN_PWROK R474 10KR/2 VCC3_SB

R473 X_0R/2 RSMRST# RSMRST# 11,27

C478 C1U16Y3

SPI FLASH ROM

Place close to SB.

VCC3_SB C399 C0.1U16Y2 R325 1KR/2

U19 CE# VDD SO HOLD# WP# SCK VSS SI SPI-FLASH-W25X80VSSIG

SPI_MISO_R289 15R/2 SPI_MISO_F

11 SPI_WP# From South-Bridge GPIO32

SPI_CS0_F# SPI_WP#

SPI_HOLD# SPI_CLK_F SPI_MOSI_F

R324 X_0R/2 SPI_HOLD_GPO# 11 From South-Bridge GPIO33

VCC3_SB R290 1KR/2

Reserved for BIOS control used

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ICH8 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH8

Trace length is less than 3inchs to ICH8.

SM_LINK0 R588 10KR/2 VCC3_SB
GPIO_10 R586 10KR/2
LINK_ALERT# R587 10KR/2
SM_LINK1 R589 10KR/2

FP_RST# RN38 8P4R-10KR/2
SIO_PME#
RI#
GPIO_9

CLEAR_CMOS# RN34 8P4R-10KR/2
SMB_ALERT#
BATTLOW#
GPIO_14

LPCPD# R412 X_10KR/2 VCC3_SB

WAKE# R359 1KR/2 VCC3_SB

GPIO12 R352 X_10KR/2 VCC3_SB

LDRQ_1# RN41 8P4R-10KR/2 VCC3
SATALED#
SIO_SMI#

SMBCLK R346 2.2KR/2
SMBDATA R351 2.2KR/2

PWRGD R314 10KR/2

INTRUDER# R340 1MR/2 VBAT

LAN100_SLP R538 330KR/2 VBAT
R539 X_330KR/2

VCC3 R375 10KR/2
27,28 VRM_GD R373 0R/2 VRM_PWRGD
R372 X_100KR/2
C444 C0.1U16Y2

SMBDATA_ICH R592 X_0R/2 SM_LINK1
SMBCLK_ICH R593 X_0R/2 SM_LINK0
6/23 UPDATE

R348 X_0R/2 THERM#
VCC3 R357 10KR/2
VCC3 R361 10KR/2
3,4 H_PROCHOT#
Q34 2N3904
Q35 2N3904

#Place near the SB

CL_VREF_ICH = 0.405V
VCC3_SB
R355 3.24KR1%/2
CL_VREF_ICH
R365 453R1%
C429 C0.1U16Y2

U24B

17 LPC_AD0 F6 LAD0
17 LPC_AD1 F5 LAD1
17 LPC_AD2 G9 LAD2
17 LPC_AD3 E5 LAD3
17 LPC_DRQ#0 G8 LDRQ_0#
LDRQ_1# C3 LDRQ_1#/GPIO23
17 LPC_FRAME# LPC_FRAME# B3 LFRAME#
LPC

AC_BITCLK_ICH AE12 ACZ_BCLK
ACRST# AE13 ACZ_RST#
21 AC_SDIN0 AE13 ACZ_SDIN_0
AC14 ACZ_SDIN_1
AH12 ACZ_SDIN_2
AD13 ACZ_SDIN_3
10 ACSDOUT ACSDOUT AH11 ACZ_SDOUT
10 ACSYNC ACSYNC AH10 ACZ_SYNC
AC-LINK

25 USB4- G2 USBP_0N
25 USB4+ G3 USBP_0P
25 USB1- H5 USBP_1N
25 USB1+ H4 USBP_1P
25 USB0- H1 USBP_2N
25 USB0+ H2 USBP_2P
25 USB5- J3 USBP_3N
25 USB5+ J2 USBP_3P
25 USB2- K5 USBP_4N
25 USB2+ K4 USBP_4P
25 USB3- K1 USBP_5N
25 USB3+ K2 USBP_5P
25 USB6- L3 USBP_6N
25 USB6+ L2 USBP_6P
25 USB7- M5 USBP_7N
25 USB7+ M4 USBP_7P
29 USB8- M2 USBP_8N
29 USB8+ M1 USBP_8P
N2 USBP_9N
N3 USBP_9P
USB

25 OC#0 AE15 OC0#
25 OC#1 AH14 OC1#/GPIO40
AG14 OC2#/GPIO41
AG15 OC3#/GPIO42
25 OC#2 AH15 OC4#/GPIO43
AE15 OC5#/GPIO29
25 OC#3 AG13 OC6#/GPIO30
AF14 OC7#/GPIO31
25 OC#4 AD14 OC8#
AG16 OC9#

6/23 UPDATE
R407 22.6R/2 USB_BIAS E1 USBRBIASN
E2 USBRBIASP

13,16,17,22,27,29 SMBCLK R590 33R/2 SMBCLK_ICH AD19 SMBCLK
13,16,17,22,27,29 SMBDATA R591 33R/2 SMBDATA_ICH AB18 SMBDATA
SMB_ALERT# AF21 SMBALERT#/GPIO11
SM_LINK0 AE19 SMLINK0
SM_LINK1 AG21 SMLINK1
LINK_ALERT# AH21 SMLALERT#
SM BUS

10,27 RSMRST# RSMRST# AD22 RSMRST#
17 SB_PWRBTN# A1 PWRBTN#
6,27 PWRGD AE24 PWROK
VRM_PWRGD AC16 VRMPWRGD_VGATE
3,4 H_PWRGD AF25 CPUPWRGD/GPIO49
16 CK_PWRGD F1 CK_PWRGD
24 FP_RST# FP_RST# AF16 SYS_RESET#
17,27 SLP_S3# AF22 SLP_S3#
27 SLP_S4# AH23 SLP_S4#
AC17 SLP_S5#
AG22 SLP_M#
LAN100_SLP AG24 LAN100_SLP
LPCPD# LPCPD# G7 SUS_STAT#/LPCPD#
E4 SUSCLK
POWER MGNT

INTRUDER# AF24 INTRUDER#
22 WAKE# AH18 WAKE#
RI# AG17 RI#
17 THERM# THERM# AH9 THERM#
BATTLOW# AF22 BATLOW#
6 ICH_SYNC# R364 0R/2 AE10 MCH_SYNC#
10,24 SPKR AF6 SPKR
MISC

AE25 DPRSTP#
AD24 DPSLP#
AD16 DFXTESTB

16 ICH_14M AG6 CLK14
16 USB_48M B1 CLK48

RN39 8P4R-22R/2
21 AC_SYNC AC_SYNC ACSYNC
21 AC_SDOUT AC_SDOUT ACSDOUT
21 AC_BITCLK AC_BITCLK AC_BITCLK_ICH
21 AC_RST# AC_RST# ACRST#
C454 X_C20P50N2
C452 X_C20P50N2

VSS_041 G24
VSS_042 G27
VSS_043 G28
VSS_044 H3
VSS_045 H7
VSS_046 H23
VSS_047 H24
VSS_048 H25
VSS_049 H26
VSS_050 J1
VSS_051 J4
VSS_052 J5
VSS_053 J7
VSS_054 J23
VSS_055 K3
VSS_056 K6
VSS_057 K7
VSS_058 K25
VSS_059 K26
VSS_060 L1
VSS_061 L4
VSS_062 L5
VSS_063 L13
VSS_064 L15
VSS_065 L27
VSS_066 L28
VSS_067 M3
VSS_068 M12
VSS_069 M13
VSS_070 M14
VSS_071 M15
VSS_072 M16
VSS_073 M17
VSS_074 M22
VSS_075 M25
VSS_076 M26
VSS_077 N1
VSS_078 N4
VSS_079 N5
VSS_080 N11
VSS_081 N12
VSS_082 N13
VSS_083 N14
VSS_084 N15
VSS_085
ICH8-DH

ICH 8
PART 2/3

SATA_0RXN AC5 SATA_RX#0 19
SATA_0RXP AC4 SATA_RX0 19
SATA_0TXN AE4 SATA_TX#0 19
SATA_0TXP AE3 SATA_TX0 19
SATA_1RXN AF1 SATA_RX#1 19
SATA_1RXP AE2 SATA_RX1 19
SATA_1TXN AH2 SATA_TX#1 19
SATA_1TXP AH1 SATA_TX1 19
SATA_2RXN W5
SATA_2RXP W4
SATA_2TXN AA3
SATA_2TXP AA4
SATA_3RXN AB1
SATA_3RXP AB2
SATA_3TXN AD2
SATA_3TXP AD1
SATA_4RXN Y1 SATA_RX#4 19
SATA_4RXP Y2 SATA_RX4 19
SATA_4TXN U3 SATA_TX#4 19
SATA_4TXP U4 SATA_TX4 19
SATA_5RXN T1 SATA_RX#5 19
SATA_5RXP T2 SATA_RX5 19
SATA_5TXN V2 SATA_TX#5 19
SATA_5TXP V1 SATA_TX5 19
SATA_CLKN AG3 CK_ICHSATA# 16
SATA_CLKP AG4 CK_ICHSATA 16
SATARBIASN R2
SATABIASP R1
SATALED# AB10 SATALED# 24
S-ATA

SATA0GP/GPIO21 AB11 GPIO_21
SATA1GP/GPIO19 AD8 GPIO_19
SATA2GP/GPIO36 AE8 GPIO_36
SATA3GP/GPIO37 AD9 GPIO_37
SATA4GP AD10 SATA4GP SATA4GP 10
SATA5GP AE9 SATA5GP SATA5GP 10

BMBUSY#/PMSYNC#/GPIO0 AE9 SIO_SMI#
GPIO8 AE16 SIO_PME# SIO_PME# 17
GLGP1O3/GPIO9 AG18 GPIO_9
GLGPIO1/GPIO10 AF20 GPIO_10
GP12 AC19 GPIO12 R227 X_0R/2 ATADET0 29
GPIO13 AF18 CLEAR_CMOS#
CLGPIO2/GPIO14 AH24 GPIO_14
GPIO15 AE21 PHY_DIS# 20
GPIO16 AE11
GPIO18 AC11
GPIO20 AG8
CLGPIO0/GPIO24 AG24 R598 X_0R/2
GPIO25 AH11 R599 X_0R/2
S4_STATE#/GPIO26 AH25 PWR_LED 24,27
QRT_STATE0/GPIO27 AD20 SUS_LED 24,27
QRT_STATE1/GPIO28 AD15 PHY_DIS# PHY_DIS# 20
GPIO32 AH7 SPI_WP# SPI_WP# 10
GPIO33 AG7 SPI_HOLD_GPO# SPI_HOLD_GPO# 10
GPIO34 AG12
SATACLKREQ#/GPIO35 AD12
SCLOCK/GPIO22 AE7 GPIO_22
SLOAD/GPIO38 AH6 GPIO_38
SDATAOUT0/GPIO39 AC10 GPIO_39
SDATAOUT1/GPIO48 AE7 GPIO_48
GPIO

FOR Quick Resume Technology

RN47
SFAN_TACH 2 1
GPIO_21 4 3
CFAN_TACH 6 5
GPIO_7 8 7
8P4R-10KR/2

RN46
GPIO_6 1 5 5
GPIO_19 2
GPIO_22 3
GPIO_48 4
GPIO_38 6
GPIO_37 7
GPIO_39 8
GPIO_36 9 9 10 10
10P8R-10KR

C407 C0.1U16Y2
VCCRTC AG26
INTVRMEN AA2 INTVRMEN R339 330KR/2 VBAT
RTCRST# AD21 RTC_RST# RTC_RST# 19
RTCX1 AH26 RTCX1
RTCX2 AH27 RTCX2
RTC

Enable internal 2.5V VRM

C391 C18P50N3
Y5 32.768KHz
R326 10MR
C402 C18P50N3

GLAN_COMPO C24
GLAN_COMPI D24
CL_CLK0 F21 CL_N_CLK 8
CL_CLK1 AH20
CL_DATA0 G21 CL_N_DATA 8
CL_DATA1 AE18
CL_VREF0 B21 CL_VREF_ICH R265 0R/2 PWRGD 6,27
CL_VREF1 AG20
CL_PWROK C2 MCH_CLPWROK MCH_CLPWROK 8
CL_RST# AG19 CL_RST 8
AMT

Open Drain Output

FAN_PWM0 AB6 ASFC_PWM0 19
FAN_PWM1 AD6 ASFC_PWM1 19
FAN_PWM2 AB8
TACH0/GPIO17 AC7 CFAN_TACH CFAN_TACH 19
TACH1/GPIO1 AF5 SFAN_TACH SFAN_TACH 19
TACH2/GPIO6 AE6 GPIO_6
TACH3/GPIO7 AC8 GPIO_7
AFSC

ASFC_PWM0 R366 2.2KR/2
ASFC_PWM1 R402 2.2KR/2

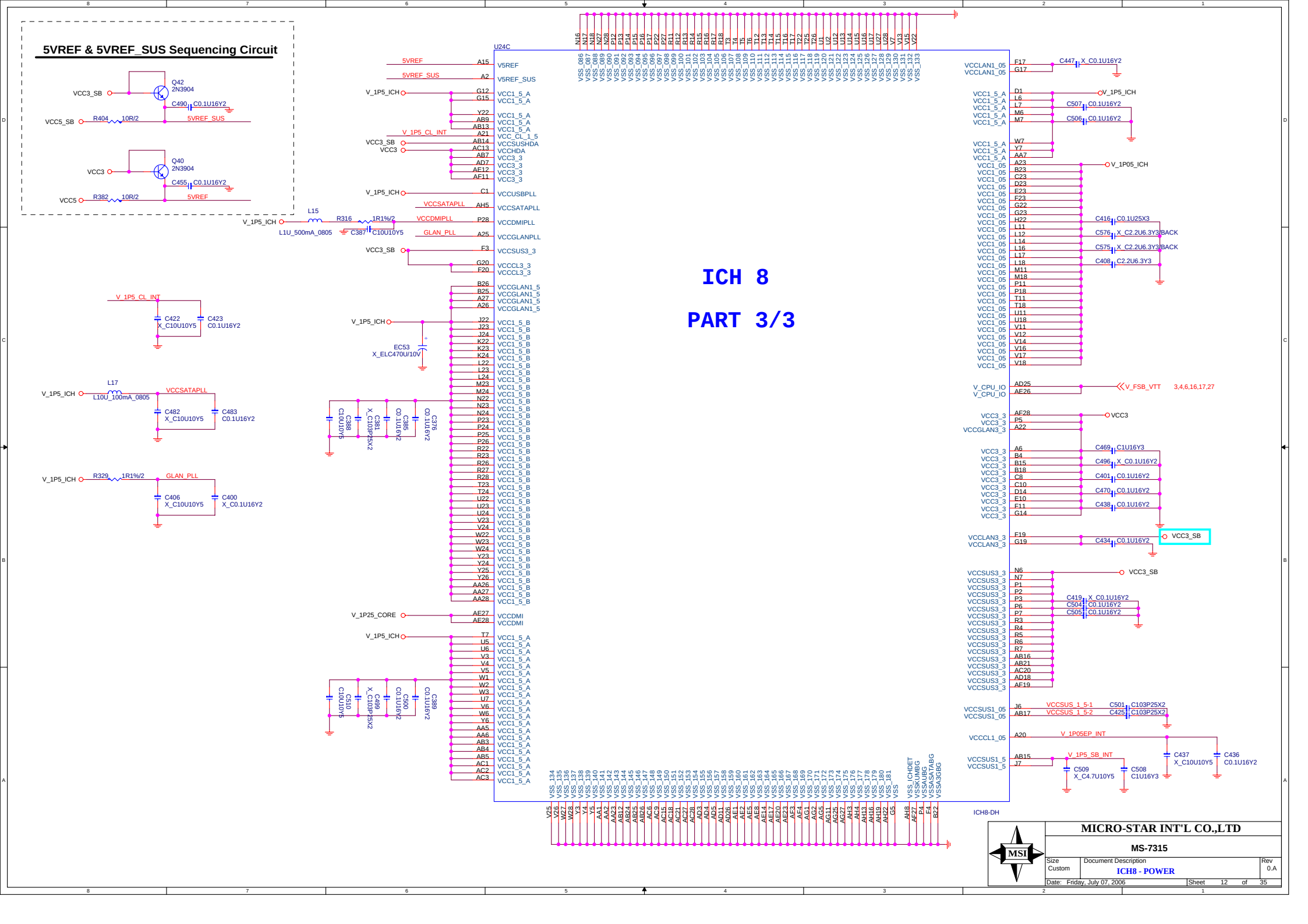
SSTCTL AD17 IO_SST 17

Address:00x48

U31
SST VCC
ADD0 GND
RES D1+
ADD1 D1-
D2- D2+
3 THERMDC_ICH8
THERMDA_ICH8 3
X_ATD7486 X_C654 C100P50N2

VCC3

MICRO-STAR INT'L CO.,LTD		
MS-7315		
Size: Custom	Document Description: ICH8 - LPC, SATA, USB, GPIO	Rev: 0.A
Date: Friday, July 07, 2006	Sheet 11 of 35	


5VREF & 5VREF_SUS Sequencing Circuit
Q42
2N3904
VCC3_SB
C490
C0.1U16Y2
VCC5_SB
R404
10R/2
5VREF_SUS
Q40
2N3904
VCC3
C455
C0.1U16Y2
VCC5
R382
10R/2
5VREF
U24C
5VREF
5VREF_SUS
V_1P5_ICH
V_1P5_CL_INT
VCC3_SB
VCC3
VCCSATAPLL
VCCDMIPLL
GLAN_PLL
L15
L1U_500mA_0805
R316
1R1%/2
C387
C10U10Y5
V5REF
V5REF_SUS
VCC1_5_A
VCC_CL_1_5
VCCSUSHDA
VCCHDA
VCC3_3
VCCUSBPLL
VCCSATAPLL
VCCDMIPLL
VCCGLANPLL
VCCSUS3_3
VCCCL3_3
VCCGLAN1_5
VCC1_5_B
EC53
X_ELC470U/10V
C422
X_C10U10Y5
C423
C0.1U16Y2
L17
L10U_100mA_0805
C482
X_C10U10Y5
C483
C0.1U16Y2
R329
1R1%/2
C406
X_C10U10Y5
C400
X_C0.1U16Y2
C388
C10U10Y5
C381
X_C103P25X2
C385
C0.1U16Y2
C376
C0.1U16Y2
C510
C10U10Y5
C499
X_C103P25X2
C500
C0.1U16Y2
C389
C0.1U16Y2
V_1P25_CORE
VCCDMI
ICH 8
PART 3/3
VSS
VCCLAN1_05
VCC1_5_A
VCC1_05
V_1P5_ICH
V_1P05_ICH
C447
X_C0.1U16Y2
C507
C506
C0.1U16Y2
C416
C0.1U25X3
C576
X_C2.2U6.3Y3_BACK
C575
C408
C2.2U6.3Y3
V_CPU_IO
V_FSB_VTT
3,4,6,16,17,27
VCC3_3
VCC3
VCCGLAN3_3
C469
C1U16Y3
C496
X_C0.1U16Y2
C401
C470
C438
VCCLAN3_3
C434
VCC3_SB
VCCSUS3_3
C419
X_C0.1U16Y2
C504
C505
VCCSUS_1_5-1
VCCSUS_1_5-2
C501
C425
C103P25X2
VCCSUS1_05
VCCCL1_05
V_1P05EP_INT
VCCSUS1_5
V_1P5_SB_INT
C509
X_C4.7U10Y5
C508
C1U16Y3
C437
X_C10U10Y5
C436
C0.1U16Y2
ICH8-DH
MICRO-STAR INT'L CO.,LTD
MS-7315
Size
Custom
Document Description
ICH8 - POWER
Rev
0.A
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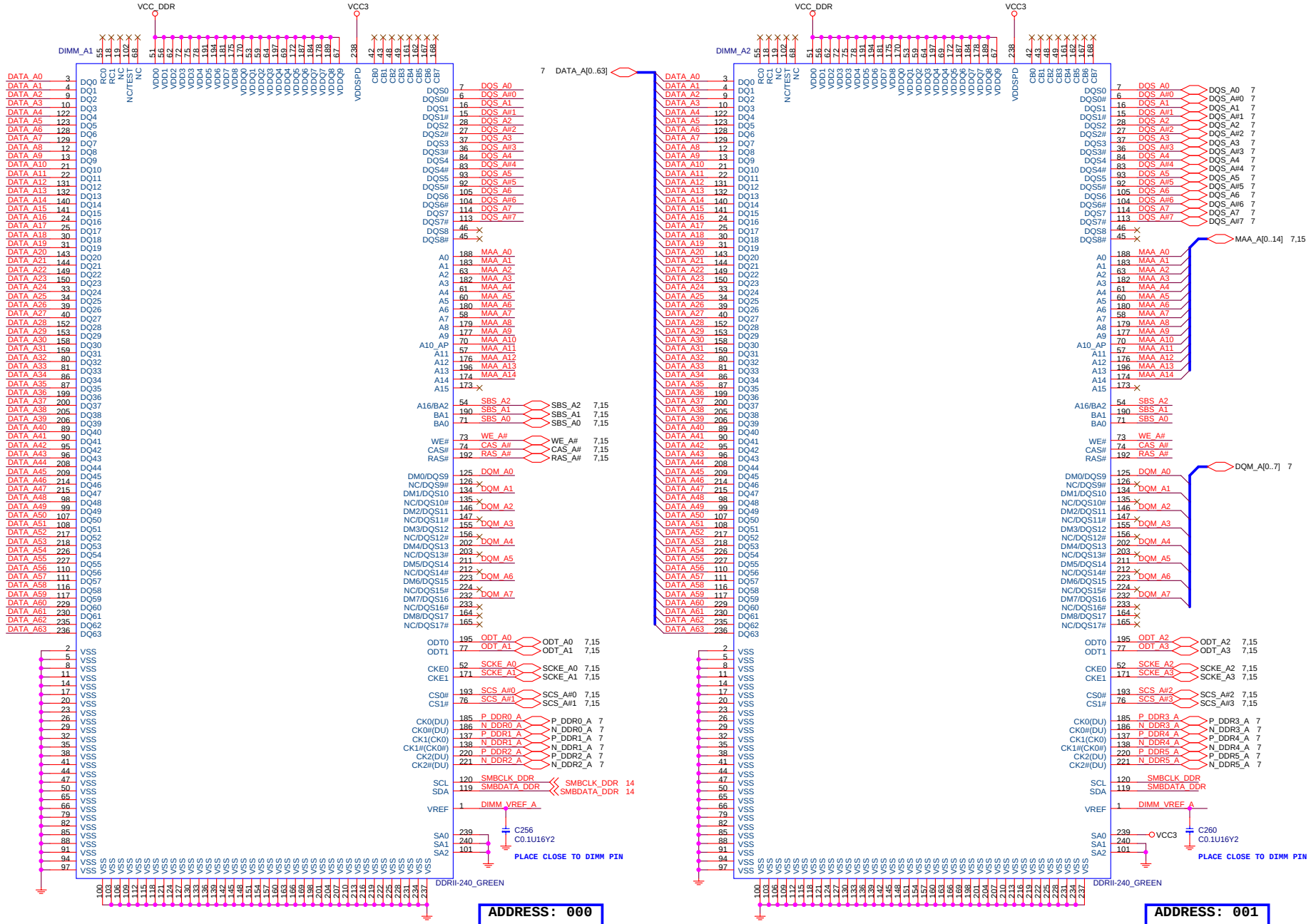
Sheet 12 of 35



MICRO-STAR INT'L CO.,LTD	
MS-7315	
Size: Custom	Document Description: DDR II DIMM 1 & 2
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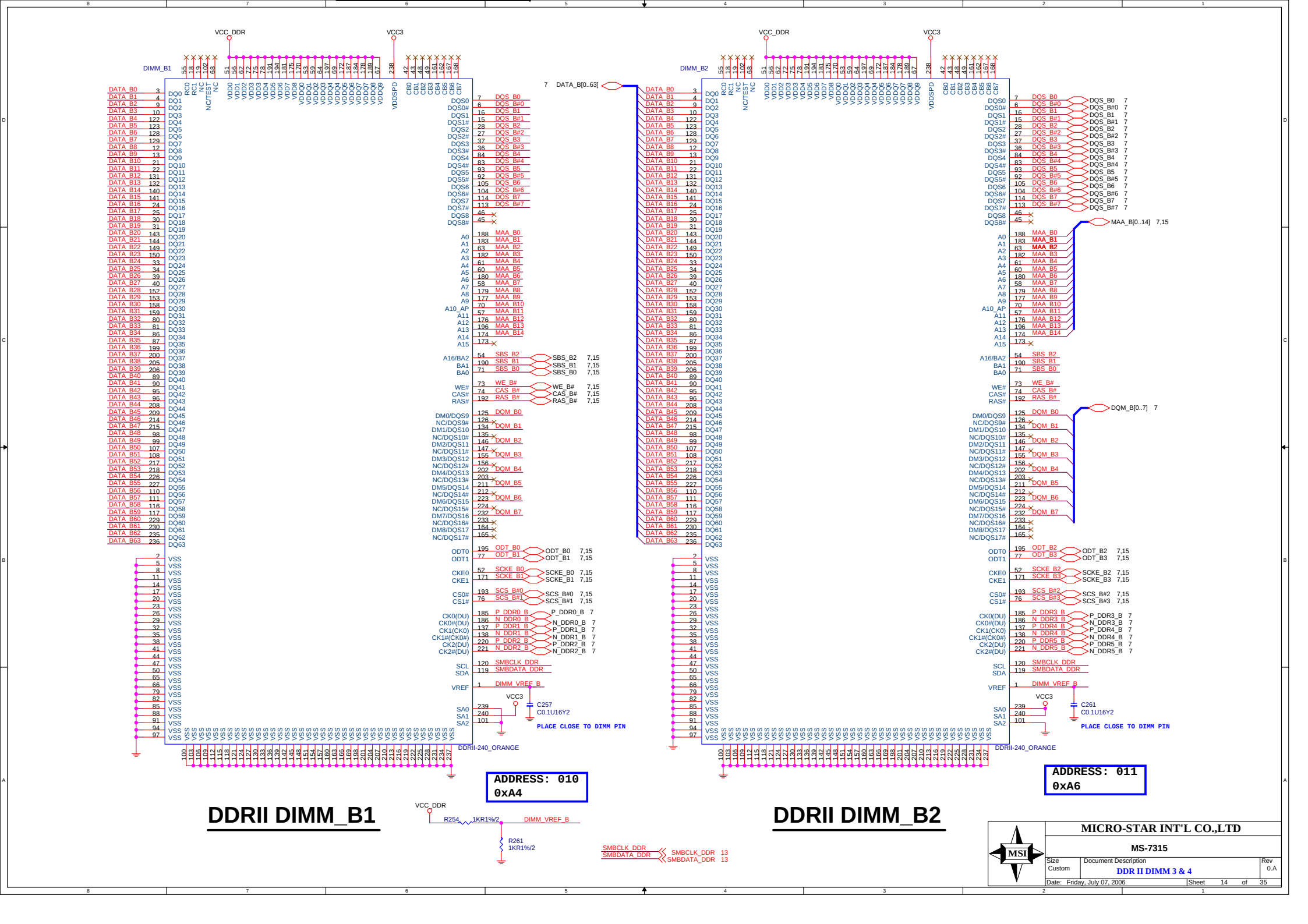
DDRII DIMM_B1
DDRII DIMM_B2
DIMM_B1
DIMM_B2
VCC_DDR
VCC3
DDRII-240_ORANGE
ADDRESS: 010
0xA4
ADDRESS: 011
0xA6
PLACE CLOSE TO DIMM PIN
C257
C0.1U16Y2
C261
C0.1U16Y2
R254
1KR1%/2
R261
1KR1%/2
DIMM_VREF_B
SMBCLK_DDR
SMBDATA_DDR
MICRO-STAR INT'L CO.,LTD
MS-7315
DDR II DIMM 3 & 4
Size
Custom
Document Description
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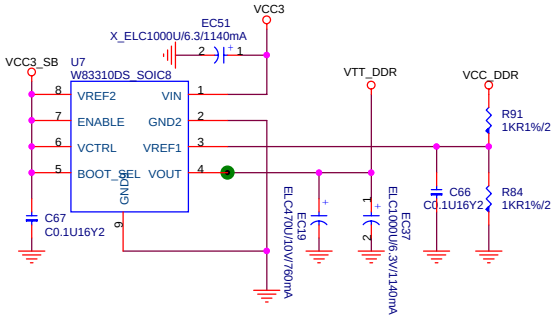
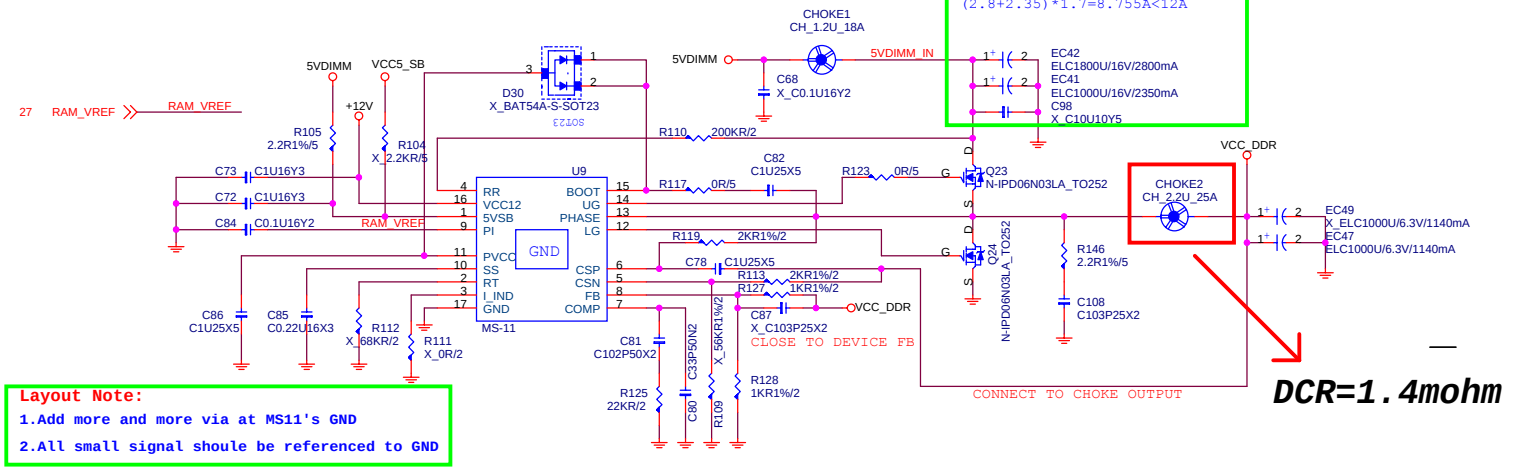
DDR II VTT POWER



DDR II 1.8V POWER...25A

Note:Iripple=Iout*[D/N-(D*D)]^0.5...D=Vout/Vin

Iripple=25*0.48=12A
(2.8+2.35)*1.7=8.755A<12A



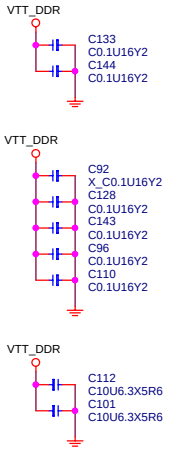
Layout Note:

1.Add more and more via at MS11's GND

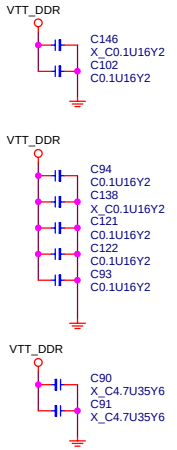
2.All small signal shoule be referenced to GND

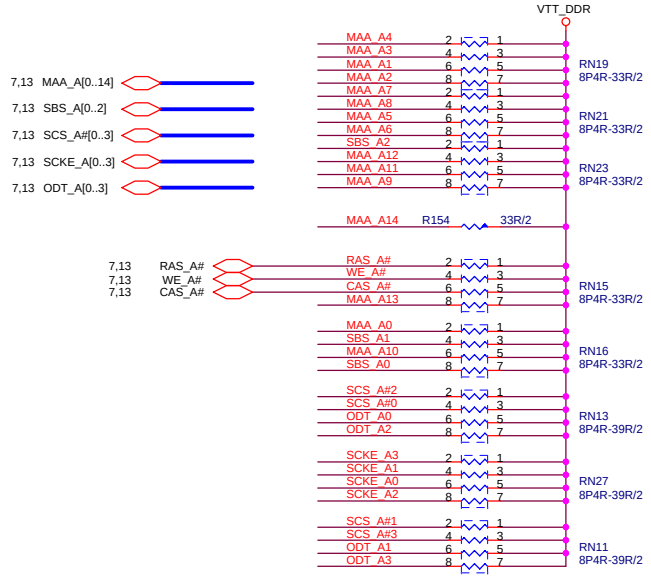
DCR=1.4mohm

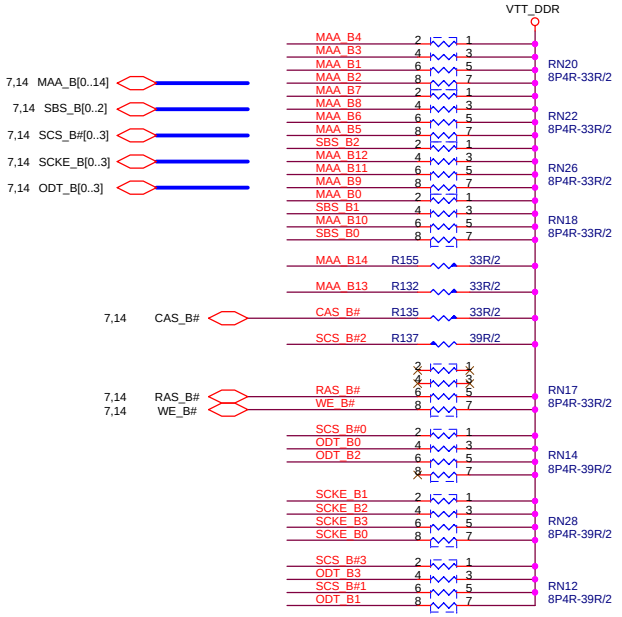
CHANNEL A V_SM_VTT DECOUPLING CAPS

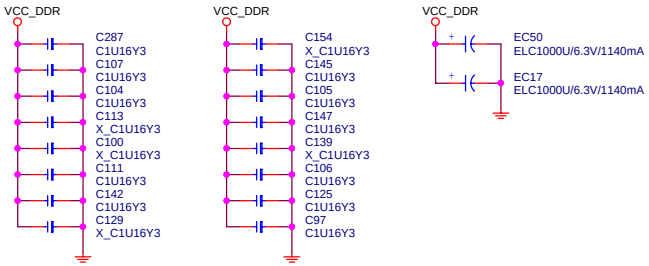


CHANNEL B V_SM_VTT DECOUPLING CAPS









MICRO-STAR INT'L CO.,LTD		
MS-7315		
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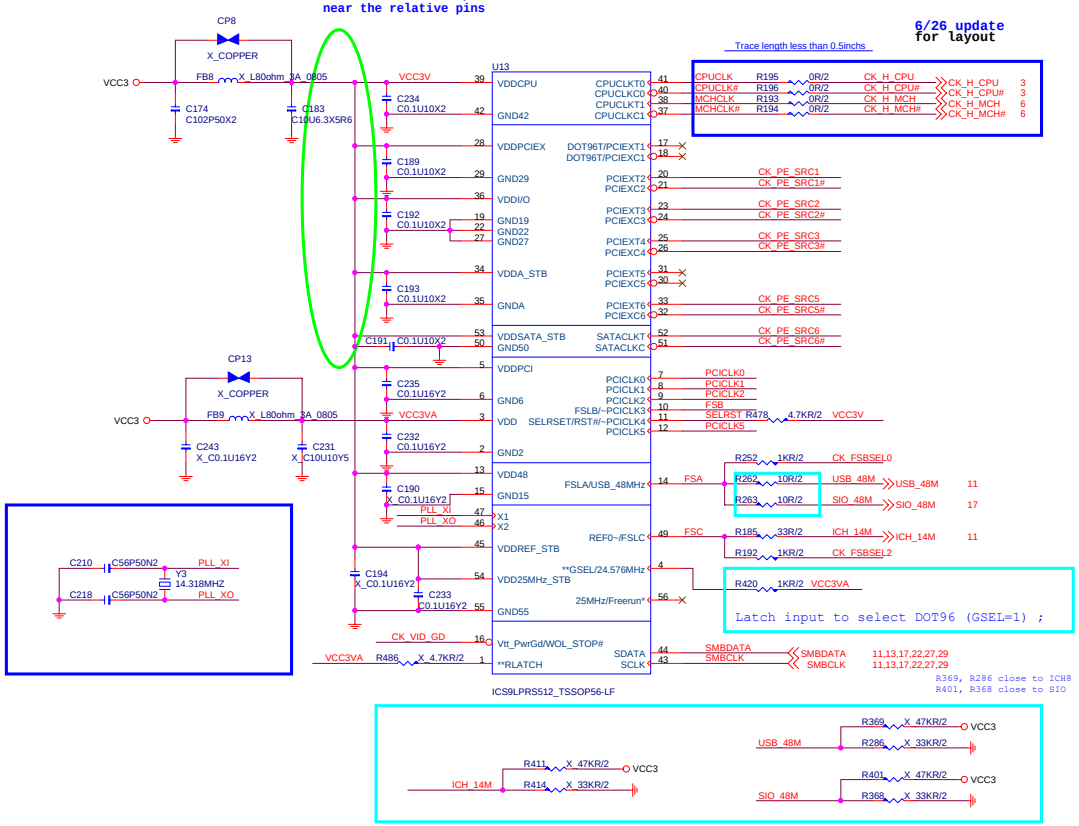
Date: Friday, July 07, 2006	Sheet 15 of 35	

Clock Generator - ICS9LPRS512

Note:Place these caps
near the relative pins

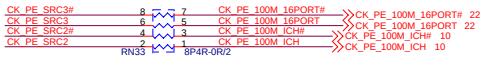
6/26 update
for layout

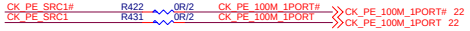
Trace length less than 0.5inchs

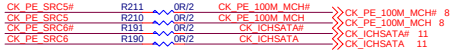


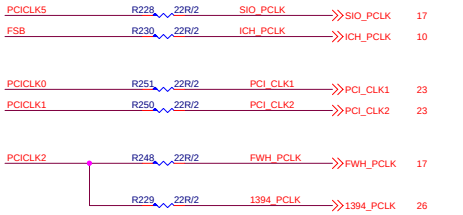
ICS9LPRS512_TSSOP56-LF

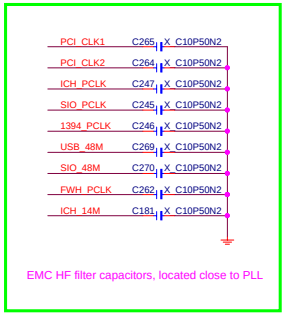
R369, R286 close to ICH8
R401, R368 close to SIO



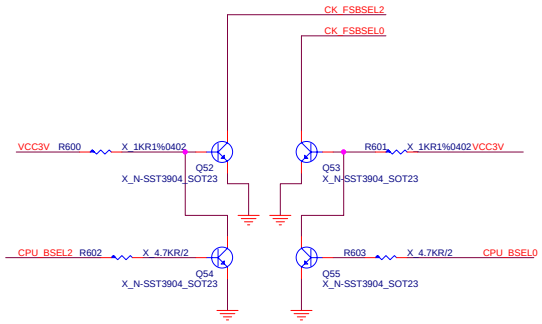




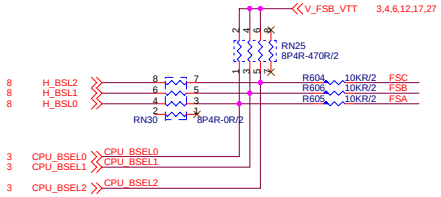




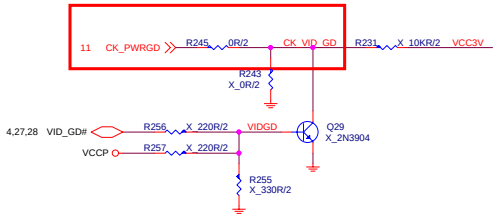
BSEL			TABLE
2			
0	0	0	266 MHz (1066)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)



BSEL[0..2] Level Shift



Clock Generator VTT Power Down Block



MICRO-STAR INT'L CO.,LTD

MS-7315

Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS512	0.A

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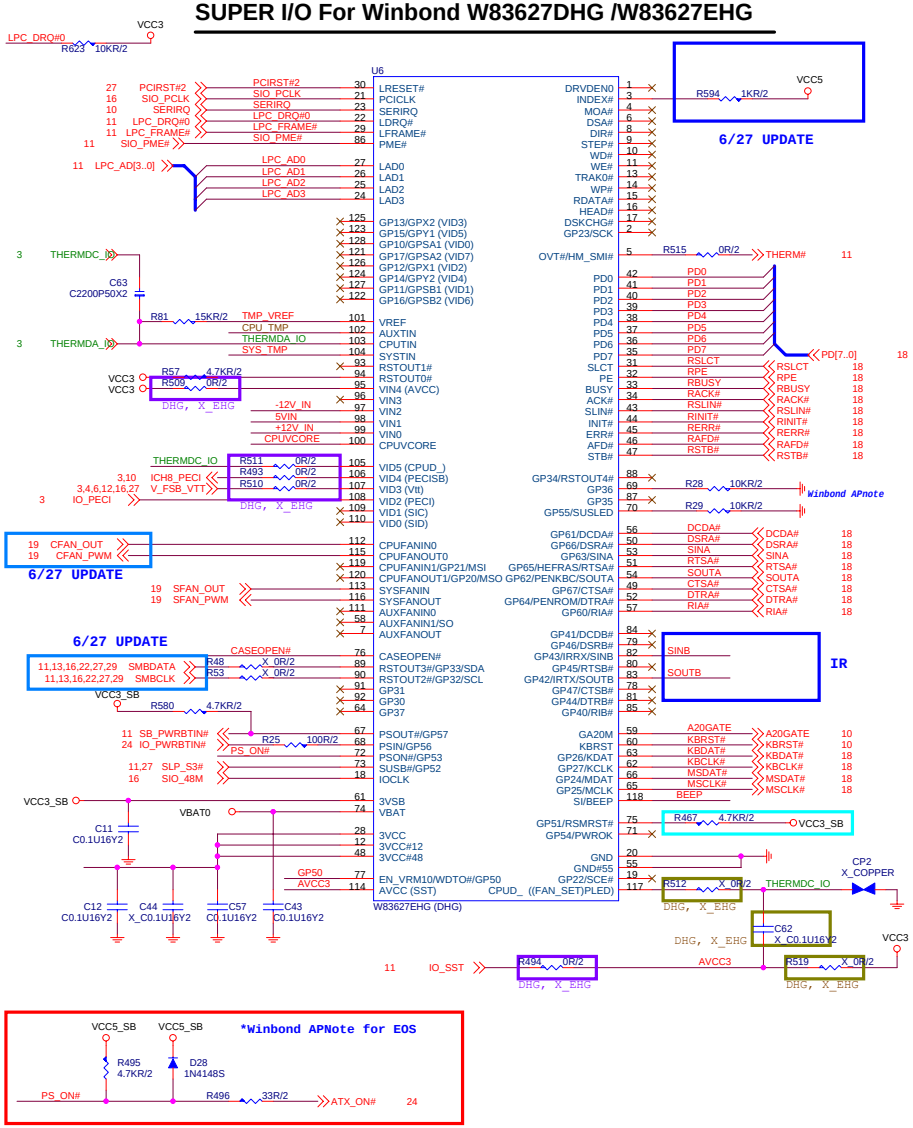
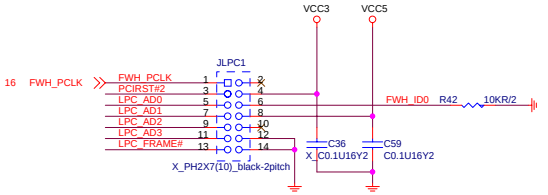
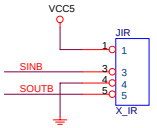
SUPER I/O For Winbond W83627DHG /W83627EHG



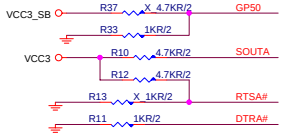
LPC Debug Port



Notice Key

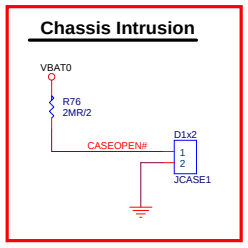


LPC I/O STRAPPING RESISTOR

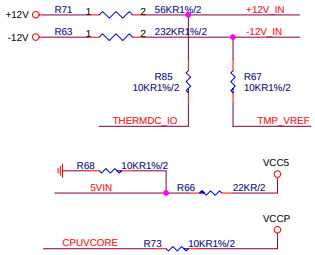


RTSA#	L: CFAD=2E	H: CFAD=4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: DIABLE SPI

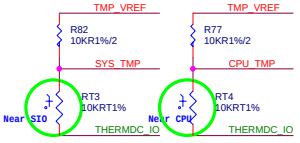
Chassis Intrusion



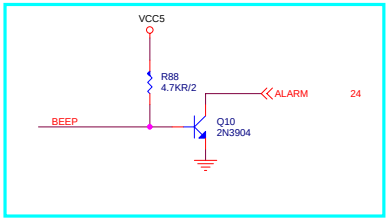
Voltage Detect



Temperature Senser



Beep



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MS-7315	
Size: Custom	Document Description: W83627DHG/ LPC
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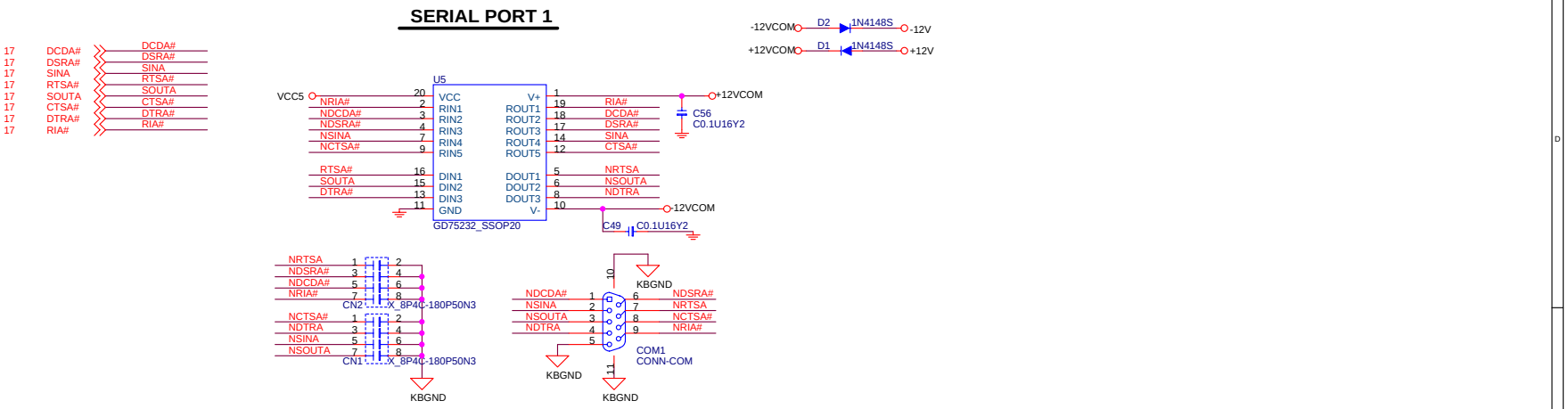
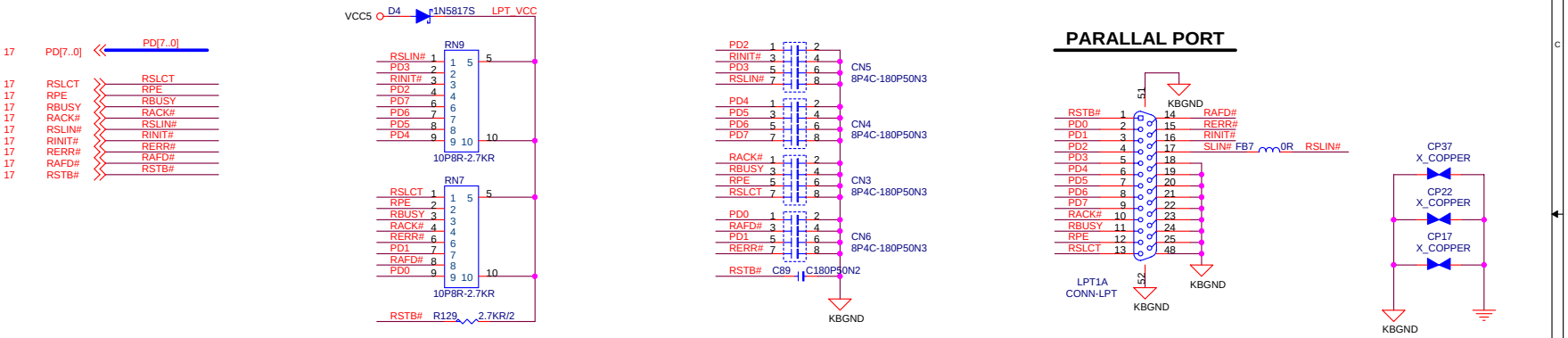
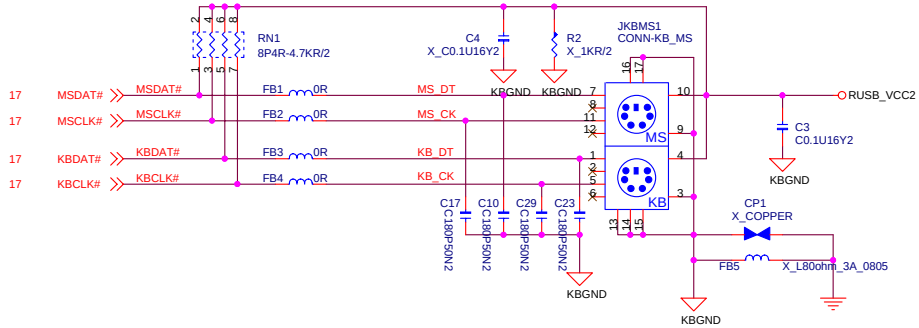
SERIAL PORT 1



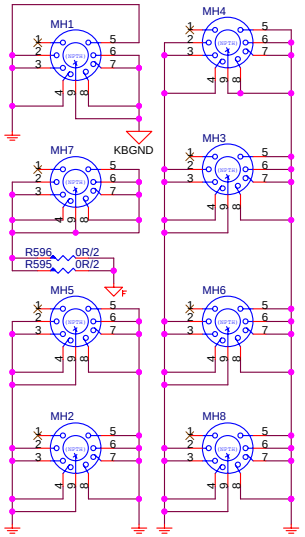
PARALLAL PORT



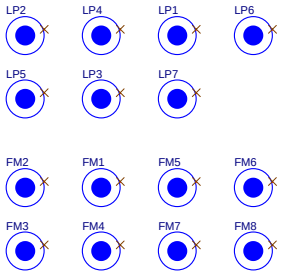
PS2 KEYBOARD & MOUSE CONNECTOR



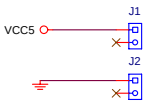
Mounting Holes



Optics Orientation Holes



Simulation



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Size: Custom	Document Description: PS2 / LPT / COM Port	Rev: 0.A
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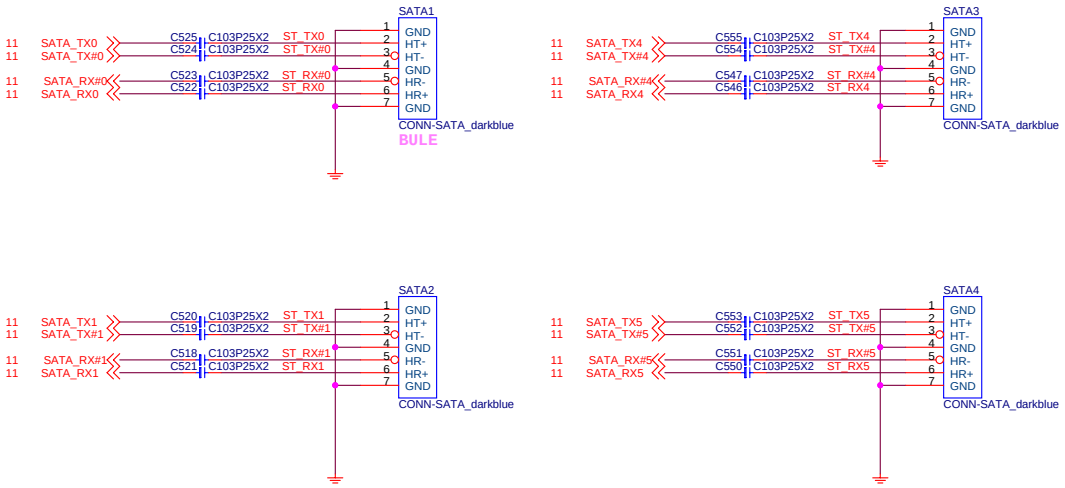
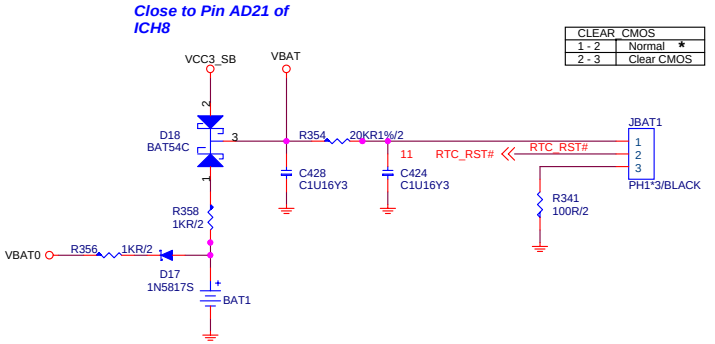
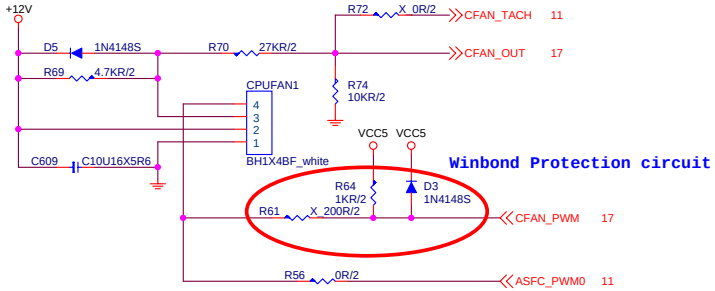
SATA CONNECTOR BLOCK



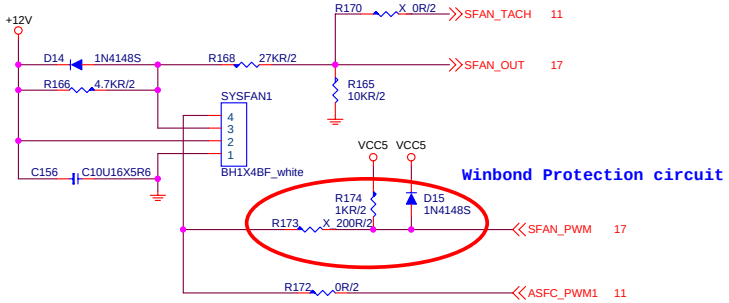
RTC BLOCK



CPU FAN



SYSTEM FAN



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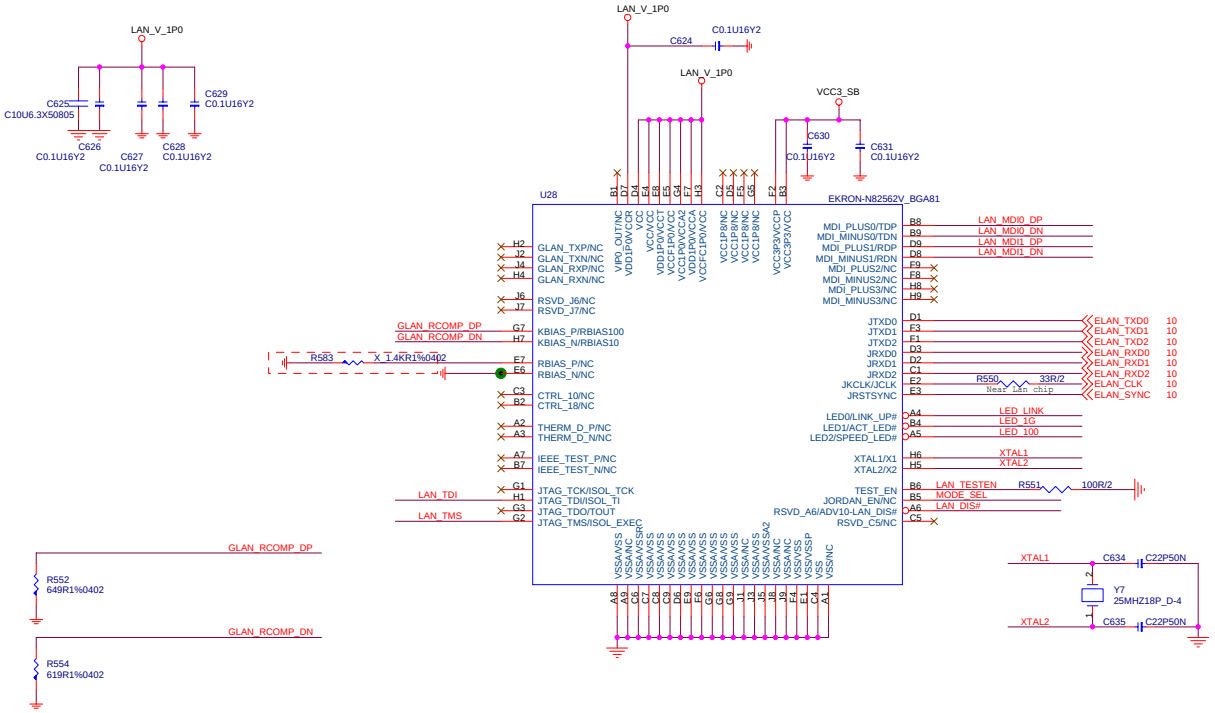
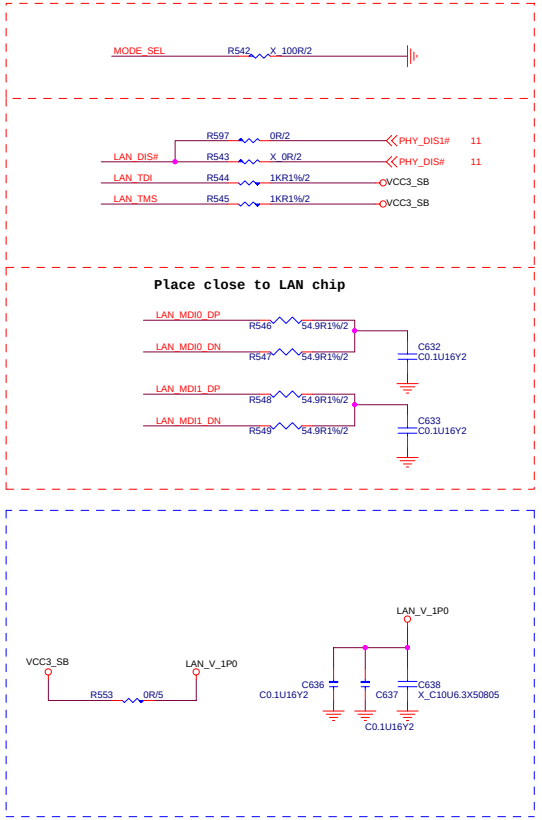
LAN - INTEL 82562V (EKRON)





Intel 82562V
Basic 10/100 Ethernet connection.

B06-8256205-I06
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

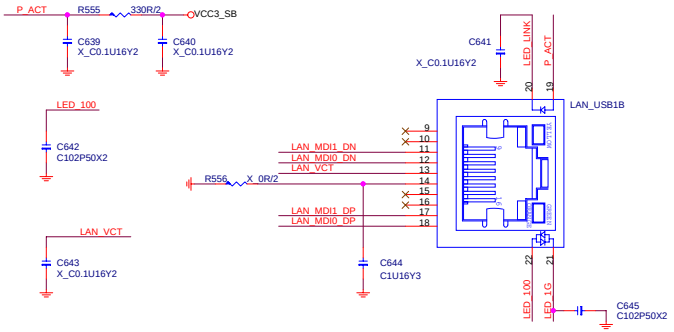
ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

10/100-Lan

N58-22F0061-S42
N58-22F0061-F02

Link	Yellow
Active	Blinking
100	Green
10	None

LAN CONNECTOR



1G:N58-22F0181-S42

Speed LED Type
100Mbps : Green
10Mbps : LED off

YELLOW : For Active/Link

MICRO-STAR INT'L CO.,LTD

MS-7315

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Custom	LAN - INTEL 82562V	0.A

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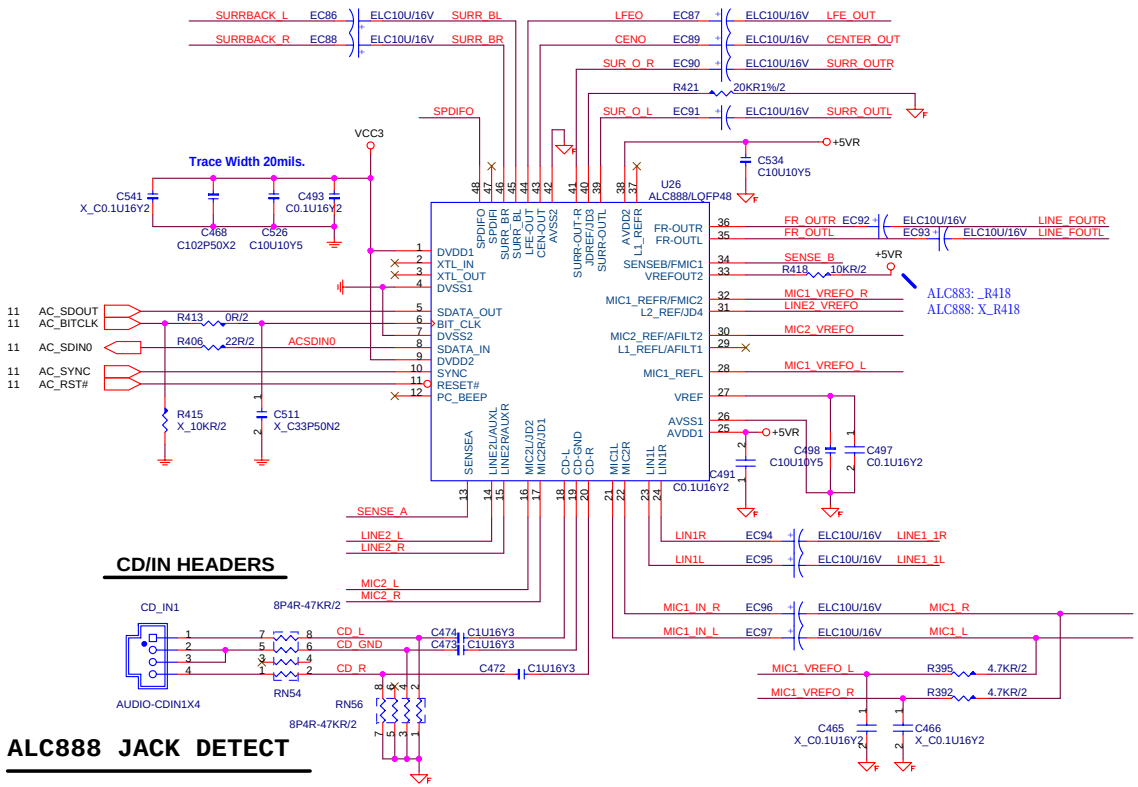
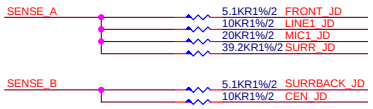
ALC888 CODEC

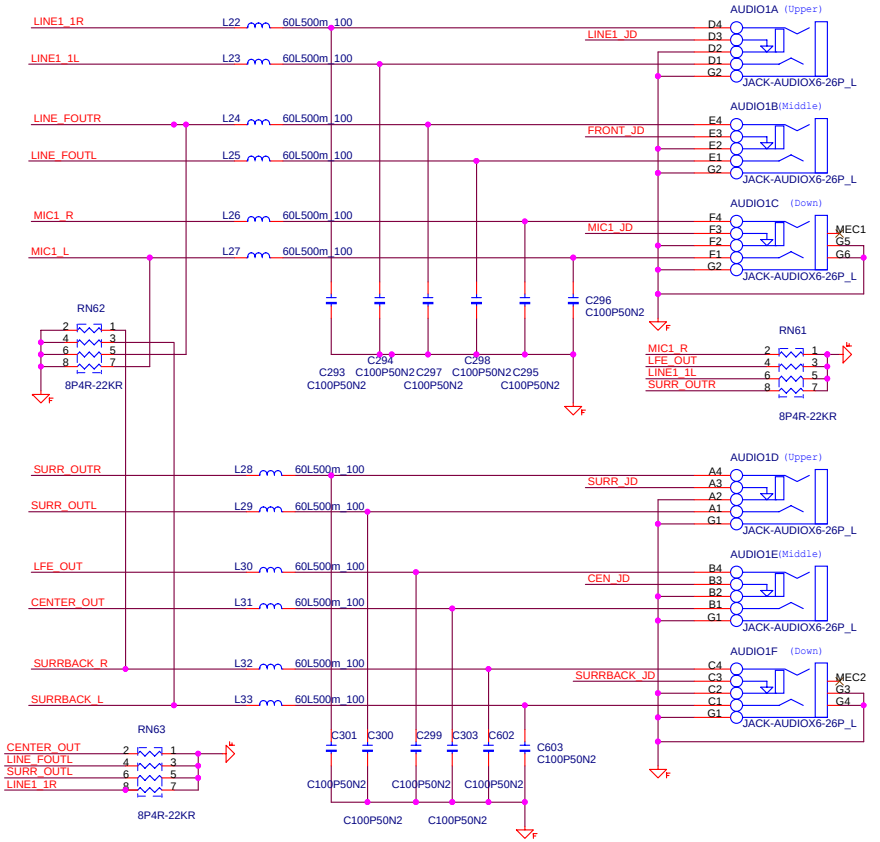


CD/IN HEADERS

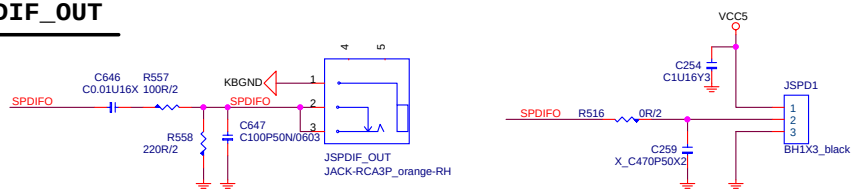
ALC888 JACK DETECT



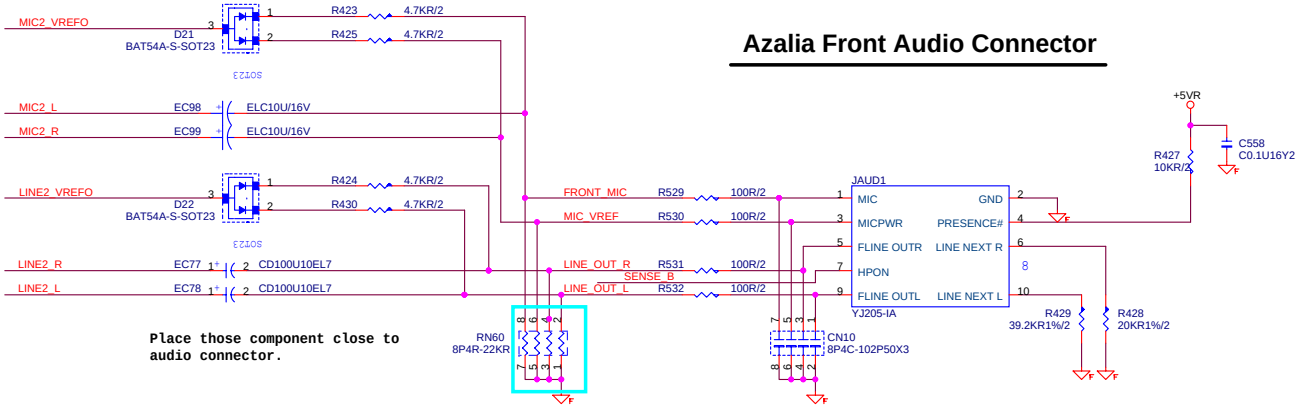
ALC888 JACK



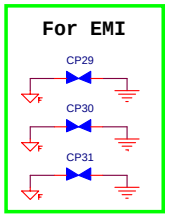
SPDIF_OUT



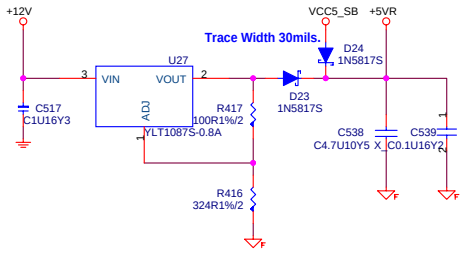
Azalia Front Audio Connector



For EMI



AUDIO CODE REGULATORS



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Size: Custom	Document Description: Azalia CODEC(ALC888)	Rev: 0.A
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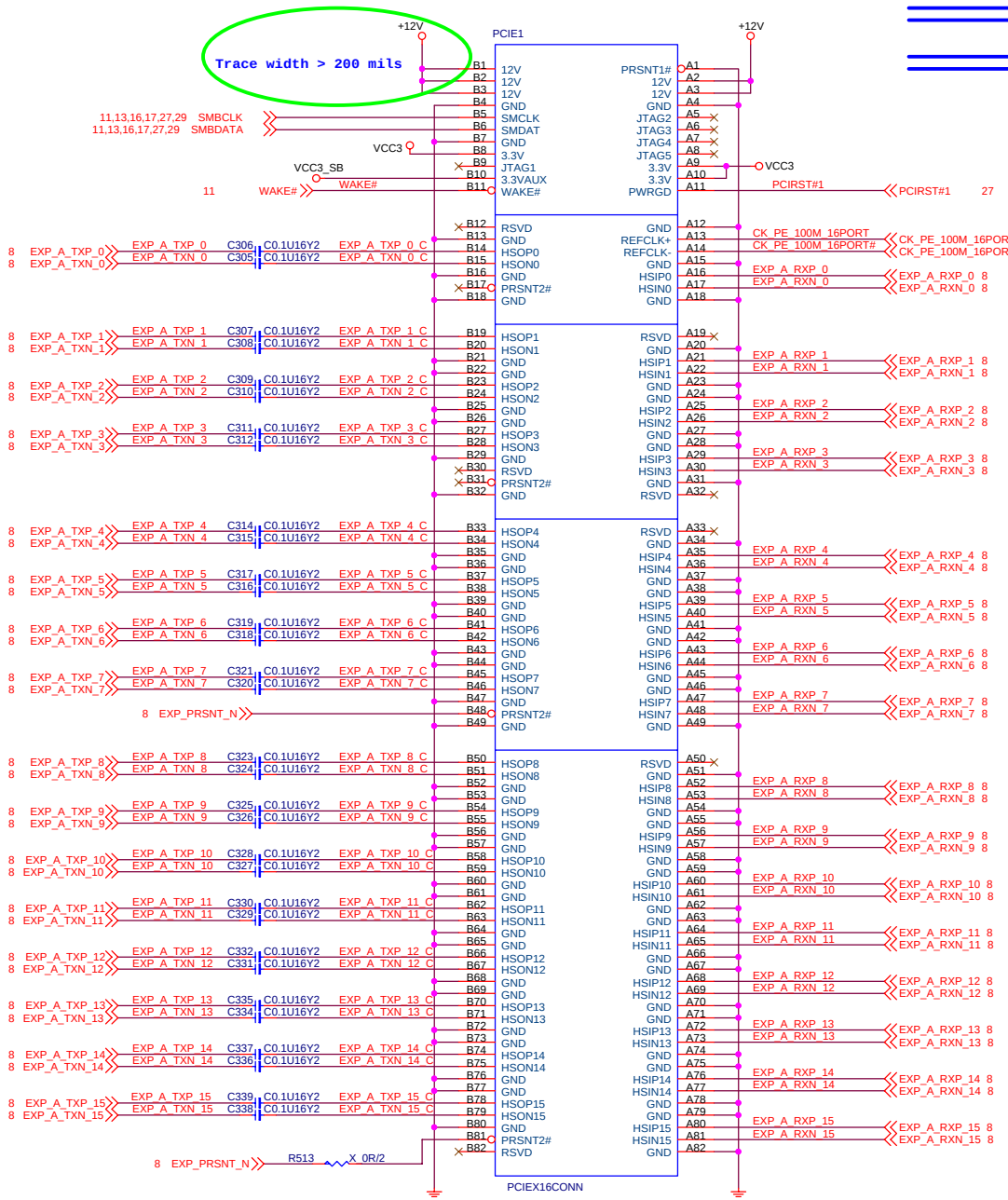
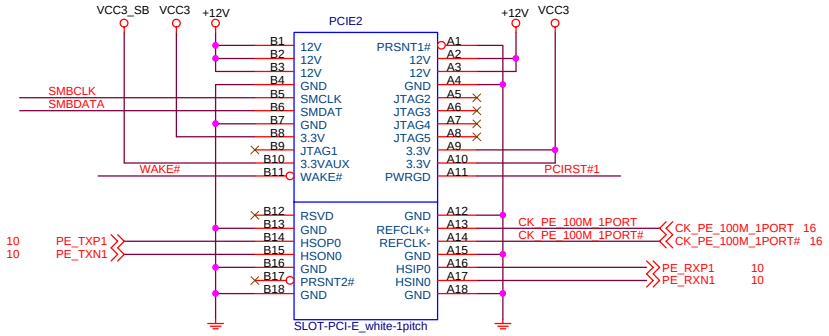
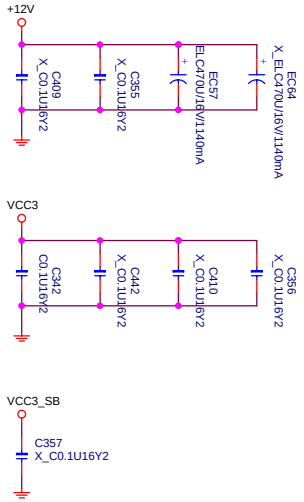
PCI EXPRESS 16-PORT



PCI EXPRESS 1-PORT





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Size: Custom	Document Description: PCIE X16 & PCIE X1 Slot	Rev: 0.A
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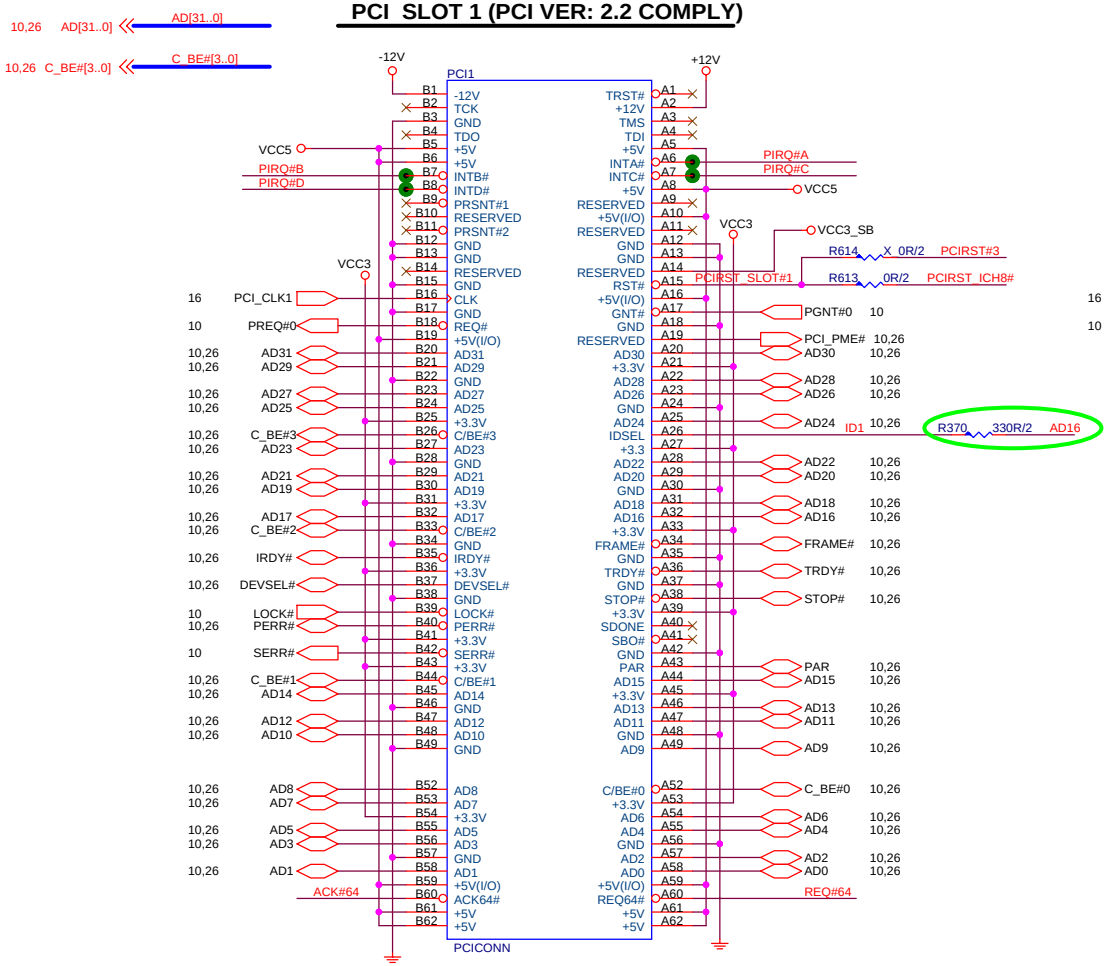
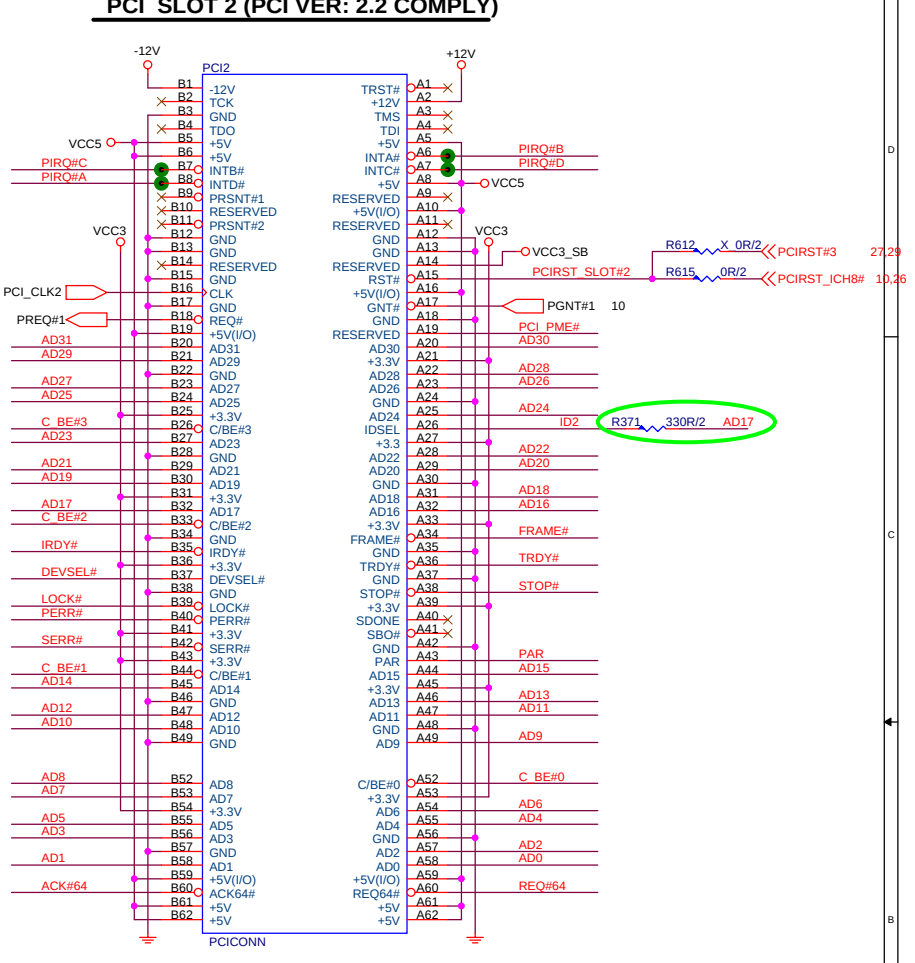
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



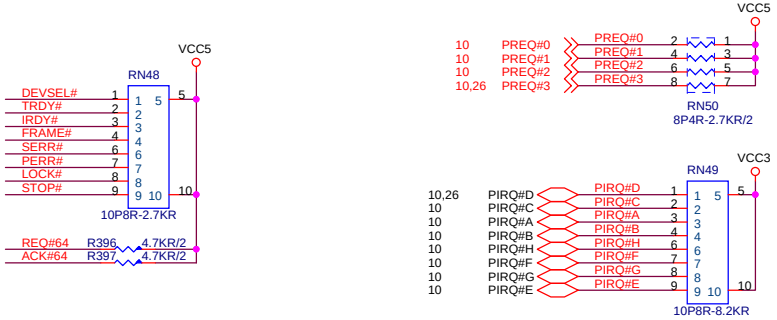
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

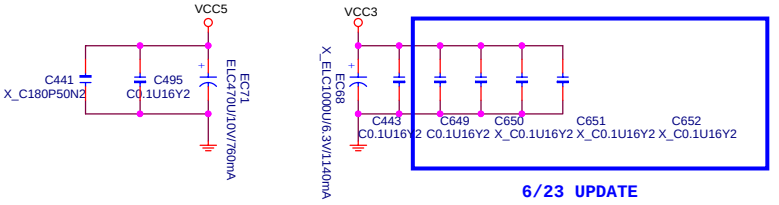


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



6/23 UPDATE

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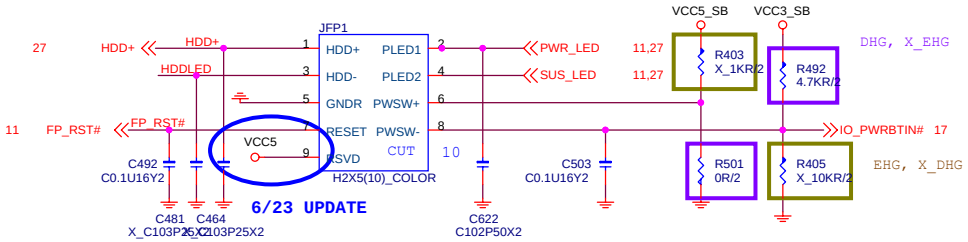
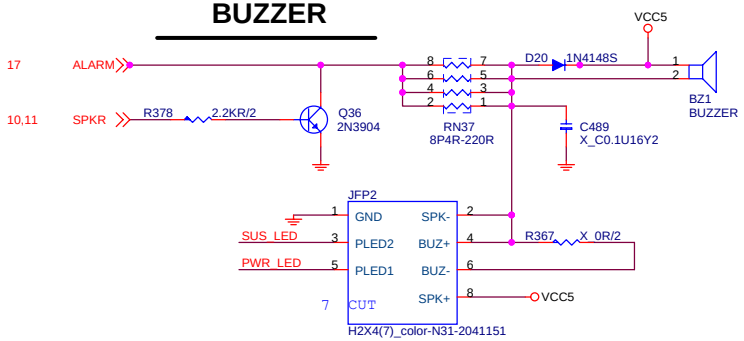
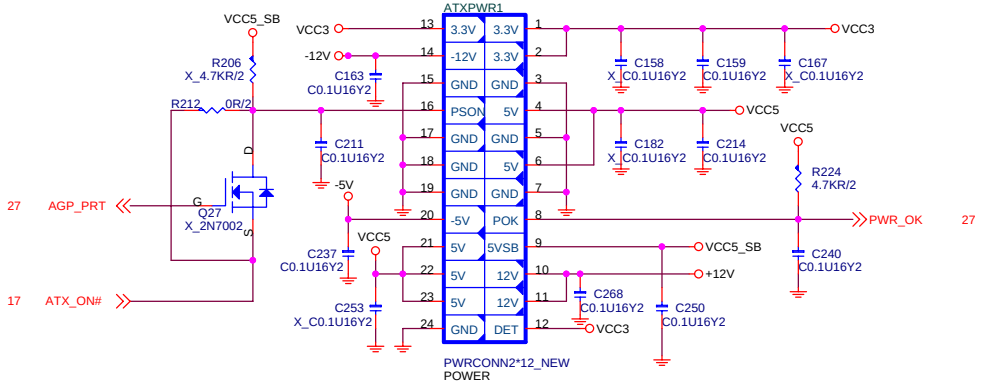
Front Panel



BUZZER

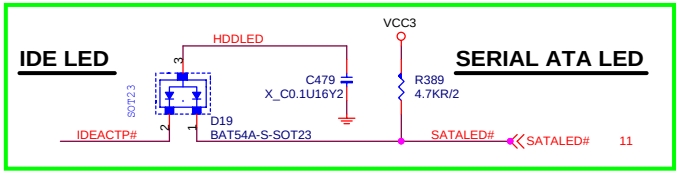


ATX CONNECTOR



IDE LED

SERIAL ATA LED



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MS-7315		
Size: Custom	Document Description: ATX & F_Panel	Rev: 0.A
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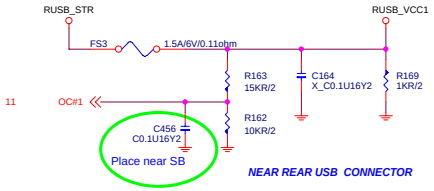
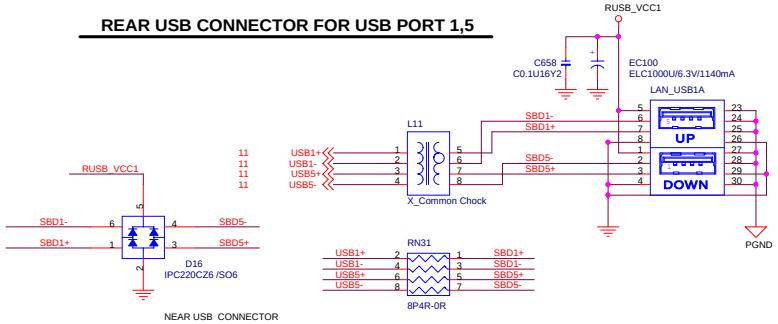
Rear USB Port 0 , 1 , 4 , 5 Circuit

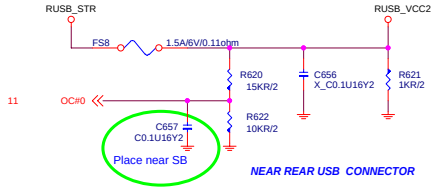
POWER CIRCUIT FOR USB PORT 1,5



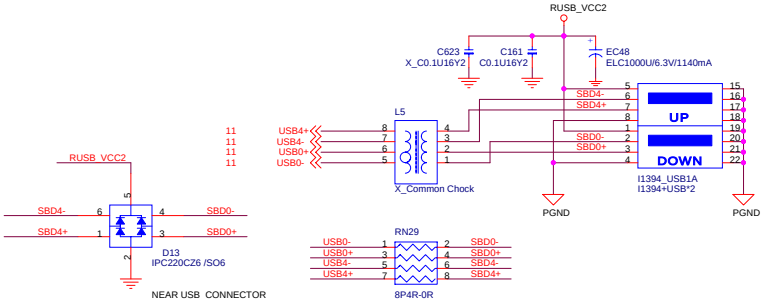
REAR USB CONNECTOR FOR USB PORT 1,5



POWER CIRCUIT FOR USB PORT 0,4

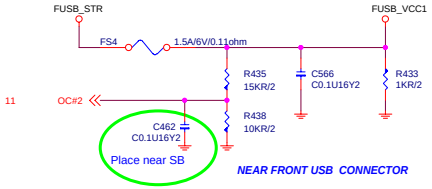


REAR USB CONNECTOR FOR USB PORT 0,4

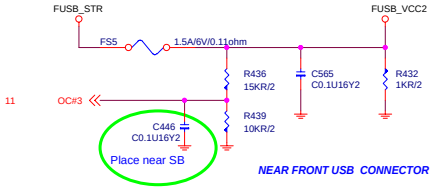


Front USB Port 4, 5, 6, 7 Circuit

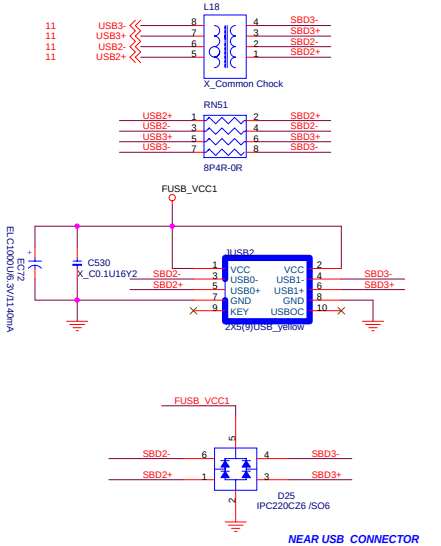
POWER CIRCUIT FOR USB PORT 4,5



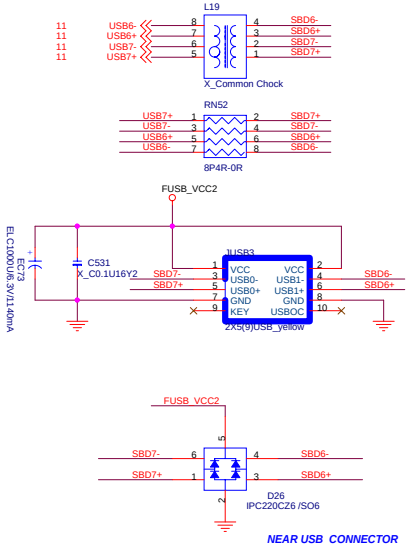
POWER CIRCUIT FOR USB PORT 6,7

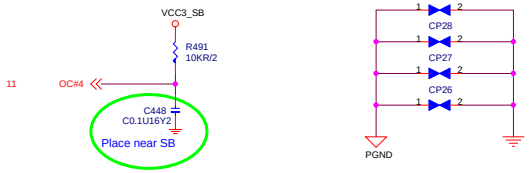


FRONT USB CONNECTOR FOR USB PORT 2,3



FRONT USB CONNECTOR FOR USB PORT 6,7





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IEEE-1394

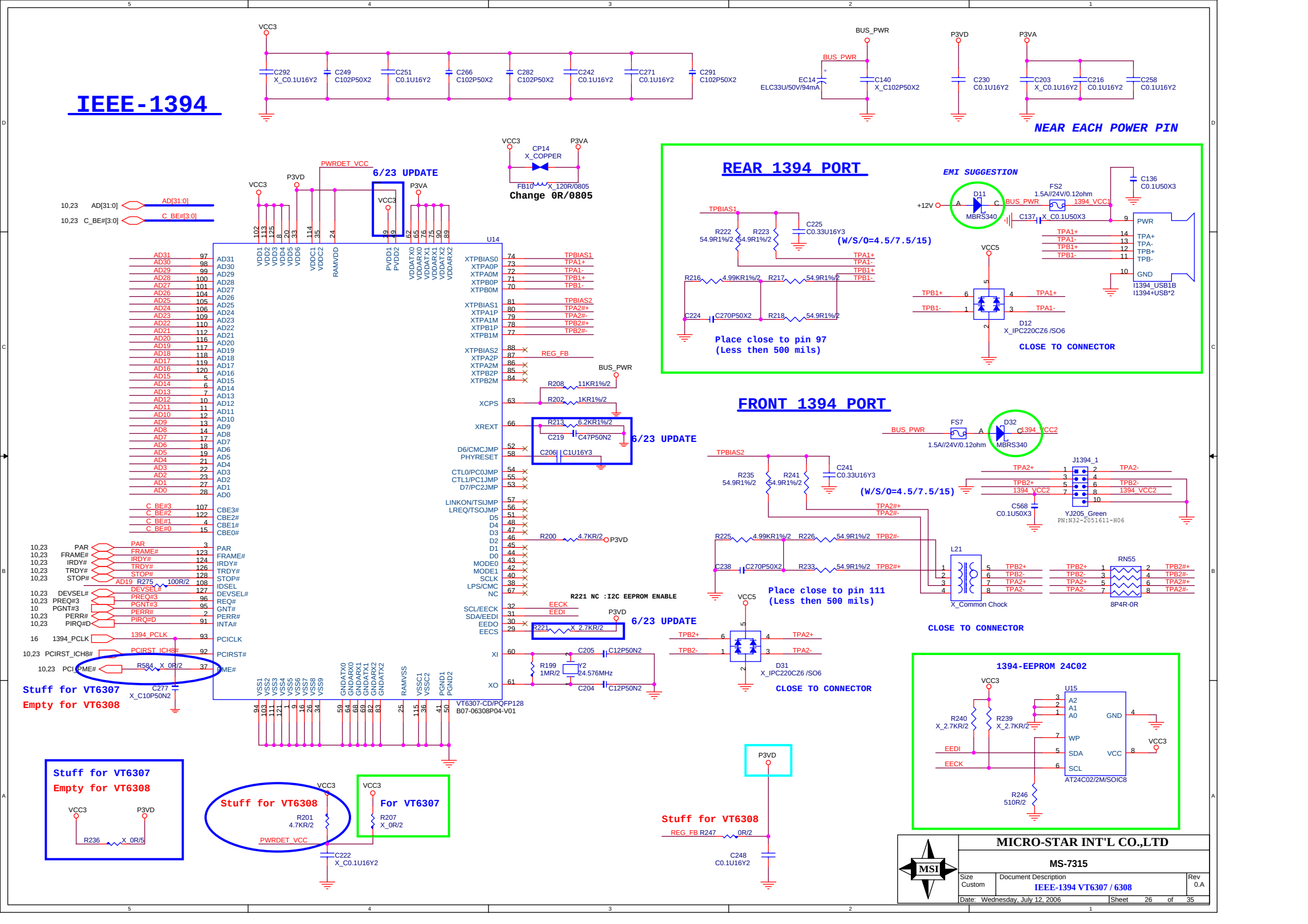
NEAR EACH POWER PIN

Change 0R/0805

Stuff for VT6307
Empty for VT6308

REAR 1394 PORT

FRONT 1394 PORT



ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR I & DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

V_FSB_VTT 6.2A

THIS PIN IS OPEN DRAIN OUTPUT

Reserved for KENTSFIELD Processor (FSB1333, Quad-Core, Low Power)

Wide Trace

Close to MS11

VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

5V DUAL Power 5A

FRONT USB

REAR USB

VCC3_SB Power

5VDIMM

V_1P25_CORE POWER...21.34A + 3.8A

*Short to V_1P25_CL if no iAMT support

Note:Iripple=Iout*[D/N-(D*D)]^0.5...D=Vout/Vin

Iripple=25*0.48=12A
(2.35*2)*1.7=7.99A<12A

CLOSE TO DEVICE FB

CONNECT TO CHOKE OUTPUT

DCR=1.68mohm

Layout Note:
1.Add more and more via at MS11's GND
2.All small signal shoule be referenced to GND

V_1P5_ICH...2A + 1.17A

V_1P05_ICH...1.17A

MICRO-STAR INT'L CO.,LTD

MS-7315

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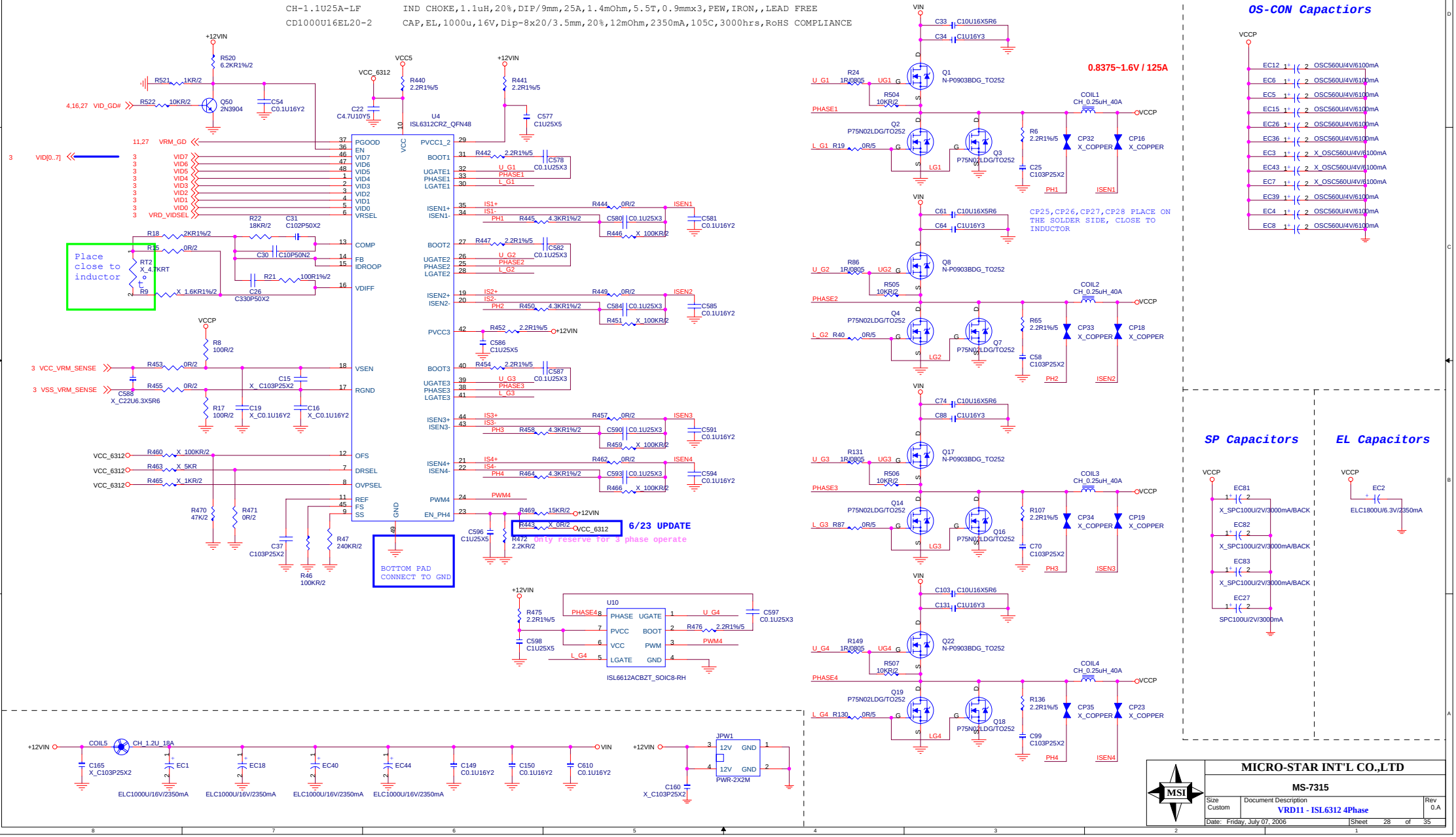
Voltage Regular Module

N-P0903BDG_TO252	mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5mΩ(10V/25A),Vgs(on) =1~3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG/TO252	mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7mΩ(@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U2SP	ESR<13mΩ,Ripple cur.<2.7A,LC<12uA,105C
CD560U4OS-2	CAP,OS-CON,560u/4V,Dip-2/8*9/3.5mm,ESR<7mohm, Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
1800UF/6.3V	ESR<12mΩ, Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.25uH/40A	,IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
CH-1.1U25A-LF	IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CD1000U16EL20-2	CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE



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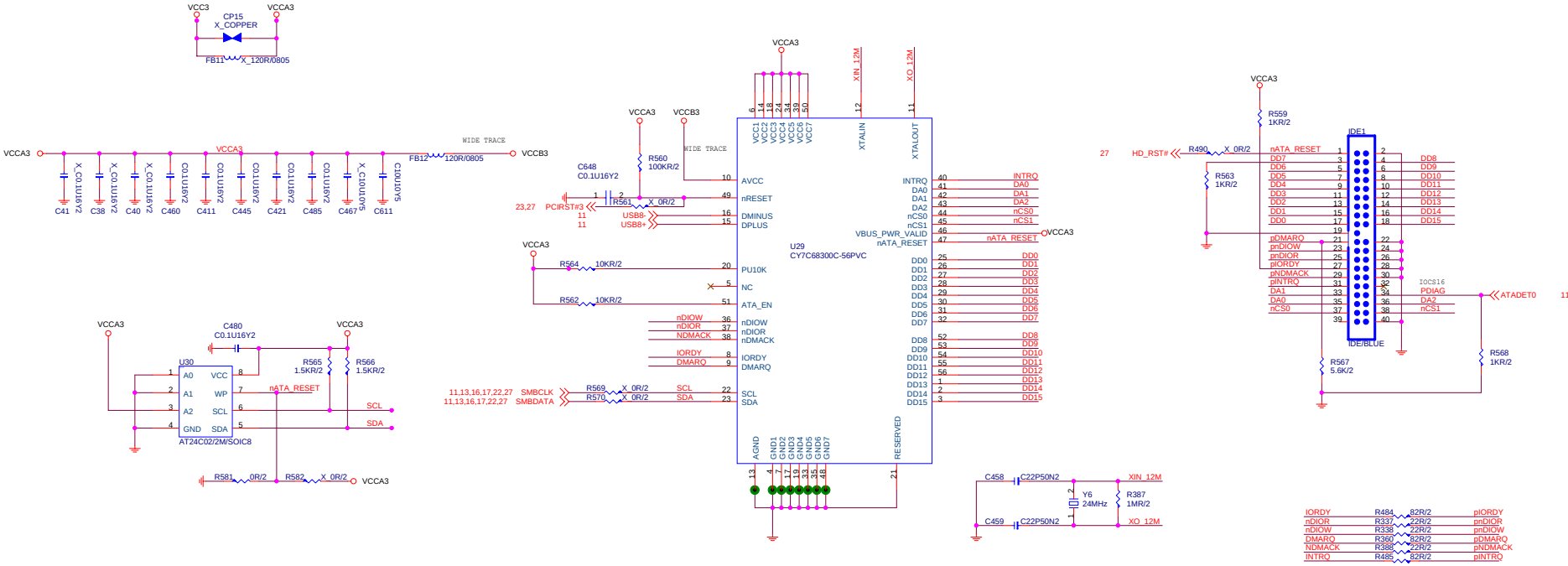
Hi-Speed USB to PATA Bridge



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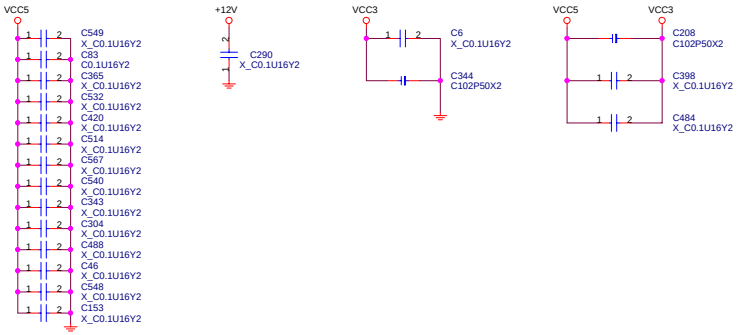

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GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO [7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO 9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO 10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO 14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO 19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO 21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO 22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO 36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO 37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO 38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO 39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO 48
GPIO[49]	CPUPWRGD		I/O	V_CPU_IO			CPU	Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK2
LAN	PIRQ#C	PREQ#2 PGNT#2	AD18	LAN_PCLK
1394	PIRQ#D	PREQ#3 PGNT#3	AD19	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, FWH
PCIRST#3	PCI SLOT1&2(OPTION) , IDE
PCIRST_ICH8#	PCI SLOT1&2(OPTION) , 1394
HD_RST#	Primary IDE
PLTRST#	MS7 ,GMCH

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

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