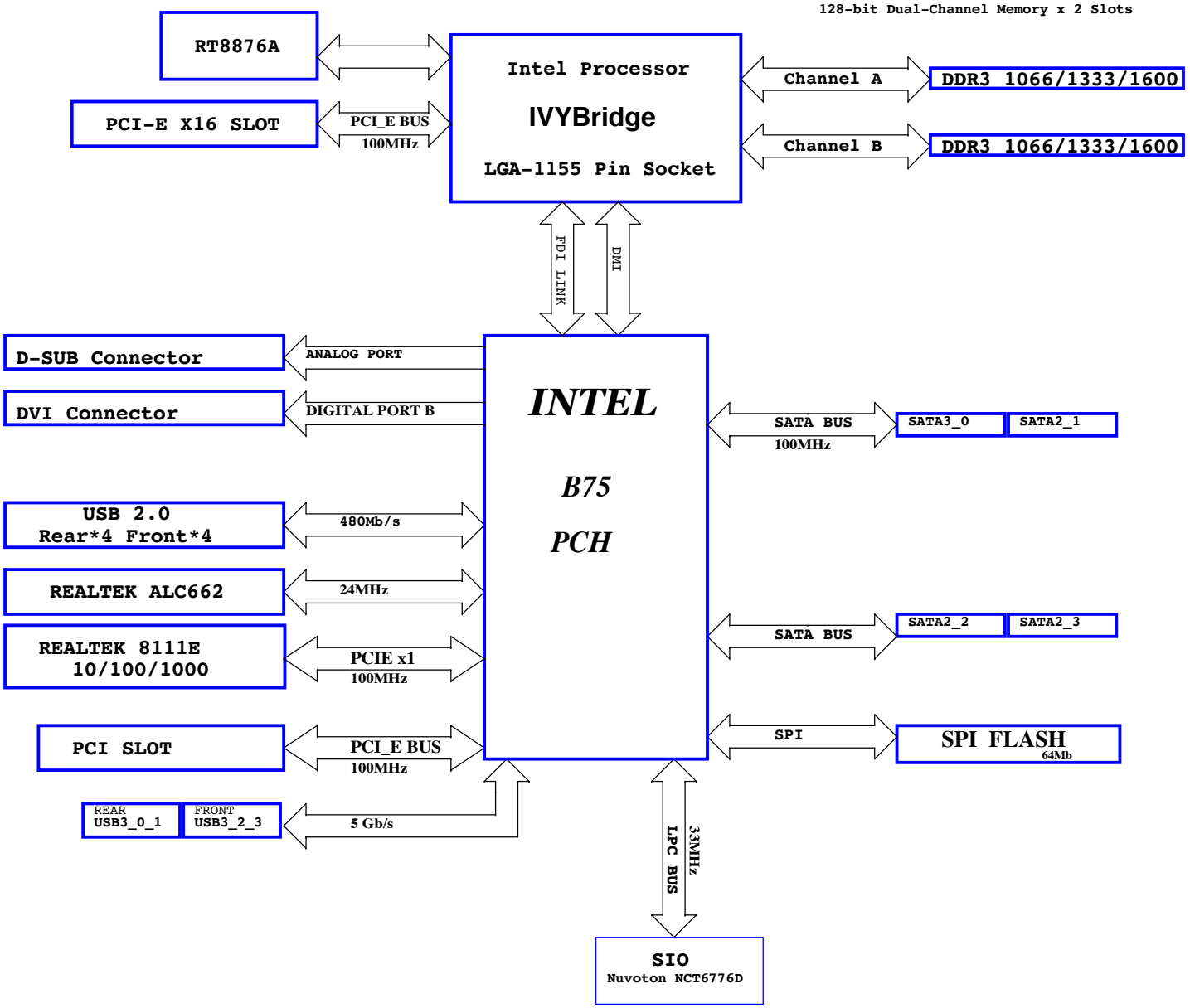
B75M-DGS R2.00



B75M-DGS

ASRock Inc.

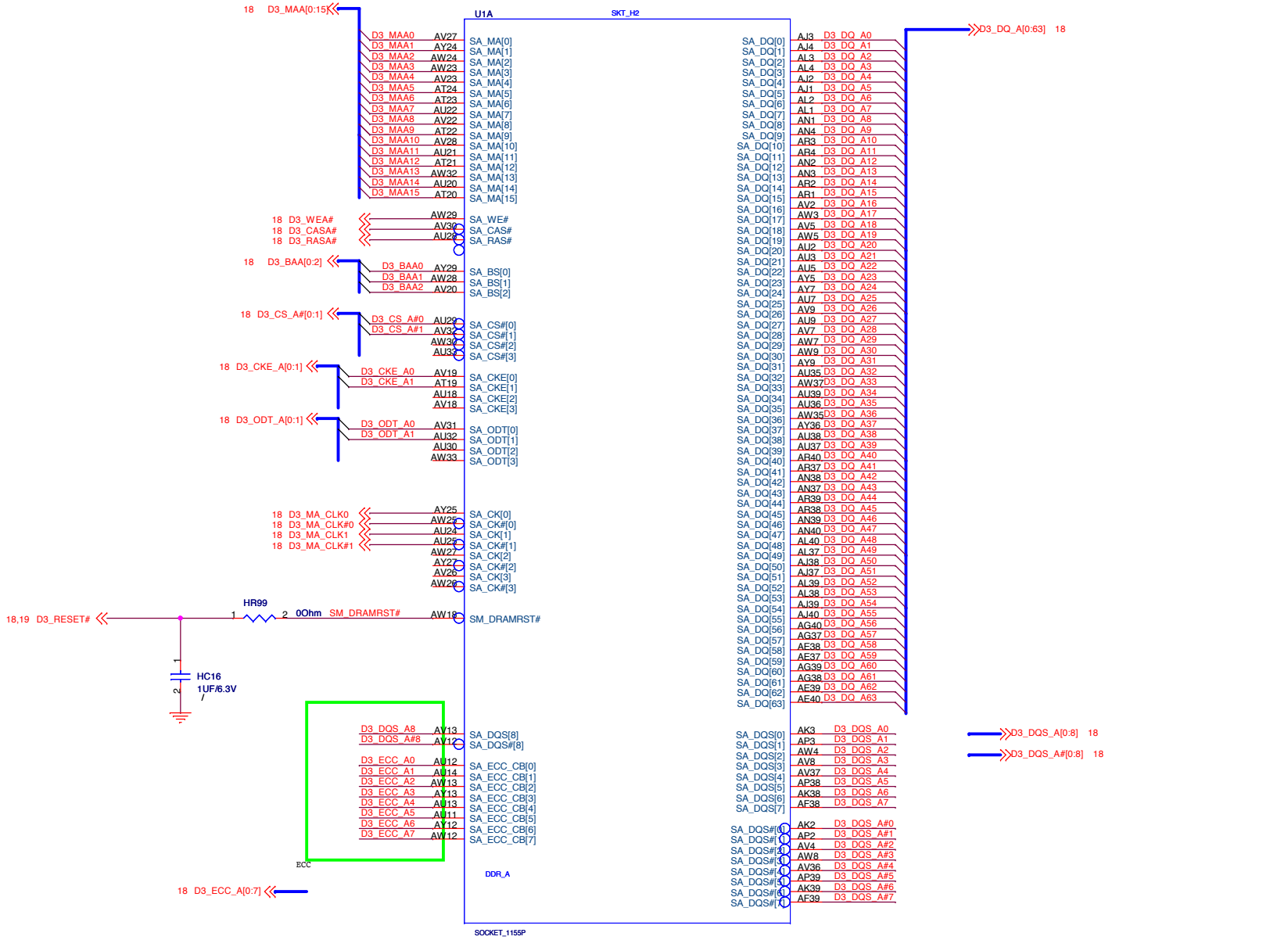
Title : Block Diagram

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 1 of 48

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



B75M-DGS

ASRock Inc.

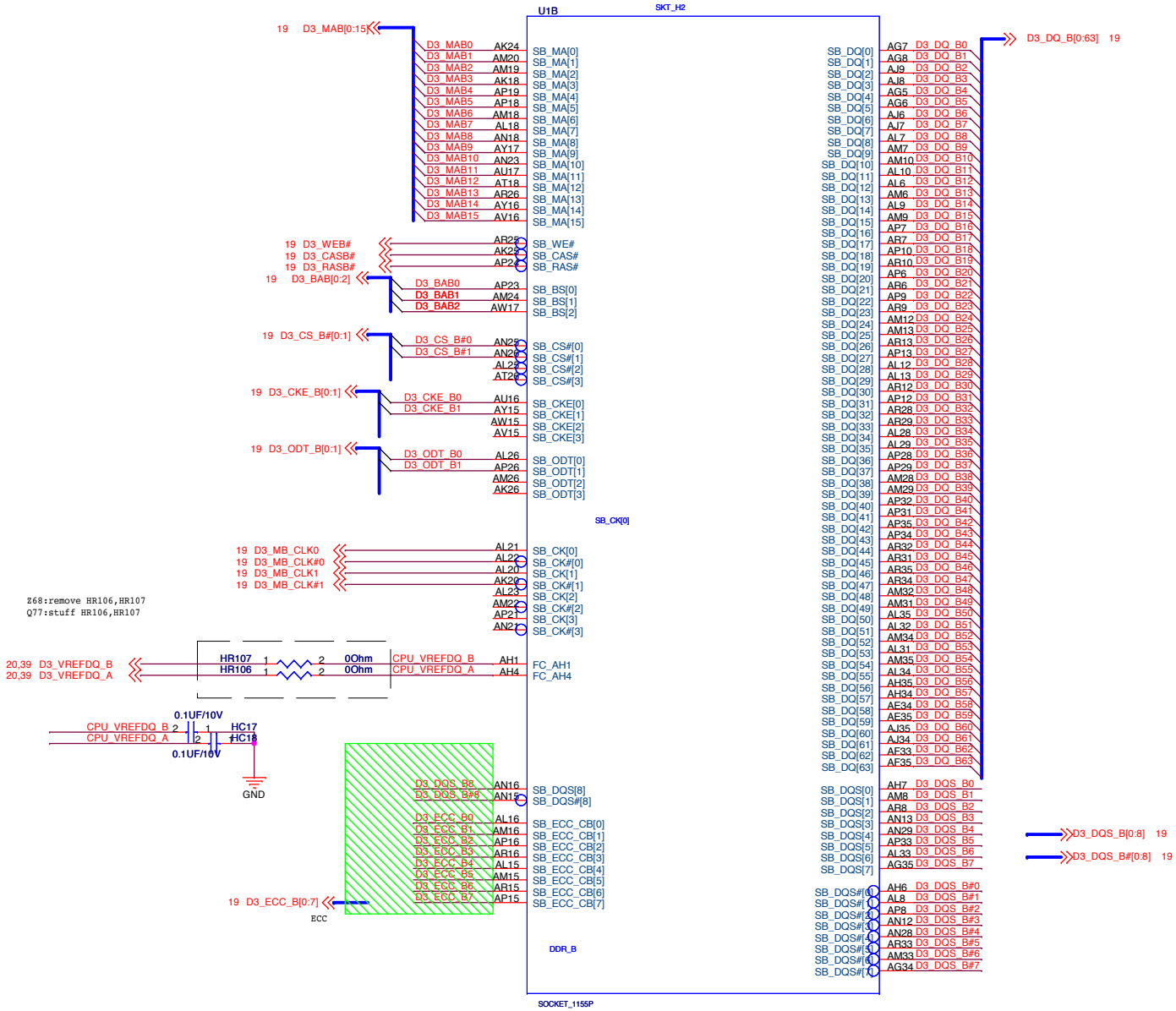
Title : MEM CTRL CHA

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 2 of 48

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



B75M-DGS

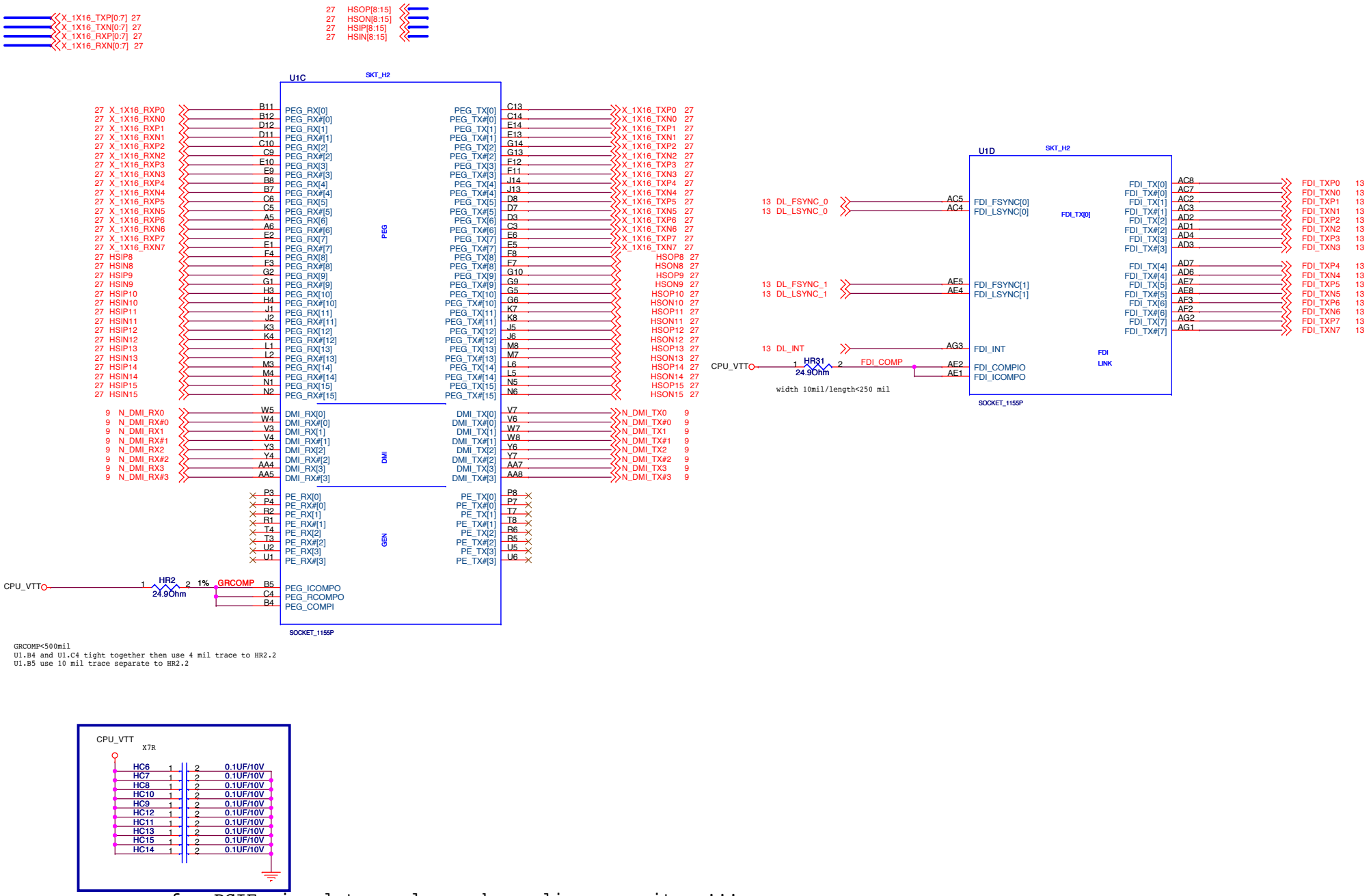
ASRock Inc.

Title : MEM CTRL CHB

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 3 of 48

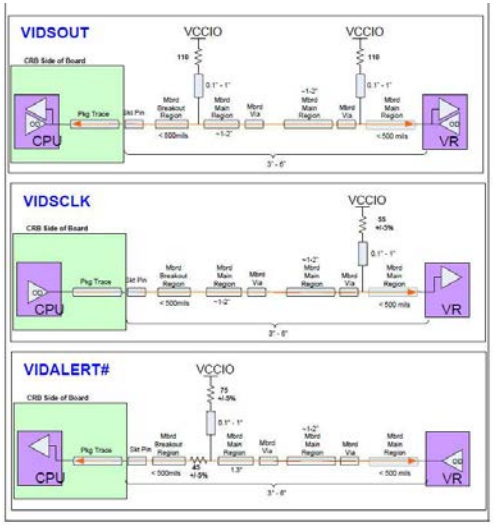


for PCIE signal trans-layer decoupling capacitors!!!
Place near trans-layer vias for PCIe lanes.

B75M-DGS

ASRock Inc.	Title : CPU - PEG/FDI	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 4 of 48	

SVID Placement needs to pay attention for pull up resistors. See PDG page 330



U1E SKT_H2

14 PCH_CK_DMI
14 PCH_CK_DMI#
can not connect to clock gen. must be provided by PCH.
45 VIDCLK
45 VIDSOUT
45 VIDALERT#
HR44 45.3Ohm 1% VIDALERT#_R
11 CPUPWRGD
VCCM
HR45 1% 1.1KOHM
HR105 0Ohm
2000 mil <U1.AJ19 to HR45 <3000 mil
11 DRAM_PWROK
17 CPU_RESET#
HR104 0Ohm
HR7 0Ohm PLT_RSTL_R
10 PM_SYNC
PECI
H_CATERR_N
45 PROCHOT#
10 H_THERMTRIP_N
17 H_SKTOCC#
16 PROC_SEL
CPU_DDR_VREF
For future processor compatibility, the PROC_SEL should be connect to the NV_CLE pin on the PCH through an isolation resistor of 4.7K ohm and a 2.2k ohm pull up to V_NAND_IO (+1.8V).
17 H_SKTOCC#
HR8 0Ohm
H_SKTOCC#_PCH 11

W2 BCLK[0]
W1 BCLK#[0]
C37 VIDSCLK
B37 VIDSOUT
A37 VIDALERT#
J40 UNCOREPWRGOOD
AJ19 SM_DRAMPWROK
F36 RESET#
E38 PM_SYNC
J35 PECI
E37 CATERR#
H34 PROCHOT#
G34 THERMTRIP#
AJ33 SKTOCC#
K32 PROC_SEL
AJ22 SM_VREF

CPU_CFG0 H36 CFG[0]
CPU_CFG1 J36 CFG[1]
CPU_CFG2 J37 CFG[2]
CPU_CFG3 K36 CFG[3]
L36 CFG[4]
N35 CFG[5]
L37 CFG[6]
M36 CFG[7]
J38 CFG[8]
L35 CFG[9]
M38 CFG[10]
N36 CFG[11]
N38 CFG[12]
N39 CFG[13]
N37 CFG[14]
N40 CFG[15]
CPU_CFG16 G37 CFG[16]
G36 CFG[17]

AT14 RSVD5
AY3 RSVD_NCTF_1
H7 RSVD44
H8 RSVD43

P33 RSVD28
P34 VCCSA_VID
T2 VCCSA_SENSE
A36 VCC_SENSE
B36 VSS_SENSE
AB4 VCCIO_SENSE
AB3 VSSIO_SENSE
L32 VCCAXG_SENSE
M32 VSSAXG_SENSE
L39 TDO
L40 TDI
M40 TCK
L38 TMS
J39 TRST#
K38 PRDY#
K40 PREQ#
E39 DBR#
C40 VCC_NCTF
D40 RSVD46

H40 BPM#[0]
H38 BPM#[1]
G38 BPM#[2]
G40 BPM#[3]
G39 BPM#[4]
F38 BPM#[5]
E40 BPM#[6]
F40 BPM#[7]

B39 VSS_NCTF3
J33 RSVD40
L34 RSVD32
L33 RSVD33
K34 RSVD36
N33 RSVD30
M34 RSVD31
AV1 RSVD_NCTF_3
AW2 RSVD_NCTF_2
L9 RSVD35
J9 RSVD42
K9 RSVD38
L31 RSVD34
J31 RSVD41
K31 RSVD37
AD34 RSVD18
AD35 RSVD17

MISC
SOCKET_1155P

VTT_CPUVID3 40
GND 4.7KOhm HR39 HR40 10KOhm +5V
VT15 TPC35t
VCCSA_VID
VCCSA_SENSE 41
VCC_SENSE 45
VSS_SENSE 45
H_CPU_VTT_DP 40
H_CPU_VTT_DN 40
H_CPU_GFX_DP 45
H_CPU_GFX_DN 45
HR46 51.1OHM
HR48 51.1OHM
HR47 51.1OHM
HR50 51.1OHM
HR49 51.1OHM
HR51 51.1OHM
CPU_VTT
GND

Reserved for testing purpose:
Must have: CFG[3:0], CFG[16] test points.
Nice to have: CFG[7:0], CFG[16] test points.
Very nice to have: Nice to have: CFG[15:0], CFG[16] test points.

GND 1KOhm HR53 CPU_CFG0
GND 1KOhm HR55 CPU_CFG1
GND 1KOhm HR57 CPU_CFG2
GND 1KOhm HR59 CPU_CFG3
GND 1KOhm HR92 CPU_CFG16

PLT_RSTL_R OR632 1% 200Ohm +3V
HR100 1% 100Ohm
VIDSOUT HR73 1% 110Ohm
VIDALERT# HR76 75OHM
H_CATERR_N HR79 1KOhm
PECI HR82 1KOhm CPU_VTT
PROCHOT# HR37 51Ohm
CPUPWRGD HR87 1KOhm
CPUPWRGD must pull down. HR110 1KOhm
C10029 18PF/50V
PROC_SEL HR91 2.2KOhm V_NAND_IO
HC19 0.1UF/16V
GND

1%
HR108 1KOhm
VCCM
CPU_DDR_VREF
1%
HR109 1KOhm
GND
HC20 0.1UF/16V

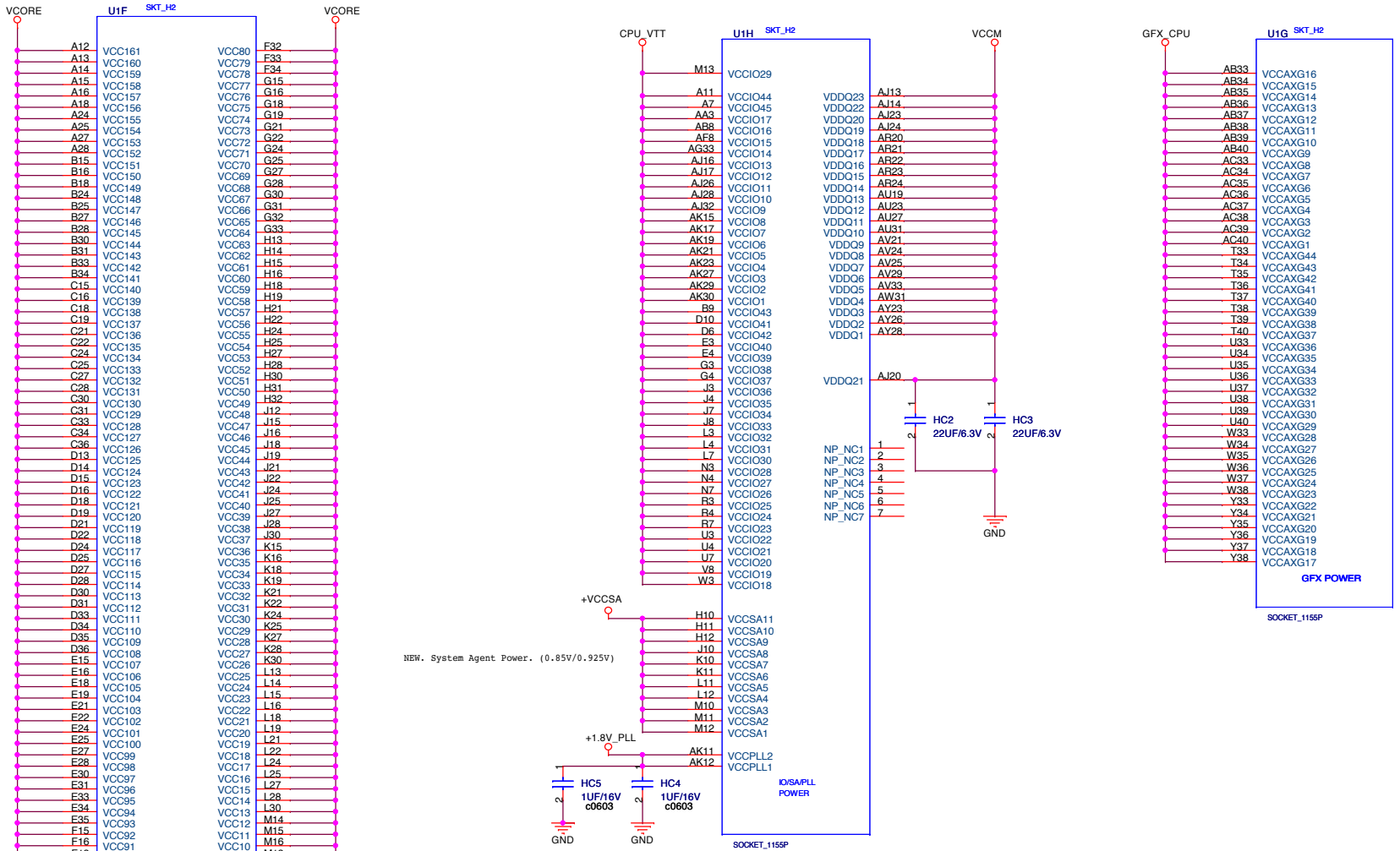
10 PCH_PECI
17 SIO_PECI
HR41 0Ohm PECI
HR52 0Ohm PECI

B75M-DGS

ASRock Inc. Title : CPU-MISC
Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 5 of 48



B75M-DGS

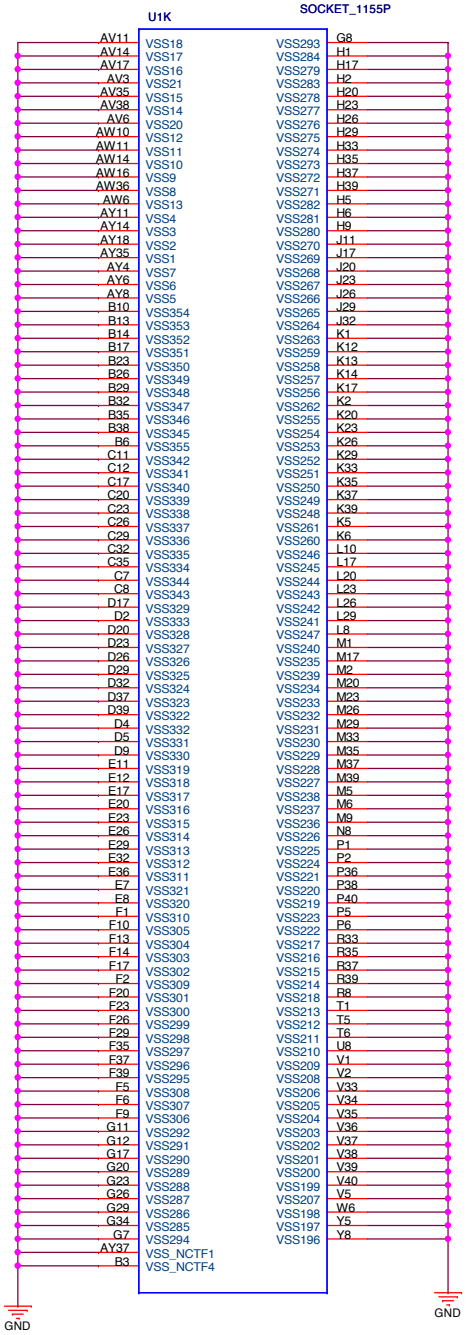
ASRock Inc.

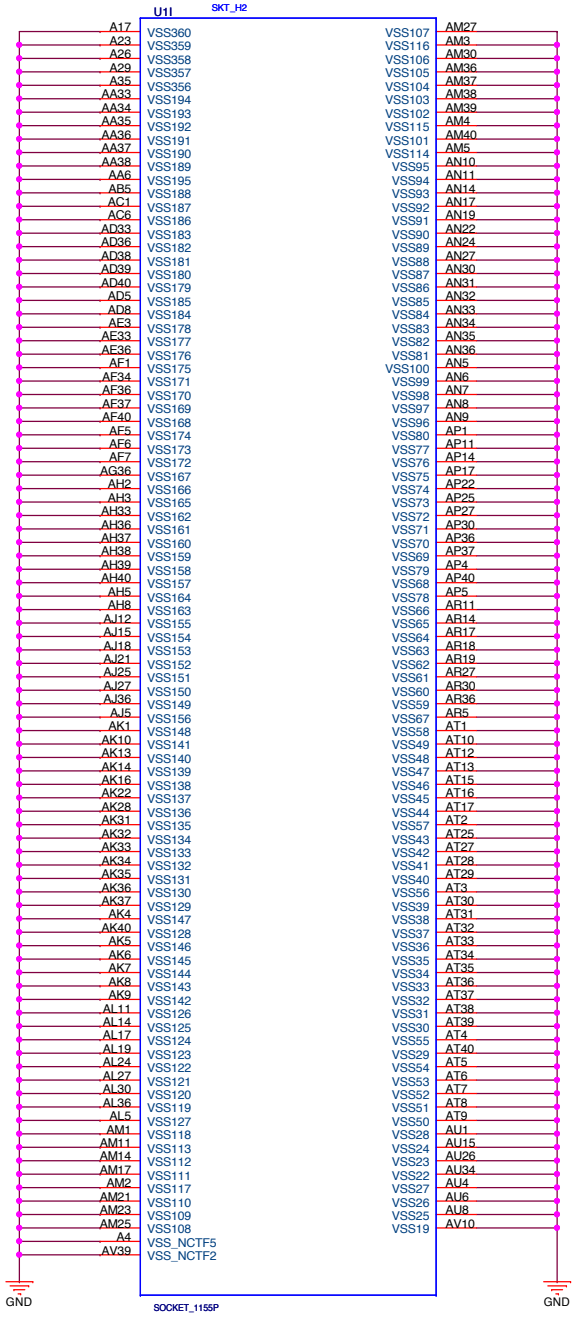
Title : CPU - Power

Engineer: Chia-wei Chang

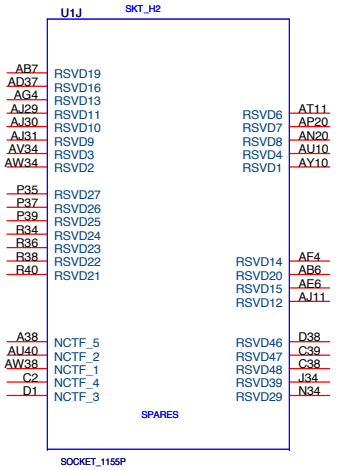
Size	Project Name	Rev
A3	B75M-DGS	2.00

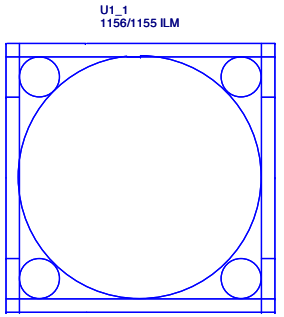
Date: Thursday, November 22, 2012 Sheet 6 of 48





All reserved. No connected.





B75M-DGS

ASRock Inc.

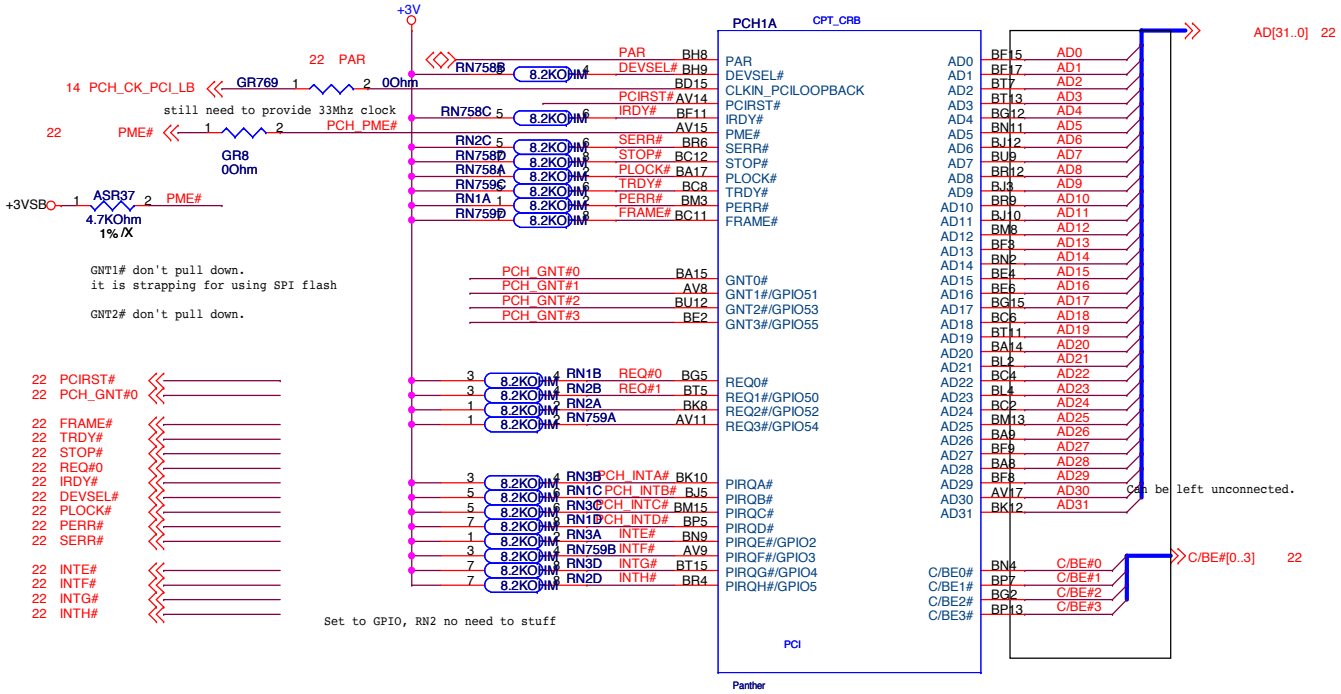
Title : CPU - GND

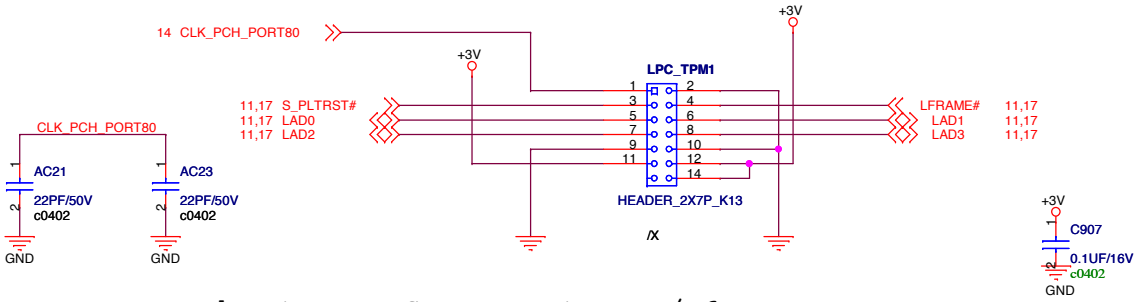
Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 7 of 48

Q77 support PCI. Check PCI solution!!!
H67/P67 do not support PCI. Check PCI solution!!!





due to no PCI support on H/P6x.
Reserved in case not boot up. Can be reomved.

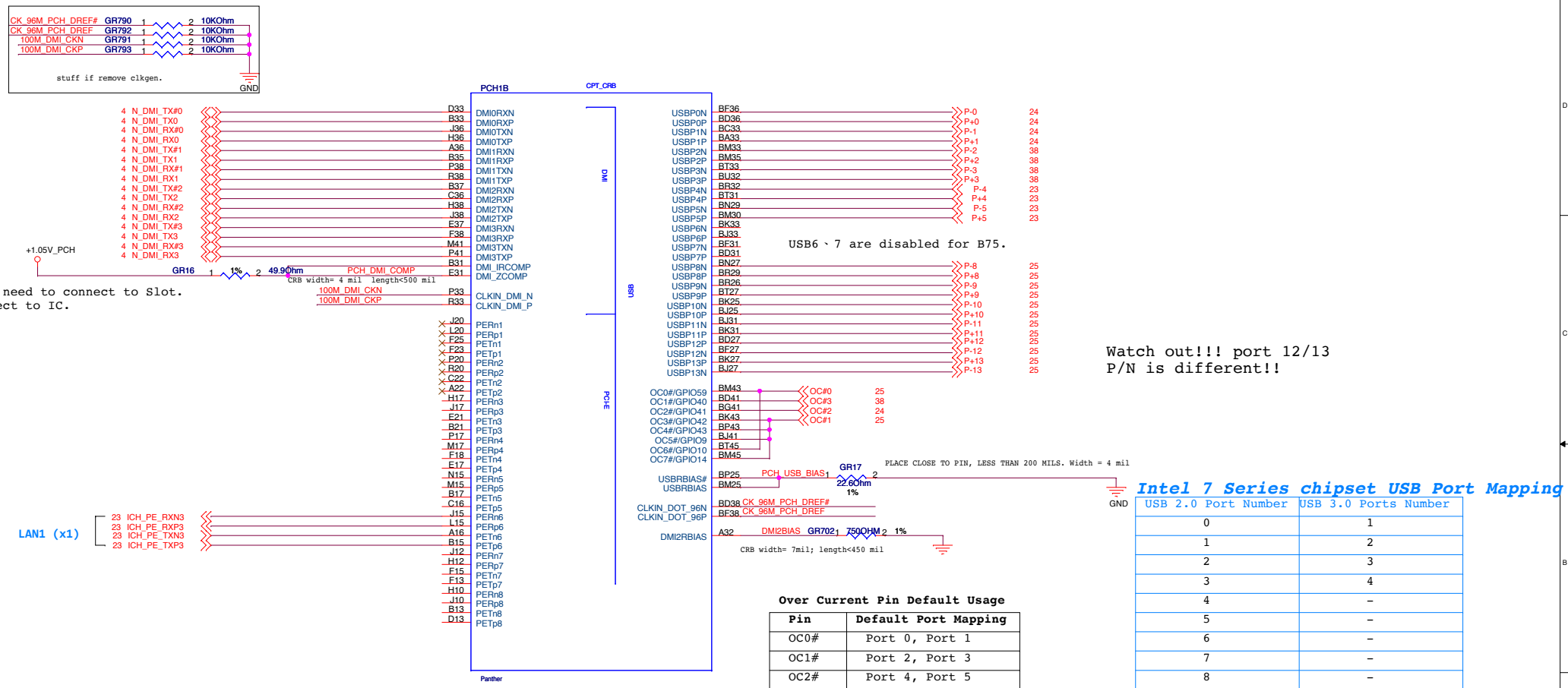
B75M-DGS

ASRock Title :SATA/HOST

ASRock Inc. Engineer: Chia-wei Chang

Size	Project Name	Rev
B	B75M-DGS	2.00

Date: Monday, November 26, 2012 Sheet 8 of 48



Over Current Pin Default Usage

Pin	Default Port Mapping
OC0#	Port 0, Port 1
OC1#	Port 2, Port 3
OC2#	Port 4, Port 5
OC3#	Port 6, Port 7
OC4#	Port 8, Port 9
OC5#	Port 10, Port 11
OC6#	Port 12, Port 13
OC7#	Not Used

Intel 7 Series chipset USB Port Mapping

USB 2.0 Port Number	USB 3.0 Ports Number
0	1
1	2
2	3
3	4
4	–
5	–
6	–
7	–
8	–
9	–
10	–
11	–
12	–
13	–

B75M-DGS

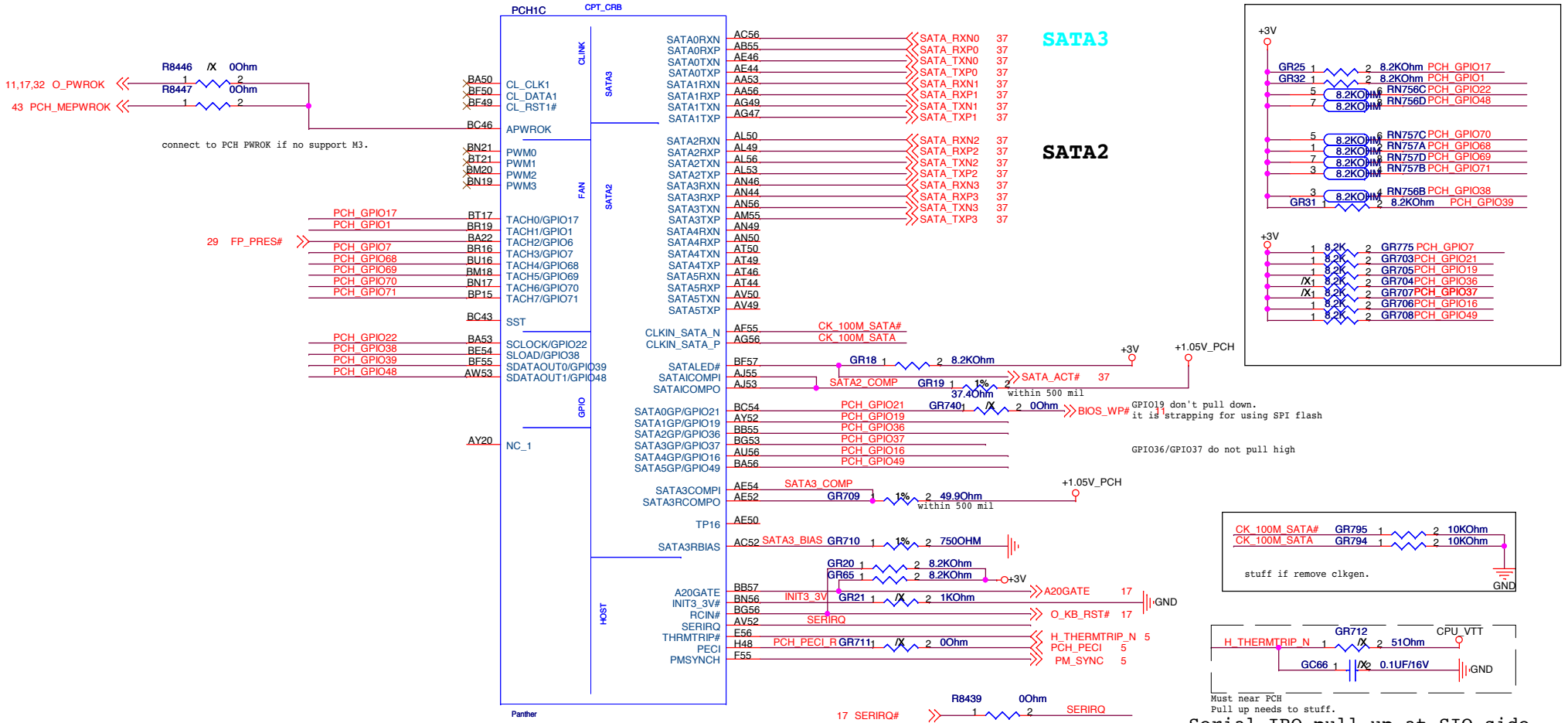
ASRock Inc.

Title : PCIEDMIUSB

Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 9 of 48



B75M-DGS

ASRock Inc.

Title : SATA/HOST

Engineer: Chia-wei Chang

Size	Project Name	Rev
B	B75M-DGS	2.00

Date: Wednesday, November 28, 2012 Sheet 10 of 48

	HIGH	LOW
GPIO8(IPU)	BTM	FCIM

Enable Internal VRM

GPIO28	High
HDA_SYNC	Low

DSW Sequence

tie together if SIO does not control DSW.

Pull High/Low

Flash descriptor overide

FET Control

make sure have ATX+5V to +3VSB_A Power in DC to DC page!

DPWROK DELAY

SPI ROM

SPI_MOSI do not pull high

RTC

RTCX1 and RTCX2 width=4,Length=<1

PWR LED BLINK

Change from GPIO27 to GPIO15

B75M-DGS

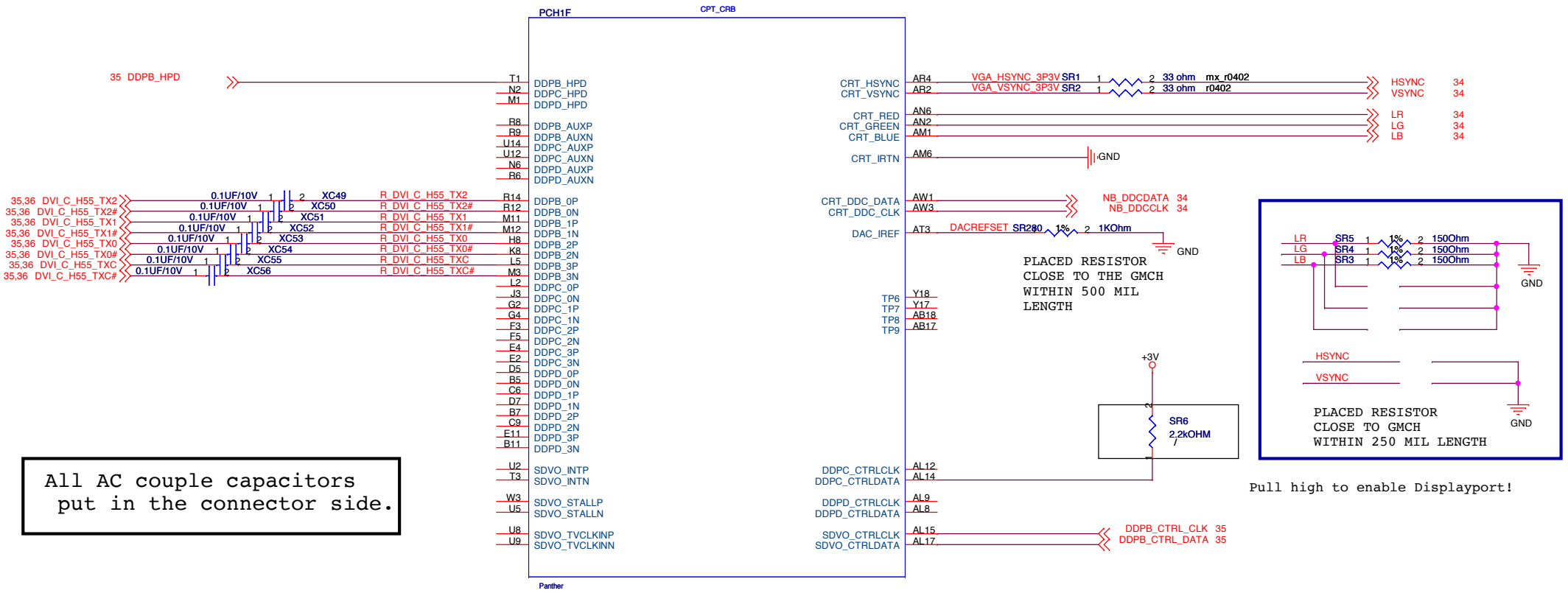
ASRock Inc.

Title : AUDIO/MISC

Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Tuesday, November 27, 2012 Sheet 11 of 48



All AC couple capacitors put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following

Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

B75M-DGS

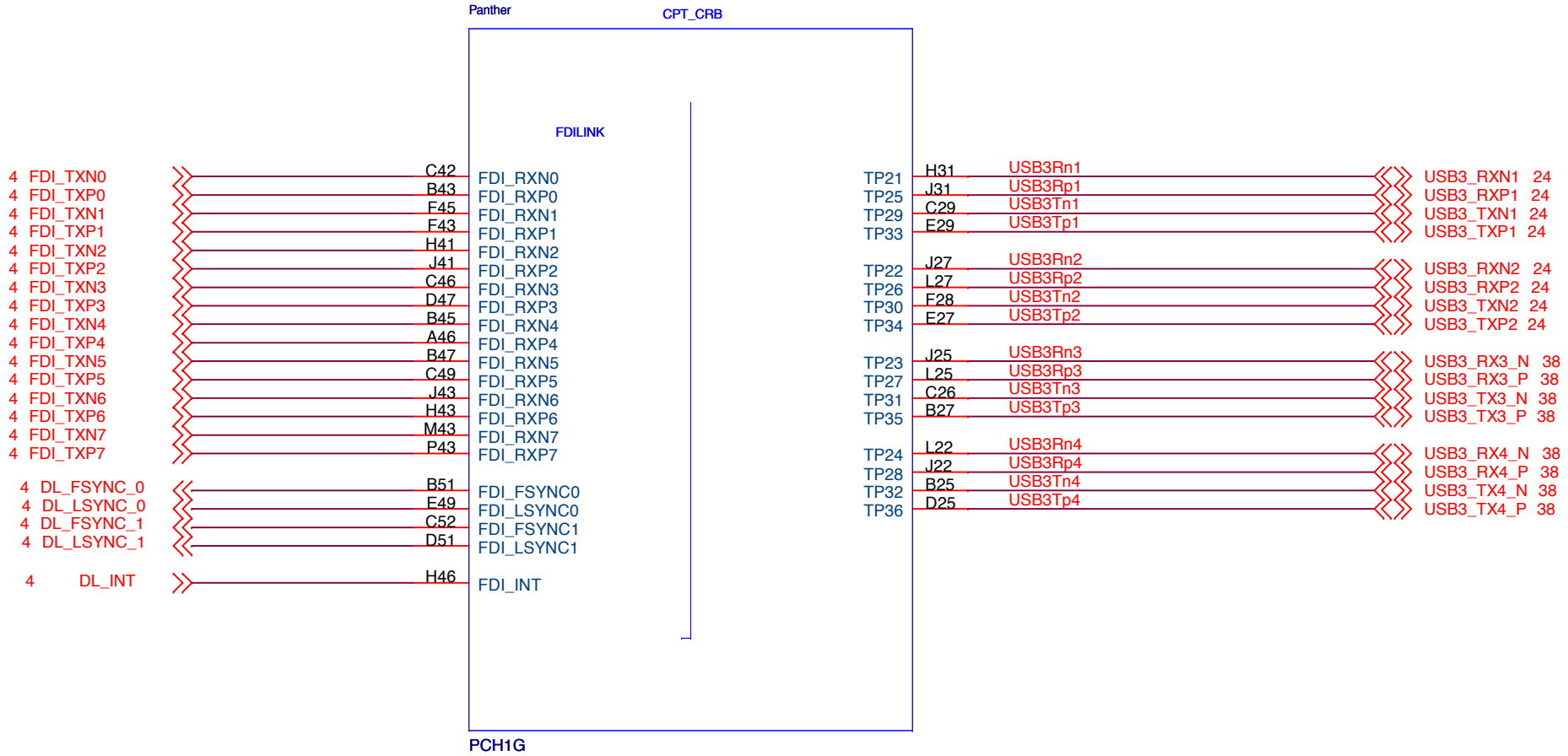
ASRock Inc.

Title : Clock Distribution

Engineer: Chia-wei Chang

Size	Project Name	Rev
B	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 12 of 48



B75M-DGS

ASRock Inc.

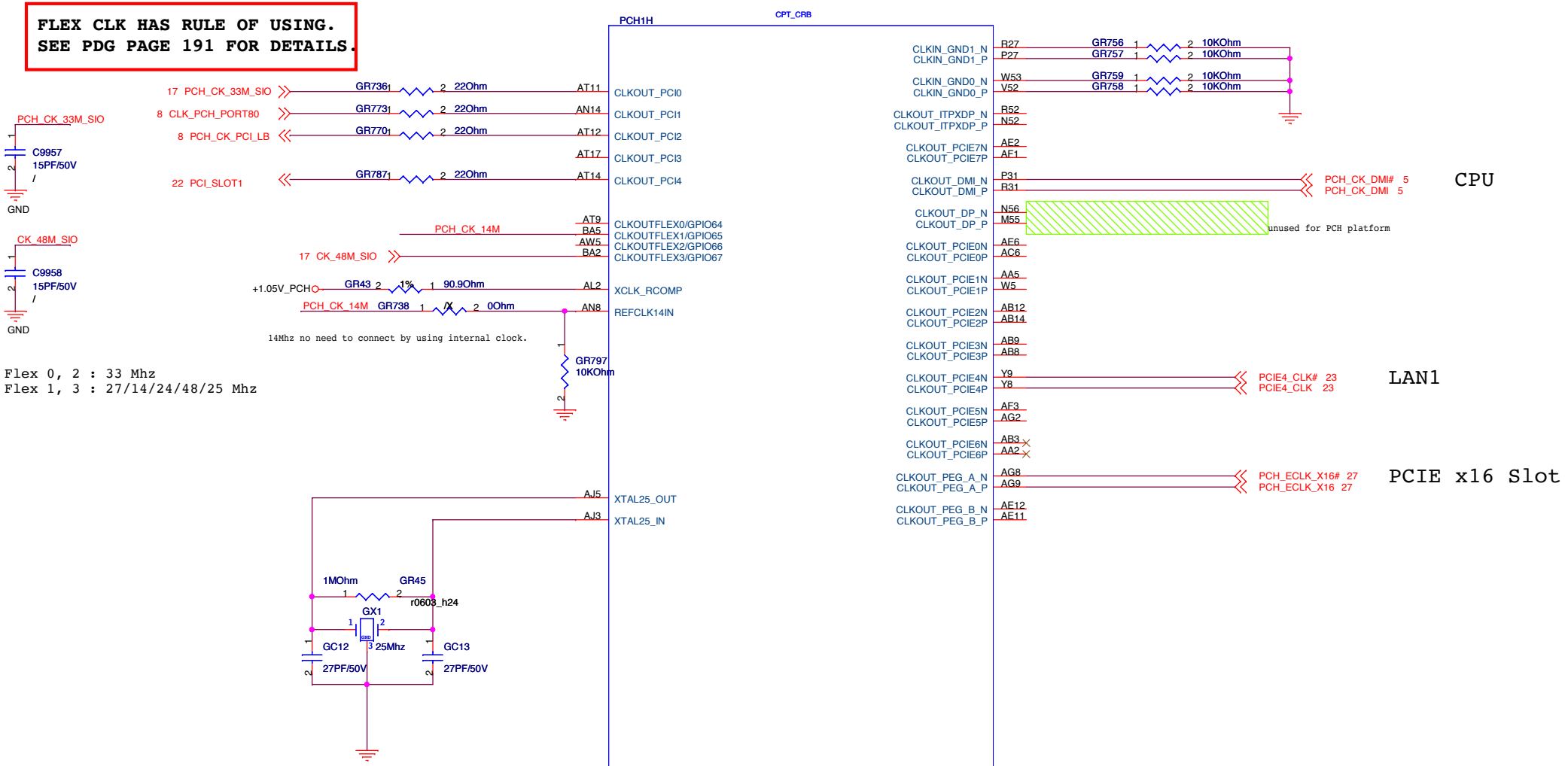
Title : FDI & USB3.0

Engineer: Chia-wei Chang

Size	Project Name	Rev
A	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 13 of 48

FLEX CLK HAS RULE OF USING.
SEE PDG PAGE 191 FOR DETAILS.



B75M-DGS

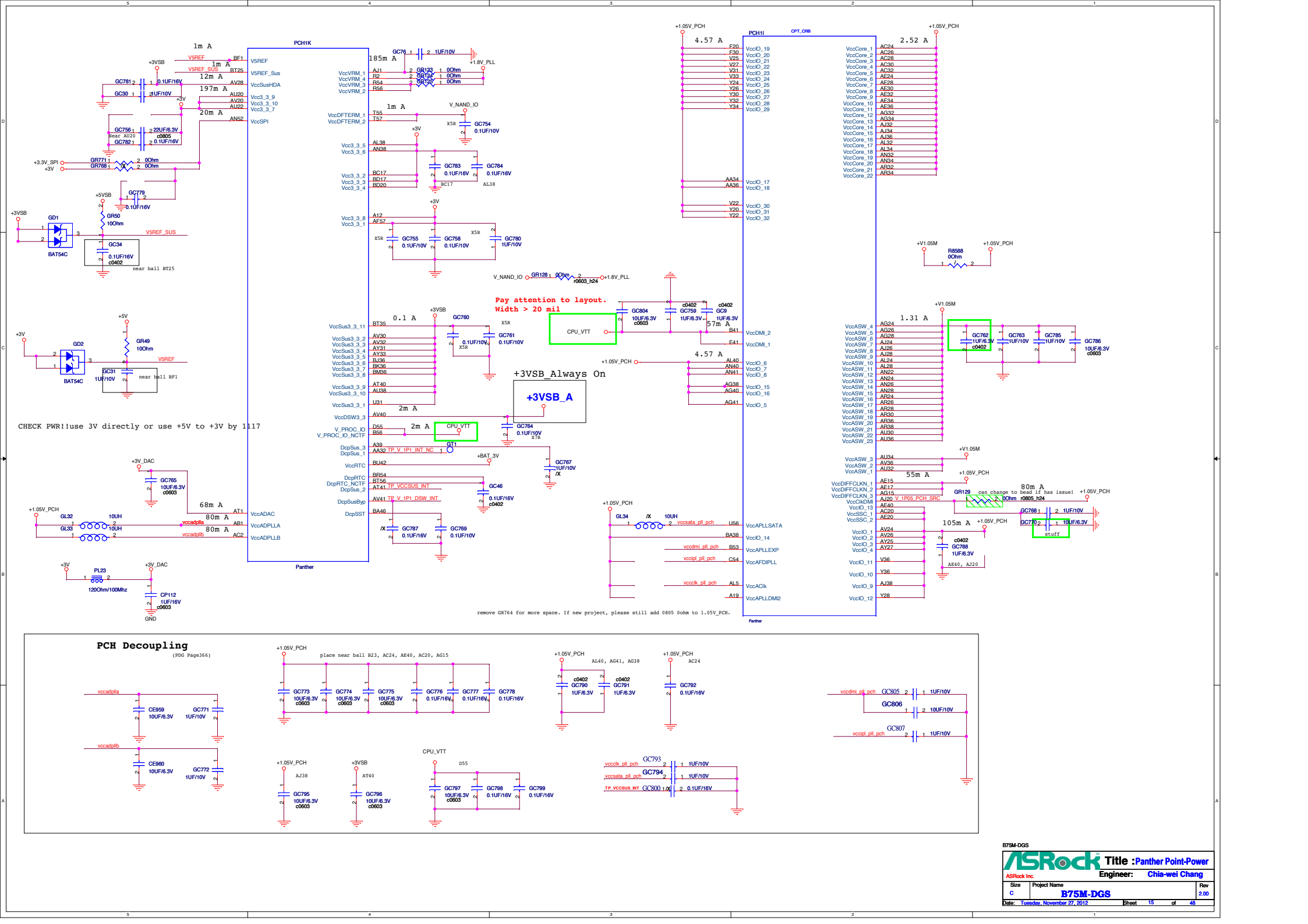
ASRock Inc.

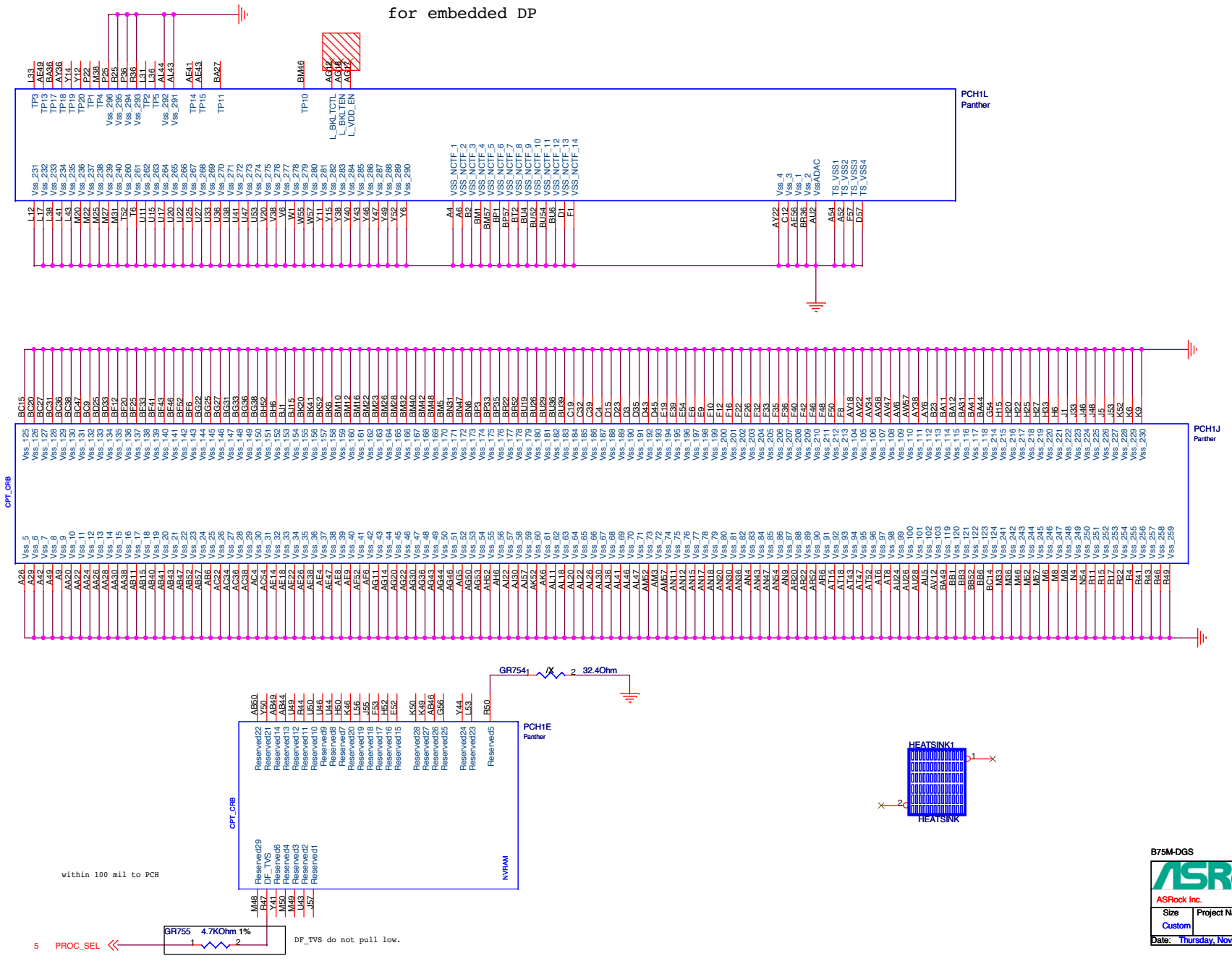
Title :CLK

Engineer: Chia-wei Chang

Size	Project Name	Rev
B	B75M-DGS	2.00

Date: Tuesday, November 27, 2012 Sheet 14 of 48


PCH1K
Panther
PCH1I
CPT_CRB
Pay attention to layout.
Width > 20 mil
+3VSB_Always On
+3VSB_A
CPU_VTT
CHECK PWR!!use 3V directly or use +5V to +3V by 1117
remove GR764 for more space. If new project, please still add 0805 0ohm to 1.05V_PCH.
PCH Decoupling
(PDG Page366)
place near ball B23, AC24, AE40, AC20, AG15
AL40, AG41, AG38
AC24
AJ38
AT40
D55
B75M-DGS
ASRock
Title :Panther Point-Power
ASRock Inc.
Engineer: Chia-wei Chang
Size C
Project Name B75M-DGS
Rev 2.00
Date: Tuesday, November 27, 2012
Sheet 15 of 48



B75M-DGS

ASRock Inc.

Title : Panther Point-GND

Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 16 of 48

677:SLOTOCC#
667:SLOTOCC

Clock source select.

VREF= 2.048V

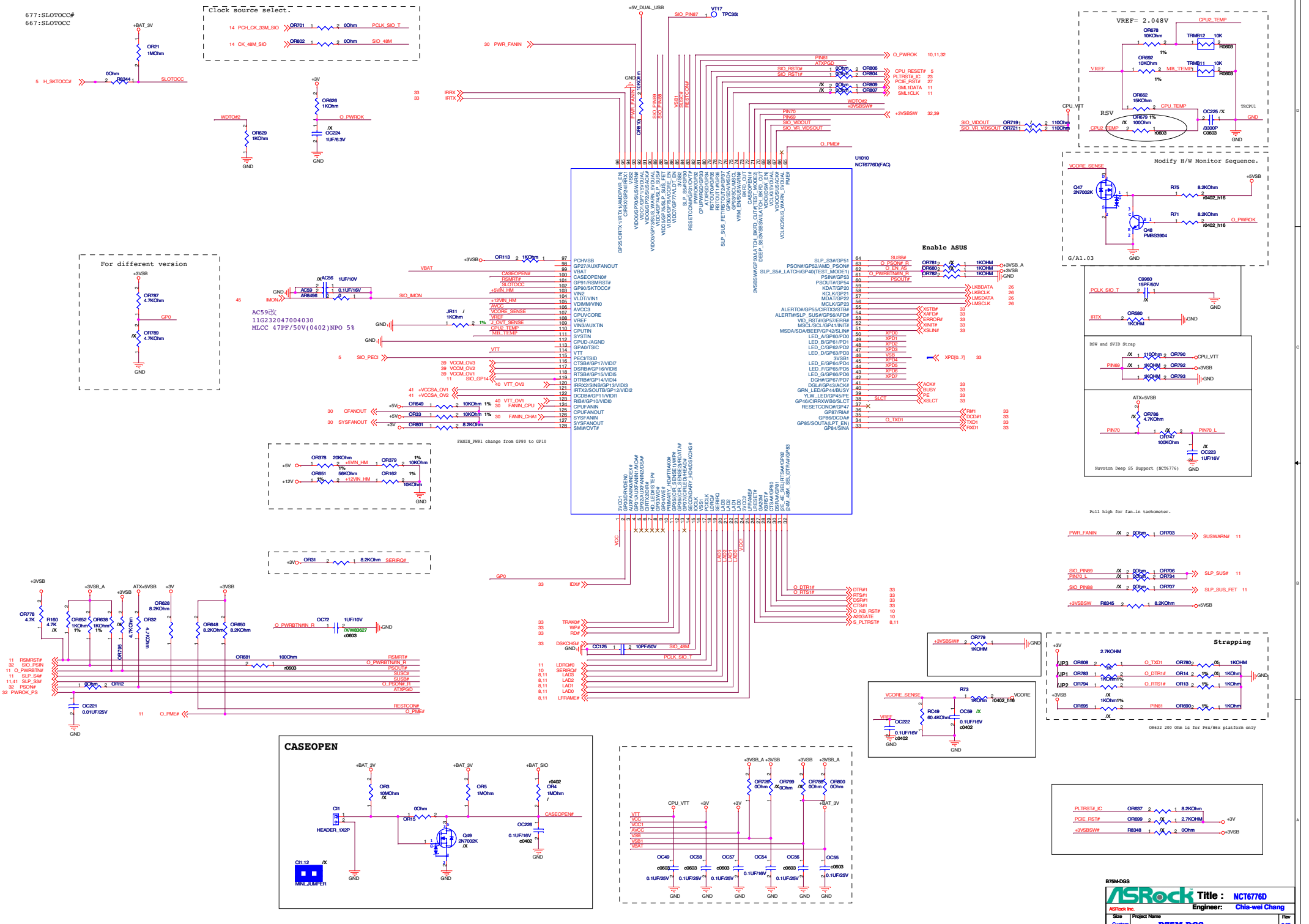
Modify H/W Monitor Sequence.

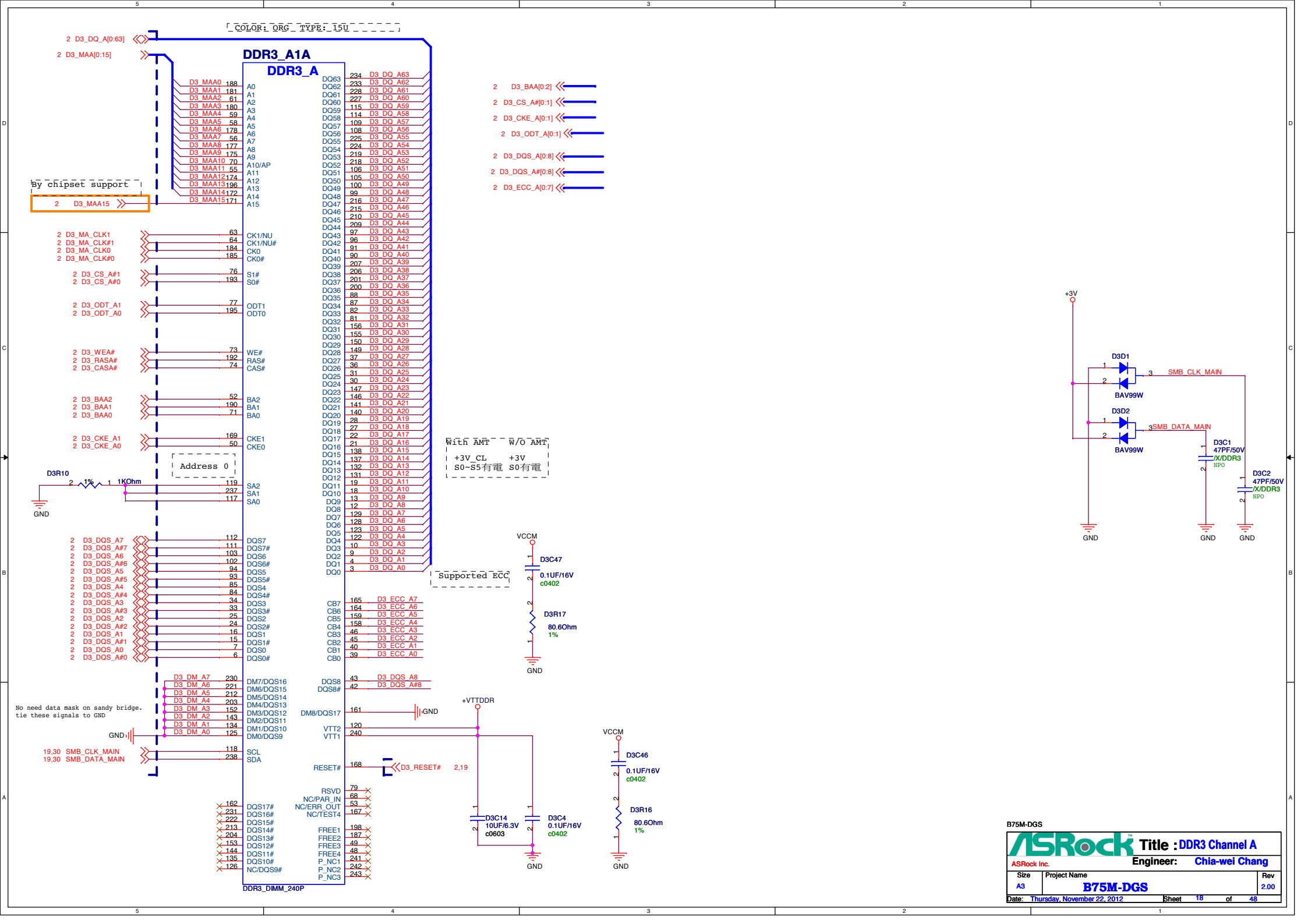
Enable ASUS

For different version

CASEOPEN

Strapping





B75M-DGS

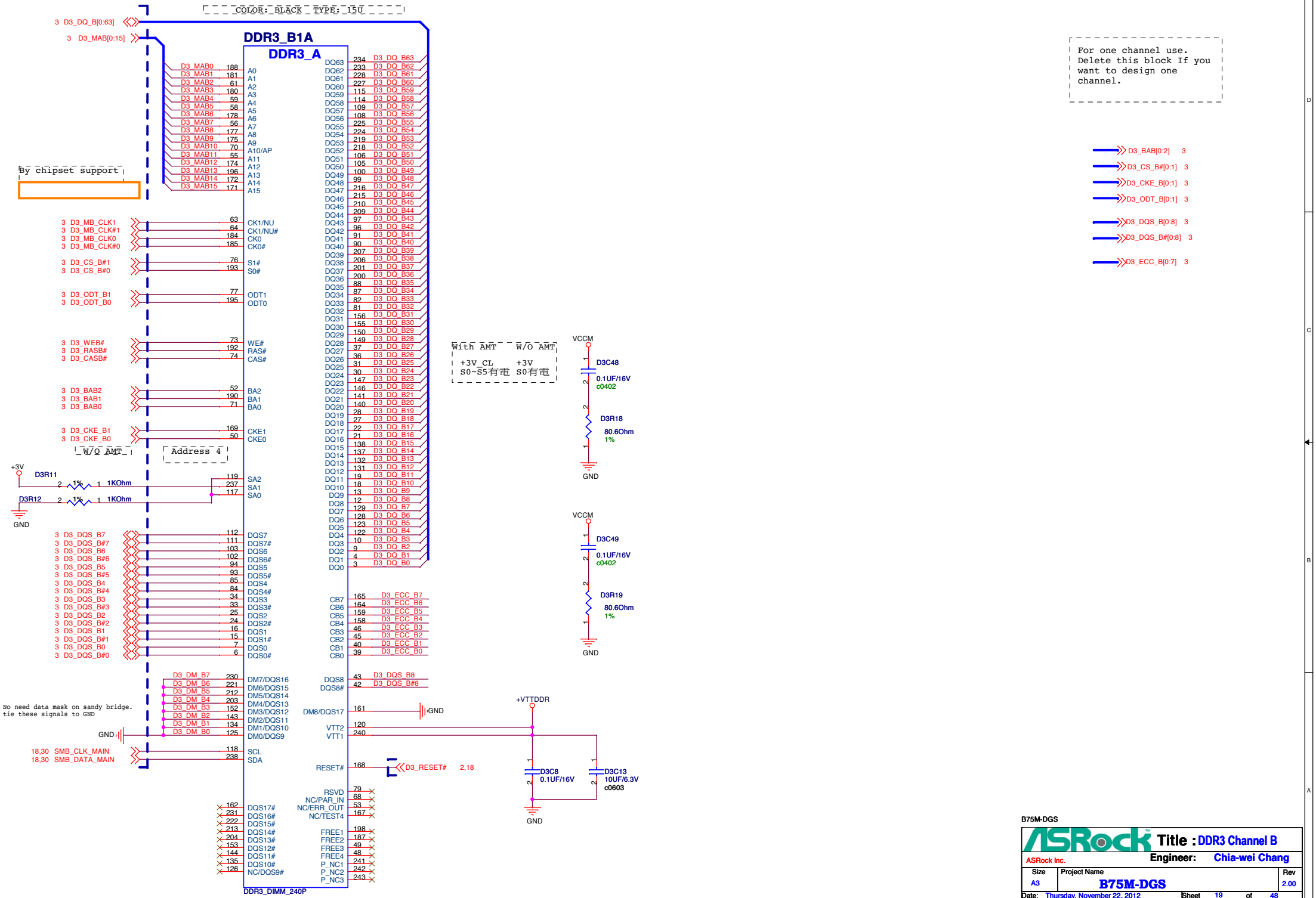
ASRock Inc.

Title : DDR3 Channel A

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 18 of 48



B75M-DGS

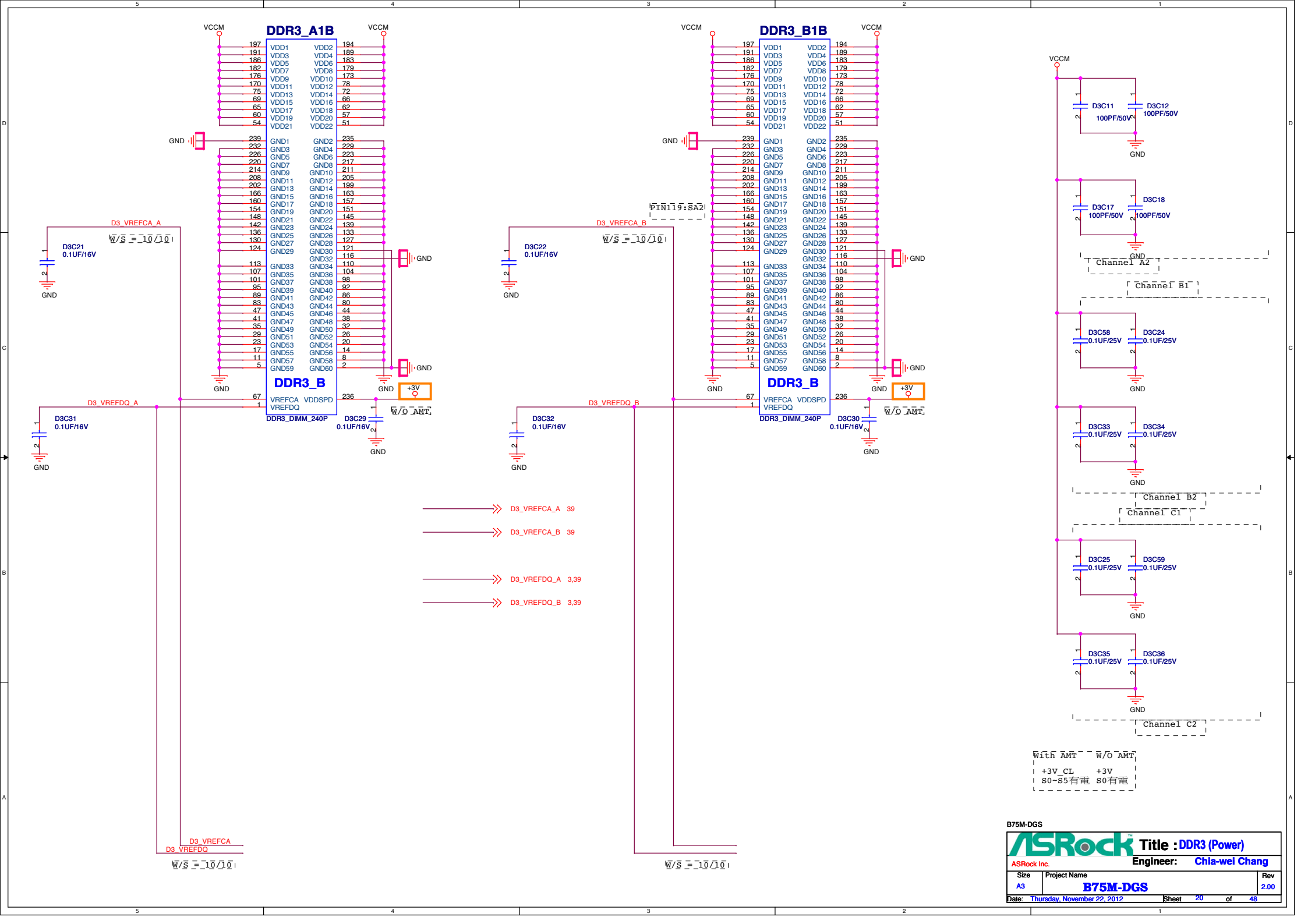
ASRock Inc.

Title : DDR3 Channel B

Engineer: Chia-wei Chang

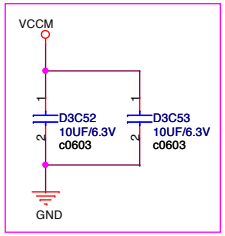
Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 19 of 48

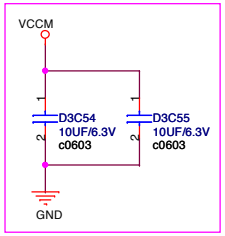

DDR3_A1B
DDR3_B1B
DDR3_B
DDR3_DIMM_240P
VCCM
GND
+3V
D3_VREFCA_A
D3_VREFCA_B
D3_VREFDQ_A
D3_VREFDQ_B
D3_VREFCA
D3_VREFDQ
W/S=10/10
W/O AMT
PIN119:SA2
D3C21 0.1UF/16V
D3C22 0.1UF/16V
D3C31 0.1UF/16V
D3C32 0.1UF/16V
D3C29 0.1UF/16V
D3C30 0.1UF/16V
D3_VREFCA_A 39
D3_VREFCA_B 39
D3_VREFDQ_A 3,39
D3_VREFDQ_B 3,39
D3C11 100PF/50V
D3C12 100PF/50V
D3C17 100PF/50V
D3C18 100PF/50V
Channel A2
Channel B1
D3C58 0.1UF/25V
D3C24 0.1UF/25V
D3C33 0.1UF/25V
D3C34 0.1UF/25V
Channel B2
Channel C1
D3C25 0.1UF/25V
D3C59 0.1UF/25V
D3C35 0.1UF/25V
D3C36 0.1UF/25V
Channel C2
With AMT W/O AMT
+3V_CL +3V
S0~S5有電 S0有電
B75M-DGS
Title : DDR3 (Power)
ASRock Inc.
Engineer: Chia-wei Chang
Size A3
Project Name B75M-DGS
Rev 2.00
Date: Thursday, November 22, 2012
Sheet 20 of 48

c.w. huang:Add 10uF cap. to improve DDR3 over clock.

channel A



channel B



B75M-DGS

ASRock Inc.

Title : DDR3 (Power 2)

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 21 of 48

8 AD[31..0]
8 C/BE#[0..3]
8 DEVSEL#
8 IRDY#
8 STOP#
8 REQ#0
8 PCH_GNT#0
GNT#0
8 INTG#
8 INTF#
8 INTE#
8 INTH#
8 SERR#
8 PAR
8 PME#
8 PCIRST#
8 FRAME#
8 TRDY#
8 PLOCK#
8 PERR#

PCI SLOT1

EFGH
IDSEL AD17

PCI1

+3V +5V -12V +12V +5V +3V +3VSB

B1	-12V		A1	TRST			
B2	TCK		A2	+12V			
B3	GND11		A3	TMS			
B4	TDO		A4	TDI			
B5	+5V22		A5	+5V1			
B6	+5V23		A6	INTA		INTE#	
INTF# B7	INTB		A7	INTC		INTG#	
INTH# B8	INTD		A8	+5V2			
B9	PRSNT1		A9	RESERVED1			
B10	RESERVED5		A10	+5V3			
B11	PRSNT2		A11	RESERVED2			
B12	GND12		A12	GND1			
B13	GND13		A13	GND2			
B14	RESERVED6		A14	RESERVED3			
B15	GND14		A15	RST		PCIRST#	
PCI_S1 B16	CLK		A16	+5V4			
B17	GND15		A17	GNT		GNT#0	
REQ#0 B18	REQ		A18	GND3			
B19	+5V8		A19	RESERVED4		PME#	
AD31 B20	AD31		A20	AD30		AD30	
AD29 B21	AD29		A21	+3.3V1			
B22	GND16		A22	AD28		AD28	
AD27 B23	AD27		A23	AD26		AD26	
AD25 B24	AD25		A24	GND4			
B25	+3.3V7		A25	AD24		AD24	
C/BE#3 B26	C/BE3		A26	IDSEL		1 2 AD17	
AD23 B27	AD23		A27	+3.3V2		ASR42 0Ohm	
B28	GND17		A28	AD22		AD22	
AD21 B29	AD21		A29	AD20		AD20	
AD19 B30	AD19		A30	GND5			
B31	+3.3V8		A31	AD18		AD18	
AD17 B32	AD17		A32	AD16		AD16	
C/BE#2 B33	C/BE2		A33	+3.3V3			
B34	GND18		A34	FRAME		FRAME#	
IRDY# B35	IRDY		A35	GND6			
B36	+3.3V9		A36	TRDY		TRDY#	
DEVSEL# B37	DEVSEL		A37	GND7			
B38	GND19		A38	STOP		STOP#	
PLOCK# B39	LOCK		A39	+3.3V4			
PERR# B40	PERR		A40	SDONE			
B41	+3.3V10		A41	SBO			
SERR# B42	SERR		A42	GND8			
B43	+3.3V11		A43	PAR		PAR	
C/BE#1 B44	C/BE1		A44	AD15		AD15	
AD14 B45	AD14		A45	+3.3V5			
B46	GND20		A46	AD13		AD13	
AD12 B47	AD12		A47	AD11		AD11	
AD10 B48	AD10		A48	GND9			
B49	GND21		A49	AD9		AD9	
AD8 B52	AD8		A52	C/BE0		C/BE#0	
AD7 B53	AD7		A53	+3.3V6			
B54	+3.3V12		A54	AD6		AD6	
AD5 B55	AD5		A55	AD4		AD4	
AD3 B56	AD3		A56	GND10			
B57	GND22		A57	AD2		AD2	
AD1 B58	AD1		A58	AD0		AD0	
B59	+5V9		A59	+5V5			
B60	ACK64		A60	REQ64		REQ64#S1	
B61	+5V10		A61	+5V6			
B62	+5V11		A62	+5V7			

hold_NC1 hold_NC2

120P

+3V
R209 2.7K
REQ64#S1 1 2

Clock

R210 0Ohm
PCI_S1 1 2 PCI_SLOT1 14

+5V
C523 0.1UF/16V c0402
C524 0.1UF/16V c0402
C516 0.1UF/16V c0402
GND

+3V
C148 0.1UF/16V c0402
C147 0.1UF/16V c0402
GND

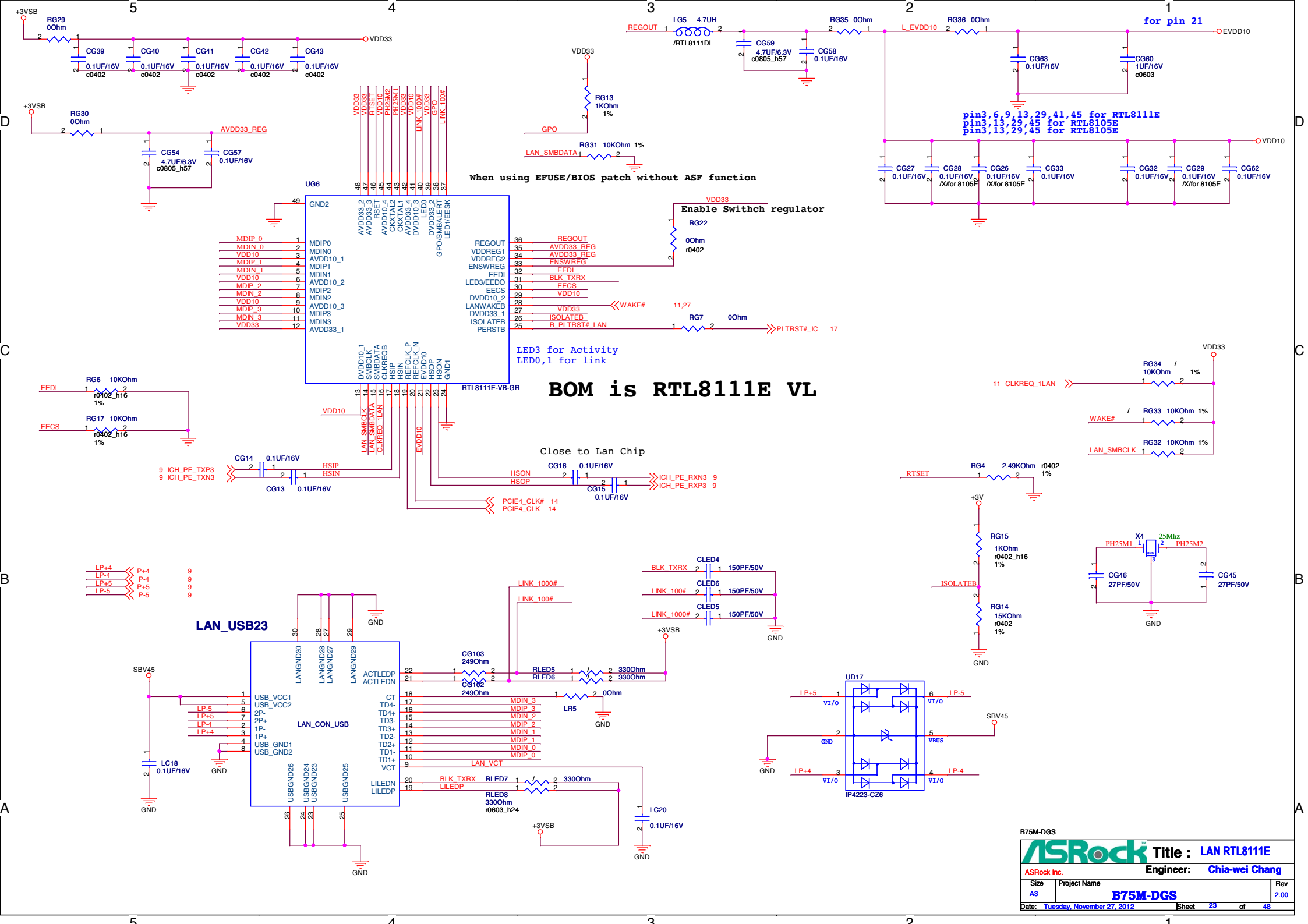
B75 Pro3-M

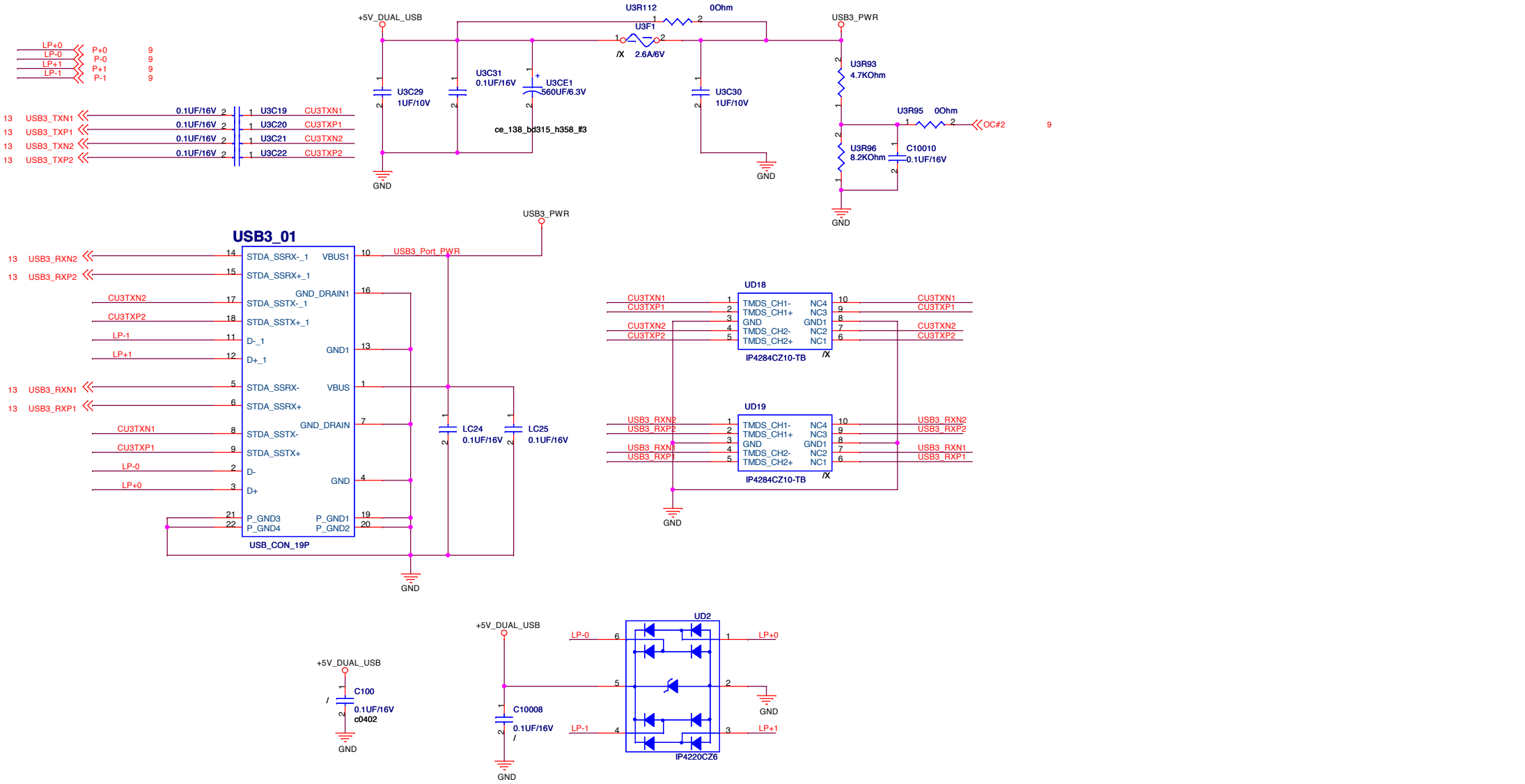
ASRock Inc.

Title : PCI Slot
Engineer: Chia-Wei Chang

Size	Project Name	Rev
A3	B75 Pro3-M	2.00

Date: Thursday, November 22, 2012 Sheet 22 of 48


When using EFUSE/BIOS patch without ASF function
Enable Swithch regulator
LED3 for Activity
LED0,1 for link
BOM is RTL8111E VL
Close to Lan Chip
for pin 21
pin3,6,9,13,29,41,45 for RTL8111E
pin3,13,29,45 for RTL8105E
pin3,13,29,45 for RTL8105E
LAN_USB23
RTL8111E-VB-GR
LAN_CON_USB
IP4223-CZ6
B75M-DGS
Title : LAN RTL8111E
ASRock Inc.
Engineer: Chia-wei Chang
Size A3
Project Name B75M-DGS
Rev 2.00
Date: Tuesday, November 27, 2012
Sheet 23 of 48



B75M-DGS

ASRock Inc.

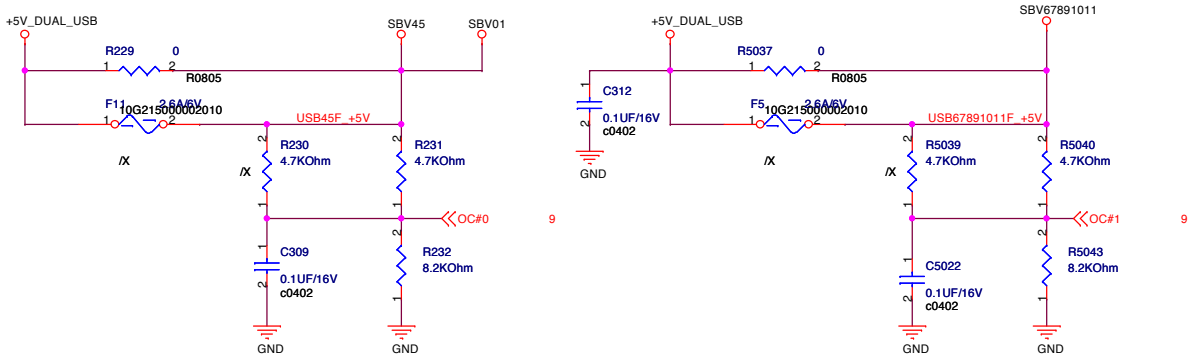
Title : LAN RTL8111E 2

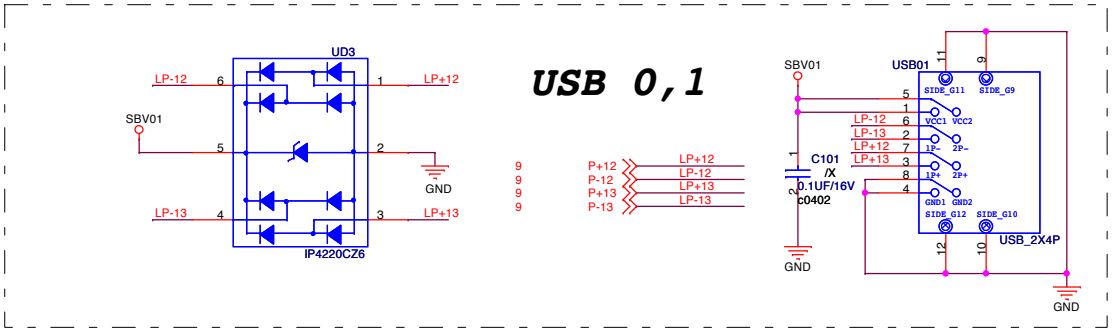
Engineer: Chia-wei Chang

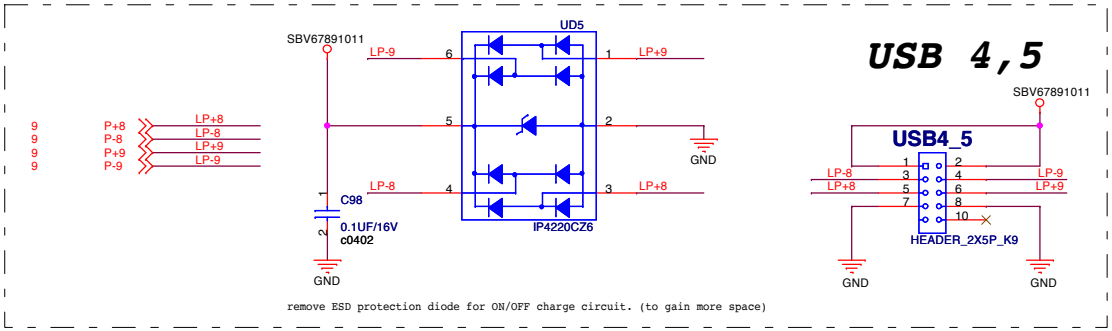
Size	Project Name	Rev
A3	B75M-DGS	2.00

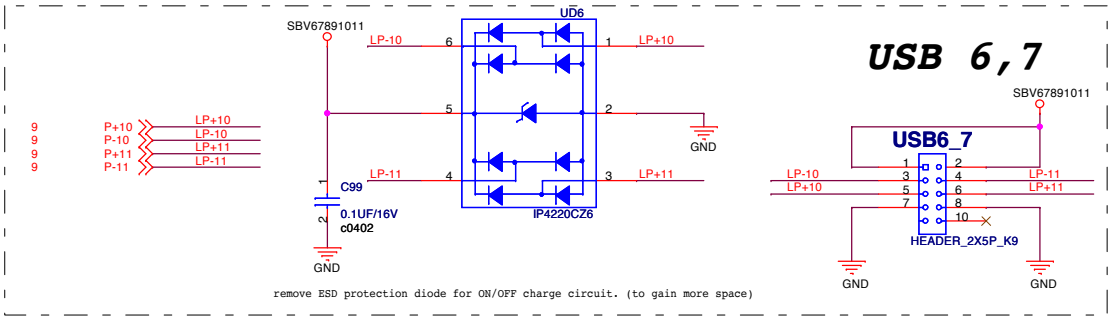
Date: Tuesday, November 27, 2012 Sheet 24 of 48

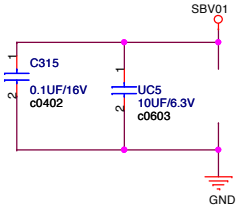
USB Power

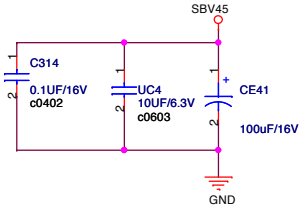


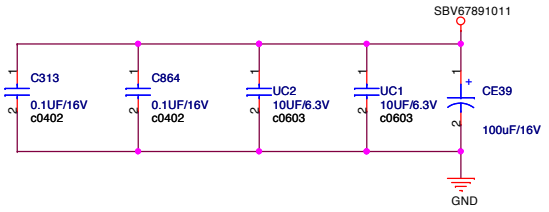






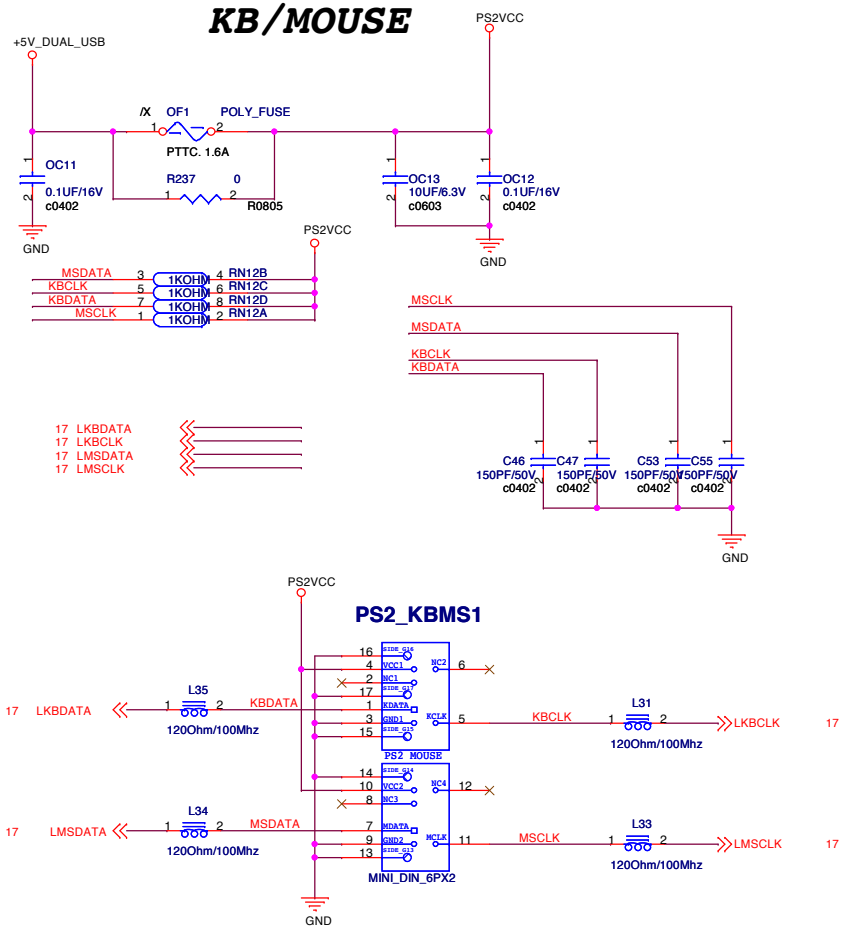






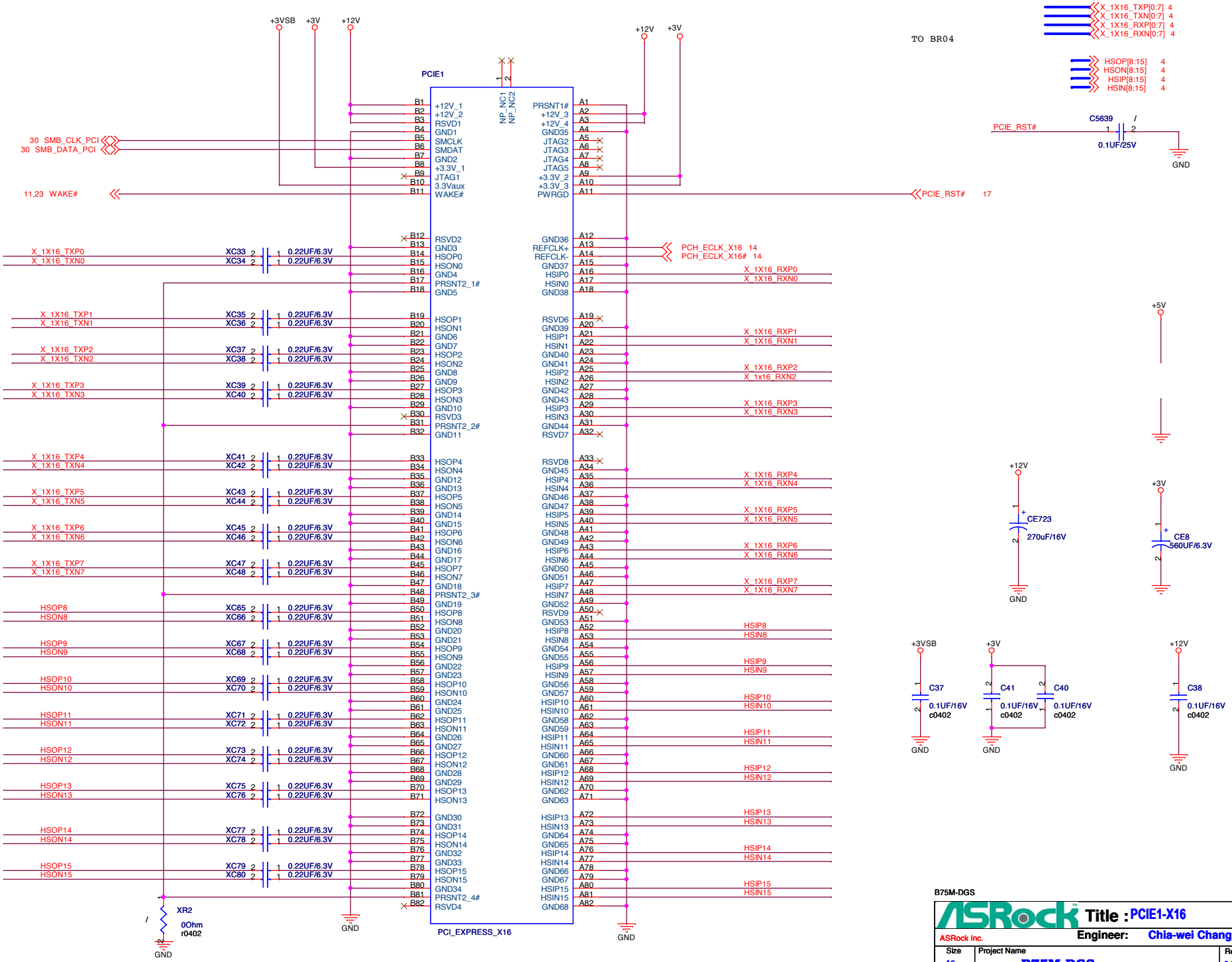
B75M-DGS

ASRock Inc.	Title : USB Port	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 25 of 48	



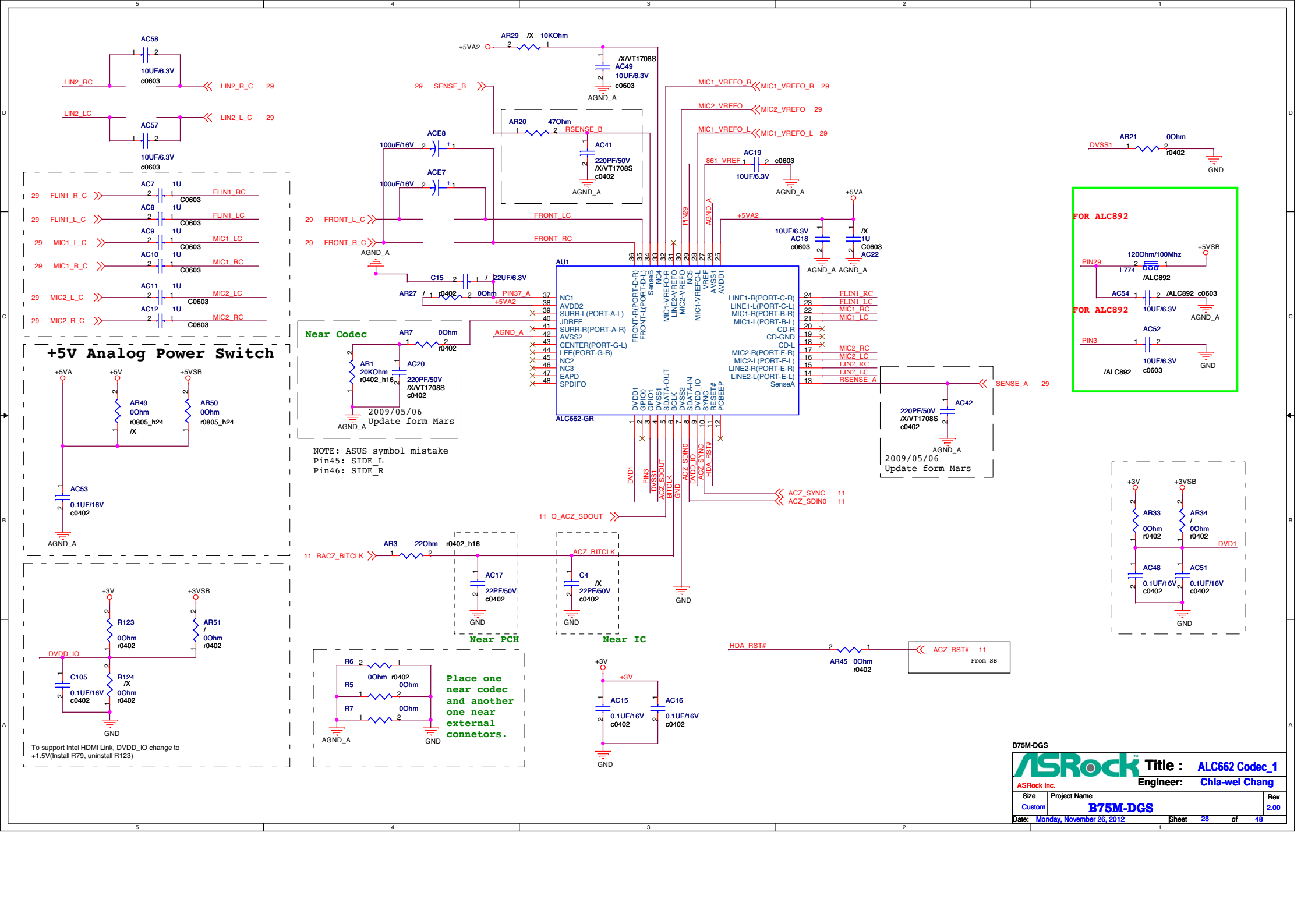
B75M-DGS

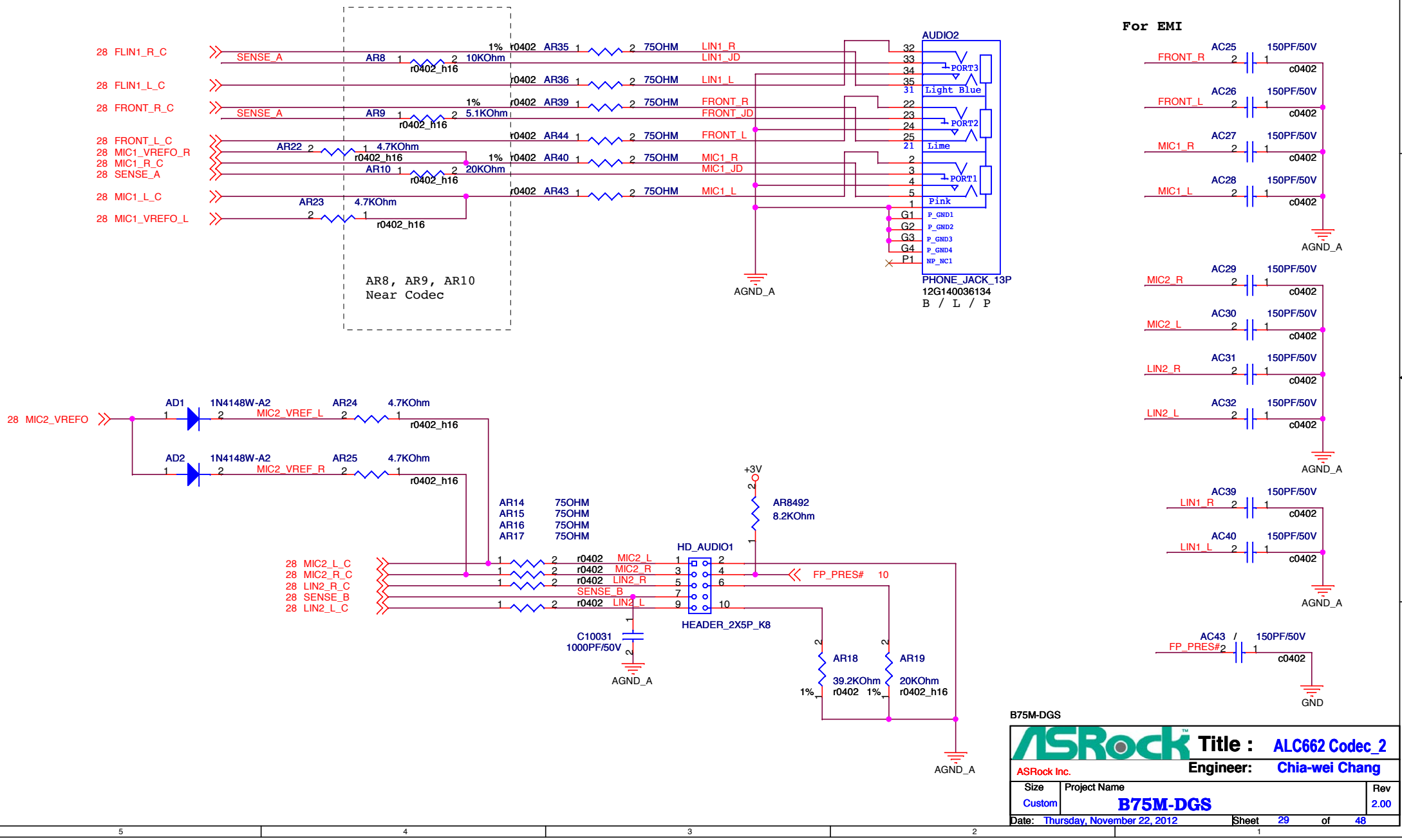
ASRock Inc.	Title : KB & MS	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Tuesday, November 27, 2012	Sheet 26 of 48	



B75M-DGS

ASRock Inc.	Title : PCIE1-X16	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 27 of 48	


AC58
LIN2_RC
LIN2_R_C 29
10UF/6.3V
c0603
AC57
LIN2_LC
LIN2_L_C 29
AR29 /X 10KOhm
+5VA2
/X/VT1708S
AC49
AGND_A
29 SENSE_B
AR20 47Ohm
RSENSE_B
AC41
220PF/50V
/X/VT1708S
c0402
ACE8
100uF/16V
ACE7
MIC1_VREFO_R
MIC2_VREFO
MIC1_VREFO_L
861_VREF
AC19
AC18
AC22
+5VA
AR21 0Ohm
DVSS1
r0402
GND
FOR ALC892
120Ohm/100Mhz
L774
/ALC892
AC54
AC52
10UF/6.3V
29 FLIN1_R_C
29 FLIN1_L_C
29 MIC1_L_C
29 MIC1_R_C
29 MIC2_L_C
29 MIC2_R_C
AC7
AC8
AC9
AC10
AC11
AC12
1U
C0603
FLIN1_RC
FLIN1_LC
MIC1_LC
MIC1_RC
MIC2_LC
MIC2_RC
29 FRONT_L_C
29 FRONT_R_C
FRONT_LC
FRONT_RC
C15 22UF/6.3V
AR27 0Ohm PIN37_A
+5VA2
AU1
NC1
AVDD2
SURR-L(PORT-A-L)
JDREF
SURR-R(PORT-A-R)
AVSS2
CENTER(PORT-G-L)
LFE(PORT-G-R)
NC2
NC3
EAPD
SPDIFO
FRONT-R(PORT-D-R)
FRONT-L(PORT-D-L)
SenseB
NC4
MIC1-VREFO-R
LINE2-VREFO-R
MIC2-VREFO
NC5
MIC1-VREFO-L
VREF
AVSS1
AVDD1
LINE1-R(PORT-C-R)
LINE1-L(PORT-C-L)
MIC1-R(PORT-B-R)
MIC1-L(PORT-B-L)
CD-R
CD-GND
CD-L
MIC2-R(PORT-F-R)
MIC2-L(PORT-F-L)
LINE2-R(PORT-E-R)
LINE2-L(PORT-E-L)
SenseA
DVDD1
GPIO0
GPIO1
DVSS1
SDATA-OUT
BCLK
DVSS2
SDATA-IN
DVDD_IO
SYNC
RESET#
PCBEEP
ALC662-GR
Near Codec
AR7 0Ohm
r0402
AR1
20KOhm
r0402_h16
AC20
220PF/50V
/X/VT1708S
c0402
2009/05/06
Update form Mars
NOTE: ASUS symbol mistake
Pin45: SIDE_L
Pin46: SIDE_R
SENSE_A 29
AC42
220PF/50V
/X/VT1708S
c0402
2009/05/06
Update form Mars
+5V Analog Power Switch
+5VA
+5V
+5VSB
AR49
0Ohm
r0805_h24
/X
AR50
0Ohm
r0805_h24
AC53
0.1UF/16V
c0402
AGND_A
11 Q_ACZ_SDOUT
ACZ_SYNC 11
ACZ_SDIN0 11
11 RACZ_BITCLK
AR3 22Ohm r0402_h16
ACZ_BITCLK
AC17
22PF/50V
c0402
C4
/X
22PF/50V
c0402
GND
Near PCH
Near IC
+3V
+3VSB
R123
0Ohm
r0402
AR51
/
0Ohm
r0402
DVDD_IO
C105
0.1UF/16V
c0402
R124
/X
0Ohm
r0402
To support Intel HDMI Link, DVDD_IO change to
+1.5V(Install R79, uninstall R123)
R6 0Ohm r0402
R5 0Ohm
R7 0Ohm
Place one
near codec
and another
one near
external
connetors.
AC15
AC16
0.1UF/16V
c0402
HDA_RST#
AR45 0Ohm
r0402
ACZ_RST# 11
From SB
AR33
AR34
AC48
AC51
0.1UF/16V
c0402
DVD1
B75M-DGS
ASRock
Title : ALC662 Codec_1
ASRock Inc.
Engineer: Chia-wei Chang
Size Custom
Project Name B75M-DGS
Rev 2.00
Date: Monday, November 26, 2012
Sheet 28 of 48



B75M-DGS

ASRock Inc.

Title : ALC662 Codec_2

Engineer: Chia-wei Chang

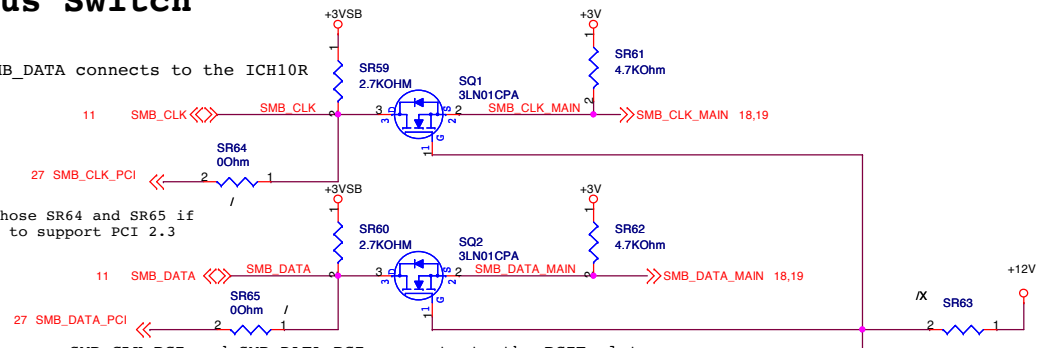
Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 29 of 48

SMBus Switch

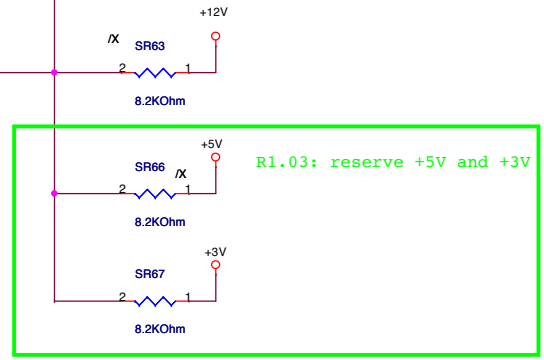
1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.
SMB_CLK and SMB_DATA for Standby device.
SMB_CLK_MAIN and SMB_DATA_MAIN for Main power device.

SMB_CLK and SMB_DATA connects to the ICH10R

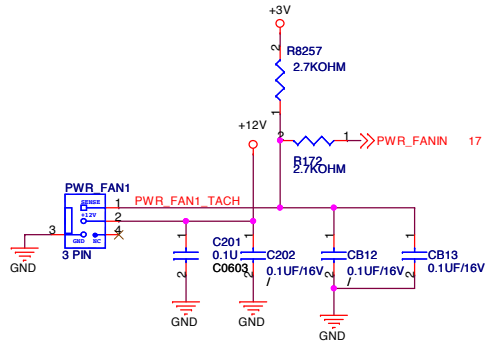


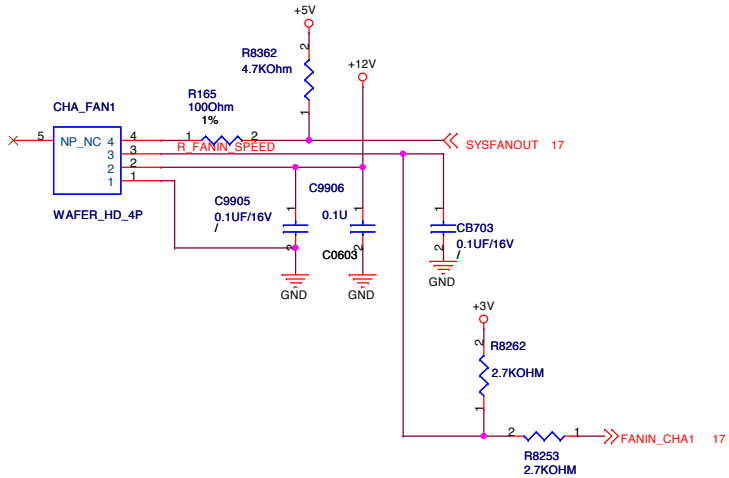
Mount those SR64 and SR65 if we want to support PCI 2.3

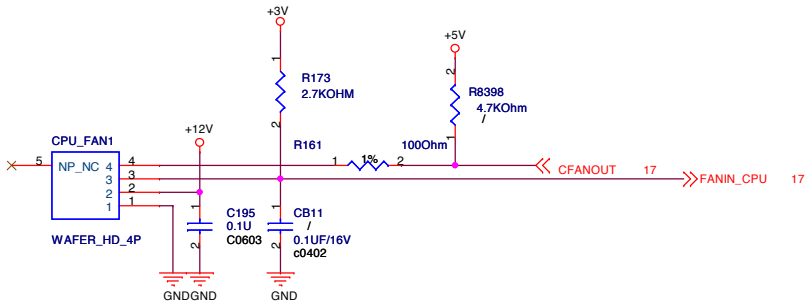
SMB_CLK_PCI and SMB_DATA_PCI connects to the PCIE slot



R1.03: reserve +5V and +3V







B75M-DGS

ASRock Inc.

Title : SMBUS SWITCH,FAN

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 30 of 48

B75M-DGS

Title : CPU FAN

ASRock Inc.

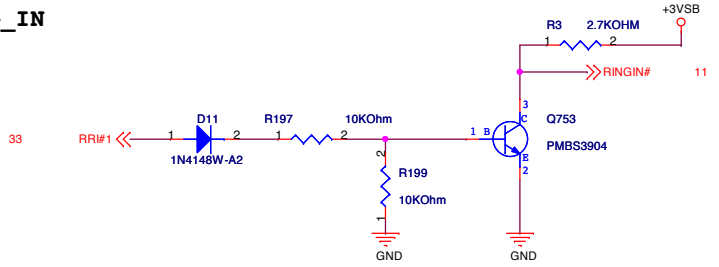
Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

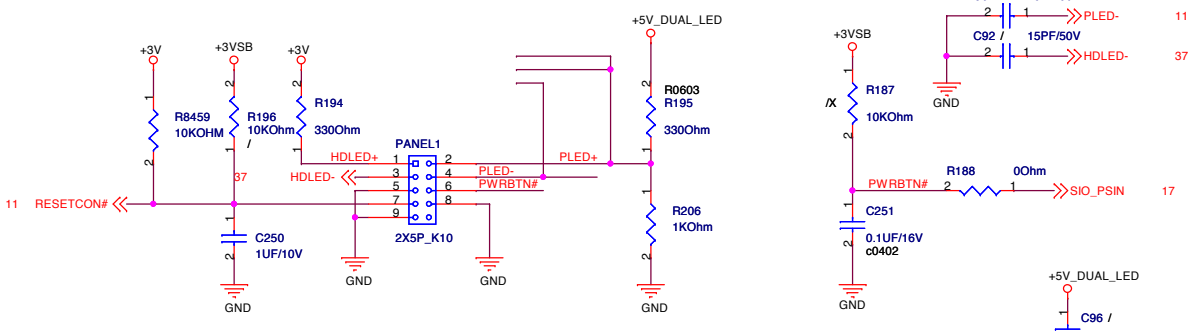
Date: Thursday, November 22, 2012 Sheet 31 of 48

+5V_DUAL_USB circuit diagram

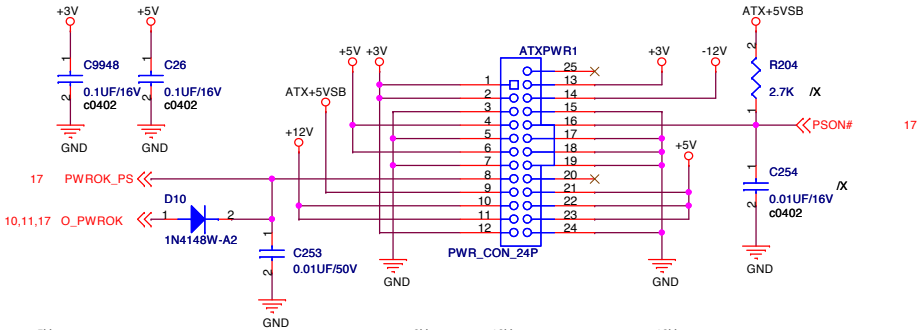
RING_IN



FRONT PANEL

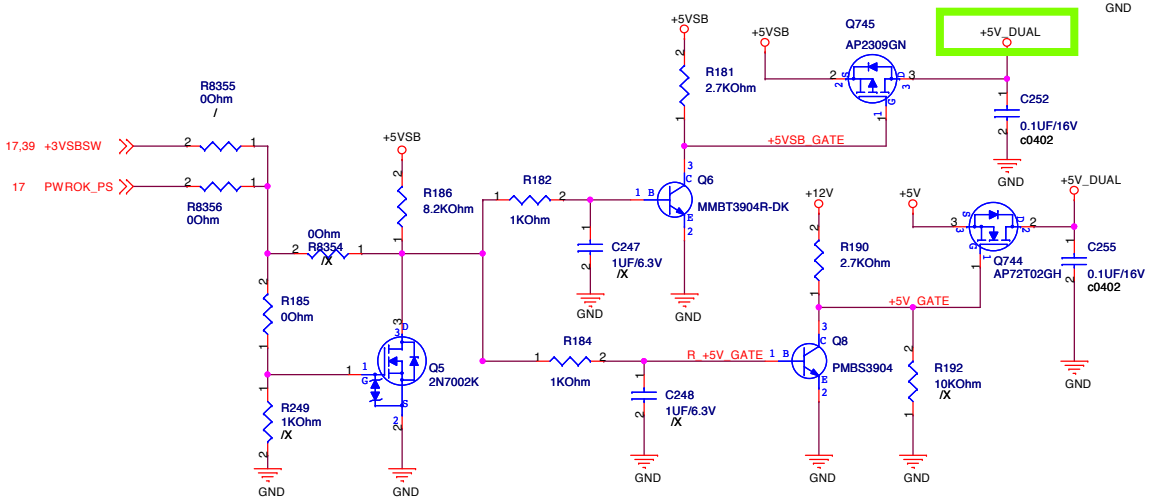


ATXPWR CONN



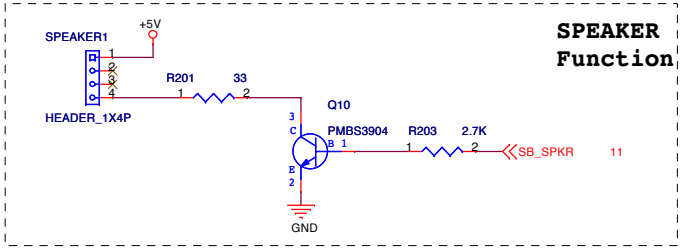
*Around the ATX Power Connector

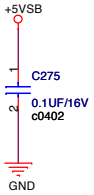
S3 circuit diagram



Logic IC : R190 = 2.7K, Q8 = 2N7002
BJT : R190 = 8.2K, Q8 = 3904, R192 = uninstall

SPEAKER Function





B75M-DGS

ASRock Inc.

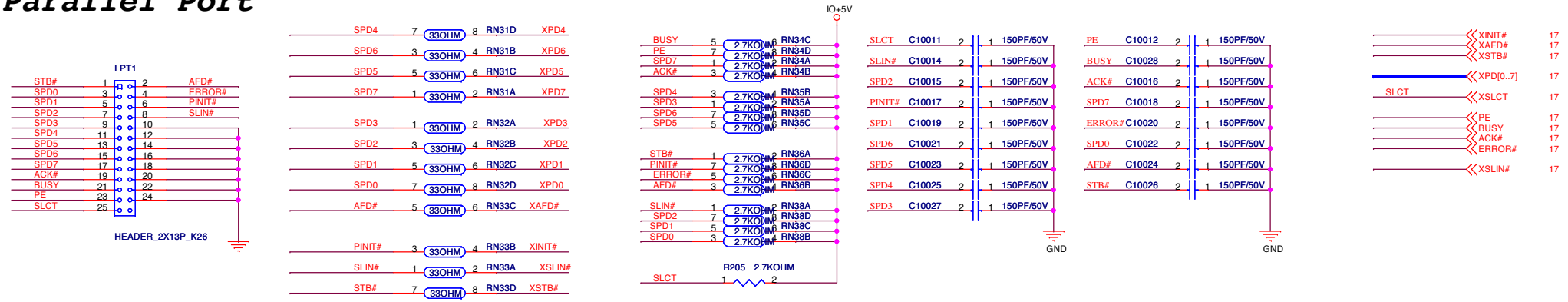
Title : POK_DUALSW_ENASUS

Engineer: Chia-wei Chang

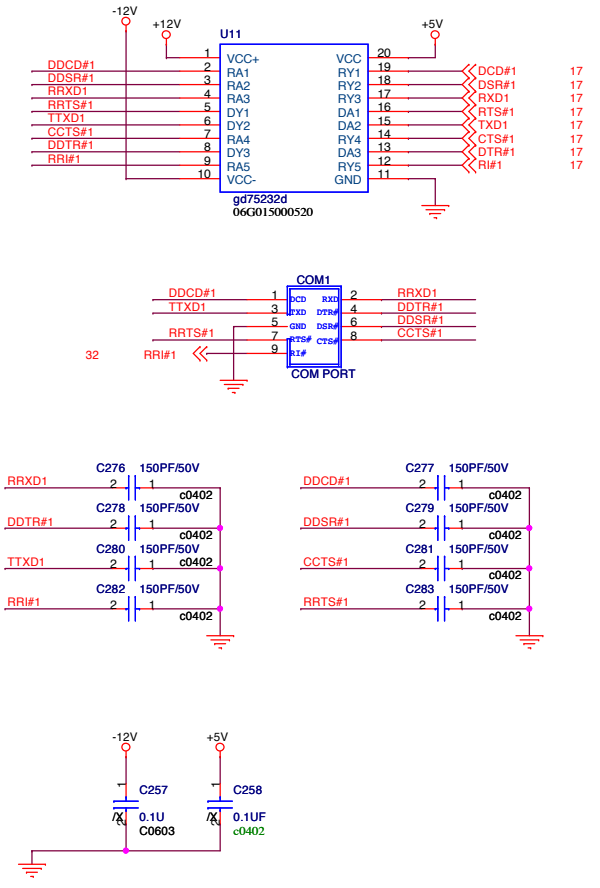
Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Tuesday, December 11, 2012 Sheet 32 of 48

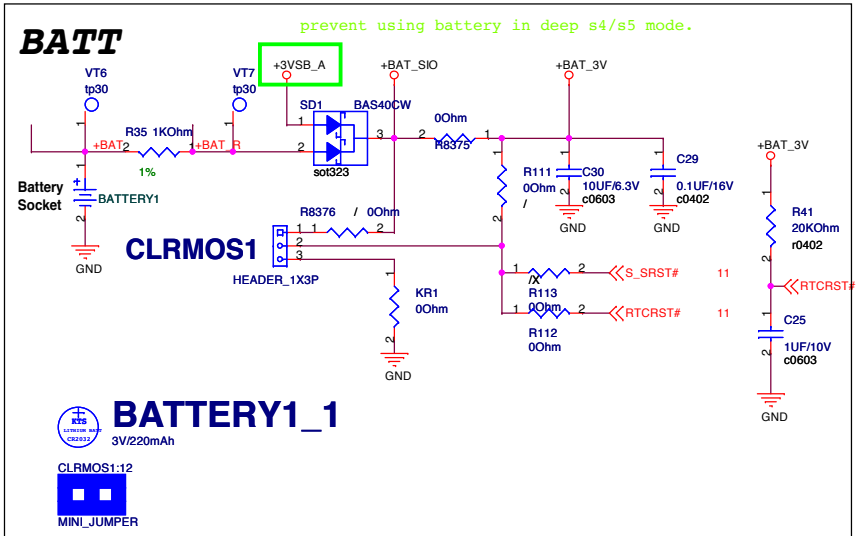
Parallel Port



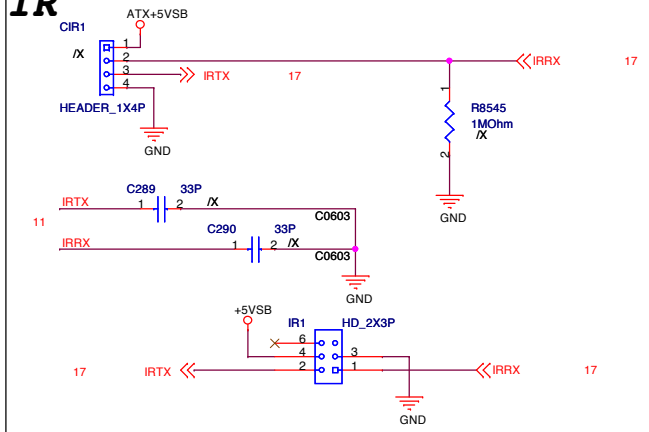
COM



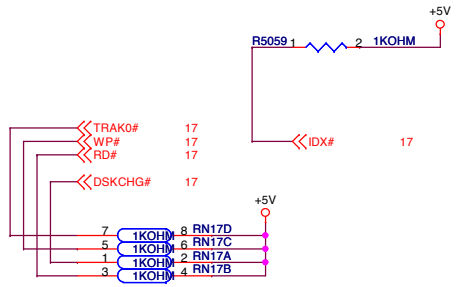
BATT



IR



TPM



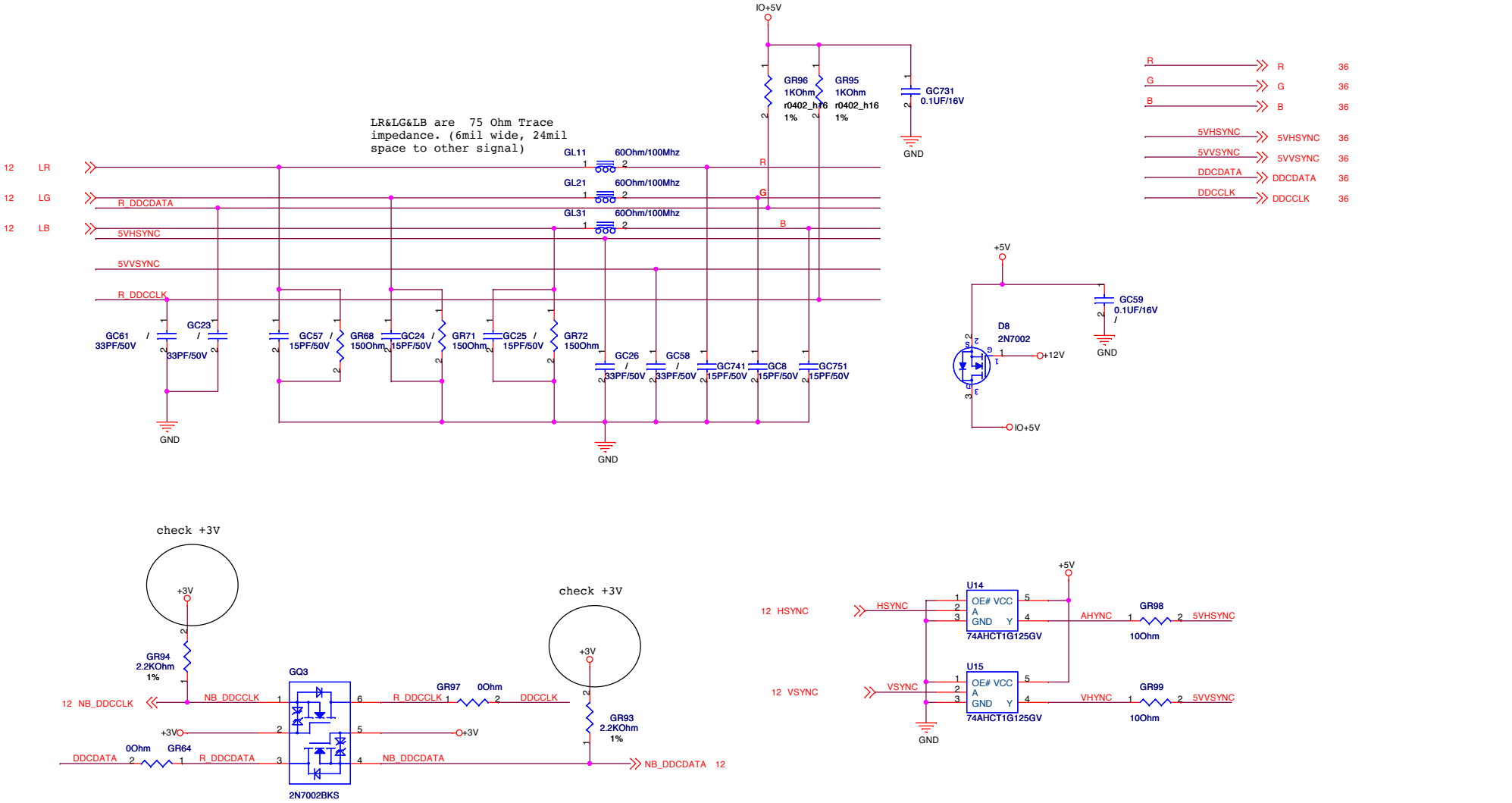
B75M-DGS

ASRock Title : IO CONNECTOR

ASRock Inc. Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

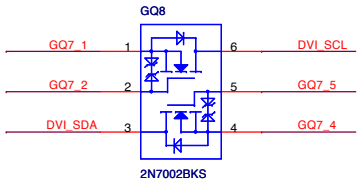
Date: Monday, November 26, 2012 Sheet 33 of 48

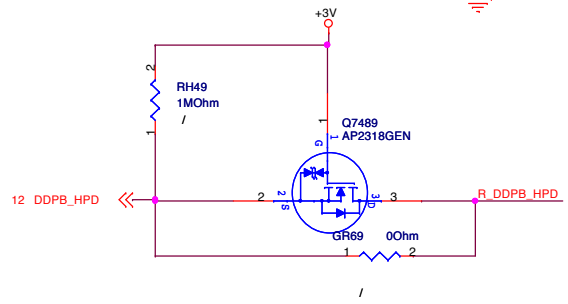


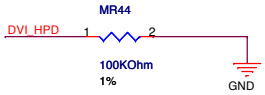
ASRock Inc.	Title : VGA LC filter	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 34 of 48	

DVI CONNECTOR

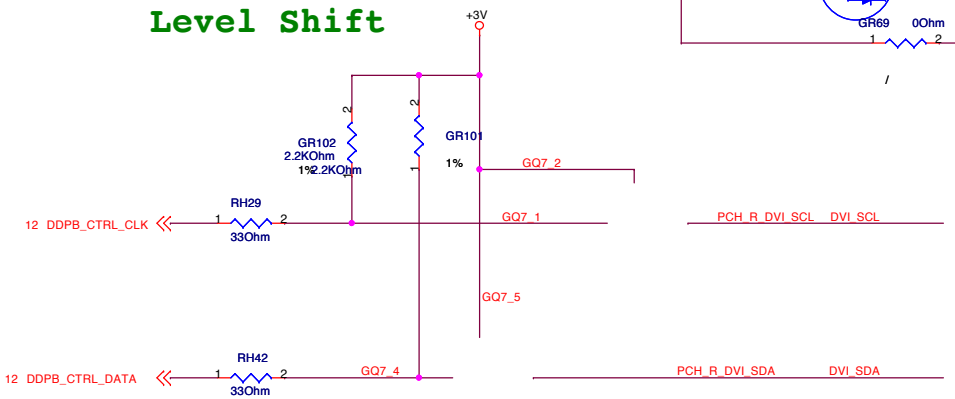
BOM焉1%



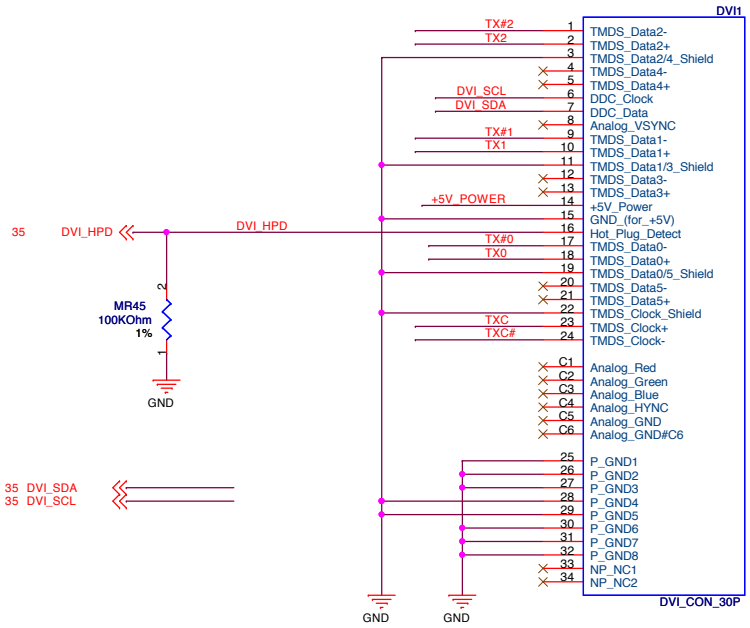


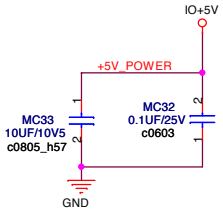


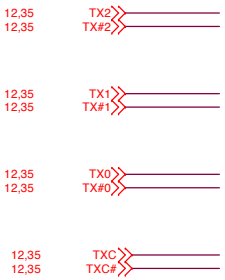
Level Shift

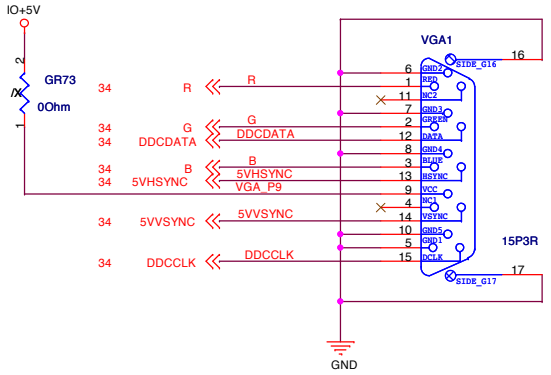


ASRock Inc.	Title : DVI LEVEL SHIFTER	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 35 of 48	

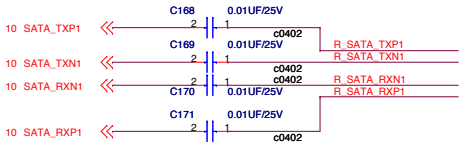


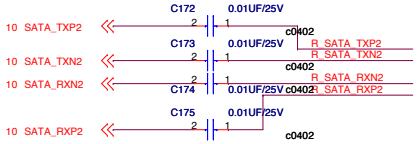


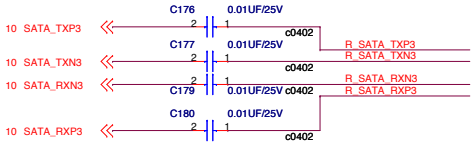


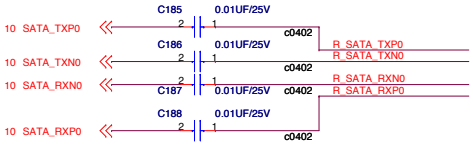


ASRock Inc.	Title : DVI VGA connector	
	Engineer: Chia-wei Chang	
Size: A3	Project Name: B75M-DGS	Rev: 2.00
Date: Thursday, November 22, 2012	Sheet 36 of 48	



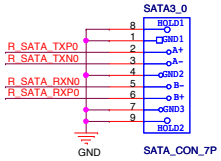




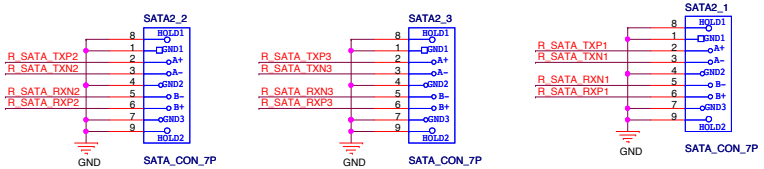


INTEL SATA3

Check SATA Port Name with leaders!!!



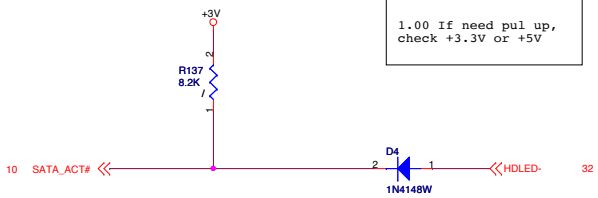
INTEL SATA2



SATA3 & SATA LED

1.00 Internal Pull UP

1.00 If need pul up, check +3.3V or +5V



B75M-DGS

ASRock Inc.

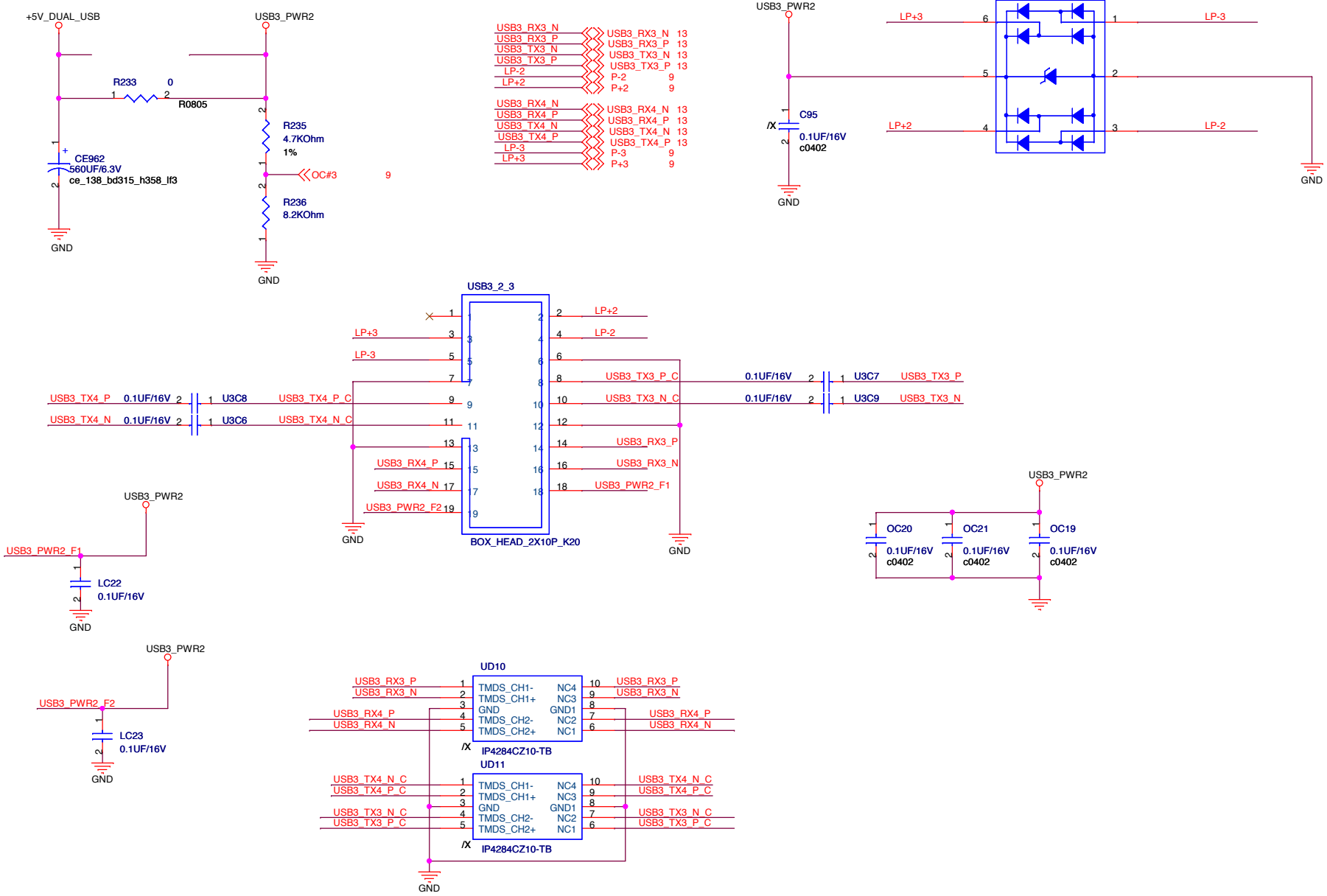
Title : SATA3/SATA2 / ESATA

Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

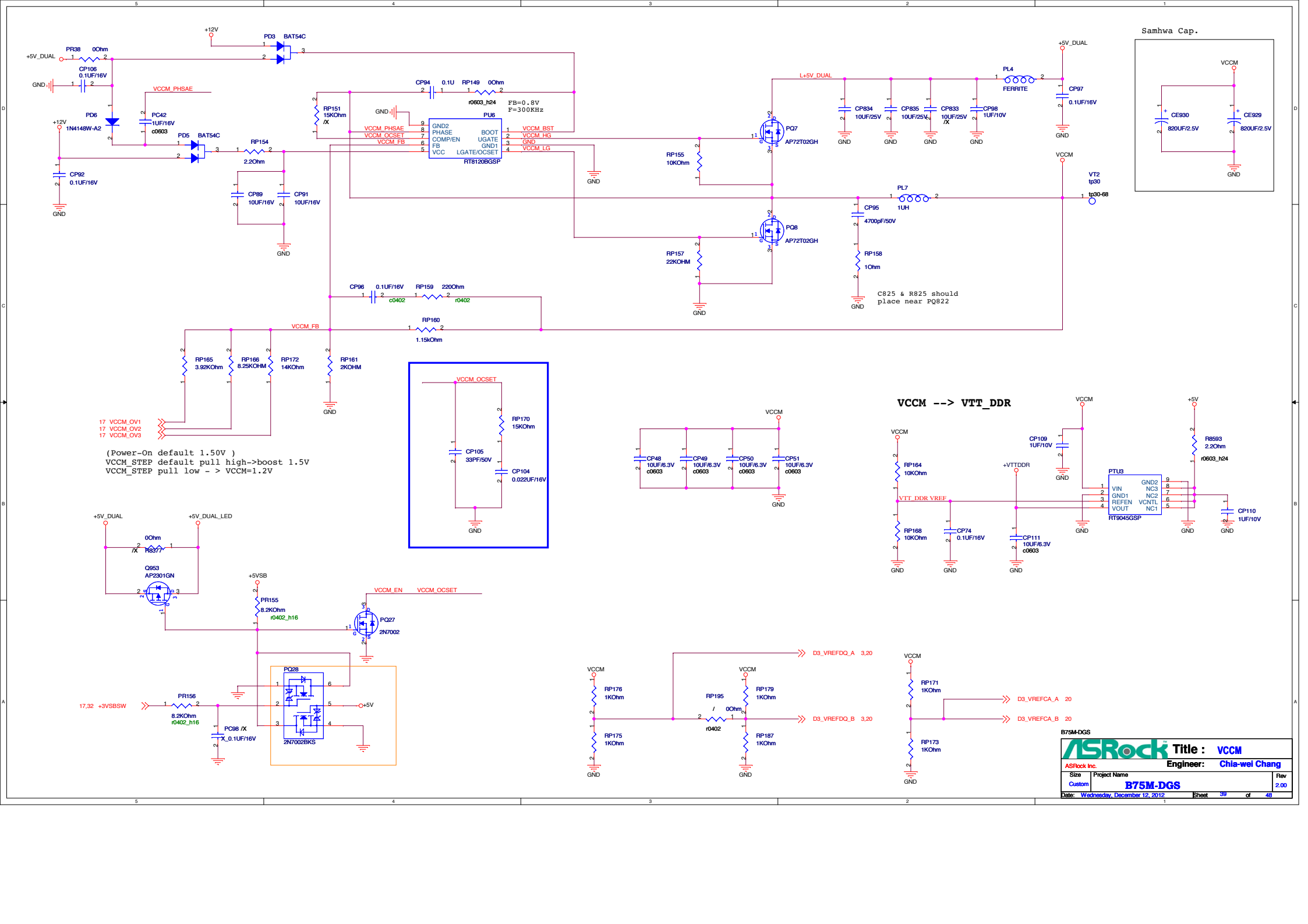
Date: Tuesday, December 11, 2012 Sheet 37 of 48

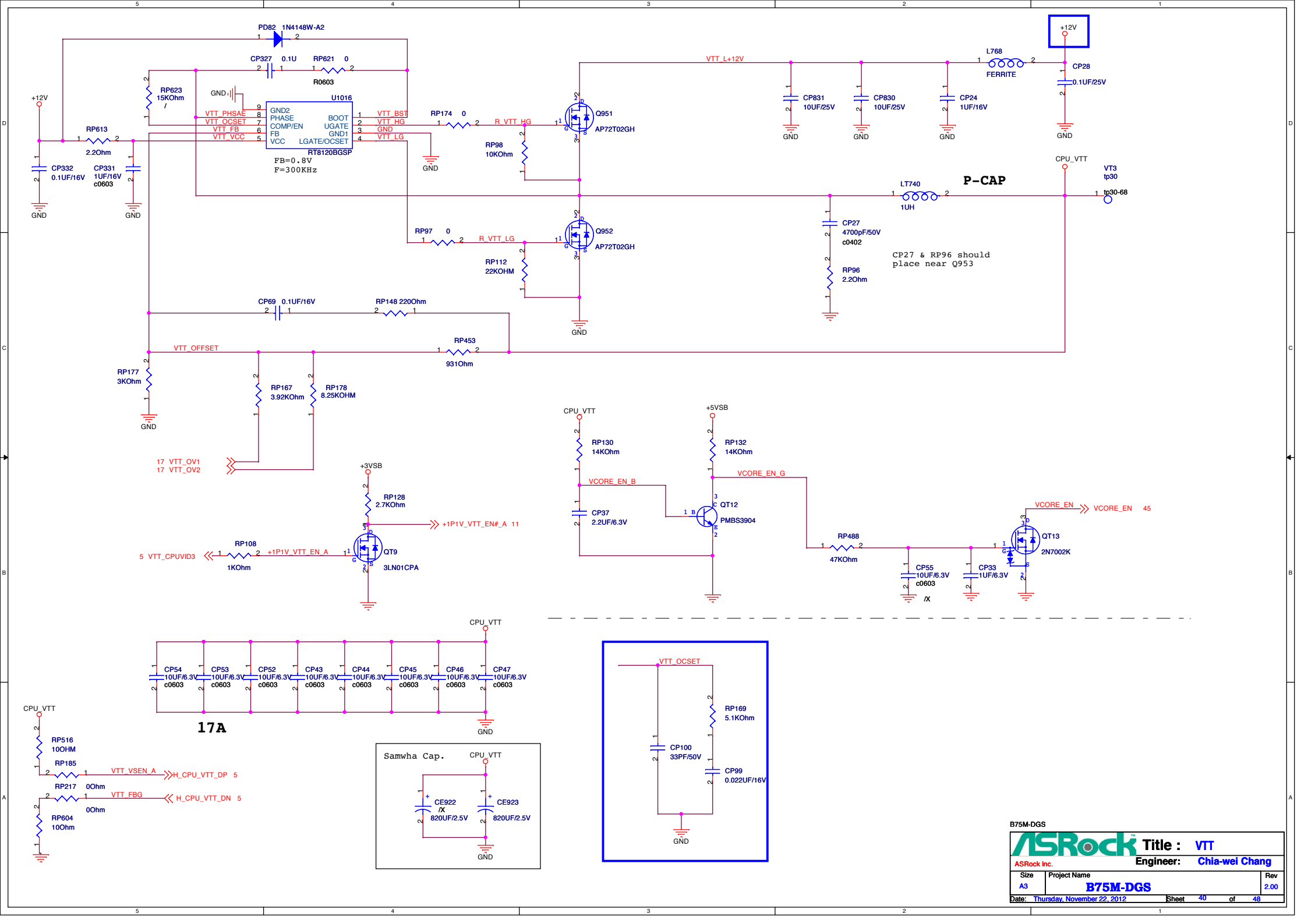
USB3_ 2_3



B75 Pro3-M

ASRock Inc.	Title : Front USB3	
	Engineer: Chia-Wei Chang	
Size: Custom	Project Name: B75 Pro3-M	Rev: 2.00
Date: Tuesday, December 11, 2012	Sheet 38 of 48	


Samhwa Cap.
VCCM
CE930
820UF/2.5V
CE929
820UF/2.5V
GND
+12V
PD3 BAT54C
+5V_DUAL
PR38 0Ohm
CP106 0.1UF/16V
GND
VCCM_PHSAE
PD6 1N4148W-A2
PC42 1UF/16V c0603
PD5 BAT54C
RP154 2.2Ohm
CP92 0.1UF/16V
CP89 10UF/16V
CP91 10UF/16V
CP94 0.1U
RP149 0Ohm
r0603_h24
FB=0.8V
F=300KHz
RP151 15KOhm /X
PU6
GND2
PHASE
COMP/EN
FB
VCC
BOOT
UGATE
GND1
LGATE/OCSET
RT8120BGSP
VCCM_PHSAE
VCCM_OCSET
VCCM_FB
VCCM_BST
VCCM_HG
GND
VCCM_LG
L+5V_DUAL
PQ7 AP72T02GH
RP155 10KOhm
CP834 10UF/25V
CP835 10UF/25V
CP833 10UF/25V /X
CP98 1UF/10V
PL4 FERRITE
+5V_DUAL
CP97 0.1UF/16V
VCCM
VT2 tp30
tp30-68
PL7 1UH
CP95 4700pF/50V
PQ8 AP72T02GH
RP157 22KOHM
RP158 1Ohm
C825 & R825 should place near PQ822
CP96 0.1UF/16V c0402
RP159 220Ohm r0402
RP160 1.15kOhm
VCCM_FB
RP165 3.92KOhm
RP166 8.25KOHM
RP172 14KOhm
RP161 2KOHM
17 VCCM_OV1
17 VCCM_OV2
17 VCCM_OV3
(Power-On default 1.50V)
VCCM_STEP default pull high->boost 1.5V
VCCM_STEP pull low - > VCCM=1.2V
VCCM_OCSET
RP170 15KOhm
CP105 33PF/50V
CP104 0.022UF/16V
VCCM
CP48 10UF/6.3V c0603
CP49 10UF/6.3V c0603
CP50 10UF/6.3V c0603
CP51 10UF/6.3V c0603
VCCM --> VTT_DDR
VCCM
RP164 10KOhm
VTT_DDR_VREF
RP168 10KOhm
CP74 0.1UF/16V
+VTTDDR
CP111 10UF/6.3V c0603
CP109 1UF/10V
PTU3
GND2
VIN
GND1
REFEN
VOUT
NC3
NC2
VCNTL
NC1
RT9045GSP
+5V
R8593 2.2Ohm r0603_h24
CP110 1UF/10V
+5V_DUAL
+5V_DUAL_LED
0Ohm /X R837
Q953 AP2301GN
+5VSB
PR155 8.2KOhm r0402_h16
VCCM_EN
VCCM_OCSET
PQ27 2N7002
PQ28
17,32 +3VSBSW
PR156 8.2KOhm r0402_h16
PC98 /X X_0.1UF/16V
2N7002BKS
+5V
VCCM
RP176 1KOhm
RP175 1KOhm
RP195 / 0Ohm r0402
RP179 1KOhm
RP187 1KOhm
D3_VREFDQ_A 3,20
D3_VREFDQ_B 3,20
RP171 1KOhm
RP173 1KOhm
D3_VREFCA_A 20
D3_VREFCA_B 20
B75M-DGS
ASRock
Title : VCCM
ASRock Inc.
Engineer: Chia-wei Chang
Size Custom
Project Name B75M-DGS
Rev 2.00
Date: Wednesday, December 12, 2012
Sheet 39 of 48



B75M-DGS

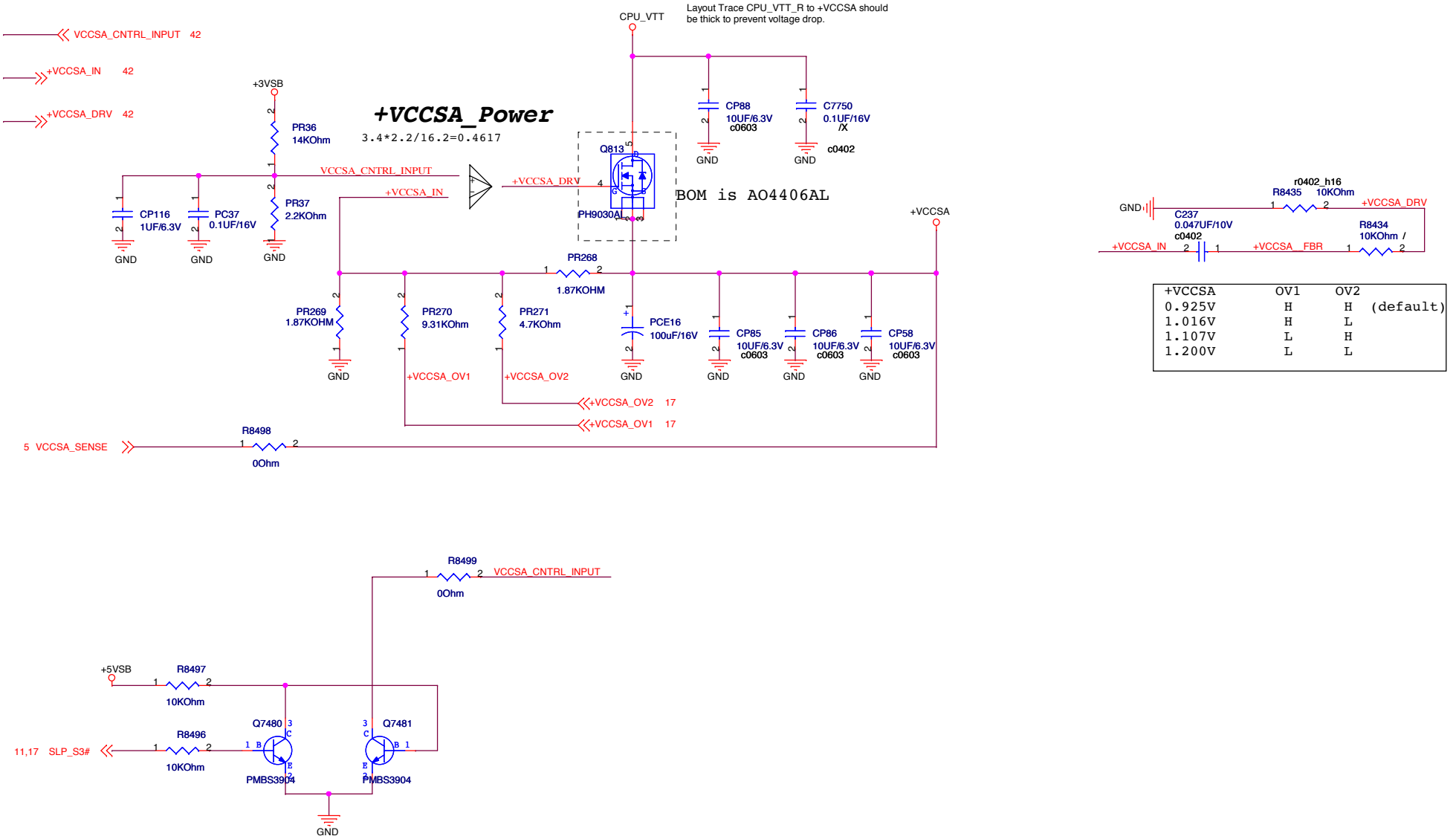
ASRock Inc.

Title : VTT

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

Date: Thursday, November 22, 2012 Sheet 40 of 48



+VCCSA	OV1	OV2	
0.925V	H	H	(default)
1.016V	H	L	
1.107V	L	H	
1.200V	L	L	

B75M-DGS

ASRock Inc.

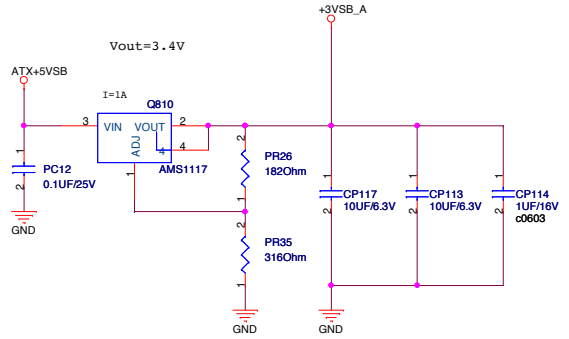
Title : VSA

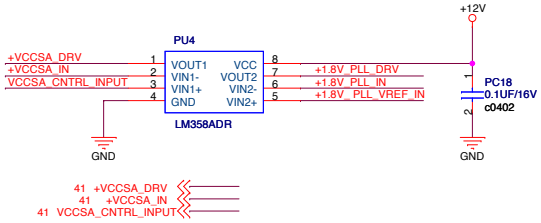
Engineer: Chia-wei Chang

Size	Project Name	Rev
B	B75M-DGS	2.00

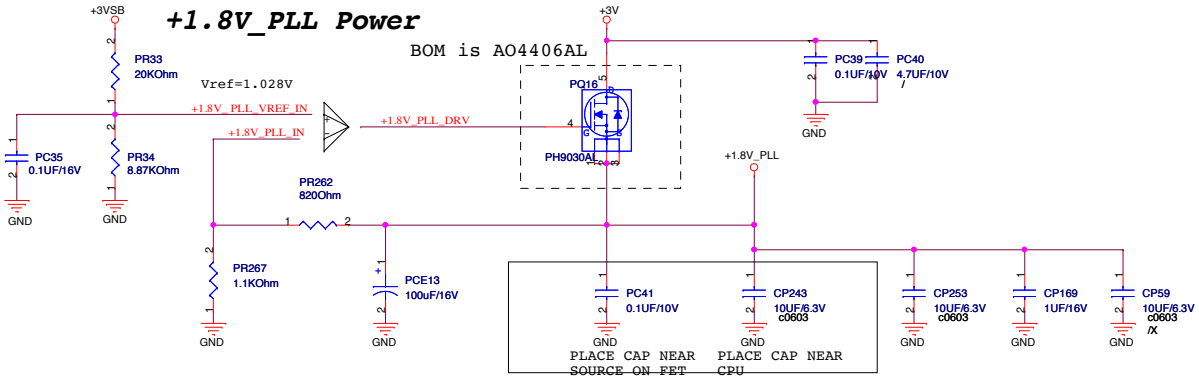
Date: Thursday, November 22, 2012 Sheet 41 of 48

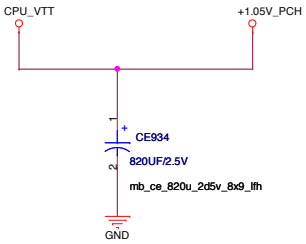
+3VSB_A

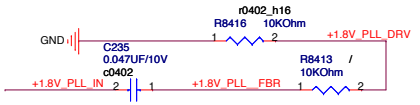




+1.8V_PLL Power







B75M-DGS

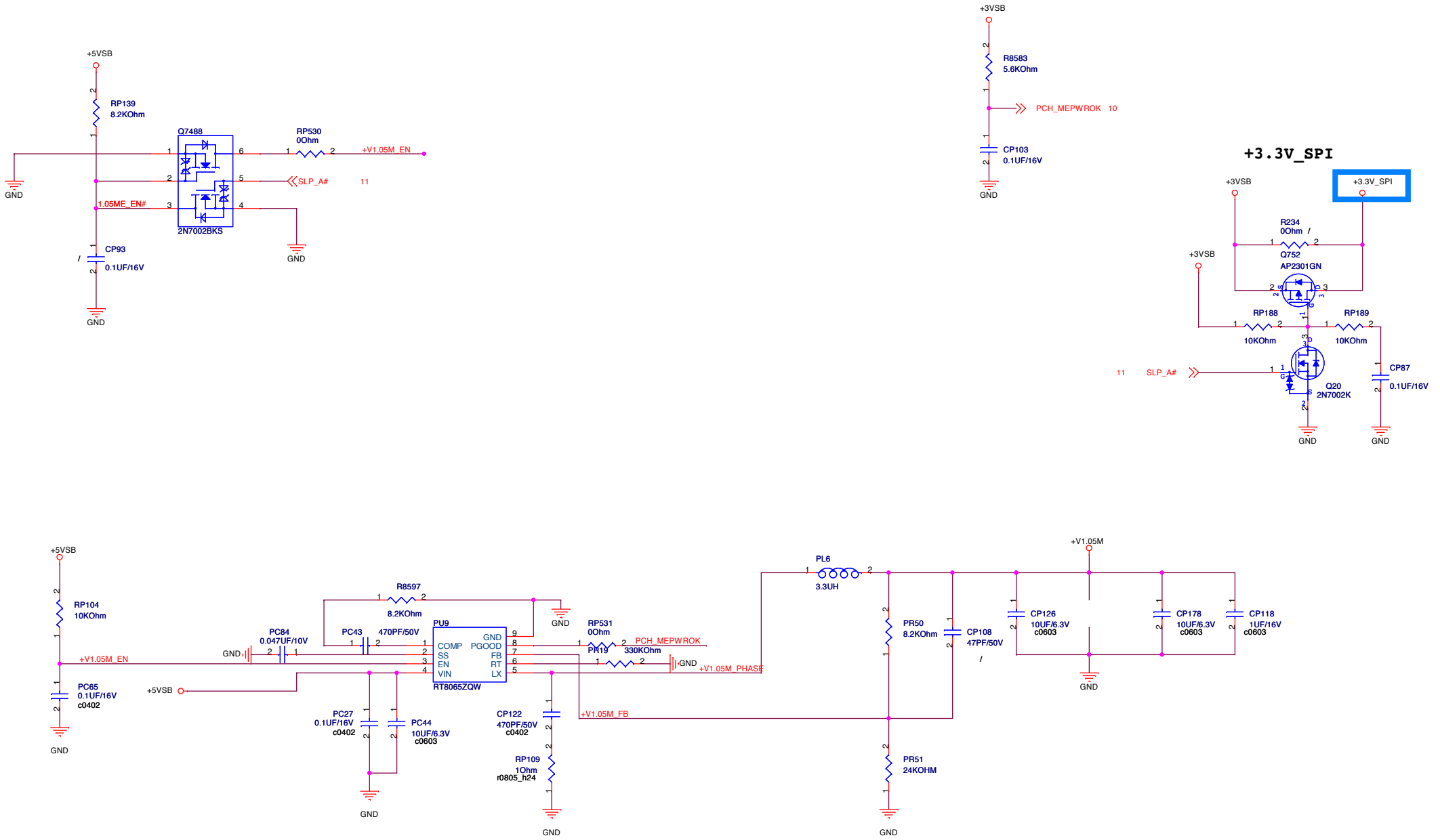
ASRock Inc.

Title : DC to DC

Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Tuesday, November 27, 2012 Sheet 42 of 48



B75M-DGS

ASRock Inc.

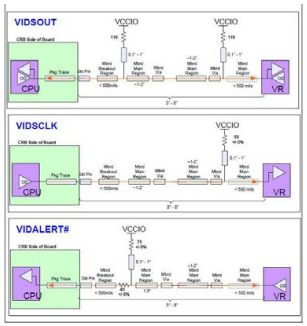
Title : ME Power

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3		2.00

Date: Tuesday, November 27, 2012 Sheet 43 of 48

Title :	Voltage_Switch
ASRock Inc.	Engineer: Chia-wei Chang
Size: B	Project Name: B75M-DGS
Rev: 2.00	
Date: Thursday, November 22, 2012	Sheet 44 of 48



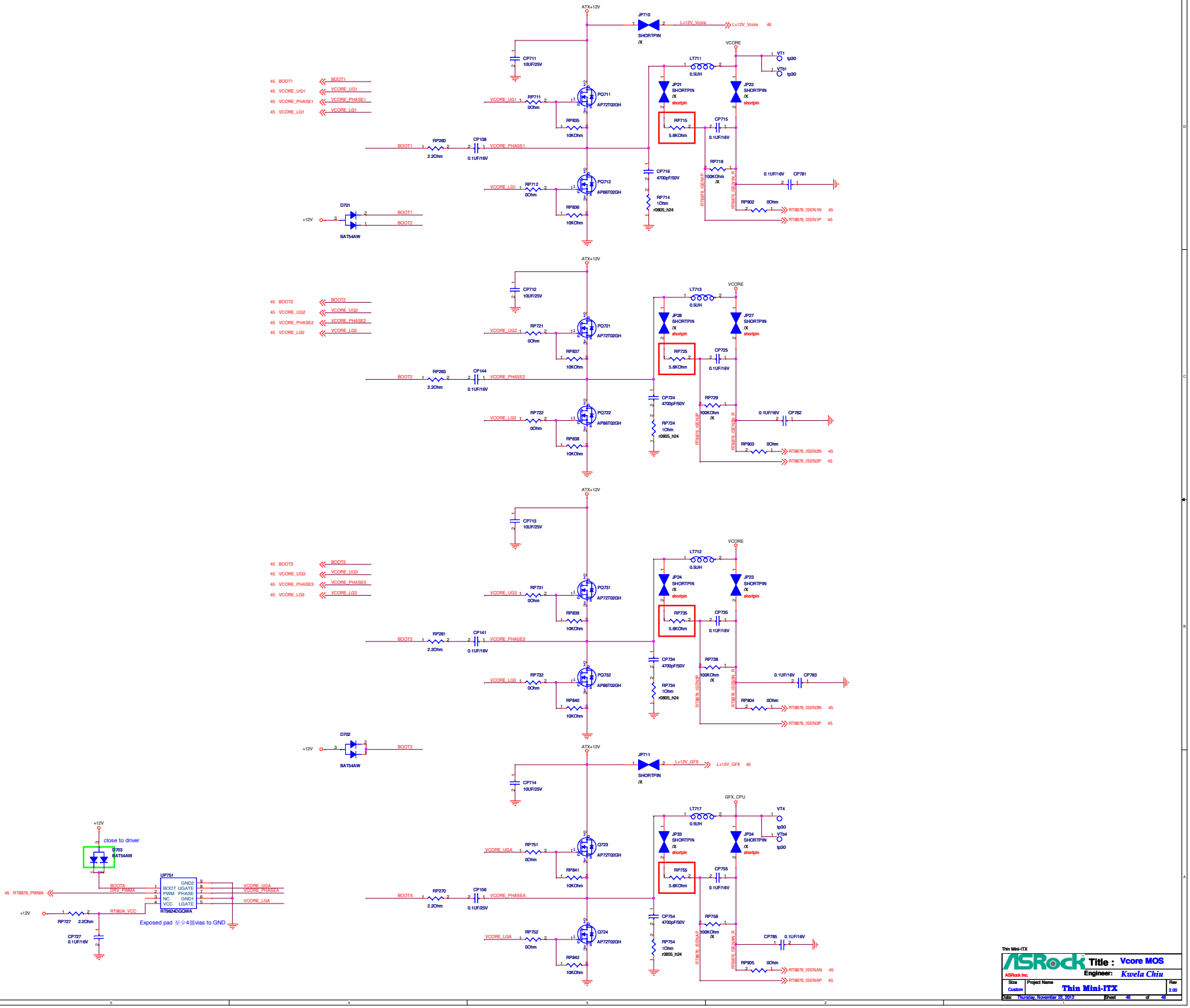
Thin Mini-ITX

ASRock Title : PWM RT8859

ASRock Inc. Engineer: Kwela Chiu

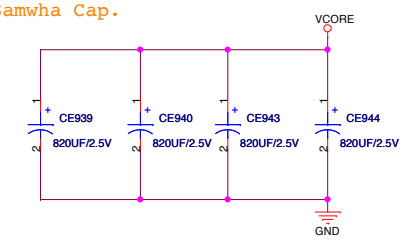
Size	Project Name	Rev
Custom	Thin Mini-ITX	2.00

Date: Thursday, November 22, 2012 Sheet 45 of 48


ATX+12V
JP710
SHORTPIN
/X
L+12V_Vcore
45
L+12V_Vcore
VCORE
CP711
10UF/25V
LT711
0.5UH
VT1
tp30
VT1
tp30
45 BOOT1
45 VCORE_UG1
45 VCORE_PHASE1
45 VCORE_LG1
BOOT1
VCORE_UG1
VCORE_PHASE1
VCORE_LG1
RP711
0Ohm
PQ711
AP72T02GH
RP835
10KOhm
JP21
SHORTPIN
/X
shortpin
JP22
SHORTPIN
/X
shortpin
RP715
5.6KOhm
CP715
0.1UF/16V
RP690
2.2Ohm
CP138
0.1UF/16V
VCORE_PHASE1
CP716
4700pF/50V
RP714
1Ohm
r0805_h24
RP718
100KOhm
/X
0.1UF/16V
CP781
RT8876_ISEN1P
RT8876_ISEN1N
RP902
0Ohm
RT8876_ISEN1N
45
RT8876_ISEN1P
45
VCORE_LG1
RP712
0Ohm
PQ712
AP86T02GH
RP836
10KOhm
D701
+12V
BOOT1
BOOT2
BAT54AW
ATX+12V
CP712
10UF/25V
LT713
0.5UH
VCORE
45 BOOT2
45 VCORE_UG2
45 VCORE_PHASE2
45 VCORE_LG2
BOOT2
VCORE_UG2
VCORE_PHASE2
VCORE_LG2
RP721
0Ohm
PQ721
AP72T02GH
RP837
10KOhm
JP28
SHORTPIN
/X
shortpin
JP27
SHORTPIN
/X
shortpin
RP725
5.6KOhm
CP725
0.1UF/16V
RP263
2.2Ohm
CP144
0.1UF/16V
VCORE_PHASE2
CP724
4700pF/50V
RP724
1Ohm
r0805_h24
RP729
100KOhm
/X
0.1UF/16V
CP782
RT8876_ISEN2P
RT8876_ISEN2N
RP903
0Ohm
RT8876_ISEN2N
45
RT8876_ISEN2P
45
VCORE_LG2
RP722
0Ohm
PQ722
AP86T02GH
RP838
10KOhm
ATX+12V
CP713
10UF/25V
LT712
0.5UH
VCORE
45 BOOT3
45 VCORE_UG3
45 VCORE_PHASE3
45 VCORE_LG3
BOOT3
VCORE_UG3
VCORE_PHASE3
VCORE_LG3
RP731
0Ohm
PQ731
AP72T02GH
RP839
10KOhm
JP24
SHORTPIN
/X
shortpin
JP23
SHORTPIN
/X
shortpin
RP735
5.6KOhm
CP735
0.1UF/16V
RP691
2.2Ohm
CP141
0.1UF/16V
VCORE_PHASE3
CP734
4700pF/50V
RP734
1Ohm
r0805_h24
RP738
100KOhm
/X
0.1UF/16V
CP783
RT8876_ISEN3P
RT8876_ISEN3N
RP904
0Ohm
RT8876_ISEN3N
45
RT8876_ISEN3P
45
VCORE_LG3
RP732
0Ohm
PQ732
AP86T02GH
RP840
10KOhm
D702
+12V
BOOT3
BAT54AW
ATX+12V
JP711
SHORTPIN
/X
L+12V_GFX
45
L+12V_GFX
CP714
10UF/25V
GFX_CPU
LT717
0.5UH
VT4
tp30
VT4
tp30
VCORE_UGA
RP751
0Ohm
Q723
AP72T02GH
RP841
10KOhm
JP33
SHORTPIN
/X
shortpin
JP34
SHORTPIN
/X
shortpin
RP755
5.6KOhm
CP755
0.1UF/16V
BOOTA
RP270
2.2Ohm
CP156
0.1UF/25V
VCORE_PHASEA
CP754
4700pF/50V
RP754
1Ohm
r0805_h24
RP758
100KOhm
/X
CP785
0.1UF/16V
RT8876_ISENAP
RT8876_ISENAN
RP905
0Ohm
RT8876_ISENAN
45
RT8876_ISENAP
45
VCORE_LGA
RP752
0Ohm
Q724
AP72T02GH
RP842
10KOhm
+12V
close to driver
D703
BAT54AW
45 RT8876_PWMA
BOOTA
DRV_PWMA
UP751
GND2
BOOT UGATE
PWM PHASE
NC GND1
VCC LGATE
RT9624DGQW
VCORE_UGA
VCORE_PHASEA
VCORE_LGA
+12V
RP727
2.2Ohm
RT9624_VCC
CP727
0.1UF/16V
Exposed pad 至少4個vias to GND
Thin Mini-ITX
ASRock
Title : Vcore MOS
ASRock Inc.
Engineer: Kwela Chiu
Size
Custom
Project Name
Thin Mini-ITX
Rev
2.00
Date: Thursday, November 22, 2012
Sheet 45 of 48

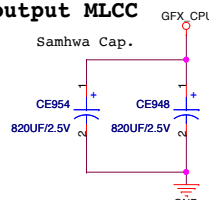
Vcore output P-CAP

Samwha Cap.

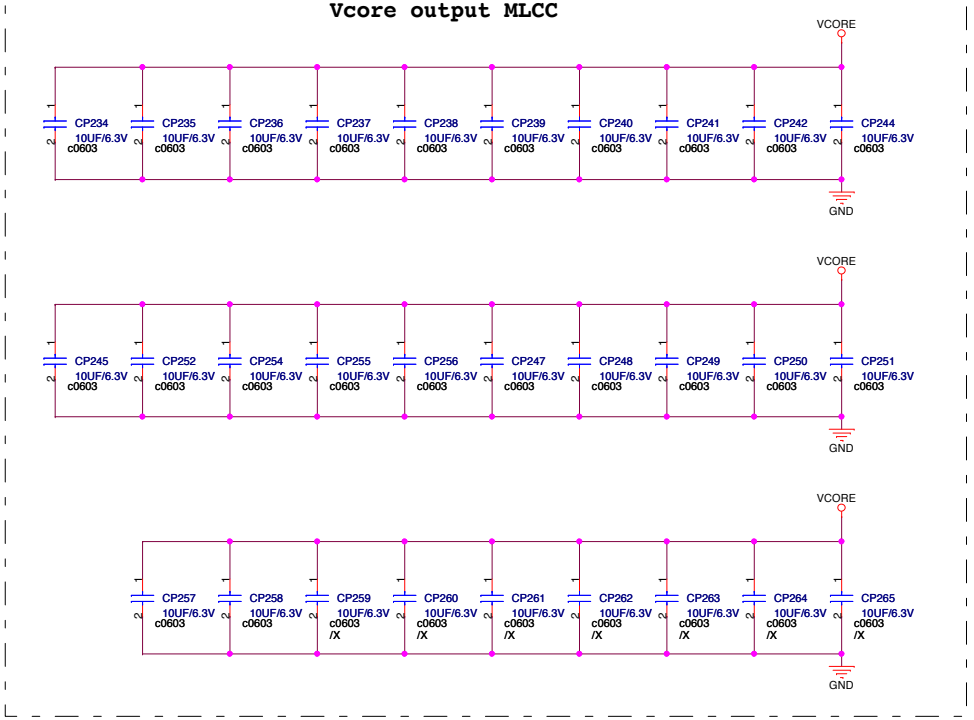


GFX output MLCC

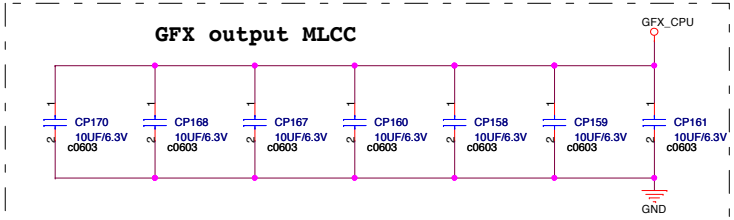
Samhwa Cap.



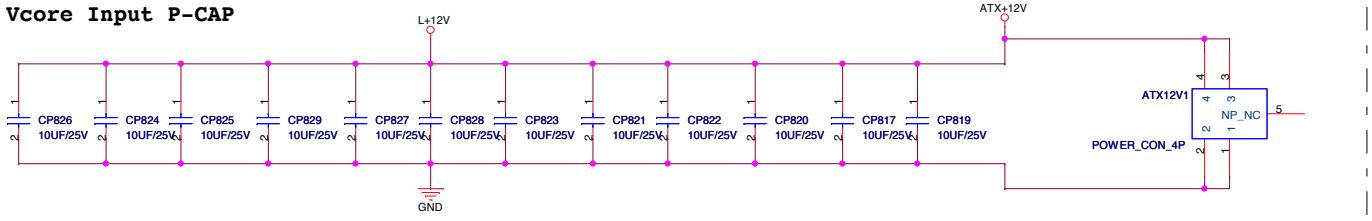
Vcore output MLCC



GFX output MLCC



Vcore Input P-CAP



B75M-DGS

ASRock Inc.

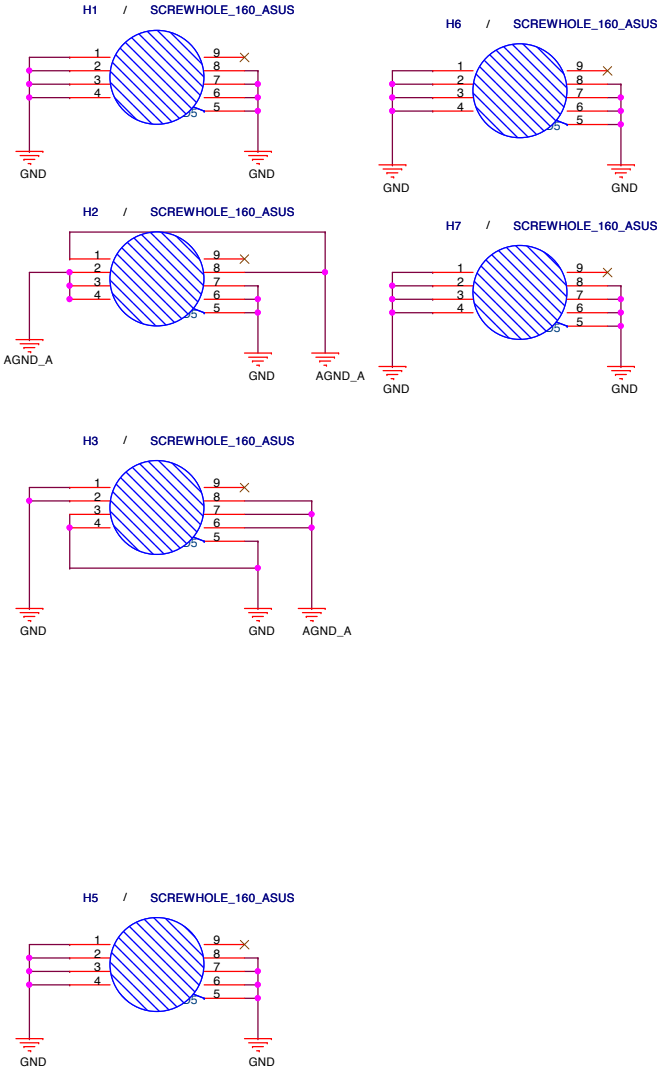
Title : CPU CAP & Offset

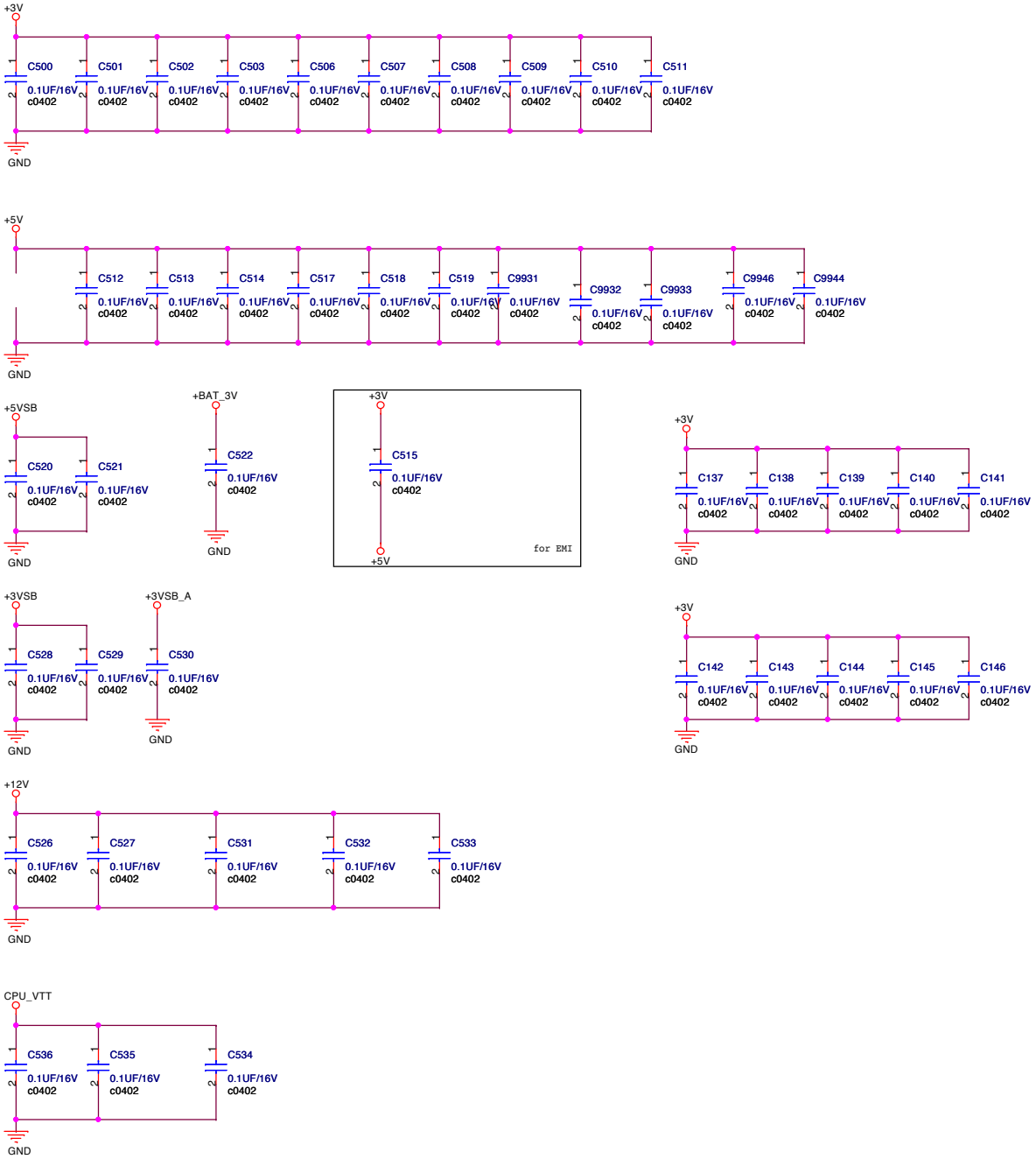
Engineer: Chia-wei Chang

Size	Project Name	Rev
Custom	B75M-DGS	2.00

Date: Wednesday, November 28, 2012 Sheet 47 of 48

SCREW_HOLE





B75M-DGS

ASRock Inc.

Title : MECHANICAL

Engineer: Chia-wei Chang

Size	Project Name	Rev
A3	B75M-DGS	2.00

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