

Rev : 1.0

REVISION HISTORY:


Rev	Date	Notes
VA	2011 0820	Initial version
VA	2011 1015	For memroy, Change DDR3*4 to DDR3*2
VA	2011 1016	Change Audio IC from ALC892 to ALC662
VA	2011 1017	ME Disable change to 2pin
VA	2011 1017	DEL PCI-EX4 and ADD PCI2
VA	2011 1018	Change SATA3.0 X2 to SATA2.0 X2
VA	2011 1019	Modify USB Ports.
VA	2011 1023	HDMI&DP co-lay => HDMI Only.
VA	2011 1023	Add 3 pin PWR_FAN,remove smart fan function;Add 3 PIN SYS_FAN
VA	2011 1031	Add GPIO to adjust V_DIMM voltage

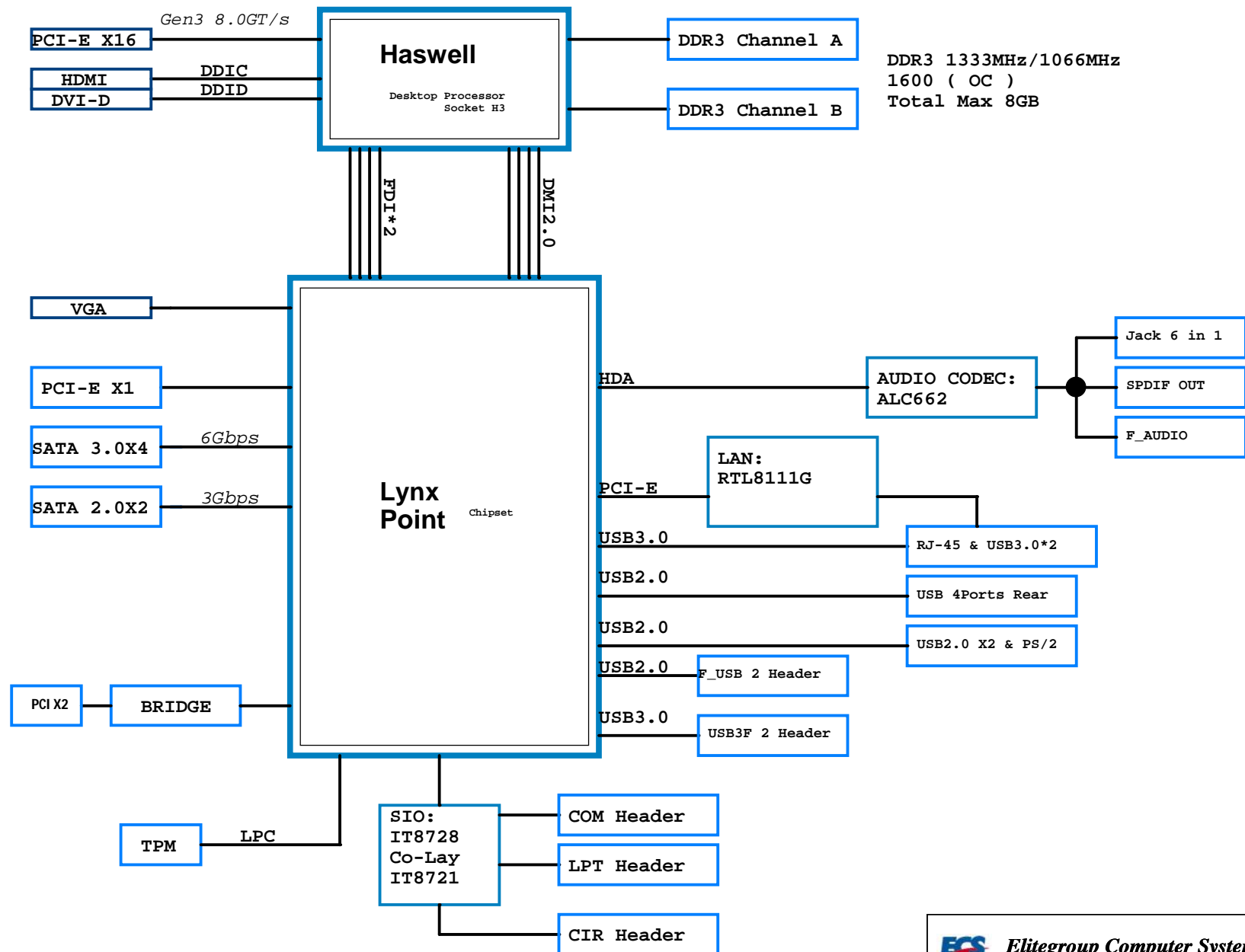
NOTE:

1. Model Code:
2. Modified from H87H3-M V:A

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 Elitegroup Computer Systems			
Title			
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PCH-GPIO function

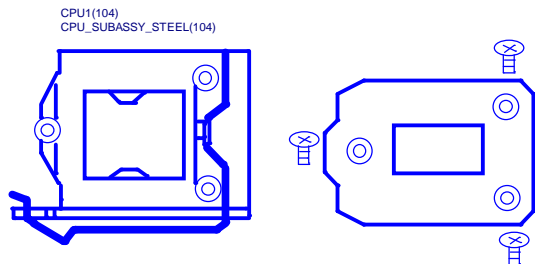
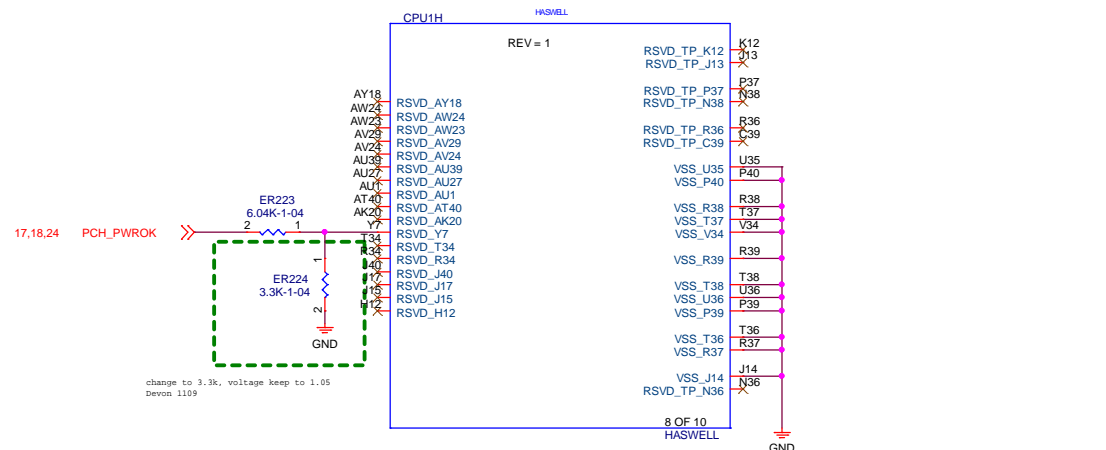
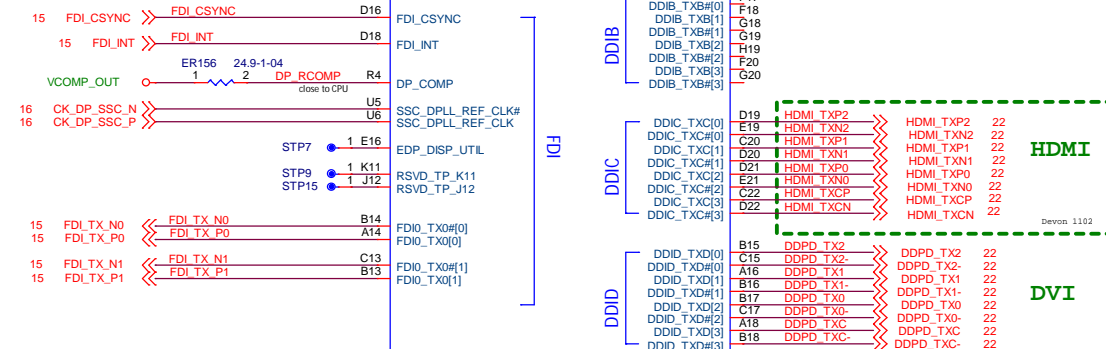
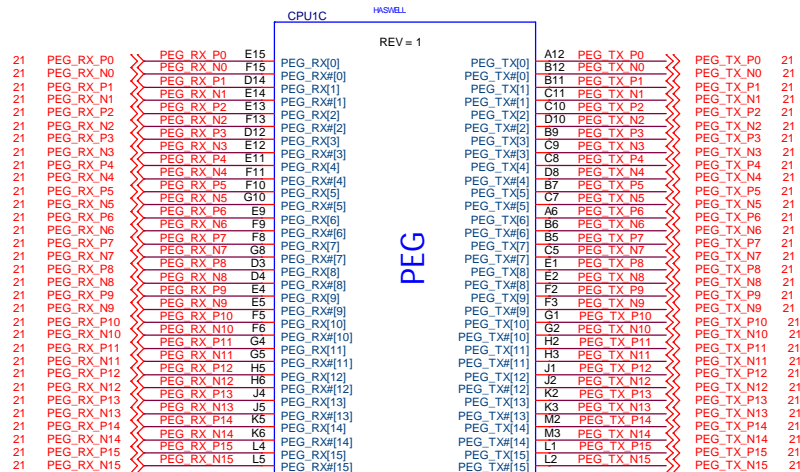
Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	case open(reserve)	GPI
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	USB_5VDUAL control	GPO
GPIO72	3VSB	USB_5VDUAL control (reserve)	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	LAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO68	VCC3	TP_VGA	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	GPIO
GP33	ATX_3VSB	SUSACK#	GPIO
GP34	ATX_3VSB	SUSWARN#	GPIO
GP55	ATX_3VSB	DPWROK	RSMRST#
GP41	3VSB	RSMRST#	PWROK2
GP63	3VSB	3VSBSW_MINI	GPIO
GP35	3VSB	LED0	GPIO
GP37	3VSB	LED1	GPIO
GP72	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP75	VCC3	BOM detect	GPIO
GP76	VCC3	BOM detect	GPIO

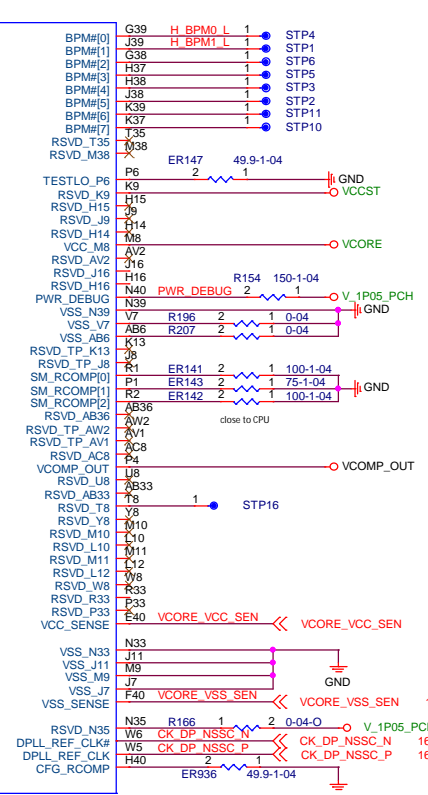
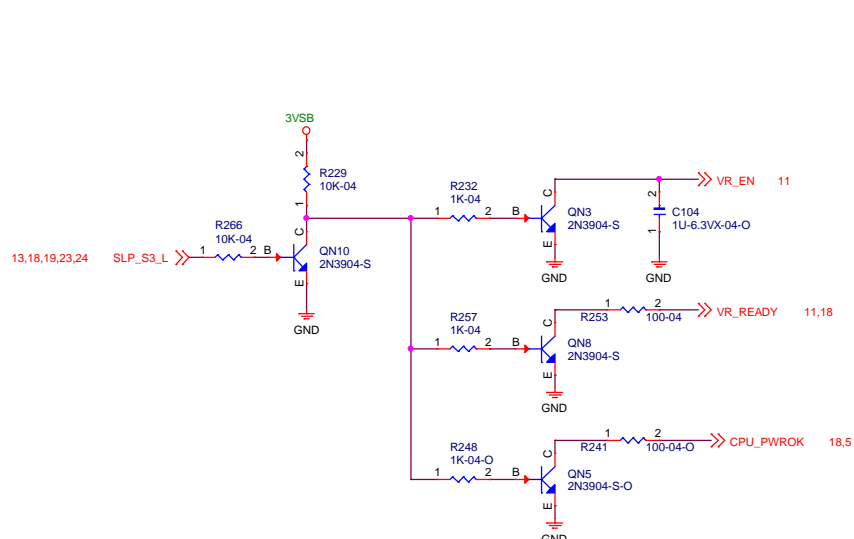
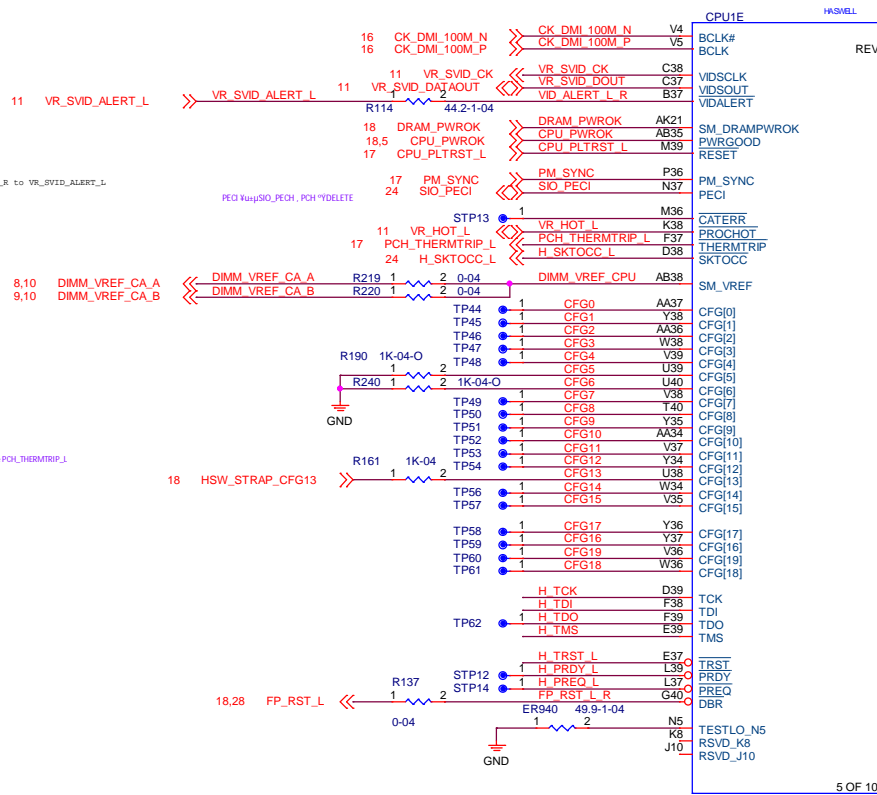
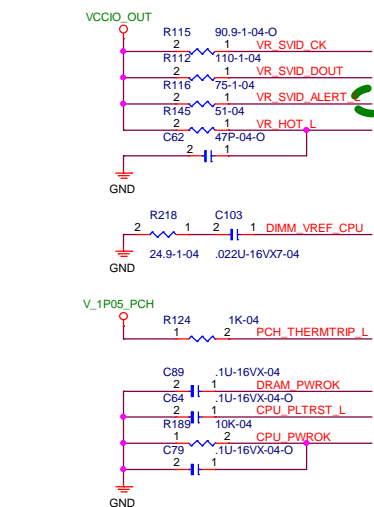
Interrupt mapping

Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
PCIEX4	INTA#/B#	port 5-8	LPT integrate
mini-PCIE	INTB#	port 2	LPT integrate
SATA	INTB#	NA	LPT integrate



CPU steel (T/U pahse)
PN:20-800-005711 CPU SOCKET STEEL SUBASSY.STEEL...LGA 1155/1156P.W/BACK PLATE,CAP.LOTES

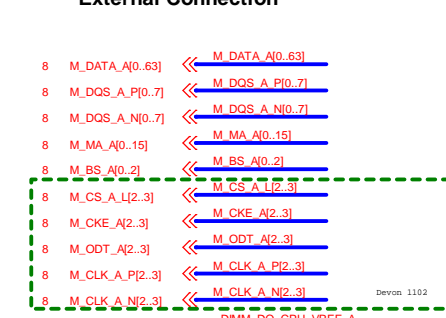
CPU socket (SMD phase)
PN:11-018-115128 SOCKET.CPU..LGA 1150P SMD..15u...BLACK.ACA-ZIF-138-P01...HF.LEAD-FREE.LOTES



CFG[1:0]: Reserved configuration lane.
 CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
 1 = Normal operation
 0 = Lane numbers reversed.
 CFG[3]: MSR Privacy Bit Feature
 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0]
 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden
 CFG[4]: Reserved configuration lane.
 CFG[6:5]: PCI Express* Bifurcation:
 CFG[19:7]: Reserved configuration lanes.

Power Down Sequencing Circuit

External Connection



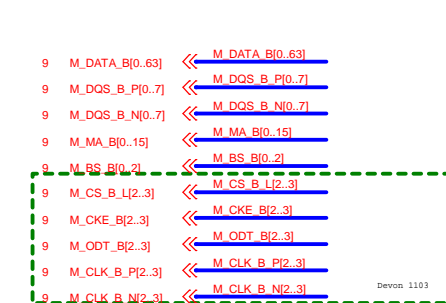
10 DIMM_DQ_CPU_VREF_A << DIMM_DQ_CPU_VREF_A

```

8  M_WE_A_L  <-- M_WE_A_L
8  M_CAS_A_L <-- M_CAS_A_L
8  M_RAS_A_L <-- M_RAS_A_L

```

DDR3 CH.A



10 DIMM DQ CPU VREF B << DIMM_DQ_CPU_VREF_B

9 M_WE_B_L M WE B L
9 M_CAS_B_L M CAS B L
9 M_RAS_B_L M RAS B L

DDR3 CH.B



8,9 DDR3_DRAMRST_L << DDR3_DRAMRST_L

```
NC_M_ODT_A[0..1],M_CKE_A[0..1],M_CS_A_L[0..1],M_CLK_A_P[0..1],M_CLK_A_N[0..1]
Devon 20121016
```

```
NC_M_ODT_B[0..1],M_CKE_B[0..1],M_CS_B_L[0..1],M_CLK_B_P[0..1],M_CLK_B_N[0..1]
Devon 20121016
```

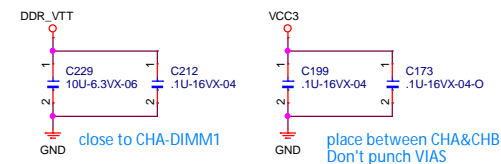
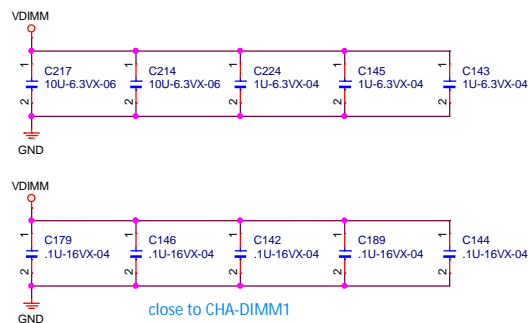
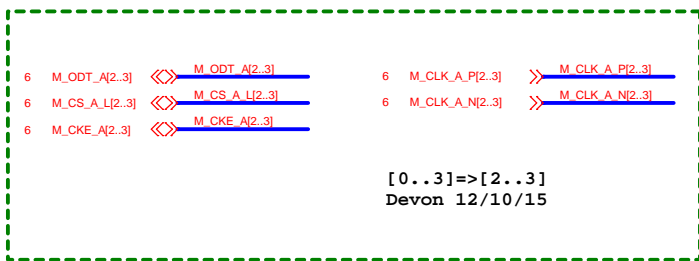
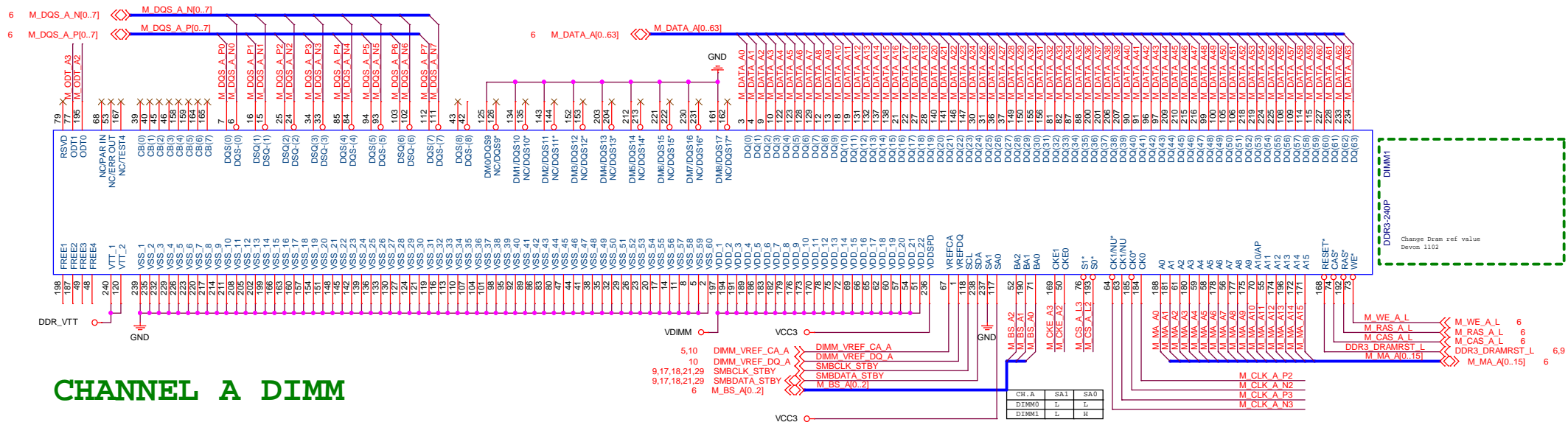
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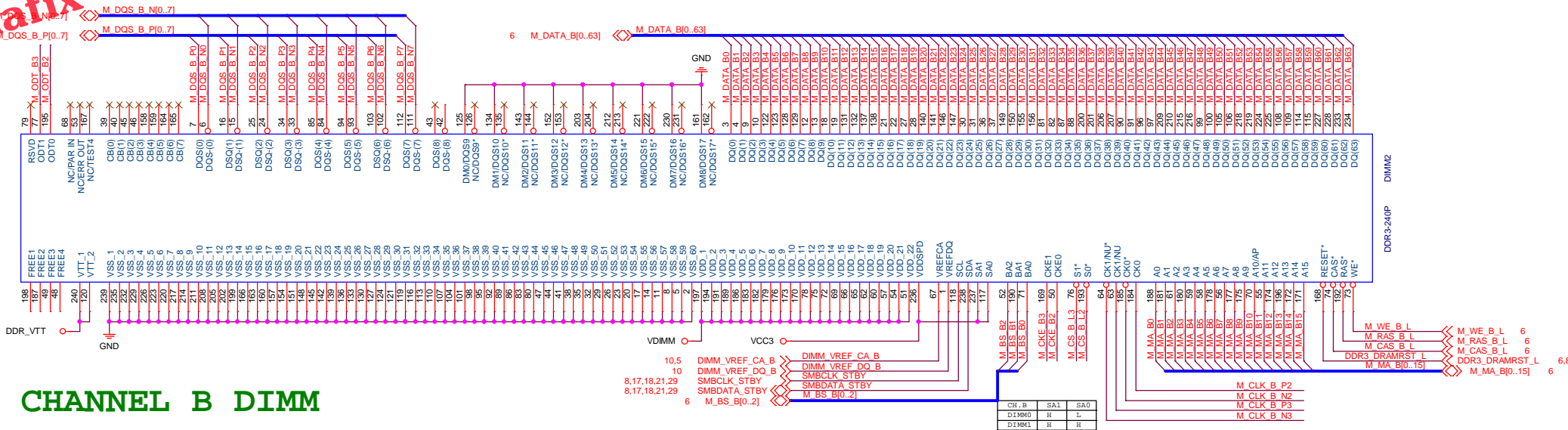


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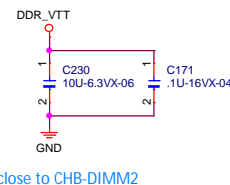
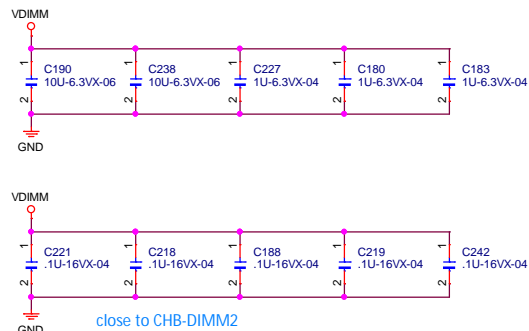
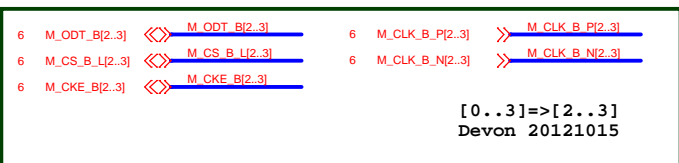
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CPU-DDR3			
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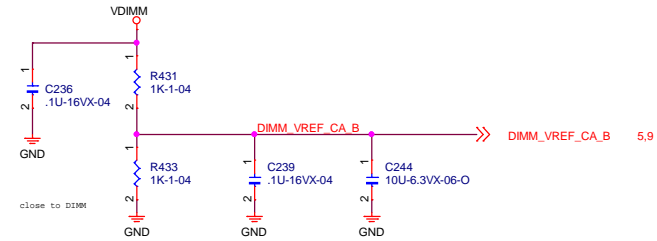
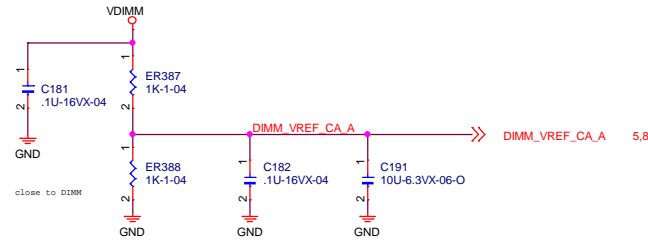




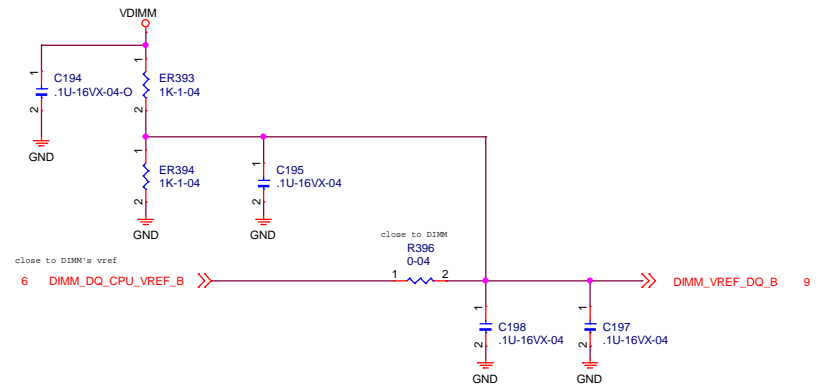
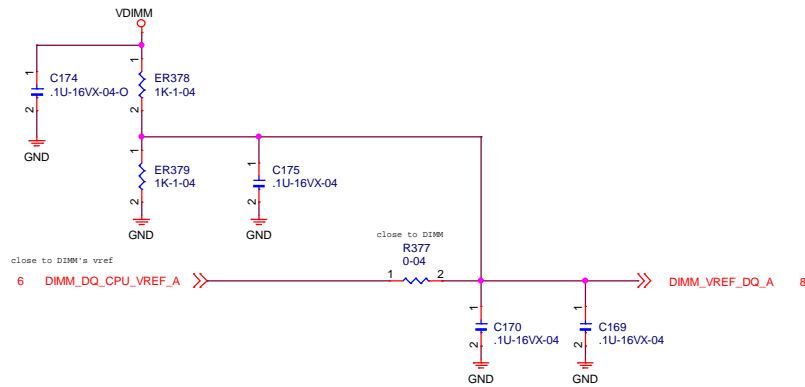
CHANNEL B DIMM



DIMM_VREF_CA Circuit



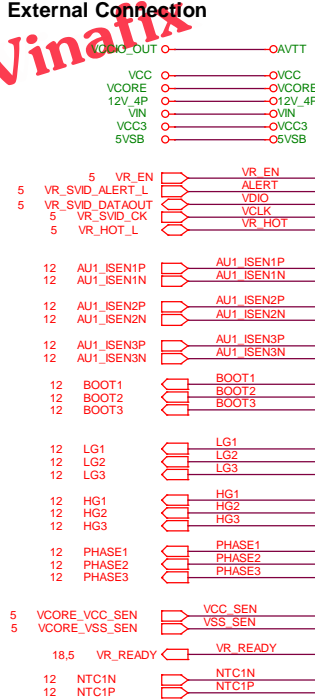
DIMM_VREF_DQ Circuit



External Connection

VCCIO_OUT

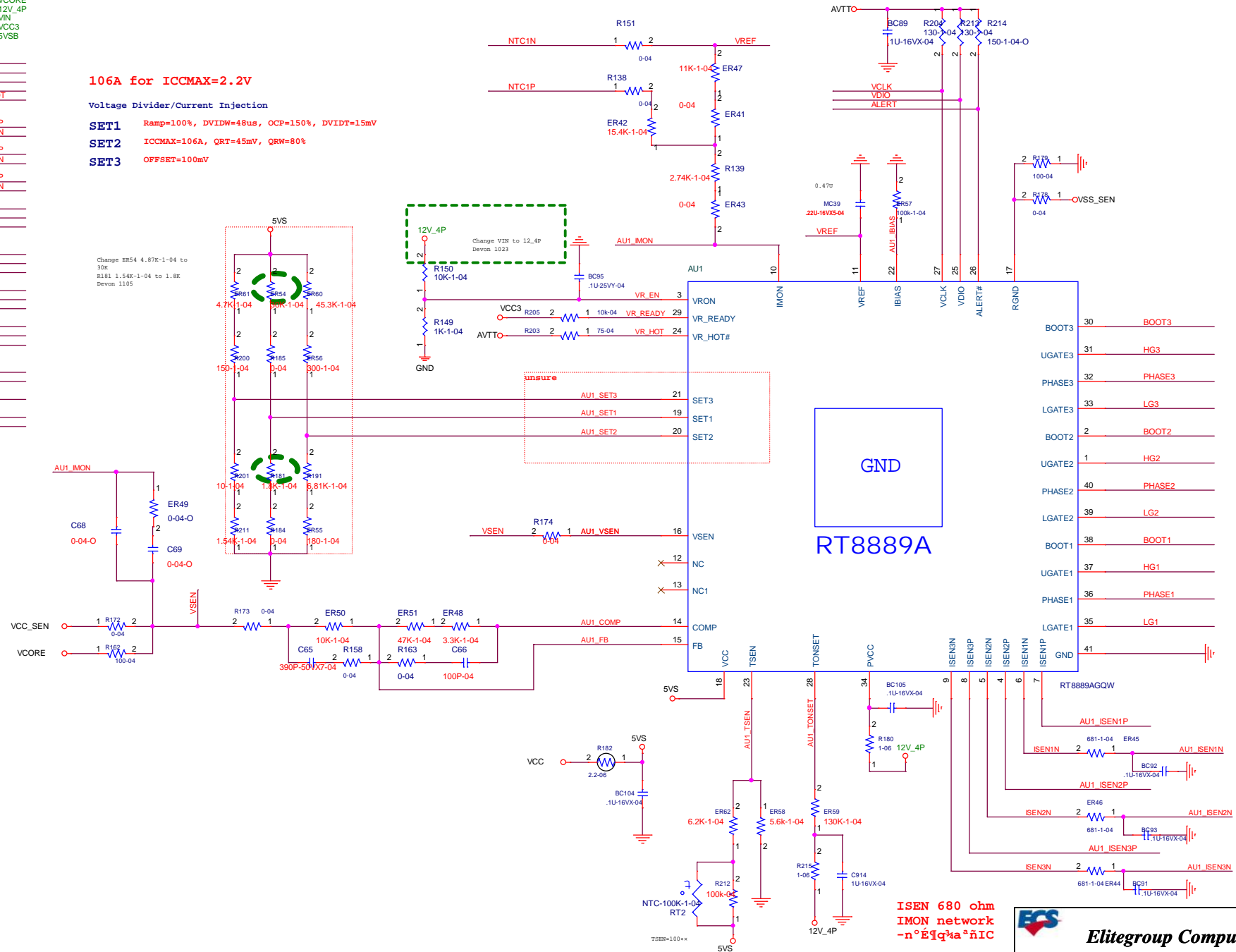
VCC

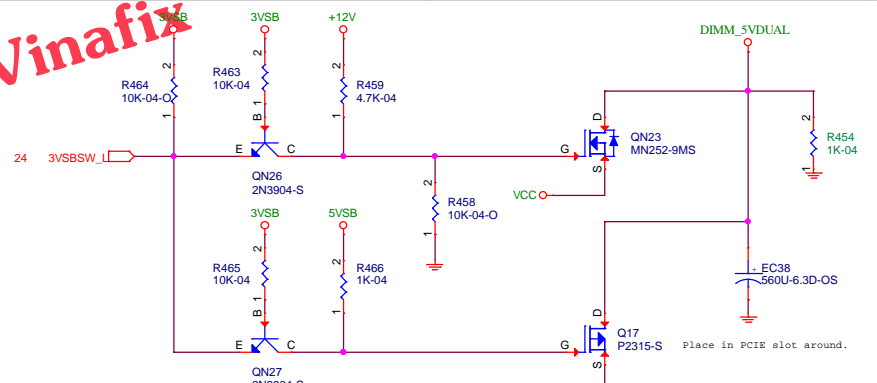


106A for ICCMAX=2.2V

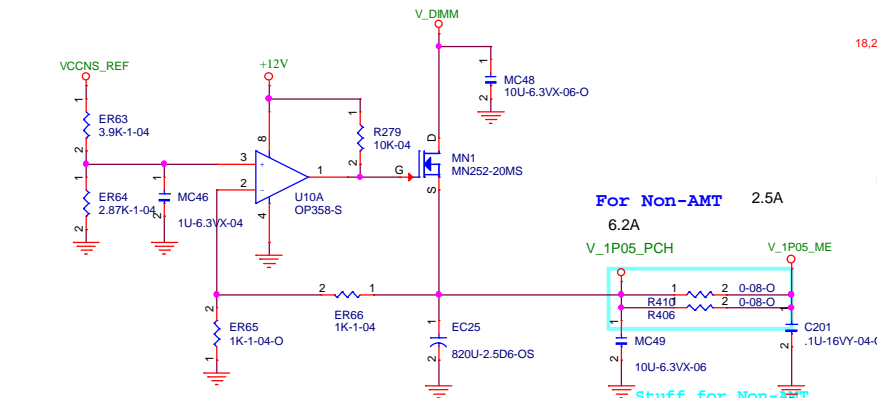
Voltage Divider/Current Injection

SET1	Ramp=100%, DVIDW=48us, OCP=150%, DVIDT=15mV
SET2	ICCMAX=106A, QRT=45mV, QRW=80%
SET3	OFFSET=100mV

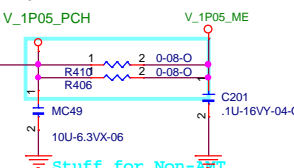




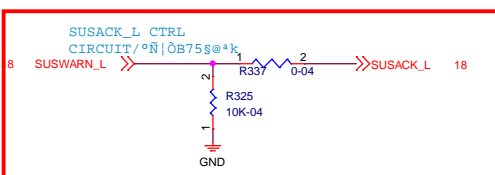
	S0	S3	S4/S5
S3_SW	H	L	H
VCC_DUAL	VCC	5VSB	0V



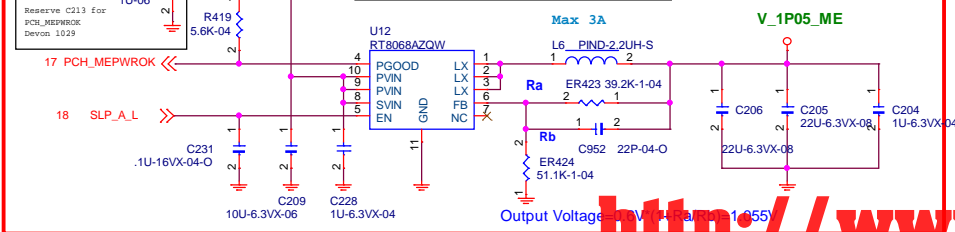
For Non-AMT 2.5A



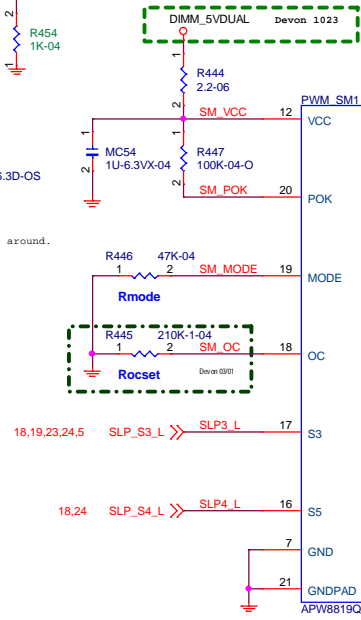
Stuff for Non-AMT



SLP_A_L	V_1P05_ME
High	Enable
Low	Disable



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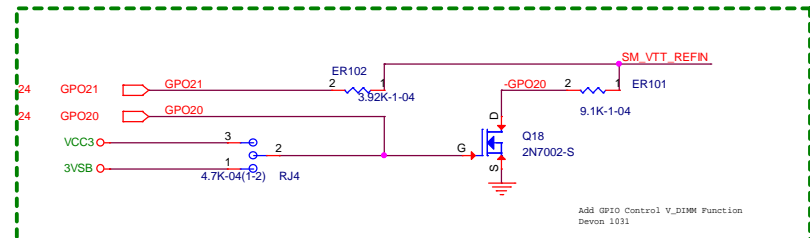


$$R_{ocset} = OCP \cdot Low-Side R_{ds(on)} / 10\mu A \cdot 8$$

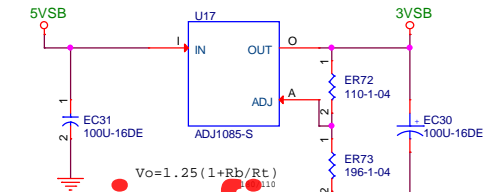
GPO20	GPO21	VDIMM
H	L	1.25V
L	L	1.35V
H	H	1.50V(default)
L	H	1.65V

S3 S5 Truth Table

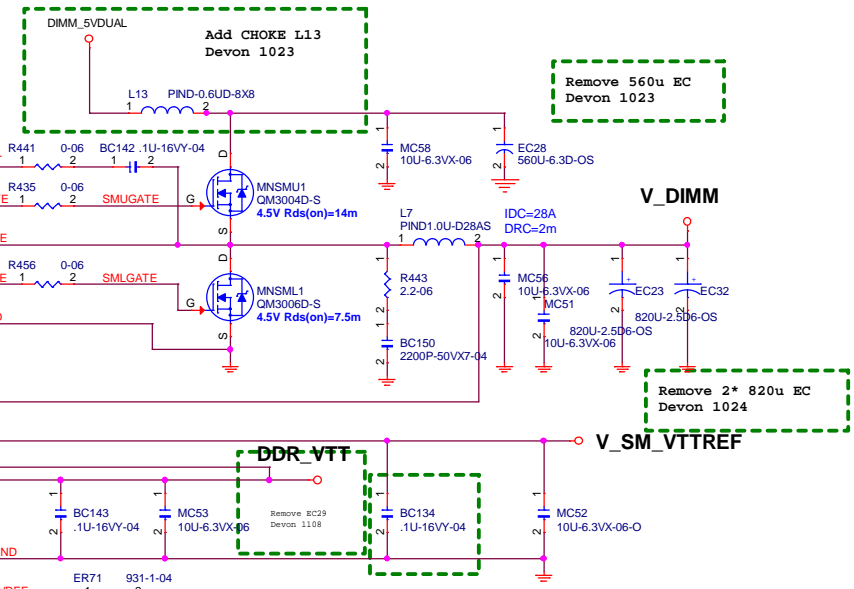
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	OUTPUT	OUTPUT	OUTPUT
S3	L	H	OUTPUT	OUTPUT	HIGH-Z
S4 / S5	L	L	DISCHARGE	DISCHARGE	DISCHARGE



Add GPO20 Control V_DIMM Function
Devon 1031

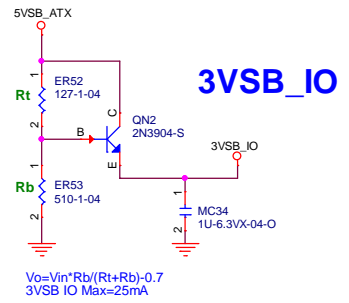


$$V_o = 1.25 \cdot (1 + R_b / R_t)$$



Frequency Selection

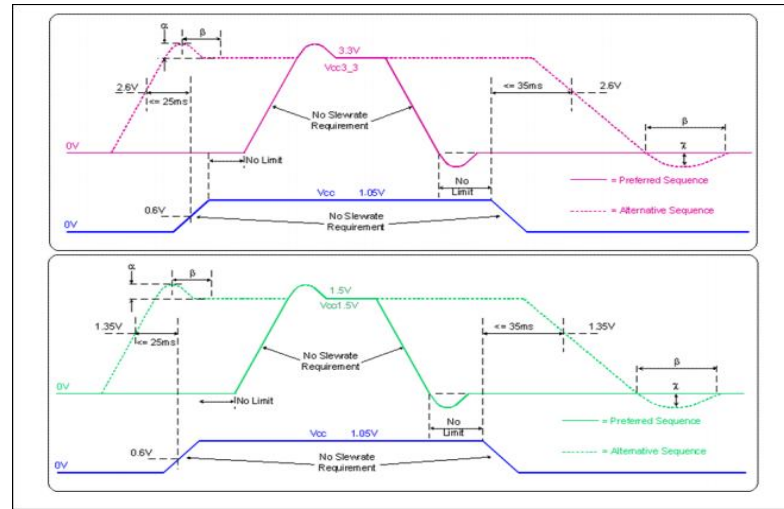
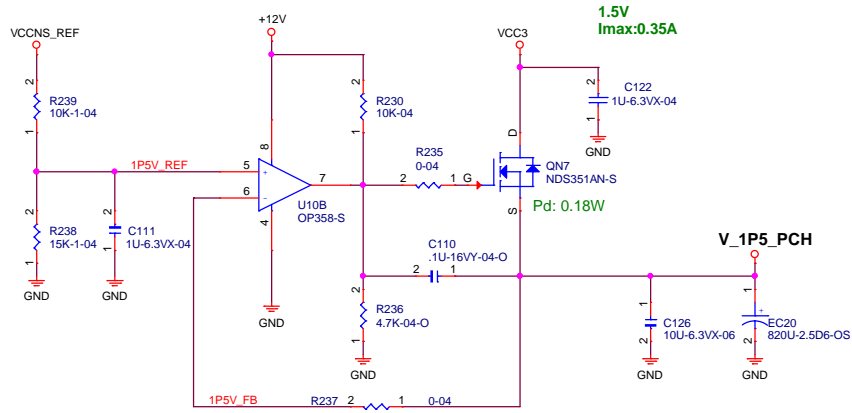
MODE	Rmode	FW(KHz)	DISCHARGE MODE
0	47K	400	Non-Tracking
1	68K	300	Non-Tracking
2	100K	300	Tracking
3	200K	400	Tracking
4	OPEN	500	Tracking



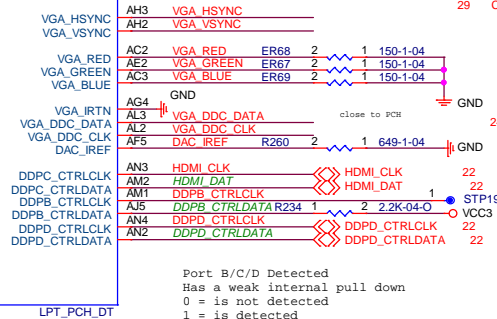
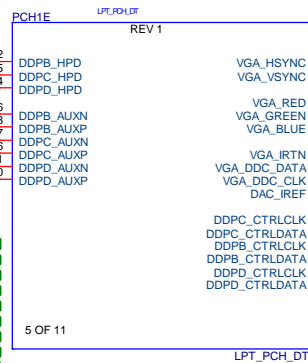
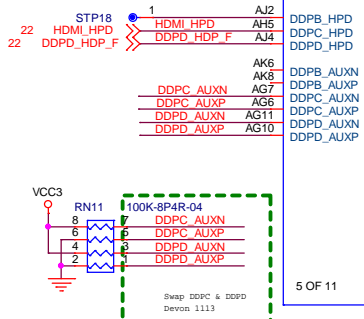
$$V_o = V_{in} \cdot R_b / (R_t + R_b) - 0.7$$

3VSB IO Max=25mA

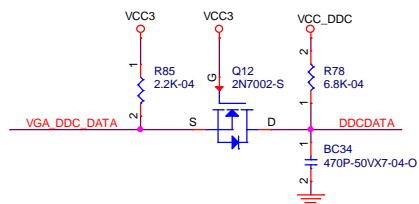
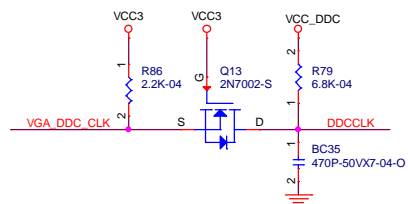
PCH DAC power



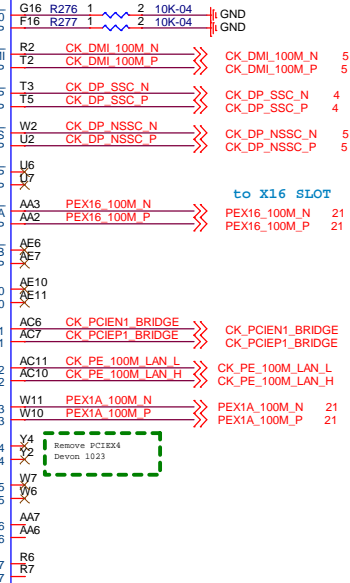
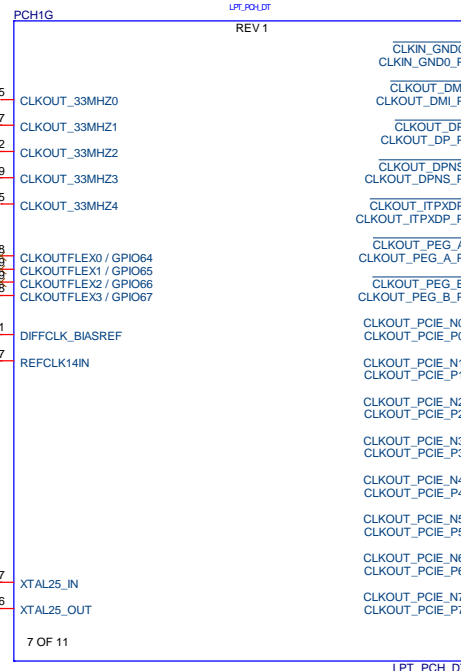
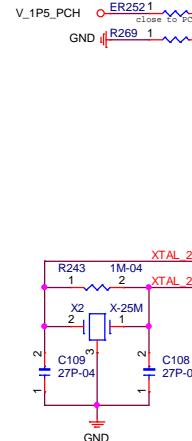
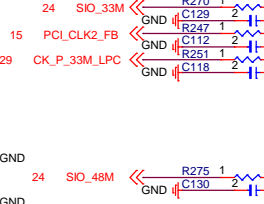
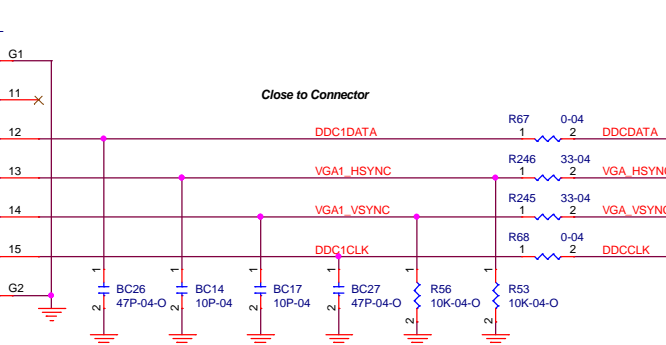
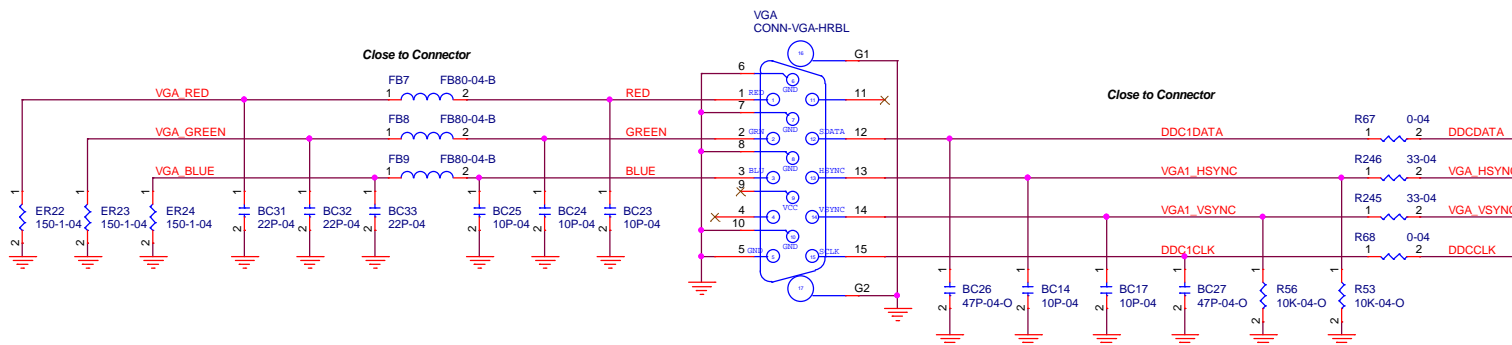
NC DDPC_AUXN,AUXP.
Devon 1023



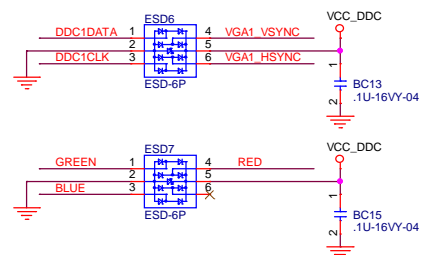
Port B/C/D Detected
Has a weak internal pull down
0 = is not detected
1 = is detected



VGA



ESD



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PCH-DDI/CLK/VGA		
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MODE	Ra	Rb
AMT	V	X
NON AMT	X	V

13 PCH_MEPWROK >> R383 1 2 0-04
4,18,24 PCH_PWROK >> R363 1 2 0-04-O
FROM S10

C164 .1U-16VX-04-O
GND

TACH0 AP28 TACH0 / GPIO17
TACH1 AT31 TACH1 / GPIO1
CR_GPIO6 AM28 TACH2 / GPIO6
CR_GPIO7 AV34 TACH3 / GPIO7
TACH4 AT30 TACH4 / GPIO68
TACH5 AV35 TACH5 / GP69

SCLOCK L38 SCLOCK / GPIO22
SLOAD H41 SLOAD / GPIO38
SDAT0 R31 SDATAOUT0 / GPIO39
SDAT1 L40 SDATAOUT1 / GPIO48

R360 10K-04 1 SATALED L
R375 10K-04 1 PCH_GPIO21
R311 10K-04 1 TACH1
R298 10K-04 1 TACH2
R300 1K-04 1 PCH_GPIO37

SATA3GP/GPIO37 1K-04 pull high VCC3
Devon 1113

RJ8 1 VCC3
PCH_GPIO16 2 3
10K-04(1-2) GND

RJ9 1 VCC3
PCH_GPIO49 2 3
10K-04(1-2) GND

Del SMBUS isolation schematic
Del pull high res.
Devon 1023

SMBus Logic Circuit

3VSB

R420 2.2K-04 1 SMBCLK_STBY <<> SMBCLK_STBY 8,9,18,21,29
R421 2.2K-04 1 SMBDATA_STBY <<> SMBDATA_STBY 8,9,18,21,29

Devon 1023

port 2,3 disable in H81
port 4,5 are SATA 3Gb/s in B85/H81

SATA_RXN0 A28 SATA3_RX_P0
SATA_RXP0 F31 SATA3_TX_N0
SATA_TXN0 H31 SATA3_TX_P0
SATA_RXN1 U30 SATA3_RX_N1
SATA_RXP1 C30 SATA3_TX_P1
SATA_TXN1 B34 SATA3_TX_N1
SATA_TXP1 C34 SATA3_TX_P1

SATA_RXN2 A31 SATA3_RX_N2
SATA_RXP2 B31 SATA3_TX_P2
SATA_TXN2 B35 SATA3_TX_N2
SATA_TXP2 D35 SATA3_TX_P2
SATA_RXN3 B32 SATA3_RX_N3
SATA_RXP3 C32 SATA3_TX_P3
SATA_TXN3 G33 SATA3_TX_N3
SATA_TXP3 F33 SATA3_TX_P3

SATA_RXN4 / PERn1 A26 SATA3_RX_N4
SATA_RXP4 / PERn1 B26 SATA3_TX_P4
SATA_TXN4 / PETn1 L28 SATA3_TX_N4
SATA_TXP4 / PETn1 K28 SATA3_TX_P4
SATA_RXN5 / PERn2 C27 SATA3_RX_N5
SATA_RXP5 / PERn2 B27 SATA3_TX_P5
SATA_TXN5 / PETn2 F28 SATA3_TX_P5
SATA_TXP5 / PETn2 H35 R316 1 2 10K-04
CLKIN_SATA H36 R315 1 2 10K-04
CLKIN_SATA_P

SATALED# J39 SATALED_L
SATA_RCOMP Q33 R309 1 2 7.5K-1-01 V_1P5_PCH

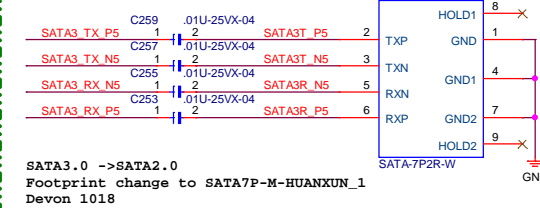
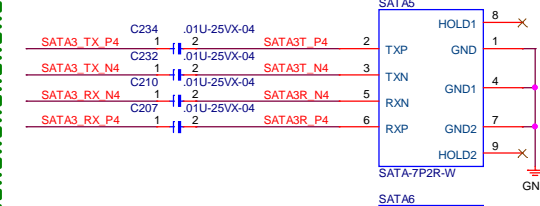
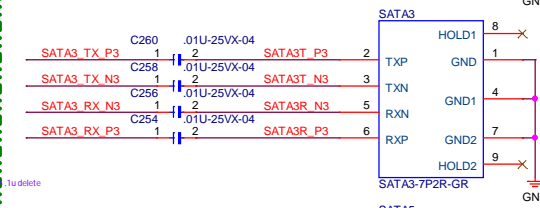
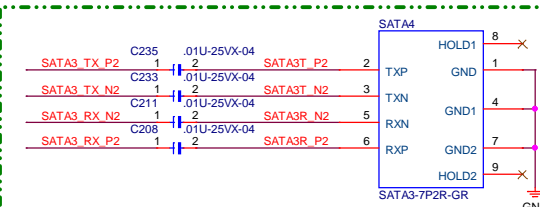
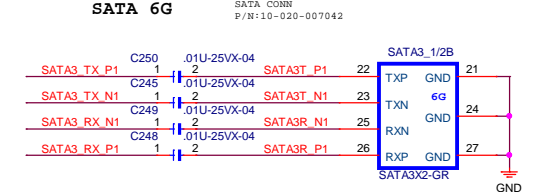
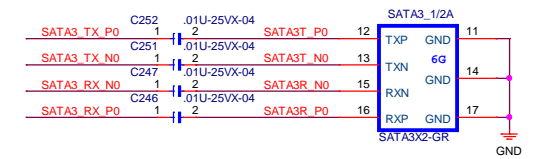
SATA0GP / GPIO21 M37 PCH_GPIO21
SATA1GP / GPIO19 J40 PCH_GPIO19
SATA2GP / GPIO36 H40 PCH_GPIO36
SATA3GP / GPIO37 N41 PCH_GPIO37
SATA4GP / GPIO16 M39 PCH_GPIO16
SATA5GP / GPIO49 N40 PCH_GPIO49

*GPIO19 with internal pull-up
*GPIO36 with internal pull-down

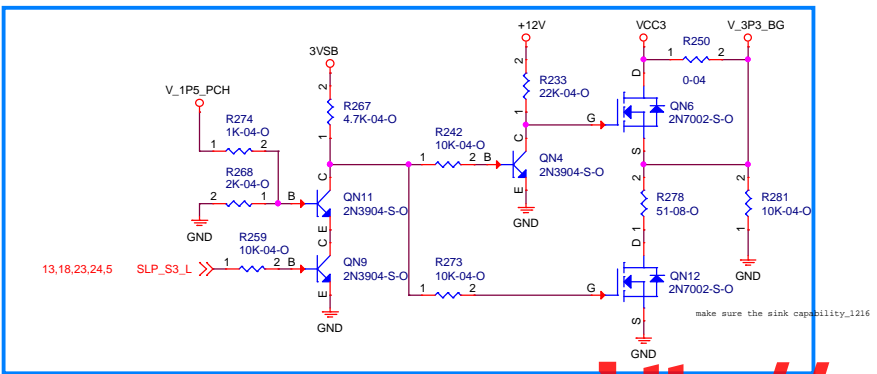
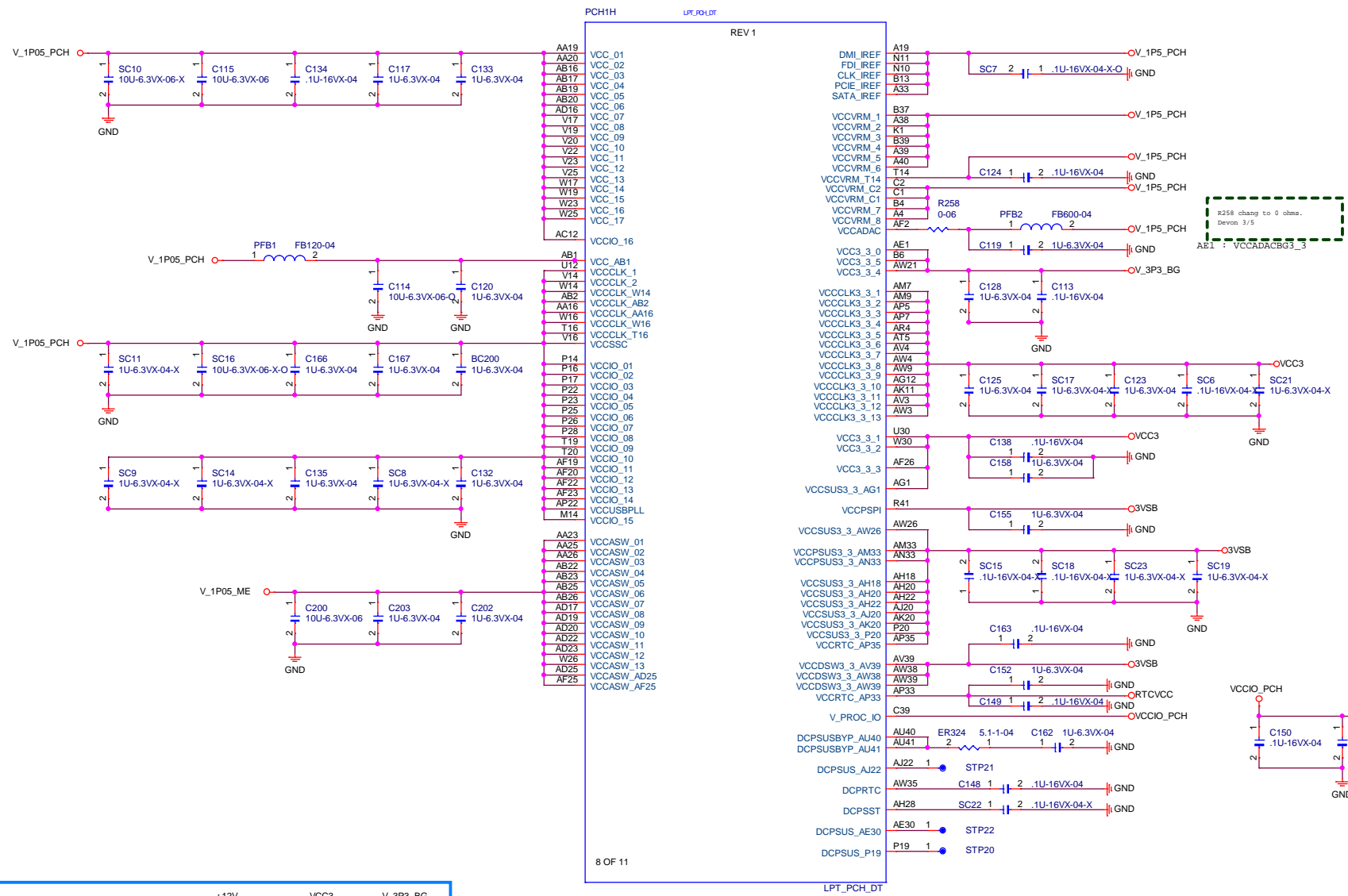
EDP_BKLTCTL AP2
EDP_BKLTEN AT2
EDP_VDDEN AP1

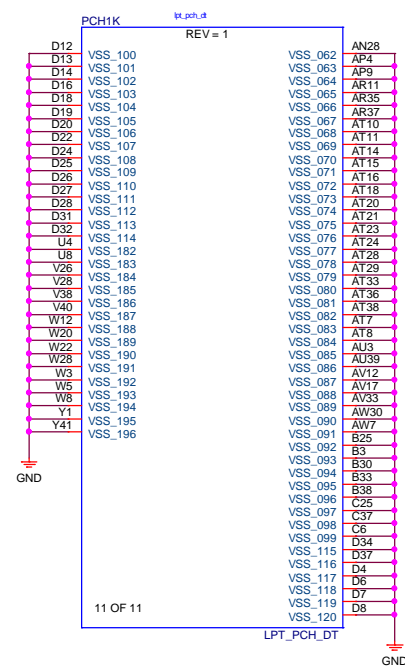
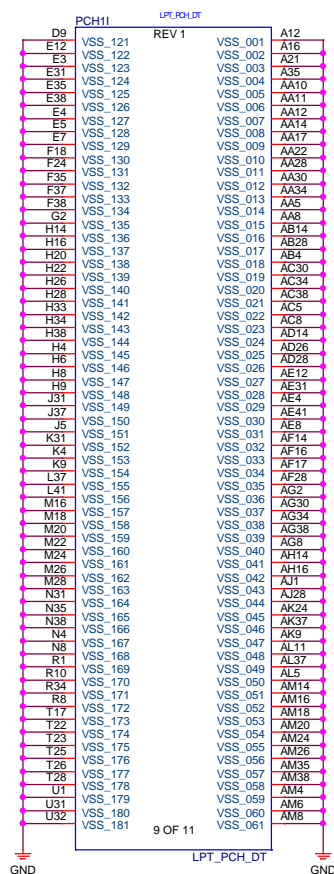
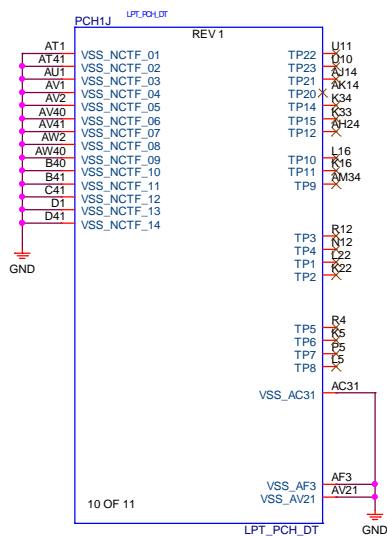
RSVD_N30 N30 A20GATE 24 KBRST_L_R change KBRST_L BY PAK to delete
RCIN# K36 KBRST_L 24
SERIRQ G39 SERIRQ 24,29 PCH_THERMTRIP_L 5
THRMTRIP# C40
PECI G40
PM_SYNC F40 PM_SYNC 5
PLTRST_PROC# F41 CPU_PLTRST_L 5

LPT_PCH_DT

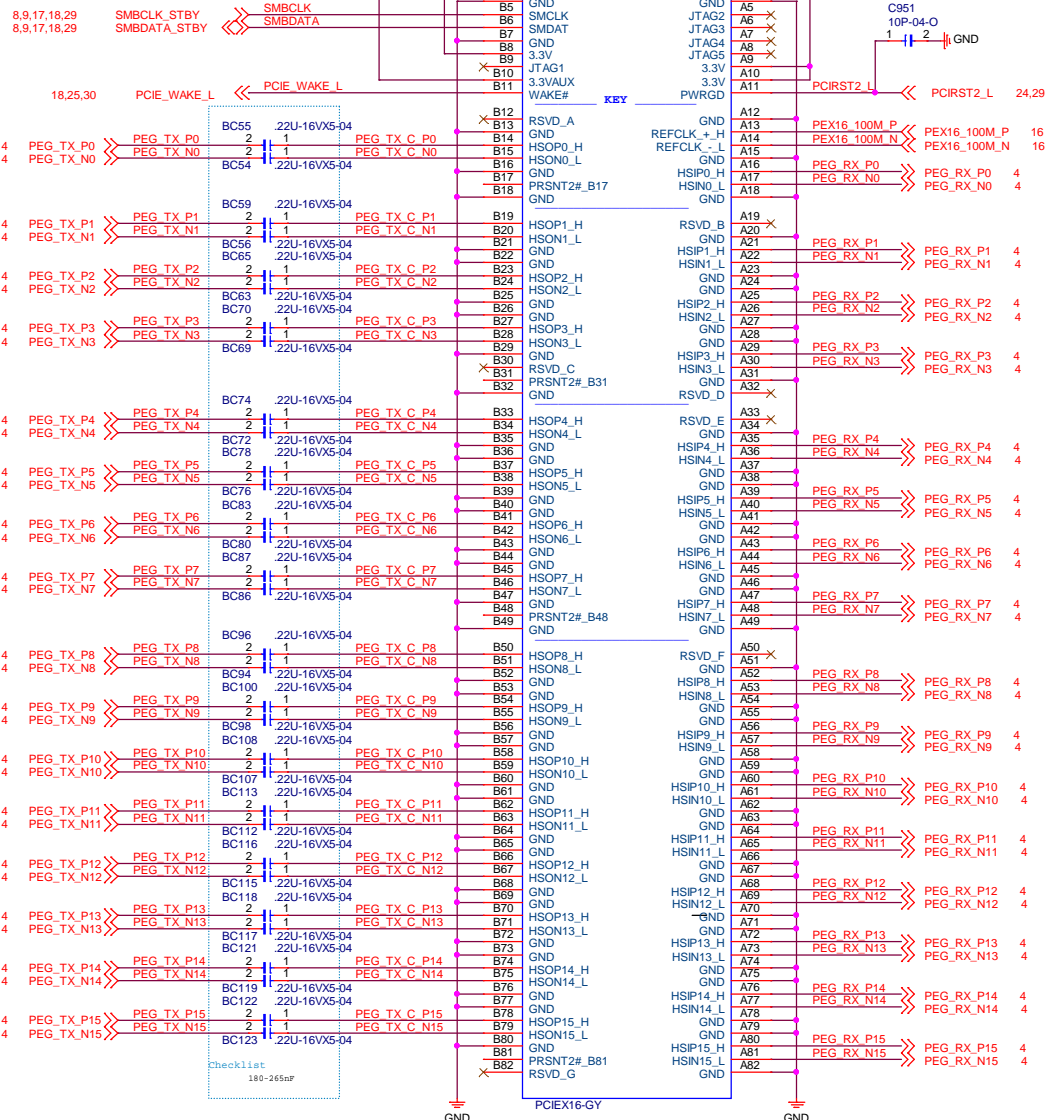


SATA3.0 ->SATA2.0
Footprint change to SATA7P-M-HUANXUN_1
Devon 1018

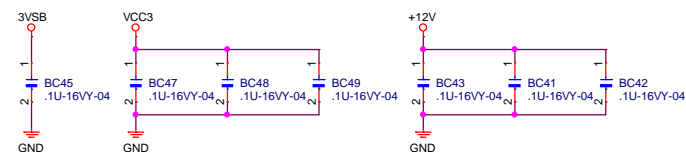
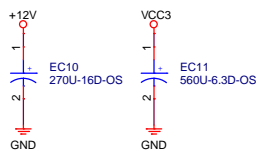
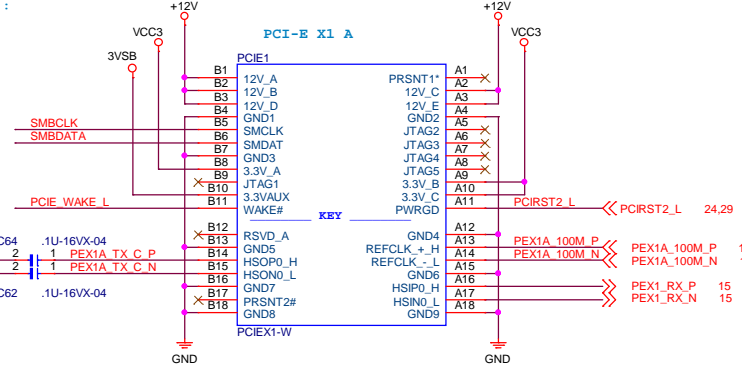




PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



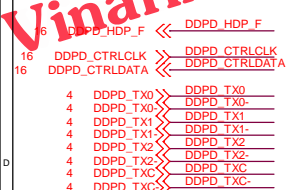
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A



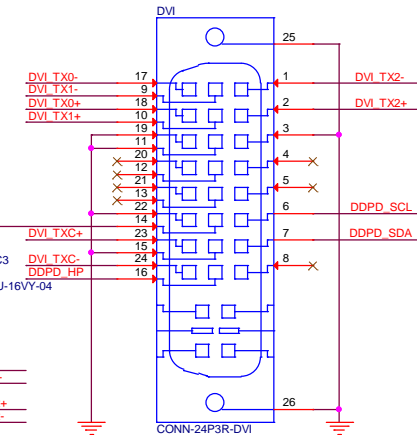
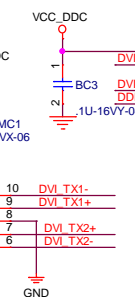
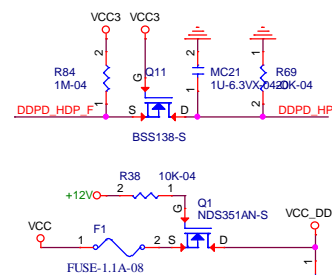
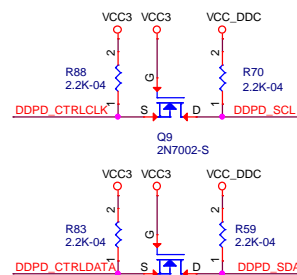
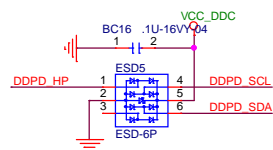
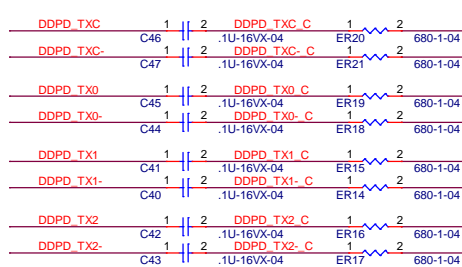
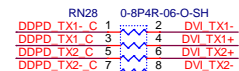
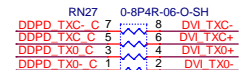
Elitegroup Computer Systems

File		
Slot PCI-EX16 / PCI-EX1		
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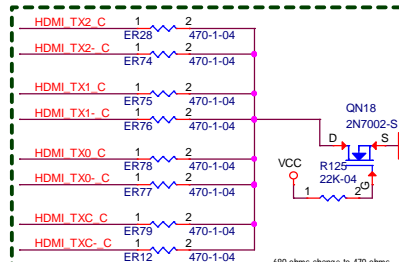
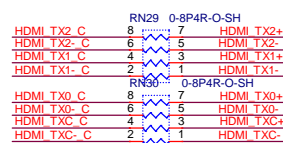
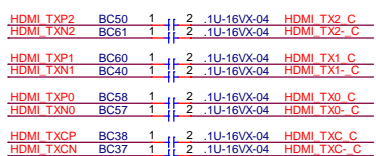
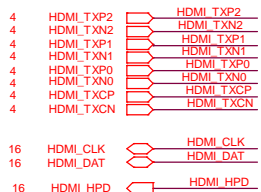
External Connection



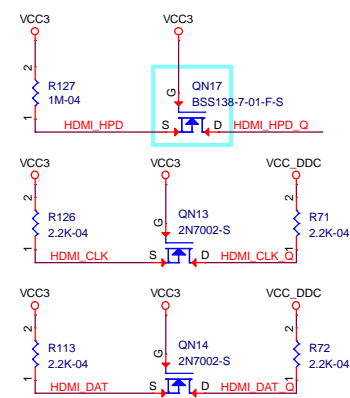
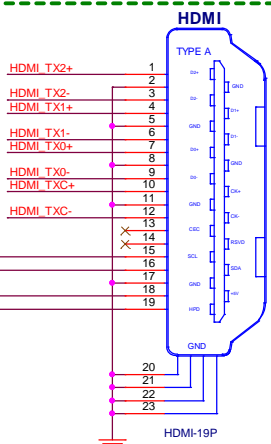
DVI



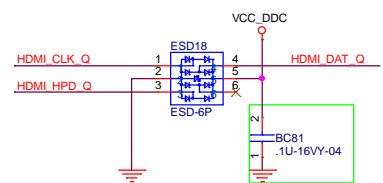
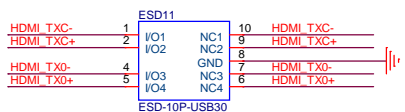
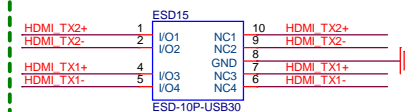
03-013-428402



680 ohms change to 470 ohms
to fix HDMI 7-2 issue
Devon 03/01

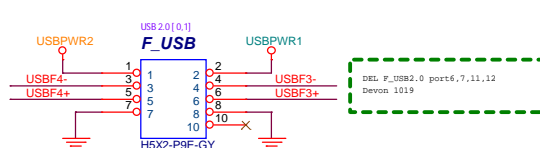
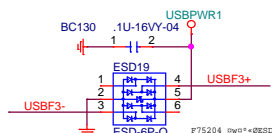


DEL DP MODULE.
Only save HDMI function.
Devon 1023

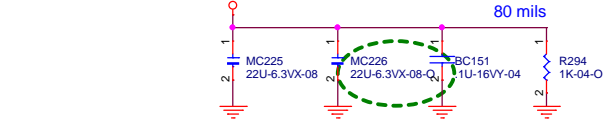
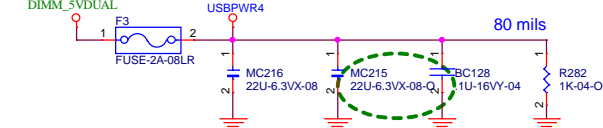
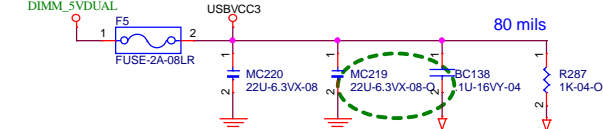
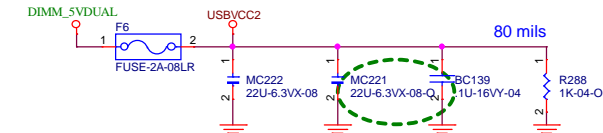
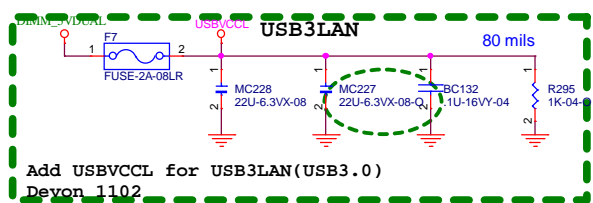


Devon 1102

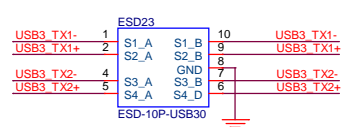
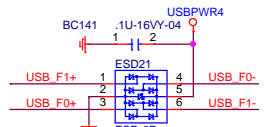
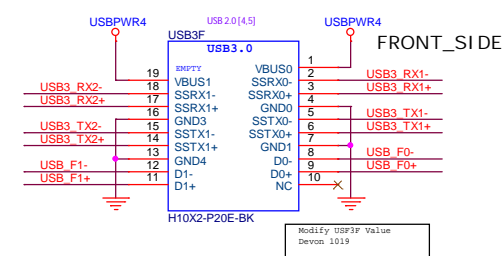
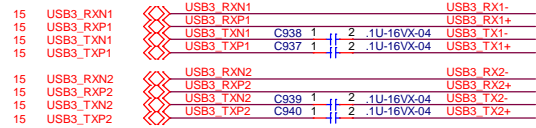
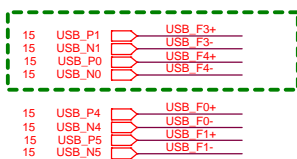
External Connection



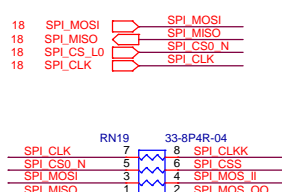
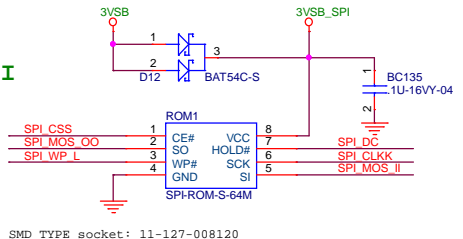
DEL USBPWR3
Devon 1022



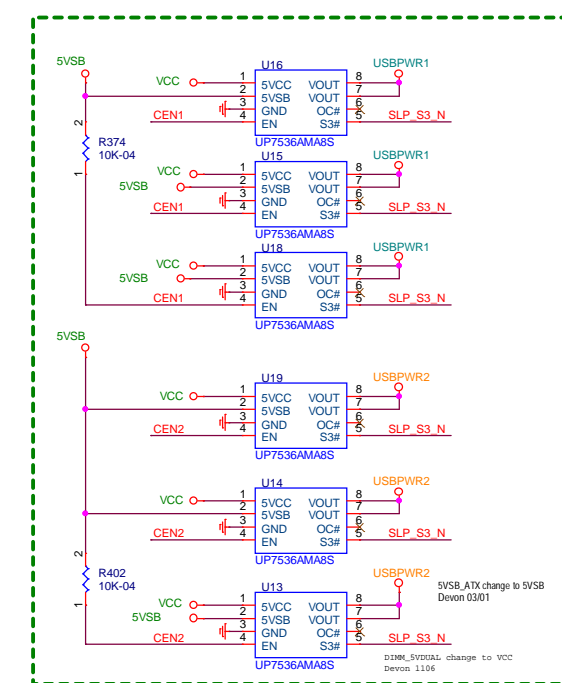
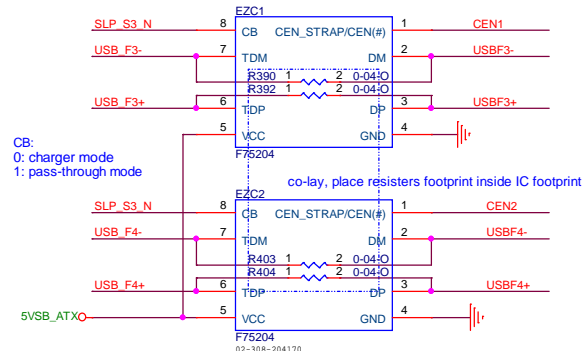
5,13,18,19,24 SLP_S3_L SLP_S3_N



SPI



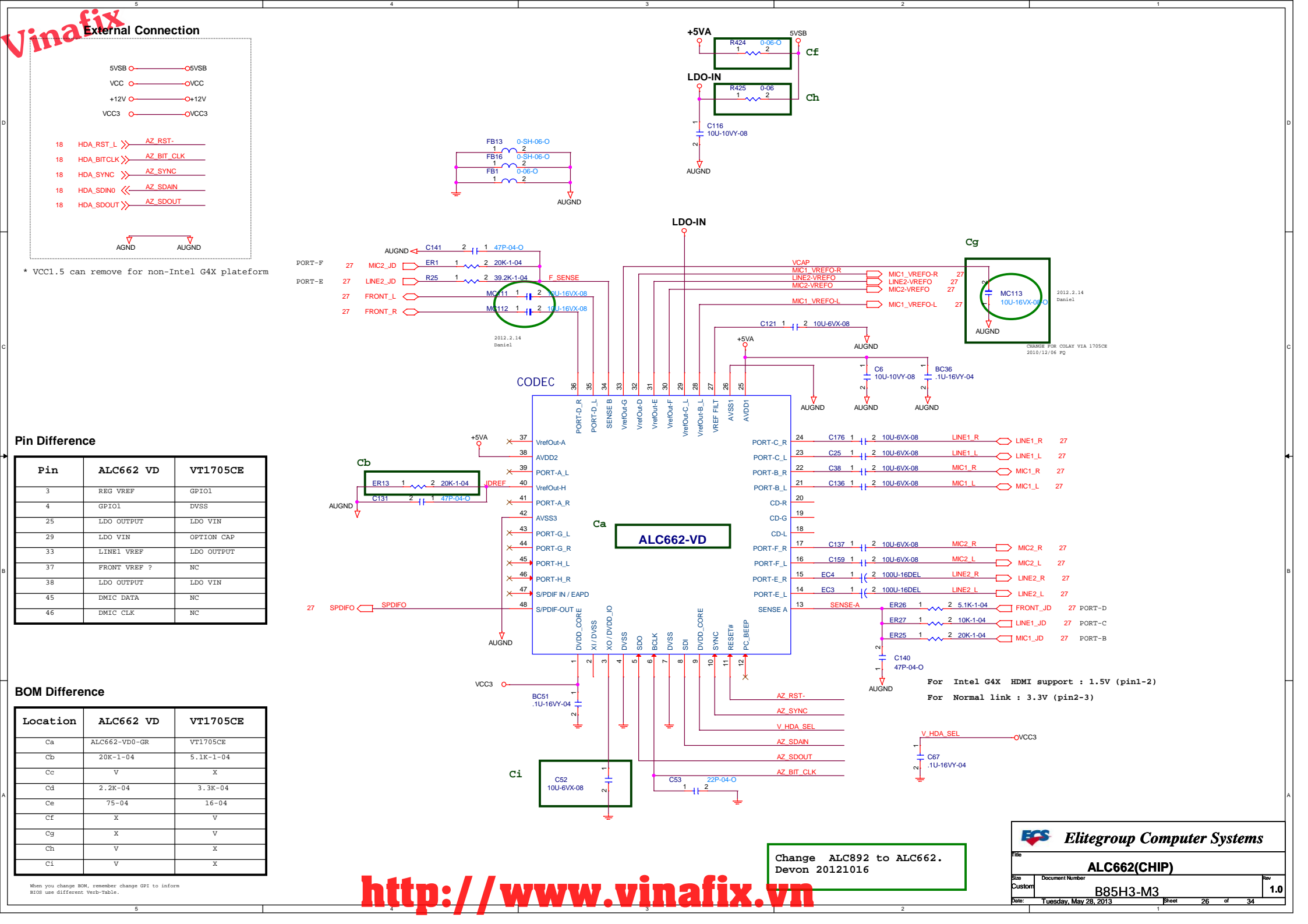
FUSB1 EZ CHARGE

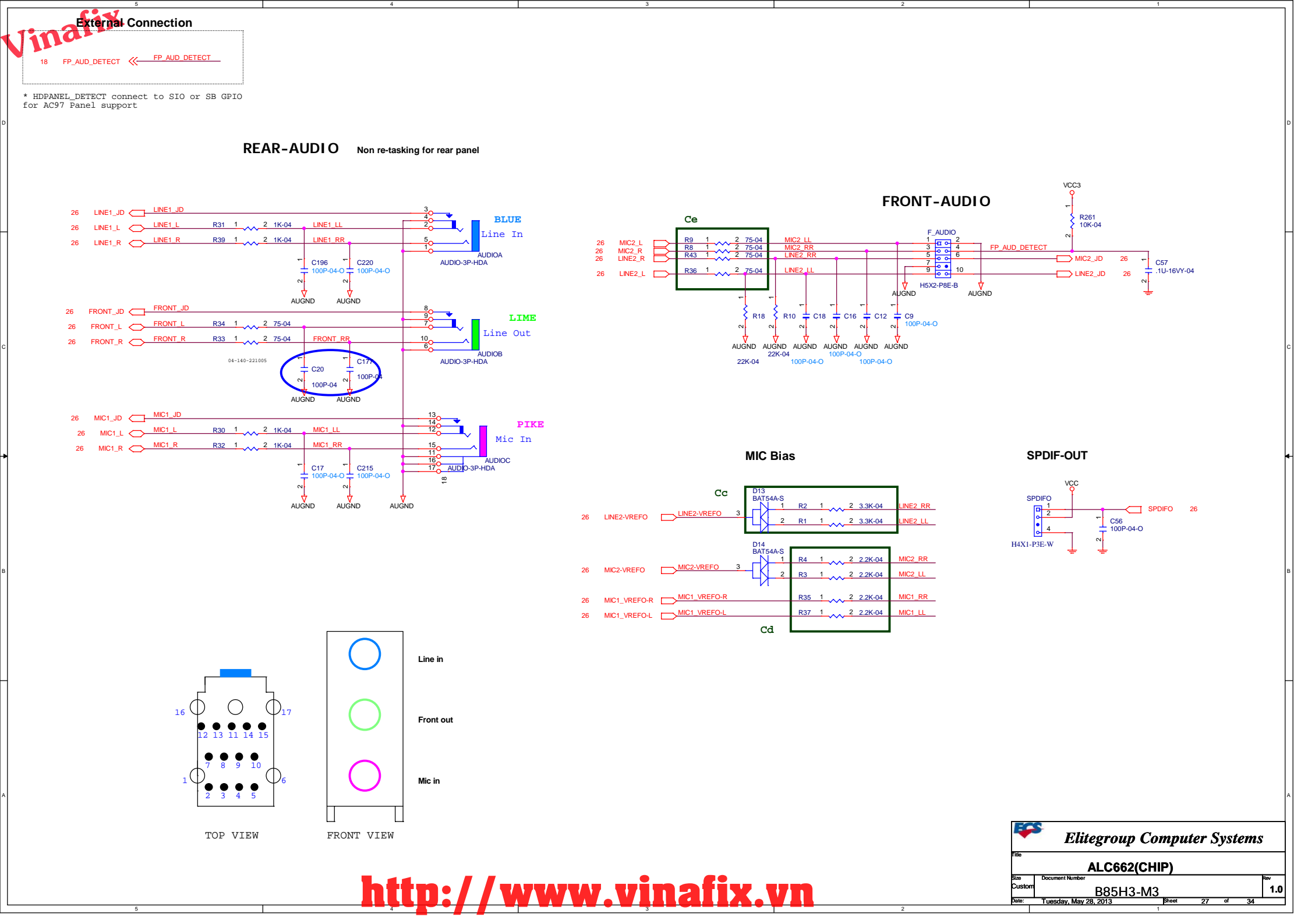


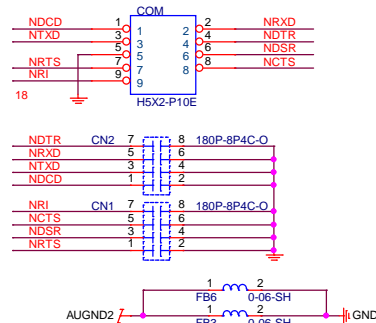
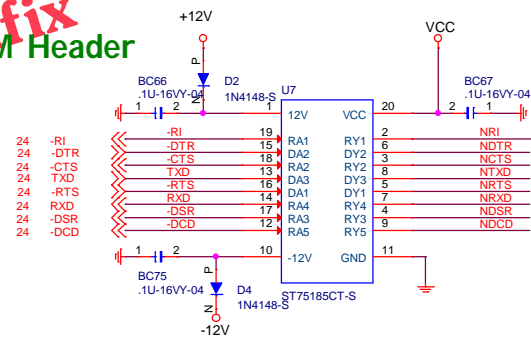
<http://www.vinafix.vn>

Elitegroup Computer Systems

File		F_USB / SPI	
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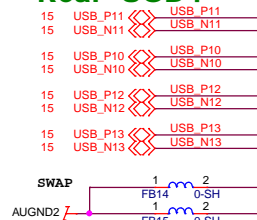




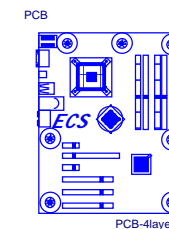
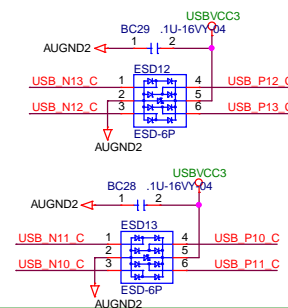
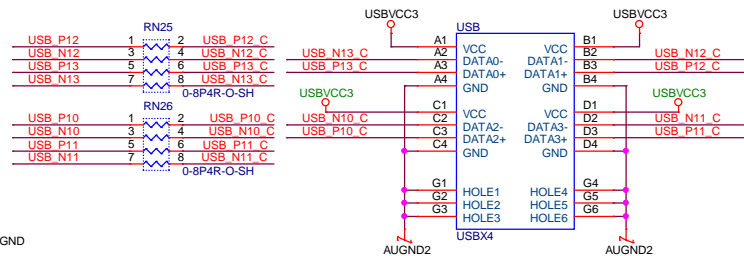
1)Circuit type 1

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Layer 2:PWR	<input type="text"/>
Layer 3:GND	<input type="text"/>
Layer 4:BOTTOM	<input type="text"/>

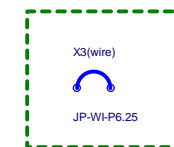
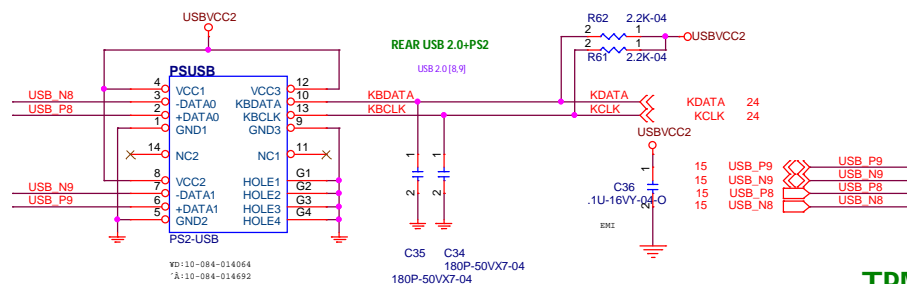
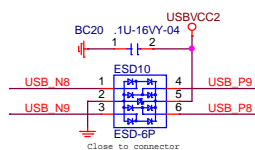
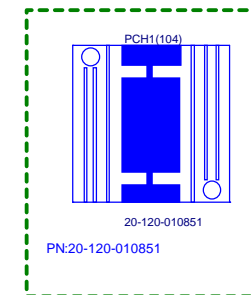
Rear USB4



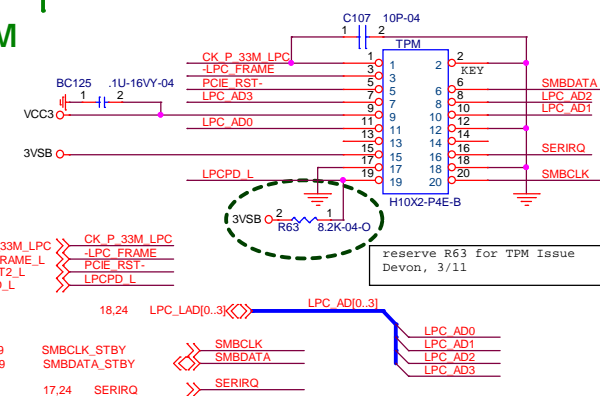
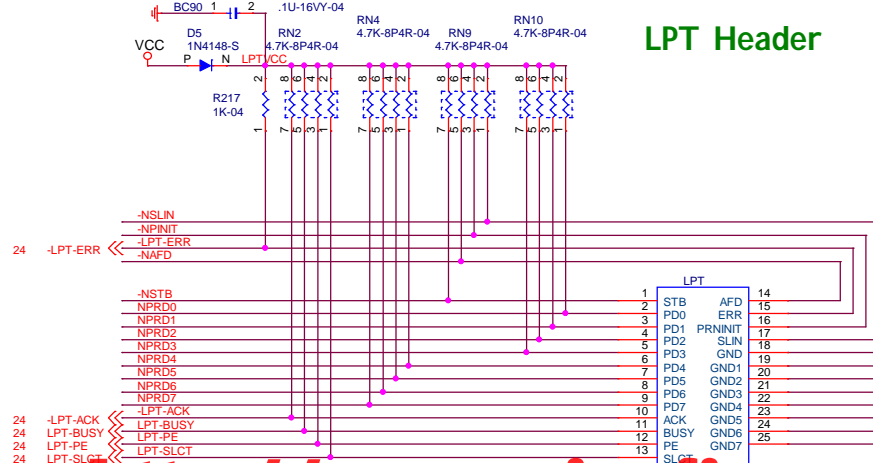
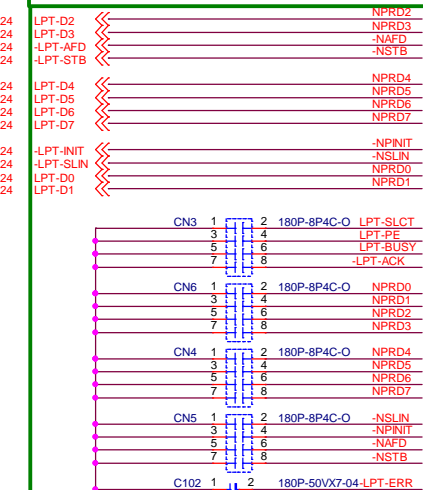
Devon 1019



PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



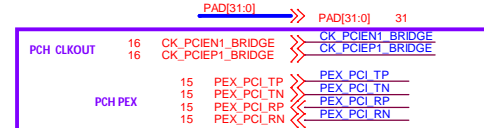
TPM



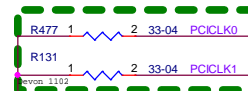
Elitegroup Computer Systems

Title			
LPT / COM / RUSB / TPM			
Size	Document Number		Rev
Custom	B85H3-M3		1.0
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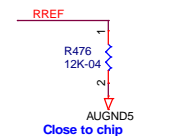
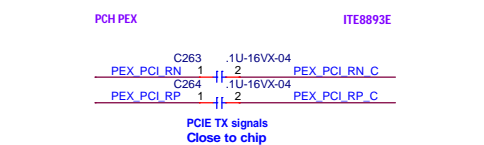
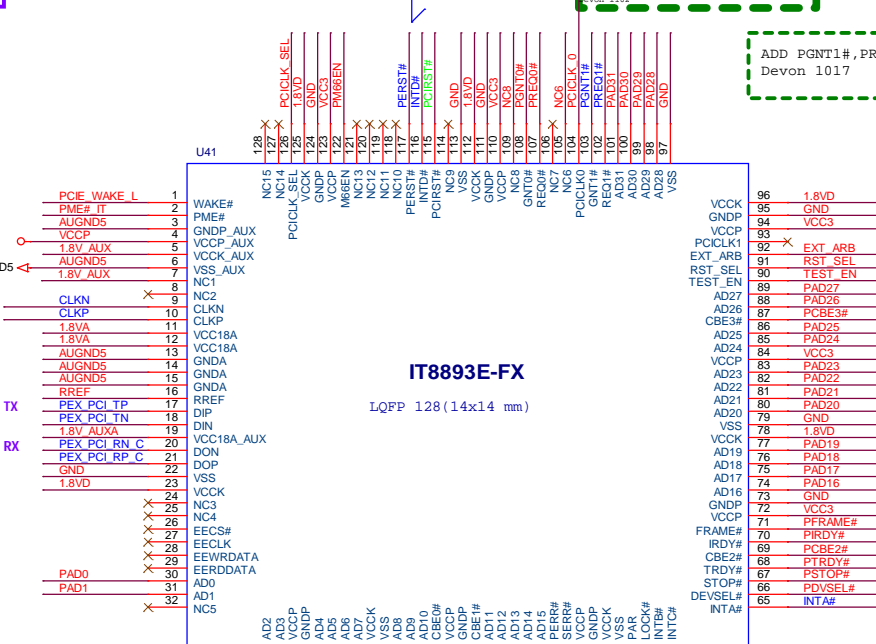
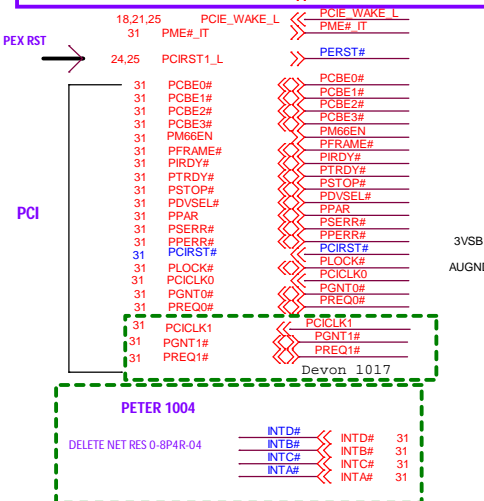
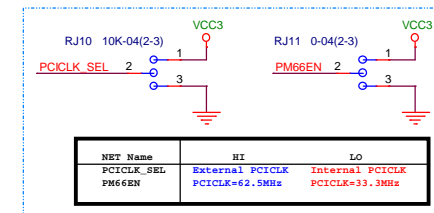
External Connection



PCB layout note:
Connect to PCIE
PERST# Signal



```
ADD PGNT1#,PREQ1#,PCICLK1
Devon 1017
```



PCIE DIP;DIN;DOP;DON PCB layout note:

To meet Differential Impedance :85 ohm +/- 15%

To meet Single-ended Impedance :50 ohm +/- 15%

PCIE DIP and DIN trace width:9.5 mils

PCIE DOP and DON trace width:9.5 mils

Space between DIP/DIN and DOP/DON:14.5 mils

L1 & L2 height:5 mils

The signal traces Number of vias: 2 (Max.)

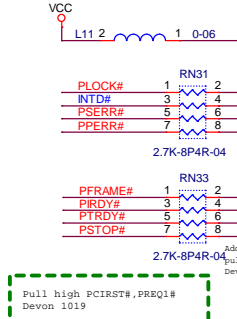
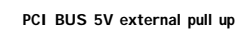
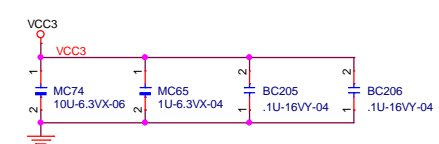
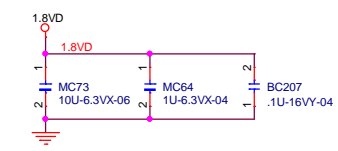
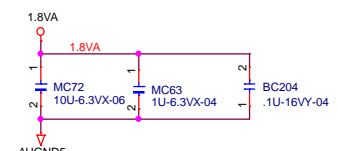
The signal trace above analog GND plane

Spacing from other groups:>25 mils

Total trace length: 12 inches (Max.)

PCIE CLK PCB layout note:

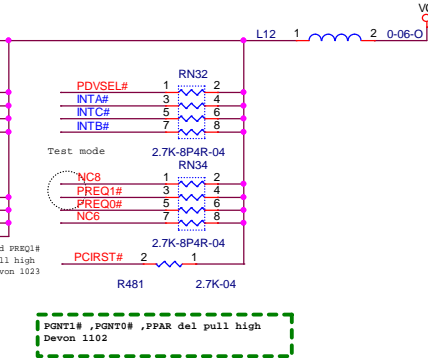
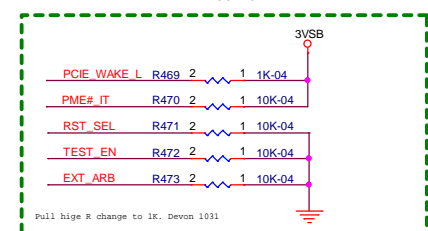
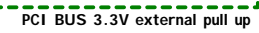
- To meet Differential Impedance :100 ohm +/- 15%
- To meet Single-ended Impedance :50 ohm +/- 15%
- CLKP and CLKN trace width:7 mils
- Space between CLKP and CLKN:14 mils
- L1 & L2 height:5 mils
- The signal traces Number of vias: 4 (Max.)
- The signal trace above analog GND plane
- Spacing from other groups:>25 mils
- Total trace length: 12 inches (Max.)

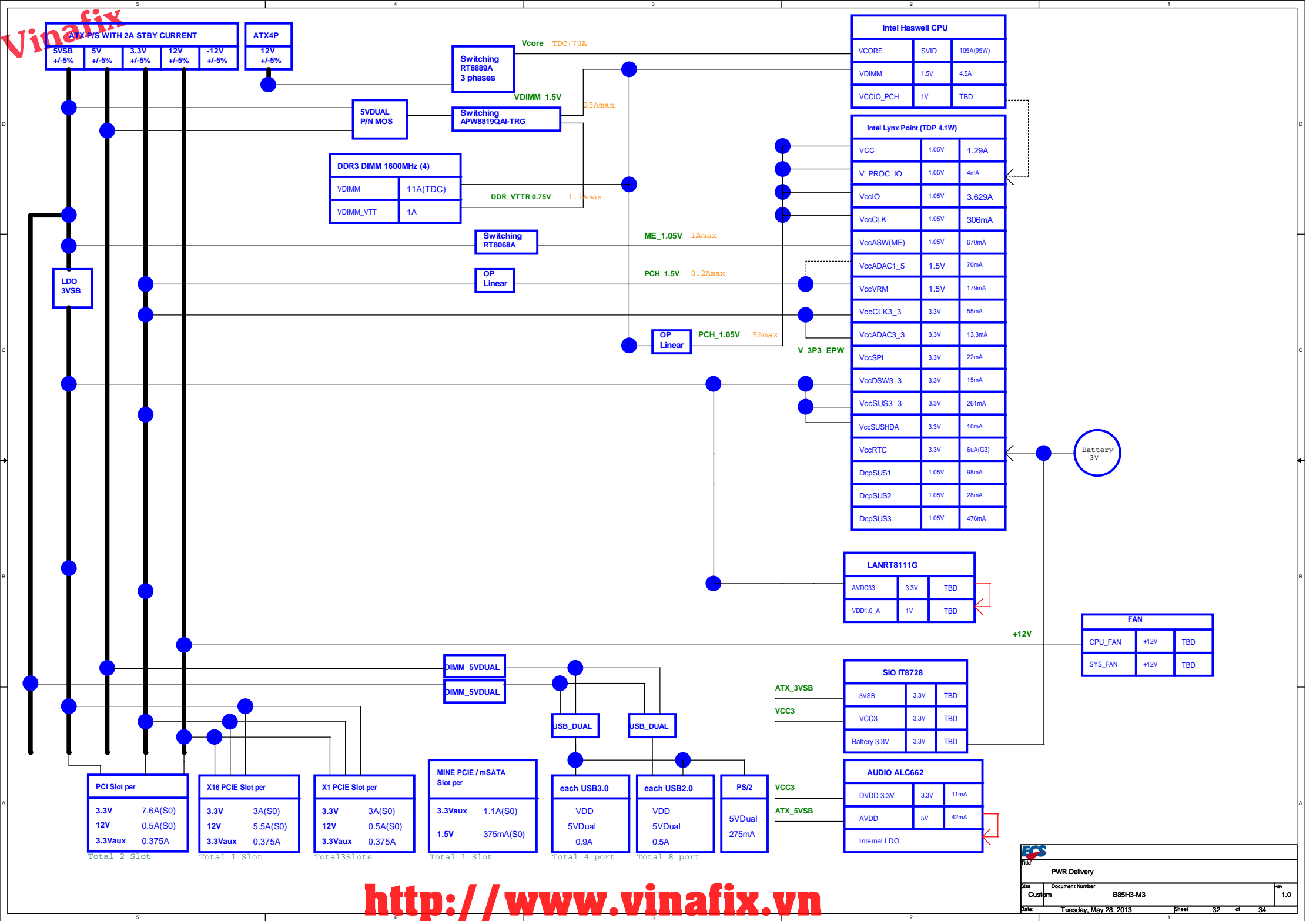


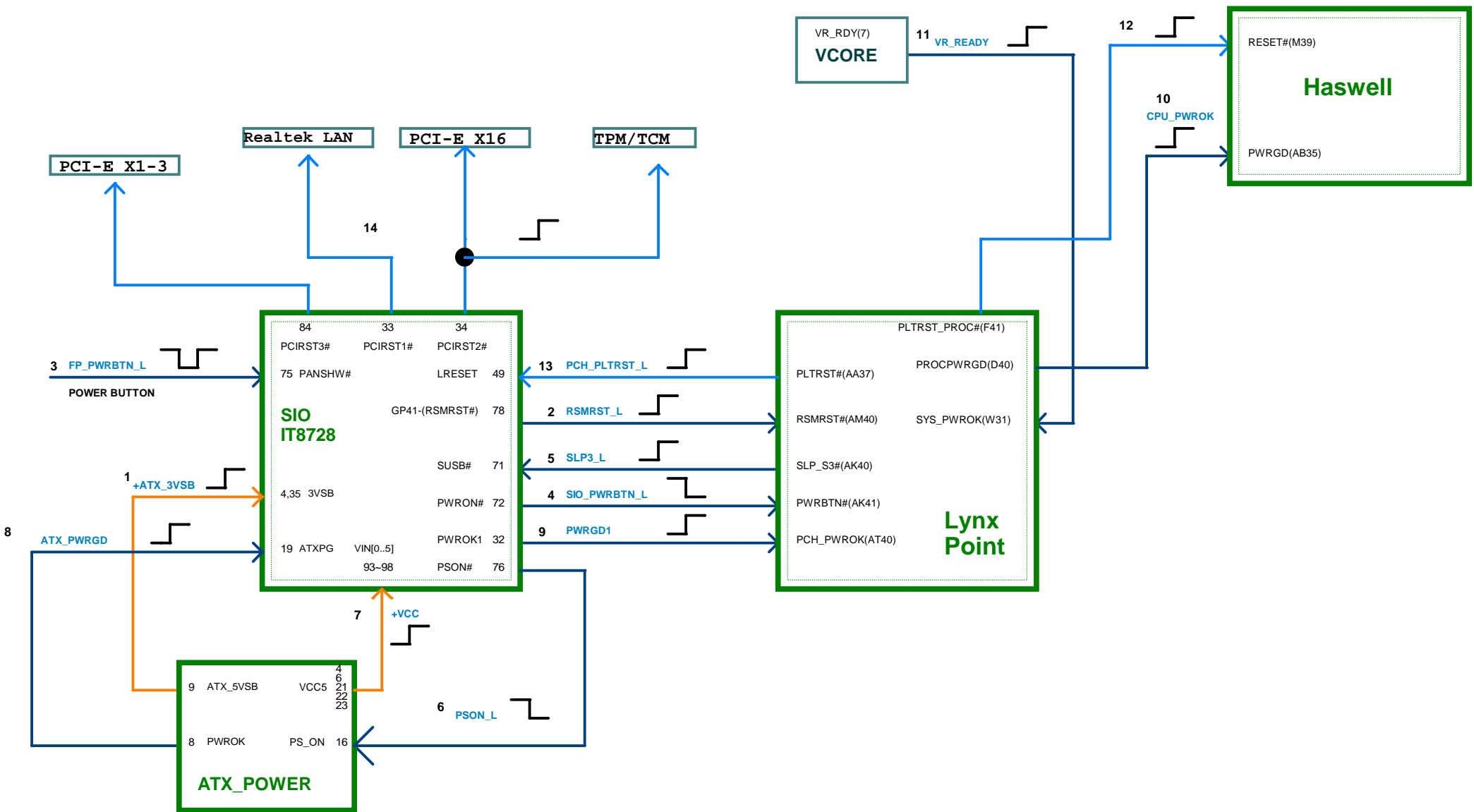
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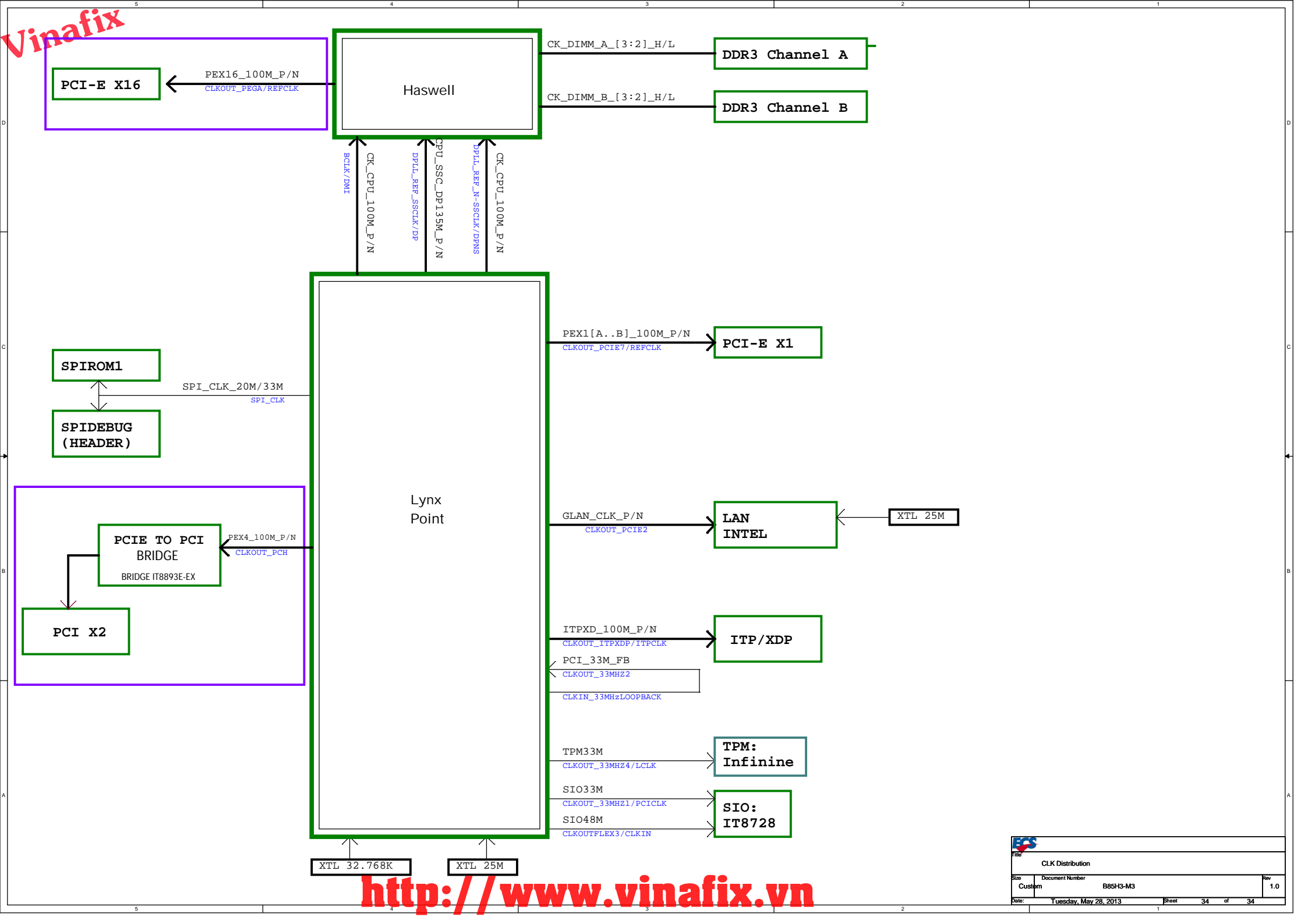
Pull high PCIRST#,PRE
Devon 1019

```









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