GA-MA74GM-S2H

Revision : 4.11

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Title: COVER SHEET		
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Model Name:GA-MA74GM-S2H

Component value change history

Version:4.11

P-Code: U97118-0

Date	Change Item	Reason
2009.08.12	4.0A New BOM Release.	Modify from 9MMA76G2H-00-01
2009.08.25	4.0B BOM Release.	Modify NB_HS 4§ to 3§ for stock issue
2009.09.11	4.0F BOM Release.	Change NB_HS & SB_HS heatsink(金黃色) to heatsink(鐵灰色)
2009.11.02	4.1A BOM Release	Add EUP function ,Colay ALC892
2009.12.01	4.1B BOM Release	Add Codec ESD PROTECT DIODE
2010.04.12	4.1B BOM Release	Add HDMI function

Circuit or PCB layout change for next version

Date	Change Item	Reason
2009.08.11	4.0 Gerber out	Modify from GA-MA76GM-S2H 0.1
2009.08.24	4.01 Gerber out	Modify NB_HS 4§ to 3§ for stock issue
2009.10.30	Rev4.1 Gerber-out	Add EUP function ,Colay ALC892
2009.11.30	Rev4.11 Gerber-out	Add Codec ESD PROTECT DIODE
2010.04.08	Rev4.11 Gerber-out	Modify silkscreen (share GA-MA74GM-S2 Rev4.11 PCB)

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Title: BOM & PCB HISTORY

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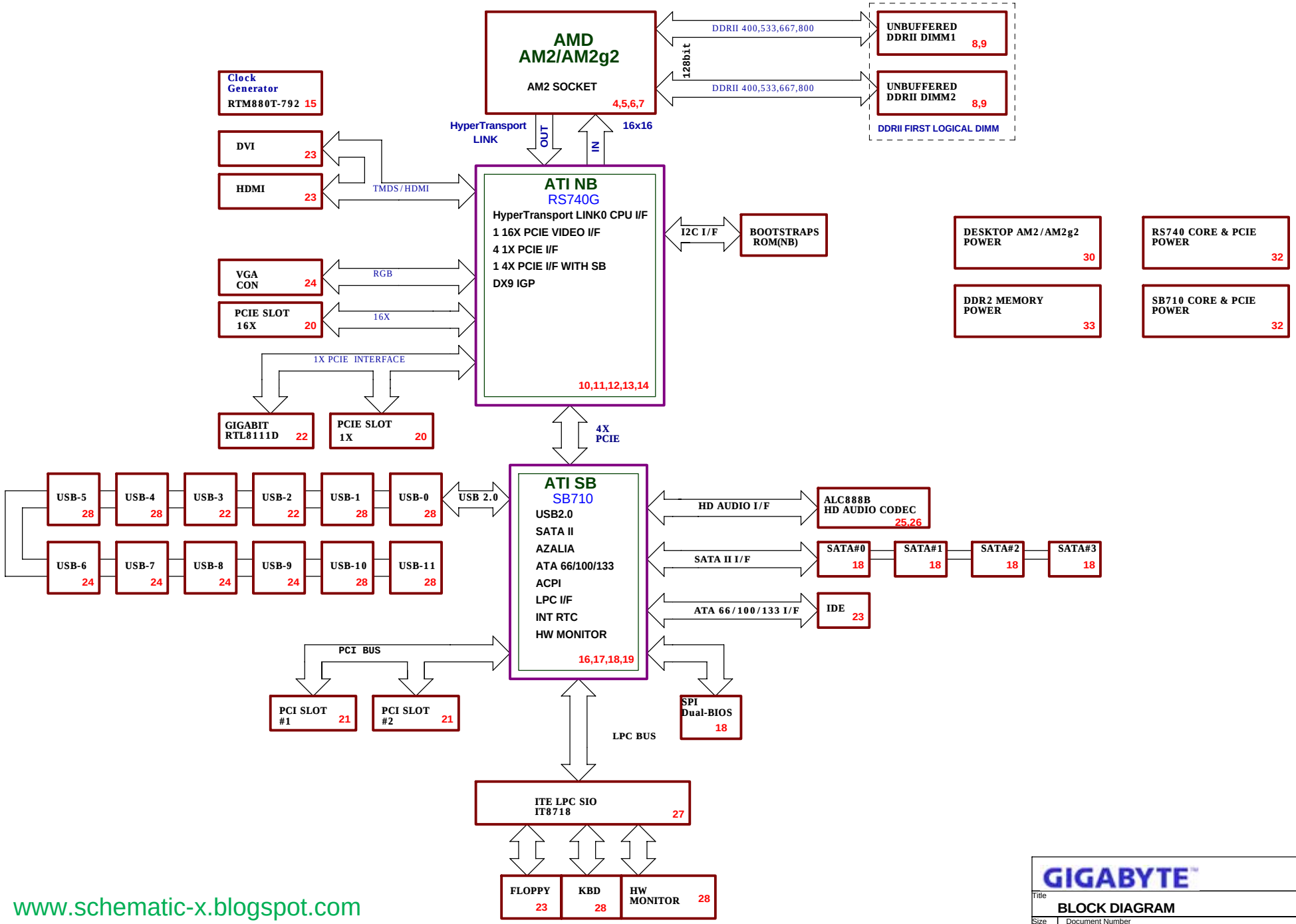
RS740 CUSTOMER DESKTOP REFERENCE DESIGN



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-MA74GM-S2H	4.11

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L0_CADIN_L[0..15] L0_CADIN_L[0..15] 10

L0_CADIN_H[0..15] L0_CADIN_H[0..15] 10

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 10

L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

VCC_SB
GND
R4 49.9/4/1 L0_CTLIN_H1
R6 49.9/4/1 L0_CTLIN_L1

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/940AM2/S/GF

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-01R]

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Title: CPU HYPER TRANSPORT

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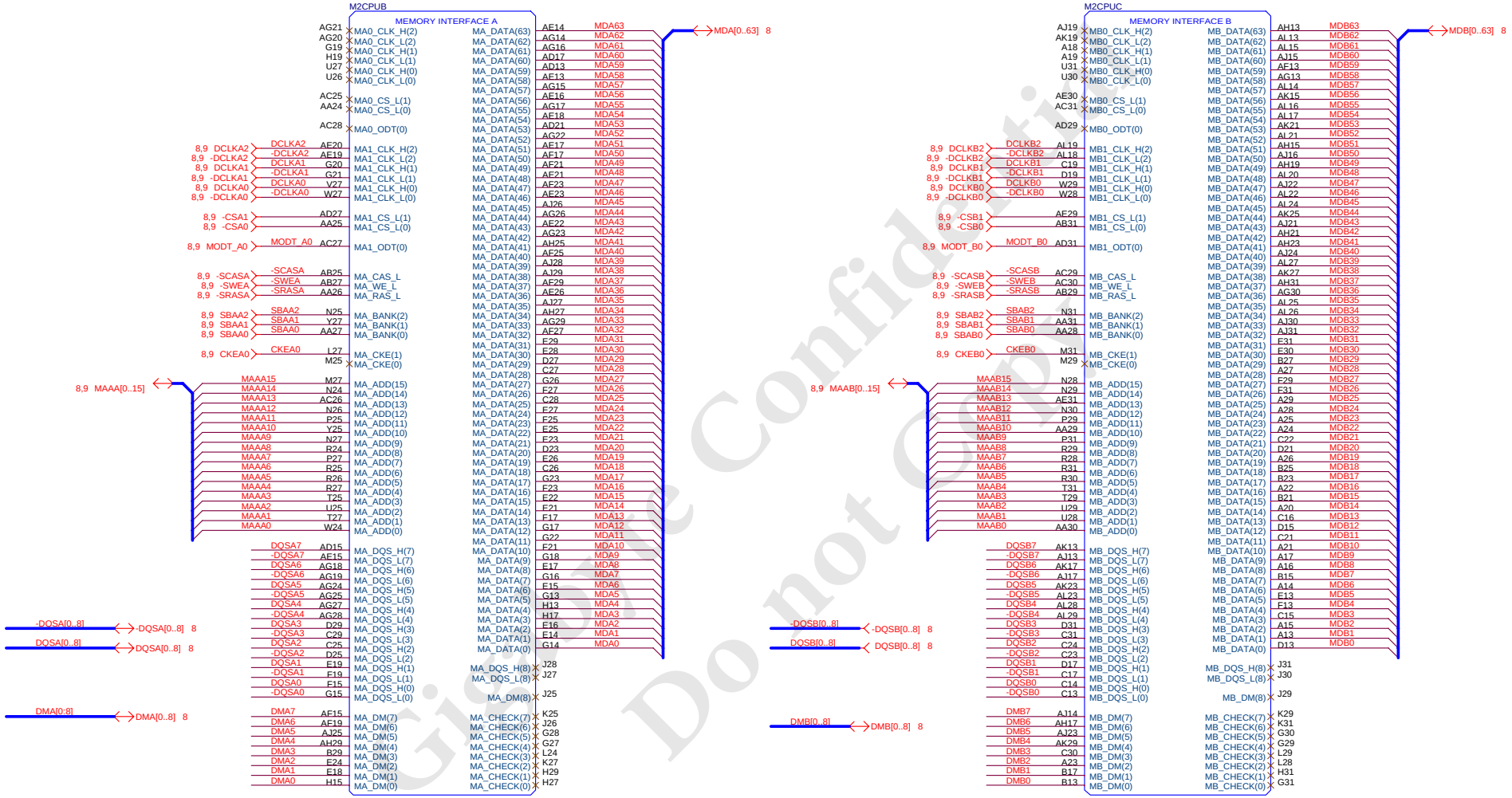

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Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-MA74GM-S2H	Rev: 4.11
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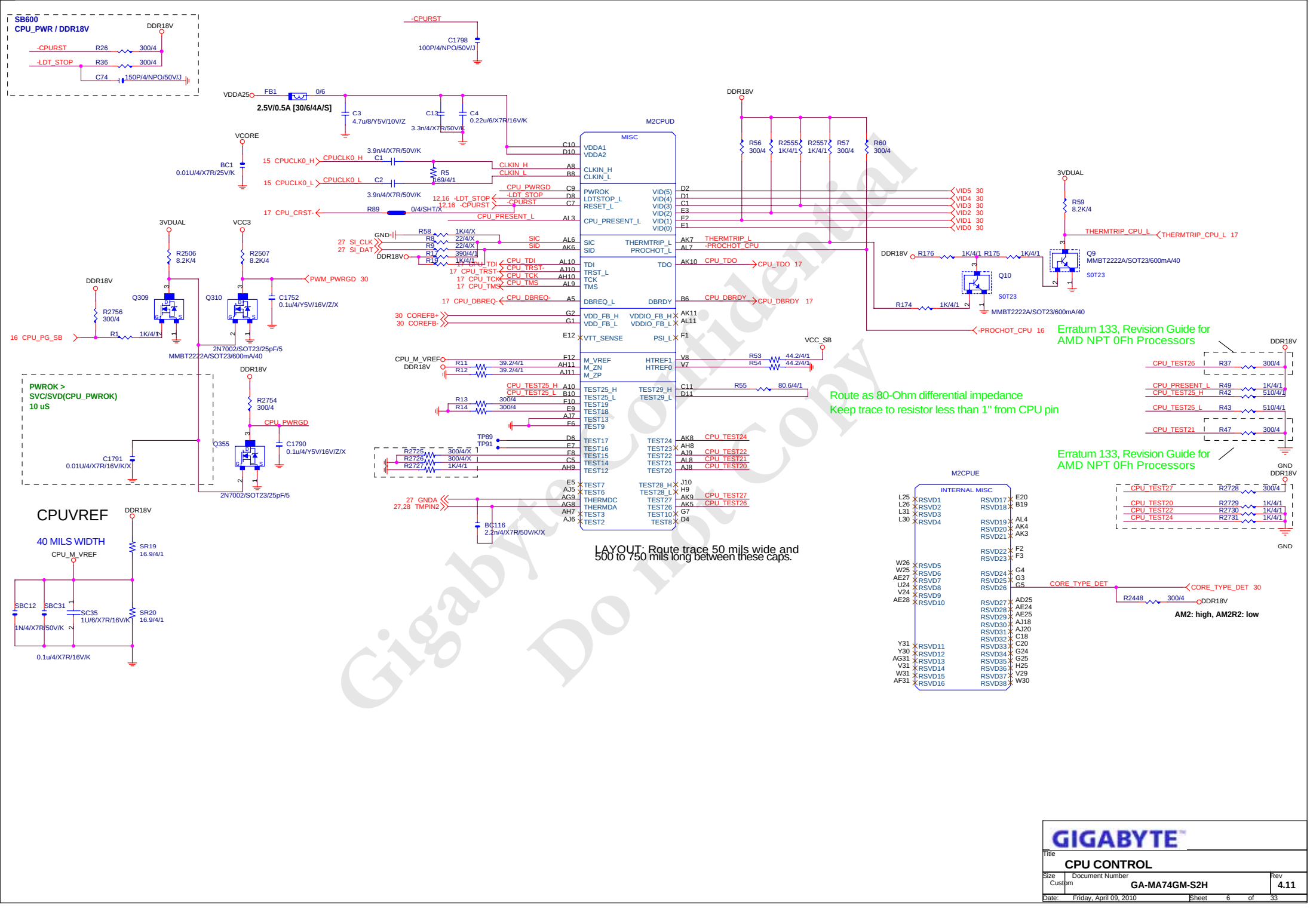
SB600
CPU_PWR / DDR18V
DDR18V
-CPURST
R26
300/4
-LDT_STOP
R36
300/4
C74
150P/4/NPO/50V/J
-CPURST
C1798
100P/4/NPO/50V/J
VDDA25
FB1
0/6
2.5V/0.5A [30/6/4A/S]
C3
4.7u/8/Y5V/10V/Z
C13
3.3n/4/X7R/50V/K
C4
0.22u/6/X7R/16V/K
VCORE
BC1
0.01U/4/X7R/25V/K
15 CPUCLK0_H
CPUCLK0_H
C1
3.9n/4/X7R/50V/K
15 CPUCLK0_L
CPUCLK0_L
C2
3.9n/4/X7R/50V/K
R5
169/4/1
CLKIN_H
CLKIN_L
CPU_PWRGD
12,16 -LDT_STOP
-LDT_STOP
12,16 -CPURST
-CPURST
17 CPU_CRST-
R89
0/4/SHT/X
CPU_PRESENT_L
M2CPUD
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
SIC
SID
THERMTRIP_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VTT_SENSE
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
DDR18V
R56
300/4
R2555
1K/4/1
R2557
1K/4/1
R57
300/4
R60
300/4
VID5 30
VID4 30
VID3 30
VID2 30
VID1 30
VID0 30
THERMTRIP_L
-PROCHOT_CPU
CPU_TDO
CPU_TDO 17
CPU_DBRDY
CPU_DBRDY 17
-PROCHOT_CPU 16
3VDUAL
R59
8.2K/4
THERMTRIP_CPU_L
THERMTRIP_CPU_L 17
DDR18V
R176
1K/4/1
R175
1K/4/1
Q10
SOT23
R174
1K/4/1
MMBT2222A/SOT23/600mA/40
Q9
MMBT2222A/SOT23/600mA/40
SOT23
3VDUAL
VCC3
R2506
8.2K/4
R2507
8.2K/4
PWM_PWRGD 30
DDR18V
R2756
300/4
Q309
Q310
C1752
0.1u/4/Y5V/16V/Z/X
16 CPU_PG_SB
R1
1K/4/1
2N7002/SOT23/25pF/5
MMBT2222A/SOT23/600mA/40
R58
1K/4/X
R8
22/4/X
R9
22/4/X
R1
390/4/1
R12
1K/4/1
27 SI_CLK
27 SI_DAT
SIC
SID
17 CPU_TDI
17 CPU_TRST-
17 CPU_TCK
17 CPU_TMS
CPU_TDI
CPU_TRST-
CPU_TCK
CPU_TMS
17 CPU_DBREQ-
CPU_DBREQ-
30 COREFB+
30 COREFB-
COREFB+
COREFB-
CPU_M_VREF
DDR18V
R11
39.2/4/1
R12
39.2/4/1
VCC_SB
R53
44.2/4/1
R54
44.2/4/1
CPU_TEST25_H
CPU_TEST25_L
R13
300/4
R14
300/4
R55
80.6/4/1
TP89
TP91
R2725
300/4/X
R2726
300/4/X
R2727
1K/4/1
CPU_TEST24
CPU_TEST22
CPU_TEST21
CPU_TEST20
CPU_TEST27
CPU_TEST26
27 GNDA
27,28 TMPIN2
BC116
2.2n/4/X7R/50V/K/X
PWROK >
SVC/SVD(CPU_PWROK)
10 uS
R2754
300/4
CPU_PWRGD
Q355
C1790
0.1u/4/Y5V/16V/Z/X
C1791
0.01U/4/X7R/16V/K/X
2N7002/SOT23/25pF/5
CPUVREF
40 MILS WIDTH
CPU_M_VREF
DDR18V
SR19
16.9/4/1
SR20
16.9/4/1
SBC12
SBC31
SC35
1U/6/X7R/16V/K
1N/4/X7R/50V/K
0.1u/4/X7R/16V/K
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
CPU_TEST26
R37
300/4
CPU_PRESENT_L
R49
1K/4/1
CPU_TEST25_H
R42
510/4/1
CPU_TEST25_L
R43
510/4/1
CPU_TEST21
R47
300/4
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
GND
DDR18V
CPU_TEST27
R2728
300/4
CPU_TEST20
R2729
1K/4/1
CPU_TEST22
R2730
1K/4/1
CPU_TEST24
R2731
1K/4/1
GND
M2CPUE
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
CORE_TYPE_DET
CORE_TYPE_DET 30
R2448
300/4
DDR18V
AM2: high, AM2R2: low
Gigabyte Confidential
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GIGABYTE
Title
CPU CONTROL
Size
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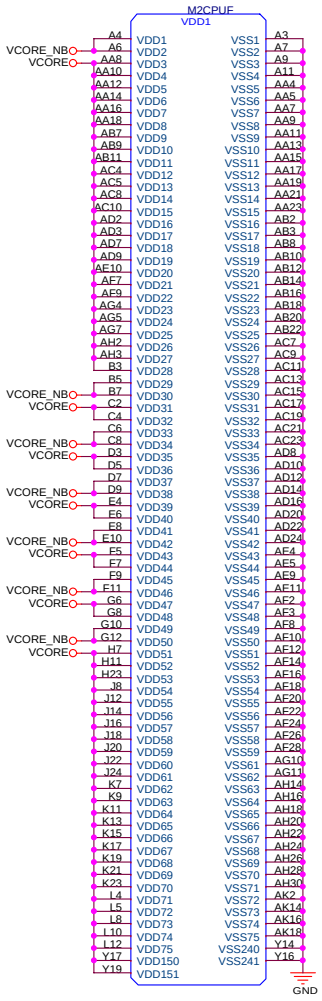
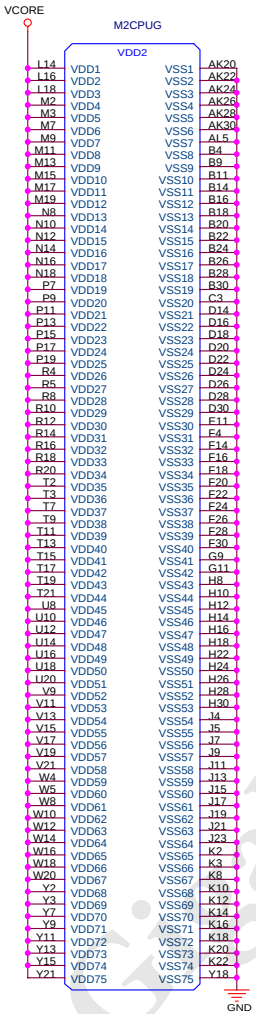
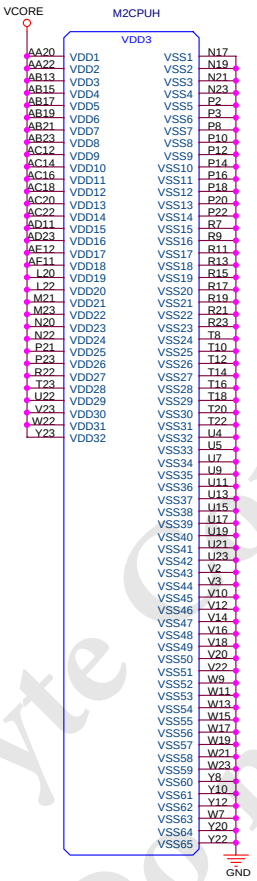
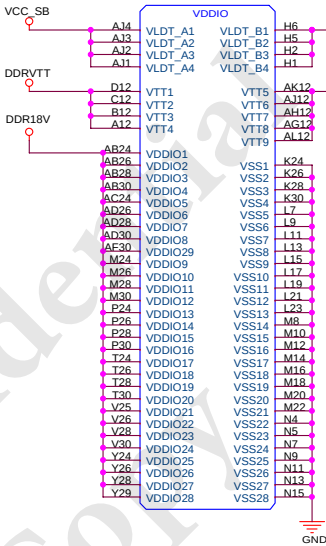
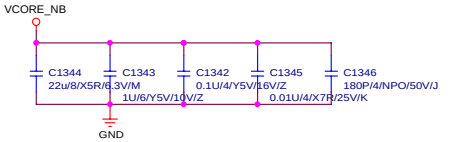
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

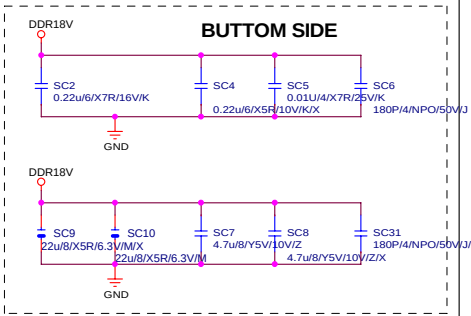


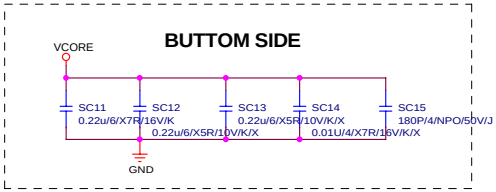


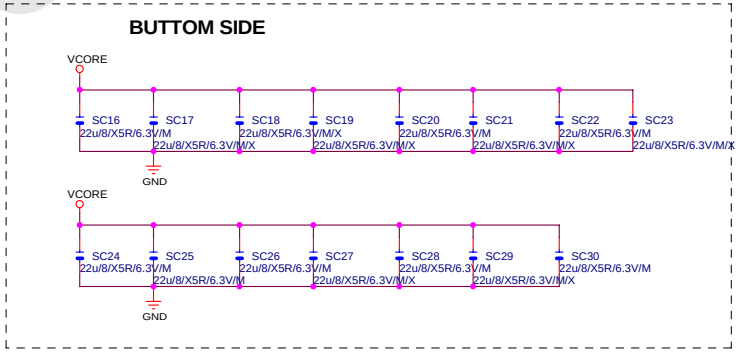


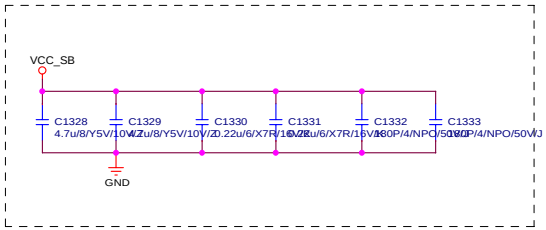


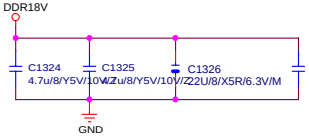


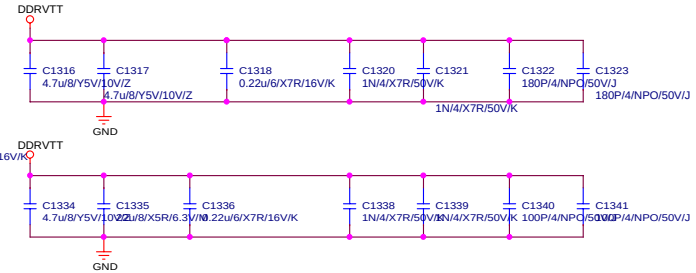


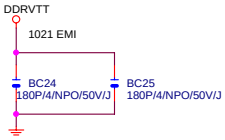












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Title	CPU POWER & GND	
Size: Custom	Document Number: GA-MA74GM-S2H	Rev: 4.11
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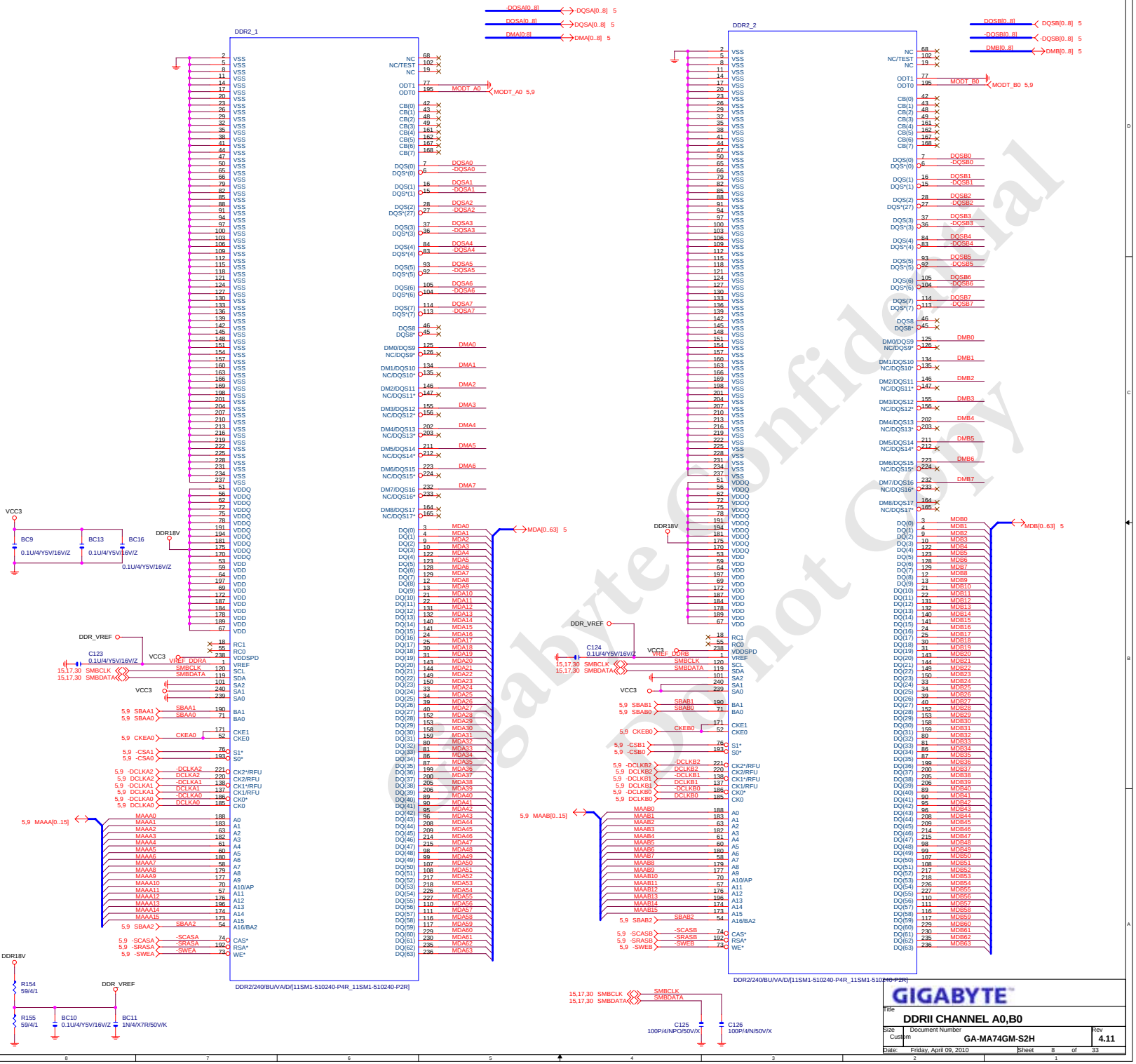
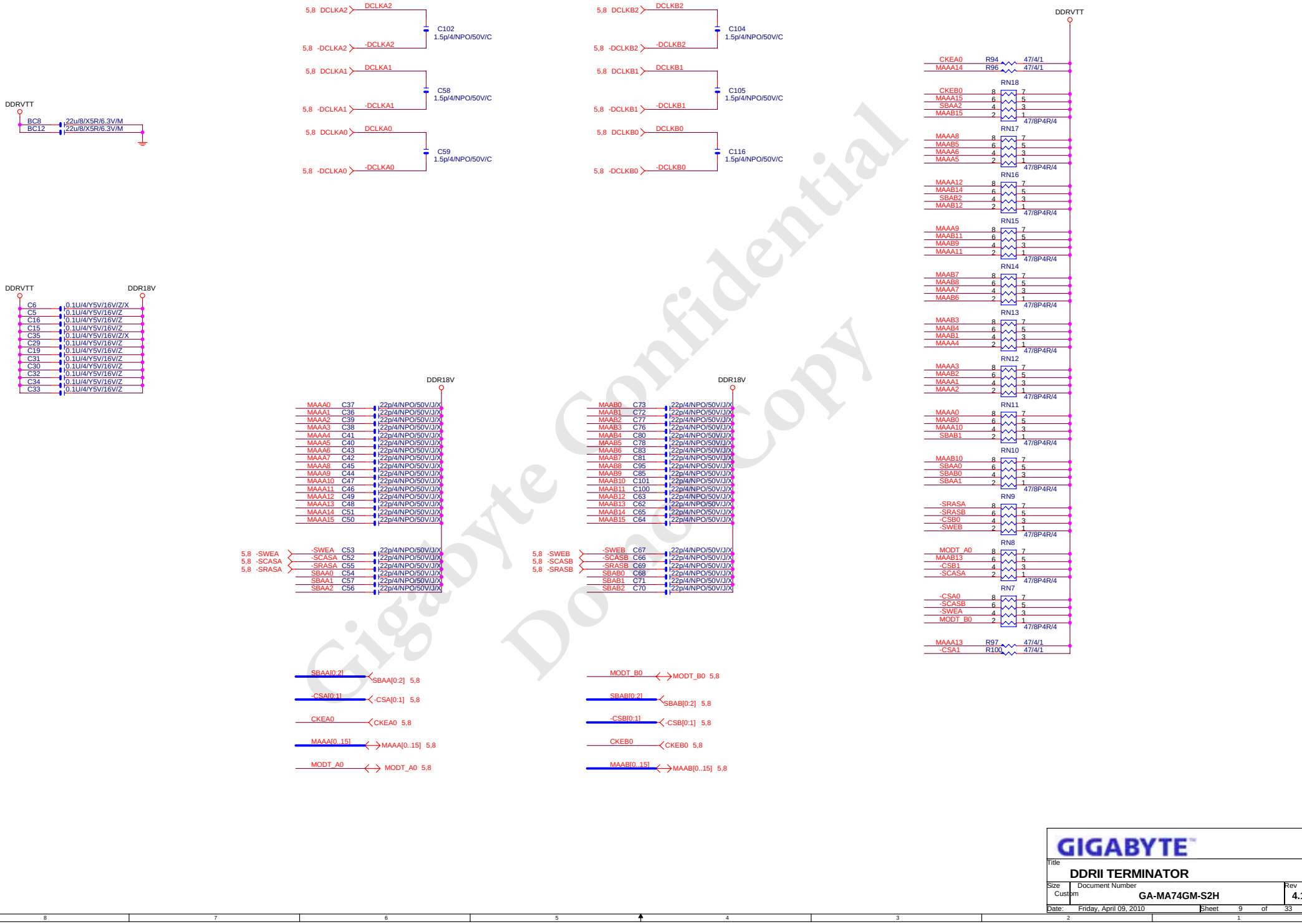
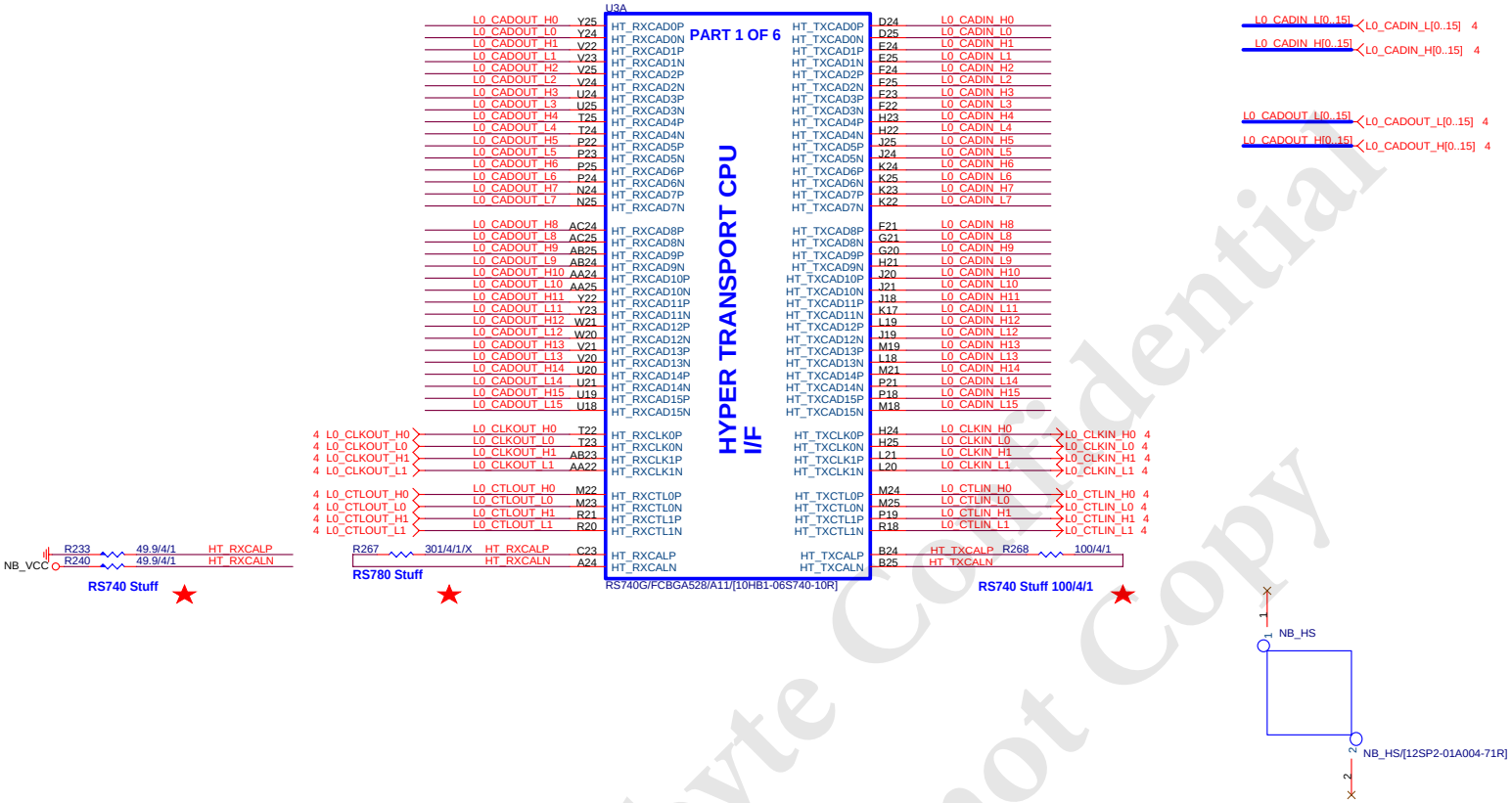




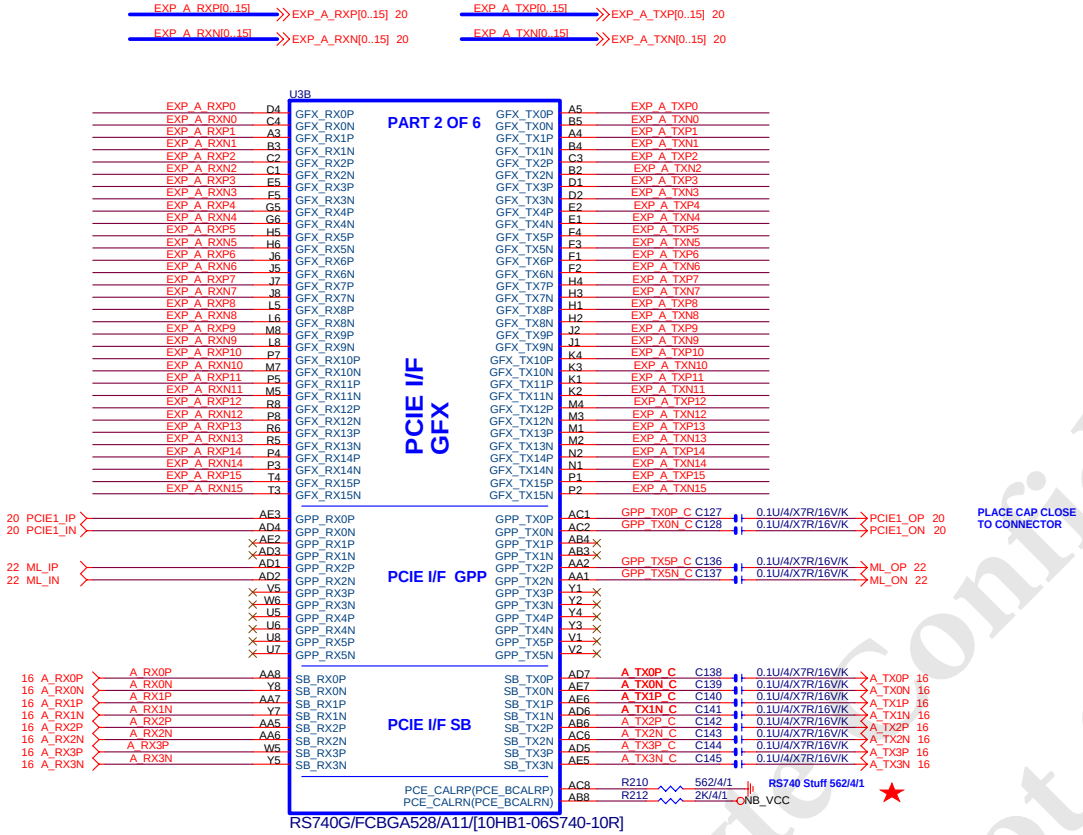


GIGABYTE

Title: RS740 HT-LINK I/F

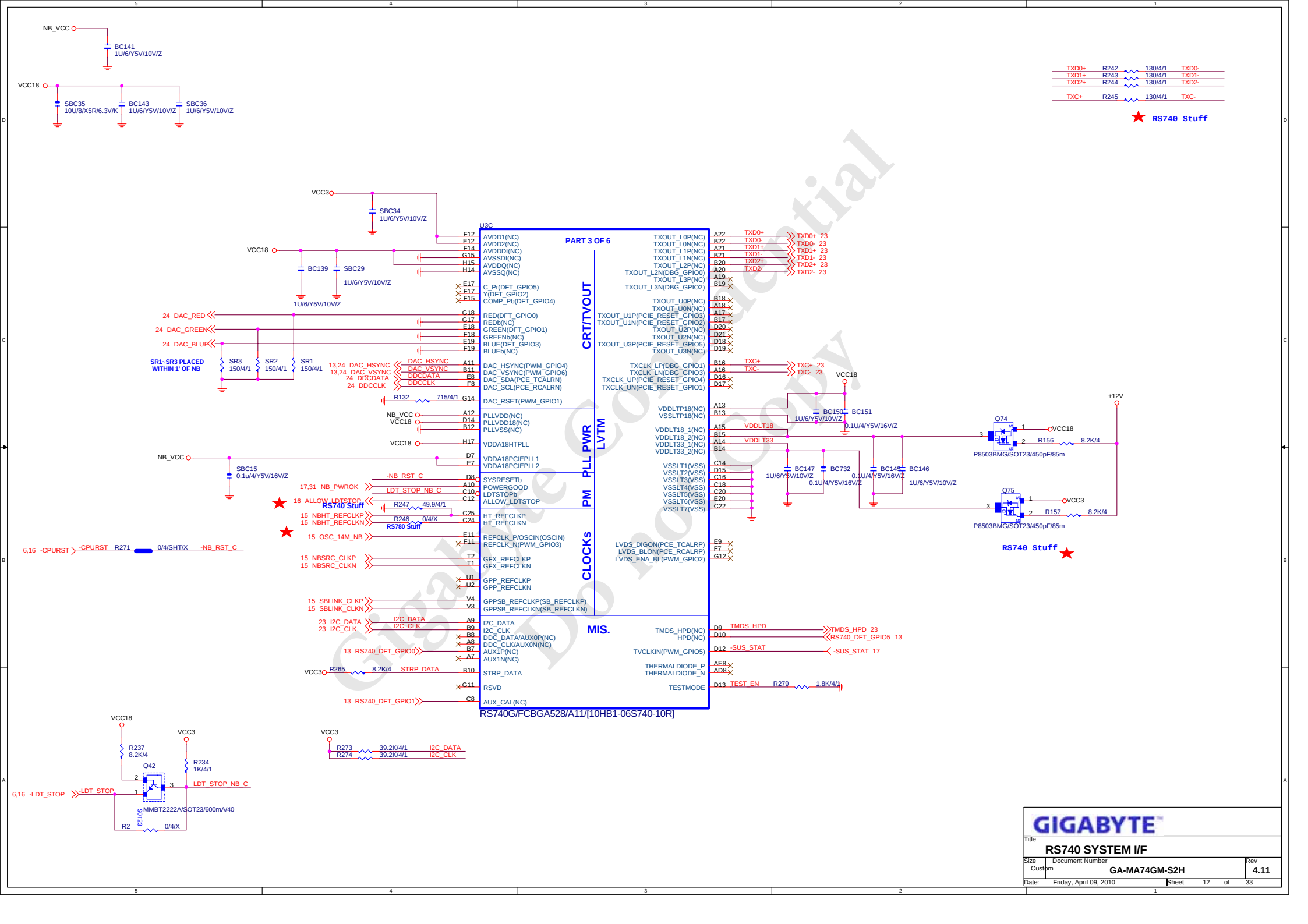
Size	Document Number	Rev
Custom	GA-MA74GM-S2H	4.11

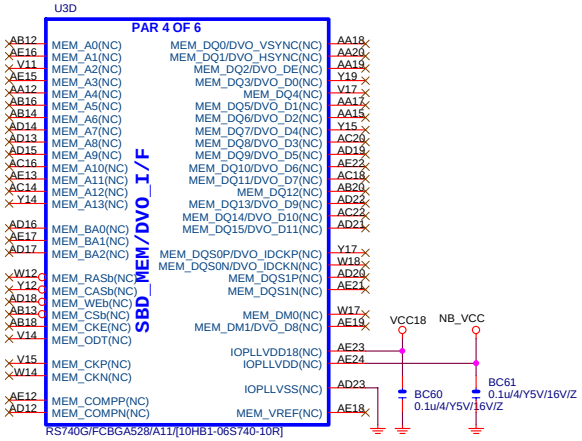
Date: Friday, April 09, 2010 Sheet 10 of 33



GIGABYTE

Title	RS740 PCIE I/F		
Size: Custom	Document Number: GA-MA74GM-S2H		Rev: 4.11
Date: Friday, April 09, 2010	Sheet 11 of 33		

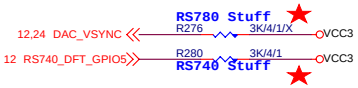

NB_VCC
BC141
1U/6/Y5V/10V/Z
VCC18
SBC35
10U/8/X5R/6.3V/K
BC143
1U/6/Y5V/10V/Z
SBC36
1U/6/Y5V/10V/Z
TXD0+ R242 130/4/1 TXD0-
TXD1+ R243 130/4/1 TXD1-
TXD2+ R244 130/4/1 TXD2-
TXC+ R245 130/4/1 TXC-
RS740 Stuff
VCC3
SBC34
1U/6/Y5V/10V/Z
U3C
PART 3 OF 6
AVDD1(NC)
AVDD2(NC)
AVDDDI(NC)
AVSSDI(NC)
AVDDQ(NC)
AVSSQ(NC)
BC139
SBC29
1U/6/Y5V/10V/Z
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)
24 DAC_RED
24 DAC_GREEN
24 DAC_BLUE
SR1~SR3 PLACED WITHIN 1' OF NB
SR3 150/4/1
SR2 150/4/1
SR1 150/4/1
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
13,24 DAC_HSYNC
13,24 DAC_VSYNC
24 DDCDATA
24 DDCCLK
DAC_HSYNC
DAC_VSYNC
DDCDATA
DDCCLK
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SDA(PCE_TCALRN)
DAC_SCL(PCE_RCALRN)
R132 715/4/1
DAC_RSET(PWM_GPIO1)
CRT/TVOUT
NB_VCC
VCC18
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
VCC18
VDDA18HTPLL
NB_VCC
SBC15
0.1u/4/Y5V/16V/Z
VDDA18PCIEPLL1
VDDA18PCIEPLL2
17,31 NB_PWROK
-NB_RST_C
SYSRESETb
POWERGOOD
LDTSTOPb
16 ALLOW_LDTSTOP
LDT_STOP_NB_C
ALLOW_LDTSTOP
RS740 Stuff
R247 49.9/4/1
15 NBHT_REFCLKP
15 NBHT_REFCLKN
R246 0/4/X
RS780 Stuff
HT_REFCLKP
HT_REFCLKN
PM_PLL_PWR_LVTM
15 OSC_14M_NB
REFCLK_P/OSCIN(OSCIN)
REFCLK_N(PWM_GPIO3)
6,16 -CPURST
-CPURST R271 0/4/SHT/X -NB_RST_C
15 NBSRC_CLKP
15 NBSRC_CLKN
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
CLOCKs
15 SBLINK_CLKP
15 SBLINK_CLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
23 I2C_DATA
23 I2C_CLK
I2C_DATA
I2C_CLK
DDC_DATA/AUX0P(NC)
DDC_CLK/AUX0N(NC)
13 RS740_DFT_GPIO0
AUX1P(NC)
AUX1N(NC)
VCC3 R265 8.2K/4 STRP_DATA
STRP_DATA
RSVD
13 RS740_DFT_GPIO1
AUX_CAL(NC)
MIS.
RS740G/FCBGA528/A11/[10HB1-06S740-10R]
TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
VDDLTP18(NC)
VSSLTP18(NC)
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)
LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
TMDS_HPD(NC)
HPD(NC)
TVCLKIN(PWM_GPIO5)
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
TXD0+ 23
TXD0- 23
TXD1+ 23
TXD1- 23
TXD2+ 23
TXD2- 23
TXC+ 23
TXC- 23
TMDS_HPD 23
RS740_DFT_GPIO5 13
-SUS_STAT 17
D13 TEST_EN R279 1.8K/4/1
VDDLT18
VDDLT33
BC150 BC151
1U/6/Y5V/10V/Z
0.1U/4/Y5V/16V/Z
BC147 BC732 BC145 BC146
1U/6/Y5V/10V/Z
0.1U/4/Y5V/16V/Z
+12V
Q74
P8503BMG/SOT23/450pF/85m
VCC18
R156 8.2K/4
Q75
VCC3
R157 8.2K/4
RS740 Stuff
VCC18
R237 8.2K/4
VCC3
R234 1K/4/1
Q42
6,16 -LDT_STOP
LDT_STOP
LDT_STOP_NB_C
MMBT2222A/SOT23/600mA/40
SOT23
R2 0/4/X
VCC3
R273 39.2K/4/1 I2C_DATA
R274 39.2K/4/1 I2C_CLK
GIGABYTE
Title
RS740 SYSTEM I/F
Size Custom
Document Number GA-MA74GM-S2H
Rev 4.11
Date: Friday, April 09, 2010
Sheet 12 of 33
Gigabyte Confidential
Do not Copy



RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly



Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
            setting only
RS740: Not supported
```


GIGABYTE

Title: **RS740 STRAP**

Size	Document Number	Rev
Custom	GA-MA74GM-S2H	4.11

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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND

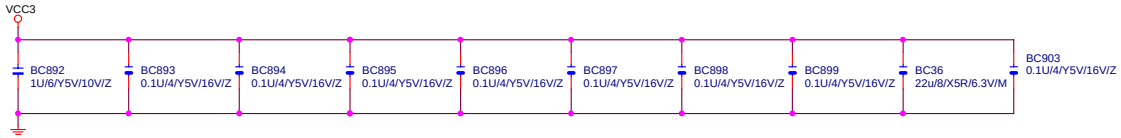
RS740G/FCBGA528/A11/[10HB1-06S740-10R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS740G/FCBGA528/A11/[10HB1-06S740-10R]

Title	RS740 POWER & GND			
Size	Custom	Document Number	GA-MA74GM-S2H	Rev 4.11
Date:	Friday, April 09, 2010	Sheet	14 of	33

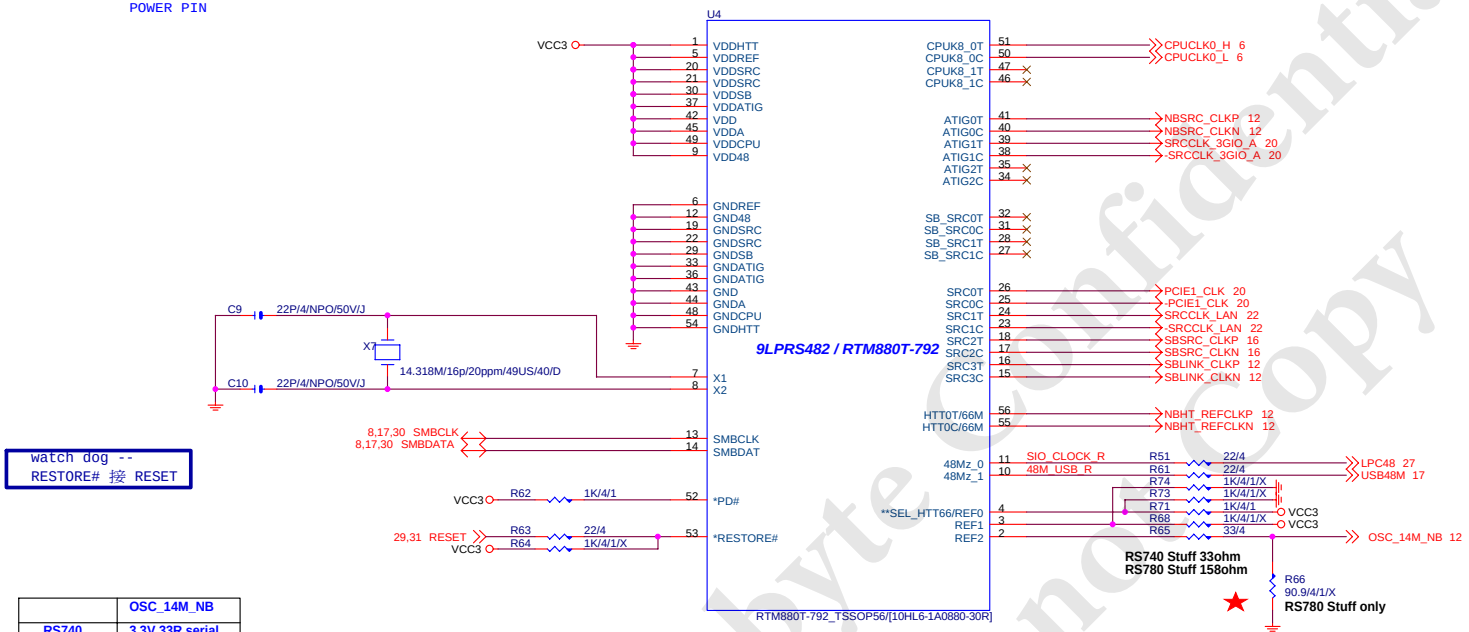


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog -- RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE

Title: RTM880T-792

Size: Custom | Document Number: GA-MA74GM-S2H | Rev: 4.11

Date: Friday, April 09, 2010 | Sheet 15 of 33

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

X4 32.768K/12.5p/20ppm/TF38/35K/D

SHW/D0.64*5.08*6.74

EMI 20071107

BIOS after boot setting
EC AOD-ACC

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

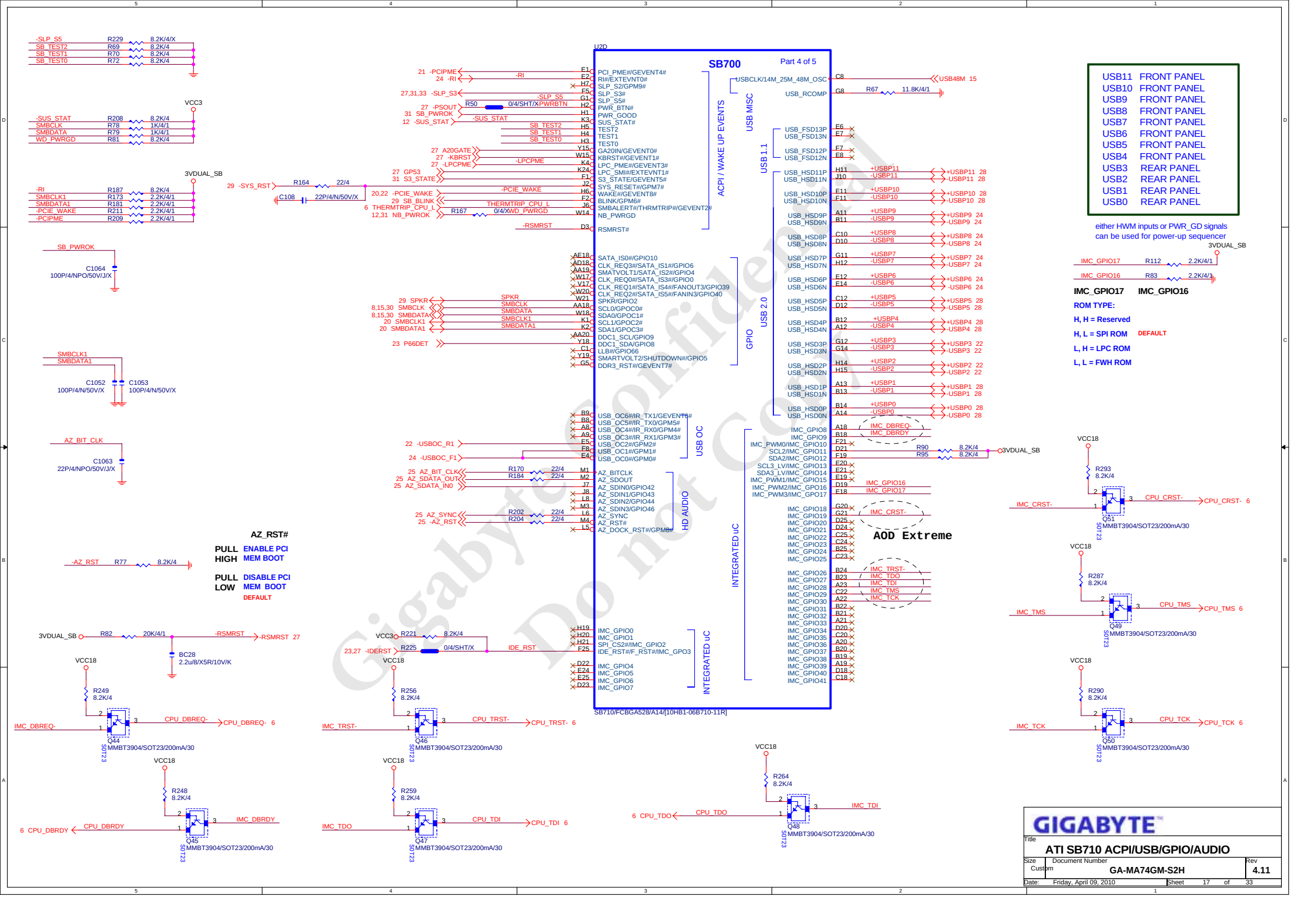
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title: ATI SB710 PCIE/PCI/CPU/LPC

Size: Custom | Document Number: GA-MA74GM-S2H | Rev: 4.11

Date: Friday, April 09, 2010 | Sheet 16 of 33


SB700
Part 4 of 5
U2D
SB710/FCBGA528/A14/[10HB1-06B710-11R]
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#/
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMATVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
AOD Extreme
IMC_DBREQ-
IMC_DBRDY
IMC_CRST-
IMC_TRST-
IMC_TDO
IMC_TDI
IMC_TMS
IMC_TCK
-SLP_S5
SB_TEST2
SB_TEST1
SB_TEST0
-SUS_STAT
SMBCLK
SMBDATA
WD_PWRGD
-RI
SMBCLK1
SMBDATA1
-PCIE_WAKE
-PCIPME
SB_PWROK
AZ_BIT_CLK
-AZ_RST
-RSMRST
-LPCPME
-PCIE_WAKE
THERMTRIP_CPU_L
SPKR
SMBCLK
SMBDATA
SMBCLK1
SMBDATA1
-USBOC_R1
-USBOC_F1
AZ_BIT_CLK
AZ_SDATA_OUT
AZ_SDATA_IN0
AZ_SYNC
AZ_RST
-IDERST
IDE_RST
-RSMRST
-PSOUT
-KBRST
GP53
S3_STATE
-SLP_S3
-SUS_STAT
A20GATE
-PCIPME
-RI
SB_PWROK
NB_PWROK
-SYS_RST
-PCIE_WAKE
SB_BLINK
THERMTRIP_CPU_L
NB_PWROK
P66DET
USB48M
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals
can be used for power-up sequencer
IMC_GPIO17
IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT DEFAULT
CPU_DBREQ-
CPU_TRST-
CPU_TDI
CPU_TDO
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_CRST-
Q44 MMBT3904/SOT23/200mA/30
Q45 MMBT3904/SOT23/200mA/30
Q46 MMBT3904/SOT23/200mA/30
Q47 MMBT3904/SOT23/200mA/30
Q48 MMBT3904/SOT23/200mA/30
Q49 MMBT3904/SOT23/200mA/30
Q50 MMBT3904/SOT23/200mA/30
Q51 MMBT3904/SOT23/200mA/30
GIGABYTE
ATI SB710 ACPI/USB/GPIO/AUDIO
GA-MA74GM-S2H
4.11
Friday, April 09, 2010
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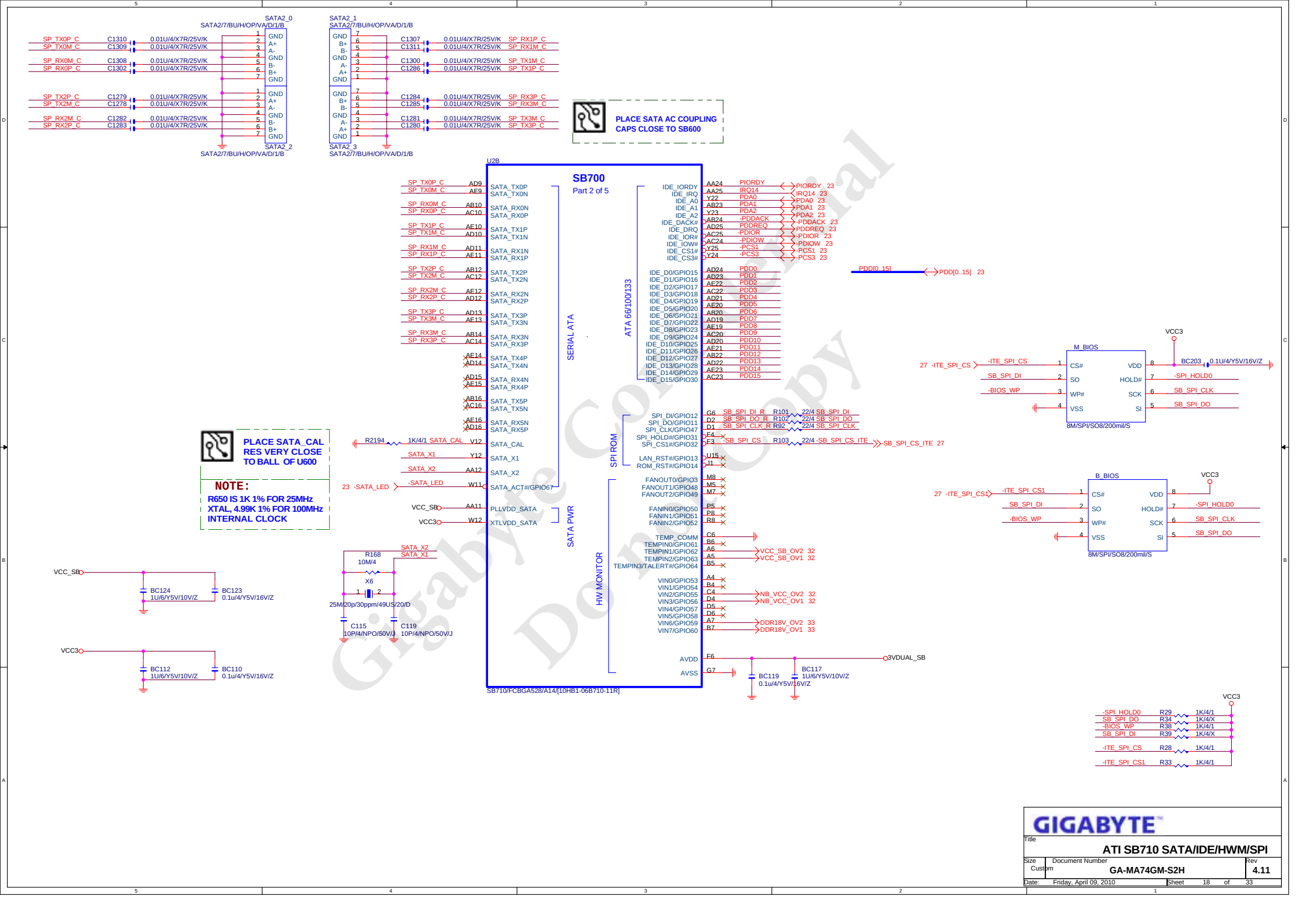
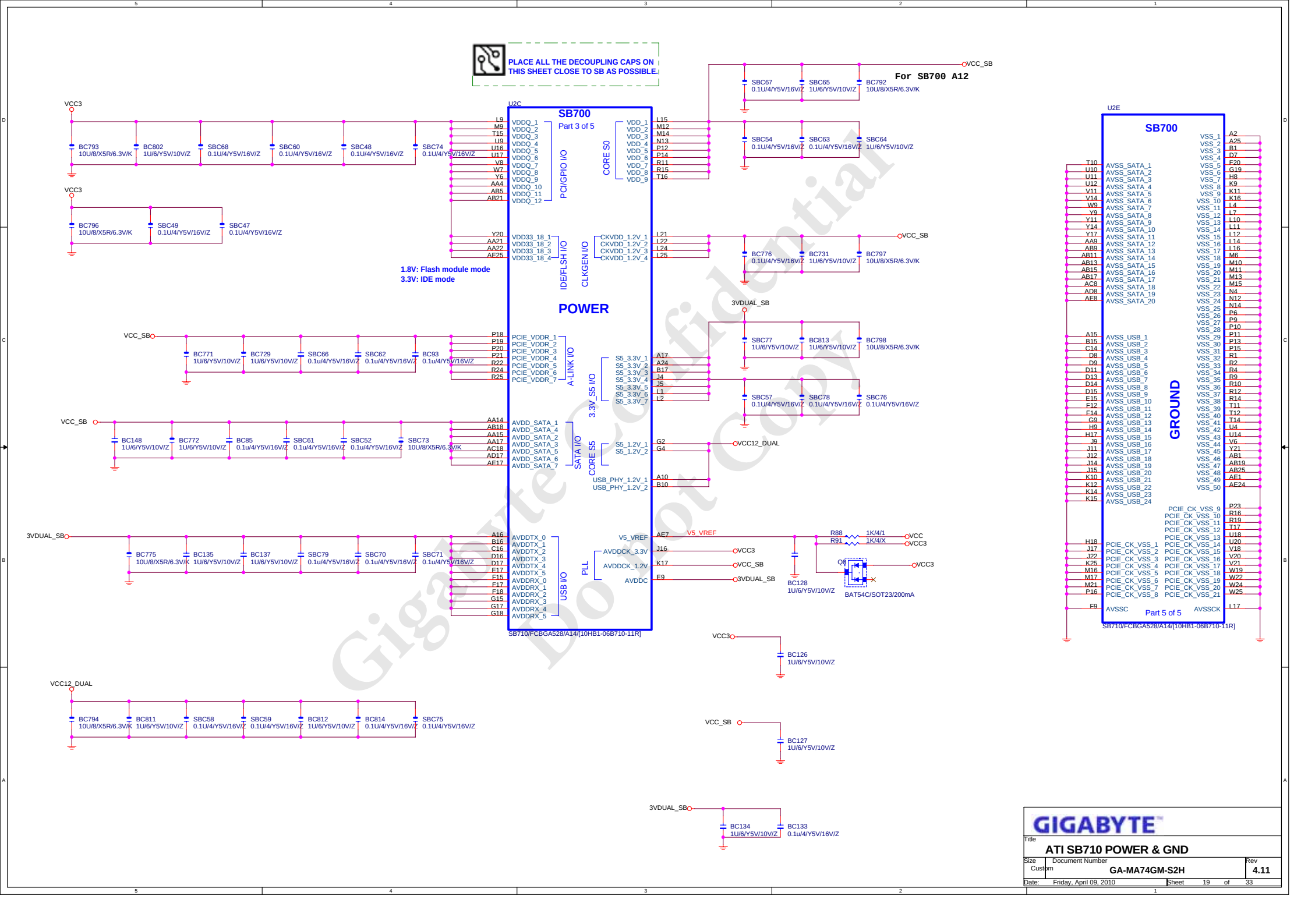
Gigabyte Confidential
Do not Copy



Title	ATI SB710 SATA/IDE/HWM/SPI
Size	Custom
Document Number	GA-MA74GM-S2H
Rev	4.11
Date:	Friday, April 09, 2010
Sheet	18 of 33


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
For SB700 A12
SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
1.8V: Flash module mode
3.3V: IDE mode
SB710/FCBGA528/A14/[10HB1-06B710-11R]
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GIGABYTE
ATI SB710 POWER & GND
GA-MA74GM-S2H
4.11
Friday, April 09, 2010
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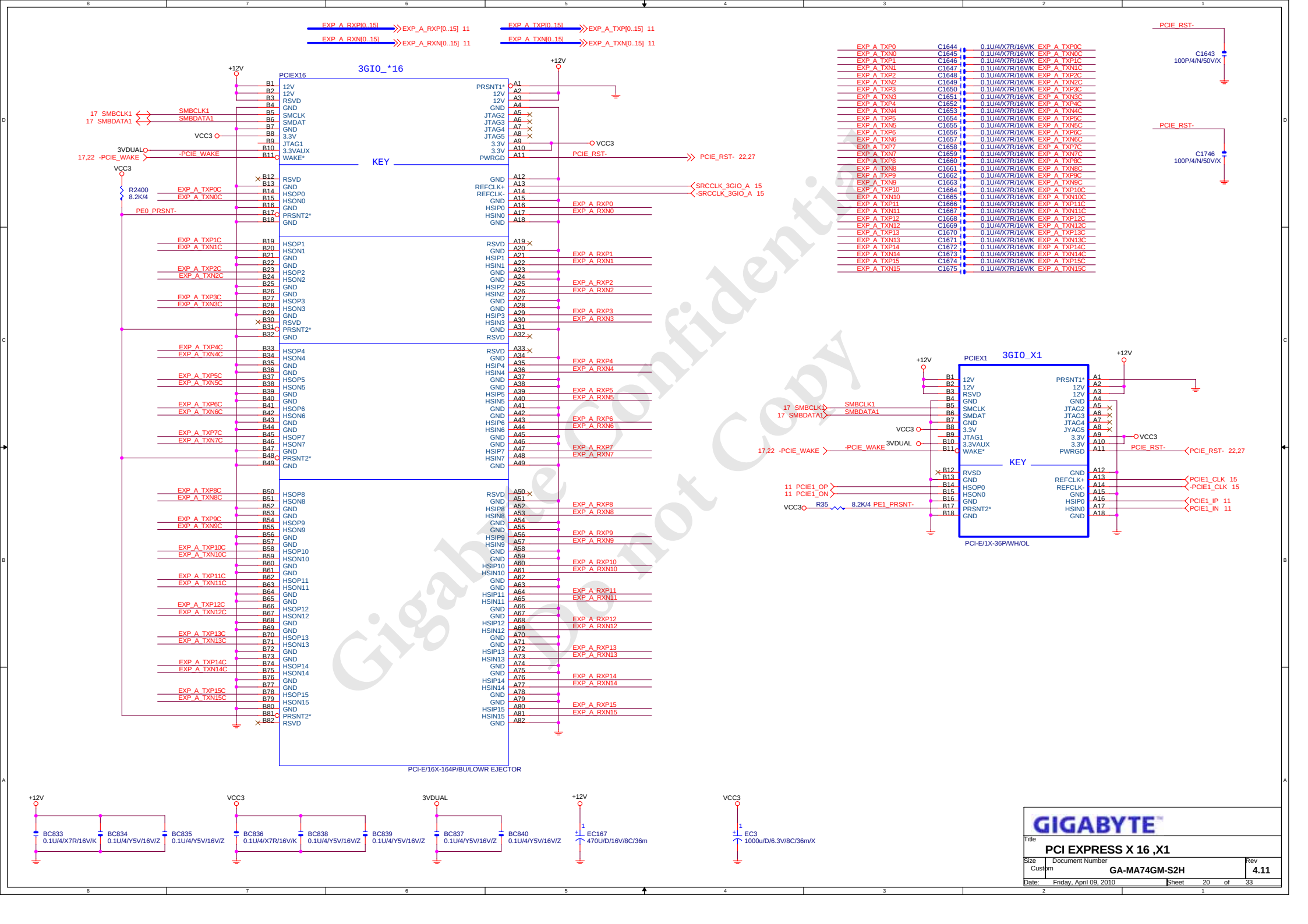

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Title	PCI EXPRESS X 16 ,X1	
Size: Custom	Document Number: GA-MA74GM-S2H	Rev: 4.11
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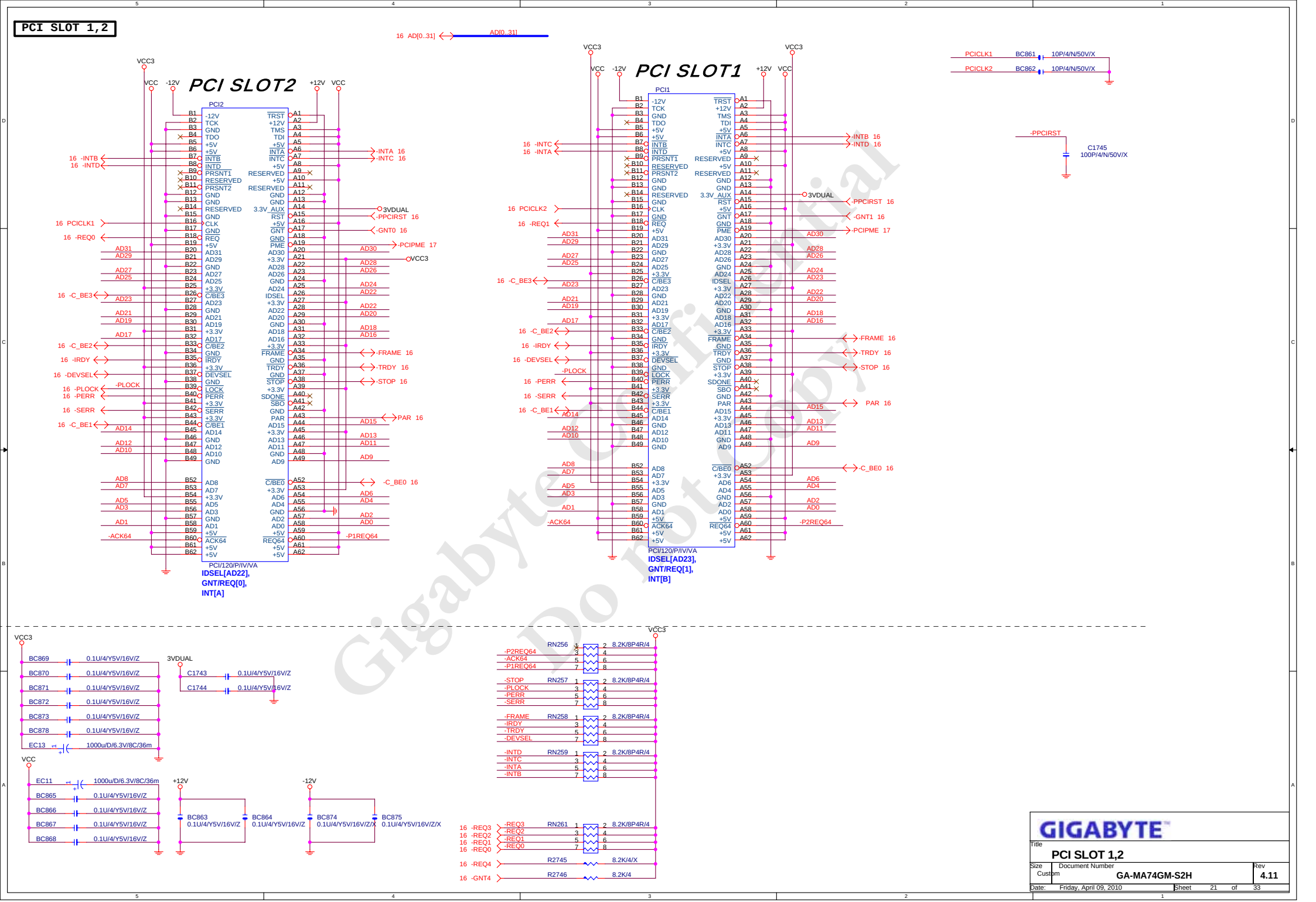
PCI SLOT 1,2



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Title: PCI SLOT 1,2		
Size: Custom	Document Number: GA-MA74GM-S2H	Rev: 4.11
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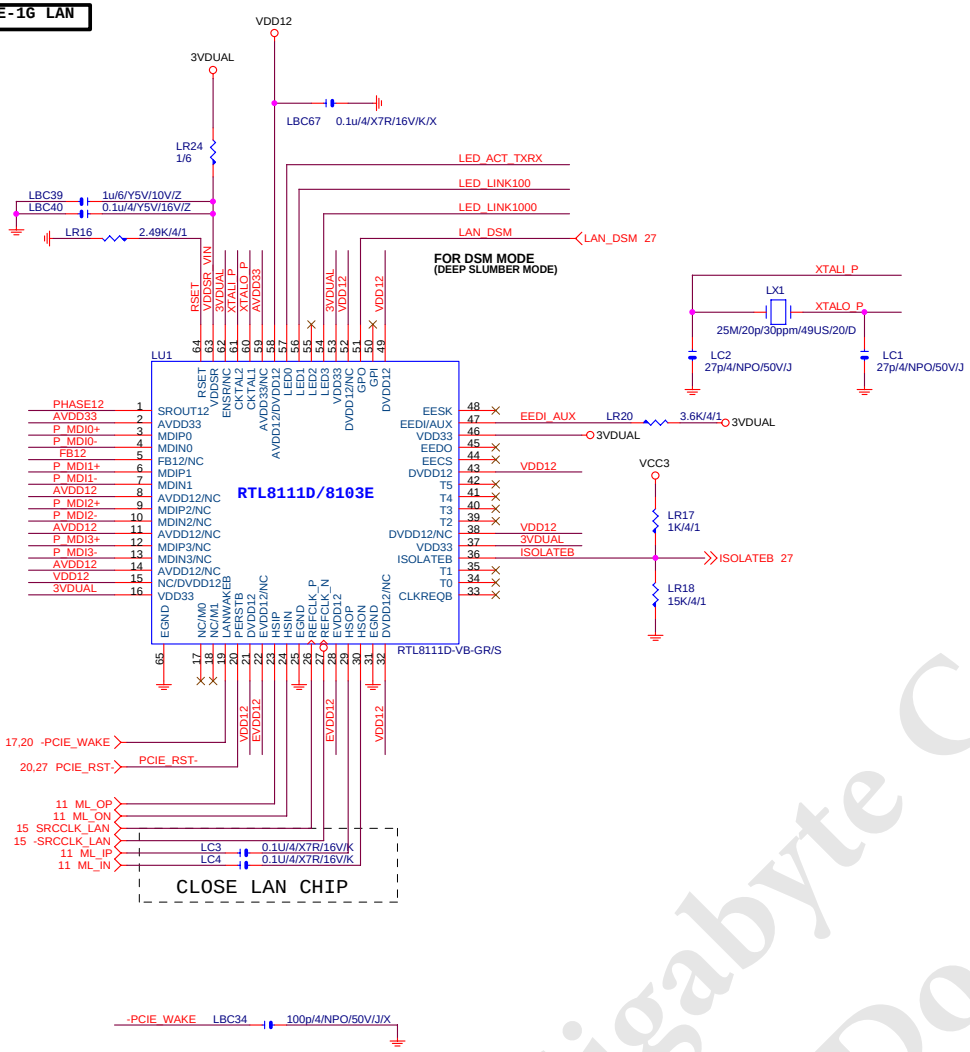
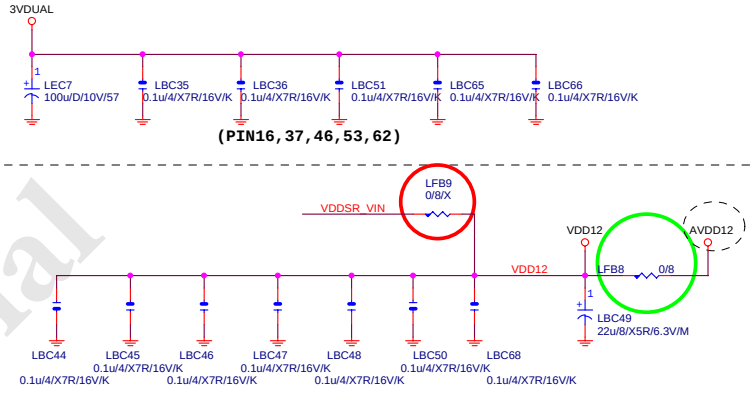
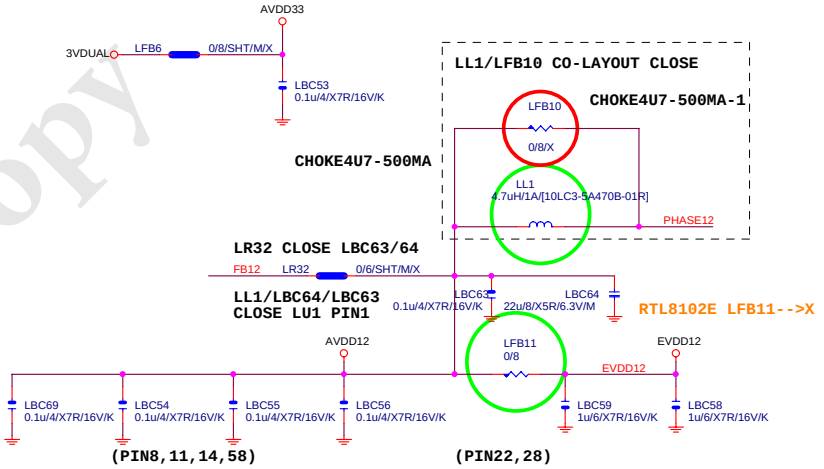
PCIE-1G LAN

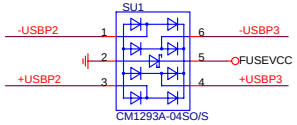


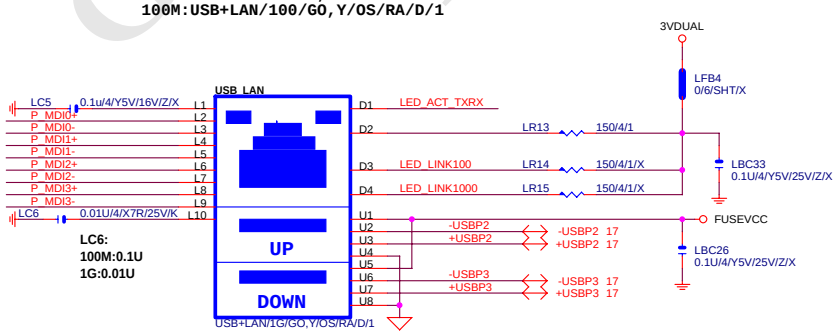




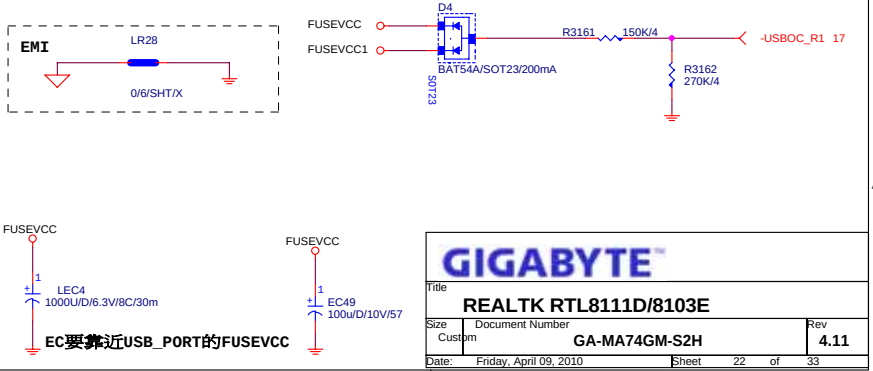
USB_LAN CONNECTOR

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1





USB_LAN



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Title	REALTK RTL8111D/8103E	
Size: Custom	Document Number: GA-MA74GM-S2H	Rev: 4.11
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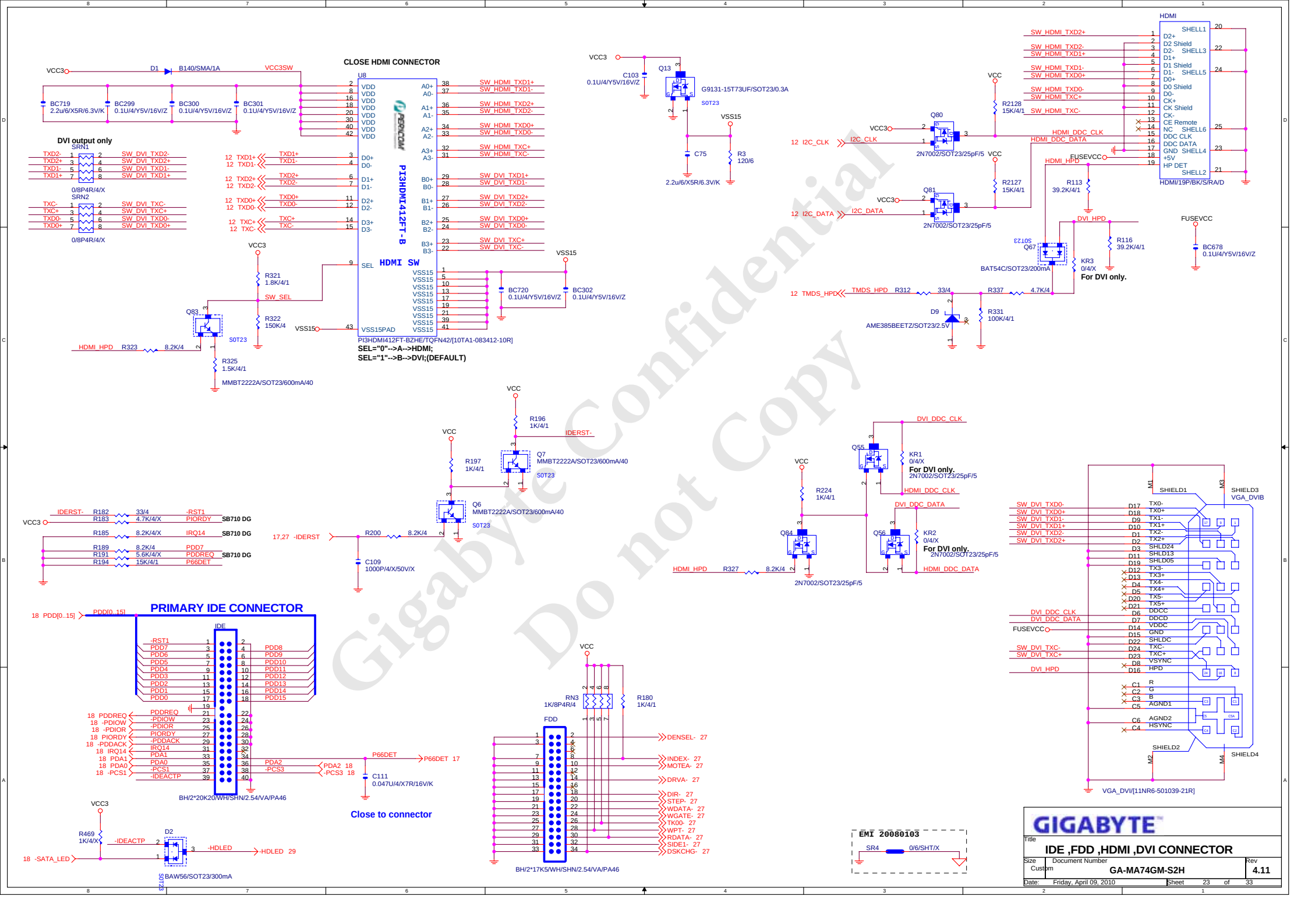
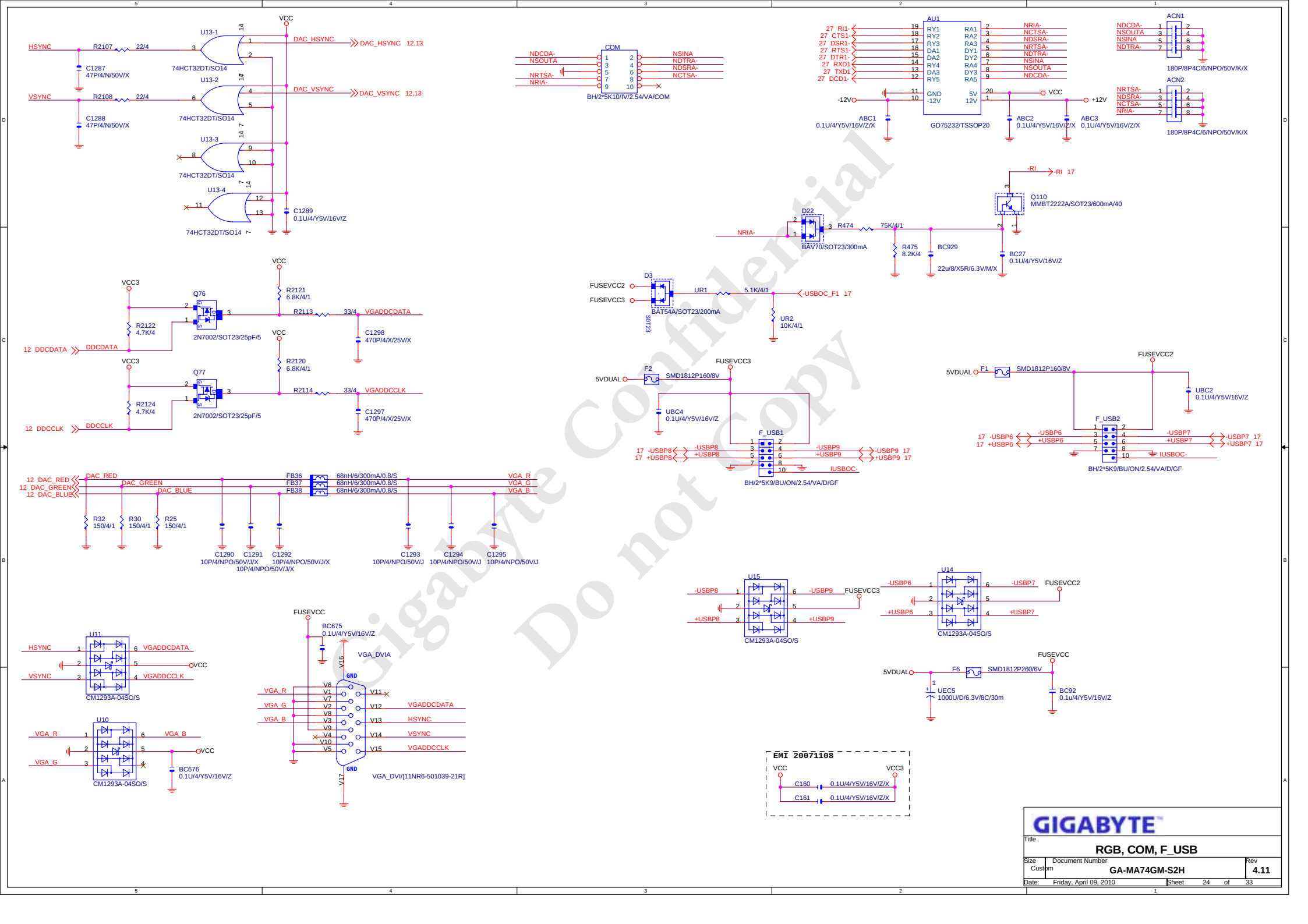
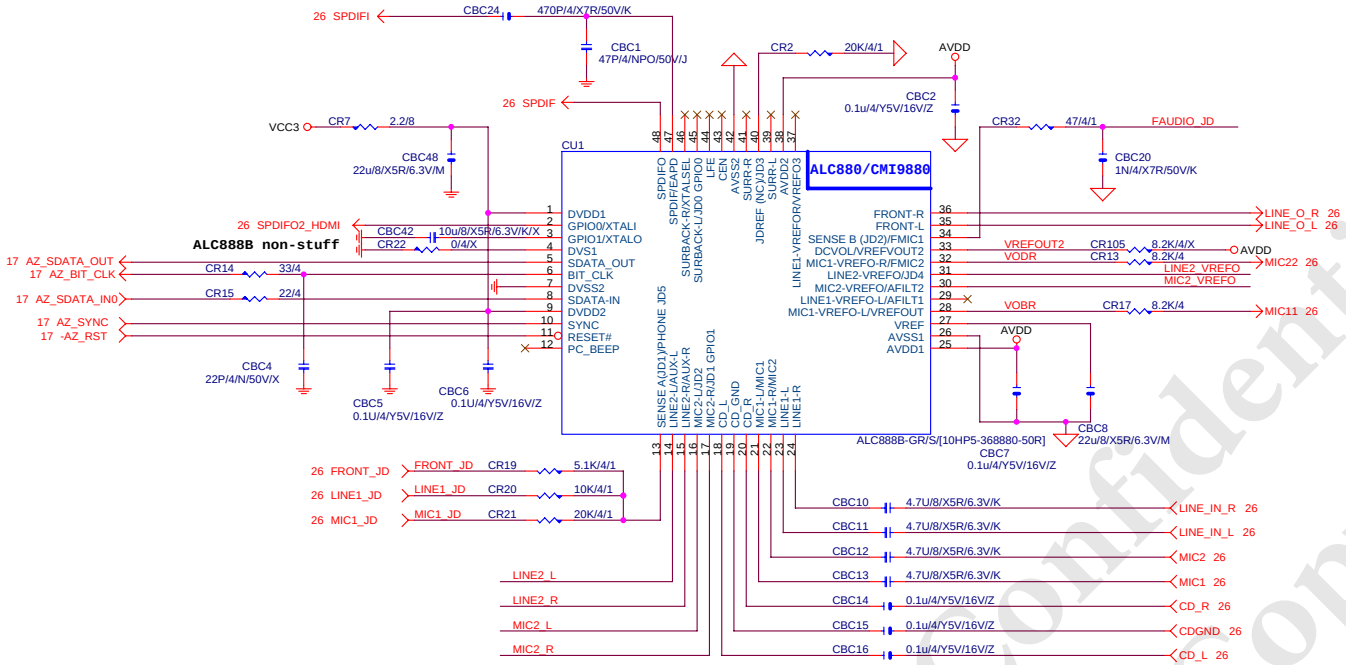
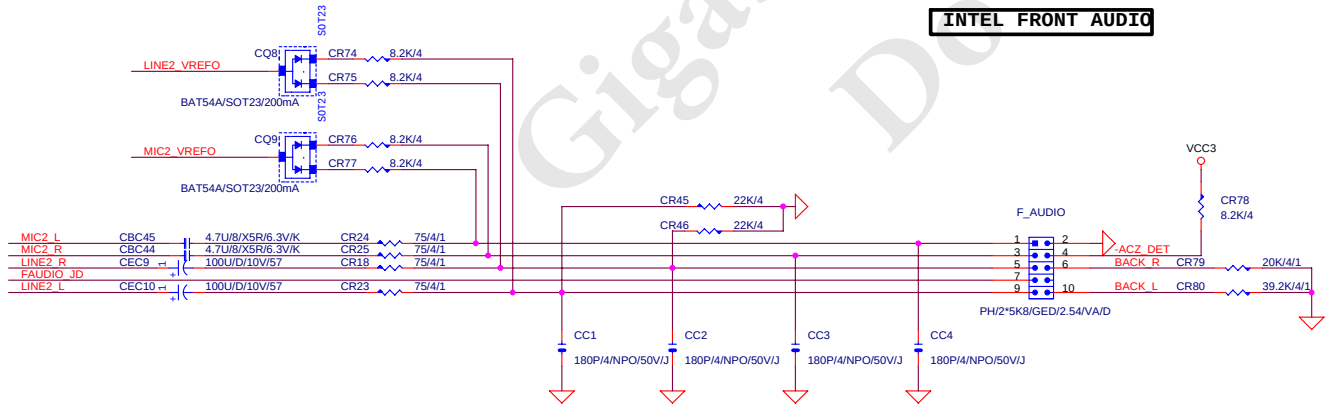






AZALIA CODEC *ALC892/ALC888B/ Colay*

	ALC892		ALC888B
CR22	X		X
CBC42	10uF/X5R		X
CR12	0		X
CR16	X		0



GIGABYTE

Title: ALC888B CODEC

Size	Document Number	Rev
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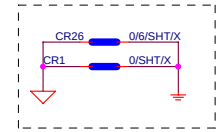

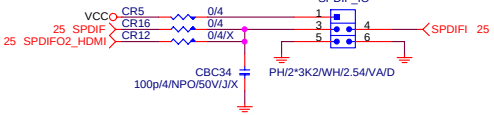

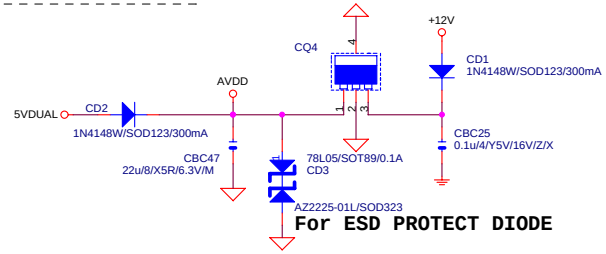

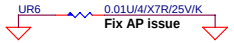

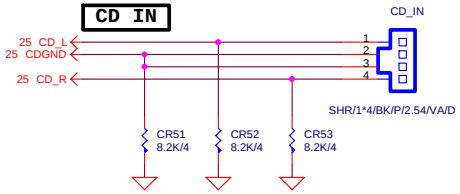

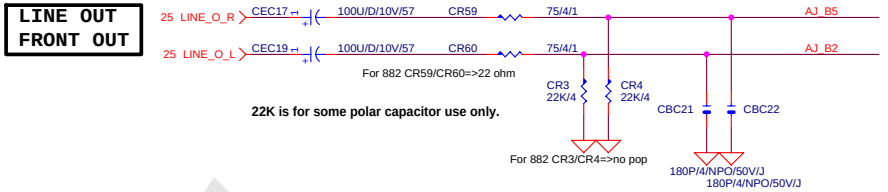

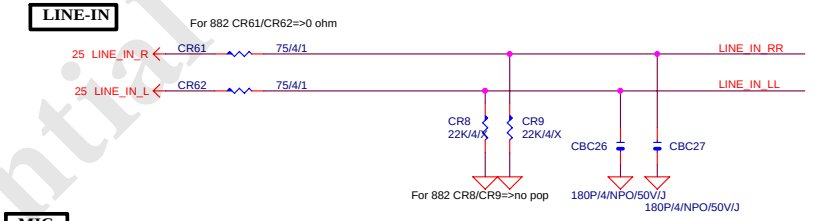

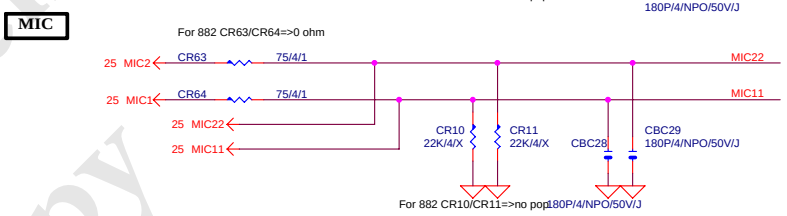

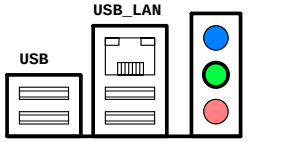

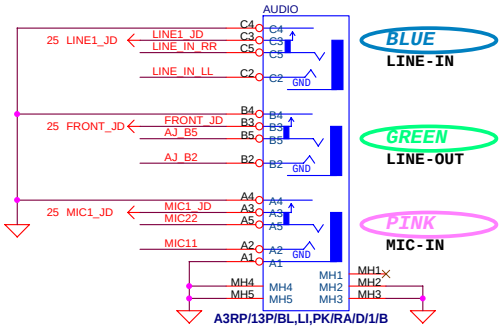

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Title: AUDIO JACK

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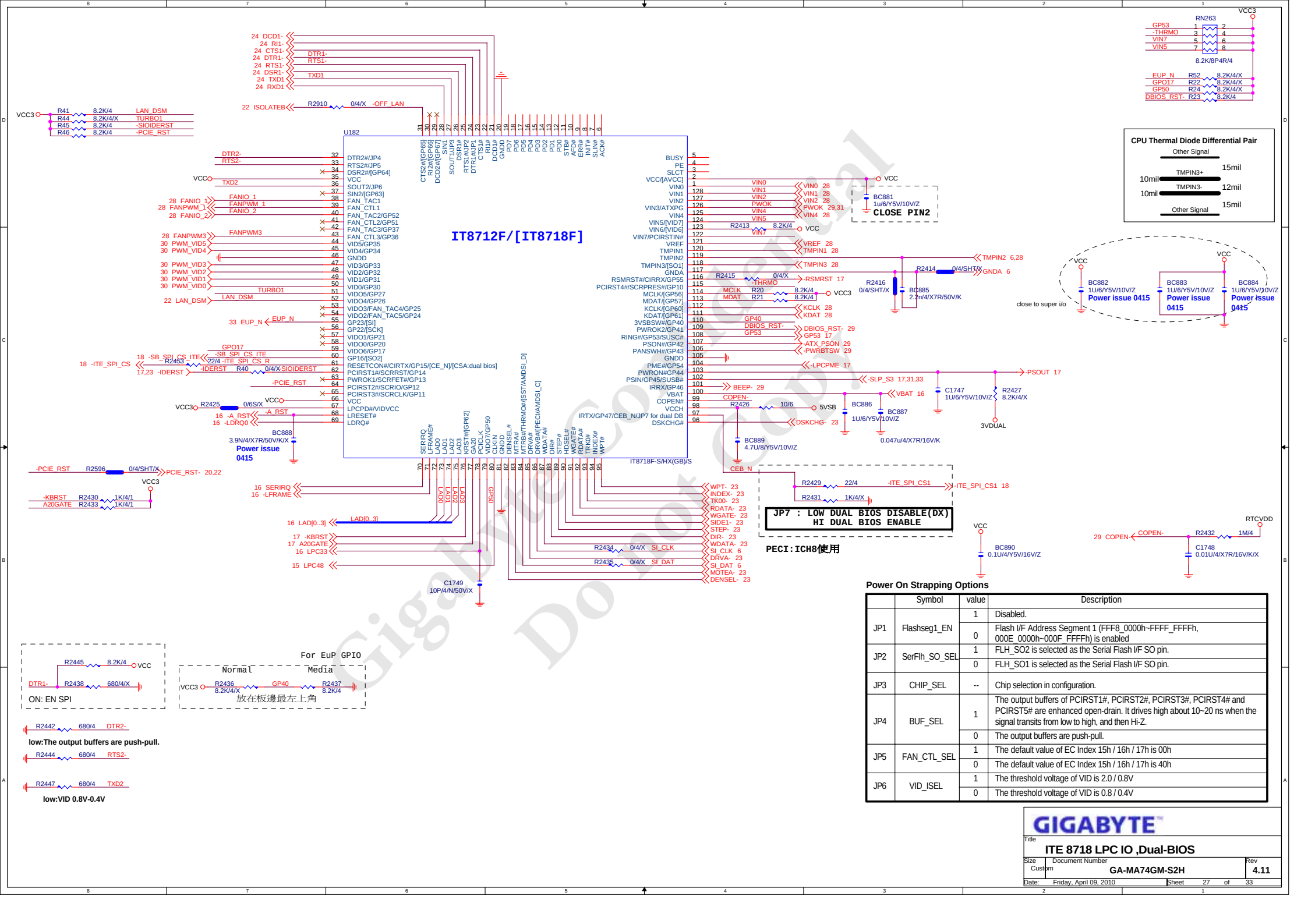

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title: ITE 8718 LPC IO ,Dual-BIOS

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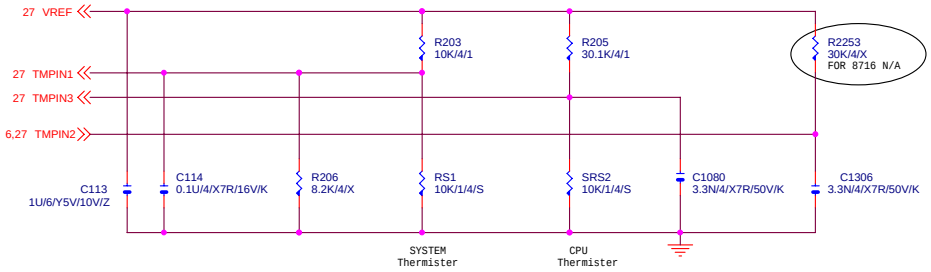
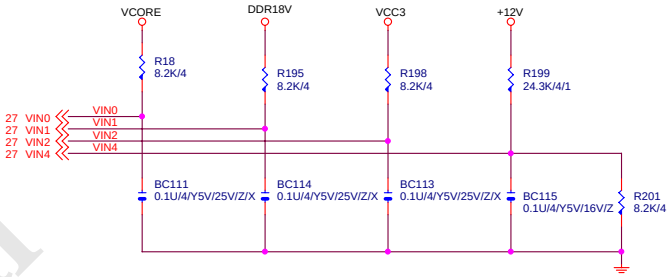
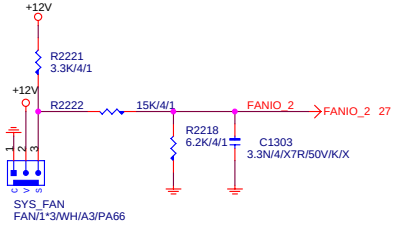
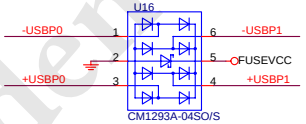
Hardware Monitor circuits



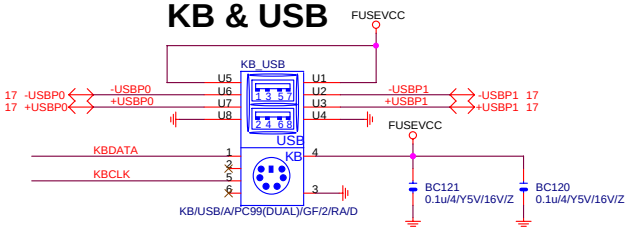


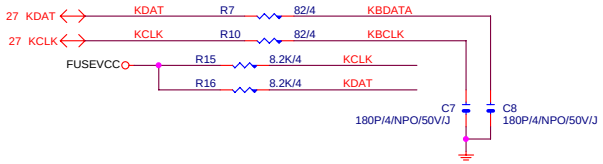
SYSTEM FAN

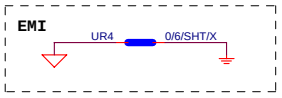




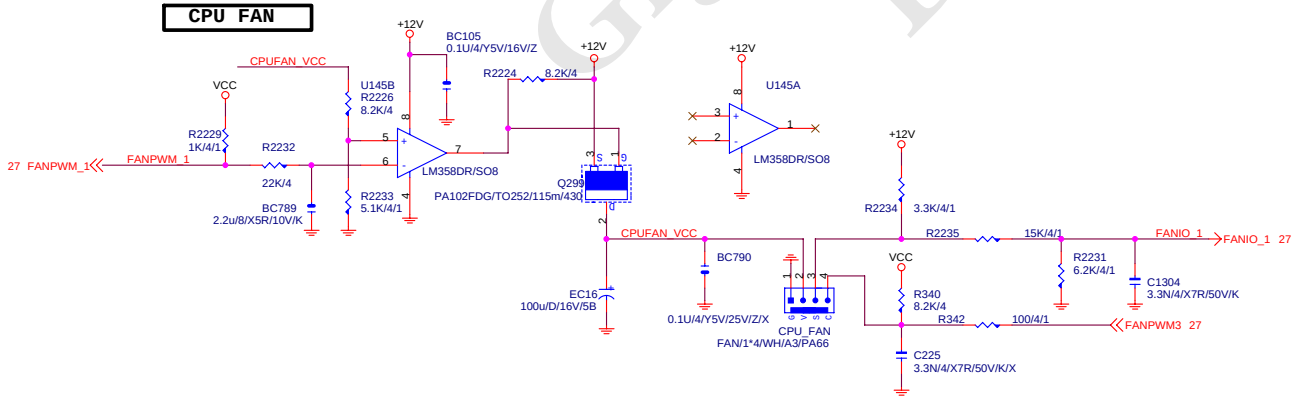
KB & USB

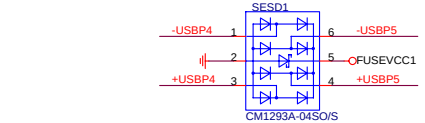


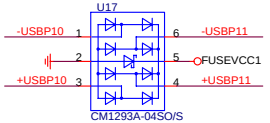


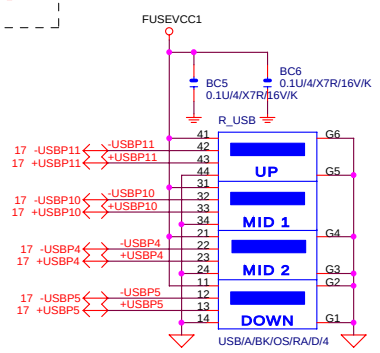


CPU FAN









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Title: FAN/HWMO ,KB/USB

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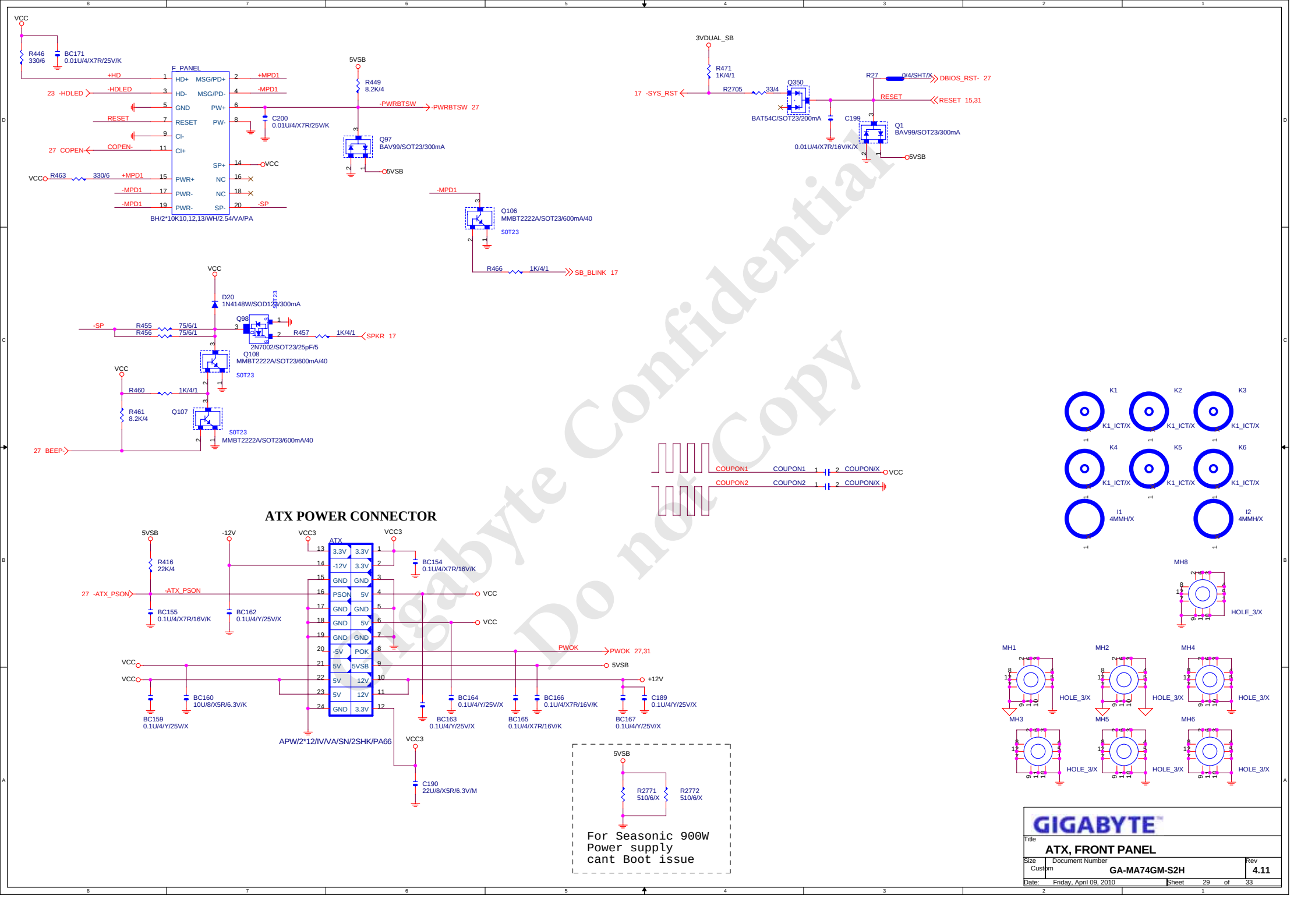

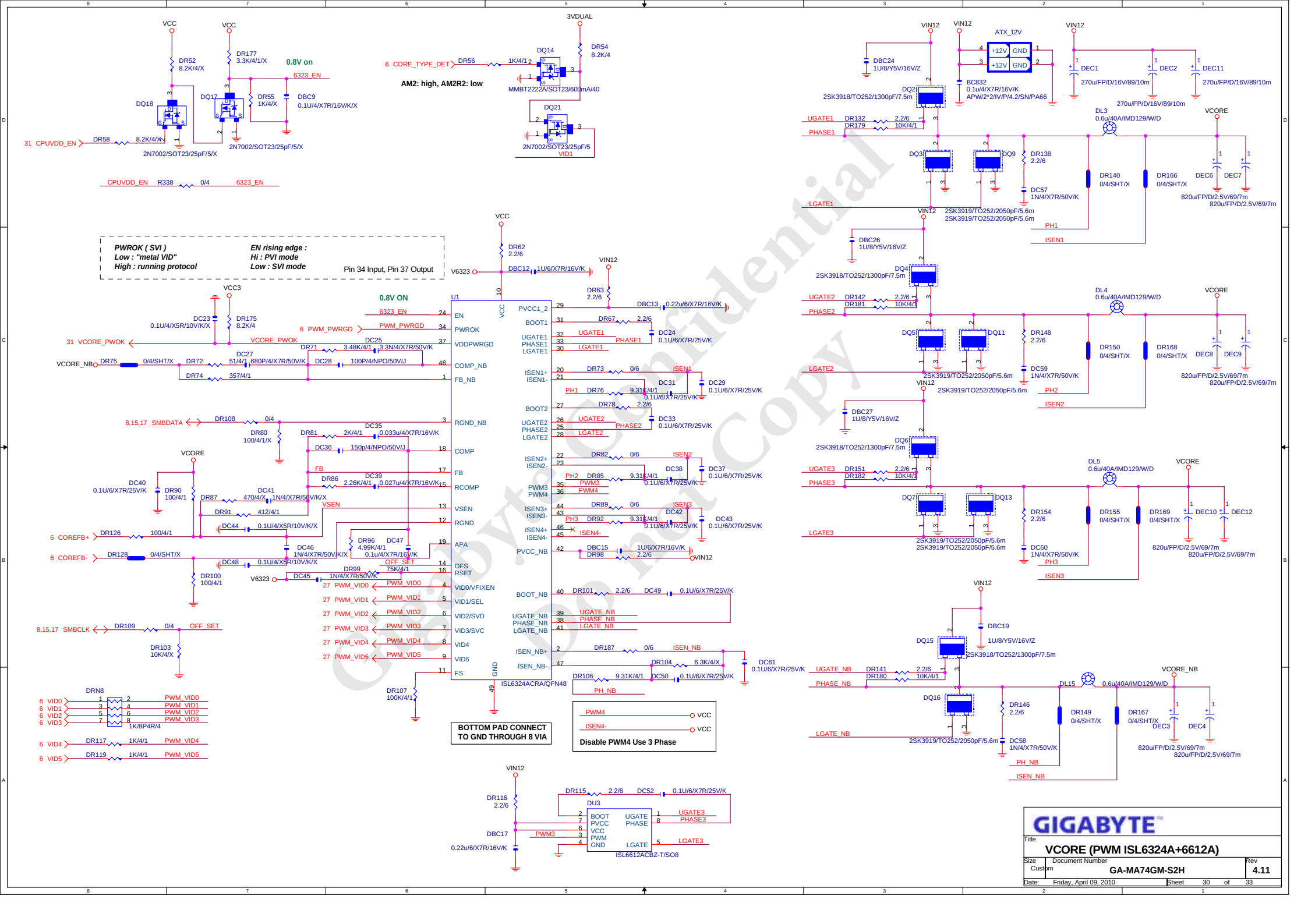

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Title	VCORE (PWM ISL6324A+6612A)	
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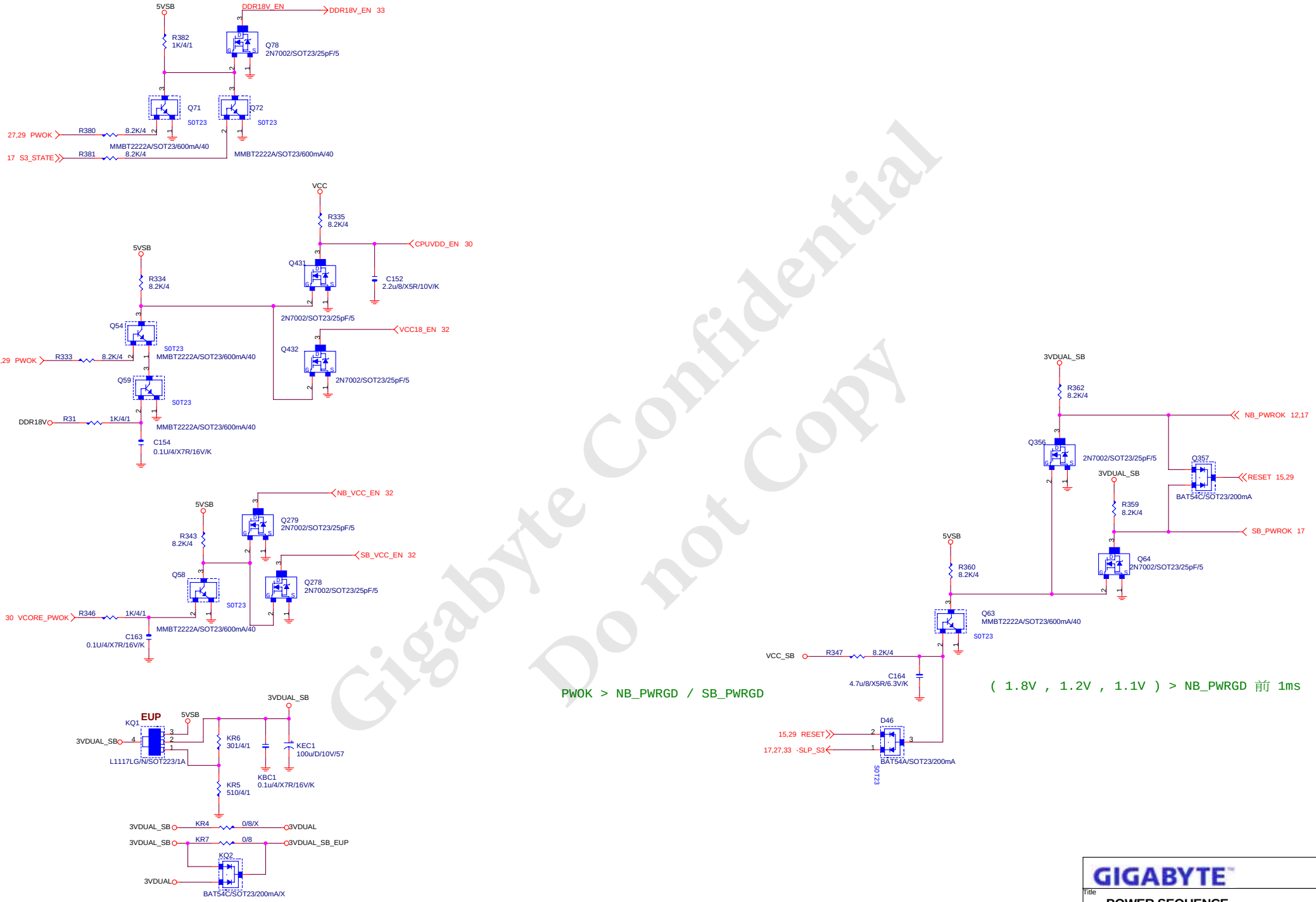

PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

GIGABYTE

Title: POWER SEQUENCE

Size	Document Number	Rev
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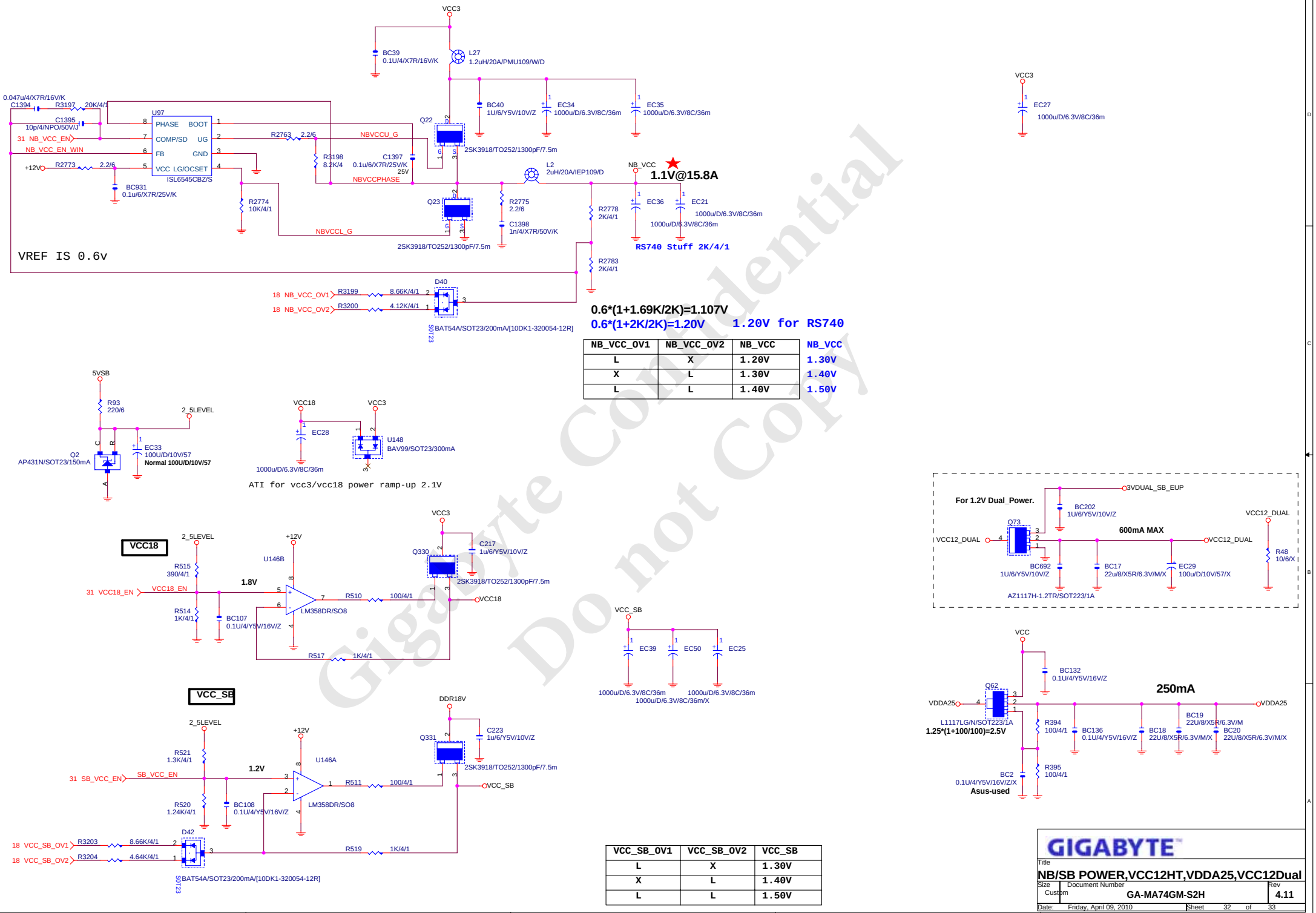

GIGABYTE

Title
NB/SB POWER,VCC12HT,VDDA25,VCC12Dual

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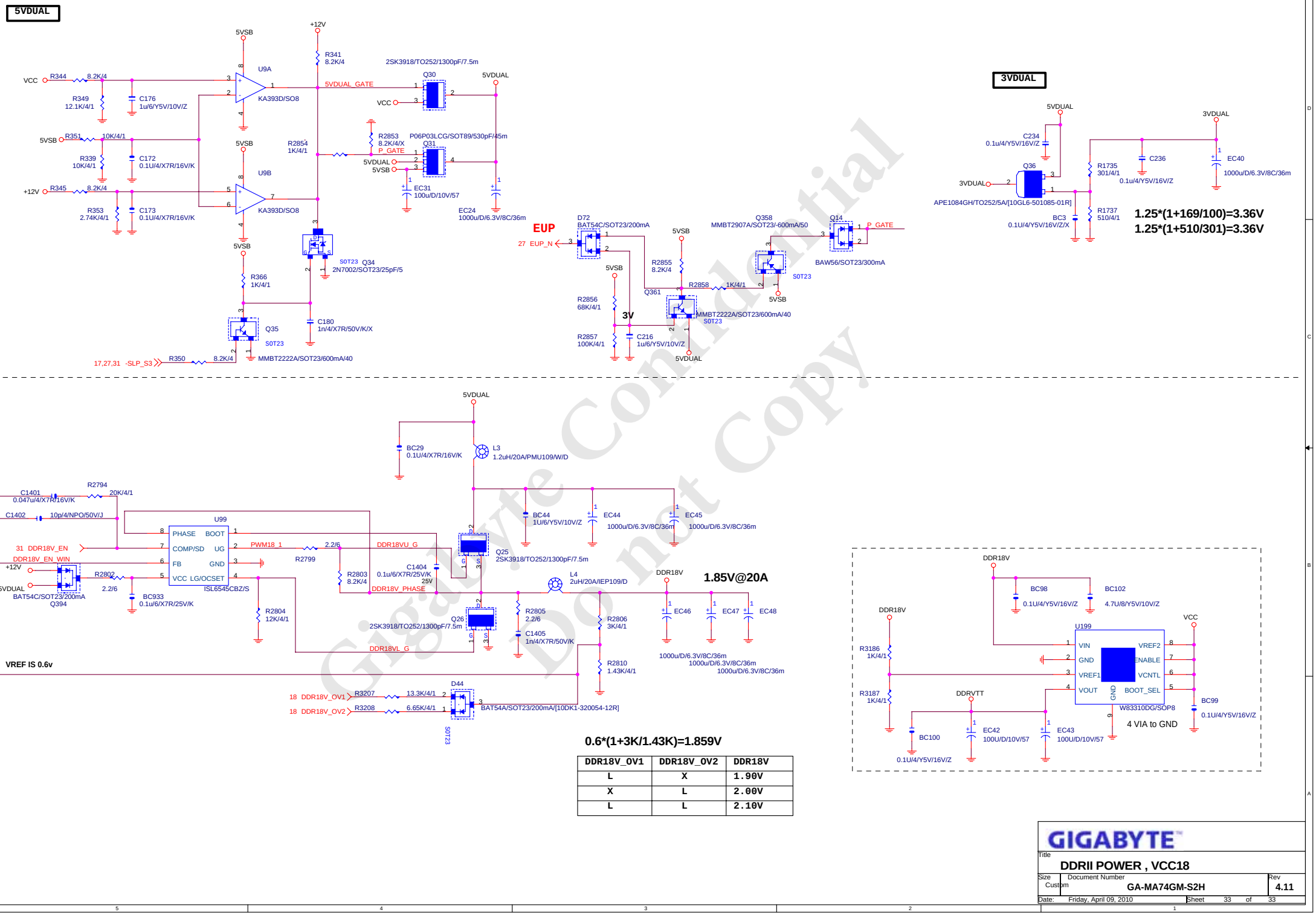

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

GIGABYTE

Title: DDRII POWER , VCC18

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