

Model Name: GA-H97M-D3H

Revision 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1150-A
05	CPU LGA1150-B
06	CPU LGA1150-C
07	DDR III CHANNEL A 1,2
08	DDR III CHANNEL B 1,2
09	PCH FDI,DMI,USB,PCIE,NVRAM
10	PCH DP,CLK BUFFER
11	PCH HOST,SATA,PCI
12	PCH GPIO,CTRL,AUDIO
13	PCH PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*4 SLOT
16	PCI SLOT1,2
17	ITE 8620 LPC IO
18	COM,KB MS USB,USB30 20
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	FP,FUSB,SPK,SATALED
22	Realtek ALC892-GR
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX ,TPM
27	VCORE ISL95820 1

SHEET

TITLE

28	VCORE ISL95820 2
29	RT8120 DDR POWER
30	LPT, M3 POWER
31	DVI, HDMI
32	IT8892E

Gigabyte Technology

Cover Sheet

Size Custom	Document Number <b>GA-H97M-D3H</b>	Rev <b>1.0</b>
Date: Monday, April 28, 2014	Sheet 1 of 32	

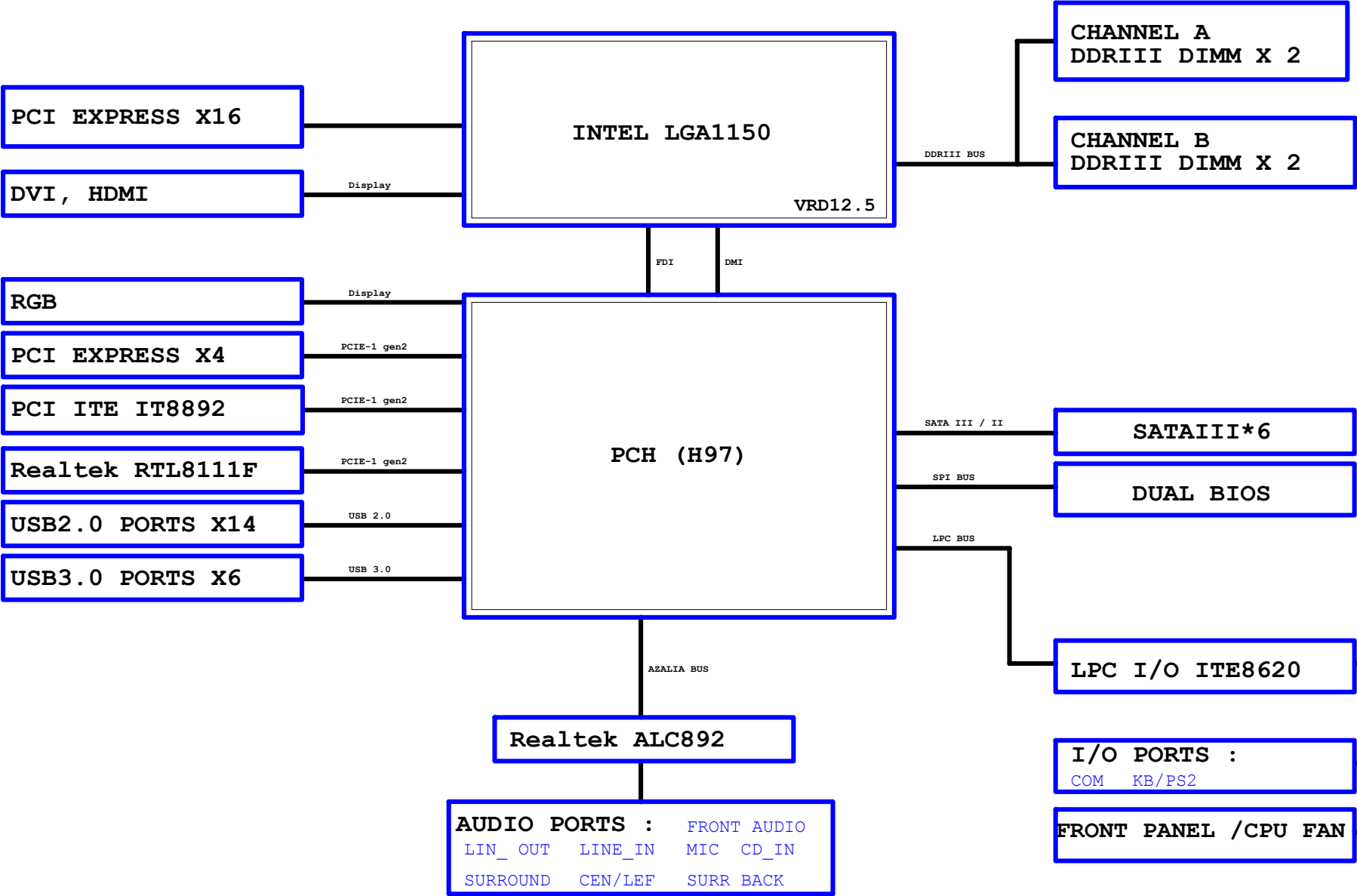
Revision 1.0

## Component value change history

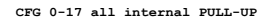
Data	Change Item	Reason
2013/12/09	機構變更MOS_HS尺寸:長度大小由89修改為79mm,孔大小由D3mm修改為D4mm	
2013/12/11	MR.LIN:移除1 PORT 1 FUSE規格	
2013/12/12	MR.LIN:移除DVI LEVEL SHIFTER改成COSTDOWN設計方式	
2013/12/20	HDD LED/FUSB3.0 ESD PROTECTOR	
2013/12/24	MODIFY AP NOTE	
2013/12/26	MODIFY AP NOTE:USB防燒,IT8620斜插ISSUE	
2013/12/27	R0.1 GERBER OUT	
2014/1/13	AP NOTE:DVI LEVEL SHIFTER改回	
	PCH_HS,MOS_HS:9 SERIES	
	加回AP431 BOM VCC1_5_PCH_OV	
2014/1/16	AP NOTE(UATX):DVI LEVEL SHIFTER移除	BIOS DRIVING 800mV 2dB
	BIOS_PH移除	
2014/1/27	COSTDOWN:5VDUAL-->FUSEVCC_R2,DEL UD7	BAT54A
2014/1/28	AP NOTE:移除F_USB保護線路及AP431	
2014/2/10	CPU FAN PIN2增加C319 0.1U/4/X7R/16V/K	
	Q47,Q48:2N7002 GATE~VCC3	
	FOOT MASK	
2014/2/18	C136:0.1u/6/X7R/25V/K	
	H97 Vcore High /low side ON: 10IF9-584081-00R NTMFS4C08NT1G	
	Non-Vcore High /low side ON: 10IF9-070410-00R NTMFS4C10NT1G	
2014/2/19	R1.0 GERBER OUT	
2014/04/11	Update H97 Chipset 料號 [10HB1-030H97-20R]	
2014/04/25	Update DDR RC	PBOM: 9MH97MD3H-00-10C
	R396: 27K -> 20K	
	R657: 487 -> 680	
	R380: 2.26K -> 2.15K	

[illegible]

BLOCK DIAGRAM



**(E)**



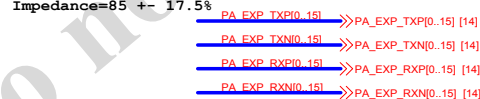
DVI-D + HDMI組態就是: DVI-D port C, HDMI port B

(D)

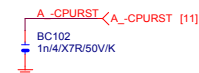


(C)

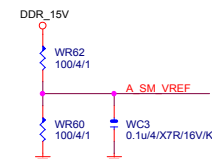
Impedance=80 +- 17.5%



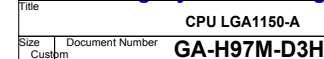
**-CPURST**



## CPU SVID



THRMTRIP DISABLE



LGA1150A			
MAAA0	AU13	DDR0_MA0	DDR0_D00
MAAA1	AV16	DDR0_MA1	DDR0_D01
MAAA2	AU16	DDR0_MA2	DDR0_D02
MAAA3	AW17	DDR0_MA3	DDR0_D03
MAAA4	AU17	DDR0_MA4	DDR0_D04
MAAA5	AW18	DDR0_MA5	DDR0_D05
MAAA6	AW17	DDR0_MA6	DDR0_D06
MAAA7	AT18	DDR0_MA7	DDR0_D07
MAAA8	AU18	DDR0_MA8	DDR0_D08
MAAA9	AT19	DDR0_MA9	DDR0_D09
MAAA10	AW11	DDR0_MA10	DDR0_D10
MAAA11	AV19	DDR0_MA11	DDR0_D11
MAAA12	AU19	DDR0_MA12	DDR0_D12
MAAA13	AT20	DDR0_MA13	DDR0_D13
MAAA14	AT20	DDR0_MA14	DDR0_D14
MAAA15	AU21	DDR0_MA15	DDR0_D15
MODT_A0	AW10	DDR0_ODT0	DDR0_D16
MODT_A1	AV3	DDR0_ODT1	DDR0_D17
MODT_A2	AW9	DDR0_ODT2	DDR0_D18
MODT_A3	AU8	DDR0_ODT3	DDR0_D19
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(F, J)



(G, H, I)



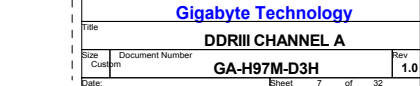
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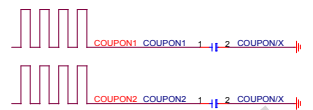
(x9)







(B)



**DIMM4 (黒)**

**DIMM2 (灰)**

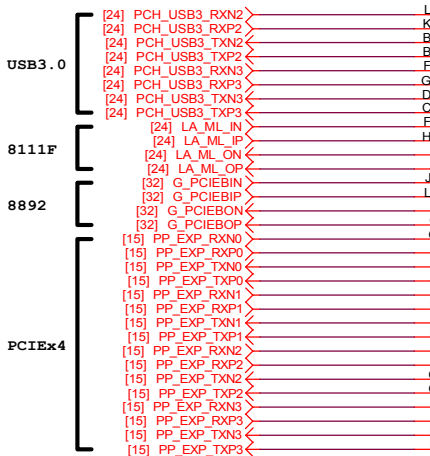
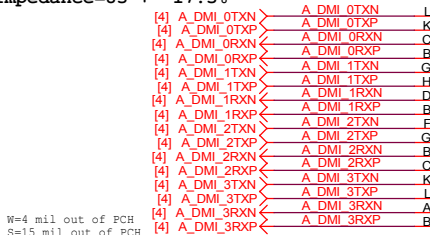
**DIMM3 (黒)**

**DIMM1 (灰)**



PCH

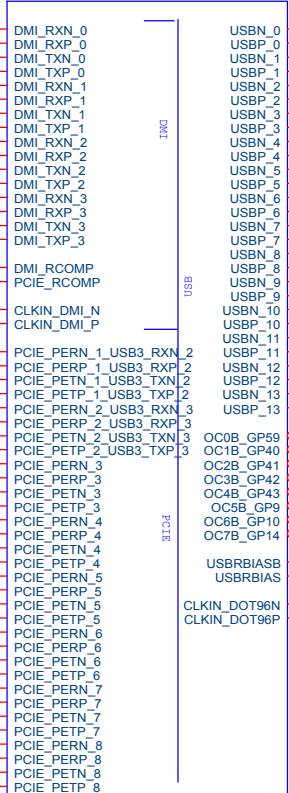
(B)

DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

電容放靠近 Device &amp; PCI-E Slot

PCIEX1:15/4/4/4/15 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

PCHB



CHIP DH82H97 A0 INTEL(10HB1-030H97-20R)

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

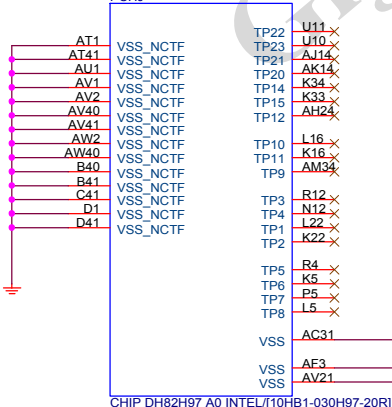
PCH

(J)

PCH PCIE ,DMI 15/4/4/4//15

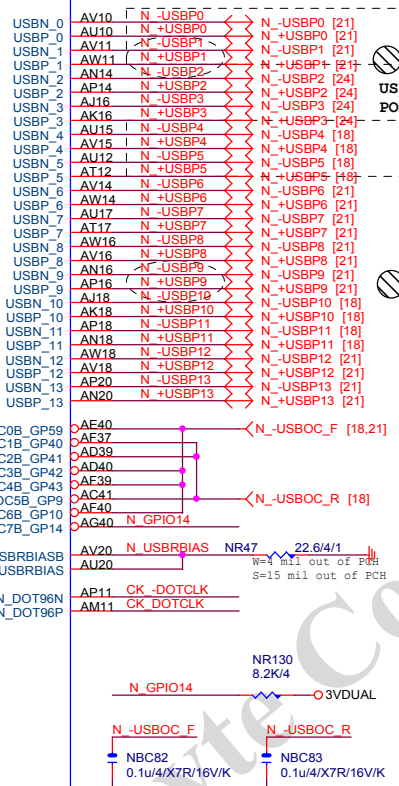
usb2.0 12/5/7/5//12  
usb3.0 20/5/7/5//20

PCHJ



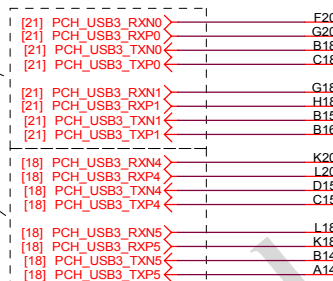
CHIP DH82H97 A0 INTEL(10HB1-030H97-20R)

PORT1,PORT9[DEBUG PORT]FOR WHQL一定要拉出PORT

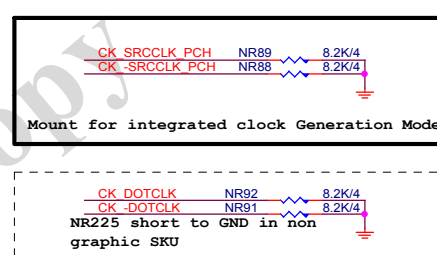
B85: Port 6/7 N/A  
H81: Port 6/7/12/13 N/A

PCH

(F)

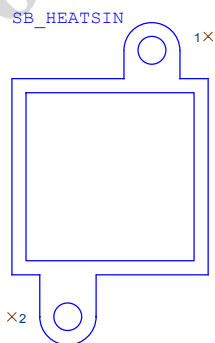


PCH CLK PD

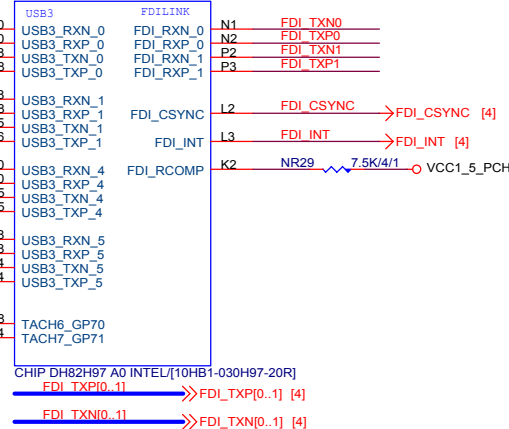


PCH H/S

9 Series PCH Heatsink

PCH\_HS  
9 SERIES PCH\_HS(12SP2-S04242-01R\_12SP2-S04242-02R\_12SP2-S04242-03R)

PCHF

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS

USB TABLE

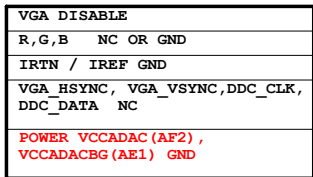
OC[3:0]# for Device 29 (ports 0-7)  
OC[7:4]# for Device 26 (ports 8-13)

USB OC#	Configure
OC0#	F_USB30
OC1#	R_USB30
OC2#	USB30_LAN
OC3#	F_USB3
OC4#	F_USB2
OC5#	KB_MS_USB
OC6#	F_USB1
OC7#	Not Use

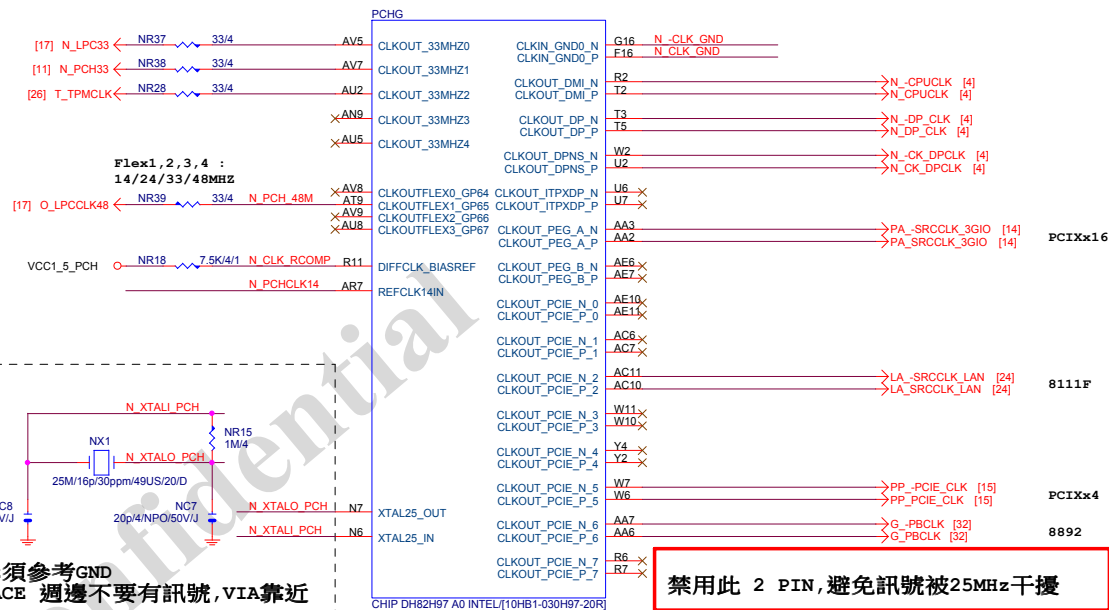
Gigabyte Technology

Title		
PCH FDI,DMI,USB ,PCIE,NVRAM		
Size	Document Number	Rev
Custom	GA-H97M-D3H	1.0
Date:	Monday, April 28, 2014	Sheet 9 of 32

(E)



(G)



Differential Clock:18/4/6/4/18  
Impedance=90 +- 15%

N -CLK GND NR42 8.2K/4  
 N CLK GND NR41 8.2K/4

Mount for integrated clock Generation  
Mode



VGADDCDATA 1 6 VGADDCCLK

2 5

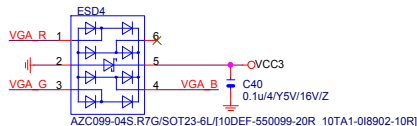
N\_GHSYNC 3 4 N\_GVSYNC

VCC

C33  
0.1uF/4Y5V/16V/Z

AZC099-04S.R7G/SOT23-6L/[10DEF-550099-20R\_10TA1-018902-10R]

SSOP6 ESD



The schematic diagram illustrates the VDDC3 power plane. It features two input signals, **N\_DDCDATA** and **N\_DDCCLK**, which are connected to the circuit through a network of resistors and capacitors. The resistors **R146** and **R147** (both 2.2K/4/1) are connected to the **VCC3** supply. The capacitors **C0723** and **C0724** (both 2N7002/SOT23/25pF/5/[10]F1-4B7002-01R) are connected to the **VCC3** supply and the **VGADDCDATA** and **VGADDCCLK** signals, respectively. The **VGADDCDATA** and **VGADDCCLK** signals are connected to the **VCC3** supply through resistors **R145** and **R144** (both 2.2K/4/1). The **VCC3** supply is connected to the **VGADDCDATA** and **VGADDCCLK** signals through a network of resistors and capacitors. The **VCC3** supply is also connected to the **VGADDCDATA** and **VGADDCCLK** signals through a network of resistors and capacitors. The **VCC3** supply is connected to the **VGADDCDATA** and **VGADDCCLK** signals through a network of resistors and capacitors.

**Close to PCH**

**Close to Filter**

Close to PCH

Close to Filter

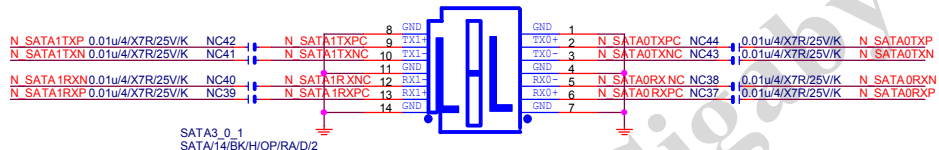
**BLACK CONNECTOR**

BLACK CONNECTOR

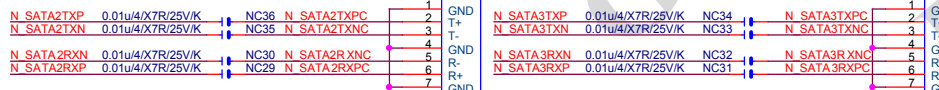
(C)



## SATA CONNECTOR

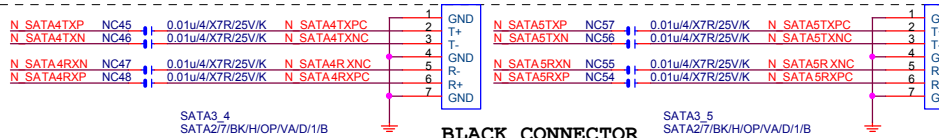


H81 Port 2/3 N/A

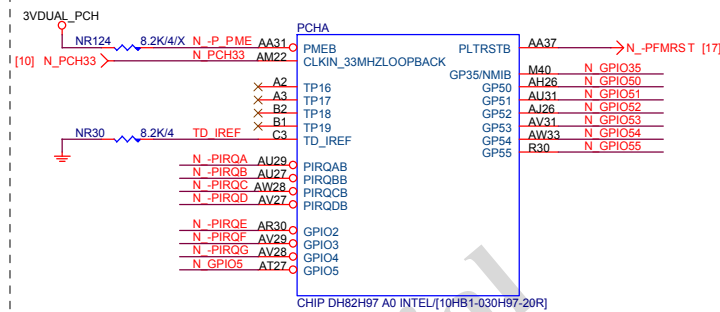


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** Z87/H87 Port 4&5 SATA3.0
```

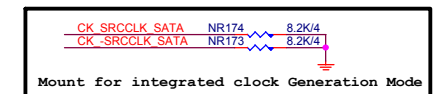
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** B85 Port 4&5 SATA2.0
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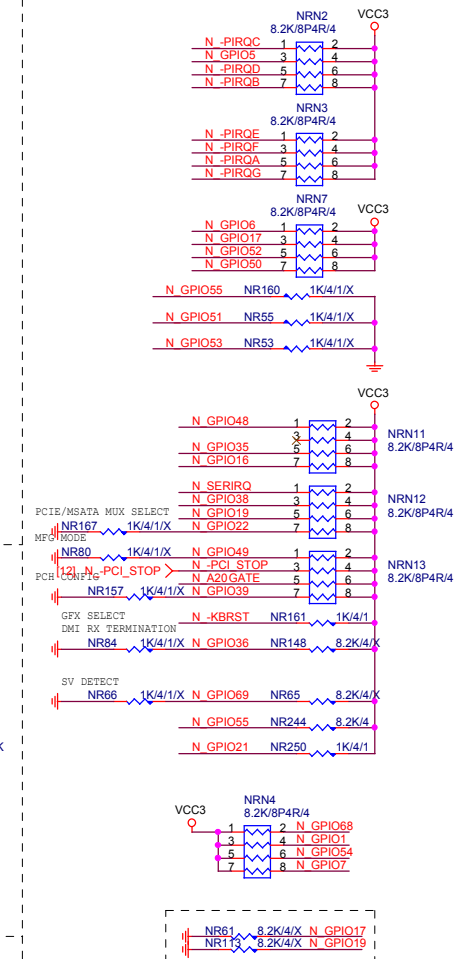
(A)



PCH	CLK	PD
-----	-----	----

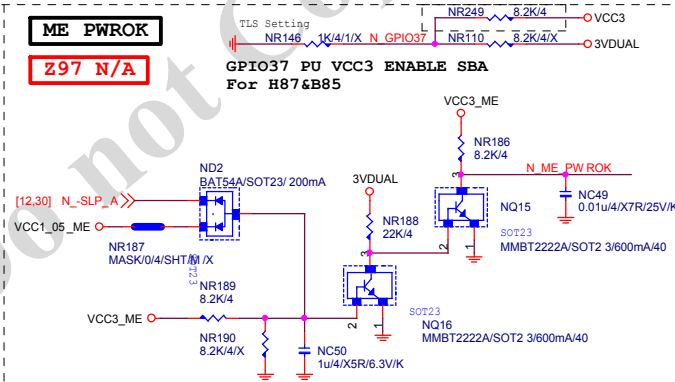


PCH	PU/PD
-----	-------

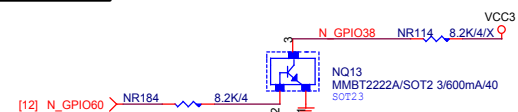


## ME PWROK

Z97 N/A



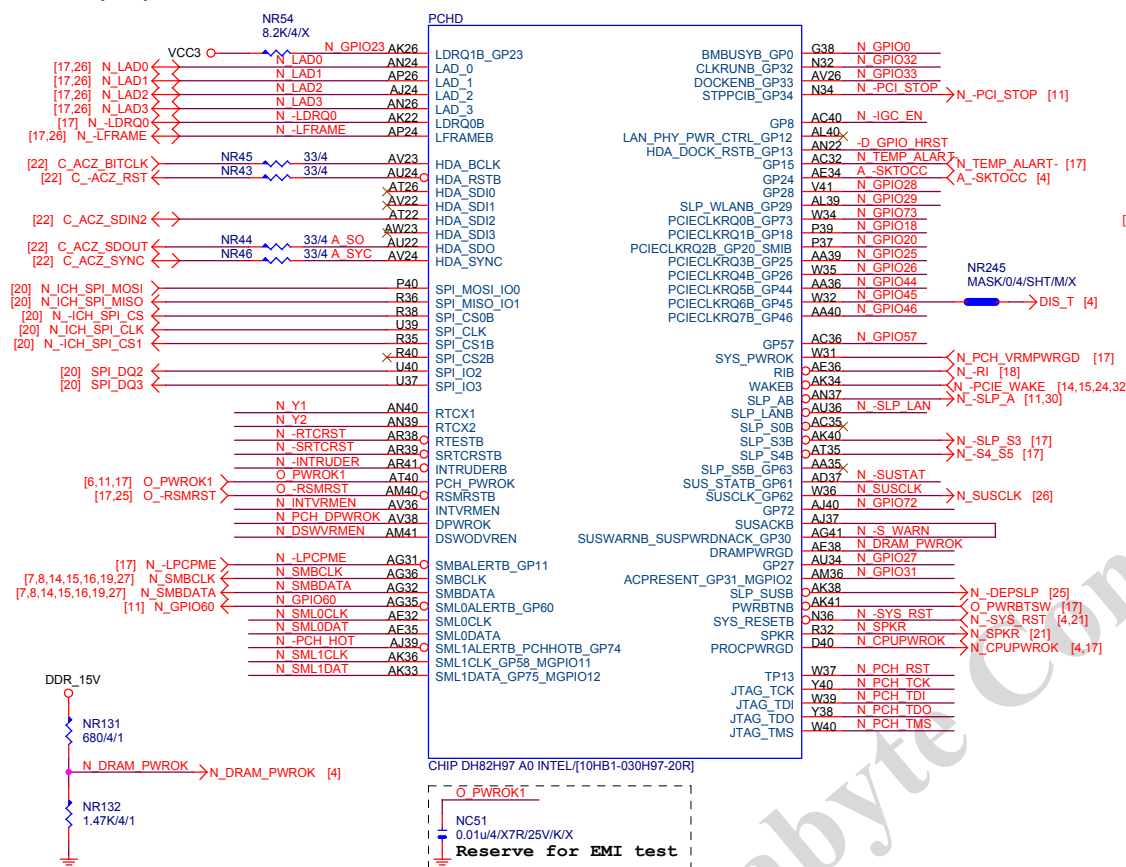
GPIO38 Ctrl



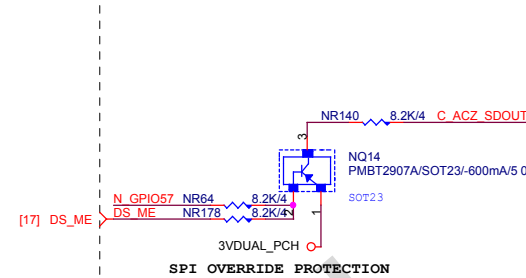
## Gigabyte Technology

Title			
PCH HOST , SATA, PCI			
Size	Document Number		Rev
Custom	GA-H97M-D3H		1.0
Date:	Monday, April 28, 2014	Sheet	11 of 32

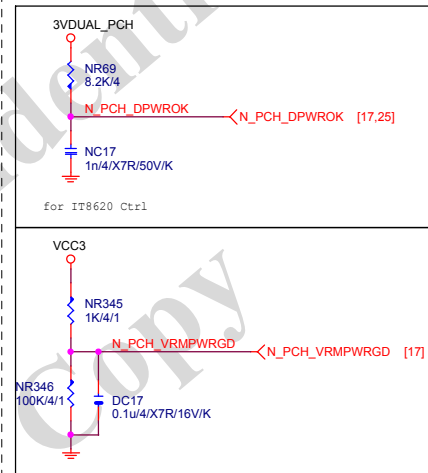
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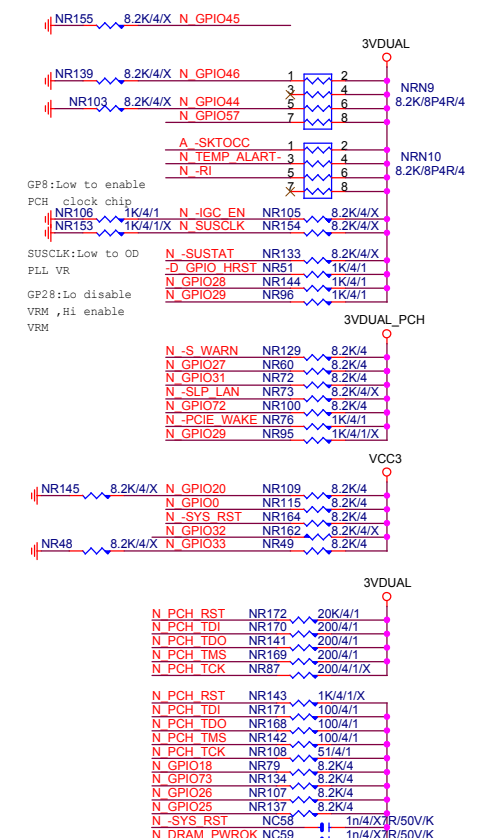
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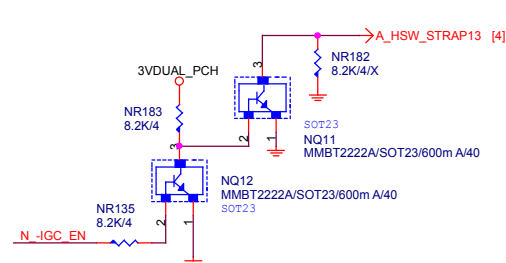
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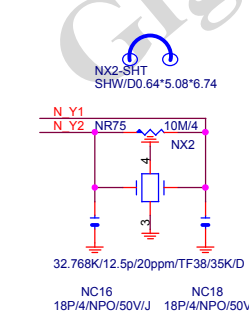
PCH	PU/PD
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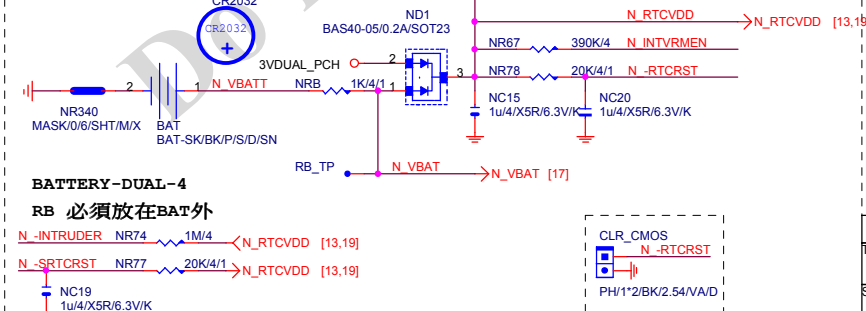
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32.768KHZ



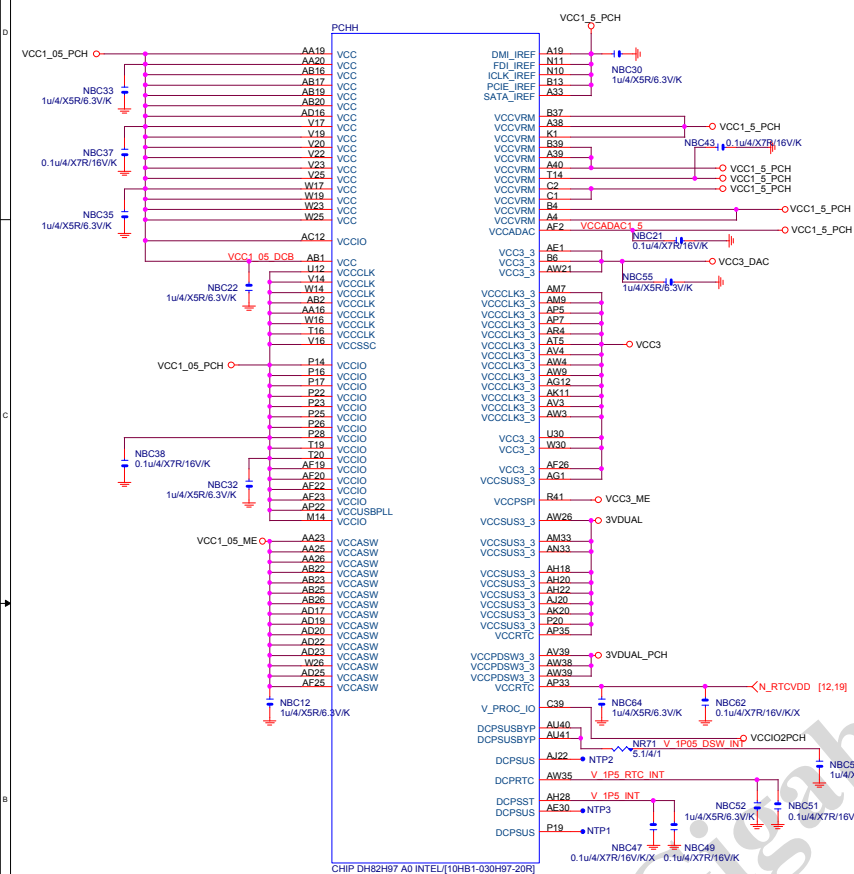
CLR	CMOS
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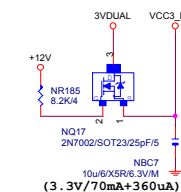
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Date:	Monday, April 28, 2014	Sheet	12 of 32

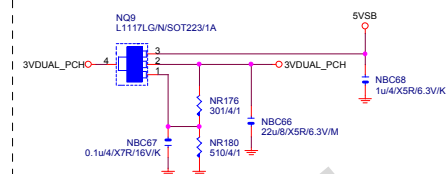
**PCH (H)**



VCC3	DAC
------	-----



## 3VDUAL PCH

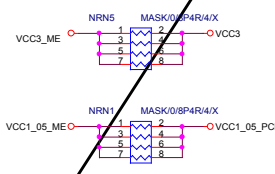


SHT PWR

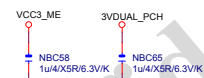
H97 N/A

**MASK FOOT**

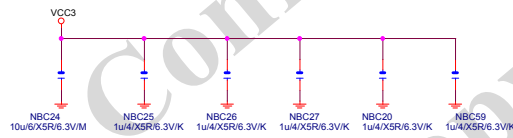
**MASK**



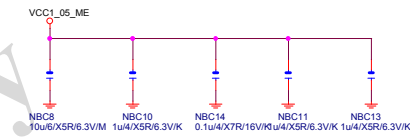
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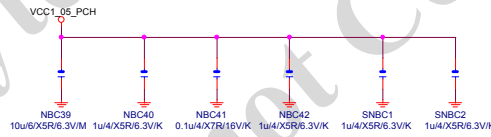
(3.3V) (X6)



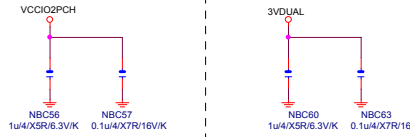
(1.05V) (x5)



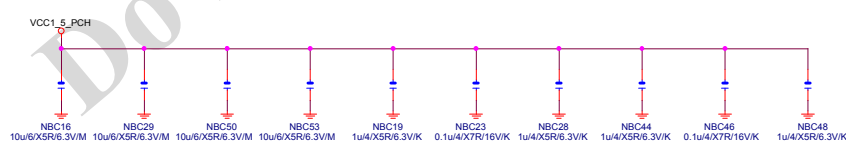
(1.05V) (x6)



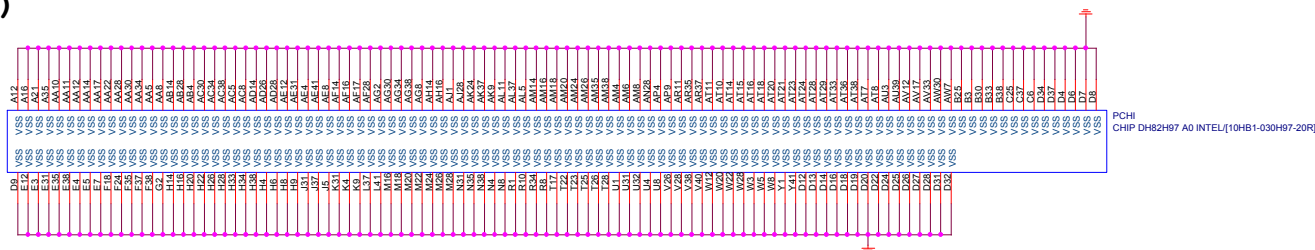
☒ (1.05V)(x2)    ☐ (3.3V) (x2)



(1.05V) (x10)

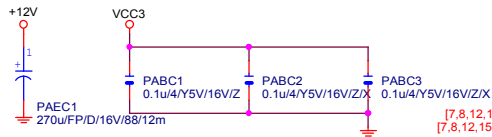


**PCH (I)**

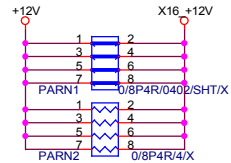




## PCIEX16 CAP



## PCIEX16 PROTECT SHT



## PCIEX16 AC CAP

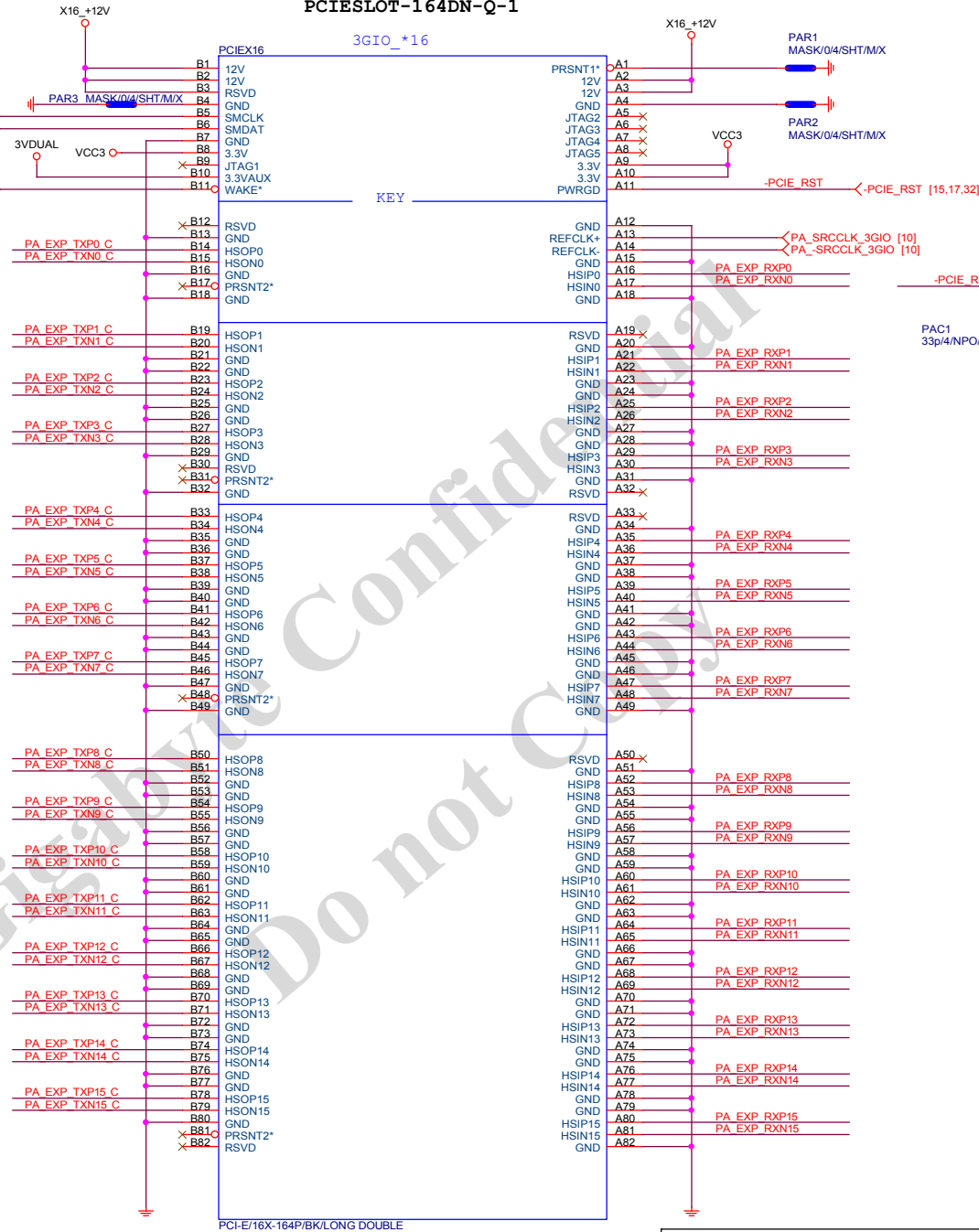
PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXP0 [0.15] >>> PA\_EXP\_RXP0[0.15] [4]  
PA EXP RXN0 [0.15] >>> PA\_EXP\_RXN0[0.15] [4]  
PA EXP TXP0 [0.15] >>> PA\_EXP\_TXP0[0.15] [4]  
PA EXP TXN0 [0.15] >>> PA\_EXP\_TXN0[0.15] [4]

## PCIEX16 SLOT

[7,8,12,15,16,19,27] N\_SMBCLK  
[7,8,12,15,16,19,27] N\_SMBDATA  
[12,15,24,32] N\_-PCIE\_WAKE

## PCIESLOT-164DN-Q-1



PCI-E/16X-164P/BK/LONG DOUBLE

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Gigabyte Technology

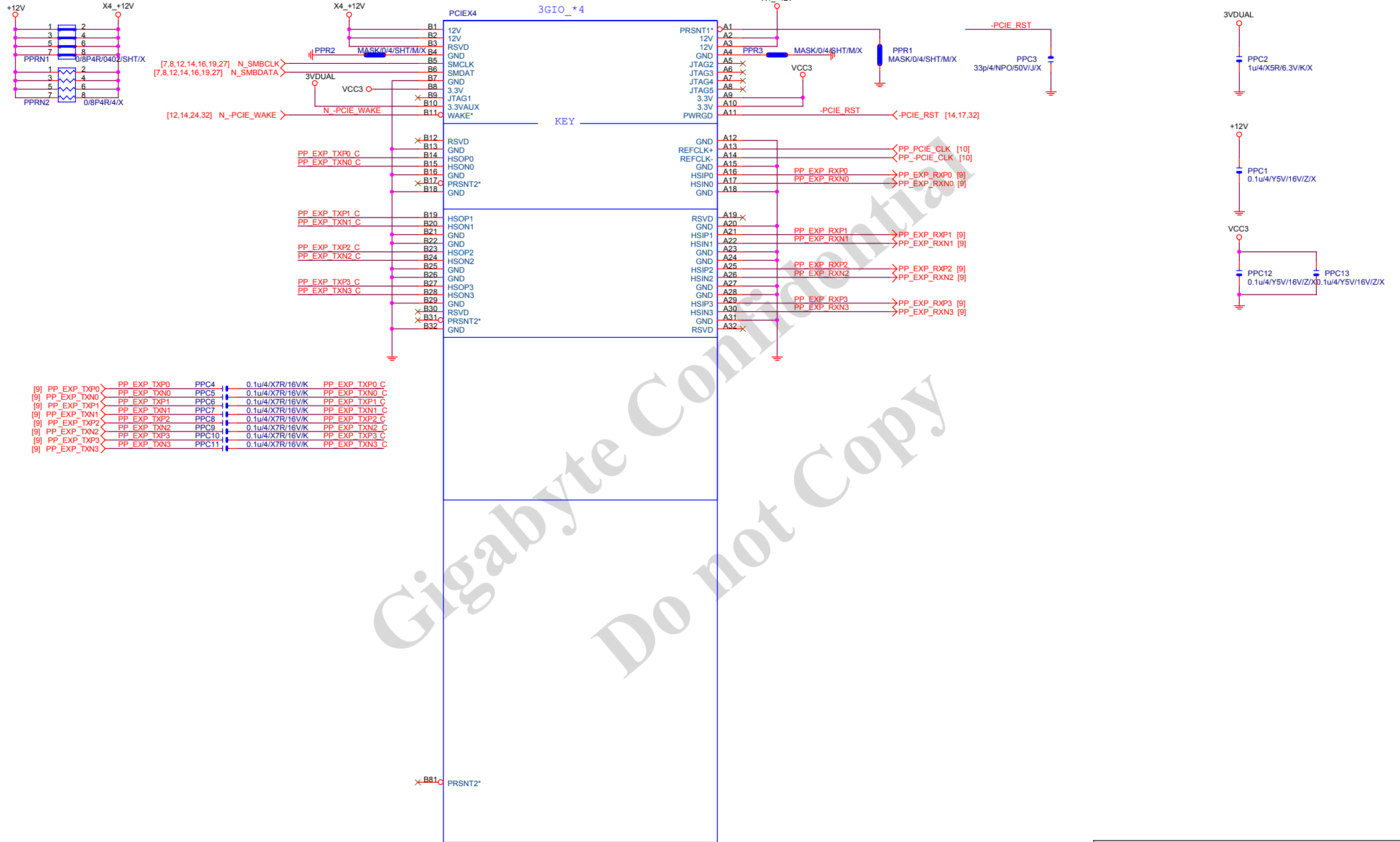
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Size			Document Number		
Custom			GA-H97M-D3H		
Date:			Monday, April 28, 2014		
Sheet			14 of 32		
Rev			1.0		



# PCIEX4 SLOT

## PCIESLOT-64D-98D-P

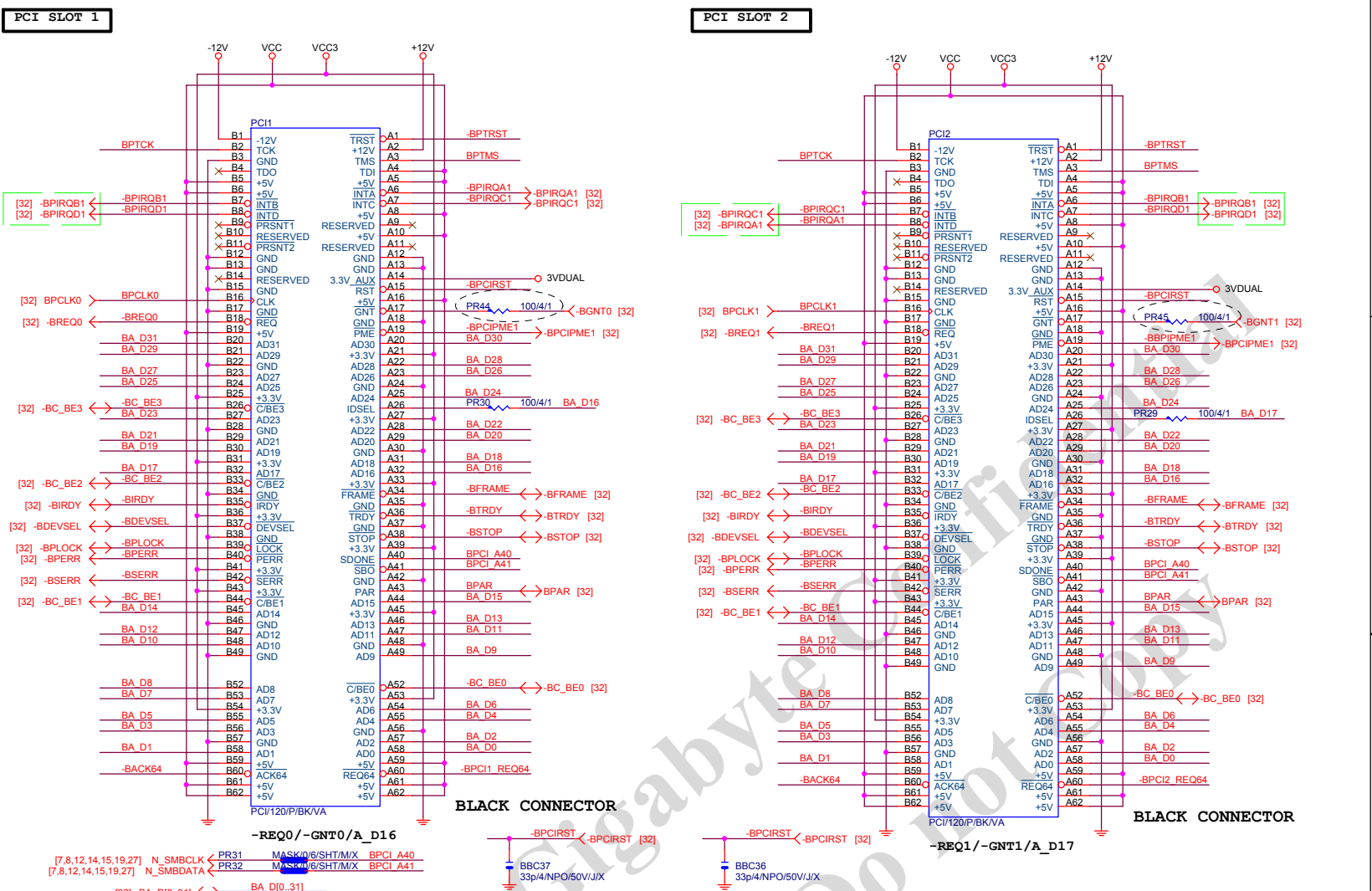
3GIO\_\*4



PCI-E/4X-65P/BK/LONG DOUBLE

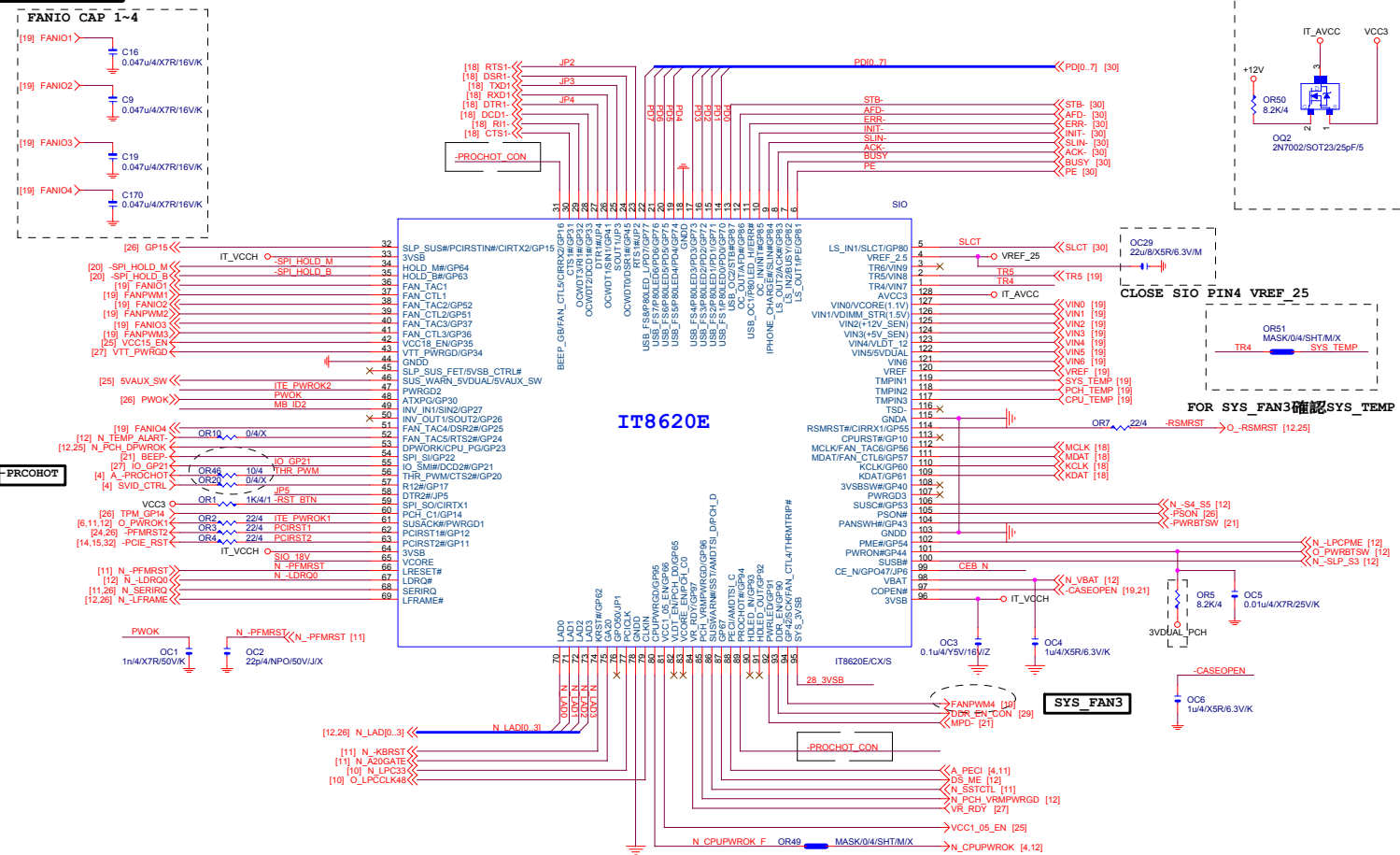
BLACK CONNECTOR

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Size	Document Number	Rev	
Custom	GA-H97M-D3H	1.0	
Date:	Monday, April 28, 2014	Sheet	15 of 32



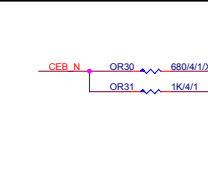
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Size			
Custom			
Document Number			
GA-H97M-D3H			
Date:			
Monday, April 28, 2014			
Sheet			
16 of 32			
Rev			
1.0			

# SIO IT8620



IT8620E GPIO問題調整	
PIN 50	第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HOLD FUNCTION, GP93 BYPASS TO GP92
	高溫時 GP92 會被拉Lo (15S)
PIN 108	8Pin 108 POWER ON 時會拉 LO
PIN 111/112	MOUSE 與FANS FUNCTION 擇一使用, 不然會互相干擾

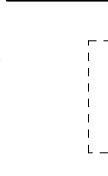
## DUAL BIOS OPT STRAP



## Power leakage N/A



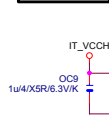
## SIO 18V

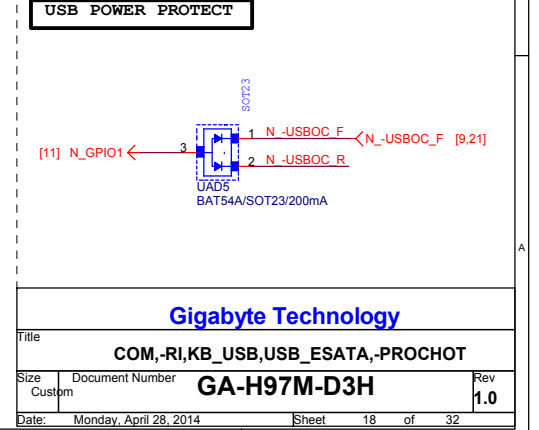
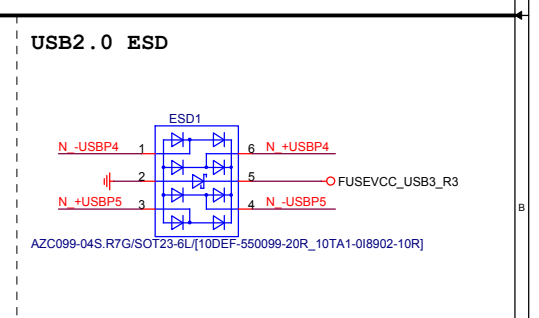
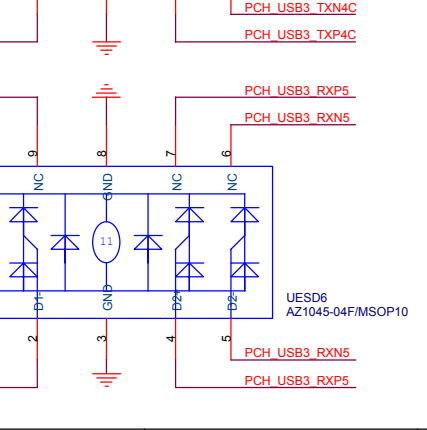
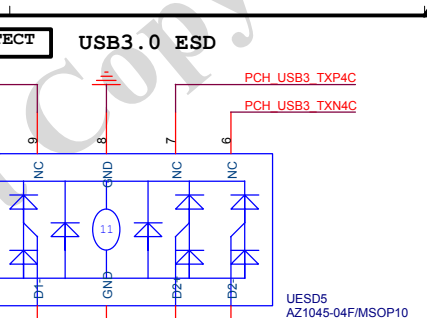
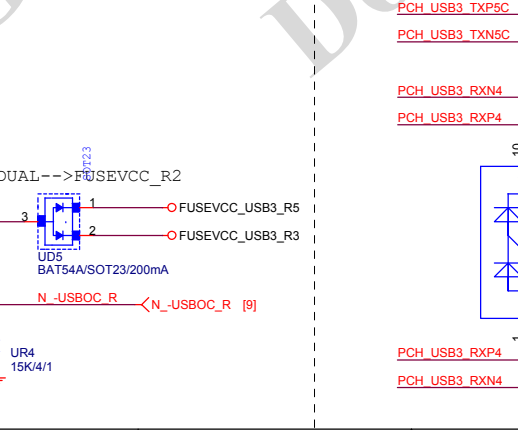
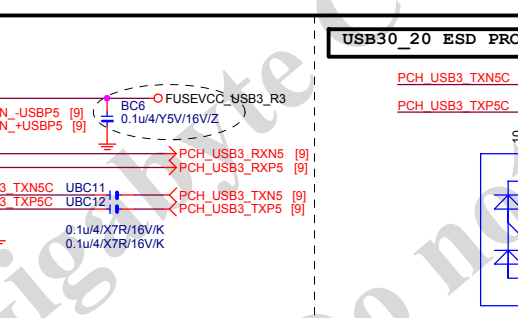
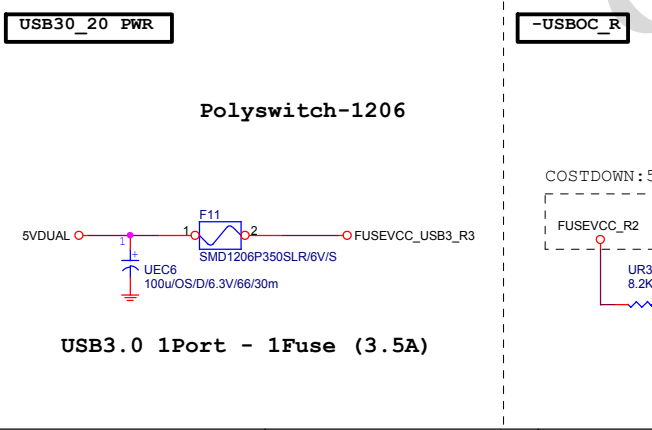
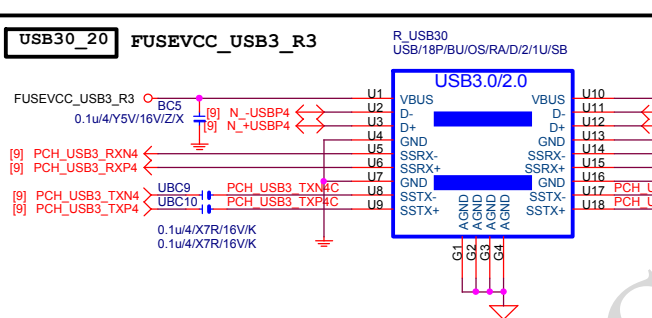
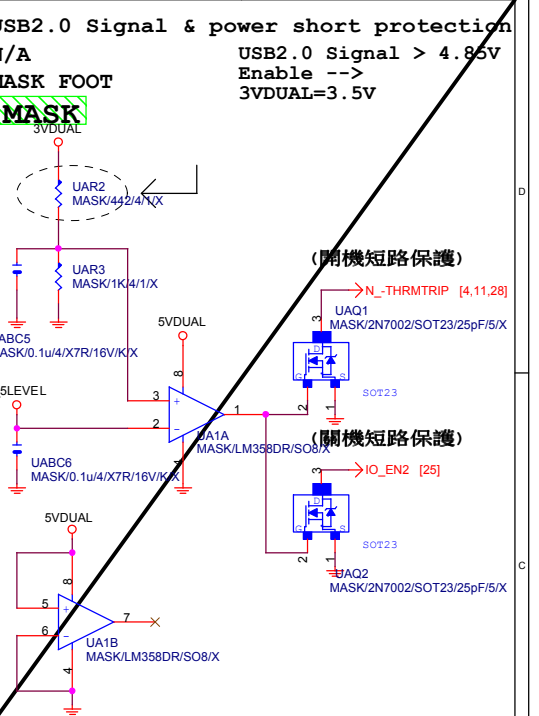
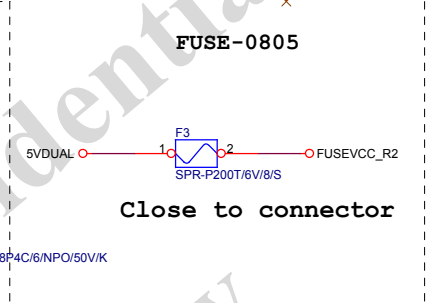
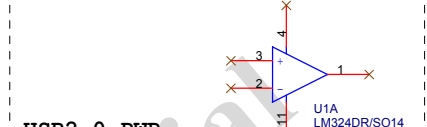
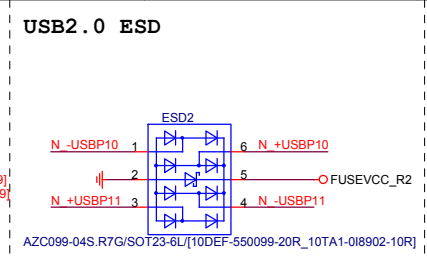
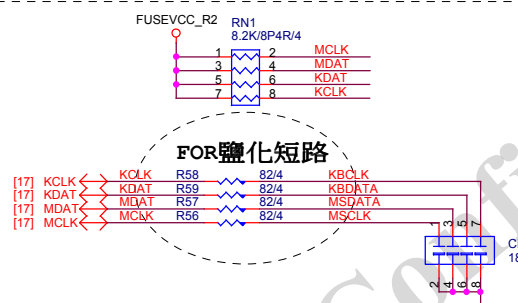
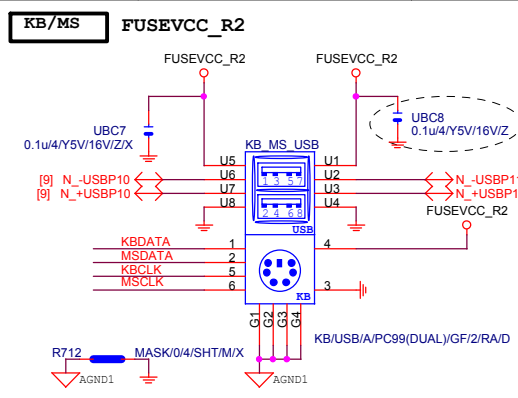
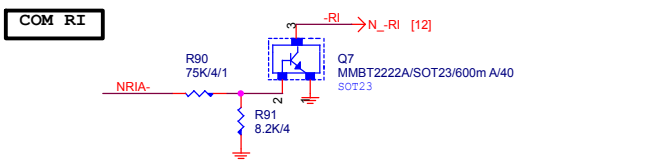
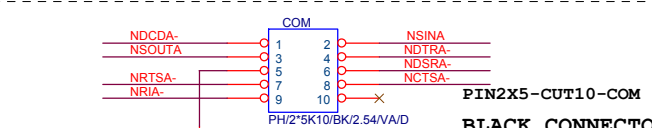
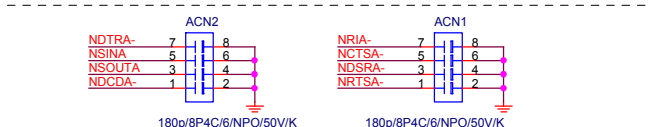
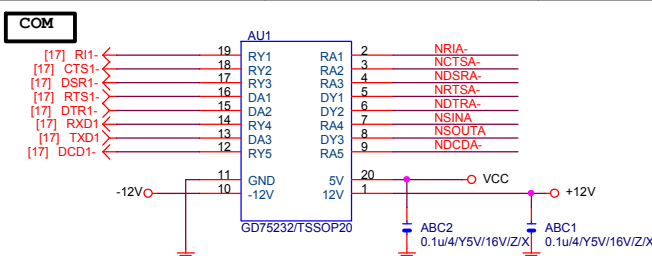


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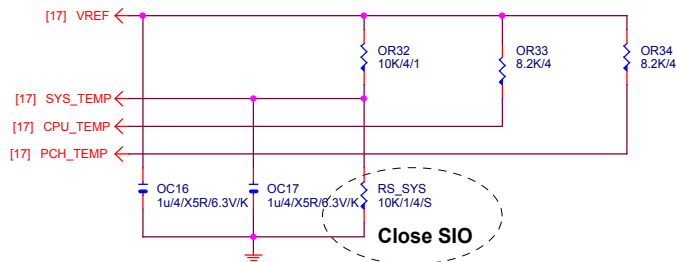


## SIO CAP

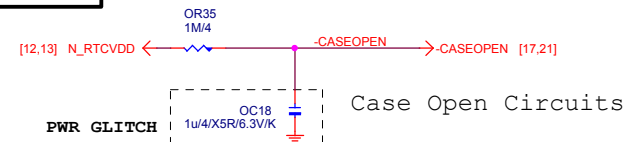




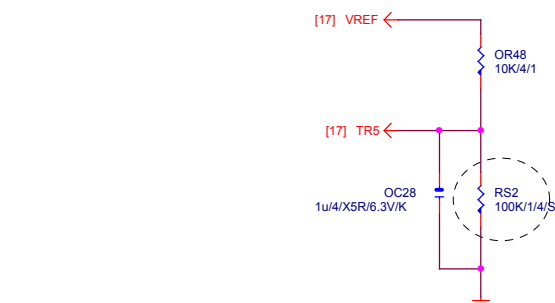
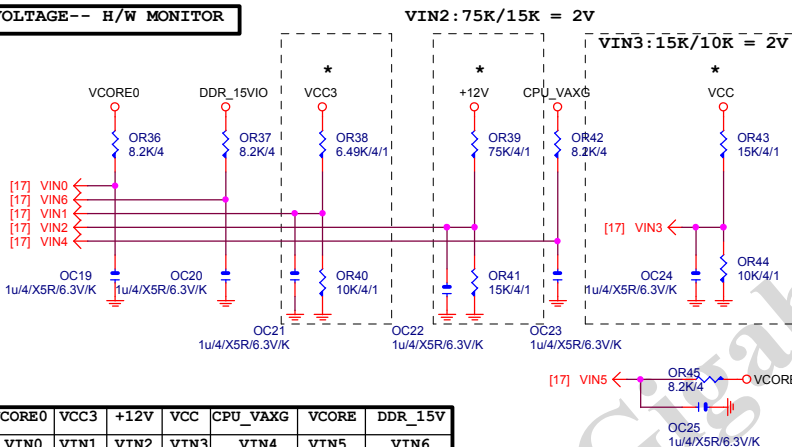
## TEMP H/W MONITOR



## CASE OPEN

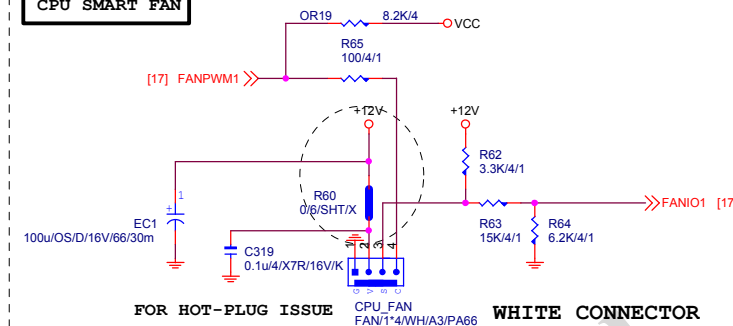


## VOLTAGE-- H/W MONITOR

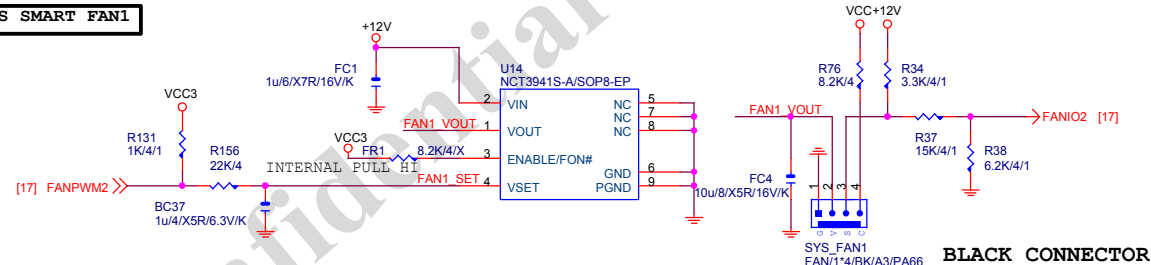


RS2 CLOSE CPU VR MOSFET  
RS2 CLOSE MOSFET (VIN) : DCQ1

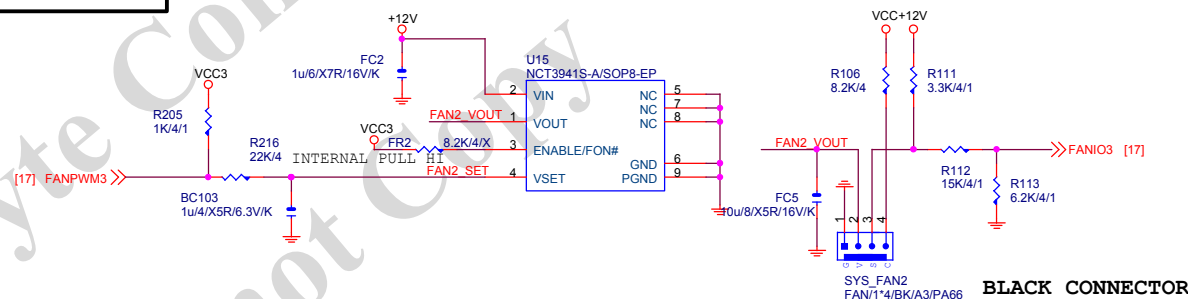
## CPU SMART FAN



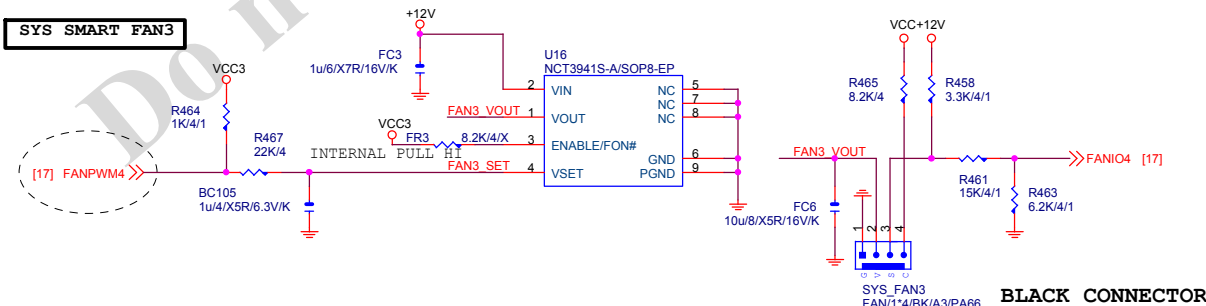
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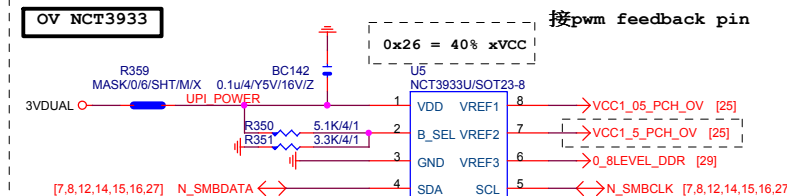
## SYS SMART FAN2



## SYS SMART FAN3

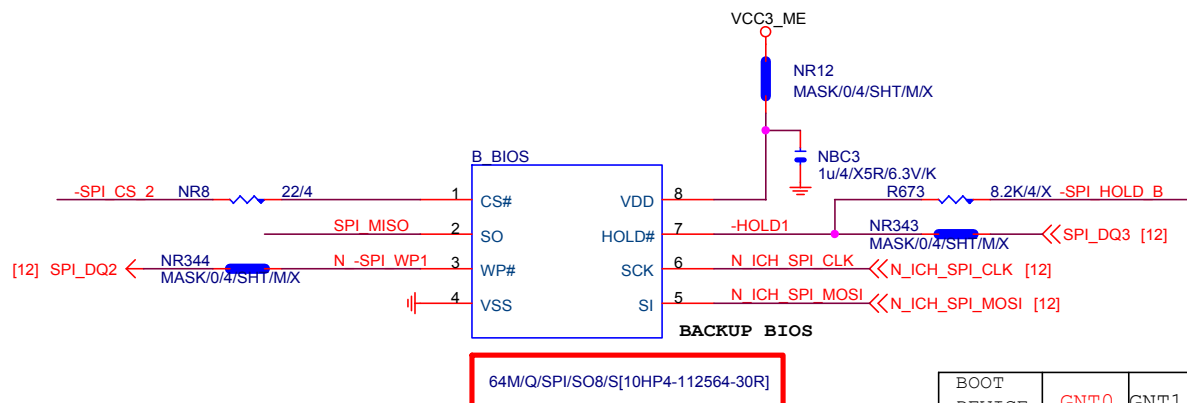
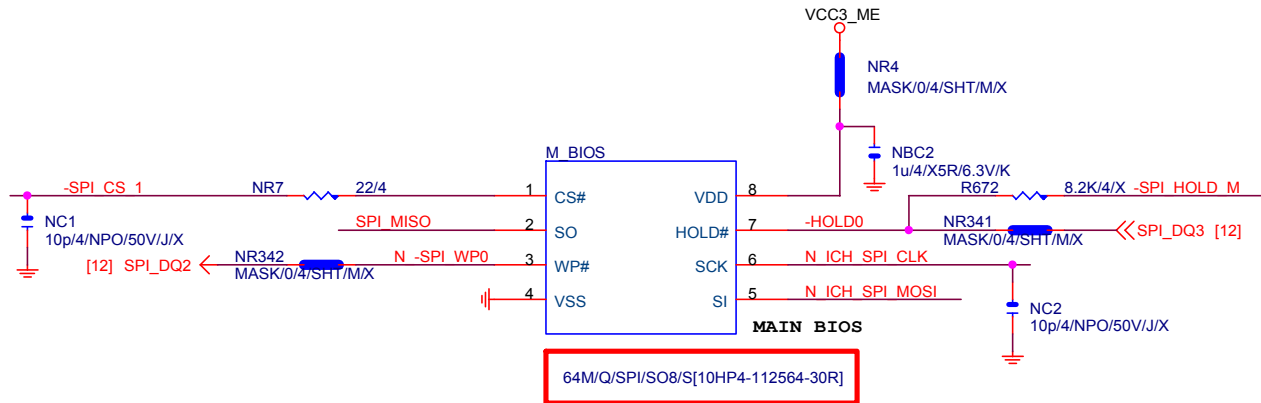


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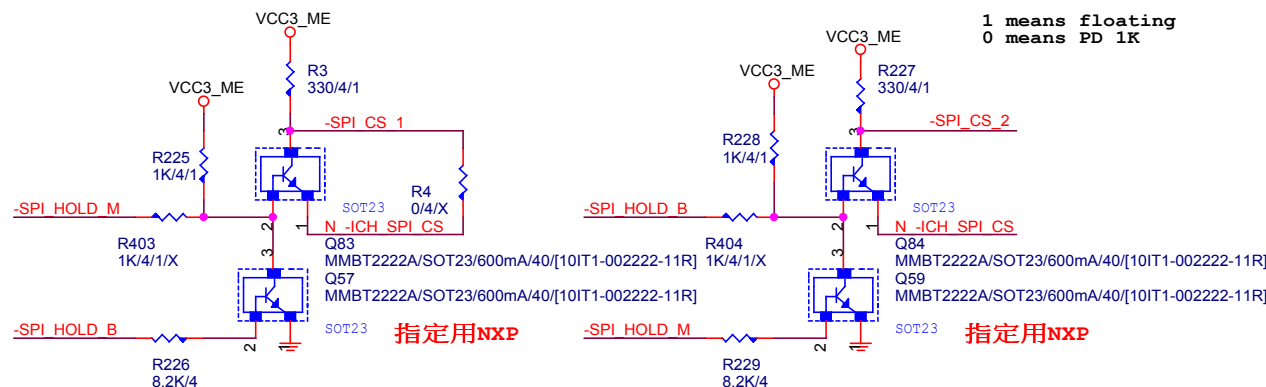
Gigabyte Technology

<b>Gigabyte Technology</b>				
Title				
HWM,FAN CTRL,OV				
Size	Document Number			Rev
Custom	GA-H97M-D3H			1.0
Date:	Mondav, April 28, 2014		Sheet	19 of 32



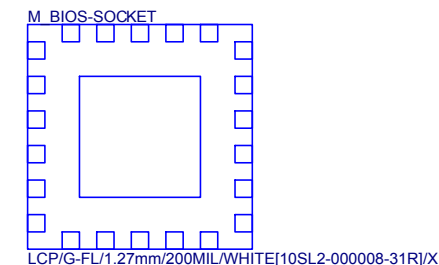
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating  
0 means PD 1K

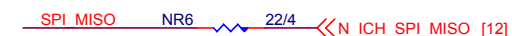
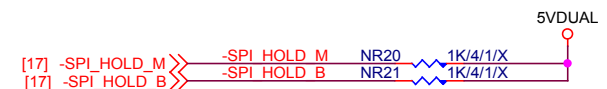
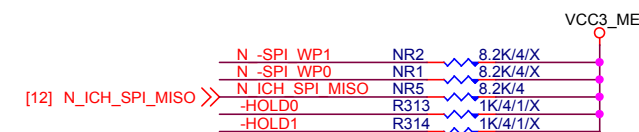
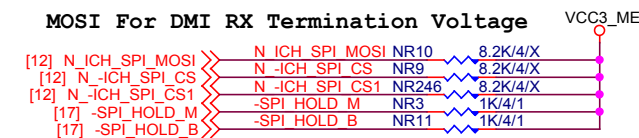


## BIOS DEBUG PORT

BIOS\_PH R1.0 移除



### MOSI For DMI RX Termination Voltage



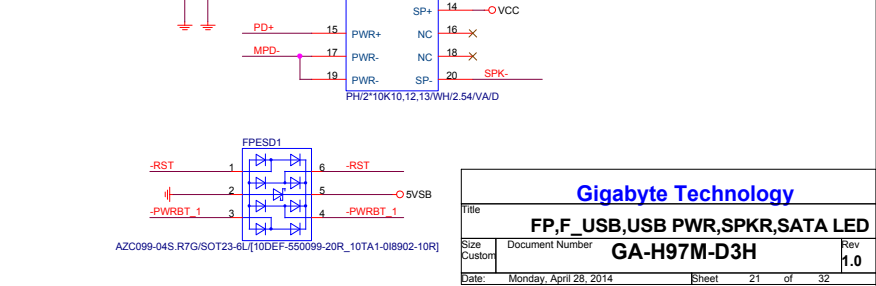
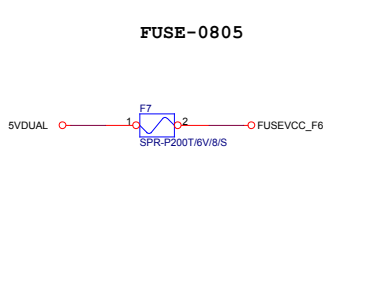
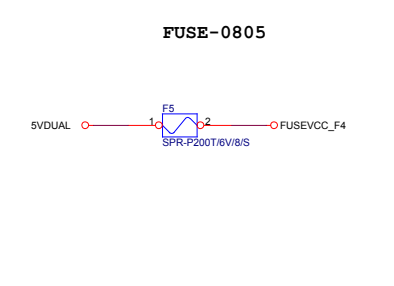
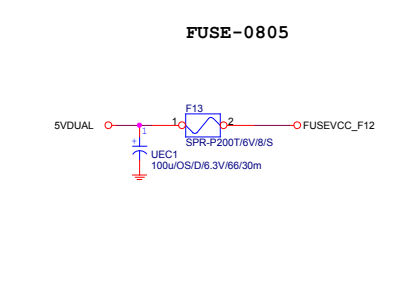
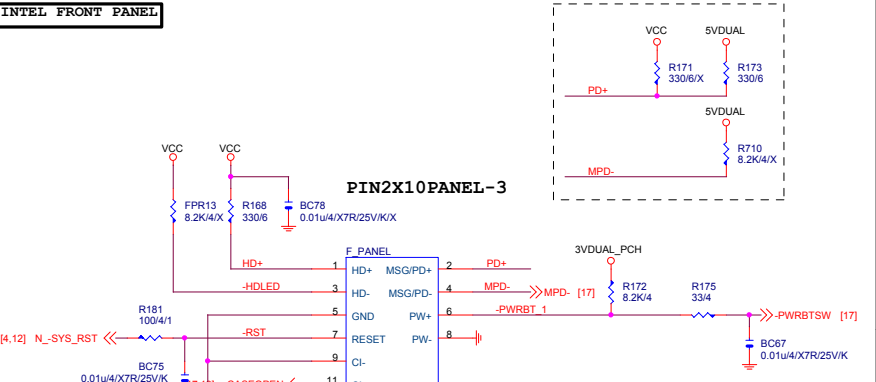
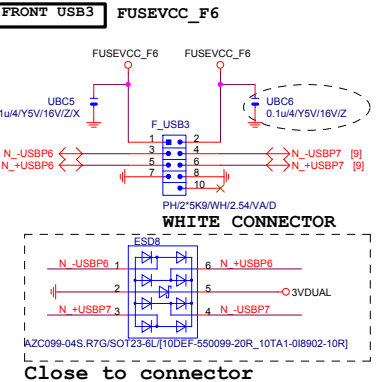
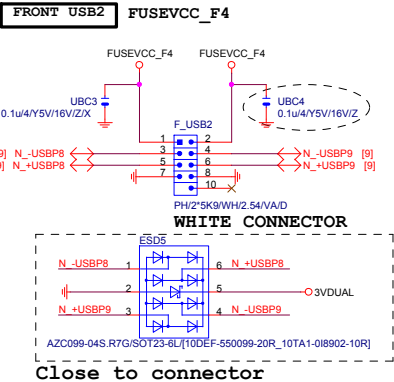
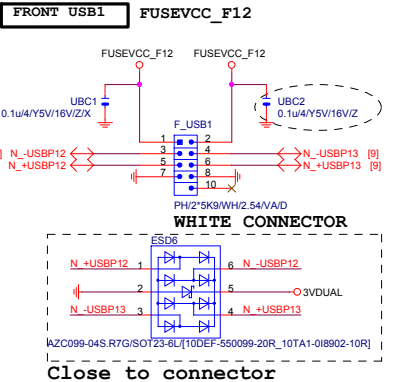
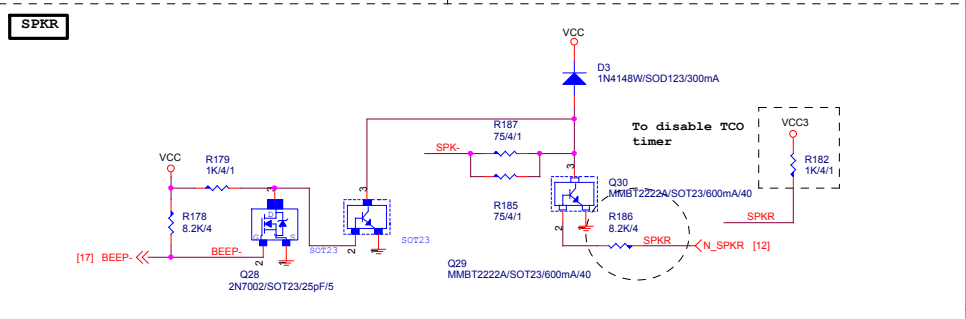
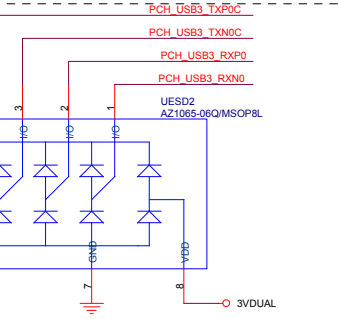
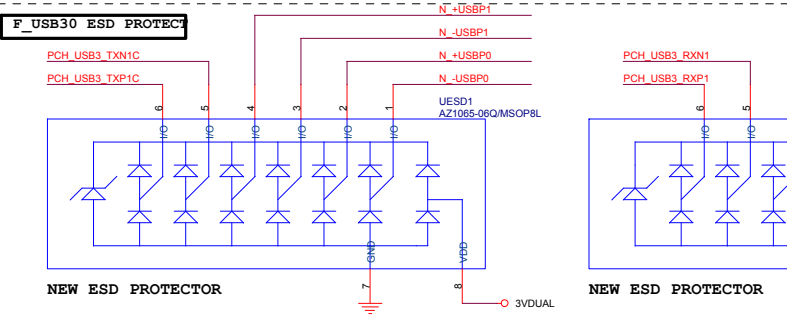
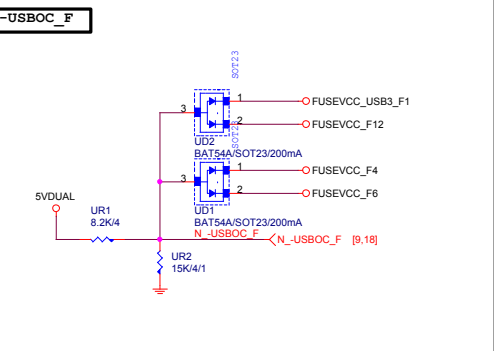
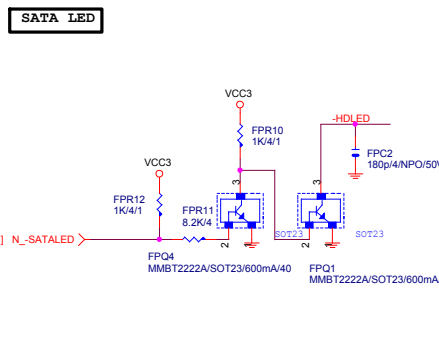
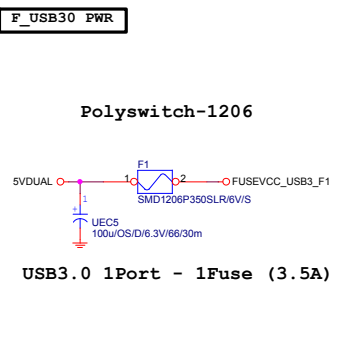
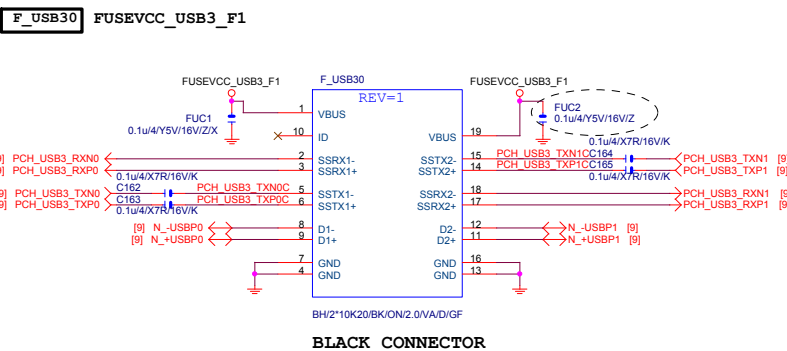
**Gigabyte Technology**

**DUAL BIOS**

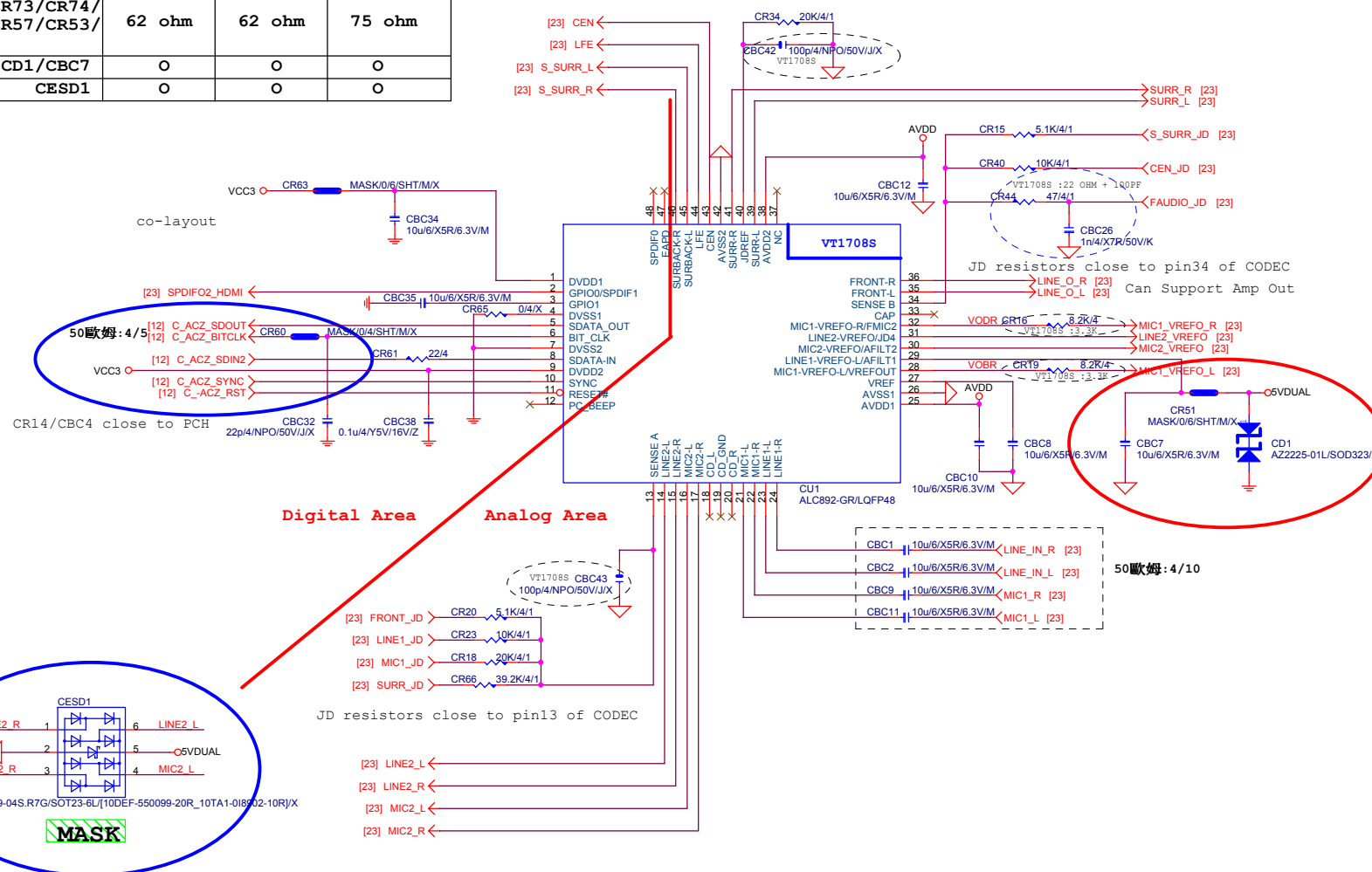
**GA-H97M-D3H**

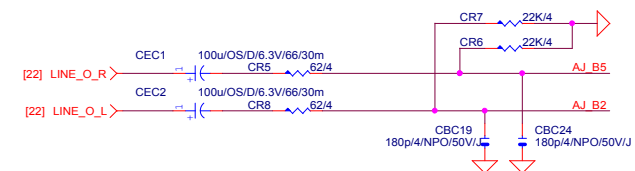
Title	Document Number	Rev
Size Custom		1.0
Date: Monday, April 28, 2014	Sheet 20 of 32	





	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O

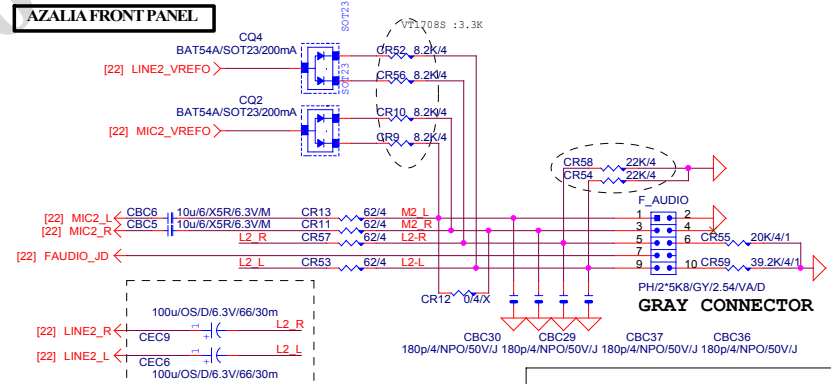
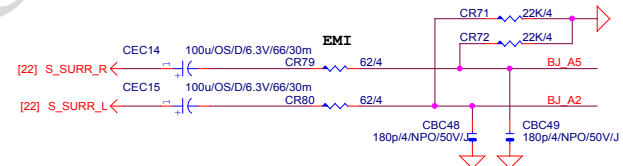
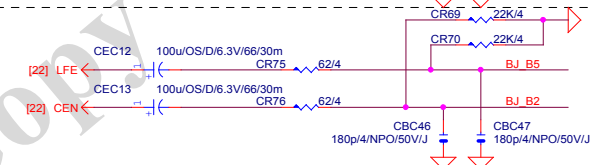
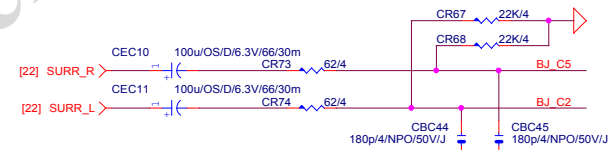
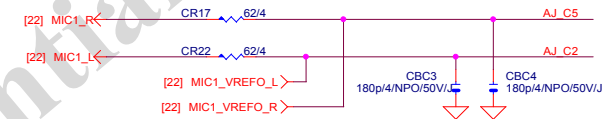




Only reserved for ALC888



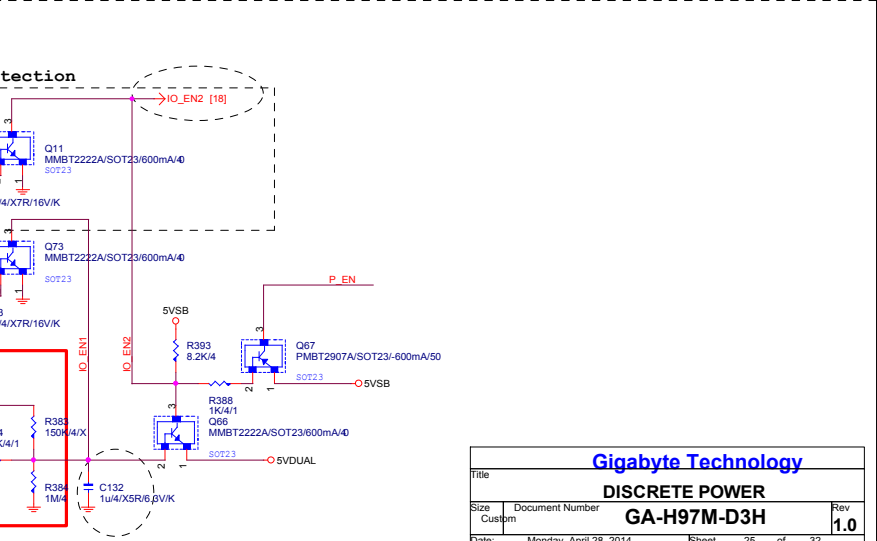
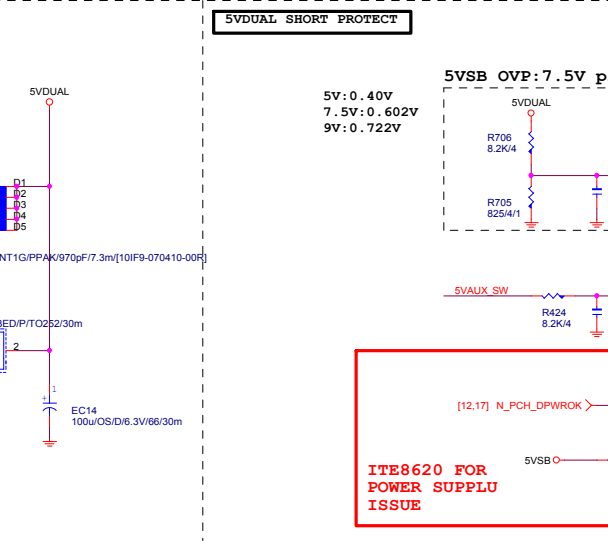
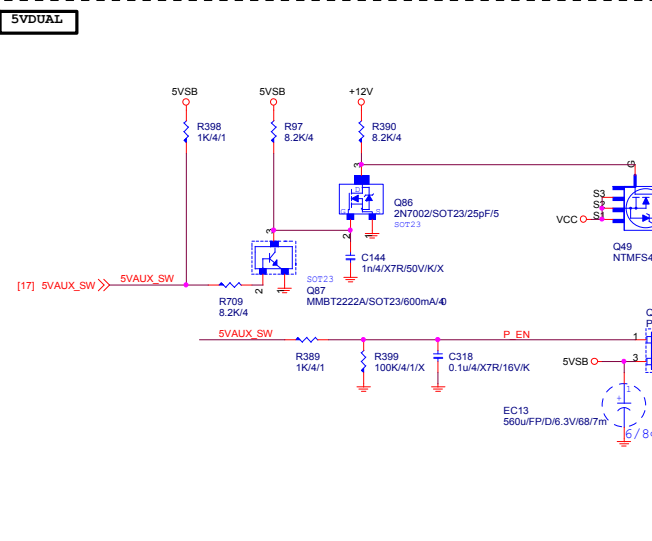
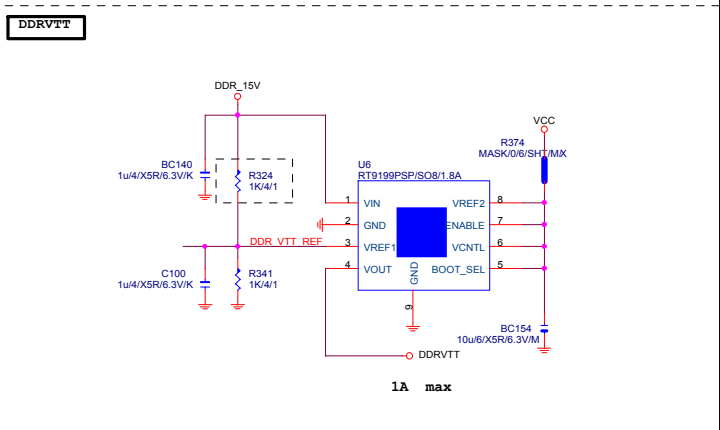
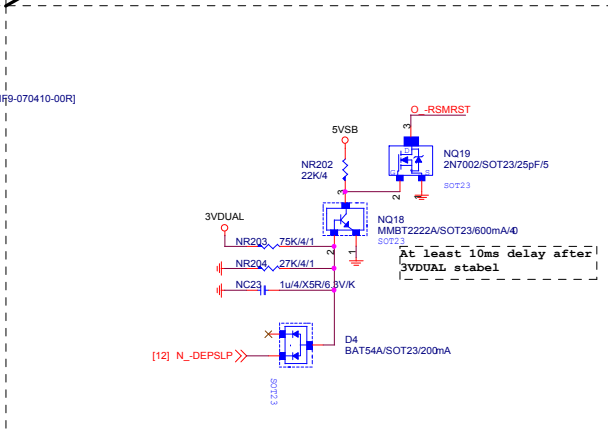
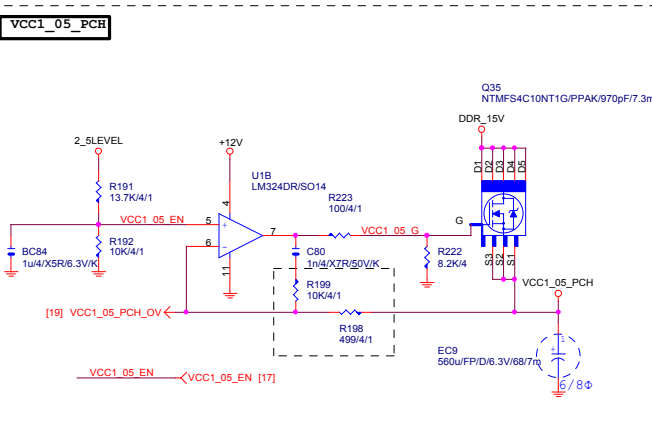
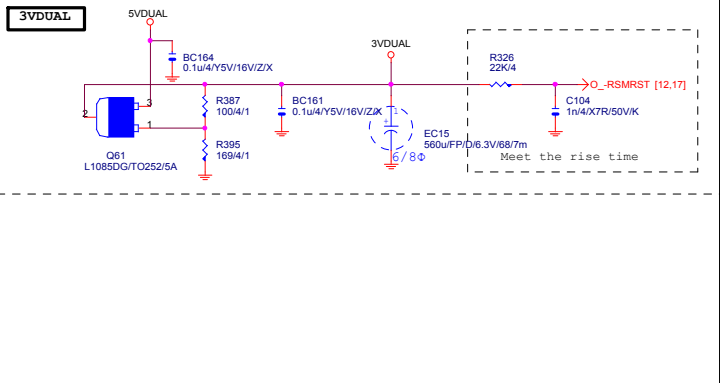
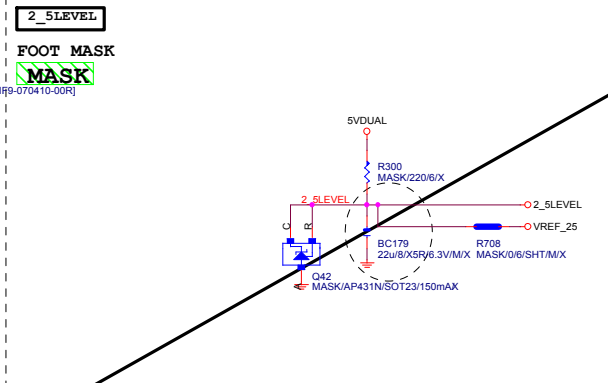
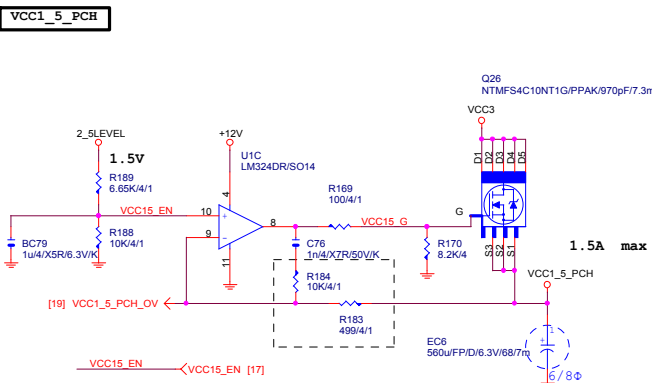
For 889A/888



## Gigabyte Technology

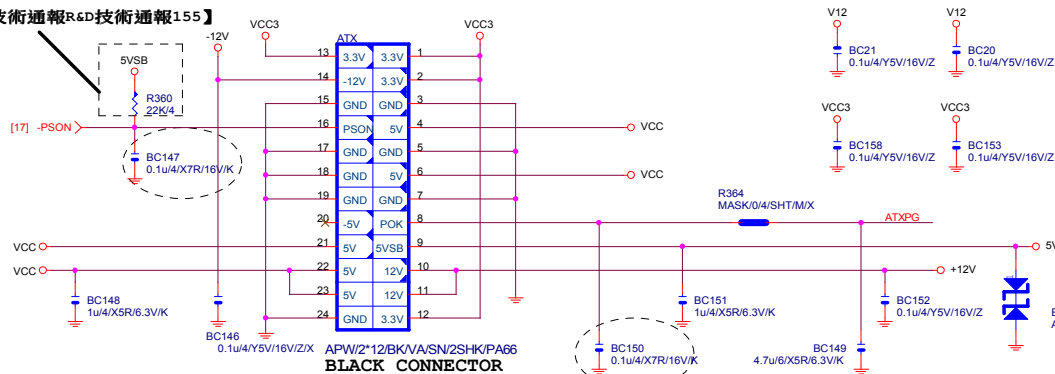
Title			
AUDIO JACK			
Size	Document Number		Rev
Custom	GA-H97M-D3H		1.0
Date:	Monday, April 28, 2014	Sheet	23 of 32





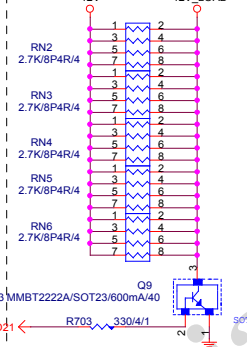
# ATXX24 POWER CONNECTOR

【技術通報R&D技術通報155】



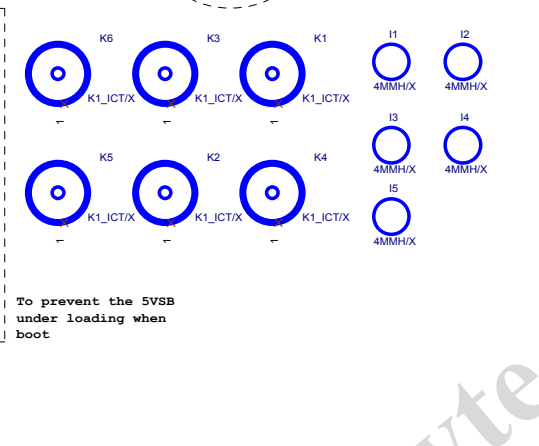
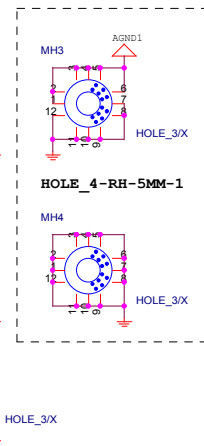
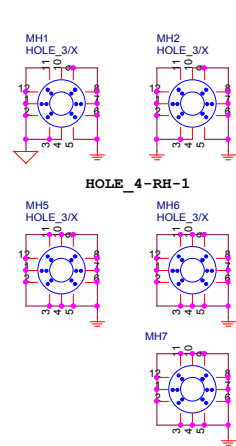
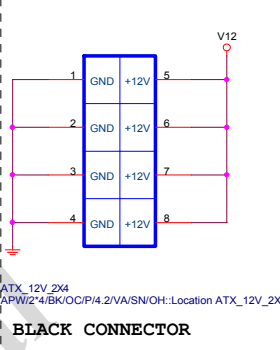
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

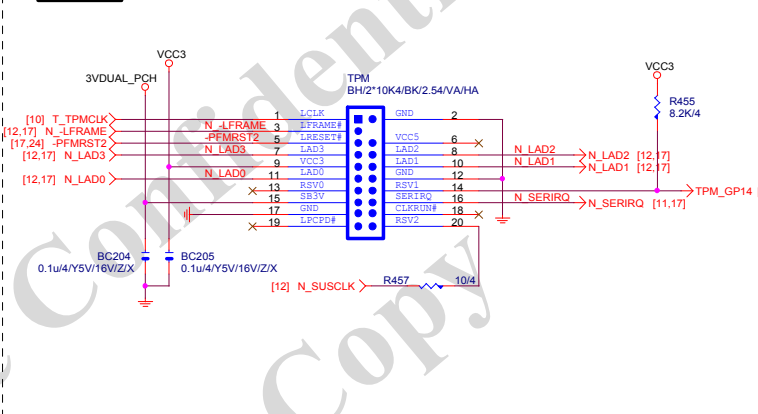


# ATXX4 POWER CONNECTOR

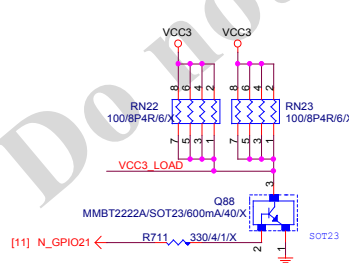
【技術通報R&D技術通報154】



## TPM

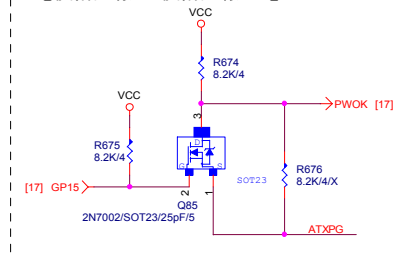


## FIX PWR MINMUN LOAD



## PWOK PATCH

【技術通報R&D技術通報154】



Gigabyte Technology

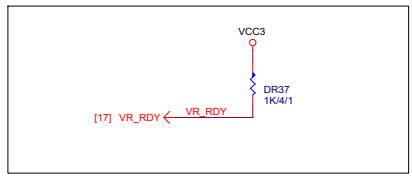
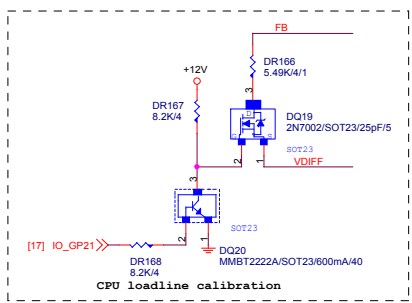
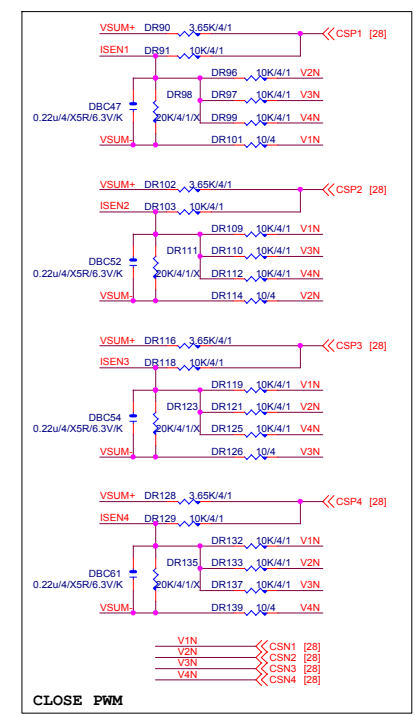
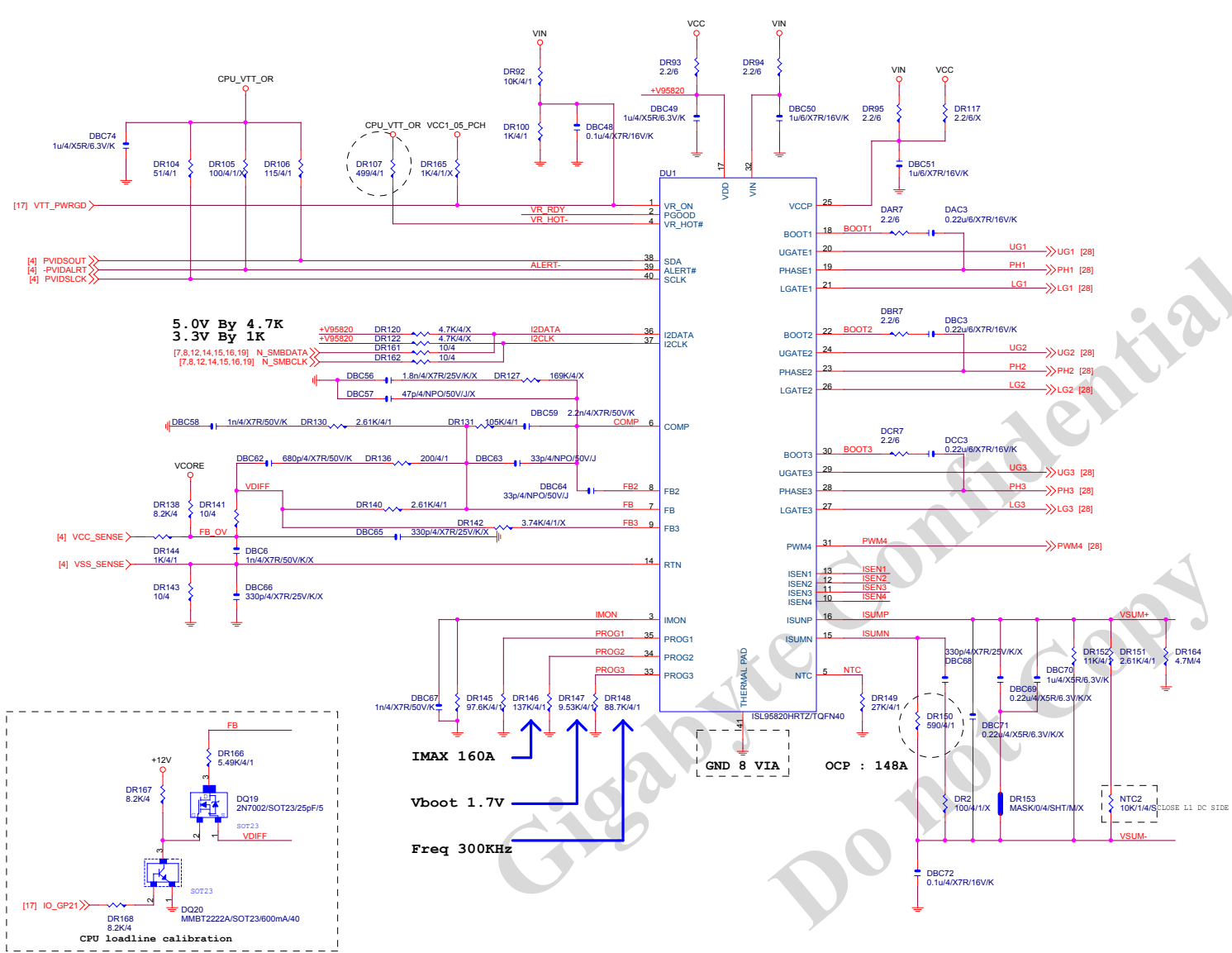
ATX CONNECTOR

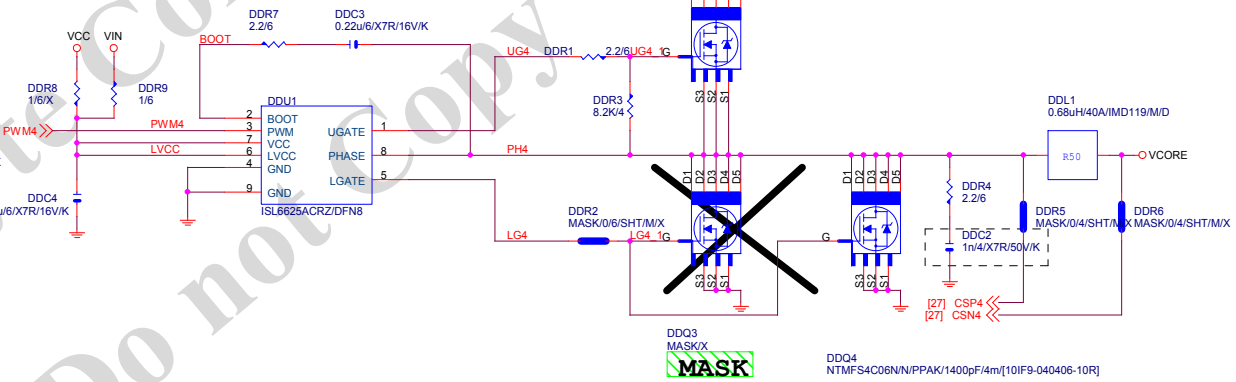
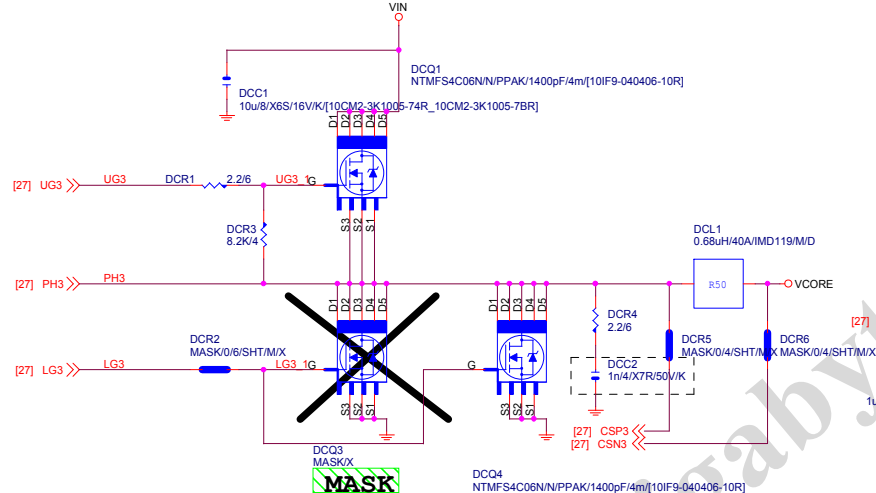
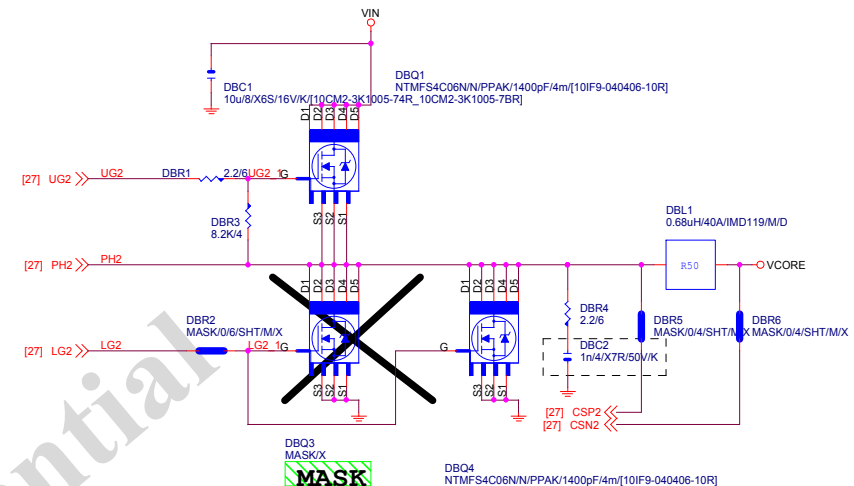
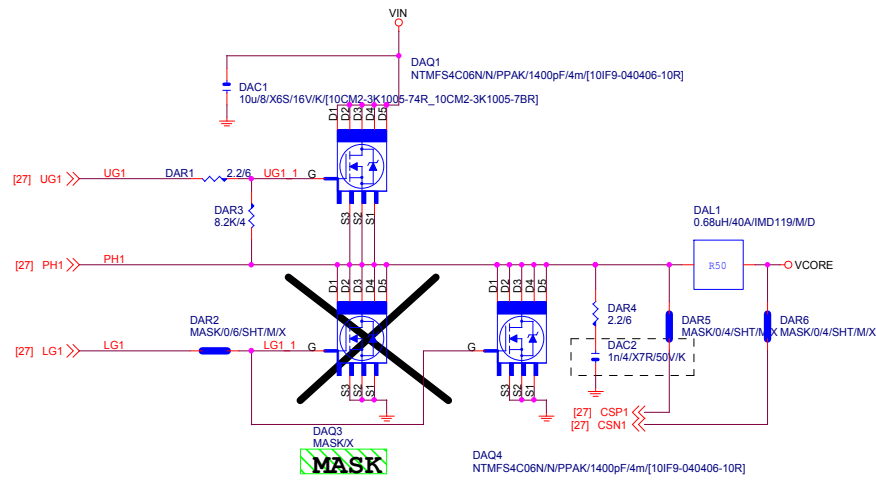
GA-H97M-D3H

Rev 1.0

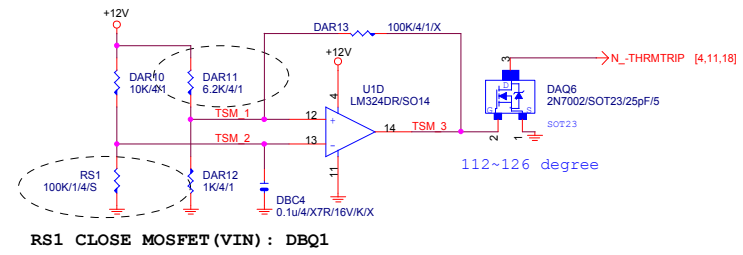
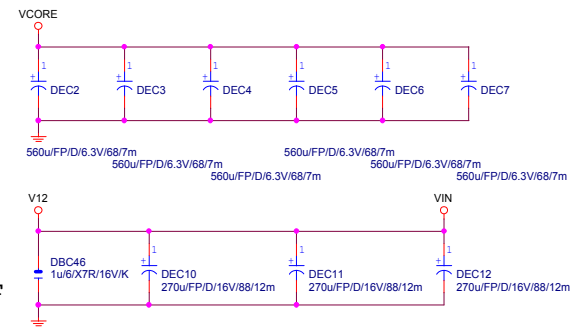
Date: Monday, April 28, 2014 Sheet 26 of 32







MOS\_HS  
9 SERIES MOS HS[12SP2-S07920-11R\_12SP2-S07920-12R\_12SP2-S07920-13R]



RS1 CLOSE MOSFET (VIN) : DBQ1

9 Series MOS Heatsink (Screw fix)

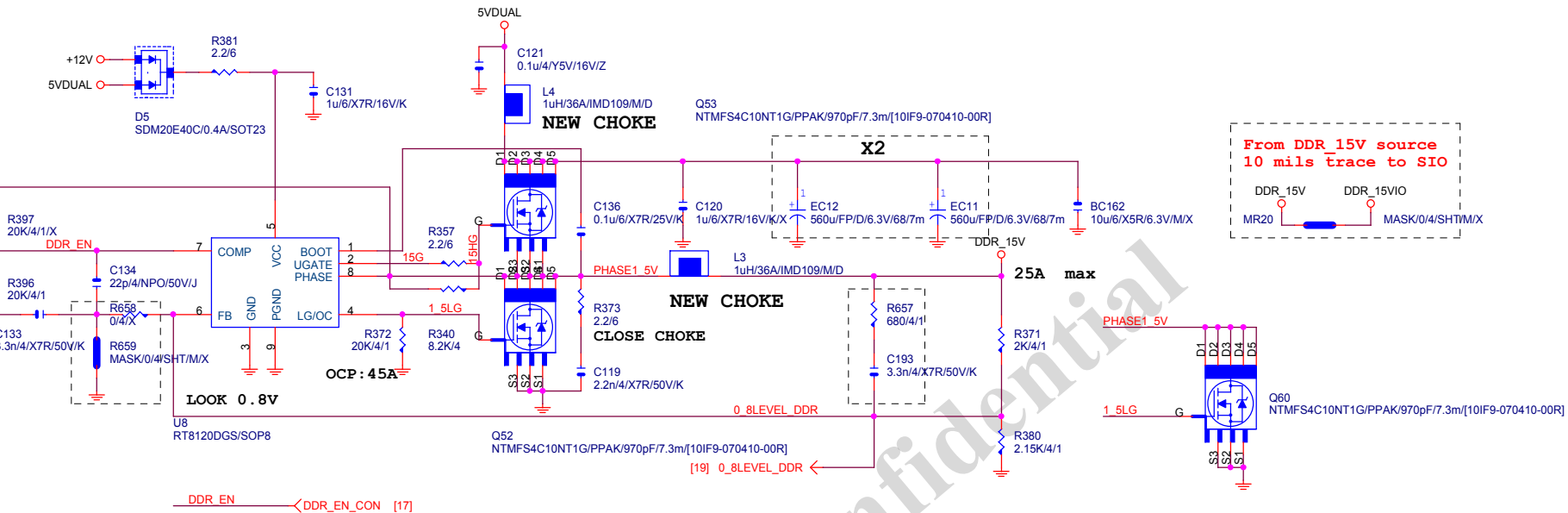
MOSHSINK-Z97X-SLI

H97 MODEL: 一上一下, DAQ3, DBQ3, DCQ3, DDQ3 MASK FOOTPRINT

Gigabyte Technology

Title			CPU CORE VR-2
Size			GA-H97M-D3H
Date			Monday, April 28, 2014
Sheet			28 of 32

DDR15V



PWR SEQ

VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1  
IRMS=11.45A  
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
Coefficient=1.7(85°C), 1(105°C)  
VIN Ripple current=4.7X1.7=7.99A(85°C)  
-->故固態電容須2X7.99=15.98>11.45A

$$\begin{aligned} \text{Rocset} &= (\text{Iocp} * \text{Lgate}, \text{rdson}) / \text{Iocset} \\ \text{Rocset} &= (45\text{A} * 6.7\text{mOhm}) / 10\text{uA} = 30\text{K} \\ \text{Iocset} &= 10\text{uA} \end{aligned}$$

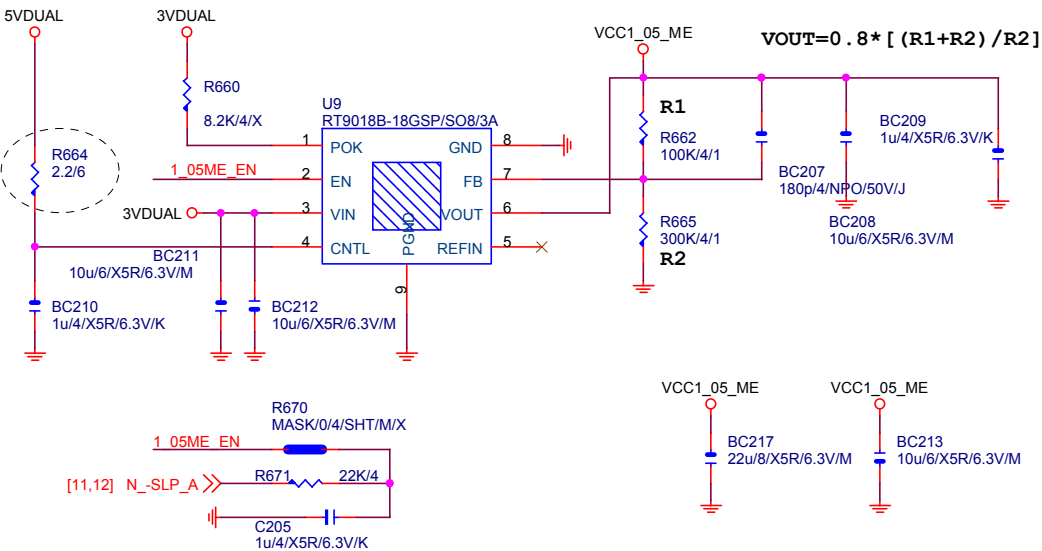
<b><i>Gigabyte Technology</i></b>			
Title			
<b>DDR POWER</b>			
Size Custom	Document Number	<b>GA-H97M-D3H</b>	Rev 1.0
Date:	Monday, April 28, 2014	Sheet 29 of 32	

VCC1\_05\_ME

Z97 N/A

## 【技術通報R&amp;D技術通報156】

(RICHTER), (NUVOTON), (EMC) 做共用  
PIN7分壓阻值須做修改為100K以上電阻值



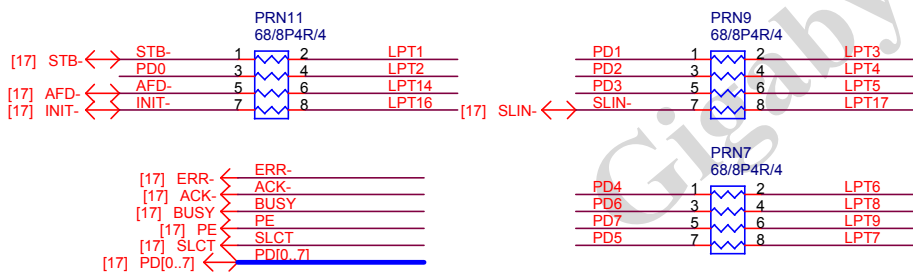
Second source

EM5103 - 10GL2-305103-01R

NCT3730S -

10GL2-303730-01R

LPT PORT

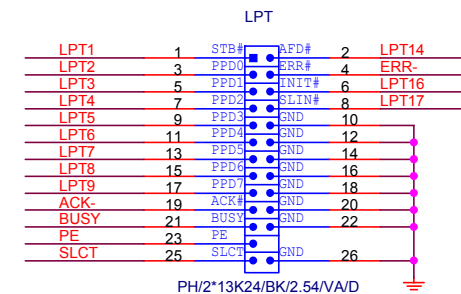
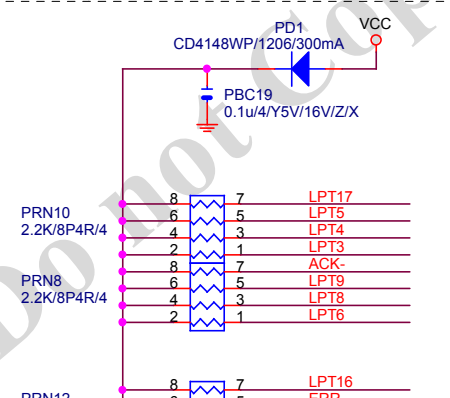
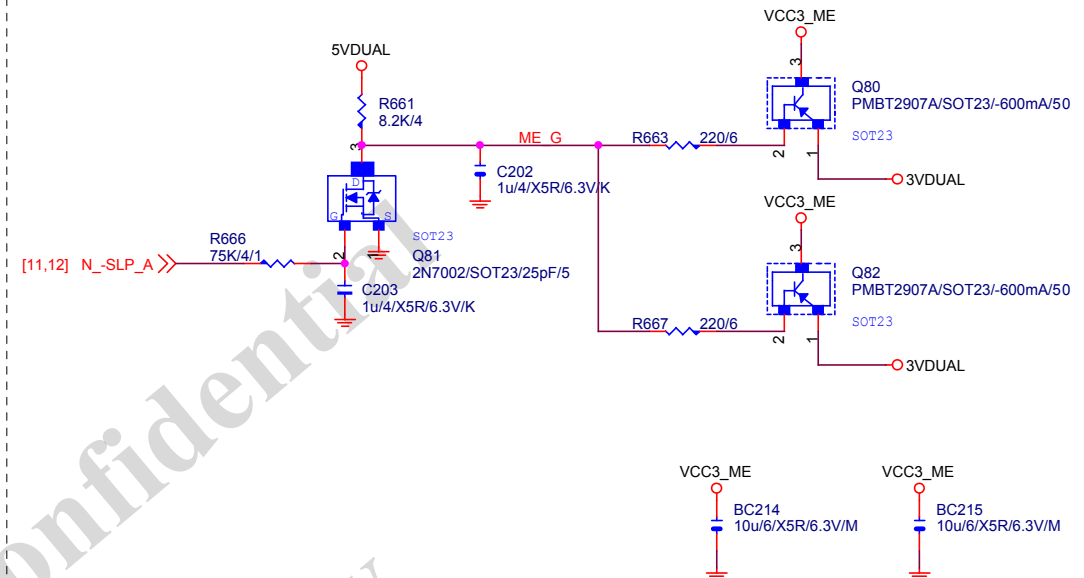


## 【技術通報R&amp;D技術通報151】

33ohm Change to 68ohm

VCC3\_ME

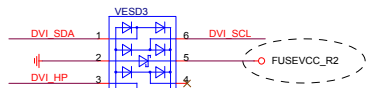
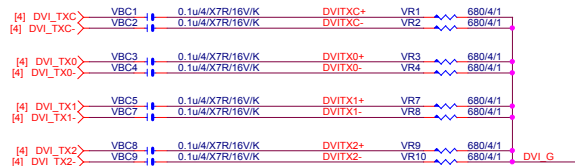
Z97 N/A



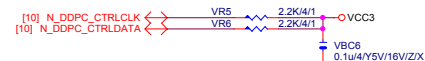
Gigabyte Technology

Title			
LPT			
Size Custom	Document Number		Rev
	GA-H97M-D3H		1.0
Date:	Monday, April 28, 2014	Sheet	30 of 32

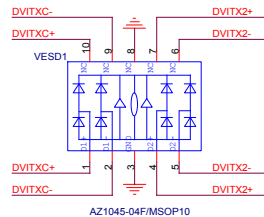
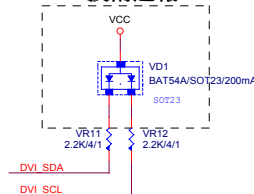
# DVI LEVEL SHIFT



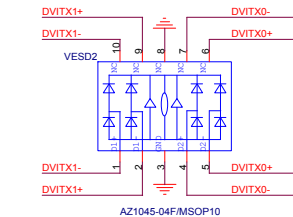
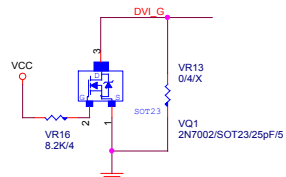
Close to connector



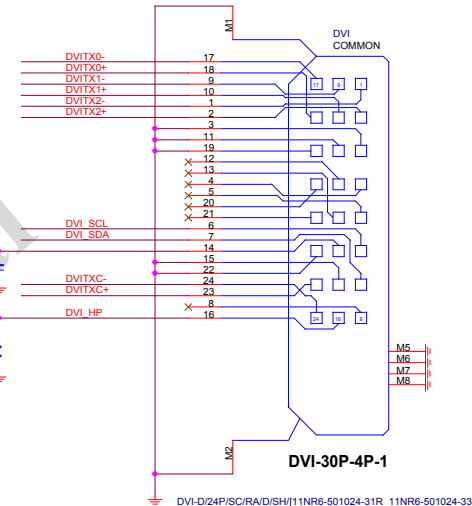
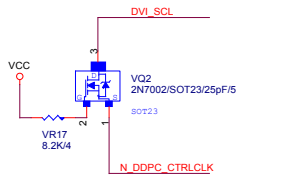
R&D技術通報 162



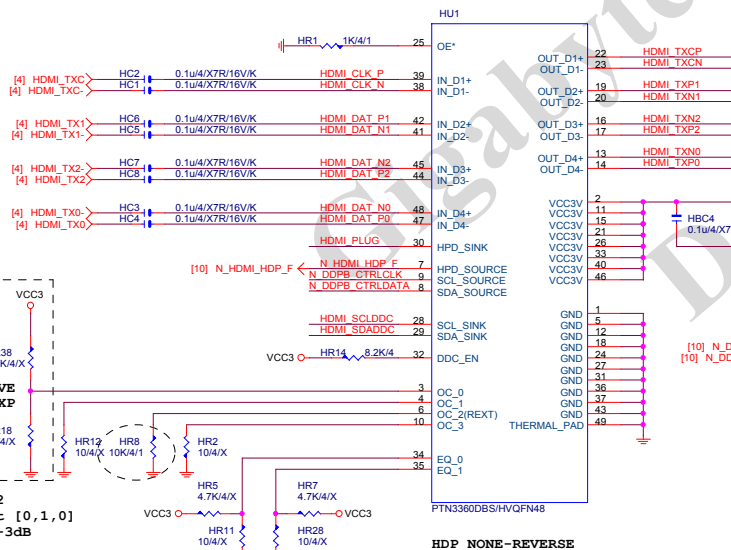
Close to connector



Close to connector

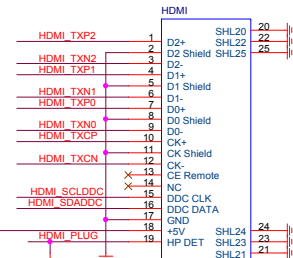
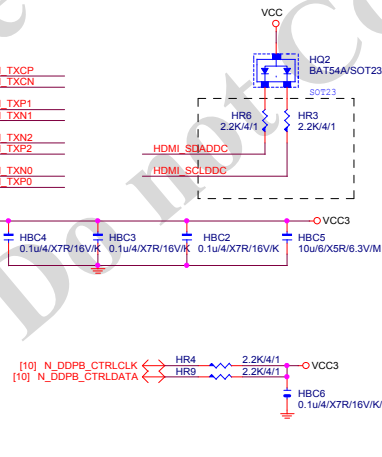


# HDMI LEVEL SHIFT



AS1442  
Default [0,1,0]  
450mv, -3dB

AS1442 Default [0,0] 3dB  
[0,1] 6dB



HDMI-3

HDMI[11NR6-H01019-91R\_11NR6-H01019-93R]

Gigabyte Technology		
DVI		
Size Custom	Document Number	GA-H97M-D3H
Date: Monday, April 28, 2014	Sheet 31 of 32	Rev 1.0

