Project Name :GK5KN6Z

Platform : CFL_H+N17E-G1

PAGE CONTENT

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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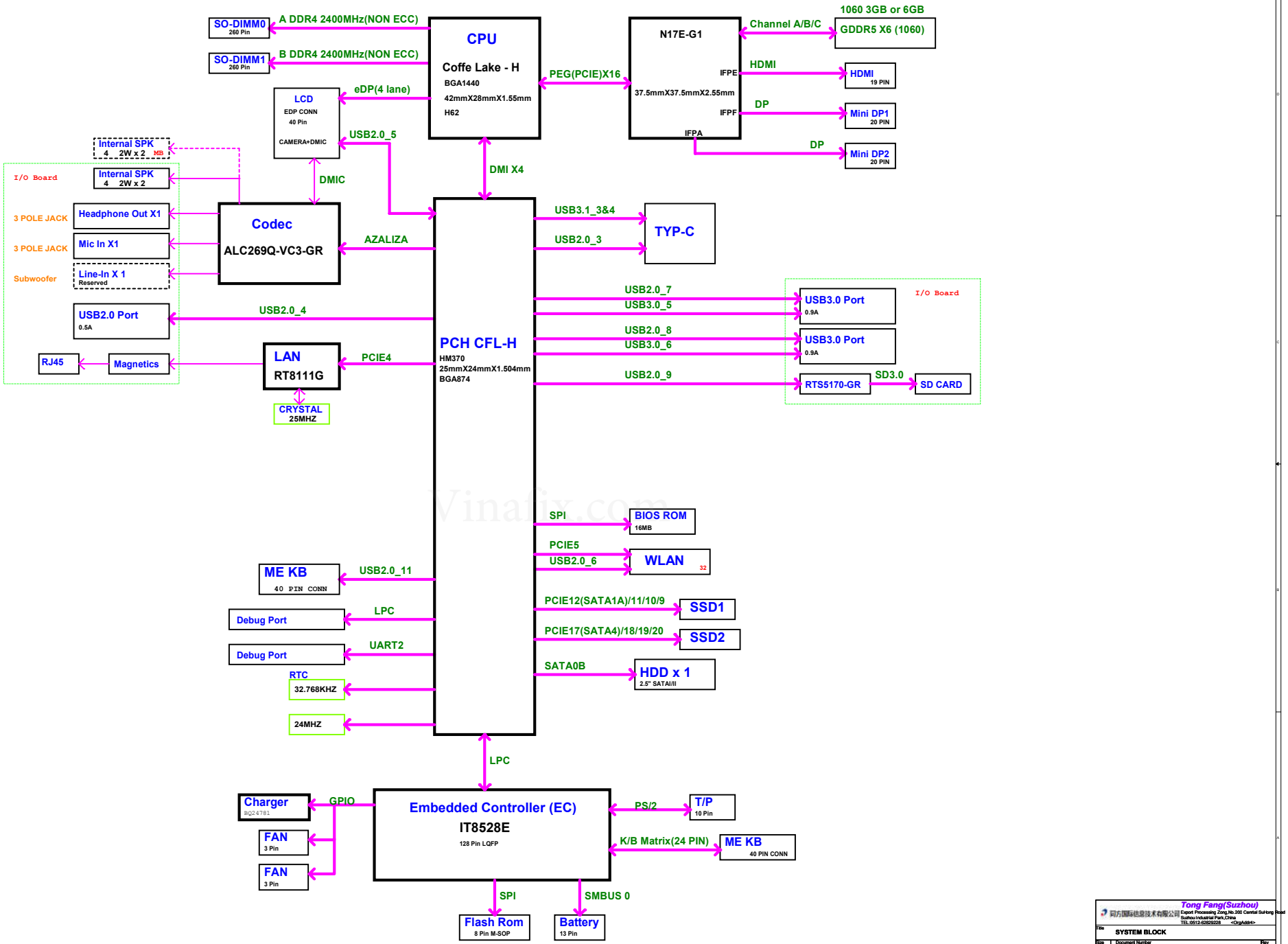
Title	INDEX	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 1 of 72	

SYSTEM BLOCK DIAGRAM



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Title
SYSTEM BLOCK
Size Custom
Document Number GK8CN6X
Rev V.A
Date: Tuesday, January 16, 2018 Sheet 2 of 72

POWER ON SEQUENCE

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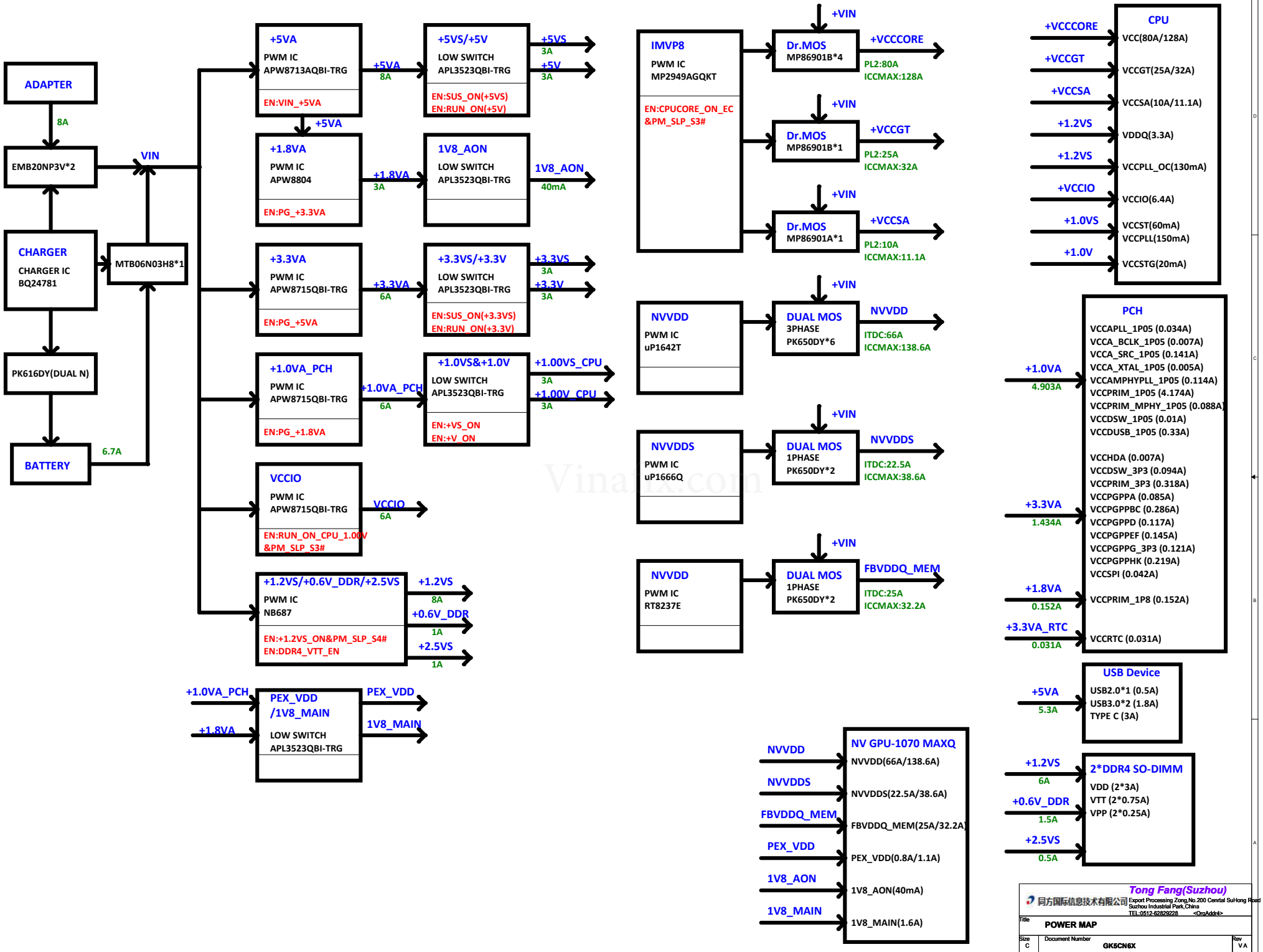
Title: POWER DIAGRAM & SEQUENCE

Size	Document Number	Rev
Custom	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 3 of 72



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Title	POWER MAP	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 4 of 72	

GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1 CHG_R_LED	
GPA5	PID_2 PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

GH5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	ME_KB_LED	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	EG_DA	
GPE2	EG_Cycle start	
GPE3	EG_CLK	
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	PANEL_VCC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC removal	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3		Dn/GPI/ID3
GPH4		Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6		Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	PANEL_DETECT	/GPI/Z
GPI2	PCIE_WAKE#	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

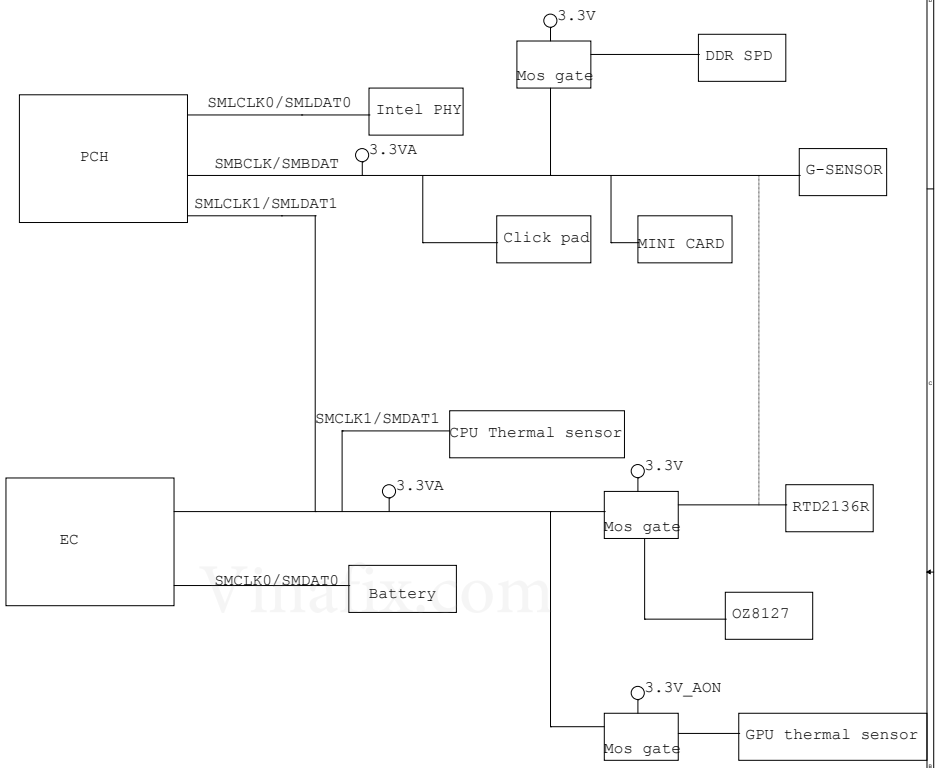
GI5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	PM_RSMRST#	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPI
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	DGPU_EN_EC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC removal	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON/SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3	DGPU_EN_EC_Keep	Dn/GPI/ID3
GPH4	Dgpu_RST_EC#	Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6	Clear CMOS	Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	EC_OVERT_NVVDD#	/GPI/Z
GPI2	PCIE_WAKE#/Dgpu_RST_EC#_keep	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

EXT EC

ITE8302 GPIO		Default Pull/Mode
GPIO4	EXT_WIFI_ON	UP / GPO
GPIO5	EC_OVERT_NVVDD#	UP / GPO
GPIO7	Dgpu_RST_EC#_keep	UP / GPO
GPIO9	SUS_ON	UP / GPO
GPIO11	CTL3	UP / GPO
GPIO13	CTL2	UP / GPO
GPIO18	EXT_Q_key0	UP / GPO
GPIO20	EXT_Q_key1	UP / GPO
GPIO22	PWR_USB#	UP / GPI
GPIO24	+1.2VS_ON	UP / GPI
GPIO26	LID1#	Dn / GPI
GPIO27	Dgpu_RST_EC#	Z / GPI
GPIO29	PM_RSMRST#	Z / GPI
GPIO31	DGPU_EN_EC_Keep	Z / GPO
GPIO33	DGPU_EN_EC	UP / GPI
GPIO35	Clear CMOS	Dn / GPI

SMBUS BLOCK



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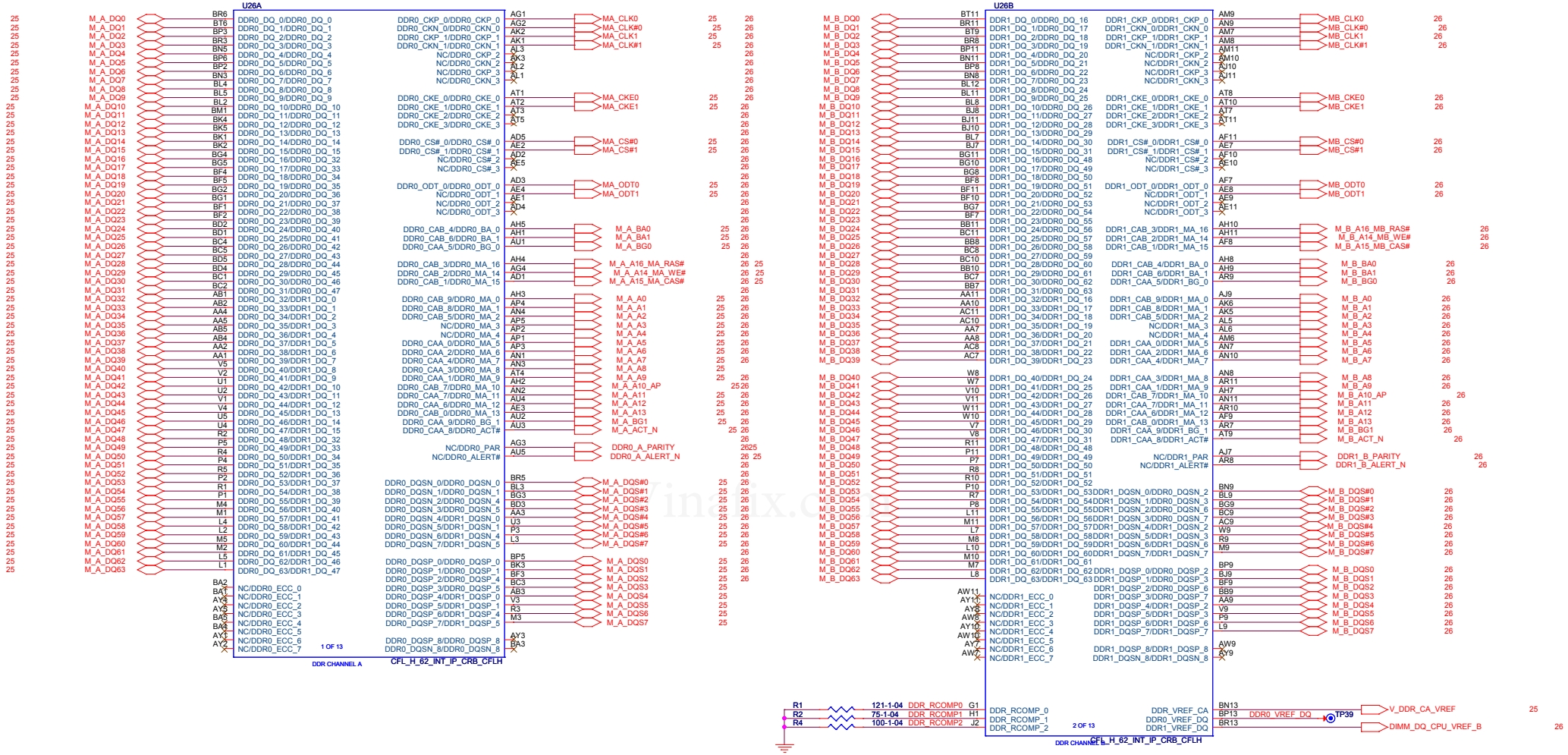
Size: Custom	Document Number: GK5CN6X		Rev: V.A
Date: Tuesday, January 16, 2018	Sheet 5 of 72		



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Size	Document Number	Rev
Custom	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 6 of 72

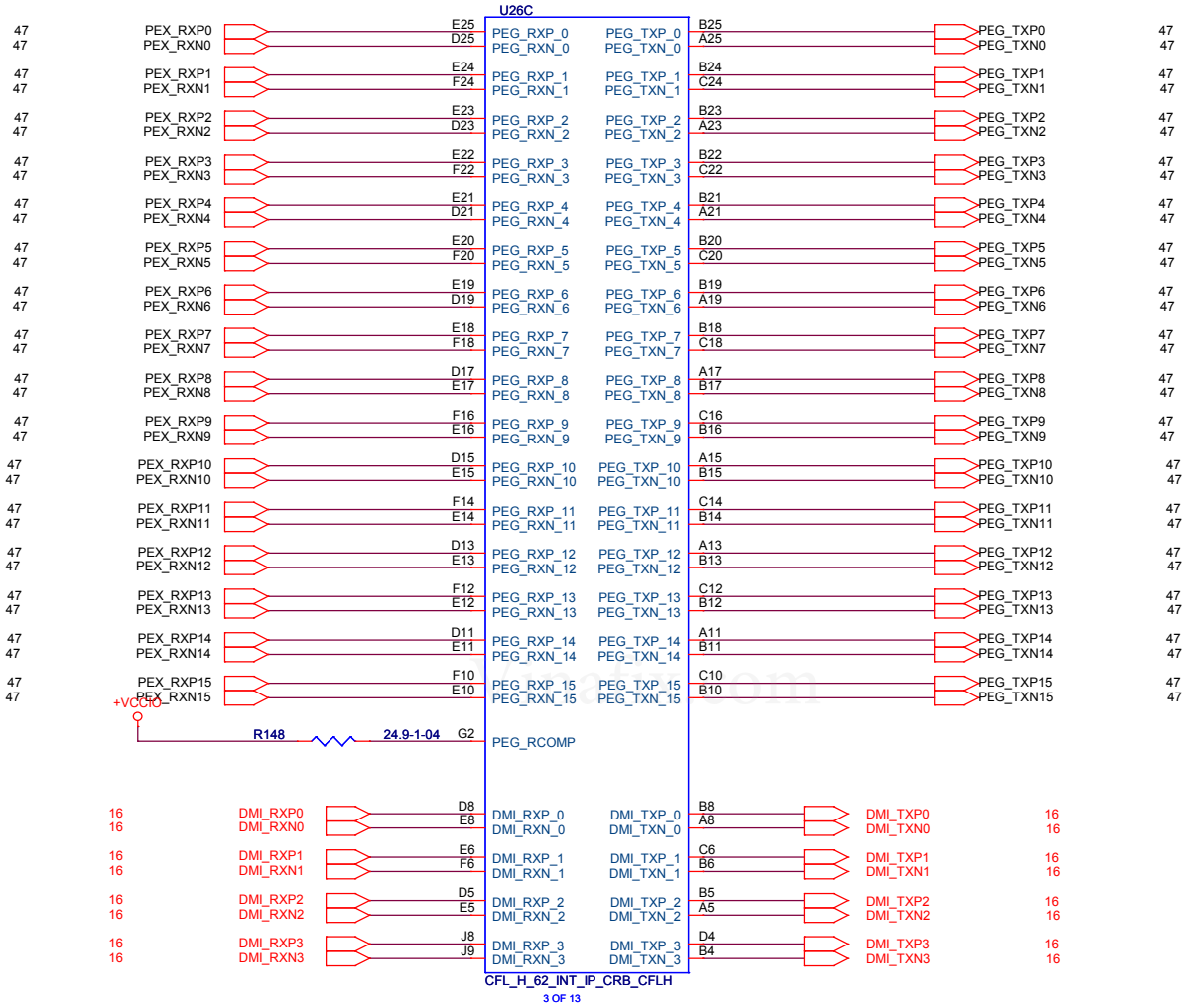

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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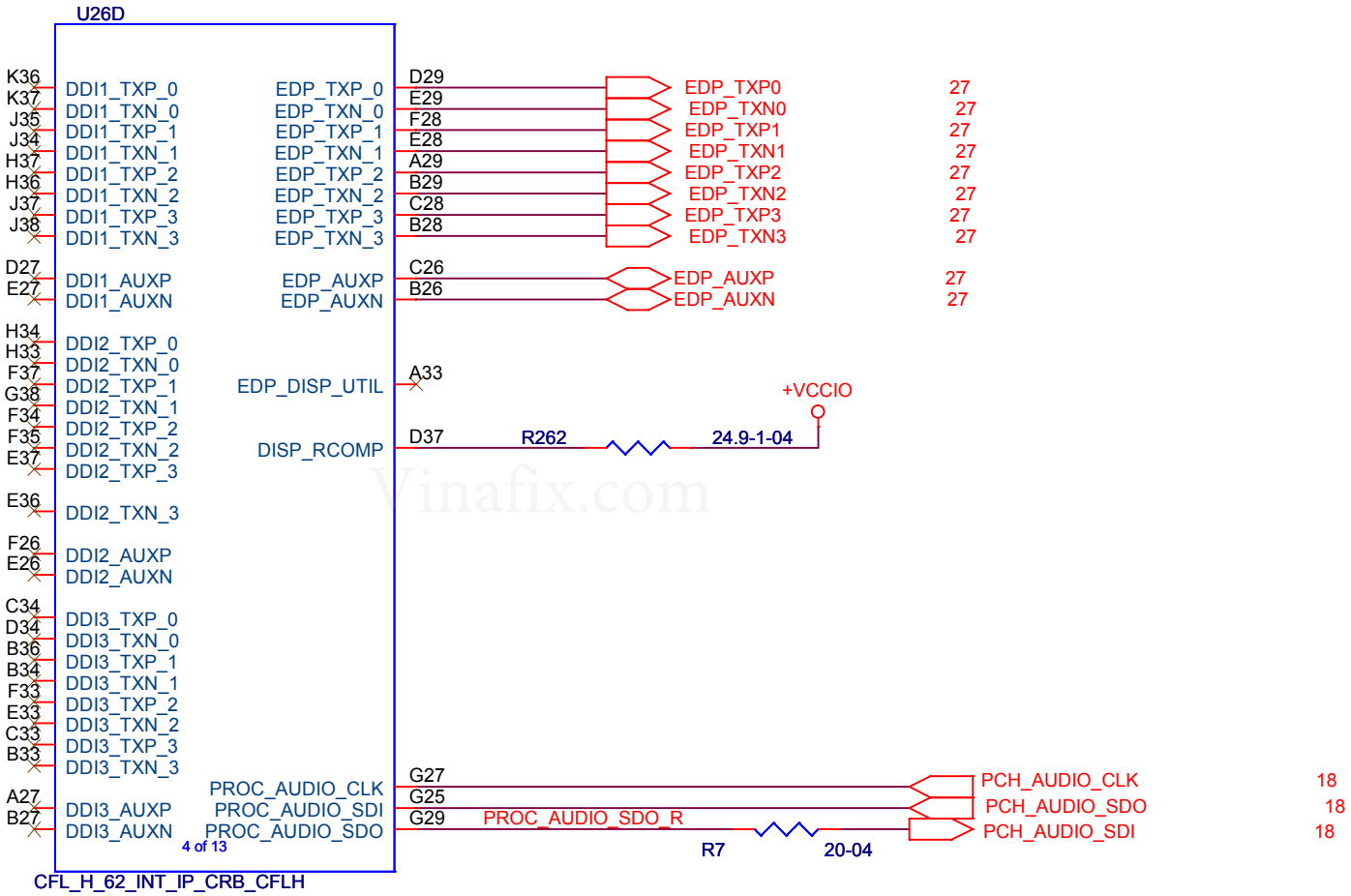
Title	CPU CFL-H : PEG/DMI	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 7 of 72	



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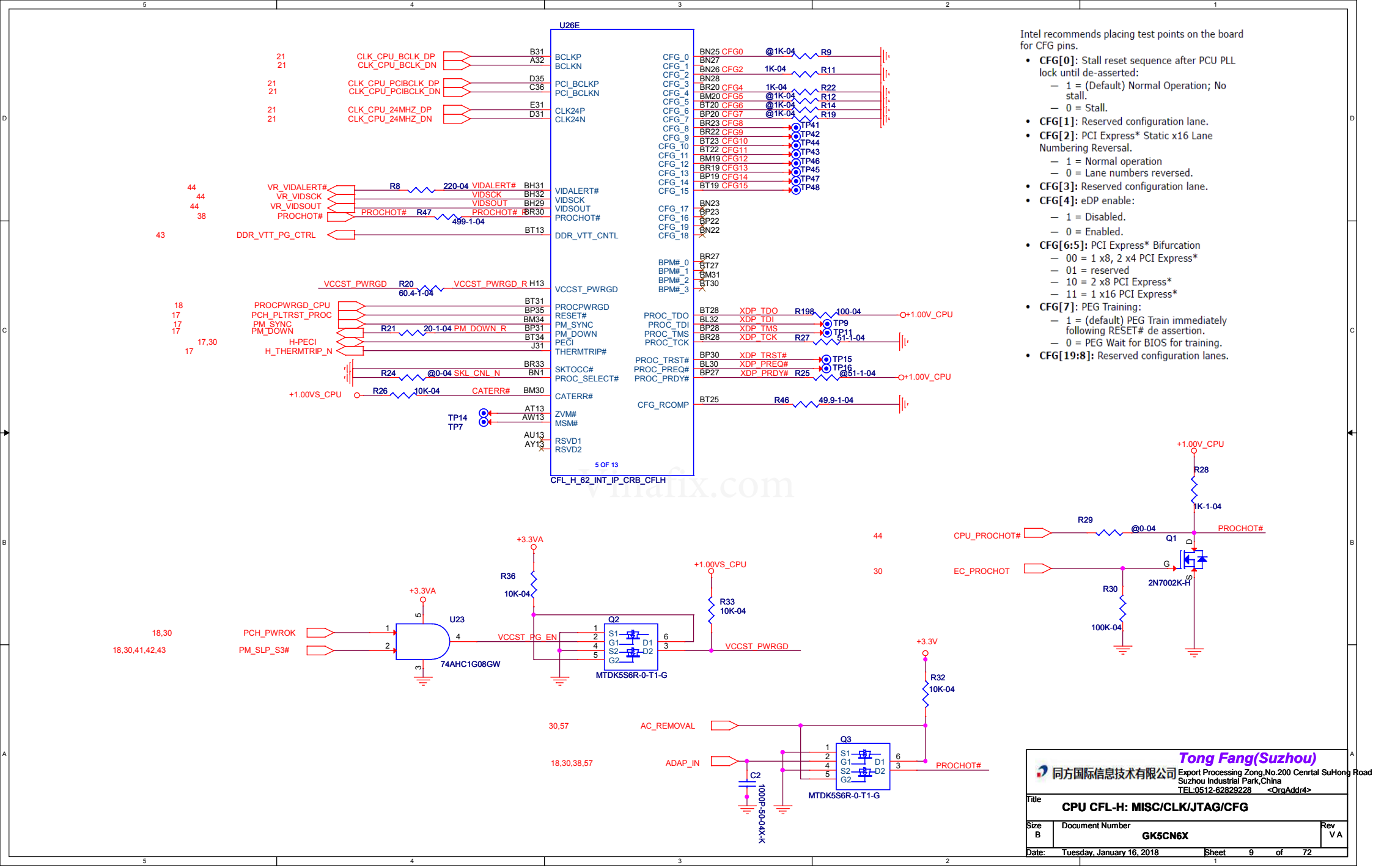
Title
CPU CFL-H : DDI/EDP

Size	Document Number	Rev
A	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 8 of 72


U26E
CFL_H_62_INT_IP_CRB_CFLH
5 OF 13
CLK_CPU_BCLK_DP
CLK_CPU_BCLK_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPU_24MHZ_DP
CLK_CPU_24MHZ_DN
VR_VIDALERT#
VR_VIDSCK
VR_VIDSOUT
PROCHOT#
DDR_VTT_PG_CTRL
VCCST_PWRGD
PROCPWRGD_CPU
PCH_PLTRST_PROC
PM_SYNC
PM_DOWN
H-PECI
H_THERMTRIP_N
+1.00VS_CPU
CATERR#
TP14
TP7
SKL_CNL_N
Intel recommends placing test points on the board for CFG pins.
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
1 = (Default) Normal Operation; No stall.
0 = Stall.
CFG[1]: Reserved configuration lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.
CFG[19:8]: Reserved configuration lanes.
XDP_TDO
XDP_TDI
XDP_TMS
XDP_TCK
XDP_TRST#
XDP_PREQ#
XDP_PRDY#
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
CFG_RCOMP
+1.00V_CPU
+3.3VA
+3.3V
U23
74AHC1G08GW
PCH_PWROK
PM_SLP_S3#
VCCST_PG_EN
VCCST_PWRGD
Q2
MTDK5S6R-0-T1-G
Q3
AC_REMOVAL
ADAP_IN
C2
1000P-50-04X-K
CPU_PROCHOT#
EC_PROCHOT
Q1
2N7002K-H
PROCHOT#
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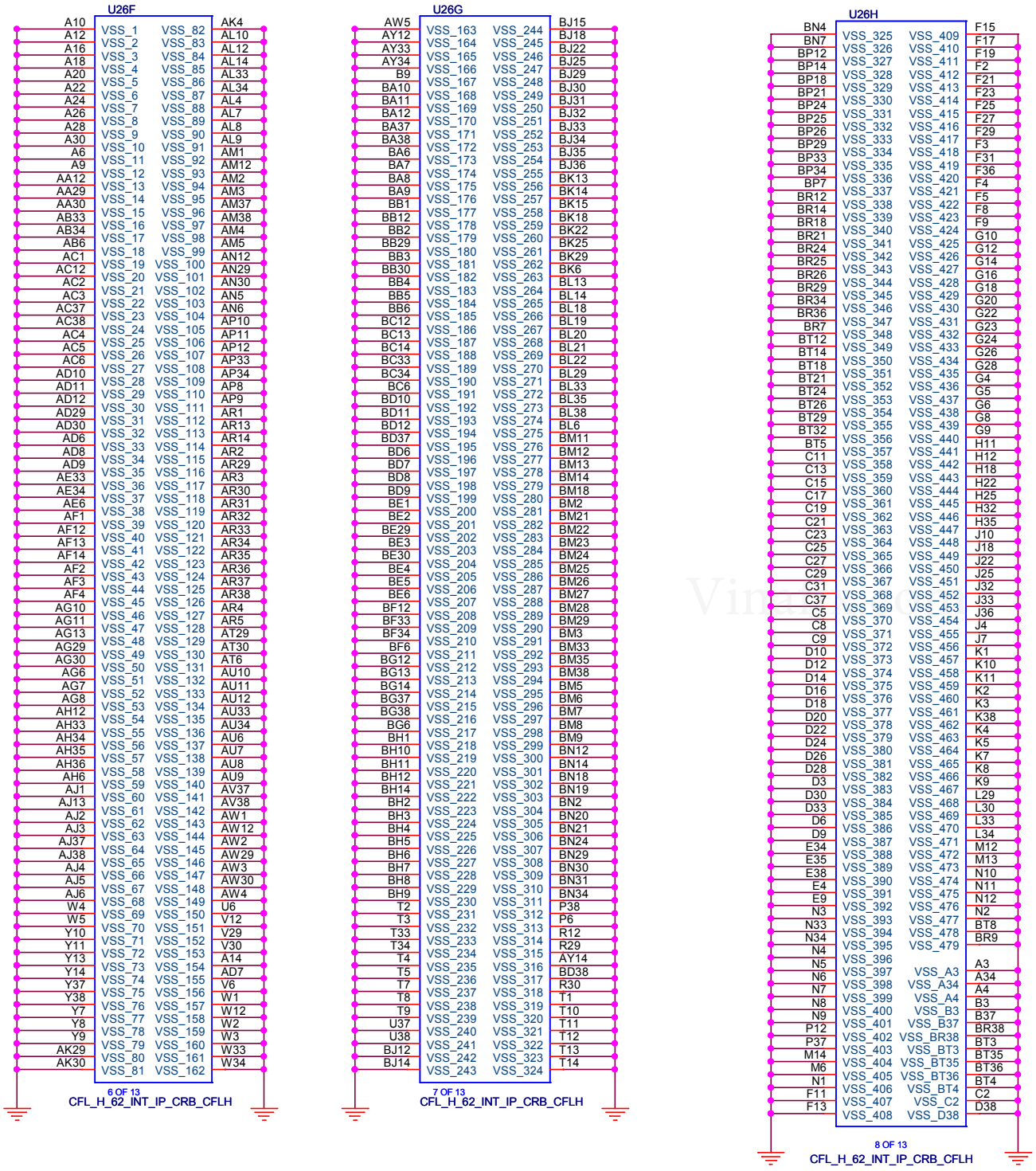
CPU CFL-H: MISC/CLK/JTAG/CFG
Size B
Document Number
GK5CN6X
Rev V A
Date: Tuesday, January 16, 2018
Sheet 9 of 72



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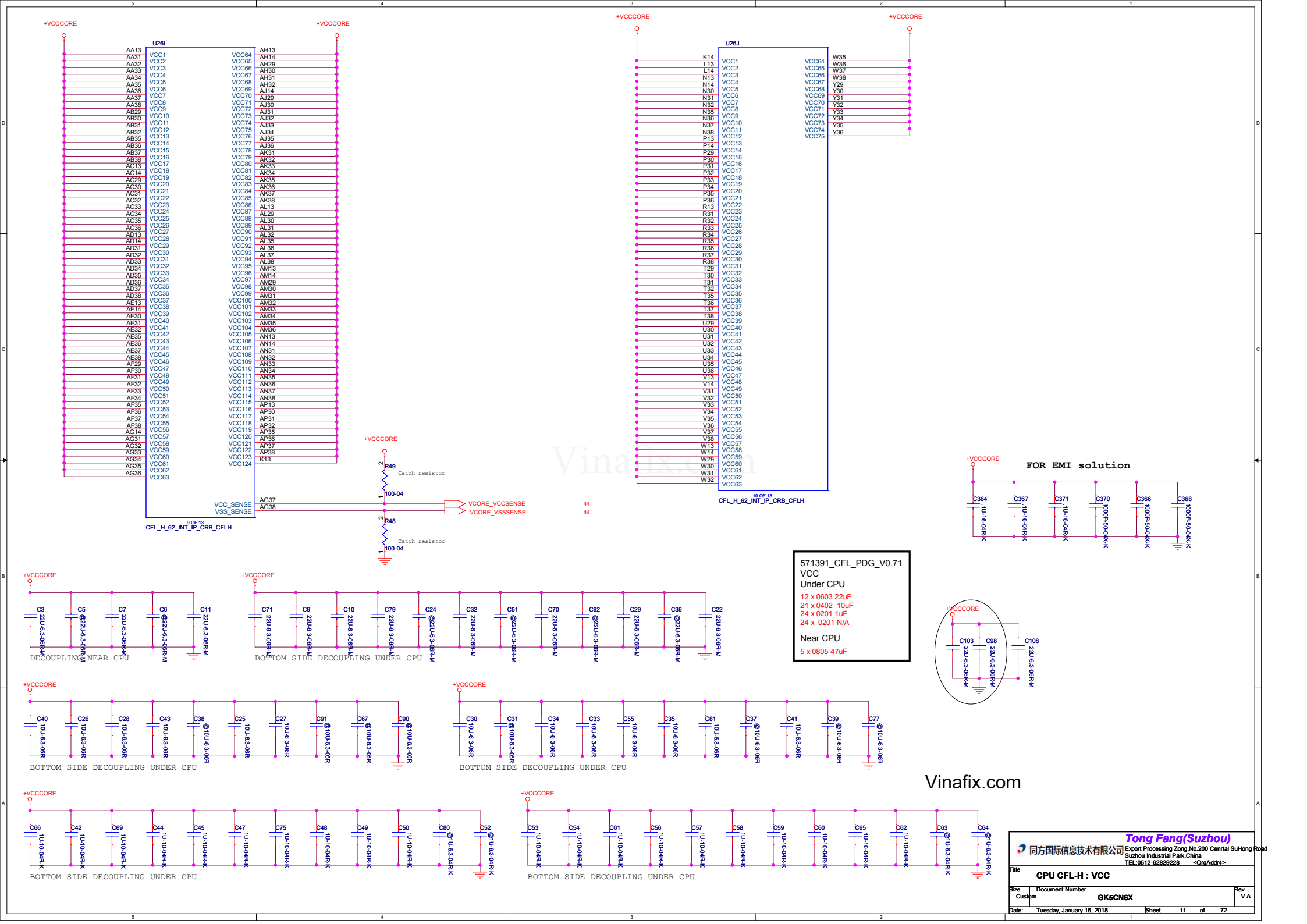
Title	CPU CFL-H : GND	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 10 of 72	


+VCCCORE
U26I
CFL_H_62_INT_IP_CRB_CFLH
9 OF 13
VCC_SENSE
VSS_SENSE
AG37
AG38
VCORE_VCCSENSE
VCORE_VSSSENSE
R49
R48
Catch resistor
100-04
U26J
CFL_H_62_INT_IP_CRB_CFLH
10 OF 13
FOR EMI solution
C364
C367
C371
C370
C366
C368
1U-16-04R-K
1000P-50-04X-K
571391_CFL_PDG_V0.71
VCC
Under CPU
12 x 0603 22uF
21 x 0402 10uF
24 x 0201 1uF
24 x 0201 N/A
Near CPU
5 x 0805 47uF
C103
C98
C108
22U-6.3-06R-M
DECOUPLING NEAR CPU
BOTTOM SIDE DECOUPLING UNDER CPU
10U-6.3-06R
@10U-6.3-06R
1U-10-04R-K
@1U-6.3-04R-K
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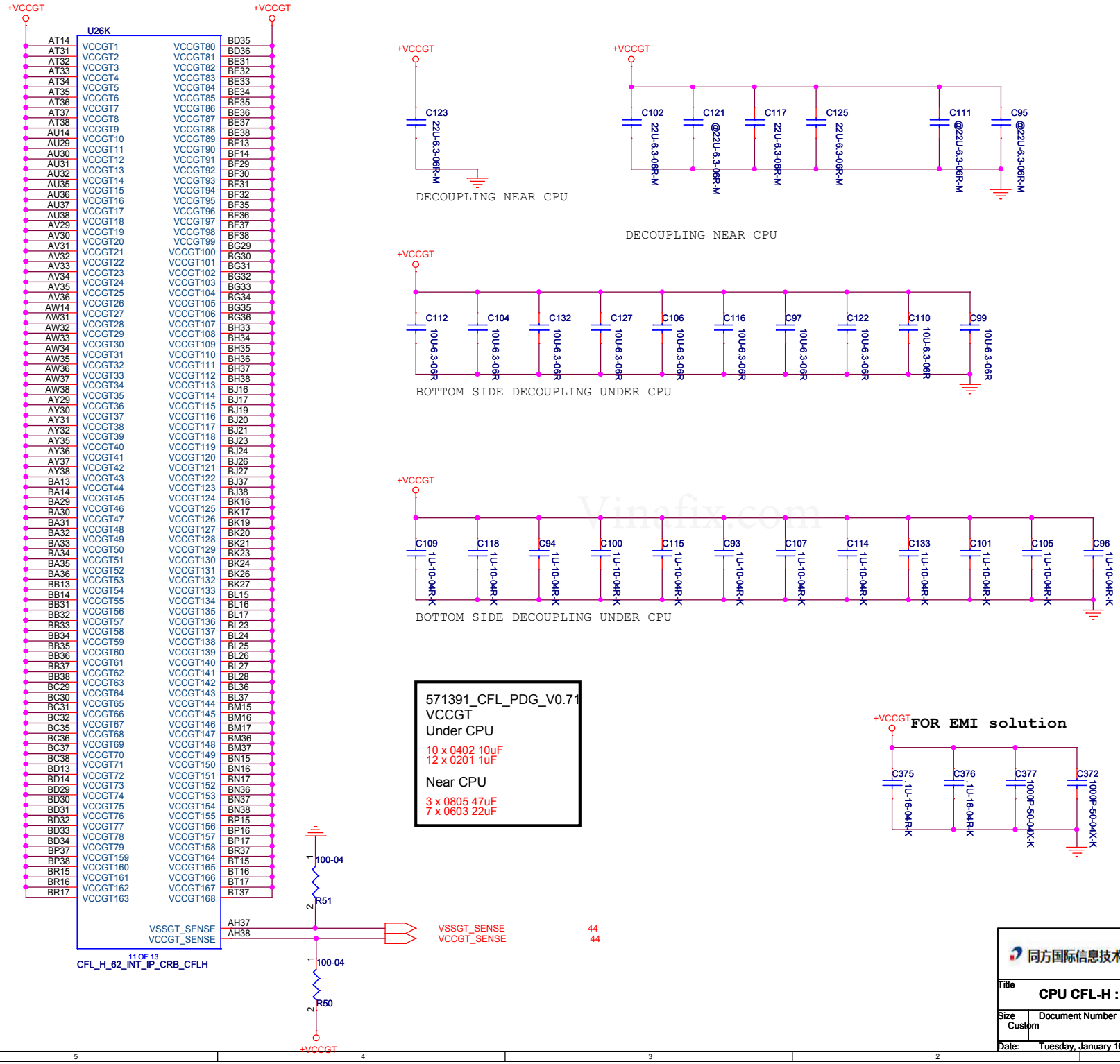
Title
CPU CFL-H : VCC
Size
Custom
Document Number
GK5CN6X
Rev
V A
Date:
Tuesday, January 16, 2018
Sheet
11
of
72



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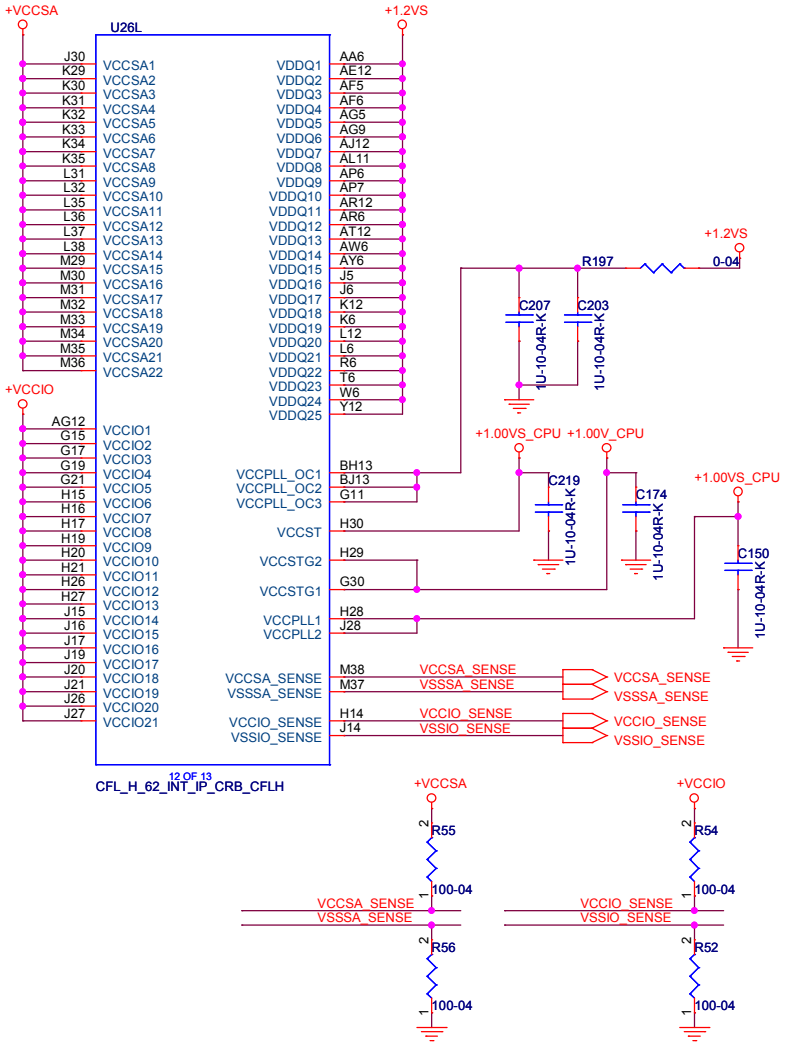
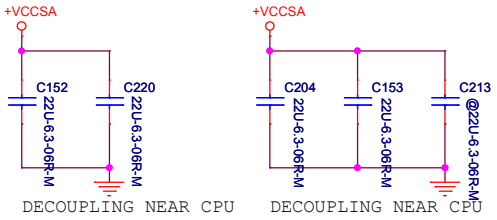
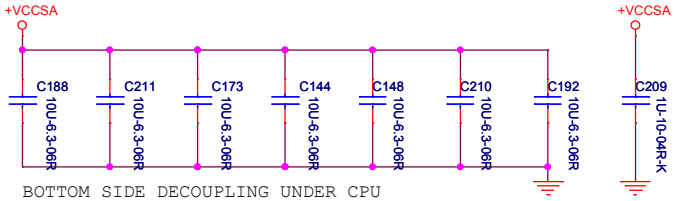
Size: Custom	Document Number: GK5CN6X		Rev: V A
Date: Tuesday, January 16, 2018		Sheet 12 of 72	



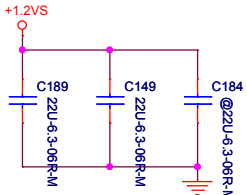
DECOUPLING NEAR CPU



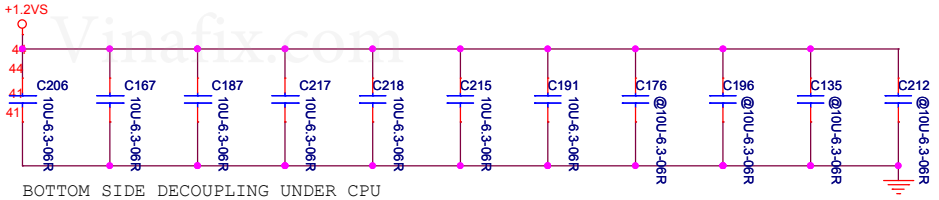
BOTTOM SIDE DECOUPLING UNDER CPU



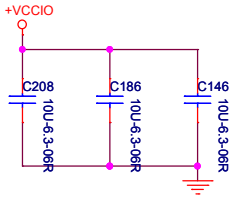
BOTTOM SIDE DECOUPLING UNDER CPU



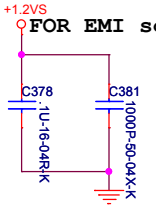
BOTTOM SIDE DECOUPLING UNDER CPU



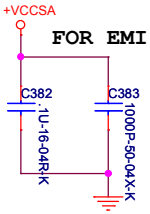
BOTTOM SIDE DECOUPLING UNDER CPU



FOR EMI solution



FOR EMI solution



571391_CFL_PDG_V0.71

VCCSA Under CPU	VCCST Under CPU
7 x 0402 10uF 1 x 0201 1uF	1 x 0201 1uF
Near CPU	VCCSTG Under CPU
2 x 0805 47uF 2 x 0603 22uF	1 x 0201 1uF
VDDQ Under CPU	VCCPLL Under CPU
4 x 0603 22uF 11 x 0402 10uF	1 x 0201 1uF
VCCIO Under CPU	VCCPLL_OC Under CPU
3 x 0402 10uF 3 x 0402 N/A	2 x 0201 1uF

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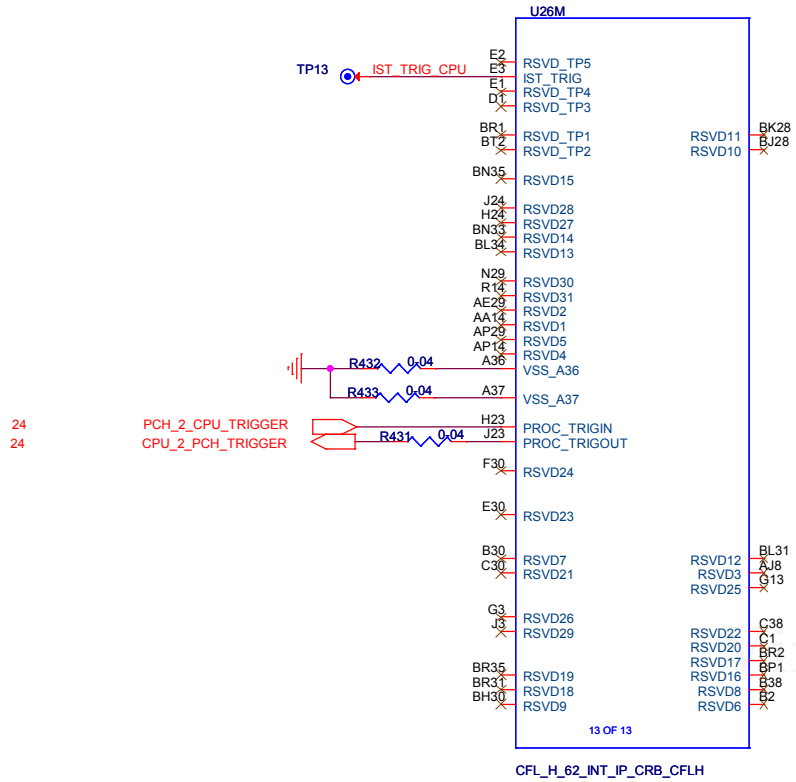
Title	CPU CFL-H : VCCSA/VCCIO/VDDQ	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 13 of 72	



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Title	CPU CFL-H : TRIG/RSVD	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 14 of 72	

BBS_BIT0 - BIOS BOOT STRAP BIT 0

BOOT BIOS STRAP		
BBS_BIT1	BBS_BIT0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	------
1	1	SPI

U28A

TP18 GPP_A11 BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#

GPP_B13/PLTRST# AV29 → PLT_RST# 30,32,33,36,47

R15 RSVD2
R13 RSVD1

GPP_K16/GSXCLK Y47
GPP_K12/GSXDOUT Y46
GPP_K13/GSXSLOAD Y48
GPP_K14/GSXDIN W46
GPP_K15/GSXSRESET# AA45

R67 @1K-1-04

+3.3VA

TP24 VSS_AL37 AL37
AN35 VSS
TP

R72 100K-04

PCH_SPI_SI R75 1 2 33-04 PCH_SPI_SI_R AU41 SPI0_MOSI
PCH_SPI_SO R57 1 2 33-04 PCH_SPI_SO_R BA45 SPI0_MISO
PCH_SPI_CS0# AY47 SPI0_CS0#
PCH_SPI_CLK R71 1 2 33-04 PCH_SPI_CLK_R AW47 SPI0_CLK
TP19 SPI0_CS1# AW48 SPI0_CS1#

GPP_E3/CPU_GP0 AL47 → EC_EXTSMI# 30
GPP_E7/CPU_GP1 AM45 → TP_INT# 37
GPP_B3/CPU_GP2 BF32
GPP_B4/CPU_GP3 BC33

PCH_SPI_WP R58 1 2 33-04 PCH_SPI0_IO2 AY48 SPI0_IO2
PCH_SPI_HOLD R74 1 2 33-04 PCH_SPI0_IO3 BA46 SPI0_IO3
TP25 SPI0_CS2# AT40 SPI0_CS2#

GPP_H18/SML4ALERT# AE44
GPP_H17/SML4DATA AJ46
GPP_H16/SML4CLK AE43
GPP_H15/SML3ALERT# AC47 GPP_H15 R73 100K-04 +3.3VA
GPP_H14/SML3DATA AD48
GPP_H13/SML3CLK AF47
GPP_H12/SML2ALERT# AB47 GPP_H12 R76 @4.7K-04 +3.3VA
GPP_H11/SML2DATA AD47
GPP_H10/SML2CLK AE48

GPP_H15 External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2

INTRUDER# BB44 → SM_INTRUDER# 18

1 OF 13

CNP_H_IP_CFL

SPI0_MOSI:
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K ifpulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_H12 eSPI Flash Sharing Mode
0:Master Attached Flash Sharing (MAFS) enabled (internal pull down)
1:Slave Attached Flash Sharing (SAFS) enabled

R3825 100K-04 PCH_SPI_CLK_R

+3.3VA

R60 1K-04

U20

PCH_SPI_CS0# 1 CS# VCC 8
PCH_SPI_SO 2 SO HOLD/IO3 7
PCH_SPI_WP 3 WP/IO2 SCK 6
4 GND SI 5

W25Q128JVSIQT

+3.3VA

+3.3VA

R59 1K-04

PCH_SPI_HOLD#
PCH_SPI_CLK
PCH_SPI_SI

C221 4.7U-6.3-06R-K

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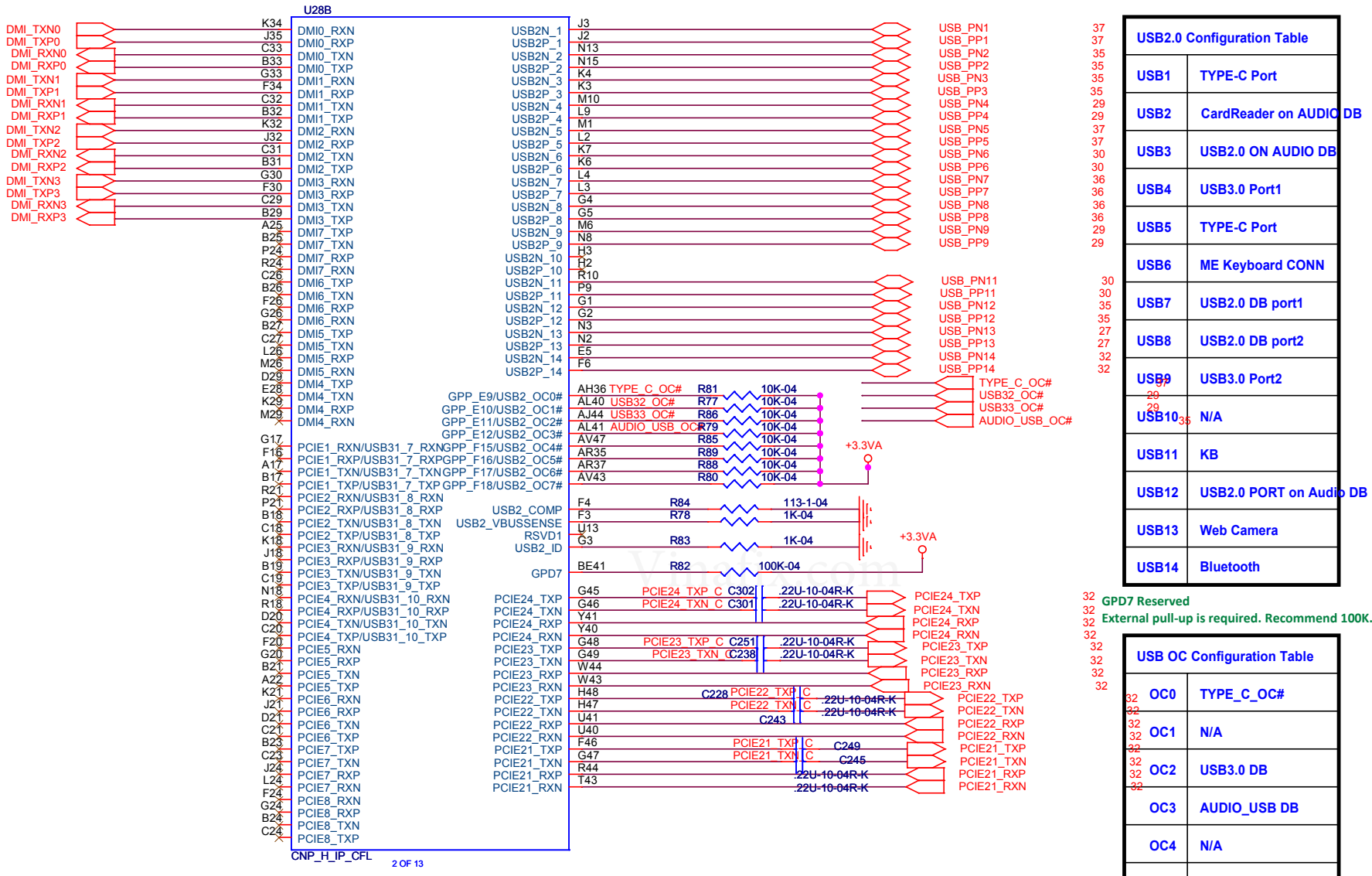
Title: PCH CFL-H : SPI

Size	Document Number	Rev
A	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 15 of 72



USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on AUDIO DB
USB3	USB2.0 ON AUDIO DB
USB4	USB3.0 Port1
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	USB2.0 DB port1
USB8	USB2.0 DB port2
USB9	USB3.0 Port2
USB10	N/A
USB11	KB
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

GPD7 Reserved
External pull-up is required. Recommend 100K.

USB OC Configuration Table	
OC0	TYPE_C_OC#
OC1	N/A
OC2	USB3.0 DB
OC3	AUDIO_USB DB
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

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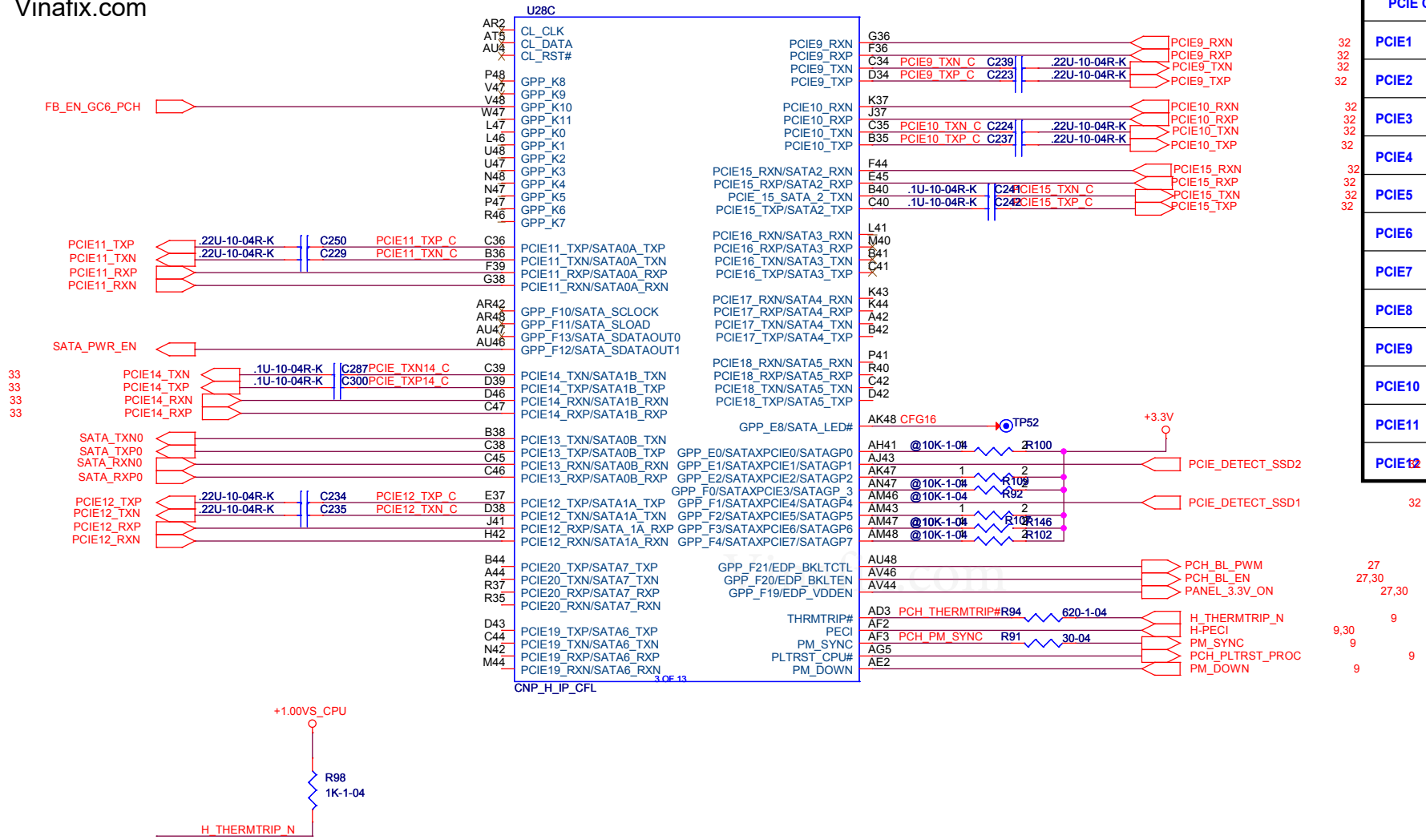
Title: PCH CFL-H : DMI/USB2.0

Size: Custom | Document Number: GK5CN6X | Rev: V A

Date: Tuesday, January 16, 2018 | Sheet 16 of 72



PCIE Configuration Table			
PCIE1	No function	PCIE13	SATA HDD
PCIE2	No function	PCIE14	LAN
PCIE3	No function	PCIE15	WLAN
PCIE4	No function	PCIE16	N/A
PCIE5	LAN	PCIE17	PCIE SSD1
PCIE6	WLAN	PCIE18	PCIE SSD1
PCIE7	No function	PCIE19	PCIE SSD1
PCIE8	No function	PCIE20	PCIE SSD1
PCIE9	PCIE SSD2	PCIE21	N/A
PCIE10	PCIE SSD2	PCIE22	N/A
PCIE11	PCIE SSD2	PCIE23	N/A
PCIE12	PCIE SSD2	PCIE24	N/A

SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD2
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD1
SATA5	N/A
SATA6	No Function
SATA7	No Function

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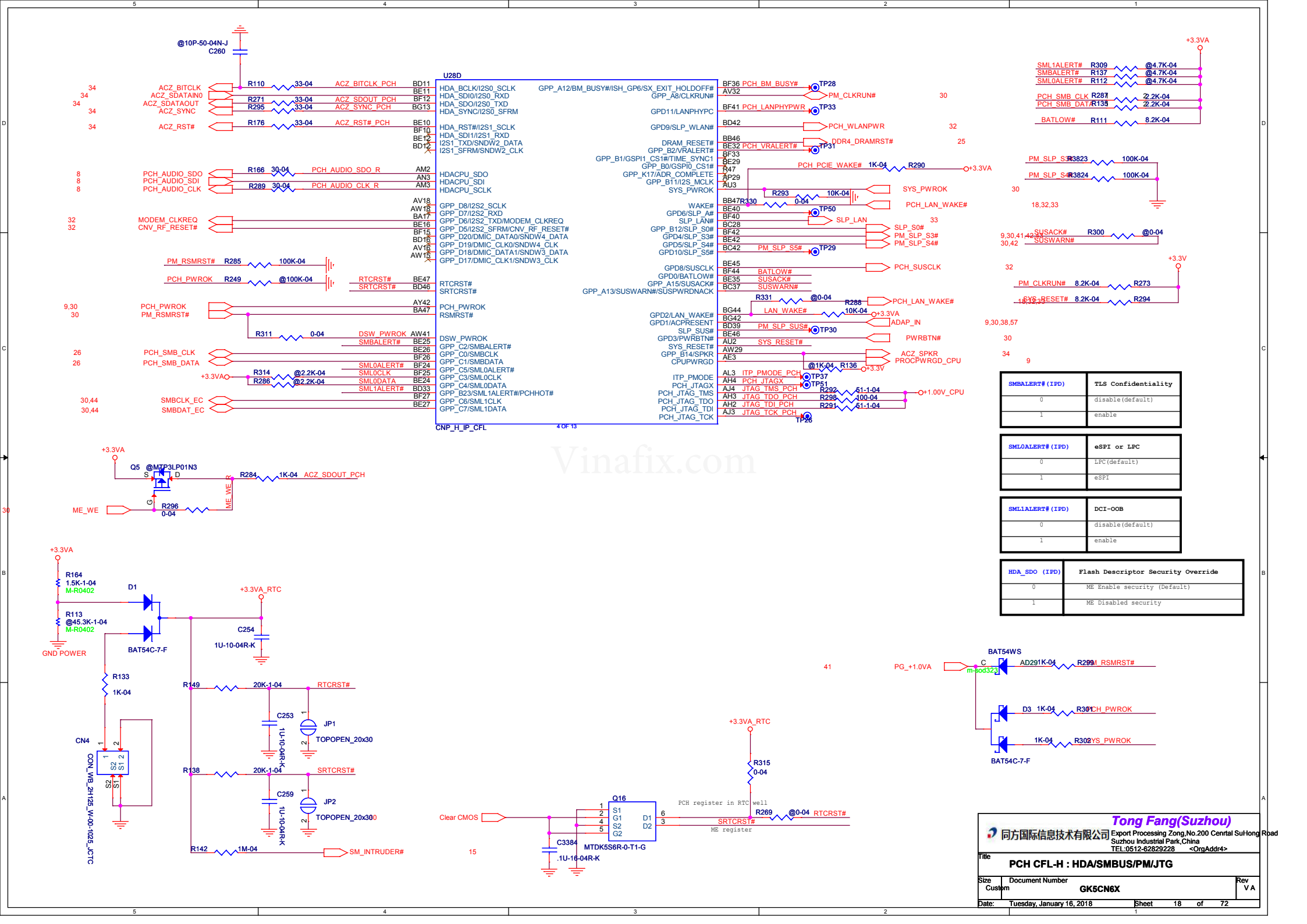
Title: PCH CFL-H : SATA/PCIE

Size	Document Number	Rev
Custom	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 17 of 72



Title	PCH CFL-H : HDA/SMBUS/PM/JTG
Size	Custom
Document Number	GK5CN6X
Rev	V A
Date:	Tuesday, January 16, 2018
Sheet	18 of 72

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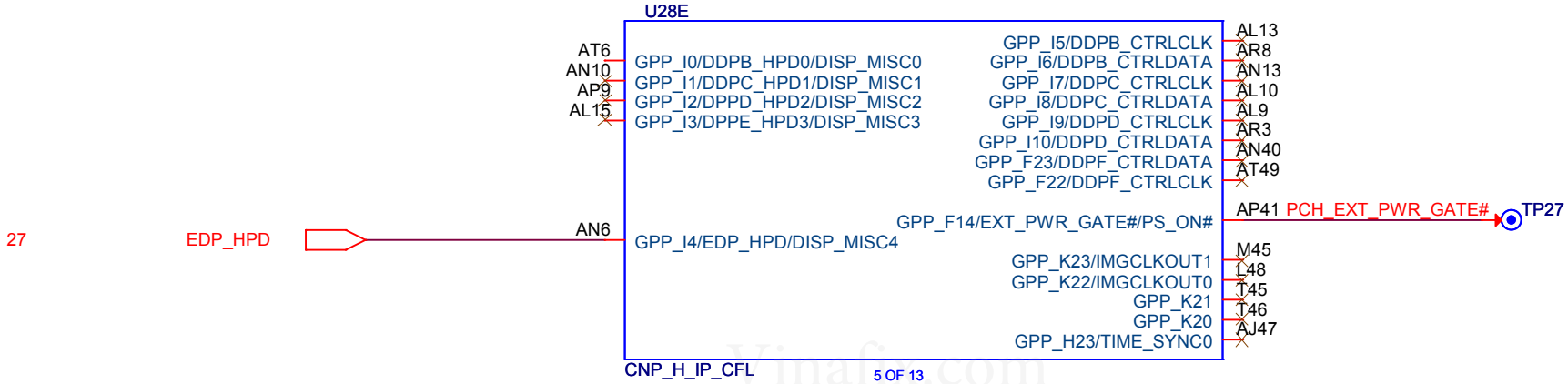

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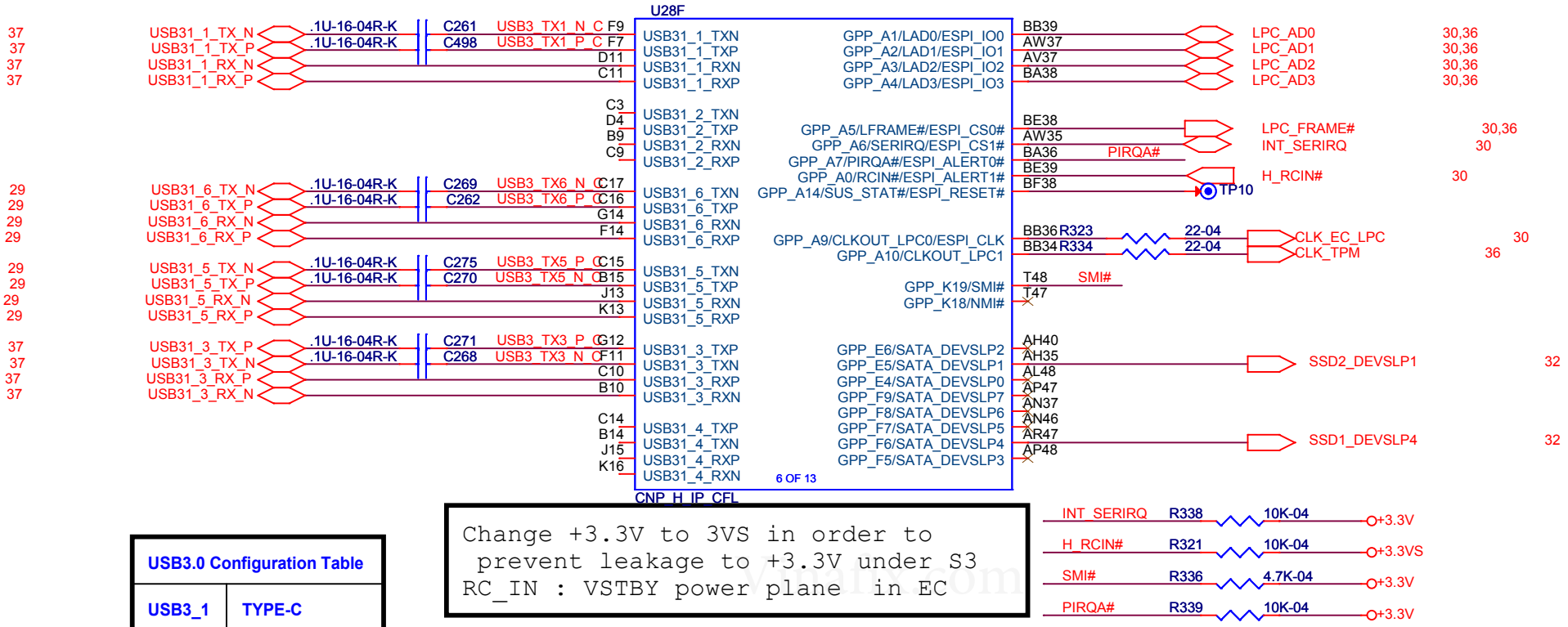
Title
PCH CFL-H : DDI CONTROL

Size	Document Number	Rev
A	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 19 of 72



Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC

USB3.0 Configuration Table	
USB3_1	TYPE-C
USB3_2	N/A
USB3_3	TYPE-C
USB3_4	N/A
USB3_5	USB3.0 Port2
USB3_6	USB3.0 Port1
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

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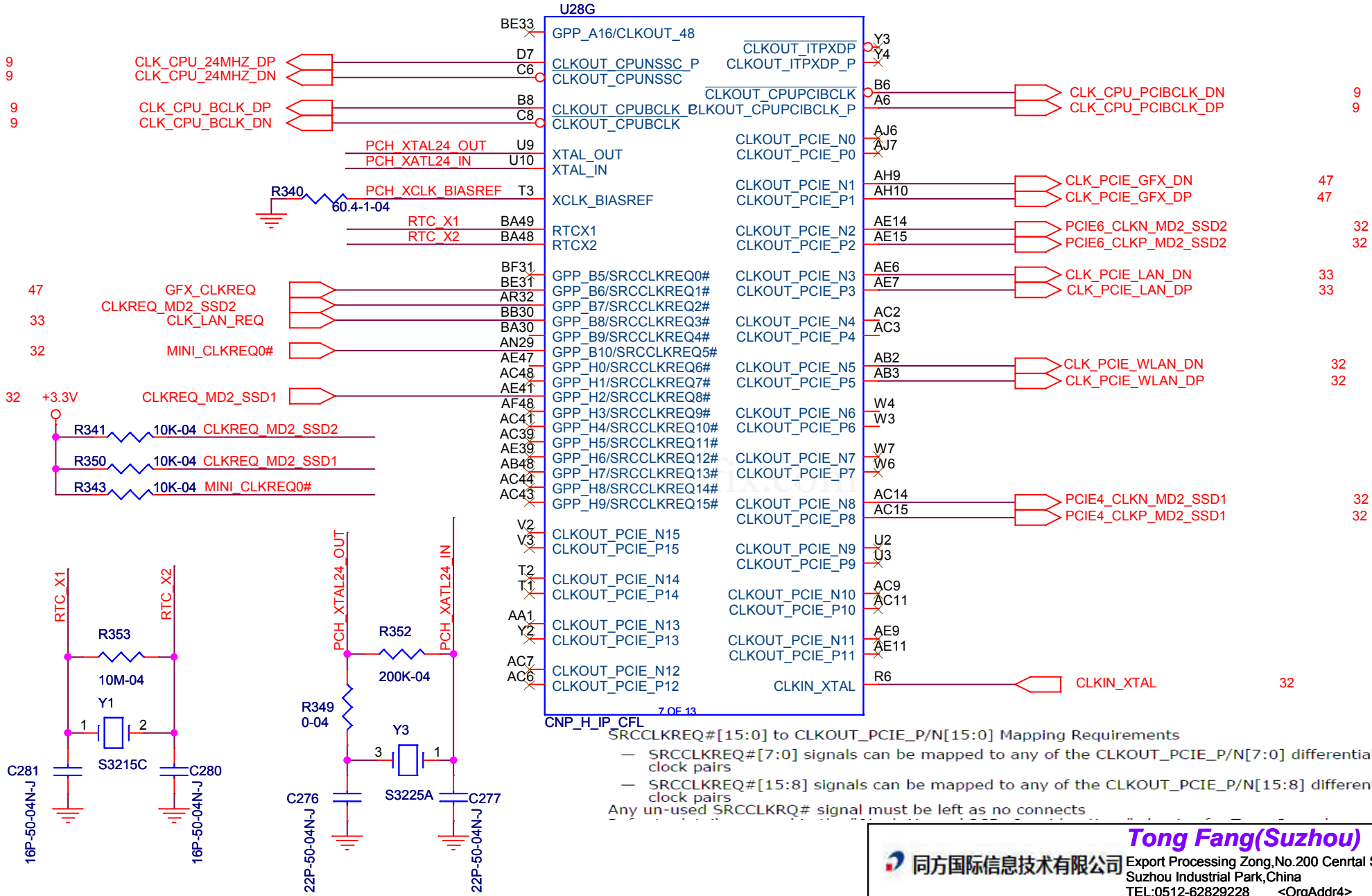
Title: PCH CFL-H : USB3.0/LPC

Size: Custom | Document Number: GK5CN6X | Rev: V A

Date: Tuesday, January 16, 2018 | Sheet 20 of 72



SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements

- SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
- SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Any un-used SRCCLKRQ# signal must be left as no connects

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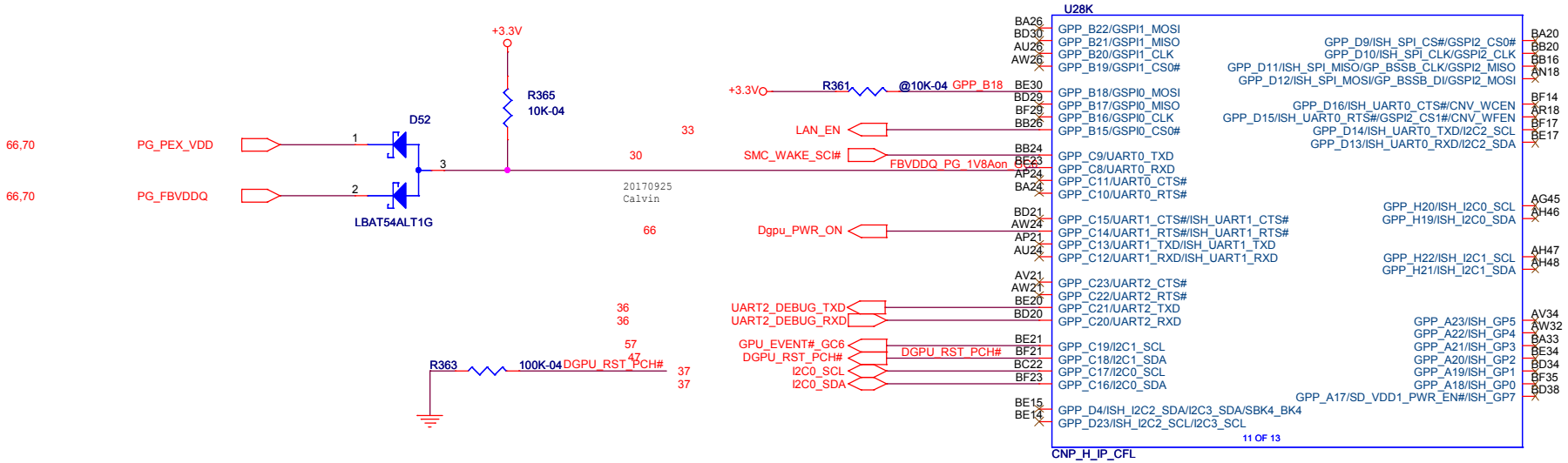
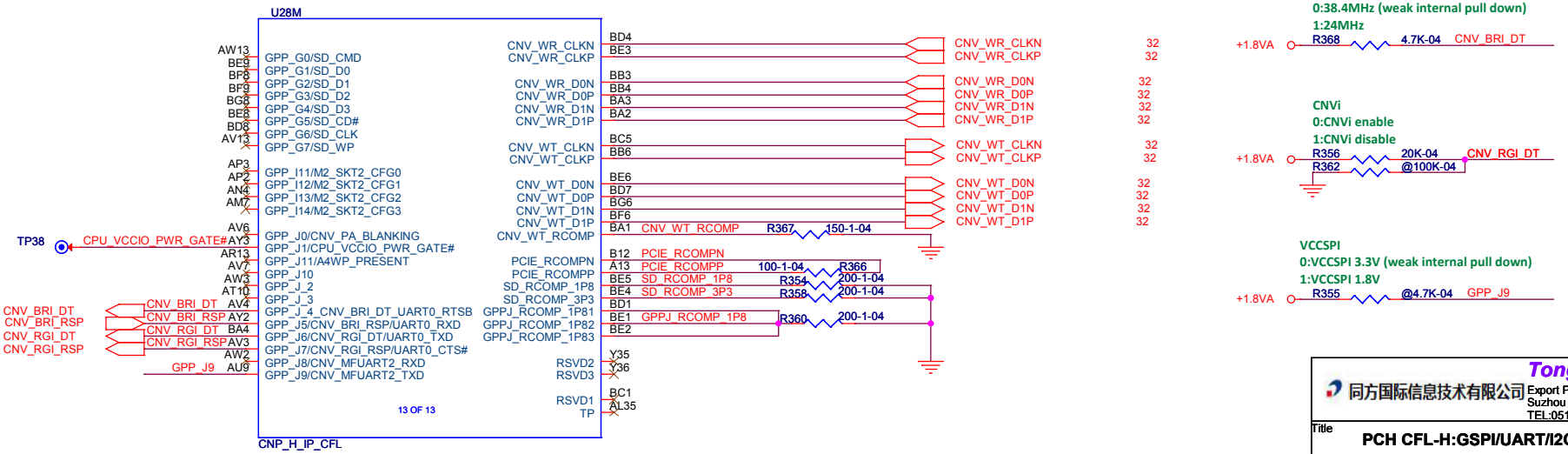
Title	PCH CFL-H : CLK	
Size A	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 21 of 72	

GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable "No Reboot" mode. (Default)
1	Enable "No Reboot" mode





XTAL
0:38.4MHz (weak internal pull down)
1:24MHz
+1.8VA R368 4.7K-04 CNV_BRI_DT

CNVi
0:CNVi enable
1:CNVi disable
+1.8VA R356 20K-04 CNV_RGI_DT
R362 @100K-04

VCCSPI
0:VCCSPI 3.3V (weak internal pull down)
1:VCCSPI 1.8V
+1.8VA R355 @4.7K-04 GPP_J9

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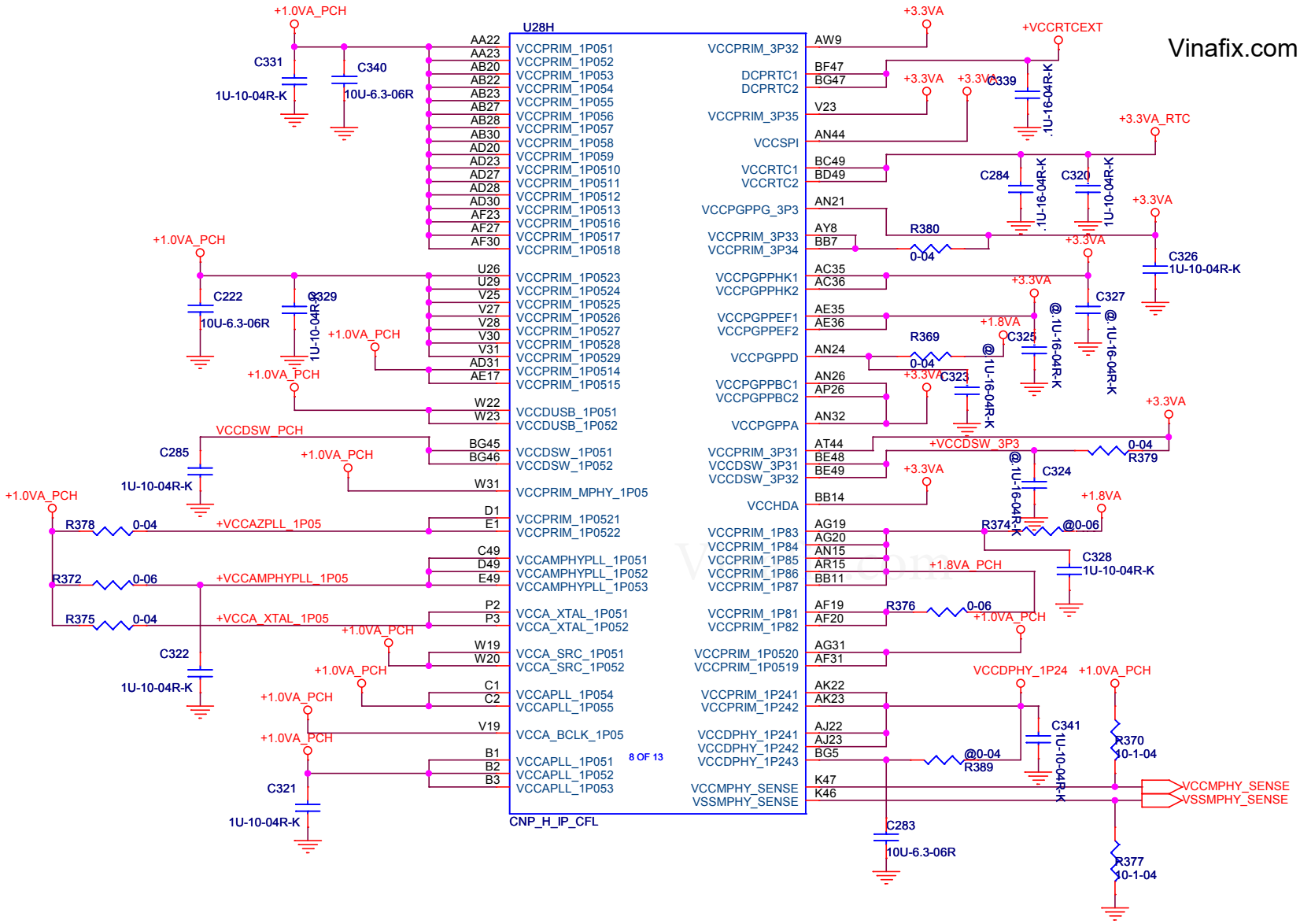
Title: PCH CFL-H:GSPI/UART/I2C/CNVi
Size: B
Document Number: GK5CN6X
Rev: V A
Date: Tuesday, January 16, 2018
Sheet 22 of 72



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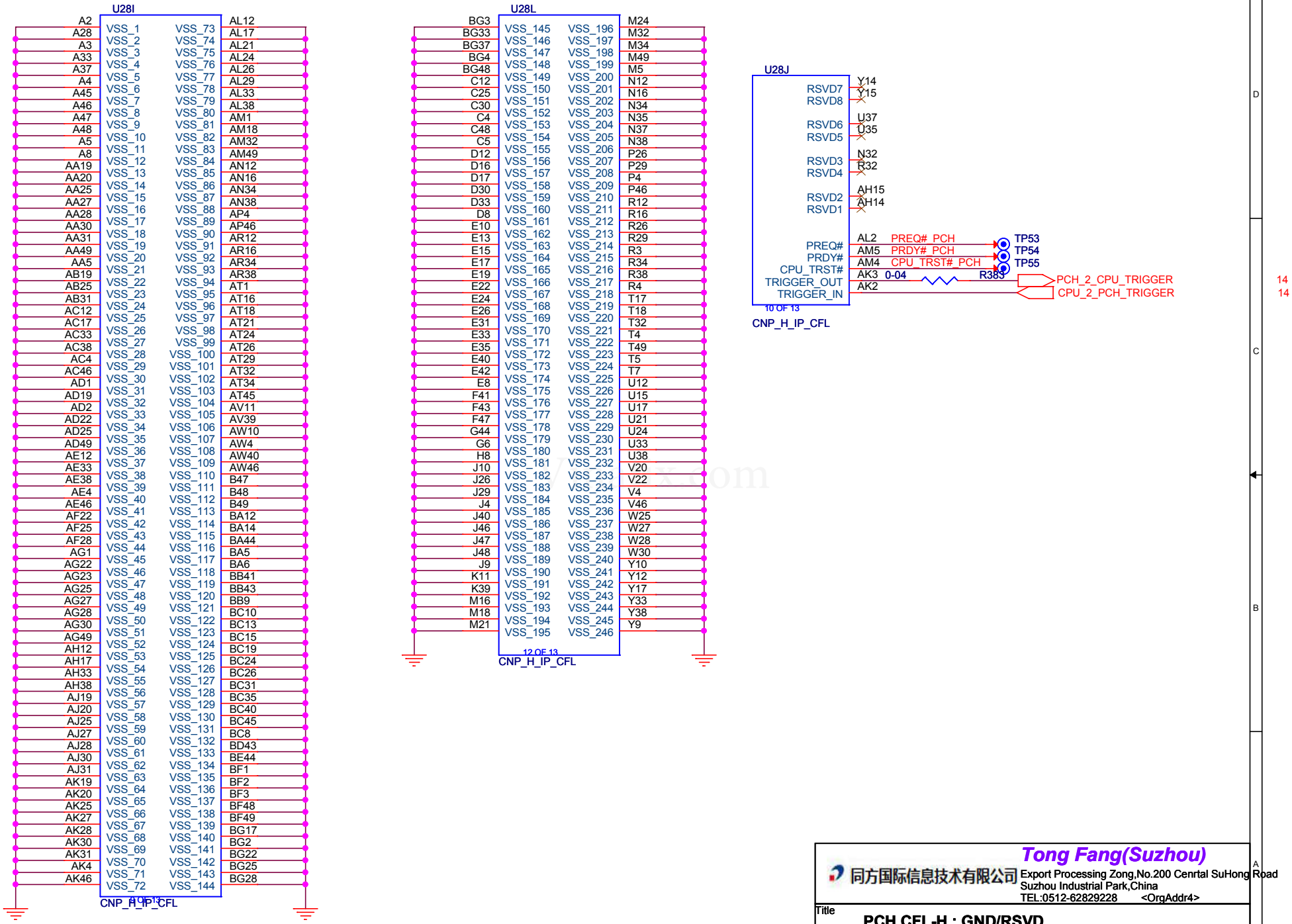
Title: PCH CFL-H : POWER			
Size: Custom	Document Number: GK5CN6X		Rev: V A
Date: Tuesday, January 16, 2018		Sheet 23 of 72	



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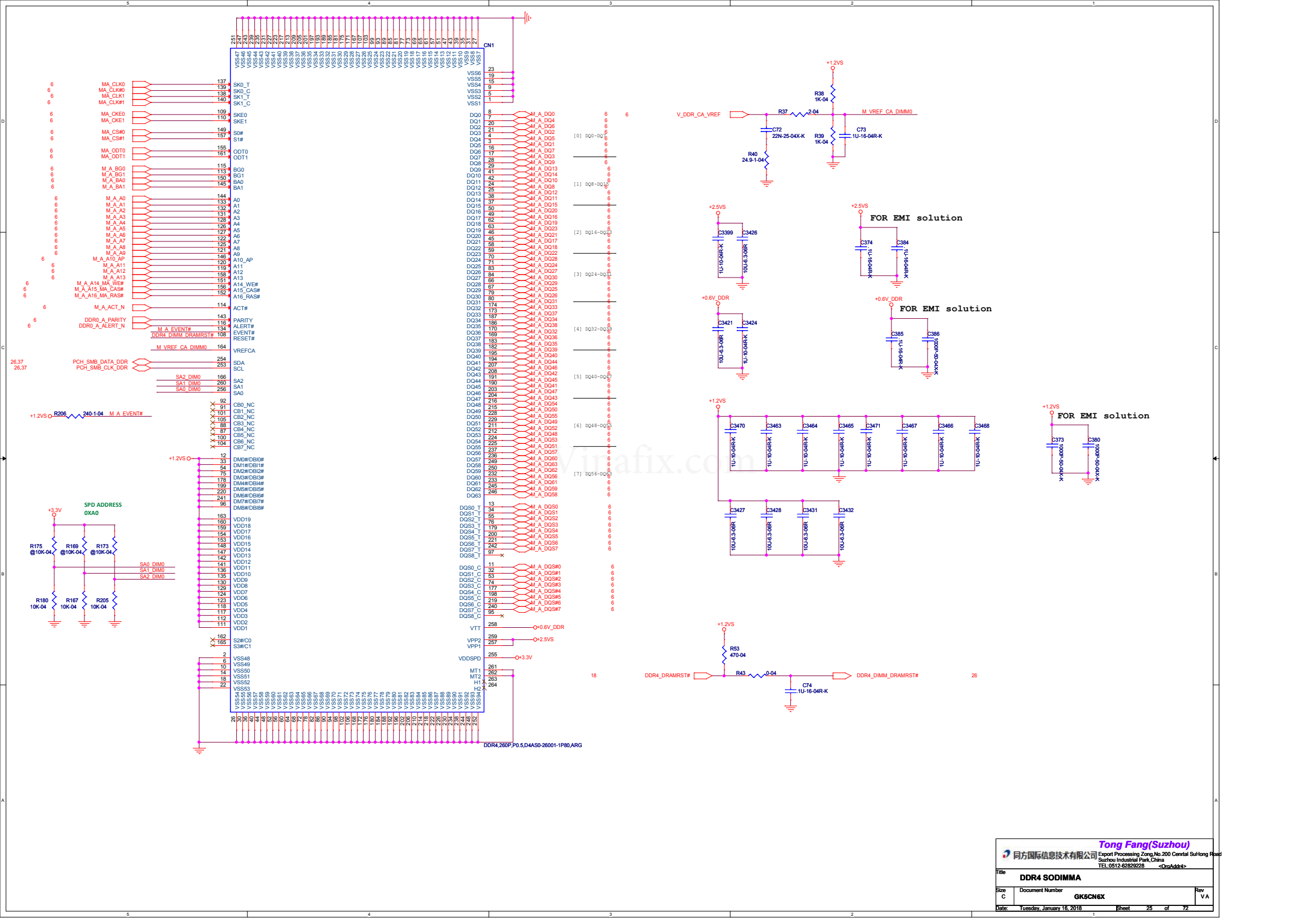
Title	PCH CFL-H : GND/RSVD	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 24 of 72	


CN1
DDR4_260P.P0.5,D4AS0-26001-1P80,ARG
SPD ADDRESS
0XA0
FOR EMI solution
FOR EMI solution
FOR EMI solution
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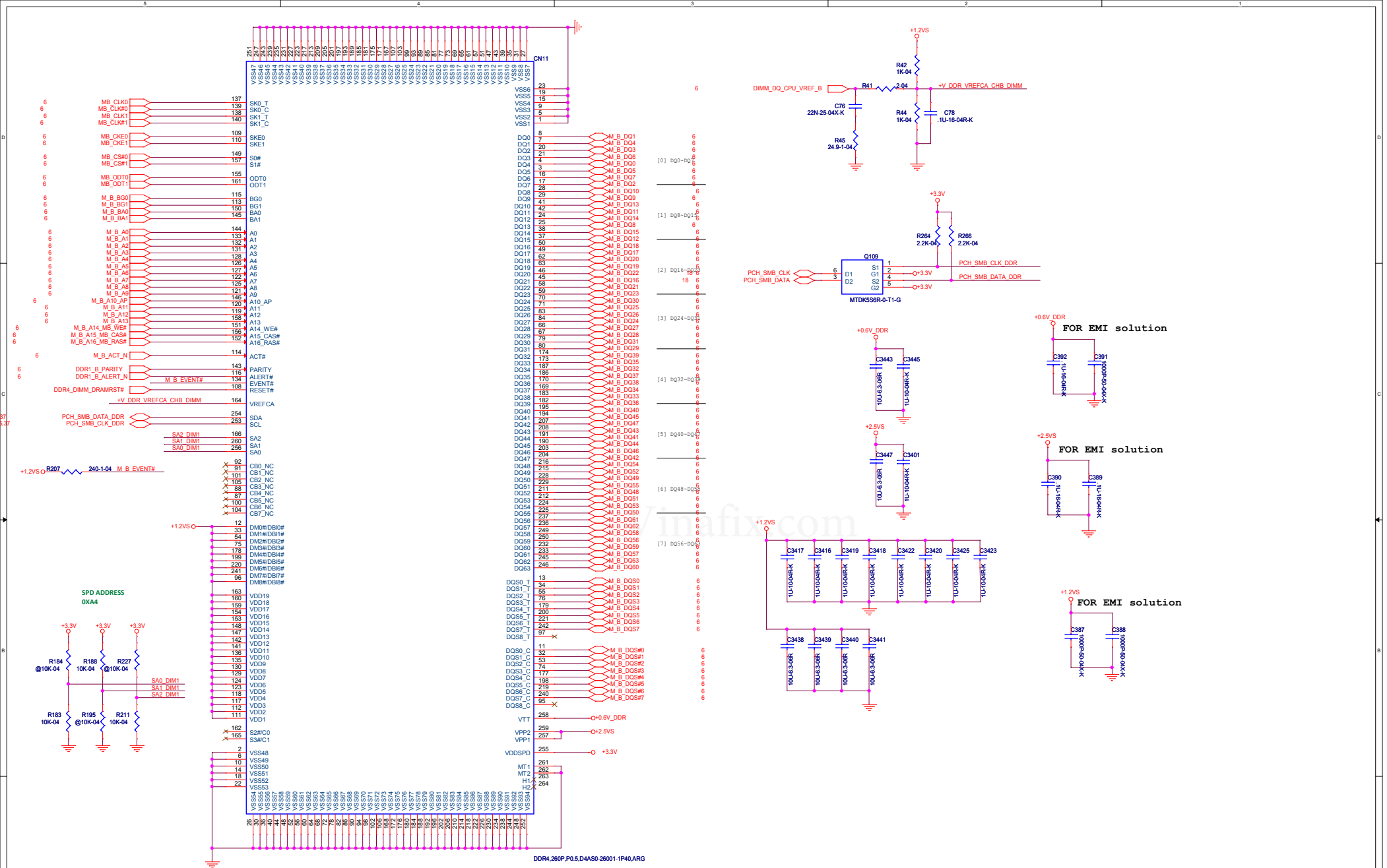
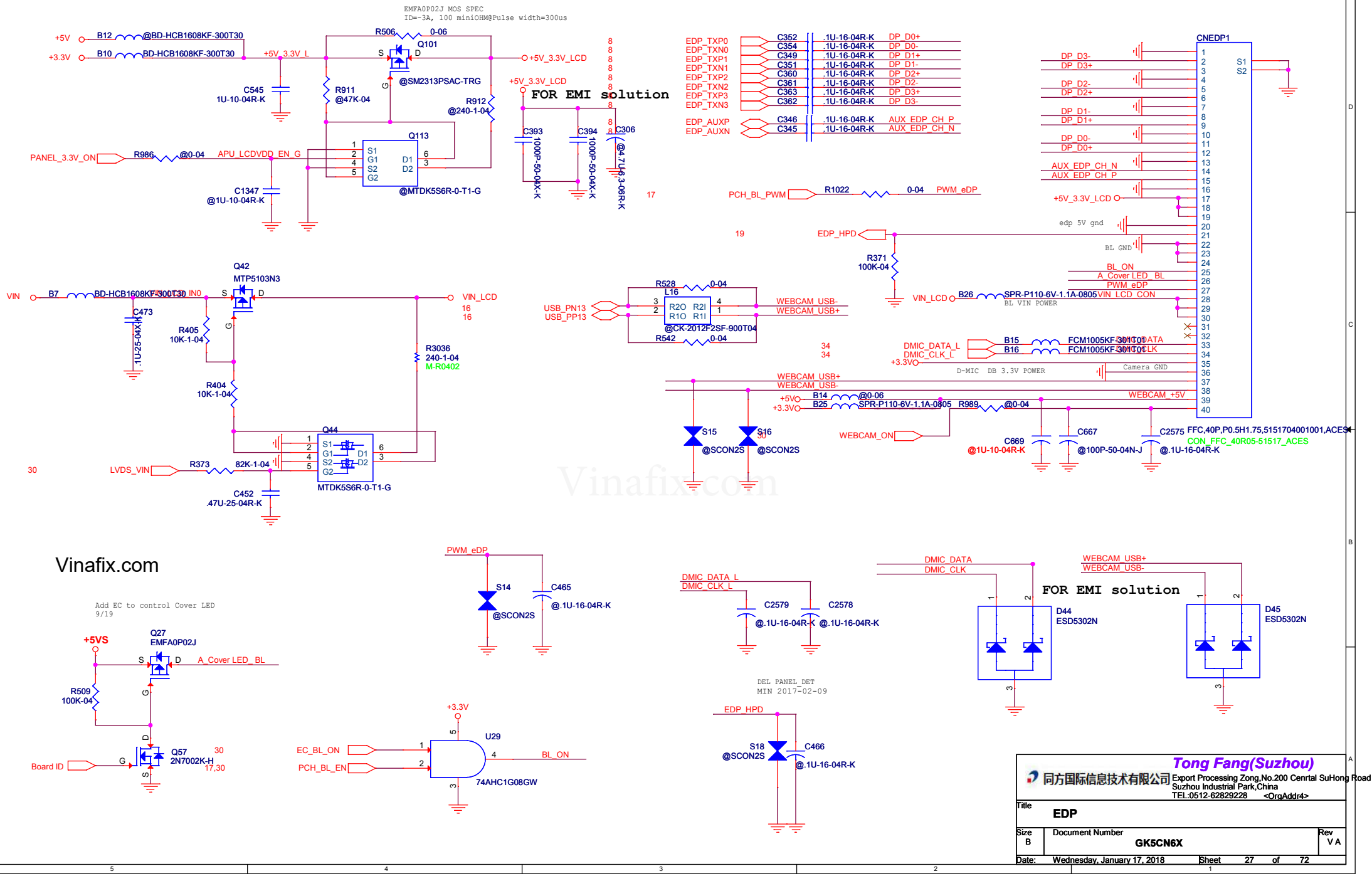
<OrgAddr4>
Title
DDR4 SODIMMA
Size C
Document Number GK5CN6X
Rev V A
Date: Tuesday, January 16, 2018
Sheet 25 of 72



Title	DDR4 SODIMMB	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 26 of 72	


EMFA0P02J MOS SPEC
ID=-3A, 100 miniOHM@Pulse width=300us
+5V
+3.3V
B12 @BD-HCB1608KF-300T30
B10 BD-HCB1608KF-300T30
+5V_3.3V_L
R506 0-06
Q101
@SM2313PSAC-TRG
+5V_3.3V_LCD
C545 1U-10-04R-K
R911 @47K-04
R912 @240-1-04
FOR EMI solution
C393 1000P-50-04X-K
C394 1000P-50-04X-K
C306 @4.7U6.3-06R-K
Q113
@MTDK5S6R-0-T1-G
PANEL_3.3V_ON
R986 @0-04
APU_LCDVDD_EN_G
C1347 @1U-10-04R-K
EDP_TXP0
EDP_TXN0
EDP_TXP1
EDP_TXN1
EDP_TXP2
EDP_TXN2
EDP_TXP3
EDP_TXN3
C352 .1U-16-04R-K DP_D0+
C354 .1U-16-04R-K DP_D0-
C349 .1U-16-04R-K DP_D1+
C351 .1U-16-04R-K DP_D1-
C360 .1U-16-04R-K DP_D2+
C361 .1U-16-04R-K DP_D2-
C363 .1U-16-04R-K DP_D3+
C362 .1U-16-04R-K DP_D3-
EDP_AUXP
EDP_AUXN
C346 .1U-16-04R-K AUX_EDP_CH_P
C345 .1U-16-04R-K AUX_EDP_CH_N
CNEDP1
DP_D3-
DP_D3+
DP_D2-
DP_D2+
DP_D1-
DP_D1+
DP_D0-
DP_D0+
AUX_EDP_CH_N
AUX_EDP_CH_P
+5V_3.3V_LCD
edp 5V gnd
BL GND
BL_ON
A_Cover LED_BL
PWM_eDP
VIN_LCD_CON
PCH_BL_PWM
R1022 0-04 PWM_eDP
EDP_HPD
R371 100K-04
VIN_LCD
B26 SPR-P110-6V-1.1A-0805
BL VIN POWER
Q42
MTP5103N3
VIN
B7 BD-HCB1608KF-300T30
IN0
C473 .1U-25-04X-K
R405 10K-1-04
R404 10K-1-04
R3036 240-1-04 M-R0402
VIN_LCD
Q44
MTDK5S6R-0-T1-G
LVDS_VIN
R373 82K-1-04
C452 .47U-25-04R-K
R528 0-04
L16
R542 0-04
@CK-2012F2SF-900T04
USB_PN13
USB_PP13
WEBCAM_USB-
WEBCAM_USB+
DMIC_DATA_L
DMIC_CLK_L
B15 FCM1005KF-301T04
B16 FCM1005KF-301T04
D-MIC DB 3.3V POWER
Camera GND
WEBCAM_USB+
WEBCAM_USB-
B14 @0-06
B25 SPR-P110-6V-1.1A-0805
R989 @0-04
WEBCAM_+5V
WEBCAM_ON
S15 @SCON2S
S16 @SCON2S
C669 @1U-10-04R-K
C667 @100P-50-04N-J
C2575 @.1U-16-04R-K
FFC,40P,P0.5H1.75,5151704001001,ACES
CON_FFC_40R05-51517_ACES
Vinafix.com
Add EC to control Cover LED
9/19
+5VS
Q27
EMFA0P02J
A_Cover LED_BL
R509 100K-04
Q57 2N7002K-H
Board ID
PWM_eDP
S14 @SCON2S
C465 @.1U-16-04R-K
DMIC_DATA_L
DMIC_CLK_L
C2579 @.1U-16-04R-K
C2578 @.1U-16-04R-K
DMIC_DATA
DMIC_CLK
WEBCAM_USB+
WEBCAM_USB-
FOR EMI solution
D44 ESD5302N
D45 ESD5302N
DEL PANEL_DET
MIN 2017-02-09
EDP_HPD
S18 @SCON2S
C466 @.1U-16-04R-K
+3.3V
U29
EC_BL_ON
PCH_BL_EN
BL_ON
74AHC1G08GW
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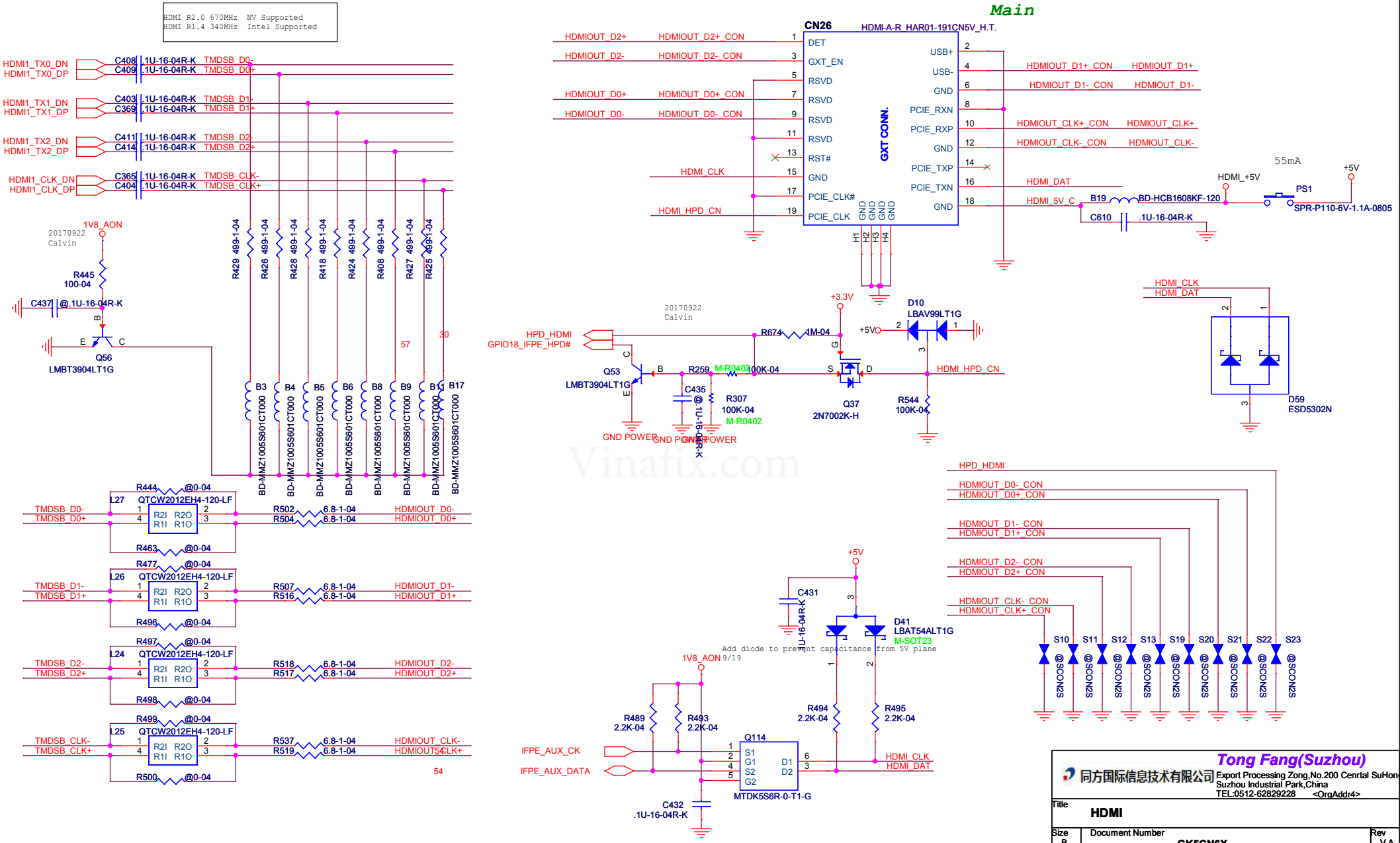
TEL:0512-62829228 <OrgAddr4>
Title
EDP
Size B
Document Number
GK5CN6X
Rev V A
Date: Wednesday, January 17, 2018
Sheet 27 of 72

HDMI CONN

HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported

Main



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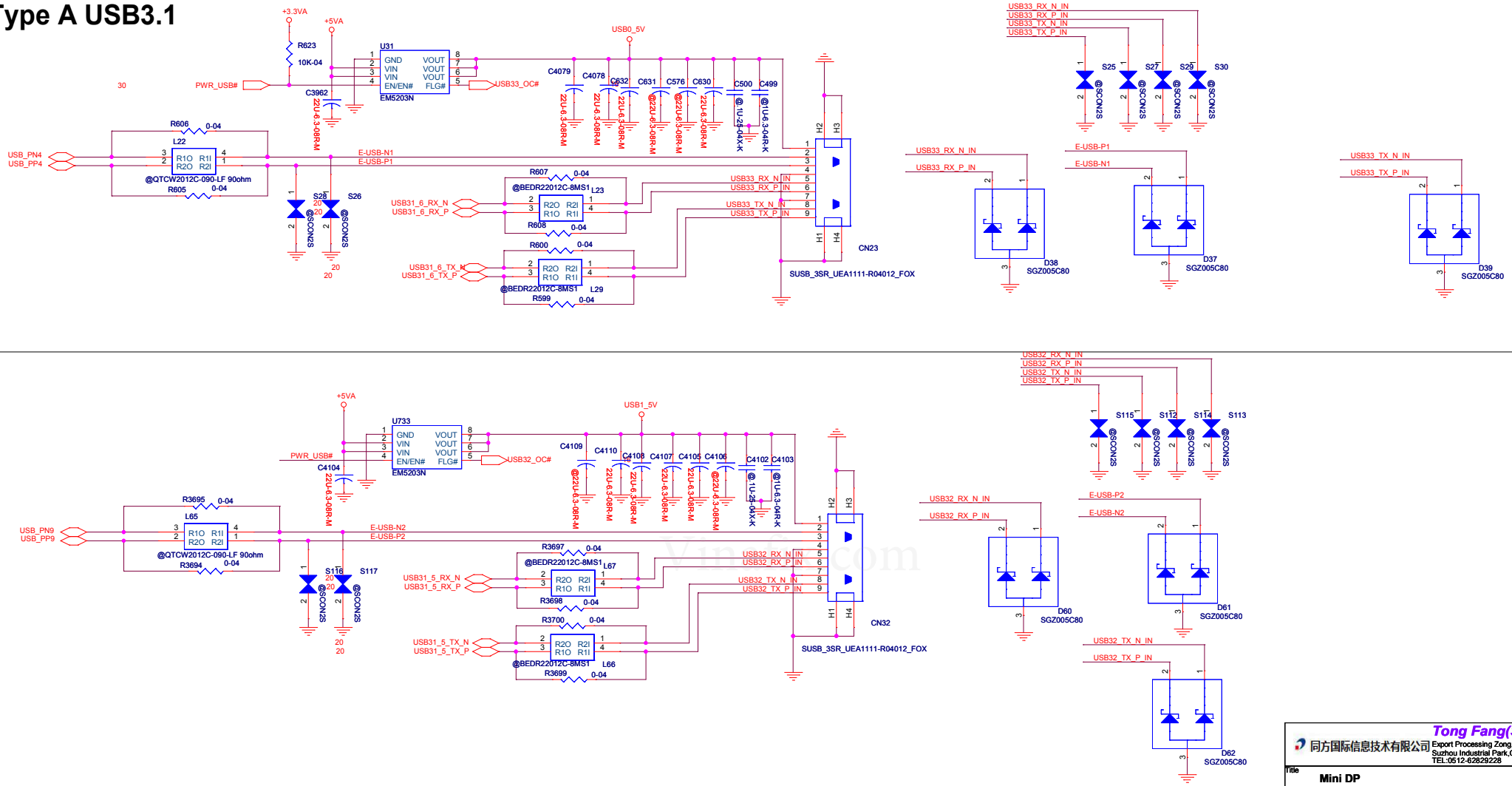
Title	HDMI	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 28 of 72	

Type A USB3.1



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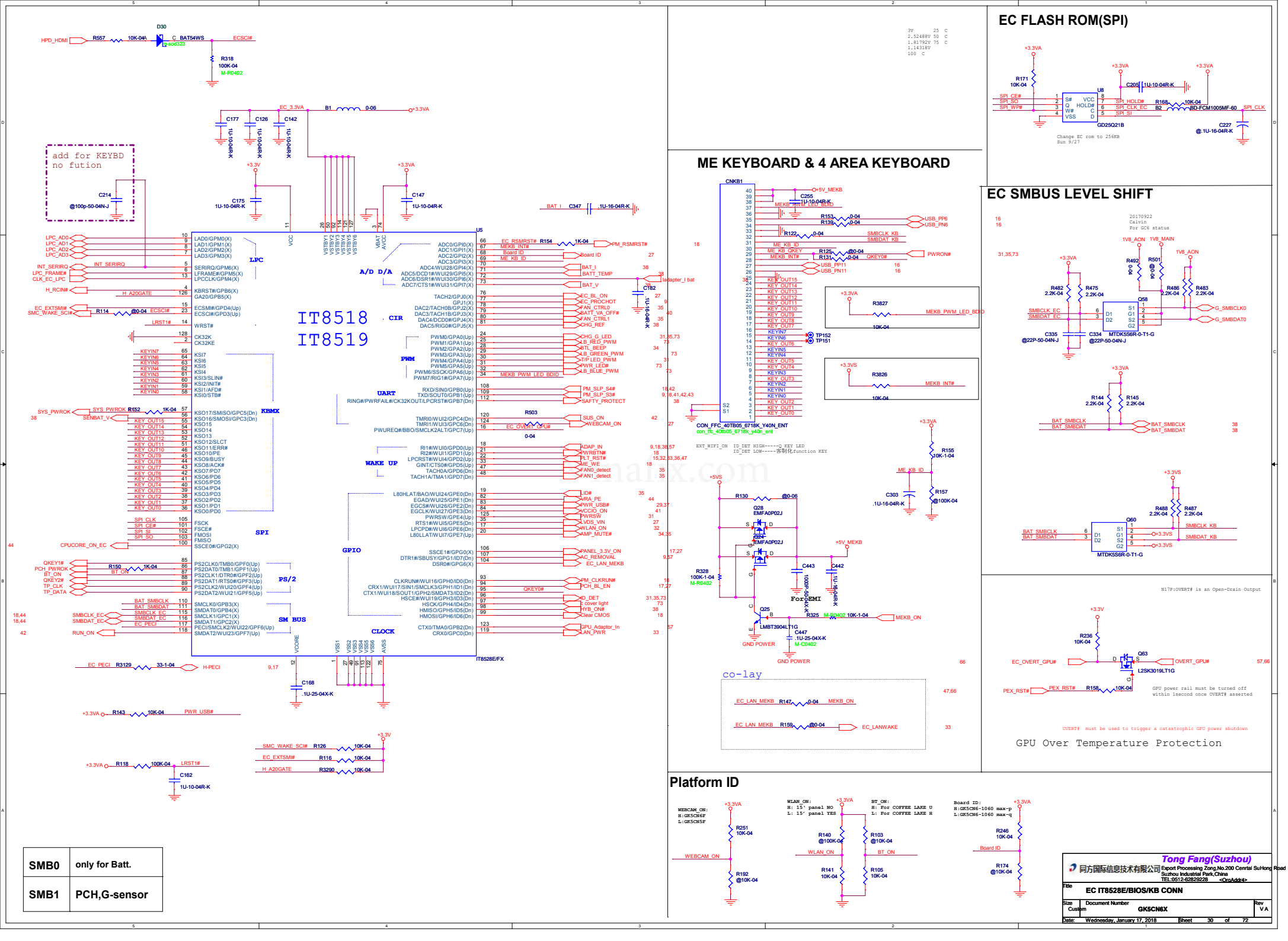
Title	Mini DP	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 29 of 72	


IT8518
IT8519
IT8528E/FX
add for KEYBD
no fution
LPC
A/D D/A
CIR
PWM
UART
WAKE UP
KBMX
SPI
GPIO
PS/2
SM BUS
CLOCK
ME KEYBOARD & 4 AREA KEYBOARD
CON_FFC_40TB05_6718K_Y40N_ENT
EC FLASH ROM(SPI)
GD25Q21B
EC SMBUS LEVEL SHIFT
MTDK5S6R-0-T1-G
GPU Over Temperature Protection
Platform ID
co-lay
SMB0 only for Batt.
SMB1 PCH,G-sensor
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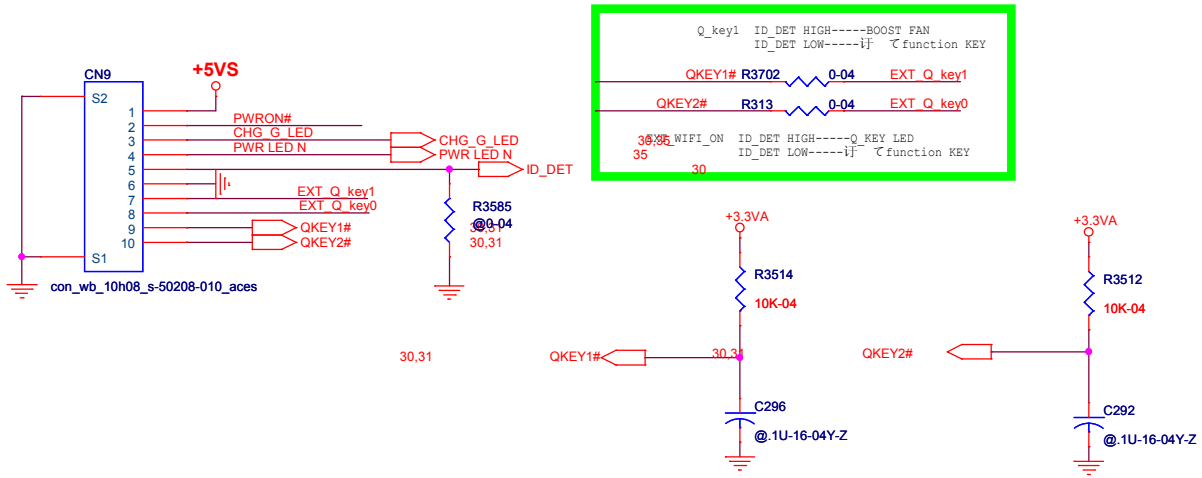
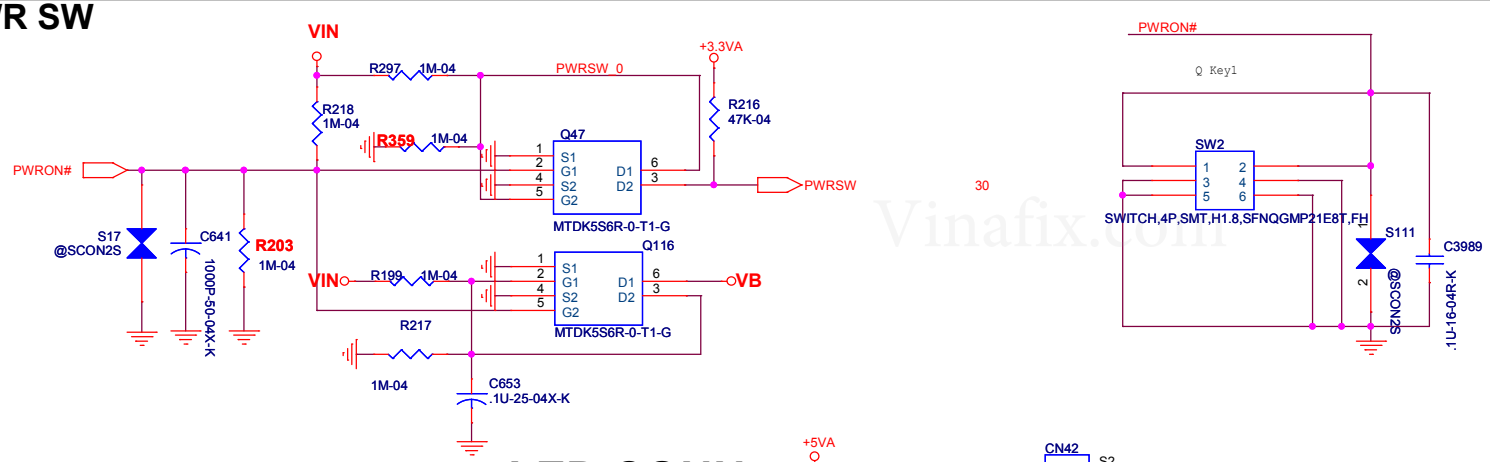
EC IT8528E/BIOS/KB CONN
GK5CN6X

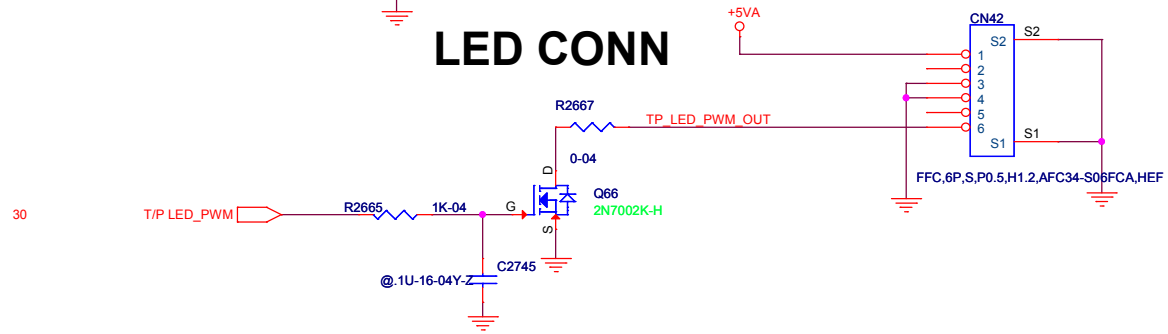
POWER DB CONN.



PWR SW



LED CONN



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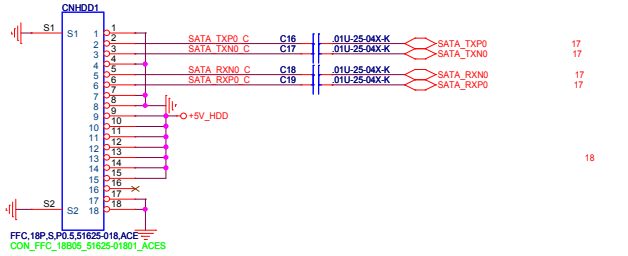
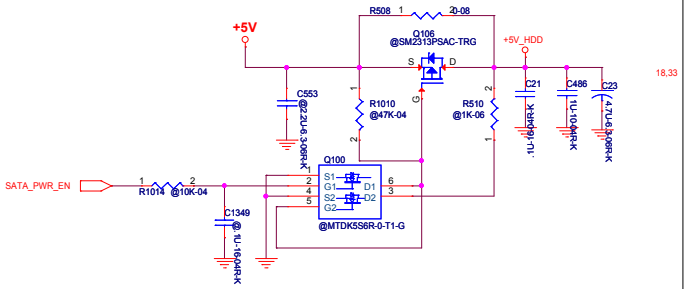
Title: PSW/PWR DB CON		
Size: B	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 31 of 72	

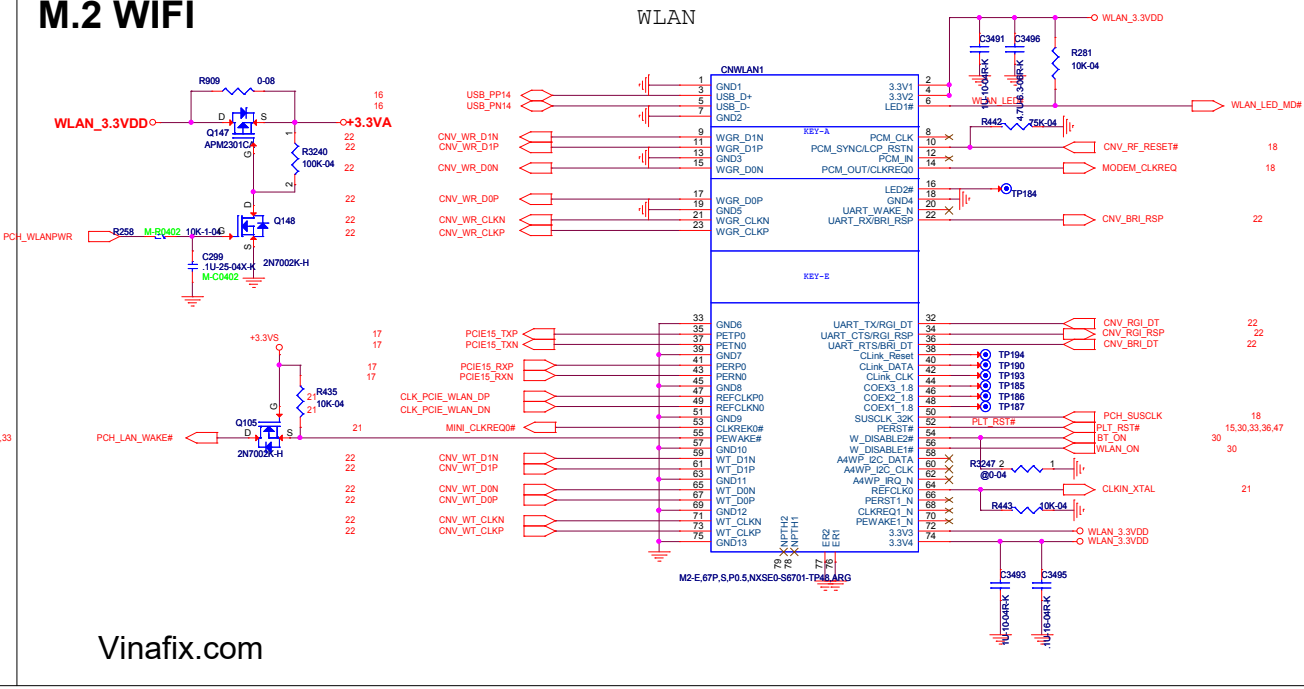
SATA-HDD



For KBL NVMe



M.2 WIFI

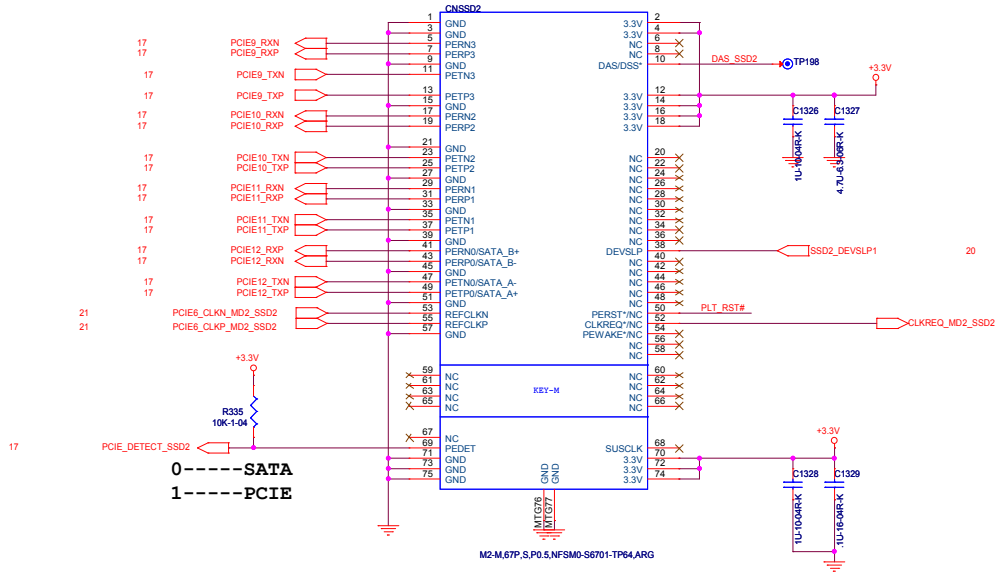


Vinafix.com

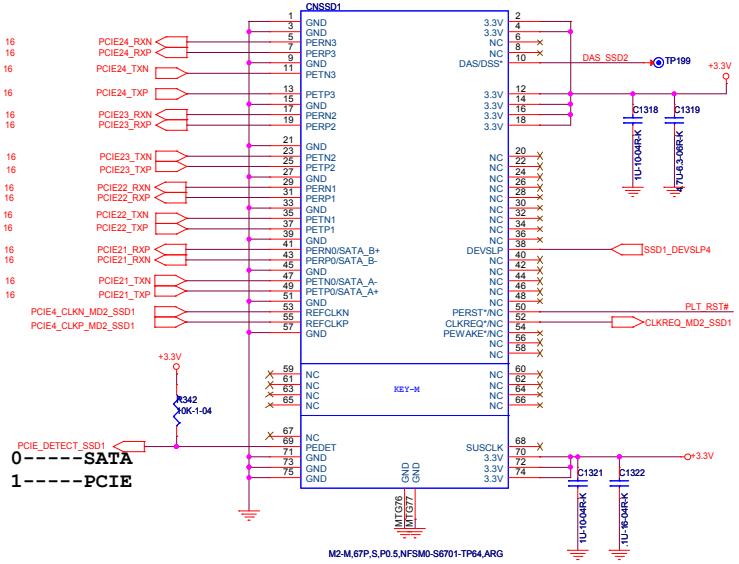
M.2 SSD

Vinafix.com

SSD2



SSD1



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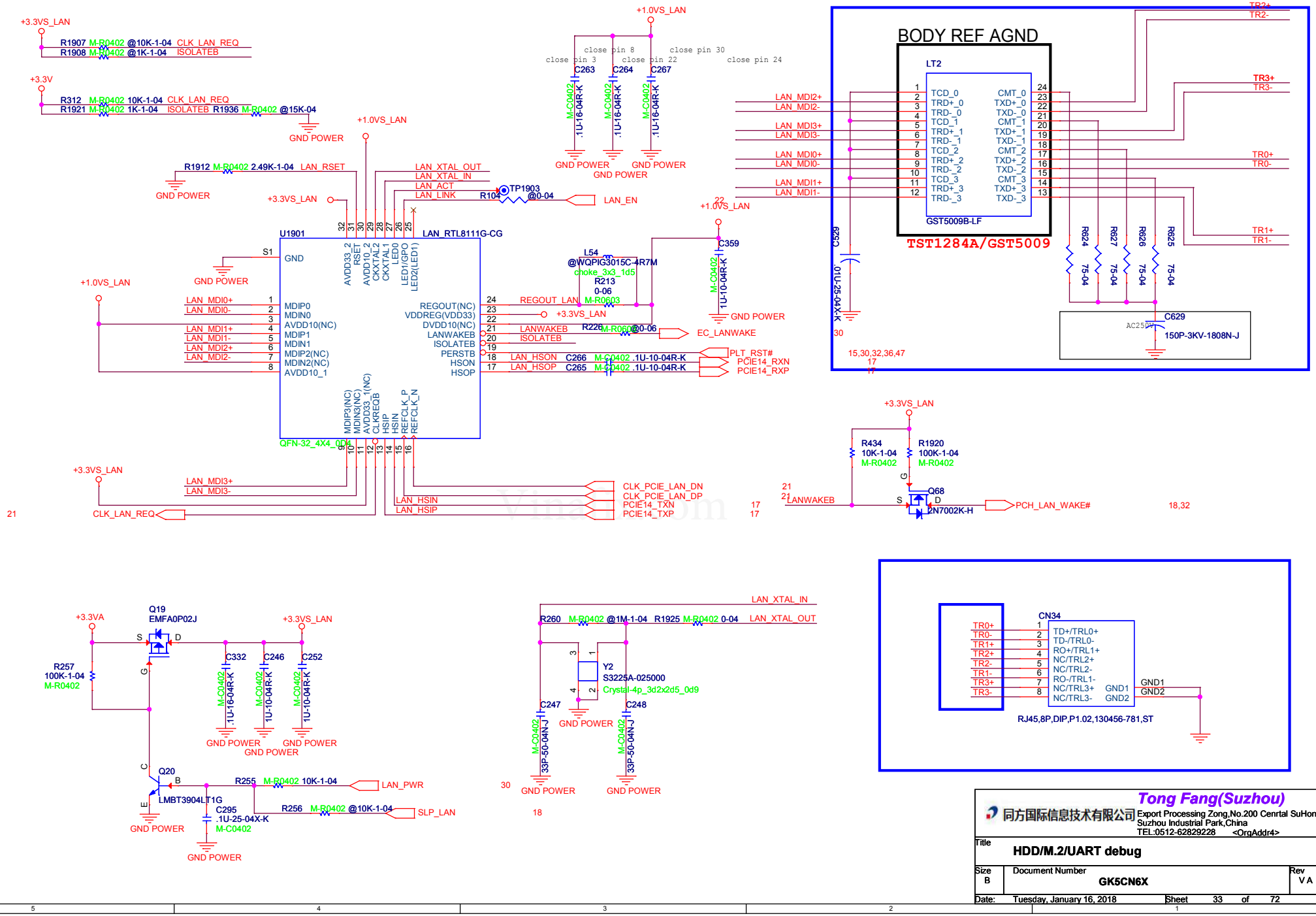
Title	LAN RTL8111	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 32 of 72	



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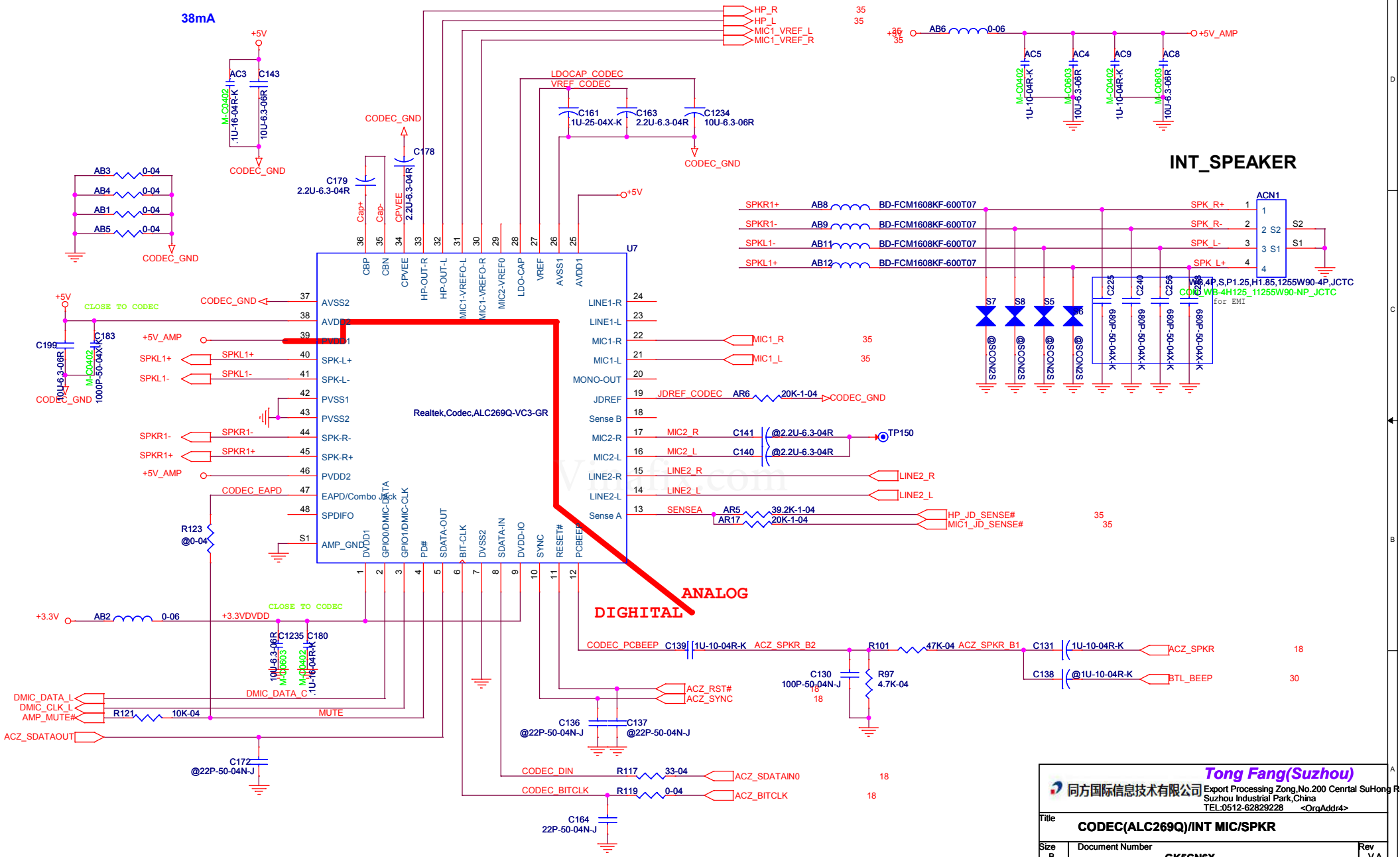
Title	HDD/M.2/UART debug	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 33 of 72	

CODEC ALC269Q

38mA

AMP VDD

INT_SPEAKER



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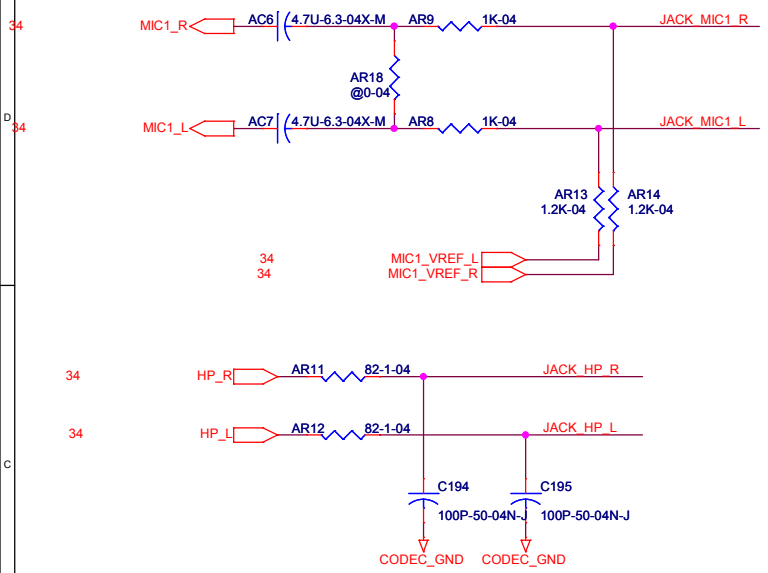
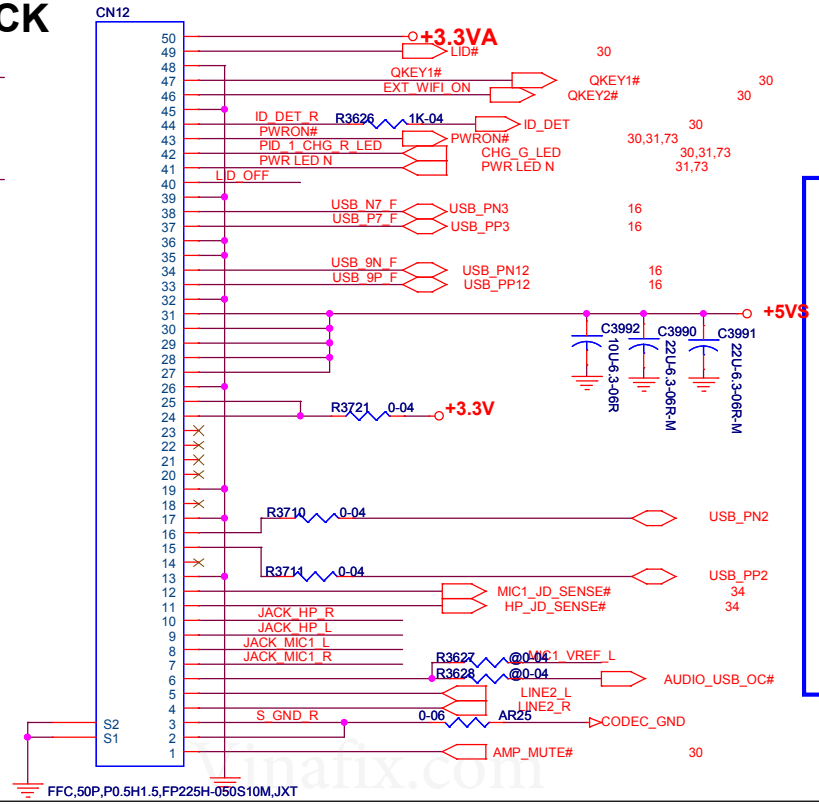
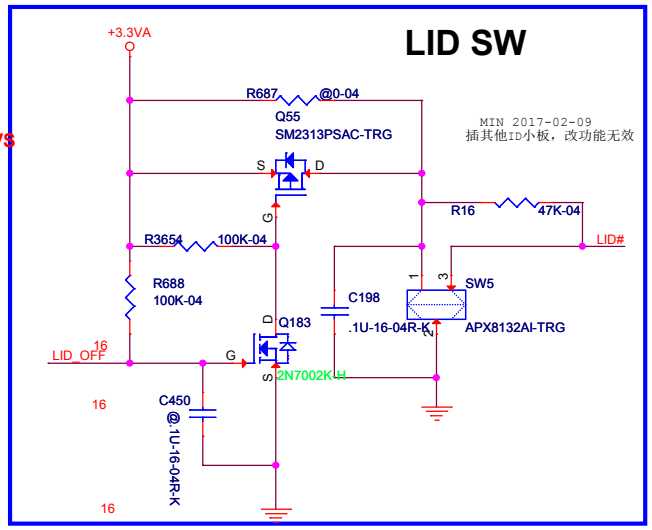
Title	CODEC(ALC269Q)/INT MIC/SPKR
Size B	Document Number GK5CN6X
Rev	V A
Date:	Tuesday, January 16, 2018
Sheet	34 of 72

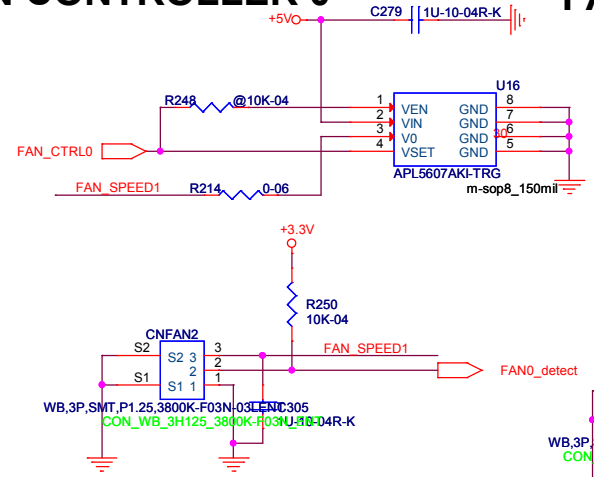
EXT MIC / EXT LINE IN / EXT USB JACK



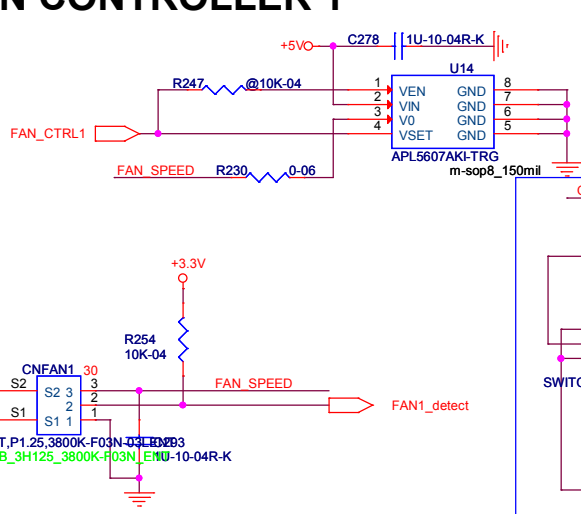


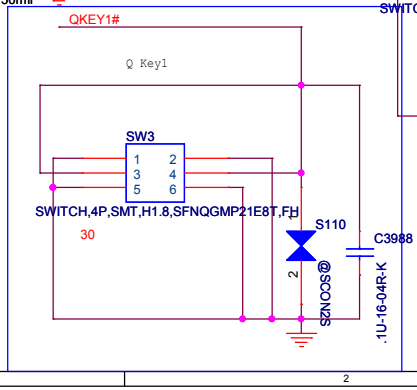


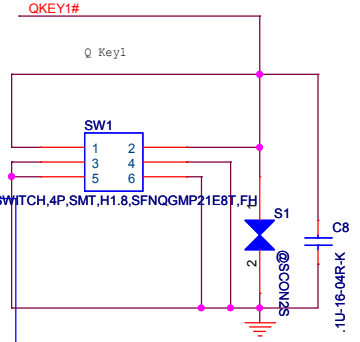
FAN CONTROLLER 0



FAN CONTROLLER 1







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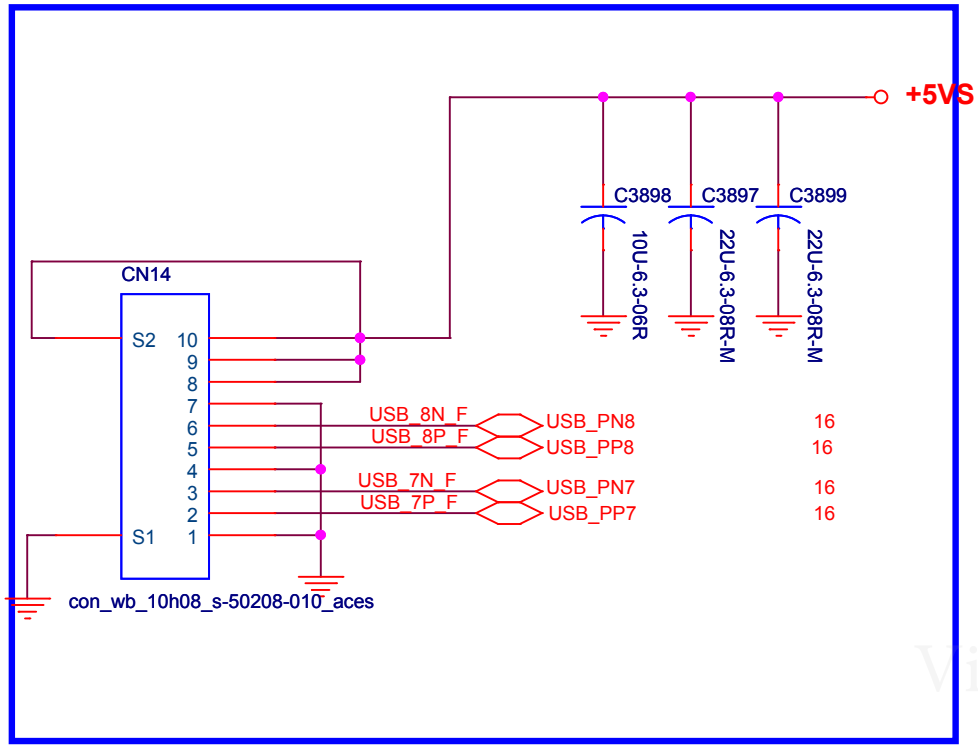
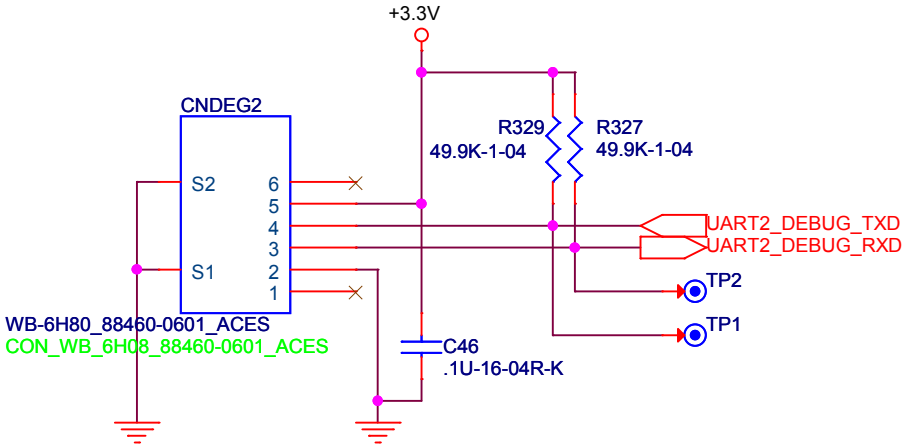
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 35 of 72	

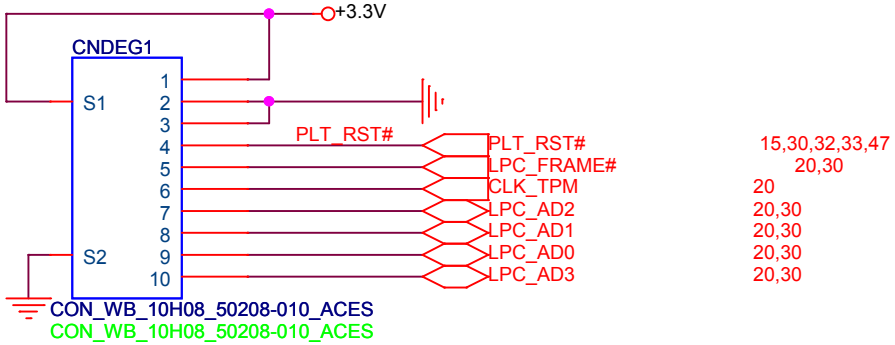
EXT USB2.0 DB



UART debug port



LPC debug port



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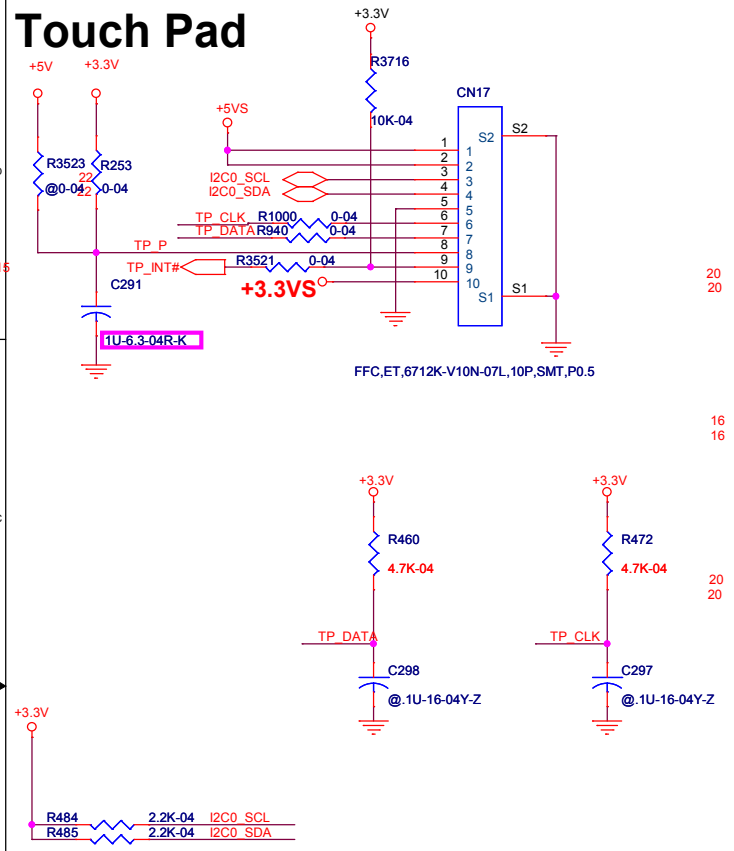
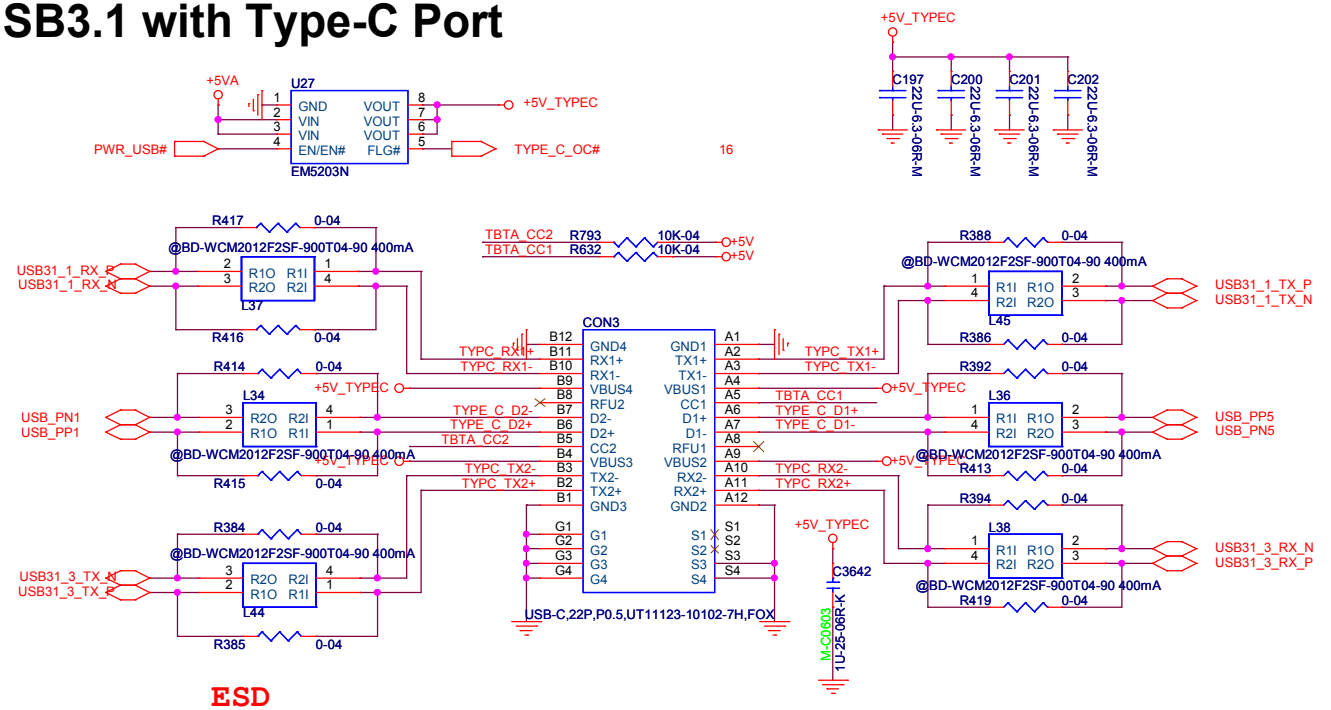
Title	EXT USB3.0	
Size A	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 36 of 72	

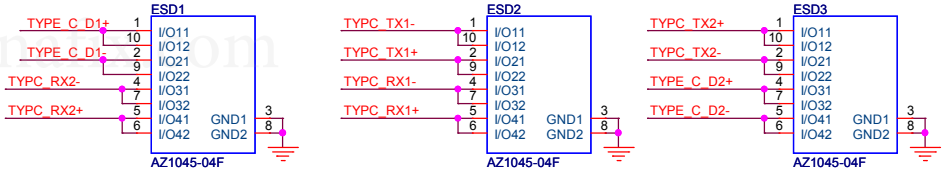
Touch Pad



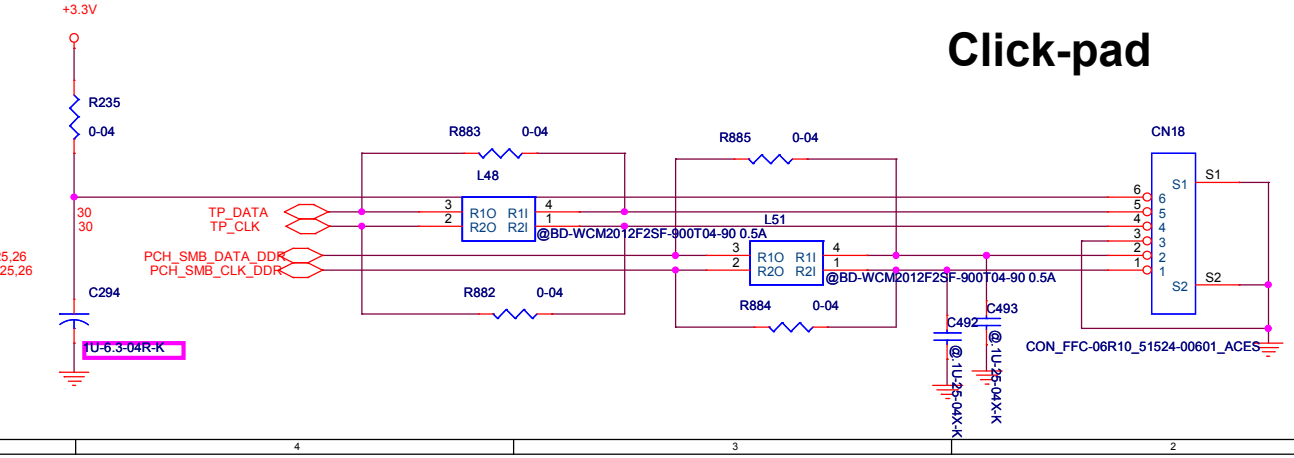
USB3.1 with Type-C Port



ESD



Click-pad



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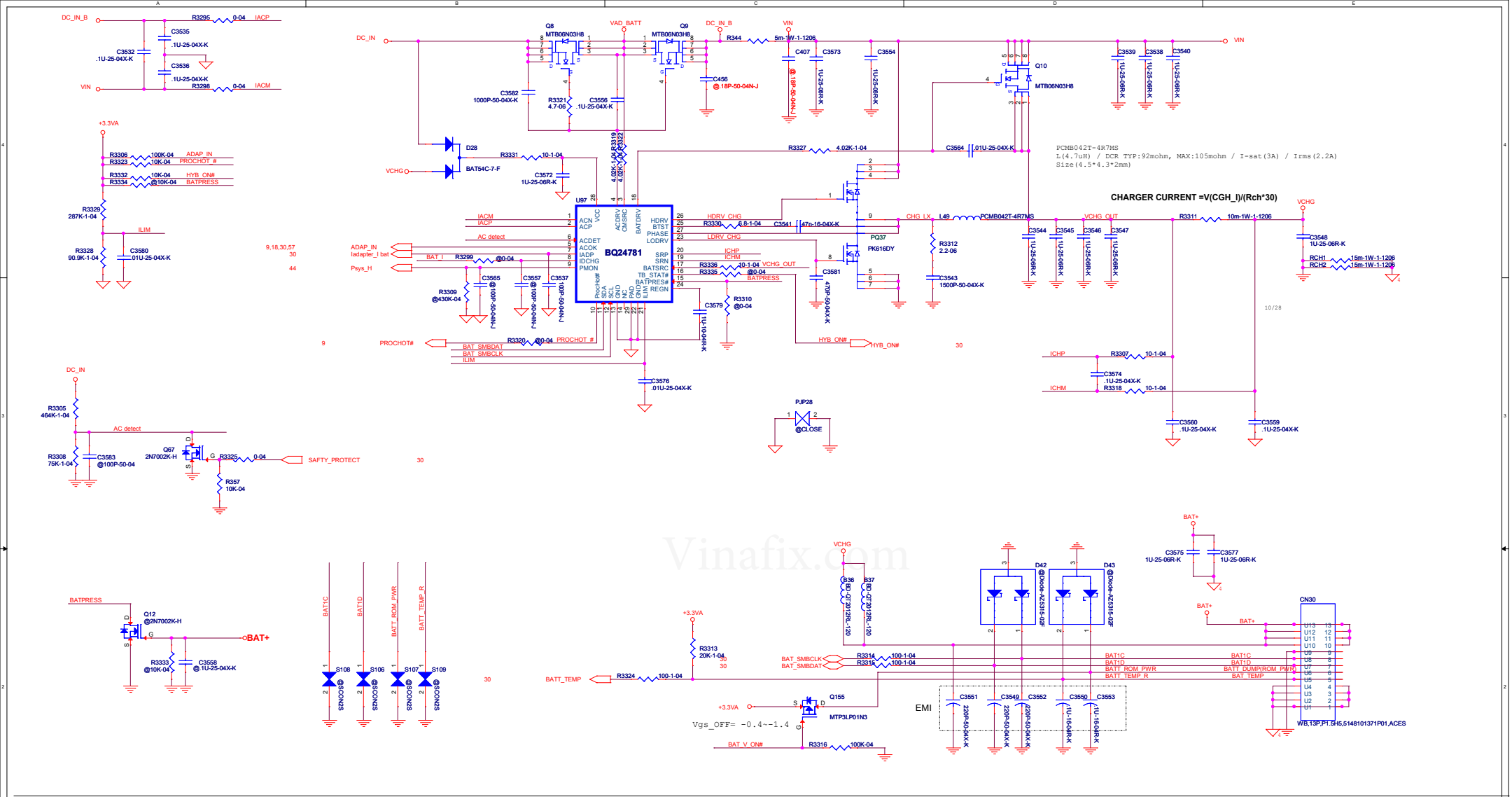
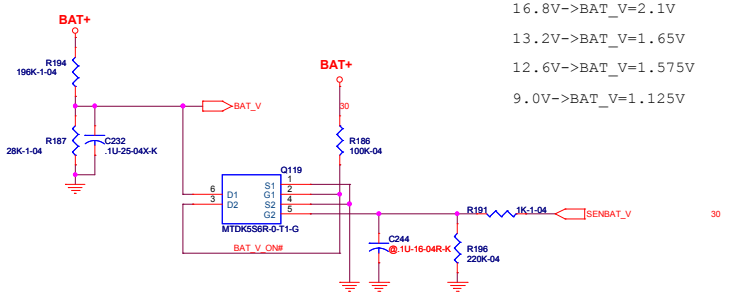
Title	TP/USB/TYPEC	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 37 of 72	



Battery Voltage Detect



17.6V->BAT_V=2.2V

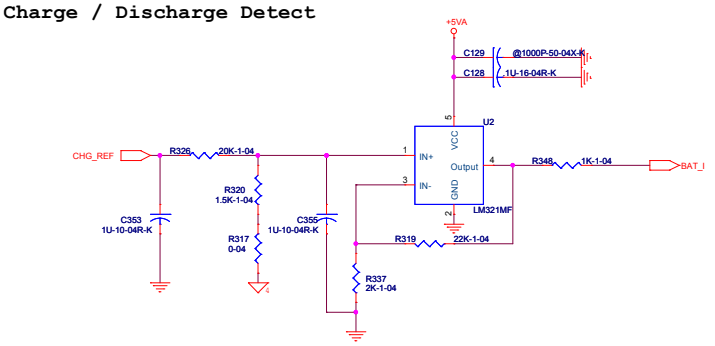
16.8V->BAT_V=2.1V

13.2V->BAT_V=1.65V

12.6V->BAT_V=1.575V

9.0V->BAT_V=1.125V

Charge / Discharge Detect



BAT_I	ICHG (0.0837V/1A)
2.0092V	4A
1.8418V	2A
1.7581V	1A
1.6744V	0A
1.5907V	-1A
1.507V	-2A
1.3396V	-4A
1.1722V	-6A
1.0048V	-8A
0.8374V	-10A

30

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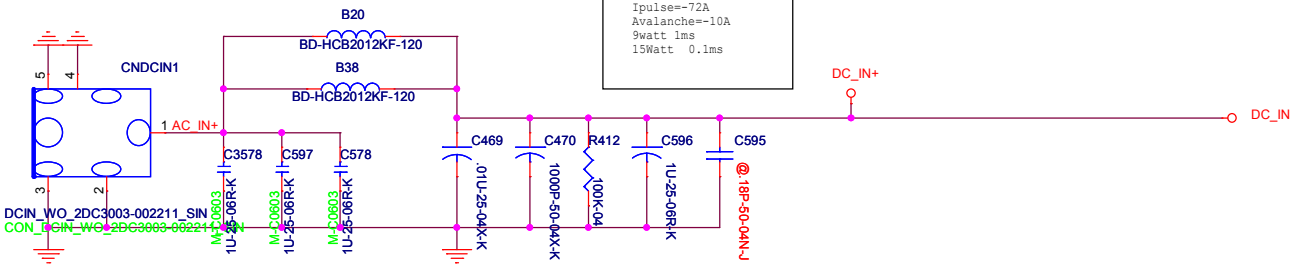
Title: BATT IN/CHARGER(BQ24781)

Size: Custom | Document Number: GK5CN6X | Rev: V A

Date: Tuesday, January 16, 2018 | Sheet 38 of 72

DC IN



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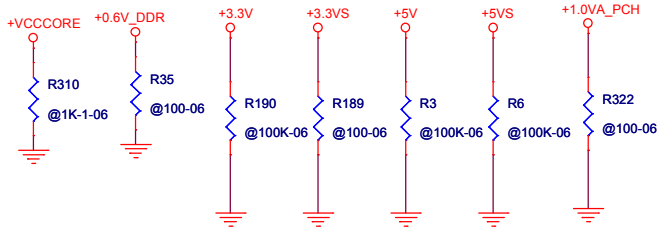
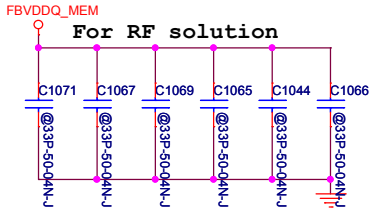
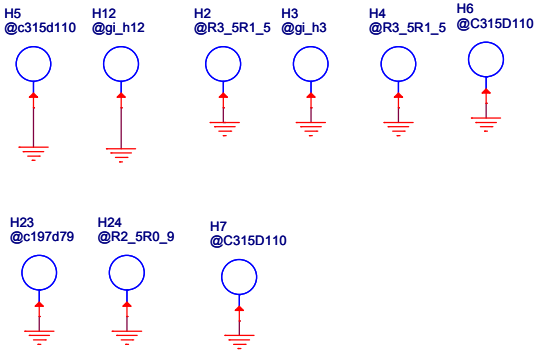
Discharge Resistor



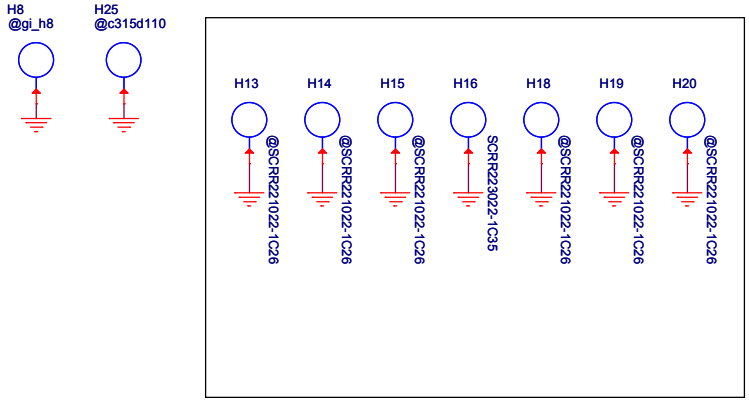
HIGH-SPEED CAP

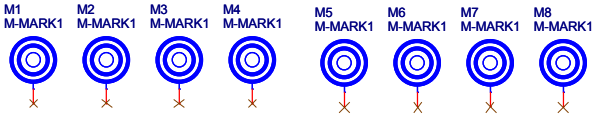


PCB HOLE



THERMAL HOLE





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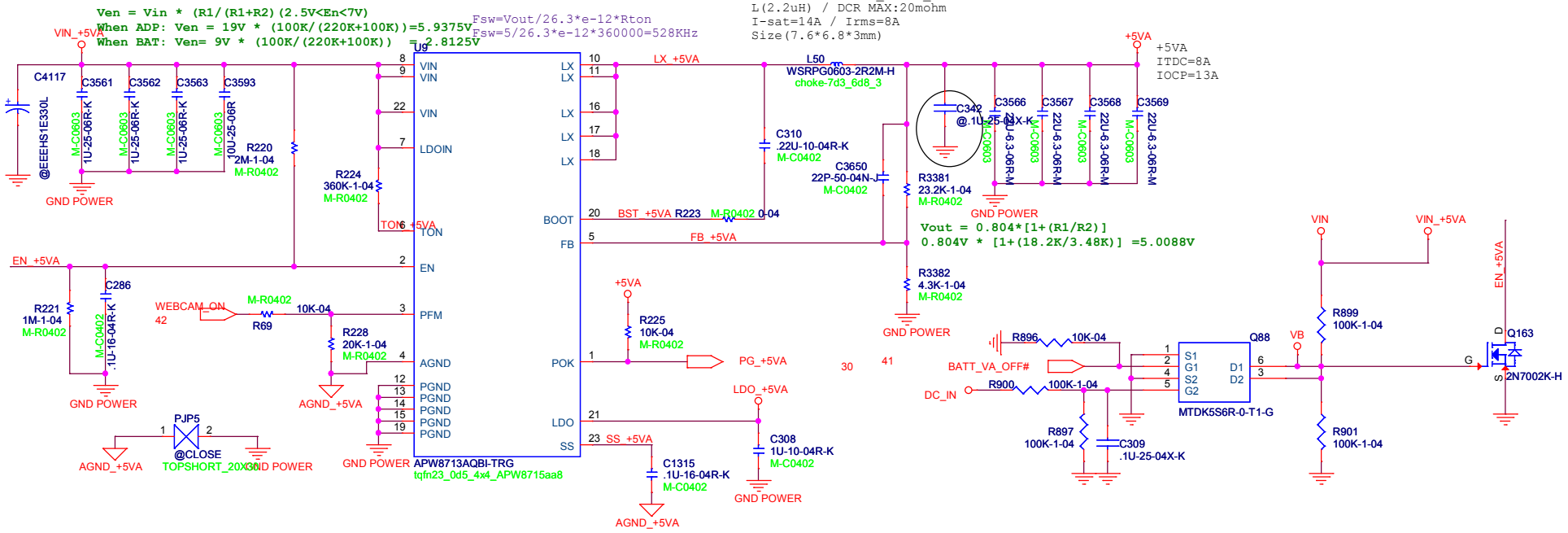
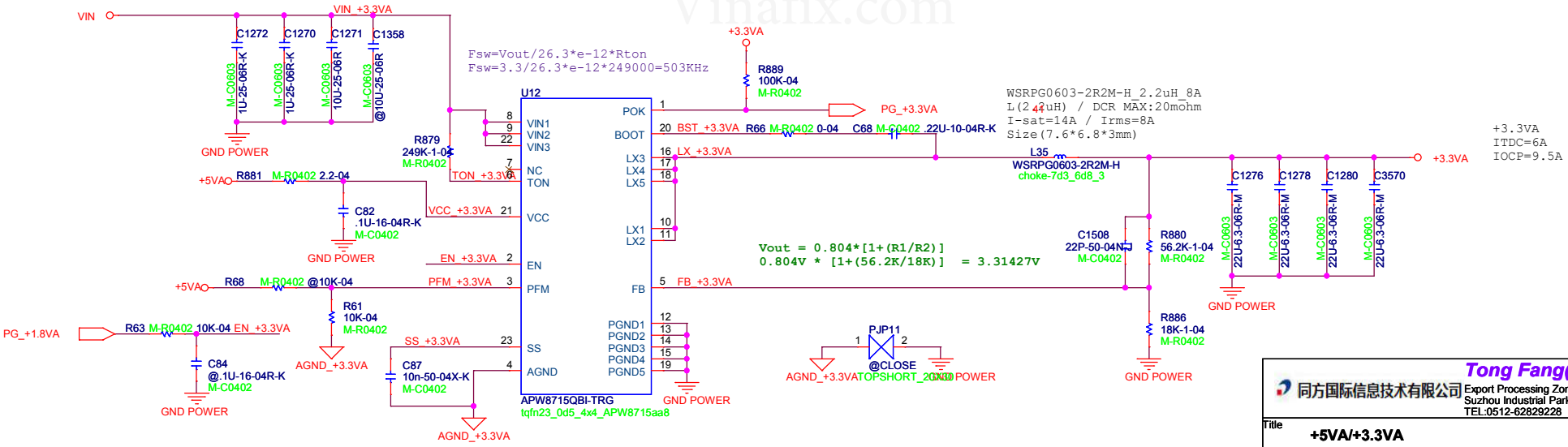
Title	DC IN/TPM/D-Resis/HOLE	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 39 of 72	

5VAL Converter





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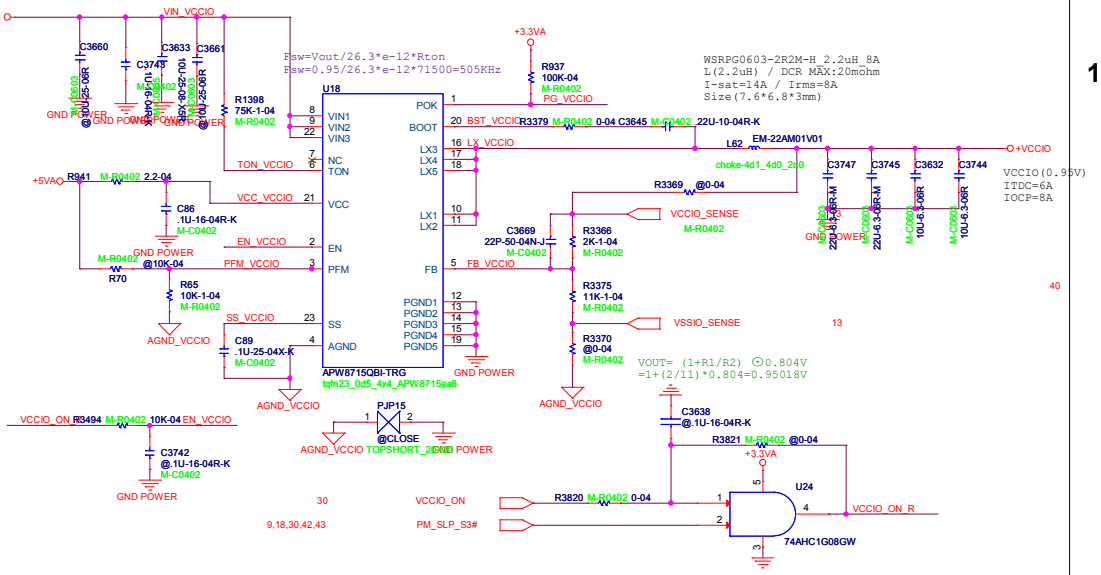
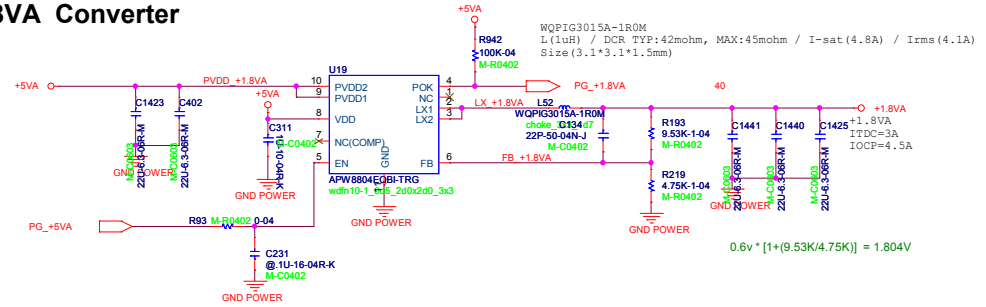
Title: +5VA/+3.3VA		
Size: B	Document Number: GK5CN6X	Rev: V A
Date: Thursday, January 18, 2018	Sheet 40 of 72	

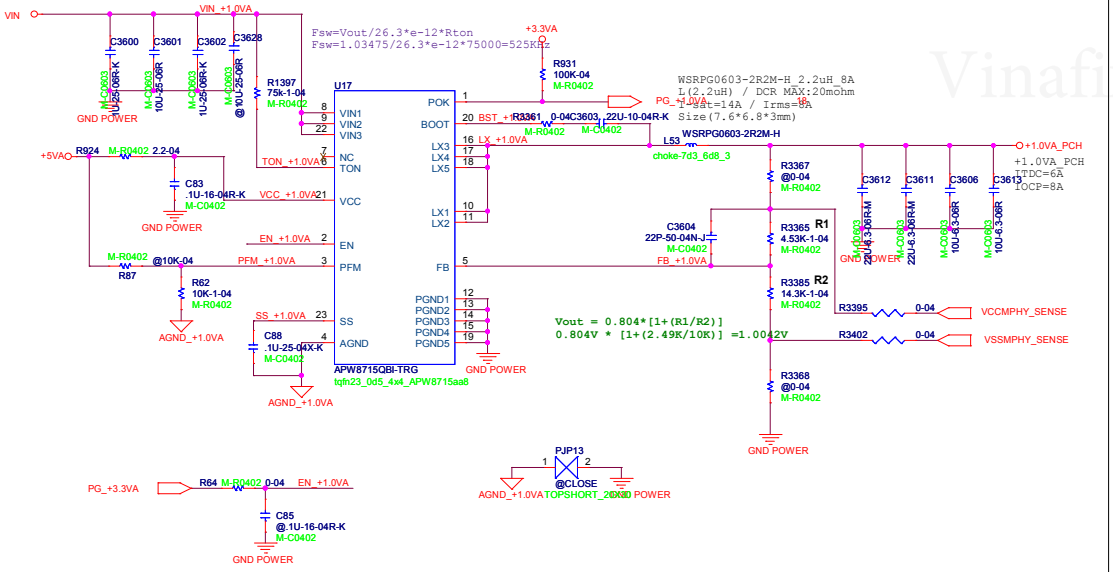
VCCIO Converter



1.8VA Converter



1.0VA Converter



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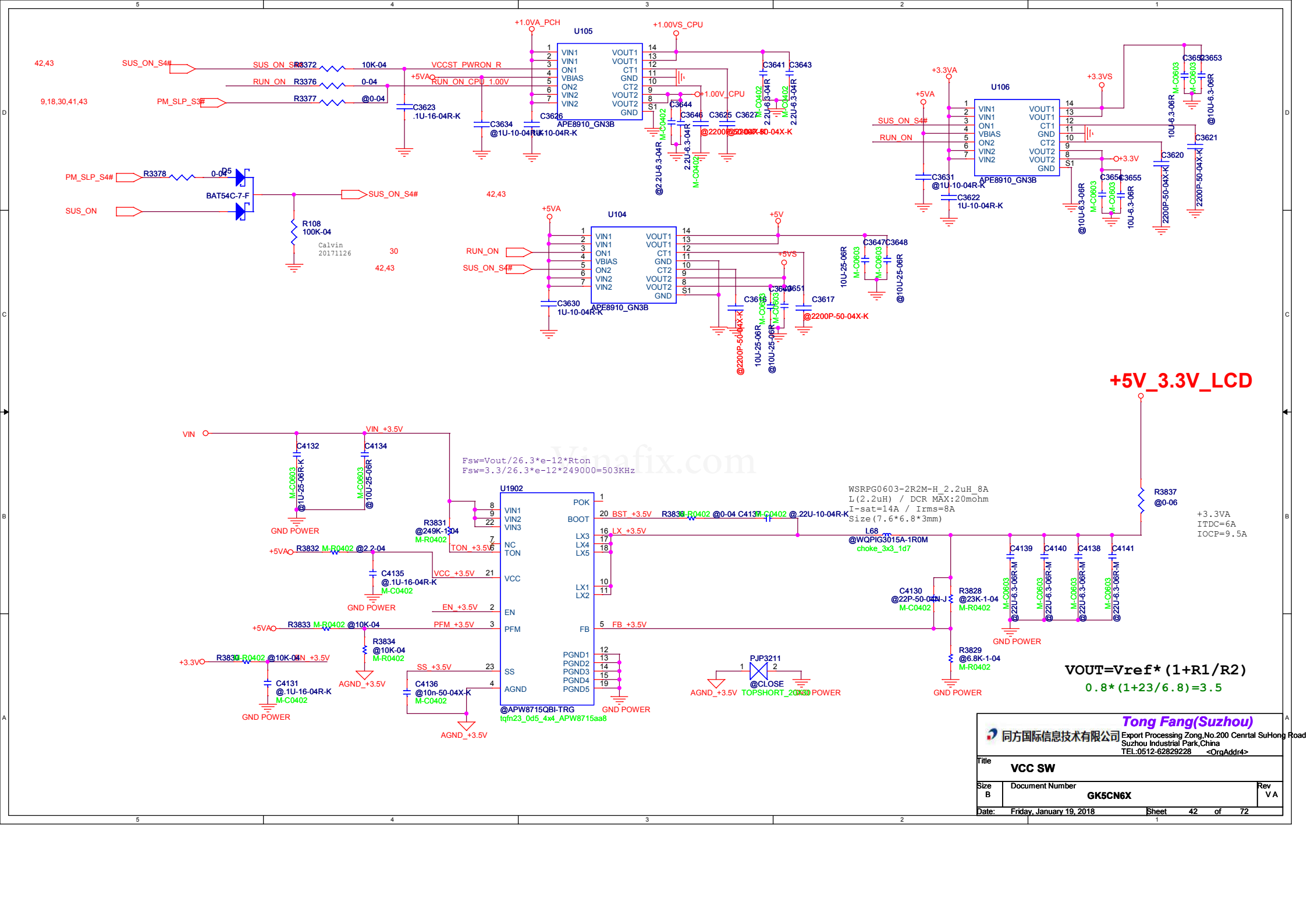
Title	+1.0VA_PCH/VCCIO/+1.8VA	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Friday, January 19, 2018	Sheet 41 of 72	


+5V_3.3V_LCD
U105
APE8910_GN3B
U106
APE8910_GN3B
U104
APE8910_GN3B
U1902
@APW8715QBI-TRG
tqfn23_0d5_4x4_APW8715aa8
SUS_ON_S4#
RUN_ON
PM_SLP_S4#
SUS_ON
BAT54C-7-F
R108 100K-04
VCCST_PWRON_R
RUN_ON_CPU 1.00V
+1.00V_CPU
+1.00VS_CPU
+1.0VA_PCH
+5VA
+3.3VA
+3.3VS
+5V
+5VS
+3.3V
VIN
VIN_+3.5V
Fsw=Vout/26.3*e-12*Rton
Fsw=3.3/26.3*e-12*249000=503KHz
WSRPG0603-2R2M-H_2.2uH_8A
L(2.2uH) / DCR MAX:20mohm
I-sat=14A / Irms=8A
Size(7.6*6.8*3mm)
L68 @WQPIG3015A-1R0M
choke_3x3_1d7
+3.3VA
ITDC=6A
IOCP=9.5A
VOUT=Vref*(1+R1/R2)
0.8*(1+23/6.8)=3.5
PJP3211
@CLOSE
TOPSHORT_20mil
GND POWER
AGND_+3.5V
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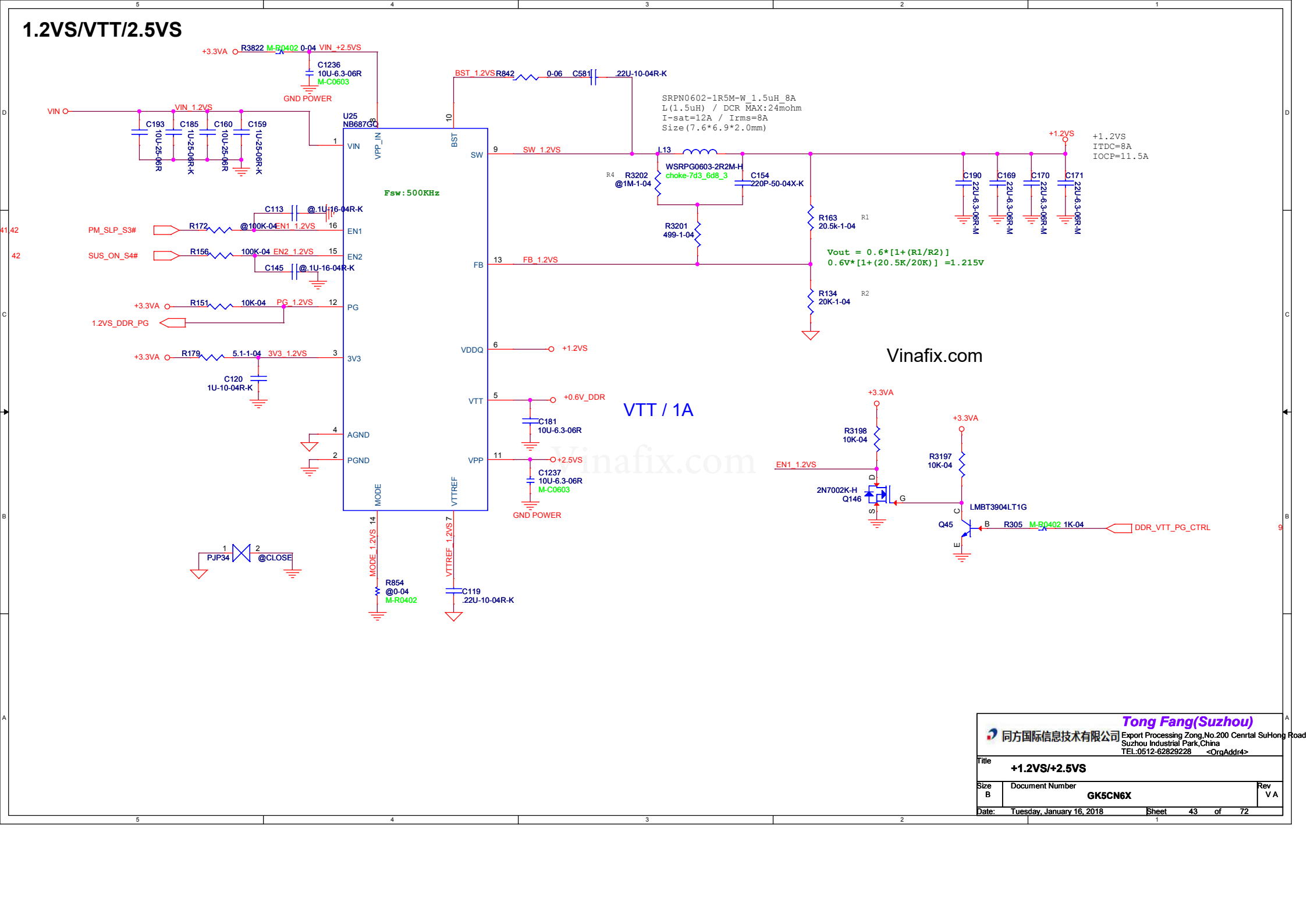
Title VCC SW
Size B
Document Number GK5CN6X
Rev V A
Date: Friday, January 19, 2018
Sheet 42 of 72

1.2VS/VTT/2.5VS



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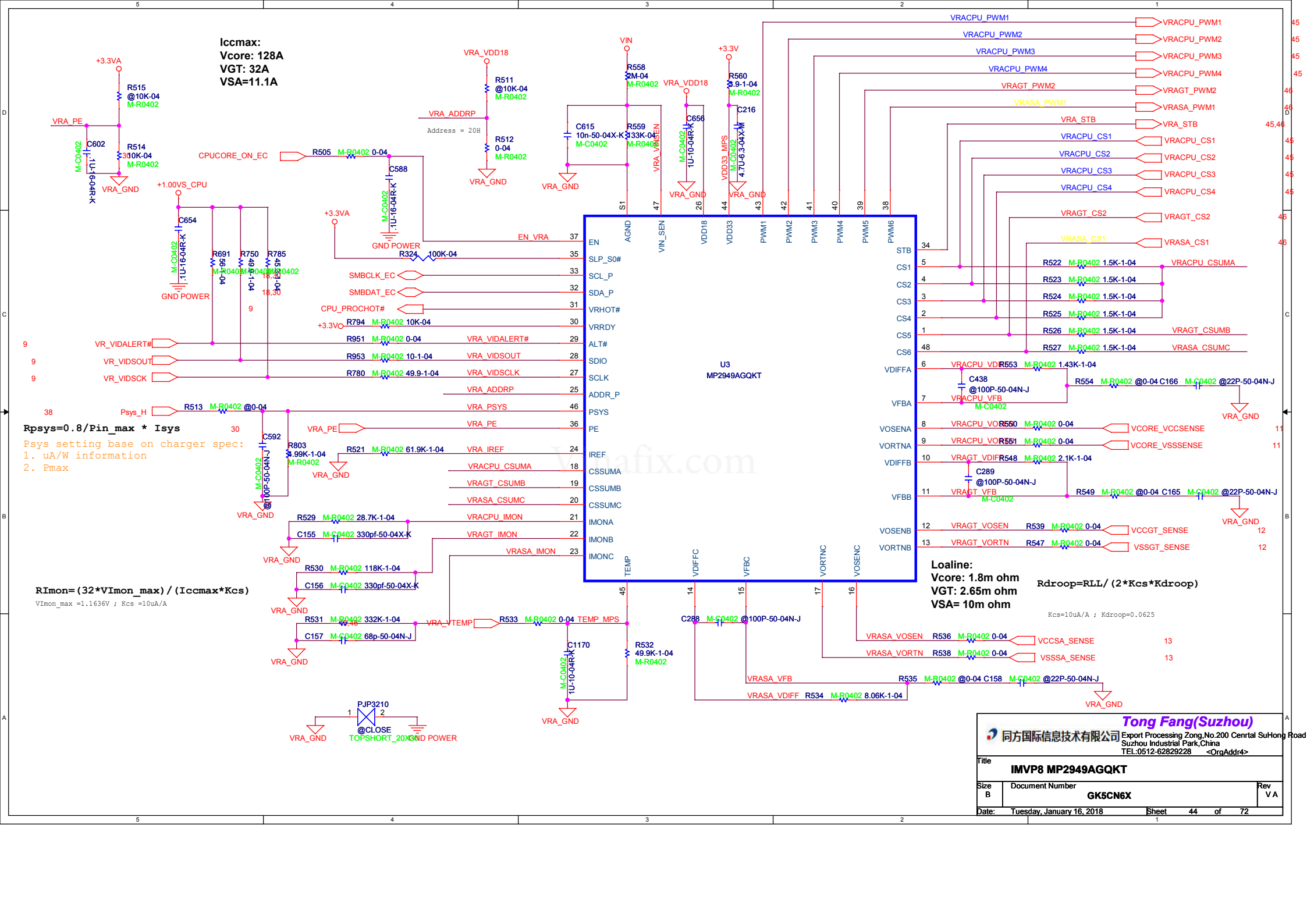
Title	+1.2VS/+2.5VS
Size B	Document Number GK5CN6X Rev V A
Date: Tuesday, January 16, 2018	Sheet 43 of 72


Iccmax:
Vcore: 128A
VGT: 32A
VSA=11.1A
U3
MP2949AGQKT
Rpsys=0.8/Pin_max * Isys
Psys setting base on charger spec:
1. uA/W information
2. Pmax
RImon=(32*VImon_max)/(Iccmax*Kcs)
VImon_max =1.1636V ; Kcs =10uA/A
Loaline:
Vcore: 1.8m ohm
VGT: 2.65m ohm
VSA= 10m ohm
Rdroop=RLL/(2*Kcs*Kdroop)
Kcs=10uA/A ; Kdroop=0.0625
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IMVP8 MP2949AGQKT
GK5CN6X
Tuesday, January 16, 2018

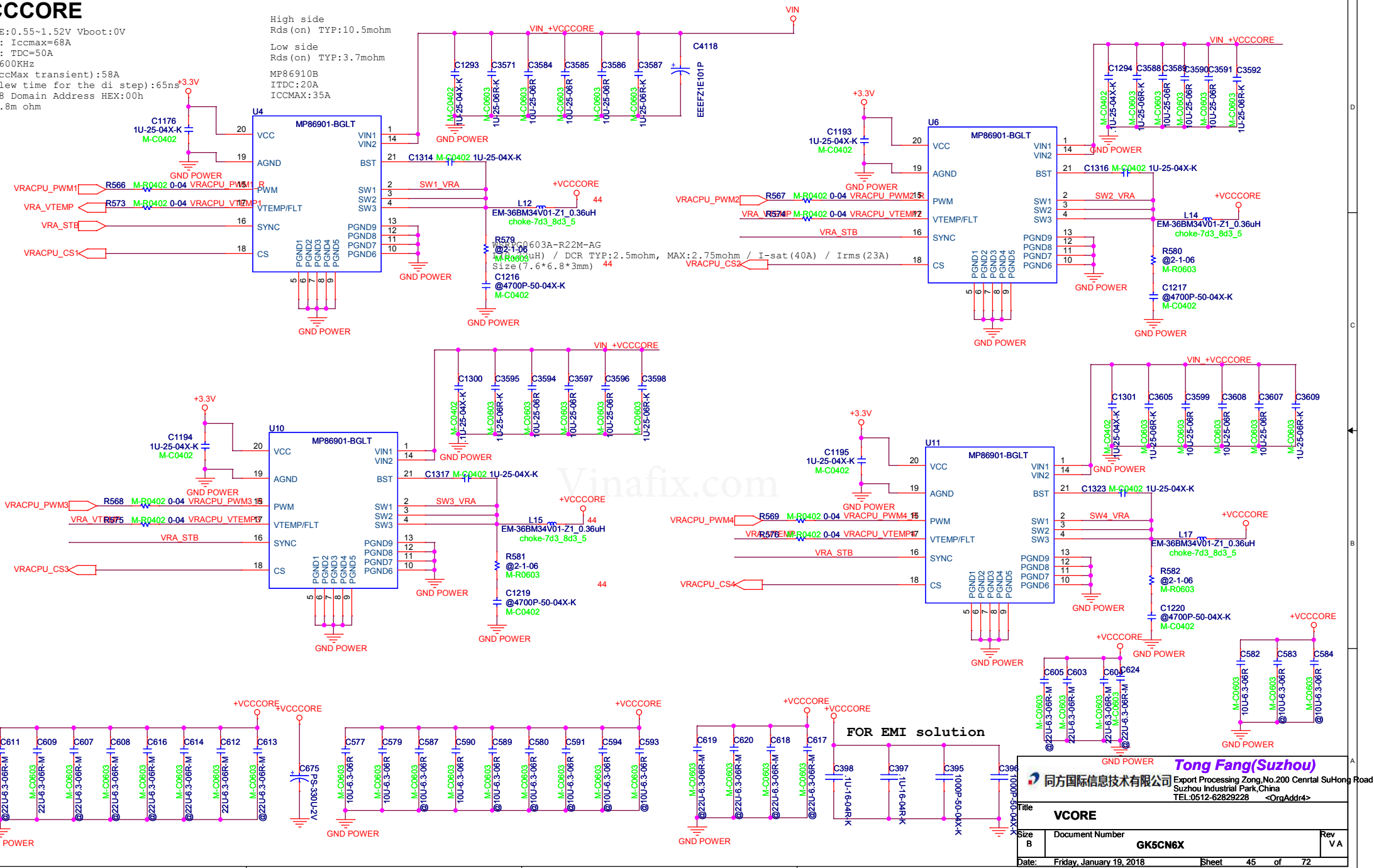
VCCCORE

VCORE:0.55~1.52V Vboot:0V
Core: Iccmax=68A
Core: TDC=50A
FSW:600KHz
di(IccMax transient):58A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:00h
LL:1.8m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



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Title	VCORE	
Size B	Document Number GK5CN6X	Rev V A
Date: Friday, January 19, 2018	Sheet 45 of 72	

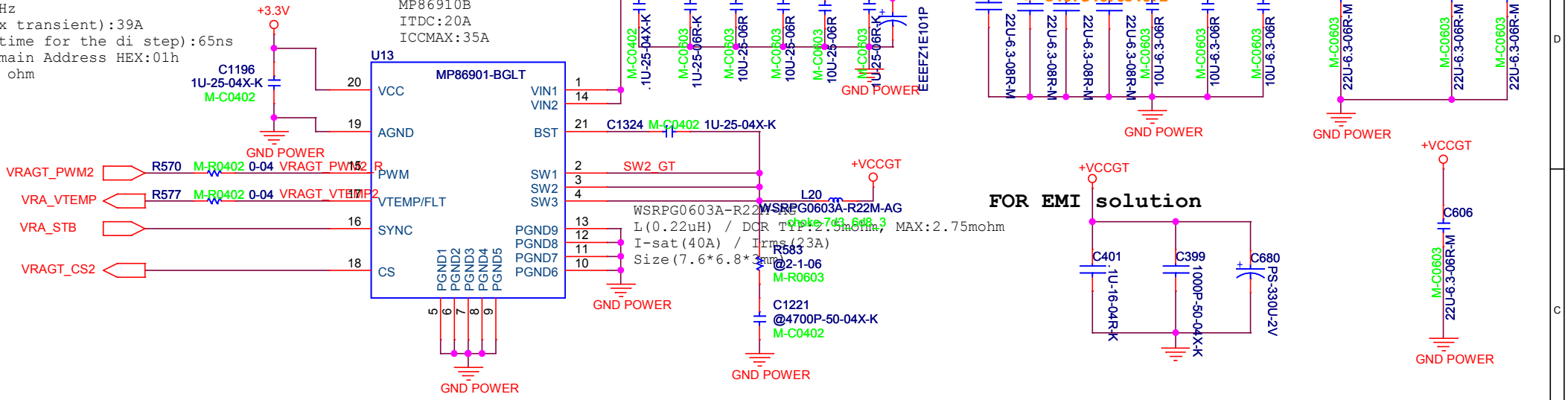
VCCGT

VGT:0.55V~1.52V Vboot:0V
GT: Iccmax=55A
GT: TDC=25A
FSW:600KHz
di(IccMax transient):39A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:01h
LL:2.65m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



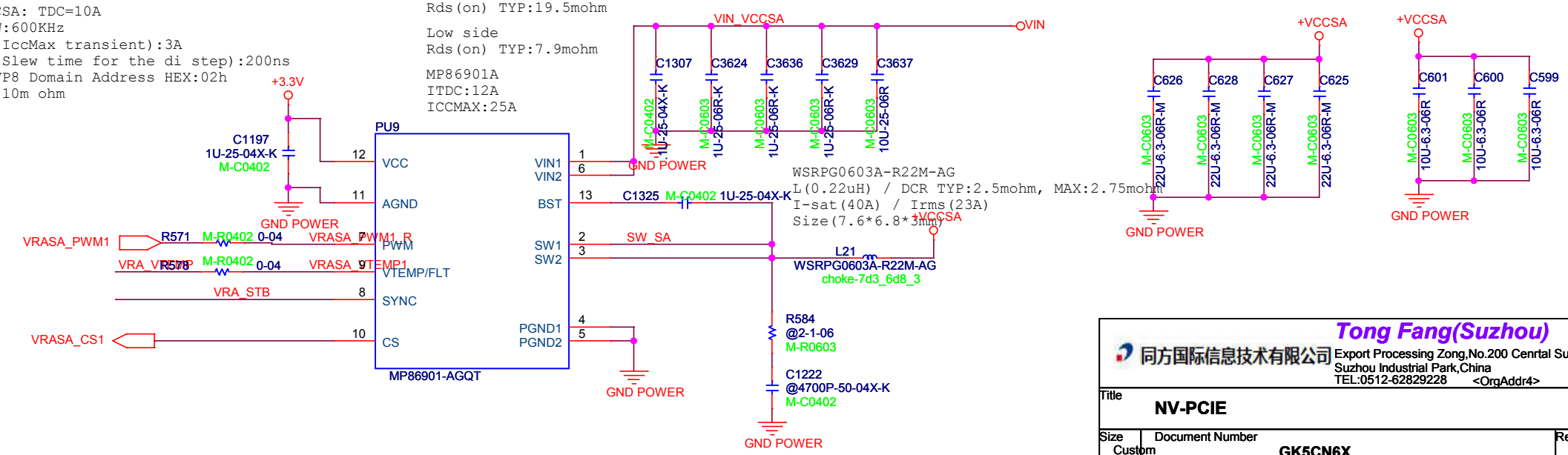
VCCSA

VCCSA:0.55~1.52V Vboot:1.05V
VCCSA: Iccmax=11.1A
VCCSA: TDC=10A
FSW:600KHz
di(IccMax transient):3A
dt(Slew time for the di step):200ns
IMVP8 Domain Address HEX:02h
LL:10m ohm

High side
Rds(on) TYP:19.5mohm

Low side
Rds(on) TYP:7.9mohm

MP86901A
ITDC:12A
ICCMAX:25A



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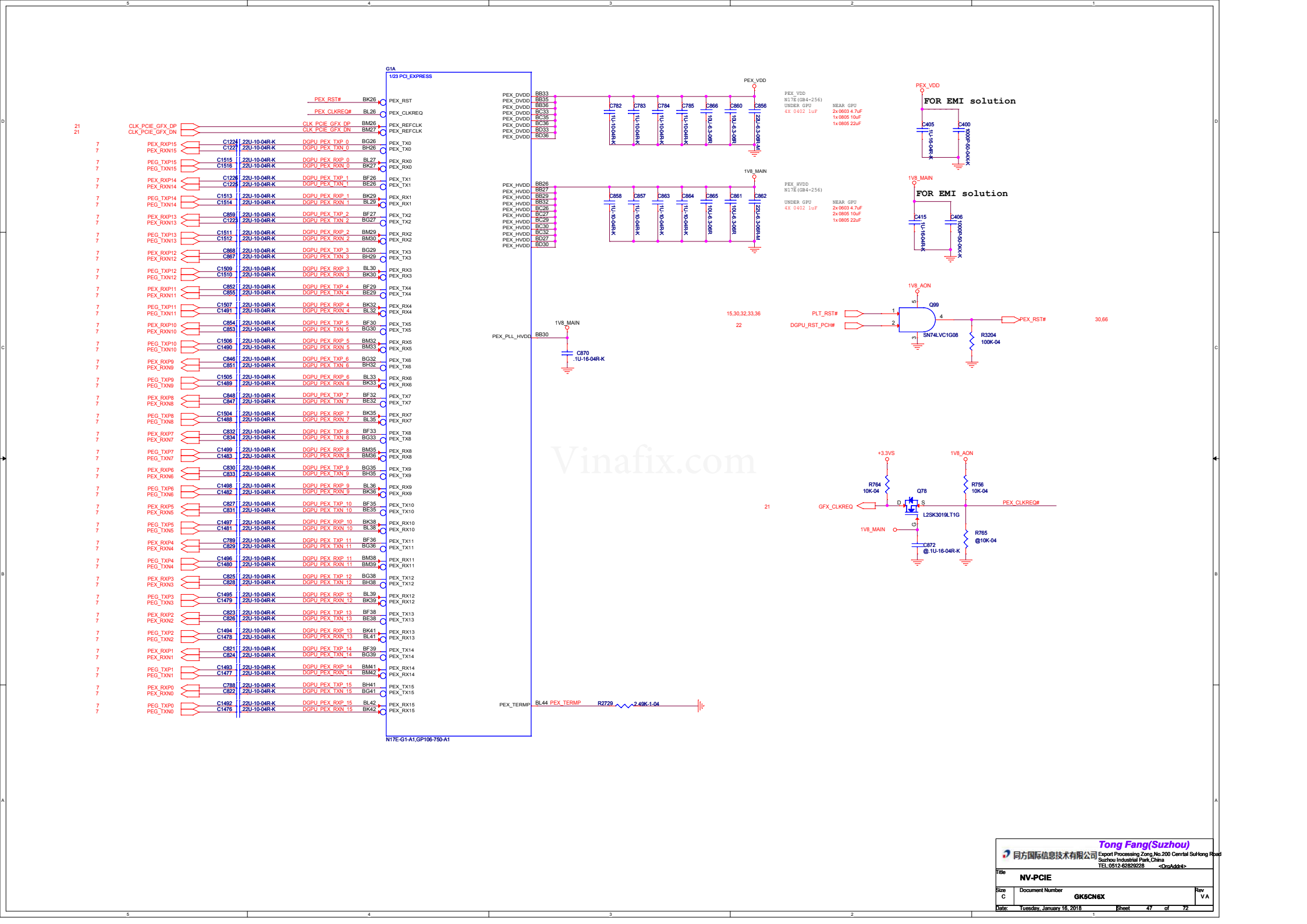
TEL:0512-62829228 <OrgAddr4>

Title	NV-PCIE	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 46 of 72	



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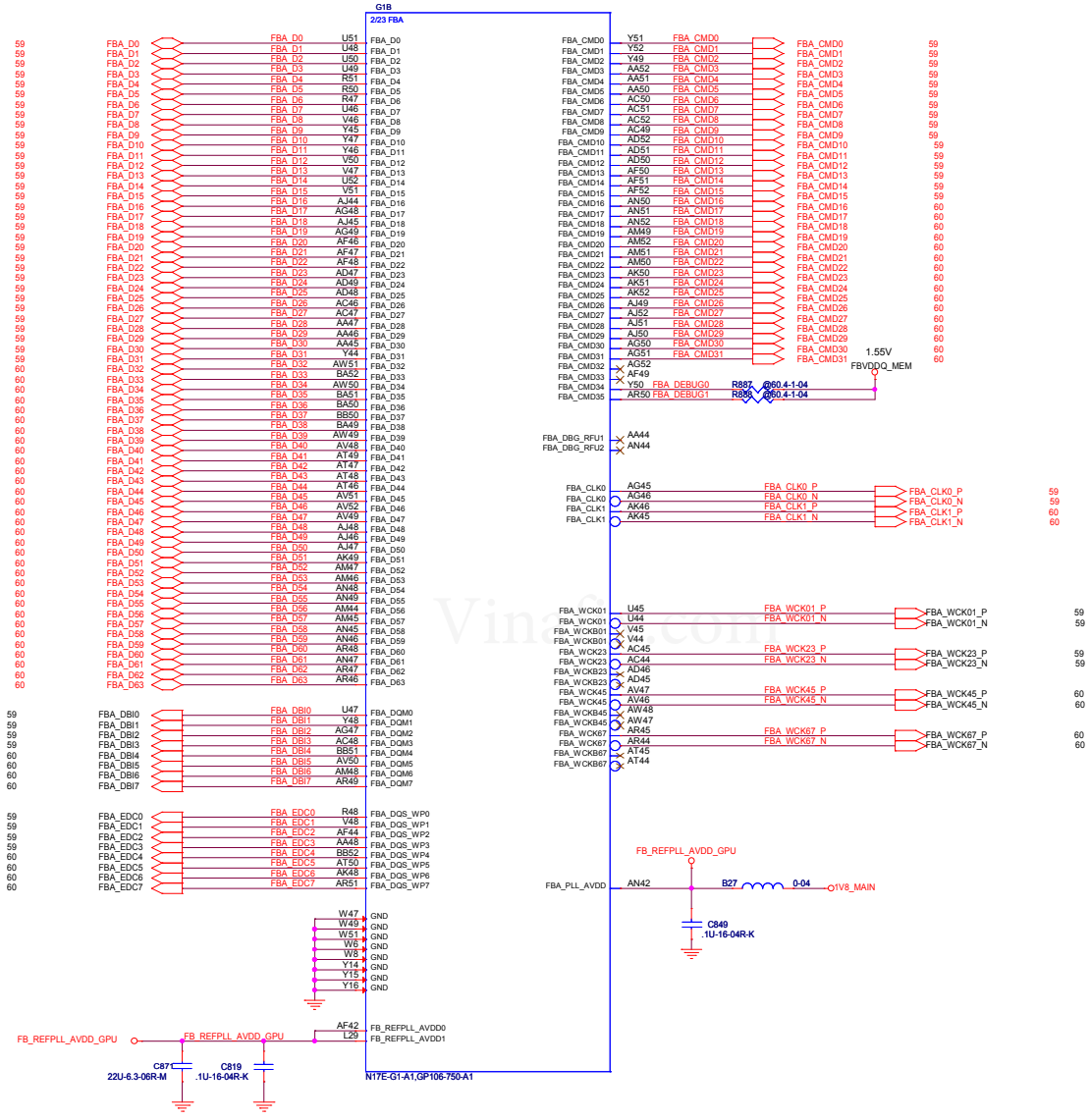
TEL	0512-62829228
Title	NV-PCIE
Size	C
Document Number	GK5CN6X
Rev	V A
Date	Tuesday, January 16, 2018
Sheet	47 of 72



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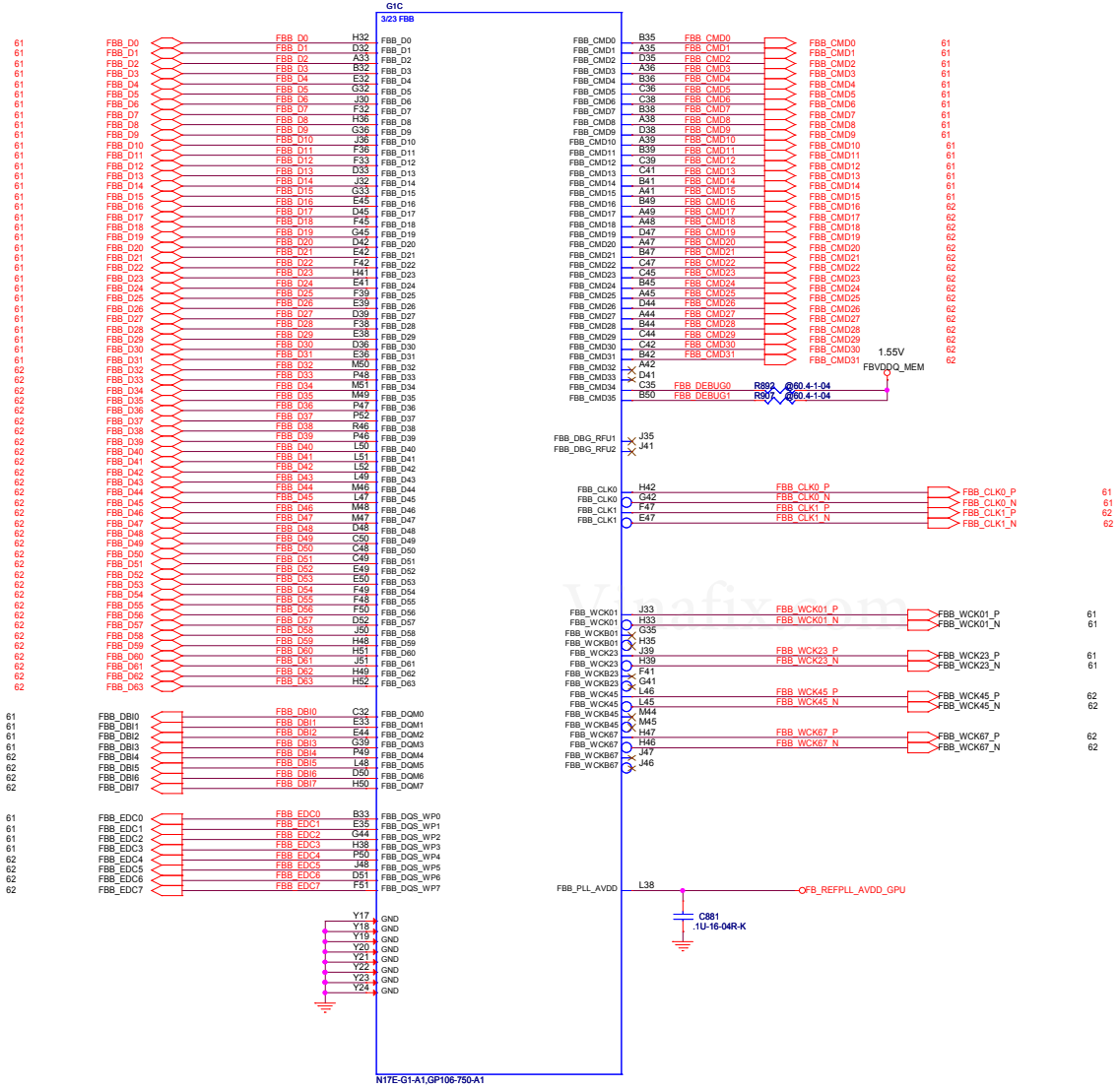
Title	NV-BIOS/XTAL	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 48 of 72	



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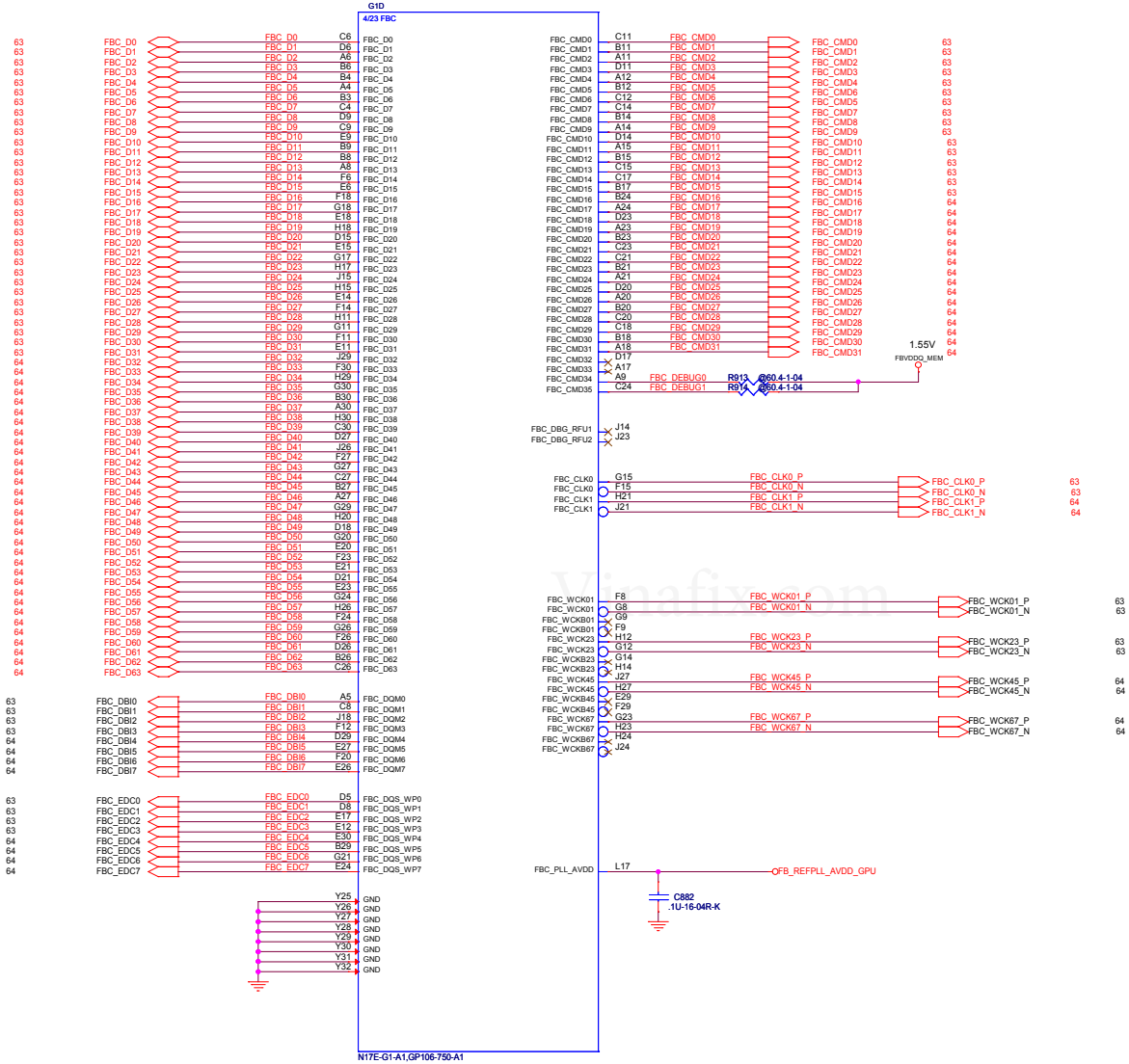
Title	NV-Frame Buffer B	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 49 of 72	



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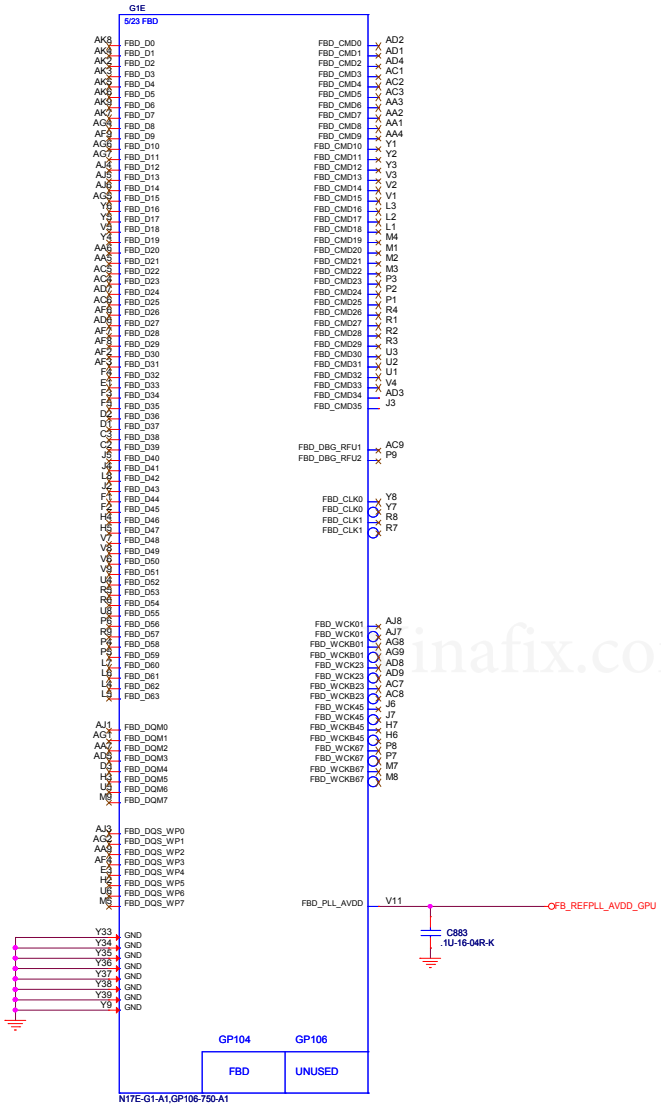
TEL:0512-62829228 <OrgAddr4>

Title	NV-Frame Buffer C	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 50 of 72	



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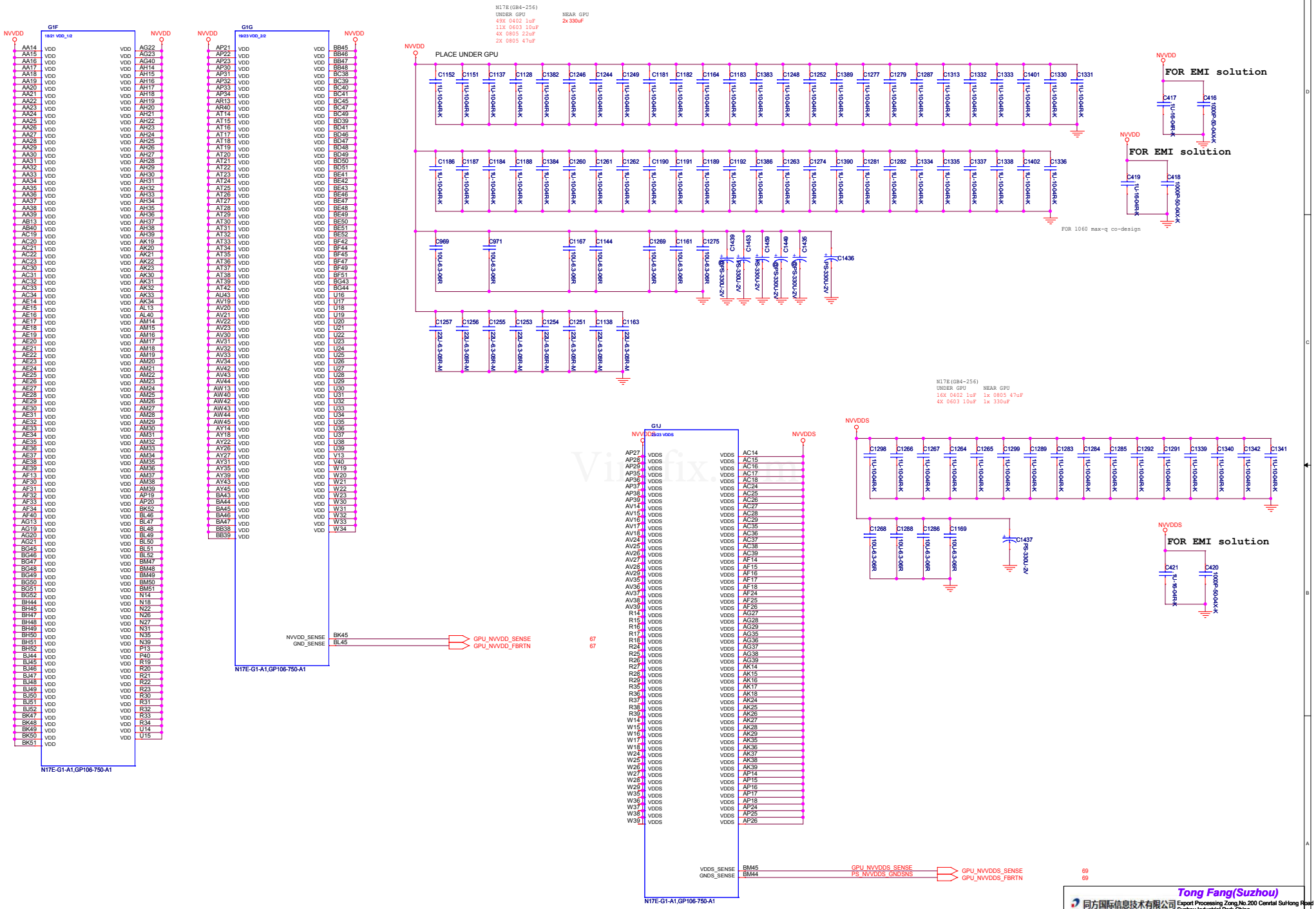
Title	NV-Frame Buffer D	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 51 of 72	


N17E(GB4-256)
UNDER GPU
49X 0402 1uF
11X 0603 10uF
4X 0805 22uF
2X 0805 47uF
NEAR GPU
2x 330uF
PLACE UNDER GPU
FOR EMI solution
FOR 1060 max-q co-design
N17E(GB4-256)
UNDER GPU
16X 0402 1uF
4X 0603 10uF
NEAR GPU
1x 0805 47uF
1x 330uF
G1F
G1G
G1J
N17E-G1-A1,GP106-750-A1
NVVDD_SENSE
GND_SENSE
GPU_NVVDD_SENSE
GPU_NVVDD_FBRTN
VDDS_SENSE
GNDS_SENSE
GPU_NVVDDS_SENSE
GPU_NVVDDS_FBRTN
Tong Fang(Suzhou)
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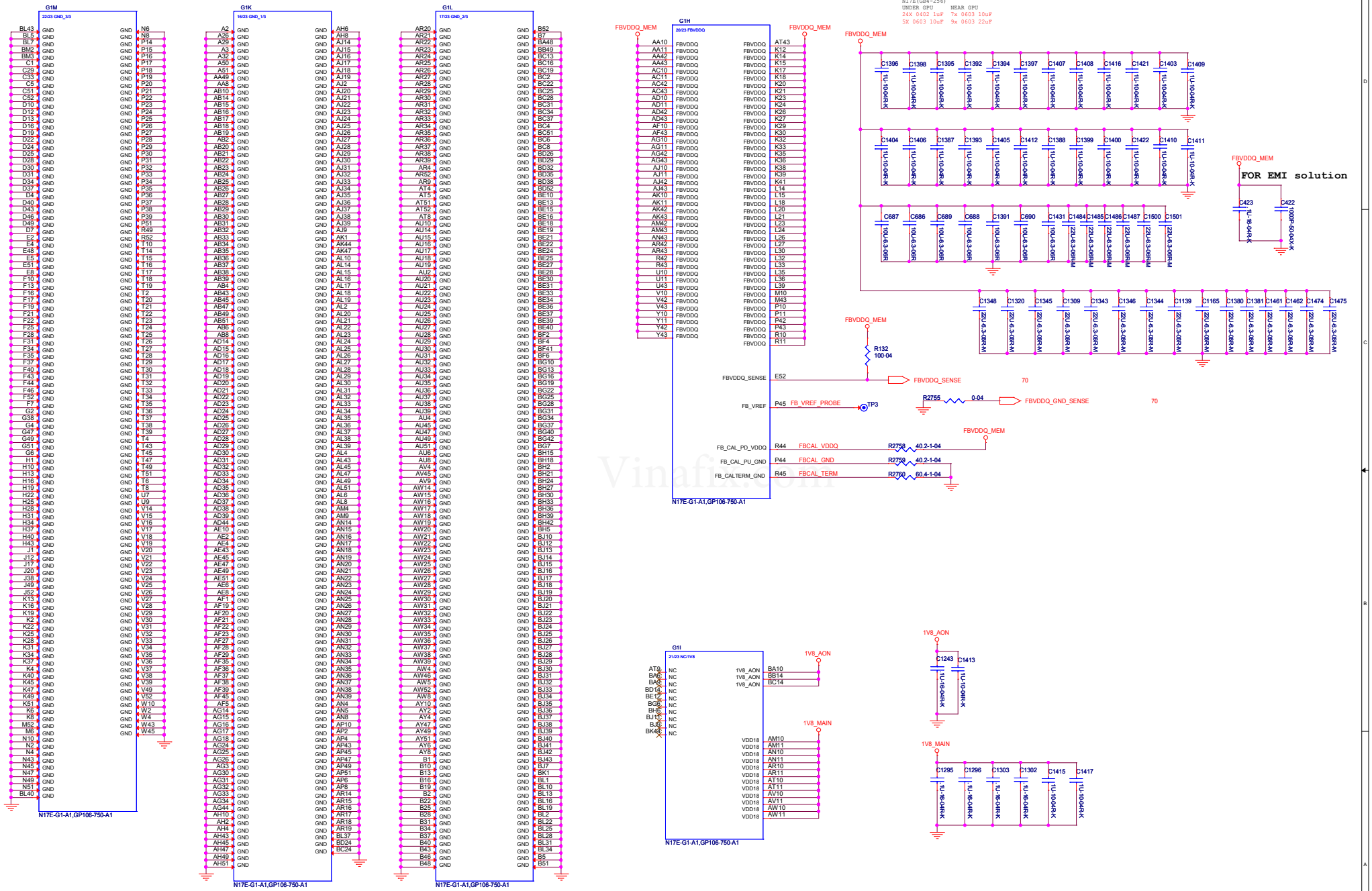
Suzhou Industrial Park,China
TEL:0512-62829228
NV-NVVDD/NVVDDS
GK5CN6X
Wednesday, January 17, 2018



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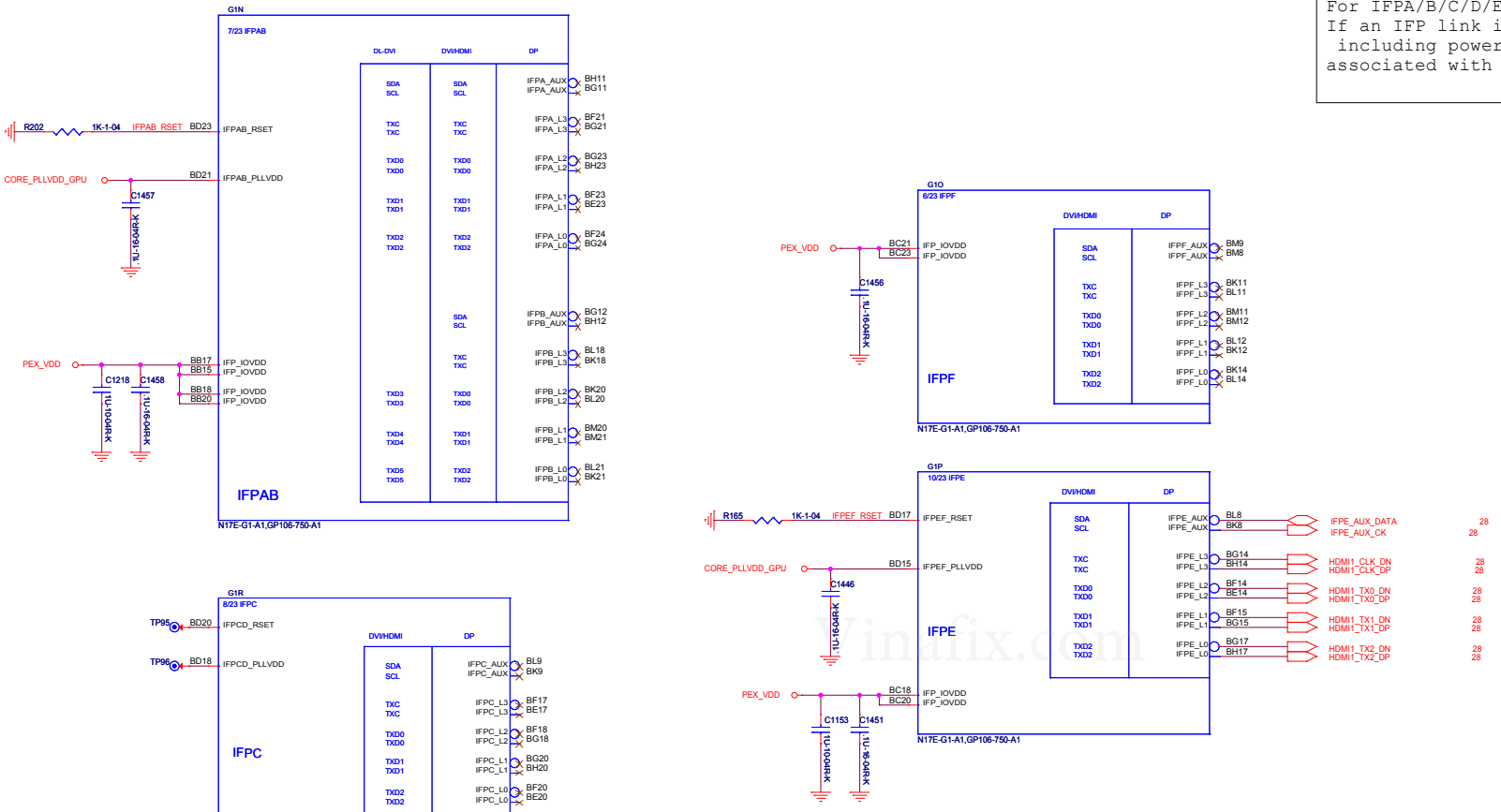
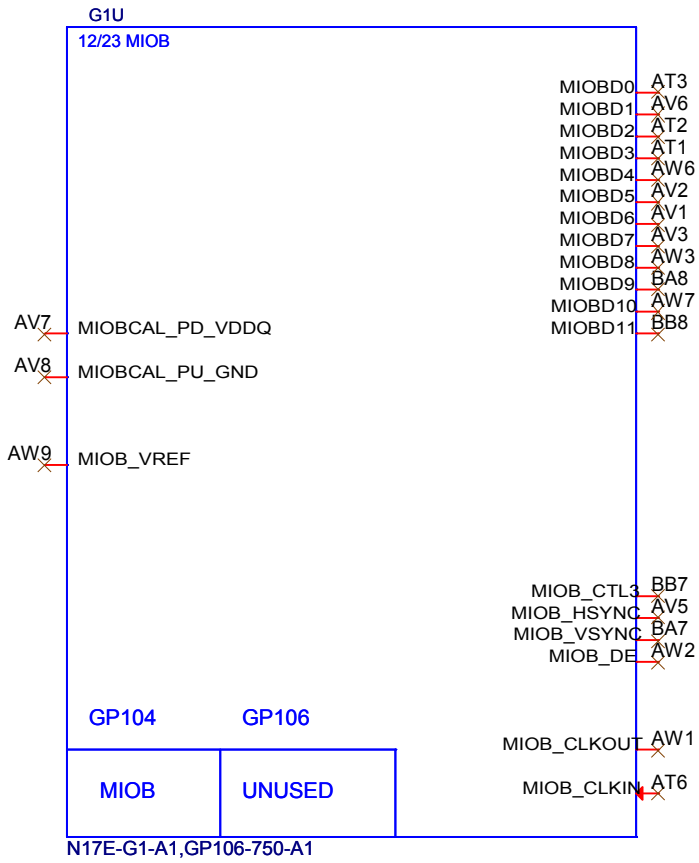
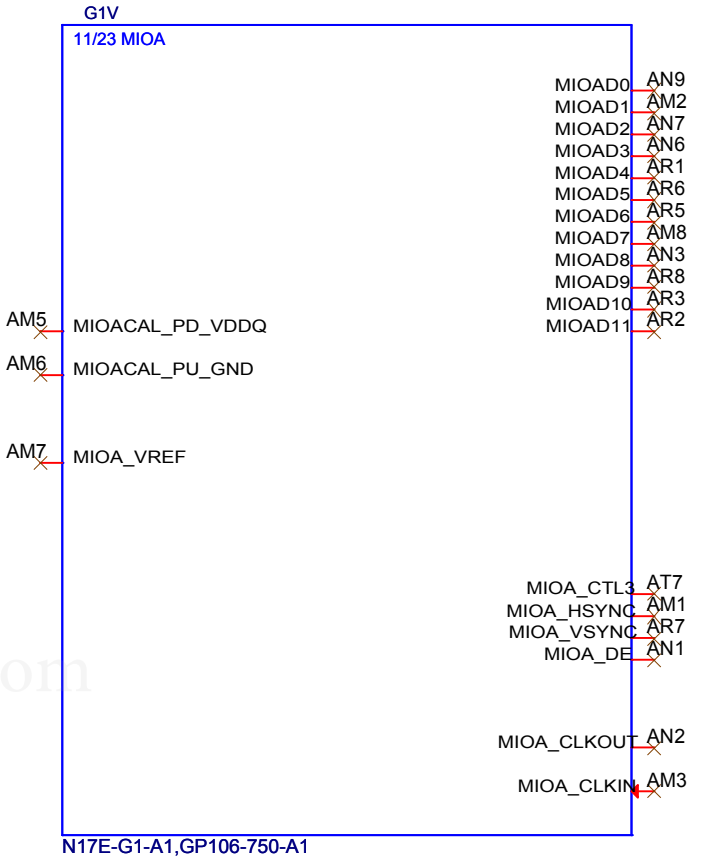
Title	NV-FBVDDQ_MEM/GND		
Size C	Document Number GK5CN6X		Rev V A
Date: Tuesday, January 16, 2018	Sheet 53 of 72		

Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX







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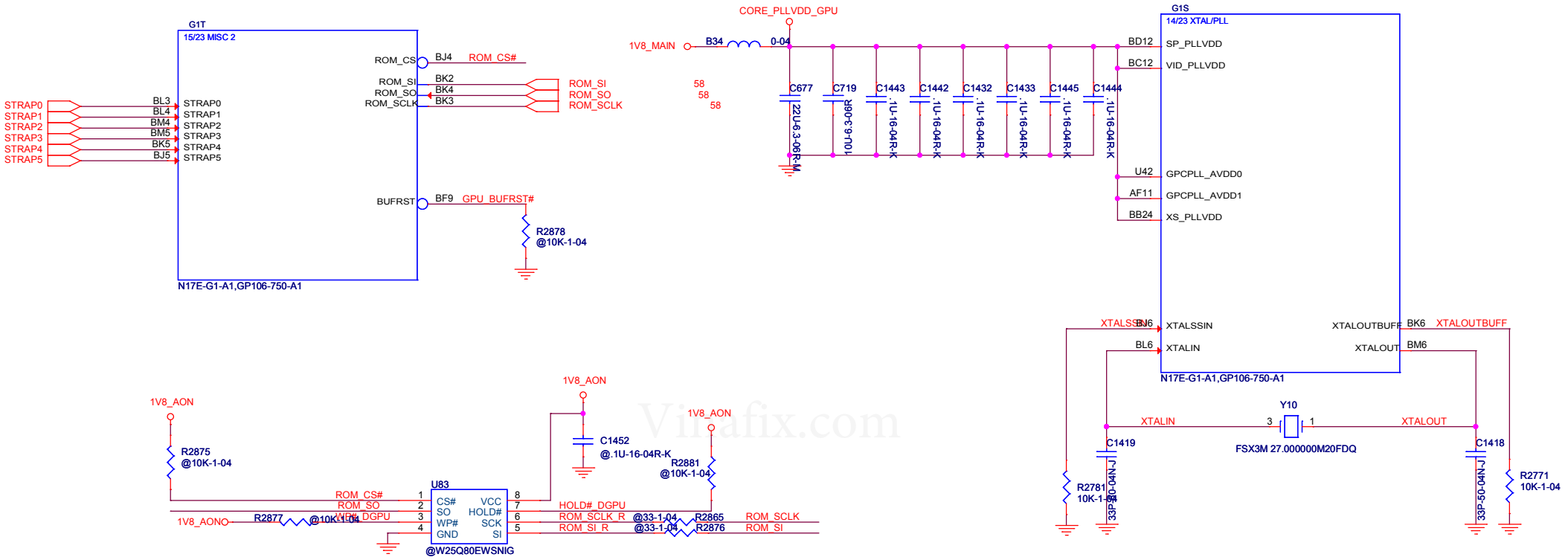
Title	NV-MIO	
Size A	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 55 of 72	



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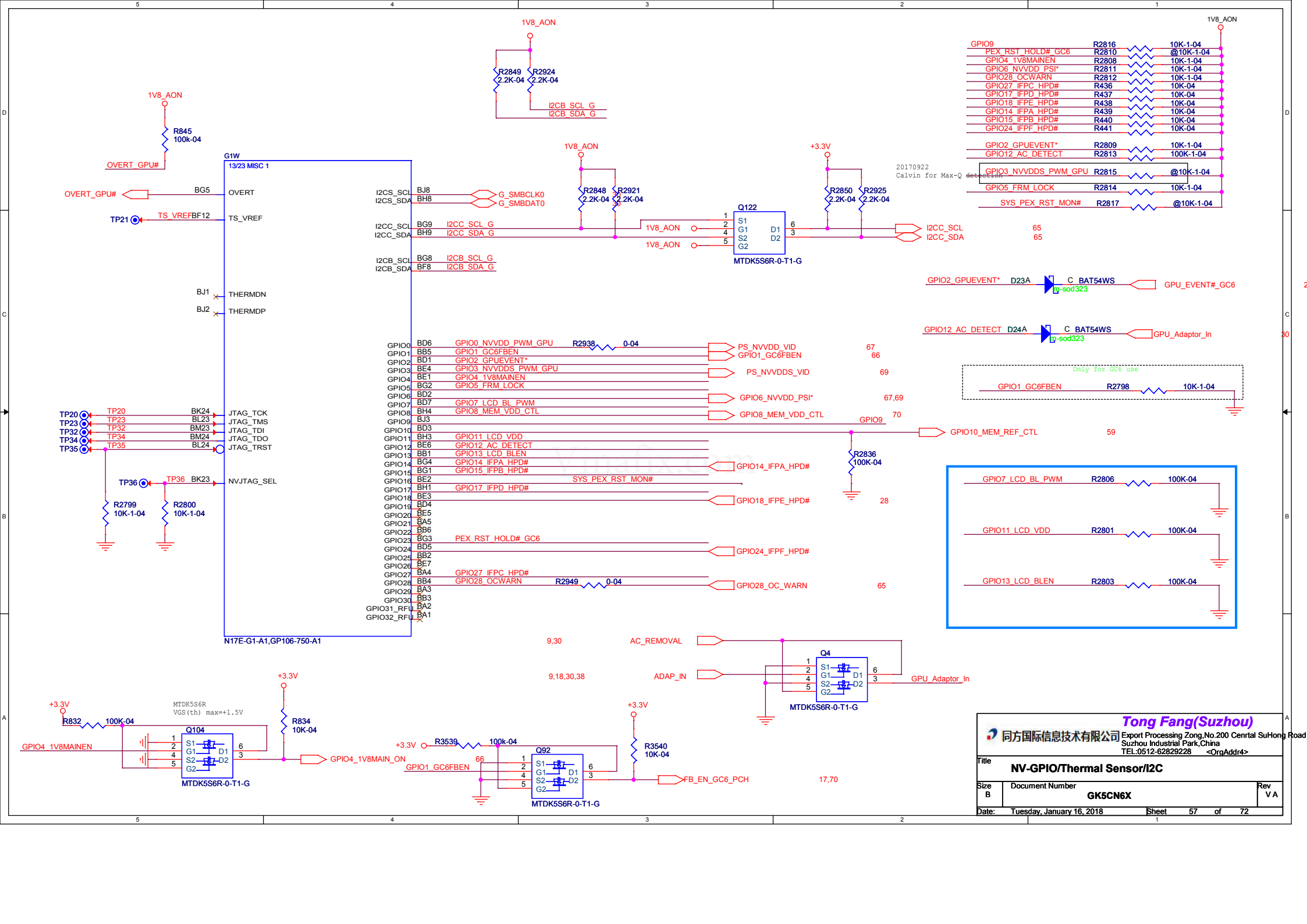
Title	NV-BIOS/XTAL
Size	B
Document Number	GK5CN6X
Rev	V A
Date	Tuesday, January 16, 2018
Sheet	56 of 72


1V8_AON
R2849 2.2K-04
R2924 2.2K-04
I2CB_SCL_G
I2CB_SDA_G
R845 100k-04
OVERT_GPU#
G1W
13/23 MISC 1
OVERT_GPU# BG5 OVERT
TP21 TS_VREF BF12 TS_VREF
BJ1 THERMDN
BJ2 THERMDP
I2CS_SCL BJ8 G_SMBCLK0
I2CS_SDA BH8 G_SMBDAT0
I2CC_SCL BG9 I2CC_SCL_G
I2CC_SDA BH9 I2CC_SDA_G
I2CB_SCL BG8 I2CB_SCL_G
I2CB_SDA BF8 I2CB_SDA_G
R2848 2.2K-04
R2921 2.2K-04
Q122
MTDK5S6R-0-T1-G
+3.3V
R2850 2.2K-04
R2925 2.2K-04
I2CC_SCL 65
I2CC_SDA 65
20170922
Calvin for Max-Q detection
GPIO9 R2816 10K-1-04
PEX_RST_HOLD#_GC6 R2810 @10K-1-04
GPIO4_1V8MAINEN R2808 10K-1-04
GPIO6_NVVDD_PSI* R2811 10K-1-04
GPIO28_OCWARN R2812 10K-1-04
GPIO27_IFPC_HPD# R436 10K-04
GPIO17_IFPD_HPD# R437 10K-04
GPIO18_IFPE_HPD# R438 10K-04
GPIO14_IFPA_HPD# R439 10K-04
GPIO15_IFPB_HPD# R440 10K-04
GPIO24_IFPF_HPD# R441 10K-04
GPIO2_GPUEVENT* R2809 10K-1-04
GPIO12_AC_DETECT R2813 100K-1-04
GPIO3_NVVDDS_PWM_GPU R2815 @10K-1-04
GPIO5_FRM_LOCK R2814 10K-1-04
SYS_PEX_RST_MON# R2817 @10K-1-04
GPIO2_GPUEVENT* D23A C BAT54WS GPU_EVENT#_GC6
GPIO12_AC_DETECT D24A C BAT54WS GPU_Adaptor_In
m-sod323
GPIO0 BD6 GPIO0_NVVDD_PWM_GPU R2938 0-04 PS_NVVDD_VID 67
GPIO1 BB5 GPIO1_GC6FBEN GPIO1_GC6FBEN 66
GPIO2 BD1 GPIO2_GPUEVENT*
GPIO3 BE4 GPIO3_NVVDDS_PWM_GPU PS_NVVDDS_VID 69
GPIO4 BE1 GPIO4_1V8MAINEN
GPIO5 BG2 GPIO5_FRM_LOCK
GPIO6 BD2 GPIO6_NVVDD_PSI* 67,69
GPIO7 BD7 GPIO7_LCD_BL_PWM
GPIO8 BH4 GPIO8_MEM_VDD_CTL GPIO8_MEM_VDD_CTL 70
GPIO9 BJ3 GPIO9
GPIO10 BD3 GPIO10_MEM_REF_CTL 59
GPIO11 BH3 GPIO11_LCD_VDD
GPIO12 BE6 GPIO12_AC_DETECT
GPIO13 BB1 GPIO13_LCD_BLEN
GPIO14 BG4 GPIO14_IFPA_HPD# GPIO14_IFPA_HPD#
GPIO15 BG1 GPIO15_IFPB_HPD#
GPIO16 BE2 SYS_PEX_RST_MON#
GPIO17 BH1 GPIO17_IFPD_HPD#
GPIO18 BE3 GPIO18_IFPE_HPD# 28
GPIO19 BD4
GPIO20 BE5
GPIO21 BA5
GPIO22 BB6
GPIO23 BG3 PEX_RST_HOLD#_GC6
GPIO24 BD5 GPIO24_IFPF_HPD#
GPIO25 BB2
GPIO26 BE7
GPIO27 BA4 GPIO27_IFPC_HPD#
GPIO28 BB4 GPIO28_OCWARN R2949 0-04 GPIO28_OC_WARN 65
GPIO29 BA3
GPIO30 BB3
GPIO31_RFU BA2
GPIO32_RFU BA1
N17E-G1-A1,GP106-750-A1
Only for GC6 use
GPIO1_GC6FBEN R2798 10K-1-04
R2836 100K-04
GPIO7_LCD_BL_PWM R2806 100K-04
GPIO11_LCD_VDD R2801 100K-04
GPIO13_LCD_BLEN R2803 100K-04
TP20 TP20 BK24 JTAG_TCK
TP23 TP23 BL23 JTAG_TMS
TP32 TP32 BM23 JTAG_TDI
TP34 TP34 BM24 JTAG_TDO
TP35 TP35 BL24 JTAG_TRST
TP36 TP36 BK23 NVJTAG_SEL
R2799 10K-1-04
R2800 10K-1-04
9,30 AC_REMOVAL
9,18,30,38 ADAP_IN
Q4
MTDK5S6R-0-T1-G
GPU_Adaptor_In
+3.3V
R832 100K-04
MTDK5S6R
VGS(th) max=+1.5V
Q104
MTDK5S6R-0-T1-G
R834 10K-04
GPIO4_1V8MAINEN
GPIO4_1V8MAIN_ON
R3539 100K-04
Q92
MTDK5S6R-0-T1-G
R3540 10K-04
GPIO1_GC6FBEN 66
FB_EN_GC6_PCH 17,70
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Title
NV-GPIO/Thermal Sensor/I2C
Size B
Document Number
GK5CN6X
Rev V A
Date: Tuesday, January 16, 2018
Sheet 57 of 72

	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

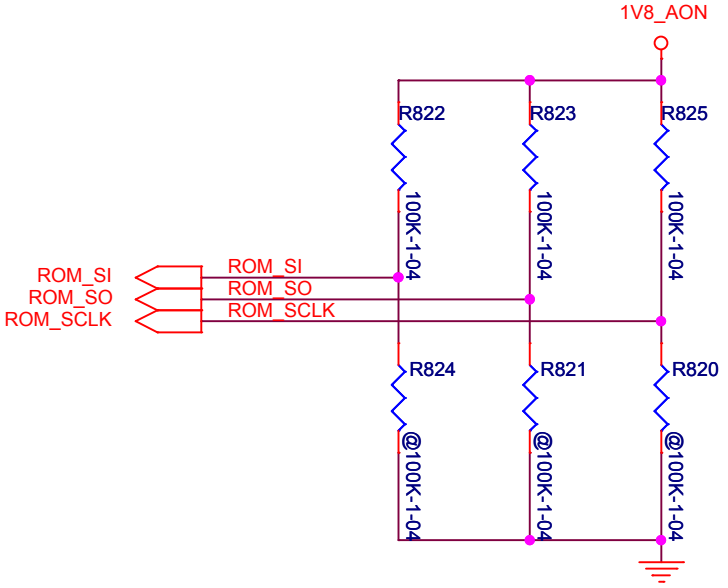
Based on RVL_07916_001_V10 JUNE 2017

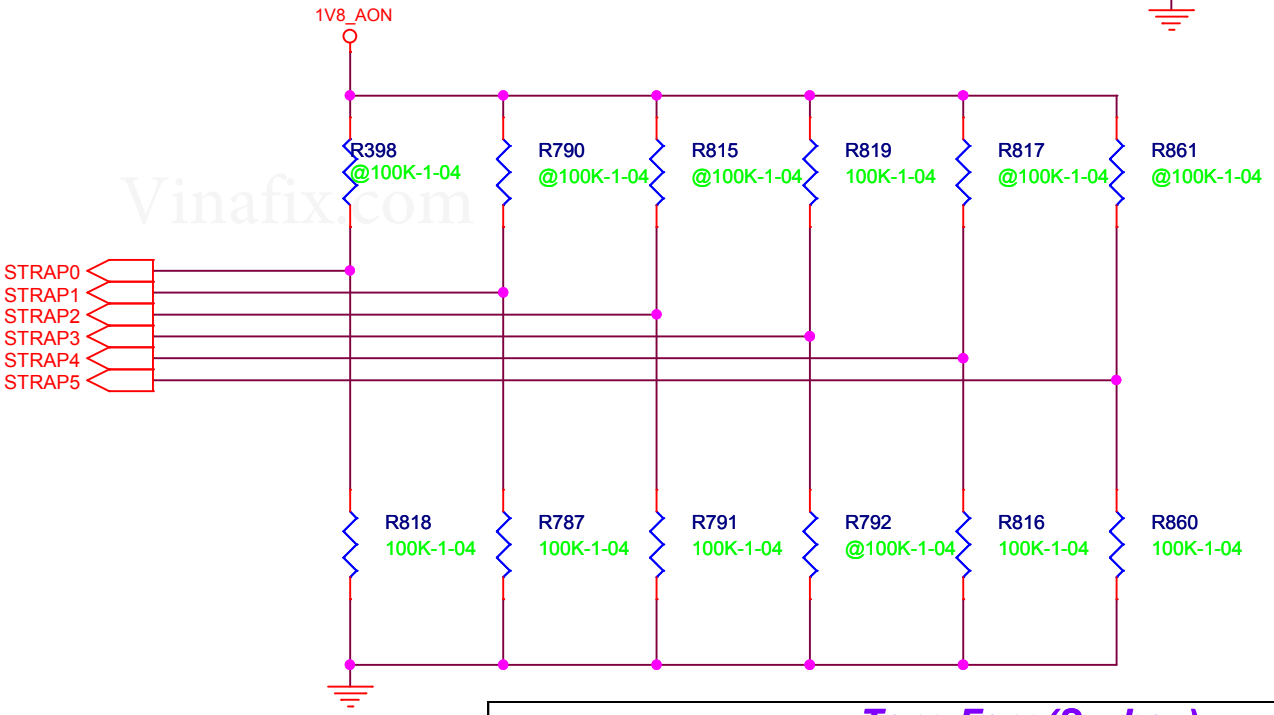
GDDR5						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4G80325FB-HC25 B-die	0X0	L	L	L
8Gb	Micron	MT51J256M32HF-80:A A-die	0X1	L	L	H
8Gb	Hynix	H5GQ8H24MJR-R4C M-die	0X2	L	H	L
4Gb	Samsung	K4G41325FE-HC25 E-die	0X7	H	H	H
4Gb	Hynix	H5GQ4H24AJR-R4C A-die	0X6	H	H	L
4Gb	Micron					

TOTAL LINK	TOTAL EN AUDIO	ROW INDEX
4	4	15
3	3	14
2	2	12
3	2	12
4	3	13

ROW INDEX	STRAP PIN		
	ROM_SO	ROM_SI	ROM_SCLK
15	L	L	L
14	L	L	H
13	L	H	L
12	L	H	H
11	H	L	L
10	H	L	H
8	H	H	H
0	H	H	M

Display Link 15





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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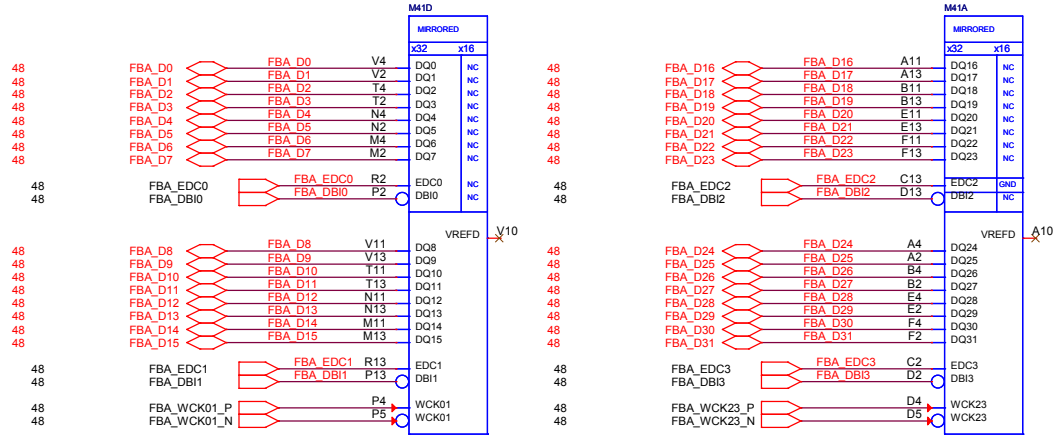
Title: **STRAP**

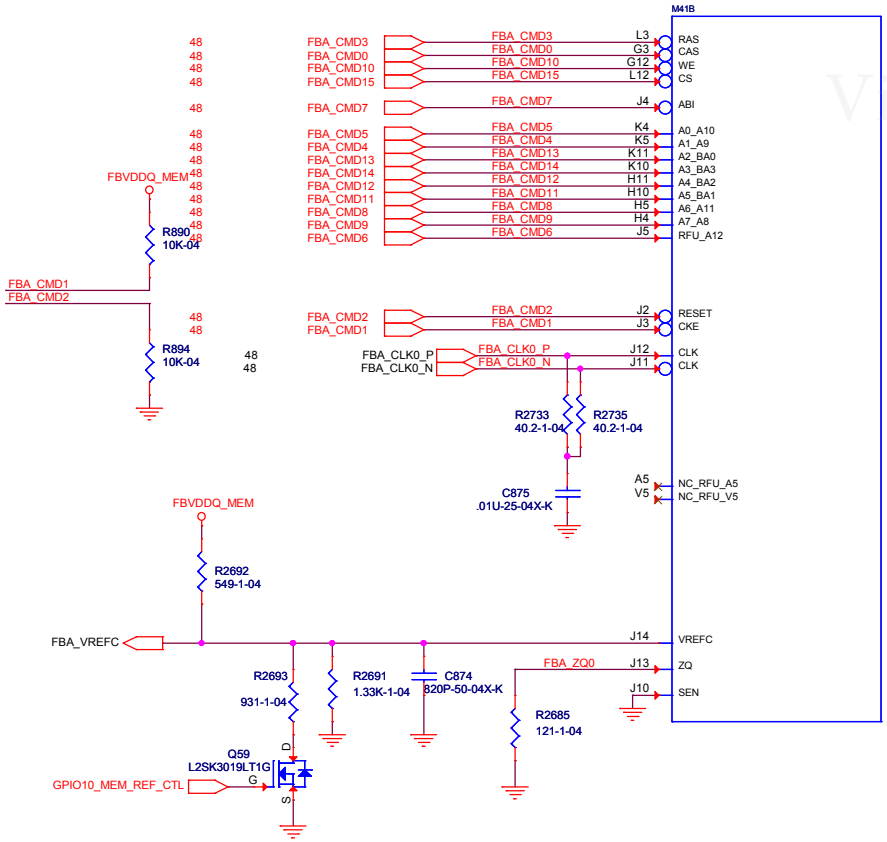
Size: A | Document Number: **GK5CN6X** | Rev: V A

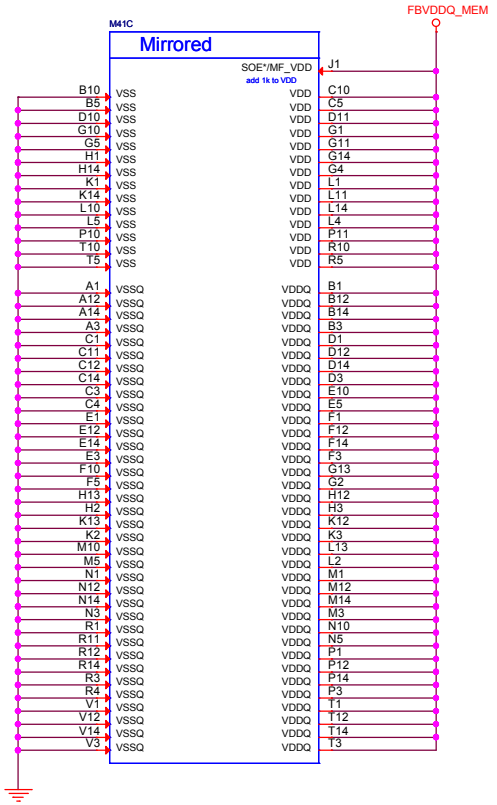
Date: Tuesday, January 16, 2018 | Sheet 58 of 72

MEM_FBA[31_0]

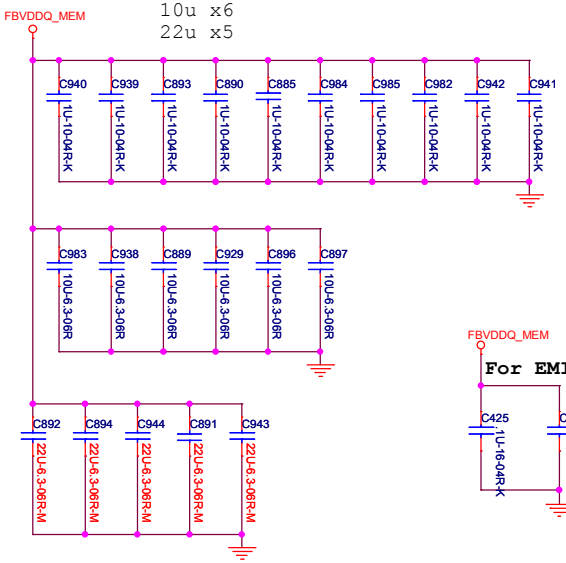
Maximum VRAM case Temp is 85 celsius degree



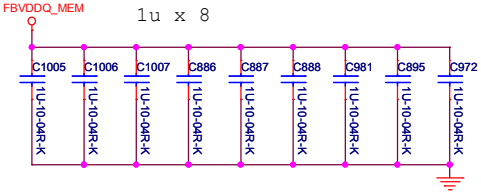




Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8



For EMI solution

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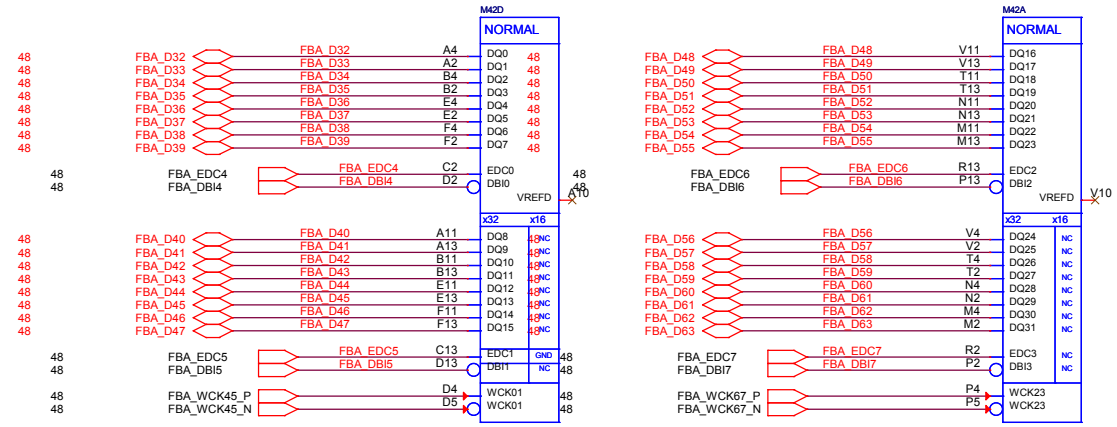
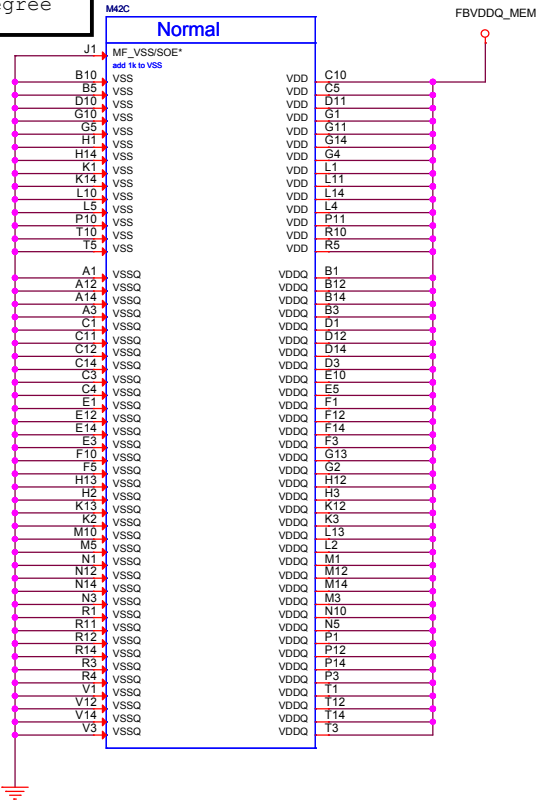
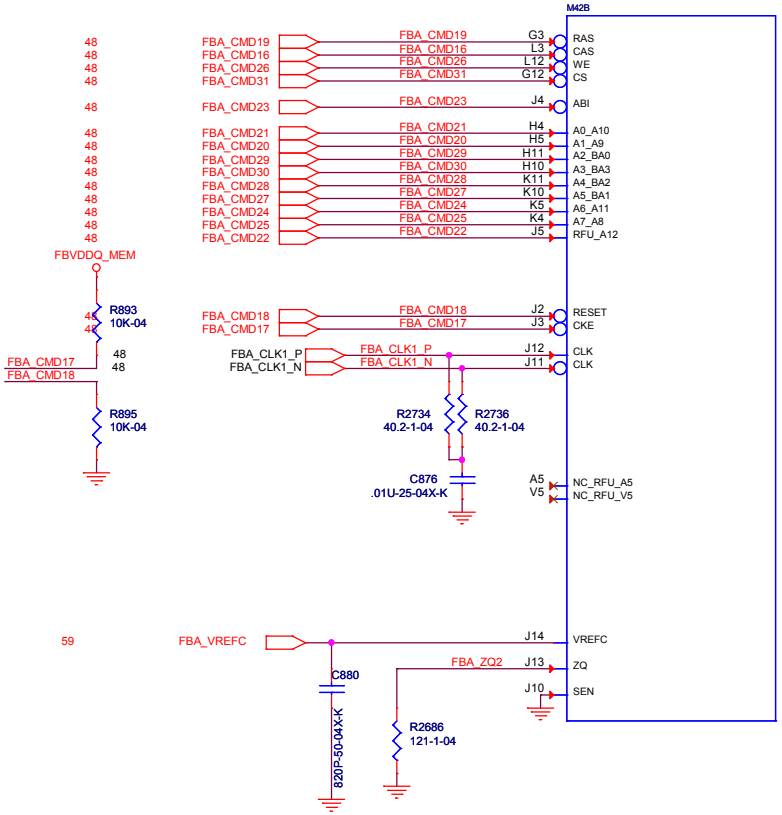
Title	Frame Buffer A0-VRAM		
Size: Custom	Document Number: GK5CN6X		Rev: V A
Date: Tuesday, January 16, 2018	Sheet 59 of 72		

MEM_FBA[63_32]

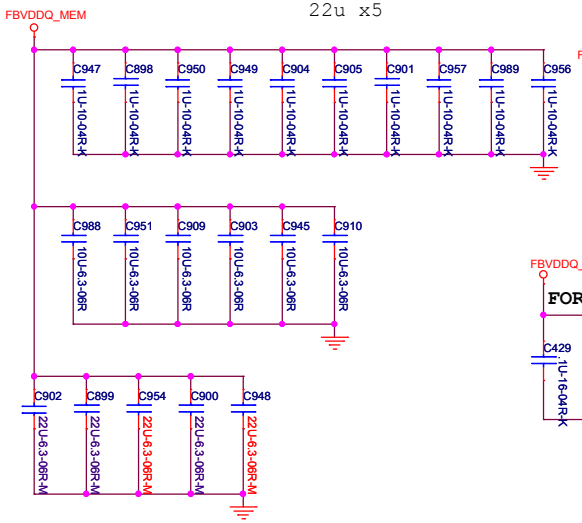
Maximum VRAM case Temp is 85 celcisus degree



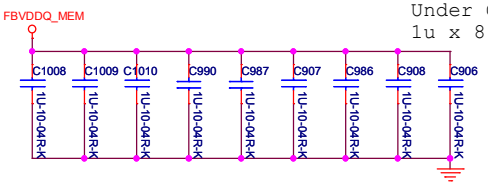


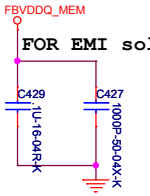


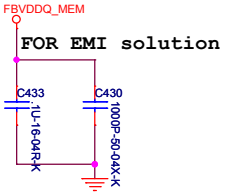
Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8







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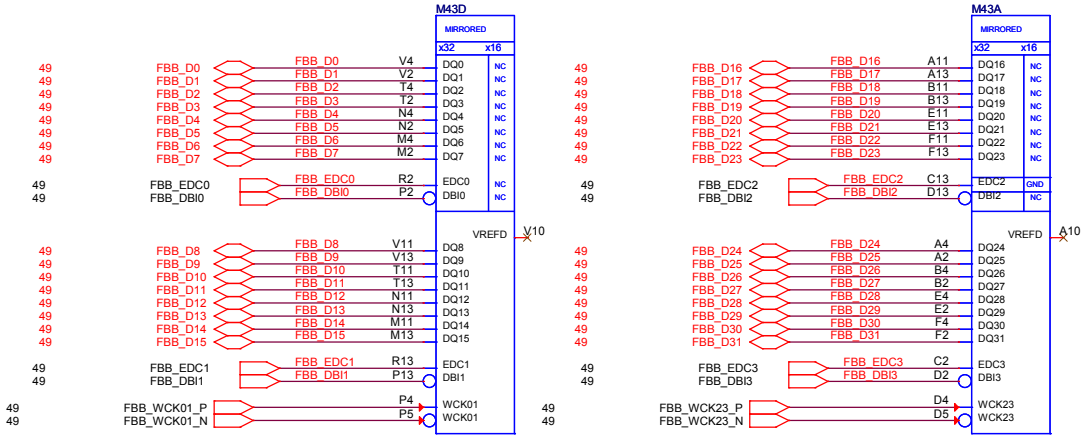
Title: Frame Buffer A1-VRAM

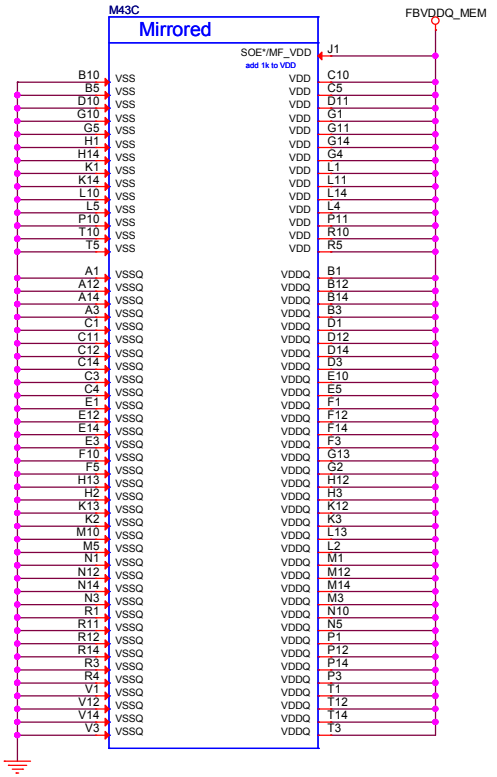
Size: Custom | Document Number: GK5CN6X | Rev: V A

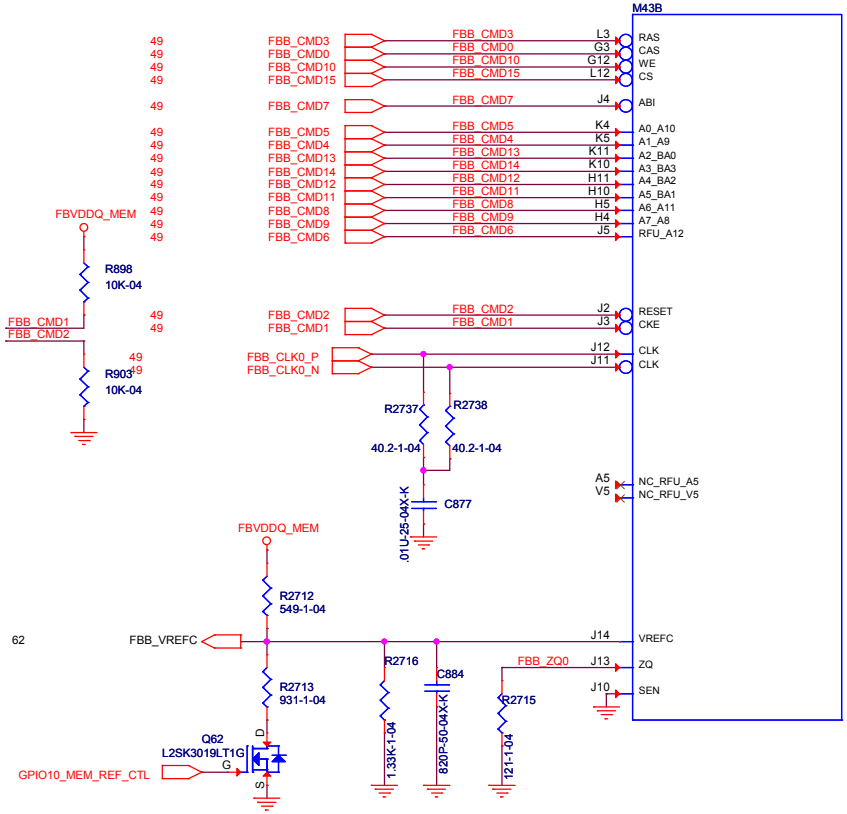
Date: Tuesday, January 16, 2018 | Sheet 60 of 72

MEM_FBB[31_0]

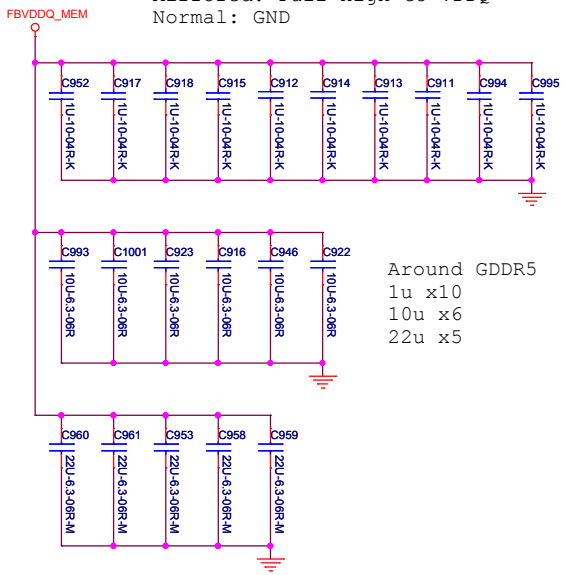
Maximum VRAM case Temp is 85 celcisus degree





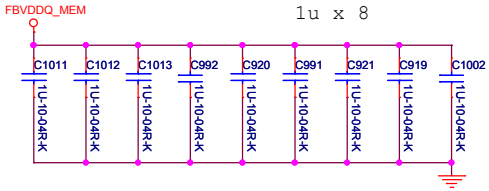


Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5

Under GDDR5
1u x 8



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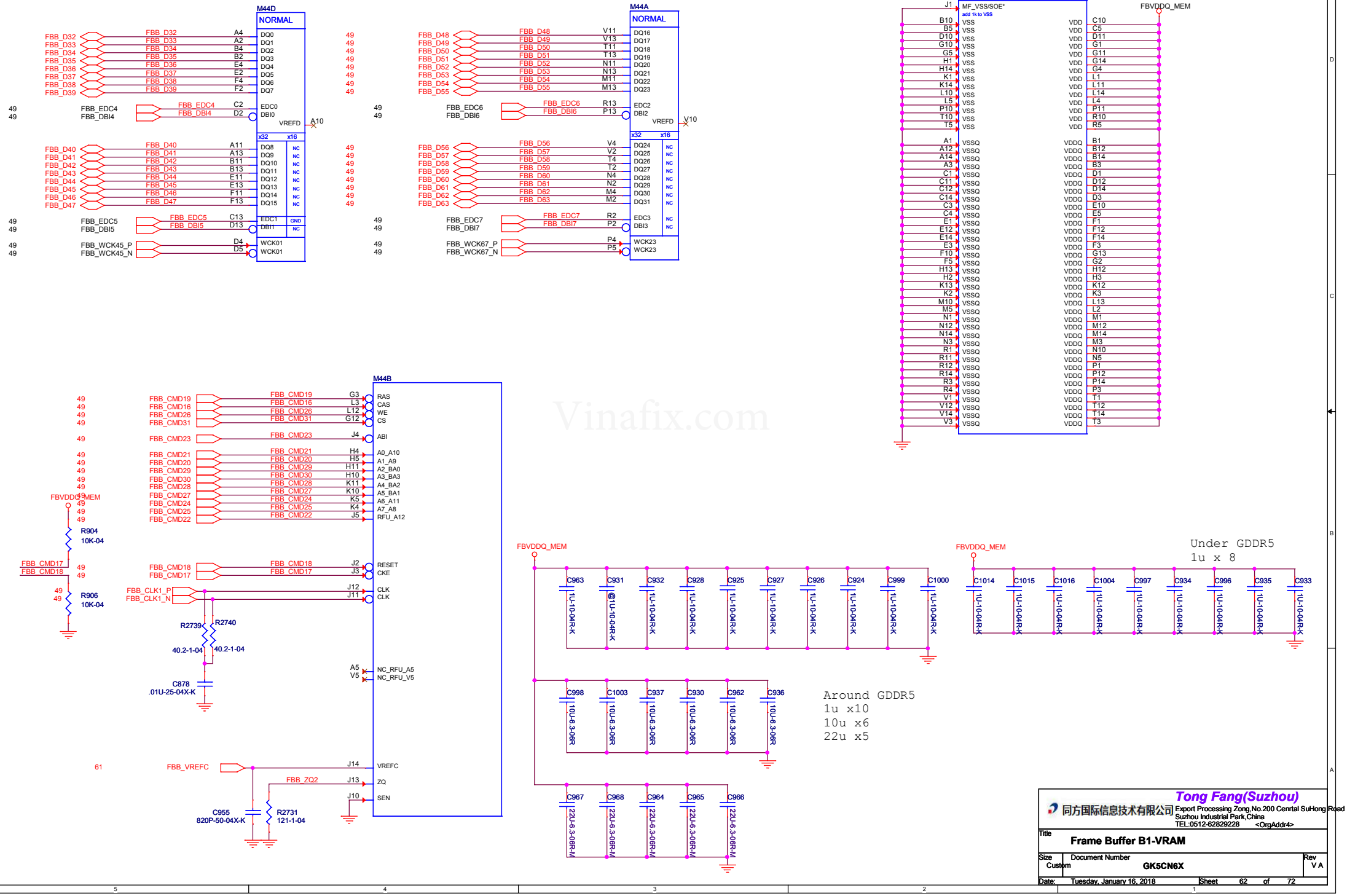
Title: Frame Buffer B0-VRAM

Size	Document Number	Rev
Custom	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 61 of 72

MEM_FBB[63_32]

Maximum VRAM case Temp is 85 celcisus degree



Title	Frame Buffer B1-VRAM
Size	Custom
Document Number	GK5CN6X
Rev	V A
Date:	Tuesday, January 16, 2018
Sheet	62 of 72

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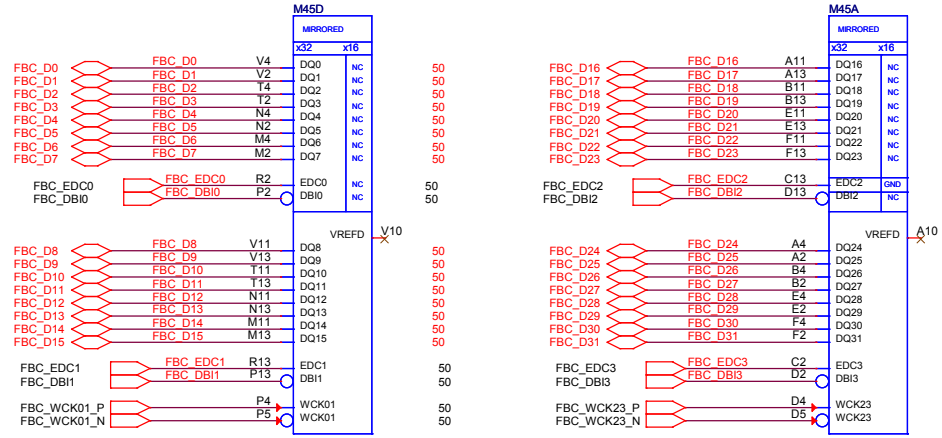
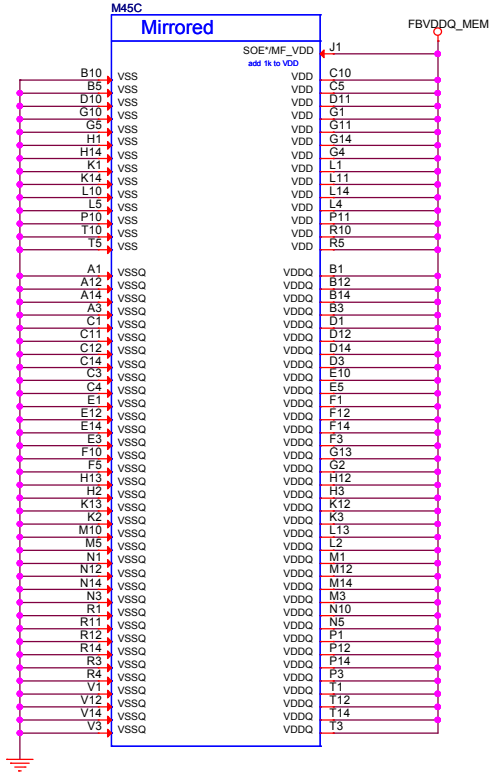
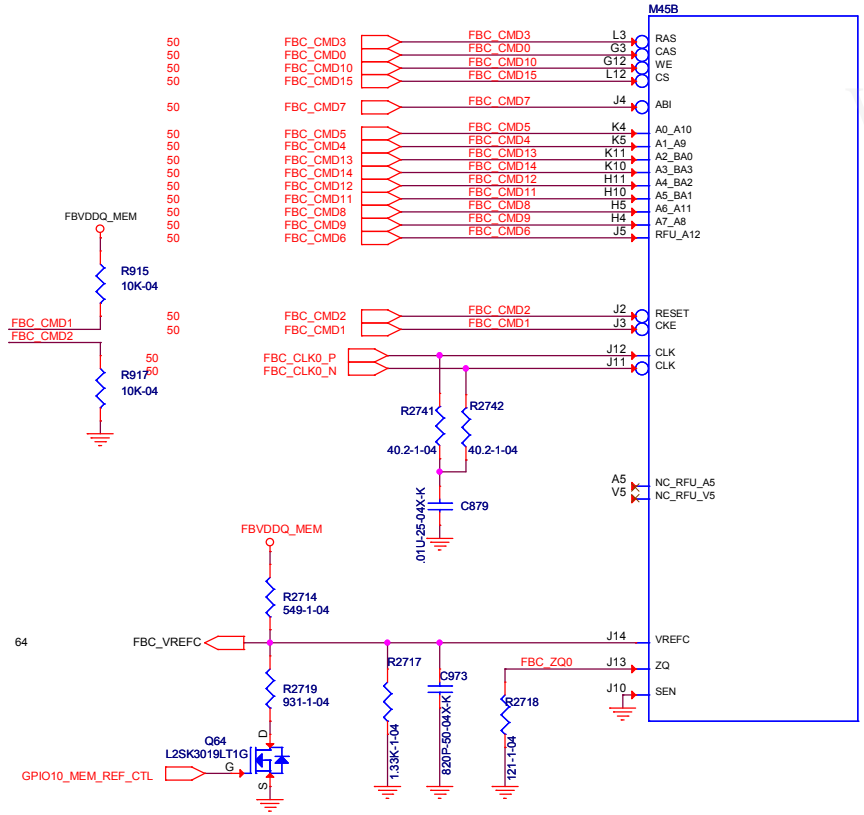
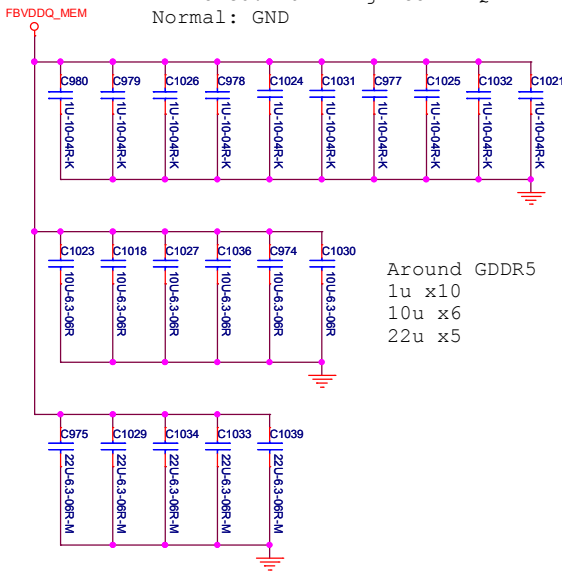
MEM_FBC[31_0]



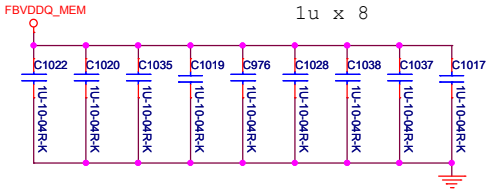




Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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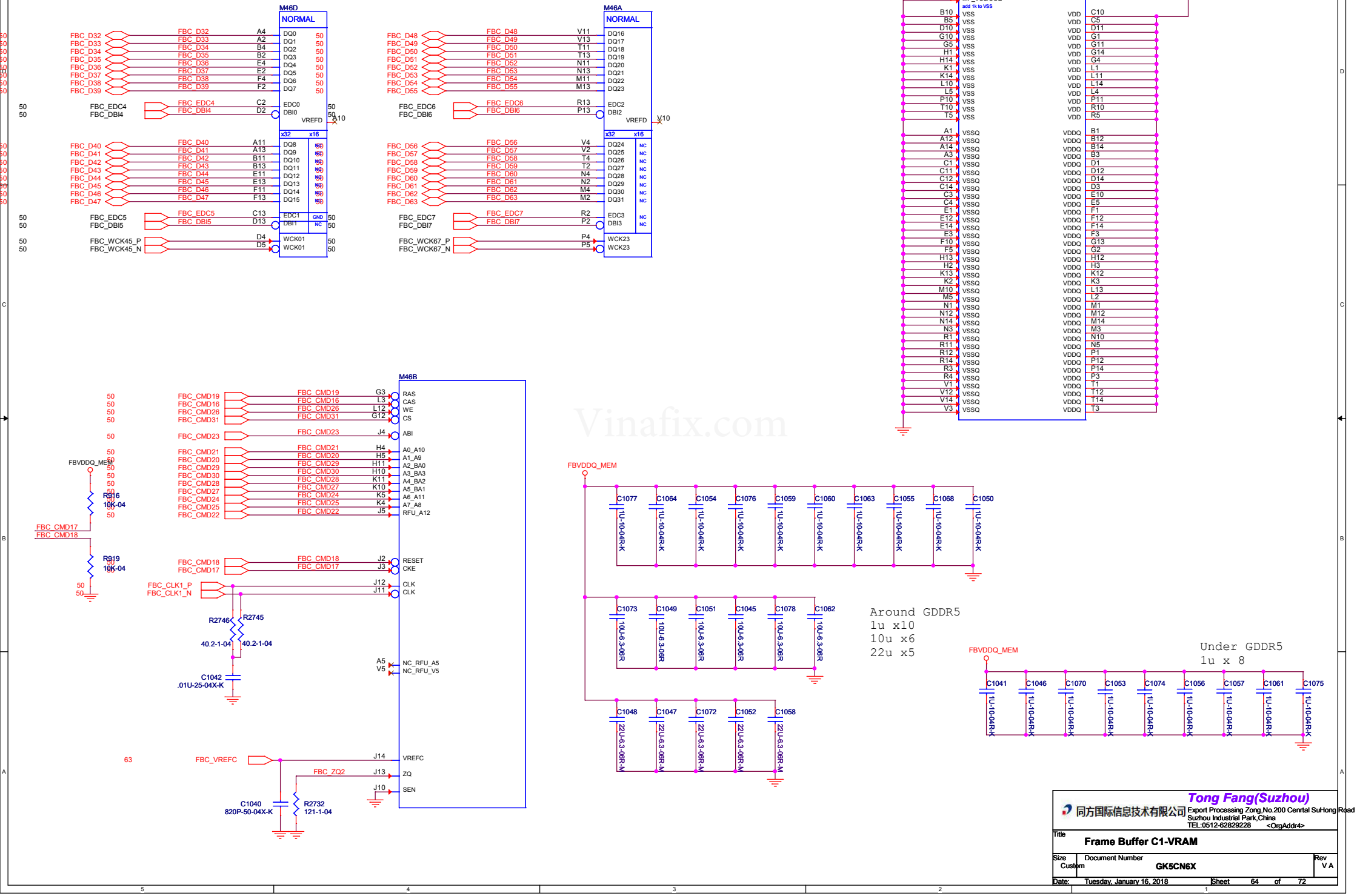
Title: Frame Buffer C0-VRAM
Size: Custom | Document Number: GK5CN6X | Rev: V A
Date: Tuesday, January 16, 2018 | Sheet 63 of 72

MEM_FBC[63_32]



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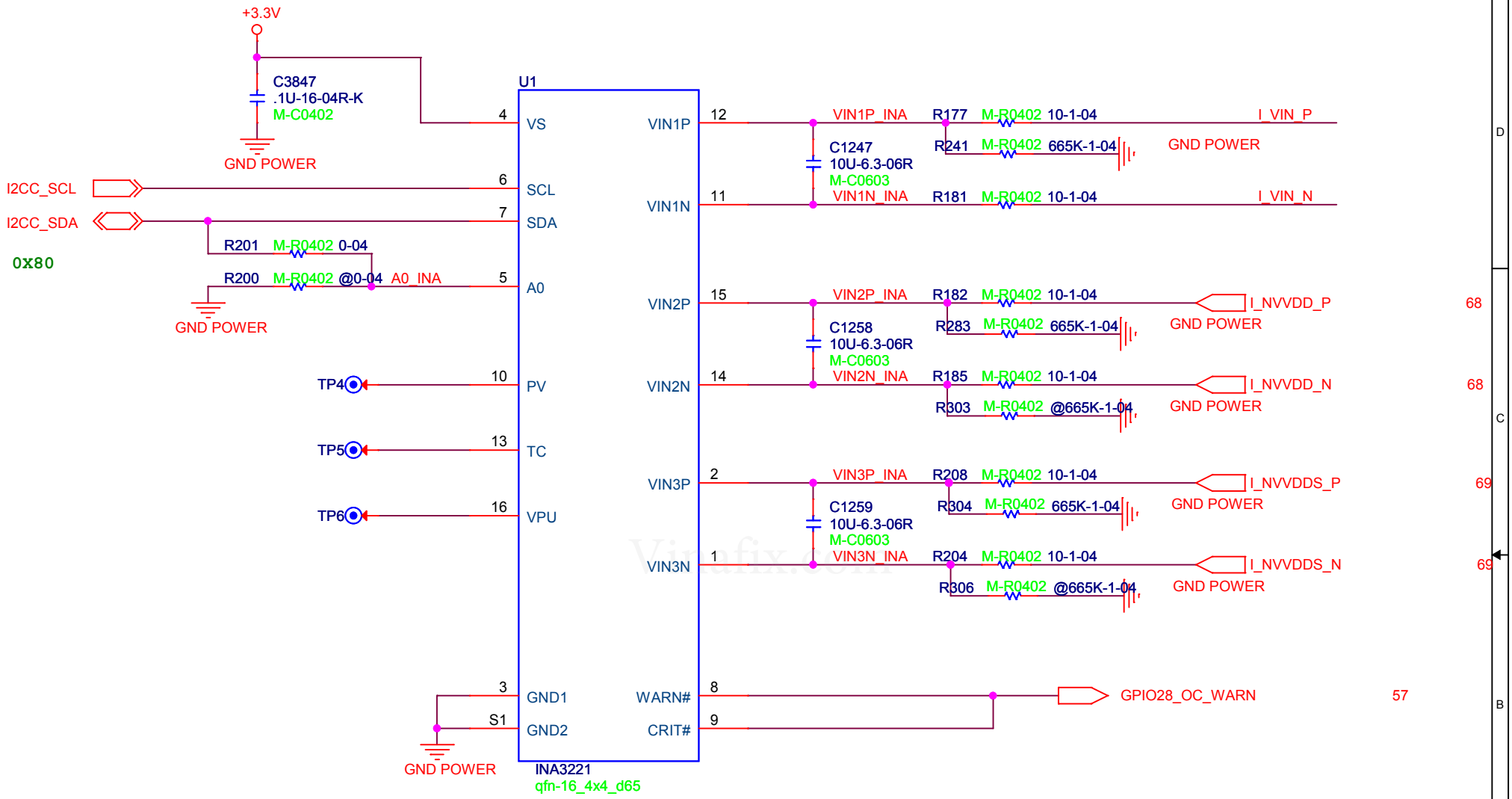
Title	Frame Buffer C1-VRAM	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Tuesday, January 16, 2018	Sheet 64 of 72	



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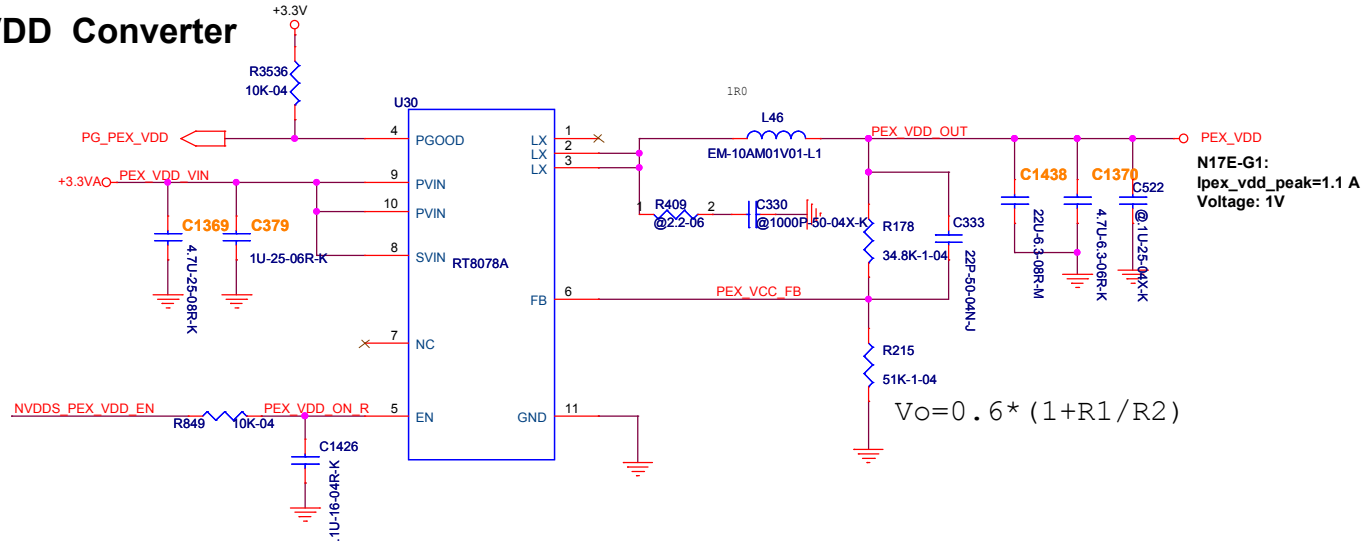
Title
PWR MEASUREMENT

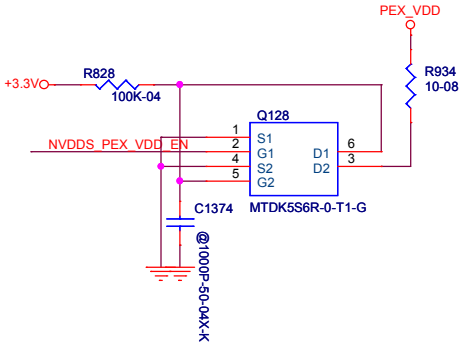
Size	Document Number	Rev
A	GK5CN6X	V A

Date: Tuesday, January 16, 2018 Sheet 65 of 72

PEX_VDD Converter

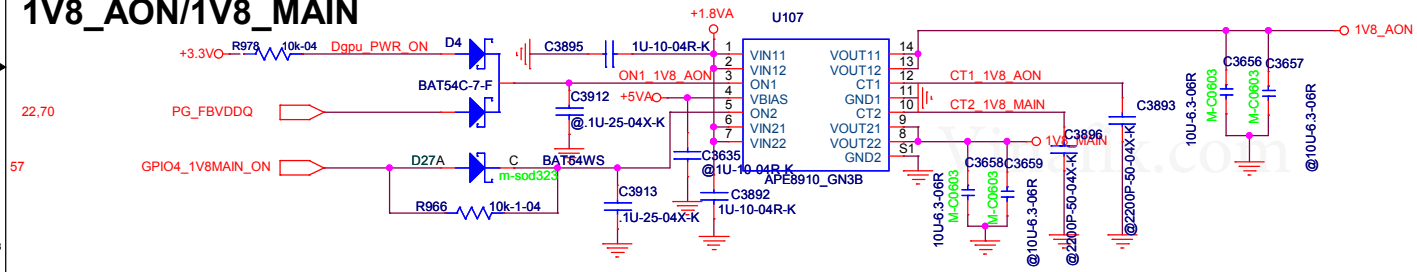


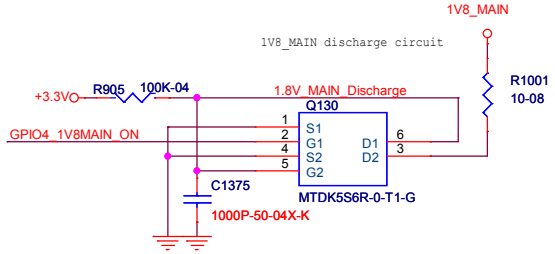
N17E-G1:
Ipex_vdd_peak=1.1 A
Voltage: 1V

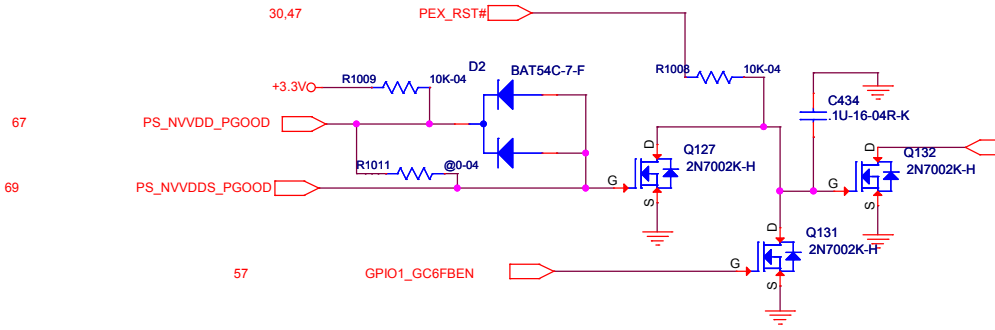


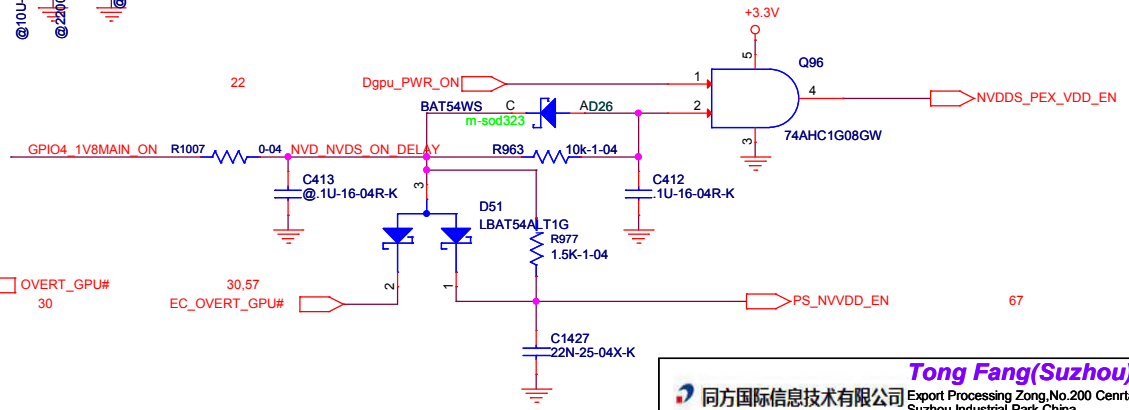
1V8_AON/1V8_MAIN

N17E-G1
1V8_AON + 1V8_MAIN 1.8V
ICC=1.6A









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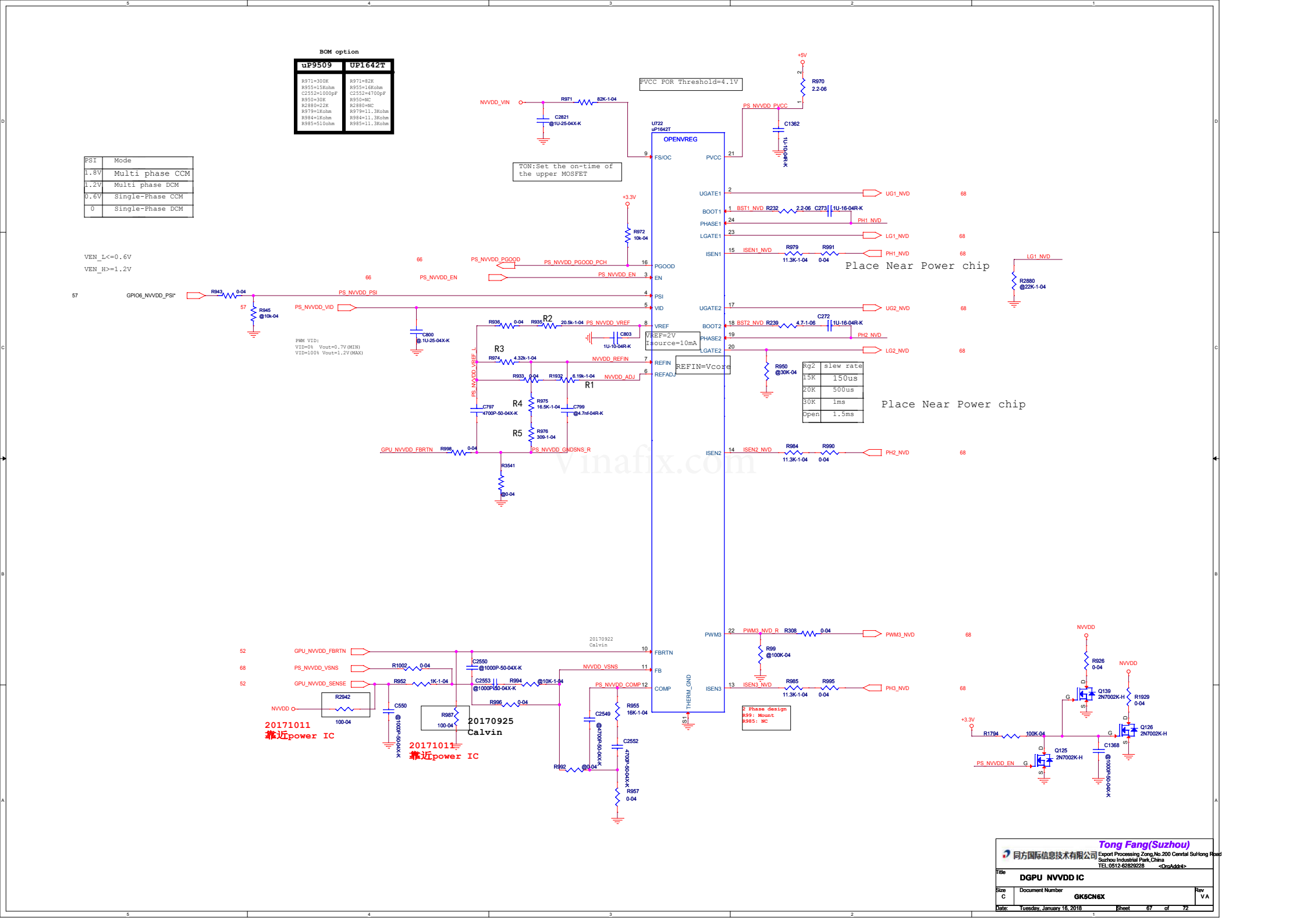
Title	DGPU PEX_VDD/1V8_AON	
Size B	Document Number GK5CN6X	Rev V A
Date: Wednesday, January 17, 2018	Sheet 66 of 72	


BOM option
uP9509
R971=300K
R955=15Kohm
C2552=1000pF
R950=30K
R2880=22K
R979=1Kohm
R984=1Kohm
R985=510ohm
UP1642T
R971=82K
R955=16Kohm
C2552=4700pF
R950=NC
R2880=NC
R979=11.3Kohm
R984=11.3Kohm
R985=11.3Kohm
PSI Mode
1.8V Multi phase CCM
1.2V Multi phase DCM
0.6V Single-Phase CCM
0 Single-Phase DCM
VEN_L<=0.6V
VEN_H>=1.2V
PVCC POR Threshold=4.1V
TON:Set the on-time of the upper MOSFET
U722 uP1642T
OPENVREG
FS/OC
PVCC
PGOOD
EN
PSI
VID
VREF
REFIN
REFADJ
UGATE1
BOOT1
PHASE1
LGATE1
ISEN1
UGATE2
BOOT2
PHASE2
LGATE2
ISEN2
PWM3
ISEN3
FBRTN
FB
COMP
THERM_GND
VREF=2V Isource=10mA
REFIN=Vcore
PWM VID:
VID=0% Vout=0.7V(MIN)
VID=100% Vout=1.2V(MAX)
Rg2 slew rate
15K 150us
20K 500us
30K 1ms
Open 1.5ms
Place Near Power chip
Place Near Power chip
2 Phase design
R99: Mount
R985: NC
20171011
靠近power IC
20170925
Calvin
20171011
靠近power IC
20170922
Calvin
Vinafix.com
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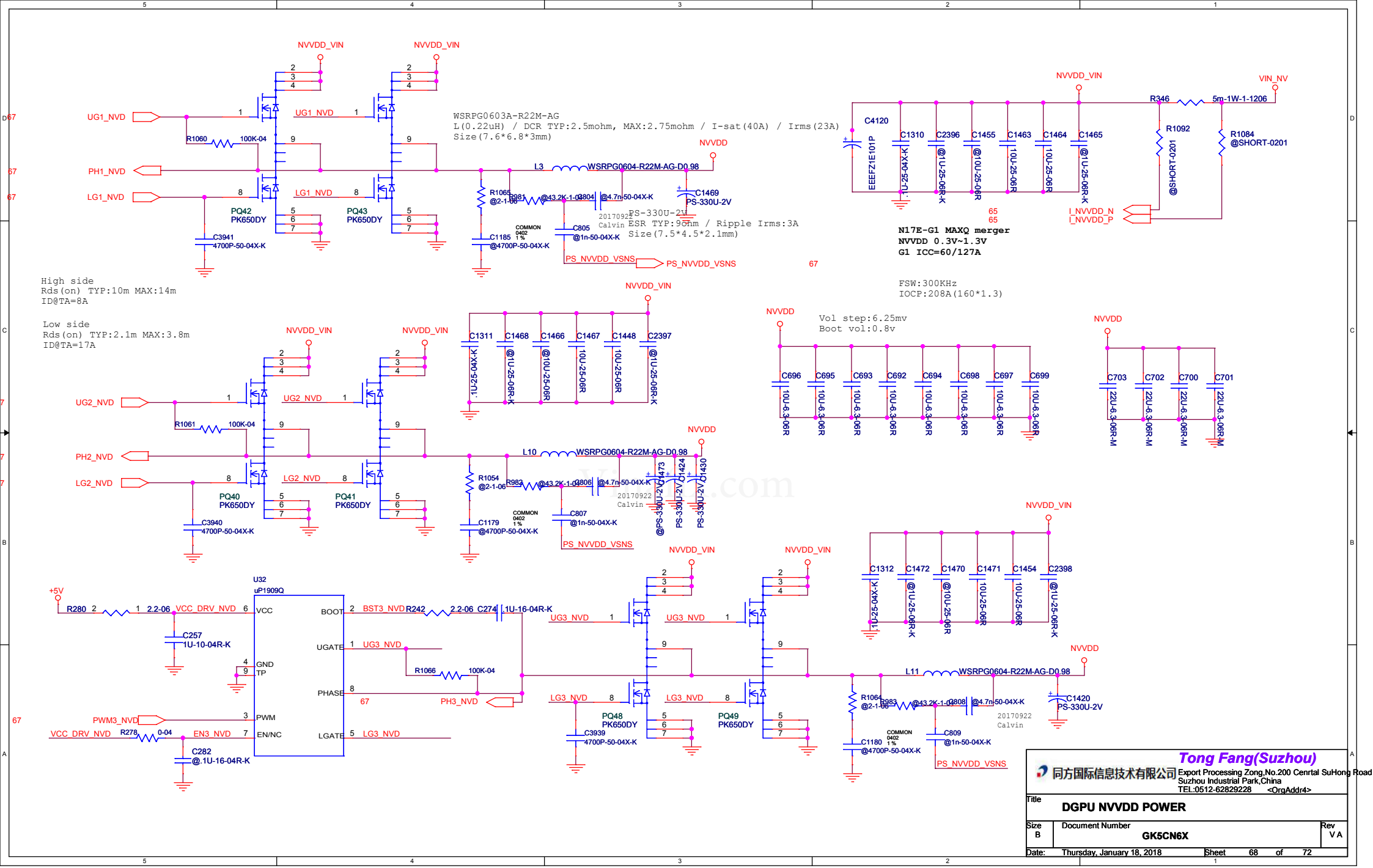
Title
DGPU NVVDD IC
Size C
Document Number GK5CN6X
Rev V A
Date: Tuesday, January 16, 2018
Sheet 67 of 72



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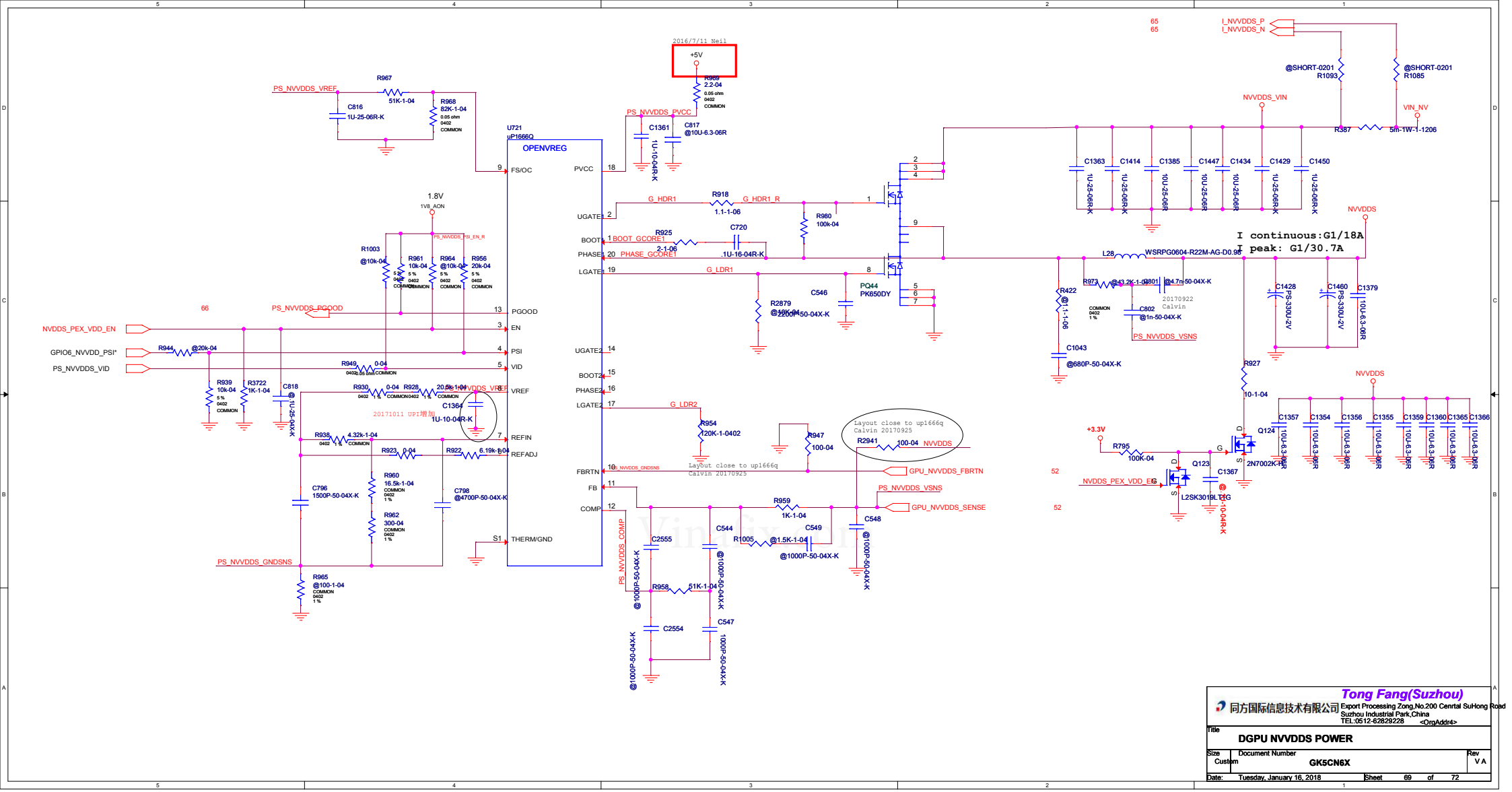
Title	DGPU NVVDD POWER	
Size B	Document Number GK5CN6X	Rev V A
Date: Thursday, January 18, 2018	Sheet 68 of 72	


U721
uP1666Q
OPENVREG
FS/OC
PVCC
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
FBRTN
FB
COMP
PGOOD
EN
PSI
VID
VREF
REFIN
REFADJ
THERM/GND
+5V
1.8V
1V8_AON
NVDDS_VIN
NVDDS
I_NVDDS_P
I_NVDDS_N
I continuous:G1/18A
I peak: G1/30.7A
PS_NVDDS_VREF
PS_NVDDS_PVCC
PS_NVDDS_PGOOD
PS_NVDDS_VSNS
PS_NVDDS_GNDSNS
PS_NVDDS_COMP
GPU_NVDDS_FBRTN
GPU_NVDDS_SENSE
NVDDS_PEX_VDD_EN
GPIO6_NVVDD_PSI*
PS_NVDDS_VID
G_HDR1
G_HDR1_R
G_LDR1
G_LDR2
BOOT_GCORE1
PHASE_GCORE1
PQ44
PK650DY
L28
WSRPG0604-R22M-AG-D0.98
L2SK3019LT1G
2N7002K-H
Layout close to up1666q
Calvin 20170925
20171011 UPI增加
2016/7/11 Neil
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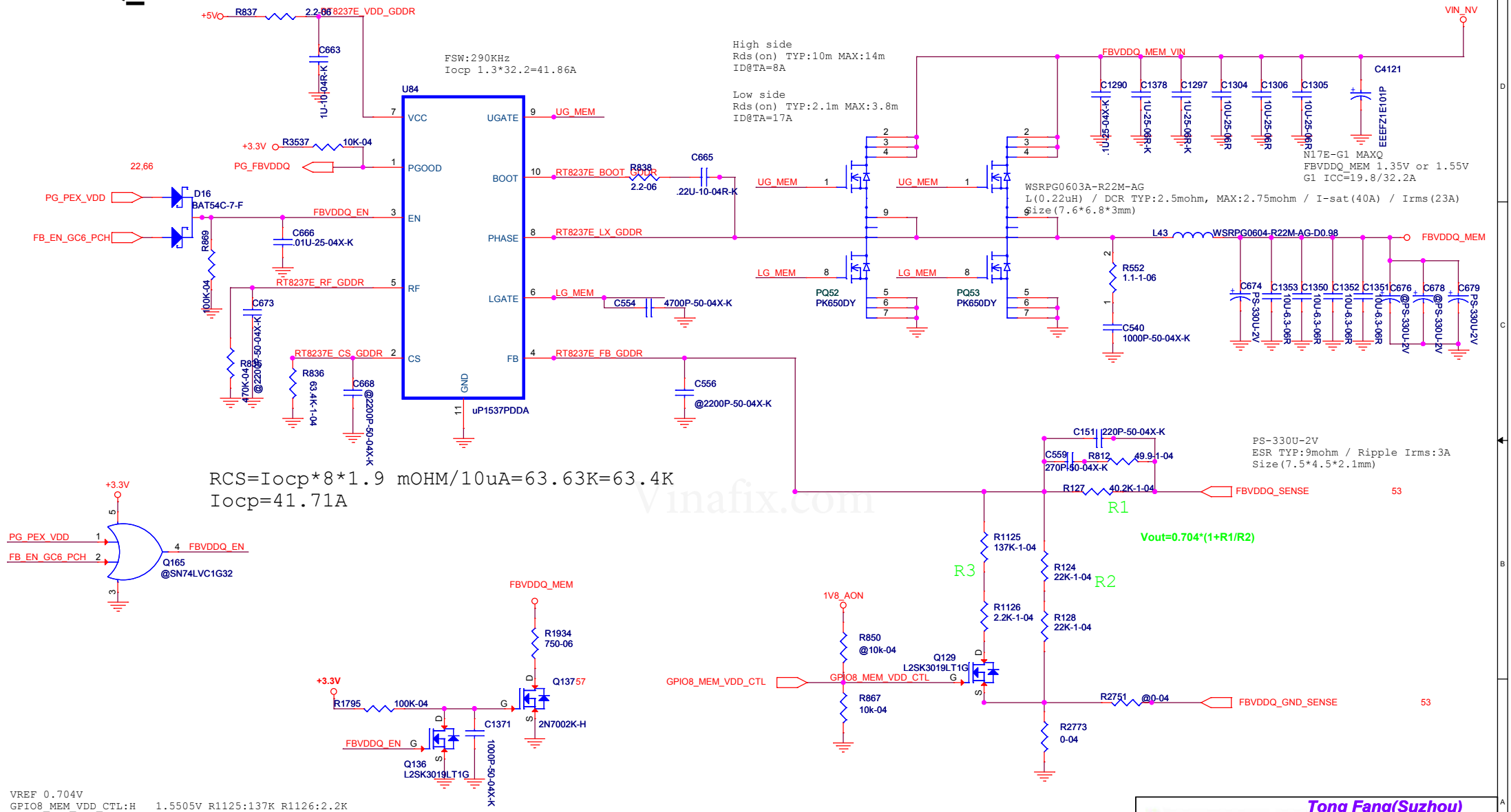
DGPU NVVDDS POWER
GK5CN6X
Rev V A
Tuesday, January 16, 2018
Sheet 69 of 72

FBVDDQ_MEM



VREF 0.704V
GPIO8_MEM_VDD_CTL:H 1.5505V R1125:137K R1126:2.2K
GPIO8_MEM_VDD_CTL:H 1.5044V R1125:180K R1126:0K
GPIO8_MEM_VDD_CTL:L 1.3472V

NOTE! If use Micron 8Gb MT51J256M32HF-80:A GPIO8_MEM_VDD_CTL:H 1.5V

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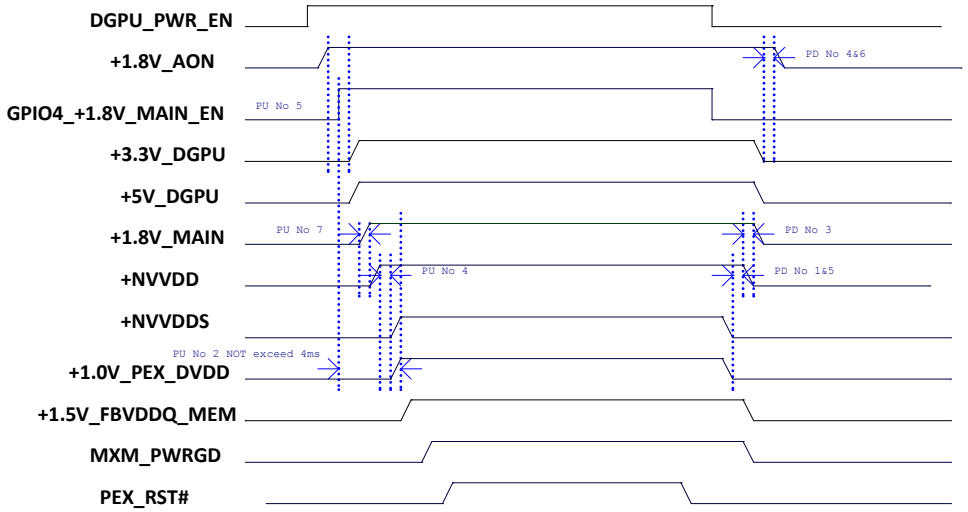
Title	DGPU FBVDDQ_MEM	
Size B	Document Number GK5CN6X	Rev V A
Date: Friday, January 19, 2018	Sheet 70 of 72	

POWER SEQUENCE



POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD/+NVVDD_PGOOD) must NOT exceed 4ms.
3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required
1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
2.All other power rails can ramp down together with NVVDD.
3.+1.8V_MAIN must power down after NVVDD power down
3.The progapation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

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Title	DGPU POWER SEQUENCING	
Size C	Document Number GK5CN6X	Rev V A
Date: Tuesday, January 16, 2018	Sheet 71 of 72	

Date Chang History

20170916
FB_EN_GC6_PCH from GPP_K0 to GPP_K10
P17 remove pull low
P22 remove pull high

20171010
1、删除Mini DP，HPD diode
2、增加RJ45，transform
3、修改成GJ power 小板
4、修改成GJ USB2.0小板
5、修改成GJ Audio小板
6、增加led
7、增加power SW
8、将wlan led GPIO改成ID_det
9、增加USB3.0x2 on borad
10、增加usb2.0x3
11、增加LID线路
12、增加Q-key1 SWx2
13、修改DDR CN1、CN11 footprint
14、删除hole H7、H9、H22
15、删除PQ45、C1430
16、修改USB3
17、修改HDMI、type-c footprint
18、增加H7、H9，删除H26
19、增加c4117、c4118、c4119、c4120、c4121
20、更新HDMI、type-c footprint
21、更新c4117、c4118、c4119、c4120、c4121 footprint
22、更新cn14、cn9 footprint
23、更新cn12、cn34 footprint
24、更新m.2、mini、bat conn footprint
25、更改GPIO扣，chg-o-led变成tp led；fanboost变成 c cover
26、更新SW6、led1、led2、led4、cn41、cn19、cn42、sw1、sw2、sw3、cn30、cn17、cn18等footprint
27、修改AUX-off线路
28、增加GPE1为VRA-PE
29、修改PCE5、PCE6电容为.1u
30、修改RJ45 pin number
31、删除H9，L24、L25、L26、L27垂直swap
32、修改L3，L10，L11，L28，L43的value footprint
33、删除NVDD和NVDSS co-lay
34、增加EC_lanwake
35、lanwake和wlanwake softstart
36、更改gpio lanwake
37、增加c1453、c1439、c1449、c1459
38、C3990，C3991的value改成22U-6.3-06R-M，footprint： M-C0603
39、更新c4117、c4118、c4119、c4120 footprint
40、修改L12、L14、L15、L17
41、修改PCIE5、6为14、15
42、NVVDD_EN改为NVDDS_PEX_VDD_EN
43、修改NV strap pin
44、增加R318，HDMI HDP释放电
45、GPU pull high GPIO9
46、增加R1003，预留NVVDDS VID pull high
47、增加C1430、C1473
48、把NVVDD和NVVDDS桥接电阻改成JUMP
49、增加C1460
50、增加HDMI bead B3、B4、B5、B6、B8、B9、B11、B17
51、修改NVVDD remote sense线路
52、增加NVVDD、NVVDDS Power GOOD loopback线路

12/05
1、R955改成16K
2、Del C2549
3、C2552改成4700P
4、R529改成28.7K
5、R530改成118K
6、R239改成4.7Ω
7、C554改成4700P
8、Del R944
9、Add C676、C678、C679 Psscap
10、删除靠近GPU Sense上拉下拉电阻
11、SSD1改成PCIE21-24
12、Add C1484、C1485、C1486、C1487、C1500、C1501、C1380、C1381、C1461、C1462、C1474、C1475---0603 footprint
13、MP2949 +3.3VA上拉加100K电阻R324

12/06
1、修改EDP pin19为power
2、删除AUX OFF线路
3、删除DCIN bead，改成FUSE
4、将APL3523改成APE8910
5、移除webcam on，增加bus_on
6、将HDMI mos改成二极管
7、Del NVVDD Snubber
8、将VRA_PE pull high +3.3VA
9、增加KB电控制线路，GPIO待定
10、增加+3.3V_LCD 电容
11、将HDD con 82改成+5VHDD
12、修改R194和R187为1%，且修改阻值
13、增加+5VA .1u电容
14、修改RTC 晶振电容为16p
15、Syspwrok、pchpwrok、rsmrst串1k电阻

12/08
1、修改USB port 5 3.1差分信号反接问题
2、增加co-lay lanwake

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Size: C
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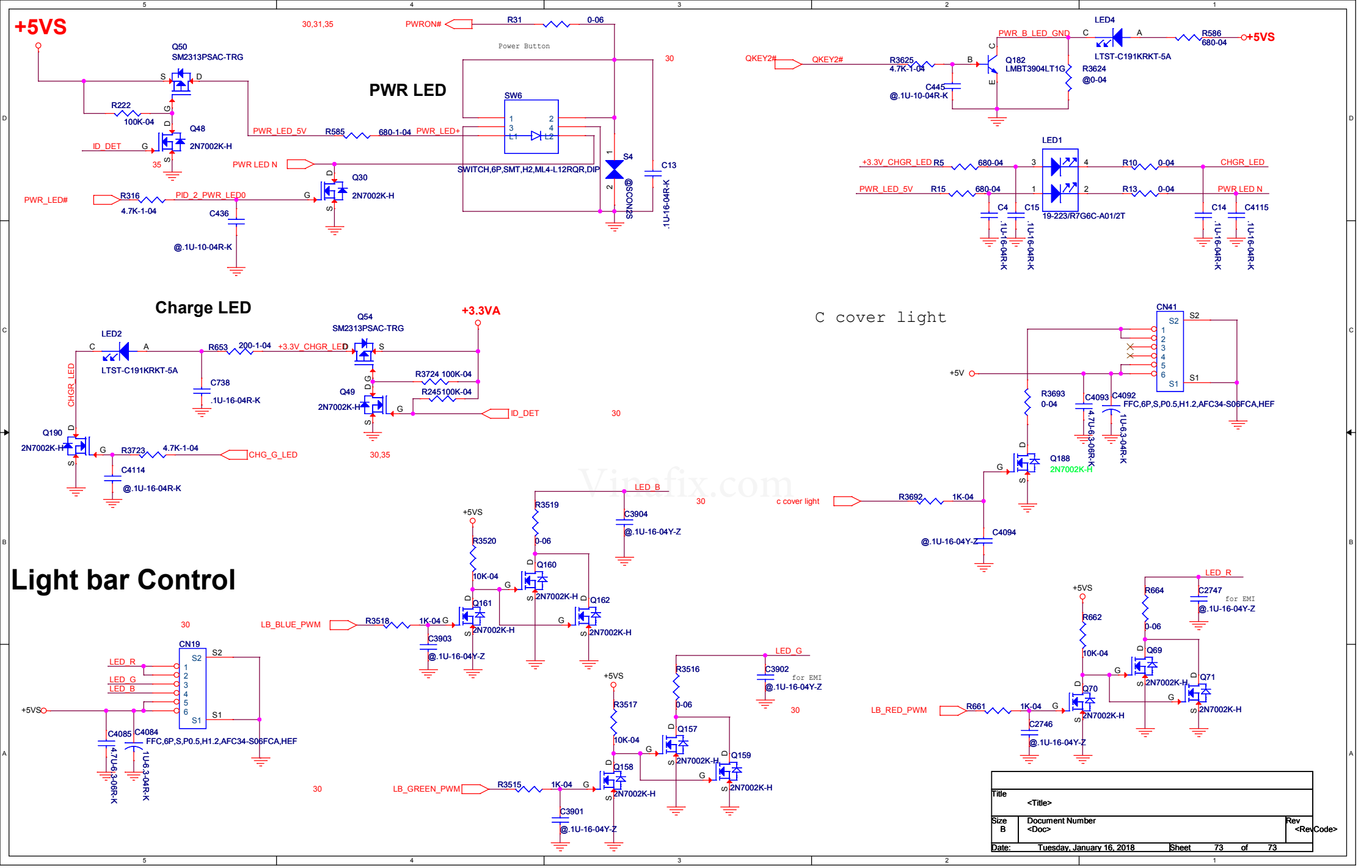
Rev: V A
Date: Tuesday, January 16, 2018
Sheet 72 of 72


+5VS
30,31,35
PWRON#
R31
0-06
Power Button
30
Q50
SM2313PSAC-TRG
PWR LED
SW6
R222
100K-04
Q48
2N7002K-H
ID_DET
35
PWR_LED_5V
R585
680-1-04
PWR_LED+
PWR LED N
Q30
2N7002K-H
PWR_LED#
R316
4.7K-1-04
PID_2_PWR_LED0
C436
@.1U-10-04R-K
SWITCH,6P,SMT,H2,ML4-L12RQR,DIP
S4
S2N50SG
C13
.1U-16-04R-K
QKEY2#
R3625
4.7K-1-04
C445
@.1U-10-04R-K
Q182
LMBT3904LT1G
PWR_B_LED_GND
LED4
LTST-C191KRKT-5A
R586
680-04
R3624
@0-04
LED1
+3.3V_CHGR_LED
R5
680-04
PWR_LED_5V
R15
680-04
19-223/R7G6C-A01/2T
R10
0-04
R13
0-04
CHGR_LED
PWR LED N
C4
C15
C14
C4115
.1U-16-04R-K
Charge LED
LED2
LTST-C191KRKT-5A
R653
200-1-04
C738
.1U-16-04R-K
CHGR_LED
Q190
2N7002K-H
R3723
4.7K-1-04
CHG_G_LED
C4114
@.1U-16-04R-K
Q54
SM2313PSAC-TRG
+3.3VA
+3.3V_CHGR_LED
R3724 100K-04
Q49
2N7002K-H
R245100K-04
ID_DET
30
30,35
C cover light
CN41
FFC,6P,S,P0.5,H1.2,AFC34-S06FCA,HEF
R3693
0-04
C4093
4.7U-6.3-06R-K
C4092
1U-6.3-04R-K
Q188
2N7002K-H
R3692
1K-04
C4094
@.1U-16-04Y-Z
c cover light
Light bar Control
CN19
LED_R
LED_G
LED_B
C4085
4.7U-6.3-06R-K
C4084
1U-6.3-04R-K
FFC,6P,S,P0.5,H1.2,AFC34-S06FCA,HEF
LB_BLUE_PWM
R3518
1K-04
C3903
@.1U-16-04Y-Z
Q161
Q160
Q162
2N7002K-H
R3519
0-06
R3520
10K-04
C3904
@.1U-16-04Y-Z
LB_GREEN_PWM
R3515
1K-04
C3901
@.1U-16-04Y-Z
Q158
Q157
Q159
R3517
R3516
C3902
for EMI
@.1U-16-04Y-Z
LB_RED_PWM
R661
1K-04
C2746
@.1U-16-04Y-Z
Q70
Q69
Q71
R662
R664
C2747
for EMI
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Title
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Size
B
Document Number
<Doc>
Rev
<RevCode>
Date:
Tuesday, January 16, 2018
Sheet
73
of
73