Project Name :GK5KN6Z

Platform : CFL_H+N17E-G1

PAGE CONTENT

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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Title: INDEX

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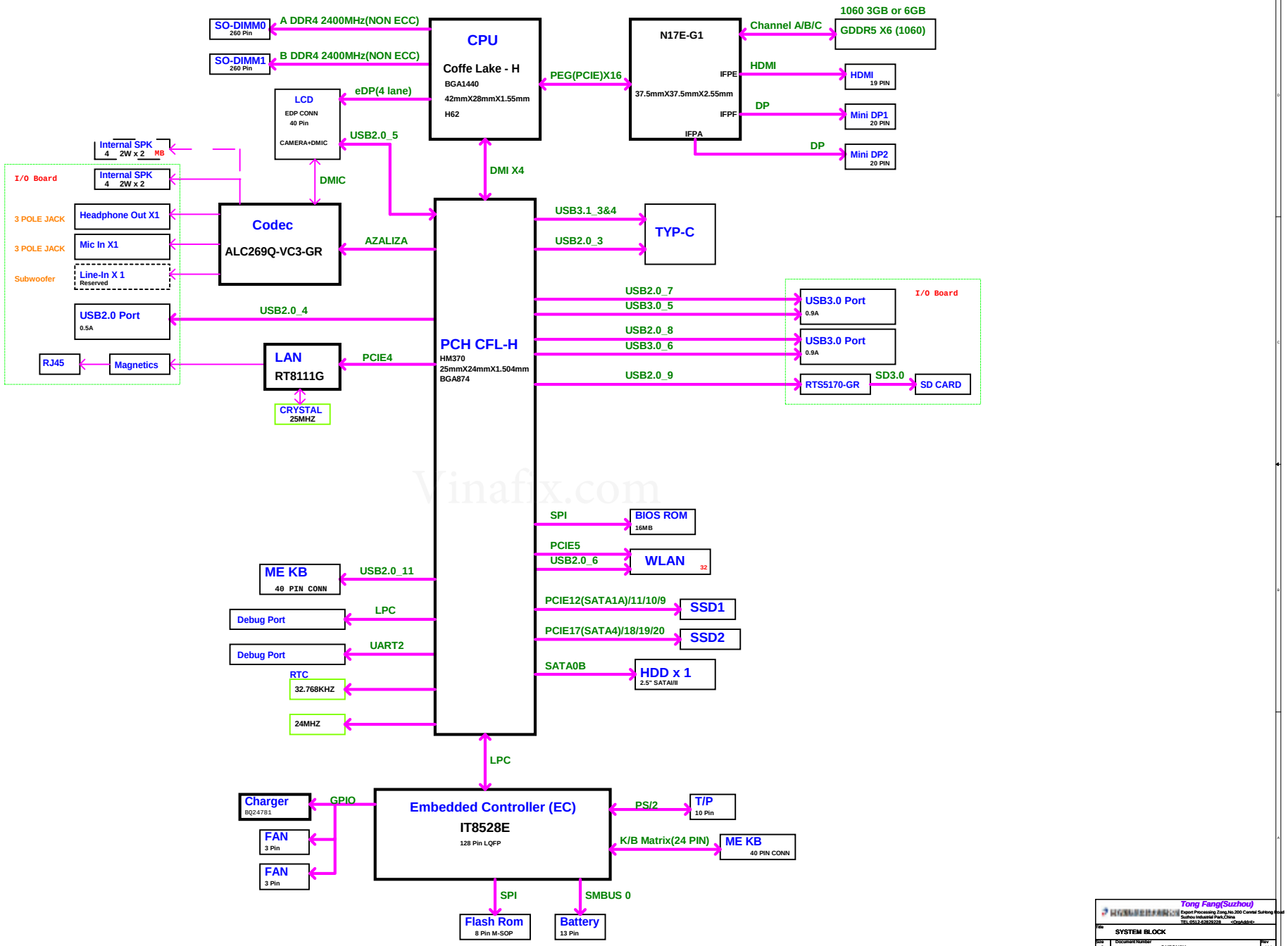
SYSTEM BLOCK DIAGRAM



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Title: SYSTEM BLOCK

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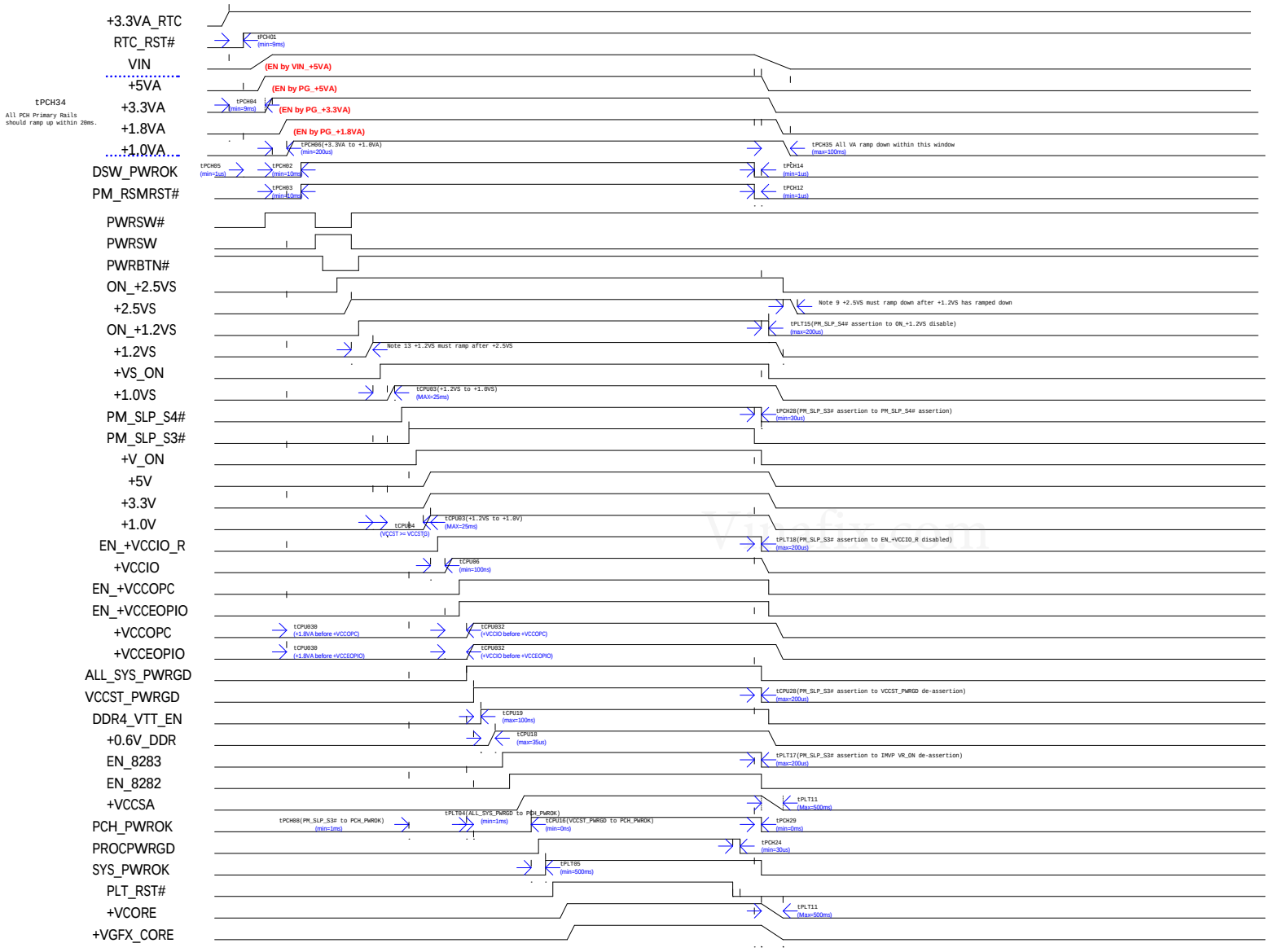
POWER ON SEQUENCE



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Title: POWER DIAGRAM & SEQUENCE

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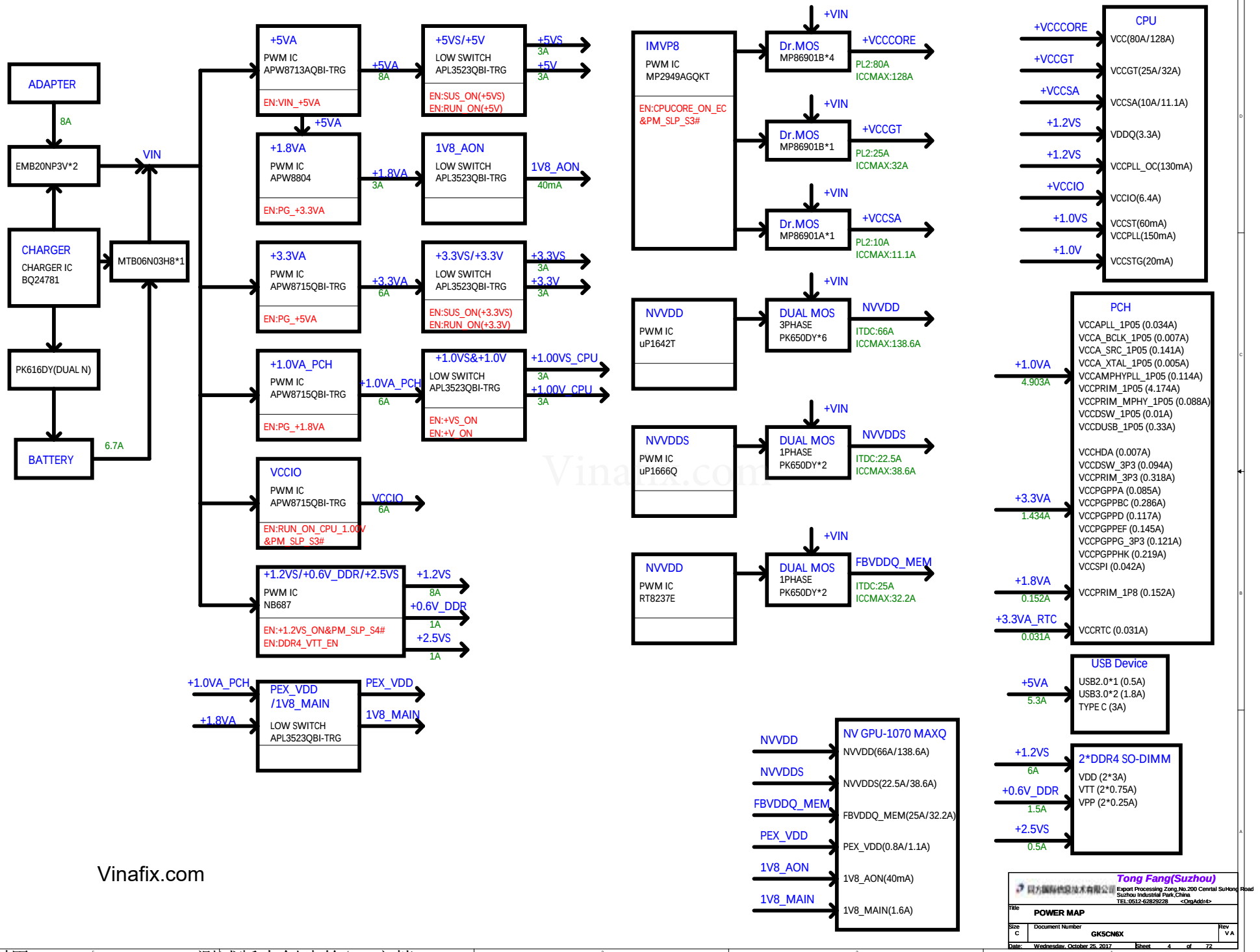


GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1_CHG_R_LED	
GPA5	PID_2_PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

GH5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1_CHG_R_LED	UP / GPO
GPA5	PID_2_PWR_LED	UP / GPO
GPA6	ME_KB_LED	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor in	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	EG_DA	
GPE2	EG_Cycle start	
GPE3	EG_CLK	
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	PANEL_VCC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC removal	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3		Dn/GPI/ID3
GPH4		Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6		Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	PANEL_DETECT	/GPI/Z
GPI2	PCIE_WAKE#	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

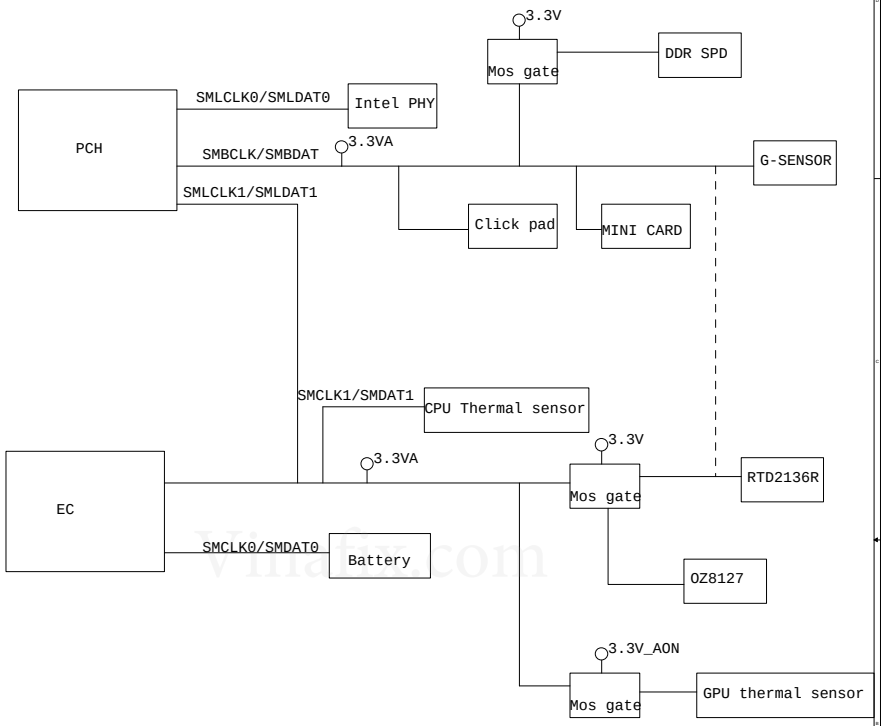
GI5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1_CHG_R_LED	UP / GPO
GPA5	PID_2_PWR_LED	UP / GPO
GPA6	PM_RSMRST#	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor in	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPI
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	DGPU_EN_EC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC removal	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON/SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3	DGPU_EN_EC_Keep	Dn/GPI/ID3
GPH4	Dgpu_RST_EC#	Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6	Clear CMOS	Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	EC_OVERT_NVVDD#	/GPI/Z
GPI2	PCIE_WAKE#/Dgpu_RST_EC#_keep	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

EXT EC

ITE8302 GPIO		Default Pull/Mode
GPIO4	EXT_WIFI_ON	UP / GPO
GPIO5	EC_OVERT_NVVDD#	UP / GPO
GPIO7	Dgpu_RST_EC#_keep	UP / GPO
GPIO9	SUS_ON	UP / GPO
GPIO11	CTL3	UP / GPO
GPIO13	CTL2	UP / GPO
GPIO18	EXT_Q_key0	UP / GPO
GPIO20	EXT_Q_key1	UP / GPO
GPIO22	PWR_USB#	UP / GPI
GPIO24	+1.2VS_ON	UP / GPI
GPIO26	LID1#	Dn / GPI
GPIO27	Dgpu_RST_EC#	Z / GPI
GPIO29	PM_RSMRST#	Z / GPI
GPIO31	DGPU_EN_EC_Keep	Z / GPO
GPIO33	DGPU_EN_EC	UP / GPI
GPIO35	Clear CMOS	Dn / GPI

SMBUS BLOCK



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File: GPIO & SMBUS Block

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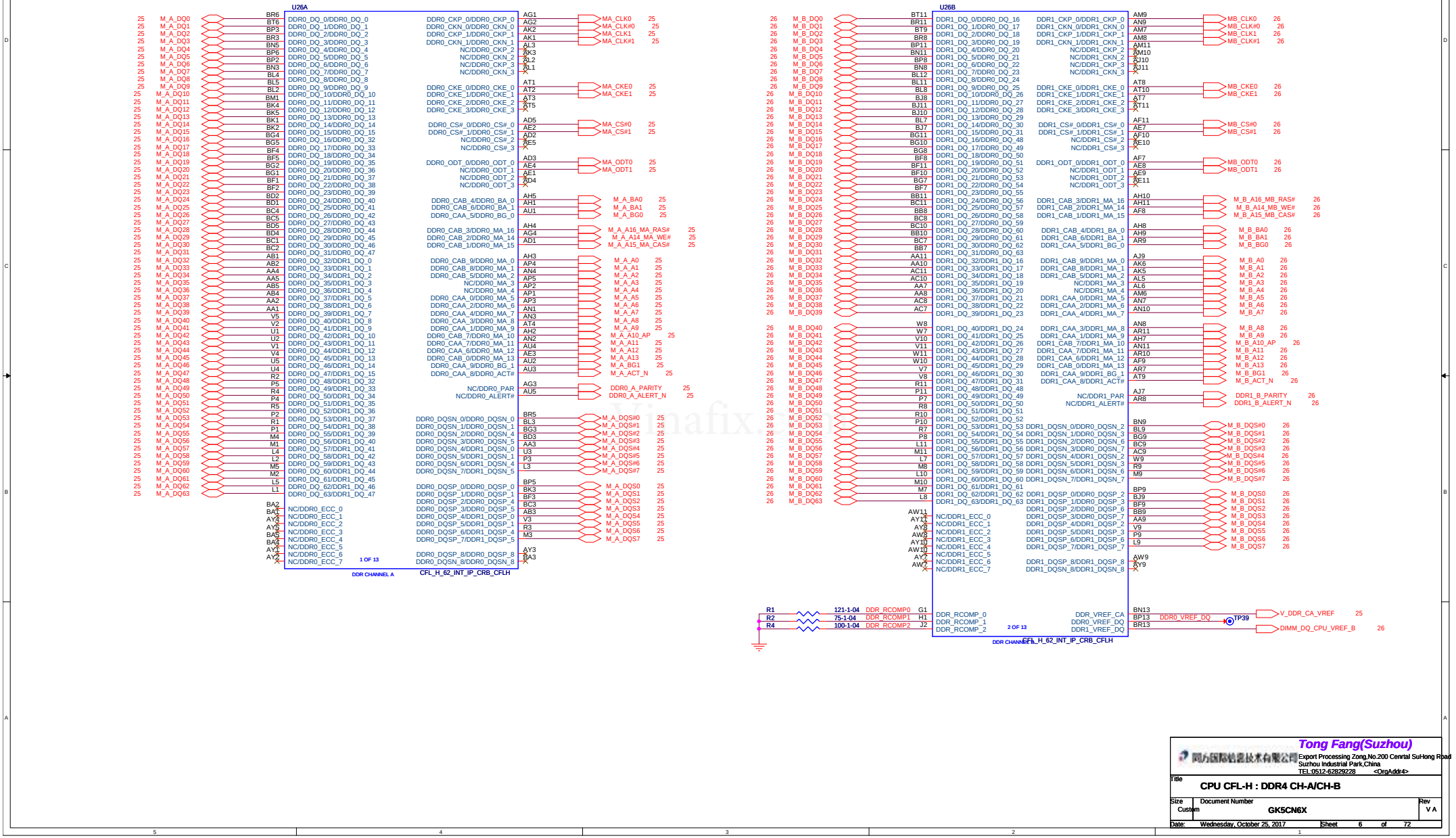

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Title: CPU CFL-H : DDR4 CH-A/CH-B

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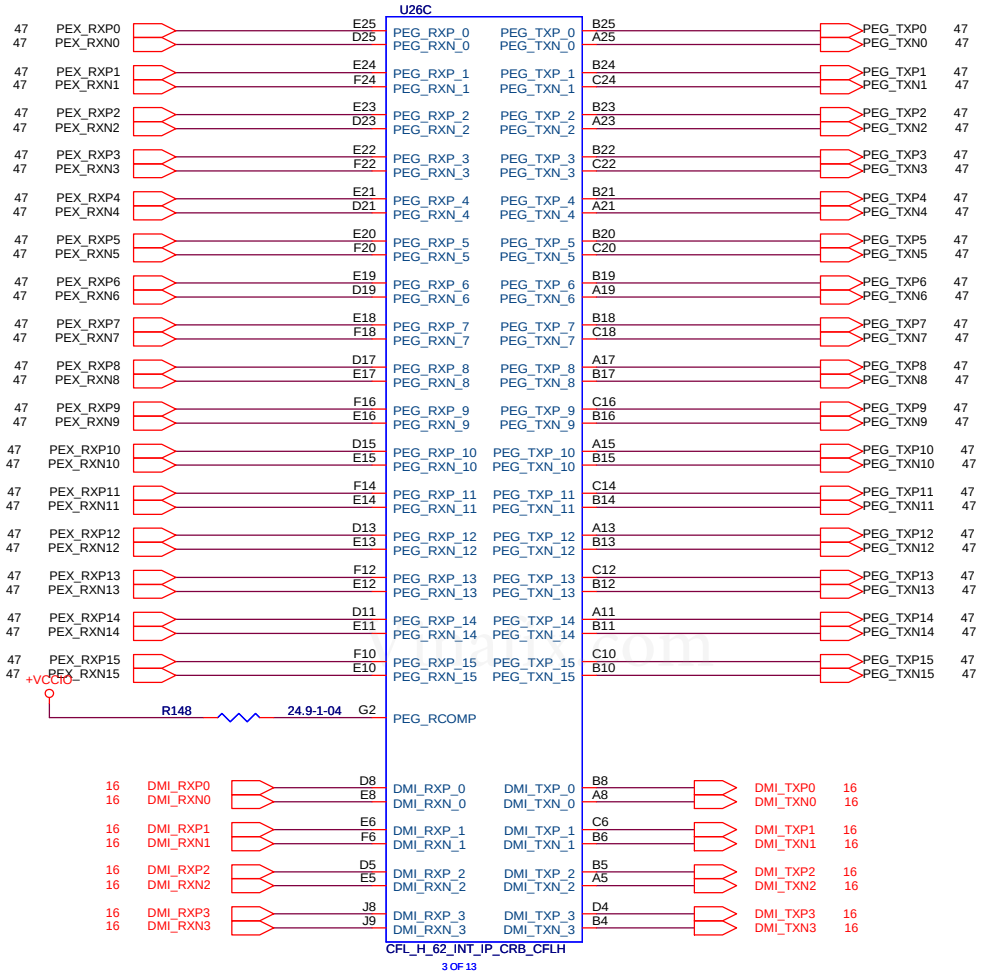

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	[2:0]	[1:0]	[0:0]	CFG [6]	CFG [5]	CFG [4]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1x8	x8	x8	N/A	1	0	1	0	1	2	3	-	5	6	7	0	1	2	3	-	5	6	7
1x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8 + 2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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Title	CPU CFL-H : PEG/DMI		
Size B	Document Number GK5CN6X		Rev V A
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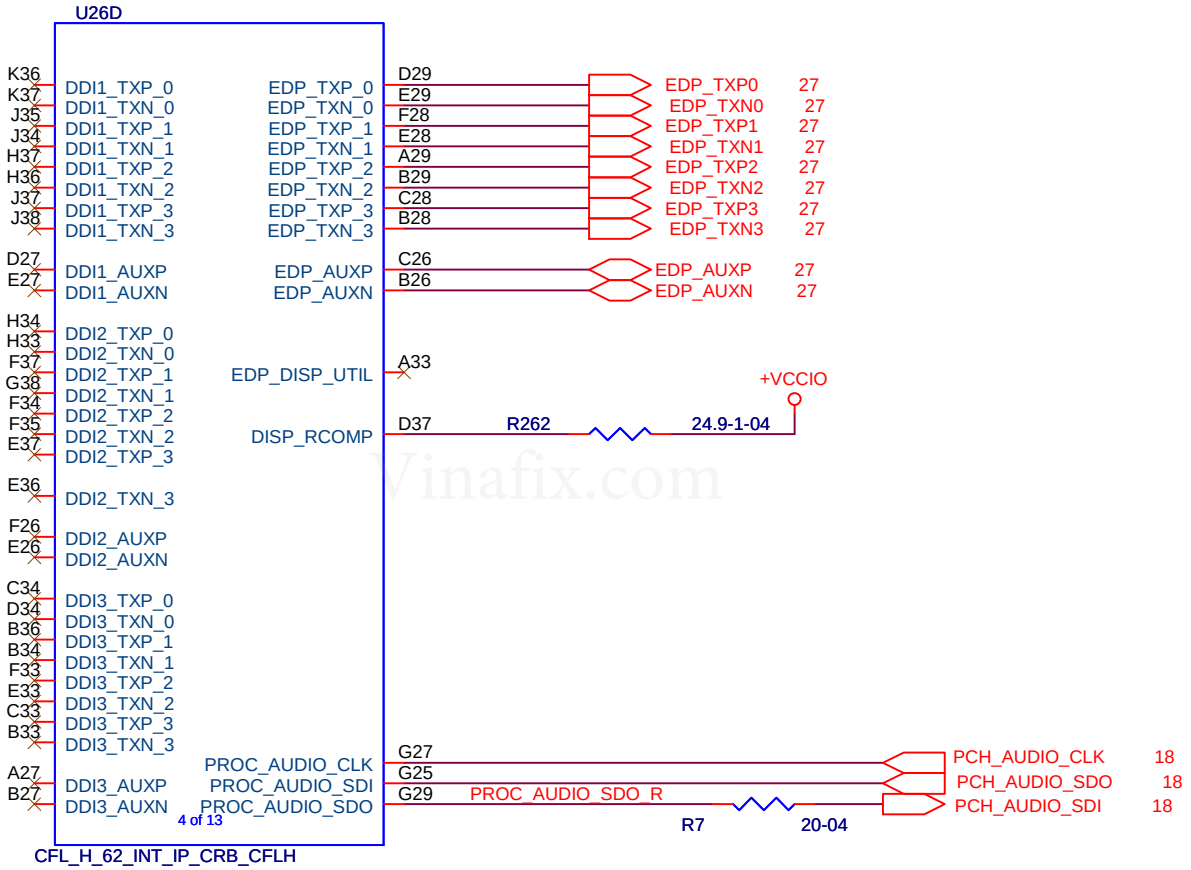

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Title
CPU CFL-H : DDI/EDP

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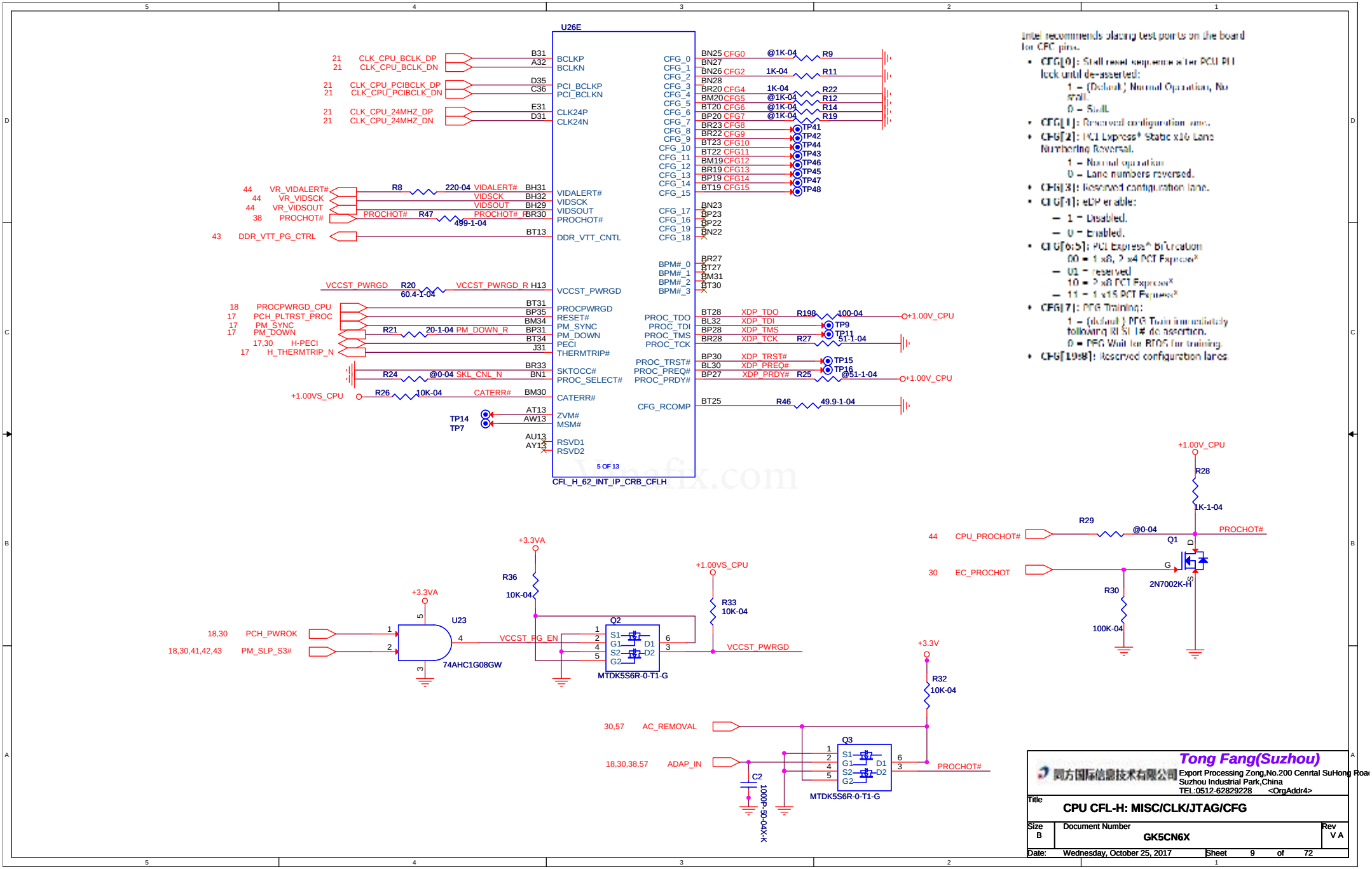

Intel recommends placing test points on the board for CFG pins.

- CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
  1 – (Default) Normal Operation, No stall.
  0 – Stall.
- CFG[1]: Reserved configuration lane.
- CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
  1 – Normal operation.
  0 – Lane numbers reversed.
- CFG[3]: Reserved configuration lane.
- CFG[4]: eDP enable:
  – 1 – Disabled.
  – 0 – Enabled.
- CFG[6:5]: PCI Express* Bifurcation
  00 – 1 x8, 2 x4 PCI Express*
  – 01 – reserved
  10 – 2 x8 PCI Express*
  – 11 – 1 x16 PCI Express*
- CFG[7]: PEG Training:
  1 – (default) PEG Train immediately following RESET# de-assertion.
  0 – PEG Wait for BIOS for training.
- CFG[19:8]: Reserved configuration lanes.

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Title: CPU CFL-H: MISC/CLK/JTAG/CFG		
Size: B	Document Number: GK5CN6X	Rev: V A
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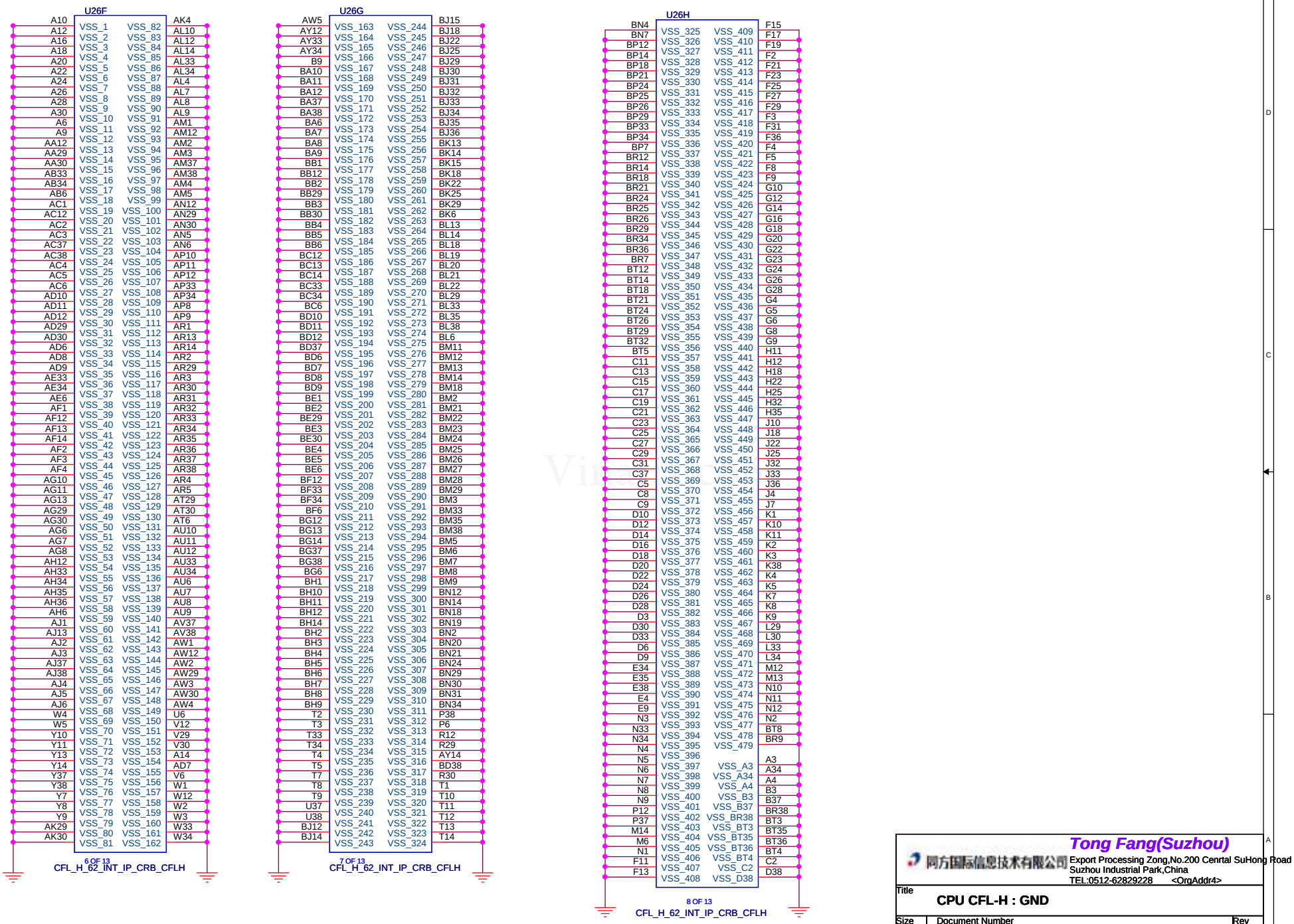

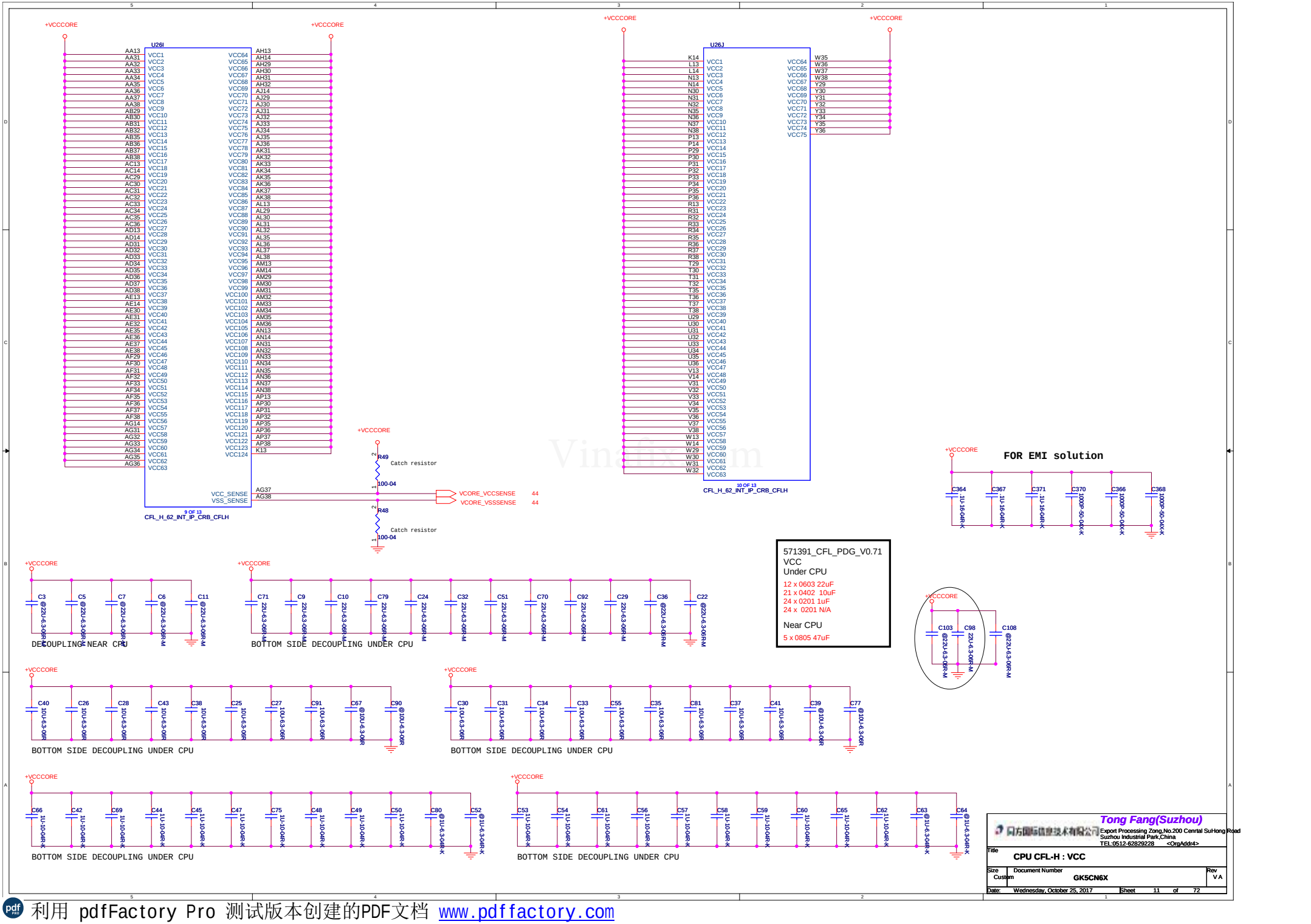

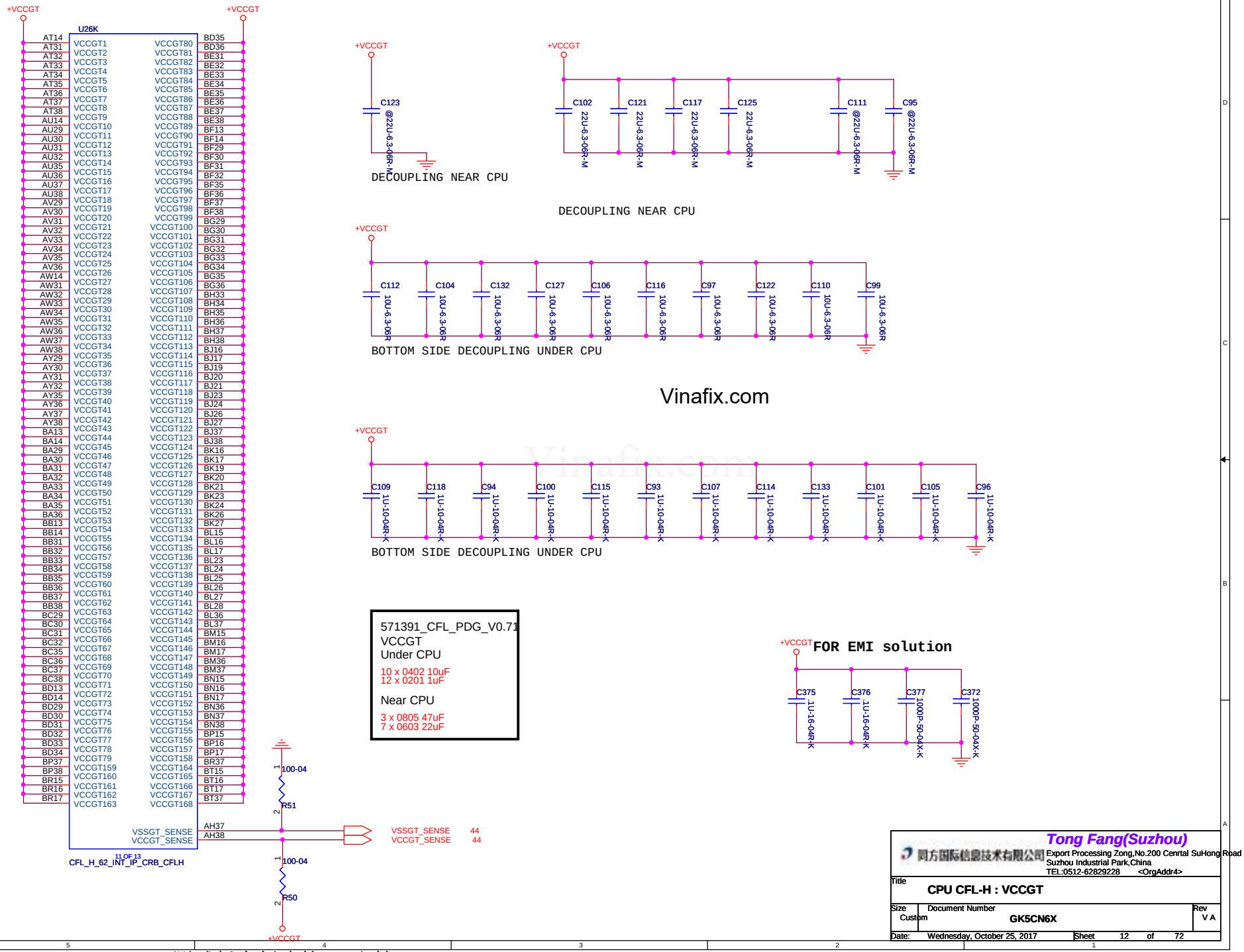

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Title	CPU CFL-H : VCCGT	
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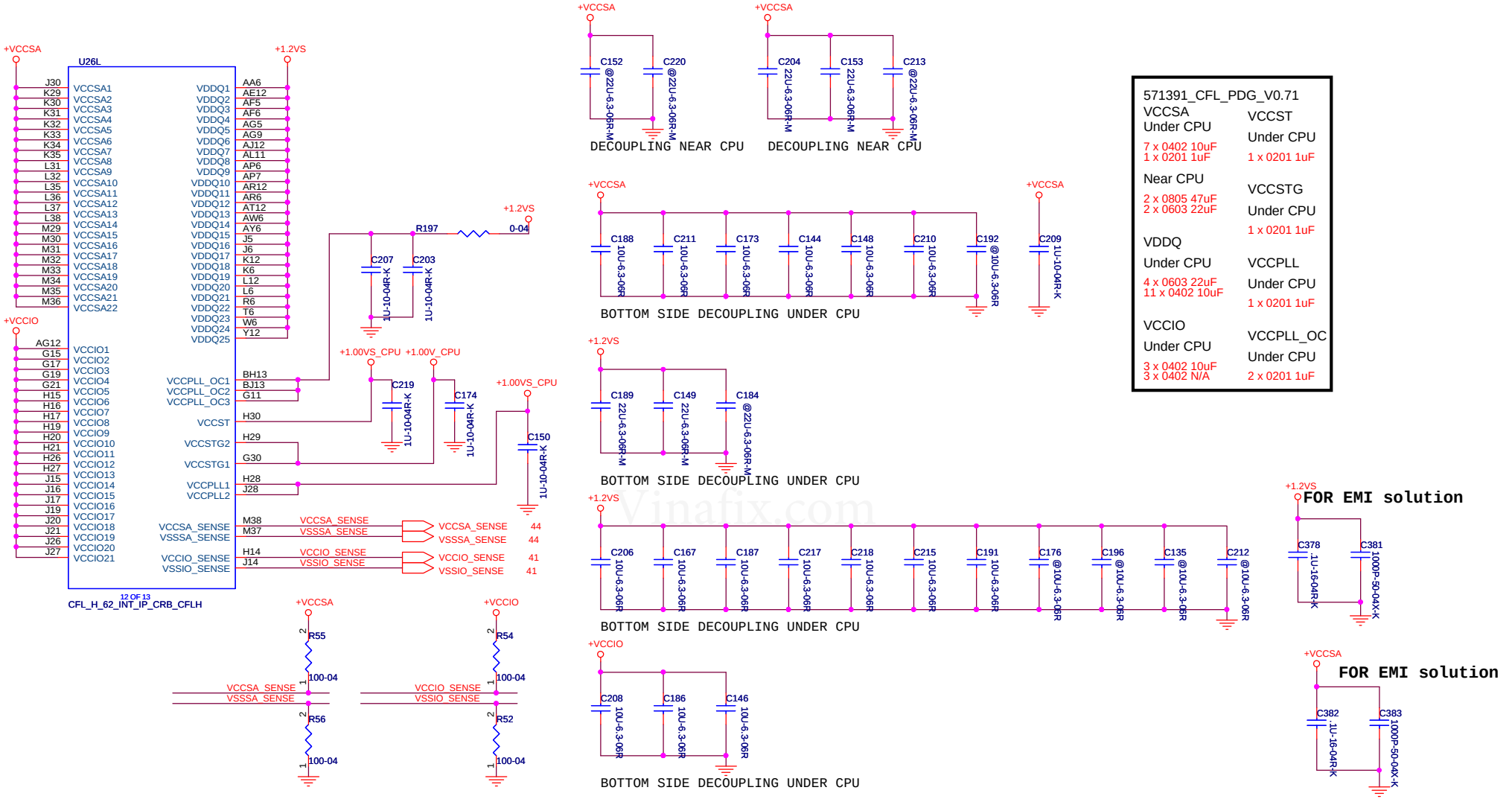

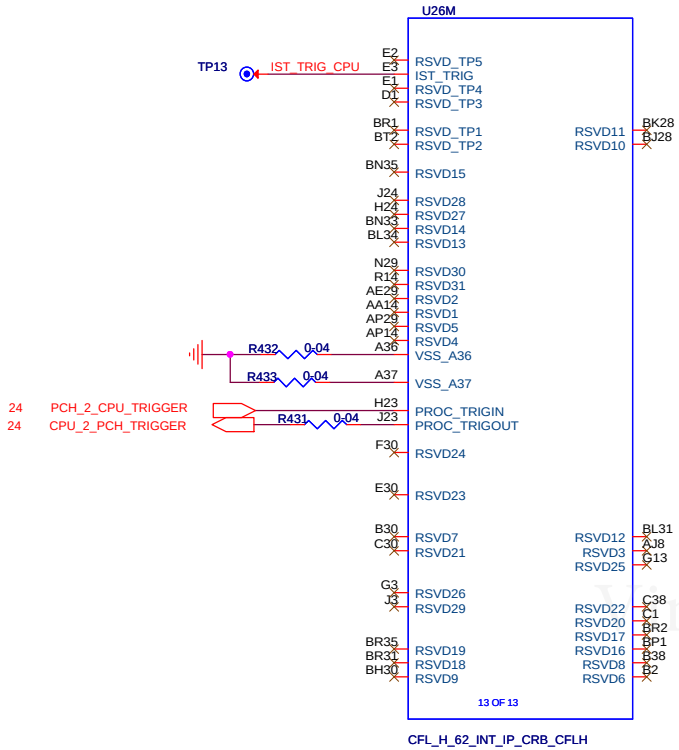

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Title: CPU CFL-H : TRIG/RSVD

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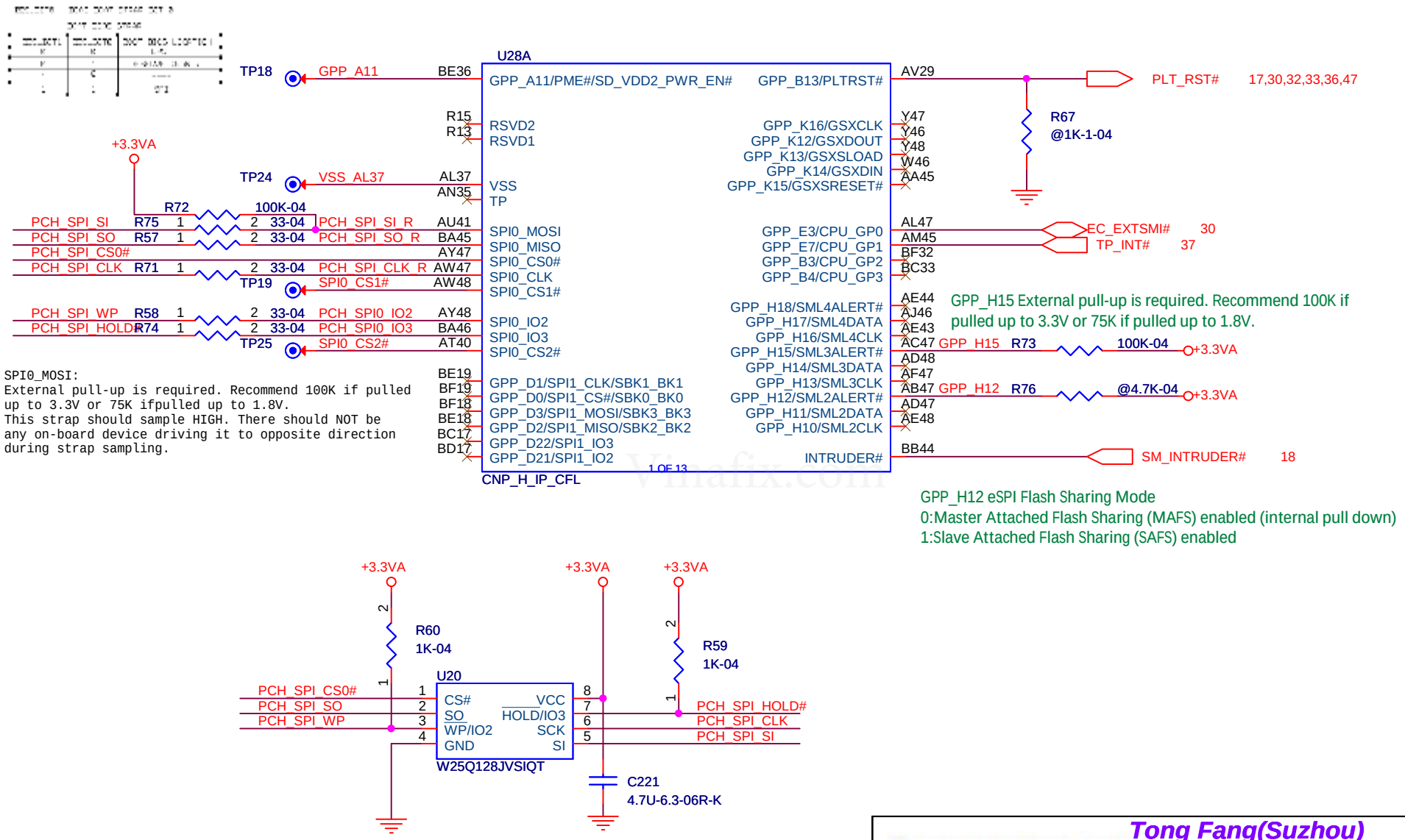

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Title: PCH CFL-H : SPI		
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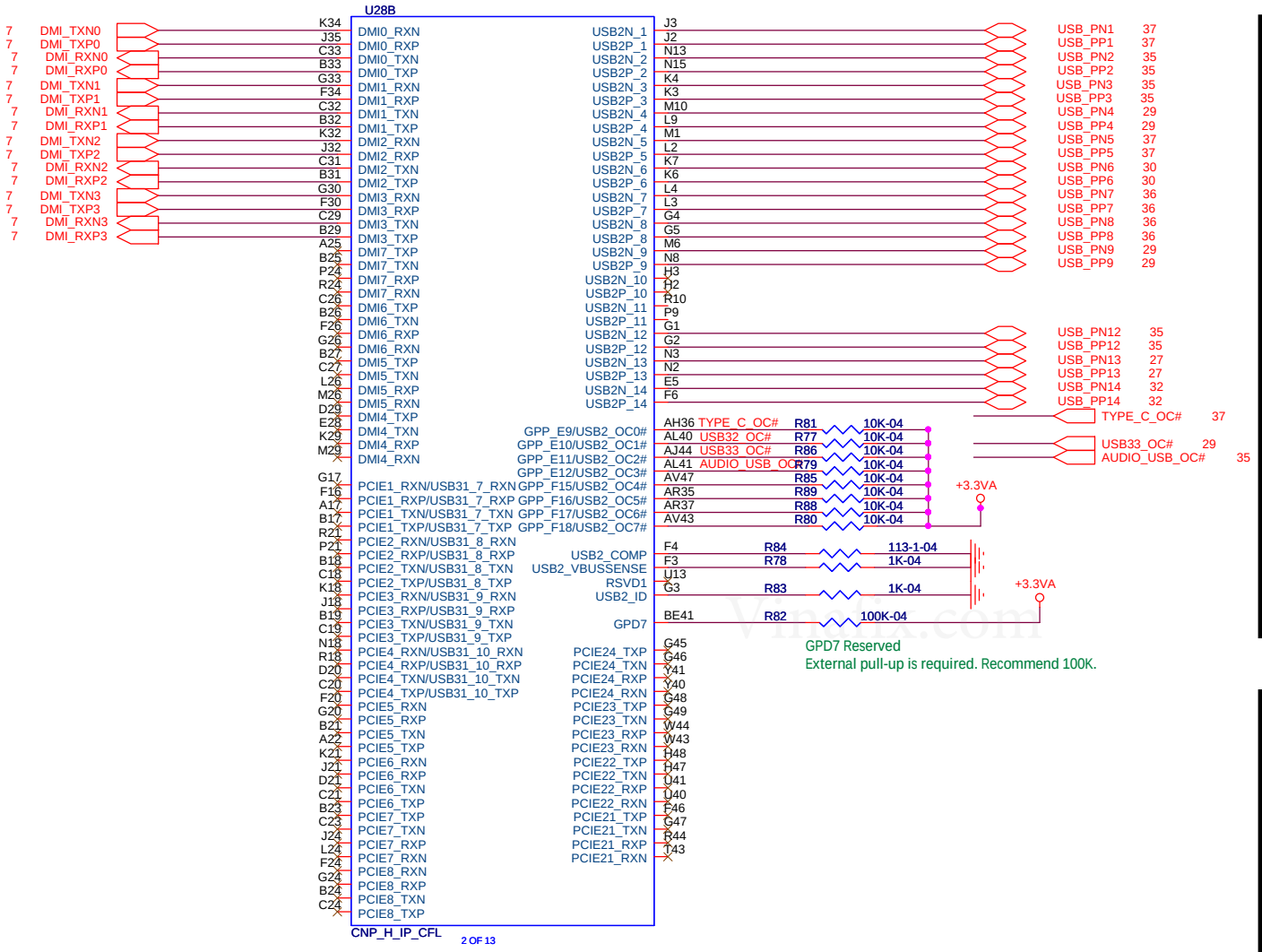

USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on AUDIO DB
USB3	USB2.0 ON AUDIO DB
USB4	USB3.0 Port1
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	USB2.0 DB port1
USB8	USB2.0 DB port2
USB9	USB3.0 Port2
USB10	N/A
USB11	N/A
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

USB OC Configuration Table	
OC0	TYPE_C_OC#
OC1	N/A
OC2	USB3.0 DB
OC3	AUDIO_USB DB
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

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Title: PCH CFL-H : DMI/USB2.0

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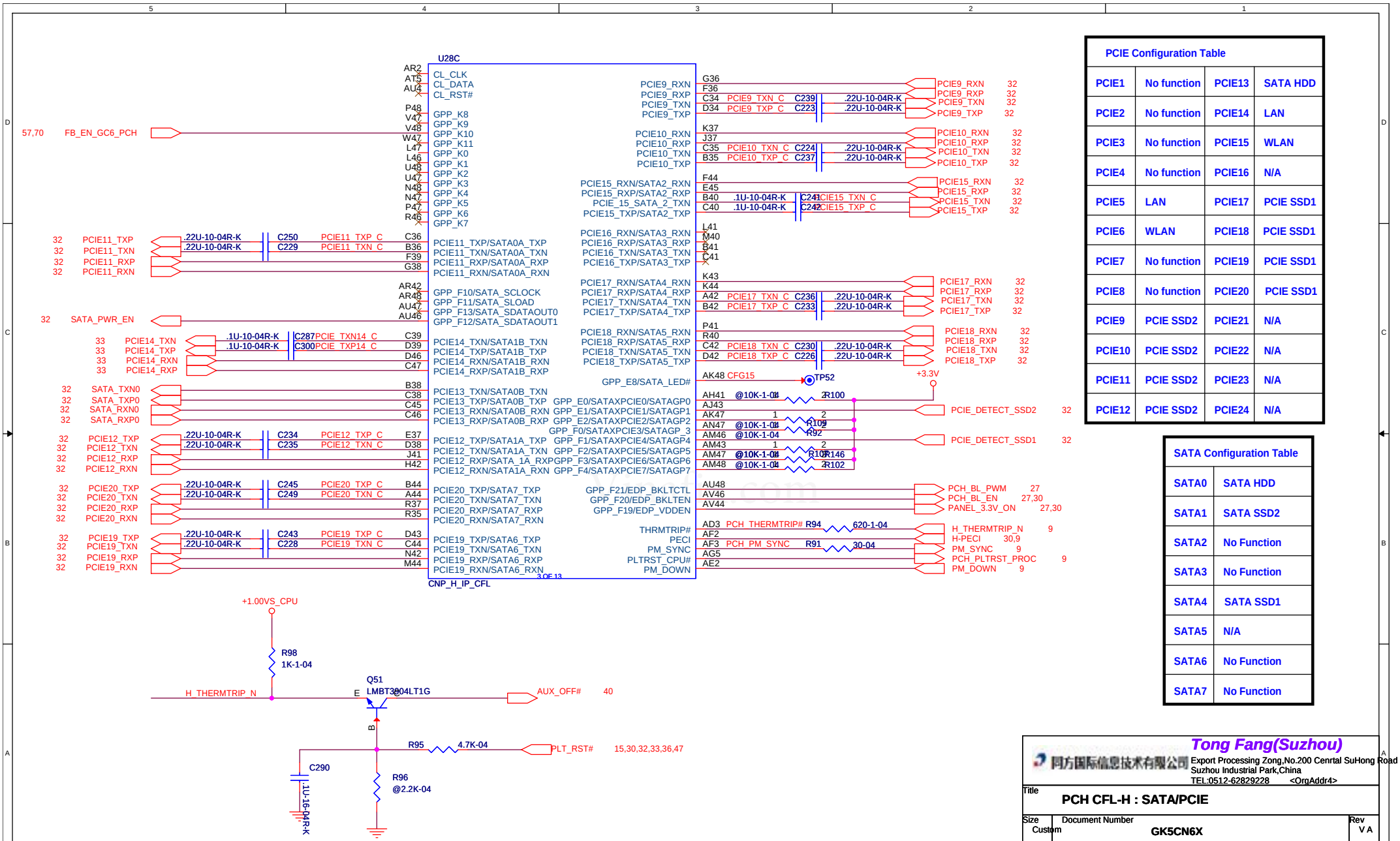

PCIE Configuration Table			
PCIE1	No function	PCIE13	SATA HDD
PCIE2	No function	PCIE14	LAN
PCIE3	No function	PCIE15	WLAN
PCIE4	No function	PCIE16	N/A
PCIE5	LAN	PCIE17	PCIE SSD1
PCIE6	WLAN	PCIE18	PCIE SSD1
PCIE7	No function	PCIE19	PCIE SSD1
PCIE8	No function	PCIE20	PCIE SSD1
PCIE9	PCIE SSD2	PCIE21	N/A
PCIE10	PCIE SSD2	PCIE22	N/A
PCIE11	PCIE SSD2	PCIE23	N/A
PCIE12	PCIE SSD2	PCIE24	N/A

SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD2
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD1
SATA5	N/A
SATA6	No Function
SATA7	No Function

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Title: PCH CFL-H : SATA/PCIE

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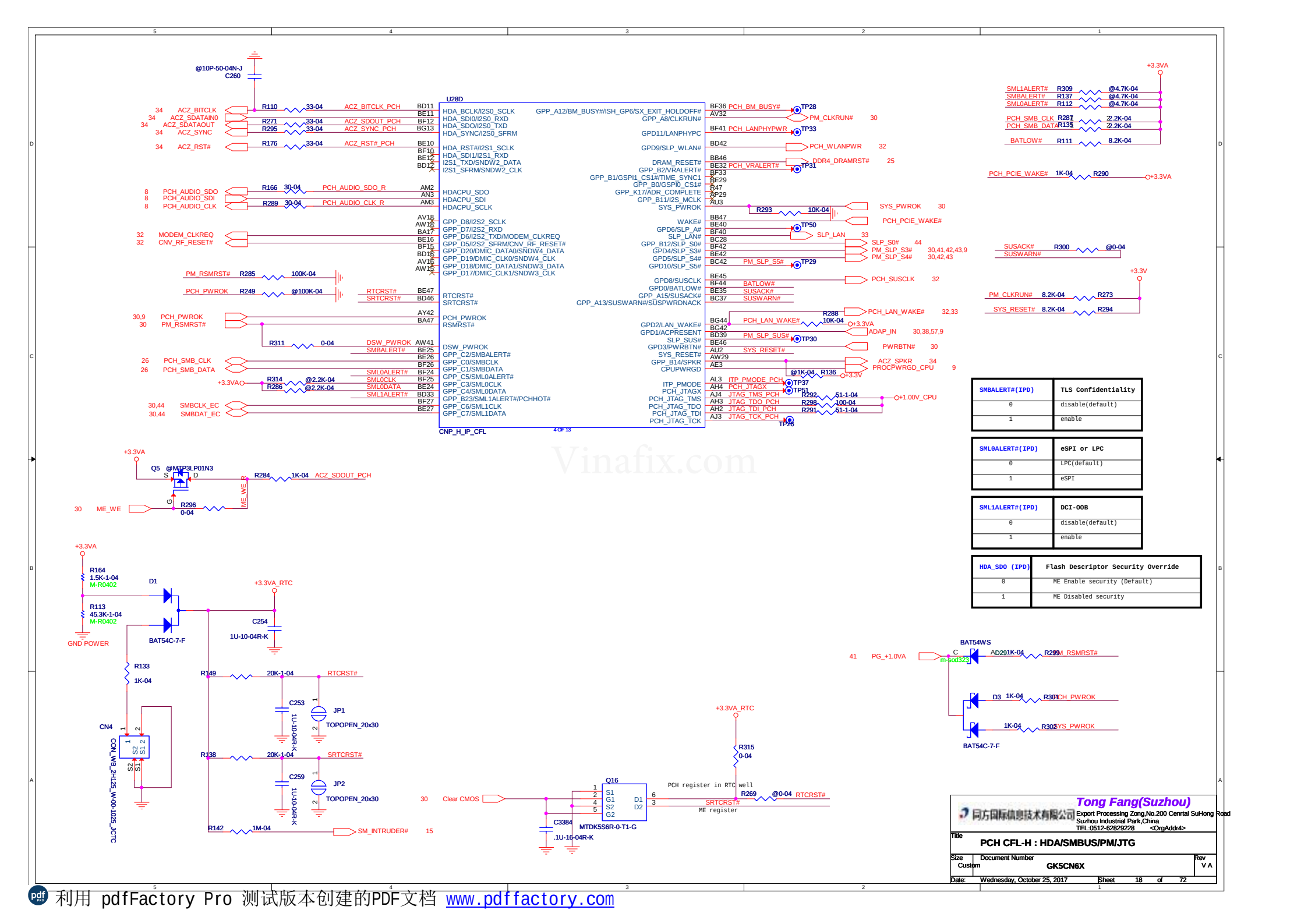

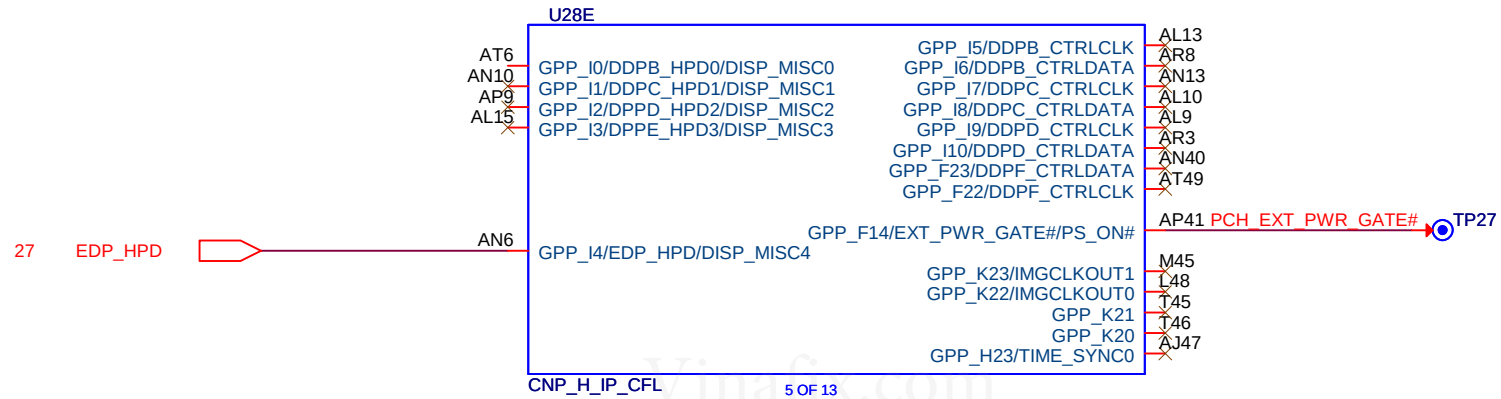

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Title
PCH CFL-H : DDI CONTROL

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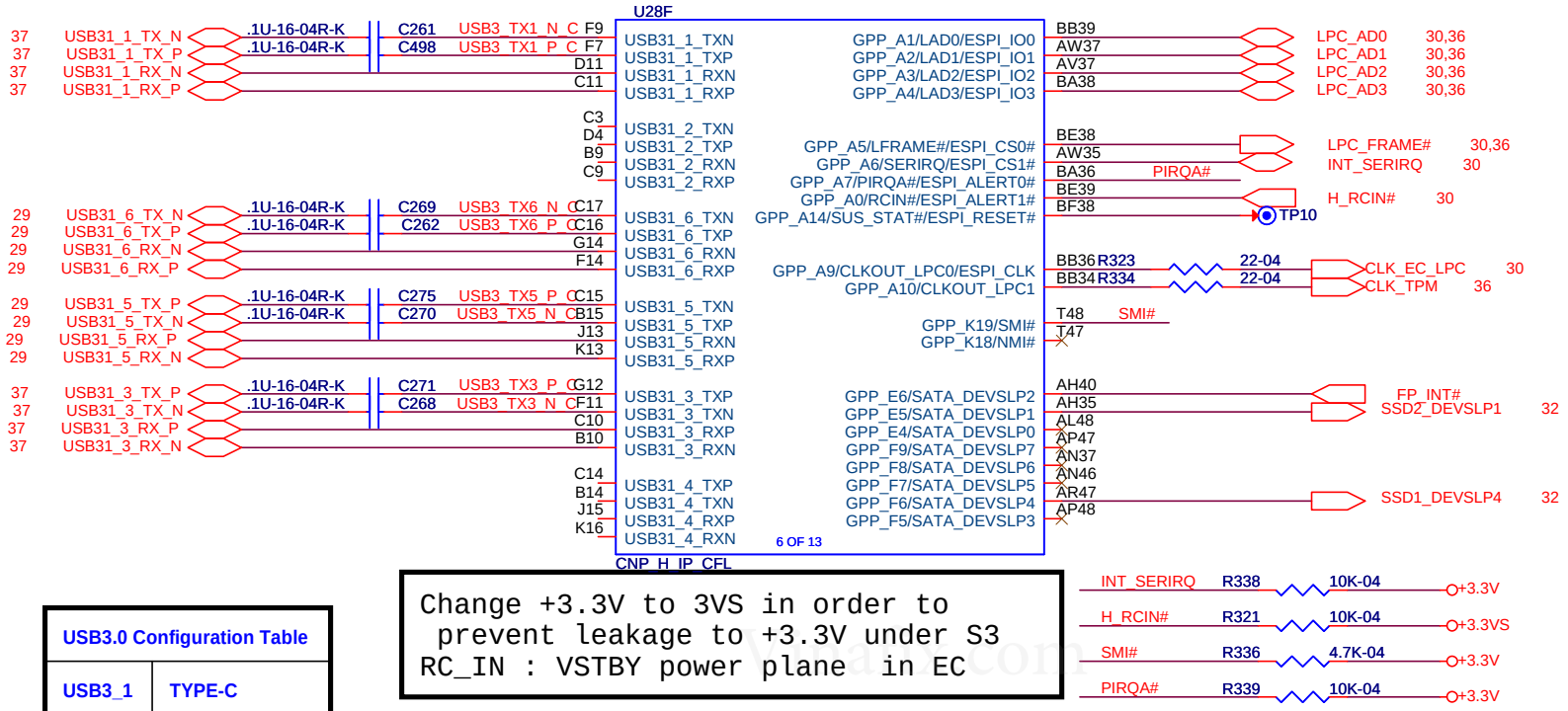

USB3.0 Configuration Table	
USB3_1	TYPE-C
USB3_2	N/A
USB3_3	TYPE-C
USB3_4	N/A
USB3_5	USB3.0 Port2
USB3_6	USB3.0 Port1
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC

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Title: PCH CFL-H : USB3.0/LPC

Size: Custom | Document Number: GK5CN6X | Rev: V A

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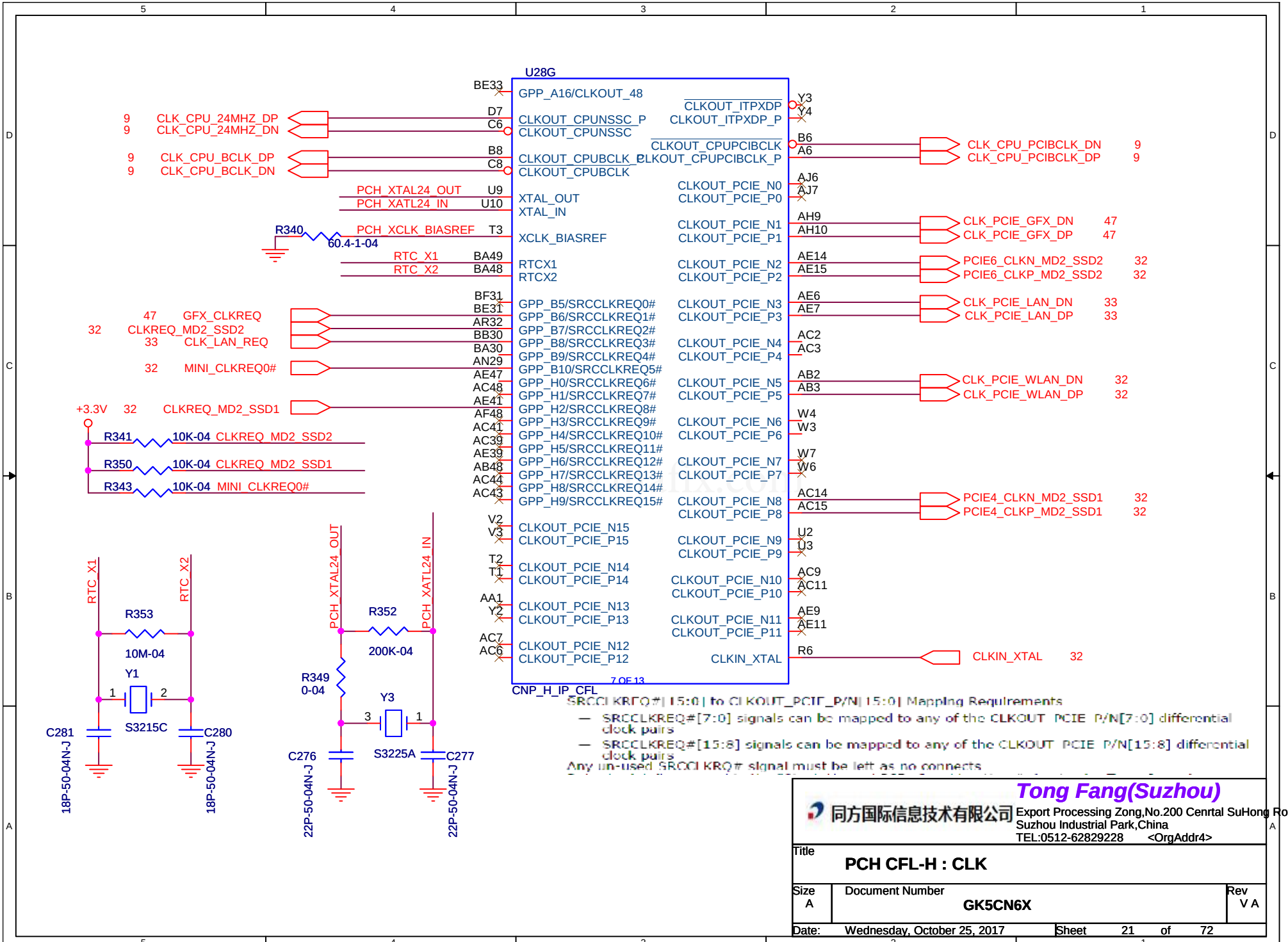

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Title	PCH CFL-H : CLK	
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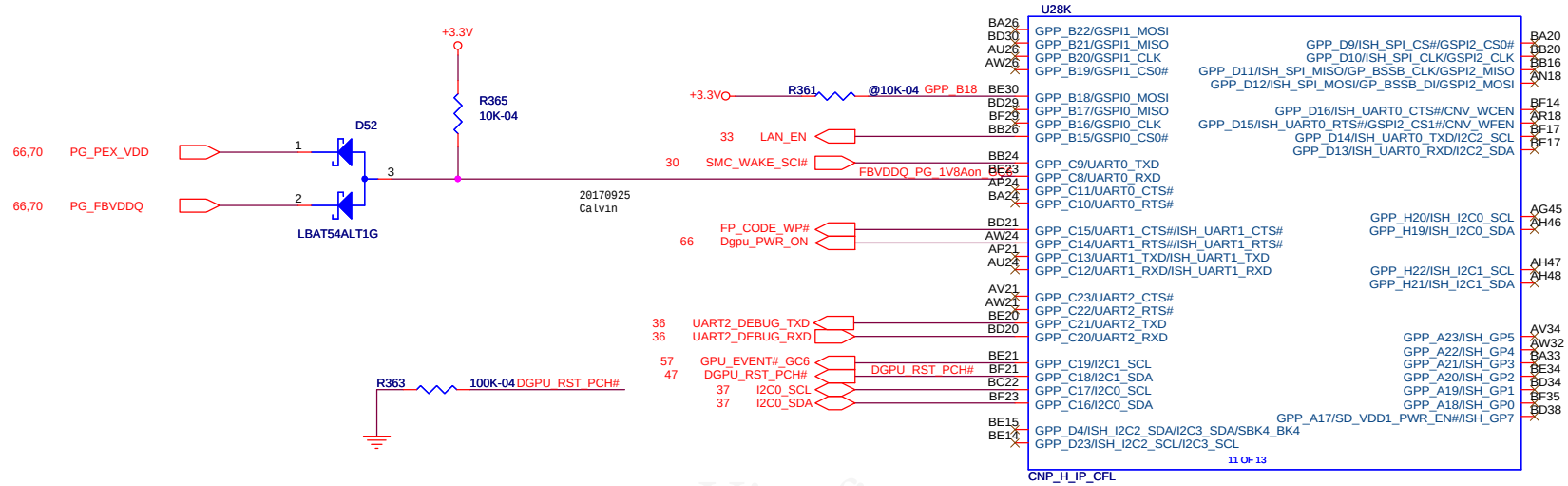
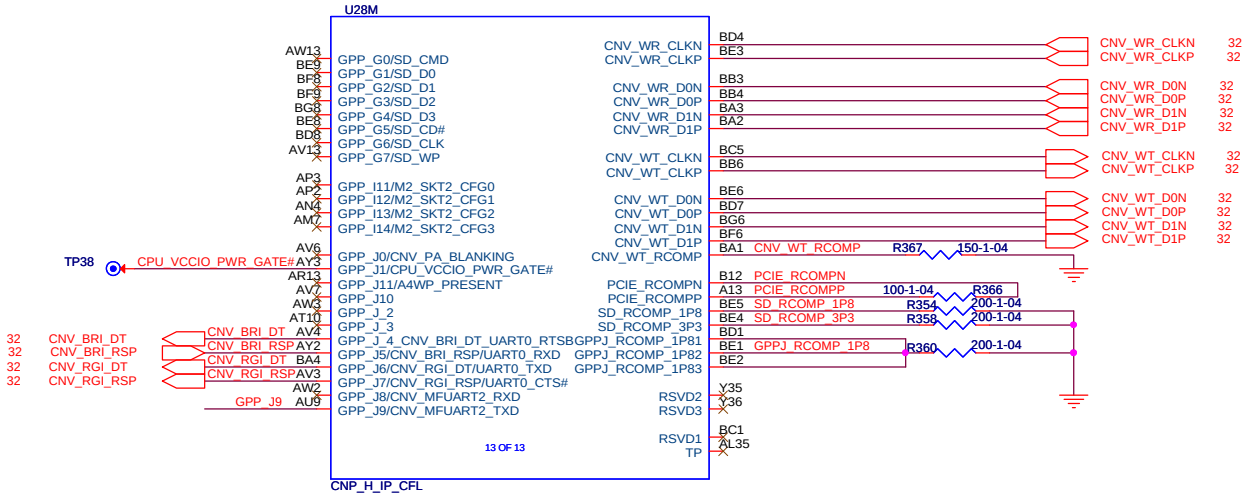
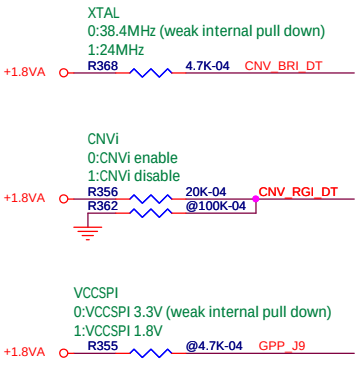
GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable "No Reboot" mode. (Default)
1	Enable "No Reboot" mode







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Title		
PCH CFL-H:GSPI/UART/I2C/CNVi		
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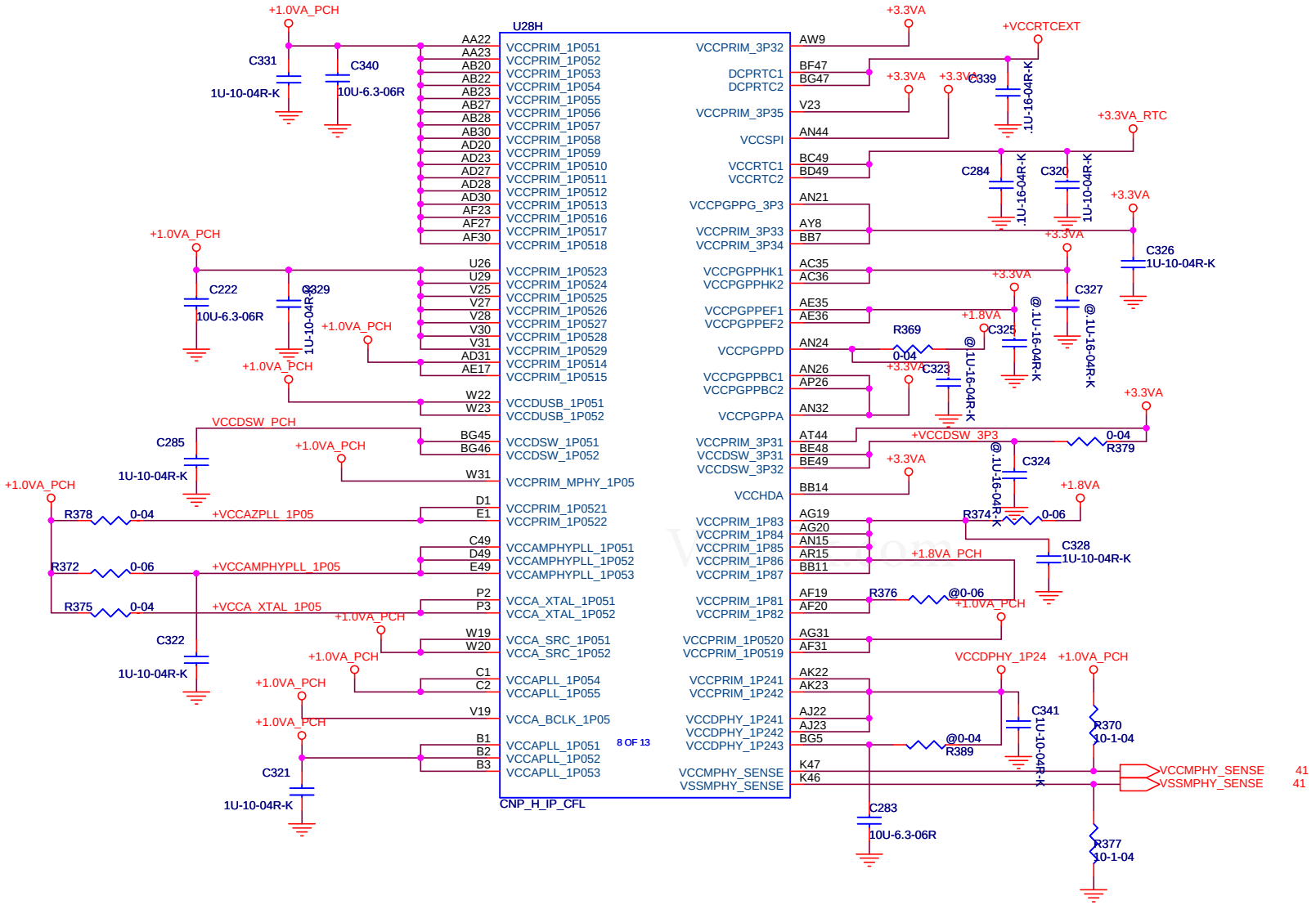

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Title	PCH CFL-H : POWER	
Size: Custom	Document Number: GK5CN6X	Rev: V A
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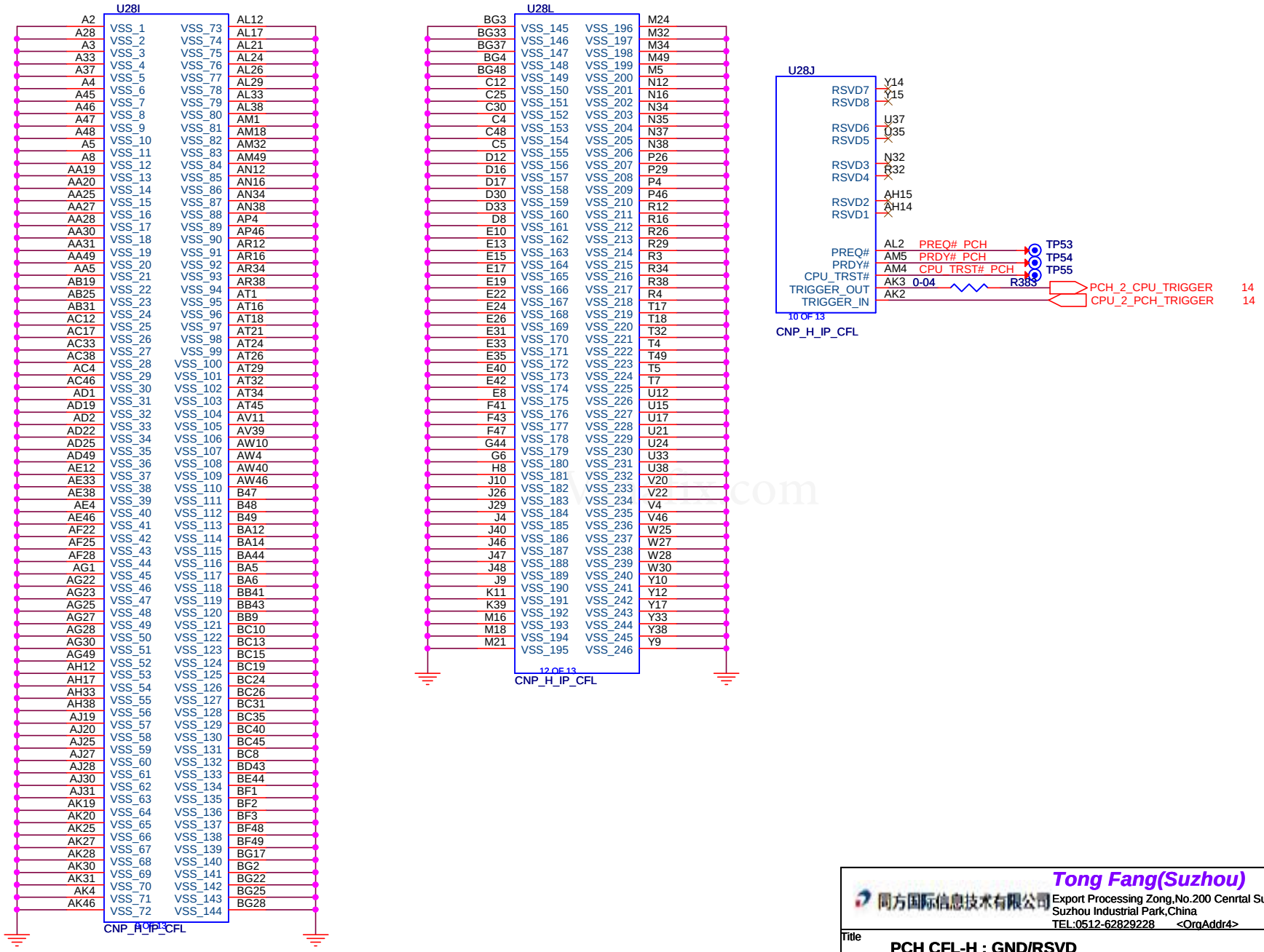

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Title: PCH CFL-H : GND/RSVD			
Size: Custom	Document Number: GK5CN6X		Rev: V A
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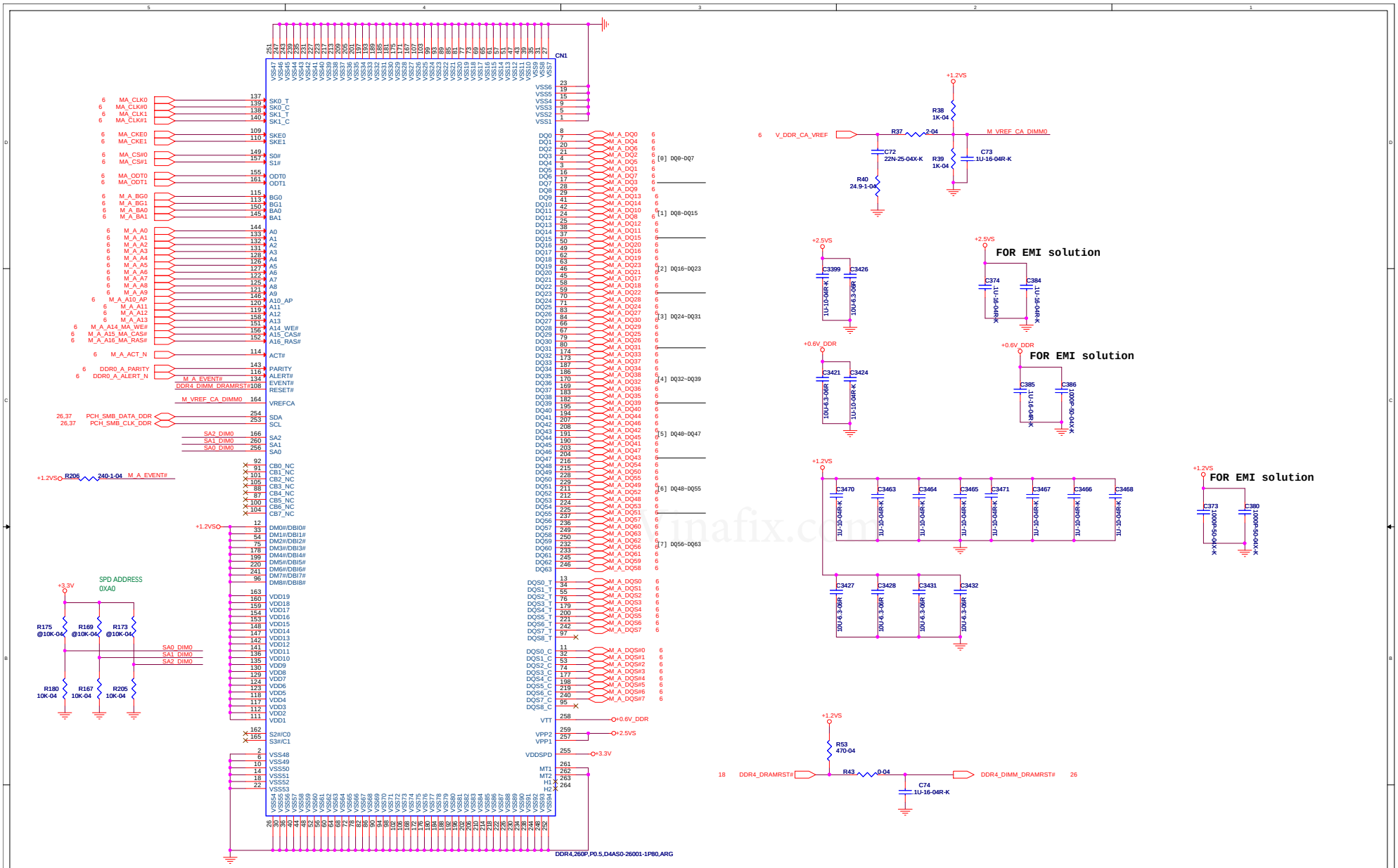
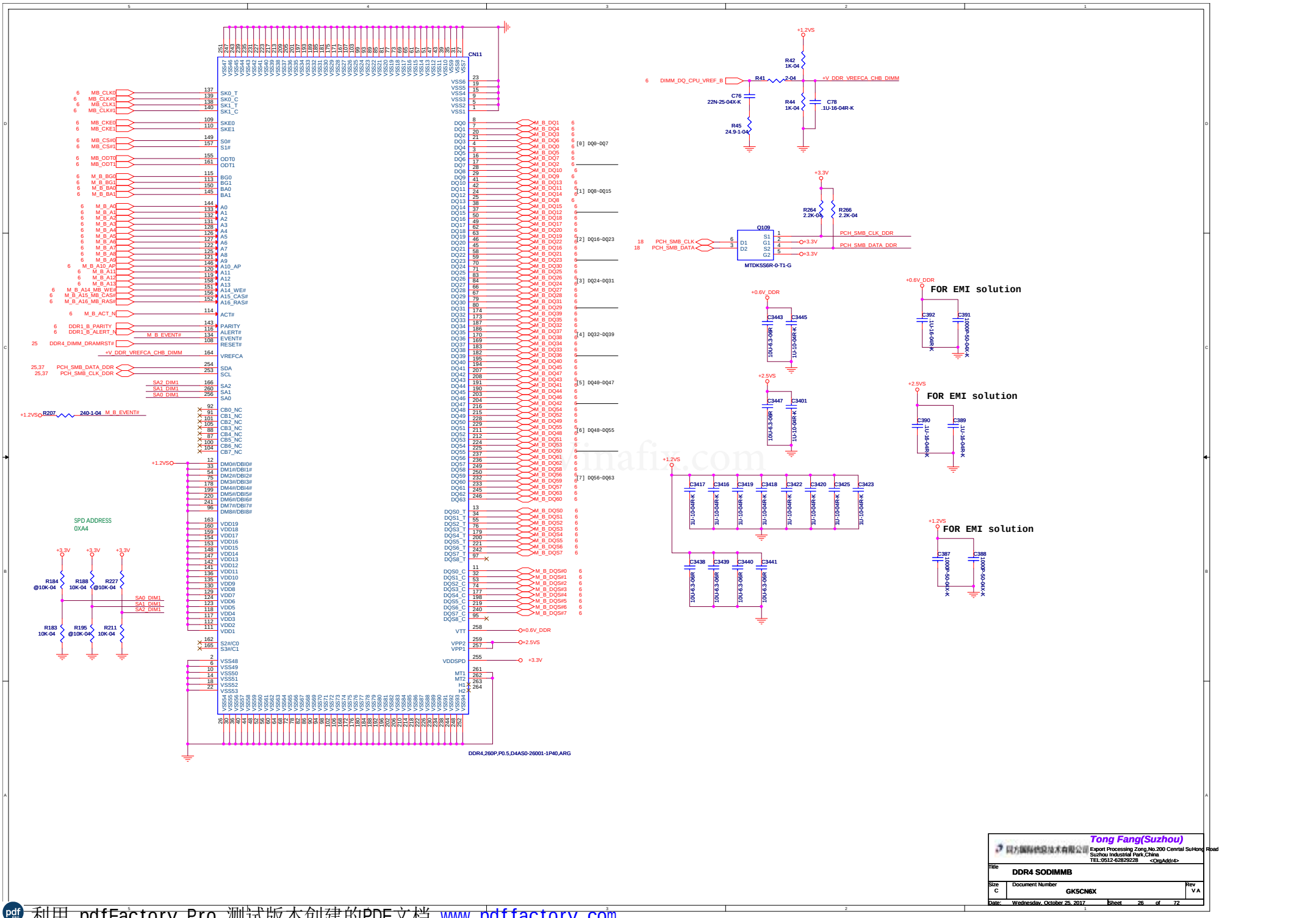
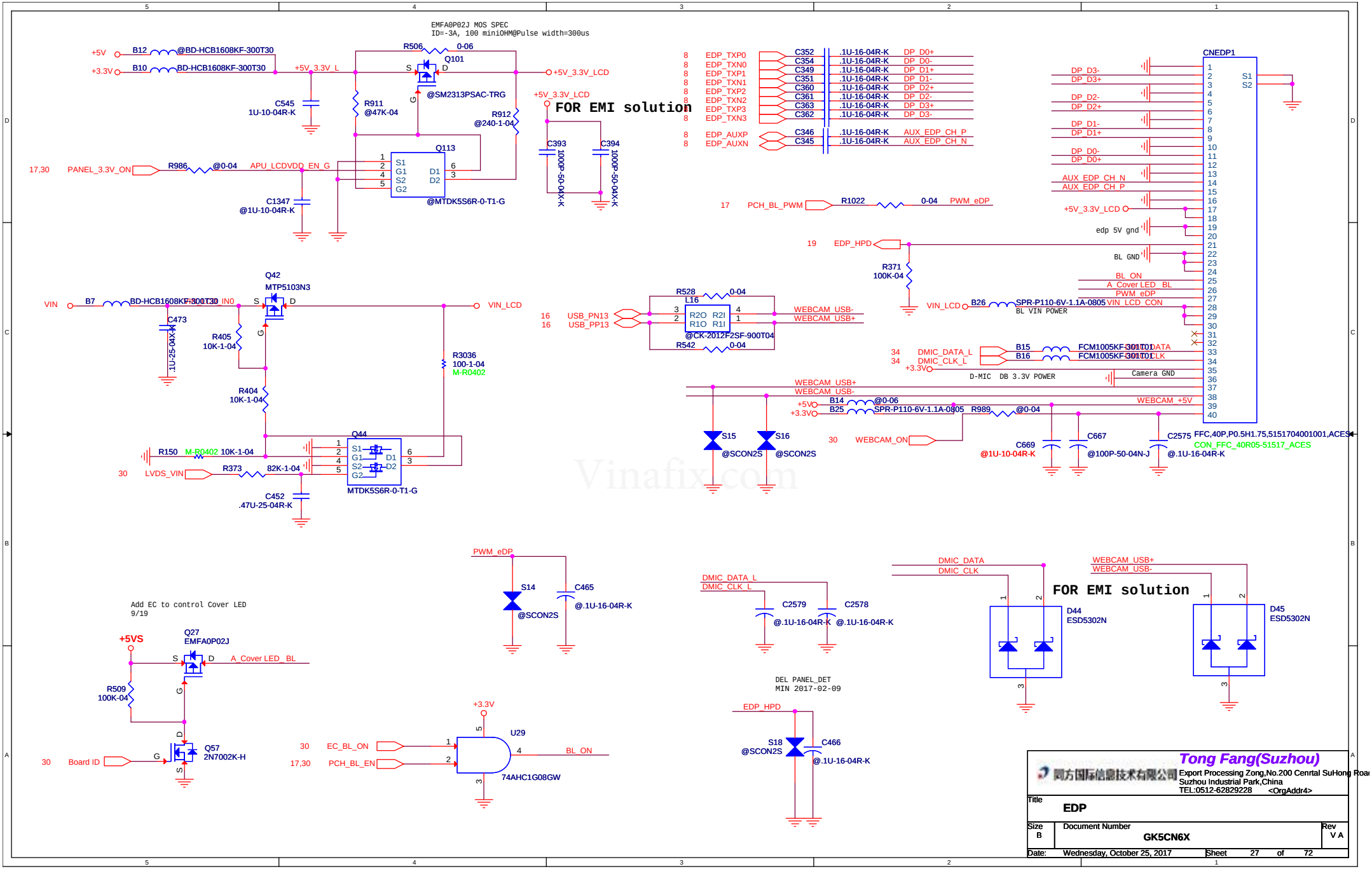


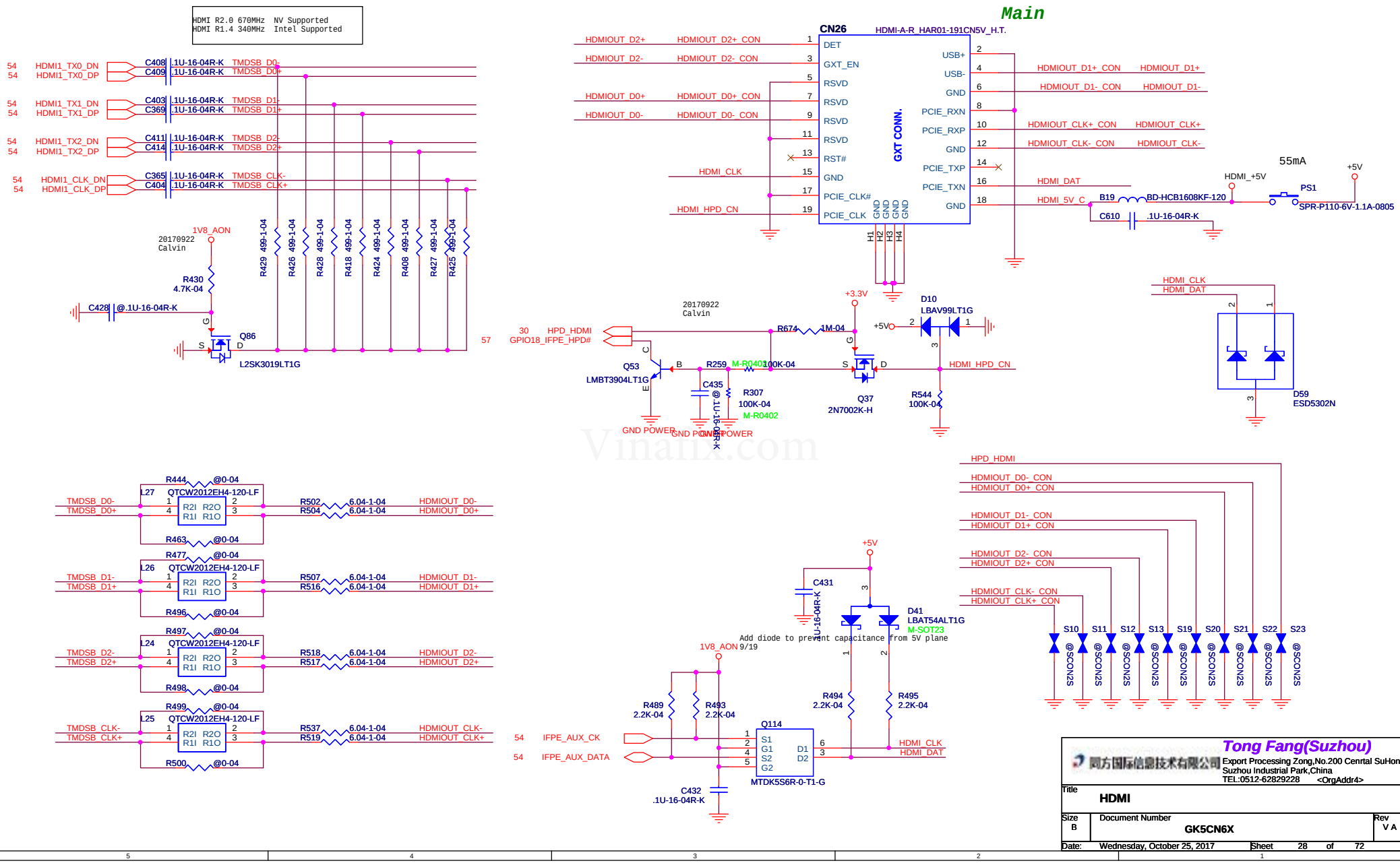




HDMI CONN

HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported



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Title: HDMI		
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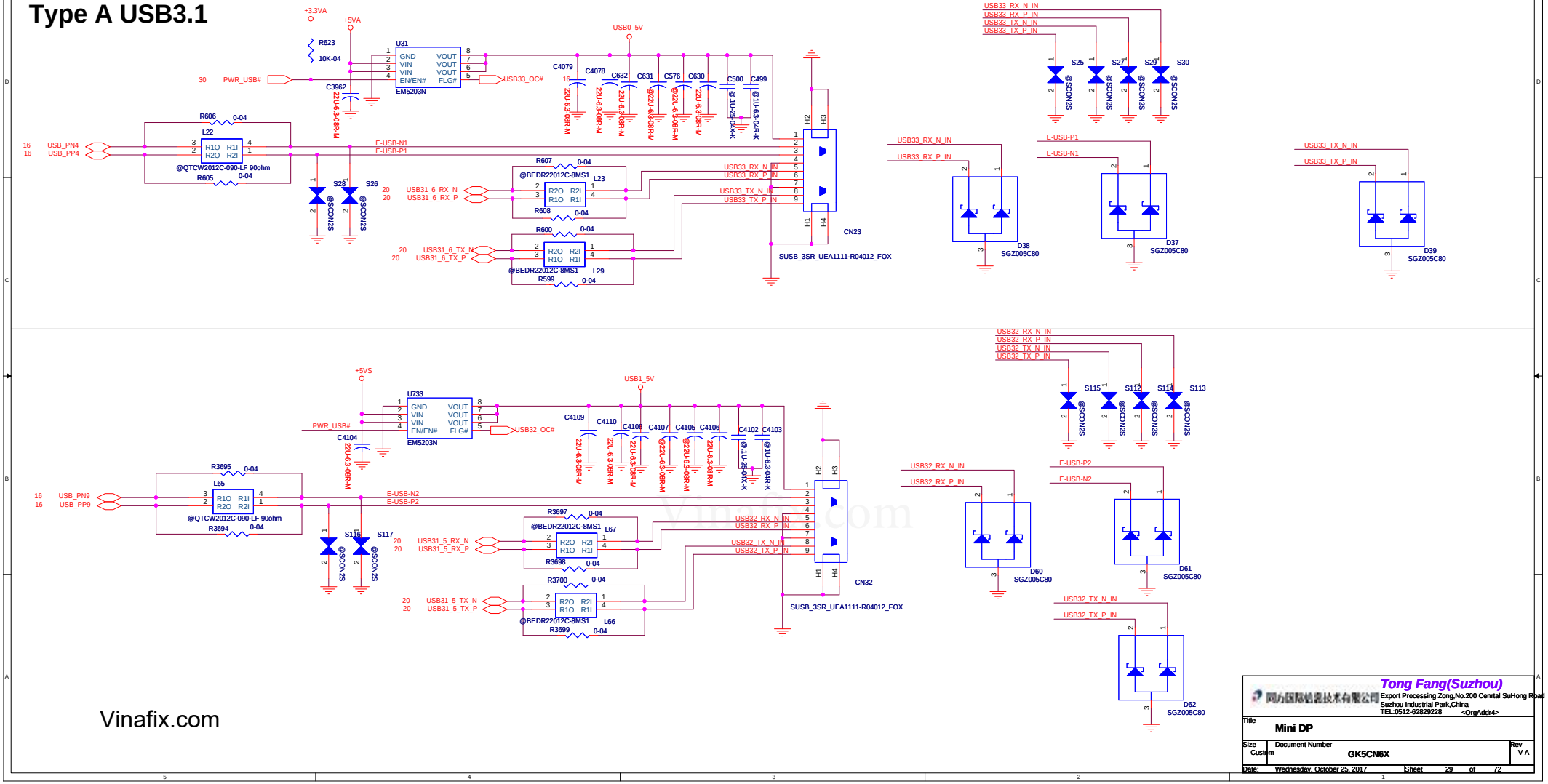
Type A USB3.1



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Title	Mini DP	
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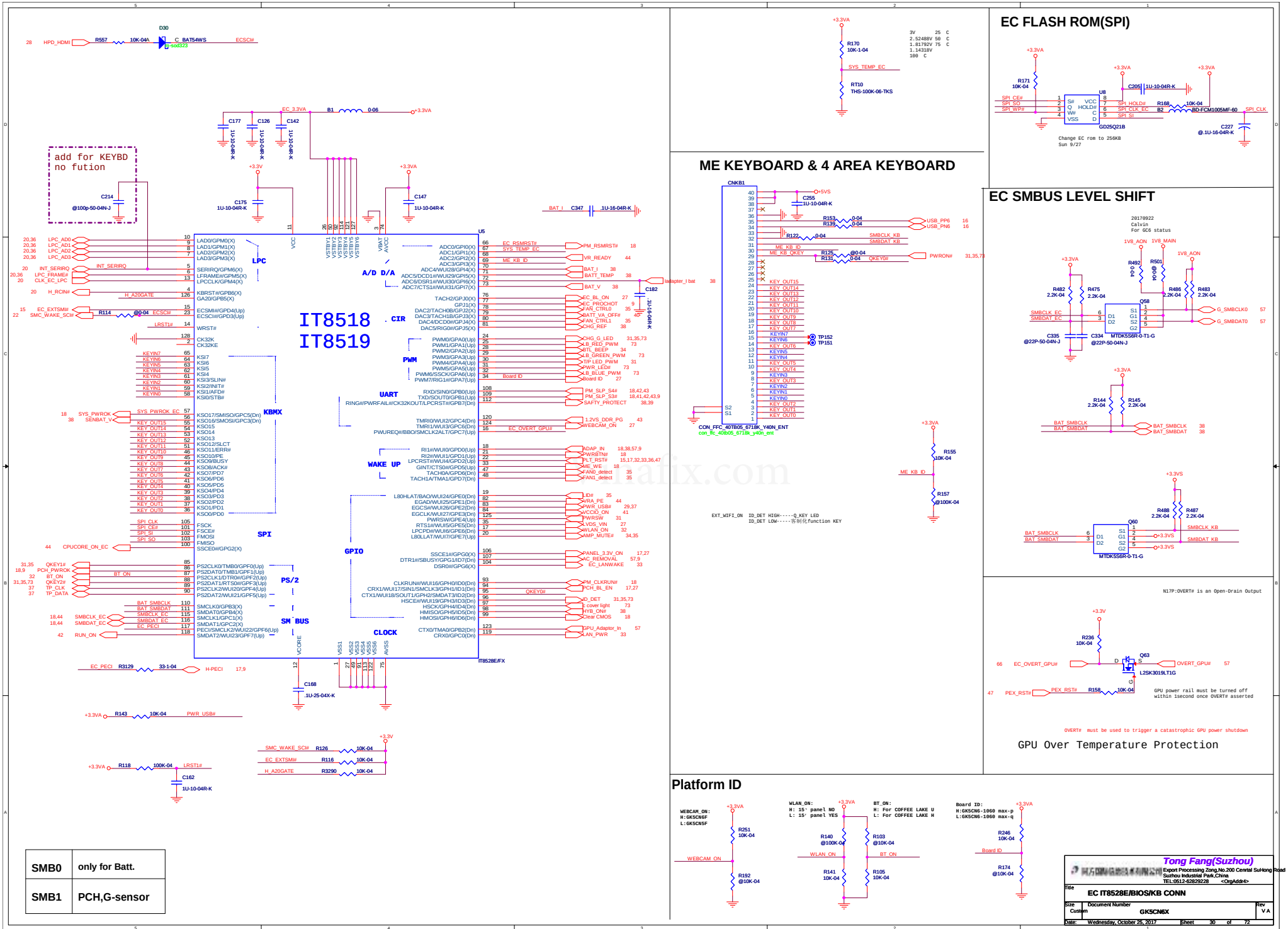
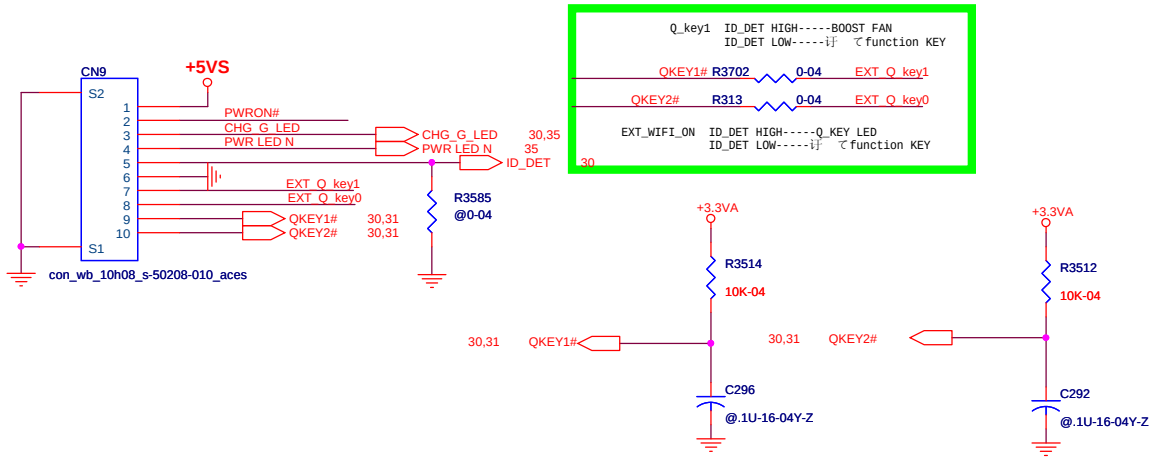
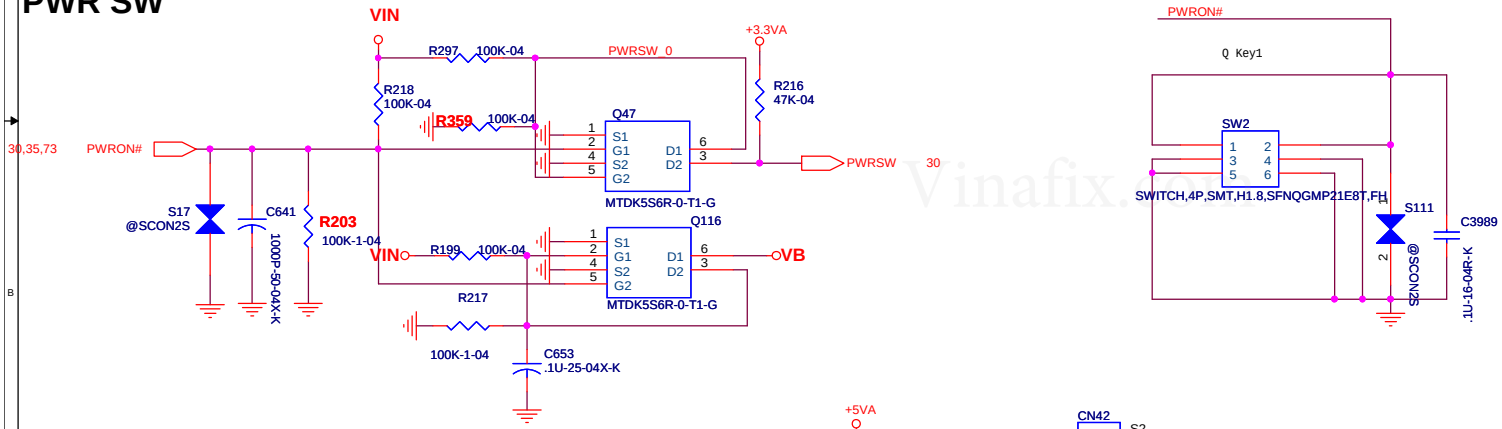


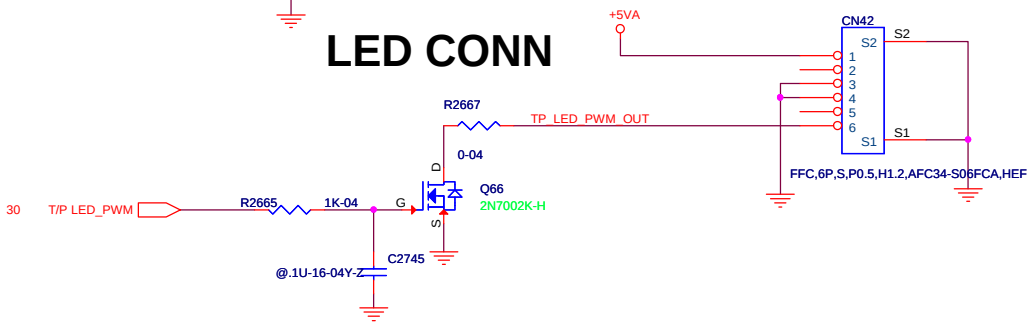
POWER DB CONN.



PWR SW



LED CONN



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Title	PSW/PWR DB CON	
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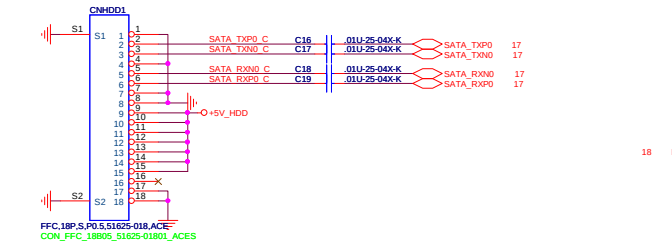
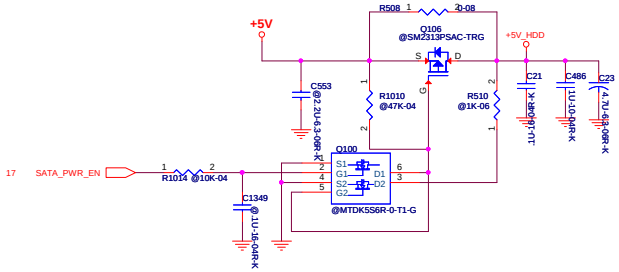
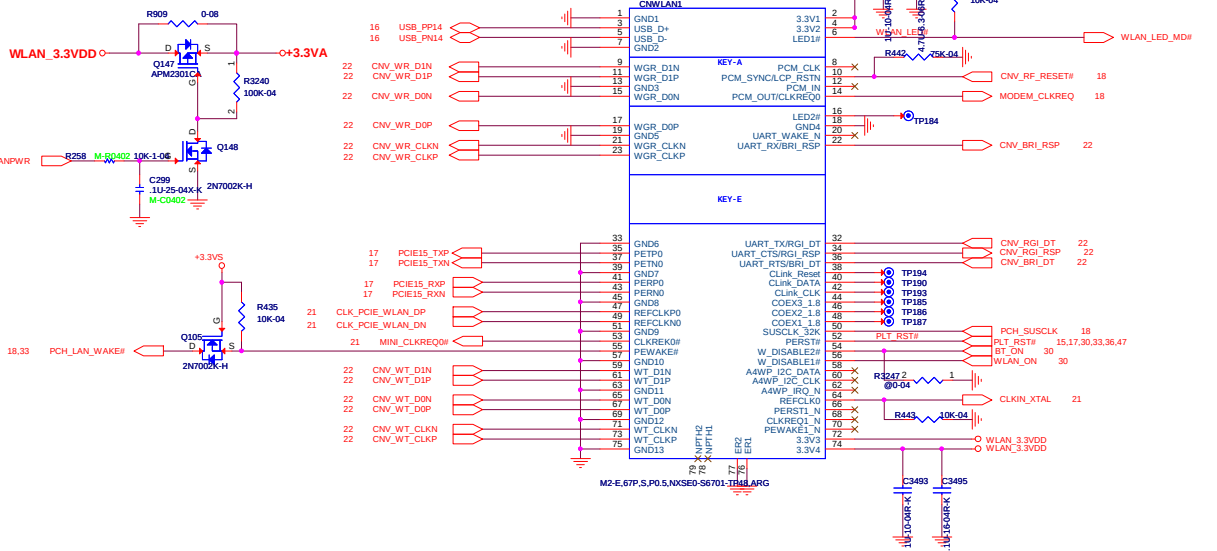
SATA-HDD



For KBL NVMe

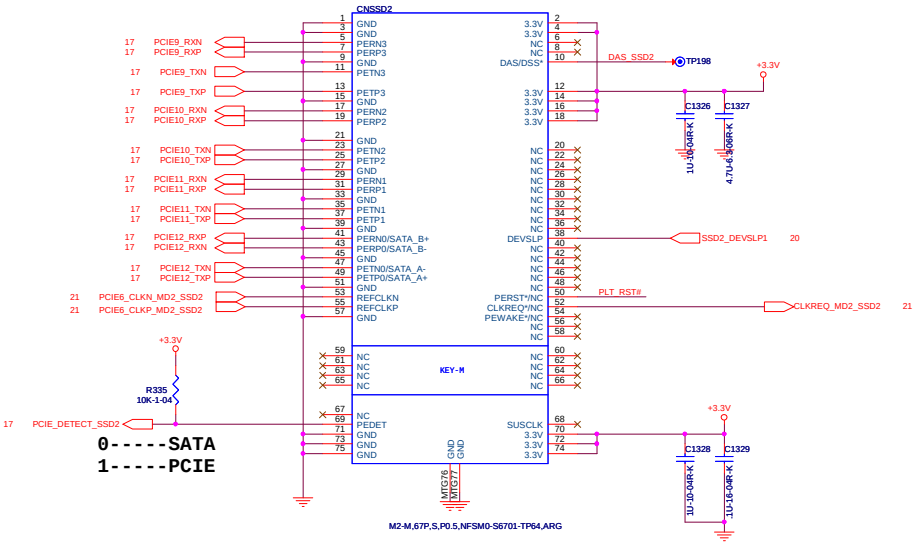


M.2 WIFI

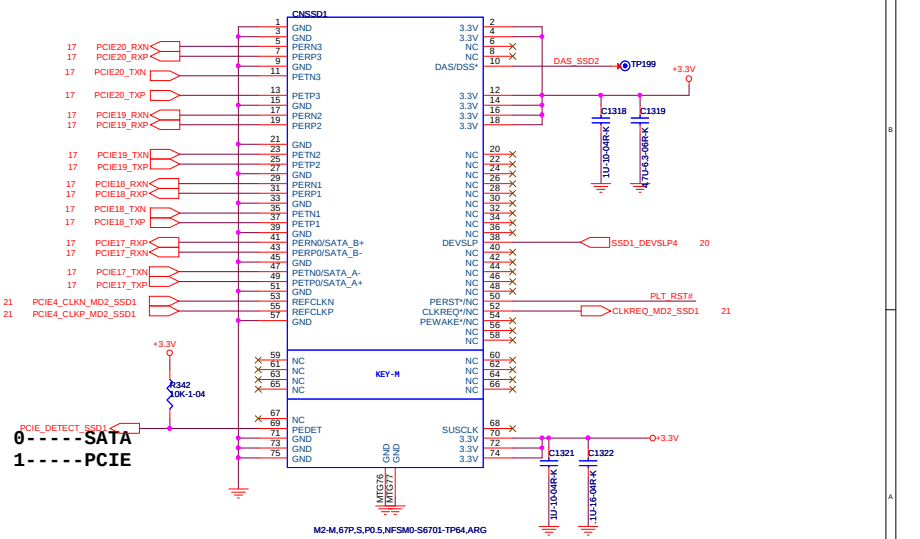


M.2 SSD

SSD2



SSD1



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Title	LAN RTL8111	
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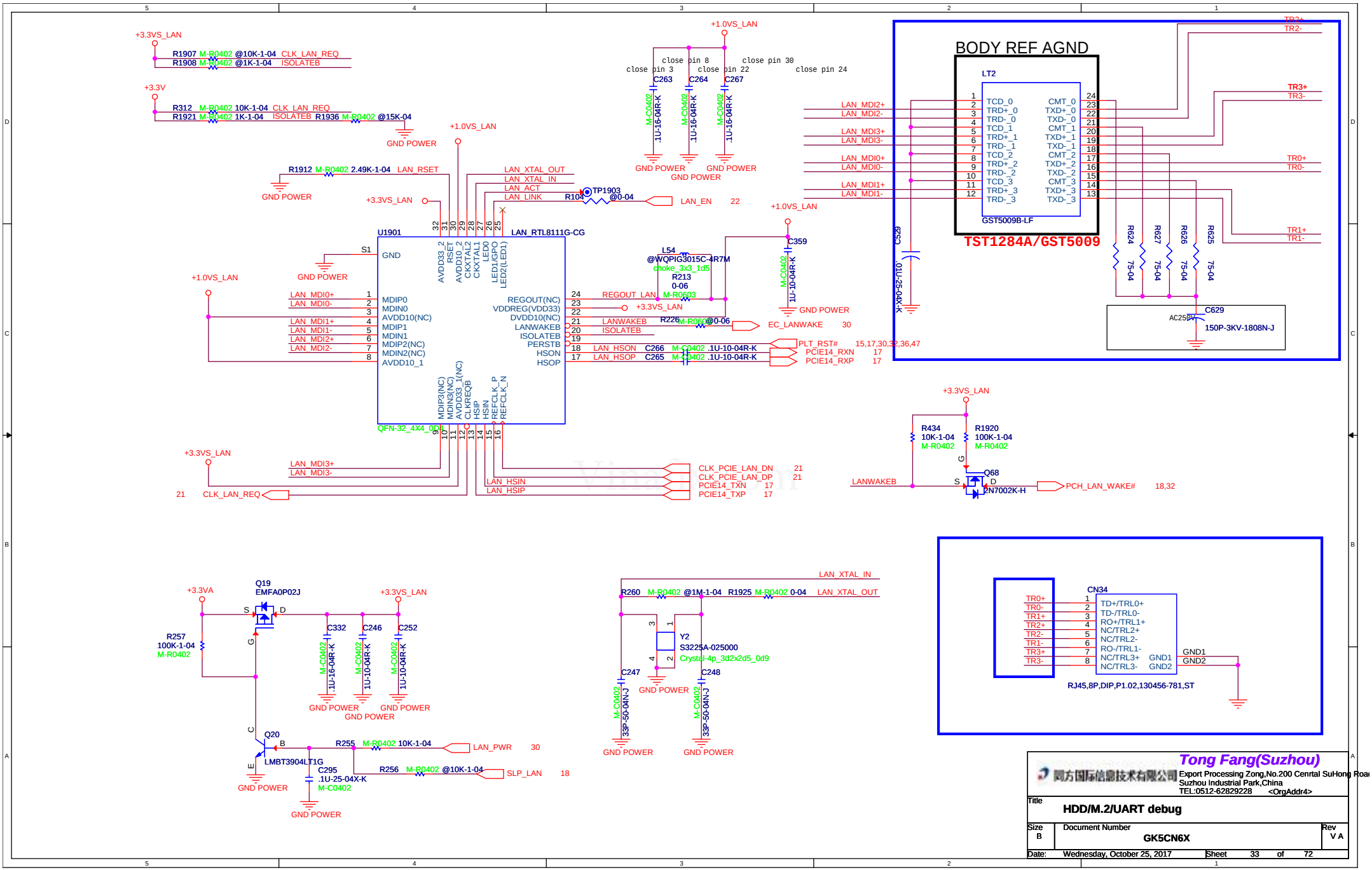
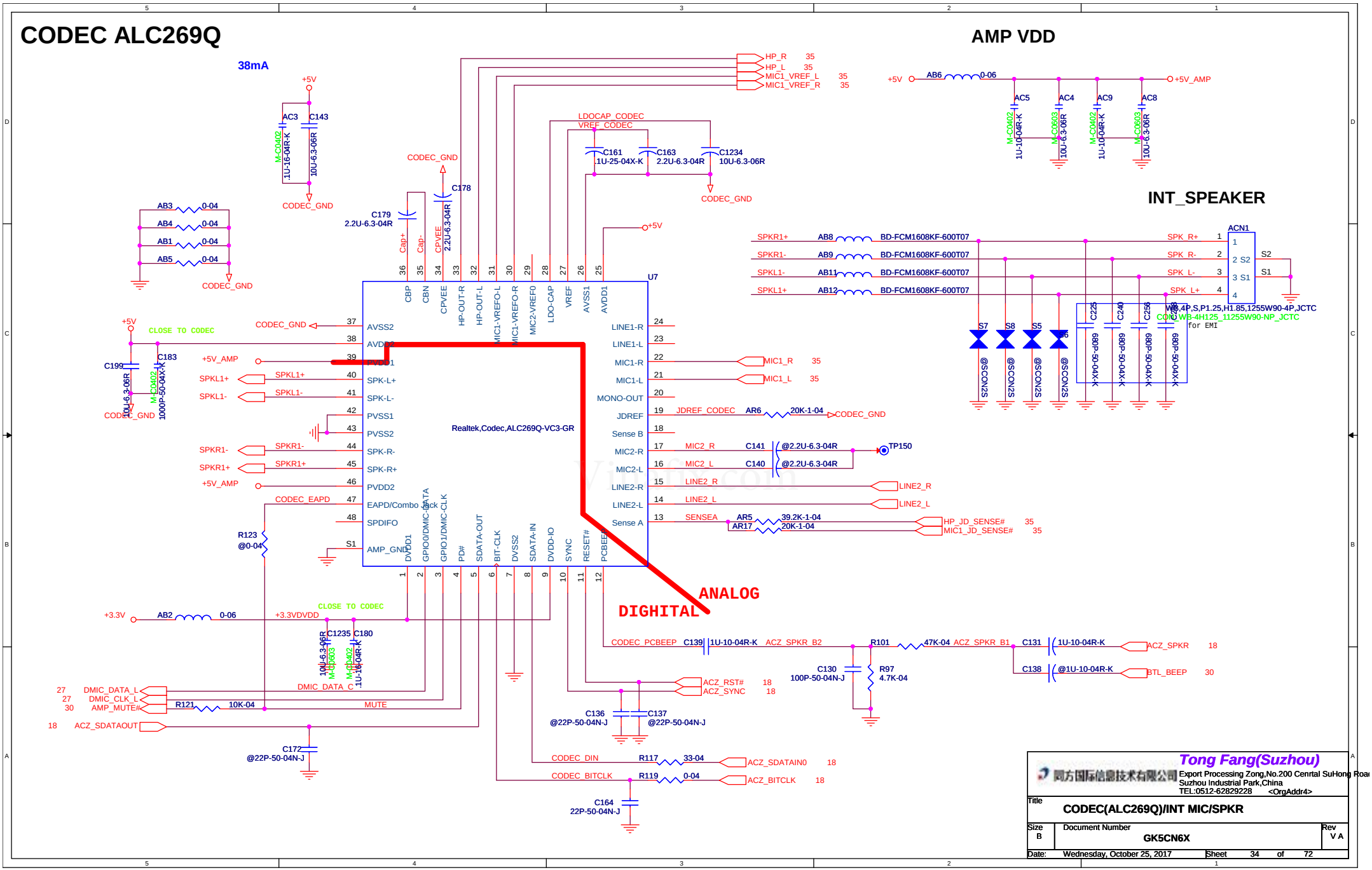
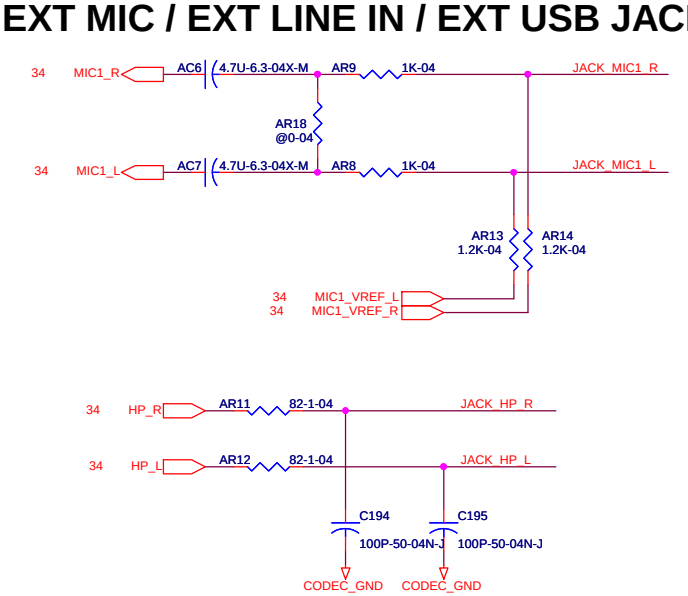
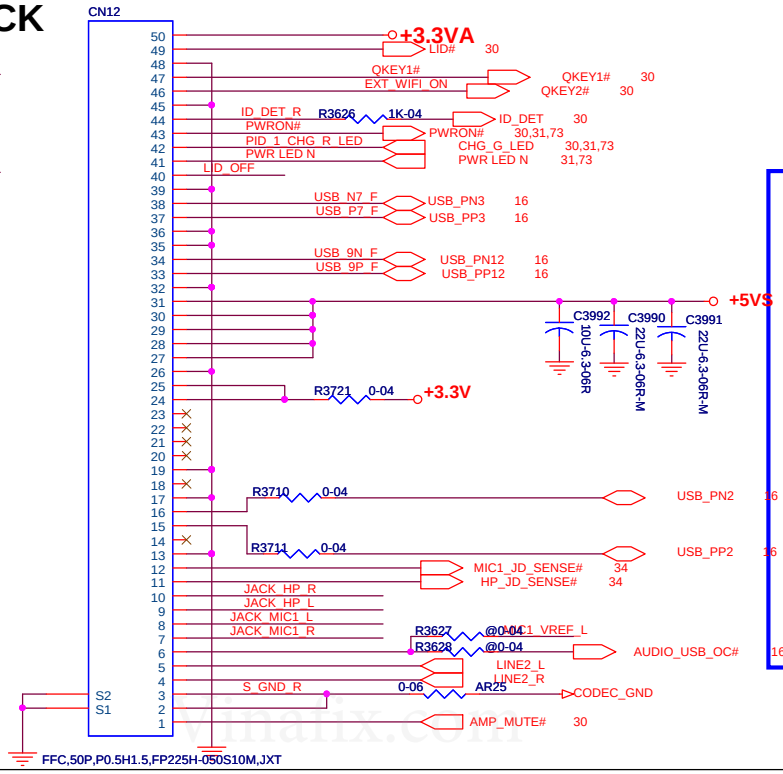
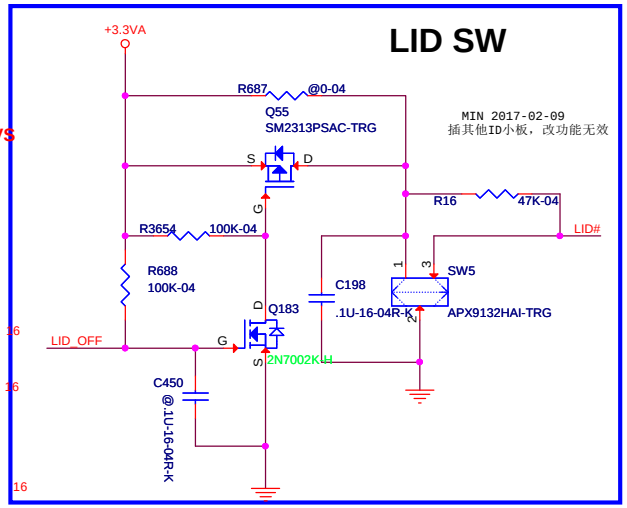




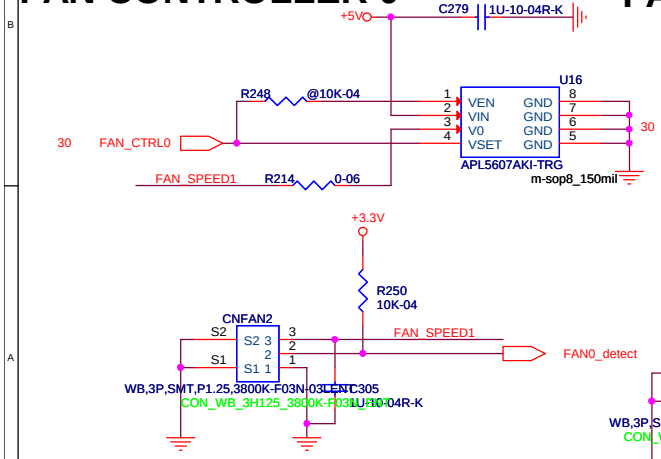
EXT MIC / EXT LINE IN / EXT USB JACK



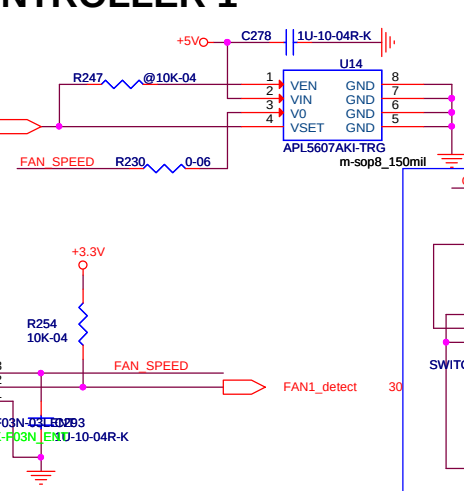


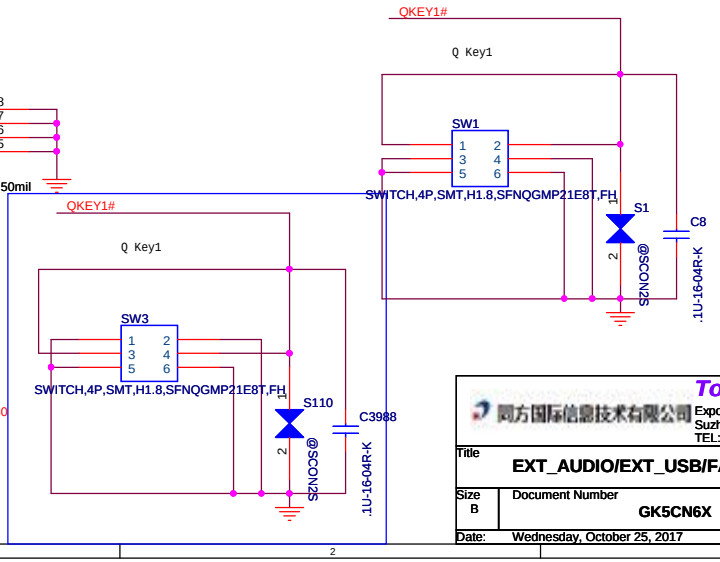


FAN CONTROLLER 0



FAN CONTROLLER 1





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Title	EXT_AUDIO/EXT_USB/FAN	
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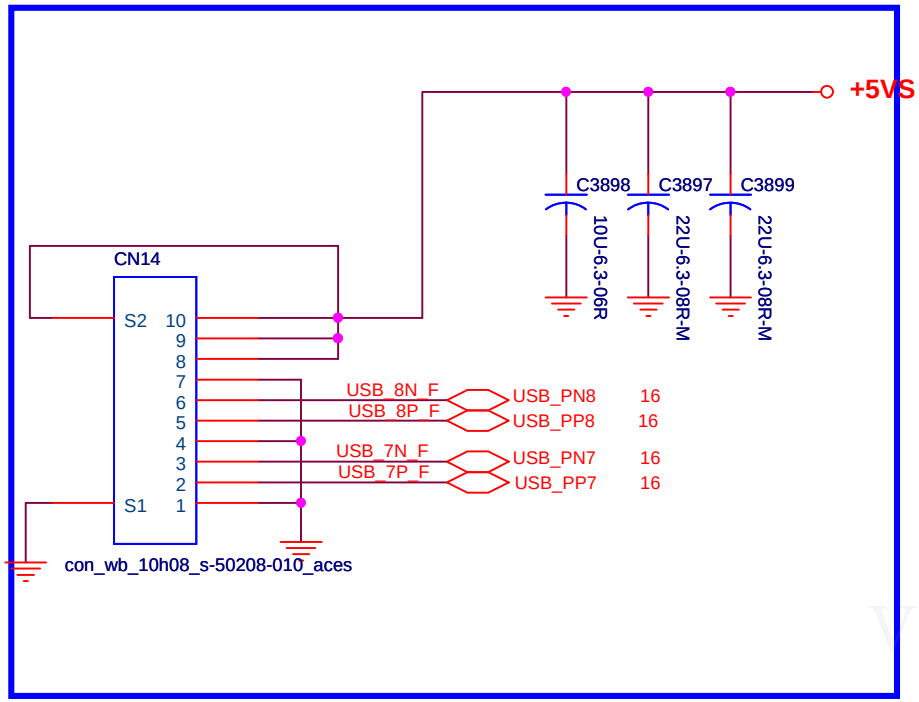
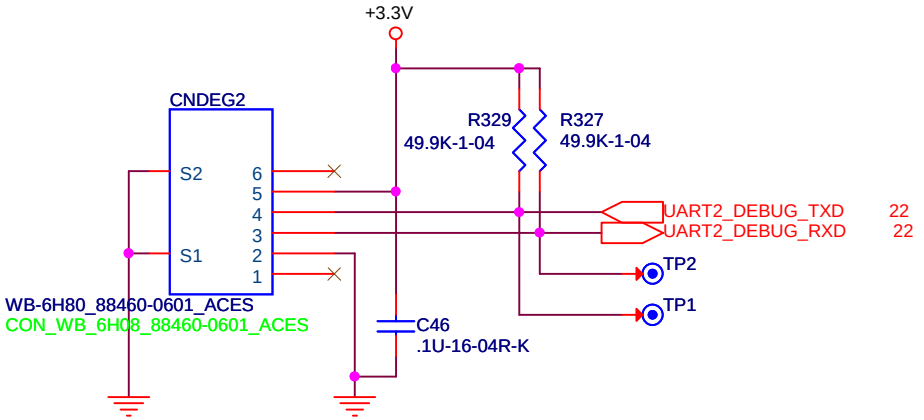
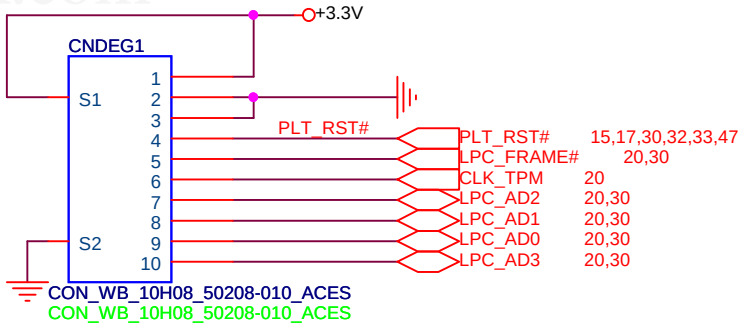
EXT USB2.0 DB



UART debug port



LPC debug port



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Title	EXT USB3.0	
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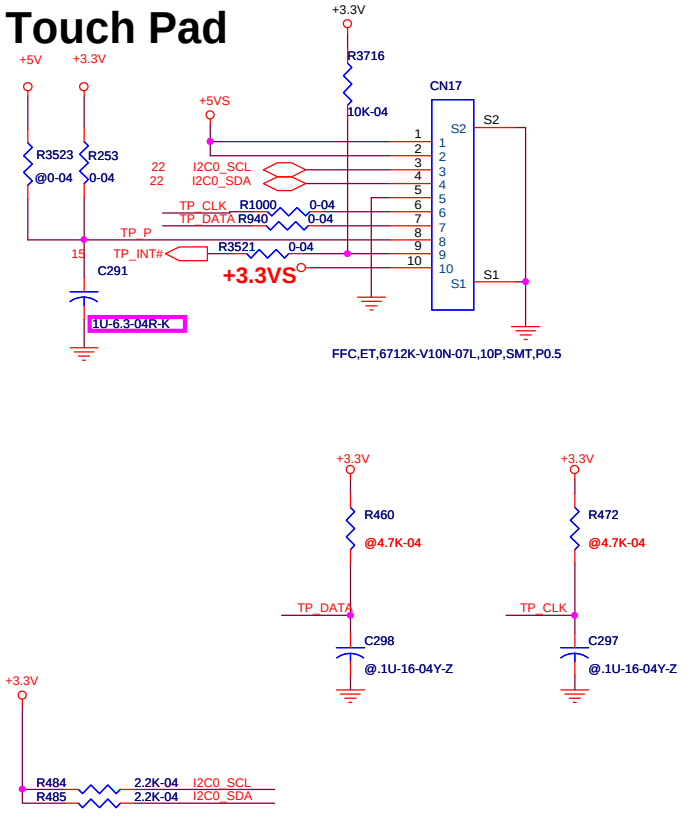
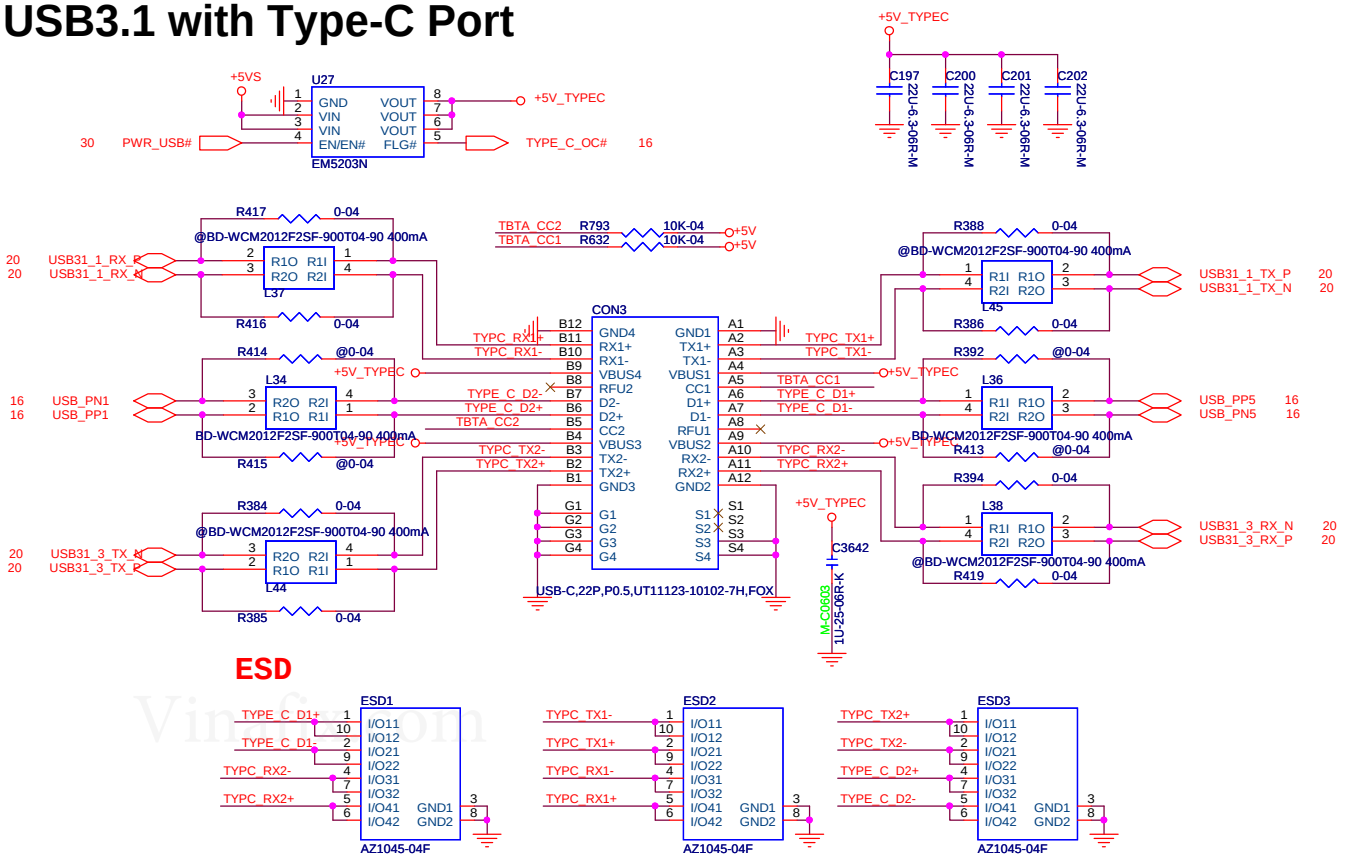
Touch Pad

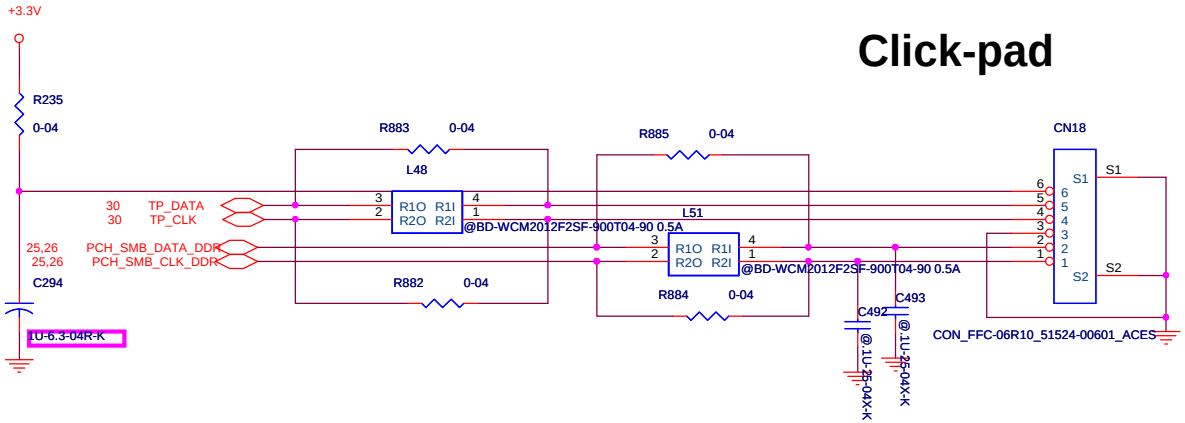


USB3.1 with Type-C Port



ESD

Click-pad



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Title: TP/USB/TYPEC		
Size: B	Document Number: GK5CN6X	Rev: V A
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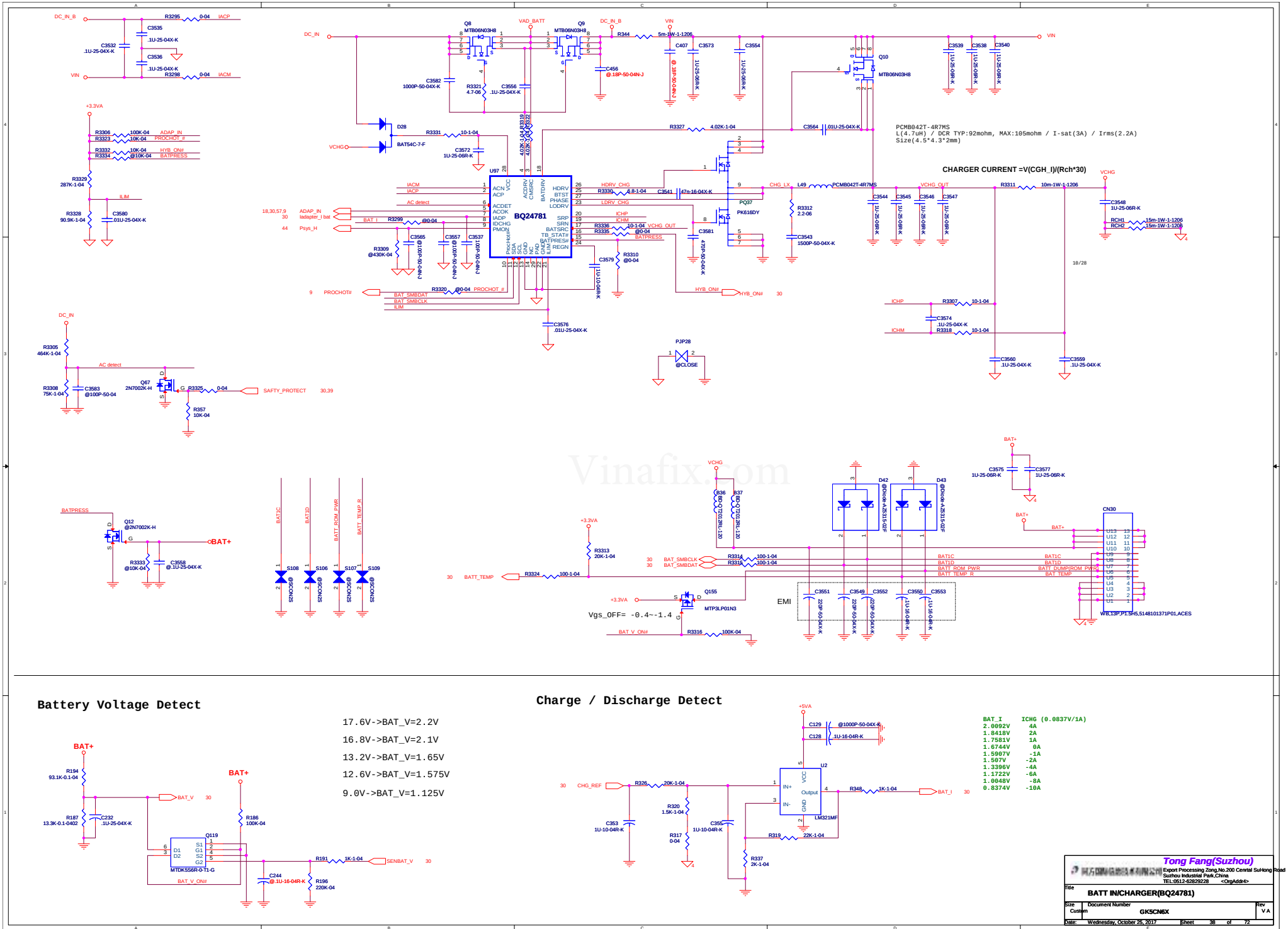
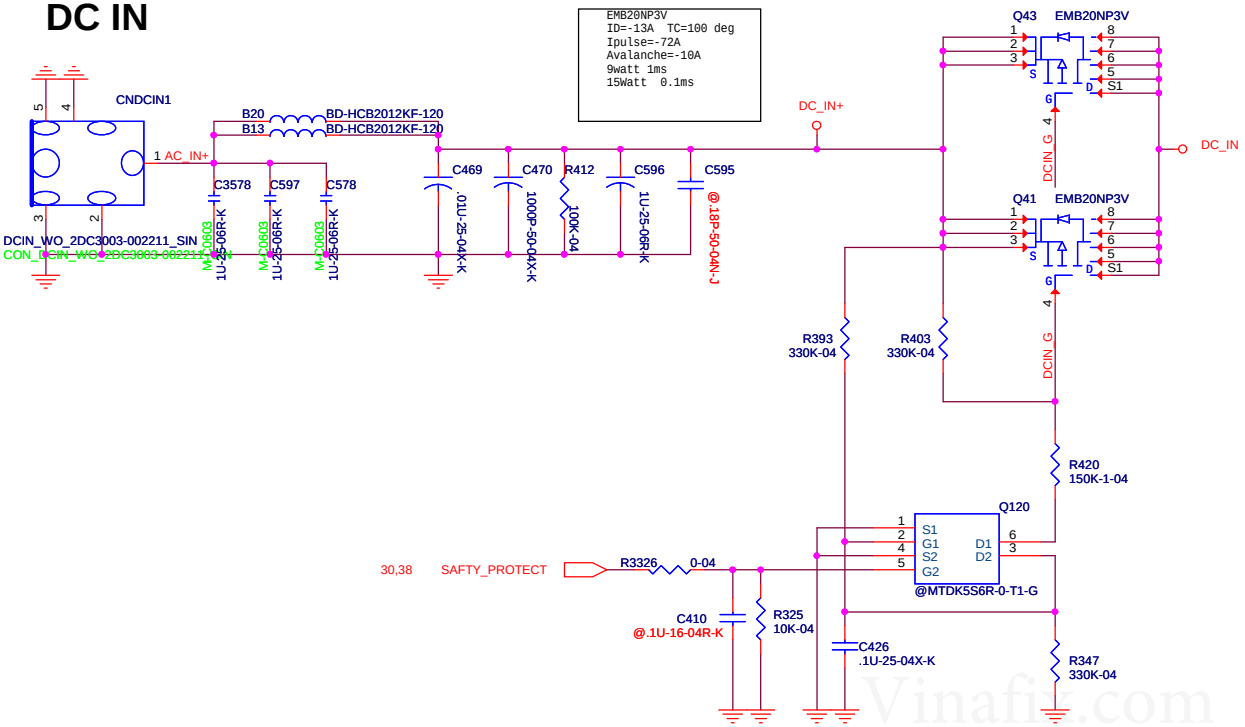
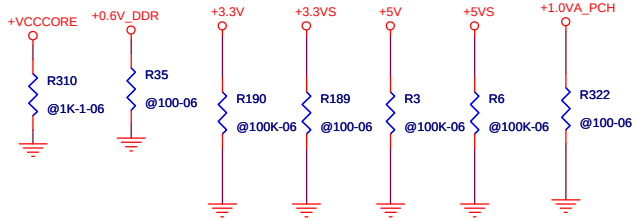


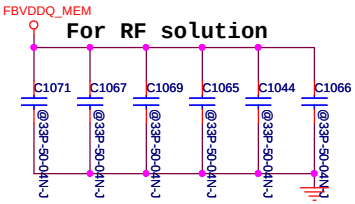
DC IN



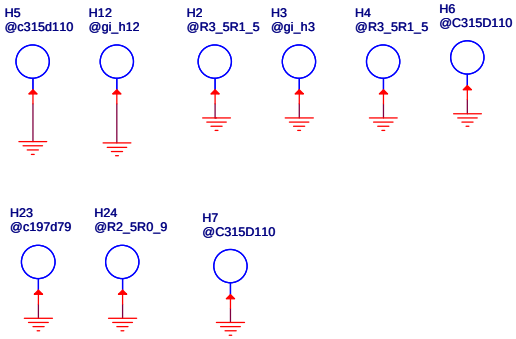
Discharge Resistor



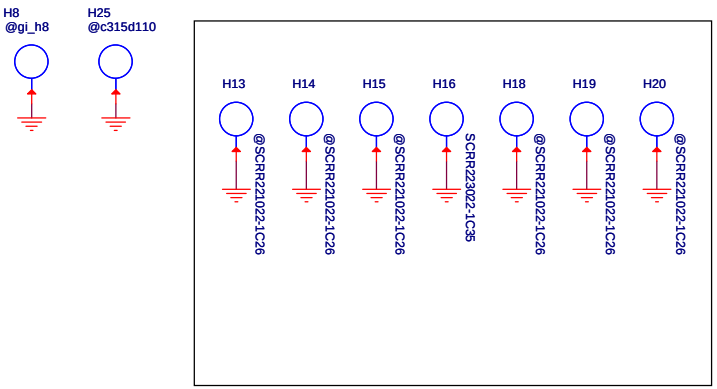
HIGH-SPEED CAP

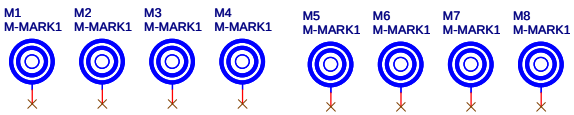


PCB HOLE



THERMAL HOLE





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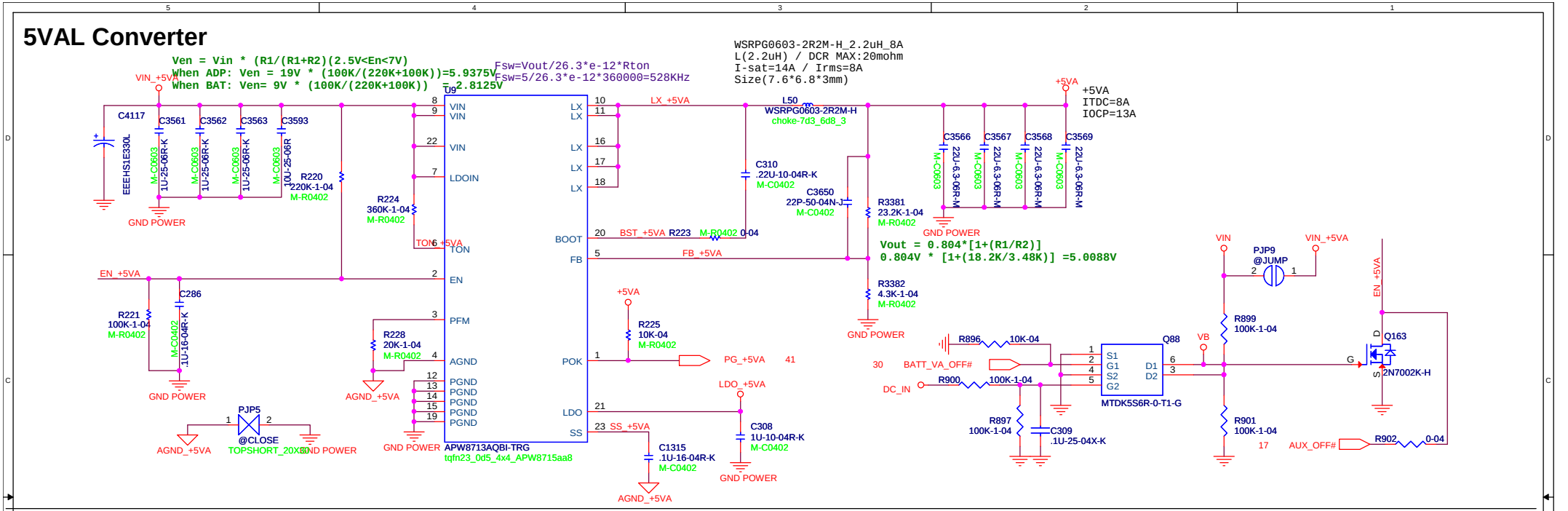
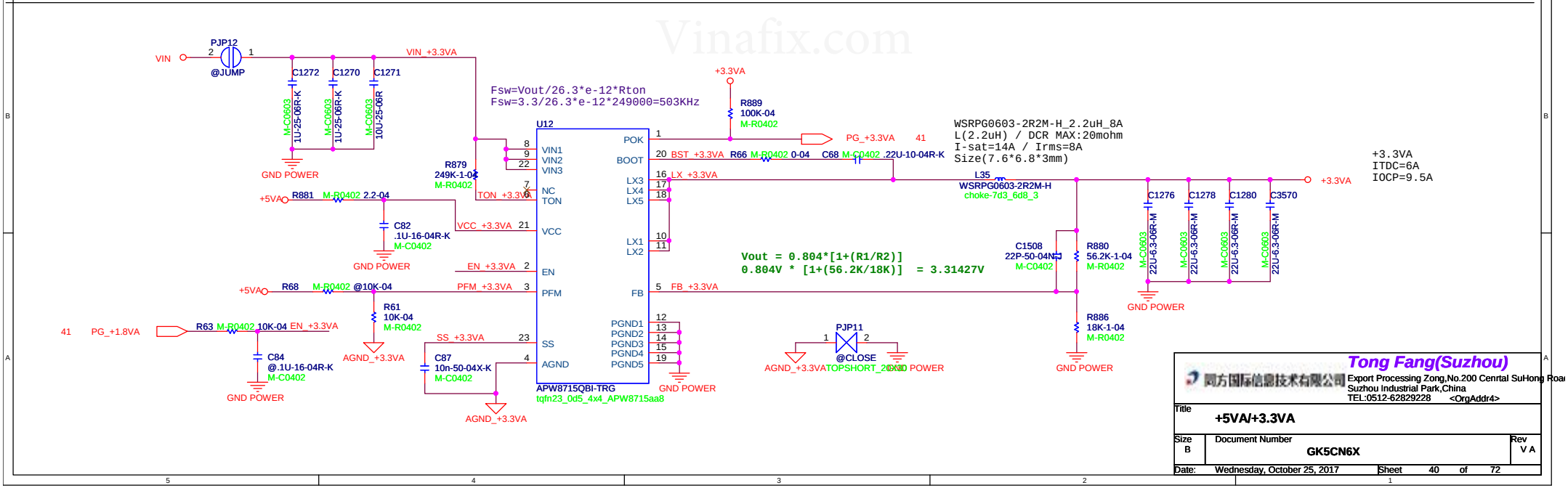
5VAL Converter





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Title	+5VA/+3.3VA	
Size B	Document Number GK5CN6X	Rev V A
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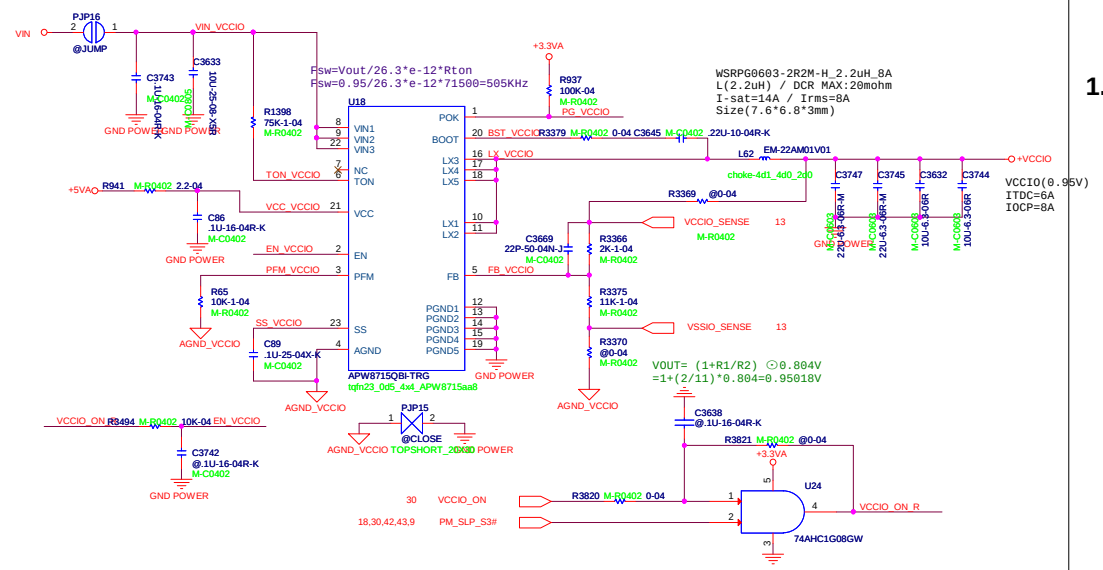
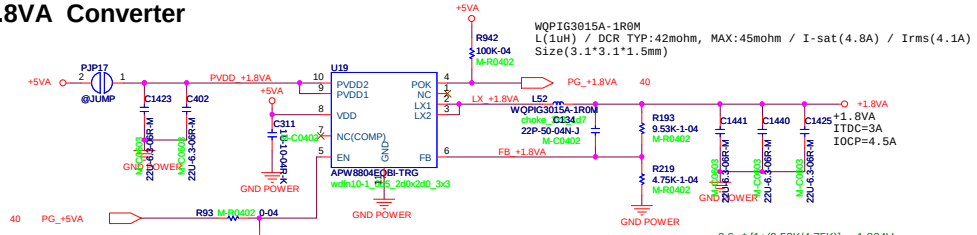
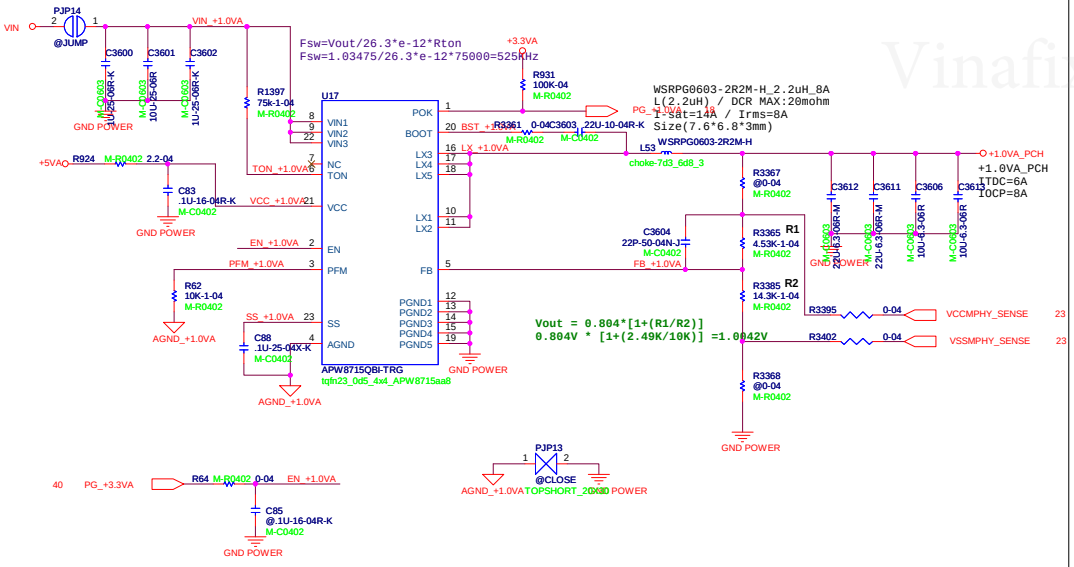
VCCIO Converter



1.8VA Converter



1.0VA Converter



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Title	+1.0VA_PCH/VCCIO/+1.8VA	
Size: Custom	Document Number: GK5CN6X	Rev: V A
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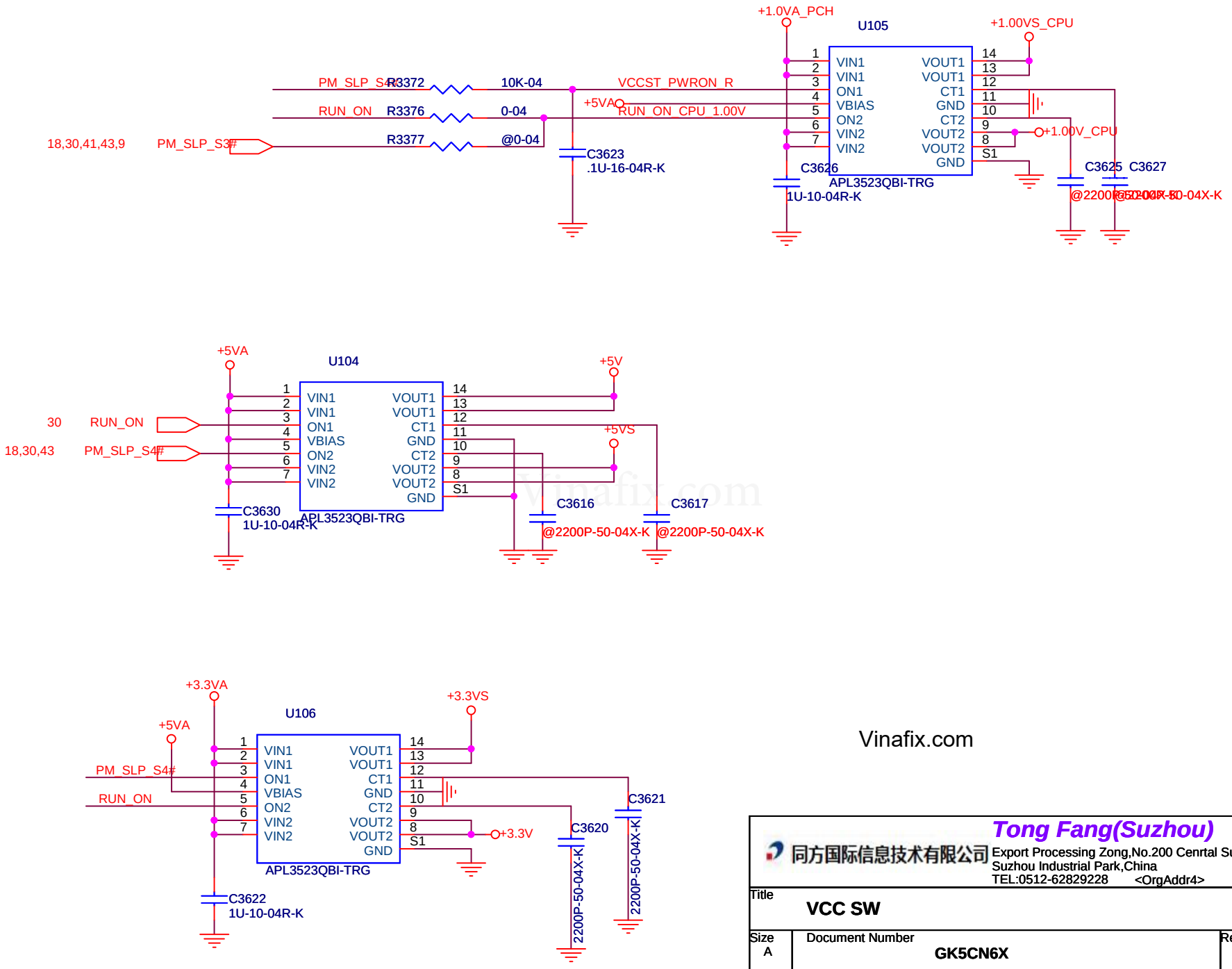

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Title	VCC SW	
Size A	Document Number GK5CN6X	Rev V A
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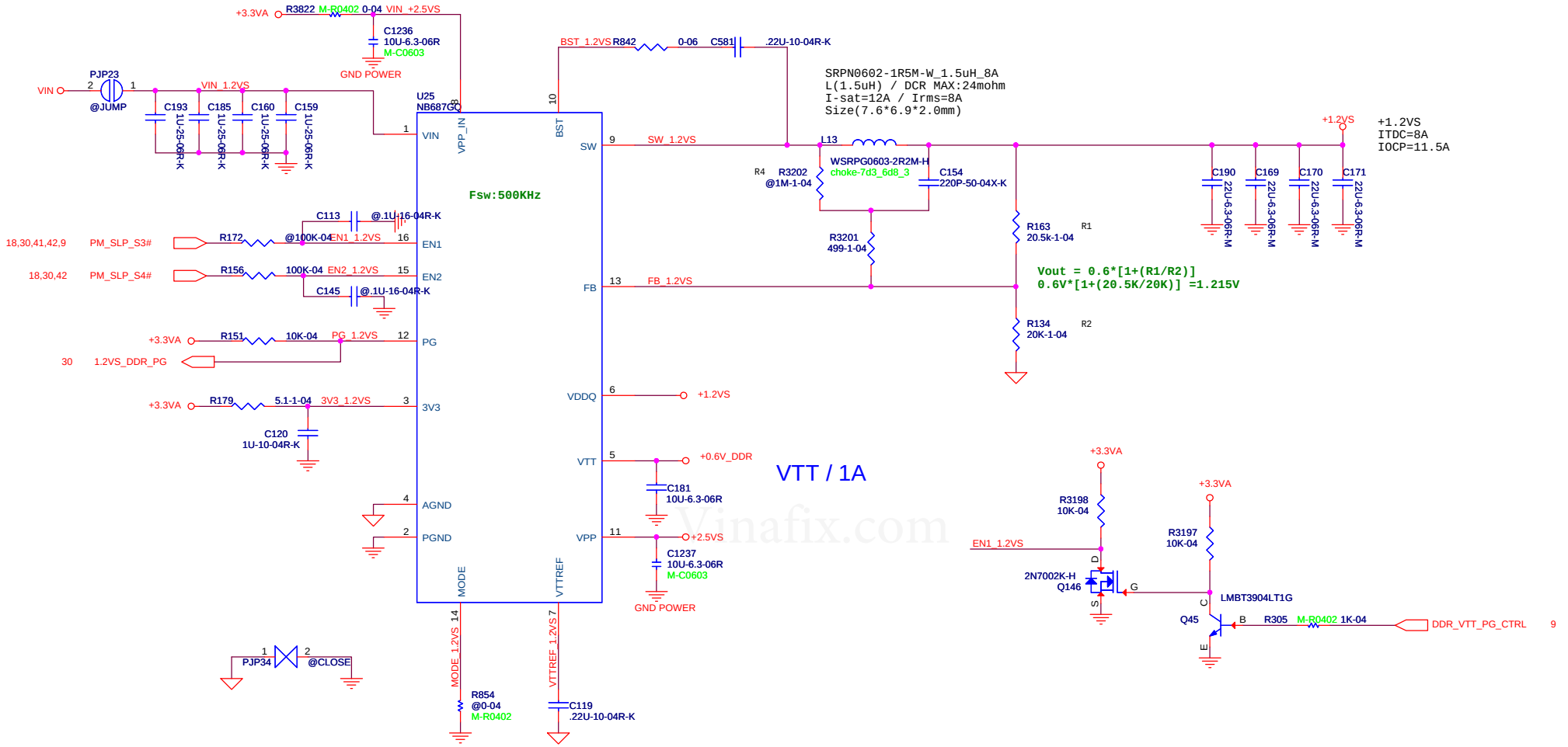
1.2VS/VTT/2.5VS



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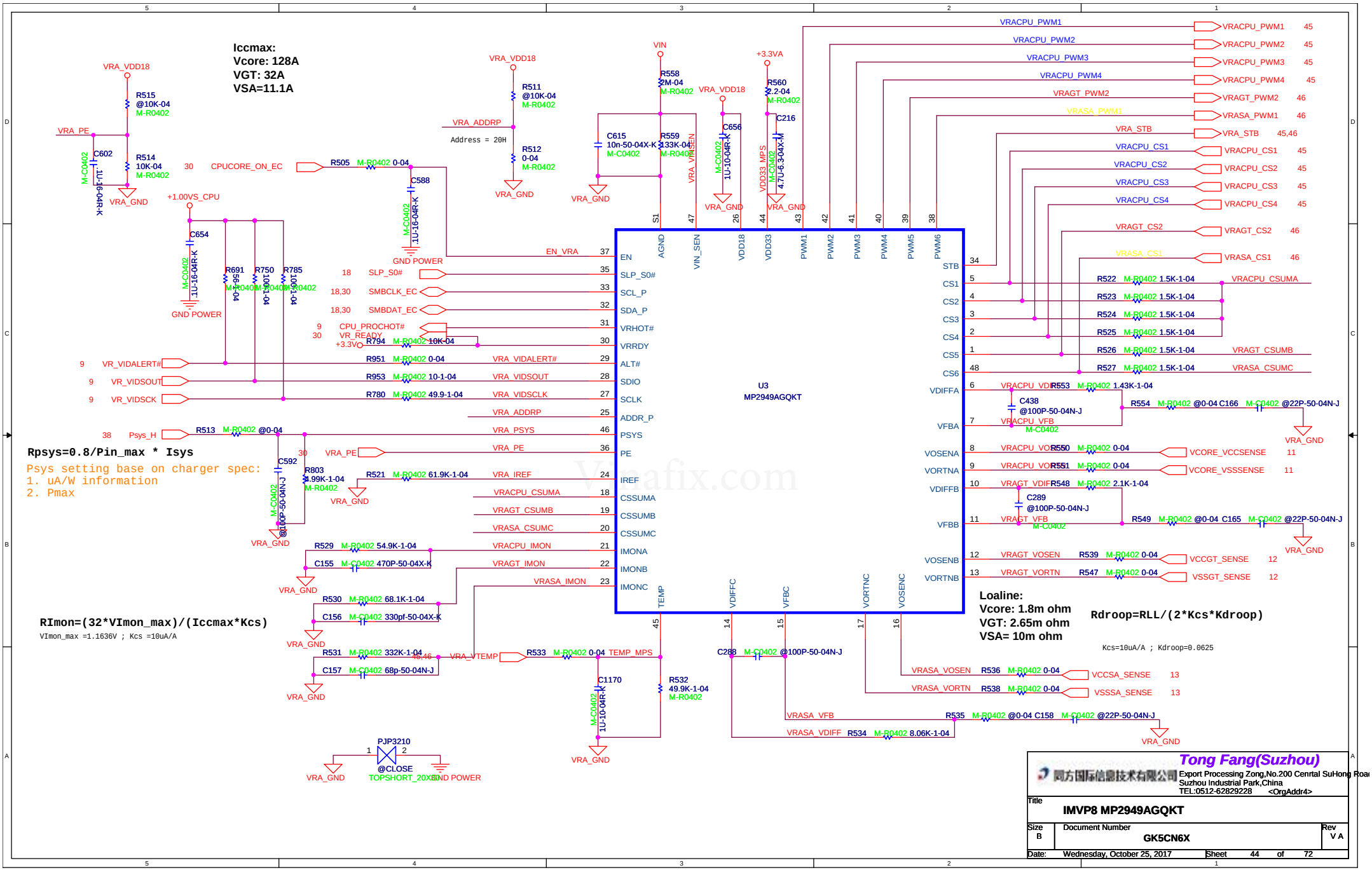
TEL:0512-62829228 <OrgAddr4>	
Title	+1.2VS/+2.5VS
Size B	Document Number GK5CN6X
Rev V A	
Date: Wednesday, October 25, 2017	Sheet 43 of 72



VCCCORE

VCORE:0.55~1.52V Vboot:0V
Core: Iccmax=68A
Core: TDC=50A
FSW:600KHz
di(IccMax transient):58A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:00h
LL:1.8m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A

WSRG0603A-R22M-AG
(@2-1-06)
L(0.22uH) / DCR TYP:2.5mohm, MAX:2.75mohm / I-sat(40A) / Irms(23A)
Size(7.6*6.8*3mm)

FOR EMI solution

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Title: VCORE
Size: B
Document Number: GK5CN6X
Rev: V A
Date: Wednesday, October 25, 2017
Sheet 45 of 72

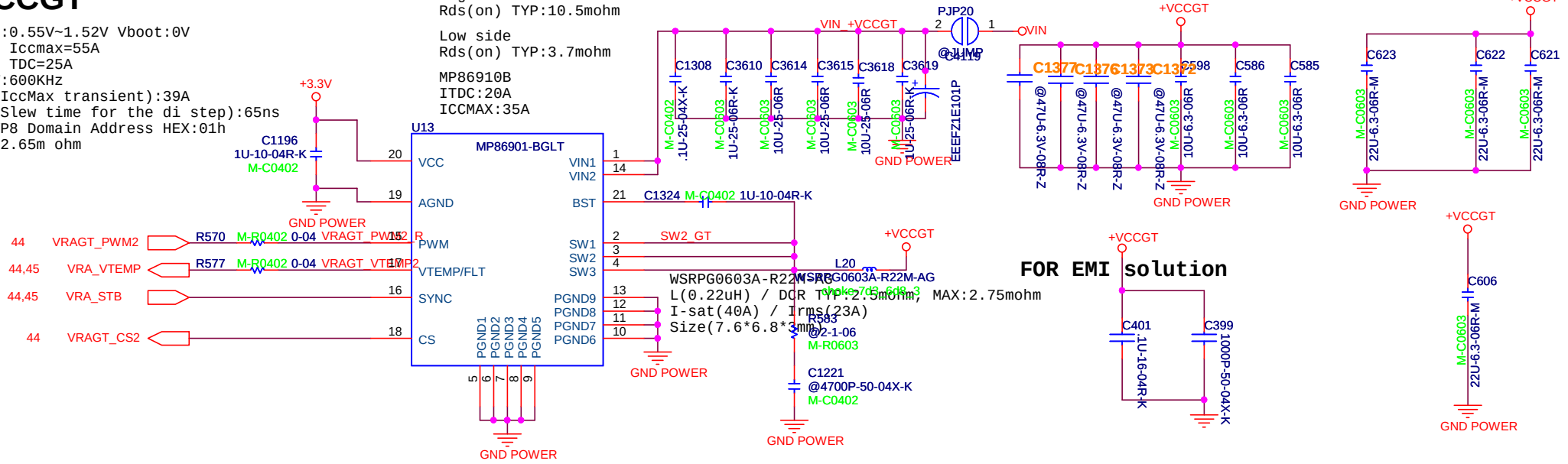
VCCGT

VGT:0.55V~1.52V Vboot:0V
GT: Iccmax=55A
GT: TDC=25A
FSW:600KHz
di(IccMax transient):39A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:01h
LL:2.65m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



WSRPG0603A-R22M-AG
L(0.22uH) / DCR TYP:2.5mohm, MAX:2.75mohm
I-sat(40A) / Irms(23A)
Size(7.6*6.8*3mm)

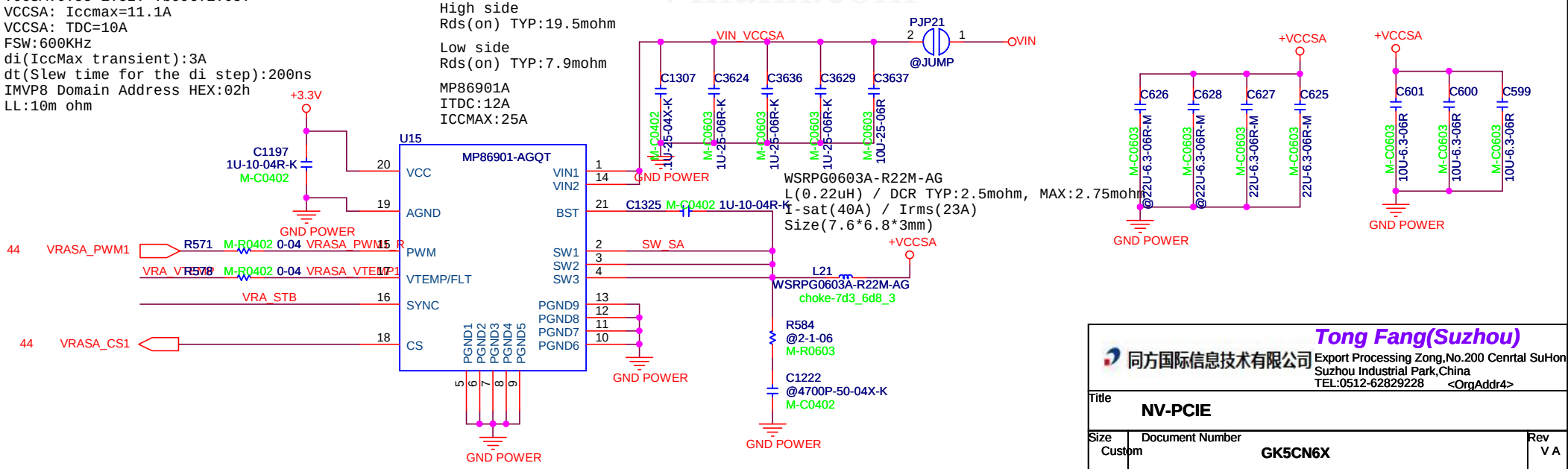
VCCSA

VCCSA:0.55~1.52V Vboot:1.05V
VCCSA: Iccmax=11.1A
VCCSA: TDC=10A
FSW:600KHz
di(IccMax transient):3A
dt(Slew time for the di step):200ns
IMVP8 Domain Address HEX:02h
LL:10m ohm

High side
Rds(on) TYP:19.5mohm

Low side
Rds(on) TYP:7.9mohm

MP86901A
ITDC:12A
ICCMAX:25A



WSRPG0603A-R22M-AG
L(0.22uH) / DCR TYP:2.5mohm, MAX:2.75mohm
I-sat(40A) / Irms(23A)
Size(7.6*6.8*3mm)

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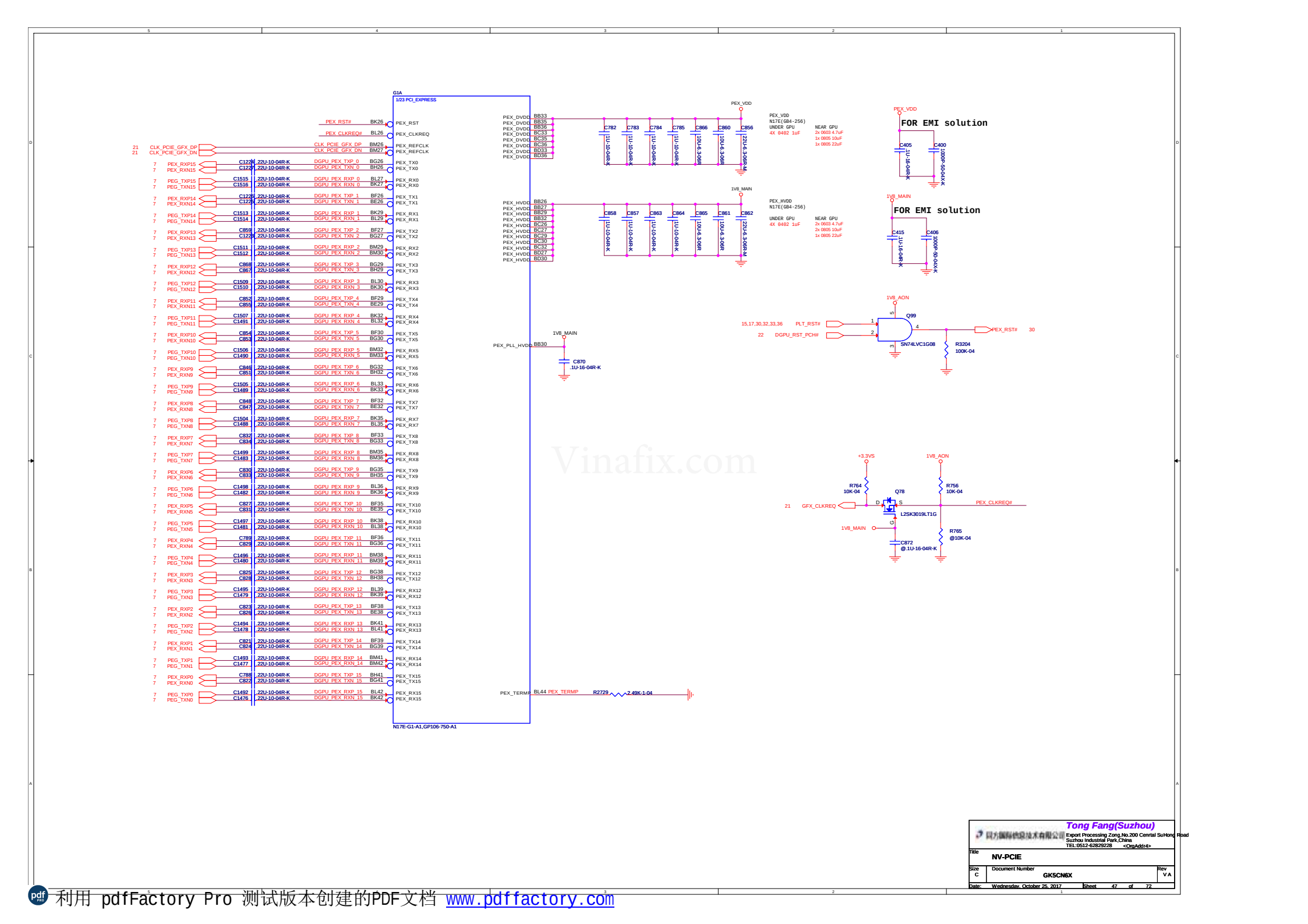
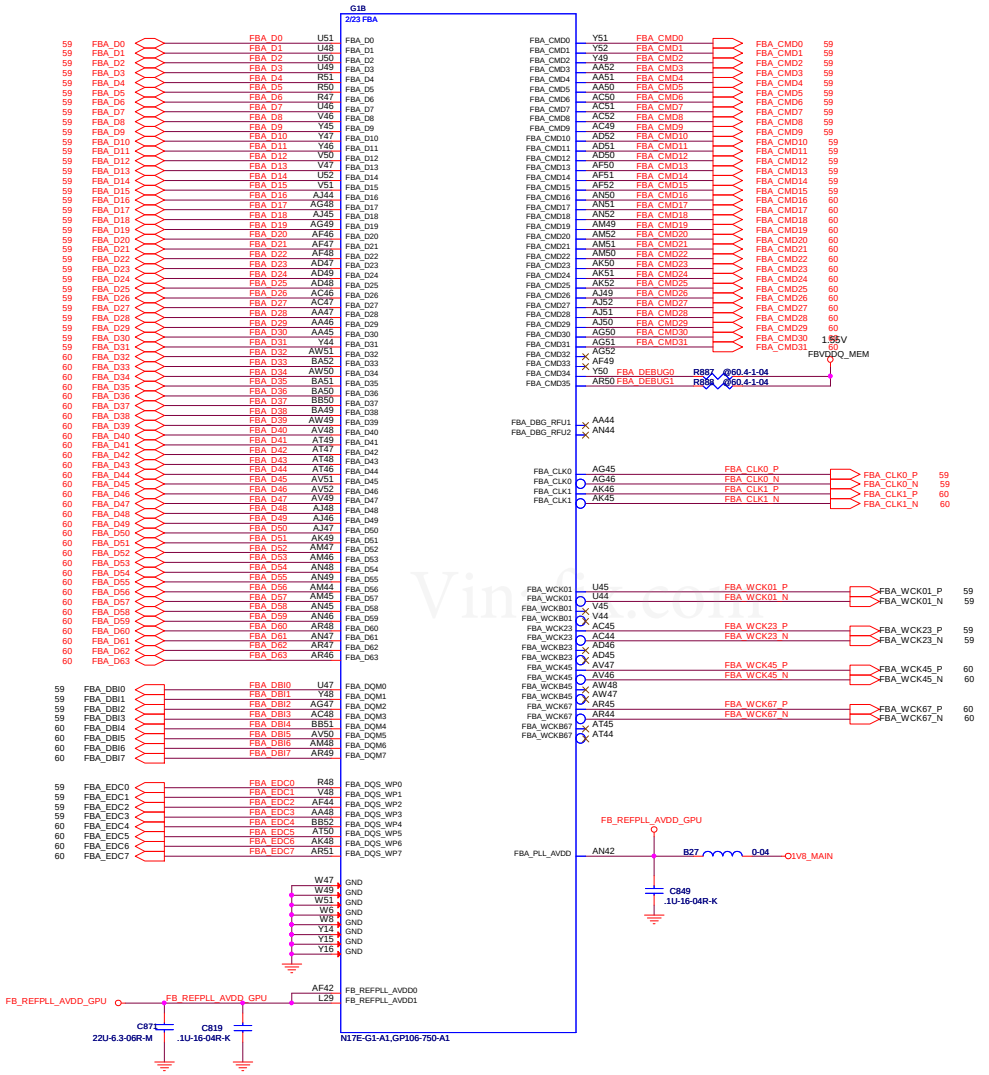
Title: NV-PCIE		
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Wednesday, October 25, 2017	Sheet 46 of 72	





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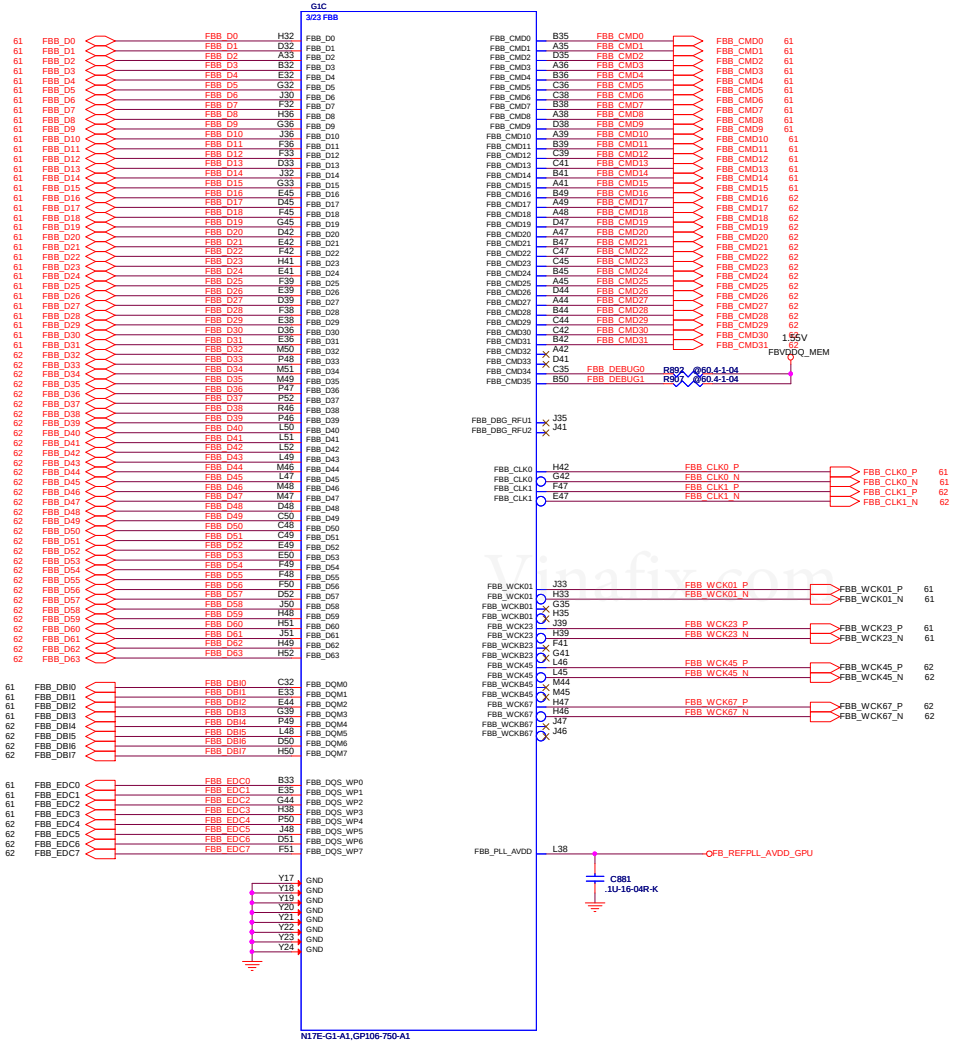
Title	NV-BIOS/XTAL	
Size C	Document Number GK5CN6X	Rev V A
Date: Wednesday, October 25, 2017	Sheet 48 of 72	



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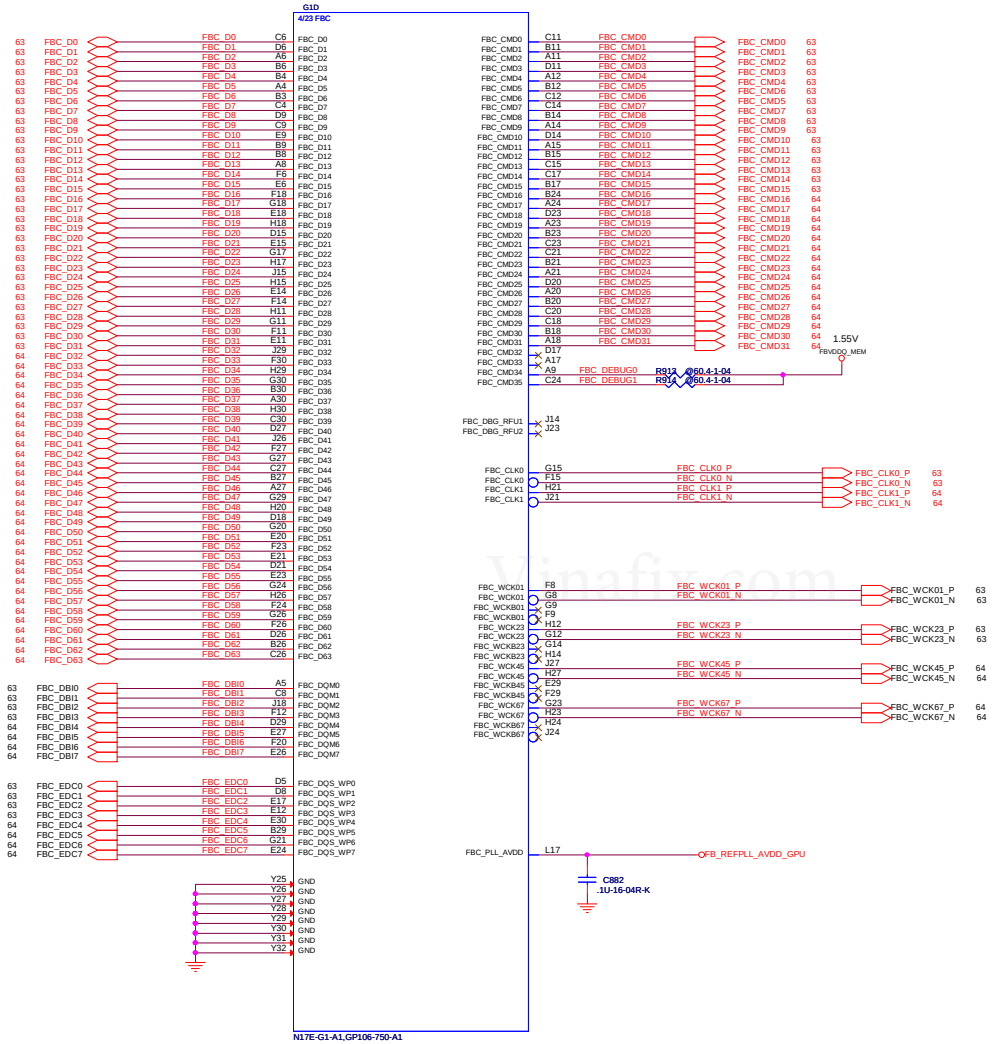
TEL:0512-62829228 <OrgAddr4>

Title	NV-Frame Buffer B	
Size C	Document Number GK5CN6X	Rev V A
Date: Wednesday, October 25, 2017	Sheet 49 of 72	



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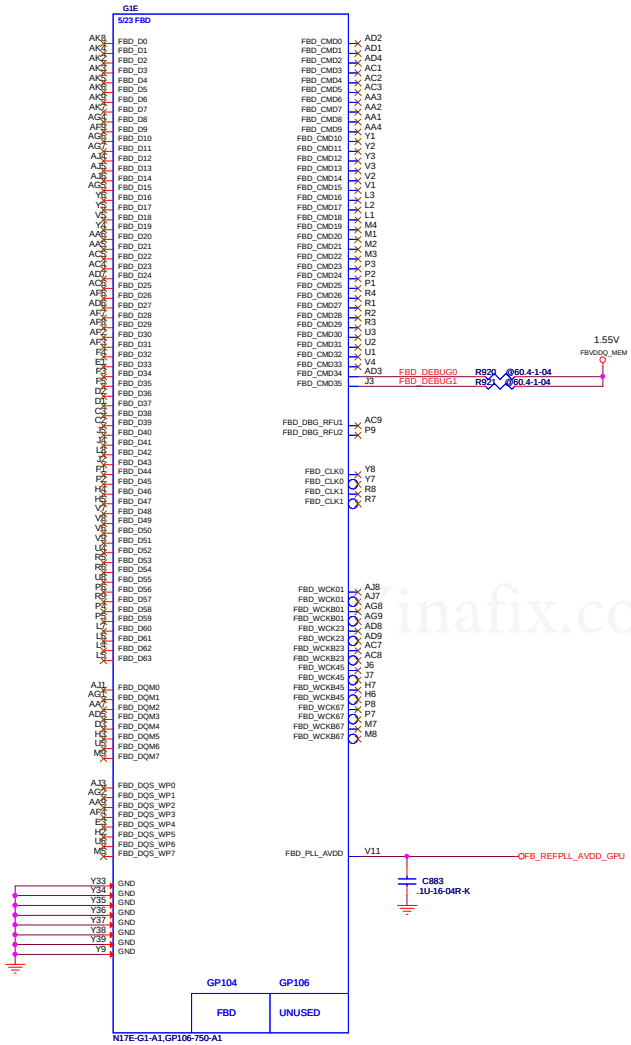
Title: NV-Frame Buffer C

Size: C | Document Number: GK5CN6X | Rev: V A

Date: Wednesday, October 25, 2017 | Sheet 50 of 72



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Title	NV-Frame Buffer D	
Size C	Document Number GK5CN6X	Rev V A
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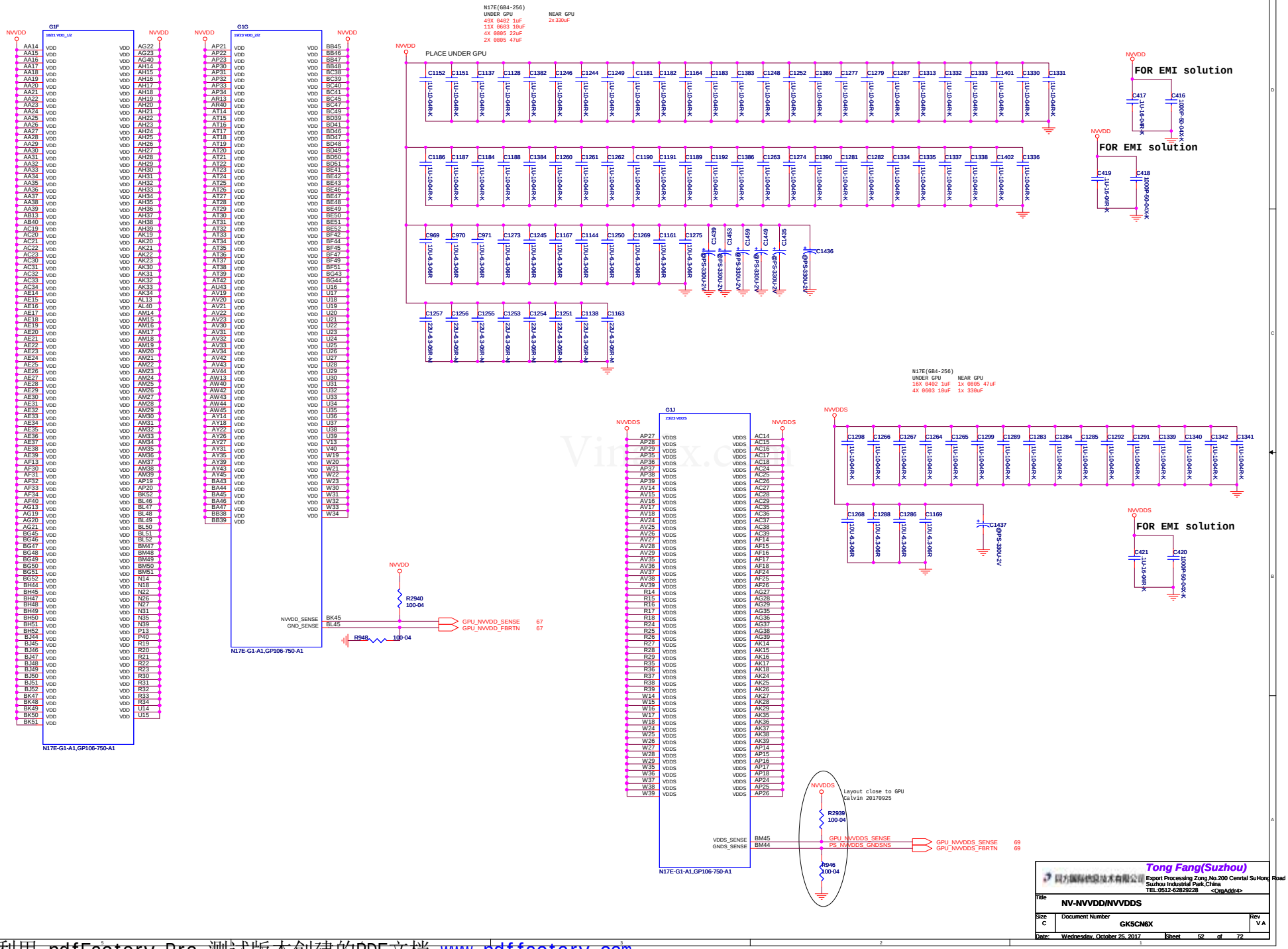

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Title	NV-NVVDD/NVVDDS	
Size C	Document Number GK5CN6X	Rev V A
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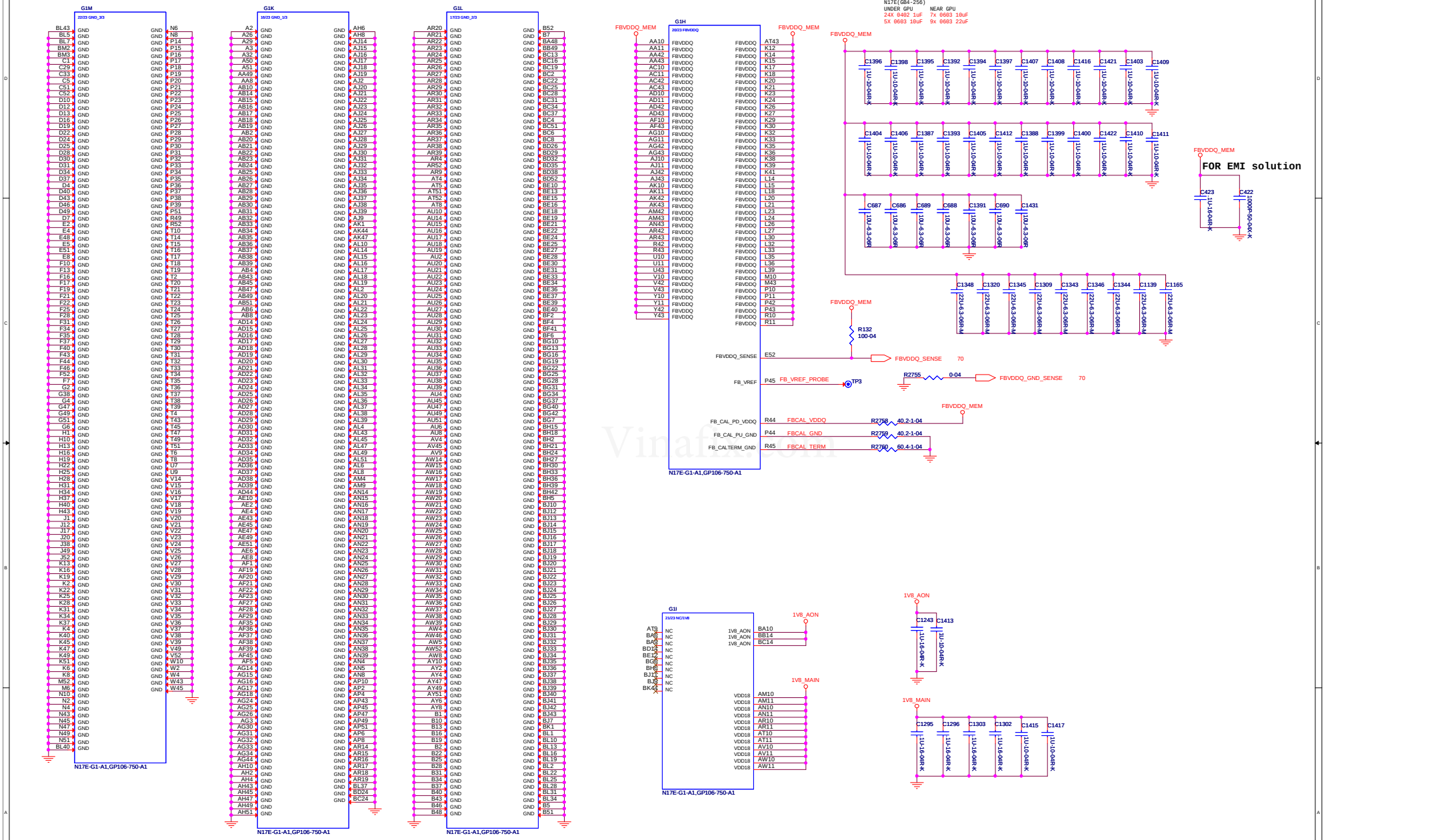
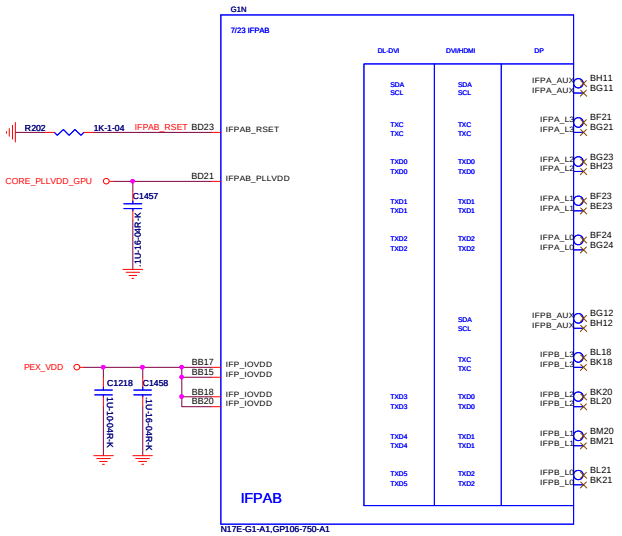
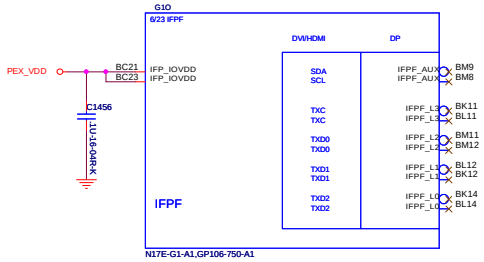
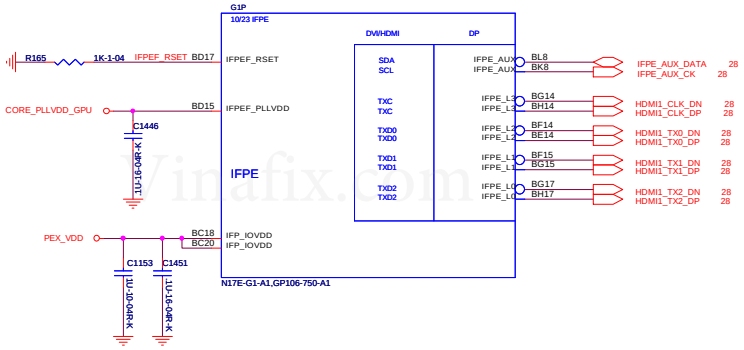
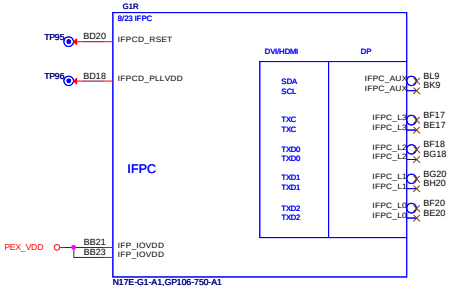


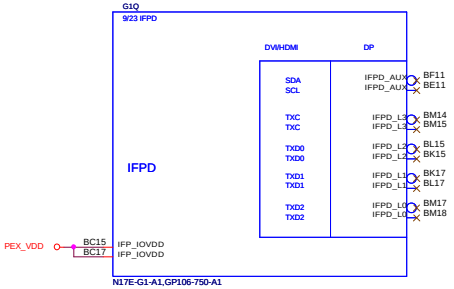
Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX











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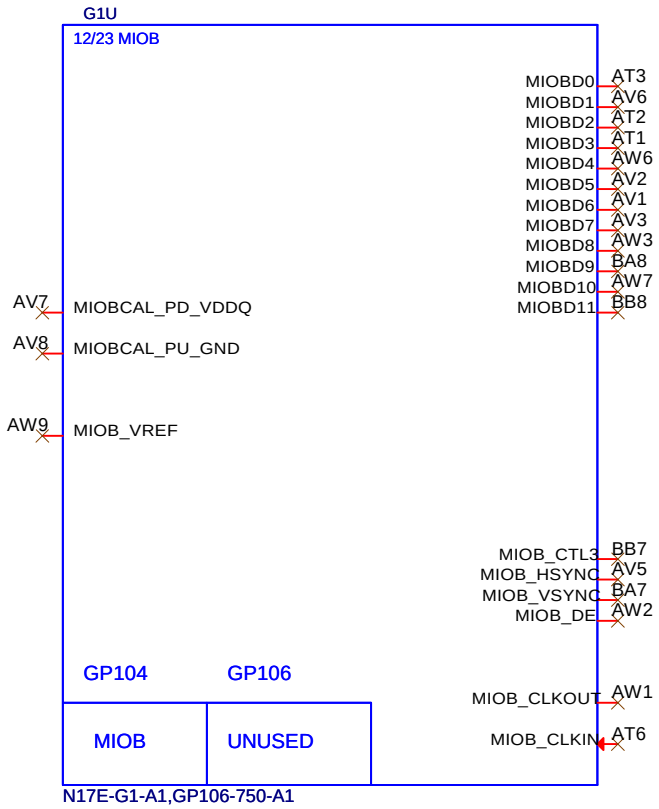
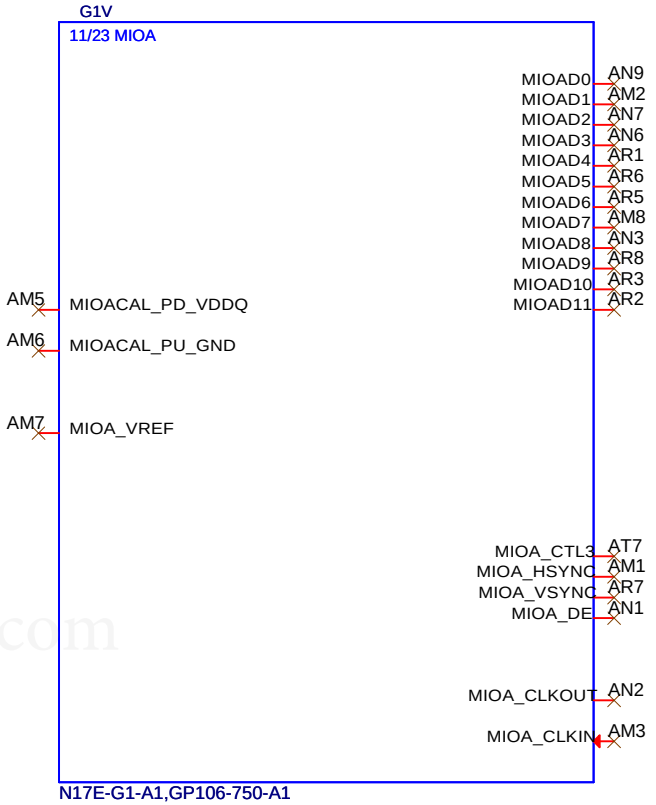
Title	NV-IPFA_B _C _D _E _F	
Size C	Document Number GK5CN6X	Rev V A
Date: Wednesday, October 25, 2017	Sheet 54 of 72	





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Title	NV-MIO	
Size A	Document Number GK5CN6X	Rev V A
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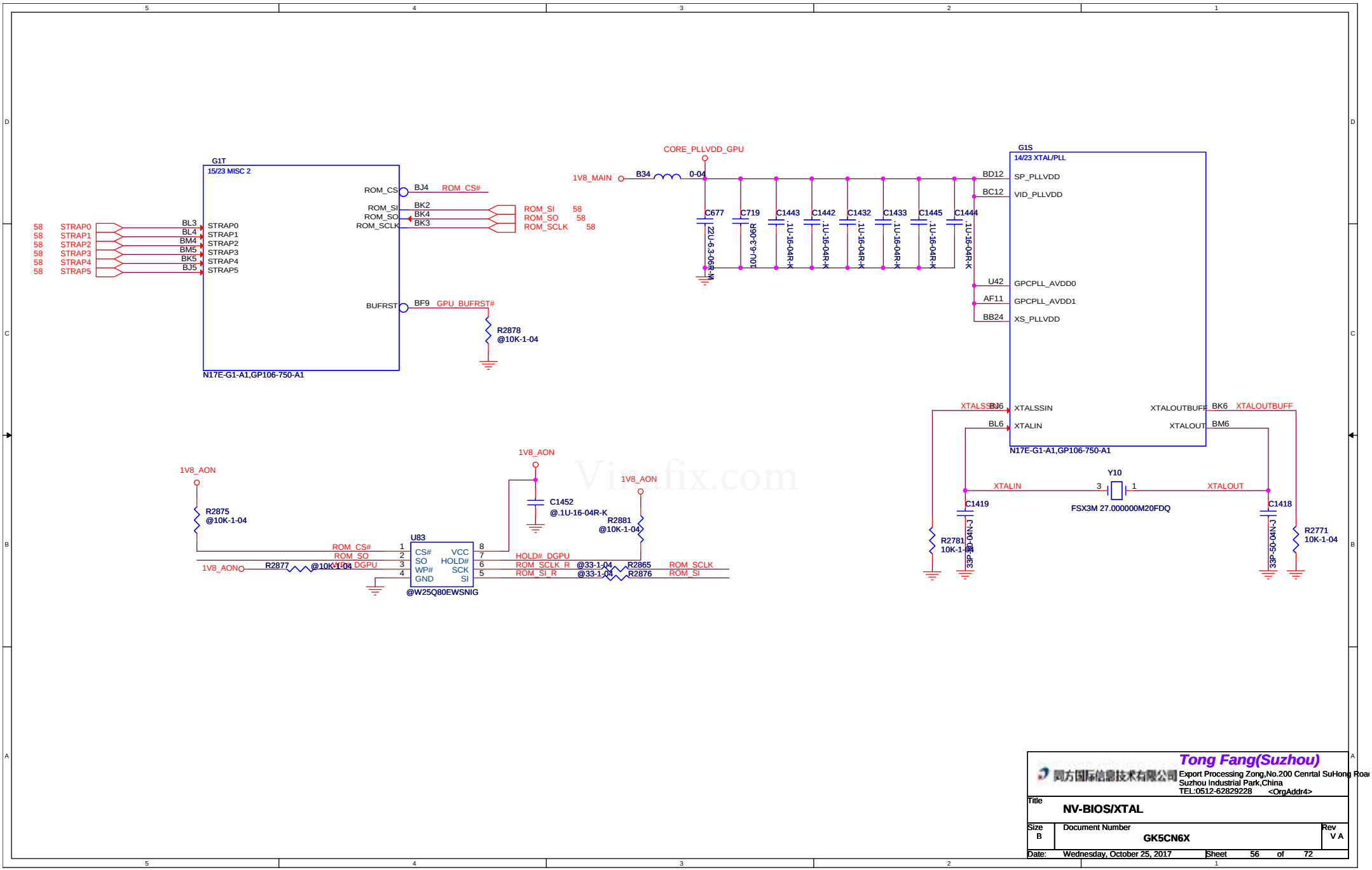

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Title: NV-BIOS/XTAL		
Size: B	Document Number: GK5CN6X	Rev: V A
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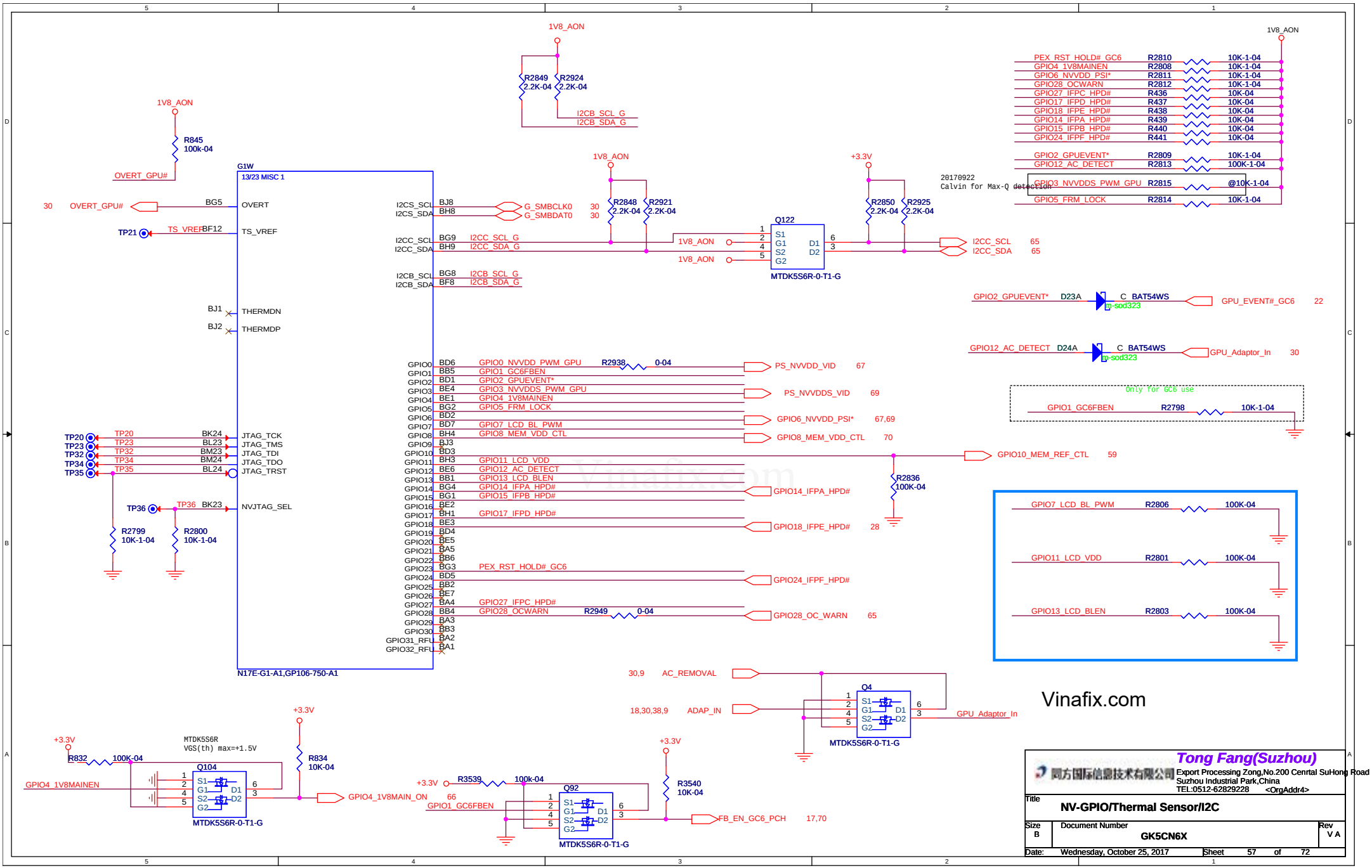


	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

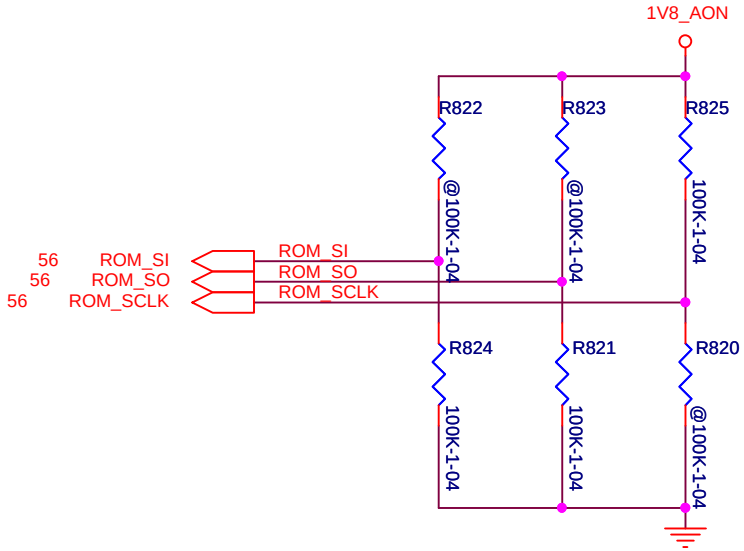
TOTAL LINK	TOTAL EN AUDIO	ROW INDEX
4	4	15
3	3	14
2	2	12
3	2	12
4	3	13

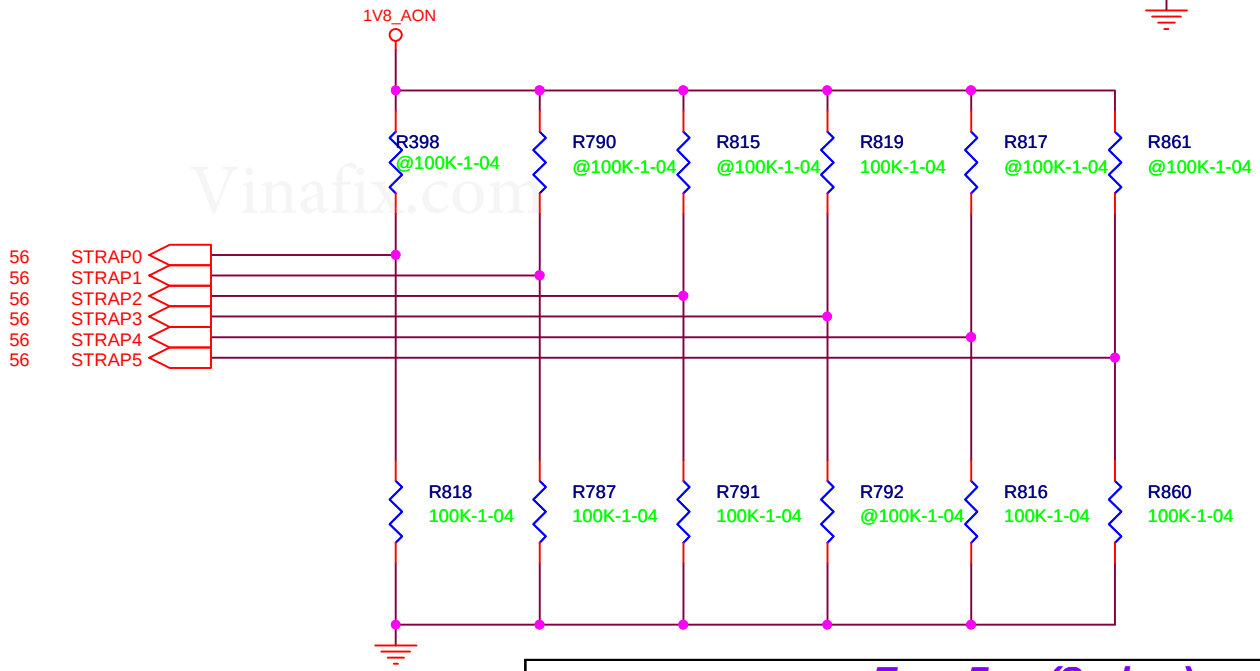
ROW INDEX	STRAP PIN		
	ROM_SO	ROM_SI	ROM_SCLK
15	L	L	L
14	L	L	H
13	L	H	L
12	L	H	H
11	H	L	L
10	H	L	H
8	H	H	H
0	H	H	M

Display Link 15

Based on RVL_07916_001_V10 JUNE 2017

GDDR5						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4G80325FB-HC25 B-die	0X0	L	L	L
8Gb	Micron	MT51J256M32HF-80:A A-die	0X1	L	L	H
8Gb	Hynix	H5GQ8H24MJR-R4C M-die	0X2	L	H	L
4Gb	Samsung	K4G41325FE-HC25 E-die	0X7	H	H	H
4Gb	Hynix	H5GQ4H24AJR-R4C A-die	0X6	H	H	L
4Gb	Micron					





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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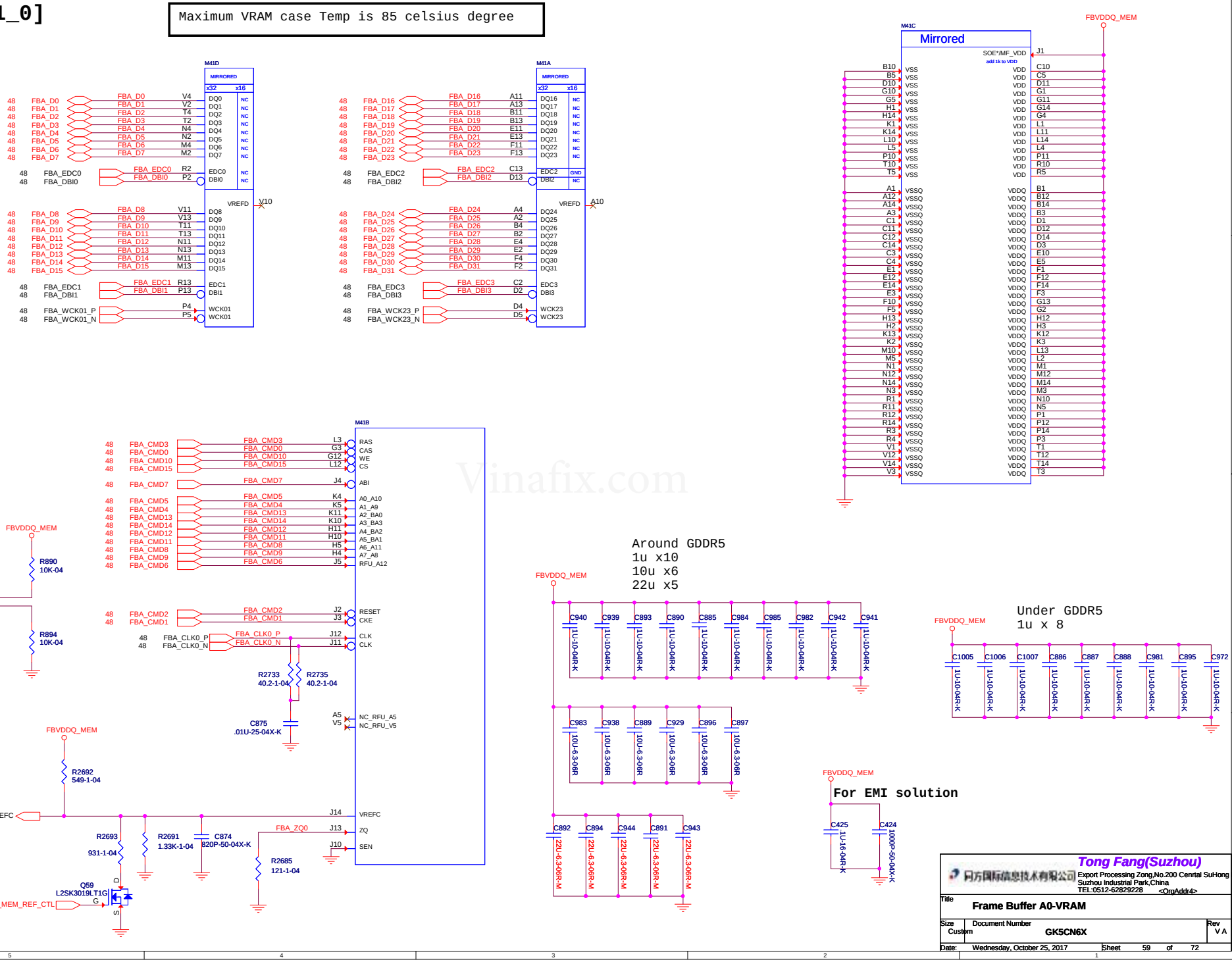
Title: STRAP

Size: A | Document Number: GK5CN6X | Rev: V A

Date: Wednesday, October 25, 2017 | Sheet 58 of 72

MEM_FBA[31_0]

Maximum VRAM case Temp is 85 celsius degree



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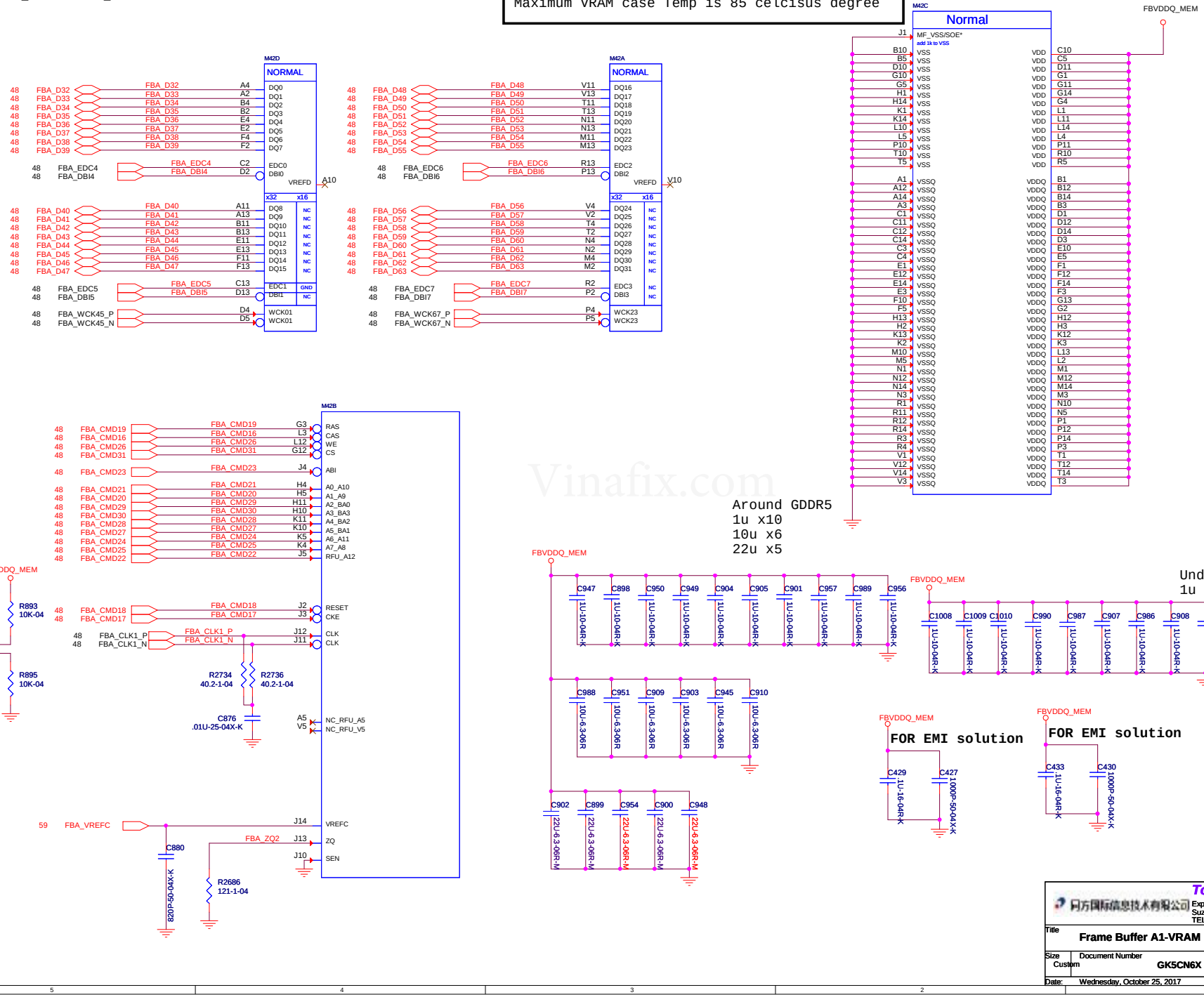
Title	Frame Buffer A0-VRAM		
Size: Custom	Document Number: GK5CN6X		Rev: V A
Date: Wednesday, October 25, 2017	Sheet 59 of 72		

MEM_FBA[63_32]

Maximum VRAM case Temp is 85 celcisus degree



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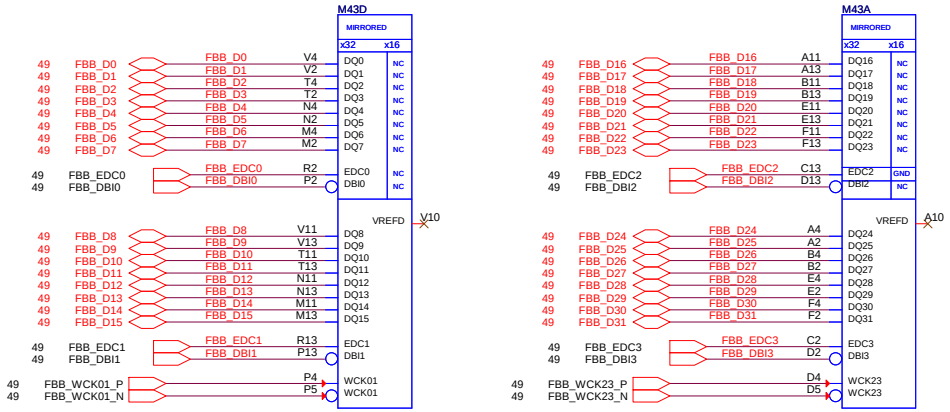
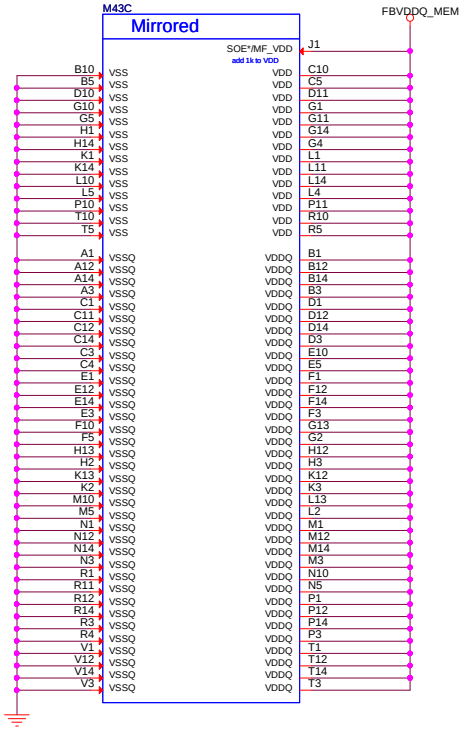
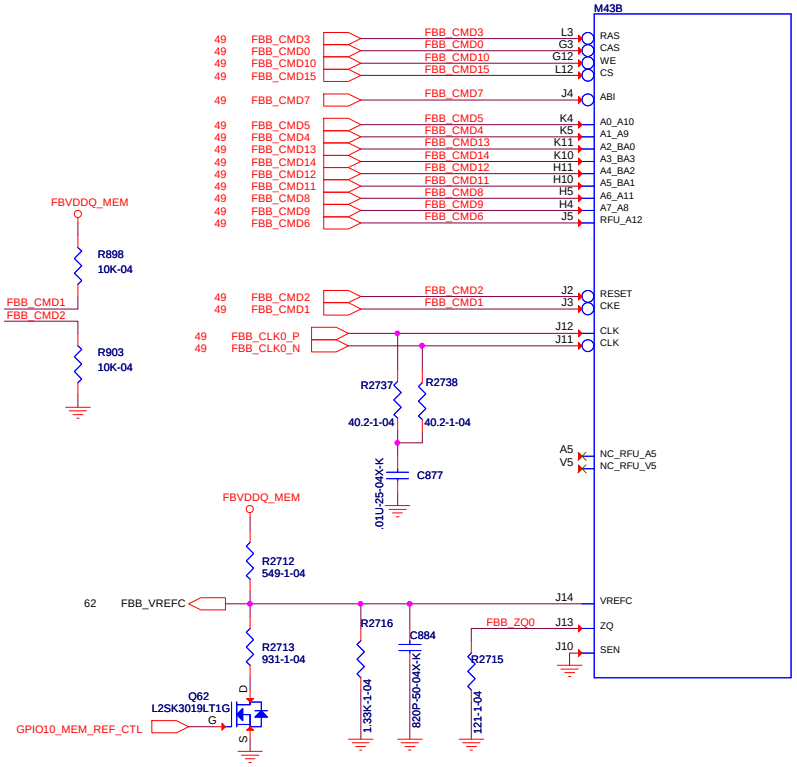
Title	Frame Buffer A1-VRAM	
Size: Custom	Document Number: GK5CN6X	Rev: V A
Date: Wednesday, October 25, 2017	Sheet 60 of 72	

MEM_FBB[31_0]

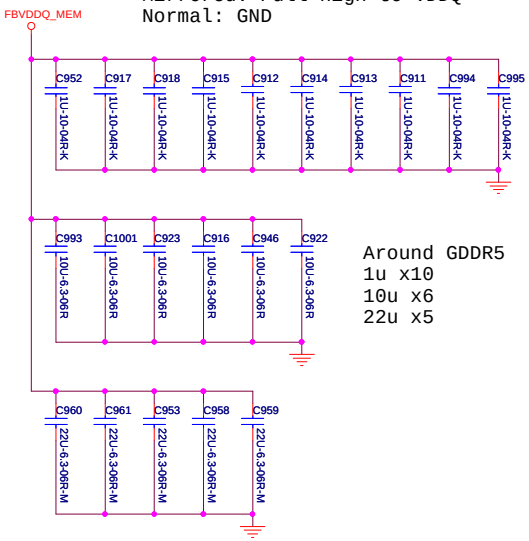
Maximum VRAM case Temp is 85 celcisus degree





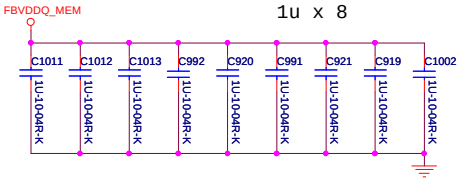


Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5

Under GDDR5
1u x 8



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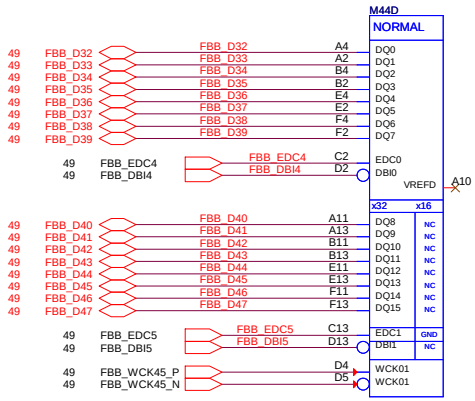
Title: Frame Buffer B0-VRAM

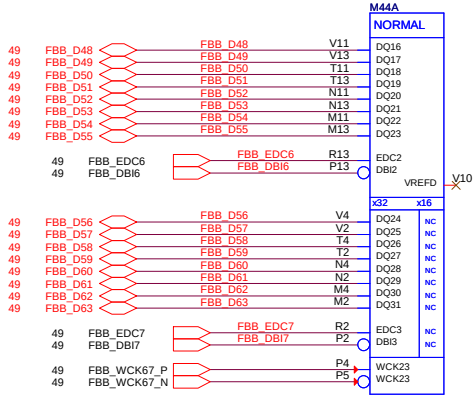
Size: Custom | Document Number: GK5CN6X | Rev: V A

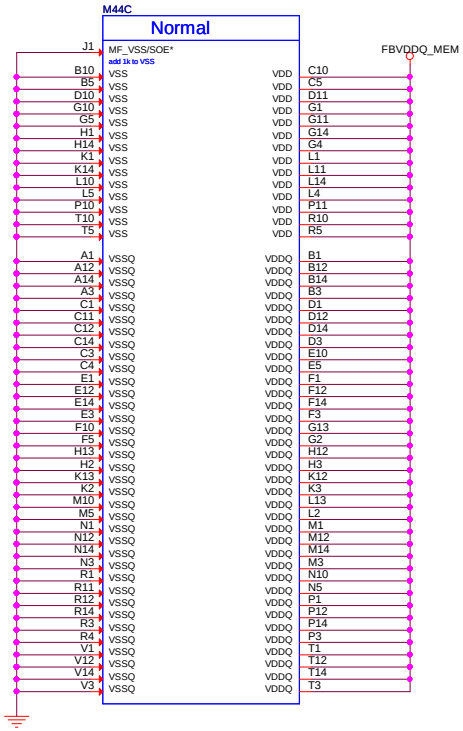
Date: Wednesday, October 25, 2017 | Sheet 61 of 72

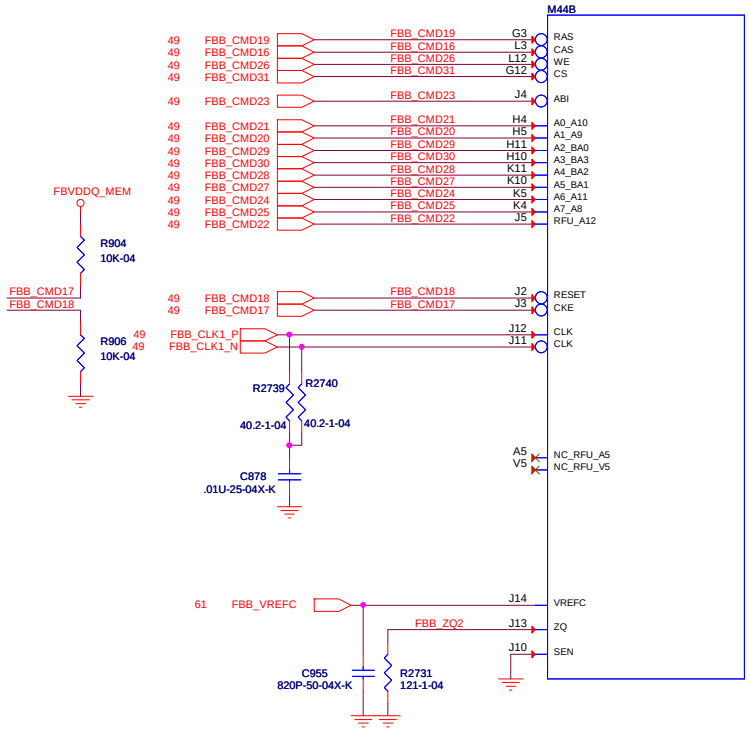
MEM_FBB[63_32]

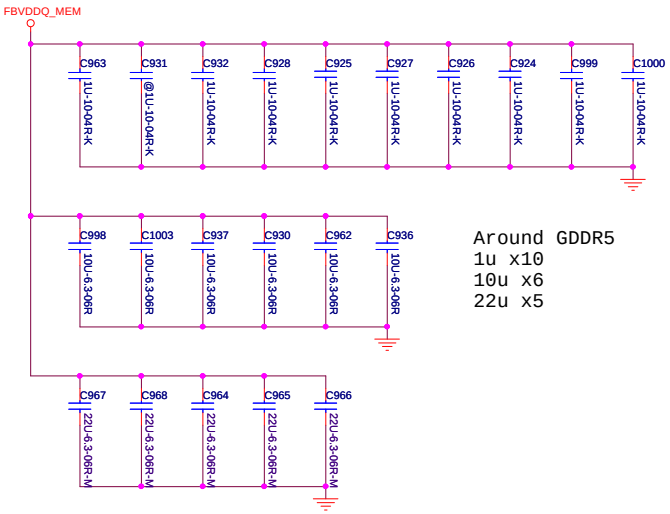
Maximum VRAM case Temp is 85 celcisus degree



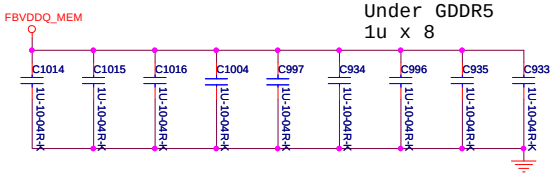








Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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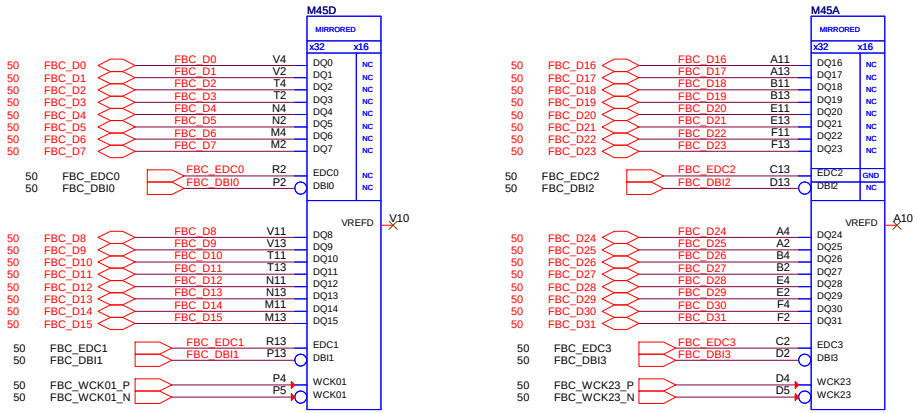
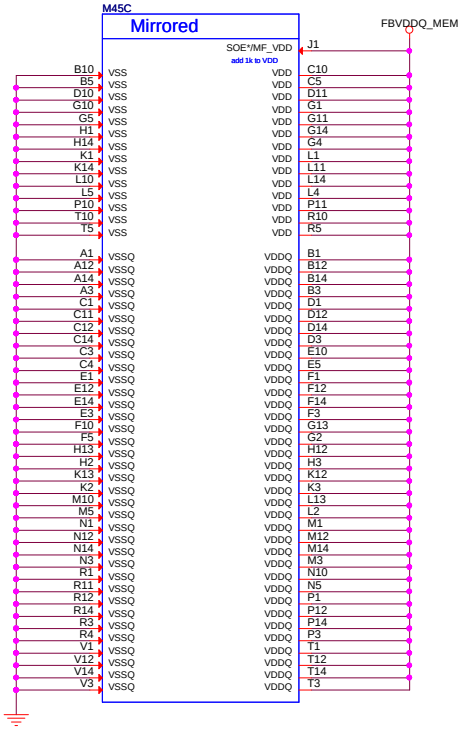
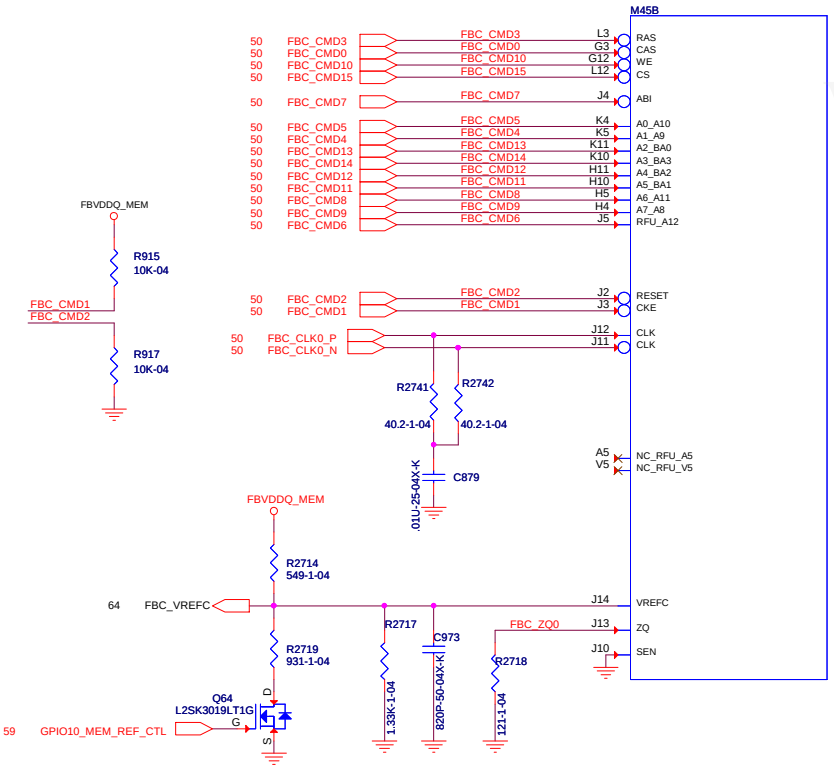
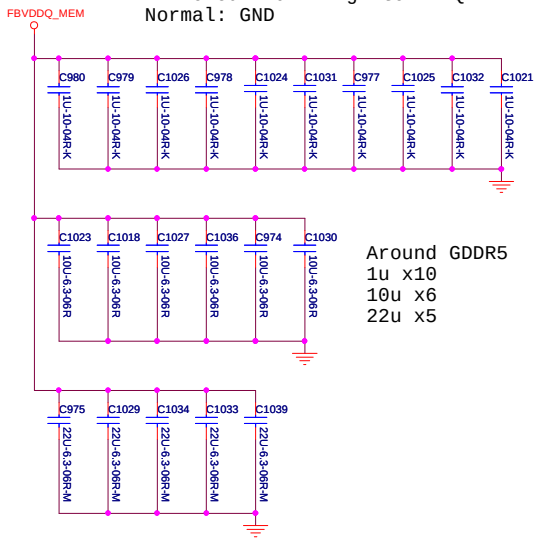
MEM_FBC[31_0]





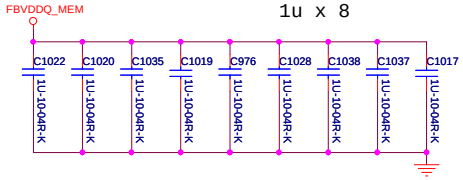


Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5

Under GDDR5
1u x 8



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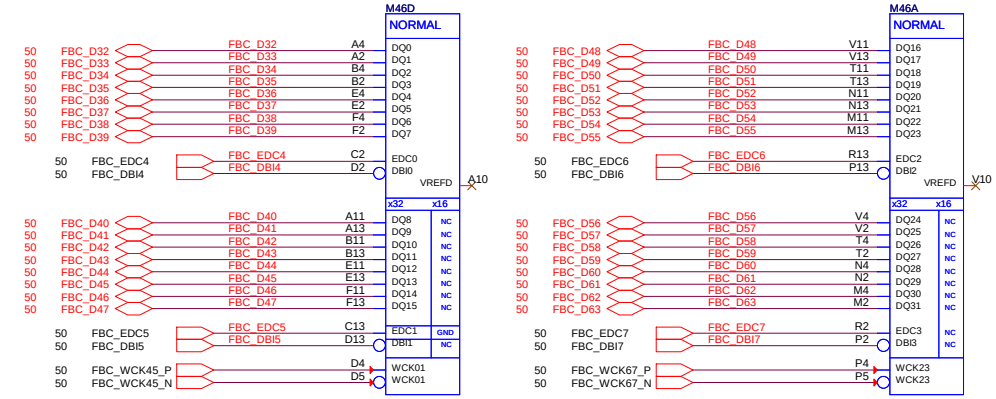
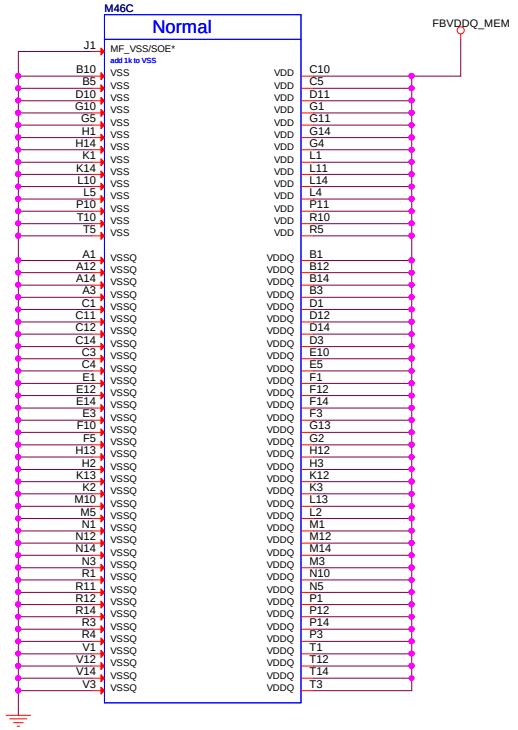
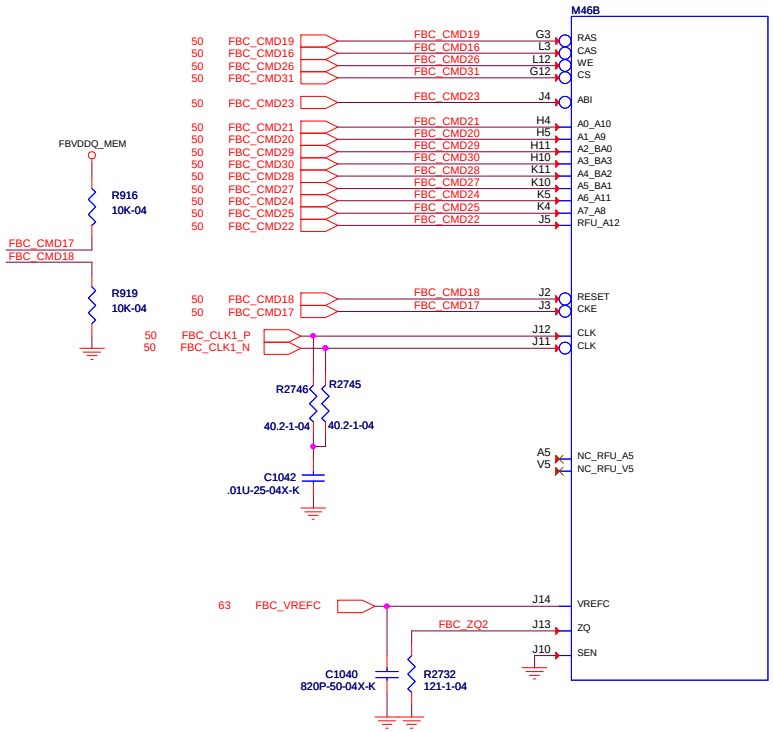
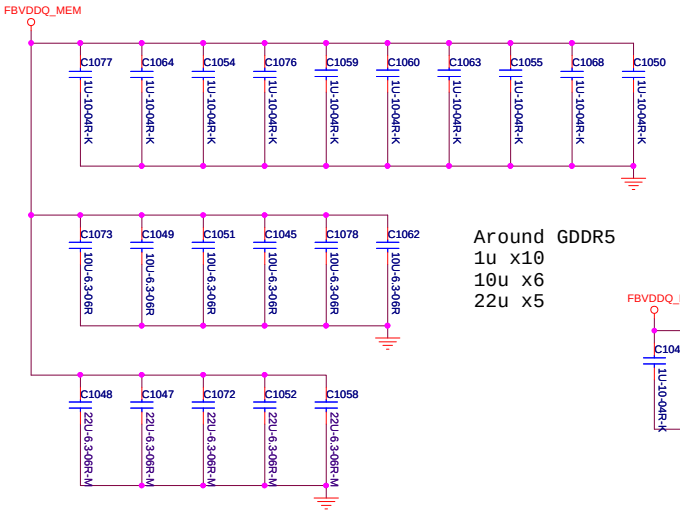
MEM_FBC[63_32]

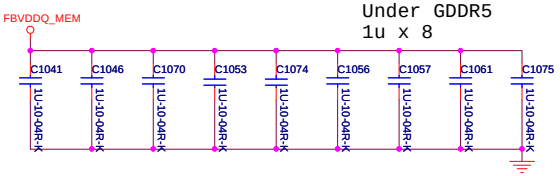








Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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Title	Frame Buffer C1-VRAM	
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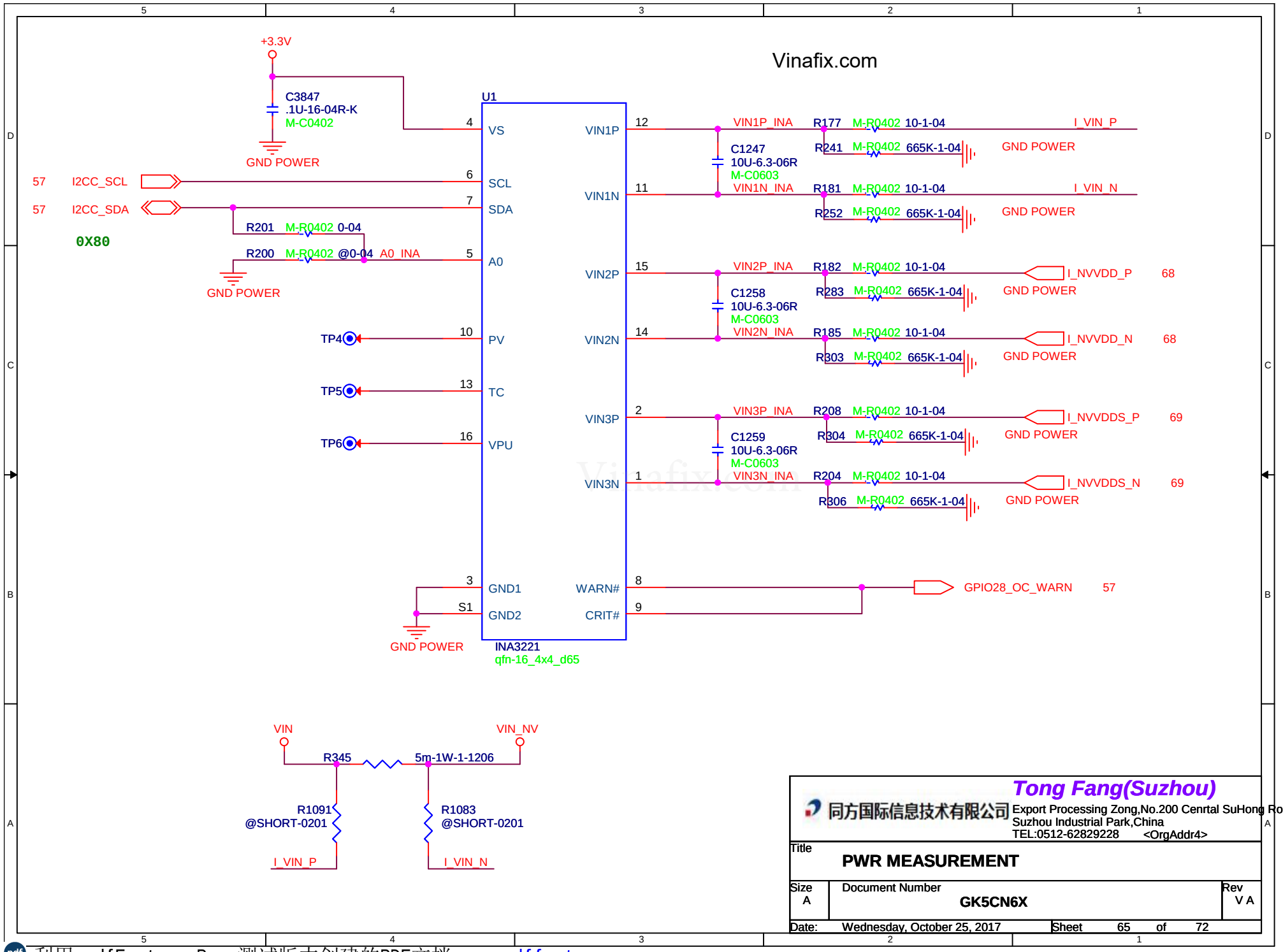
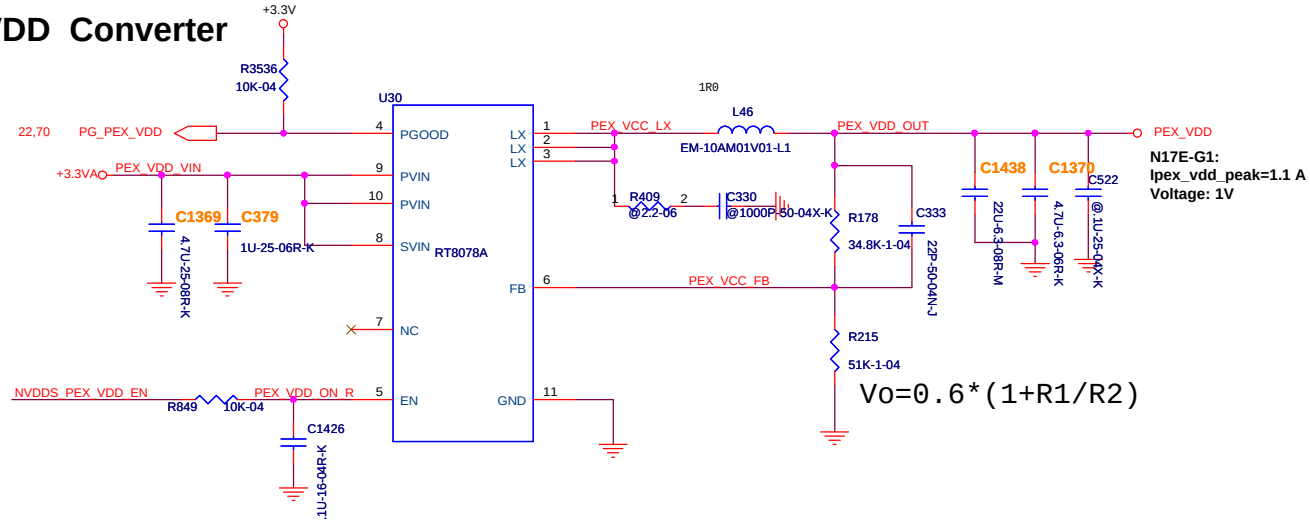
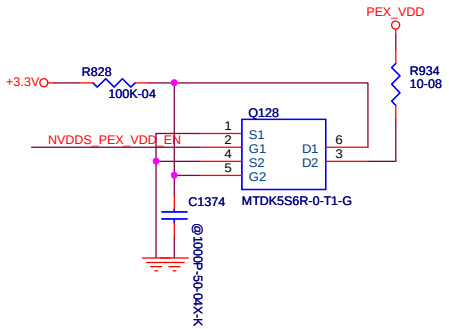
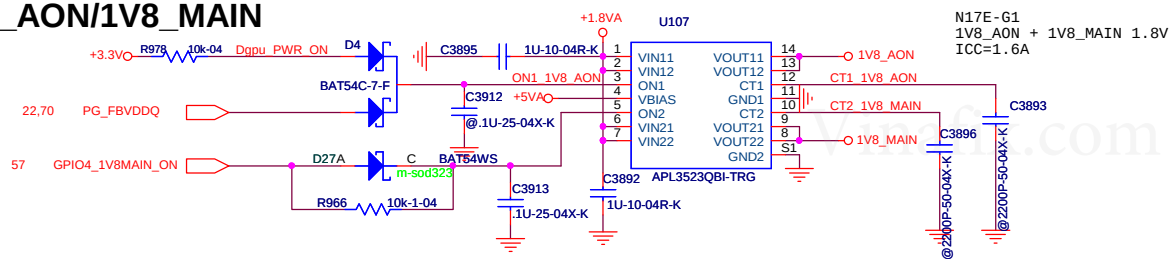


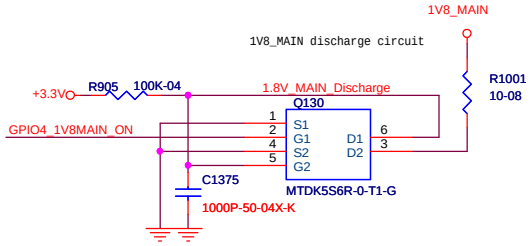
PEX_VDD Converter

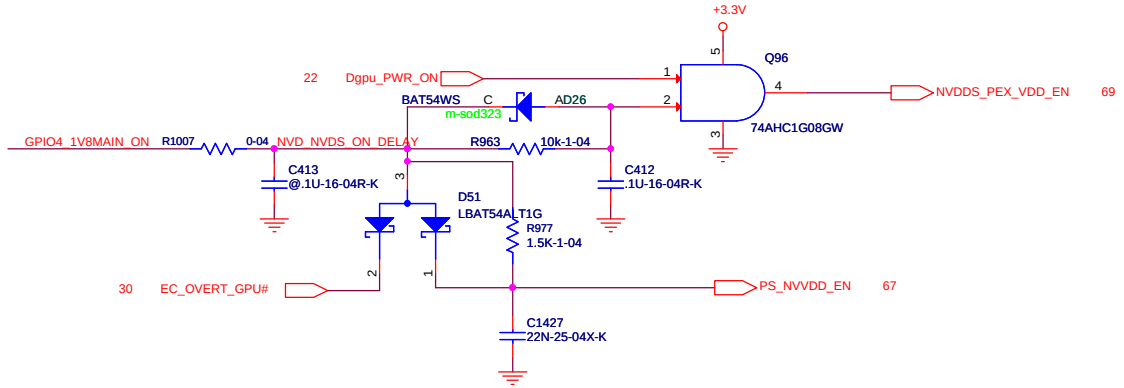




1V8_AON/1V8_MAIN







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Title: DGPU PEX_VDD/1V8_AON		
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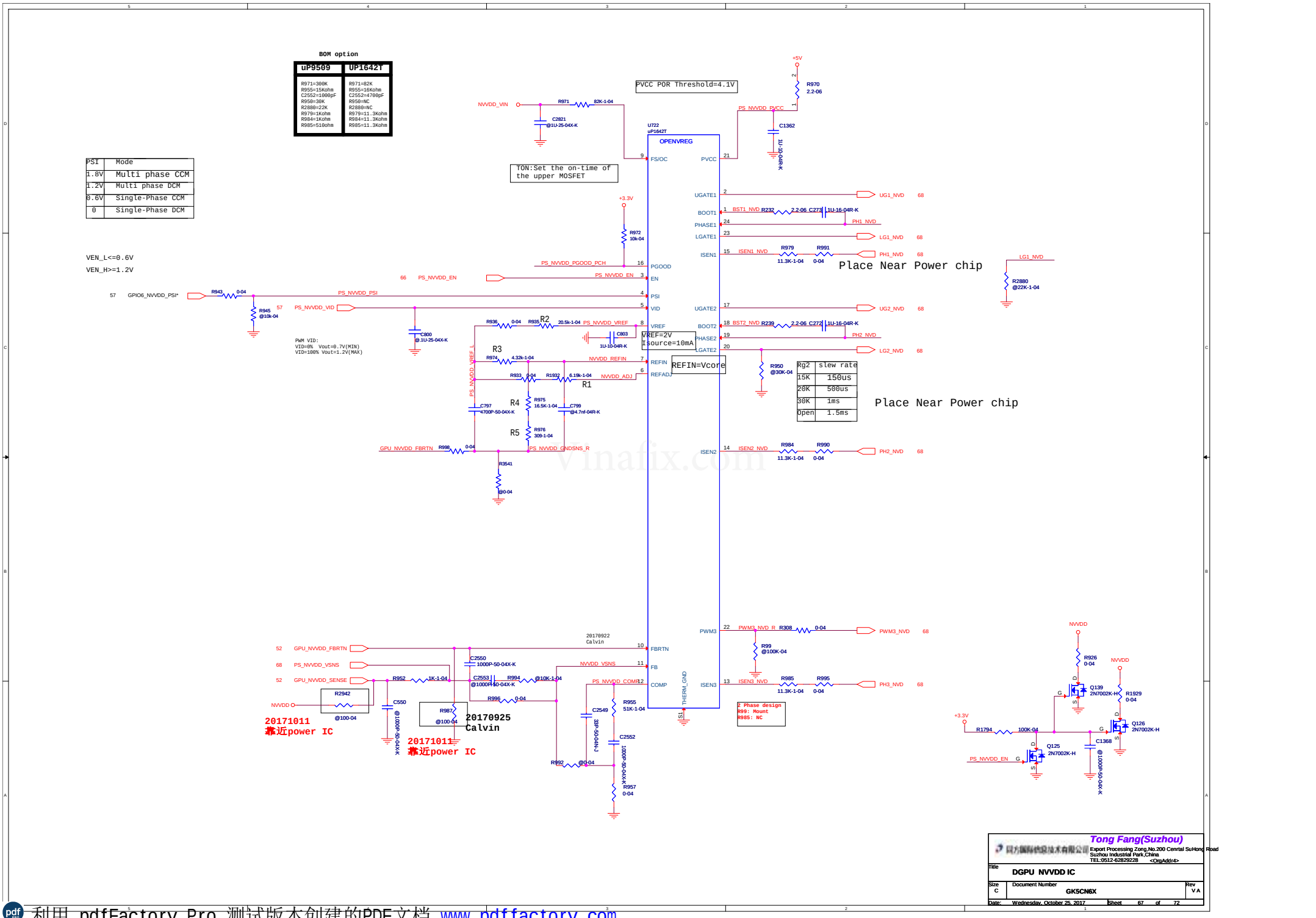
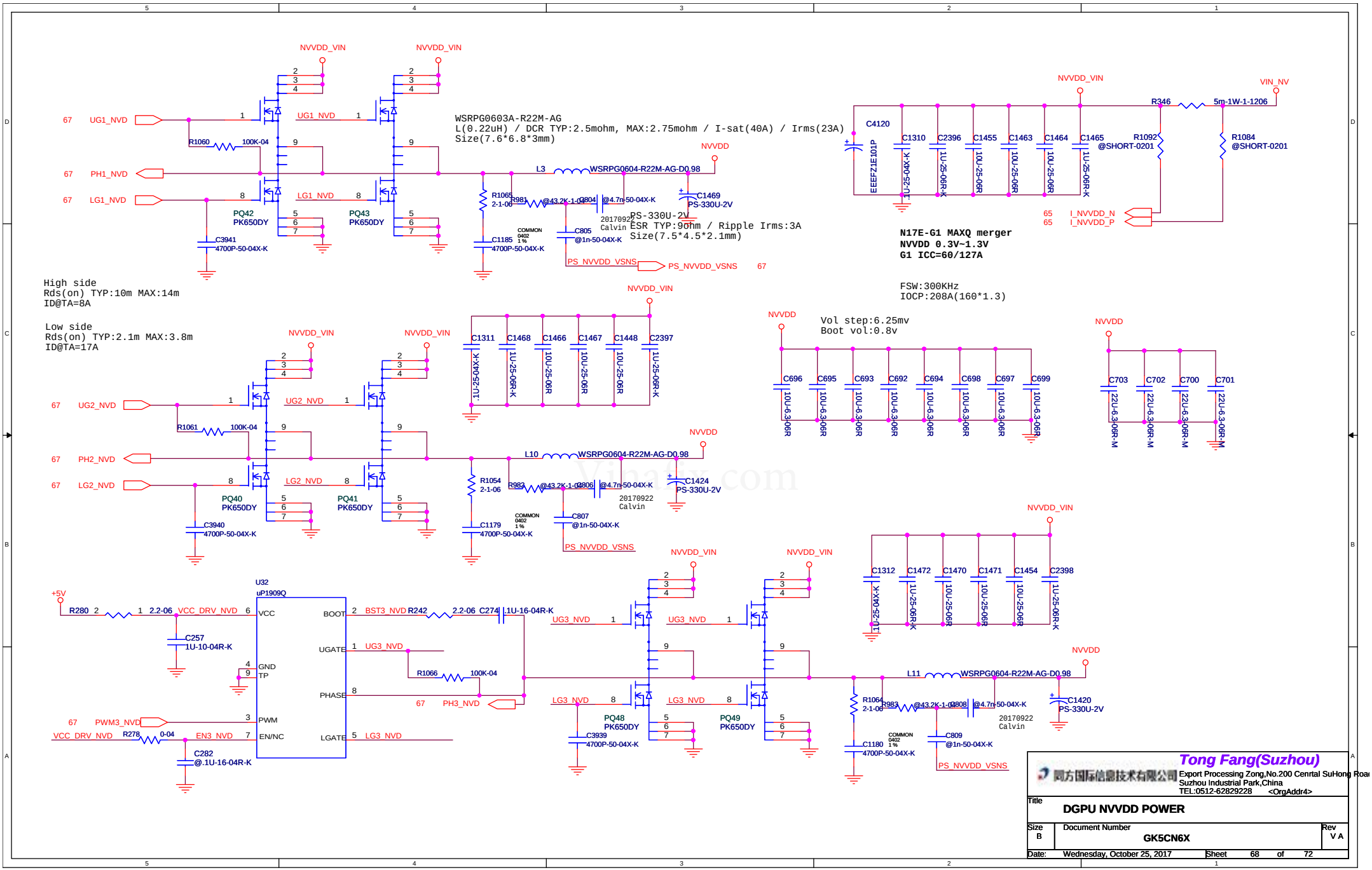
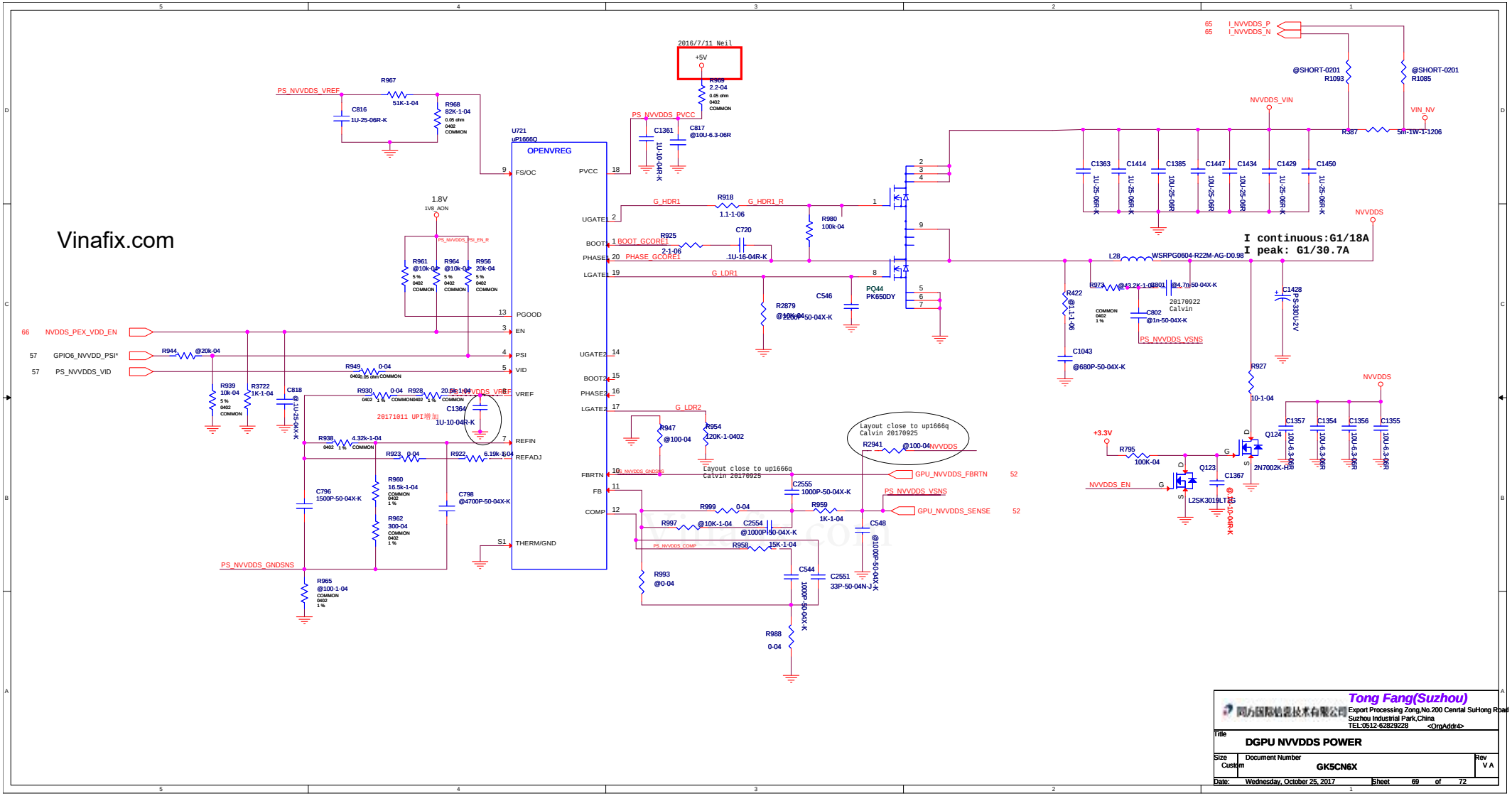
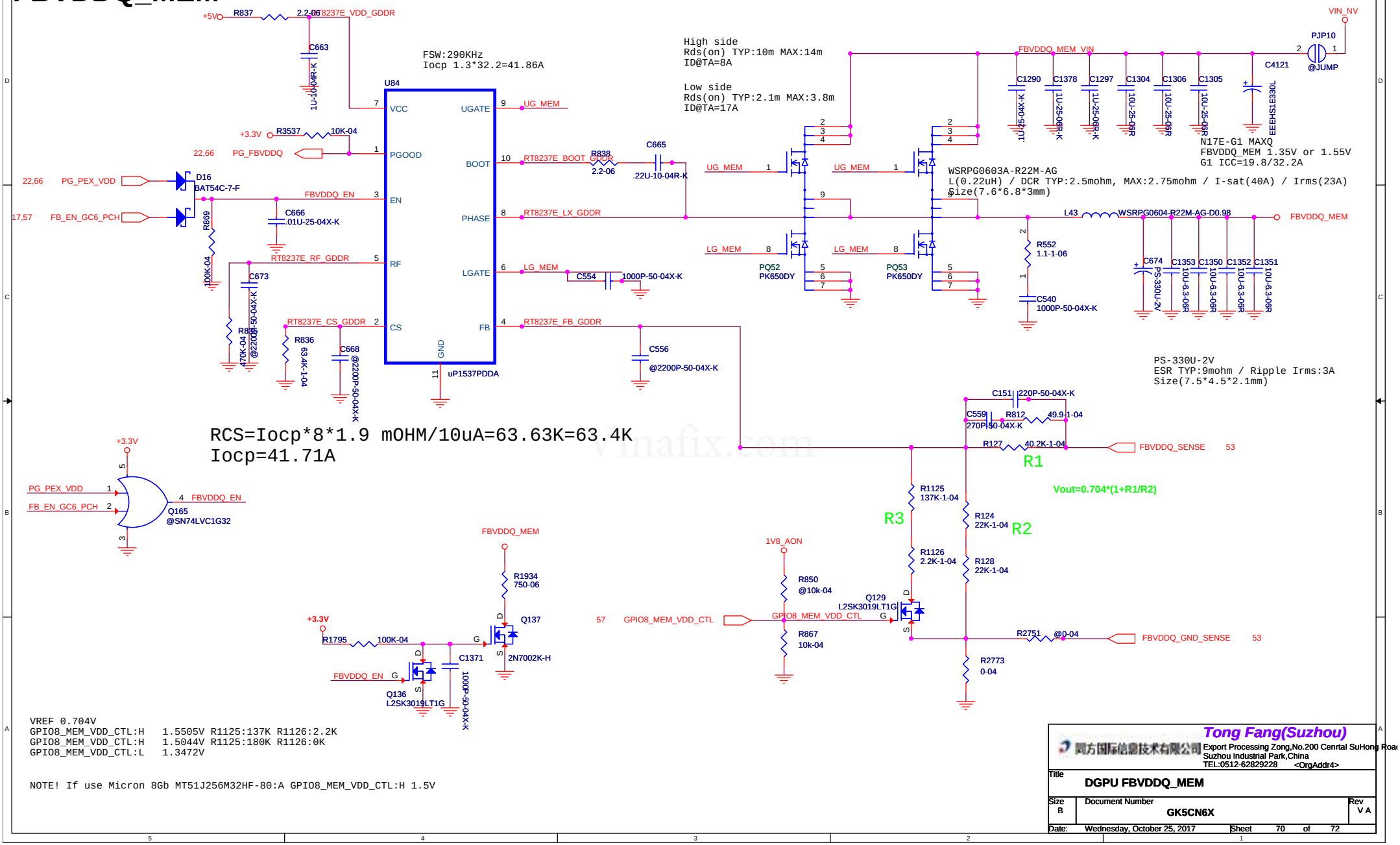






FBVDDQ_MEM



VREF 0.704V
GPIO8_MEM_VDD_CTL:H 1.5505V R1125:137K R1126:2.2K
GPIO8_MEM_VDD_CTL:H 1.5044V R1125:180K R1126:0K
GPIO8_MEM_VDD_CTL:L 1.3472V

NOTE! If use Micron 8Gb MT51J256M32HF-80:A GPIO8_MEM_VDD_CTL:H 1.5V

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Title	DGPU FBVDDQ_MEM	
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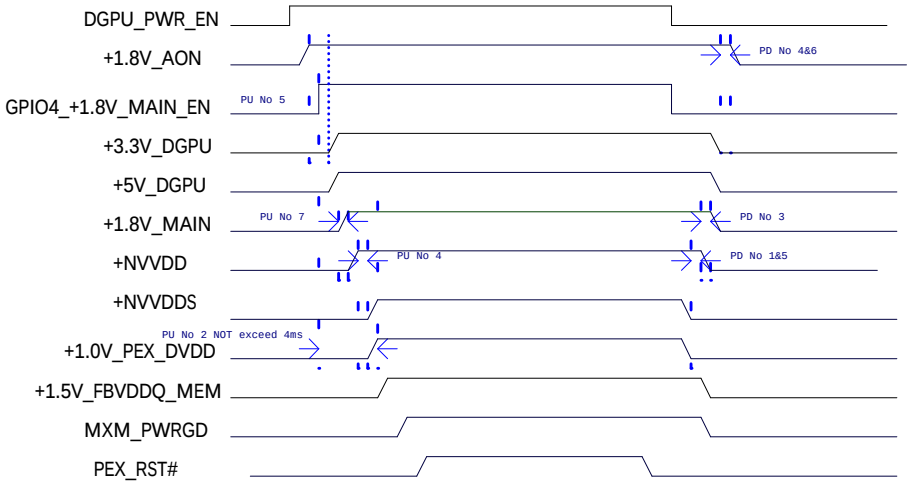
POWER SEQUENCE



POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD/+NVVDD_PGOOD) must NOT exceed 4ms.
3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required
1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
2.All other power rails can ramp down together with NVVDD.
3.+1.8V_MAIN must power down after NVVDD power down
3.The progapation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

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Title: DGPU POWER SEQUENCING
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Date Chang History

20170916
FB_EN_GC6_PCH from GPP_K0 to GPP_K10
P17 remove pull low
P22 remove pull high

20171010
1、删除Mini DP，HPD diode
2、增加RJ45，transform
3、修改成GJ power 小板
4、修改成GJ USB2.0小板
5、修改成GJ Audio小板
6、增加led
7、增加power SW
8、将wlan led GPIO改成ID_det
9、增加USB3.0x2 on borad
10、增加usb2.0x3
11、增加LID线路
12、增加Q-key1 SWx2
13、修改DDR CN1、CN11 footprint
14、删除hole H7、H9、H22
15、删除PQ45、C1430
16、修改USB3
17、修改HDMI、type-c footprint
18、增加H7、H9，删除H26
19、增加c4117、c4118、c4119、c4120、c4121
20、更新HDMI、type-c footprint
21、更新c4117、c4118、c4119、c4120、c4121 footprint
22、更新cn14、cn9 footprint
23、更新cn12、cn34 footprint
24、更新m.2、mini、bat conn footprint
25、更改GPIO扣，chg-o-led变成tp led；fanboost变成 c cover
26、更新SW6、led1、led2、led4、cn41、cn19、cn42、sw1、sw2、sw3、cn30、cn17、cn18等footprint
27、修改AUX-off线路
28、增加GPE1为VRA-PE
29、修改PCE5、PCE6电容为.1u
30、修改RJ45 pin number
31、删除H9，L24、L25、L26、L27垂直swap
32、修改L3, L10, L11, L28, L43的value footprint
33、删除NVDD和NVDSS co-lay
34、增加EC_lanwake
35、lanwake和wlanwake softstart
36、更改gpio lanwake
37、增加c1453、c1439、c1449、c1459
38、C3990, C3991的value改成22U-6.3-06R-M，footprint: M-C0603
39、更新c4117、c4118、c4119、c4120 footprint
40、修改L12、L14、L15、L17

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Title	History	
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