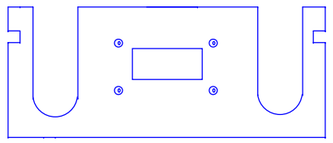
MODEL NAME : ***Centenario (DDP31)***

PCB NO : ***LA-G172P***

BOM P/N :

ZZZ1 LA-G172P_MB



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Schematic Document

(CENTENARIO ICE Lake U)

2019-05-29

Rev: 1.0 (A00)

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	*P001 - Cover*		
Size	Document Number *LA-G172P*		Rev 1.0 (A00)
Date: Wednesday, May 29, 2019	Sheet 1 of 101		

Hinge up

PCH SPI Flash ROM 32M p.9
SPI
SPI#0
TPM1.2/2.0 ST ST33TPHF2XSPI p.66
SSD 20x16 BGA 128G/256GB / 512GB p.68
PCIe Gen3 x 4lanes
PCIe#9,10,11,12
M.2 SSD-Key B Debug p.67
PCIe Gen3 x 2lanes
PCIe#13,14
RFFEM
WLAN/BT 5.1 Solder down Harrison Peak AX 22560 &Killer 1435-S 1216 SIP p.52
1216
PCIe Gen2 x 1lane
PCIe#3
USB2.0
USB2#3
CNVi Gen2
CNVi Gen2
uSD Connector p.70
SD4.0/SDXC
SD_WP
Card Reader 4.0 RealTek RTS5242 PCIe to SD p.70
PCIe Gen2 x 1lane
PCIe#16
GPIO (BIOS Controlled)
TBT ~4dB/2"
SBU 2
Burnside Bridge TBT Re-Timer p.46,47
SMBUS
TBT ~15dB / 7"
LSx / AUX
I2C
SML#0
TBT#0
LSx / AUX
SML#1
USB2#8
RT SPI Flash ROM 8M p.46
USB Type-C TBT with PD (Left)
VBUS
CC 2
TPS65987-DH
VBUS
PP_HV1
PP_HV2
CC
VCONN
CHRG_IN
5VALW
I2C2
I2C1
SPI
p.42
PD SPI Flash ROM 8M p.42
to EC
USB2/I2C MUXES_L
USB (Top)
USB (Bottom)
USB
p.43
p.50
TBT ~4dB/2"
SBU 2
Burnside Bridge TBT Re-Timer p.48,49
SMBUS
TBT ~15dB / 7"
LSx / AUX
I2C
TBT#2
LSx / AUX
USB2#9
RT SPI Flash ROM 8M p.48
USB Type-C TBT with PD (Right)
TPS65987-DH
VBUS
PP_HV1
PP_HV2
CC
VCONN
CHRG_IN
5VALWB
I2C2
I2C1
SPI
p.44
PD SPI Flash ROM 8M p.44
to EC
USB2/I2C MUXES_R
USB (Top)
USB (Bottom)
USB
p.45
p.50

IceLake-U 4+2

DDI#A
eDP x4 lanes
13.3" 16:10 Sharp FHD+/UHD+ eDP v1.4b LED Driver Artic sand ARC3C0845
I2C#0
I2C
Touch Screen Controller Wacom G14T-W90xx p.38

LPDDR4 4GB X32x4 Memory Down
LPDDR4x 8/16/32 GB X32x4 Memory Down
Memory Bus (LPDDR4 / x)
Dual Channel 3733MHz
LPDDR4/x - ChA p.23,24
Memory Bus (LPDDR4 / x)
Dual Channel 3733MHz
LPDDR4/x - ChB p.23,24

Middle Board
UFCAM module
CSI2-E#1
MIPI CSI-2 x 1lanes
I2C#3
I2C
ISH_I2C#1
ISH_I2C
RGB camera OV01A
CAM LED
AMS TSL2584TSV
2xDMIC
DMIC
SMB
SMB
MIPI60 Debug p.79
Gyro + Accelerometer ST LSM6DS3USTR
e-compass ST LIS2MDLTR
DMIC
DMIC
DMIC
Audio Codec with Amplifier ALC3281-CG p.56
HDA
HDA
Universal Headset Jack p.57
2xSpeaker p.57
Sensor Board
Gyro + Accelerometer ST LSM6DS3USTR
e-compass ST LIS2MDLTR
ISH_I2C#0
ISH_I2C
USB2#1
USB2#2
USB2.0
USB3.1
USB DCI Debug p.79
ISH_GP#5
NB_LID#
Fingerprint module
Fingerprint Controller GOODIX GF5288+HT32 p.77
USB2.0
USB2#5
ISH_GP#6
TAB_LID#
I2C#1
I2C
Power Button p.77
PWRBTN#
GPP_D13
GPP_D14
eSPI
SMBUS
eSPI
KB Transfer Board
+3V_NB_LID
Hall Sensor BU52058
SMB#03
GPIO
GPIO
TAB_LID#
GPIO
GPIO
NB_LID#
GPIO 161 (VCI_IN2#)
GPIO
BATBTN#
to Battery Gauge FPC
EC MEC5105
PWM
PWM#0
Fan 1 p.77
PWM
PWM#1
Fan 2 p.77
2nd Accelerometer ST LNG2DMTR
to PD & USB2/I2C MUXES
SMBUS
SMB#04
BCM#1
BC Bus
KB Controller ECE1117
Keyboard
Touchpad
VCCIN Controller MP2940AGRT p.91
SMBUS
SMB#05
Charger p.83
SMBUS
SMB#10
PS/2
PS/2
SMB#00
SMBUS
Battery Connector p.82
LED
p.33
+3V_NB_LID
Battery Gauge
LNG2DMTR

EC UART Debug/80 port
MIPI60 Debug
SPI Programmer
APS Debug
PD Programmer/I2C
BIOS UART Debug
DCI Debug
JESPI Debug
RT Programmer
Coin Cell

Hinge Down

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.
Title: P002 - Block Diagram
Size: Document Number: LA-G172P
Rev: 3.0 (ADI)
Date: Friday, May 04, 2018
Sheet 2 of 101

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 5%	4700p	M00	0.1
1	130K +/- 5%	4700p	X00	0.2
2	62K +/- 5%	4700p	X01	0.3
3	33K +/- 5%	4700p	X02	0.4
4	8.2K +/- 5%	4700p	X03	0.5
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p		

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	VCCIN Controller	PD Controller	MIPI60	USB/I2C MUX	BurnSide Bridge	Accel+Gyro
PCH_SML0CLK PCH_SML0DATA	PCH								V	
PCH_SML1CLK PCH_SML1DATA	PCH					V			V	
SMBCLK SMBDATA	PCH						V			
EC_SMB03_CLK EC_SMB03_DAT	MEC5105	V								
EC_SMB04_CLK EC_SMB04_DAT	MEC5105					V		V		
EC_SMB05_CLK EC_SMB05_DAT	MEC5105				V					
EC_SMB10_CLK EC_SMB10_DAT	MEC5105		V	V						
EC_SMB00_CLK EC_SMB00_DAT	MEC5105									V

PCIE/USB3.1

Flexible I/O	Interface	DESTINATION
0	PCI-E#1 / USB 3.1#1	None
1	PCI-E#2 / USB 3.1#2	USB DCI Debug
2	PCI-E#3 / USB 3.1#3	WLAN PCIe Gen2(Reserve)
3	PCI-E#4 / USB 3.1#4	None
4	PCI-E#5 / USB 3.1#5	None
5	PCI-E#6 / USB 3.1#6	None
6	PCI-E#7	None
7	PCI-E#8	None
8	PCI-E#9	BGA SSD PCIe x4 GEN3
9	PCI-E#10	
10	PCI-E#11 / SATA#0	
11	PCI-E#12 / SATA#1a	
12	PCI-E#13	M.2 SSD Debug(Reserve)
13	PCI-E#14	
14	PCI-E#15 / SATA#1b	None
15	PCI-E#16 / SATA#2	Card Reader PCIE GEN2

USB 2.0

USB 2.0 PORT#	DESTINATION
1	USB DCI Debug
2	None
3	BT(Reserve)
4	None
5	FPR
6	None
7	None
8	Type-C_L
9	Type-C_R
10	None

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	WLAN(Reserve)
	CLKOUT_PCIE1	M.2 SSD(Reserve)
	CLKOUT_PCIE2	SSD
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Thunderbolt

	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None

Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

CSI2

CSI2 PORT#	DESTINATION
C/D	None
E	UF
F	None
G/H	None

Symbol Note :

@ : means de-pop

: means Digital Ground

: means Analog Ground

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P003 - Notes List

Size: | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 3 of 101

Centenario POWER BLOCK DIAGRAM

Power Rail

Audio Power Rail

2S2P Battery
51W

Type-C Port-L

Type-C Port-R

PD1
Controller
TPS65987DH

EC
MEC5105

PD2
Controller
TPS65987DH

Buck-boost
Charger
ISL9538B
(NVDC)
Page:83

B+

B+

B+

B+

PCH_PRIM_EN

+1.8VPRIM
TDC 2.56A
Peak Current 3.65A
(NB691)
Page:88

UC22
AOZ1334DI-01
CPU_C10_GATE#
+VCC1P8A

UC25
AOZ1336DI
AUD_PWR_EN
+1.8VS_AUDIO

UC24
AOZ1336DI
RUN_ON_P
+1.8VS

UC23
AOZ1334DI-01
SUS_ON_P
+1.8V_MEM

ALWON_3VALW

+3.3VALW
TDC: 5.1A
Peak Current 7.22A
(NB502)
Page:84

U7
SY6288
ENVDD
+LCDVDD

U31
AOZ1331DI
VCCDSW_EN_GPIO
+3V_PRIM
VCCDSW_EN_GPIO
+3VALW_DSW

U34
AOZ1331DI
WLAN_PWR_EN
+3VS_WLAN
TS_EN_R
+3VS_TS

UC30
AOZ1336DI
RUN_ON_P
+3VS

U51
AOZ1336DI
AUD_PWR_EN
+3VS_AUDIO

U733
AOZ1336DI
SSD_PWR1_EN
+3.3VDX_SSD

UC31
SY6288
SD_PWR_EN
+3VS_CR

UT1
AOZ1336DI
3.3V_TBT_L_EN
+3.3V_TBT_L

UT2
AOZ1336DI
3.3V_TBT_R_EN
+3.3V_TBT_R

Transfer Board

UKBC26
AOZ1336DI
TP_EN
+TRN_3VS_TP

IMVP_VR_ON_EN

VCCIN
TDC 36A
Peak Current 62A
(MP2940A)
Page:91,92,93

+VCC1.05_OUT_FET

UC13
AOZ1334DI-01
VCCST_EN
+VCCST_CPU

+VCC1.05_OUT_FET

UC12
AOZ1334DI-01
VCCSTG_EN
+VCCSTG_CPU

1.8V_PRIM_PG

VCCIN_AUX
TDC 10A
Peak Current 26A
(MP2941)
Page:89,90

+1.1V_MEM

UC27
AOZ1334DI-01
VCC_SFR_OC_EN
+VCC_SFR_OC

0.6V_VDDQ_EN_P

+0.6V_VDDQ (LPDDR4X only)
TDC 1.25A
Peak Current 1.79A
(NB691)
Page:87

1.1V_MEM_EN

+1.1V_MEM
TDC 4A
Peak Current 5.7A
(RT6243B)
Page:86

SSD_PWR3_EN_P

+SSD_PWR3
TDC 1.4A
Peak Current 2A
(NB693)
Page:95

U735
AOZ1336D
SSD_PWR3_EN
+SSD_PWR_3

SSD_PWR2_EN_P

+SSD_PWR2
TDC 1.4A
Peak Current 2A
(NB691)
Page:94

U734
AOZ1336D
SSD_PWR2_EN
+1.8V_1.2V_SSD

Q15
SI3457BDV
EN_INVPWR
+INV_PWR_SRC

ALWON_5VALW

+5VALW
TDC 5A
Peak Current 7.2A
(NB502)
Page:85

U36
AOZ1336DI
AUD_PWR_EN
+5VS_AUDIO

UPD1
TPS65987DH
+5VALWB_L_TBT

UC28
AOZ1336DI
RUN_ON_P
+5VS

U55
SY6288
3.3V_CAM_EN
+CAM_PWR

Middle Board

UMID1
RT9078N
+MID_CAM_PWR
+MID_UF_AVDD_2.8V

UMID2
RT9078N
+MID_CAM_PWR
+MID_UF_DVDD_1.2V

UMID3
RT9078N
+MID_CAM_PWR
+MID_UF_VDD_1.8V

ALWON_5VALWB

+5VALWB
TDC 3.5A
Peak Current 5A
(NB502)
Page:85

U60
AOZ1336DI
RUN_ON_P
+5VBS

UPD2
TPS65987DH
+5VALWB_R_TBT

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	P004 - Power MAP
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				Date: Friday, May 24, 2019	Sheet 4 of 101

Power On Sequence

[AC in]

ITEM	Measure Point			Time
Ta	TBT_VBUS	To	+3V_LDO	
Tb	+3V_LDO	To	+CHG_VIN_20V	
Tc	+CHG_VIN_20V	To	B+	
Td	B+	To	ACAV_IN	
Te	ACAV_IN	To	ALWON	
Tf	ALWON	To	+3VALW	
Tg	ALWON	To	+5VALW (+5VALWB)	
Th	+3VALW	To	ALW_PWRGD_3V_5V	

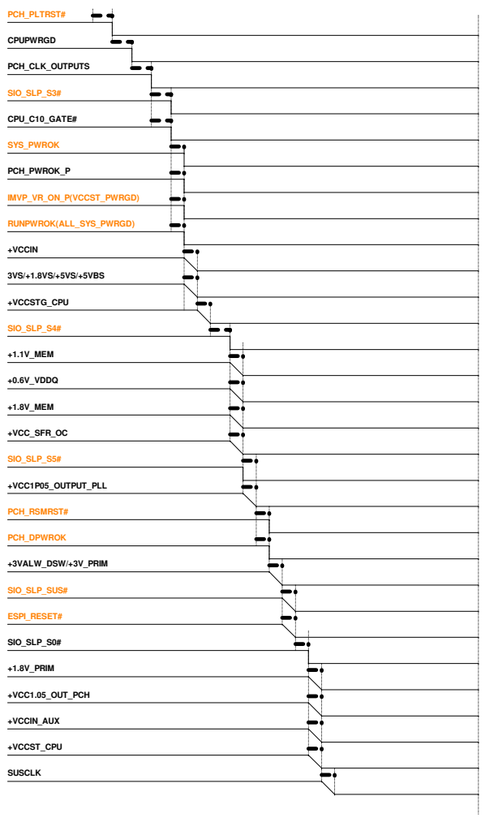
[Battery only, AC absent]

ITEM	Measure Point			Time
Tc	B+	To	POWER_SW_IN#	
Th	POWER_SW_IN#		Low pluse width	
Td	POWER_SW_IN#	To	ALWON	
Te	ALWON	To	+3VALW	
Tf	ALWON	To	+5VALW (+5VALWB)	
Tg	+3VALW	To	ALW_PWRGD_3V_5V	

ITEM	Measure Point			Time
T1	VCCDSW_EN_GPIO	To	+3VALW_DSW/+3V_PRIM	
T2	+3VALW_DSW/+3V_PRIM	To	PCH_DPWROK	
T3	PCH_DPWROK	To	SIO_SLP_SUS#	
T4	SIO_SLP_SUS#	To	+1.8V_PRIM	
T5	+1.8V_PRIM	To	+VCC1.05_OUT_PCH	
T6	+1.8V_PRIM	To	+VCC1.05_OUT_FET	
T7	+VCC1.05_OUT_FET	To	+VCCST_CPU	
T8	+1.8V_PRIM	To	1.8V_PRIM_PG	
T9	1.8V_PRIM_PG	To	+VCCIN_AUX	
T10	+VCCIN_AUX	To	VCCIN_AUX_VR_PG	
T11	VCCIN_AUX_VR_PG	To	PCH_RSMRST#	
T12	PCH_RSMRST#	To	ESPI_RESET#	
T13	ESPI_RESET#	To	AC_PRESENT	
T14	SIO_SLP_S5#	To	SIO_SLP_S4#	
T15	SIO_SLP_S4#	To	SIO_SLP_S3#	
T16	SIO_SLP_S4#	To	CPU_C10_GATE#	
T17	SIO_SLP_S4#	To	SIO_SLP_S0#	
T18	SIO_SLP_S4#	To	RUN_ON_EC	
T19	SIO_SLP_S4#	To	+1.1V_MEM	
T20	SIO_SLP_S4#	To	+0.6V_VDDQ	
T21	SIO_SLP_S4#	To	+1.8V_MEM	
T22	SIO_SLP_S4#	To	+1.8V_MEM	
T23	SIO_SLP_S4#	To	+VCC1P8A	
T24	SIO_SLP_S4#	To	+VCC_SFR_OC	
T25	RUN_ON_EC	To	+3VS	
T26	RUN_ON_EC	To	+1.8VS	
T27	RUN_ON_EC	To	+5VS/+5VBS	
T28	RUN_ON_EC	To	+3.3VDX_SSD	
T29	RUN_ON_EC	To	+SSD_PWR2	
T30	RUN_ON_EC	To	+SSD_PWR3	
T31	+3VS	To	RUNPWROK	
T32	RUNPWROK	To	IMVP_VR_ON_P	
T33	IMVP_VR_ON_P	To	+VCCIN	
T34	+VCCIN	To	PCH_PWROK_P	
T35	PCH_PWROK_P	To	CPUPWRGD	
T36	CPUPWRGD	To	SYS_PWROK	
T37	SYS_PWROK	To	PCH_PLTRST#_EC	

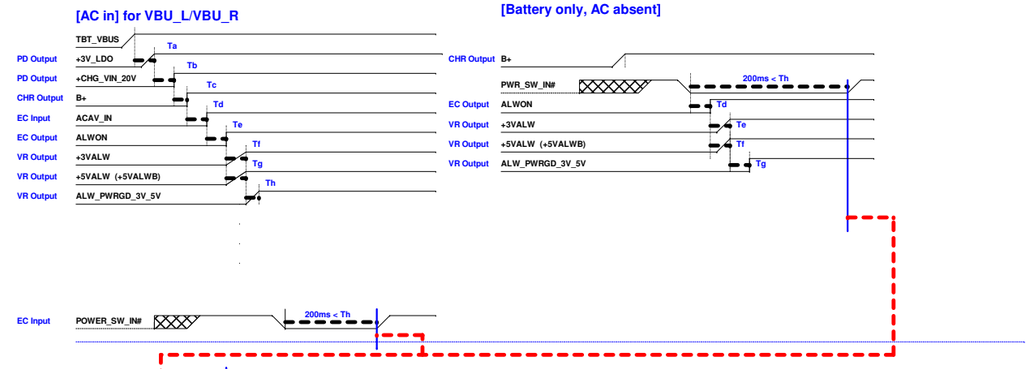
Power Down Sequence

EC pay attention timing

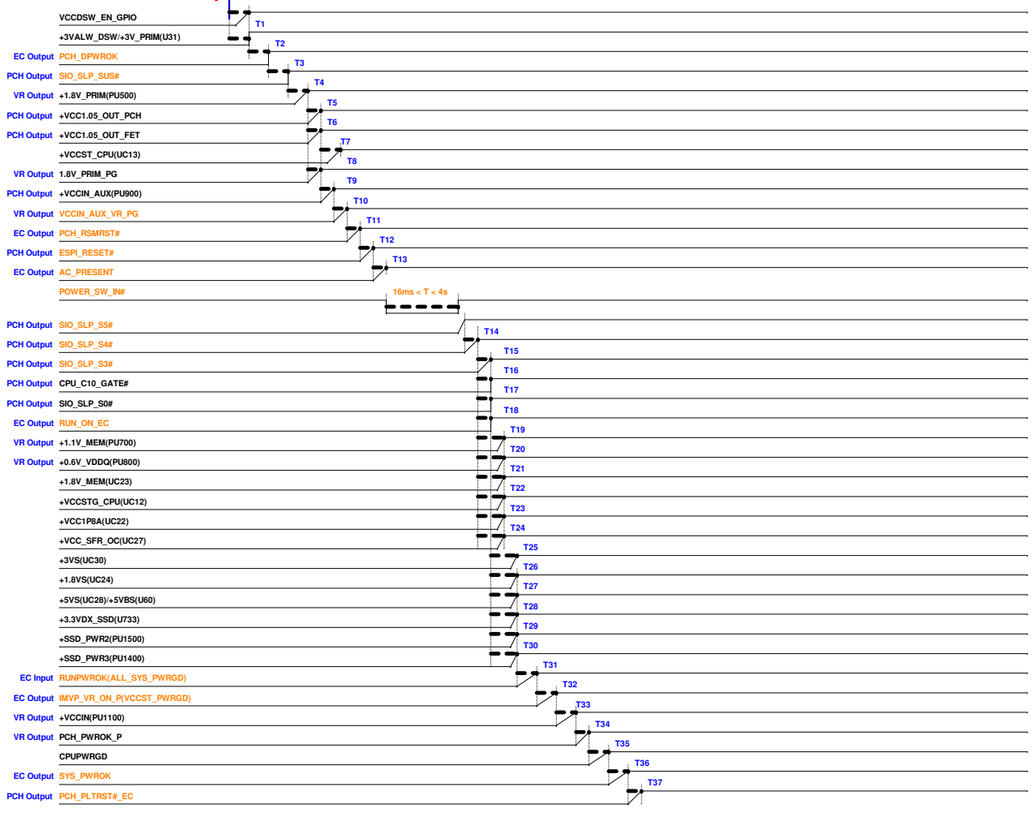


[AC in] for VBU_L/VBU_R

[Battery only, AC absent]



EC pay attention timing



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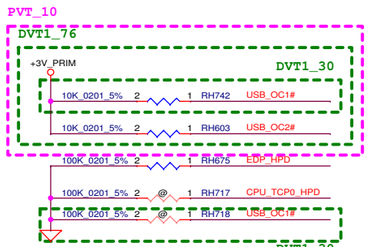
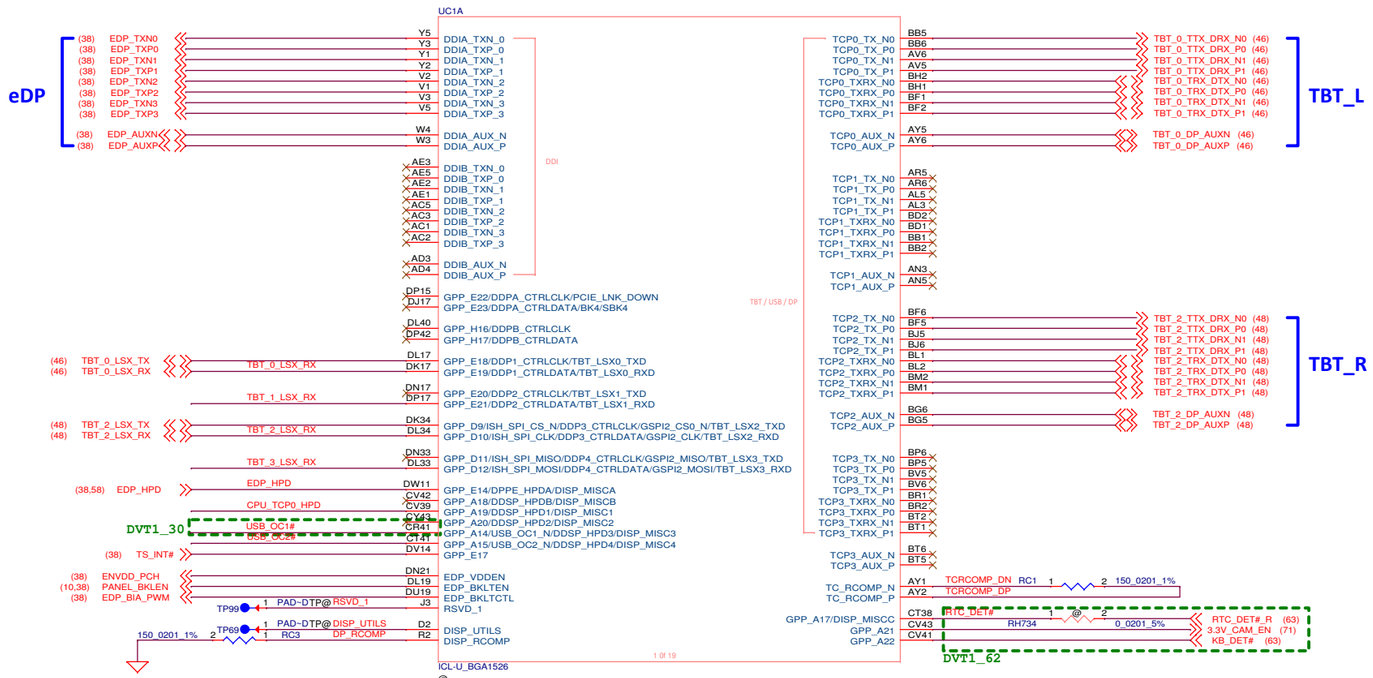
Compal Electronics, Inc.

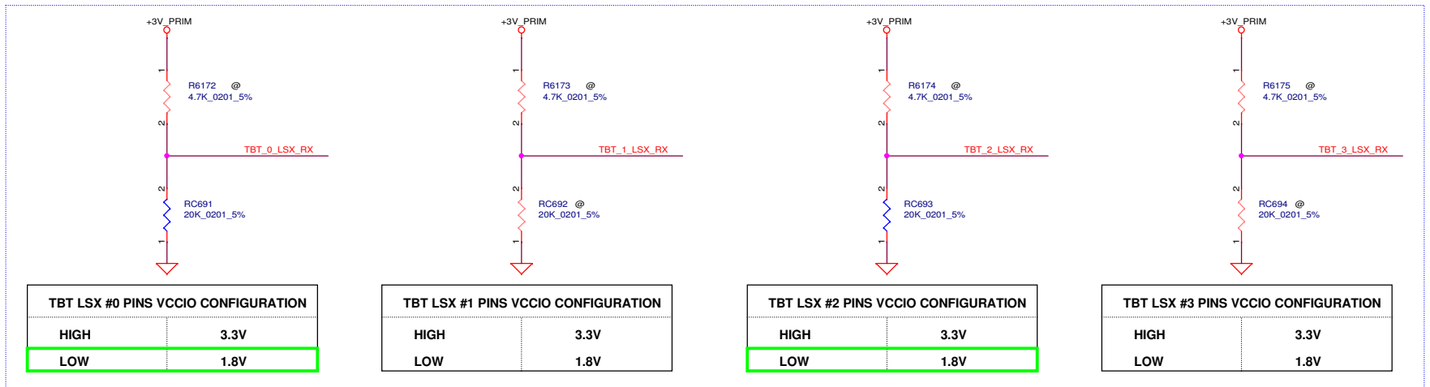
Title: P005 - Power Sequence

Size: A3 | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 5 of 151







TBT LSX #0 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #1 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #2 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

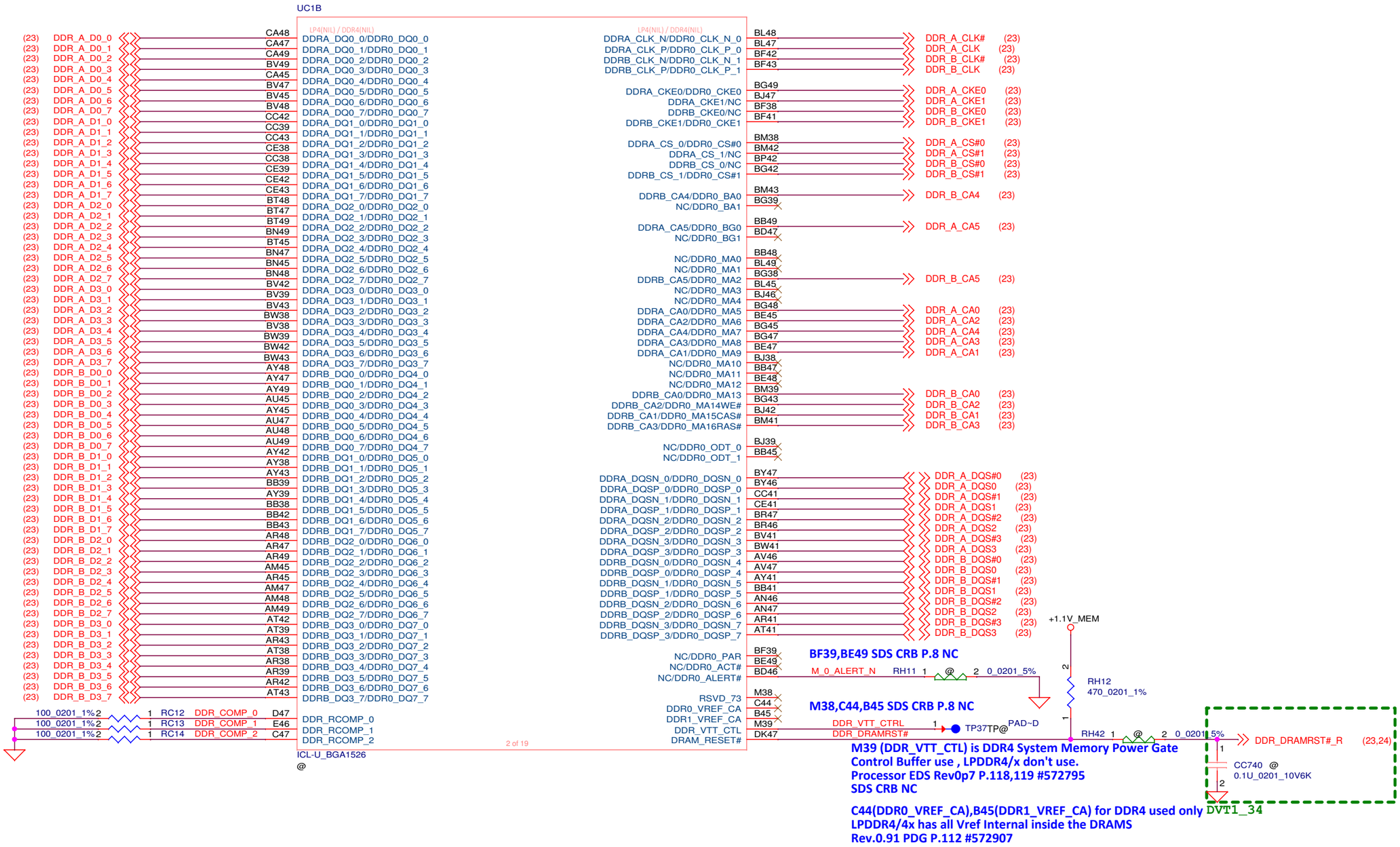
TBT LSX #3 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P006 - ICL-U(1/13)TCSS,EDP
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	6 of 101

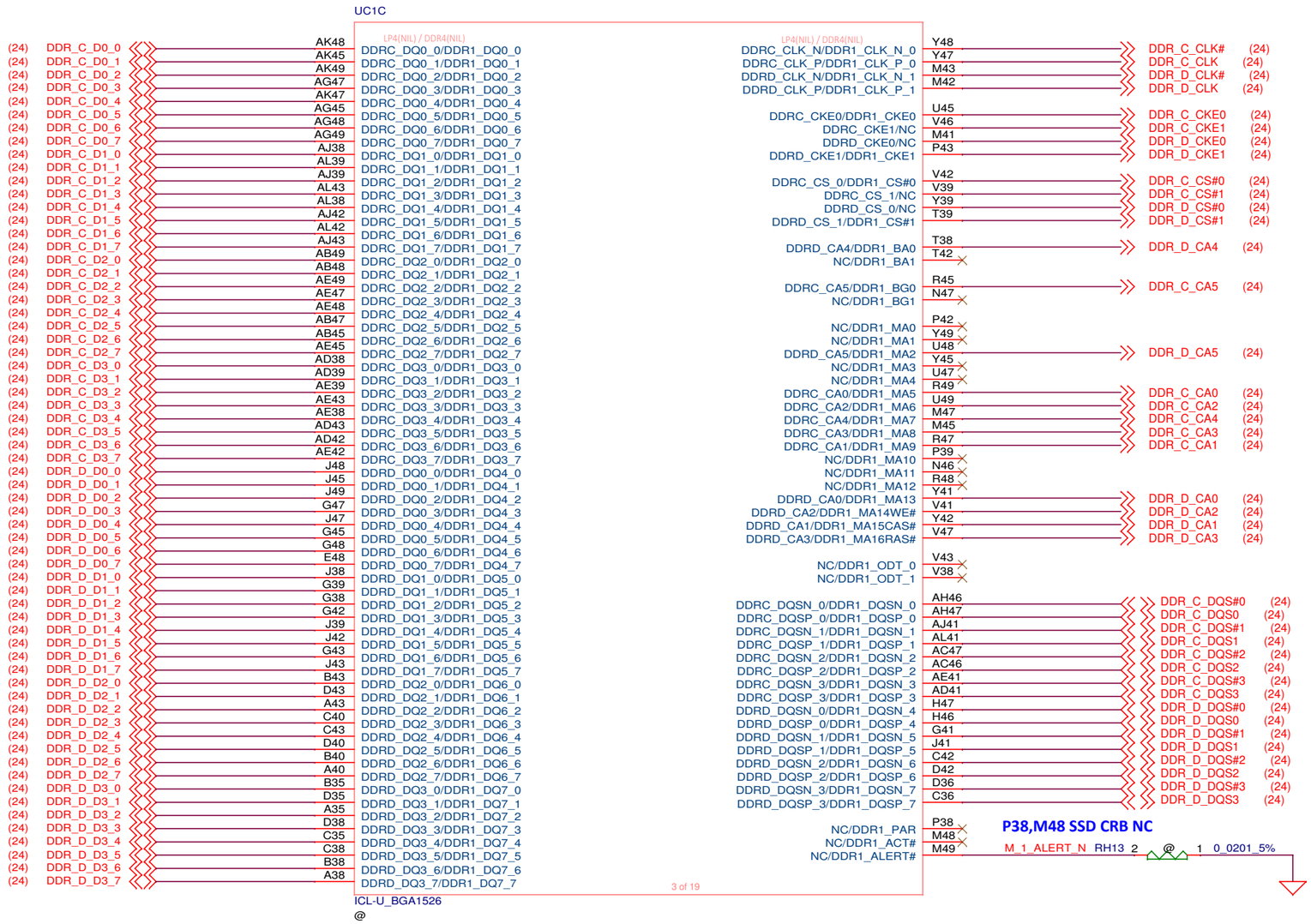
Memory connection follow J72913-201 Rev 01_20181217



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P007 - ICL-U(2/13)LPDDR4/x			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 7 of 101		

Memory connection follow J72913-201 Rev 01_20181217



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P008 - ICL-U(3/13)LPDDR4/x**

Size: | Document Number: **LA-G172P** | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 8 of 101

BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

+V3.3A_1.8A_PCH_SPI

RH643 1 2 100K_0201_5%

PCH_SPI_SI — RH641 1 @ 2 4.7K_0201_5%

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

+V3.3A_1.8A_PCH_SPI

RH141 1 2 100K_0201_5%

PCH_SPI_IO2 — RH142 1 @ 2 4.7K_0201_5%

A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable

+V3.3A_1.8A_PCH_SPI

RH635 1 2 100K_0201_5%

PCH_SPI_IO3 — RH636 1 @ 2 100K_0201_5%

TLS CONFIDENTIALITY

GPP_C2/SMBALERT#(INTERNAL PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

+3V_PRIM

GPP_C2 — RH692 1 2 4.7K_0201_5%

ESPI OR EC LESS

GPP_C5 (Internal 20 K internal Pull Down): SML0ALERT#

0 = Enable eSPI. (Default)

1 = Disable eSPI.

+3V_PRIM

GPP_C5 — RH98 1 @ 2 20K_0201_5%

RH666 1 @ 2 4.7K_0201_5%

---

(66) PCH_SPI_CLK_R — PCH_SPI_CLK_R RH719 1 2 4.99_0201_1% PCH_SPI_CLK — DB42

(66) PCH_SPI_SI_R — PCH_SPI_SI_R RH720 1 2 4.99_0201_1% PCH_SPI_SI — Strap Pin — DD43

(66) PCH_SPI_SO_R — PCH_SPI_SO_R RH721 1 2 4.99_0201_1% PCH_SPI_SO — DF43

PCH_SPI_IO2_R RH722 1 2 4.99_0201_1% PCH_SPI_IO2 — Strap Pin — DF42

PCH_SPI_IO3_R RH723 1 2 4.99_0201_1% PCH_SPI_IO3 — Strap Pin — DD41

PCH_SPI_CS0#_R RH736 1 @ 2 0_0201_5% PCH_SPI_CS0# — DB43

PCH_SPI_CS1#_R RH735 1 @ 2 0_0201_5% PCH_SPI_CS1# — DF41

(66) PCH_SPI_CS2# — PCH_SPI_CS2# — DB41

EVT2_28

DVT1_36

RH687 1 2 100K_0201_5% PCH_SPI_CLK

(79) MIPI60_SPI0_MOSI — 1K_0201_5% 1 2 RH640 MIPI60@ — PCH_SPI_SI

(79) MIPI60_SPI0_IO2 — 1K_0201_5% 1 2 RH634 MIPI60@ — PCH_SPI_IO2

UC1E

SPI0_CLK
SPI0_MOSI
SPI0_MISO
SPI0_IO2
SPI0_IO3
SPI0_CS1#
SPI0_CS2#
SPI0

GPP_B13/SPI1_CLK/BK1/SBK1
GPP_E13/SPI1_MOSI/BK3/SBK3
GPP_E12/SPI1_MISO/BK2/SBK2
GPP_E1/SPI1_IO2
GPP_E2/SPI1_IO3
GPP_E10/SPI1_CS_N/BK0/SBK0
GPP_E8/SATALED#/SPI1_CS1#
SPI1

CL_CLK
CL_DATA
CL_RST#
MLINK

SMBUS: GPP_C0/SMBCLK DK27 — SMB_CLK (79); GPP_C1/SMBDATA DP24 — SMB_DATA (79); GPP_C2/SMBALERT# DL24 — GPP_C2

SML 0: GPP_C3/SML0CLK DK24 — SML0_SMBCLK — SML0_SMBCLK (46,48); GPP_C4/SML0DATA DJ24 — SML0_SMBDATA — SML0_SMBDATA (46,48); GPP_C5/SML0ALERT# DP22 — GPP_C5

SML1: GPP_C6/SML1CLK/SUSWARN_N/SUSPWRDNACK DN22 — SML1_SMBCLK_R; GPP_C7/SML1DATA/SUSACK# DL22 — SML1_SMBDATA_R

eSPI:
GPP_A5/ESPI_CLK CR47 — ESPI_CLK — RC569 2 1 49.9_0201_1%
GPP_A0/ESPI_IO0 CN45 — ESPI_IO0_R — RC336 1 2 10_0201_1%
GPP_A1/ESPI_IO1 CN48 — ESPI_IO1_R — RC367 1 2 10_0201_1%
GPP_A2/ESPI_IO2 CN49 — ESPI_IO2_R — RC368 1 2 10_0201_1%
GPP_A3/ESPI_IO3 CN47 — ESPI_IO3_R — RC369 1 2 10_0201_1%
GPP_A4/ESPI_CS# CT45 — ESPI_CS#
GPP_A6/ESPI_RESET# CR46 — ESPI_RESET#

ESPI_CLK_5105 (58,79); ESPI_IO0 (58,79); ESPI_IO1 (58,79); ESPI_IO2 (58,79); ESPI_IO3 (58,79); ESPI_CS# (58,79); ESPI_RESET# (58,79)

5 of 19

ICL-U_BGA1526

NO support C-Link

MIPI60

BB_L&BB_R (For support Vpro)

BB_L&BB_R
PD_L&PD_R

ESPI 1.8V

SML1_SMBCLK_R RH639 1 @ 2 0_0201_5% — SML1_SMBCLK (42,44,46,48)

SML1_SMBDATA_R RH638 1 @ 2 0_0201_5% — SML1_SMBDATA (42,44,46,48)

+3V_PRIM

SML0_SMBDATA 499_0201_1% RH144
SML0_SMBCLK 499_0201_1% RH143
SML1_SMBCLK_R 1K_0201_5% RH606
SML1_SMBDATA_R 1K_0201_5% RH607
ESPI_CS# 75K_0201_1% RC712
ESPI_RESET# 75K_0201_1% RC711

DVT1_32 DVT1_61

Closed to ROM

SPI_SI_VROM0 RH23 1 2 49.9_0201_1% PCH_SPI_SI_R
SPI_CLK_VROM0 RH24 1 2 49.9_0201_1% PCH_SPI_CLK_R
SPI_SO_VROM0 RH25 1 2 49.9_0201_1% PCH_SPI_SO_R
SPI_IO2_VROM0 RH26 1 2 49.9_0201_1% PCH_SPI_IO2_R
SPI_IO3_VROM0 RH27 1 2 49.9_0201_1% PCH_SPI_IO3_R

Serial Peripheral Interface (SPI) Topology Guidelines

PCH → SPI, TPM, JSPI

NPI pop D20
MP pop RC745

SPI ROM (32MByte)
ROM is Quad SPI

UH8
PCH_SPI_CS0#_R 1 CS# — VCC 8
SPI_SO_VROM0 2 DO — IO3 7 SPI_IO3_VROM0
SPI_IO2_VROM0 3 IO2 — CLK 6 SPI_CLK_VROM0
4 GND — DI 5 SPI_SI_VROM0
ThemalPad 9
W25Q256JVEIQ_WSON8_8X6

+3V_SPI — @ D20 RB751S40T1G_SOD523-2 — +3V_PRIM
0_0402_5% CH35 0.1U_0201_10V6K
2 @ 1 RC745

PVT_03

JSPI1
PCH_SPI_CS1#_R 1
PCH_SPI_SI_R 2
PCH_SPI_SO_R 3
PCH_SPI_CLK_R 4
PCH_SPI_CS0#_R 5
(78) PROM_BIOS_R PCH_SPI_IO3_R 6
+3V_SPI 7 8 9 10
G1 11 G2 12
ACES_50521-01041-P01_10P
CONN@

EVT2_28

DVT1_36

Follow Pebble Creek MLK

PVT_02

UC1J

WLAN--->
(52) CLK_PCIE_N0 — CJ3 CLKOUT_PCIE_N0
(52) CLK_PCIE_P0 — CJ5 CLKOUT_PCIE_P0
RH40 1 @ 2 10K_0201_5% — DK33 GPP_D5/SRCCLKREQ0#
(52) CLKREQ_PCIE#0
DVT1.2_17

Reserved debug SSD-->
(67) CLK_PCIE_N1 — CL1 CLKOUT_PCIE_N1
(67) CLK_PCIE_P1 — CL2 CLKOUT_PCIE_P1
RH727 1 @ 2 10K_0201_5% — DN34 GPP_D6/SRCCLKREQ1#
(67) CLKREQ_PCIE#1
DVT1.2_16

SSD-->
(68) CLK_PCIE_N2 — CL3 CLKOUT_PCIE_N2
(68) CLK_PCIE_P2 — CL5 CLKOUT_PCIE_P2
RH41 1 @ 2 10K_0201_5% — DP34 GPP_D7/SRCCLKREQ2#
(68) CLKREQ_PCIE#2
DVT1.2_02

CK3 CLKOUT_PCIE_N3
CK4 CLKOUT_PCIE_P3
DP36 GPP_D8/SRCCLKREQ3#

Card Reader--->
(70) CLK_PCIE_N4 — CJ2 CLKOUT_PCIE_N4
(70) CLK_PCIE_P4 — CJ1 CLKOUT_PCIE_P4
RH39 1 2 10K_0201_5% — DN40 GPP_H10/SRCCLKREQ4#
(70) CLKREQ_PCIE#4

CLKOUT_PCIE_N5 CF5
CLKOUT_PCIE_P5 CF3
GPP_H11/SRCCLKREQ5# DP40

RTC: RTCX1 DL48 — PCH_RTCX1; RTCX2 DL49 — PCH_RTCX2
RTCRST# DT47 — PCH_RTCRST# — PCH_RTCRST# (63,79)
SRTCRST# DK46 — SRTCRST#
GPD8/SUSCLK DF49 — SUSCLK — SUSCLK (52,68)
XTAL: XTAL_IN DW8 — XTAL_38P4M_IN_CPU — RH14 1 2 0_0201_5% — XTAL_38P4M_IN
XTAL_OUT DU8 — XTAL_38P4M_OUT_CPU — RH15 1 2 0_0201_5% — XTAL_38P4M_OUT
XCLK_BIASREF DU6 — CLK_BIASREF — RH475 1 2 60.4_0201_1%

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ICL-U_BGA1526

SUSCLK — CH49 @EMI@ 0.1U_0201_10V6K

+RTCVCC_R
CH47 1U_0201_6.3V6K
RH573 20K_0201_5% — PCH_RTCRST#
RH572 20K_0201_5% — SRTCRST#
CH46 1U_0201_6.3V6K

PDG_An RC delay circuit with a time delay in the range of 18~25 ms should be provided. The circuit should be connected to VCCRTC.

XTAL_38P4M_IN
XTAL_38P4M_OUT — RH17 1 2 200K_0201_1%
YH1 1 2 3 4 38.4MHZ_10PF_8Y38420005
CH10 10P_0201_50V8J
CH11 10P_0201_50V8J

EVT1_30

Intel SPEC :
CL = Specified Crystal Capacitive Load = 10 pF
Series Resistance < or = 30 Ω
Frequency Tolerance < or 100 PPM
Aging ±3 PPM

PCH_RTCX2
PCH_RTCX1 — RH16 1 2 10M_0201_1%
RH637 0_0201_5%
YC1 1 2 PCH_RTCX2_R
32.768KHZ_12.5PF_9H03200042
CRB XTAL ESR = 50K MAX
CH12 15P_0201_50V8J
CH13 15P_0201_50V8J

DVT1_06 DVT1_79

EMI Request

PCH_SPI_CLK
RC734 @EMI@ 33_0201_5%
CC659 @EMI@ 33P_0201_50V8J

RF Request

SMB_CLK CC655 @RF@ 1 2 33P_0201_50V8J
SML0_SMBCLK CC656 @RF@ 1 2 33P_0201_50V8J
SML1_SMBCLK_R CC657 @RF@ 1 2 33P_0201_50V8J
ESPI_CLK_5105 CC658 @RF@ 1 2 33P_0201_50V8J

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P009 - ICL-U(4/13)SPI,SMB,ESPI**

Size: — Document Number: **LA-G172P** — Rev: 1.0 (A00)

Date: Friday, May 24, 2019 — Sheet 9 of 101

NO REBOOT

GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

1 = NO REBOOT

CPUNSSC CLOCK FREQ

GPP_B23 (Internal 20 K Pull Down)

0 = 38.4 MHz clock (direct from crystal) (default)

1 = 19.2 MHz clock (from internal divider)

TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

EVT2_28 / EVT2_05 / EVT1_34 / EVT1_15

UC1F — ICL-U_BGA1526

For TS lid open reserved

DVT1.2_18 / DVT1.2_10

TS / TP / Reserved / UFCAM

CPU I3/I5/I7 Option for different thermal table

Pin Name	I3	I5	I7
CPU_ID_0	0	0	1
CPU_ID_1	0	1	0

EC

2nd Accelerometer

ALS,Ecompass,Main Accelerometer on SDB.
Ecompass,Main Accelerometer on DB.

ISH_GP0 for Main Accelerometer (Sensor Board)INT1#
ISH_GP1 for 2nd Accelerometer (MB)
ISH_GP2 for Main Accelerometer (Sensor Board)INT2#
ISH_GP3 for NB_MODE
ISH_GP4 for ISH_GP4# (ON TABLE)
ISH_GP5 for NB_LID#
ISH_GP6 for TAB_LID#
ISH_GP7 for ALS_ALERT#

DVT1.2_11 / EVT2_32 / DVT1_82

UC1G — ICL-U_BGA1526

EVT2_06 / EVT2_43 / EVT1_23

Reserved for debug

SPCE p.30 PU or PD 100K~10K
PDG define only JFP need to PD 10K.

DVT1_59 / DVT1_31 / DVT_08

Intel DMIC for WOV reserved

HDA for AUDIO

EVT1_36

FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)

RF Request. Place near CPU side

EVT2_09

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P010 - ICL-U(5/13)HDA,I2C,ISH*

Size: | Document Number: *LA-G172P* | Rev: 1.0 (A00)

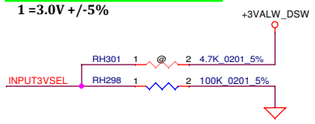
Date: Friday, May 24, 2019 | Sheet 10 of 101

3V SELECT STRAP

INPUT3VSEL

0 = 3.3V +/-5%

1 =3.0V +/-5%

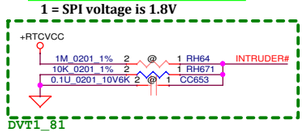


STRAP FOR SPI 1.8V/3.3V SEL

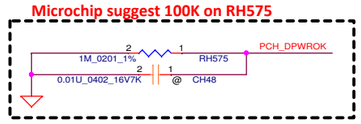
INTRUDER#

0 = SPI voltage is 3.3V

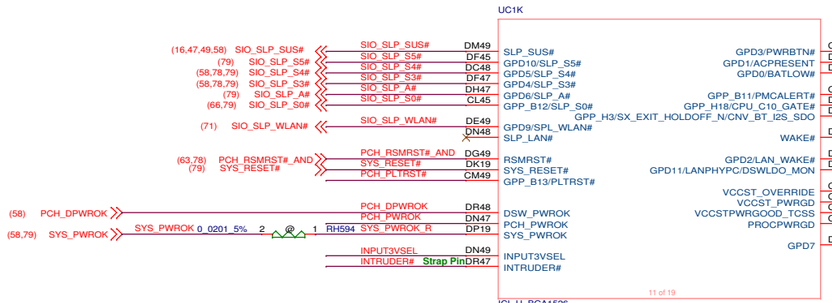
1 = SPI voltage is 1.8V

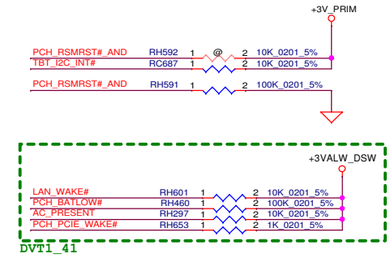


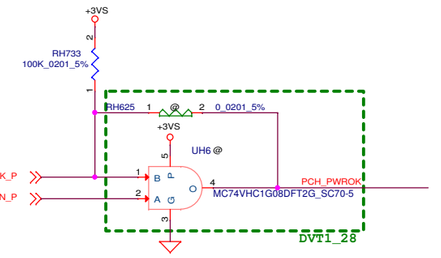
Microchip suggest 100K on RH575

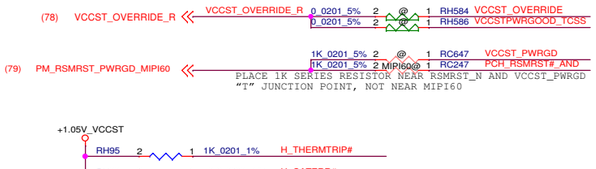


UC1K

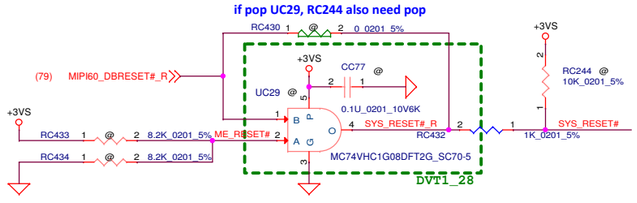


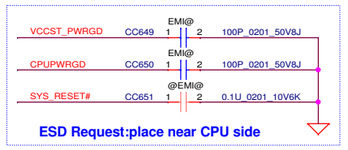




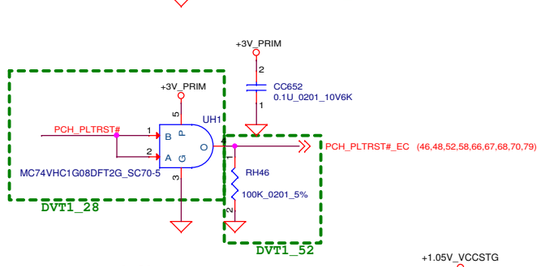


if pop UC29, RC244 also need pop

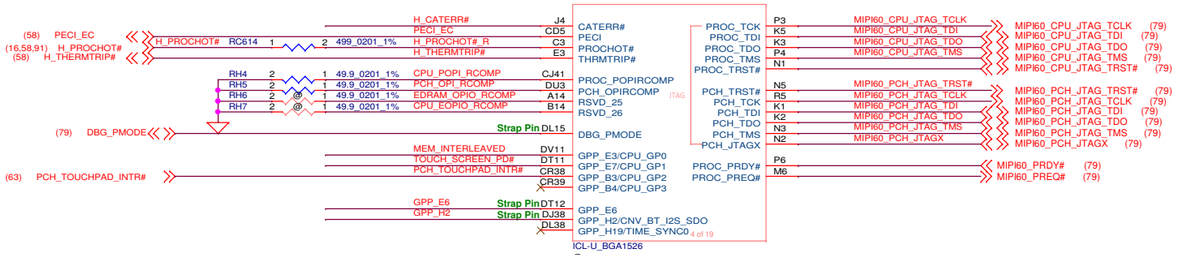


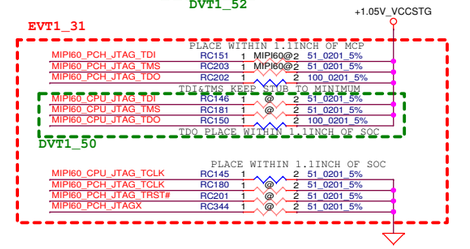


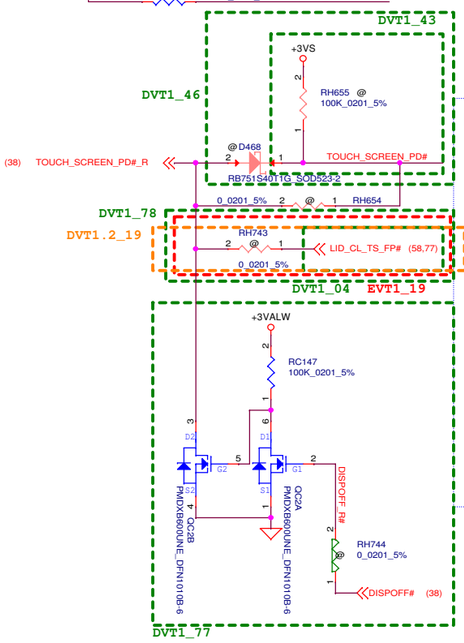
ESD Request:place near CPU side



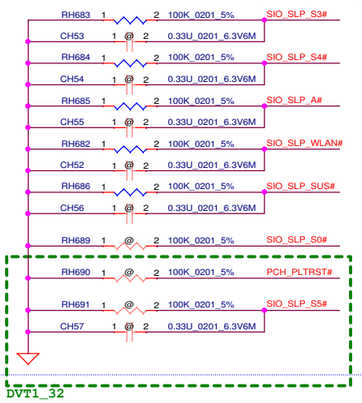
UC1D



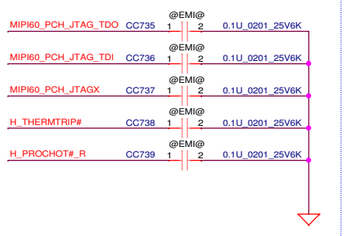




PCH GLITCH ISSUE MITIGATION(PDG p.306)



EMI request,Place near CPU side.

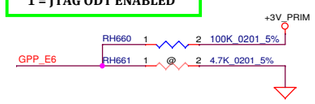


JTAG ODT DISABLE

GPP_E6

0 = JTAG ODT DISABLED

1 = JTAG ODT ENABLED

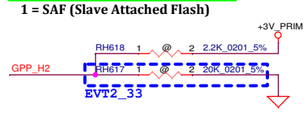


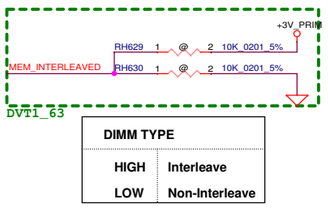
MAF/SAF STRAP(eSPI Flash Sharing Mode)

GPP_H2/CNV_BT_I2S_SDI(INTERNAL PD 20K)

0 = MAF (Master Attached Flash)

1 = SAF (Slave Attached Flash)

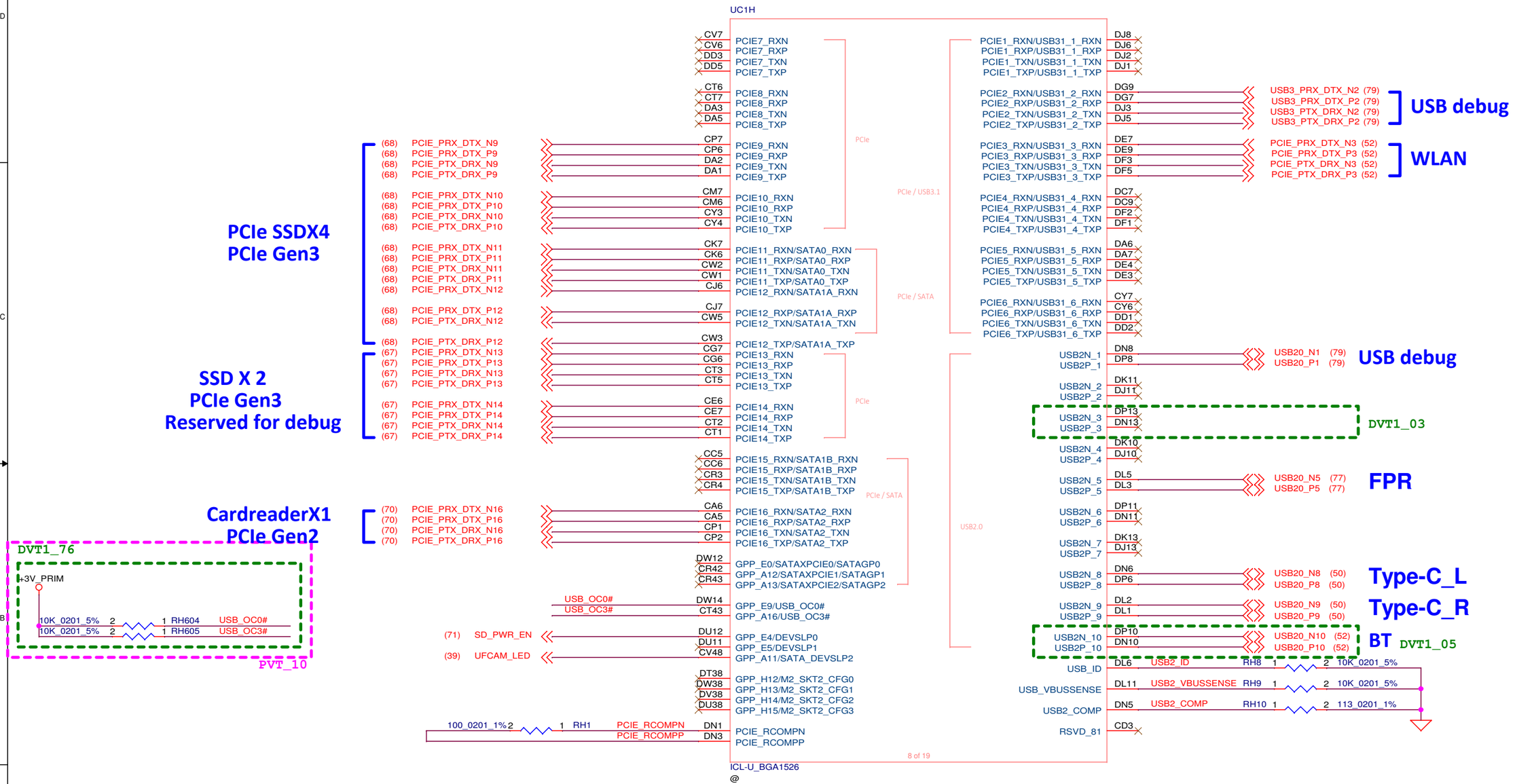




DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P011 - ICL-U(6/13)GPIO		
Size	Document Number LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 11 of 101		



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P012 - ICL-U(7/13)PCIE,USB			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 12 of 101		

EVT1_14

UF CAMERA

(39) MCSI_E_CLKN
(39) MCSI_E_CLKP
(39) MCSI_E_DN0
(39) MCSI_E_DP0

DVT1_11

MCSI_E_CLKN
MCSI_E_CLKP
MCSI_E_DN0
MCSI_E_DP0

UC1I

D12 CSI_E_CLK_N
C12 CSI_E_CLK_P
B12 CSI_E_DN_0
A12 CSI_E_DP_0
G13 CSI_E_DN_1
F13 CSI_E_DP_1

K10 CSI_F_CLK_N
L10 CSI_F_CLK_P
L8 CSI_F_DN_0
M8 CSI_F_DP_0
M11 CSI_F_DN_1
L11 CSI_F_DP_1

D9 CSI_D_CLK_N
C9 CSI_D_CLK_P
A7 CSI_D_DN_0
B7 CSI_D_DP_0
B9 CSI_D_DN_1
A9 CSI_D_DP_1
D7 CSI_D_DN_2/CSI_C_DN_0
C7 CSI_D_DP_2/CSI_C_DP_0
D8 CSI_D_DN_3/CSI_C_CLK_N
C8 CSI_D_DP_3/CSI_C_CLK_P

CSI2

G11 CSI_H_CLK_N
J11 CSI_H_CLK_P
F6 CSI_H_DN_0
G6 CSI_H_DP_0
G10 CSI_H_DN_1
F10 CSI_H_DP_1
G8 CSI_H_DN_2/CSI_G_DN_0
J8 CSI_H_DP_2/CSI_G_DP_0
K6 CSI_H_DN_3/CSI_G_CLK_N
L6 CSI_H_DP_3/CSI_G_CLK_P

100_0201_1% 2 — 1 RC8 — CSI_RCOMP

B4 CSI_RCOMP

(42,44,46,48) RT_FORCE_PWR
(39) UFCAM_MCLK

DT34 GPP_D4/IMGCLKOUT0
DP38 GPP_H20/IMGCLKOUT1
DK36 GPP_H21/IMGCLKOUT2
DL36 GPP_H22/IMGCLKOUT3
DN38 GPP_H23/IMGCLKOUT4

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ICL-U_BGA1526

@

eMMC

GPP_F8/EMMC_DATA0 DP27 MEM_CONFIG0
GPP_F9/EMMC_DATA1 DU30 MEM_CONFIG1
GPP_F10/EMMC_DATA2 DT30 MEM_CONFIG2
GPP_F11/EMMC_DATA3 DT29 MEM_CONFIG3
GPP_F12/EMMC_DATA4 DV30 MEM_CONFIG4
GPP_F13/EMMC_DATA5 DU29
GPP_F14/EMMC_DATA6 DW30
GPP_F15/EMMC_DATA7 DW29
GPP_F7/EMMC_CMD DV28
GPP_F16/EMMC_RCLK DW28
GPP_F17/EMMC_CLK DN27
GPP_F18/EMMC_RESET# DT28
EMMC_RCOMP DU28

EMMC_RCOMP — RC17 1 — 2 200_0201_1%

CNVi

CNV_WT_D0N DV45
CNV_WT_D0P DU45
CNV_WT_D1N DU44
CNV_WT_D1P DT44
CNV_WT_CLKN DL42
CNV_WT_CLKP DK42

CNV_PTX_DRX_N0 (52)
CNV_PTX_DRX_P0 (52)
CNV_PTX_DRX_N1 (52)
CNV_PTX_DRX_P1 (52)
CLK_CNV_PTX_DRX_N (52)
CLK_CNV_PTX_DRX_P (52)

CNV_WR_D0N DP44
CNV_WR_D0P DN44
CNV_WR_D1N DG42
CNV_WR_D1P DG44
CNV_WR_CLKN DK44
CNV_WR_CLKP DJ44

CNV_PRX_DTX_N0 (52)
CNV_PRX_DTX_P0 (52)
CNV_PRX_DTX_N1 (52)
CNV_PRX_DTX_P1 (52)
CLK_CNV_PRX_DTX_N (52)
CLK_CNV_PRX_DTX_P (52)

CNV_WT_RCOMP — RC15 1 — 2 150_0201_1%

DT45 CNV_WT_RCOMP

DL29 CNV_BRI_PRX_DTX

GPP_F1/CNV_BRI_RSP/UART0_RXD DP31 Strap Pin CNV_RGI_PTX_DRX RC503 1 — 2 22_0201_1%
GPP_F2/CNV_RGI_DT/UART0_TXD DL31 Strap Pin CNV_BRI_PTX_DRX RC504 1 — 2 22_0201_1%
GPP_F0/CNV_BRI_DT/UART0_RTS# DN29 CNV_RGI_PRX_DTX

CNV_BRI_PRX_DTX (52)
CNV_RGI_PTX_R_DRX (52)
CNV_BRI_PTX_R_DRX (52)
CNV_RGI_PRX_DTX (52)

GPP_F4/CNV_RF_RESET# DJ29 GPP_F4 2 — @ — 1 RC746
GPP_F6/CNV_PA_BLANKING DP29 0_0201_5% GPP_F19
GPP_F19/A4WP_PRESENT DL27 GPP_F19
GPP_F5/MODEM_CLKREQ DK29 GPP_F5

DVT2_02

EVT1_15

DVT1_54

+1.8V_PRIM

CNV_BRI_PRX_DTX RH724 1 — @ — 2 20K_0201_5%
CNV_RGI_PRX_DTX RH725 1 — @ — 2 20K_0201_5%

GPP_F19 RH749 1 — 2 75K_0201_5%

DVT2_02

For EA MIPI signal measure use
Need to close CPU

DVT1_11

MCSI_E_CLKP — 2 — @ — 1 — MCSI_E_CLKN
MCSI_E_DP0 — 0_0201_5% 2 — @ — 1 RC748
MCSI_E_DN0 — 0_0201_5% 2 — @ — 1 RC749
0_0201_5% RC750

Memory Type Configuration Strap pin

+1.8V_PRIM

RH612 1 — @ — 2 10K_0201_5% MEM_CONFIG0 RH129 1 — @ — 2 10K_0201_5%
RH613 1 — @ — 2 10K_0201_5% MEM_CONFIG1 RH139 1 — @ — 2 10K_0201_5%
RH614 1 — @ — 2 10K_0201_5% MEM_CONFIG2 RH145 1 — @ — 2 10K_0201_5%
RH615 1 — @ — 2 10K_0201_5% MEM_CONFIG3 RH185 1 — @ — 2 10K_0201_5%
RH616 1 — @ — 2 10K_0201_5% MEM_CONFIG4 RH665 1 — @ — 2 10K_0201_5%

Pin Name	Micron 8GB SA0000BX51L	Micron 16GB SA0000BX61L	Micron 32GB SA0000BX71L	Hynix 8GB SA0000BYX1L	Hynix 16GB SA0000AW2YL (EOL and NO SUPPORT)	Hynix 32GB SA0000C7V1L 3733	Samsung 8GB SA0000C6K1L	Samsung 16GB SA0000AU40L (EOL and NO SUPPORT)	Samsung 32GB SA0000CGN1L	Samsung 16GB SA0000C6L1L NEW	Hynix 16GB SA0000BYW1L NEW	Samsung 4GB SA0000AV71L	Micron 4GB SA0000BWF0L (Micron 4GB EOL)	Hynix 4GB SA0000AD11L	Hynix 32GB SA0000BWU1L P-RTS(4266)
MEM_CONFIG0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
MEM_CONFIG2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
MEM_CONFIG3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Compal Electronics, Inc.

Title: P013 - ICL-U(8/13)CSI,CNVi,EMMC

Size: Document Number: LA-G172P Rev: 1.0 (A0)

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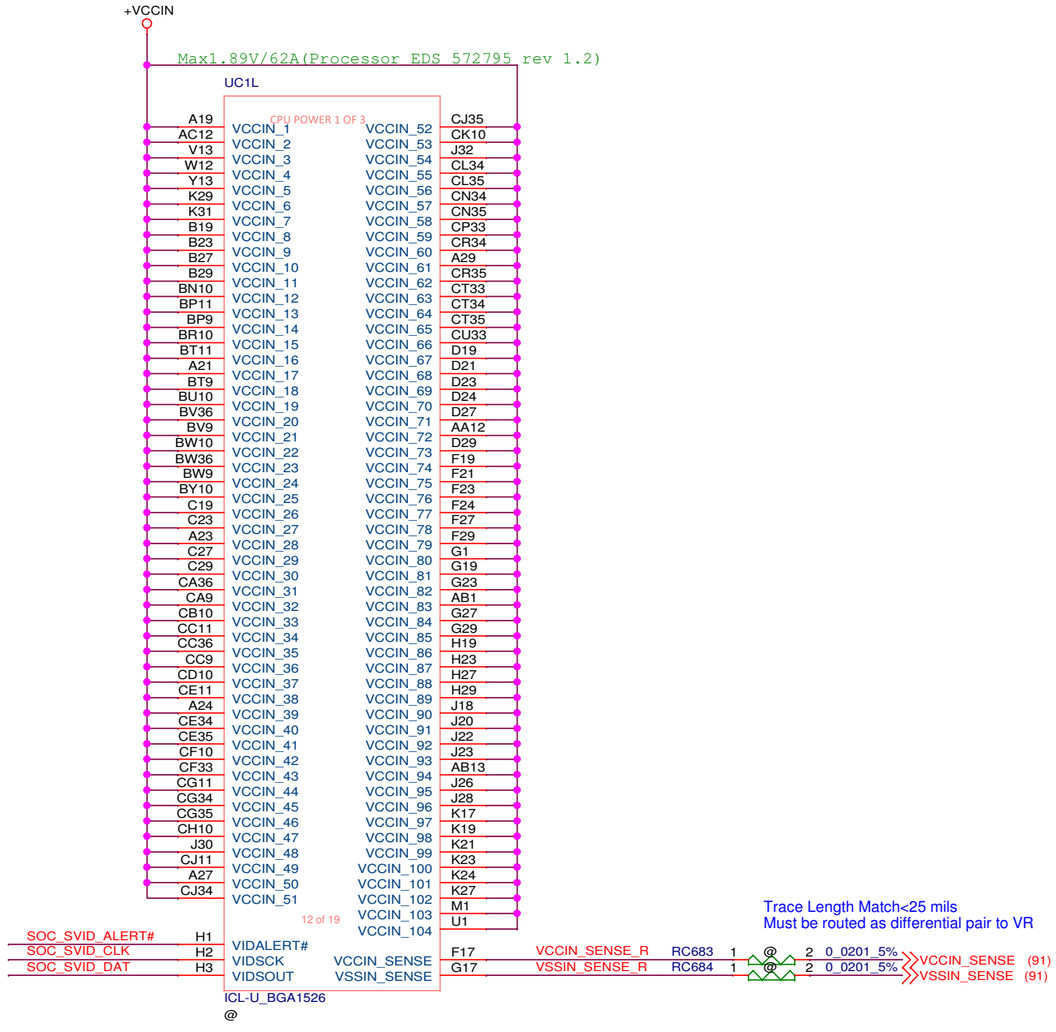
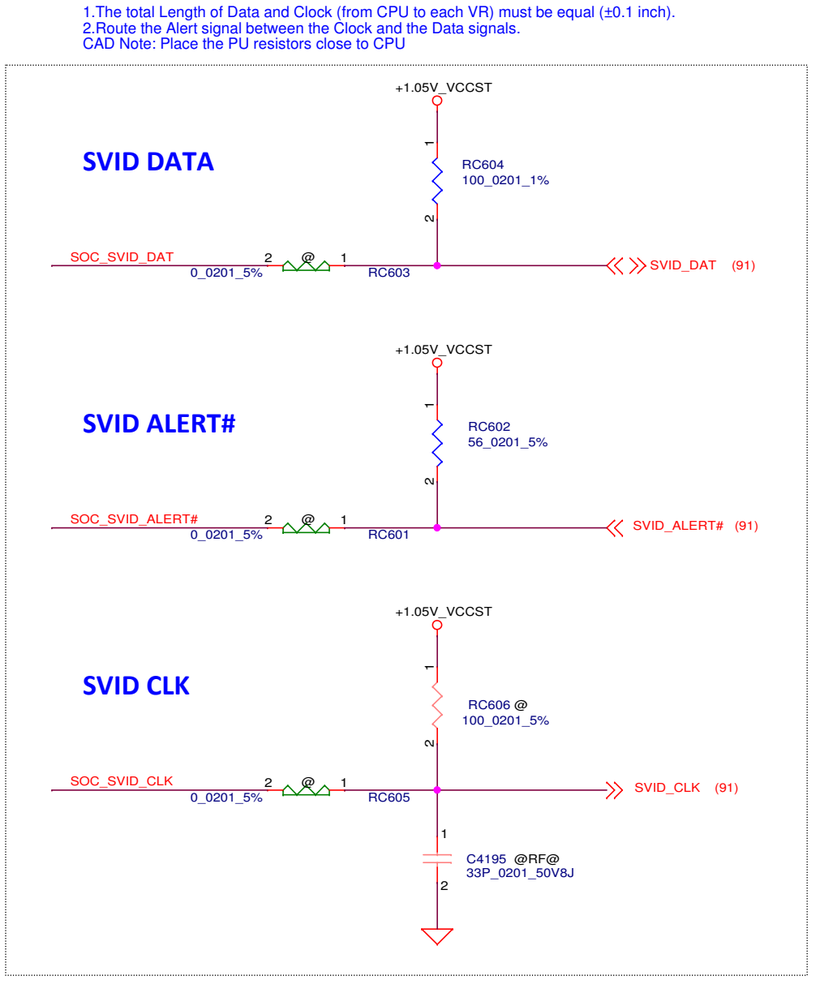
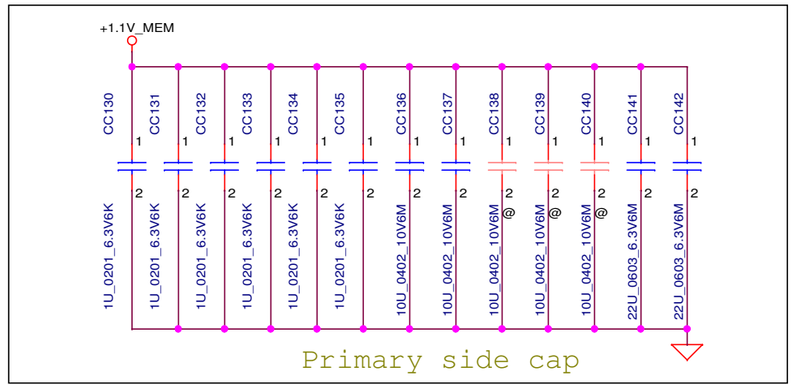


1.The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU

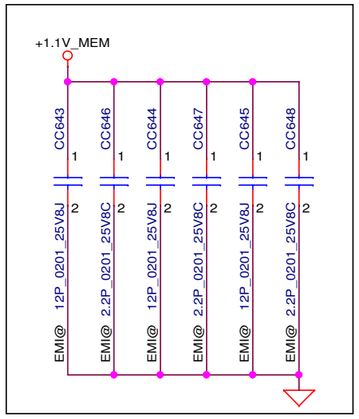


Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

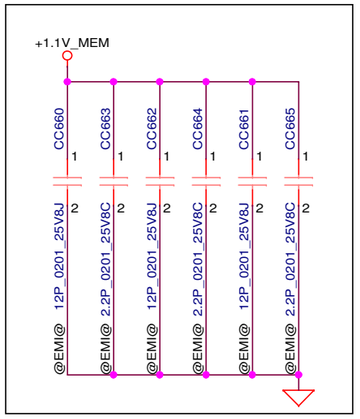
Compal Electronics, Inc.			
Title	P014 - ICL-U(9/13)CPU PWR,SVID		
Size	Document Number LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 14 of 101		

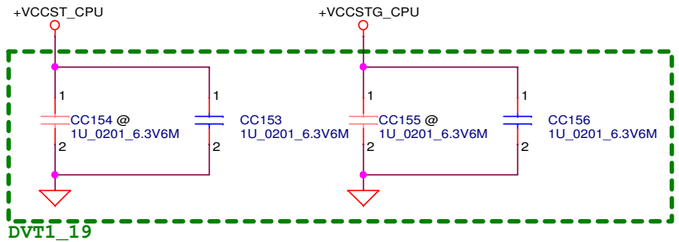


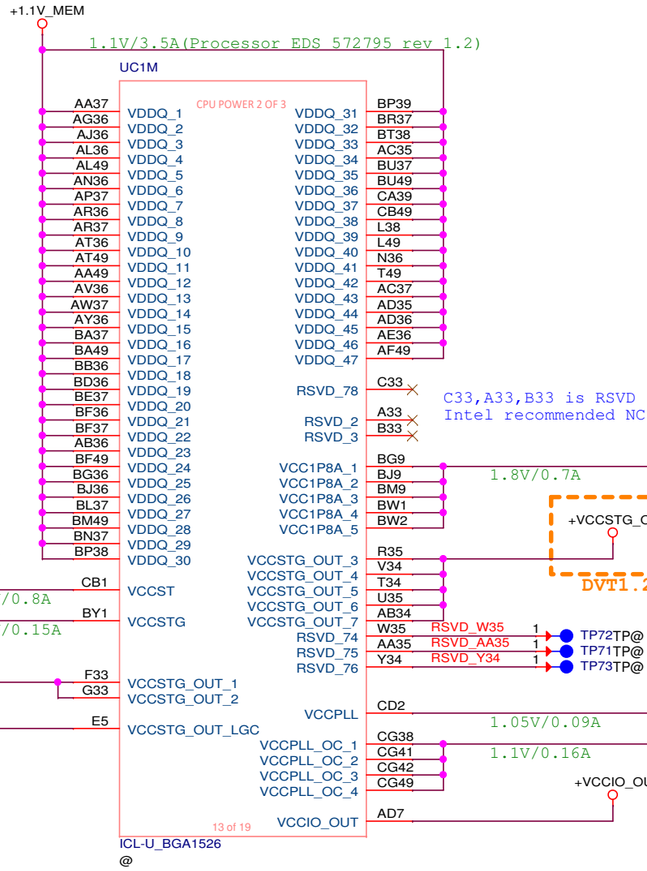
Follow PDG rev1.1 P.545

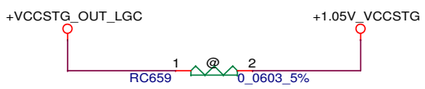


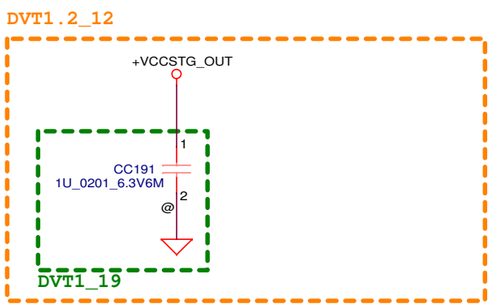
EMC CAPS
PLACE <160mil FROM SOC VDDQ,
WITH EACH PAIR <470mil APART



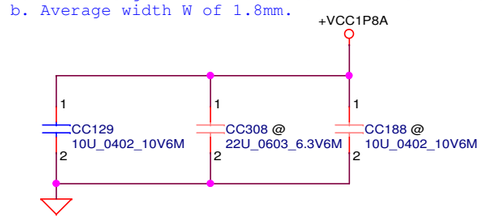


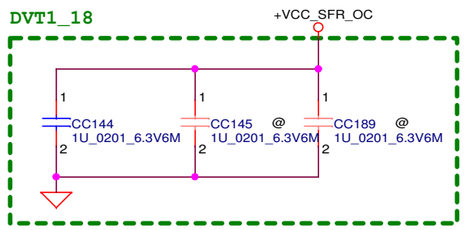


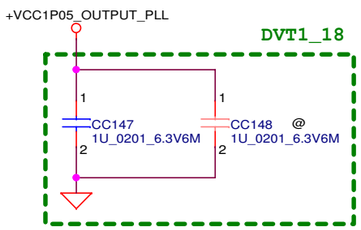




VCC1P8A shape from VR to VCC1P8A pins should have:
a. total length L of < 22mm between VR and BGA.
b. Average width W of 1.8mm.







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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P015 - ICL-U(10/13)CPU PWR**

Size | Document Number: **LA-G172P** | Rev: 1.0 (A00)

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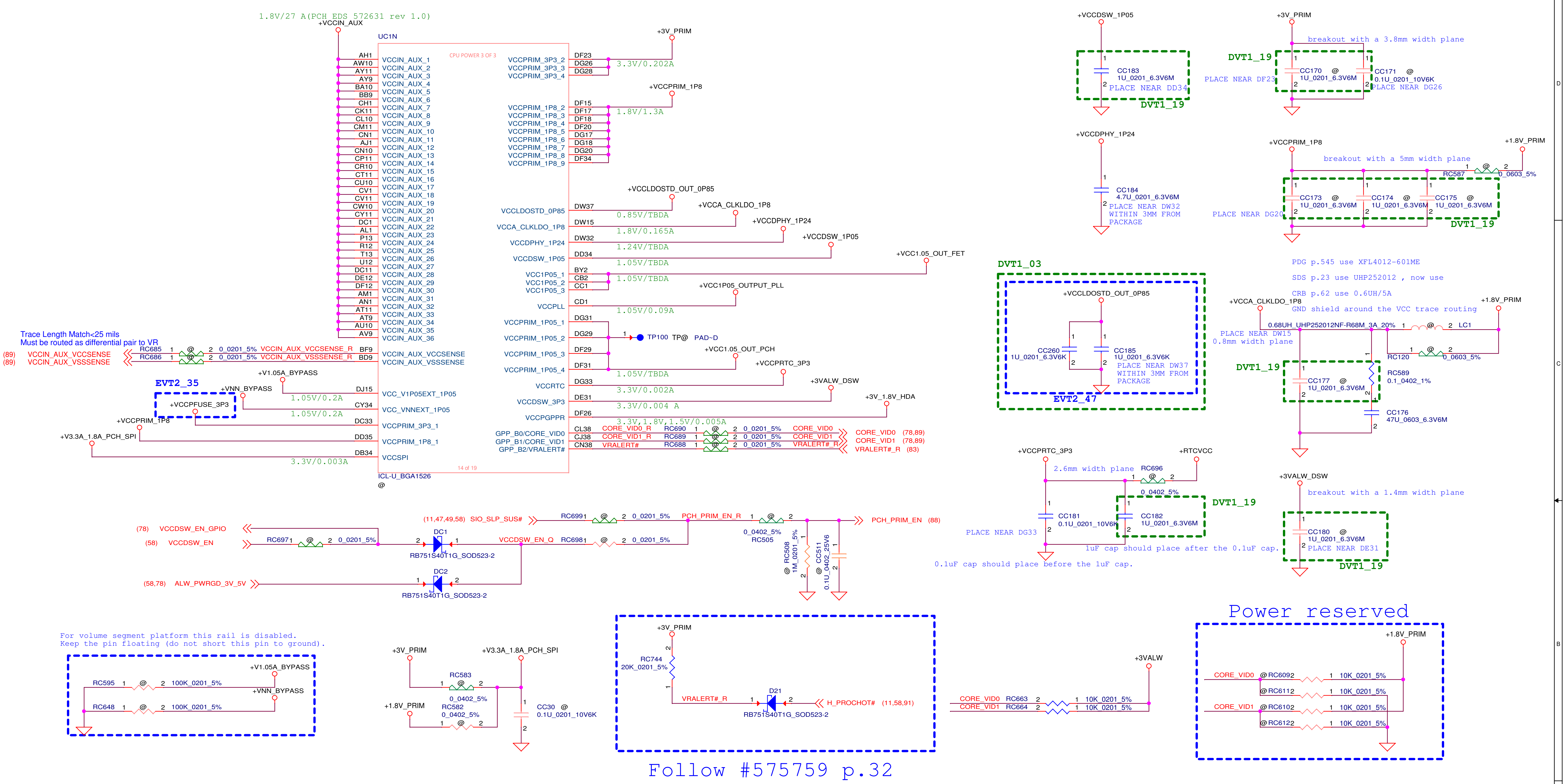

1.8V/27 A(PCH EDS 572631 rev 1.0)
+VCCIN_AUX
UC1N
CPU POWER 3 OF 3
ICL-U_BGA1526
Trace Length Match<25 mils
Must be routed as differential pair to VR
VCCIN_AUX_VCCSENSE
VCCIN_AUX_VSSSENSE
3.3V/0.202A
1.8V/1.3A
0.85V/TBDA
1.8V/0.165A
1.24V/TBDA
1.05V/TBDA
1.05V/0.09A
1.05V/0.2A
3.3V/0.002A
3.3V/0.004 A
3.3V,1.8V,1.5V/0.005A
3.3V/0.003A
EVT2_35
DVT1_19
DVT1_03
EVT2_47
PLACE NEAR DD34
PLACE NEAR DF23
PLACE NEAR DG26
breakout with a 3.8mm width plane
breakout with a 5mm width plane
PLACE NEAR DW32 WITHIN 3MM FROM PACKAGE
PLACE NEAR DG20
PDG p.545 use XFL4012-601ME
SDS p.23 use UHP252012 , now use
CRB p.62 use 0.6UH/5A
GND shield around the VCC trace routing
PLACE NEAR DW15
0.8mm width plane
PLACE NEAR DW37 WITHIN 3MM FROM PACKAGE
2.6mm width plane
PLACE NEAR DG33
1uF cap should place after the 0.1uF cap.
0.1uF cap should place before the 1uF cap.
breakout with a 1.4mm width plane
PLACE NEAR DE31
SIO_SLP_SUS#
PCH_PRIM_EN
VCCDSW_EN_GPIO
VCCDSW_EN
ALW_PWRGD_3V_5V
RB751S40T1G_SOD523-2
For volume segment platform this rail is disabled.
Keep the pin floating (do not short this pin to ground).
H_PROCHOT#
Follow #575759 p.32
Power reserved

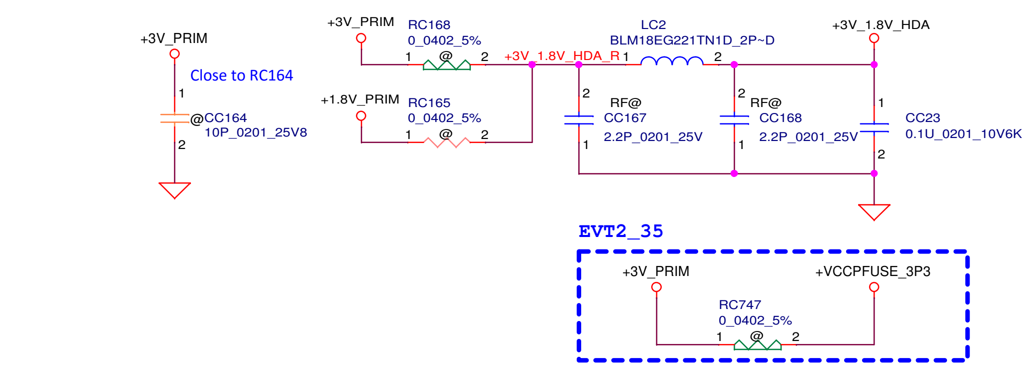


Table 11-1. VCCIN_AUX VID

VID[1] Pin State	VID[0] Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.65	Full Current, ICL-Y
1	1	1.8	Initial boot for ICL-U/Y Full current, ICL-U

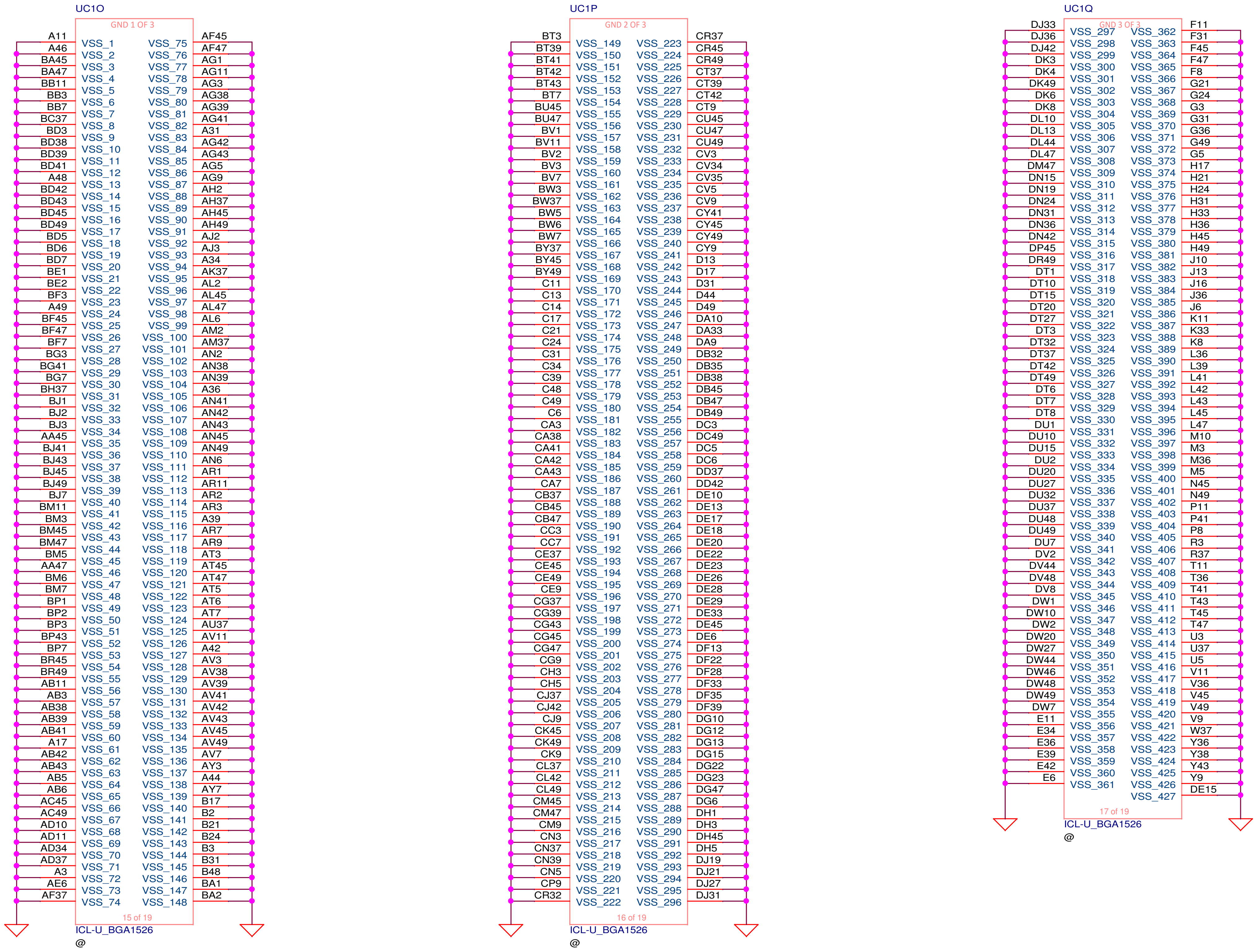
Note: Logic "0"is 0V and Logic "1" is 1.8V based logic, but the VID pins must be 3.3V tolerant as well.

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

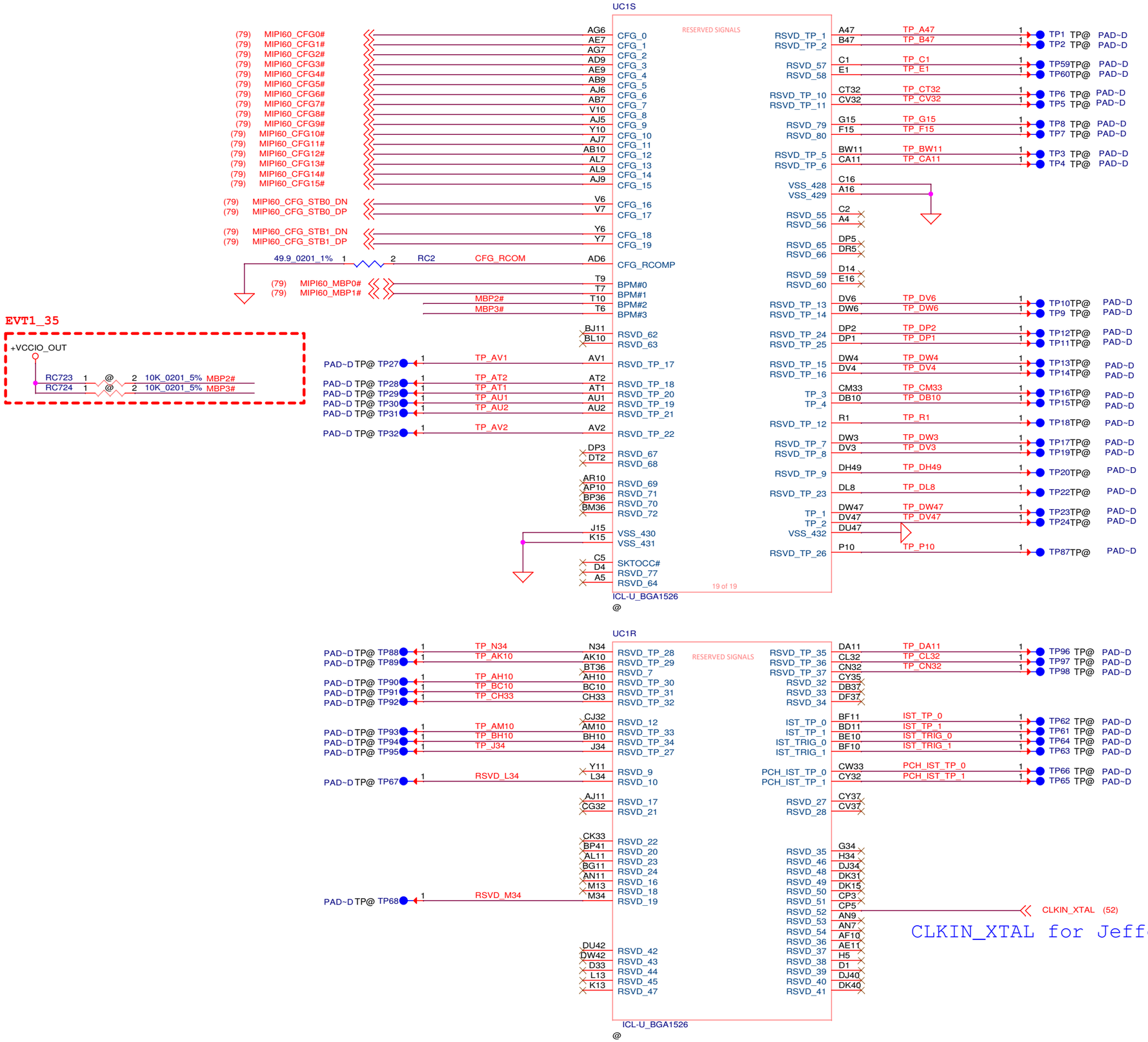
Compal Electronics, Inc.

Title: **P016 - ICL-U(11/13)PCH Power**

Size | Document Number: **LA-G172P** | Rev 1.0 (A00)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title: P017 - ICL-U(12/13)GND
				Size / Document Number: LA-G172P / Rev 1.0 (A00)
				Date: Friday, May 24, 2019 / Sheet 17 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P018 - ICL-U(13/13)RSVD,MIPI60		
Size	Document Number LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 18 of 101		

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P019 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 19 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P020 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 20 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P021 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 21 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

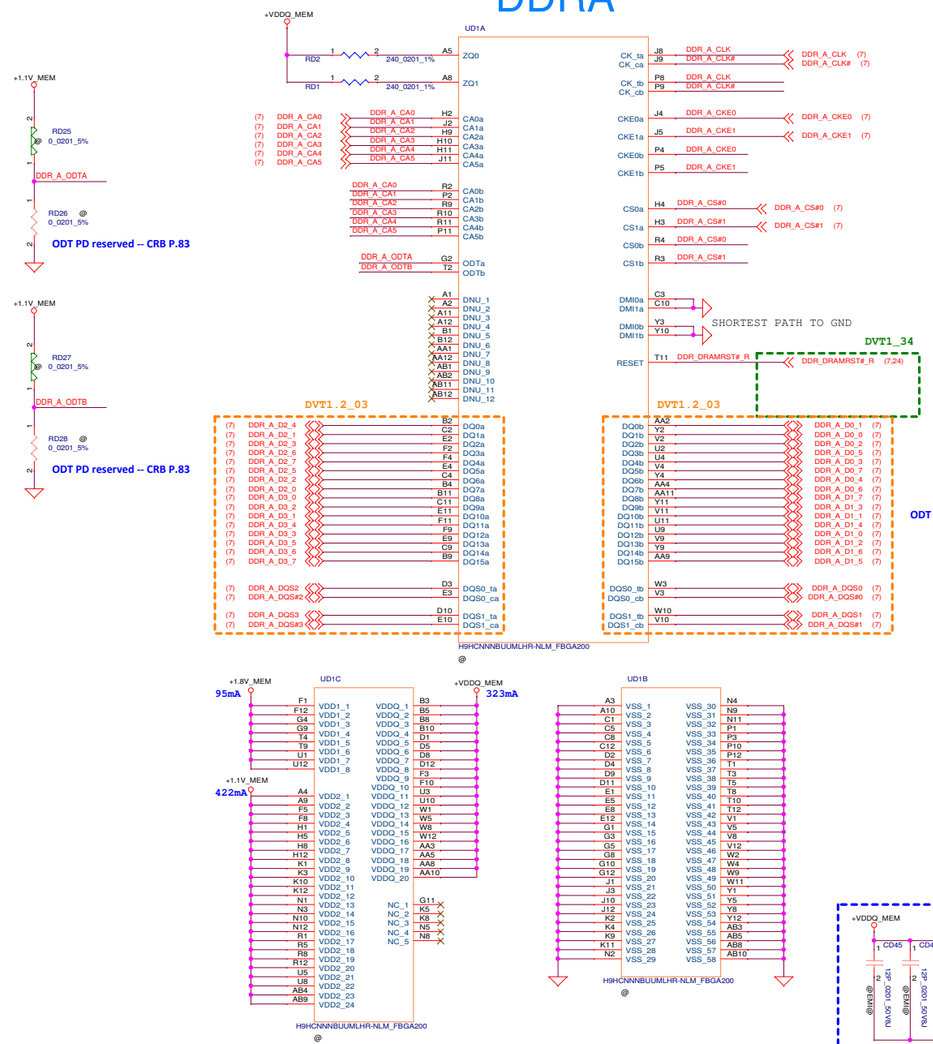
Title: **P022 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

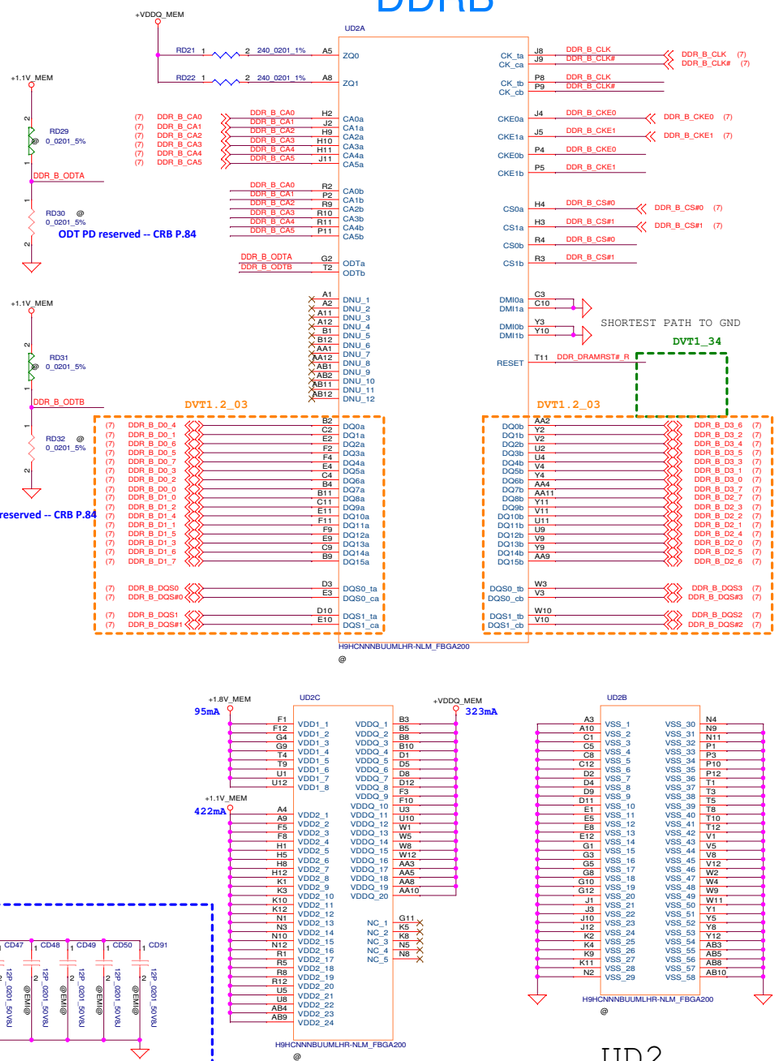
Date: Friday, May 24, 2019 | Sheet 22 of 101

Memory connection follow J72913-201 Rev 01_20181217

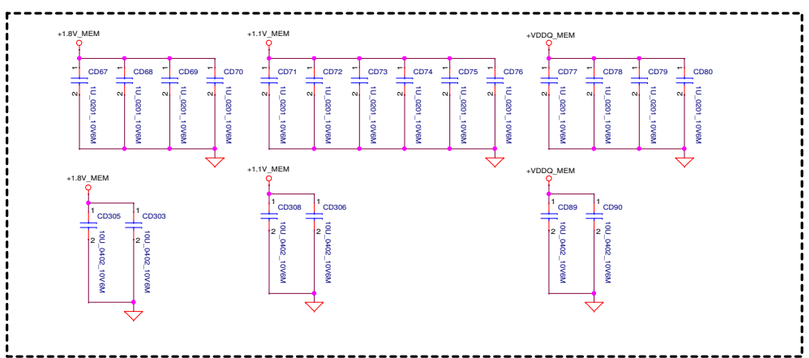
DDRA



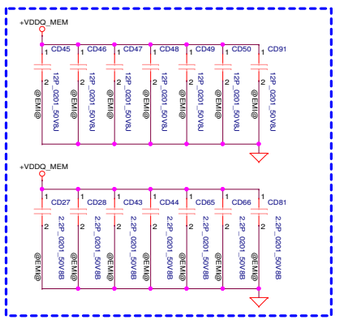
DDRB



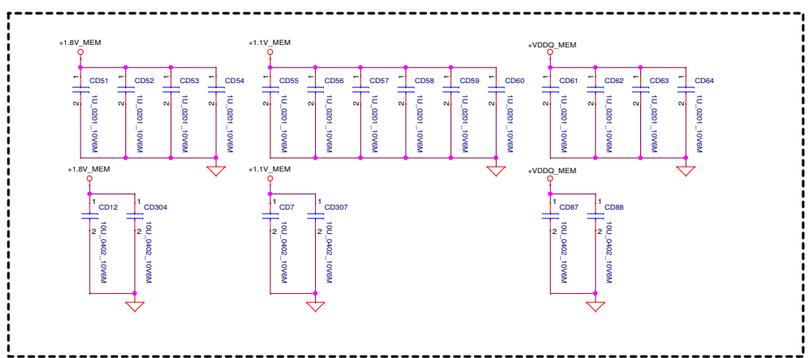
UD1



EMC CAPS



UD2



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

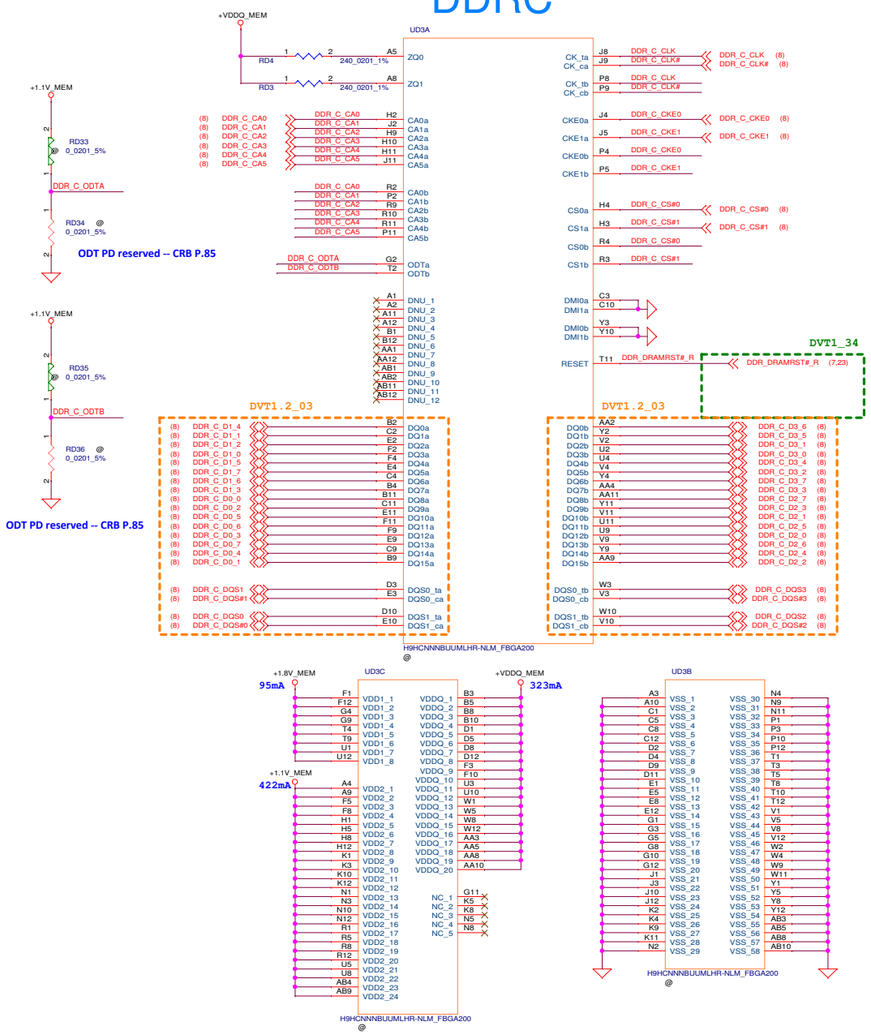
Title: **P023 - LPDDR4/x Channel A/B**

Size: | Document Number: **LA-G172P** | Rev: 3.0 (A00)

Date: Friday, May 24, 2019 | Sheet 23 of 101

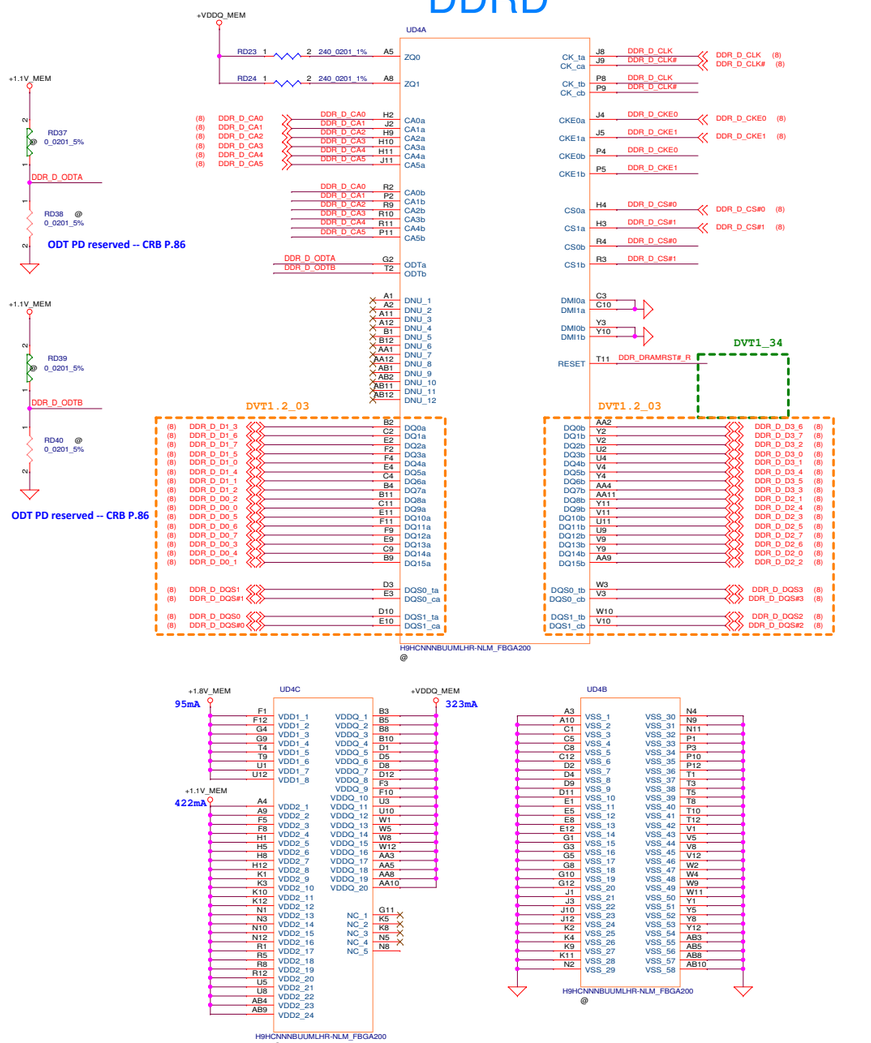
Memory connection follow J72913-201 Rev 01_20181217

DDRC

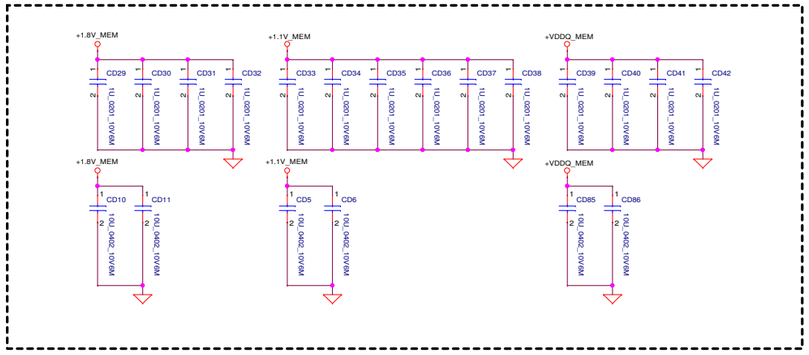


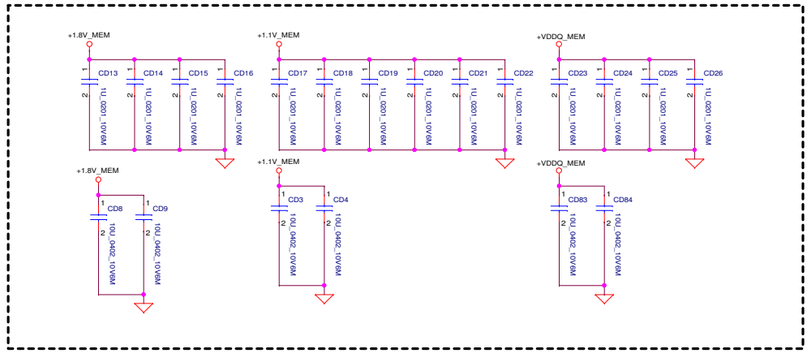
UD3

DDRD



UD4





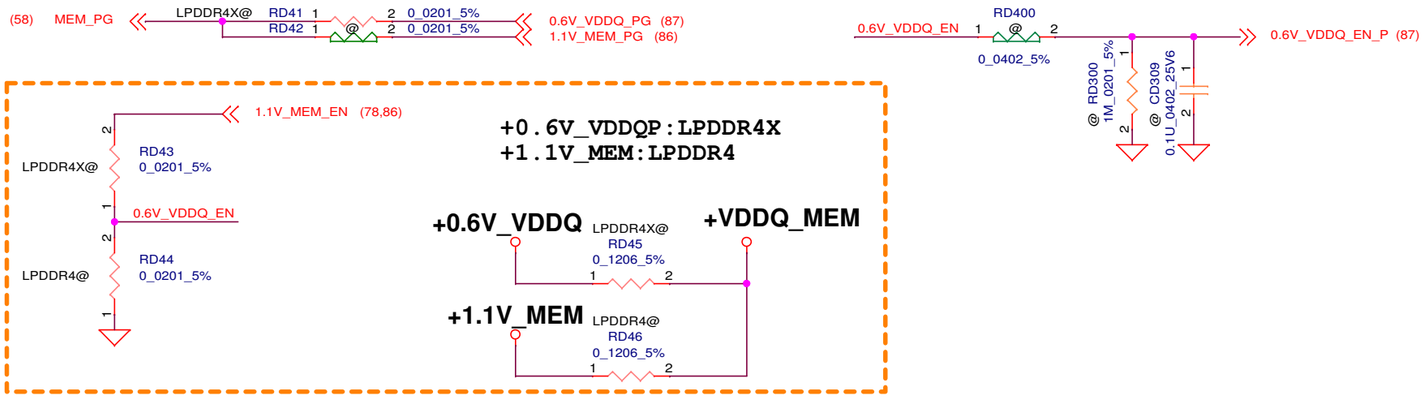
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P024 - LPDDR4/x Channel C/D**

Size: | Document Number: **LA-G172P** | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 24 of 101



	RD43	RD45	RD44	RD46
LPDDR4(1.1V) :	@	@		
LPDDR4X(1.1v&0.6V):			@	@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28
Title	P025 - LPDDR4&4X BOM OPTION		
Size	Document Number LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 25 of 101		

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P026 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 26 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P027 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 27 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P028 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 28 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P029 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 29 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P030 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 30 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P031 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 31 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P032 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 Sheet 32 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P033 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 33 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P034 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 34 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P035 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 35 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P036 - Reserve**

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Date: Friday, May 24, 2019 | Sheet 36 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

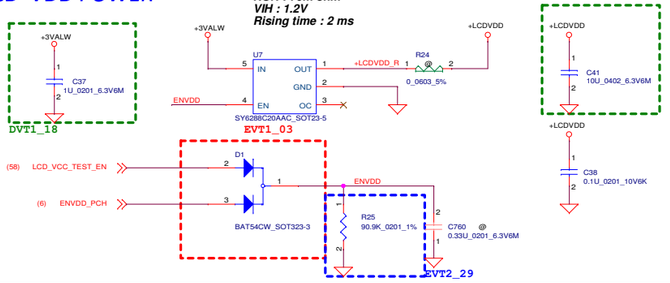
Title: **P037 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

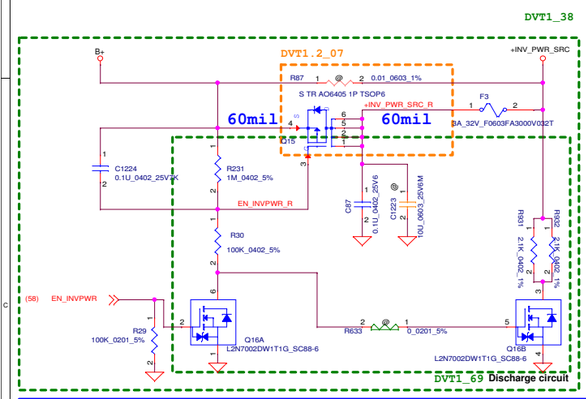
Date: Friday, May 24, 2019 | Sheet 37 of 101

LCD VDD POWER

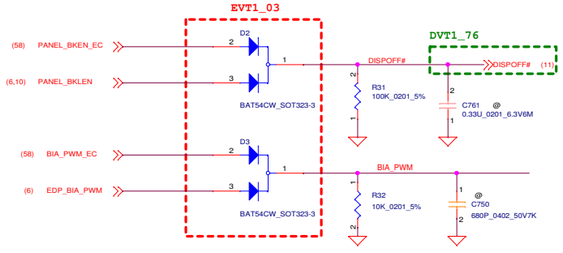
OCP : 1.5A
RON : 70m ohm
VIH : 1.2V
Rising time : 2 ms



eDP BackLight Power



BackLight PWM Control



eDP Conn

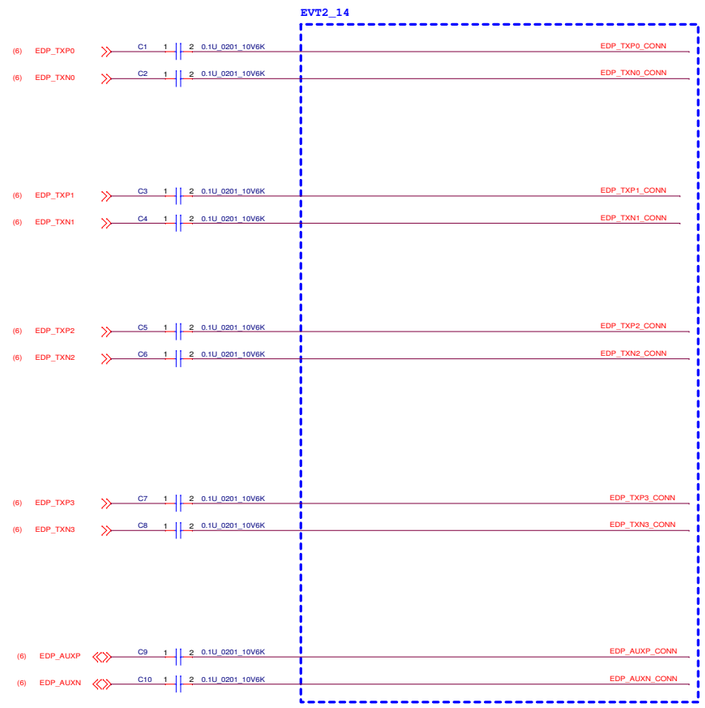
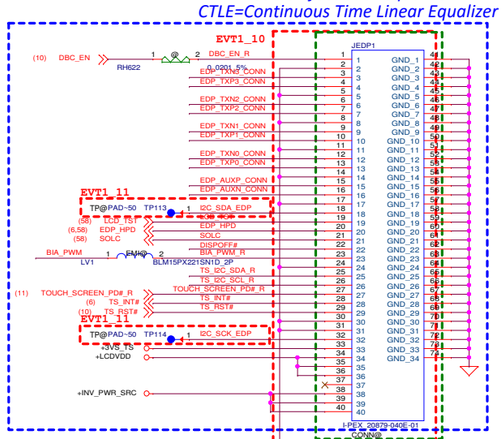


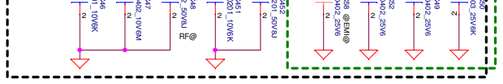
Table 5-41. eDP* Bit Rates

Bit Rate	Lane Supports (max # of lanes)	Peak Bandwidth
1.62 Gb/s (RBR)	4	4 x 162 MB/s = 648 MB/s
2.7 Gb/s (HBR)	4	4 x 270 MB/s = 1080 MB/s
5.4 Gb/s (HBR2)	4	4 x 540 MB/s = 2160 MB/s
8.1 Gb/s (HBR3)	4	4 x 810 MB/s = 3240 MB/s

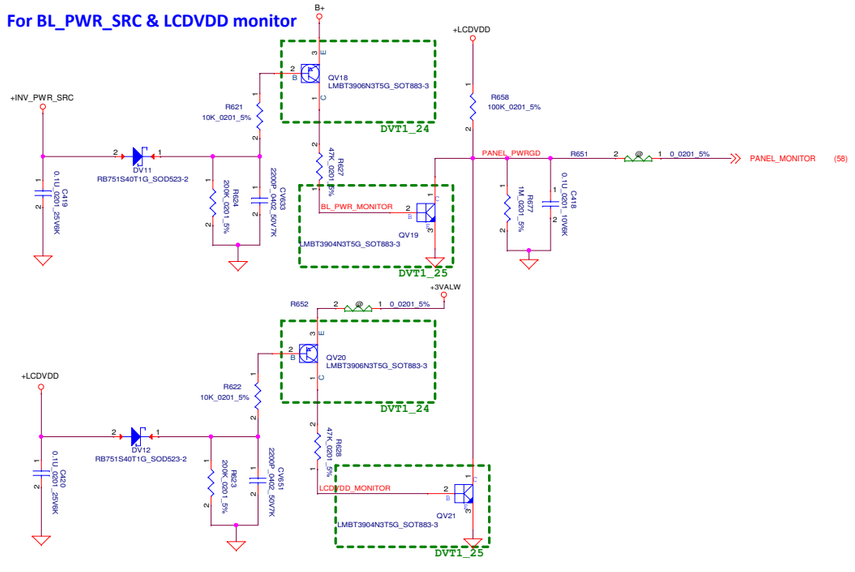
eDP Bit Rates 8.1 Gb/s (HBR3)*
In TCON side , RX Equalization is CTLE + DFE
DFE=Decision feedback equalizer
CTLE=Continuous Time Linear Equalizer

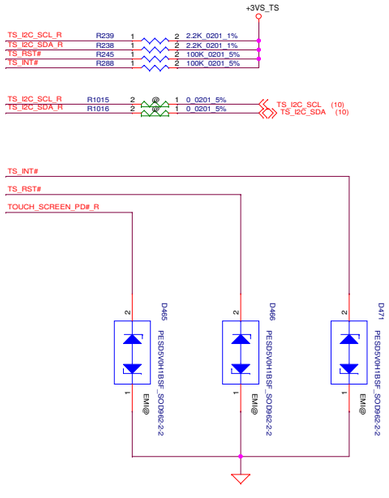


Connecter	Pin	NAME	IN/OUT	FUNCTION
CN1	1	/STOP	I	HIGH : Normal Operation LOW : Stop Scanning Build-in pull/up (to 3.3 volts) resistor 35kohm
	2	IIC SDA	I/O	IIC Data Open drain output, pull-up resister at Host is needed
	3	IIC SCL	I	IIC Clock Open drain output, pull-up resister at Host is needed
	4	NC	-	No Connection
	5	NC	-	No Connection
	6	IIC IRQ	O	IIC Data Ready Output "LOW" when data ready to send Open drain output, pull-up resister at Host is needed
	7	/RESET	I	Hardware RESET : Low Active Stop operation when pull "LOW" Build-in pull-up (to 3.3 volts) resister 100kohm
	8	VDD +3.3V	-	3.3 volts (typ) power input
	9	NC	-	No Connection
	10	DGND	-	Ground



For BL_PWR_SRC & LCDVDD monitor





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Compal Electronics, Inc.

Title: **P038 - eDP,Touch Screen**

Size: Document Number: **LA-G172P** Rev: 1.0 (A00)

Date: Friday, May 24, 2019 Sheet 38 of 101

EVT2_11 For factory test request

TP@PAD~50 TP132 1 I2C_3_SCL_UFCAM_R
TP@PAD~50 TP133 1 I2C_3_SDA_UFCAM_R
TP@PAD~50 TP134 1 ISH_I2C1_SCL_R
TP@PAD~50 TP135 1 ISH_I2C1_SDA_R
TP@PAD~50 TP136 1 UFCAM_LED_R
TP@PAD~50 TP137 1 UFCAM_RESET#_R
TP@PAD~50 TP138 1 ALS_ALERT#_R
TP@PAD~50 TP139 1 UFCAM_MCLK_R
TP@PAD~50 TP140 1 ACC1_INT1#
TP@PAD~50 TP141 1 ACC1_INT2#
TP@PAD~50 TP142 1
TP@PAD~50 TP143 1 +CAM_PWR
TP@PAD~50 TP144 1 +DVDD_MIC
+3VS_MID
TP@PAD~50 TP145 1 CAM_DET#_R
DVT1_59

+3VS F5 +3VS_MID
0.5A_65V_T0603FF0500TM

UF Camera HD (720p)
ALS
Accelerometer+Gyro
Ecompass
DMIC

EVT2_10
EVT1_12
JUFC1
I-PEX_20879-030E-01
CONN@
DVT1_40

UFCAM_RESET#
I2C_3_SDA_UFCAM_R
I2C_3_SCL_UFCAM_R
EVT1_14
MCSI_E_DP0
MCSI_E_DN0
MCSI_E_CLKP
MCSI_E_CLKN

Camera vendor detect
0 = Liteon
1 = Azurewave

+CAM_PWR
+DVDD_MIC
+3VS_MID
EVT1_14
(13) MCSI_E_CLKP MCSI_E_CLKP
(13) MCSI_E_CLKN MCSI_E_CLKN
(13) MCSI_E_DP0 MCSI_E_DP0
(13) MCSI_E_DN0 MCSI_E_DN0
(56) DMIC_CLK12 DMIC_CLK12
(56) DMIC_DATA12 DMIC_DATA12
(10) I2C_3_SCL_UFCAM R6114 1 @ 2 0_0201_5% I2C_3_SCL_UFCAM_R
(10) I2C_3_SDA_UFCAM R6115 1 @ 2 0_0201_5% I2C_3_SDA_UFCAM_R
DVT1_59
(10) ISH_I2C1_SCL R6116 1 @ 2 0_0201_5% ISH_I2C1_SCL_R
(10) ISH_I2C1_SDA R6117 1 @ 2 0_0201_5% ISH_I2C1_SDA_R
(10) CAM_DET# R6208 1 2 100K_0201_5% CAM_DET#_R
(10) UFCAM_RESET# R6142 1 @ 2 0_0201_5% UFCAM_RESET#_R
(10) ALS_ALERT# R6118 1 @ 2 0_0201_5% ALS_ALERT#_R
(13) UFCAM_MCLK R6141 1 @ 2 0_0201_5% UFCAM_MCLK_R
(10) ACC1_INT1# ACC1_INT1#
(10) ACC1_INT2# ACC1_INT2#

D444 PESD5V0H1BSF_SOD962-2-2 @EMI@
D445 PESD5V0H1BSF_SOD962-2-2 @EMI@
D446 PESD5V0H1BSF_SOD962-2-2 @EMI@
D447 PESD5V0H1BSF_SOD962-2-2 @EMI@
D448 PESD5V0H1BSF_SOD962-2-2 @EMI@
D449 PESD5V0H1BSF_SOD962-2-2 @EMI@
D450 PESD5V0H1BSF_SOD962-2-2 @EMI@
EVT1_24

Intel DMIC for WOV reserved

+3V_PRIM R6205 1 @ 2 0_0201_5%
+1.8V_PRIM R6206 1 @ 2 0_0201_5%
+DVDD R636 1 @ 2 0_0201_5%
F1 0.5A_65V_T0603FF0500TM
+DVDD_MIC
(10) PCH_DMIC_DATA12 R655 1 @ 2 0_0402_5% DMIC_DATA12
R618 @ 10K_0201_5%
+5VS_AUDIO
R612 @ 0.01_0402_1%
C635 @ 0.1U_0201_16V6K
C625 @ 10U_0402_10V6M
(10) PCH_DMIC_CLK12 R634 1 @ 2 0_0402_5% DMIC_CLK12
PVT_08

Camera module
LED control

+3VS 10K_0201_5% R6157 ALS_ALERT#
+1.8VS 2.2K_0201_5% R6128 I2C_3_SDA_UFCAM_R
2.2K_0201_5% R6129 I2C_3_SCL_UFCAM_R

PLED R4 0(0201) AVDD28 R3 330(0201)/NC
LED1 LTW-C283DS5(0402)
DGND

+5VALW
EVT1_04
R6207 1 @ 2 0_0201_5%
QC1 PJQ1900_DFN3L
R710 1 2 680_0201_5% UFCAM_LED_R
(12) UFCAM_LED
R709 10K_0201_5%
DVT1_44

Bypass cap close to CONN
+3VS CC17 1U_0201_6.3V6M
+DVDD_MIC C1540 0.1U_0201_10V6K
+CAM_PWR C1539 0.1U_0201_10V6K
DVT1_18

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.
Title: P039 - UF Camera,MIC,ALS
Size: Document Number: LA-G172P
Rev: 1.0 (A00)
Date: Friday, May 24, 2019 Sheet 39 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P040 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 40 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P041 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

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+TBT_VBUS_L

EVT1_07

TP110 TP@ PAD-D

EMI@ HCB2012KF-800T50_2P LT11

EMI@ HCB2012KF-800T50_2P LT13

EMI@ CT338 220P_0201_25V7K

EMI@ CT339 0.01U_0201_25V6K

EMI@ CT340 0.01U_0201_25V6K

EMI@ CT341 100P_0201_50V8J

EMI@ CT318 1U_0402_25V6K

EMI@ CT34 10U_0603_25V6M

+TBT_VBUS_L_PD

EVT1_07

EMI@ CT319 1U_0402_25V6K

EMI@ CT342 220P_0201_25V7K

EMI@ CT343 1000P_0201_50V7K

EMI@ CT344 100P_0201_50V8J

EMI@ CT345 0.1U_0201_25V6K

EMI@ CT346 1U_0402_25V6K

@EMI@ RT150 1M_0201_1%

DVT1_09

EVT1_01

+TBT_VBUS_L_PD

Close pin 3,4

CPD42 1U_0402_25V6K

Close pin 13,14

CPD49 1U_0402_25V6K

+VIN_3V3_L_TBT

Close pin 5

CPD5 10U_0402_10V6M

+CHG_VIN_20V

Close pin 11,12

CPD40 10U_0603_35V6M

CPD47 10U_0603_35V6M

+5VALW_L_TBT

Close pin 1,2

CPD7 10U_0402_10V6M

Close pin 25

CPD8 22U_0603_10V6M

+3VALW

+VIN_3V3_L_TBT

RPD84 1 @ 2 0_0402_5%

+3.3V_BAT_LDO

EVT2_40

RPD114 1 @ 2 0_0201_5%

+5VALW

+5VALW_L_TBT

RPD121 1 @ 2 0_1206_5%

DVT2_14

PD_L_GPIO17

PD_L_GPIO16

UPD1

+CHG_VIN_20V

20V/3.5A

+5VALW_L_TBT

5V/3.5A

+VIN_3V3_L_TBT

+VCC3V3_TBT_L_LDO

+VCC1V8_TBT_L_LDO

3V/25 mA

BUSPOWER

I2C Address

ADCIN1_L_PD

ADCIN2_L_PD

PP_HV1_1

PP_HV1_2

PP_HV2_1

PP_HV2_2

PP1_CABLE

VIN_3V3

LDO_3V3

LDO_1V8

ADCIN1

ADCIN2

GPIO16(FEXT1)

GPIO17(FEXT2)

VBUS2_1

VBUS2_2

VBUS1_1

VBUS1_2

3.5A

C1_CC1

C1_CC2

TBT_L_CC1

TBT_L_CC2

EVT1_18

C1_USB_P(GPIO18)

C1_USB_N(GPIO19)

PD_L_GPIO18

PD_L_GPIO19

DVT1_14

I2C1_SCL

I2C1_SDA

I2C1_IRQ

I2C1_PD_L_CLK

I2C1_PD_L_DAT

I2C1_PD_L_INT#

I2C Port 1 to System Control

I2C2_SCL

I2C2_SDA

I2C2_IRQ

I2C2_PD_L_CLK

I2C2_PD_L_DAT

I2C2_PD_L_INT#

I2C Port 2 to Thunderbolt Controller

SPI_MISO(GPIO8)

SPI_MOSI(GPIO9)

SPI_CLK(GPIO10)

SPI_SS(GPIO11)

PD_EE_MISO_L

PD_EE_MOSI_L

PD_EE_CLK_L

PD_EE_CS#_L

HRESET

HRESET_L_PD

RPD88 1 @ 2 0_0201_5%

DRAIN1_1

DRAIN1_2

DRAIN1_3

DRAIN1_4

PD_L_DRAIN1

DRAIN2_1

DRAIN2_2

DRAIN2_3

DRAIN2_4

PD_L_DRAIN2

GND_1

GND_4

GND_5

GND_6

GND_2

GND_3

SA0000CM71L @

SN1806026RSHR VQFN 56P

EVT2_38

PVT_14

+TBT_VBUS_L_PD

D461 ESD@ LMBR4010H3T5G DFN-1608

DVT2_05

PVT_11

PVT_04

+VCC3V3_TBT_L_LDO

Close pin 9

CPD4 10U_0402_10V6M

+VCC1V8_TBT_L_LDO

Close pin 35

CPD6 4.7U_0402_6.3V6M

EVT2_44

+VCC3V3_TBT_L_LDO

RPD11 1 2 3.3K_0201_5% PD_EE_CS#_L

RPD12 1 2 3.3K_0201_5% PD_EE_MISO_L

RPD13 1 2 3.3K_0201_5% PD_HOLD#_L

RPD14 1 2 3.3K_0201_5% PD_EE_WP#_L

RPD181 1 @ 2 10K_0201_5% PD_EE_MISO_L

(36) PD_EE_MISO:

'0' - SPI-less

'1' - SPI

+VCC3V3_TBT_L_LDO

UPD3

PD_EE_CS#_L

PD_EE_MISO_L

PD_EE_WP#_L

/CS

DO(IO1)

/WP(IO2)

GND

VCC

/HOLD(IO3)

CLK

DI(IO0)

thermal pad

PD_HOLD#_L

PD_EE_CLK_L

PD_EE_MOSI_L

W25Q64JVZPIQ_WSON8_6X5

Left PD Controller SPI FLASH

+VCC3V3_TBT_L_LDO

CPD1 0.1U_0201_10V6K

DVT1_13

TBT_L_CC1

TBT_L_CC2

CPD3 1 2 220P_0201_25V6K

CPD2 1 2 220P_0201_25V6K

JDB1

PD_EE_CLK_L

PD_EE_MOSI_L

PD_EE_MISO_L

PD_EE_CS#_L

I2C1_PD_L_CLK

I2C1_PD_L_DAT

I2C2_PD_L_CLK

I2C2_PD_L_DAT

GND1

GND2

ACES_50521-01041-P01

CONN@

I2C1_PD_L_CLK RPD163 1 @ 2 0_0201_5% UPD_SMBCLK_Q (44,50,58)

I2C1_PD_L_DAT RPD164 1 @ 2 0_0201_5% UPD_SMBDAT_Q (44,50,58)

I2C1_PD_L_INT# RPD17 1 @ 2 0_0201_5% UPD_L_SMBINT# (58)

I2C2_PD_L_CLK RPD21 1 @ 2 0_0201_5% SML1_SMBCLK (9,44,46,48)

I2C2_PD_L_DAT RPD22 1 @ 2 0_0201_5% SML1_SMBDATA (9,44,46,48)

I2C2_PD_L_INT# RPD112 1 @ 2 0_0201_5% TBT_I2C_INT# (11,44,46,48)

EVT1_08

I2C3 on TGL

(50) PD_L_USB_MUX1_EN

(46) TCP0_RST#

(47) PD_TCP0_LS_EN

(46) I2C3_PD_L_CLK_R

(46) I2C3_PD_L_DAT_R

(46) I2C3_PD_L_INT#_R

(44,82) PD_L_R_PROCHOT#

(50) MUX_L_FLIP#

(50) PD_L_DDM_MUX1_EN

(13,44,46,48) RT_FORCE_PWR

(44) PD_R_SLAVE_IN

(44) PD_L_SLAVE_IN

RPD187 1 @ 2 0_0201_5% PD_L_USB_MUX1_EN_R

RPD124 1 @ 2 0_0201_5% TCP0_RST#_R

PD_L_GPIO2

RPD126 1 @ 2 0_0201_5% PD_TCP0_LS_EN_R

PD_L_GPIO4

RPD194 1 @ 2 0_0201_5% I2C3_PD_L_CLK

RPD142 1 @ 2 0_0201_5% I2C3_PD_L_DAT

RPD155 1 @ 2 0_0201_5% I2C3_PD_L_INT#

RPD185 1 @ 2 0_0201_5% PD_L_PROCHOT#

RPD127 1 @ 2 0_0201_5% MUX_L_FLIP#_R

RPD123 1 @ 2 0_0201_5% PD_L_DDM_MUX1_EN_R

RPD130 1 @ 2 0_0201_5% RT_L_FORCE_PWR

RPD174 1 @ 2 0_0201_5% PD_L_SINK_ARB_MASTER_OUT

RPD172 1 @ 2 0_0201_5% PD_L_SINK_ARB_SLAVE_IN

GPIO0

GPIO1

GPIO2

HPD1(GPIO3)

GPIO4

GPIO5

GPIO6

GPIO7

GPIO12

GPIO13

GPIO14(PWM)

GPIO15(PWM)

GPIO20

GPIO21

+VCC3V3_TBT_L_LDO

EVT1_08

PVT_07

10K_0201_5% RPD198 I2C3_PD_L_CLK_R

10K_0201_5% RPD197 I2C3_PD_L_DAT_R

10K_0201_5% RPD196 I2C3_PD_L_INT#_R

10K_0201_5% RPD183 PD_L_PROCHOT#

10K_0201_5% RPD129 MUX_L_FLIP#

10K_0201_5% RPD170 TCP0_RST#

DVT1_51

10K_0201_5% RPD189 PD_L_SINK_ARB_SLAVE_IN

100K_0201_5% RPD190 PD_L_USB_MUX1_EN_R

100K_0201_5% RPD191 PD_L_DDM_MUX1_EN_R

1M_0201_5% RPD169 TCP0_RST#

100K_0201_5% RPD128 MUX_L_FLIP#

EVT1_08

Reserved for debug

PD_L_GPIO18 RPD204 1 @ 2 0_0201_5% PD_L_GPIO19

PD_L_GPIO17 RPD139 1 @ 2 0_0201_5% PD_L_GPIO2

PD_L_GPIO4 RPD141 1 @ 2 0_0201_5% PD_L_GPIO16

DVT1_14

RPD152 1 @ 2 0_0201_5%

RPD153 1 @ 2 0_0201_5%

RPD154 1 @ 2 0_0201_5%

Pin 45,46,47

In TPS65987DH need to connect to GND

EVT2_39

BUSPOWER Config
BP_NoWait value 0.7~0.78

+VCC3V3_TBT_L_LDO

R1

RPD92 100K_0201_1%

ADCIN1_L_PD

R2

RPD91 300K_0201_1%

EVT2_45

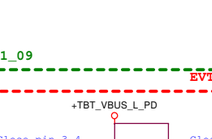

Figure 22. ADCIN1 Resistor Divider

Table 2. BUSPOWER Configuration

DIV = R2/(R1+R2)(1)		Configuration	Description	Recommended for
DIV MIN	DIV MAX			
0.00	0.18	BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present	Ports intended to operate as DFP/iSource only, or applications that do not support charging or operation during dead battery conditions
0.20	0.38	BP_WaitForV3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.40	0.58	BP_WaitForV3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.60	1.00	BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and do not depend on outside system components for device configuration and operation.

I2C Address Divider:010b

+VCC3V3_TBT_L_LDO

R1

RPD90 100K_0201_1%

ADCIN2_L_PD

R2

RPD100 100K_0201_1%

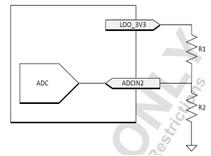

Figure 36. I²C Address Divider

Table 6 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 6. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
0.00	0.18	000b
0.20	0.38	001b
0.40	0.58	010b
0.60	1.00	011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

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Compal Electronics, Inc.	
Title	P042 - TYPE-C Port L_PD
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LEFT Type-C Connector

EVT2_08

(46) TBT_0_TTX_CD_DRX_P0
(46) TBT_0_TTX_CD_DRX_N0
(46) TBT_0_TTX_CD_DRX_P1
(46) TBT_0_TTX_CD_DRX_N1

CT30 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_P0
CT31 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_N0
CT32 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_P1
CT33 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_N1

EVT1_05

DVT1_02

EVT2_22

+TBT_VBUS_L

JUSBC1

A1	GND_1	B12	GND_4
TBT_0_TTX_C_DRX_P0 A2	SSTXp1	B11	SSRXp1 TBT_0_TRX_RT_DTX_P0 TBT_0_TRX_RT_DTX_P0 (46)
TBT_0_TTX_C_DRX_N0 A3	SSTXn1	B10	SSRXn1 TBT_0_TRX_RT_DTX_N0 TBT_0_TRX_RT_DTX_N0 (46)
CT3101 2 0.1U_0201_25V6K A4	VBUS_1	B9	VBUS_4 2 1 CT1313 0.1U_0201_25V6K
(42) TBT_L_CC1 TBT_L_CC1 A5	CC1	B8	SBU2 TBT_0_SBU2 TBT_0_SBU2 (46)
SW_TBT_L_USB20_P1_R A6	Dp1	B7	Dn2 SW_TBT_L_USB20_N2_R
SW_TBT_L_USB20_N1_R A7	Dn1	B6	Dp2 SW_TBT_L_USB20_P2_R
(46) TBT_0_SBU1 TBT_0_SBU1 A8	SBU1	B5	CC2 TBT_L_CC2 TBT_L_CC2 (42)
CT3121 2 0.1U_0201_25V6K A9	VBUS_2	B4	VBUS_3 2 1 CT1311 0.1U_0201_25V6K
(46) TBT_0_TRX_RT_DTX_N1 TBT_0_TRX_RT_DTX_N1 A10	SSRXn2	B3	SSTXn2 TBT_0_TTX_C_DRX_N1
(46) TBT_0_TRX_RT_DTX_P1 TBT_0_TRX_RT_DTX_P1 A11	SSRXp2	B2	SSTXp2 TBT_0_TTX_C_DRX_P1
A12	GND_2	B1	GND_3
JUSBC1_GND 1	GND_5	5	GND_6
2	GND_7	6	GND_8
3	GND_9	7	GND_10
4	GND_11	8	GND_12

TOP
BOTTOM

FOX_UT12123-10001-7H CONN@

EVT1_18 EVT2_08 EVT2_08 EVT1_18

JUSBC1_GND

+TBT_VBUS_L

CT347 10U_0603_25V6M

+TBT_VBUS_L

AZ4520-01F.R7G_DFN1610P2E2 D459 ESD@

DVT1_23

EVT1_26

EVT2_08

JUSBC1_GND

EMI@ CT35 0.1U_0201_25V6K

LT1 EMI@ HCB2012KF-800T50_2P

EVT1_18

TBT_0_SBU1

@ CT206 100P_0201_50V8J

RT118 @ 1M_0201_1%

TBT_0_SBU2

@ CT207 100P_0201_50V8J

RT119 @ 1M_0201_1%

EVT2_08

PVT_05

ML6 EMI@

(50) SW_TBT_L_USB20_N1 1 2 SW_TBT_L_USB20_N1_R
(50) SW_TBT_L_USB20_P1 4 3 SW_TBT_L_USB20_P1_R

HCM1012GH900BP_4P

ML7 EMI@

(50) SW_TBT_L_USB20_N2 1 2 SW_TBT_L_USB20_N2_R
(50) SW_TBT_L_USB20_P2 4 3 SW_TBT_L_USB20_P2_R

HCM1012GH900BP_4P

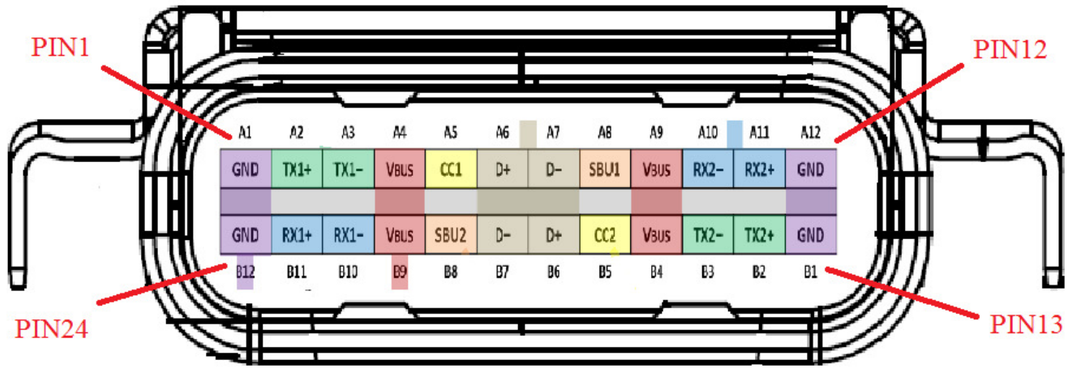
EVT2_08

TBT_0_TTX_C_DRX_P0	D75 ESD@ PESD5V0H1BSF_SOD962-2-2	D76 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_0_TTX_C_DRX_P1
TBT_0_TTX_C_DRX_N0	D77 ESD@ PESD5V0H1BSF_SOD962-2-2	D78 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_0_TTX_C_DRX_N1
TBT_0_TRX_RT_DTX_P0	D79 ESD@ PESD5V0H1BSF_SOD962-2-2	D80 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_0_TRX_RT_DTX_P1
TBT_0_TRX_RT_DTX_N0	D81 ESD@ PESD5V0H1BSF_SOD962-2-2	D82 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_0_TRX_RT_DTX_N1

ESD Diodes should be located as close as possible to USBC.

SW_TBT_L_USB20_P1_R1	D407 ESD@ PESD5V0H1BSF_SOD962-2-2	D408 ESD@ PESD5V0H1BSF_SOD962-2-2	SW_TBT_L_USB20_N1_R
SW_TBT_L_USB20_P2_R1	D409 ESD@ PESD5V0H1BSF_SOD962-2-2	D410 ESD@ PESD5V0H1BSF_SOD962-2-2	SW_TBT_L_USB20_N2_R
TBT_L_CC1	D411 ESD@ PESD5V0H1BSF_SOD962-2-2	D412 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_0_SBU1
TBT_0_SBU2	D413 ESD@ PESD5V0H1BSF_SOD962-2-2	D414 ESD@ PESD5V0H1BSF_SOD962-2-2	TBT_L_CC2

EVT1_18



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Compal Electronics, Inc.

Title: P043 - TYPE-C Conn L

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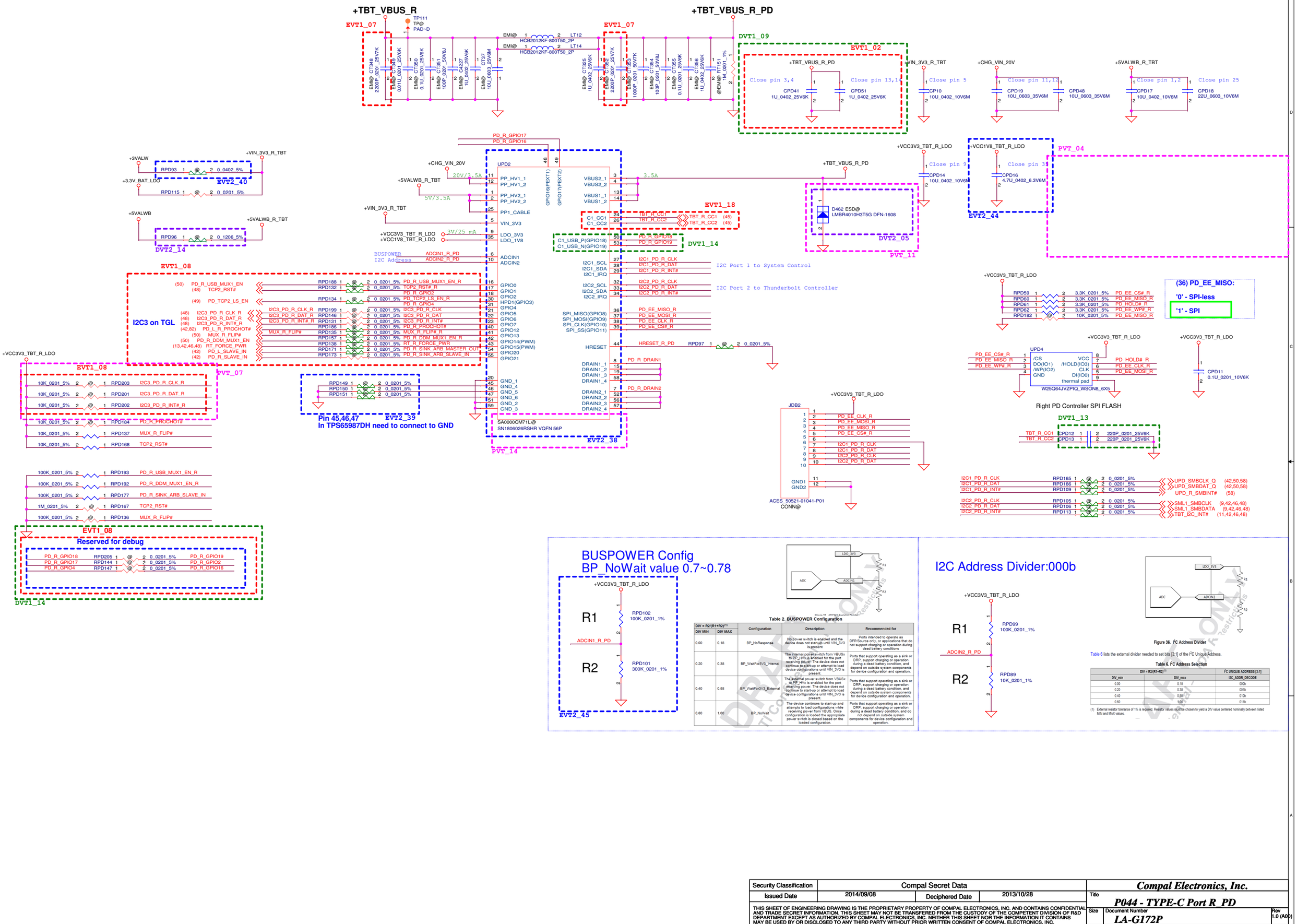

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	P044 - TYPE-C Port R_PD		
Size	Document Number		Rev
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RIGHT Type-C Connector

EVT2_08

(48) TBT_2_TTX_CD_DRX_P0
(48) TBT_2_TTX_CD_DRX_N0
(48) TBT_2_TTX_CD_DRX_P1
(48) TBT_2_TTX_CD_DRX_N1

CT38 1 2 0.22U_0201_6.3V6M TBT_2_TTX_C_DRX_P0
CT39 1 2 0.22U_0201_6.3V6M TBT_2_TTX_C_DRX_N0
CT40 1 2 0.22U_0201_6.3V6M TBT_2_TTX_C_DRX_P1
CT41 1 2 0.22U_0201_6.3V6M TBT_2_TTX_C_DRX_N1

EVT1_06

DVT1_02
EVT2_22

+TBT_VBUS_R

JUSBC2

A1	GND_1	GND_4	B12
A2	SSTXp1	SSRXp1	B11
A3	SSTXn1	SSRXn1	B10
A4	VBUS_1	VBUS_4	B9
A5	CC1	SBU2	B8
A6	Dp1	Dn2	B7
A7	Dn1	Dp2	B6
A8	SBU1	CC2	B5
A9	VBUS_2	VBUS_3	B4
A10	SSRXn2	SSTXn2	B3
A11	SSRXp2	SSTXp2	B2
A12	GND_2	GND_3	B1
1	GND_5	GND_6	5
2	GND_7	GND_8	6
3	GND_9	GND_10	7
4	GND_11	GND_12	8

TOP
BOTTOM

FOX_UT12123-10001-7H CONN@

EVT1_18

TBT_2_TTX_C_DRX_P0
TBT_2_TTX_C_DRX_N0
CT3141 2 0.1U_0201_25V6K
(44) TBT_R_CC1 TBT_R_CC1
SW_TBT_R_USB20_P1_R
SW_TBT_R_USB20_N1_R
(48) TBT_2_SBU1 TBT_2_SBU1
CT3161 2 0.1U_0201_25V6K
(48) TBT_2_TRX_RT_DTX_N1 TBT_2_TRX_RT_DTX_N1
(48) TBT_2_TRX_RT_DTX_P1 TBT_2_TRX_RT_DTX_P1

EVT2_08

JUSBC2_GND

+TBT_VBUS_R

TBT_2_TRX_RT_DTX_P1 TBT_2_TRX_RT_DTX_P0 (48)
TBT_2_TRX_RT_DTX_N1 TBT_2_TRX_RT_DTX_N0 (48)
2 CT317 0.1U_0201_25V6K
TBT_2_SBU2 TBT_2_SBU2 (48)
SW_TBT_R_USB20_N2_R
SW_TBT_R_USB20_P2_R
TBT_R_CC2 TBT_R_CC2 (44)
2 CT315 0.1U_0201_25V6K
TBT_2_TTX_C_DRX_N1
TBT_2_TTX_C_DRX_P1

EVT2_08

EVT1_18

JUSBC2_GND

+TBT_VBUS_R

CT357 10U_0603_25V6M EMI@

+TBT_VBUS_R

AZ4520-01F.R7G_DFN1610P2E2 D460 ESD@

DVT1_22

EVT1_26

EVT2_08

EVT1_18

JUSBC2_GND

EMI@ CT36 0.1U_0201_25V6K
LT2 EMI@ HCB2012KF-800T50_2P

TBT_2_SBU1
@ CT306 100P_0201_50V8J
RT120 @ 1M_0201_1%

TBT_2_SBU2
@ CT307 100P_0201_50V8J
RT121 @ 1M_0201_1%

EVT2_08

PVT_05

ML16 EMI@
(50) SW_TBT_R_USB20_N1
(50) SW_TBT_R_USB20_P1
SW_TBT_R_USB20_N1_R
SW_TBT_R_USB20_P1_R
HCM1012GH900BP_4P

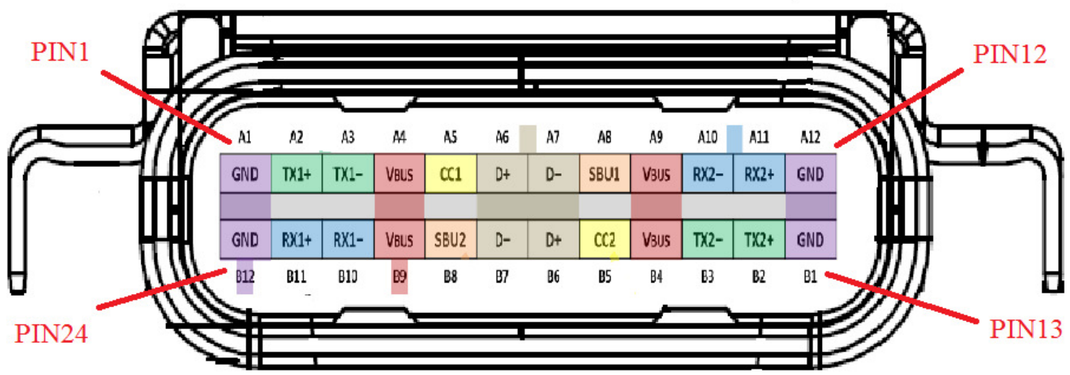
ML17 EMI@
(50) SW_TBT_R_USB20_N2
(50) SW_TBT_R_USB20_P2
SW_TBT_R_USB20_N2_R
SW_TBT_R_USB20_P2_R
HCM1012GH900BP_4P

D83 ESD@ TBT_2_TTX_C_DRX_P0 — PESD5V0H1BSF_SOD962-2-2
D84 ESD@ TBT_2_TTX_C_DRX_P1 — PESD5V0H1BSF_SOD962-2-2
D85 ESD@ TBT_2_TTX_C_DRX_N0 — PESD5V0H1BSF_SOD962-2-2
D86 ESD@ TBT_2_TTX_C_DRX_N1 — PESD5V0H1BSF_SOD962-2-2
D87 ESD@ TBT_2_TRX_RT_DTX_P0 — PESD5V0H1BSF_SOD962-2-2
D88 ESD@ TBT_2_TRX_RT_DTX_P1 — PESD5V0H1BSF_SOD962-2-2
D89 ESD@ TBT_2_TRX_RT_DTX_N0 — PESD5V0H1BSF_SOD962-2-2
D90 ESD@ TBT_2_TRX_RT_DTX_N1 — PESD5V0H1BSF_SOD962-2-2

ESD Diodes should be located as close as possible to USBC.

D415 ESD@ SW_TBT_R_USB20_P1_R1 — PESD5V0H1BSF_SOD962-2-2
D416 ESD@ SW_TBT_R_USB20_N1_R — PESD5V0H1BSF_SOD962-2-2
D417 ESD@ SW_TBT_R_USB20_P2_R1 — PESD5V0H1BSF_SOD962-2-2
D418 ESD@ SW_TBT_R_USB20_N2_R — PESD5V0H1BSF_SOD962-2-2
D420 ESD@ TBT_R_CC1 — PESD5V0H1BSF_SOD962-2-2
D419 ESD@ TBT_2_SBU1 — PESD5V0H1BSF_SOD962-2-2
D422 ESD@ TBT_2_SBU2 — PESD5V0H1BSF_SOD962-2-2
D421 ESD@ TBT_R_CC2 — PESD5V0H1BSF_SOD962-2-2

EVT1_18



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Compal Electronics, Inc.

Title: P045 - TYPE-C Conn R

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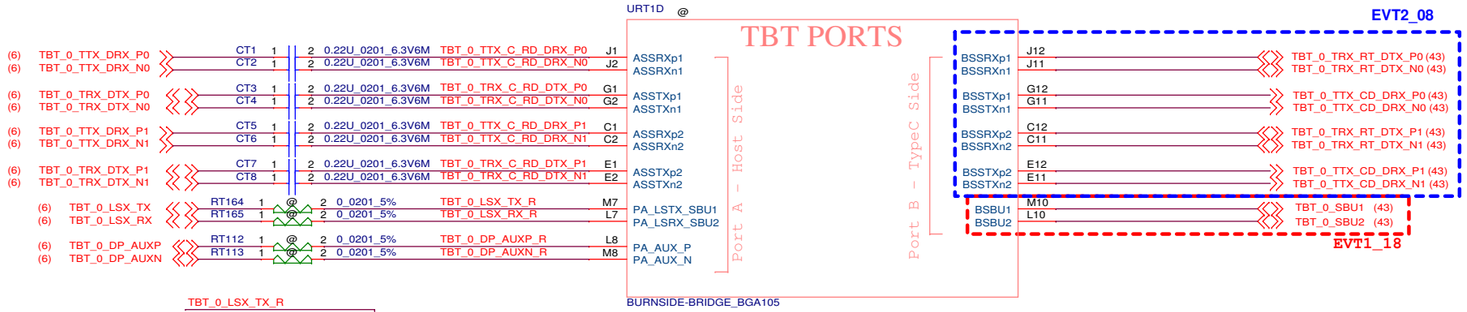
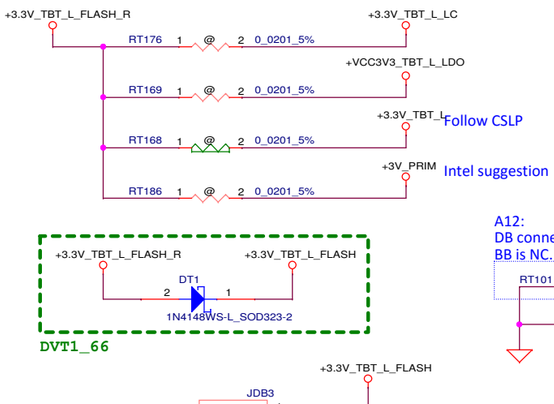
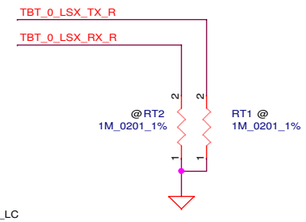
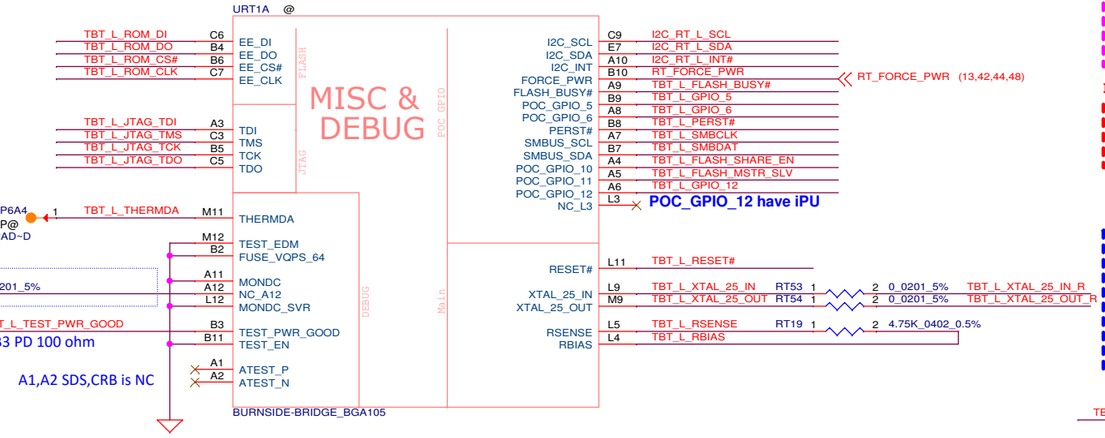
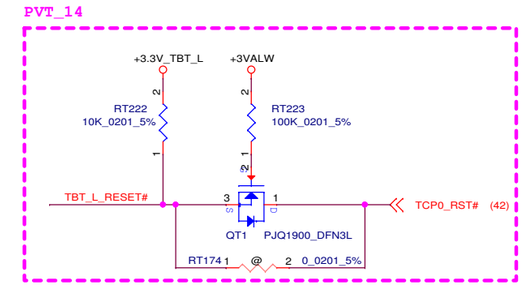
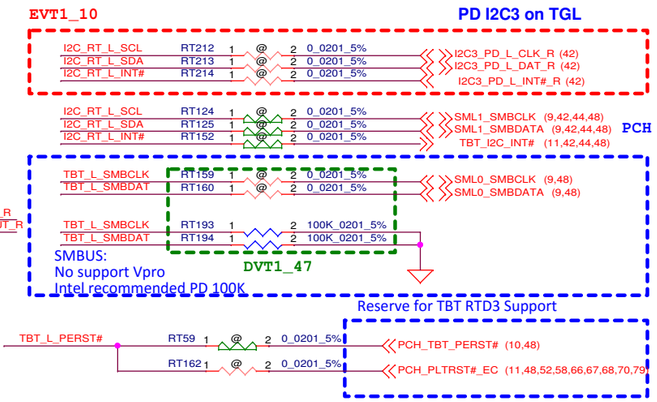


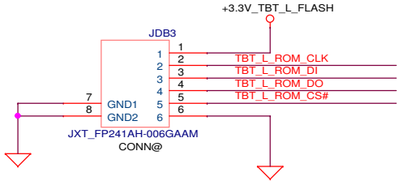


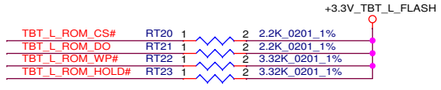


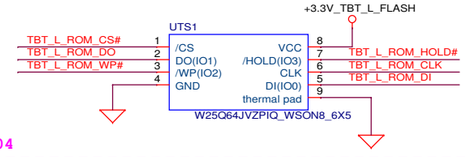




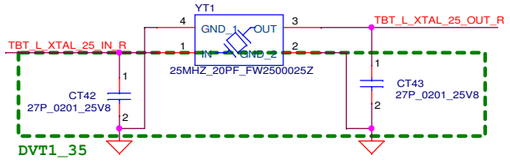


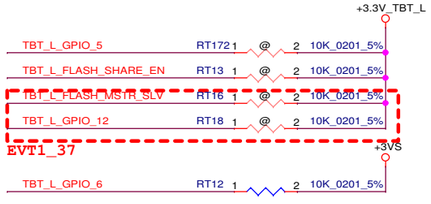


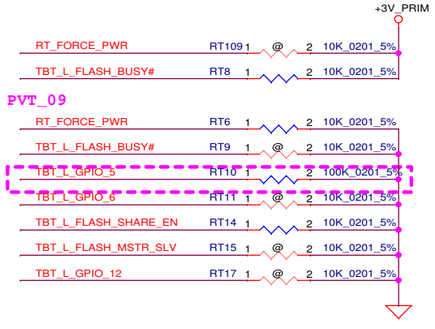


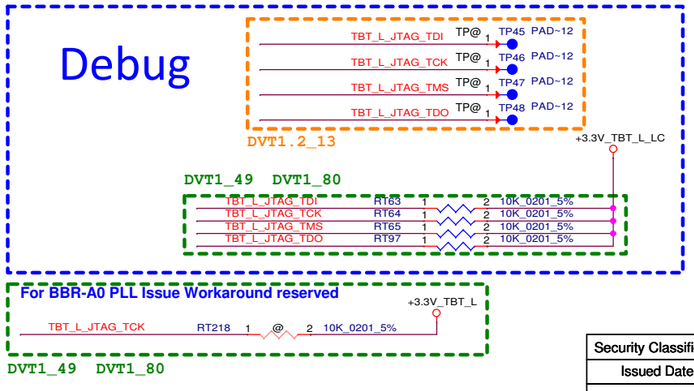


PVT_04









EVT2_08

EVT1_18

PVT_14

EVT1_10

PD I2C3 on TGL

PCH

SMBUS:
No support Vpro
Intel recommended PD 100K

DVT1_47

Reserve for TBT RTD3 Support

DVT1_66

A12:
DB connect to GND.
BB is NC.

B3 PD 100 ohm

A1,A2 SDS,CRB is NC

POC_GPIO_12 have iPU

RT_FORCE_PWR (13,42,44,48)

Follow CSLP

Intel suggestion

RT ref p.5 XTAL Recommended
FW2500025Z by Pericom
XRCGB25M000F3L12R0 by Murata

Suggest adding GND shield across Crystal and 18pF caps for better RFI.

DVT1_35

EVT1_37

PVT_09

EVT2_26

Debug

DVT1.2_13

DVT1_49 DVT1_80

For BBR-A0 PLL issue Workaround reserved

DVT1_49 DVT1_80

(L11) DG_P1_RST#:

For PD based systems, DG_P1_RST# should be output from PD.

For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR:Connect to PCH for FW update

'0' - by default

'1' - for debug only

(A9) DG_FLASH_BUSY#:conenction to PU

(A4) DG_FLSH_SHARE_EN (iPU):

'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.

'1' - Flash is shared between 2 Re-timers.

(A5) DG_FLSH_MSTR_SLV (iPU):

'0' - Set Re-timer to be Slave on shared flash SPI I/F.

'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:

'0' -Reserved for debug

'1' -Indication to S0 state for Re-timer

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	P046 - TYPE-C TBT_BB L_TCSS
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
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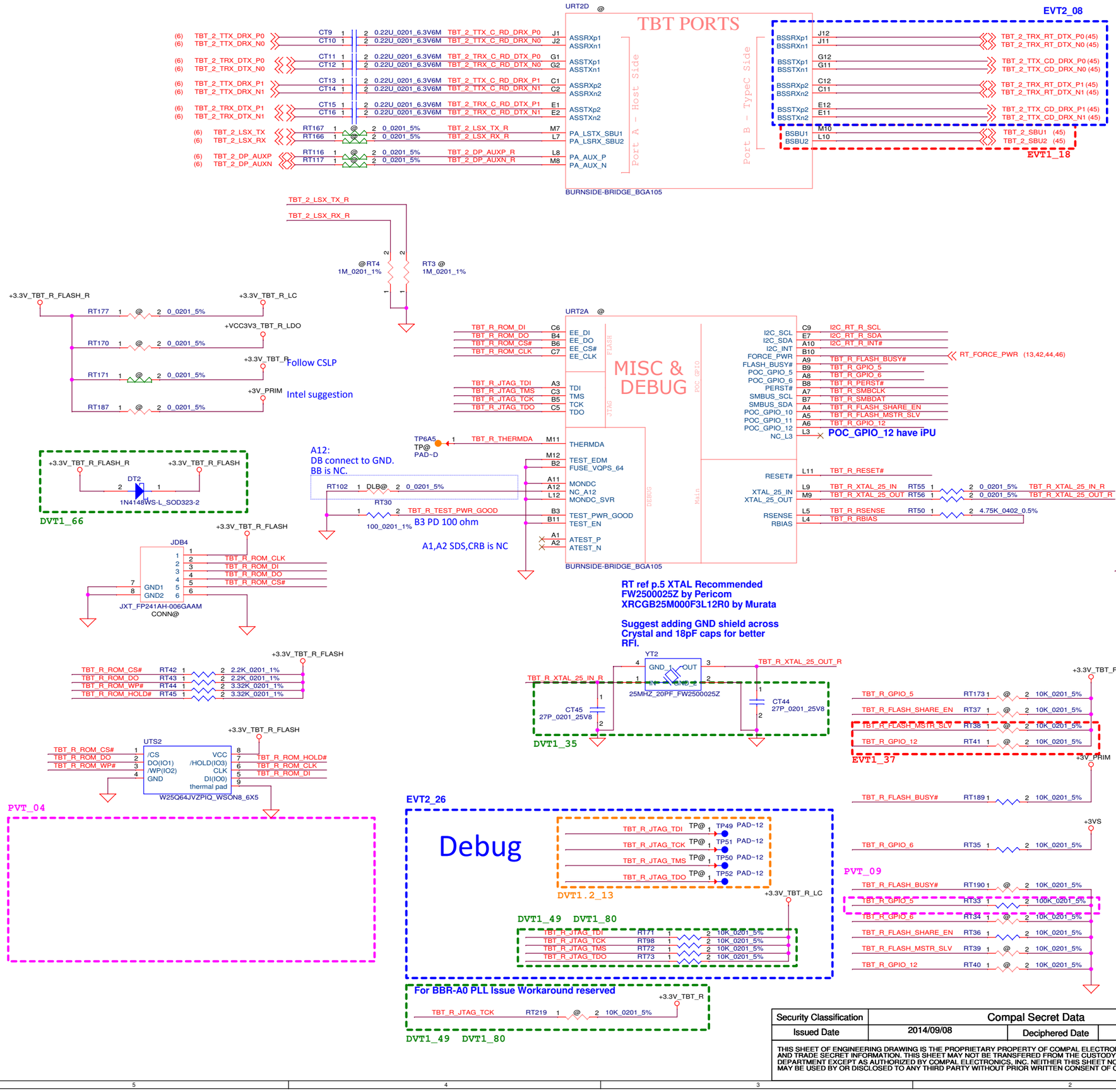
EVT2_41
+3.3V_TBT_L_LC
CT57 1U_0201_6.3V6K
Place near Pin E5
+3.3V_TBT_L_ANA
CT58 1U_0201_6.3V6K
Place near Pin L2
+0.9V_TBT_L_LVR
CT60 1U_0201_6.3V6K
CT200 10U_0402_10V6M
Place near Pin L6,M6
+0.9V_TBT_L_LC
CT59 1U_0201_6.3V6K
Place near Pin J3
+3.3V_TBT_L_ANA
+3.3V_TBT_L_LC
+0.9V_TBT_L_SVR
+0.9V_TBT_L_LC
+0.9V_TBT_L_LVR
URT1B @
L2 VCC3P3_ANA
E5 VCC3P3_LC
F6 VCC0P9_SVR_ANA_1
G6 VCC0P9_SVR_ANA_2
E3 VCC0P9_SVR_1
G3 VCC0P9_SVR_2
E9 VCC0P9_SVR_PB_ANA_1
G9 VCC0P9_SVR_PB_ANA_2
J3 VCC0P9_LC
L6 VCC0P9_LVR
M6 VCC0P9_LVR_SENSE
Power
BURNSIDE-BRIDGE_BGA105
VCC3P3_SX E6 +3.3V_TBT_L_SX RT180 0_0402_5%
VCC3P3_SVR_1 M4 +3.3V_TBT_L_SVR RT181 0_0402_5%
VCC3P3_SVR_2 M5
VCC3P3_SVR_3 J5 +3.3V_TBT_L_DB
VCC3P3A J7 RT203 DLB@ 0_0201_5%
SVR_IND_1 L1
SVR_IND_2 M1
SVR_VSS_1 M2
SVR_VSS_2 M3
NC_J6 J6 RT122 DLB@ 0_0201_5%
J5:
DB connect to +3.3V_TBT_L.
BB is NC.
+3.3V_TBT_L
+3.3VA_TBT_L
+TBT_L_SVR_IND
connect via inductor to VCC0P9_SVR
J6:
DB connect to GND.
BB is NC.
EVT2_41
+3.3V_TBT_L_SVR
CT3365 47U_0603_6.3V6M
CT163 1U_0201_6.3V6K
CT62 1U_0201_6.3V6K
+3.3V_TBT_L_SX
CT61 1U_0201_6.3V6K
Place near Pin M4, M5, J5
GND share with Pin M2, M3
3.3v @ 290mA
Place near Pin E6
3.3v @ 80mA
+3.3V_TBT_L
RT79 0_0402_5%
+3.3VA_TBT_L
CT303 10U_0402_10V6M
CT302 18P_0201_25V8J
CT64 1U_0201_6.3V6K
EVT2_41
Place near Pin J7
3.3v @ 50mA
+TBT_L_SVR_IND
LT8
0.68UH_MLV-YT10NR68N-M1L_2.7A_30%
EVT2_41
+0.9V_TBT_L_SVR
CT49 1U_0201_6.3V6K
CT50 1U_0201_6.3V6K
CT51 1U_0201_6.3V6K
CT52 1U_0201_6.3V6K
CT53 1U_0201_6.3V6K
CT54 1U_0201_6.3V6K
CT55 47U_0603_6.3V6M
CT56 18P_0201_25V8J
Place near Pin F6,G6,E3,G3,E9,G9
GND share with Pin M2, M3
0.9v @ 850mA
DVT1_06
DVT1_53 BB ref sch Rev 1.4 change to CAP Place near Pin F6,E3,E9
G3,G6,G9 CAP change to NC
+3VALW
CT361 1U_0201_6.3V6K
+3VALW
UT1
VIN_1 VIN_2 VOUT_1 VOUT_2 ON CT VBIAS GND_1 GND_2
AOZ1336DI_DFN8_2X2
+3.3V_TBT_L_B
LT3
EMI@
BLM18KG331SN1D_2P
3.3v @ 370mA
+3.3V_TBT_L
CT362 470P_0402_50V7K
CT363 0.1U_0201_10V6K
(42) PD_TCP0_LS_EN
RT83 0_0201_5%
(11,16,49,58) SIO_SLP_SUS#
RT84 0_0201_5%
3.3V_TBT_L_EN
3.3V_TBT_L_EN
RT178 100K_0201_5%
RT179 10K_0201_5%
+3VALW
EVT2_34
URT1C
GND
VSS_ANA_1 B1
VSS_ANA_2 B12
VSS_ANA_3 D1
VSS_ANA_4 D2
VSS_ANA_5 D11
VSS_ANA_6 D12
VSS_ANA_7 F1
VSS_ANA_8 F2
VSS_ANA_9 F7
VSS_ANA_10 F9
VSS_ANA_11 F11
VSS_ANA_12 F12
VSS_ANA_13 G7
VSS_ANA_14 H1
VSS_ANA_15 H2
VSS_ANA_16 H11
VSS_ANA_17 H12
VSS_ANA_18 J9
VSS_ANA_19 K1
VSS_ANA_20 K2
VSS_ANA_21 K11
VSS_ANA_22 K12
VSS_1 G5
VSS_2 F5
VSS_3 F3
BURNSIDE-BRIDGE_BGA105
@
BB ref sch p.6 note
DG_P1_PWR_GATE_EN:
For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.
For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.
Title: P047 - TYPE-C TBT_BB L_PWR,GND
Size: | Document Number: LA-G172P | Rev: 1.0 (A00)
Date: Friday, May 24, 2019 | Sheet 47 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P048 - TYPE-C TBT_BB R_TCSS			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 48 of 101		

EVT2_41

+3.3V_TBT_R_LC — CT68 1U_0201_6.3V6K — Place near Pin E5

+3.3V_TBT_R_ANA — CT69 1U_0201_6.3V6K — Place near Pin L2

+0.9V_TBT_R_LVR — EVT2_41 — CT84 1U_0201_6.3V6K, CT201 10U_0402_10V6M — Place near Pin L6,M6

+0.9V_TBT_R_LC — EVT2_41 — CT82 1U_0201_6.3V6K — Place near Pin J3

URT2B @ — BURNSIDE-BRIDGE_BGA105

+3.3V_TBT_R_ANA	L2	VCC3P3_ANA	
+3.3V_TBT_R_LC	E5	VCC3P3_LC	
+0.9V_TBT_R_SVR	F6	VCC0P9_SVR_ANA_1	
	G6	VCC0P9_SVR_ANA_2	
	E3	VCC0P9_SVR_1	
	G3	VCC0P9_SVR_2	
	E9	VCC0P9_SVR_PB_ANA_1	
+0.9V_TBT_R_LC	G9	VCC0P9_SVR_PB_ANA_2	
+0.9V_TBT_R_LVR	J3	VCC0P9_LC	
	L6	VCC0P9_LVR	
	M6	VCC0P9_LVR_SENSE	
		Power	
	E6	VCC3P3_SX	+3.3V_TBT_R_SX — RT184 — +3.3V_TBT_R
	M4	VCC3P3_SVR_1	+3.3V_TBT_R_SVR — RT185 — +3.3V_TBT_R
	M5	VCC3P3_SVR_2	
	J5	VCC3P3_SVR_3	+3.3V_TBT_R_DB — RT202 DLB@ 0_0201_5%
	J7	VCC3P3A	+3.3VA_TBT_R
	L1	SVR_IND_1	+TBT_R_SVR_IND
	M1	SVR_IND_2	
	M2	SVR_VSS_1	
	M3	SVR_VSS_2	
	J6	NC_J6	RT123 DLB@ 0_0201_5%

J5:
DB connect to +3.3V_TBT_R.
BB is NC.

connect via inductor to VCC0P9_SVR

J6:
DB connect to GND.
BB is NC.

EVT2_41

+3.3V_TBT_R_SVR — CT366 47U_0603_6.3V6M, CT372 1U_0201_6.3V6K, CT371 1U_0201_6.3V6K

+3.3V_TBT_R_SX — CT370 1U_0201_6.3V6K

Place near Pin M4, M5, J5
GND share with Pin M2, M3
3.3v @ 290mA

Place near Pin E6
3.3v @ 80mA

+3.3V_TBT_R — RT88 0_0402_5%

+3.3VA_TBT_R — CT304 10U_0402_10V6M, CT305 18P_0201_25V8J, CT81 1U_0201_6.3V6K

EVT2_41

Place near Pin J7
3.3v @ 50mA

+TBT_R_SVR_IND — LT5 0.68UH_MLV-YT10NR68N-M1L_2.7A_30%

EVT2_41 / DVT1_06

+0.9V_TBT_R_SVR — CT73 1U_0201_6.3V6K @, CT74 1U_0201_6.3V6K @, CT75 1U_0201_6.3V6K, CT76 1U_0201_6.3V6K, CT77 1U_0201_6.3V6K, CT78 1U_0201_6.3V6K @, CT79 47U_0603_6.3V6M, CT80 18P_0201_25V8J

Place near Pin F6,G6,E3,G3,E9,G9
GND share with Pin M2, M3
0.9v @ 850mA

DVT1_53 BB ref sch Rev 1.4 change to CAP Place near Pin F6,E3,E9 G3,G6,G9 CAP change to NC

+3VALW — CT211 1U_0201_6.3V6K

UT2 — AOZ1336DI_DFN8_2X2

	1	VIN_1	VOUT_1 — 7 — +3.3V_TBT_R_B — LT15 EMI@ BLM18KG331SN1D_2P — 3.3v @ 370mA +3.3V_TBT_R
	2	VIN_2	VOUT_2 — 8
	3	ON	CT — 6 — CT210 470P_0402_50V7K
	4	VBIAS	
		GND_1	5
		GND_2	9

+3.3V_TBT_R — CT212 0.1U_0201_10V6K

(44) PD_TCP2_LS_EN — RT94 0_0201_5%

(11,16,47,58) SIO_SLP_SUS# — RT95 0_0201_5% — 3.3V_TBT_R_EN

+3VALW — 3.3V_TBT_R_EN — RT93 100K_0201_5%, RT158 10K_0201_5% — EVT2_34

BB ref sch p.6 note
DG_P1_PWR_GATE_EN:

For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.

For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.

URT2C — BURNSIDE-BRIDGE_BGA105 @

B1	VSS_ANA_1	VSS_ANA_12	F12
B12	VSS_ANA_2	VSS_ANA_13	G7
D1	VSS_ANA_3	VSS_ANA_14	H1
D2	VSS_ANA_4	VSS_ANA_15	H2
D11	VSS_ANA_5	VSS_ANA_16	H11
D12	VSS_ANA_6	VSS_ANA_17	H12
F1	VSS_ANA_7	VSS_ANA_18	J9
F2	VSS_ANA_8	VSS_ANA_19	K1
F7	VSS_ANA_9	VSS_ANA_20	K2
F9	VSS_ANA_10	VSS_ANA_21	K11
F11	VSS_ANA_11	VSS_ANA_22	K12
	GND	VSS_1	G5
		VSS_2	F5
		VSS_3	F3

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

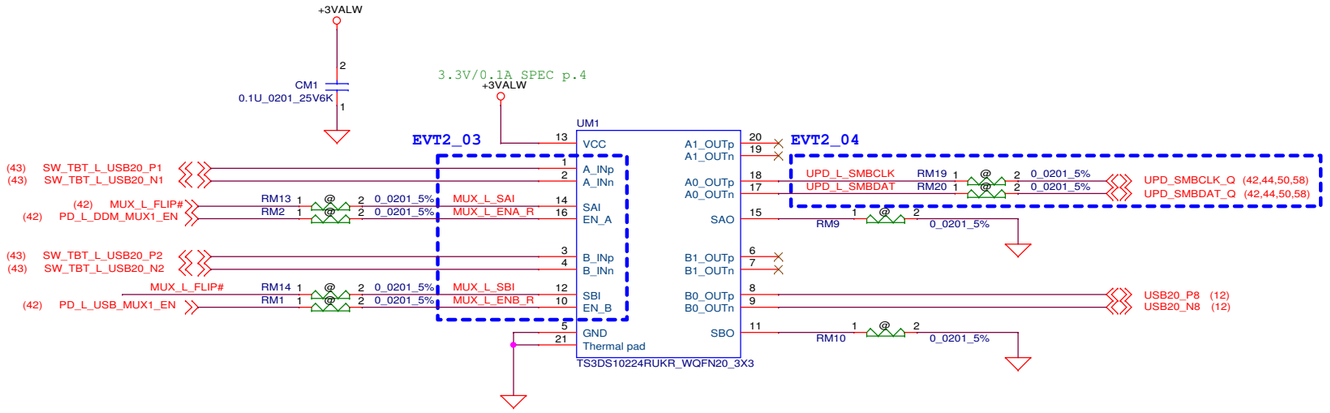
Compal Electronics, Inc.

Title: P049 - TYPE-C TBT_BB R_PWR,GND

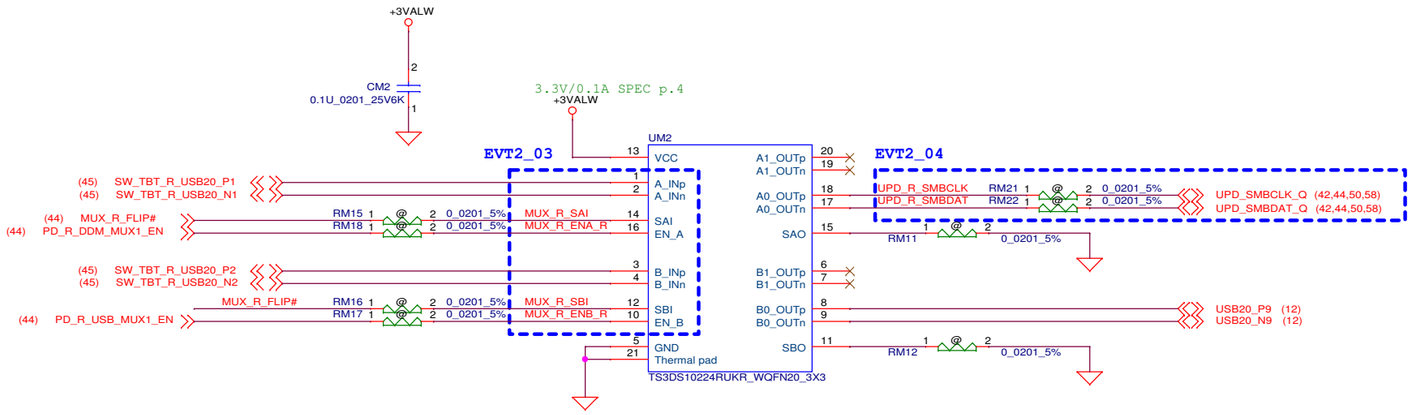
Size: | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 49 of 101

USB2/I2C MUXES_L



USB2/I2C MUXES_R



EVT1_17

ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	–	–
10	–	–	Hi-Z	Hi-Z
11	–	–	–	–

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0001	INB	–	–	INA
0010	INB	–	INB	–
0011	INB	–	–	INB
0100	–	INB	INA	–
0101	–	INB	–	INA
0110	–	INB	INB	
0111	–	INB	–	INB
1000	INA	–	INA	–
1001	INA	–	–	INA
1010	INA	–	INB	–
1011	INA	–	–	INB
1100	–	INA	INA	–
1101	–	INA	–	INA
1110	–	INA	INB	–
1111	–	INA	–	INB

Channel	INA	INB
Signal Name	TOP	BOT

					I2C	USB		
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux Functional Mode	PD Controller W/DDM
0	1	–	0	–	Hi-Z	TOP	–	USB only on TOP
0	1	–	1	–	Hi-Z	BOT	–	USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint Switch	USB on BOT W/DDM

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P050 - TYPE-C USB/I2C MUX			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 50 of 101		

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

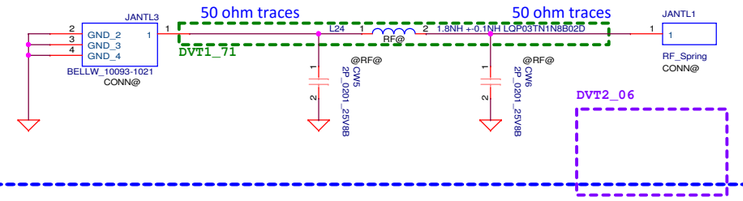
Compal Electronics, Inc.

Title: **P051 - Reserve**

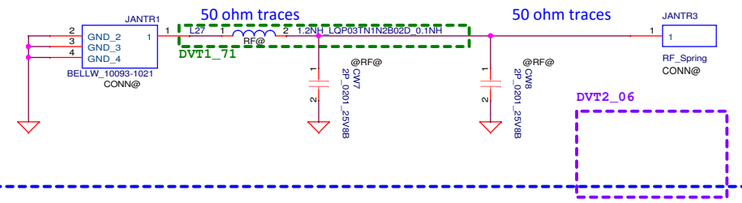
Size	Document Number	Rev
	LA-G172P	1.0 (A00)

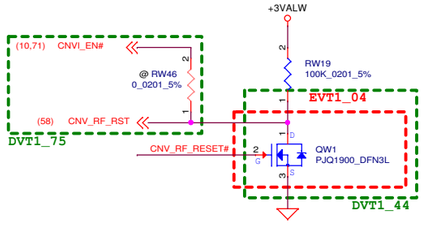
Date: Friday, May 24, 2019 Sheet 51 of 101

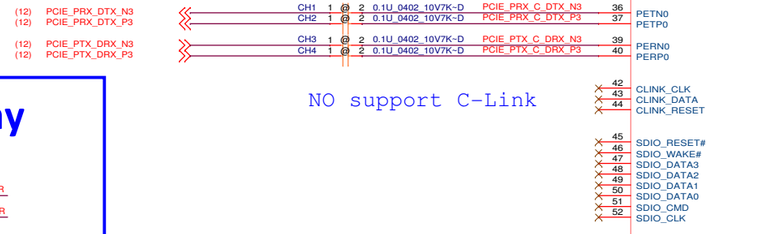
Reserved for RF Antenna L debug



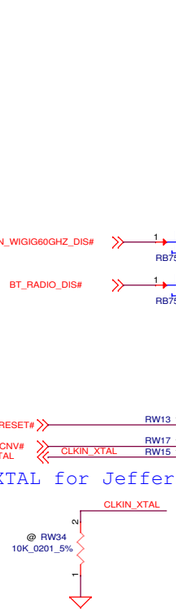
Reserved for RF Antenna R debug



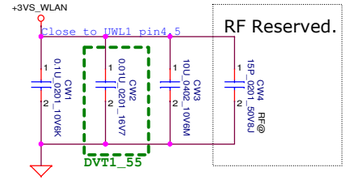


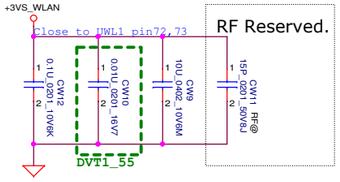


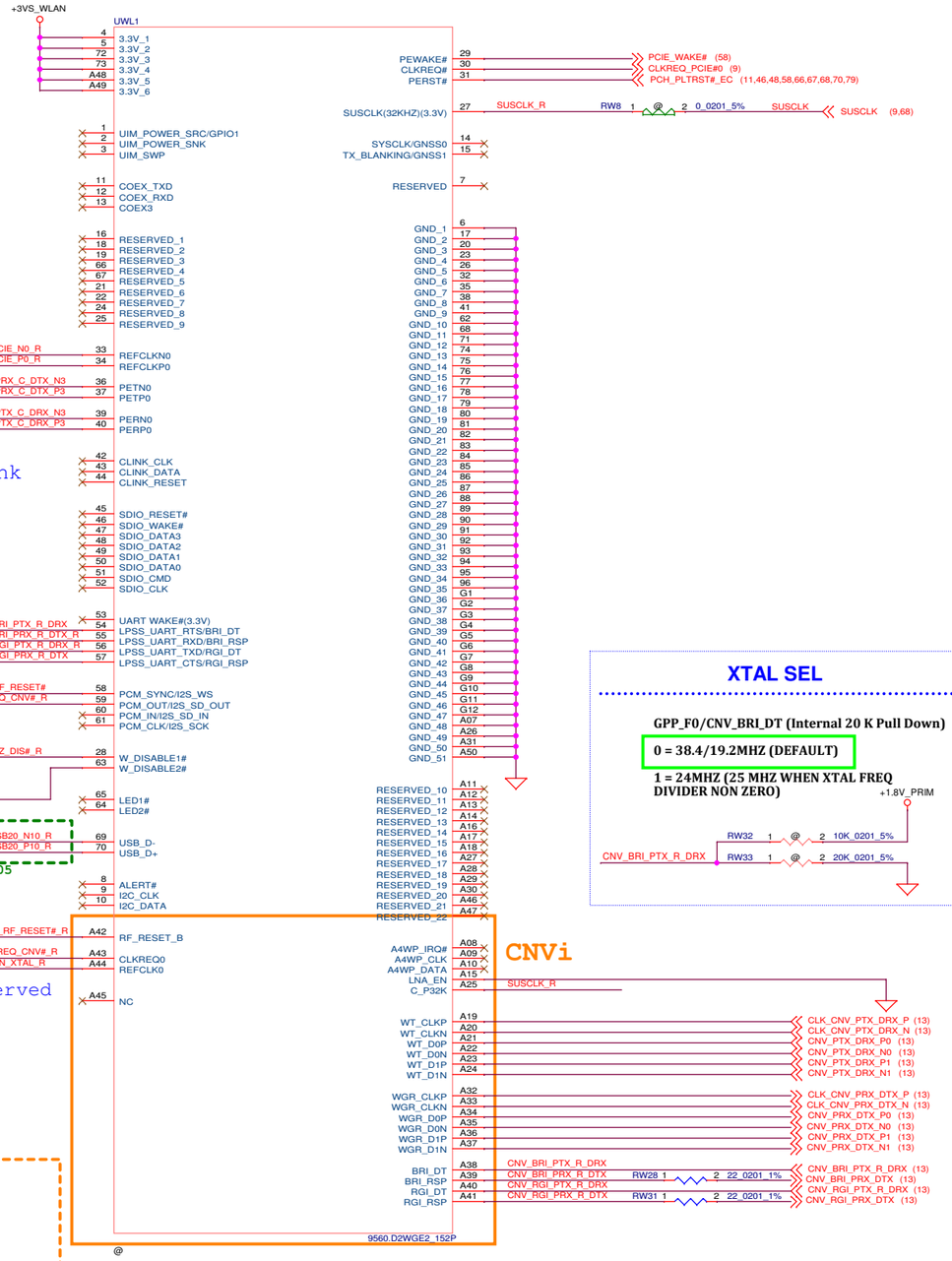
NO support C-Link

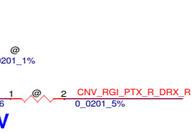


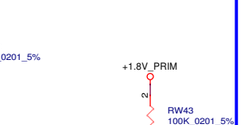
CLKIN_XTAL for Jefferson Peak reserved





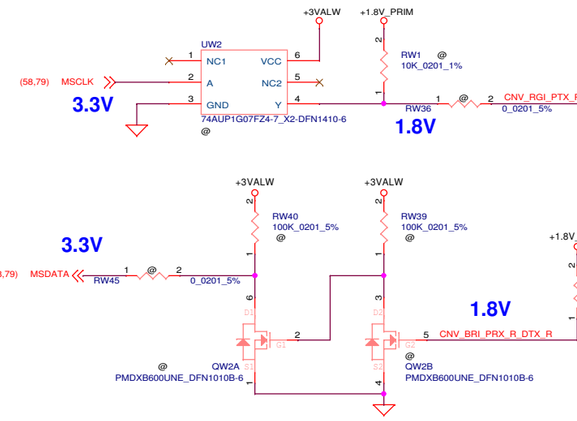




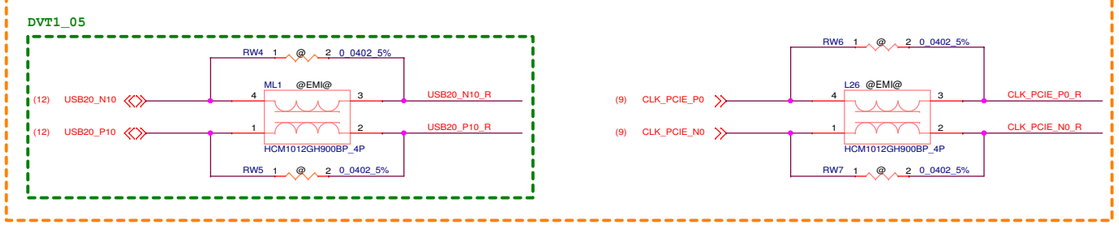


CNVi&KILLER BOM option co-lay

EC Side
MSCLK:TX
MSDATA:RX
If pop KIEER@ components ,
RE205 need de-pop



DVT1.2_17



XTAL SEL

GPP_F0/CNV_BRI_DT (Internal 20 K Pull Down)

0 = 38.4/19.2MHZ (DEFAULT)

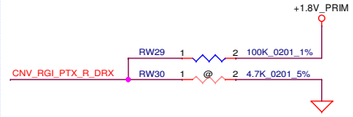
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

M.2 CNVI MODES

GPP_F2/CNV_RGI_DT

0 = INTEGRATED CNVI ENABLE

1 = INTEGRATED CNVI DISABLE



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P052 - WLAN/BT (w/ CNVi)
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	52 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P053 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 53 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P054 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 54 of 101

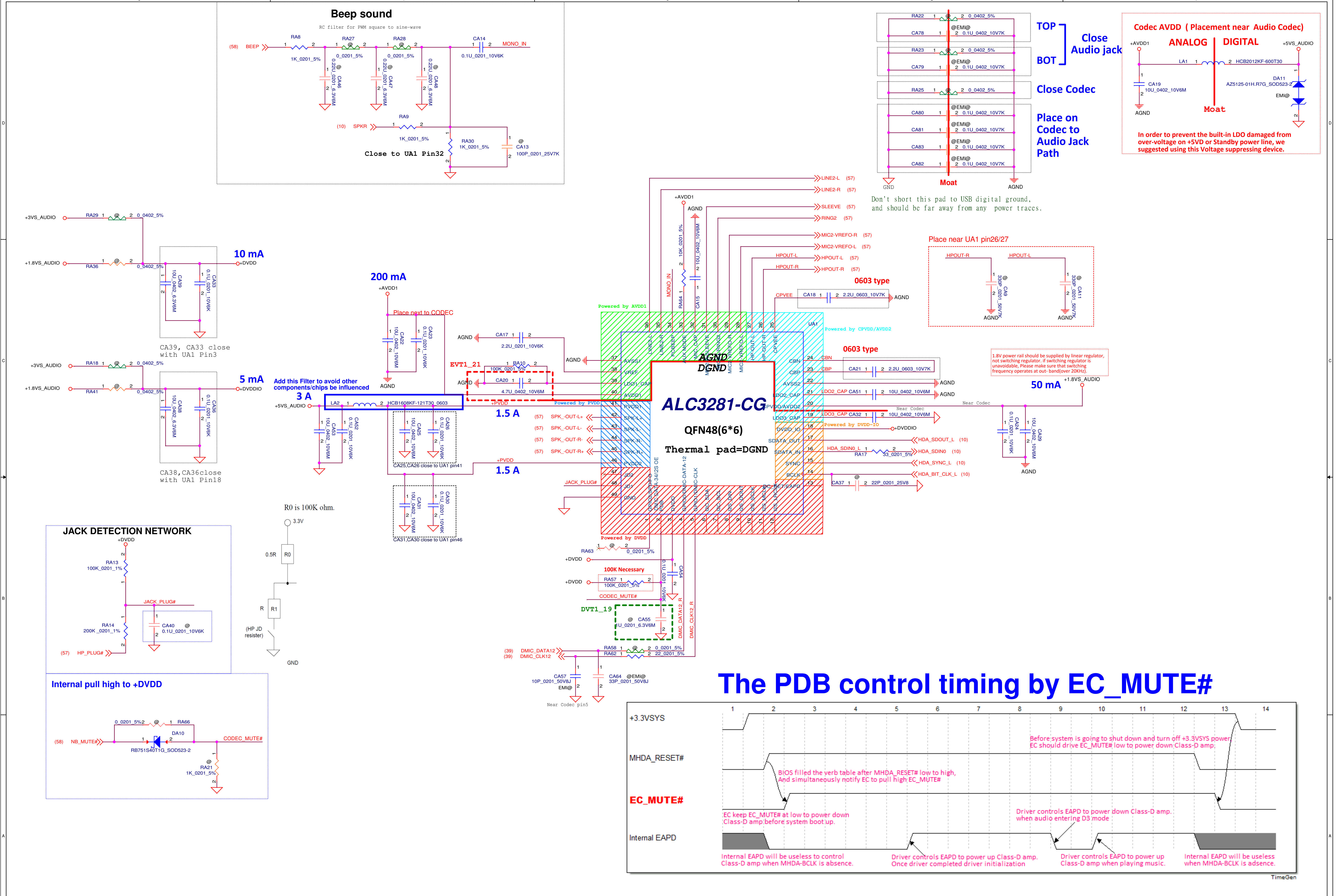
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P055 - Reserve**

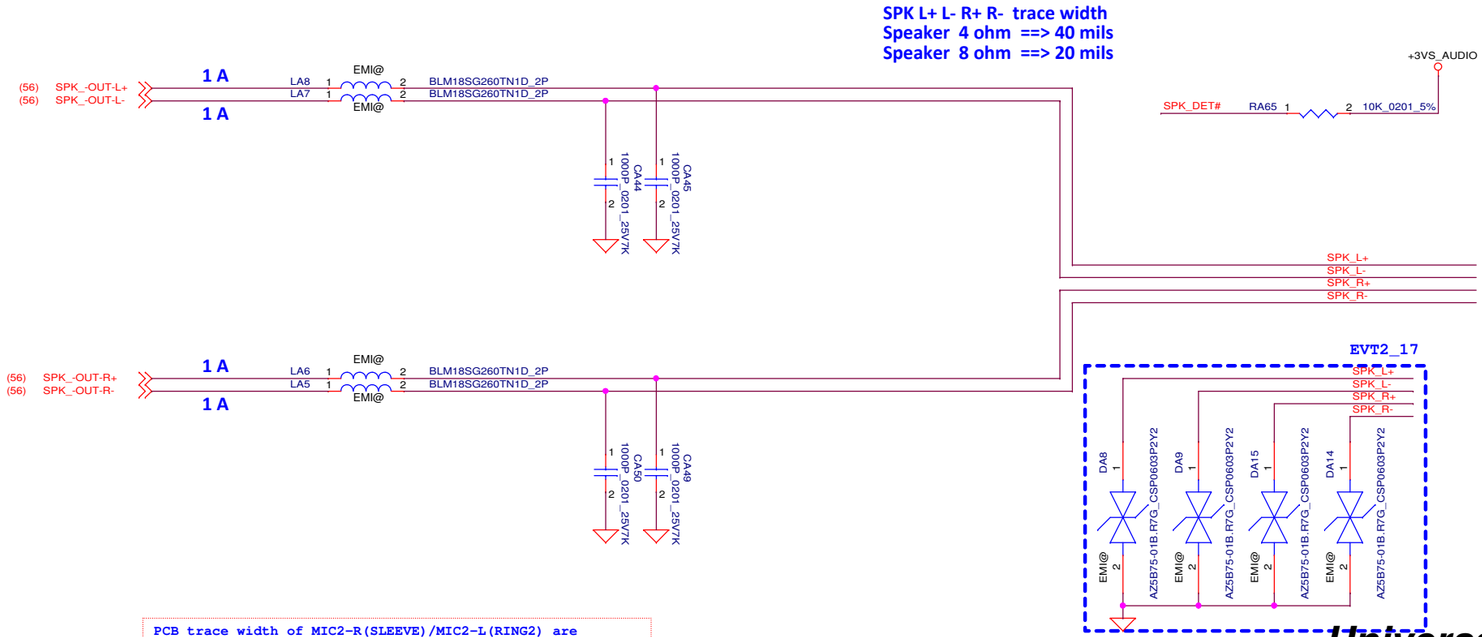
Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 Sheet 55 of 101


Beep sound
RC filter for PWM square to sine-wave
BEEP
MONO_IN
SPKR
Close to UA1 Pin32
TOP
BOT
Close Audio jack
Close Codec
Place on Codec to Audio Jack Path
Moat
Don't short this pad to USB digital ground, and should be far away from any power traces.
Codec AVDD（Placement near Audio Codec)
ANALOG
DIGITAL
In order to prevent the built-in LDO damaged from over-voltage on +5VD or Standby power line, we suggested using this Voltage suppressing device.
10 mA
CA39, CA33 close with UA1 Pin3
200 mA
Place next to CODEC
EVT1_21
Add this Filter to avoid other components/chips be influenced
3 A
1.5 A
5 mA
CA38,CA36close with UA1 Pin18
Place near UA1 pin26/27
0603 type
1.8V power rail should be supplied by linear regulator, not switching regulator. It switching regulator is unavailable, Please make sure that switching frequency operates at out- band(over 20KHz).
50 mA
Powered by AVDD1
Powered by CPVDD/AVDD2
Powered by PVDD
Powered by DVDD-IO
Powered by DVDD
AGND
DGND
ALC3281-CG
QFN48(6*6)
Thermal pad=DGND
CA25,CA26 close to UA1 pin41
CA31,CA30 close to UA1 pin46
R0 is 100K ohm.
JACK DETECTION NETWORK
100K Necessary
DVT1_19
Internal pull high to +DVDD
Near Codec pin5
The PDB control timing by EC_MUTE#
+3.3VSYS
MHDA_RESET#
EC_MUTE#
Internal EAPD
Before system is going to shut down and turn off +3.3VSYS power, EC should drive EC_MUTE# low to power down Class-D amp.
BIOS filled the verb table after MHDA_RESET# low to high, And simultaneously notify EC to pull high EC_MUTE#
EC keep EC_MUTE# at low to power down Class-D amp before system boot up.
Driver controls EAPD to power down Class-D amp. when audio entering D3 mode
Internal EAPD will be useless to control Class-D amp when MHDA-BCLK is absence.
Driver controls EAPD to power up Class-D amp. Once driver completed driver initialization
Driver controls EAPD to power up Class-D amp when playing music.
Internal EAPD will be useless when MHDA-BCLK is adsence.
TimeGen

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title: P056 - Audio ALC3281
				Size: Document Number: LA-G172P; Rev 1.0 (A00)
				Date: Friday, May 24, 2019; Sheet 56 of 101

Int. Speaker Conn.

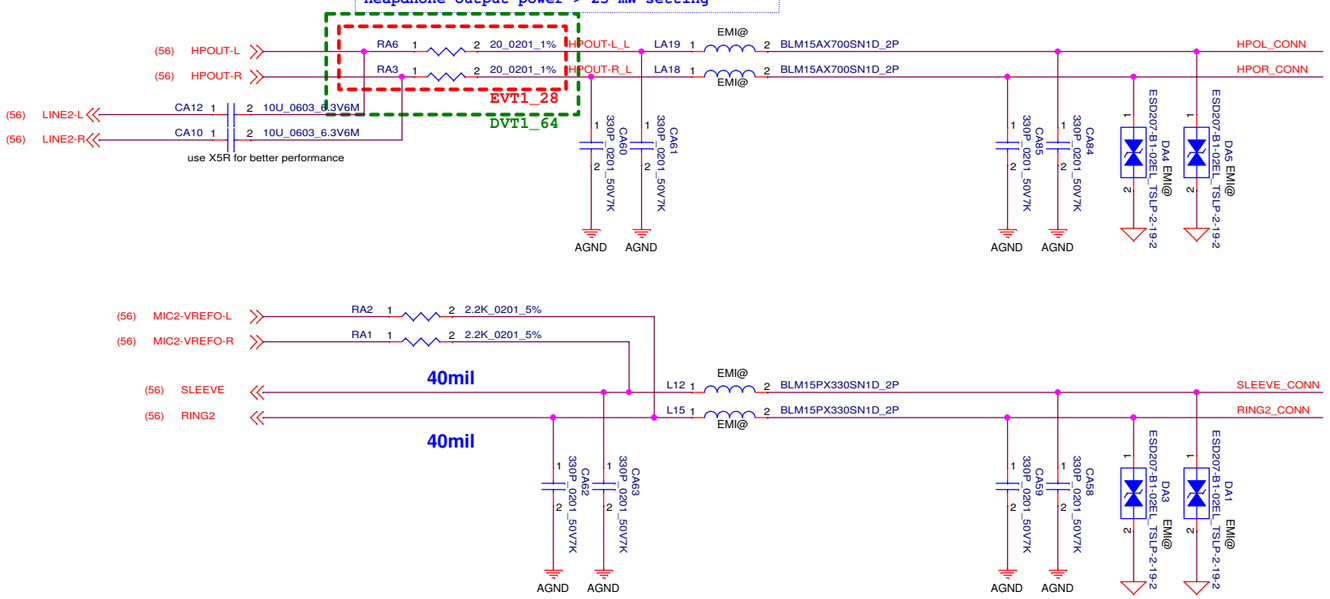


PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.

LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

Universal Audio Jack

change RA6/RA3 to 5.6 ohm to meet Dell Grade A heapdhone output power > 25 mW setting



Universal Audio Jack CONN

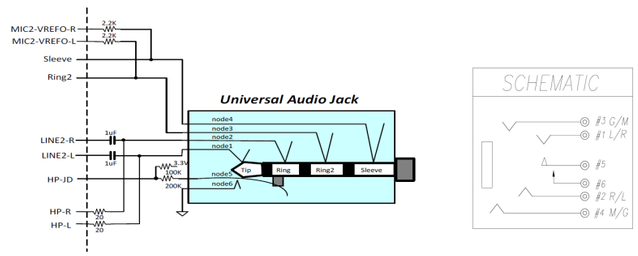
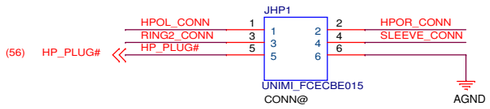
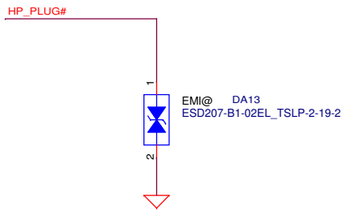


Figure 2. Analog Connector and Device



Contact with PC BEAN



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P057 - Audio Jack/Speaker			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 57 of 101		

POWER SW

DVT1_04

S5 LID OPEN POWER ON

DVT1_04

NB LID/TAB LID

DVT1_04

Touch Pad PS2

Charger and Battery

VCCIN VR

PD

System crash protection

Connect to PCH

Reserved for debug

32 KHz Clock

ESPI only support 1.8V

Setting for Thermal Design

Thermal diode mapping

MEC5105 pins	thermal diode	Location
DP1/DN1	QE4	CPU(OTP)
DN1a/DP1a	QE14	DDR
DP2/DN2	QE17	SSD
DN2a/DP2a	QE8	WLAN
DP3/DN3	QE10	Charger
DN3a/DP3a	QE3	Ambient
DP4/DN4	Reserved	Reserved
DN4a/DP4a	---	---

FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

RE194	CE75	REV
240K	4700p	M00
130K	4700p	X00
62K	4700p	X01
33K	4700p	X02
8.2K	4700p	X03
4.3K	4700p	X04
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

RE525	CE432	CPU TYPE
240K	4700p	Non V-PRO I3
130K	4700p	Non V-PRO I5
62K	4700p	Non V-PRO I7
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: P058 - EC MEC5105

Document Number: LA-G172P

Rev: 1.0 (A03)

Date: Friday, May 24, 2019 Sheet 56 of 101

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P059 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 59 of 101

Security Classification	Compal Secret Data		
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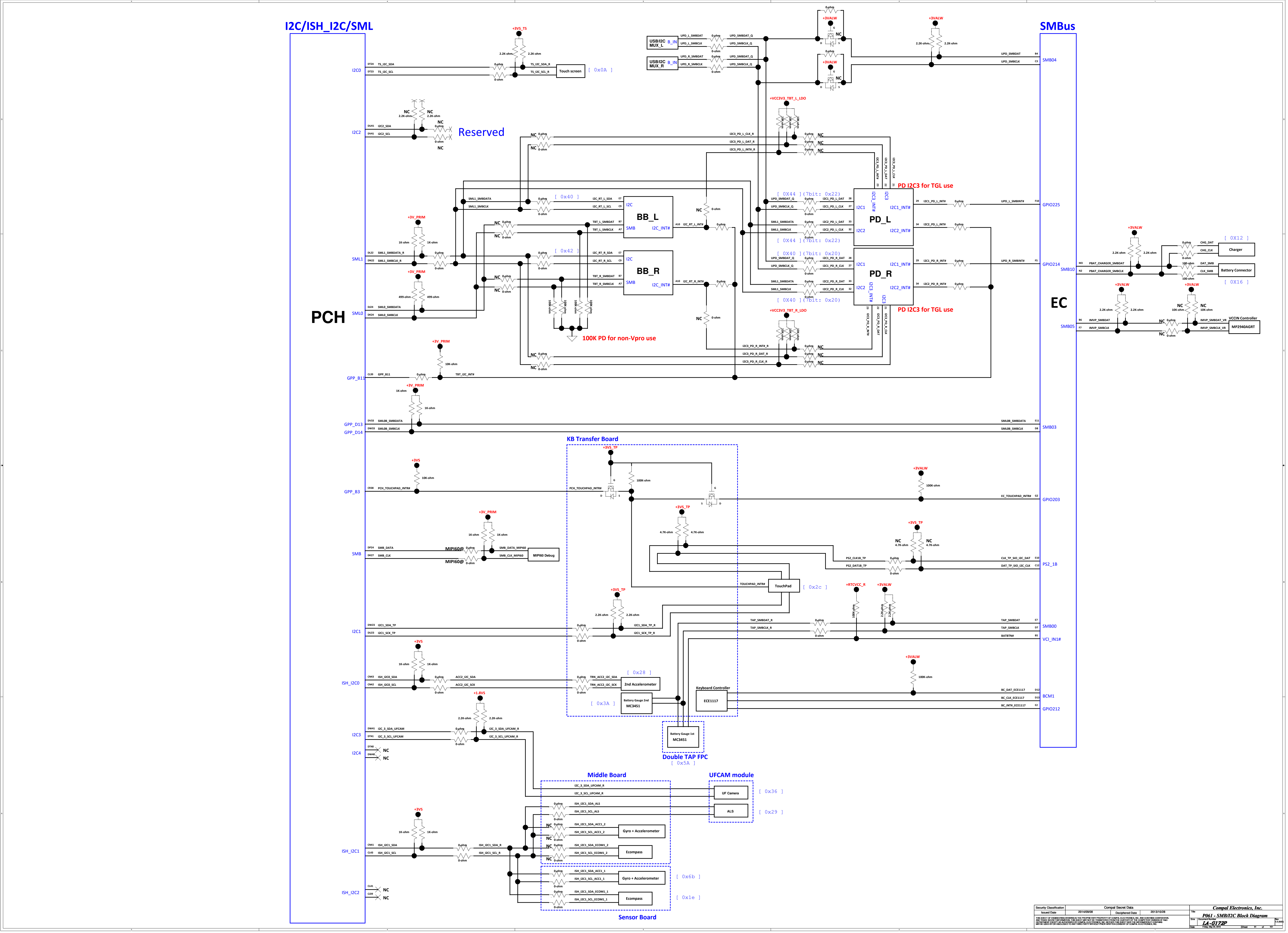
Compal Electronics, Inc.

Title: **P060 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 60 of 101


I2C/ISH_I2C/SML
SMBus
PCH
EC
I2C0
I2C2
SML1
SML0
GPP_B11
GPP_D13
GPP_D14
GPP_B3
SMB
I2C1
ISH_I2C0
I2C3
I2C4
ISH_I2C1
ISH_I2C2
SMB04
GPIO225
GPIO214
SMB10
SMB05
SMB03
GPIO203
PS2_1B
SMB00
VCI_IN1#
BCM1
GPIO212
Touch screen
[0x0A]
Reserved
BB_L
BB_R
[0x40]
[0x42]
PD_L
PD_R
PD I2C3 for TGL use
[0X44](7bit: 0x22)
[0X40](7bit: 0x20)
100K PD for non-Vpro use
Charger
Battery Connector
[0X12]
[0X16]
VCCIN Controller
MP2940AGRT
KB Transfer Board
TouchPad
[0x2c]
MIPI60 Debug
2nd Accelerometer
[0x28]
Battery Gauge 2nd MC3451
[0x3A]
Keyboard Controller
ECE1117
Battery Gauge 1st MC3451
Double TAP FPC
[0x5A]
Middle Board
UFCAM module
UF Camera
ALS
[0x36]
[0x29]
Gyro + Accelerometer
Ecompass
[0x6b]
[0x1e]
Sensor Board
Compal Electronics, Inc.
P061 - SMB/I2C Block Diagram
LA-G172P

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

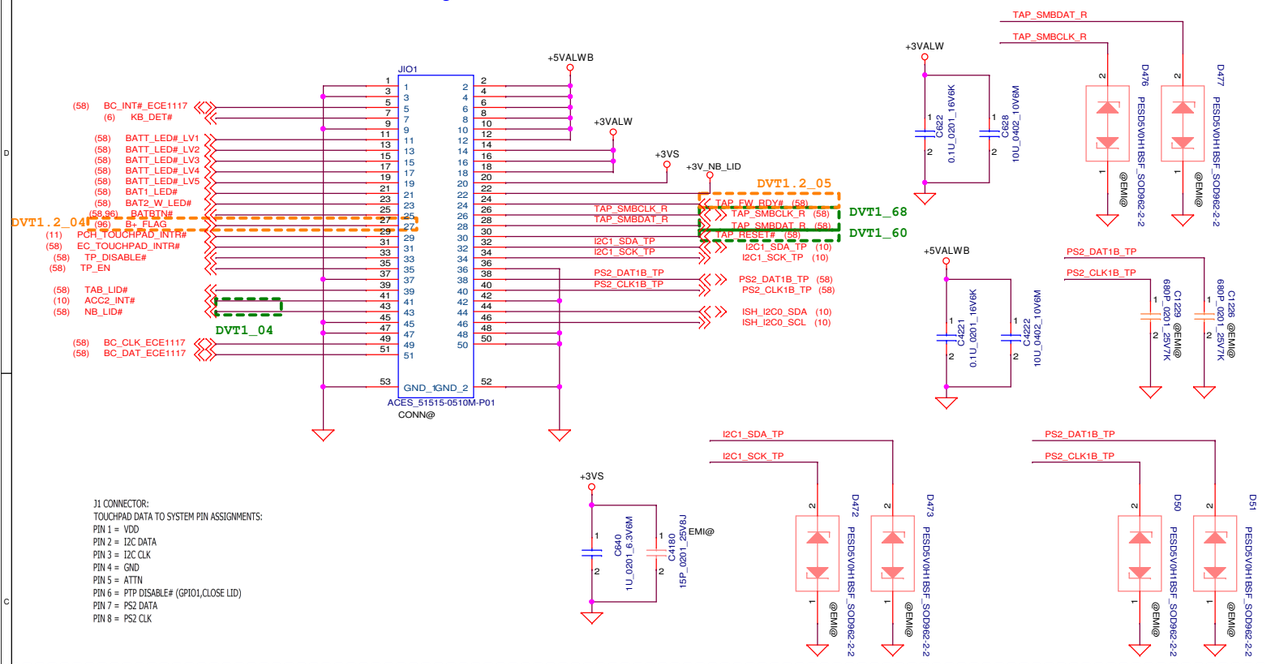
Compal Electronics, Inc.

Title: **P062 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

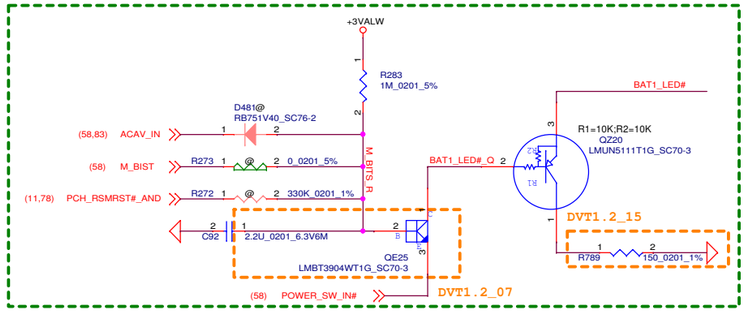
Date: Friday, May 24, 2019 Sheet 62 of 101

KB Controller & TP transfer Conn



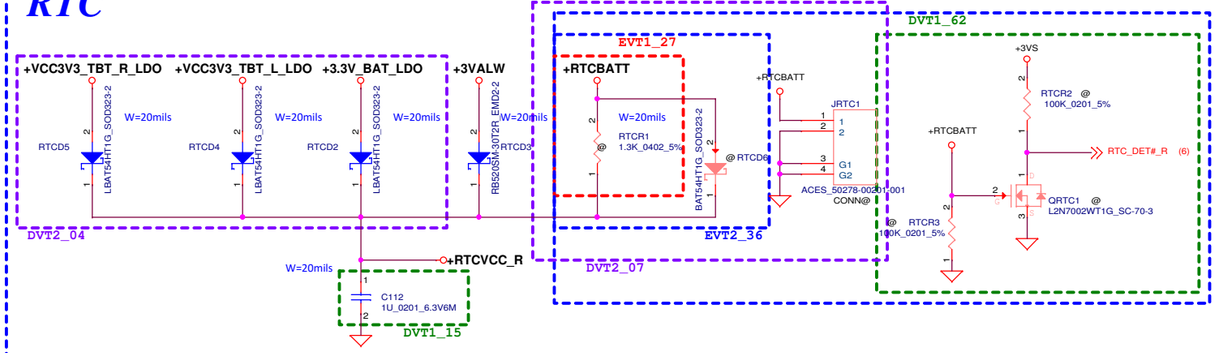
J1 CONNECTOR:
TOUCHPAD DATA TO SYSTEM PIN ASSIGNMENTS:
PIN 1 = VDD
PIN 2 = I2C DATA
PIN 3 = I2C CLK
PIN 4 = GND
PIN 5 = ATTN
PIN 6 = PTP DISABLE# (GPIO1,CLOSE LID)
PIN 7 = PS2 DATA
PIN 8 = PS2 CLK

M-BIST

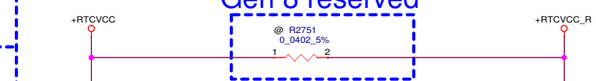


RTC

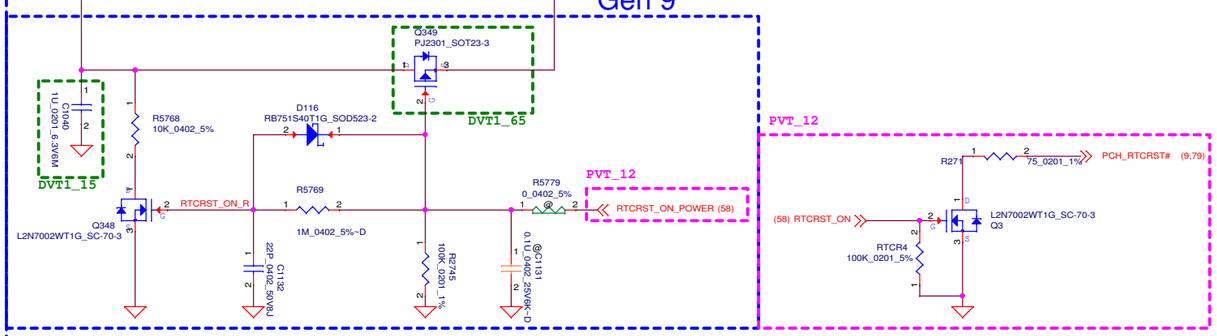
For manufacturer process use only



Gen 8 reserved



Gen 9



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P063 - KB/TP/RTC
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	63 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P064 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 64 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P065 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 65 of 101

For ST TPM

EVT1_16

DVT1.2_08

+3VALW — R626 1 @ 2 0.01_0603_1% — +3.3V_VPS_TPM

+3V_PRIM — R5717 1 @ 2 0_0603_5% — +3.3V_VPS_TPM

R687 1 @ 2 0_0402_5% — +3.3V_VPS_TPM

+3VS — R200 1 @ 2 0_0402_5% — +3VS_TPM

+3VALW — R688 1 @ 2 0_0402_5% — +3VALW_TPM

+3V_PRIM — R656 1 2 10K_0201_5% — TPM_PIRQ#_R

U712 ST33HTPH2032AHC1_VQFN32_5X5

(11,46,48,52,58,67,68,70,79) PCH_PLTRST#_EC	17	RST#	
(10) TPM_PIRQ#_R — TPM_PIRQ#_R	18	PIRQ#	
(9) PCH_SPI_CLK_R — R703 1 EMI@ 2 49.9_0201_1% — PCH_SPI_CLK_TPM	19	SCLK	
(9) PCH_SPI_CS2# — R702 1 @ 2 0_0201_5% — PCH_SPI_CS2#_TPM	20	CS#	
(9) PCH_SPI_SI_R — R700 1 2 49.9_0201_1% — PCH_SPI_SI_TPM	21	MOSI	
(9) PCH_SPI_SO_R — R701 1 2 49.9_0201_1% — PCH_SPI_SO_TPM	24	MISO	
+3VS — R649 1 @ 2 10K_0201_5%	6	GPIO	
(11,79) SIO_SLP_S0# — R747 1 @ 2 TPM_GPIO0 0_0201_5%	29	NC19	
R54 1 @ 2 TPM_GPIO0_NU 0_0201_5%	7	PP	
	9	NC6	
	16	NC13	
	23	NC14	
	32	NC22	
	2	GND	
	33	PAD	
+3.3V_VPS_TPM	22	VPS	
	14	NC11	
+3VALW_TPM	1	NC1	
	8	NC5	
	3	NC2	
	4	NC3	
	5	NC4	
	10	NC7	
	11	NC8	
	12	NC9	
	13	NC10	
	15	NC12	
	25	NC15	
	26	NC16	
	27	NC17	
	28	NC18	
	30	NC20	
	31	NC21	

EVT2_46

DVT1_45

+3VS_TPM: @ C94 10U_0402_6.3V6M; @ C95 0.1U_0201_10V6K

+3.3V_VPS_TPM: @ C421 10U_0402_6.3V6M; @ C422 0.1U_0201_10V6K

DVT1_16: C96 0.1U_0201_10V6K; C1387 10U_0402_6.3V6M; @ C97 0.1U_0201_10V6K

place C96,C97,C1387 as close as U712.22

place C421, C422 as close as U712.1

place C94, C95 as close as U712.8

For NPTC750
Depop R747,R5717
Pop C94,C95,C97,C421,C422,R54,R687,R200,R688

Close to U712

PCH_SPI_CLK_TPM — R648 33_0201_5% @EMI@ — C453 0.1U_0201_10V6K @EMI@

RF Request

+3VALW — C454 12P_0201_50V8J RF@ — C455 68P_0201_50V8J RF@

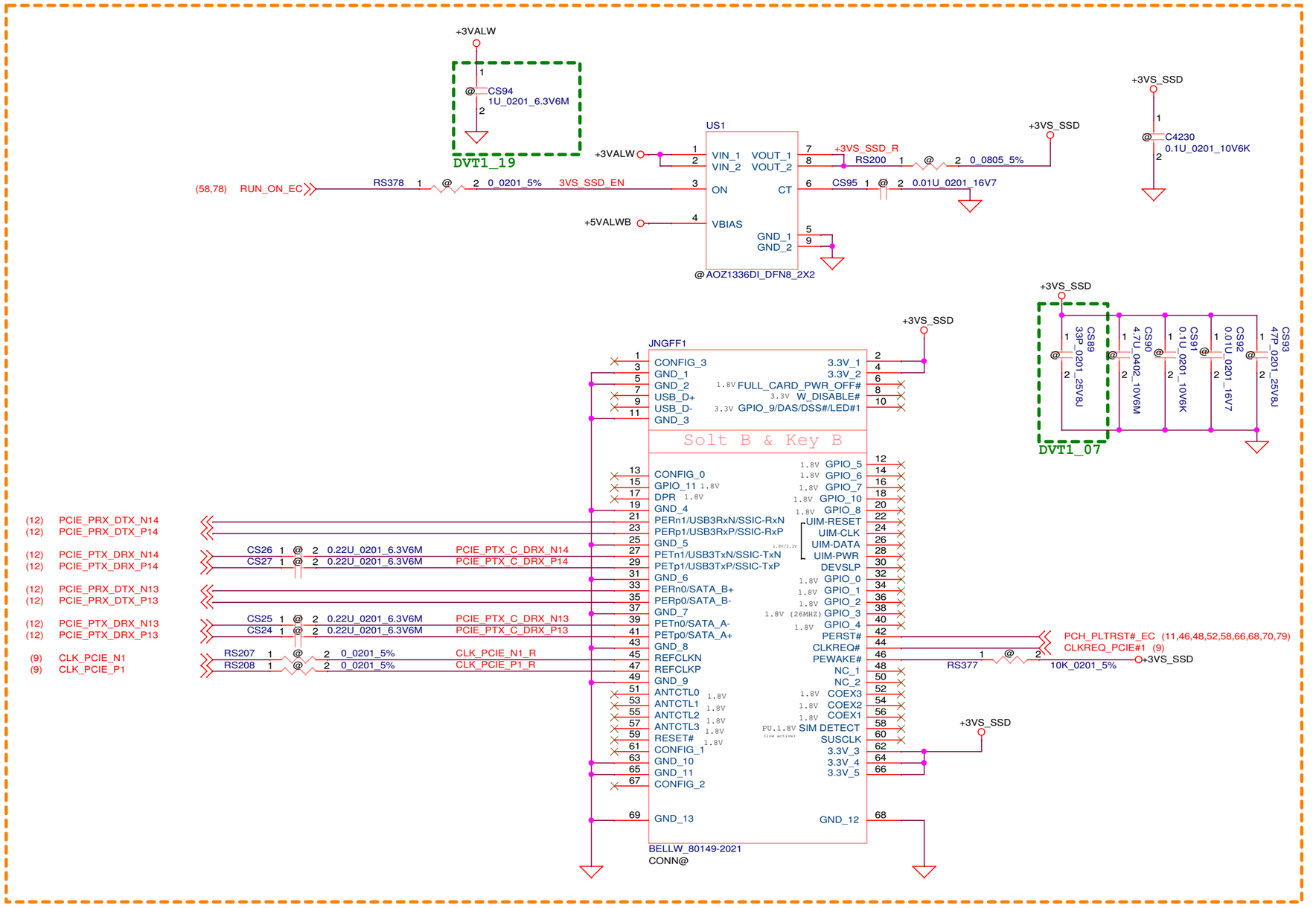
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P066 - TPM

Size | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 66 of 101



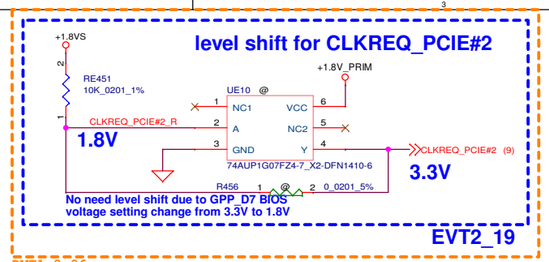
DVT1.2_16

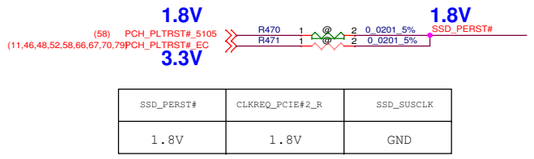
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: P067 - M.2 SSD CONN Reserve		
Size	Document Number: LA-G172P	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 67 of 101	

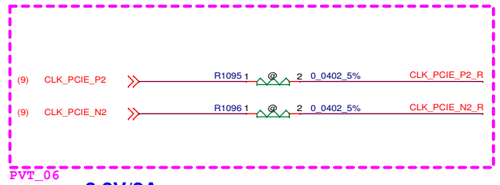
Power Rail Configuration Pins for 16x20 BGA SSD

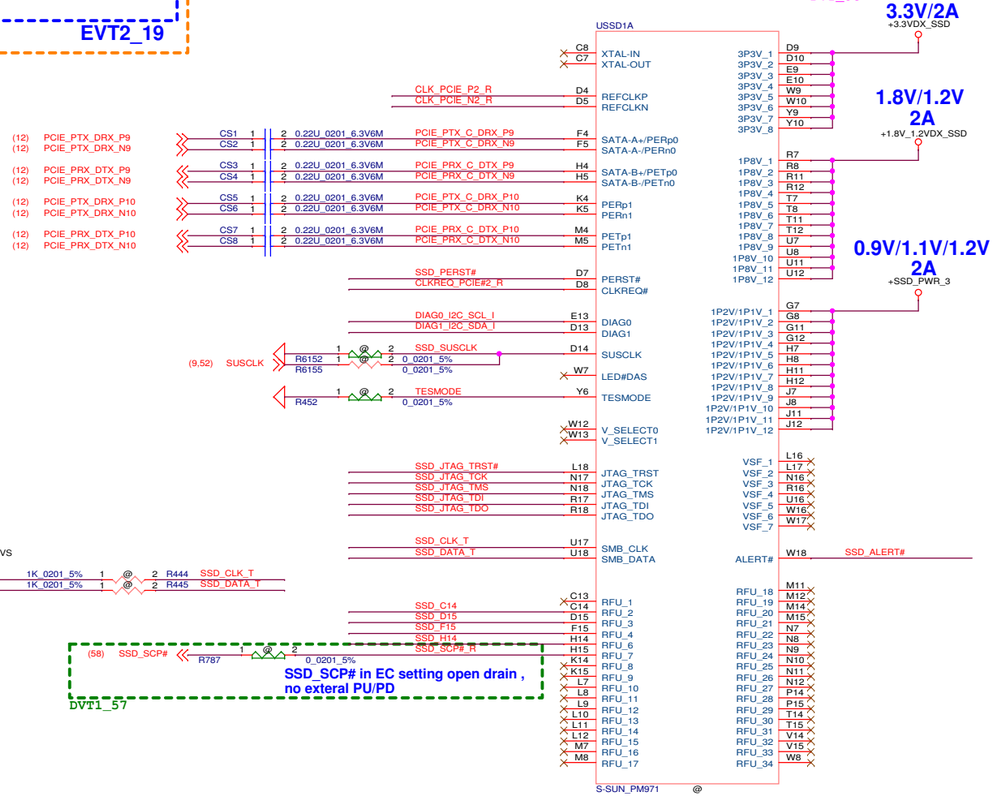
PWR_2		PWR_3			
C14	Voltage	D15	F15	H14	Voltage
GND	1.8V	GND	NC	NC	0.9V
NC	1.2V	NC	GND	NC	1.1V
		NC	NC	GND	1.2V





SSD_PERST#	CLKREQ_PCIE#2_R	SSD_SUSCLK
1.8V	1.8V	GND



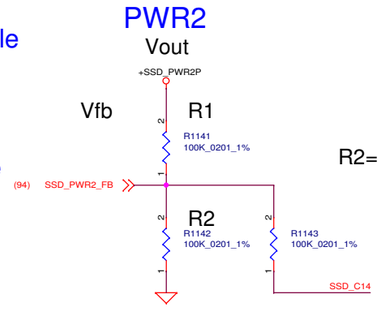


PWR2 BOM option power select table

+SSD_PWR2P	R1142	R1143
1.8V	49.9K	Non-POP
1.2V	100K	Non-POP

PWR2 SSD C14 power select table (All component POP)

+SSD_PWR2P	SSD_C14
1.8V	GND
1.2V	NC

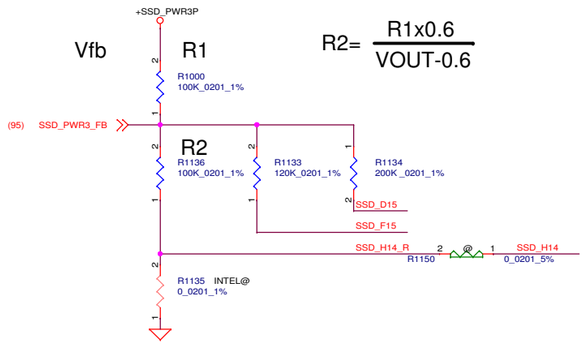


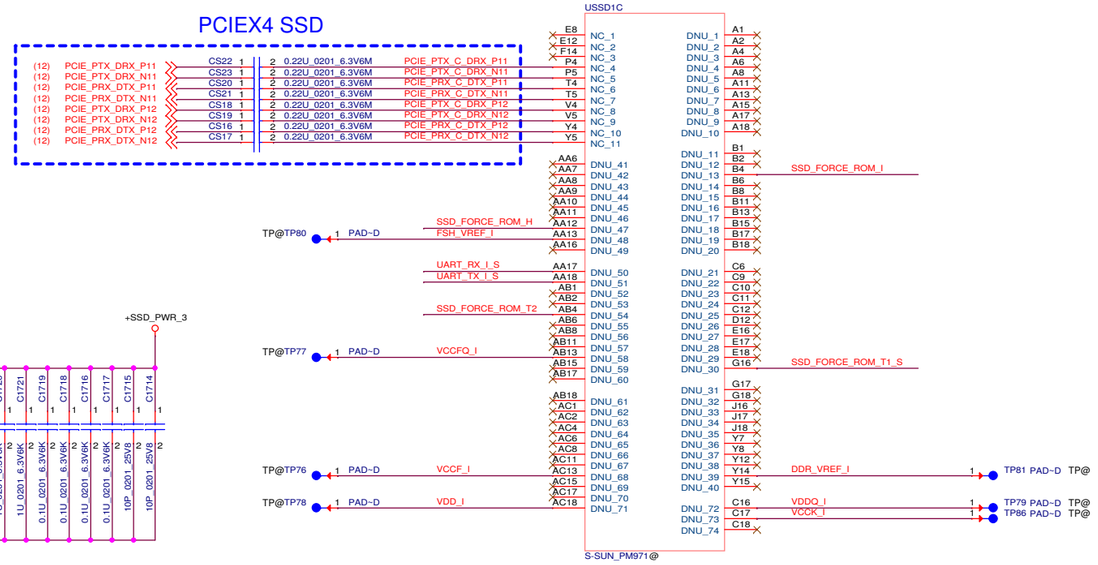
PWR3 BOM option power select table

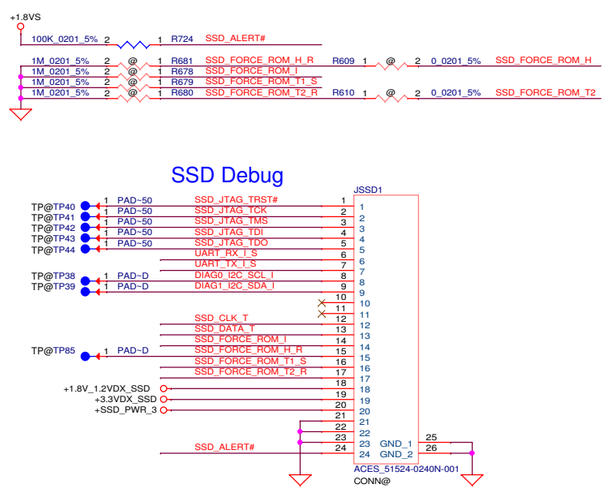
+SSD_PWR3P	R1136	R1133	R1134	R1135	R1150
0.9V	200K	Non-POP	Non-POP	POP	Non-POP
1.1V	120K	Non-POP	Non-POP	POP	Non-POP
1.2V	100K	Non-POP	Non-POP	POP	Non-POP

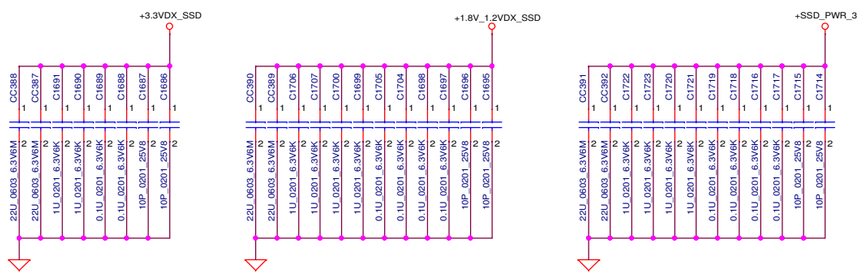
PWR3 SSD CFG power select table (All component POP , except R1135)

+SSD_PWR3P	SSD_D15	SSD_F15	SSD_H14	R1135	R1150
0.9V	GND	NC	NC	Non-POP	POP
1.1V	NC	GND	NC	Non-POP	POP
1.2V	NC	NC	GND	Non-POP	POP









Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: P068 - 1620 BGA SSD

Size: | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 68 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P065 - Reserve**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 69 of 101

Card Reader

1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
   - Bulk capacitor for Card_3V3 place closed to flash card socket.
   - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.

PVT_06

(9) CLK_PCIE_N4 — R6090 0_0402_5% — CLK_PCIE_N4_R

(9) CLK_PCIE_P4 — R6089 0_0402_5% — CLK_PCIE_P4_R

+3VS_CR

CR20 0.1U_0201_10V6K

CR23 4.7U_0402_6.3V6M

+3VS_CR

CR7 10U_0402_6.3V6M

CR8 0.1U_0201_10V6K

UCR1 RTS5242

3V3aux 27

3V3_IN 11

(11,46,48,52,58,66,67,68,75) PCH_PLTRST#_EC

(9) CLKREQ_PCIE#4

PERST#

CLK_REQ#

CLK_PCIE_P4_R

CLK_PCIE_N4_R

REFCLKP

REFCLKN

(12) PCIE_PTX_DRX_P16 — CR11 0.1U_0201_10V6K — PCIE_PTX_C_DRX_P16 — HSIP

(12) PCIE_PTX_DRX_N16 — CR21 0.1U_0201_10V6K — PCIE_PTX_C_DRX_N16 — HSIN

(12) PCIE_PRX_DTX_P16 — CR31 0.1U_0201_10V6K — PCIE_PRX_C_DTX_P16 — HSOP

(12) PCIE_PRX_DTX_N16 — CR41 0.1U_0201_10V6K — PCIE_PRX_C_DTX_N16 — HSON

(10) MEDIACARD_IRQ#_R — RR12 0_0201_5% — CD_WAKE# — WAKE#

+3VS_CR — RR11 10K_0201_1% — MS_INS#

SD_CD# — SD_CD#

Close to UR1

CR9 0.1U_0201_10V6K — DV12S — AV12 / DV12S

+SD_VDD2 — SD_VDD2

RR1 6.2K_0402_1% — RREF

Close to UR1

CR6 0.1U_0201_10V6K

CR5 4.7U_0402_6.3V6M

CARD_3V3

DV33_18

DVT1_19

+SD_VDD1

DV33_18 — 1U_0201_6.3V6M — CR15 EMC@

SP1 SD_RCLK_M_L — RR2 0_0201_5% — SD_RCLK_M

SP2 SD_RCLK_P_L — RR3 0_0201_5% — SD_RCLK_P

SP3 SD_CLK_L — RR4 0_0201_5% — SD_CLK

SP4 SD_CMD_L — RR6 0_0201_5% — SD_CMD

SP5 SD_D3_L — RR8 0_0201_5% — SD_D3

SP6 SD_D2_L — RR9 0_0201_5% — SD_D2

SP7 SP7_SDWP

CR18 2.2P_0201_50V8C @EMC@

CR17 2.2P_0201_50V8C @EMC@

CR16 2.2P_0201_50V8C @EMC@

CR13 2.2P_0201_50V8C @EMC@

CR11 2.2P_0201_50V8C @EMC@

CR10 2.2P_0201_50V8C @EMC@

DVT1_12

SD_LN1_P — SD_LN1_P

SD_LN1_M — SD_LN1_M

SD_LN0_P — SD_LN0_P

SD_LN0_M — SD_LN0_M

SDREG2 — SD_REG2

GPIO — 10K_0201_1% — RR10 — +3VS_CR

E-PAD 33

RTS5242-GR_QFN32_4X4-S

CR19 EMC@ 1U_0201_6.3V6M

DVT1_19

If GPIO not use for LED function, must be pull-high (Layout guide)

EVT2_02

JCR1

SD_D2 — DAT2

SD_D3 — CD/DAT3

SD_CMD — CMD

VDD1

SD_CLK — CLK

VSS_1

SD_RCLK_P — DAT0/RCLK+

SD_RCLK_M — DAT1/RCLK-

SD_CD# — CD

VDD2

SWIO

SD_LN0_P — D0+

SD_LN0_M — D0-

SD_LN1_M — D1-

SD_LN1_P — D1+

VSS_2 VSS_3 VSS_4

GND_1 GND_2 GND_3 GND_4

T-SOL_158-9090302600

CONN@

+SD_VDD1

Close to JCR1

CR21 10U_0402_6.3V6M

CR25 0.1U_0402_10V7K

+SD_VDD2

CR22 4.7U_0402_6.3V6M

CR24 0.1U_0402_10V7K

EVT1_04

For GPIO control SD_WP

QR1 PJQ1900_DFN3L

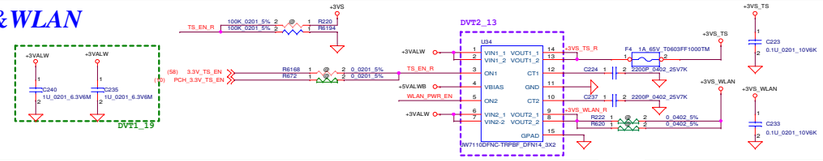
SP7_SDWP

(10) HOST_SD_WP#

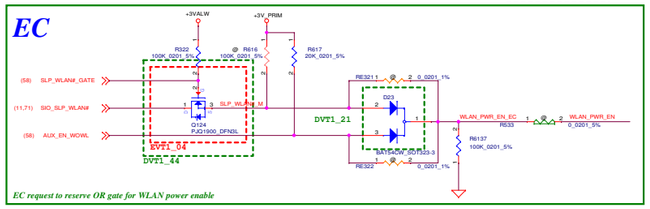
DVT1_44

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title: P070 - Card reader uSD RTS5242
				Size: — Document Number: LA-G172P — Rev: 1.0 (A00)
				Date: Friday, May 24, 2019 — Sheet 70 of 101

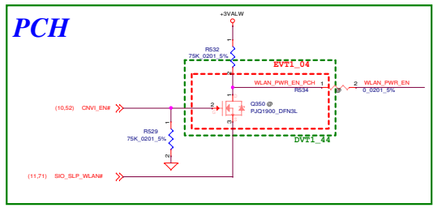
TS&WLAN



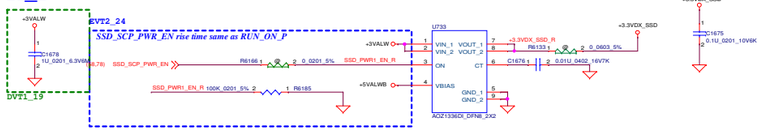
EC



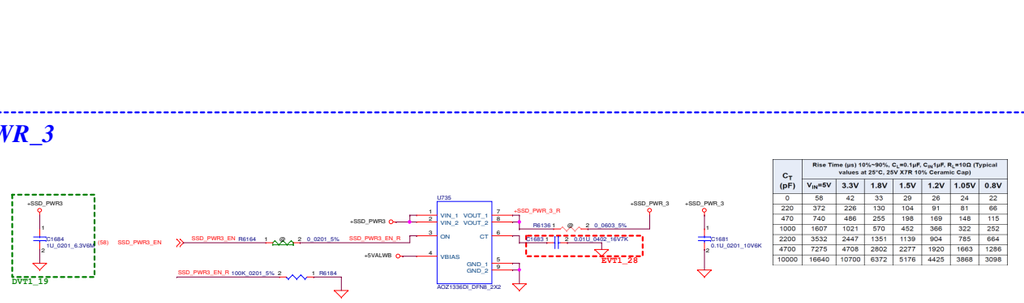
PCH



SSD_PWR_1

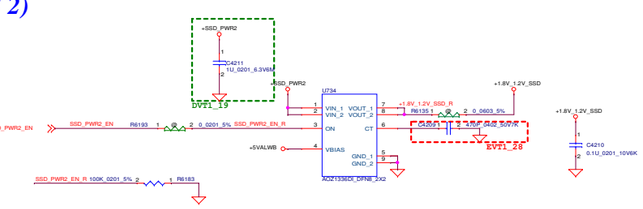


SSD_PWR_3

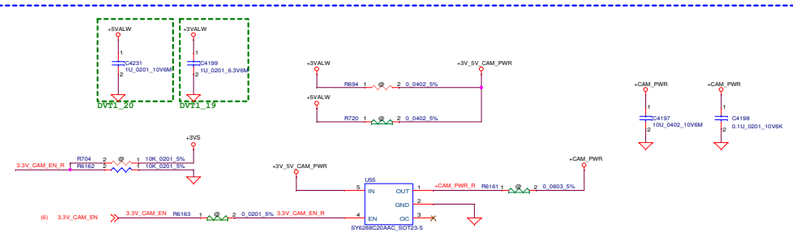


C_T (pF)	Rise Time (µs) 10%~90%, C_L=0.1µF, C_{IN}=1µF, R_L=10Ω (Typical values at 25°C, 25V X7R 10% Ceramic Cap)							
	V_{IN}=5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V	
0	58	42	33	29	26	24	22	
220	372	226	130	104	91	81	66	
470	740	486	255	198	169	148	115	
1000	1607	1021	570	452	366	322	252	
2200	3532	2447	1351	1139	904	785	664	
4700	7275	4708	2802	2277	1920	1663	1286	
10000	16640	10700	6372	5176	4425	3868	3098	

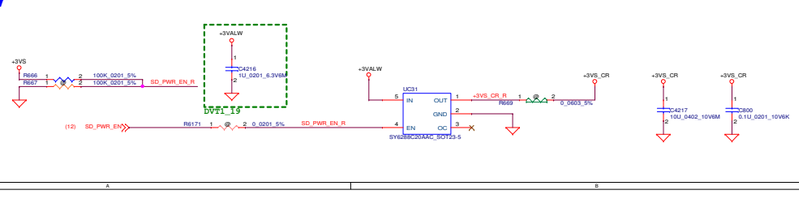
SSD_PWR_2(GEN 2)



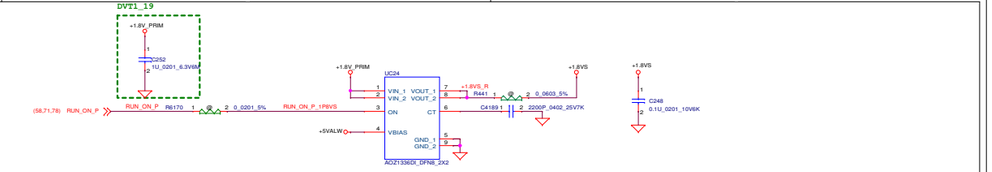
CAMERA



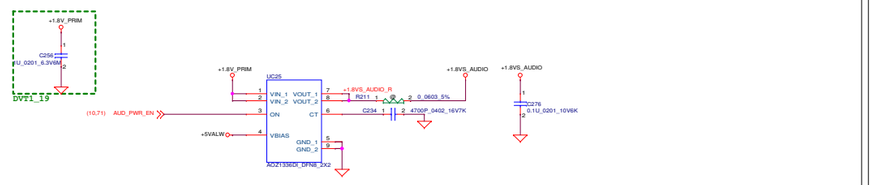
Card Reader



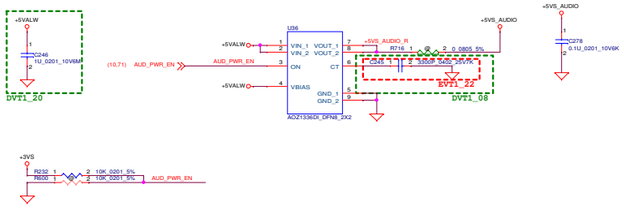
1.8VS



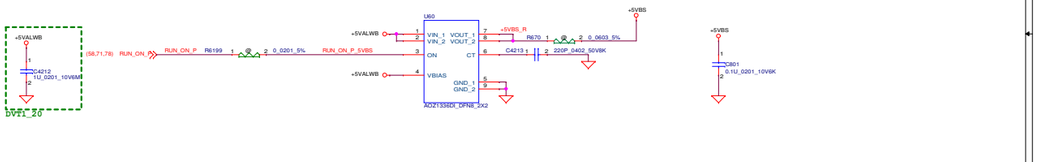
1.8VS_AUDIO



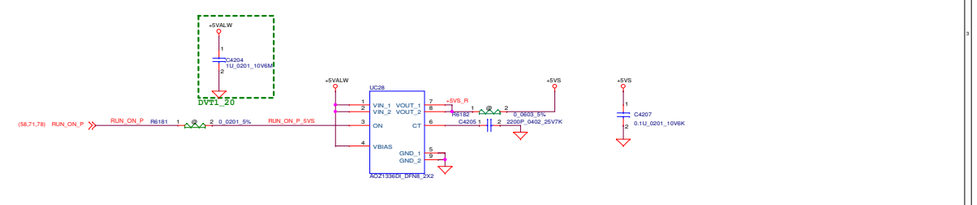
5VS_AUDIO



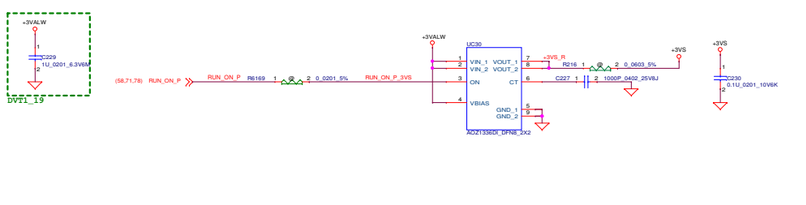
5VBS



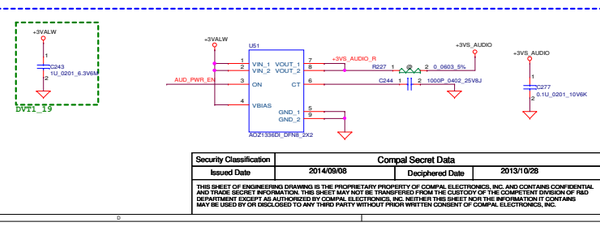
5VS



3VS



3VS_AUDIO



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Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Title	P071 - DC/DC		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet 71 of 101	

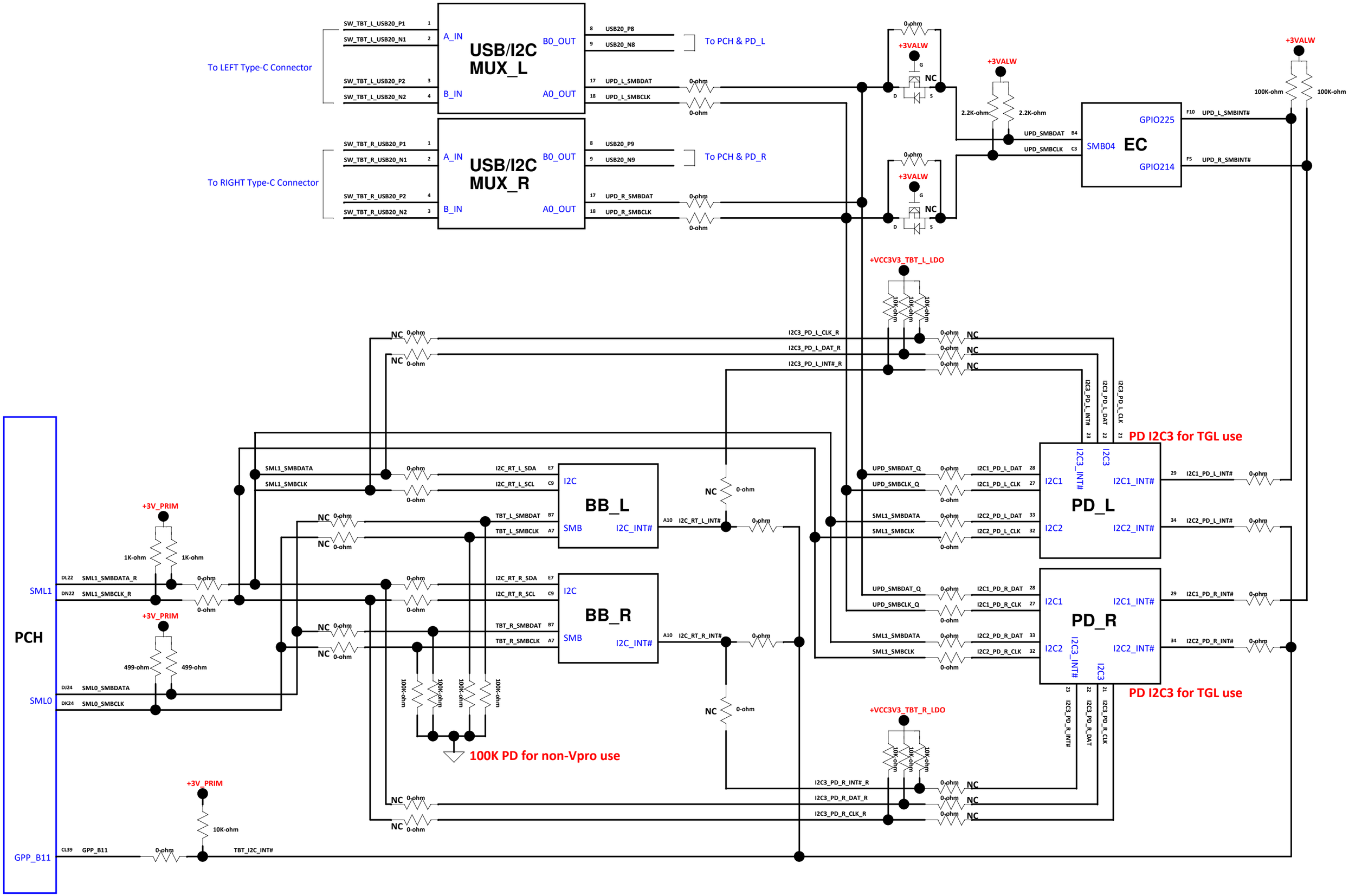
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P072 - Reserve**

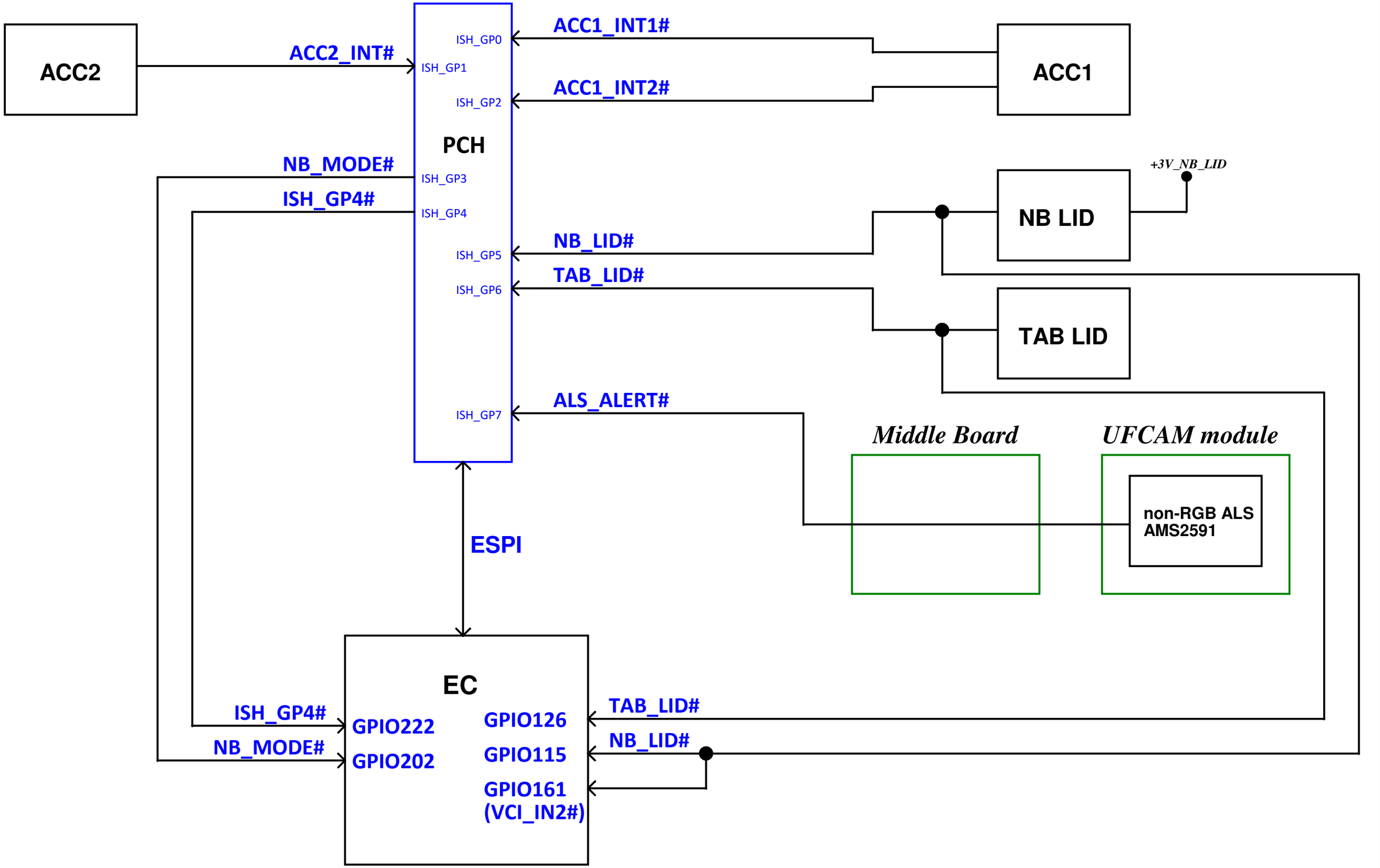
Size	Document Number	Rev
	LA-G172P	1.0 (A00)

Date: Friday, May 24, 2019 Sheet 72 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P073 -TBT I2C/SML block diagram		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet 73 of 101	



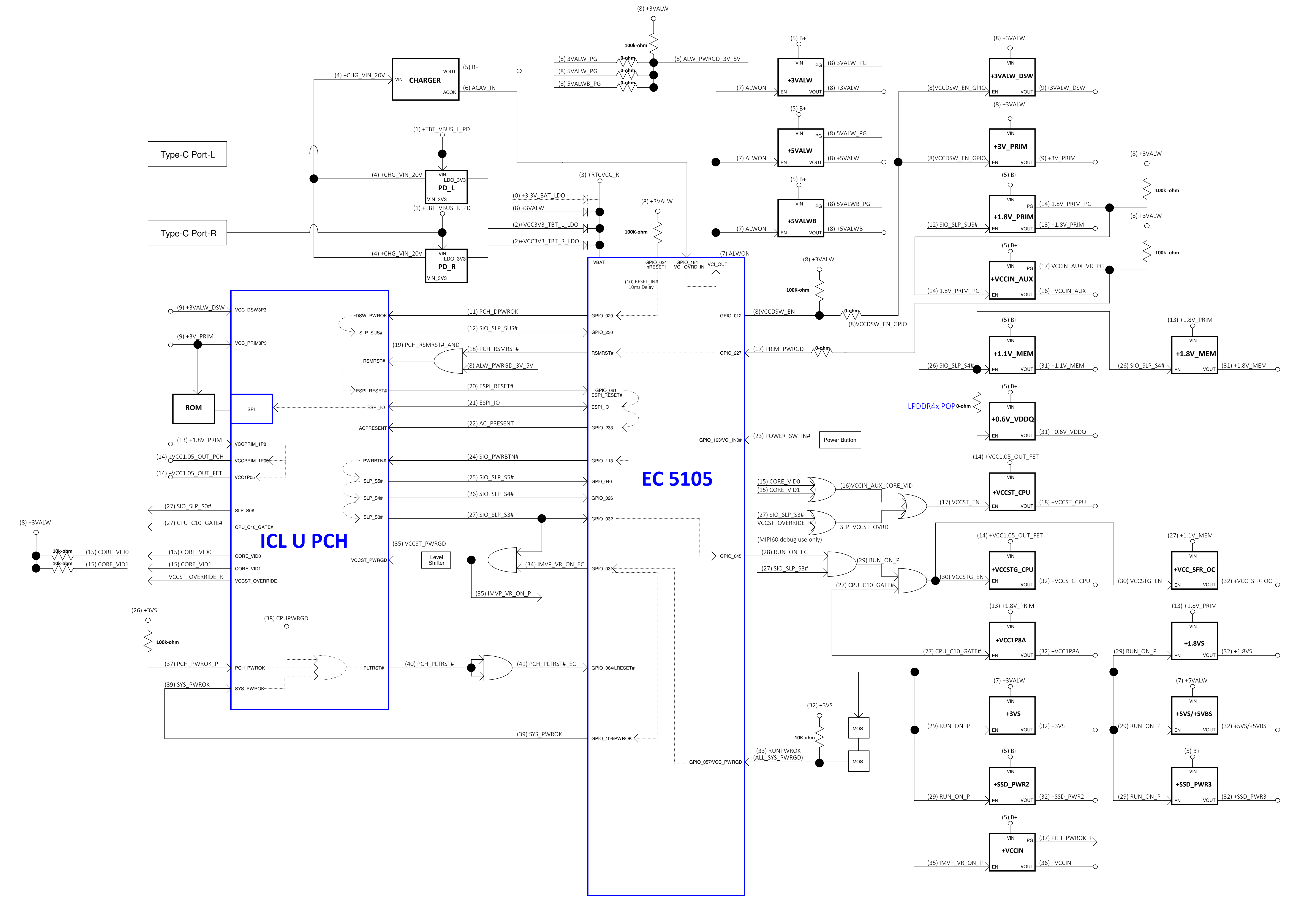
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P074 - Sensor block diagram

Size | Document Number: LA-G171P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 74 of 101



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date 2013/10/28	Title: P075 - AC_Power up Sequence
			Document Number: LA-G172P, Rev 1.0 (A00)
			Date: Friday, May 24, 2019 — Sheet 75 of 101

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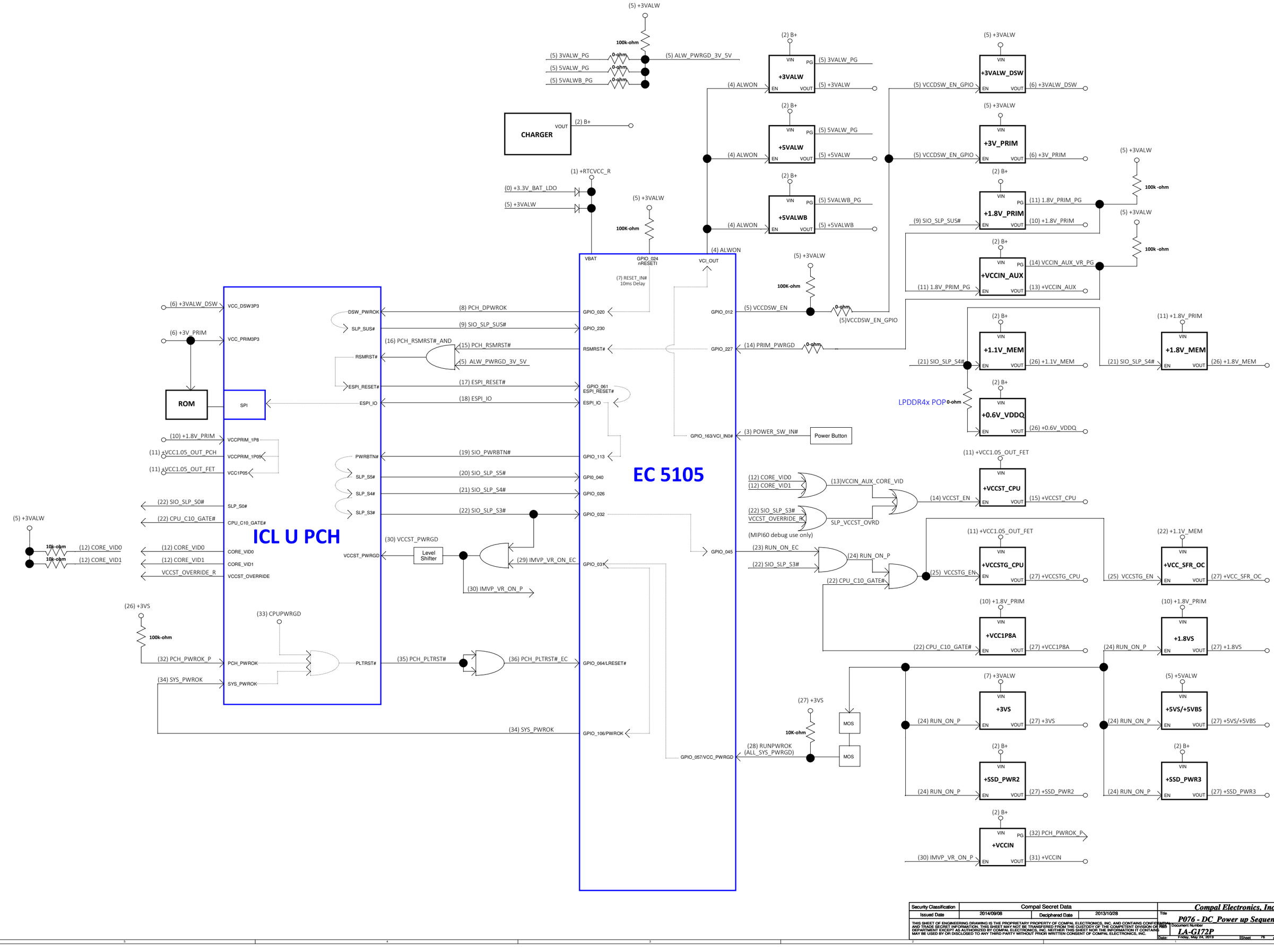

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: P076 - DC_Power up Sequence

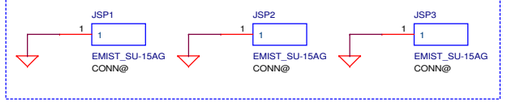
Document Number: LA-G172P

Rev: 1.0 (A00)

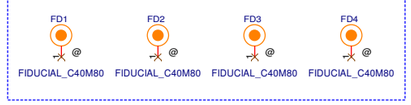
Date: Friday, May 24, 2019 | Sheet 76 of 101

Screw Hole

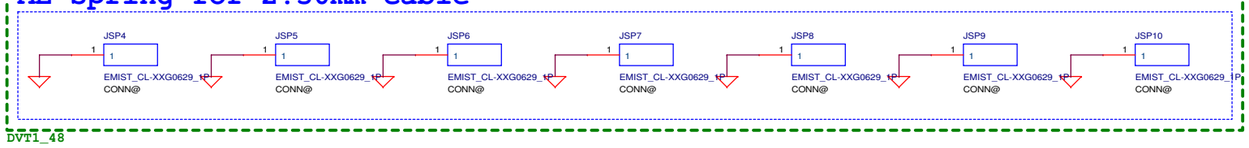
ME Spring for 1.13mm cable



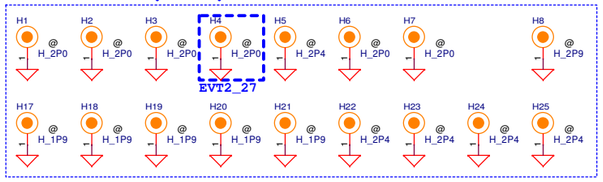
Fiducial Mark



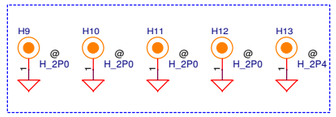
ME Spring for 2.50mm cable



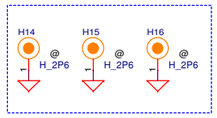
PCB X 17(PTH)



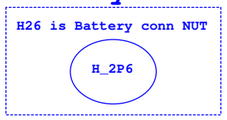
CPU X 5



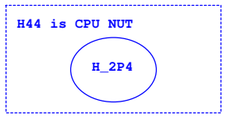
RF X 3



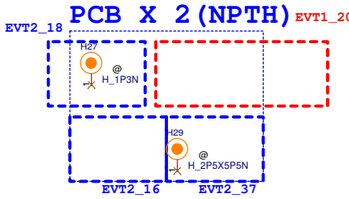
Battery X 1



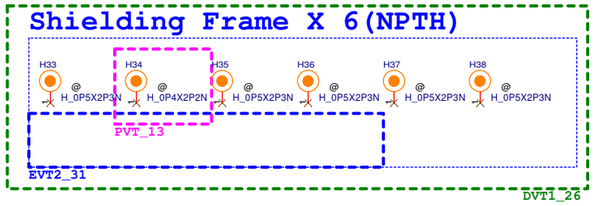
CPU X 1



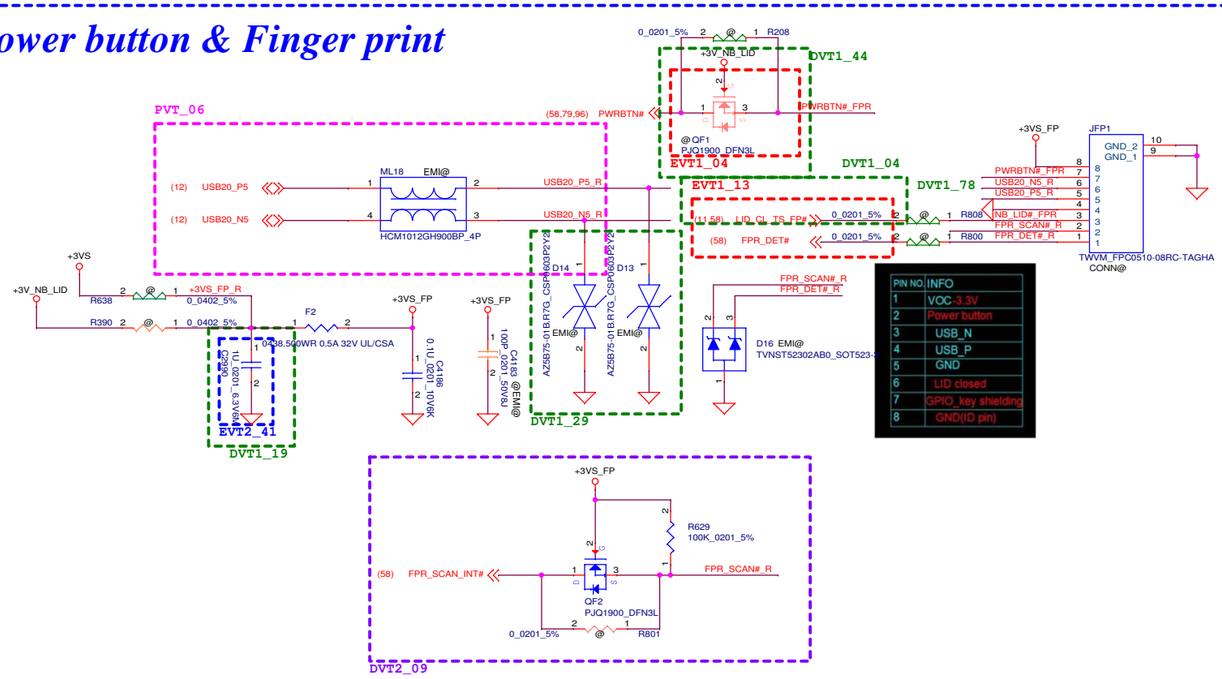
PCB X 2(NPTH)



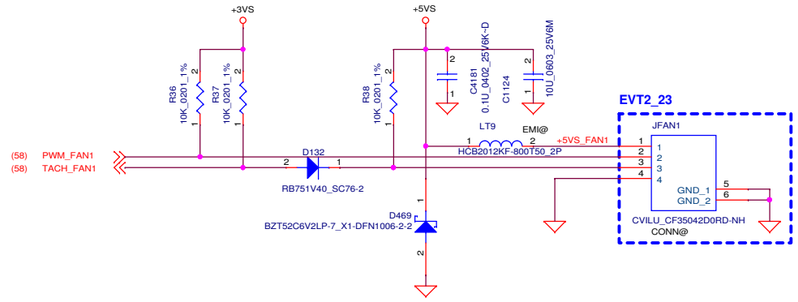
Shielding Frame X 6(NPTH)



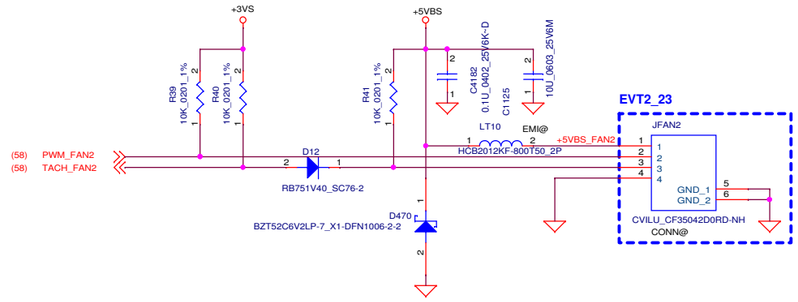
Power button & Finger print



FAN1



FAN2



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P077 - PWRBTN&FPR/SCREW/FAN
Size	Document Number: LA-G172P
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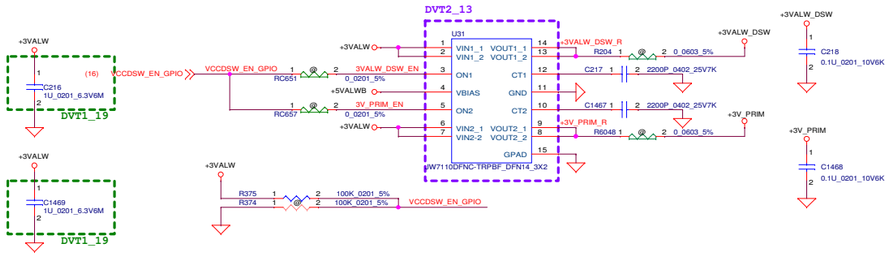
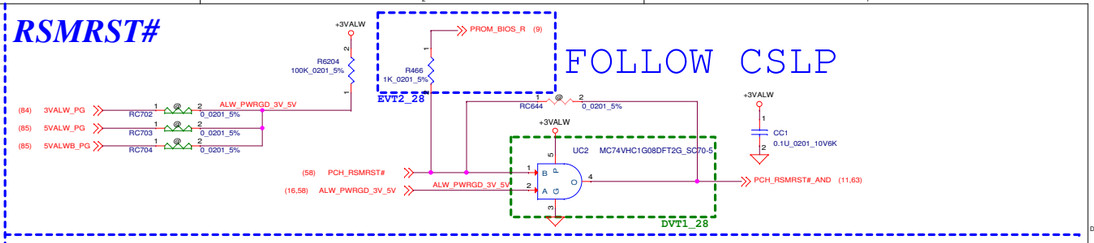
Date: Friday, May 24, 2019	Sheet 77 of 101

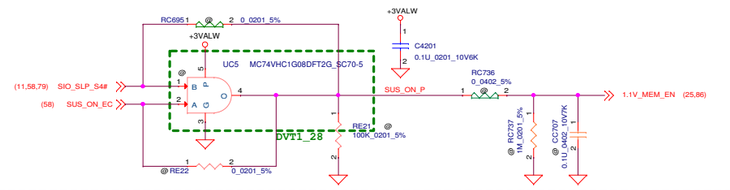
+3VALW_DSW&+3V_PRIM



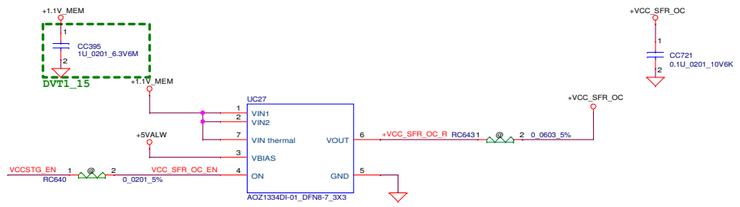
RSMRST#



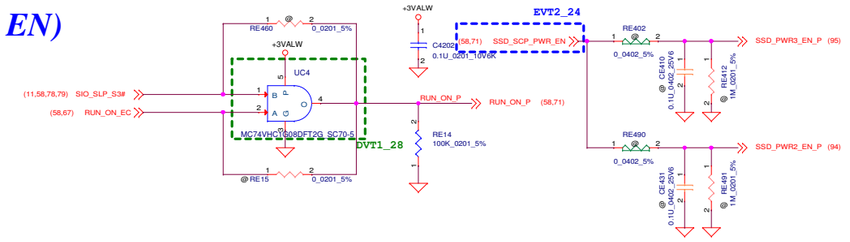
SUS_ON(DDR EN)



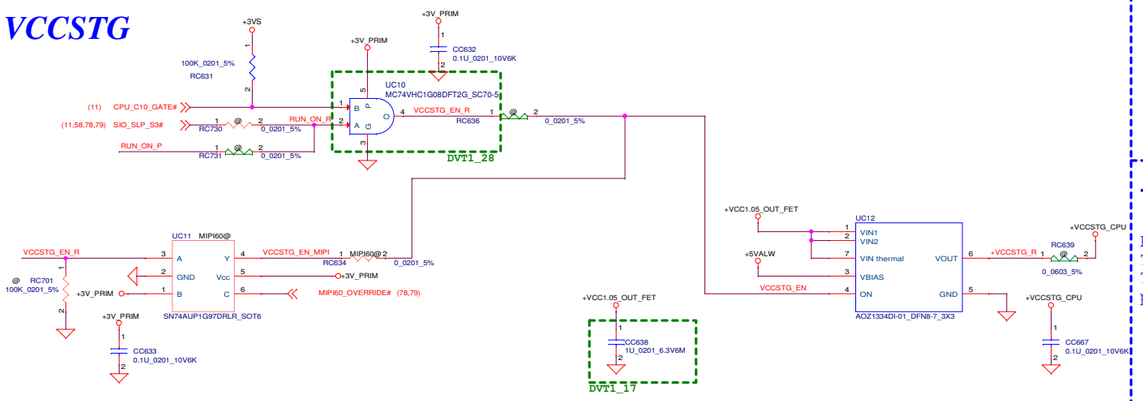
VCC_SFR_OC(VCCPLL_OC)



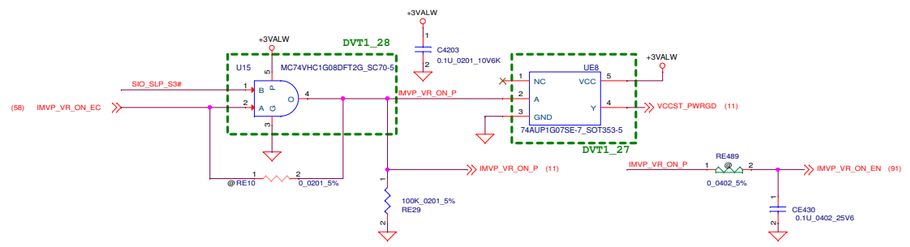
RUN_ON(VS EN)



VCCSTG



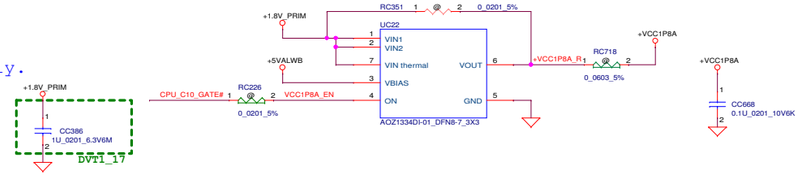
IMVP_VR_ON&VCCST_PWRGD



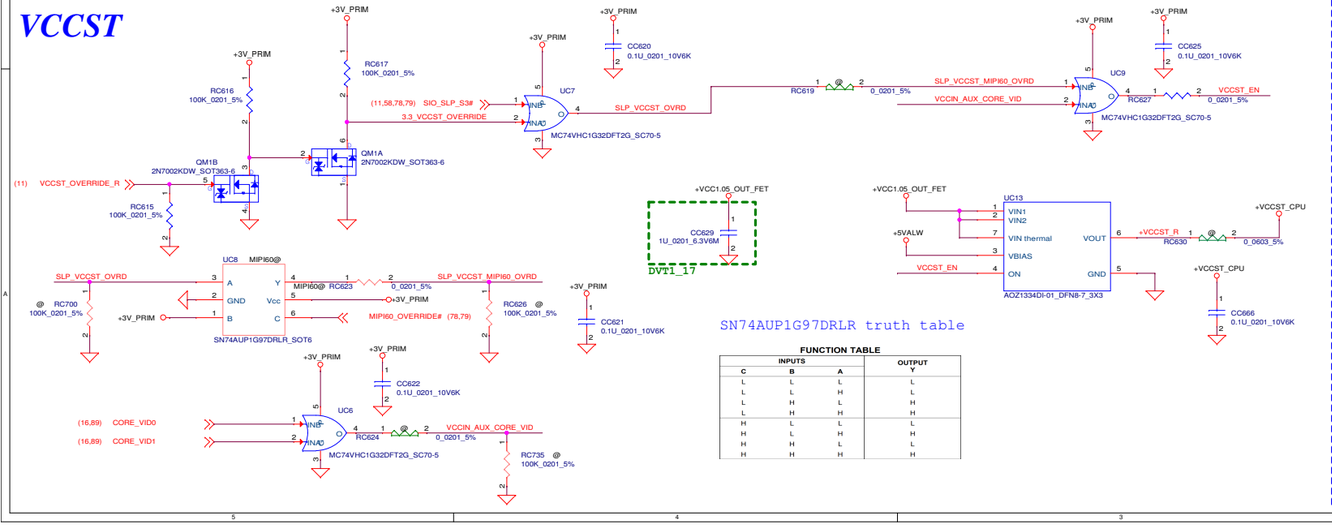
+VCC1P8A

PDG p.615
TCSS and AGSH
Type C Sub system and
processor analog supply.

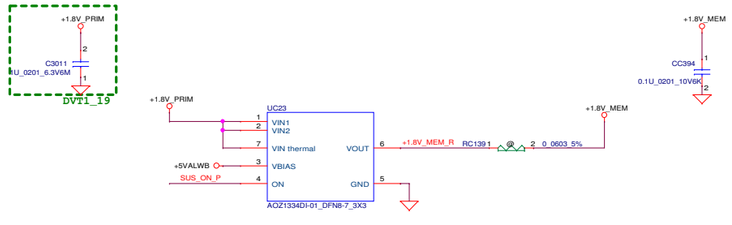
VCC1P8A shape from VR to VCC1P8A pins should have:
a. total length L of < 22mm between VR and BGA.
b. Average width W of 1.8mm.



VCCST



+1.8_MEM



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Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P078 - DC/DC & Sequence Logic**

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	LA-G172P	1.0 (A0#)

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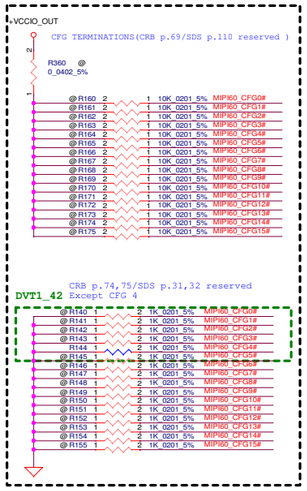
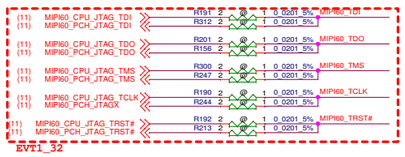
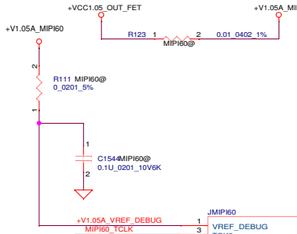
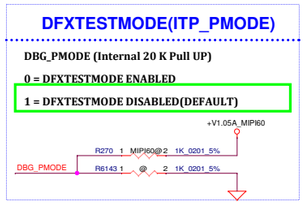
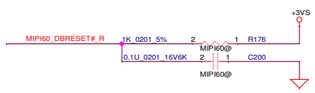
MIPI 60

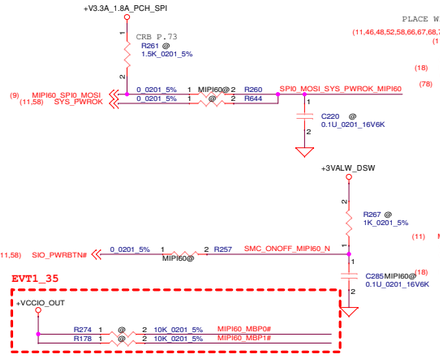


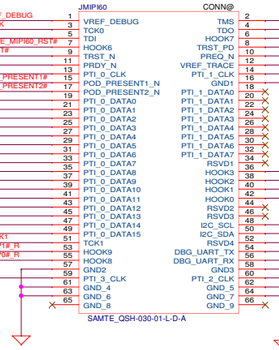




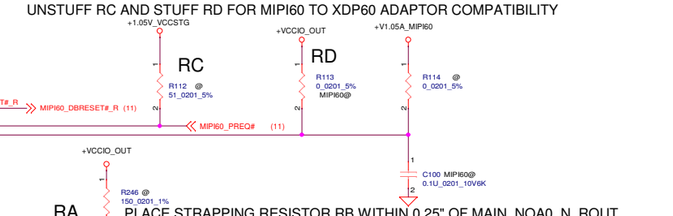




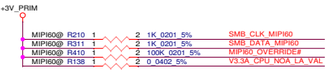


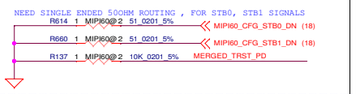


UNSTUFF RC AND STUFF RD FOR MIPI60 TO XDP60 ADAPTOR COMPATIBILITY



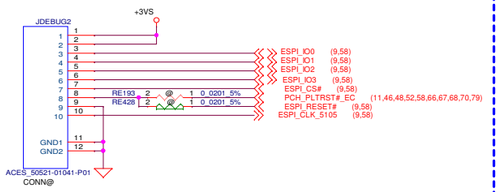
RA SHOULD BE STUFFED ONLY FOR MIPI60 TO XDP60 ADAPTOR COMPATIBILITY



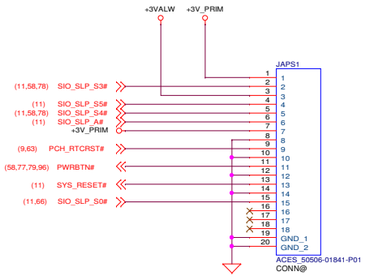


JESPI

LPC 80Port Debug	LPC	ESPI
1	+3VS	+3VS
2	+3VS	+3VS
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLK	ESPI_CLK

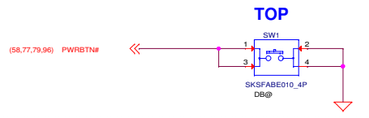


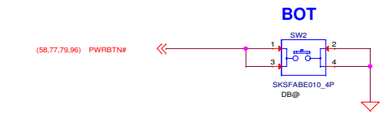
APS



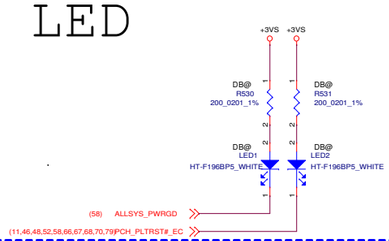
BIOS UART Debug

Power Button Debug



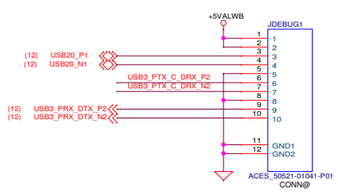


Debug LED



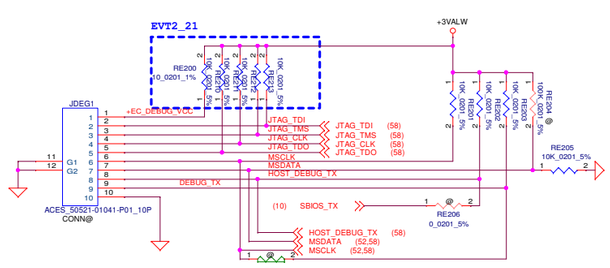
DCI Debug

EVT2_20



JDEG1
EC UART Debug/80 port

EVT2_21



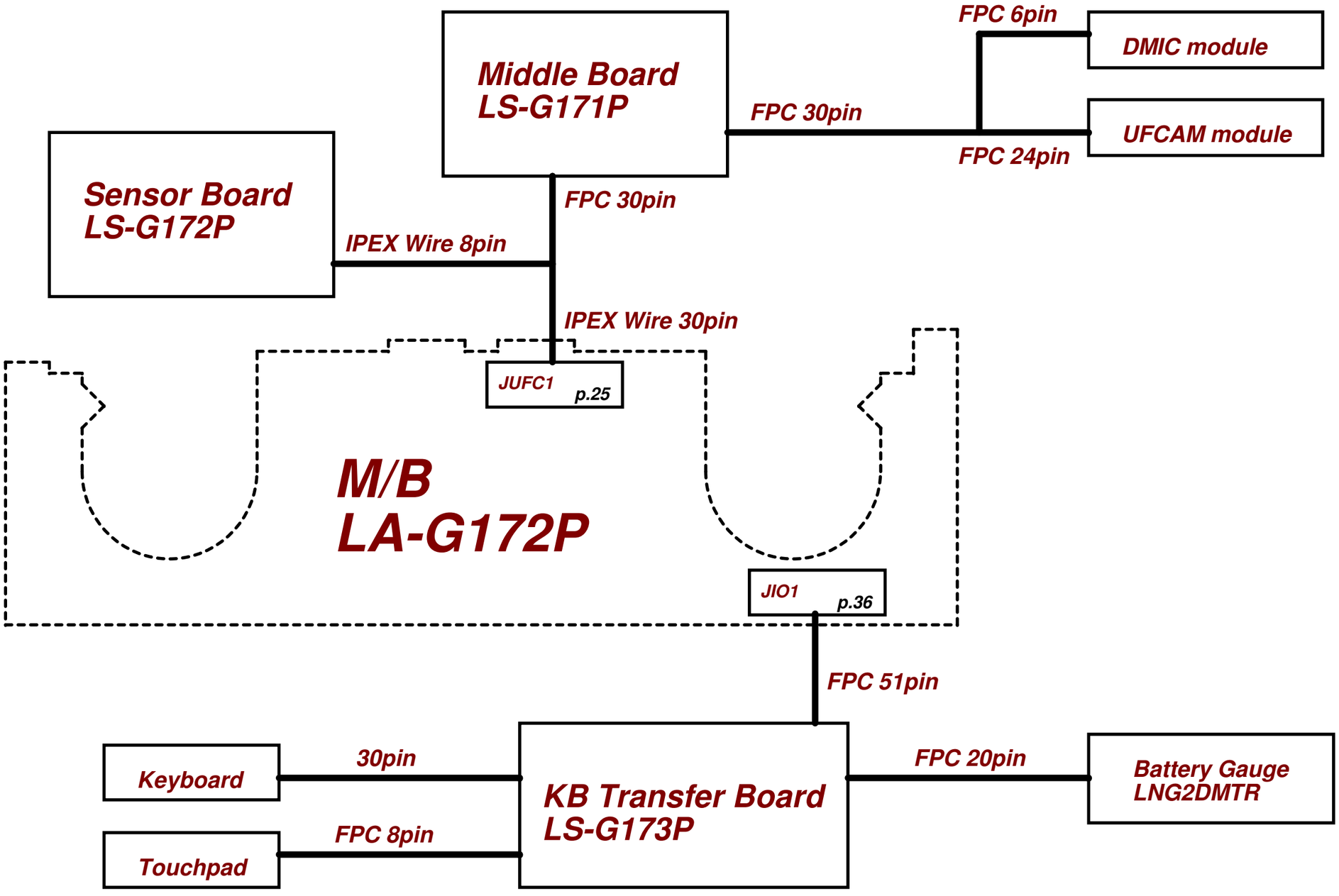
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P079 - Debug APS,DEG,eSPI,LED*

Size: | Document Number: *LA-G172P* | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 79 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

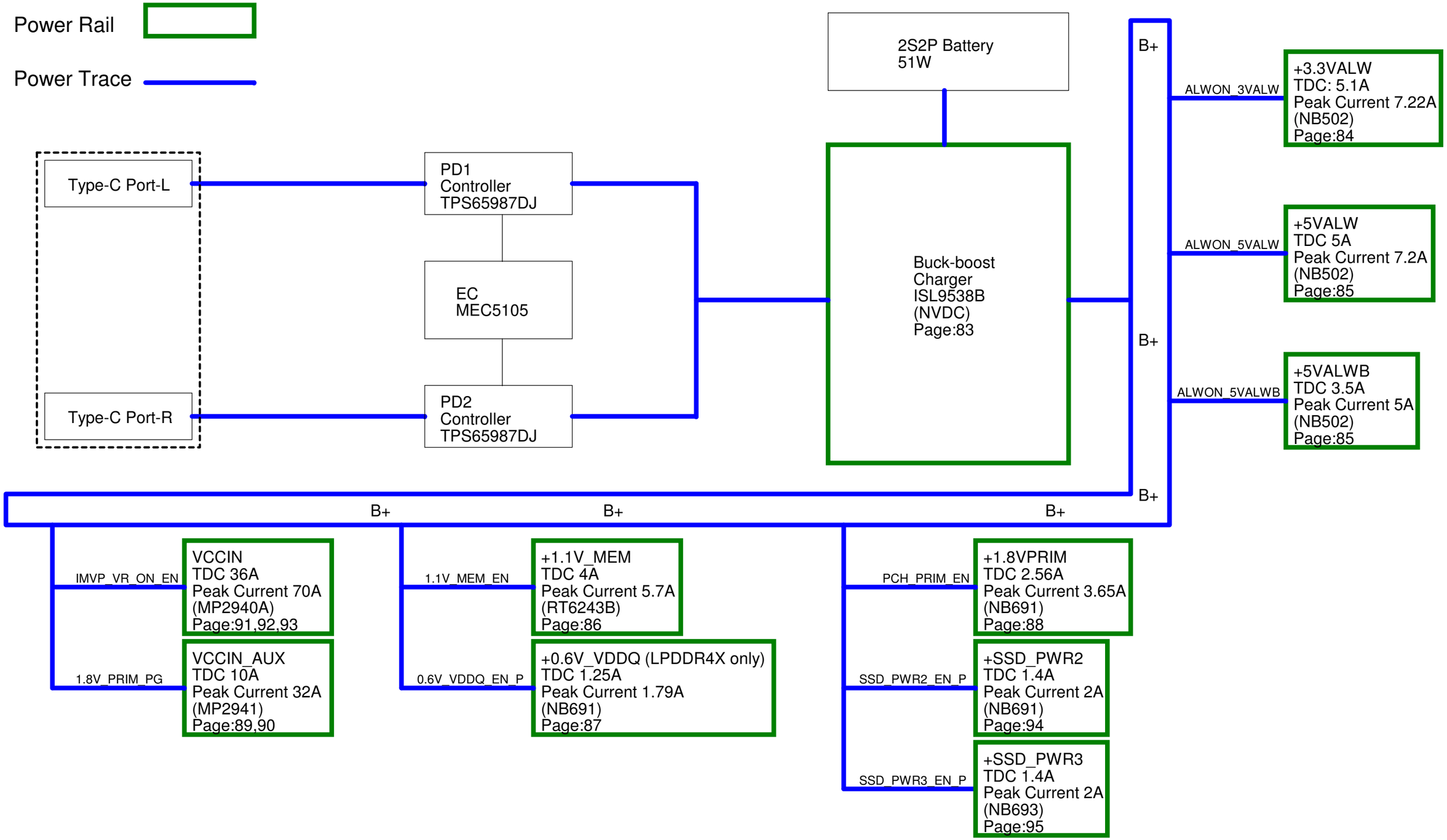
Compal Electronics, Inc.

Title: P080 - DaughterB Block Diagram

Size | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 80 of 101

Centenario POWER BLOCK DIAGRAM



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
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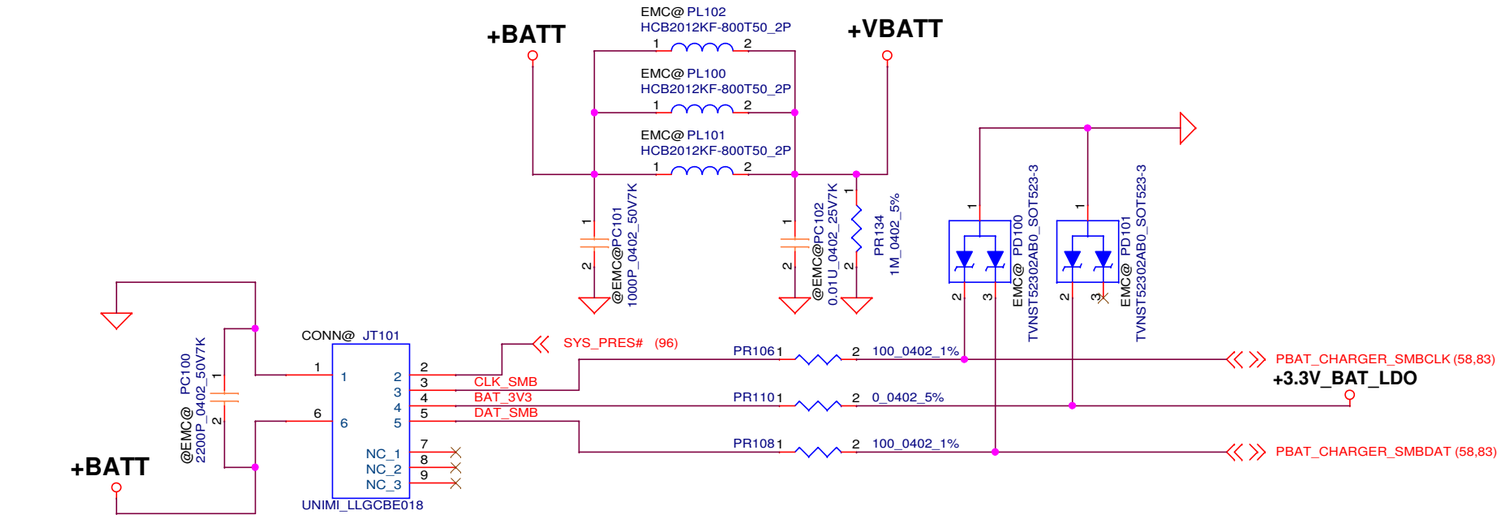

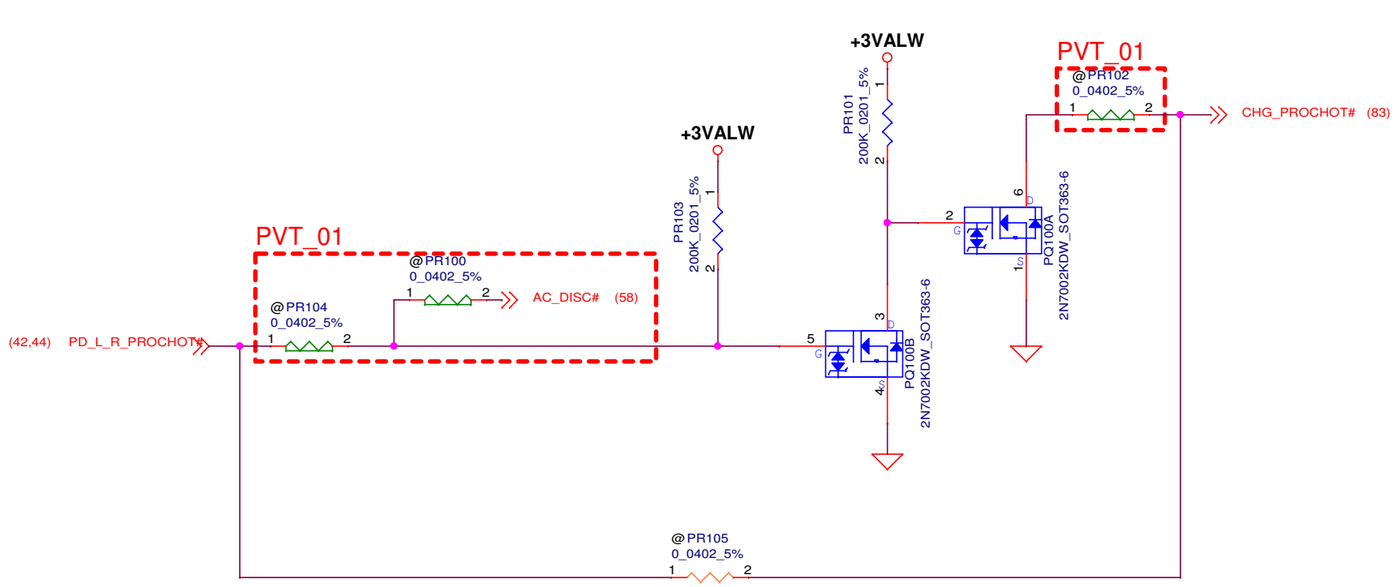

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR DCIN			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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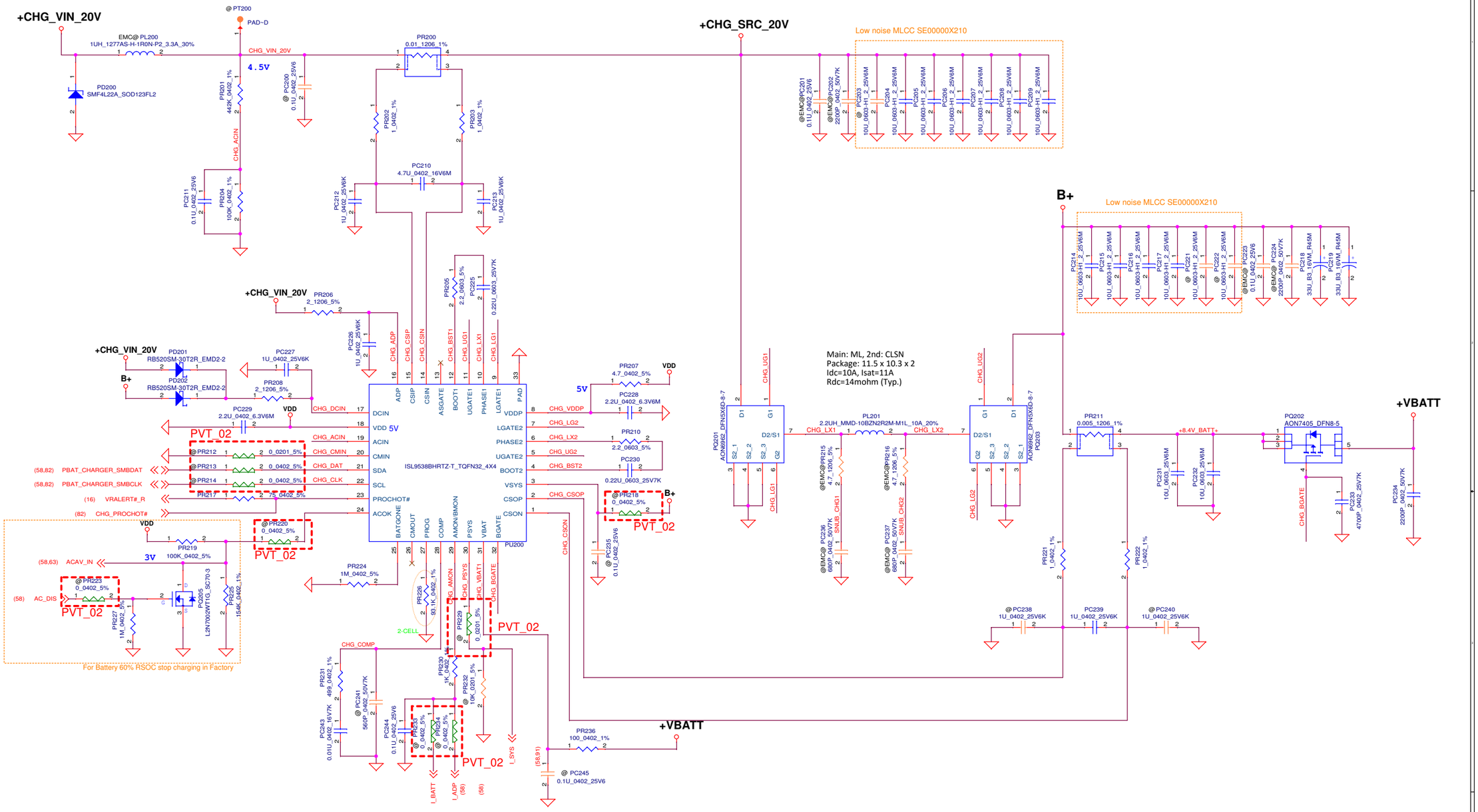
Charger controller(40.1), Support component(40.2)



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR_Charger			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 83 of 101		

3VALW
TDC 5.05A
Peak Current 7.22A
OCP 10A
700kHz

VCC	MODE2 Set
INT VCC	0
EXT VCC	Connect to VIN

CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

Main: CLSN, 2nd:
Package: 7.3 x 6.8 x 1.5
Idc=6.5A, Isat=12A
DCR=20mohm (Typ.)

B+
EMC@ PL302 HCB2012KF-800T50_2P
EMC@ PL300 HCB2012KF-800T50_2P
@EMC@ PC301 0.1U_0402_25V6
@EMC@ PC302 220P_0402_50V7K
PC303 10U_0603_25V6M
PC304 10U_0603_25V6M
@PR300 0_0402_5%
PVT_03
PR301 90.9K_0201_1%
PR303 0_0603_5%
PC300 0.22U_0402_16V7K
BST_3V
PU300
VIN
MODE2
CLM
BST
SW
LX_3V
PL301 1.5UH_MHCB06015-1R5M-C1_6.5A_20%
+3VALWP
R4
PR306 768K_0402_1%
PC305 220P_0201_25V7K
PR304 26.1K_0402_1%
R1
PR307 499_0402_1%
PR309 30.1K_0402_1%
R2
PC306 22U_0603_6.3V6M
PC307 22U_0603_6.3V6M
PC308 22U_0603_6.3V6M
PC309 22U_0603_6.3V6M
PC310 22U_0603_6.3V6M
PC311 22U_0603_6.3V6M
(58,96) ALWON_3VALW
EN
FB
FB_3V
(78) 3VALW_PG
PG
NB502GQ-Z_QFN16_3X3
@PR308 150K_0201_5%
+3.3V_ALW2
3V3 3.6V
PGND
GND_1
GND_2
GND_3
GND_4
MODE1
NC
PC313 2.2U_0402_6.3V6M
@PR310 0_0402_5%
@EMC@ PR311 4.7_0805_5%
@EMC@ PC314 680P_0603_50V7K

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

MODE	VREF
Vo<3V	0.6V
Vo>3V	1.8V

$$R1 = \frac{1}{\frac{VREF}{VOUT-VREF} - \frac{R2}{R4}} \times R2$$

+3VALWP
@PJP300
JUMP_43X118
+3VALW

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: ***PWR_+3VALW***

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5VALW
TDC 5A
Peak Current 7.2A
OCP 10A
700kHz

Main: ML, 2nd: CLSN
Package: 5.7 x 5.4 x 1.8
Idc=6.2A, Isat=8.4A
DCR=29mohm (Typ.)

VCC	MODE2 Set
INT VCC	0
EXT VCC	Connect to VIN

CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

MODE	VREF
Vo<3V	0.6V
Vo>3V	1.8V

$$R1 = \frac{1}{\frac{VREF}{VOUT-VREF} - \frac{R2}{R4}} \times R2$$

5VALWB
TDC 3.5A
Peak Current 5A
OCP 7A
700kHz

Main: ML, 2nd: CLSN
Package: 5.7 x 5.4 x 1.8
Idc=6.2A, Isat=8.4A
DCR=29mohm (Typ.)

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: **PWR_+5VALW/+5VALWB**

Size | Document Number: **LA-G172P** | Rev: 1.0 (A00)

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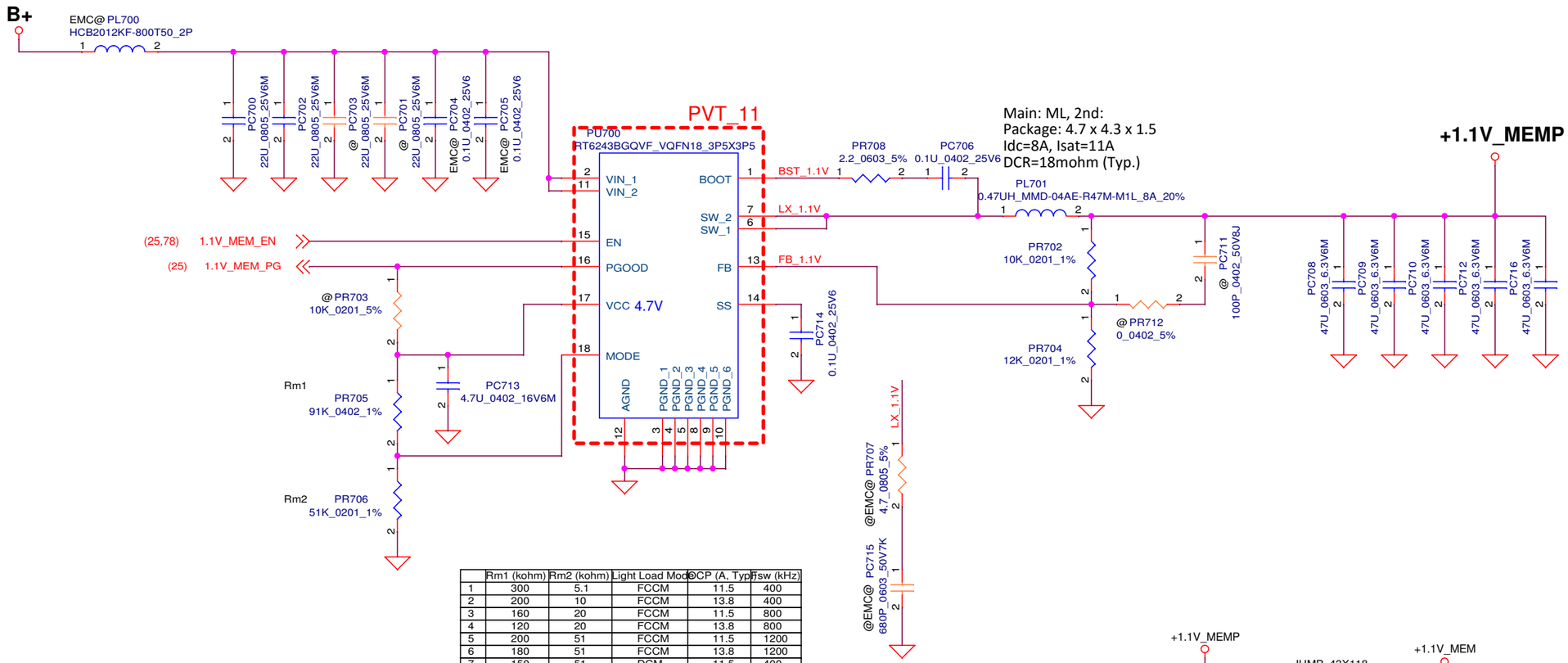
1.1V_MEM
TDC 4A
Peak Current 5.7A
OCP 11.5A
800KHz



	Rm1 (kohm)	Rm2 (kohm)	Light Load Mode	OCP (A, Typ)	Fsw (kHz)
1	300	5.1	FCCM	11.5	400
2	200	10	FCCM	13.8	400
3	160	20	FCCM	11.5	800
4	120	20	FCCM	13.8	800
5	200	51	FCCM	11.5	1200
6	180	51	FCCM	13.8	1200
7	150	51	DCM	11.5	400
8	120	51	DCM	13.8	400
9	91	51	DCM	11.5	800
10	82	51	DCM	13.8	800
11	62	51	DCM	11.5	1200
12	51	51	DCM	13.8	1200

Compal Electronics, Inc.

Title: ***PWR_+1.1V_MEM***

Size | Document Number: ***LA-G172P*** | Rev: 1.0 (A00)

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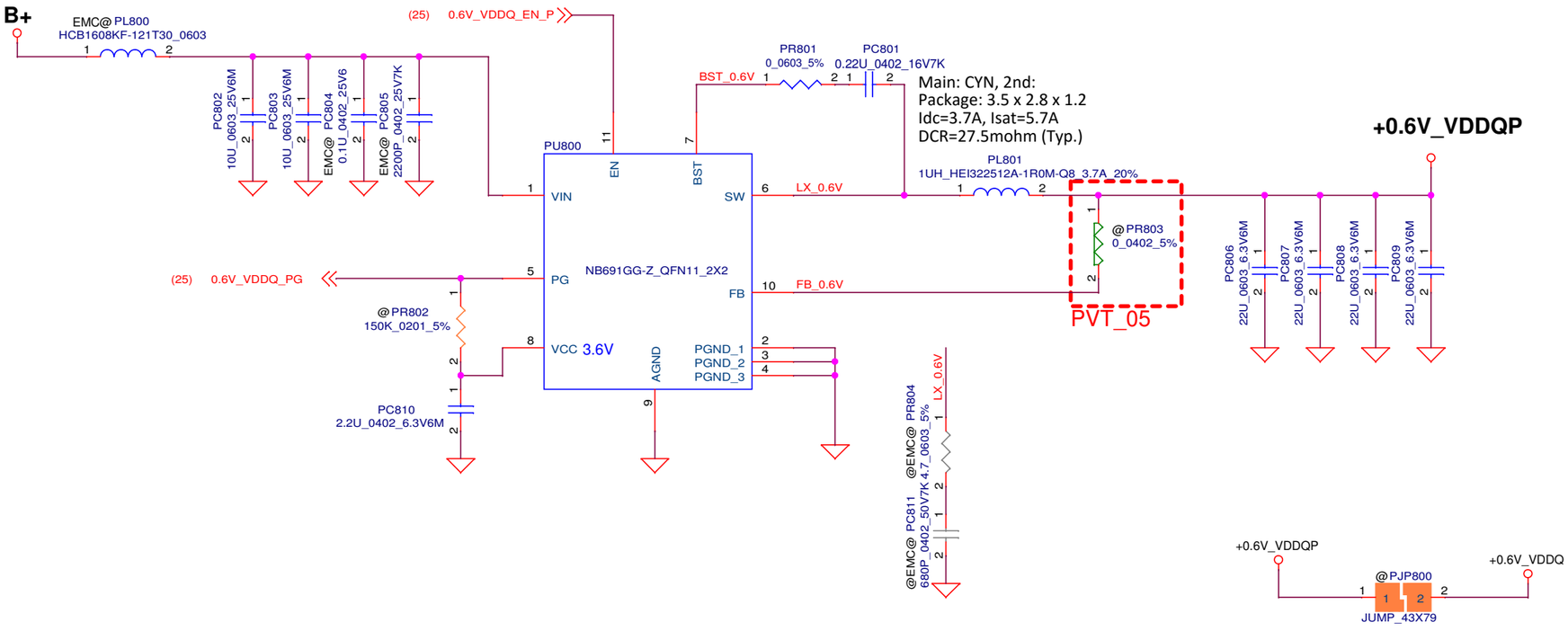
0.6V_VDDQ
TDC 1.25A
Peak Current 1.79A
OCP 7.5 (Typ.)
750kHz



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR_VDDQ4x			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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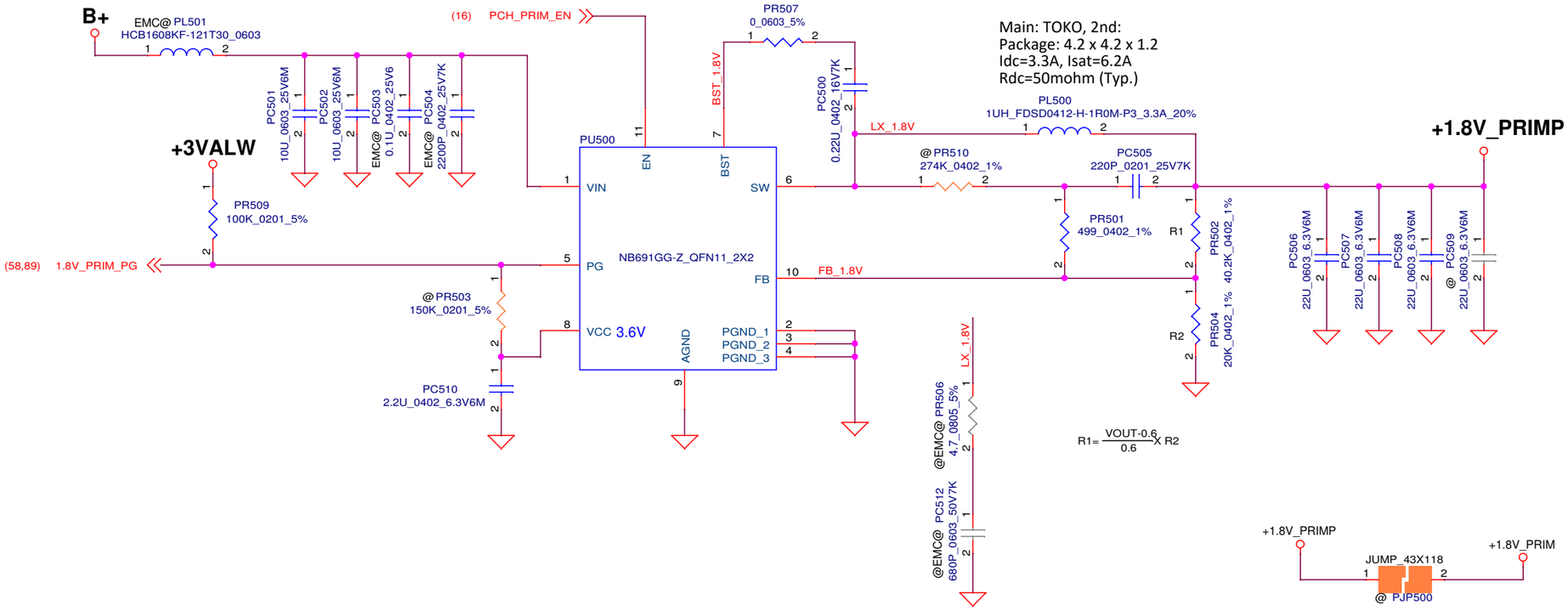
1.8V_PRIM
TDC 2.56A
Peak Current 3.65A
OCP 7.5A (Typ.)
750kHz



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: PWR_+1.8VPRIM

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VCCIN_AUX (Base on PDG rev 1.35)
Peak Current 32A (ICCmax)
TDC :14A
OCP Current 32A "valley" current-sensing
Fsw=1MHz

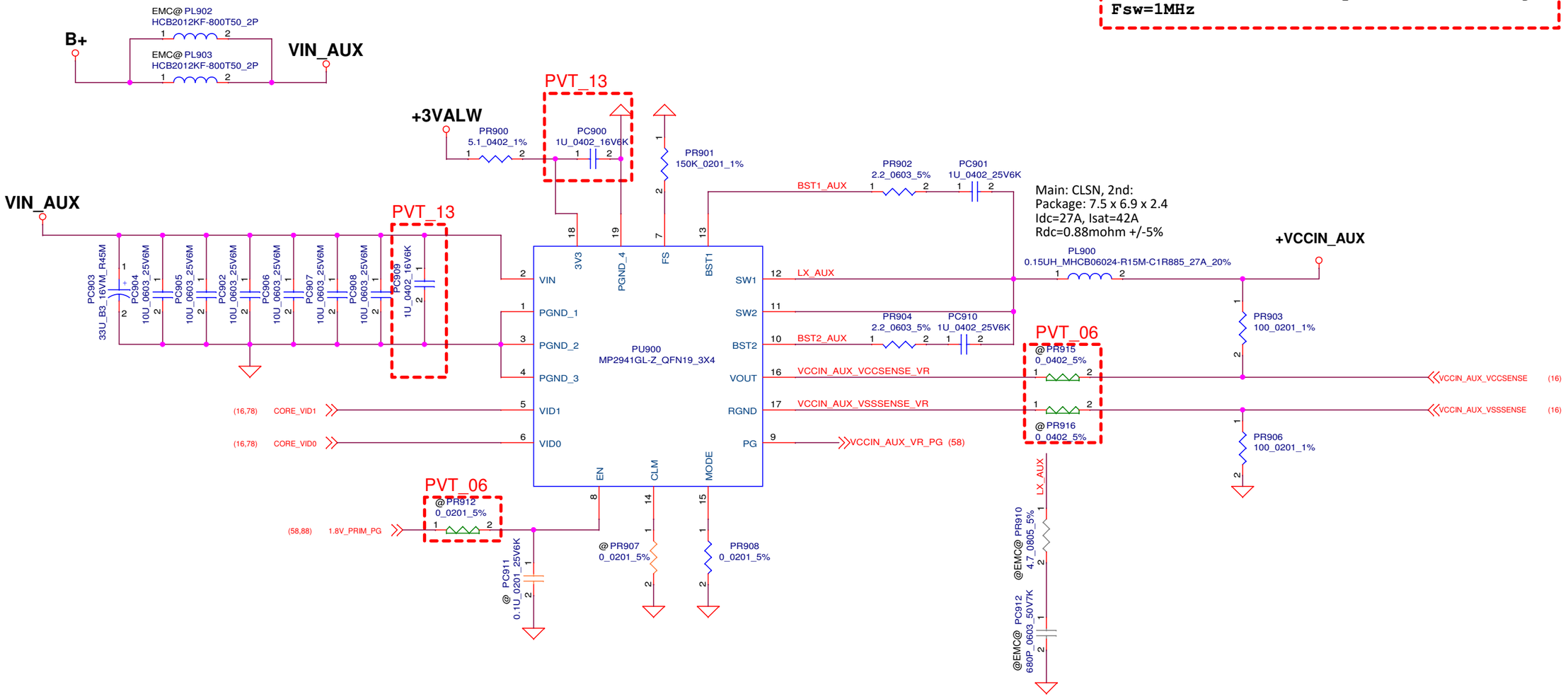

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

Compal Electronics, Inc.

Title: **PWR_VCCIN_AUX**

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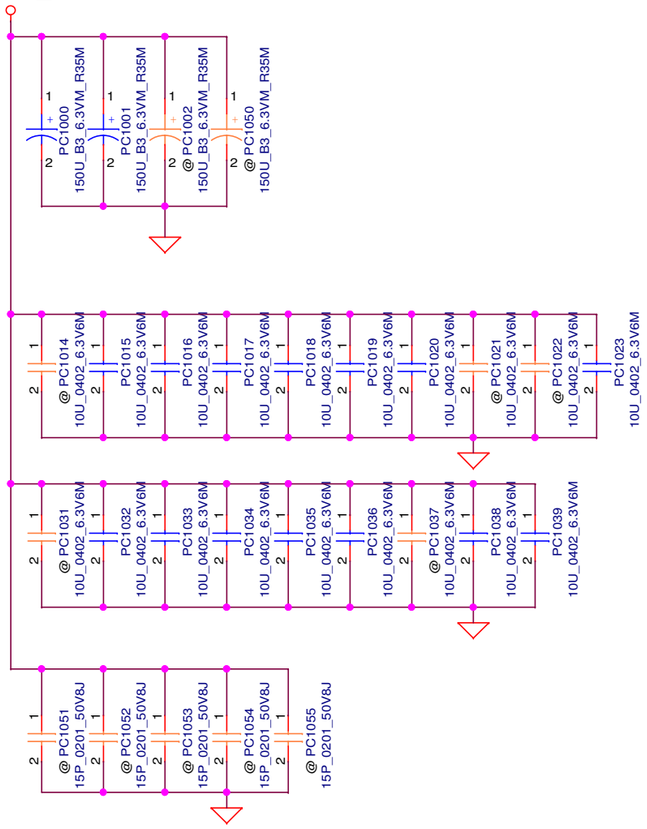
150U_B3 * 4 (POP*2, NC*2)
10U_0402 * 19 (POP*14, NC*5)
22U_0603 * 10 (POP*1, NC*9)
47U_0603 * 7 (POP*1, NC*6)
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)

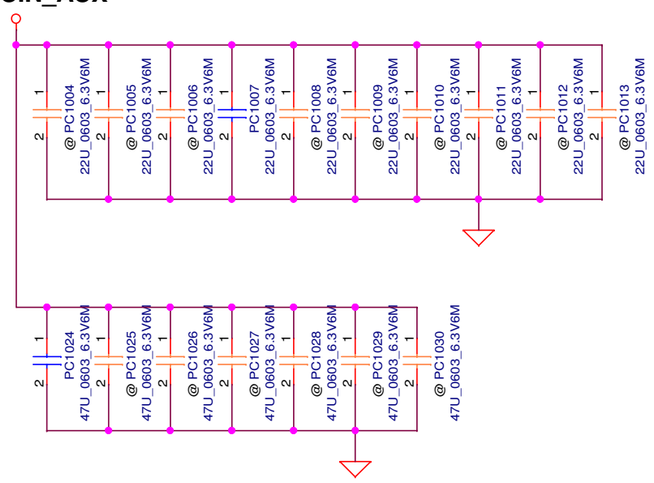
PDG ver 1.35 Primary side:
2x 330uF 7343
3x 22uF 0603
12x 10uF 0402
1x 47uF 0805

Primary side

+VCCIN_AUX



+VCCIN_AUX



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: PWR_DECOUPLING-VCCIN_AUX

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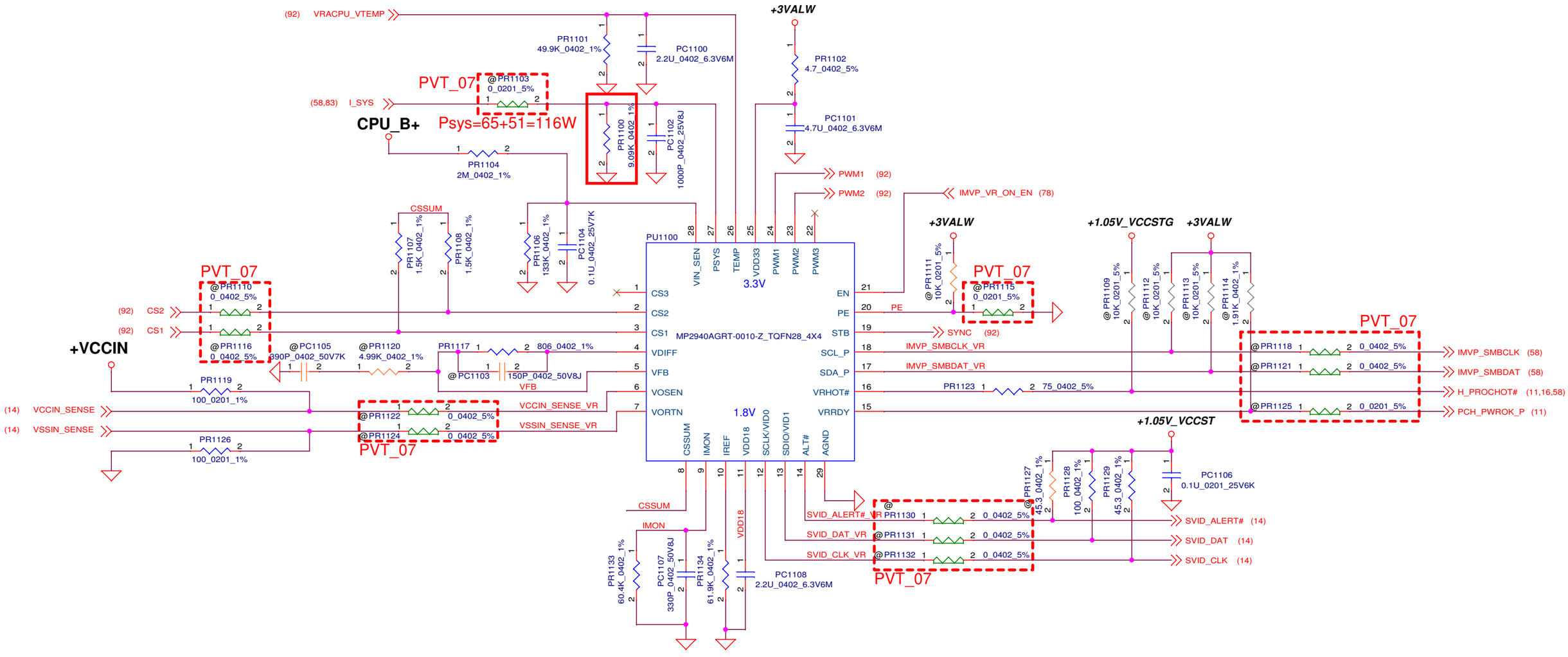
VCCIN (Base on PDG rev 1.35)
Peak Current 70A (ICCmax)
PL2 TDC :39A
DC Load line :2mV/A
AC Load line :4.2mV/A
OCP Current 90A
Fsw=600kHz



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: **PWR_VCCIN_CTRL**

Size	Document Number	Rev
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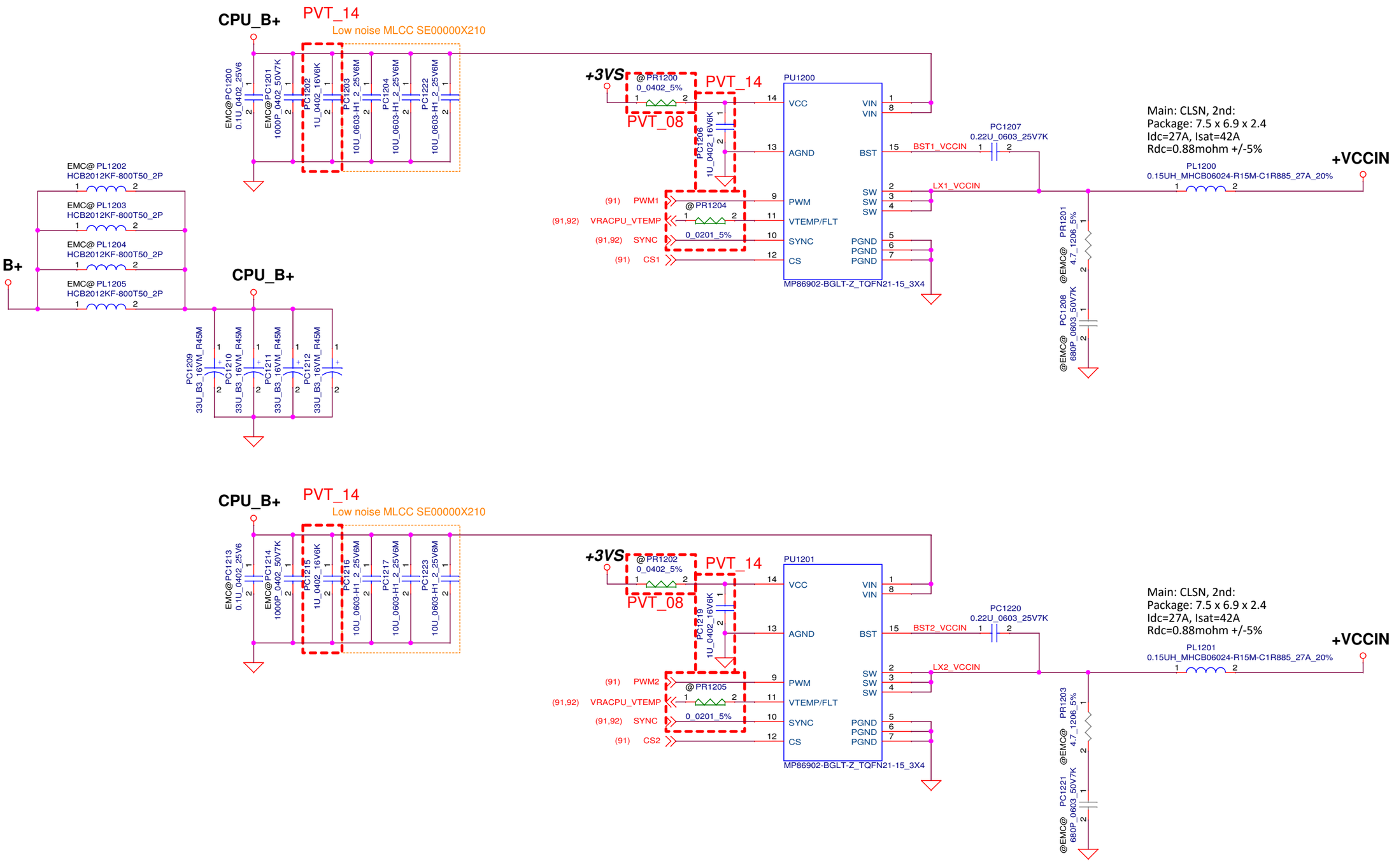

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR_VCCIN_Driver MOS			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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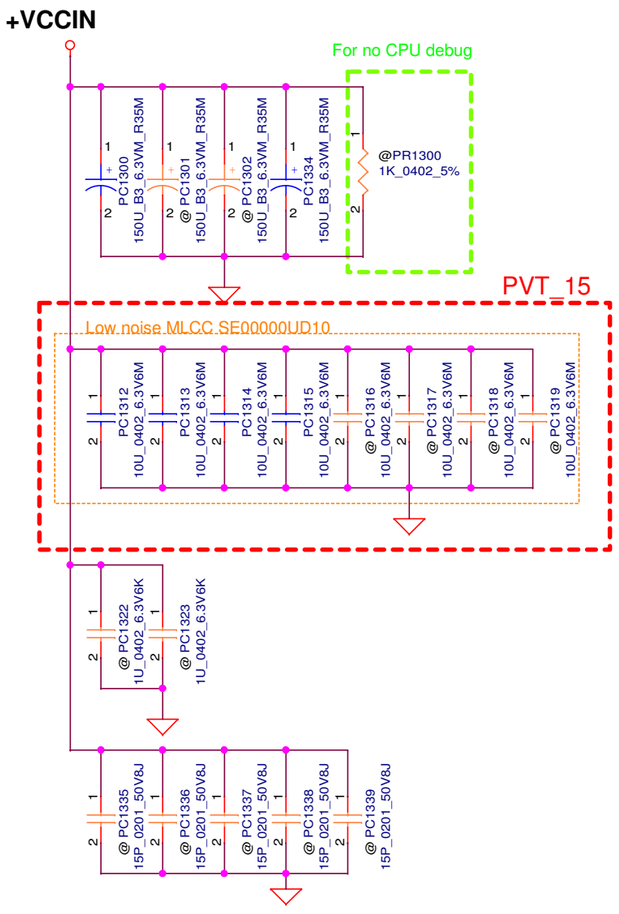
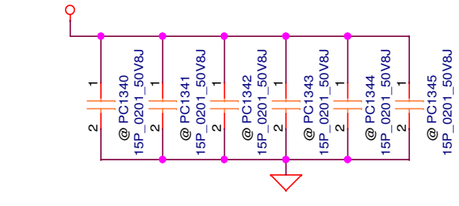
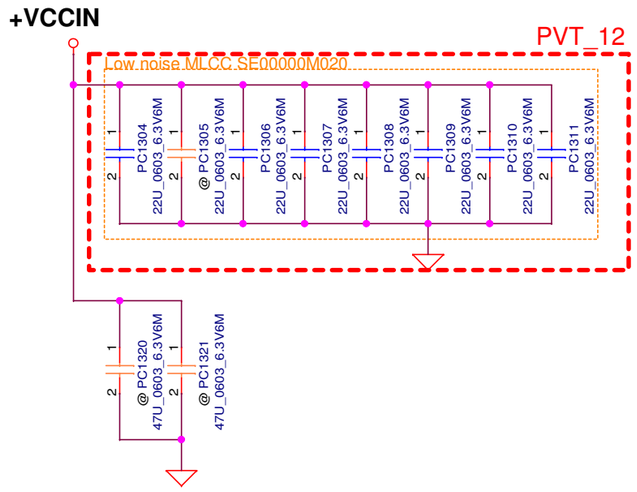
Primary side



BOT side



150U_B3 * 4 (pop*2, NC*2)
10U_0402 * 8 (pop*4, NC*4)
22U_0603 * 8 (pop*7, NC*1)
47U_0603 * 2 (NC*2)
1U0402 * 2
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)



PDG ver 1.35 Primary side:
2x 1uF 0402
4x 10uF 0402
8x 22uF 0603
1x 47uF 0805
2x 330uF 7343

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.		
Title: PWR_DECOUPLING-VCCIN		
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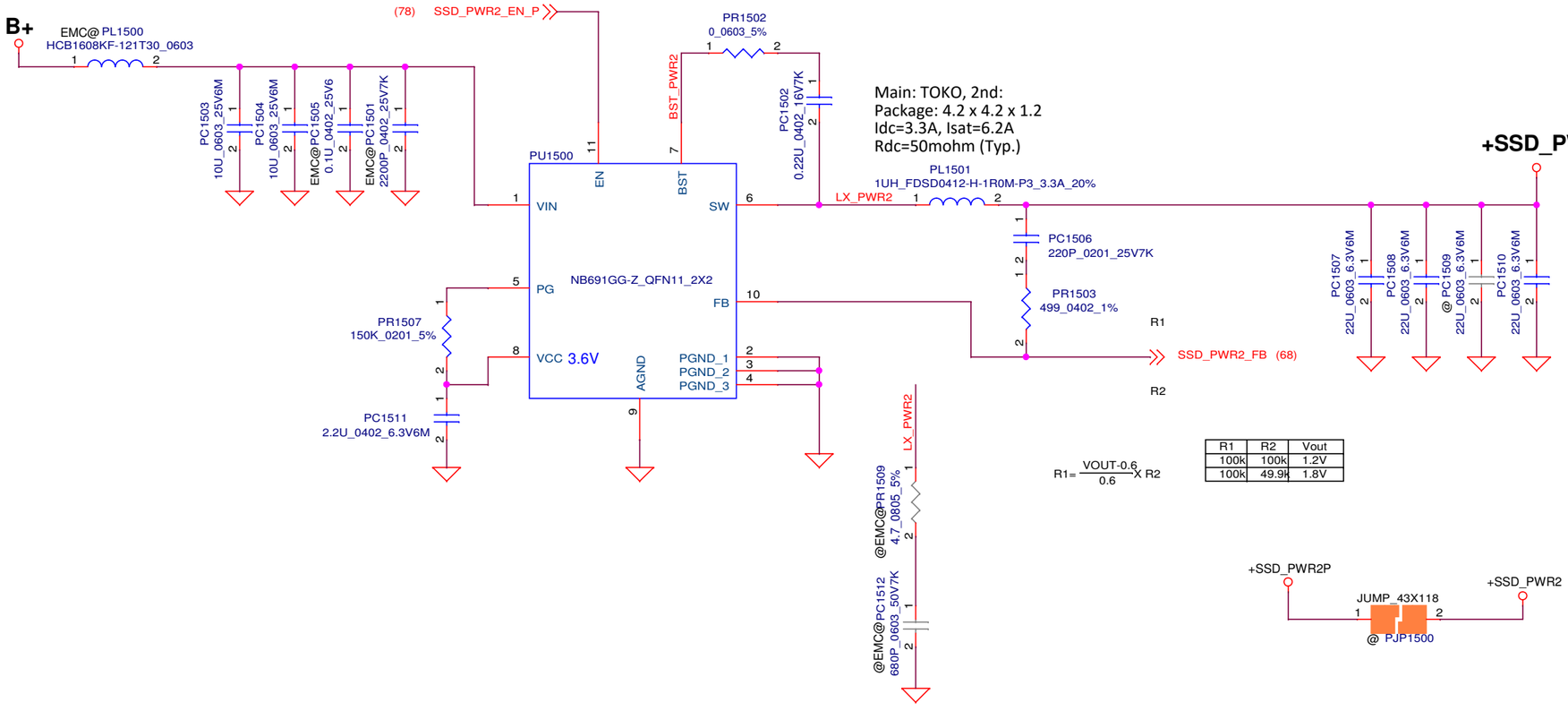
+1.2VDX_SSD
TDC 1.4A
Peak Current 2A
OCP 7.5A (Typ.)
750kHz



R1	R2	Vout
100k	100k	1.2V
100k	49.9k	1.8V

Compal Electronics, Inc.

Title: ***PWR_+1.2/+1.8V***

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SSD_PWR3
TDC 1.4A
Peak Current 2A
OCP 8.5A
700kHz

State	CLM	Resistor to GND
M1	8.5A	0
M2	10A	90K
M3	13A	150K
M4	16.5A	>230K or float

PVT_09

@PR1400 0_0201_5%

B+

EMC@ PL1400 HCB2012KF-800T50_2P

@EMC@PC1401 0.1U_0402_25V6

@EMC@PC1402 2200P_0402_50V7K

PC1403 10U_0603_25V6M

PC1404 10U_0603_25V6M

PR1401 2.2_0603_5%

PC1400 0.22U_0402_16V7K

BST_PWR3

PU1400

NB693GQ-Z_QFN16_3X3

VIN, NC_2, CLM, BST, SW, EN, FB, PG, 3V3, PGND_1, PGND_2, PGND_3, PGND_4, PGND_5, MODE, NC_1

LX_PWR3

Main: CLSN, 2nd:
Package: 4.8 x 4.3 x 1.5
Idc=5A, Isat=8A
Rdc=30mohm (Typ.)

PL1401 0.68UH_MHCI04015-R68M-R8_5A_20%

+SSD_PWR3P

PC1405 220P_0201_25V7K

PC1406 22U_0603_6.3V6M

PC1407 22U_0603_6.3V6M

PC1408 22U_0603_6.3V6M

@ PC1409 22U_0603_6.3V6M

(78) SSD_PWR3_EN_P

PR1403 499_0402_1%

R1

R2

SSD_PWR3_FB (68)

@PR1408 0_0402_5%

PVT_09

PR1406 100K_0201_5%

+3VALW

PR1409 5.1_0402_1%

PC1411 2.2U_0402_6.3V6M

R1	R2	Vout
100k	200k	0.9V
100k	120k	1.1V
100k	100k	1.2V

$$R1 = \frac{VOUT-0.6}{0.6} X\ R2$$

@EMC@PR1411 4.7_0805_5%

@EMC@PC1412 680P_0603_50V7K

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

+SSD_PWR3P

JUMP_43X118

+SSD_PWR3

@ PJP1400

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Compal Electronics, Inc.

Title: PWR_+1.2/+1.1/+0.9V

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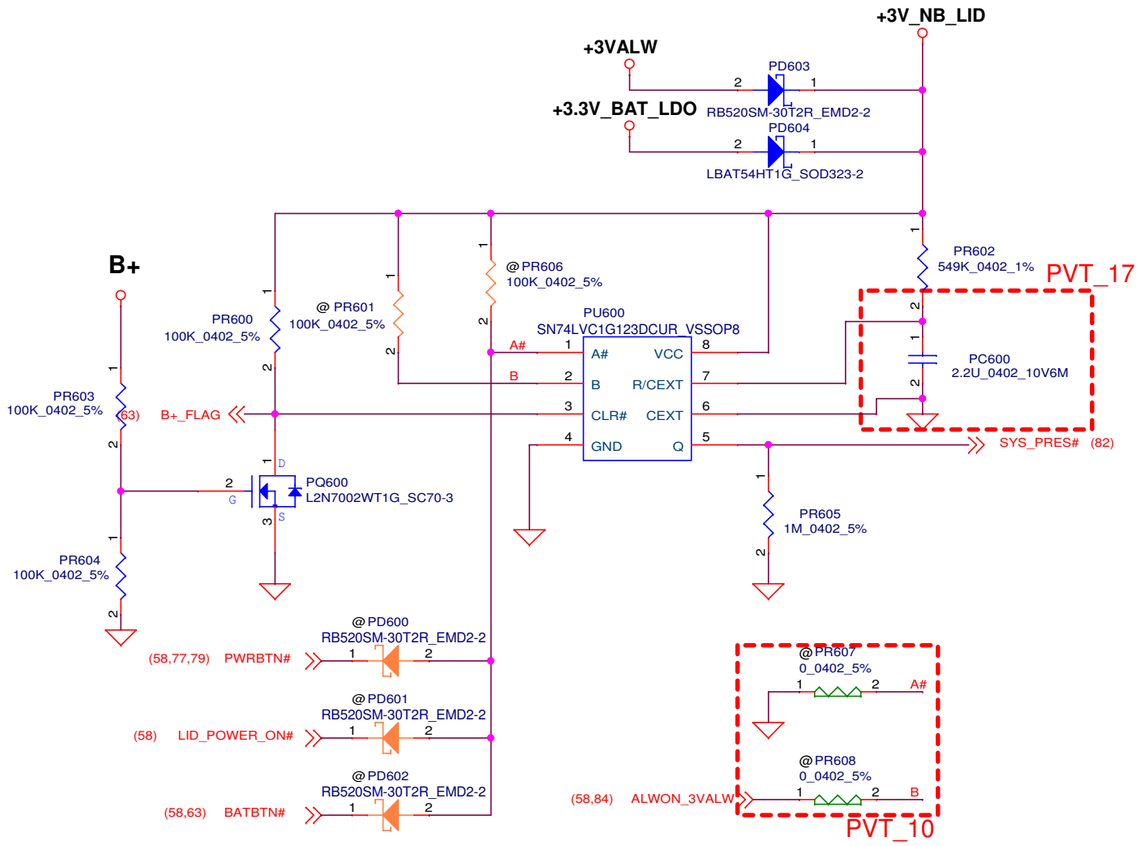

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⊓
H	↓	H	⊓
↑	L	H	⊓

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: PWR_SHIP_MODE		
Size	Document Number: LA-G172P	Rev: 1.0 (A00)
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Security Classification	Compal Secret Data			Compal Electronics, Inc.
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Security Classification	Compal Secret Data			Compal Electronics, Inc.
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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **RESERVE**

Size	Document Number	Rev
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CPU Option

UC1 SRG0N@ — SA0000CT62L — ICE LAKE SRG0N

UC1 SRGKL@ — SA0000CT82L — ICE LAKE SRGKL

UC1 SRG0S@ — SA0000CTD2L — ICE LAKE SRG0S

SSD debug Option

R610 TOSHIBA_DB@ — SD043000080 — 0_0201_5%

SSD power Option

Power 3

R6136 NINTEL@ — SD013000080 — 0_0603_5%

LS2 NINTEL@ — SM01000BW00 — HCB1608KF-121T30_0603

TBT Option

URT1 BB@ — SA0000CAH3L — JHL8040R QURW

URT2 BB@ — SA0000CAH3L — JHL8040R QURW

CPU I3/I5/I7 Option for different thermal table

I3: RE525 I3@ — SD028240380 — 240K_0402_5%

I5: RE525 I5@ — SD028130380 — 130K_0402_5%

I7: RE525 I7@ — SD028620280 — 62K_0402_5%

EC

PD Option

UPD1 DJ@ — SA0000CM71L — SN1806026RSHR

UPD2 DJ@ — SA0000CM71L — SN1806026RSHR

CPU I3/I5/I7 Option for different thermal table

I3:

RH747 I3@ — SD043100380 — 100K_0201_5%

RH748 I3@ — SD043100380 — 100K_0201_5%

I5:

RH747 I5@ — SD043100380 — 100K_0201_5%

RH746 I5@ — SD043100380 — 100K_0201_5%

I7:

RH745 I7@ — SD043100380 — 100K_0201_5%

RH748 I7@ — SD043100380 — 100K_0201_5%

BIOS

WLAN Option

UWL1 KILLER@ — PK29S009L0L — KILLER1650S.01

SSD Option

USSD1 BG4_256GB@ — SA0000C6G1L — KBG40ZPZ256G

USSD1 BG4_512GB@ — SA0000CG61L — KBG40ZPZ512G

USSD1 BG4_1TB@ — SA0000CG21L — KBG40ZPZ1T02

USSD1 INTEL_256GB@ — SA0000C5M2L — SSDPEBKW256G8

USSD1 INTEL_512GB@ — SA0000C7K1L — SSDPEBKW512G8

EC Option

UE1 5105@ — SA00009GL30 — MEC5105_WFBGA169_11X11

UE1 5106@ — SA0000C5D00 — MEC5106_WFBGA169_11X11

Pin Name	Micron 8GB SA0000BX51L	Micron 16GB SA0000BX61L	Micron 32GB SA0000BX71L	Hynix 8GB SA0000BYX1L	Hynix 16GB SA0000AW2QL OLD and NO SUPPORT	Hynix 32GB SA0000C7V1L 3733	Samsung 8GB SA0000C6K1L	Samsung 16GB SA0000AU40L OLD and NO SUPPORT	Samsung 32GB SA0000CGN1L	Samsung 16GB SA0000C6L1L NEW	Hynix 16GB SA0000BYW1L NEW	Samsung 4GB SA0000AV71L	Micron 4GB SA0000BWF0L Micron 4GB EOL	Hynix 4GB SA0000AD11L	Hynix 32GB SA0000BWU1L PRTS(4266)
MEM_CONFIG0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
MEM_CONFIG2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
MEM_CONFIG3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X76	DRAM Option R1	DRAM Config Option (Resistor pop location) MEM_CONFIG4 / MEM_CONFIG3 / MEM_CONFIG2 / MEM_CONFIG1 / MEM_CONFIG0
X7678131L06 (Micron 4GB EOL)	**Micron 4GB/3733** — X76_M4GB_R1@ UD1 MT53B256M32D1NP-053 WT SA0000BWF0L; UD2 MT53B256M32D1NP-053 WT SA0000BWF0L; UD3 MT53B256M32D1NP-053 WT SA0000BWF0L; UD4 MT53B256M32D1NP-053 WT SA0000BWF0L	X76_M4GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH614 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L03	**Micron 8GB/4266** — X76_M8GB_R3@ UD1 MT53E512M32D2NP-046 WT SA0000BX51L; UD2 MT53E512M32D2NP-046 WT SA0000BX51L; UD3 MT53E512M32D2NP-046 WT SA0000BX51L; UD4 MT53E512M32D2NP-046 WT SA0000BX51L	X76_M8GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L09	**Micron 16GB/4266** — X76_M16GB_R3@ UD1 MT53E1G32D4NQ-046 WT SA0000BX61L; UD2 MT53E1G32D4NQ-046 WT SA0000BX61L; UD3 MT53E1G32D4NQ-046 WT SA0000BX61L; UD4 MT53E1G32D4NQ-046 WT SA0000BX61L	X76_M16GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L11	**Micron 32GB/4266** — X76_M32GB_R3@ UD1 MT53E2G32D8QD-046 WT SA0000BX71L; UD2 MT53E2G32D8QD-046 WT SA0000BX71L; UD3 MT53E2G32D8QD-046 WT SA0000BX71L; UD4 MT53E2G32D8QD-046 WT SA0000BX71L	X76_M32GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L07	**Hynix 4GB/3733** — X76_H4GB_R3@ UD1 H9HCNNN8KUMLHR-NME SA0000AD11L; UD2 H9HCNNN8KUMLHR-NME SA0000AD11L; UD3 H9HCNNN8KUMLHR-NME SA0000AD11L; UD4 H9HCNNN8KUMLHR-NME SA0000AD11L	X76_H4GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH614 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L05	**Hynix 8GB/4266** — X76_H8GB_R3@ UD1 H9HCNNNBKMALHR-NEE SA0000BYX1L; UD2 H9HCNNNBKMALHR-NEE SA0000BYX1L; UD3 H9HCNNNBKMALHR-NEE SA0000BYX1L; UD4 H9HCNNNBKMALHR-NEE SA0000BYX1L	X76_H8GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L12	**Hynix 16GB/4266(NEW)** — X76_H16GB_R3@ UD1 H9HCNNNCPMALHR-NEE SA0000BYW1L; UD2 H9HCNNNCPMALHR-NEE SA0000BYW1L; UD3 H9HCNNNCPMALHR-NEE SA0000BYW1L; UD4 H9HCNNNCPMALHR-NEE SA0000BYW1L	X76_H16GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L10	**Hynix 32GB/3733** — X76_H32GB_R3@ UD1 H9HCNNNFAMALTR-NME SA0000C7V1L; UD2 H9HCNNNFAMALTR-NME SA0000C7V1L; UD3 H9HCNNNFAMALTR-NME SA0000C7V1L; UD4 H9HCNNNFAMALTR-NME SA0000C7V1L	X76_H32GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH614 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L04	**Samsung 4GB/3733** — X76_S4GB_R3@ UD1 K4F8E304HB-MGCJ SA0000AV71L; UD2 K4F8E304HB-MGCJ SA0000AV71L; UD3 K4F8E304HB-MGCJ SA0000AV71L; UD4 K4F8E304HB-MGCJ SA0000AV71L	X76_S4GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L08	**Samsung 8GB/4266** — X76_S8GB_R3@ UD1 K4U6E3S4AA-MGCL SA0000C6K1L; UD2 K4U6E3S4AA-MGCL SA0000C6K1L; UD3 K4U6E3S4AA-MGCL SA0000C6K1L; UD4 K4U6E3S4AA-MGCL SA0000C6K1L	X76_S8GB@ RH665 10K_0201_5% SD043100280; RH185 10K_0201_5% SD043100280; RH614 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L13	**Samsung 16GB/4266(NEW)** — X76_S16GB_R3@ UD1 K4UBE3D4AA-MGCL SA0000C6L1L; UD2 K4UBE3D4AA-MGCL SA0000C6L1L; UD3 K4UBE3D4AA-MGCL SA0000C6L1L; UD4 K4UBE3D4AA-MGCL SA0000C6L1L	X76_S16GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH612 10K_0201_5% SD043100280
X7678131L14	**Samsung 32GB/4266** — X76_S32GB_R3@ UD1 K4UCE3Q4AA-MGCL SA0000CGN1L; UD2 K4UCE3Q4AA-MGCL SA0000CGN1L; UD3 K4UCE3Q4AA-MGCL SA0000CGN1L; UD4 K4UCE3Q4AA-MGCL SA0000CGN1L	X76_S32GB@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH145 10K_0201_5% SD043100280; RH139 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280
X7678131L21	**Hynix 32GB/4266(PRTS)** — X76_H32GB_R3_P@ UD1 H9HCNNNFAMALTR-NEE SA0000BWU1L; UD2 H9HCNNNFAMALTR-NEE SA0000BWU1L; UD3 H9HCNNNFAMALTR-NEE SA0000BWU1L; UD4 H9HCNNNFAMALTR-NEE SA0000BWU1L	X76_H32GB_P@ RH665 10K_0201_5% SD043100280; RH615 10K_0201_5% SD043100280; RH614 10K_0201_5% SD043100280; RH613 10K_0201_5% SD043100280; RH129 10K_0201_5% SD043100280

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