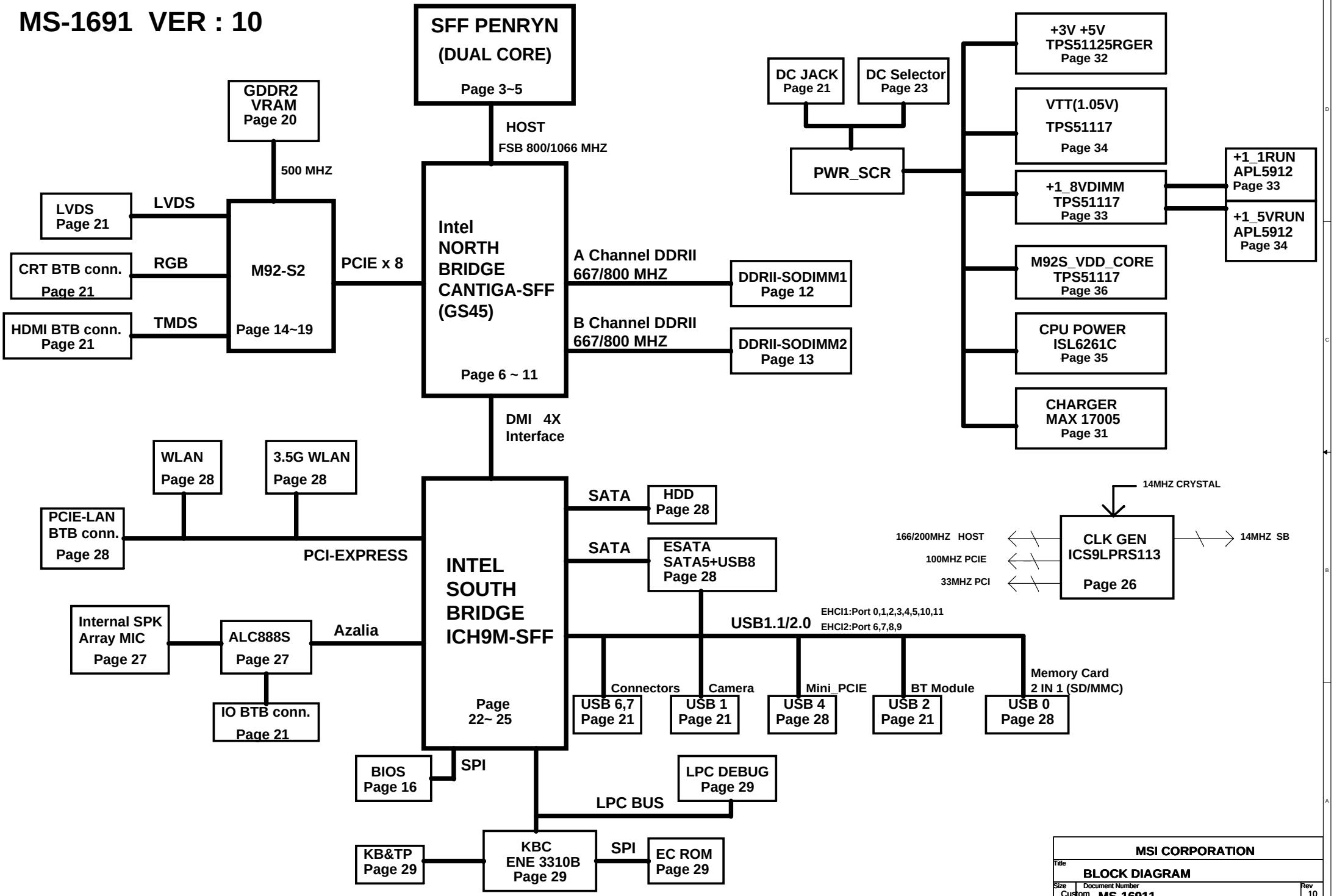
MS-1691 VER : 10



MSI CORPORATION

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 1 of 38

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHCORE	Core Voltage for Processor	VR_ON
VTT	1.05 rail for Processor & 965GM I/O	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5)	RUN_ON
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
SMDDR_VTERM	0.9V DDR Termination voltage (off in S3-S5)	RUN_ON
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	DIMM_ON
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
ADD5V	5.0V Power rail Audio codec(off in S3-S5)	RUND

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

POWER STATES

Wake on LAN:Enable

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks	+1_8VDIMM
Full ON	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW	ON
S3(Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF	ON
S4(Suspend to Disk)	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	ON	ON	OFF	OFF	OFF

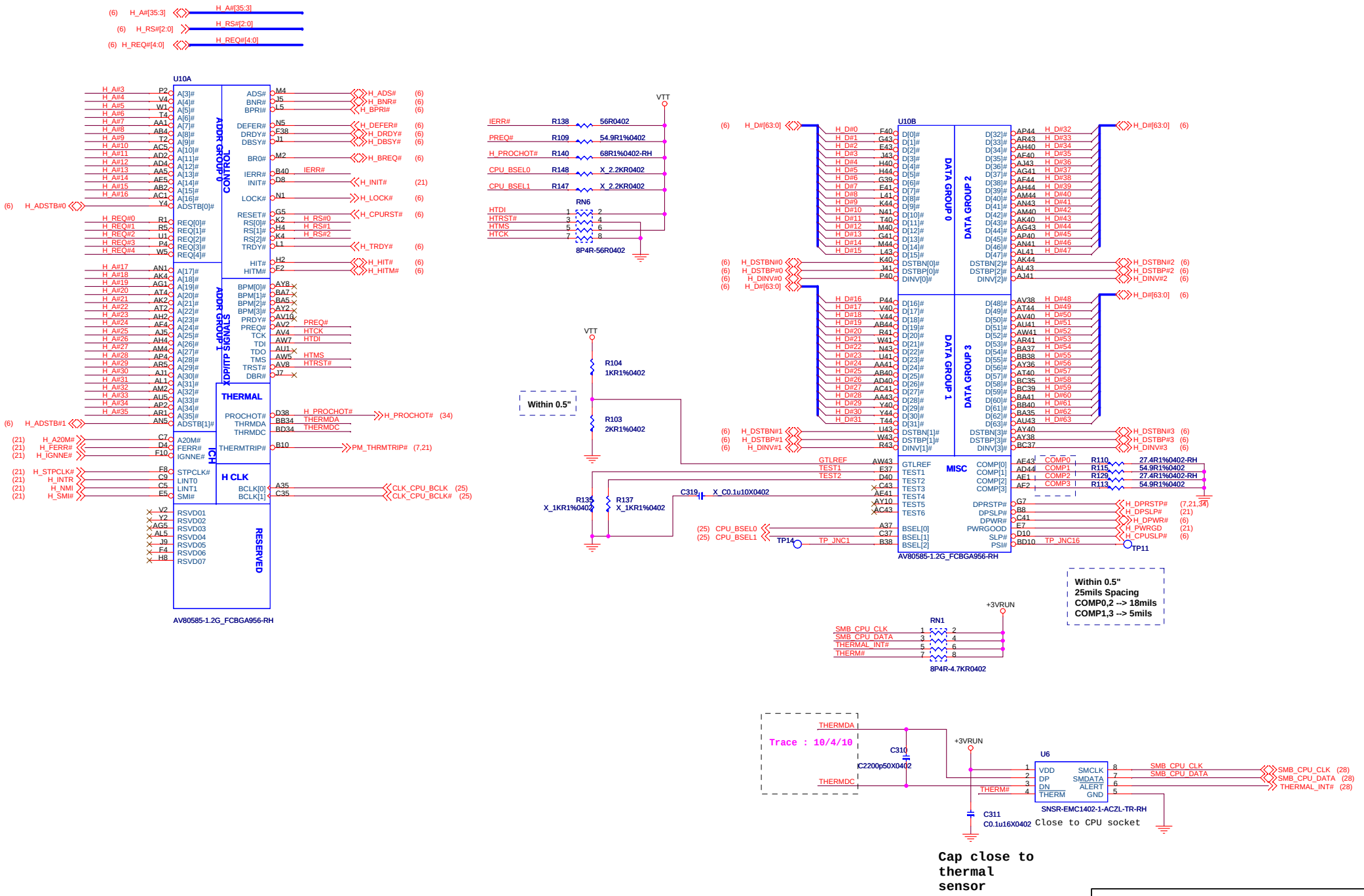
*Note : WHEN AC MODE , System turn on then +V*SUS will always keep high*

MSI CORPORATION

Title: PLATFORM

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 2 of 38



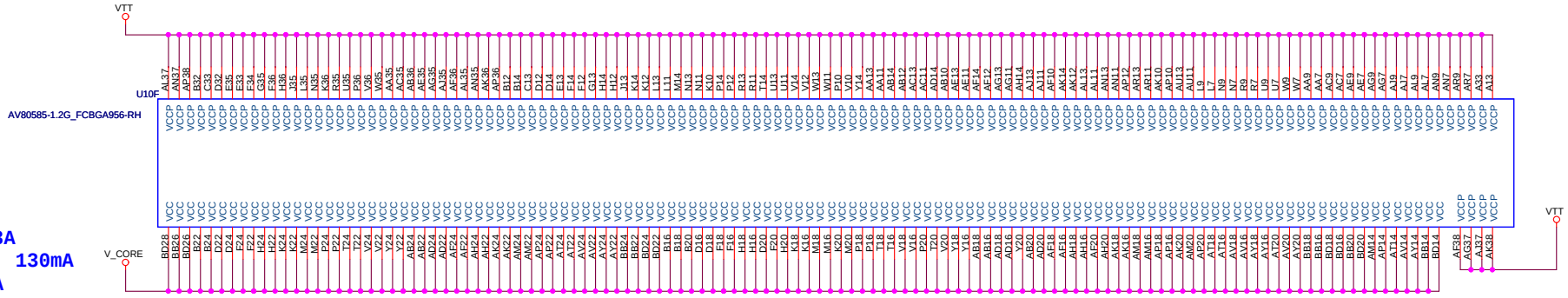
MSI CORPORATION

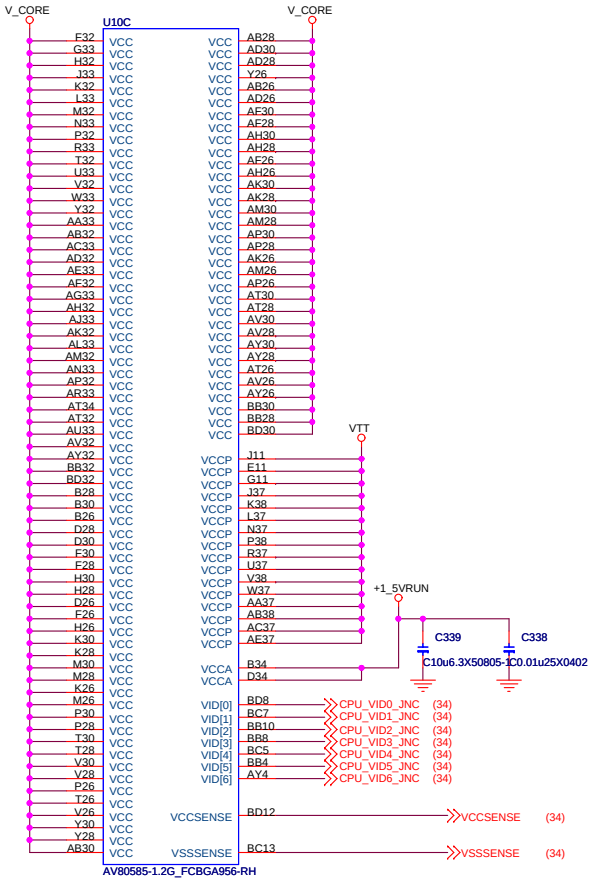
Title: SFF PENRYN-1 (HOST BUS)

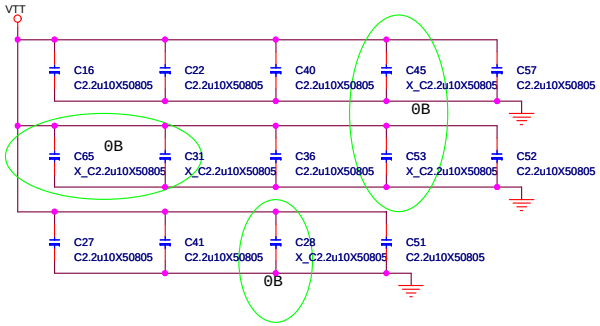
Size: Custom | Document Number: MS-16911 | Rev: 10

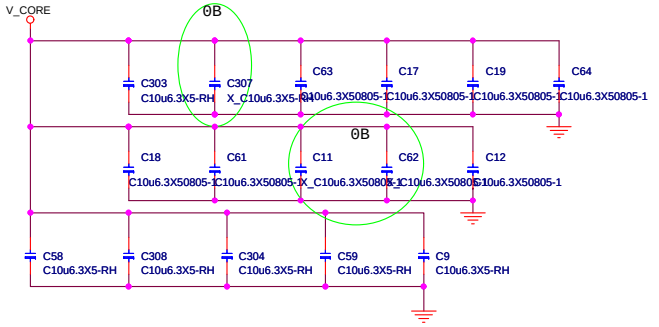
Date: Saturday, April 18, 2009 | Sheet 3 of 38

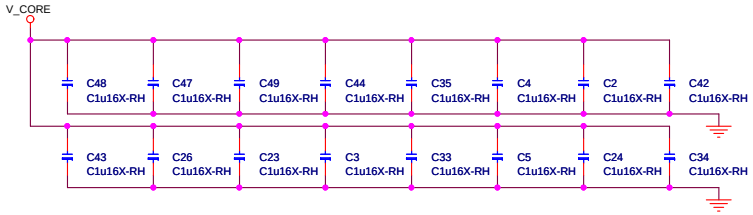
VCC (V_Core) : 13A
VCCA (+1_5VRUN) : 130mA
VCCP (VTT) : 2.5A



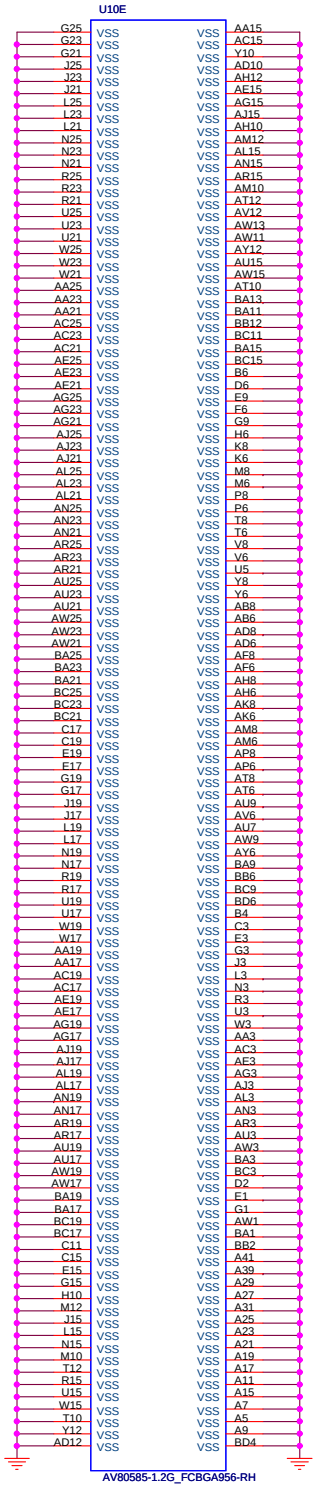




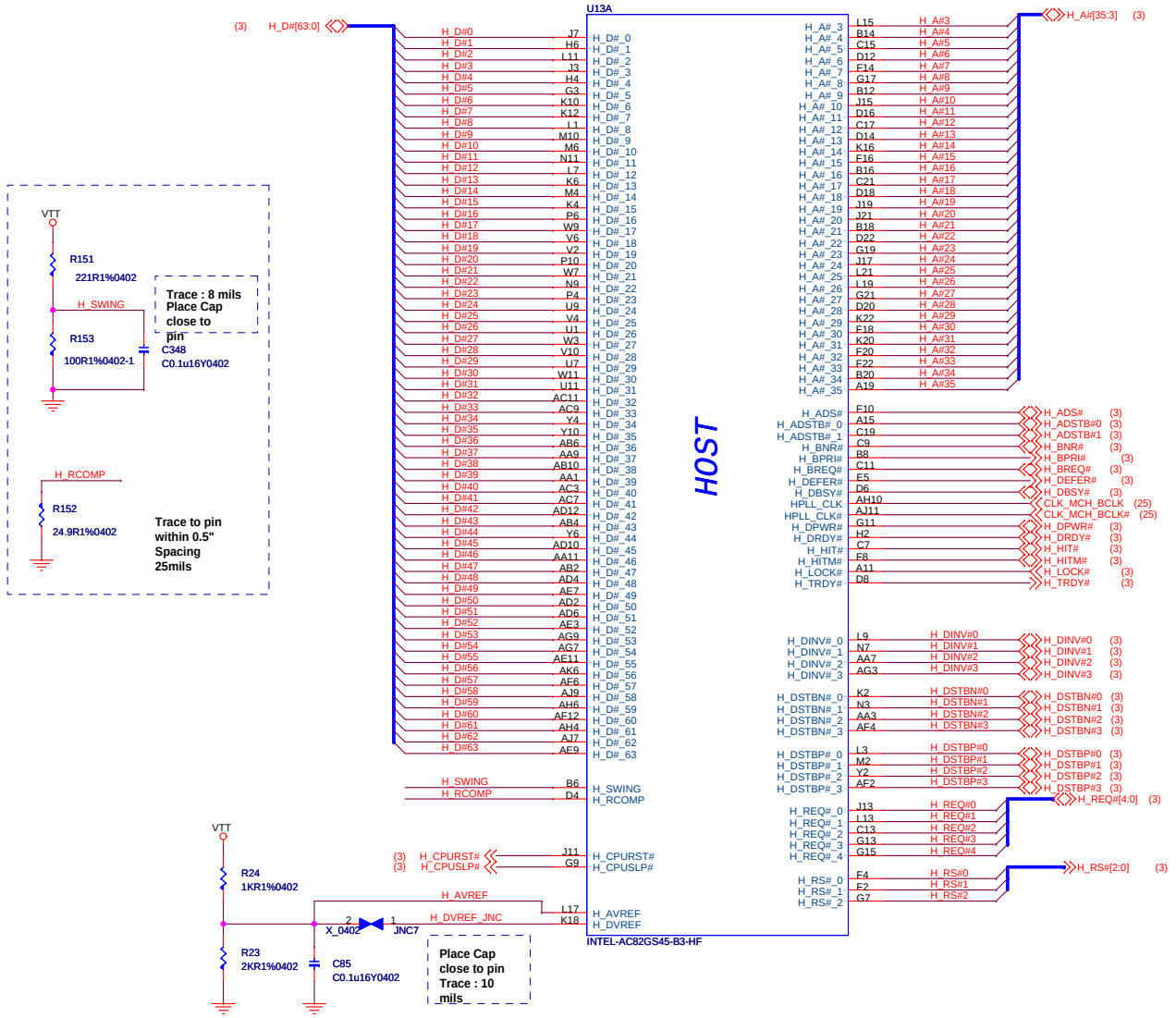




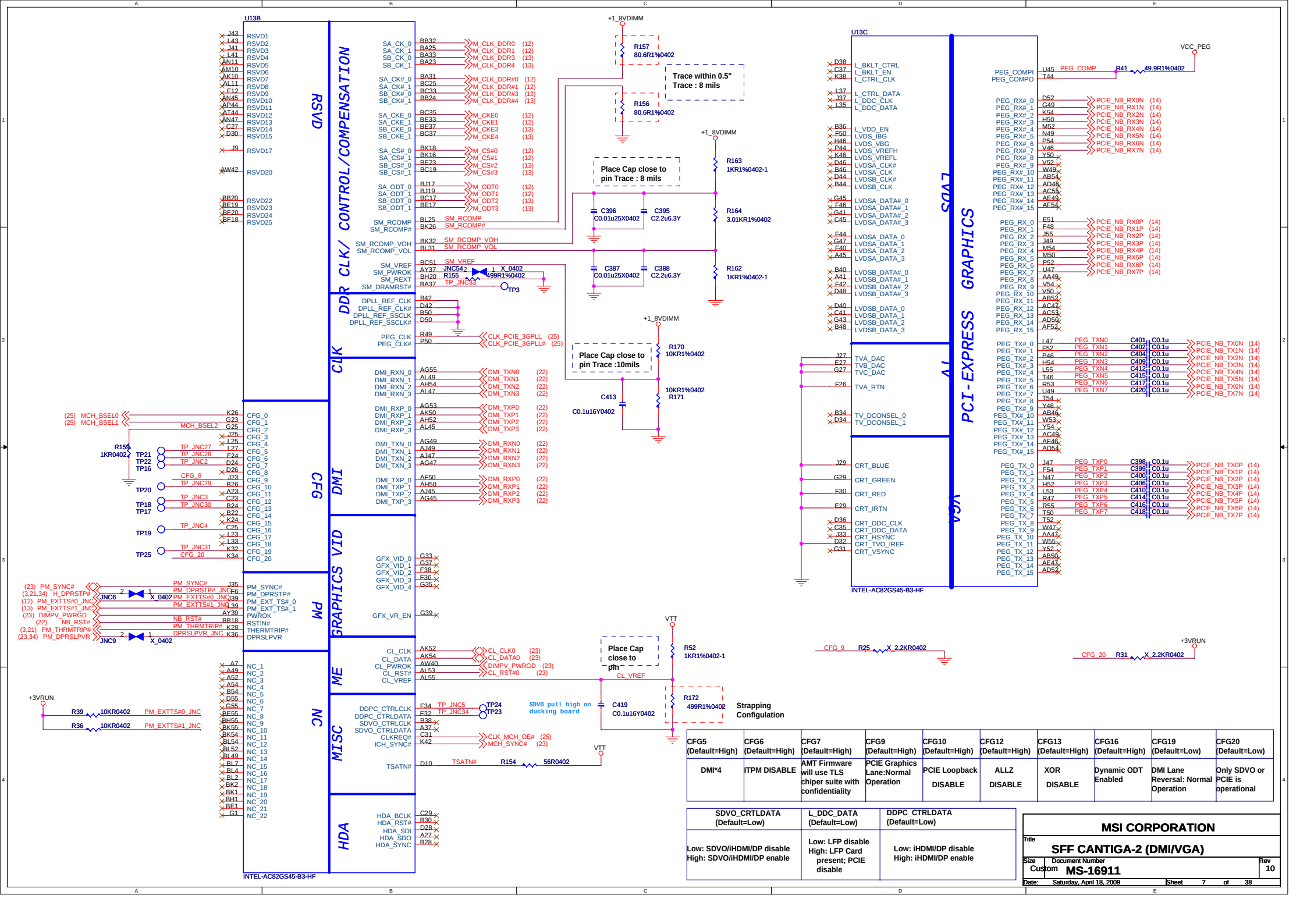
MSI CORPORATION		
Title: SFF PENRYN-2 (POWER)		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 4 of 38	



MSI CORPORATION		
Title: SFF Penryn-2 (GND)		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 5 of 38	

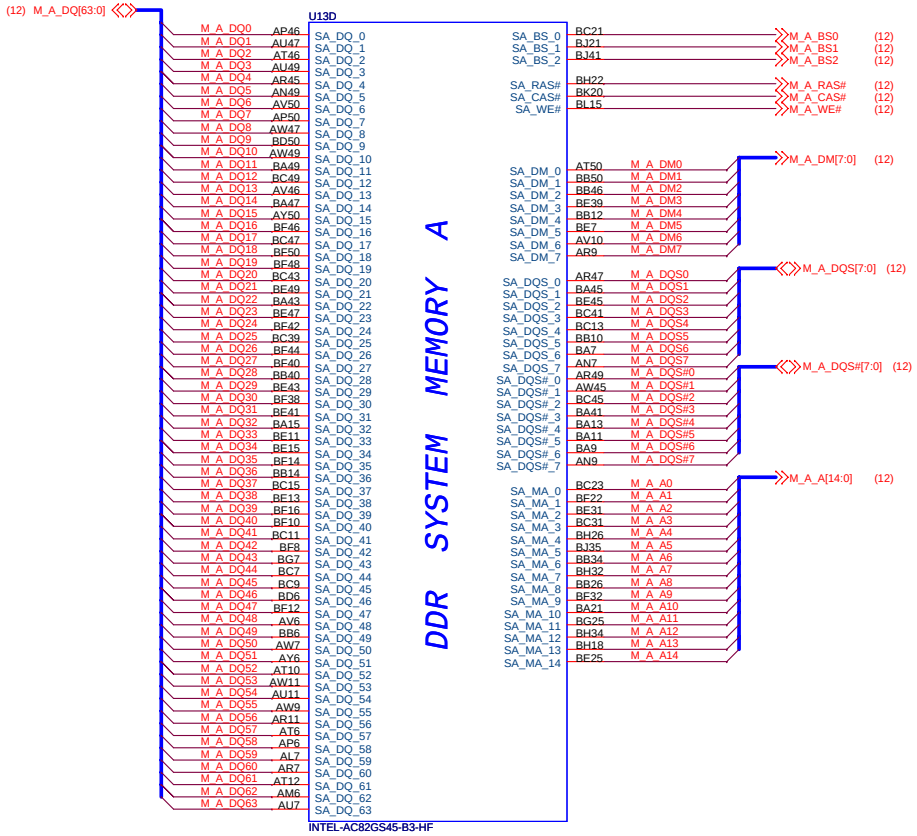


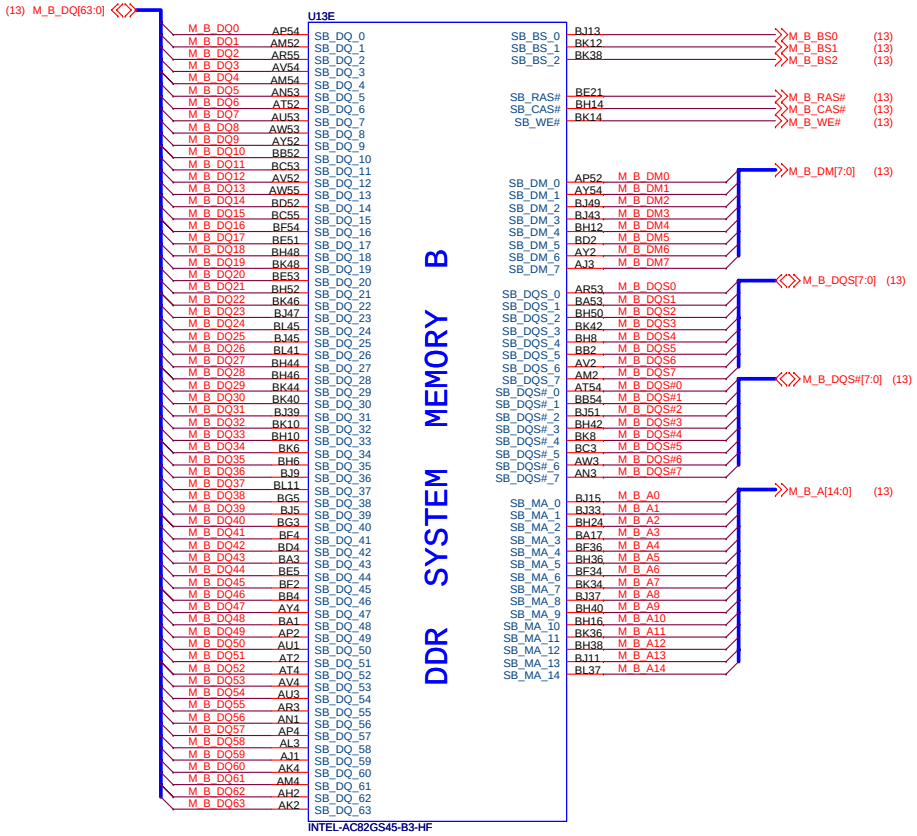
MSI CORPORATION			
Title: SFF CANTIGA-1 (HOST BUS)			
Size: Custom	Document Number: MS-16911		Rev: 10
Date: Saturday, April 18, 2009		Sheet 6 of 38	



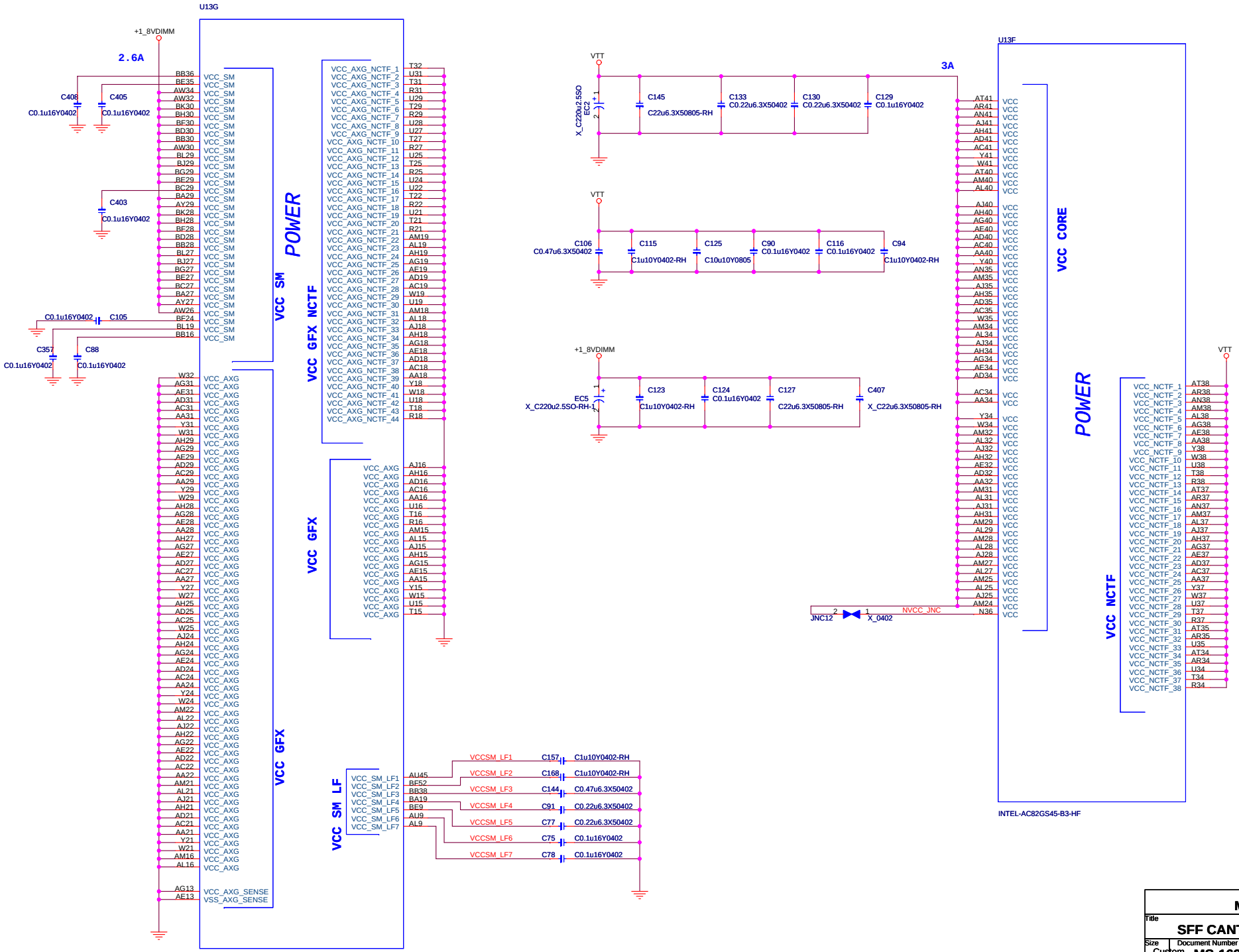
CFG5 (Default=High)	CFG6 (Default=High)	CFG7 (Default=High)	CFG9 (Default=High)	CFG10 (Default=High)	CFG12 (Default=High)	CFG13 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)
DMI*4	ITPM DISABLE	AMT Firmware will use TLS chiper suite with confidentiality	PCIE Graphics Lane:Normal Operation	PCIE Loopback DISABLE	ALLZ DISABLE	XOR DISABLE	Dynamic ODT Enabled	DMI Lane Reversal: Normal Operation	Only SDVO or PCIE is operational

SDVO_CRTLDATA (Default=Low)	L_DDC_DATA (Default=Low)	DDPC_CTRLDATA (Default=Low)
Low: SDVO/iHDMI/DP disable High: SDVO/iHDMI/DP enable	Low: LFP disable High: LFP Card present; PCIE disable	Low: iHDMI/DP disable High: iHDMI/DP enable



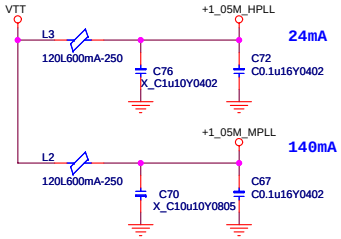


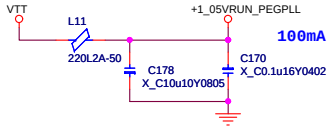
MSI CORPORATION		
Title: SFF CANTIGA-3 (DDRII)		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 8 of 38	

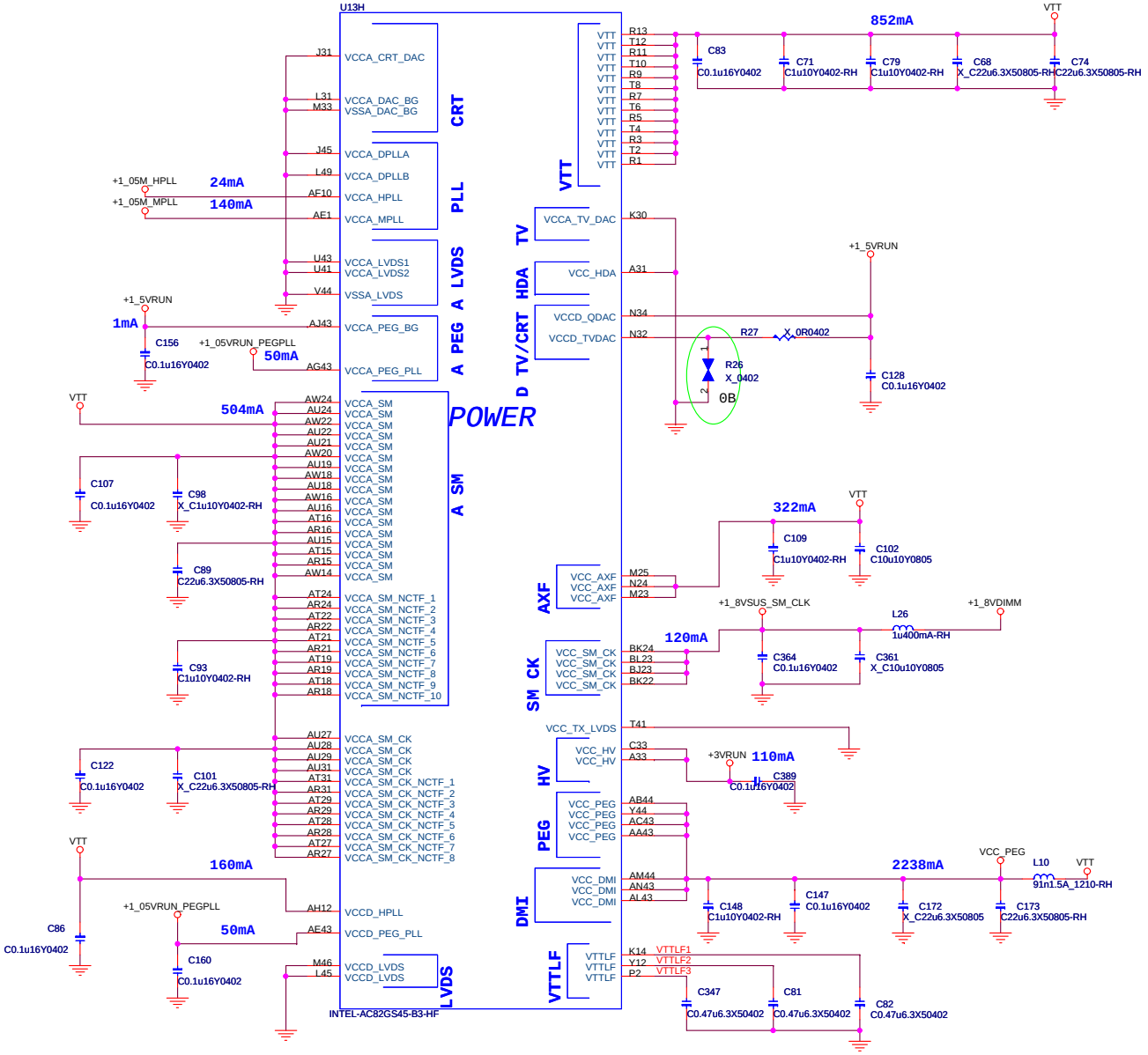


Title	SFF CANTIGA-4 (POWER-1)
Size	Custom
Document Number	MS-16911
Rev	10
Date:	Saturday, April 18, 2009
Sheet	9 of 38

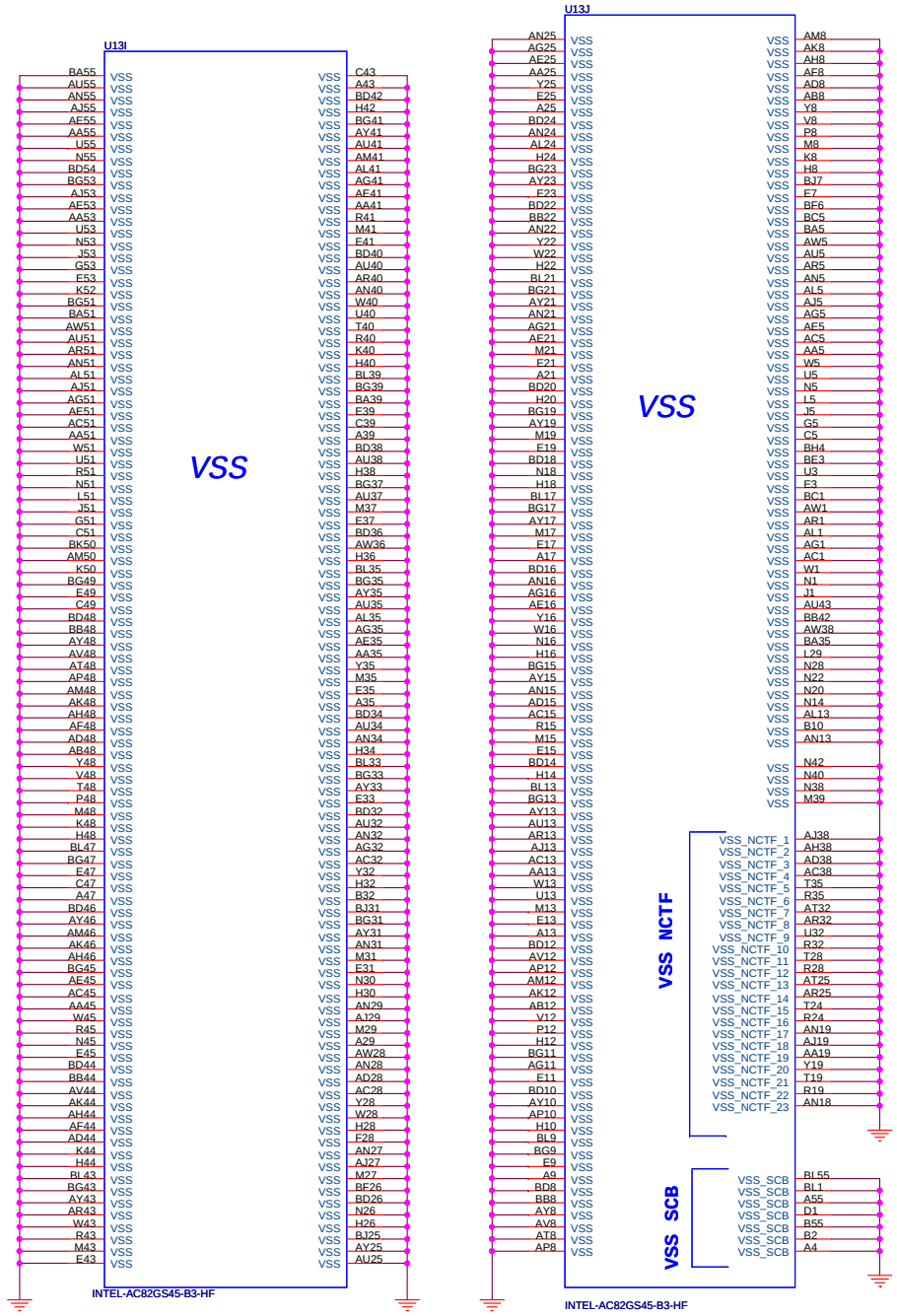
MSI CORPORATION



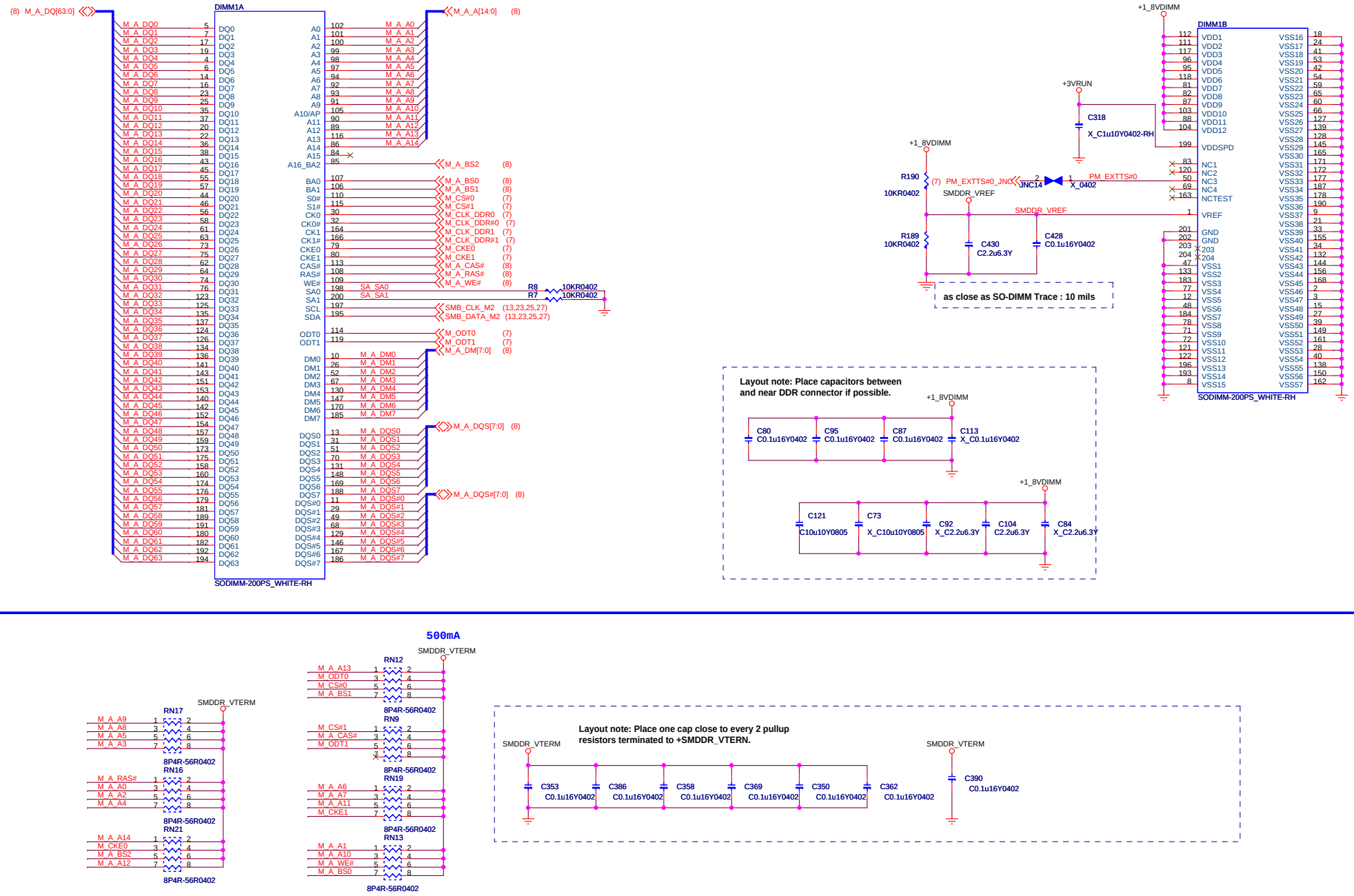




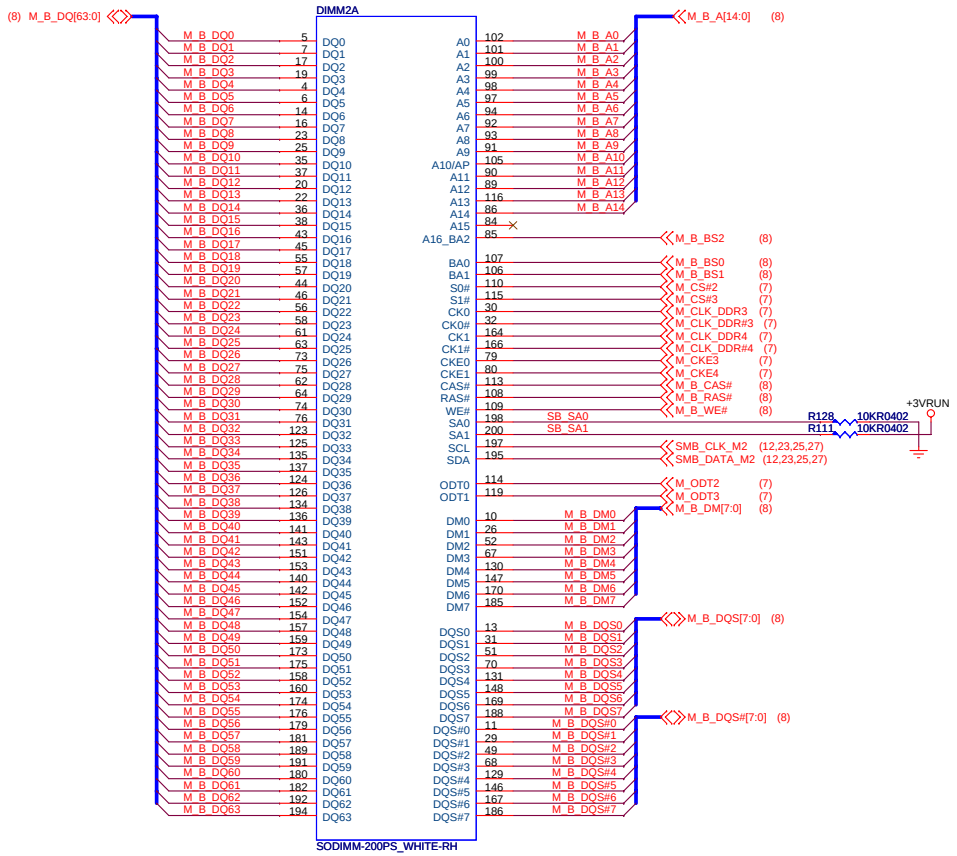
MSI CORPORATION		
Title: SFF CANTIGA-5 (POWER-2)		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 10 of 38	

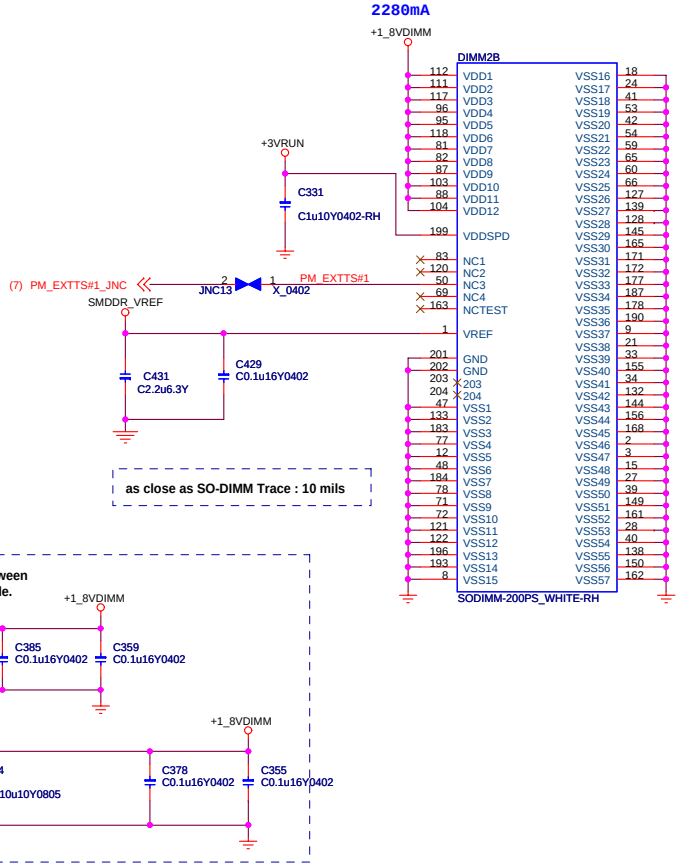


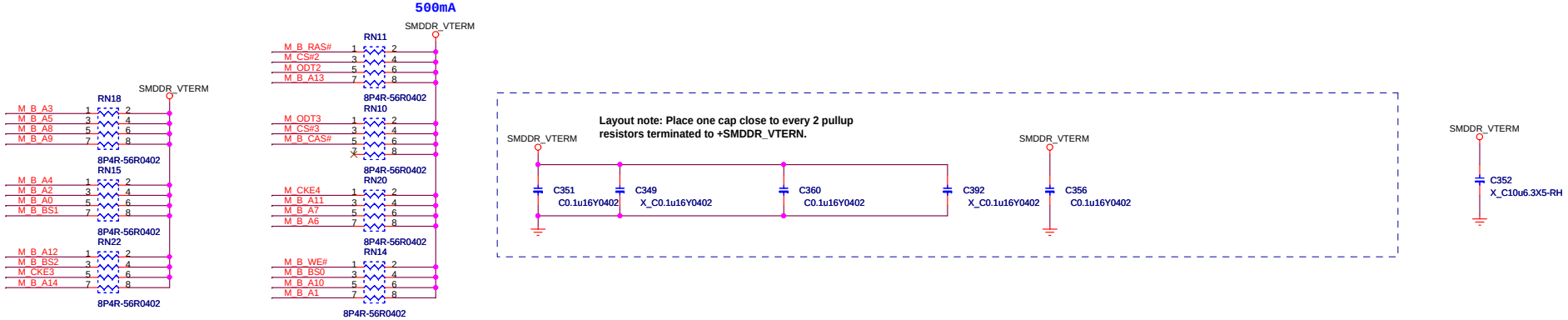
MSI CORPORATION	
Title	SFF GANTIGA-6 (VSS)
Size: Custom	Document Number: MS-16911
Rev: 10	
Date: Saturday, April 18, 2009	Sheet 11 of 38



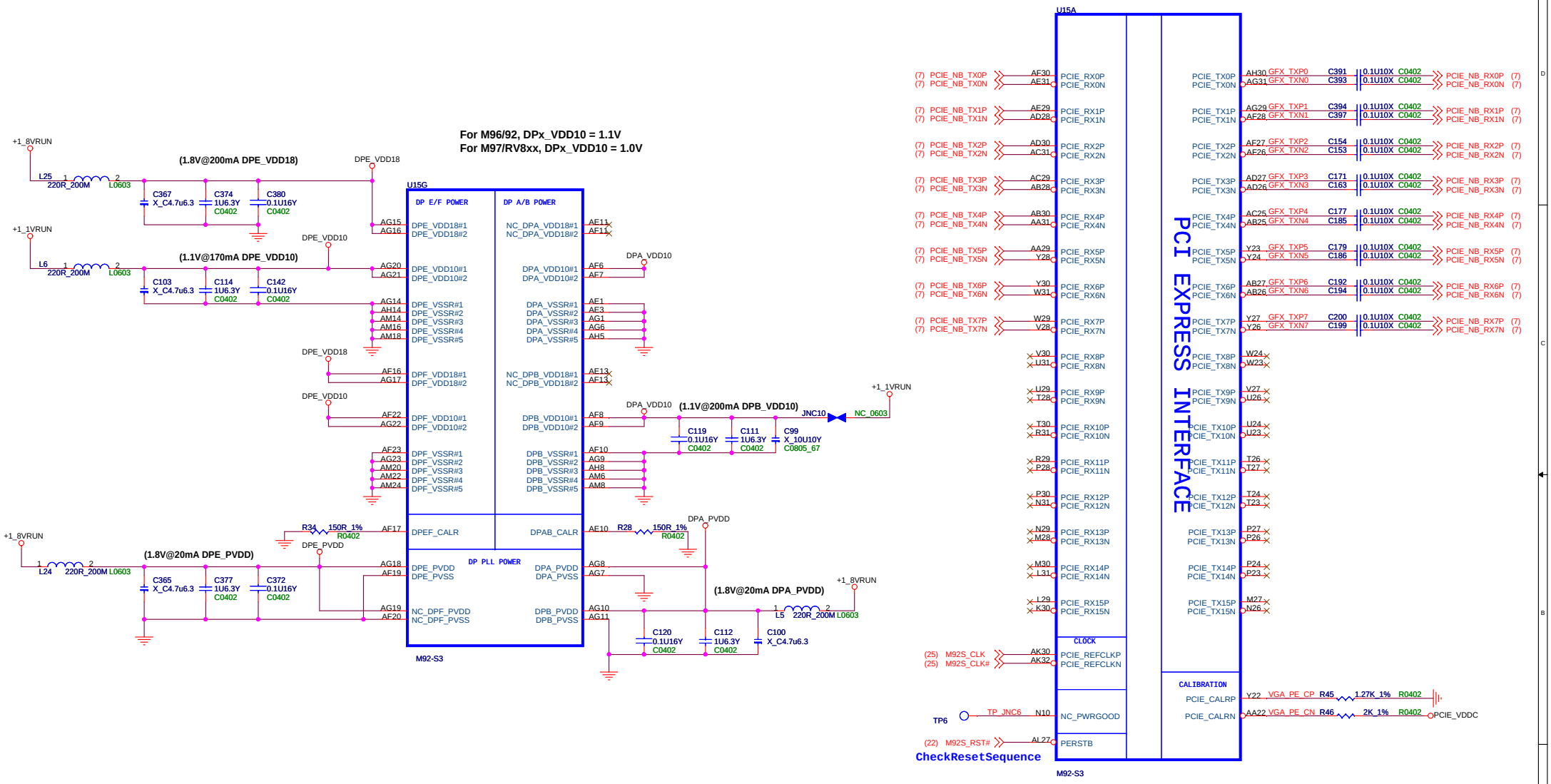
Company	MSI CORPORATION
Title	DDR2 SODIMM & TREMINATION
Size	Custom
Document Number	MS-16911
Rev	10
Date:	Saturday, April 18, 2009
Sheet	12 of 38



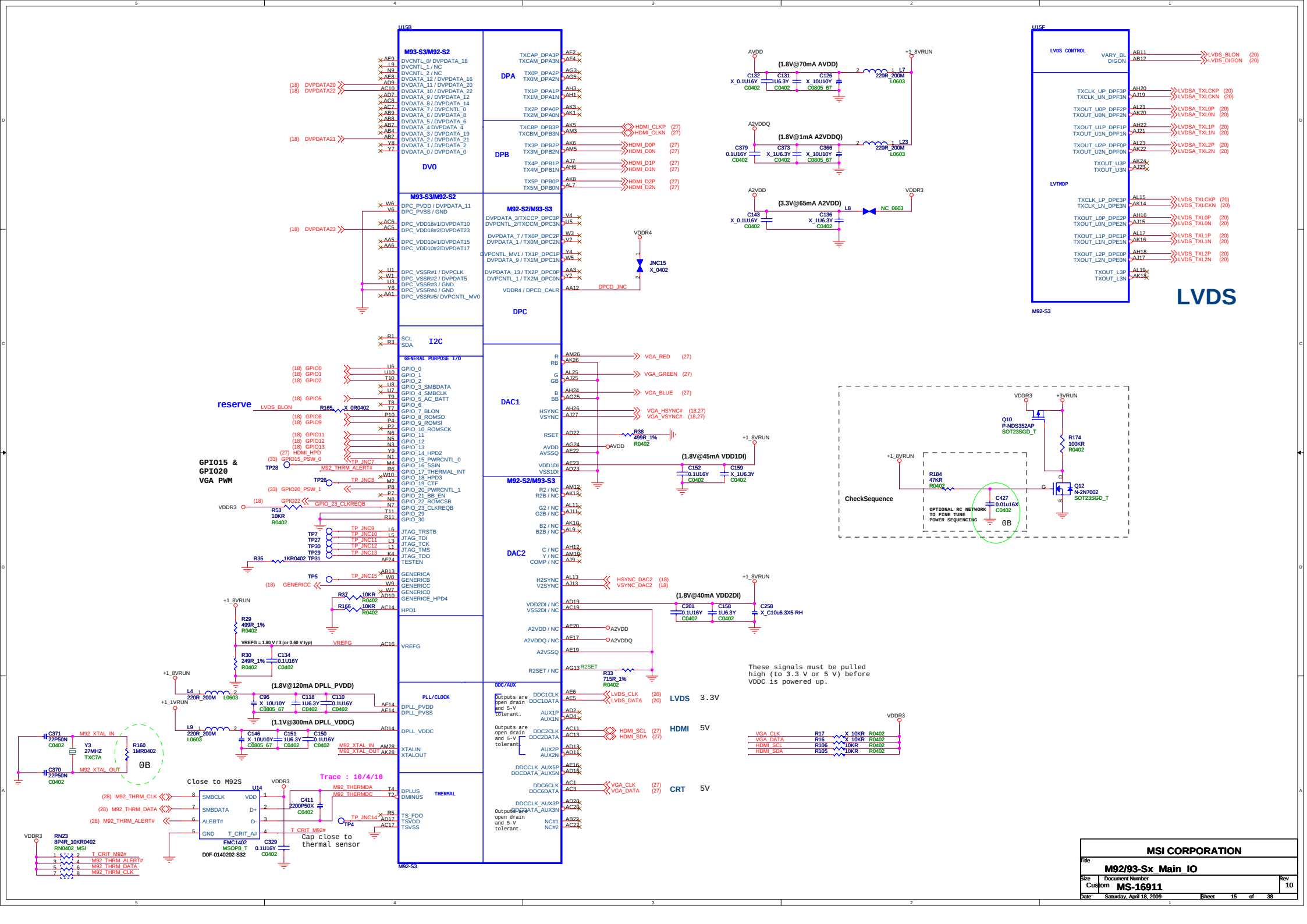


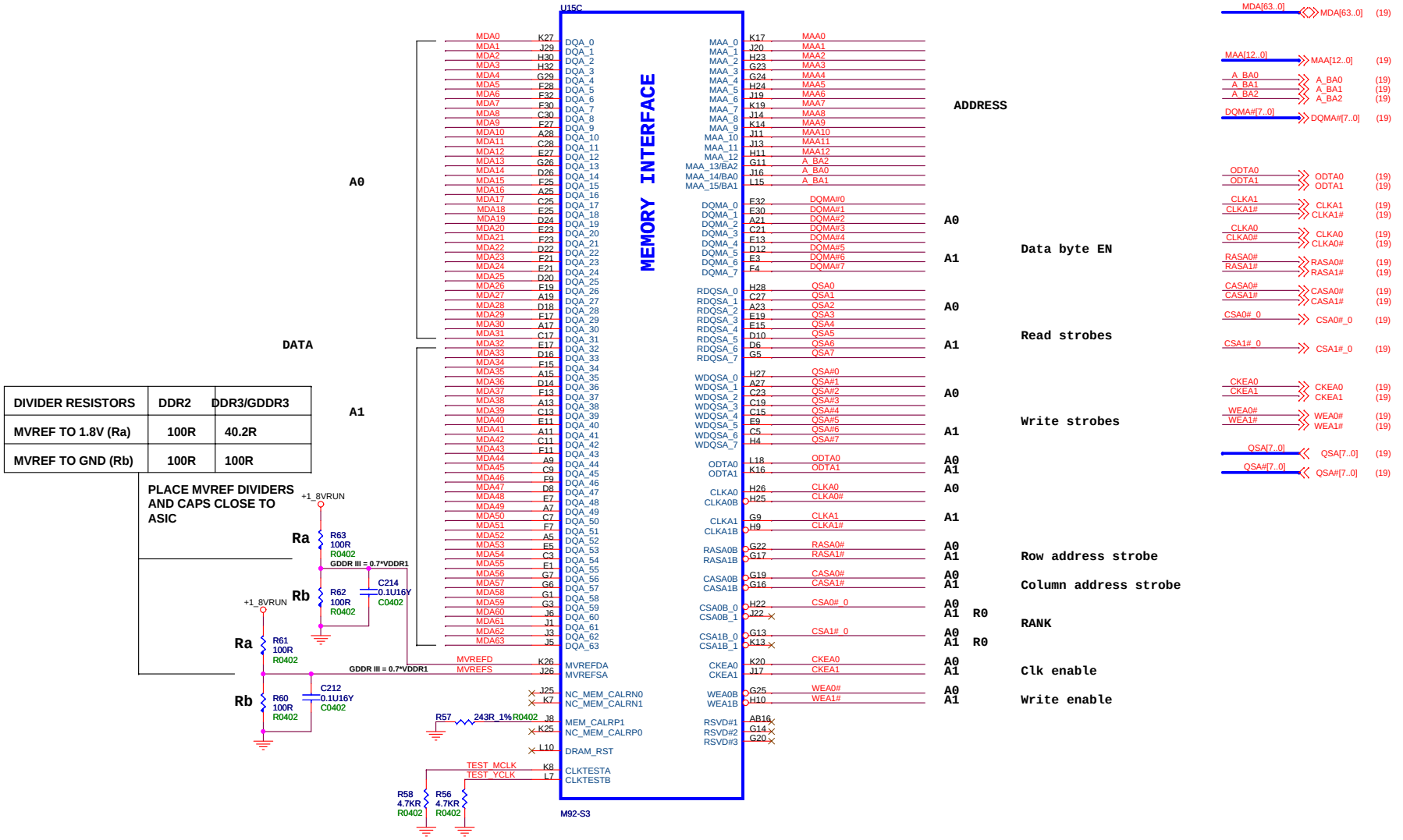


MSI CORPORATION		
Title: DDR2 SODIMM & TREMINATION		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 13 of 38	

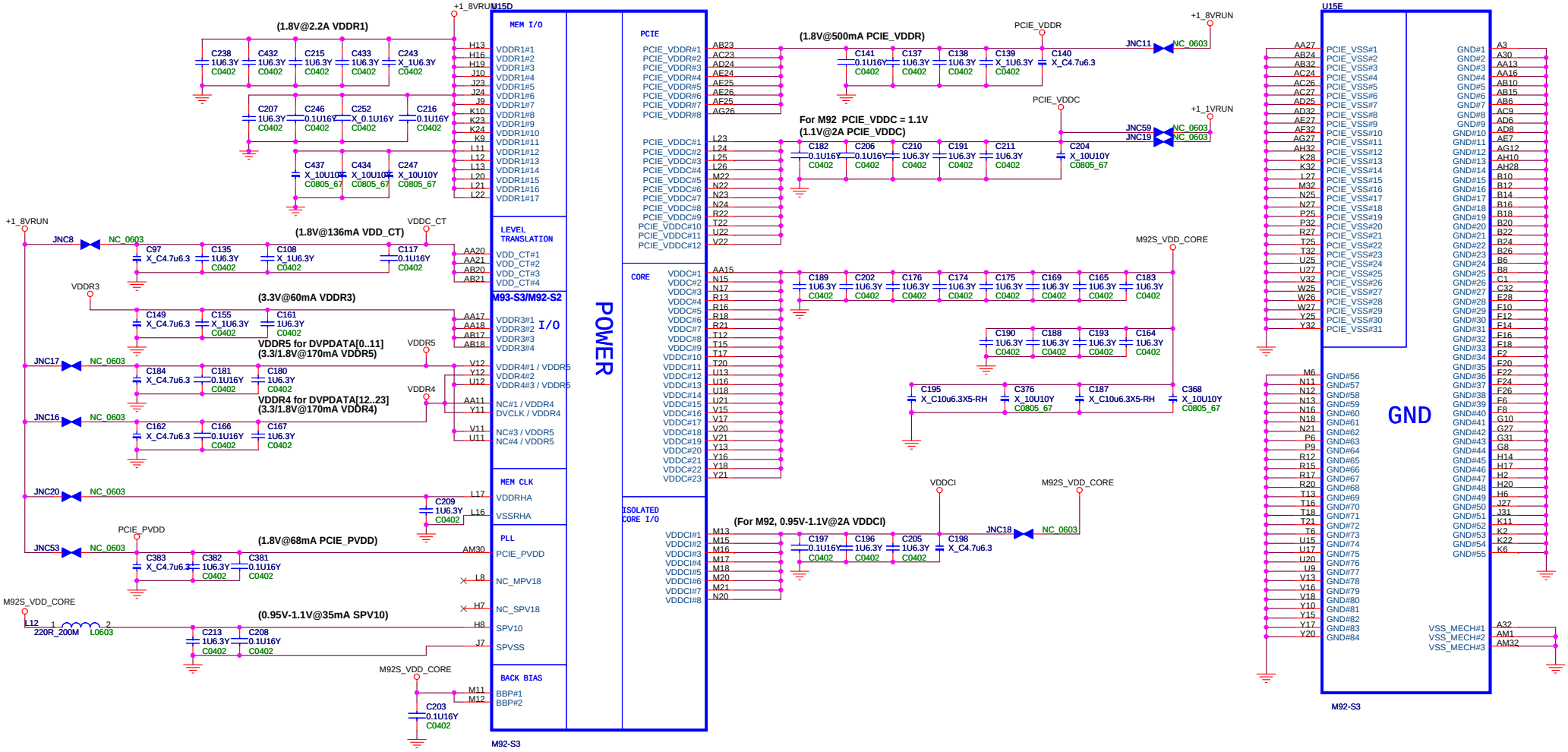


MSI CORPORATION	
Title	M92/93-Sx(PCIE_Interface)
Size: Custom	Document Number: MS-16911
Rev	10
Date: Saturday, April 18, 2009	Sheet 14 of 38


U15B
M93-S3/M92-S2
DVCNTL_0/ DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / NC
DVDATA_12 / DVPDATA_16
DVDATA_11 / DVPDATA_20
DVDATA_10 / DVPDATA_22
DVDATA_9 / DVPDATA_12
DVDATA_8 / DVPDATA_14
DVDATA_7 / DVPCNTL_0
DVDATA_6 / DVPDATA_8
DVDATA_5 / DVPDATA_6
DVDATA_4 DVPDATA_4
DVDATA_3 / DVPDATA_19
DVDATA_2 / DVPDATA_21
DVDATA_1 / DVPDATA_2
DVDATA_0 / DVPDATA_0
DVO
DPA
DPB
DPC
I2C
SCL
SDA
GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
GPIO_29
GPIO_30
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1
VREFG
PLL/CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT
THERMAL
DPLUS
DMINUS
TS_FDO
TSVDD
TSVSS
M92-S3
M93-S2/M93-S3
DPC_PVDD / DVPDATA_11
DPC_PVSS / GND
DPC_VDD18#1/DVPDAT10
DPC_VDD18#2/DVPDAT23
DPC_VDD10#1/DVPDAT15
DPC_VDD10#2/DVPDAT17
DPC_VSSR#1 / DVPCLK
DPC_VSSR#2 / DVPDAT5
DPC_VSSR#3 / GND
DPC_VSSR#4 / GND
DPC_VSSR#5/ DVPCNTL_MV0
M92-S2/M93-S3
DVPDATA_3/TXCCP_DPC3P
DVPCNTL_2/TXCCM_DPC3N
DVPDATA_7 / TX0P_DPC2P
DVPDATA_1 / TX0M_DPC2N
DVPCNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPCNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR
DPCD_JNC
JNC15
X_0402
M92-S2/M93-S3
R / RB
G / GB
B / BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC
DAC1
DAC2
DDC/AUX
H2SYNC
V2SYNC
VDD2DI / NC
VSS2DI / NC
A2VDD / NC
A2VDDQ / NC
A2VSSQ
R2SET / NC
DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCCLK_AUX5P
DDCDATA_AUX5N
DDC6CLK
DDC6DATA
DDCCLK_AUX3P
DDCDATA_AUX3N
NC#1
NC#2
Outputs are open drain and 5-V tolerant.
VGA_RED (27)
VGA_GREEN (27)
VGA_BLUE (27)
VGA_HSYNC# (18,27)
VGA_VSYNC# (18,27)
HSYNC_DAC2 (18)
VSYNC_DAC2 (18)
LVDS_CLK (20)
LVDS_DATA (20)
LVDS 3.3V
HDMI_SCL (27)
HDMI_SDA (27)
HDMI 5V
VGA_CLK (27)
VGA_DATA (27)
CRT 5V
HDMI_CLKP (27)
HDMI_CLKN (27)
HDMI_D0P (27)
HDMI_D0N (27)
HDMI_D1P (27)
HDMI_D1N (27)
HDMI_D2P (27)
HDMI_D2N (27)
DVPDATA20
DVPDATA22
DVPDATA21
DVPDATA23
GPIO0
GPIO1
GPIO2
GPIO5
GPIO8
GPIO9
GPIO11
GPIO12
GPIO13
HDMI_HPD
GPIO15_PSW_0
GPIO20_PSW_1
GPIO22
GENERICC
GPIO_23_CLKREQB
LVDS_BLON
R165 X_0R0402
TP_JNC7
M92_THRM_ALERT#
TP_JNC8
TP_JNC9
TP_JNC10
TP_JNC11
TP_JNC12
TP_JNC13
TP_JNC15
TP_JNC14
R53 10KR R0402
R35 1KR0402
R37 10KR R0402
R166 10KR R0402
R29 499R_1% R0402
R30 249R_1% R0402
C134 0.1U16Y C0402
VREFG = 1.80 V / 3 (or 0.60 V typ)
(1.8V@120mA DPLL_PVDD)
(1.1V@300mA DPLL_VDDC)
L4 220R_200M L0603
L9 220R_200M L0603
C96 X_10U10Y C0805_67
C118 1U6.3Y C0402
C110 0.1U16Y C0402
C146 X_10U10Y C0805_67
C151 1U6.3Y C0402
C150 0.1U16Y C0402
C371 22P50N C0402
C370 22P50N C0402
Y3 27MHZ TXC7A
R160 1MR0402
0B
M92_XTAL_IN
M92_XTAL_OUT
Close to M92S
Trace : 10/4/10
U14
EMC1402 MSOP8_T D0F-0140202-S32
C411 2200P50X C0402
C329 0.1U16Y C0402
Cap close to thermal sensor
M92_THERMDA
M92_THERMDC
T_CRIT_M92#
RN23 8P4R_10KR0402 RN0402_MSI
M92_THRM_CLK
M92_THRM_DATA
M92_THRM_ALERT#
reserve
GPIO15 & GPIO20 VGA PWM
(1.8V@70mA AVDD)
(1.8V@1mA A2VDDQ)
(3.3V@65mA A2VDD)
(1.8V@45mA VDD1DI)
(1.8V@40mA VDD2DI)
L7 220R_200M L0603
L23 220R_200M L0603
L8 NC_0603
R38 499R_1% R0402
C152 0.1U16Y C0402
C159 X_1U6.3Y C0402
C201 0.1U16Y C0402
C158 1U6.3Y C0402
C258 X_C10u6.3X5-RH
R33 715R_1% R0402
These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.
U15F
LVDS CONTROL
VARY_BL
DIGON
LVDS_BLON (20)
LVDS_DIGON (20)
TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
LVDSA_TXLCKP (20)
LVDSA_TXLCKN (20)
LVDSA_TXL0P (20)
LVDSA_TXL0N (20)
LVDSA_TXL1P (20)
LVDSA_TXL1N (20)
LVDSA_TXL2P (20)
LVDSA_TXL2N (20)
LVTMDP
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N
LVDS_TXLCKP (20)
LVDS_TXLCKN (20)
LVDS_TXL0P (20)
LVDS_TXL0N (20)
LVDS_TXL1P (20)
LVDS_TXL1N (20)
LVDS_TXL2P (20)
LVDS_TXL2N (20)
M92-S3
LVDS
CheckSequence
Q10 P-NDS352AP SOT23SGD_T
Q12 N-2N7002 SOT23SGD_T
R174 100KR R0402
R184 47KR R0402
C427 0.01u16X C0402
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
MSI CORPORATION
M92/93-Sx_Main_IO
MS-16911
Rev 10
Saturday, April 18, 2009
Sheet 15 of 38



MSI CORPORATION		
Title: M92/93-Sx_MEM_Interface		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 16 of 38	



MSI CORPORATION	
Title	M92/93-Sx_Power & GND
Size: Custom	Document Number: MS-16911
Rev	10
Date: Saturday, April 18, 2009	Sheet 17 of 38

STRAPS

GPIO0
Transmitter Power Savings Enable
0: 50% Tx output swing
Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.)
1: Full Tx output swing

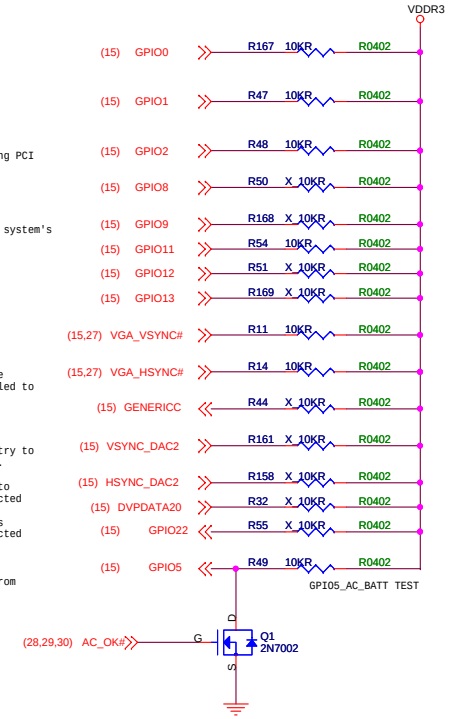
GPIO1
PCI Express Transmitter De-emphasis Enable
0: Tx de-emphasis disabled
1: Tx de-emphasis enabled

GPIO2
0 = Advertises the PCIe device as 2.5 GT/s capable at power-on.
1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.
Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).

GPIO9
VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space):
0 – VGA Controller capacity enabled
1 – The device will not be recognized as the system's VGA controller

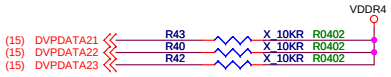
HSYNC VSYNC
AUD[1:0]:
00 - No audio function;
01 - Audio for DisplayPort and HDMI if adapter is detected;
10 - Audio for DisplayPort only;
11 - Audio for both DisplayPort and HDMI.
HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

V2SYNC
VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host interface.
0 - Driver would ignore the value sampled on DVPDATA_20 during reset.
1 - Driver would use the sampled value sampled at reset from DVPDATA_20 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, DVPDATA_20 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card.
Note:
If the strap is needed, it must be placed between the ball and the VSYNC output buffer. This output buffer prevents monitors from affecting the value at reset.



GPIO_13 12 11 Size of the primary memory apertures	CONFIG[3:0]
128MB	x000
256MB	x001
64MB	x010
32MB	x011
512MB	x100
1GB	x101
2GB	x110
4GB	x111

DVPDATA23	DVPDATA22	DVPDATA21	MEM_TYPE
0	0	0	SAMSUNG 64Mx16 (M12-K4N1G25-S02)
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

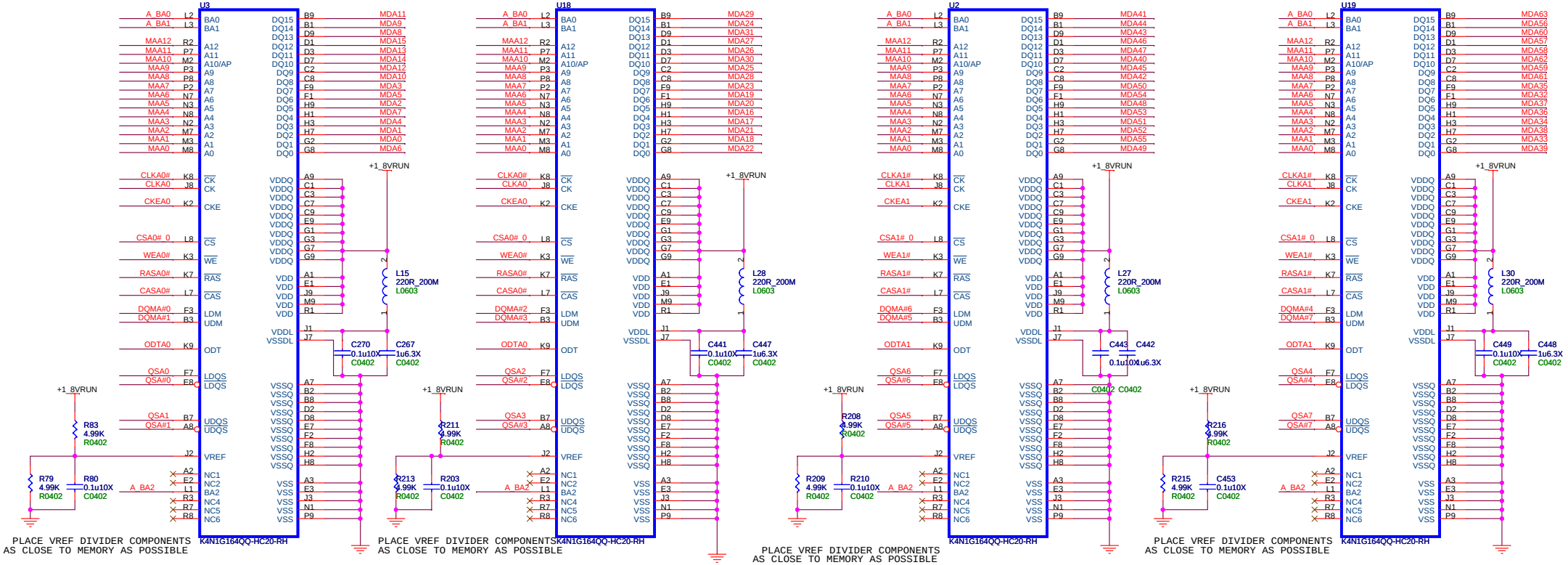
MSI CORPORATION

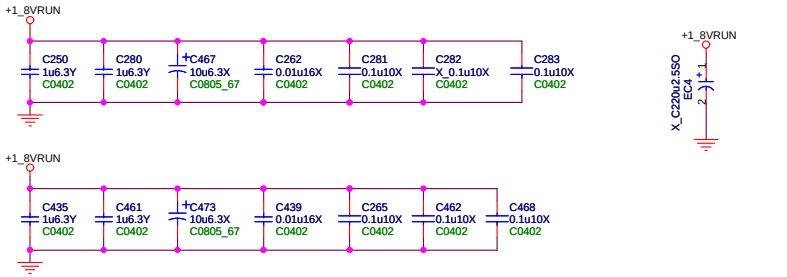
Title: M92/93-Sx_Straps & Thermal

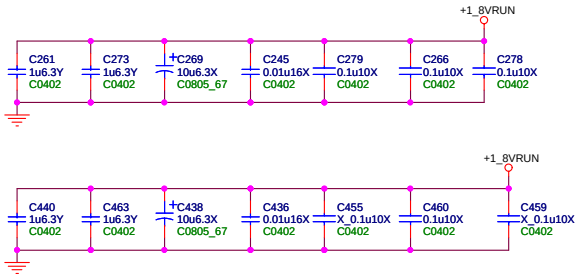
Size: Custom | Document Number: MS-16911 | Rev: 10

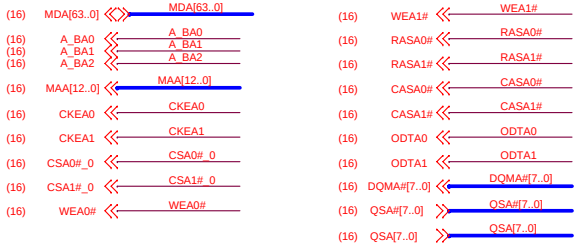
Date: Saturday, April 18, 2009 | Sheet 18 of 38

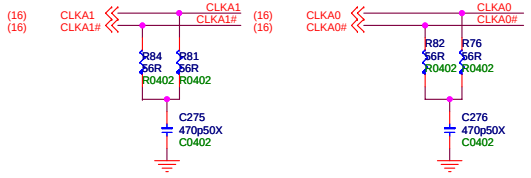
512MB DDR2 MEMORY









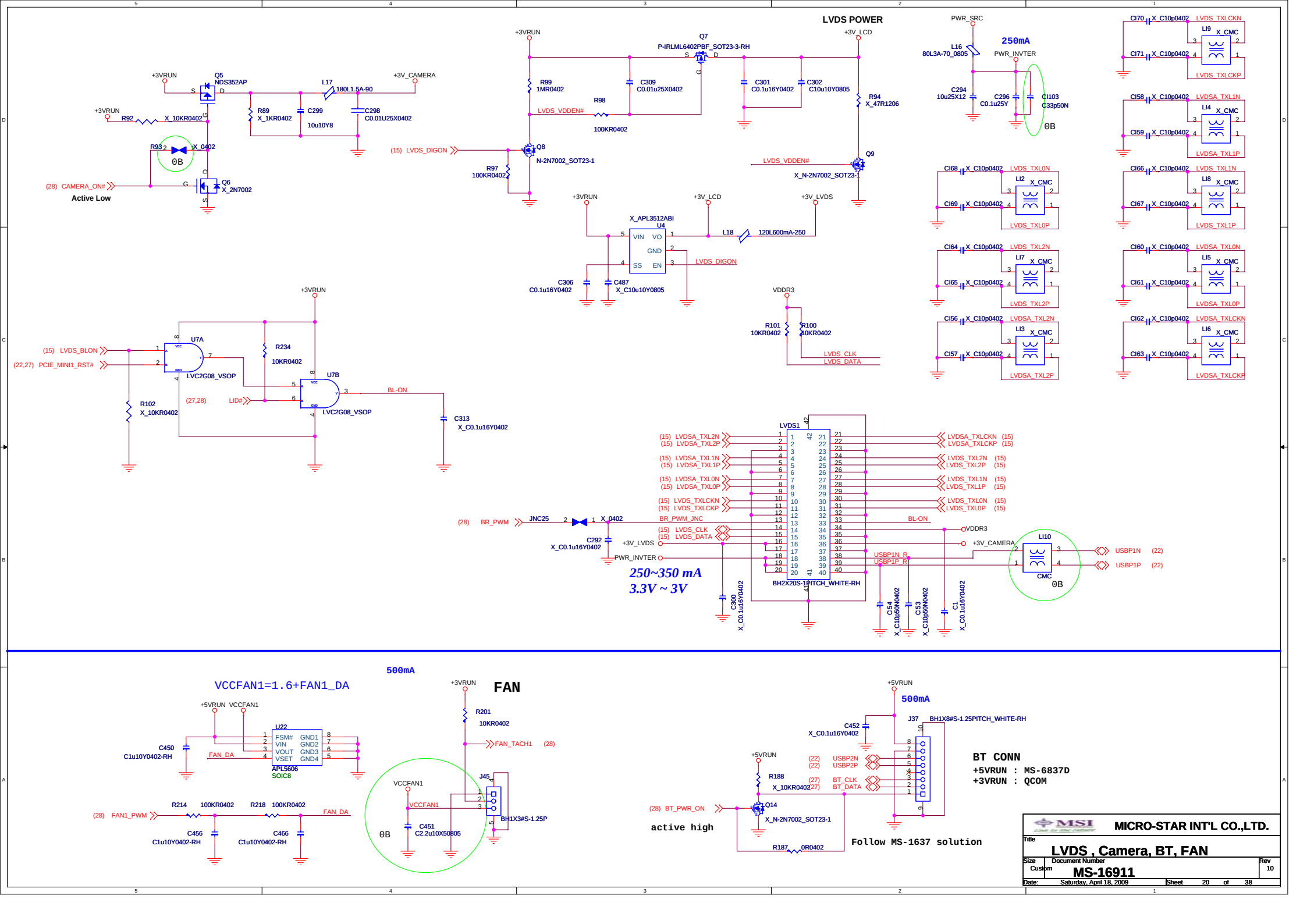


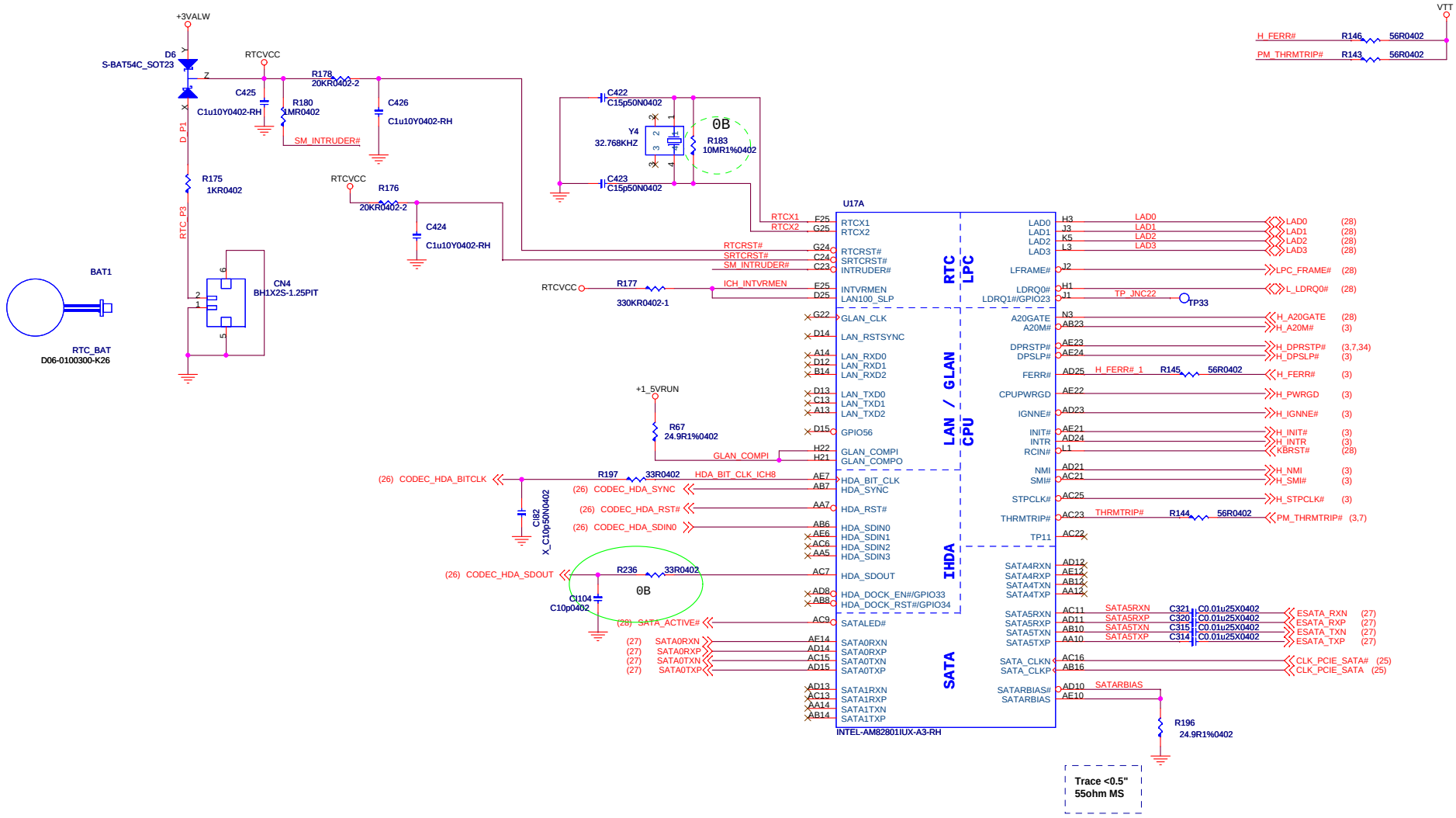
MSI MICRO-STAR INT'L CO.,LTD.

Title: DDR2 (64Mx16bit)

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 19 of 38


LVDS POWER
Active Low
250mA
0B
500mA
VCCFAN1=1.6+FAN1_DA
FAN
250~350 mA
3.3V ~ 3V
BT CONN
+5VRUN : MS-6837D
+3VRUN : QCOM
active high
Follow MS-1637 solution
MICRO-STAR INT'L CO.,LTD.
LVDS , Camera, BT, FAN
MS-16911
Saturday, April 18, 2009
Sheet 20 of 38



Strapping Configulation

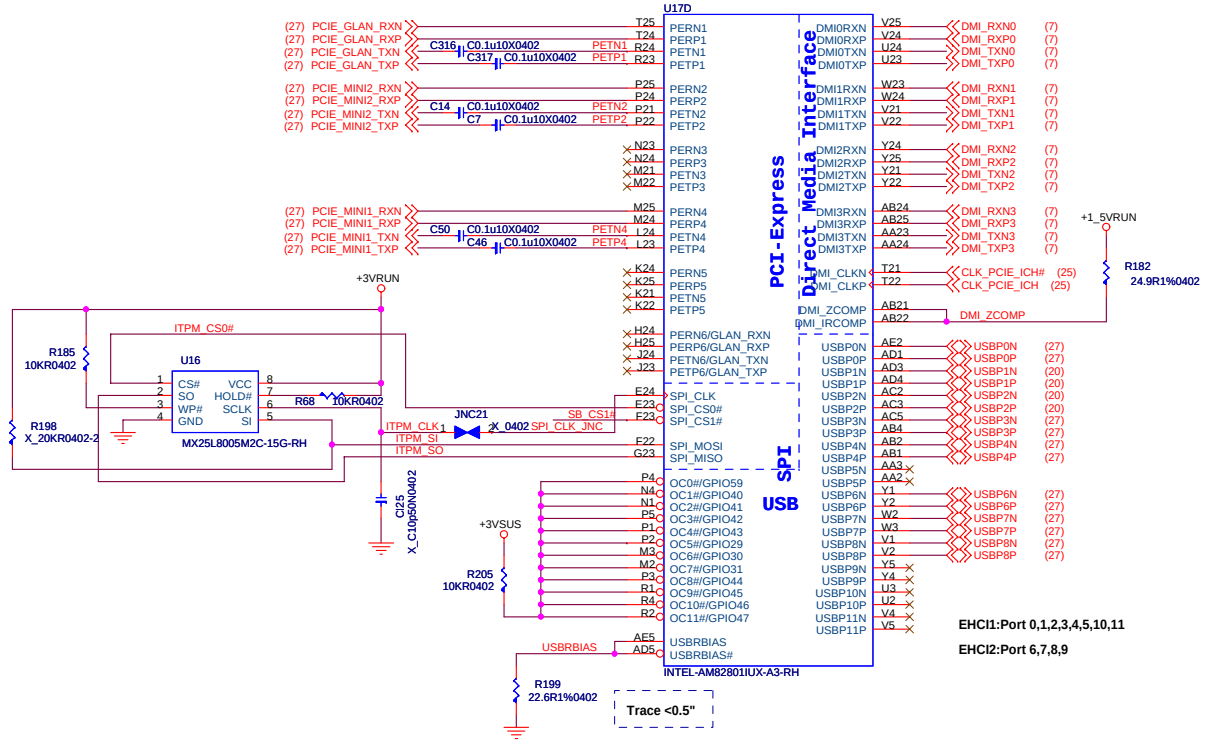
HDA_SDOUT (default=Low)	HDA_SYNC (Default=Low)	GNT2# / GPIO53 (Default=High)	GPIO20 (Default=Low)	GNT1# / GPIO51 (Default=High)	GNT3# / GPIO55 (Default=High)	GNT0# (Default=High)	SPI_CS1# / GPIO58 (Default=High)	SATALED (Default=High)	SPKR (Default=Low)	TP3 (Default=High)	GPIO33 / HDA_DOCK_EN# (Default=High)	GPIO49	SPI_MOSI (Default=Low)
Low : XOR Chain Entrance=Enable	PCI Express Port config 1 bit 0	PCI Express Port config 2 bit 2	Reserved	ESI Strap (Server Only) Should not be pull low for DT and NB.	Top-Block Swap Override	Boot BIOS destination GNT0#=0 & SPI_CS1#=1 : SPI BIOS		PCI Express Lane Reversal (Lanes 1-4)	High=No Reboot	XOR Chain Entrance	Flash Descriptor Security Override Strap	DMI Termination Voltage Low: for DT High: for NB	Integrated TPM enable Low: TPM disable

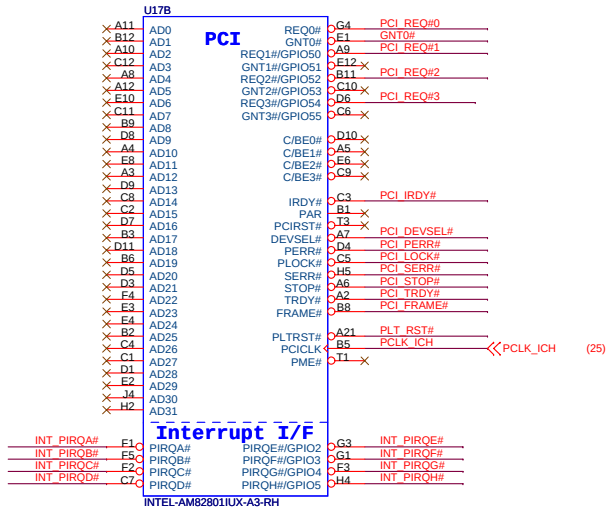
MICRO-STAR INT'L CO.,LTD.

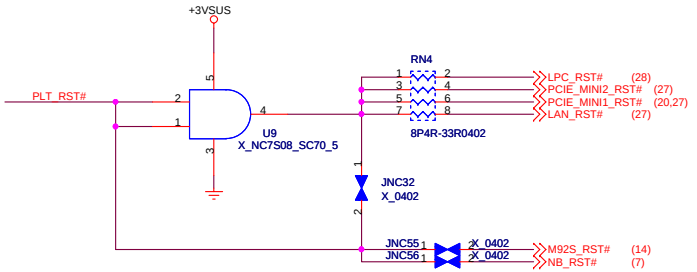
Title: SFF_ICH9M-1 (CPU/SATA/Azalia)

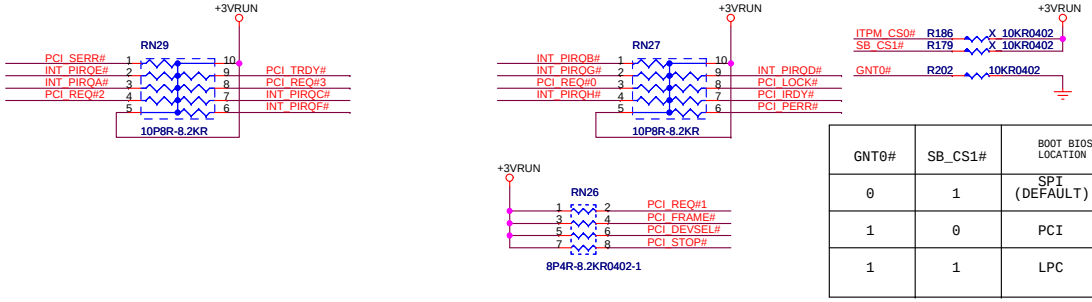
Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 21 of 38









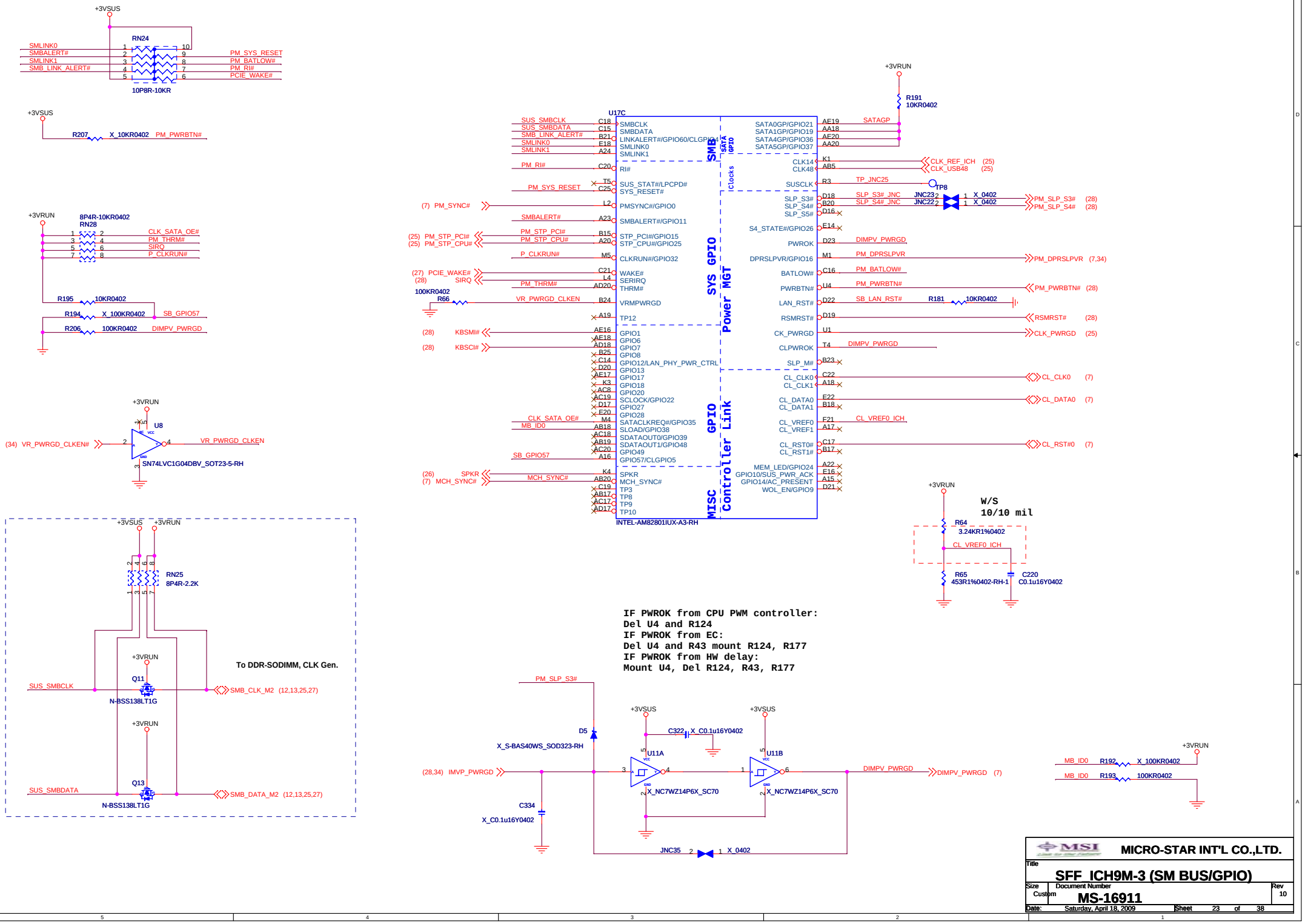
GNT0#	SB_CS1#	BOOT BIOS LOCATION
0	1	SPI (DEFAULT)
1	0	PCI
1	1	LPC

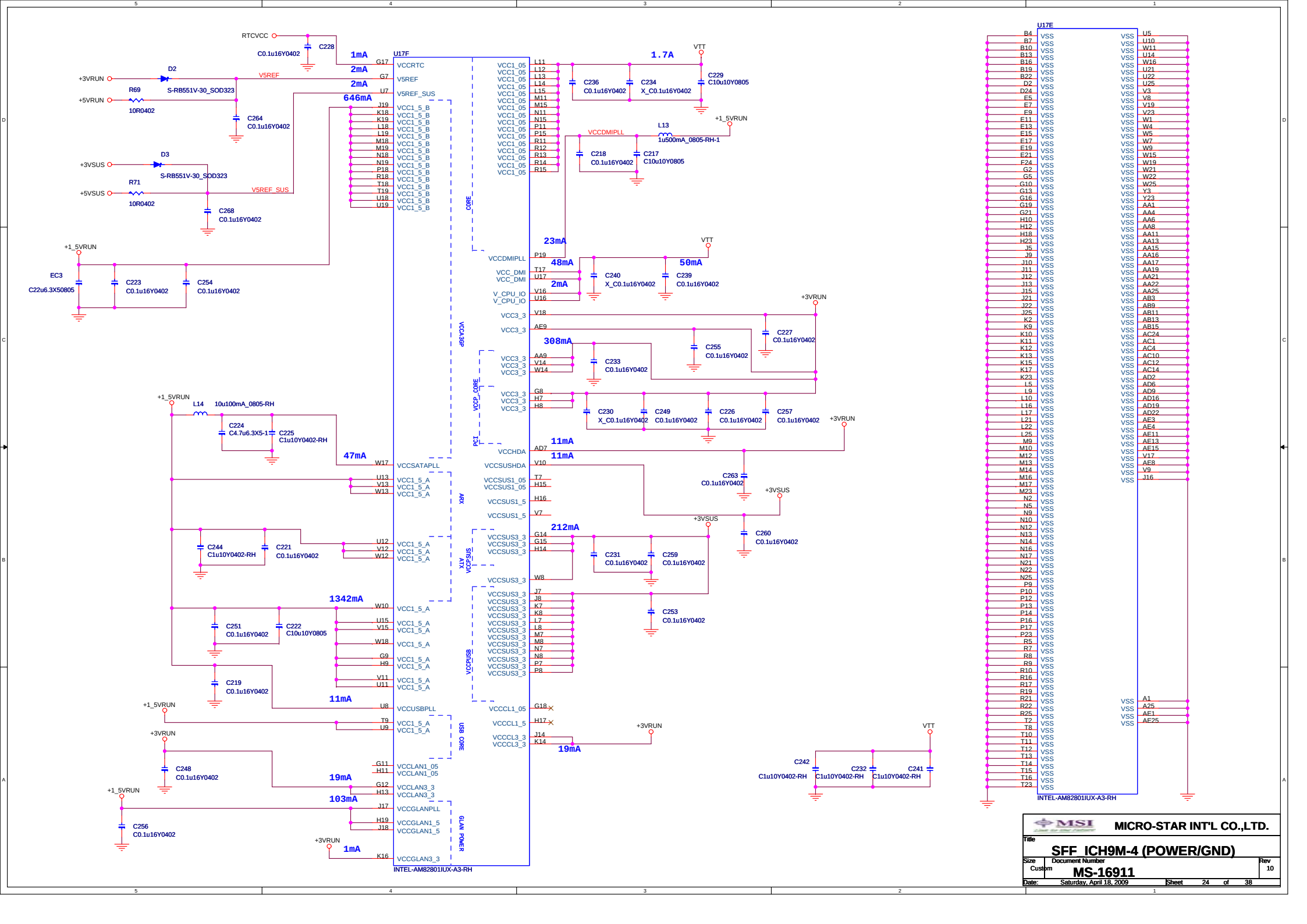
MICRO-STAR INT'L CO.,LTD.

Title: SFF_ICH9M-2 (PCI/USB/PCIE/DMI)

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 22 of 38


+3VSUS
RN24
SMLINK0
SMBALERT#
SMLINK1
SMB_LINK_ALERT#
PM_SYS_RESET
PM_BATLOW#
PM_RI#
PCIE_WAKE#
10P8R-10KR
R207 X_10KR0402 PM_PWRBTN#
+3VRUN
8P4R-10KR0402
RN28
CLK_SATA_OE#
PM_THRM#
SIRQ
P_CLKRUN#
R195 10KR0402
R194 X_100KR0402 SB_GPIO57
R206 100KR0402 DIMPV_PWRGD
U8
(34) VR_PWRGD_CLKEN#
VR_PWRGD_CLKEN
SN74LVC1G04DBV_SOT23-5-RH
RN25
8P4R-2.2K
To DDR-SODIMM, CLK Gen.
Q11
SUS_SMBCLK
SMB_CLK_M2 (12,13,25,27)
N-BSS138LT1G
Q13
SUS_SMBDATA
SMB_DATA_M2 (12,13,25,27)
U17C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP12
GPIO1
GPIO6
GPIO7
GPIO8
GPIO12/LAN_PHY_PWR_CTRL
GPIO13
GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10
INTEL-AM82801IUX-A3-RH
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
R191 10KR0402
SATAGP
CLK_REF_ICH (25)
CLK_USB48 (25)
TP_JNC25
TP8
SLP_S3#_JNC
SLP_S4#_JNC
JNC23
JNC22
X_0402
PM_SLP_S3# (28)
PM_SLP_S4# (28)
DIMPV_PWRGD
PM_DPRSLPVR (7,34)
PM_BATLOW#
PM_PWRBTN# (28)
SB_LAN_RST#
R181 10KR0402
RSMRST# (28)
CLK_PWRGD (25)
DIMPV_PWRGD
CL_CLK0 (7)
CL_DATA0 (7)
CL_VREF0_ICH
CL_RST#0 (7)
(7) PM_SYNC#
(25) PM_STP_PCI#
(25) PM_STP_CPU#
(27) PCIE_WAKE#
(28) SIRQ
PM_THRM#
100KR0402
R66
VR_PWRGD_CLKEN
(28) KBSMI#
(28) KBSCI#
CLK_SATA_OE#
MB_ID0
SB_GPIO57
(26) SPKR
(7) MCH_SYNC#
P_CLKRUN#
W/S
10/10 mil
R64
3.24KR1%0402
CL_VREF0_ICH
R65
453R1%0402-RH-1
C220
C0.1u16Y0402
IF PWROK from CPU PWM controller:
Del U4 and R124
IF PWROK from EC:
Del U4 and R43 mount R124, R177
IF PWROK from HW delay:
Mount U4, Del R124, R43, R177
PM_SLP_S3#
D5
X_S-BAS40WS_SOD323-RH
(28,34) IMVP_PWRGD
C322 X_C0.1u16Y0402
U11A
U11B
X_NC7WZ14P6X_SC70
DIMPV_PWRGD
DIMPV_PWRGD (7)
C334
X_C0.1u16Y0402
JNC35
X_0402
MB_ID0 R192 X_100KR0402
MB_ID0 R193 100KR0402
MSI
MICRO-STAR INT'L CO.,LTD.
Title
SFF_ICH9M-3 (SM BUS/GPIO)
Size Custom
Document Number MS-16911
Rev 10
Date: Saturday, April 18, 2009
Sheet 23 of 38



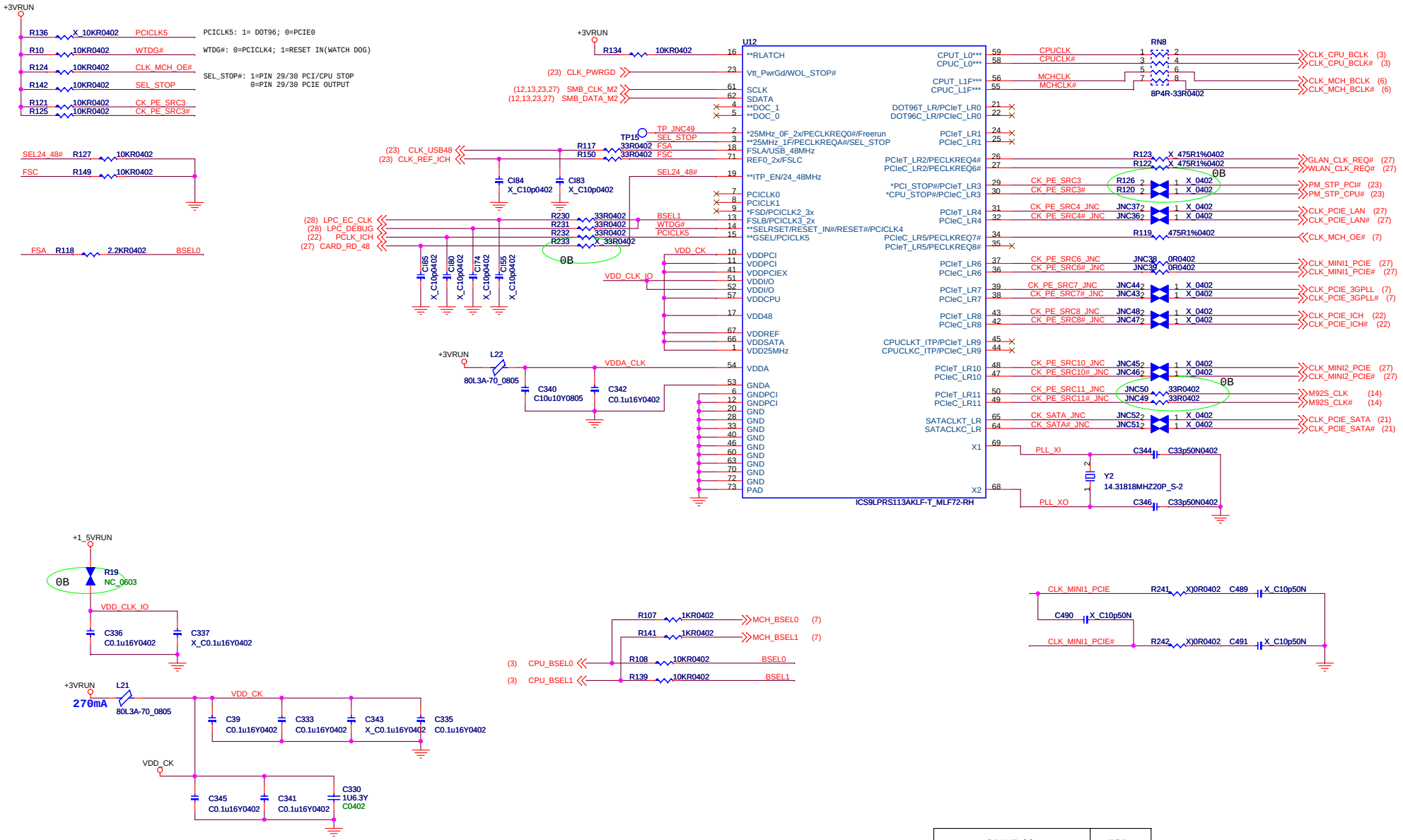
MICRO-STAR INT'L CO.,LTD.

Title: SFF_ICH9M-4 (POWER/GND)

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 24 of 38

CLK STRAP PIN



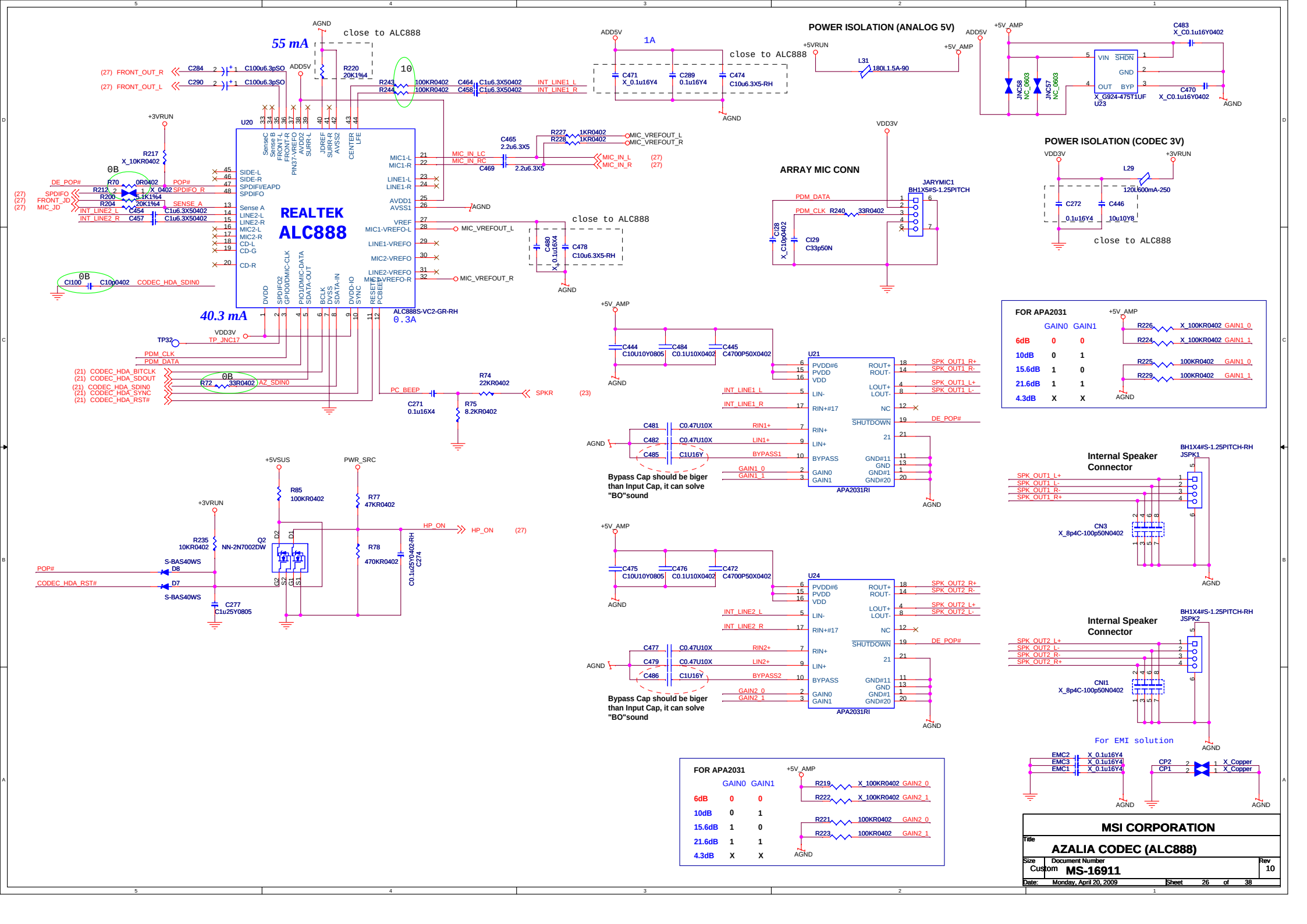
CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz
L	L	L	1066 MHz

MICRO-STAR INT'L CO.,LTD.

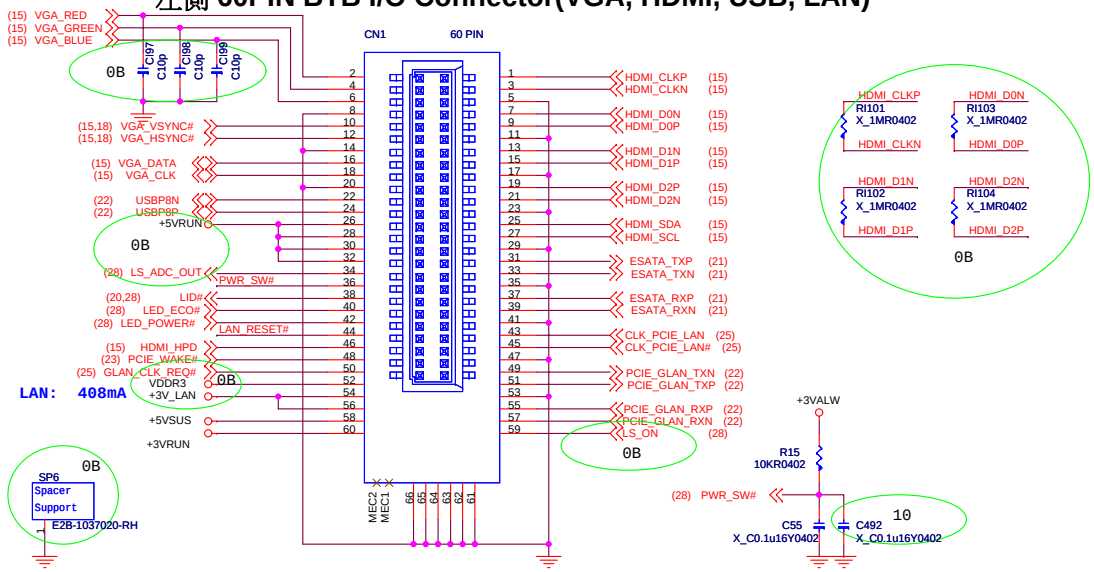
Title: CLOCK GEN (ICS9LPRS113A)

Size: Custom | Document Number: MS-16911 | Rev: 10

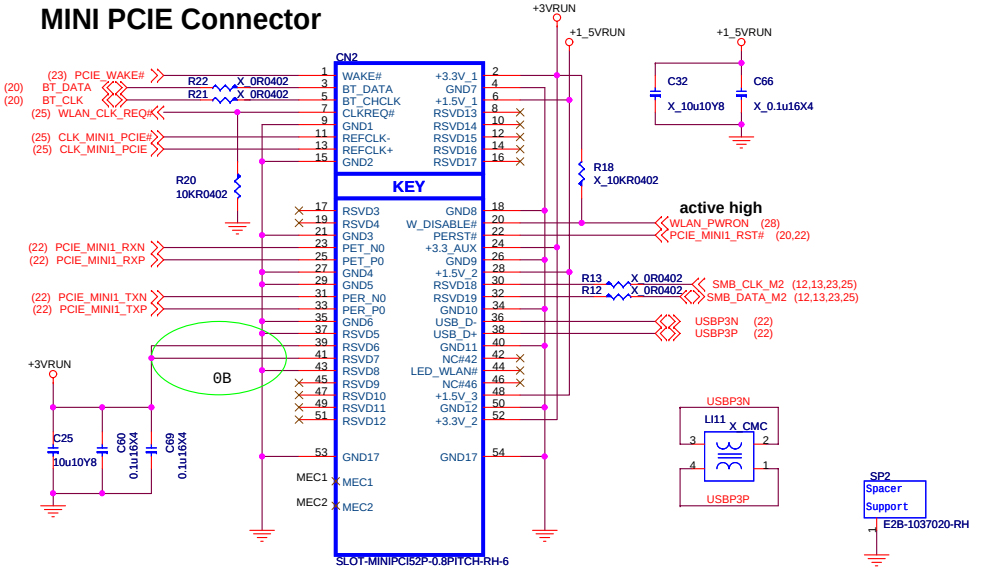
Date: Saturday, April 18, 2009 | Sheet 25 of 38


55 mA
close to ALC888
REALTEK
ALC888
ALC888S-VC2-GR-RH
0.3A
40.3 mA
POWER ISOLATION (ANALOG 5V)
POWER ISOLATION (CODEC 3V)
ARRAY MIC CONN
JARYMIC1
BH1X5#S-1.25PITCH
APA2031RI
Bypass Cap should be biger than Input Cap, it can solve "BO"sound
FOR APA2031
GAIN0 GAIN1
6dB 0 0
10dB 0 1
15.6dB 1 0
21.6dB 1 1
4.3dB X X
Internal Speaker Connector
BH1X4#S-1.25PITCH-RH
JSPK1
JSPK2
CN3
CNI1
For EMI solution
MSI CORPORATION
AZALIA CODEC (ALC888)
Custom
MS-16911
Rev 10
Monday, April 20, 2009
Sheet 26 of 38

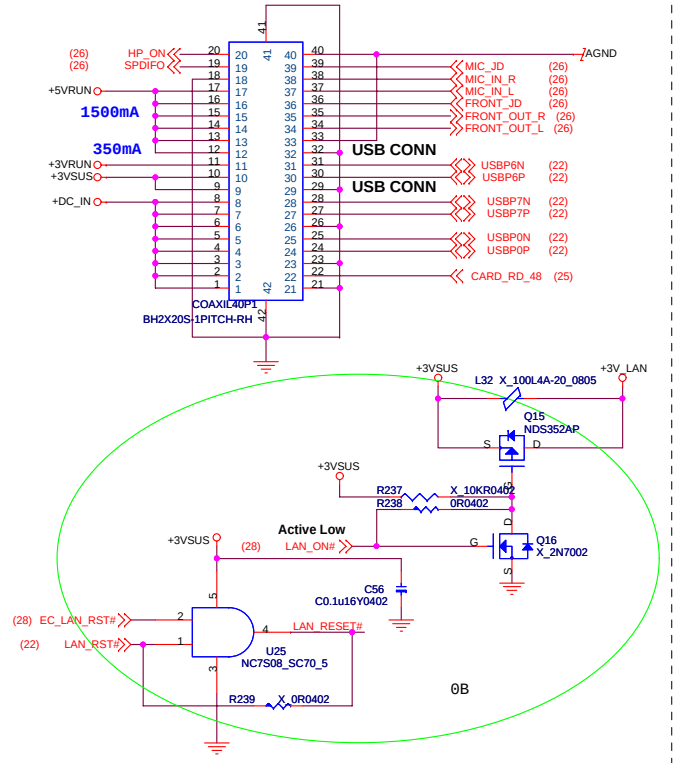
左側 60PIN BTB I/O Connector(VGA, HDMI, USB, LAN)

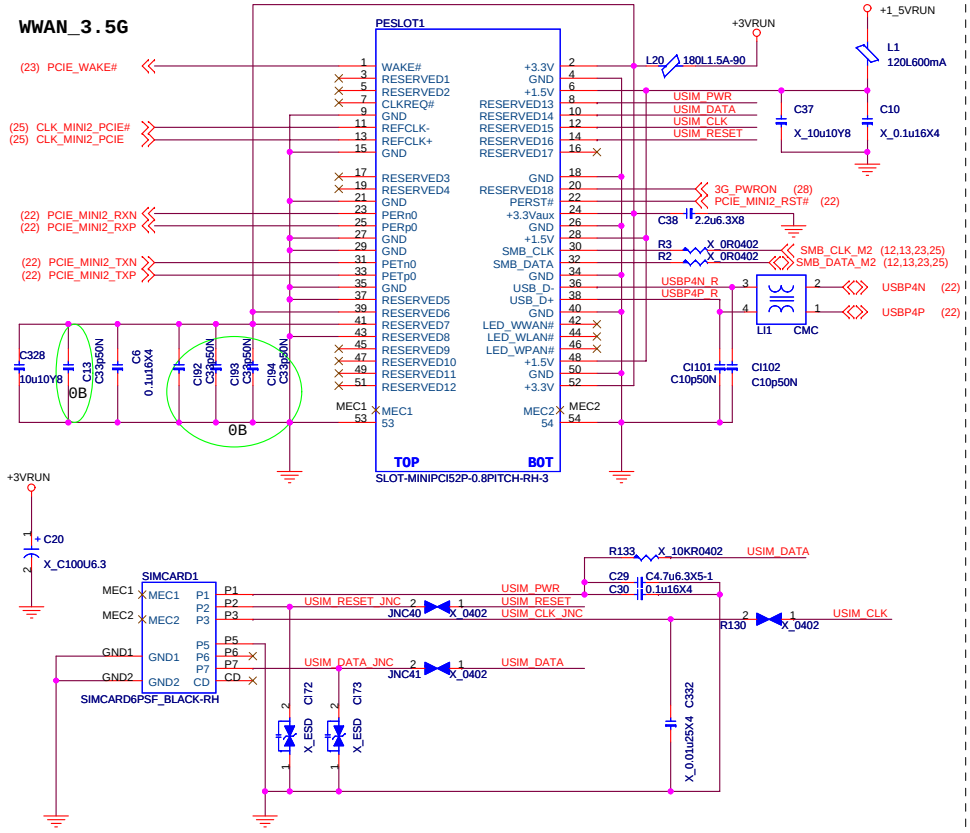


MINI PCIE Connector

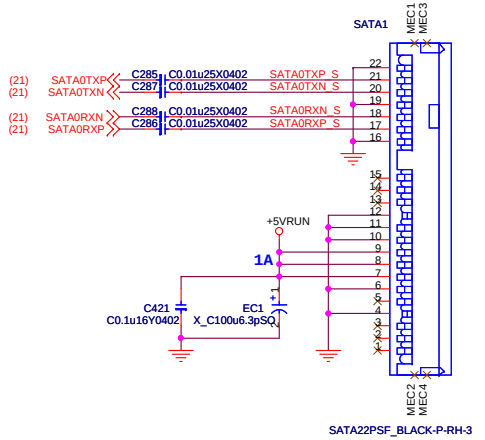


右側 40PIN I/O Connector
(AC IN, USB x 2, MIC, Earphone, Cardreader)

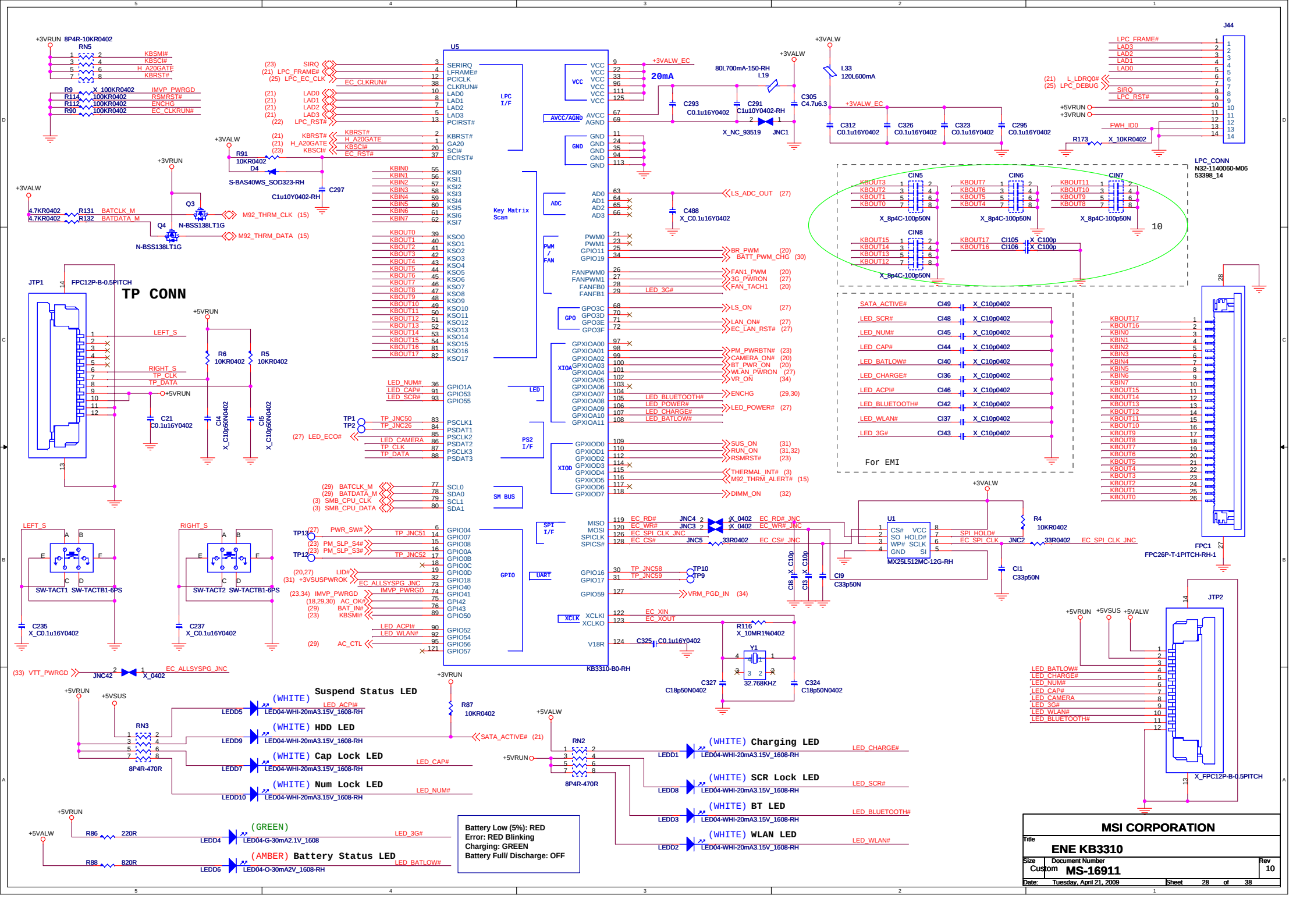


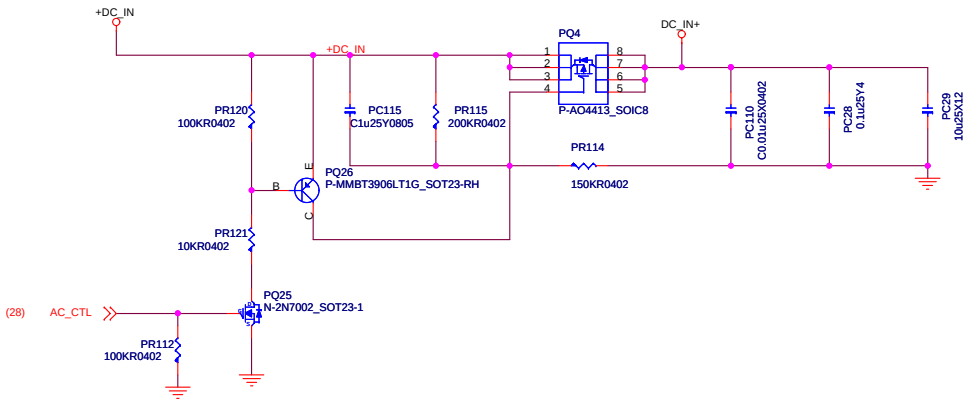


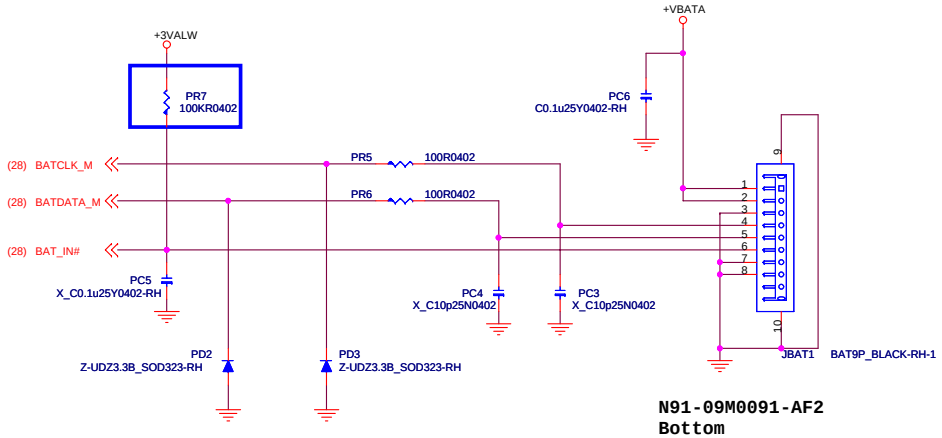
SATA HDD Connector



MSI CORPORATION		
Title: HDD, CON,MINI_PCIE		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Tuesday, April 21, 2009	Sheet 27 of 38	


TP CONN
U5
KB3310-B0-RH
Key Matrix Scan
Suspend Status LED
(WHITE) HDD LED
(WHITE) Cap Lock LED
(WHITE) Num Lock LED
(WHITE) Charging LED
(WHITE) SCR Lock LED
(WHITE) BT LED
(WHITE) WLAN LED
(GREEN)
(AMBER) Battery Status LED
Battery Low (5%): RED
Error: RED Blinking
Charging: GREEN
Battery Full/ Discharge: OFF
For EMI
MSI CORPORATION
ENE KB3310
MS-16911
Tuesday, April 21, 2009

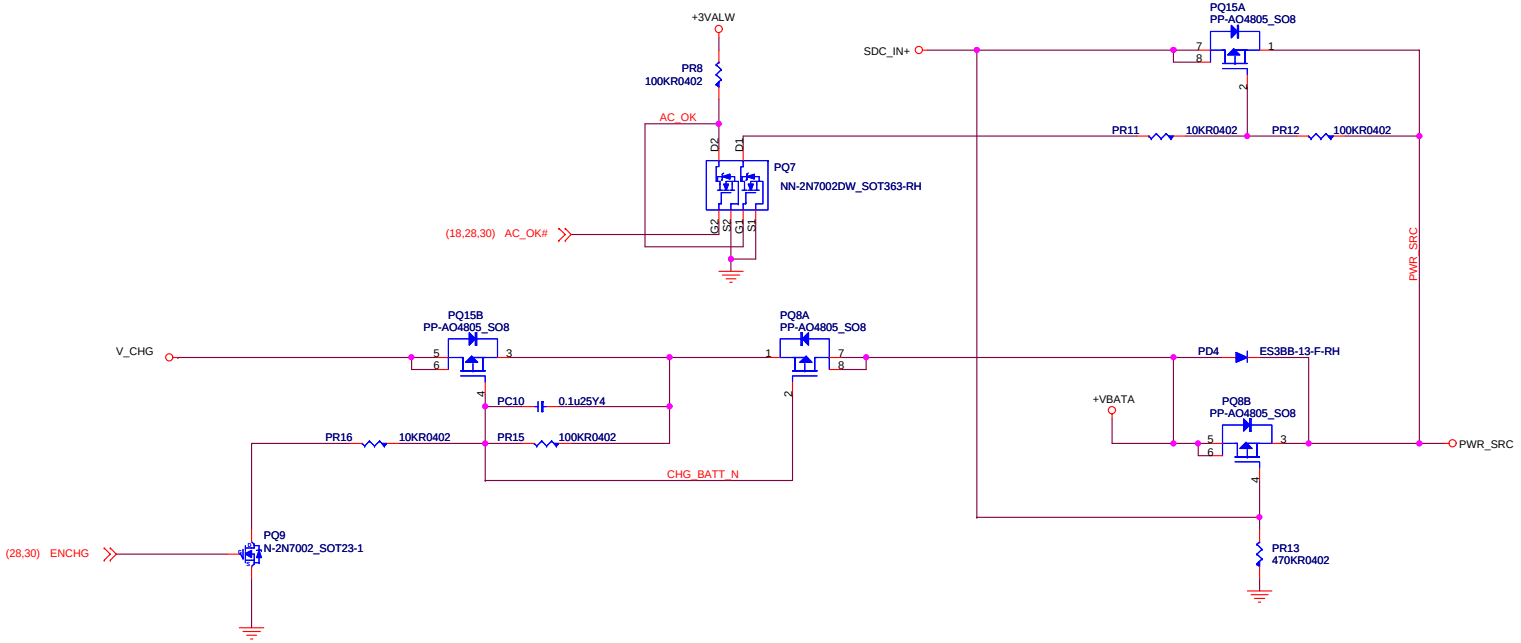




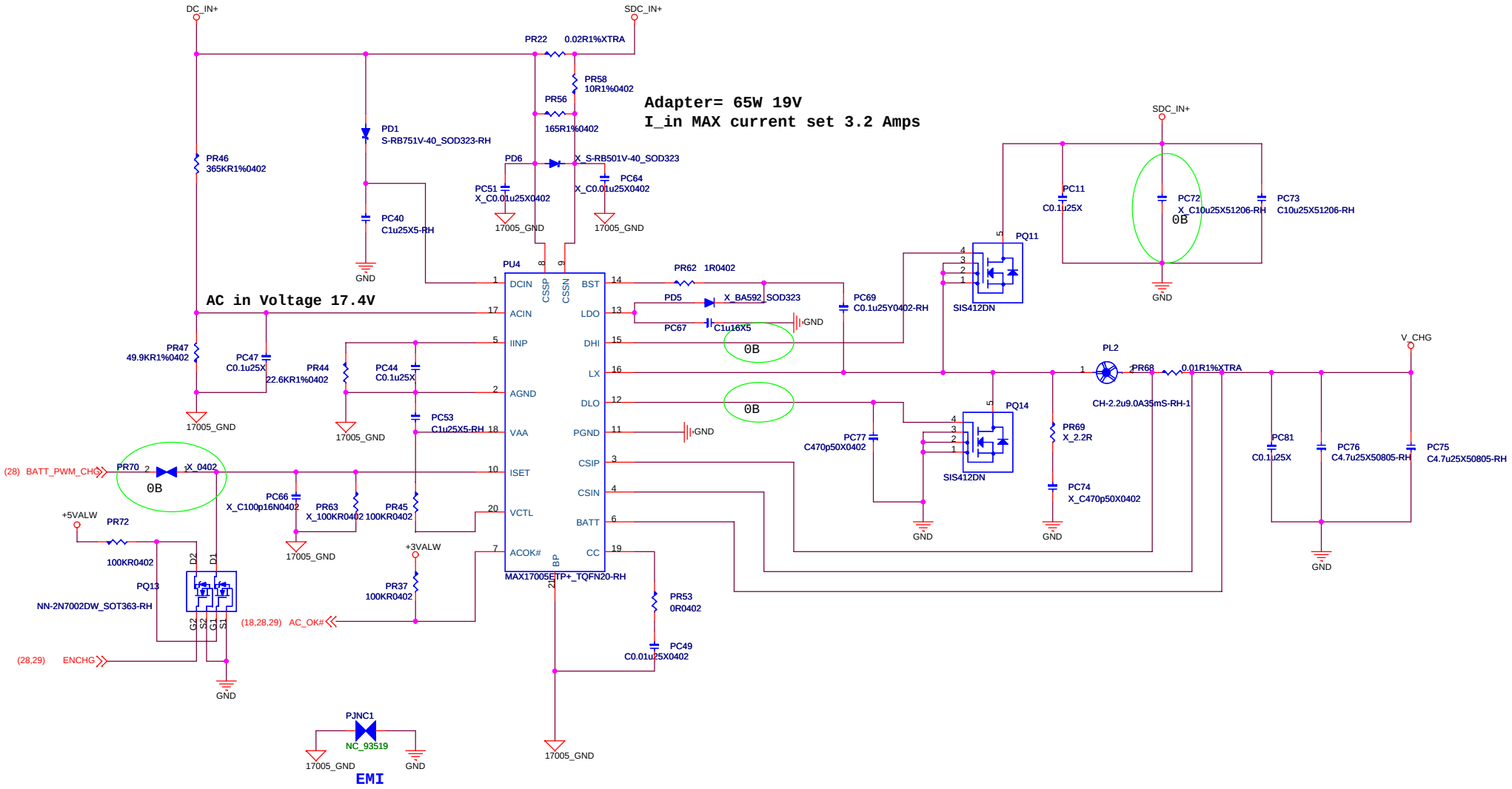
N91-09M0091-AF2
Bottom

JBAT1 Pin Definition

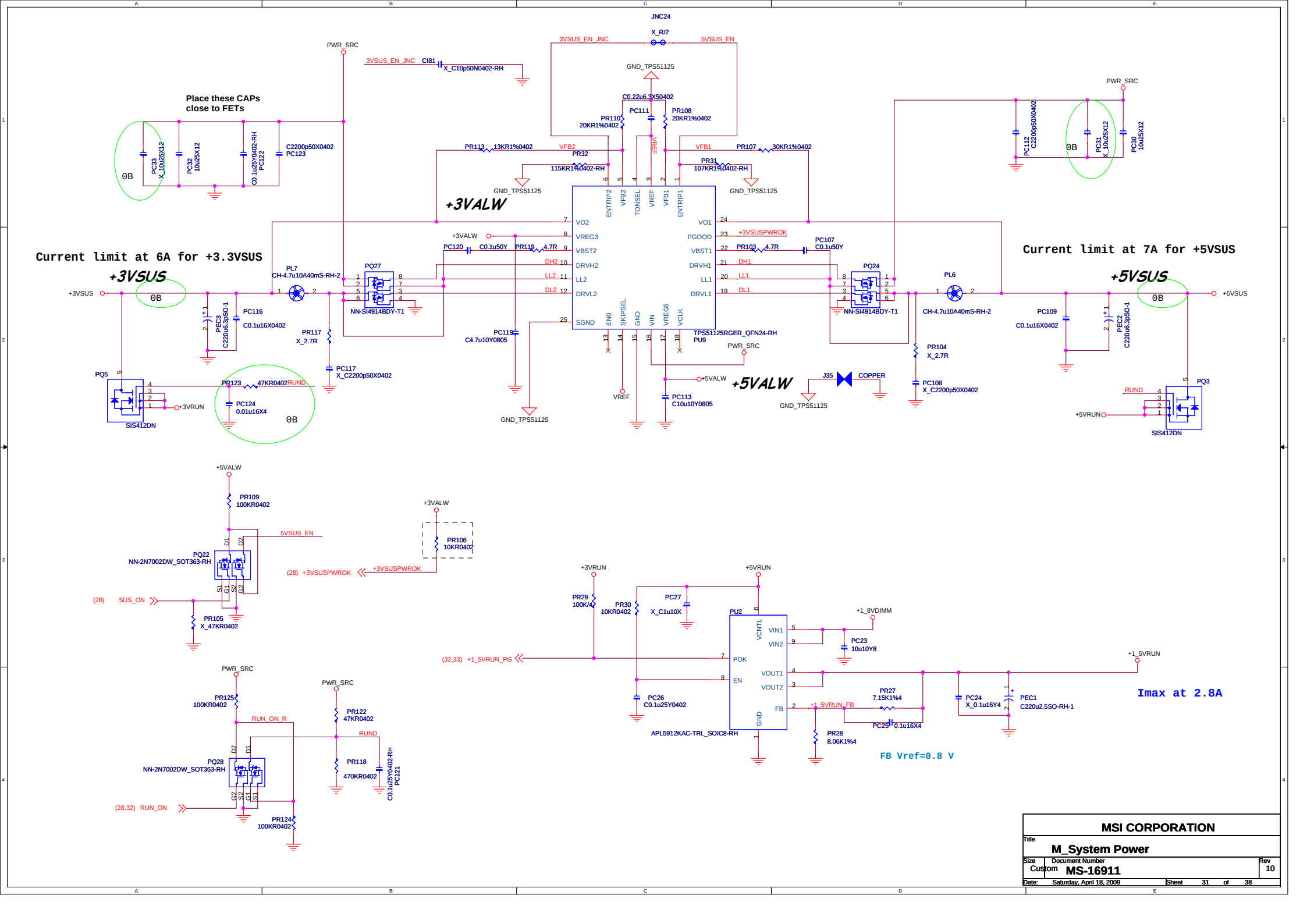
1: VBATA+
2: VBATA+
3: SYSTEM_CONTROL
4: SMBCLK
5: SMBDATA
6: BAT_IN#
7: GND
8: GND

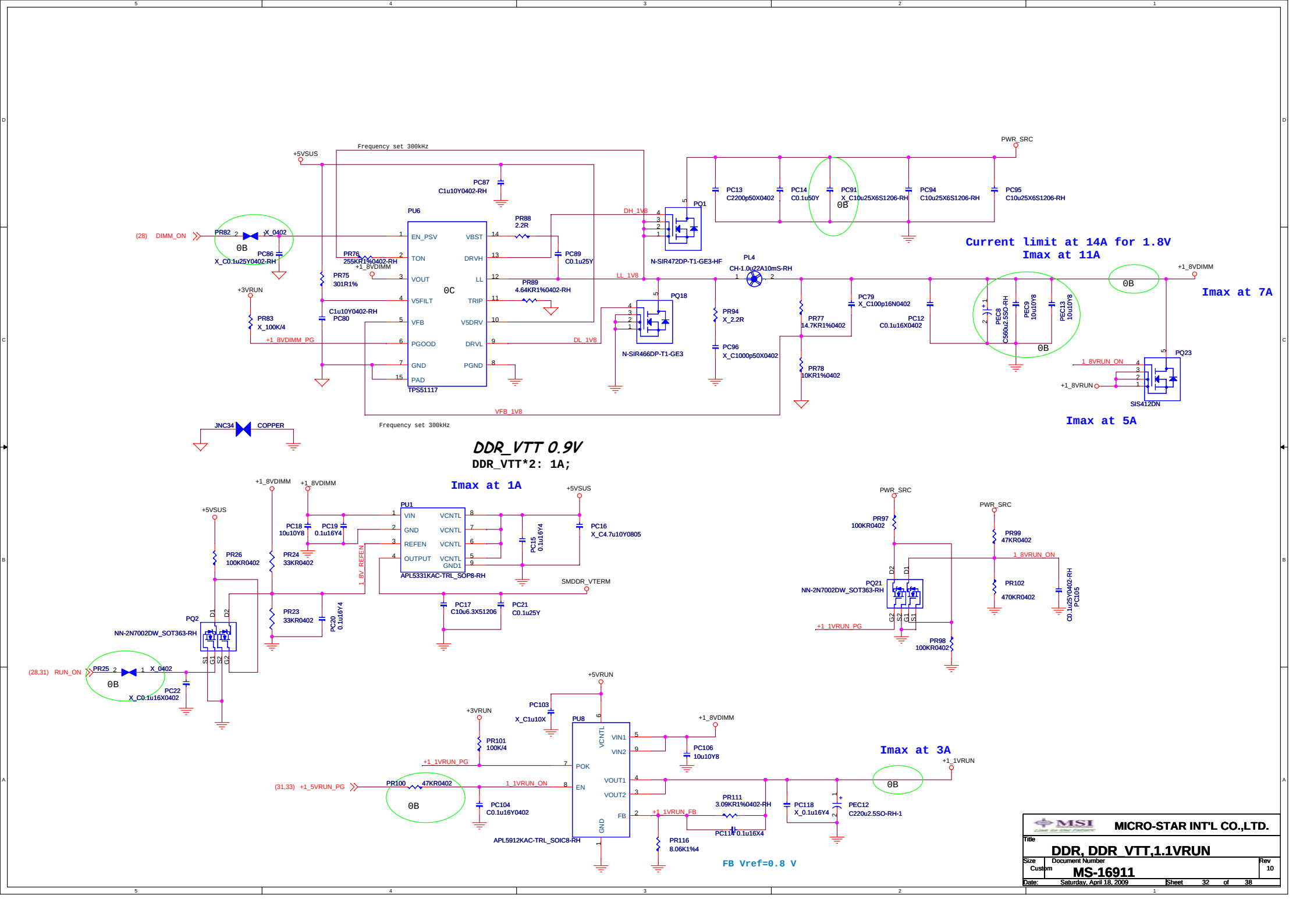


MSI CORPORATION		
Title: M_Battery Select		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 29 of 38	

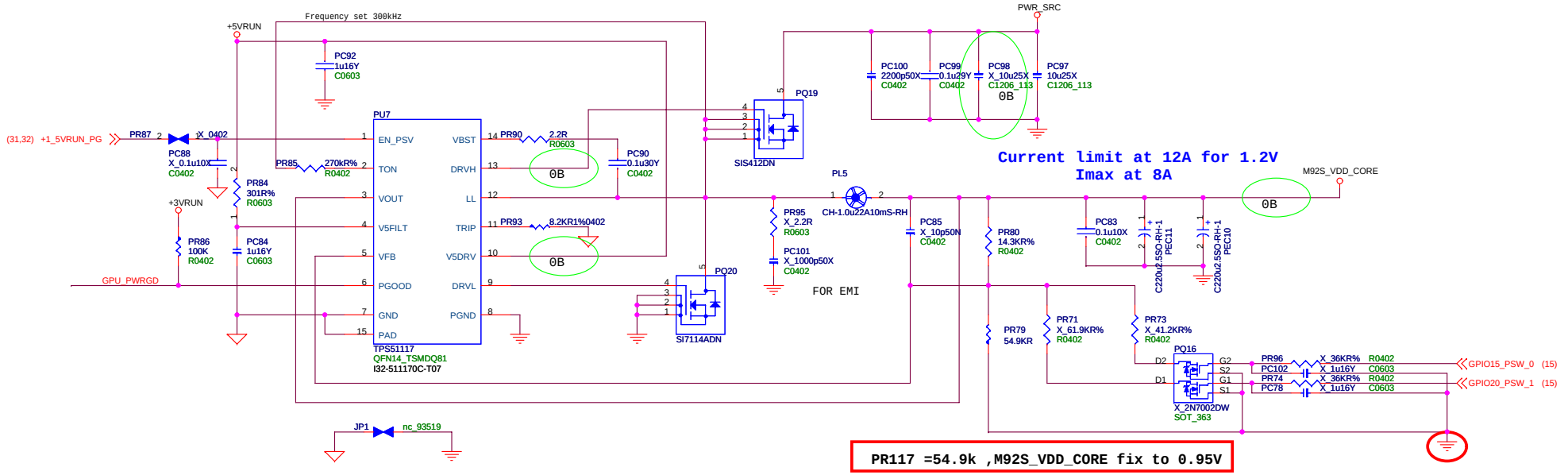


MSI CORPORATION	
Title	M_Battery Charger
Size	A3
Document Number	MS-16911
Rev	10
Date:	Saturday, April 18, 2009
Sheet	30 of 38


Place these CAPs close to FETs
Current limit at 6A for +3.3VSUS
Current limit at 7A for +5VSUS
+3VALW
+5VALW
+3VSUS
+5VSUS
+5VRUN
+3VRUN
TPS51125RGER_QFN24-RH
PU9
APL5912KAC-TRL_SOIC8-RH
PU2
NN-SI4914BDY-T1
NN-2N7002DW_SOT363-RH
SIS412DN
CH-4.7u10A40mS-RH-2
Imax at 2.8A
FB Vref=0.8 V
MSI CORPORATION
M_System Power
MS-16911
Saturday, April 18, 2009

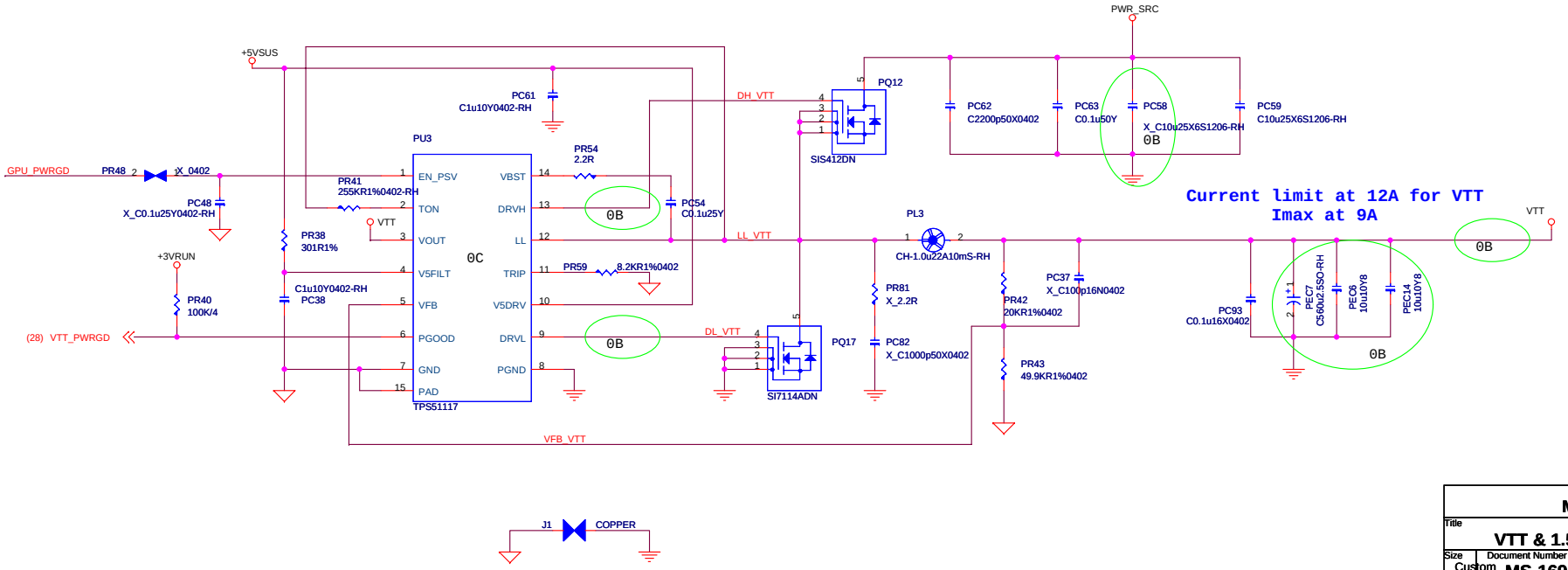


MSI	MICRO-STAR INT'L CO.,LTD.	
Title	DDR, DDR_VTT,1.1VRUN	
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 32 of 38	

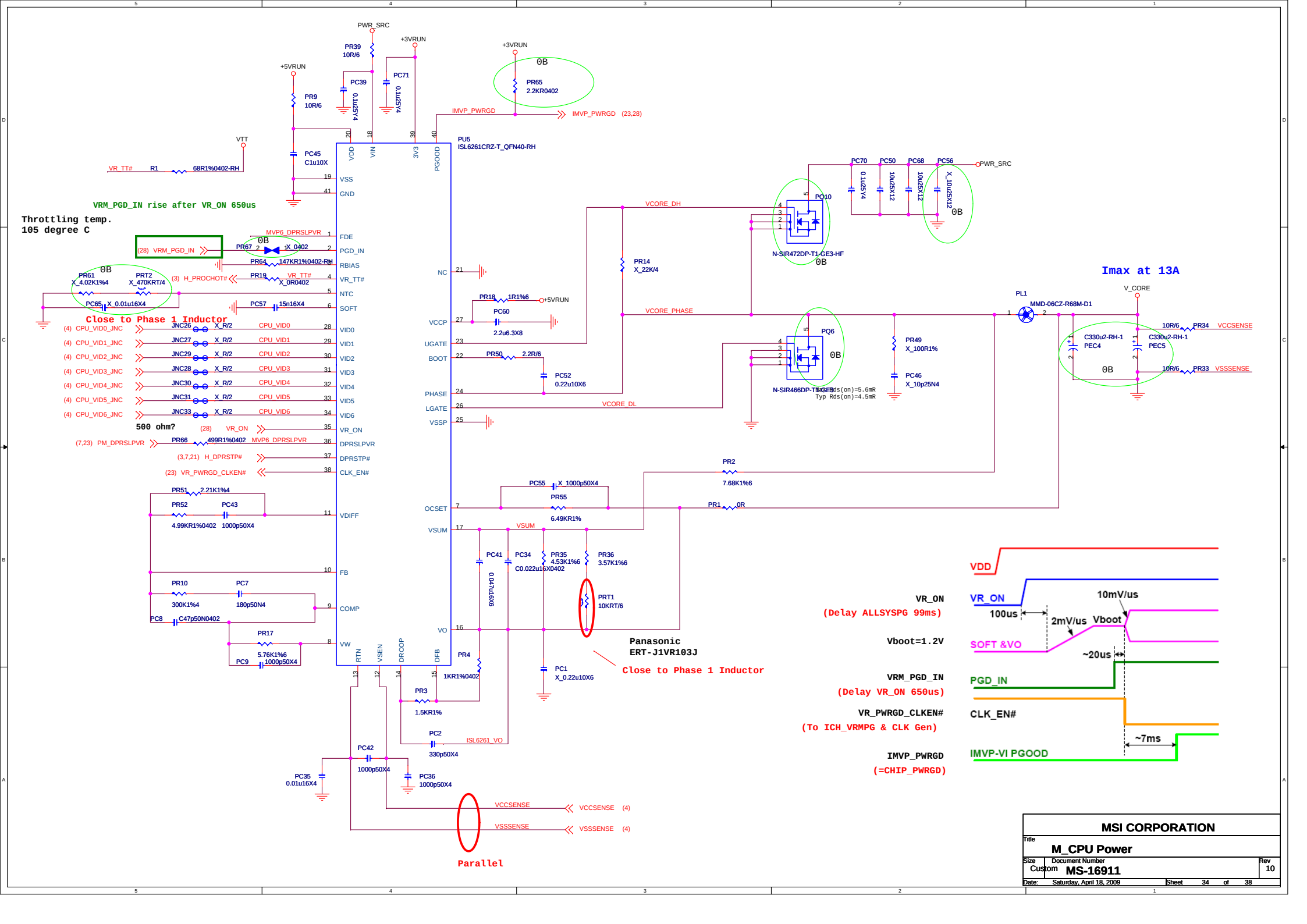


PR117 =54.9k ,M92S_VDD_CORE fix to 0.95V

PR117 change to 53.6k		
PSW_0	PSW_1	
1	0	1.2V
0	1	1.1V
0	0	0.95V



MSI CORPORATION	
Title: VTT & 1.5VRUN	
Size: Custom	Document Number: MS-16911
Rev: 10	
Date: Saturday, April 18, 2009	Sheet 33 of 38


PWR_SRC
+3VRUN
+5VRUN
PR39 10R/6
PC39 0.1u25V4
PC71 0.1u25V4
PR9 10R/6
PR65 2.2KR0402
0B
IMVP_PWRGD
IMVP_PWRGD (23,28)
VTT
VR_TT# R1 68R1%0402-RH
PC45 C1u10X
PU5 ISL6261CRZ-T_QFN40-RH
VDD
VIN
3V3
PGOOD
VSS
GND
VRM_PGD_IN rise after VR_ON 650us
Throttling temp.
105 degree C
(28) VRM_PGD_IN
PR67 X_0402
MVP6_DPRSLPVR
PR64 147KR1%0402-RH
PR61 X_4.02K1%4
PRT2 X_470KRT/4
(3) H_PROCHOT#
PR19 X_0R0402
VR_TT#
PC65 X_0.01u16X4
PC57 15n16X4
Close to Phase 1 Inductor
FDE
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
(4) CPU_VID0_JNC
(4) CPU_VID1_JNC
(4) CPU_VID2_JNC
(4) CPU_VID3_JNC
(4) CPU_VID4_JNC
(4) CPU_VID5_JNC
(4) CPU_VID6_JNC
JNC26 X_R/2 CPU_VID0
JNC27 X_R/2 CPU_VID1
JNC29 X_R/2 CPU_VID2
JNC28 X_R/2 CPU_VID3
JNC30 X_R/2 CPU_VID4
JNC31 X_R/2 CPU_VID5
JNC33 X_R/2 CPU_VID6
VID0
VID1
VID2
VID3
VID4
VID5
VID6
500 ohm?
(28) VR_ON
VR_ON
(7,23) PM_DPRSLPVR
PR66 499R1%0402 MVP6_DPRSLPVR
DPRSLPVR
(3,7,21) H_DPRSTP#
DPRSTP#
(23) VR_PWRGD_CLKEN#
CLK_EN#
PR51 2.21K1%4
PR52 4.99KR1%0402
PC43 1000p50X4
VDIFF
FB
PR10 300K1%4
PC7 180p50N4
PC8 C47p50N0402
COMP
PR17 5.76K1%6
PC9 1000p50X4
VW
RTN
VSEN
DROOP
DFB
NC
VCCP
UGATE
BOOT
PHASE
LGATE
VSSP
PR18 1R1%6
+5VRUN
PC60 2.2u6.3X8
PR50 2.2R/6
PC52 0.22u10X6
VCORE_DH
VCORE_PHASE
VCORE_DL
PR14 X_22K/4
PC70 0.1u25V4
PC50 10u25X12
PC68 10u25X12
PC56 X_10u25X12
PWR_SRC
PQ10
N-SIR472DP-T1-GE3-HF
PQ6
N-SIR466DP-T1-GE3
Typ Rds(on)=5.6mR
Typ Rds(on)=4.5mR
PR49 X_100R1%
PC46 X_10p25N4
Imax at 13A
PL1
MMD-06CZ-R68M-D1
V_CORE
C330u2-RH-1 PEC4
C330u2-RH-1 PEC5
10R/6 PR34 VCCSENSE
10R/6 PR33 VSSSENSE
PR2 7.68K1%6
PR1 0R
PC55 X_1000p50X4
PR55 6.49KR1%
OCSET
VSUM
PC41 0.047u16X6
PC34 C0.022u16X0402
PR35 4.53K1%6
PR36 3.57K1%6
PRT1 10KRT/6
VO
PR4 1KR1%0402
PR3 1.5KR1%
PC1 X_0.22u10X6
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
PC2 330p50X4
ISL6261_VO
PC42 1000p50X4
PC35 0.01u16X4
PC36 1000p50X4
VCCSENSE
VCCSENSE (4)
VSSSENSE
VSSSENSE (4)
Parallel
VR_ON
(Delay ALLSYSPG 99ms)
Vboot=1.2V
VRM_PGD_IN
(Delay VR_ON 650us)
VR_PWRGD_CLKEN#
(To ICH_VRMPG & CLK Gen)
IMVP_PWRGD
(=CHIP_PWRGD)
VDD
VR_ON
100us
10mV/us
2mV/us
Vboot
SOFT &VO
~20us
PGD_IN
CLK_EN#
~7ms
IMVP-VI PGOOD
MSI CORPORATION
Title
M_CPU Power
Size
Custom
Document Number
MS-16911
Rev
10
Date: Saturday, April 18, 2009
Sheet 34 of 38

PCB1
PCB
PCB_V0A

UME1
BIOS LABEL
X_BIOS_LABEL

P30-169110A-D05,昆嶺,
P30-169110A-H73,瀚宇博德

SP1 Spacer Support — E2B-1634020-RH
SP3 Spacer Support — X_E2B-1634020-RH
SP5 Spacer Support — X_E2B-1634020-RH
SP4 Spacer Support — E2B-1634020-RH

thermal stand off

FM3 X_F_PAD_M120
FM6 X_F_PAD_M100
FM7 X_F_PAD_M100
FM8 X_F_PAD_M100
FM4 X_F_PAD_M120
FM5 X_F_PAD_M120

holes_S295d110_P MH2 X_S7.5D2.8
holes_S295d110_P MH7 X_S7.5D2.8
holes_S295d110_P MH11 X_S7.5D2.8
holes_S295d110_P MH8 X_S7.5D2.8
holes_S295d110_P MH4 X_S7.5D2.8
holes_S295d110_P MH10 X_S7.5D2.8
AGND
holes_S295d110_P MH3 X_S7.5D2.8

NPTH118 MH1 X_S7.5D2.8
NPTH118 MH9 X_S7.5D2.8

MYLAR1 Hexscrew MYLAR E26-1022220-Y42
MYLAR2 Hexscrew MYLAR E26-1022220-Y42
MYLAR3 Hexscrew MYLAR E2P-6910811-Y42
MYLAR4 Hexscrew MYLAR E2P-6910811-Y42
MYLAR5 Hexscrew MYLAR E2P-6910711-Y42

0B

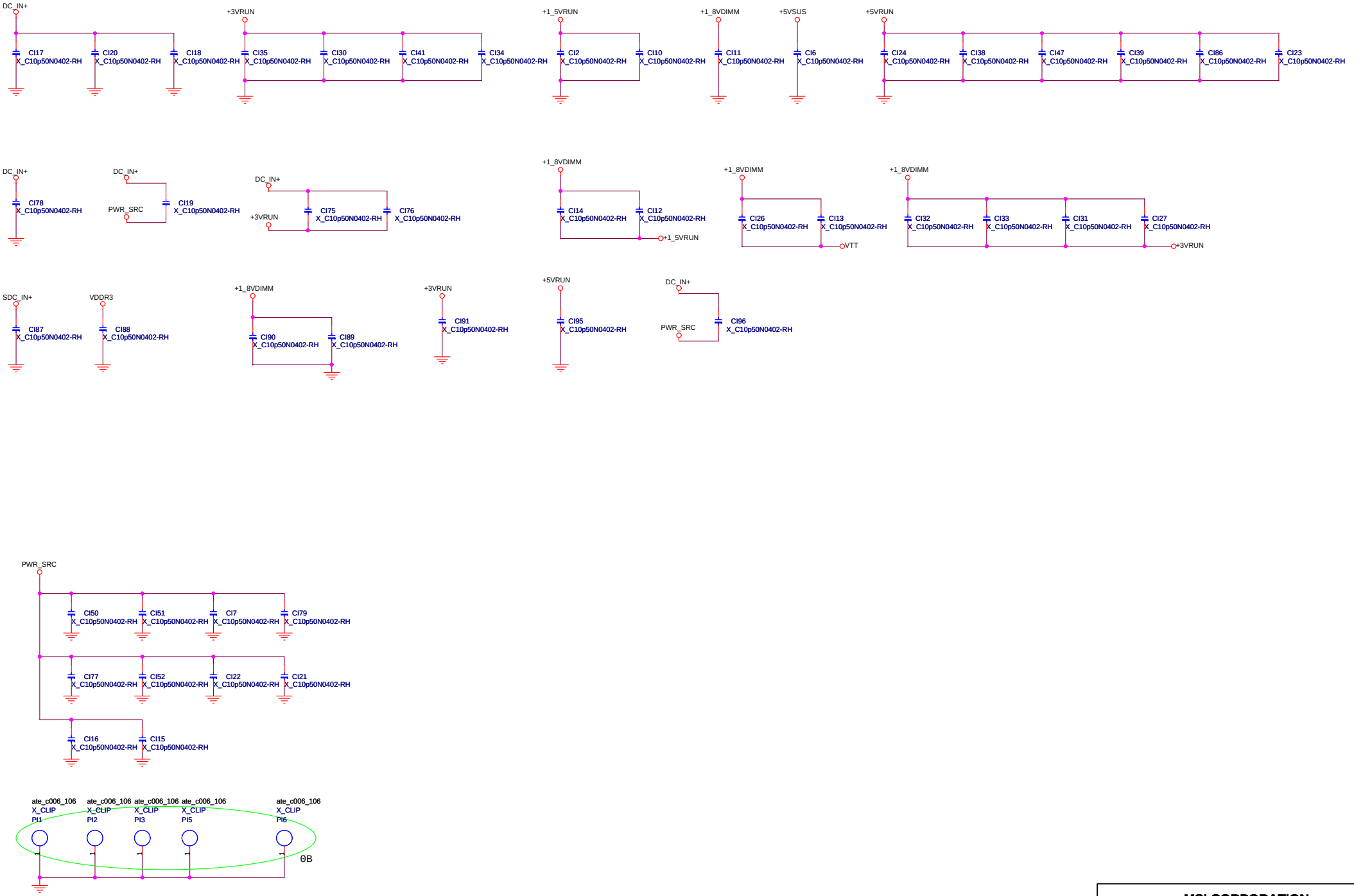
J17 L1_10mil_35_Ohm X_H1X2_black-RH	J15 L3_7.5mil_35_Ohm X_H1X2_black-RH	J25 L6_10mil_35_Ohm X_H1X2_black-RH		35 OHM
J7 L1_8mil_40_Ohm X_H1X2_black-RH	J5 L4_5.5mil_40_Ohm X_H1X2_black-RH	J22 L6_8mil_40_Ohm X_H1X2_black-RH 0B		40 OHM
J11 L1_6mil_45_Ohm X_H1X2_black-RH	J4 L3_5mil_45_Ohm X_H1X2_black-RH	J3 L4_5mil_45_Ohm X_H1X2_black-RH	J2 L6_6mil_45_Ohm X_H1X2_black-RH	45 OHM
J39 L1_5mil_50_Ohm X_H1X2_black-RH	J38 L6_5mil_50_Ohm X_H1X2_black-RH	J36 L3_3.5mil_50_Ohm X_H1X2_black-RH	J6 L4_3.5mil_50_Ohm X_H1X2_black-RH	50 OHM
		J10 L1_4mil_55_Ohm X_H1X2_black-RH	J13 L6_4mil_55_Ohm X_H1X2_black-RH	55 OHM
J19 L1_DIFF_4/5/4_95_Ohm+ X_H1X2_black-RH J29 L1_DIFF_4/5/4_95_Ohm- X_H1X2_black-RH	J21 L3_DIFF_3.5/8/3.5_95_Ohm+ X_H1X2_black-RH J31 L3_DIFF_3.5/8/3.5_95_Ohm- X_H1X2_black-RH	J24 L4_DIFF_3.5/8/3.5_95_Ohm+ X_H1X2_black-RH J33 L4_DIFF_3.5/8/3.5_95_Ohm- X_H1X2_black-RH	J27 L6_DIFF_4/5/4_95_Ohm+ X_H1X2_black-RH J34 L6_DIFF_4/5/4_95_Ohm- X_H1X2_black-RH	DIFF_95 OHM
J30 L1_DIFF_5/6.5/5/_90_Ohm+ X_H1X2_black-RH J23 L1_DIFF_5/6.5/5/_90_Ohm- X_H1X2_black-RH	J28 L3_DIFF_4/8/4_90_Ohm+ X_H1X2_black-RH J20 L3_DIFF_4/8/4_90_Ohm- X_H1X2_black-RH	J26 L4_DIFF_4/8/4_90_Ohm+ X_H1X2_black-RH J16 L4_DIFF_4/8/4_90_Ohm- X_H1X2_black-RH	J18 L6_DIFF_5/6.5/5/_90_Ohm+ X_H1X2_black-RH J32 L6_DIFF_5/6.5/5/_90_Ohm- X_H1X2_black-RH	DIFF_90 OHM
J9 L1_DIFF_7/5/7_75_Ohm+ X_H1X2_black-RH J8 L1_DIFF_7/5/7_75_Ohm- X_H1X2_black-RH	J12 L3_DIFF_5.5/7/5.5_75_Ohm+ X_H1X2_black-RH J14 L3_DIFF_5.5/7/5.5_75_Ohm- X_H1X2_black-RH	J42 L4_DIFF_5.5/7/5.5_75_Ohm+ X_H1X2_black-RH J43 L4_DIFF_5.5/7/5.5_75_Ohm- X_H1X2_black-RH	J40 L6_DIFF_7/5/7_75_Ohm+ X_H1X2_black-RH J41 L6_DIFF_7/5/7_75_Ohm- X_H1X2_black-RH	DIFF_75 OHM

MSI CORPORATION

Title: Non_Footprint for BOM

Size: Custom | Document Number: MS-16911 | Rev: 10

Date: Saturday, April 18, 2009 | Sheet 35 of 38

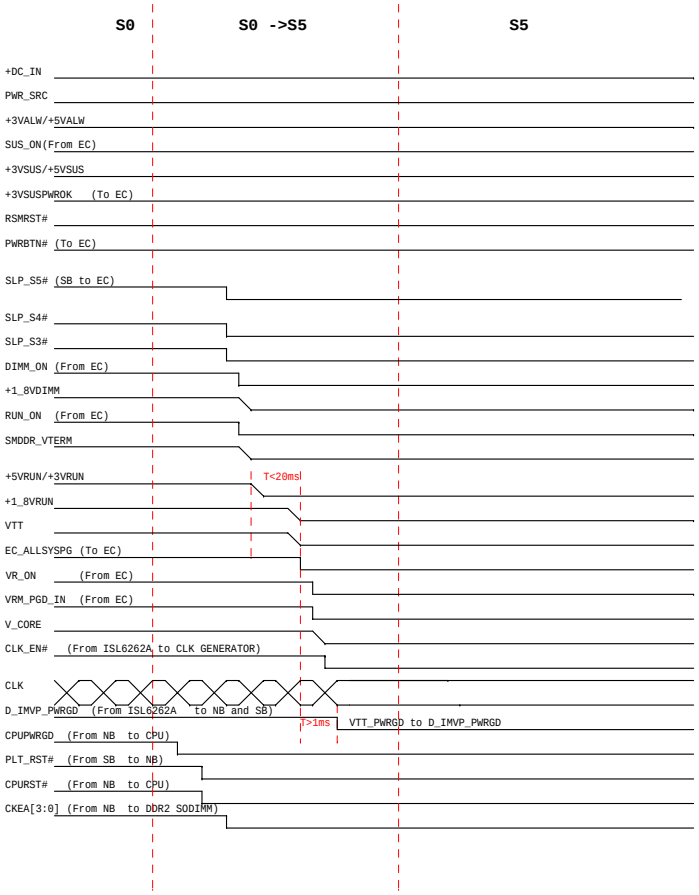


MSI CORPORATION		
Title: EMI		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Wednesday, April 22, 2009	Sheet 36 of 38	

AC S0-S5

EC programming timing

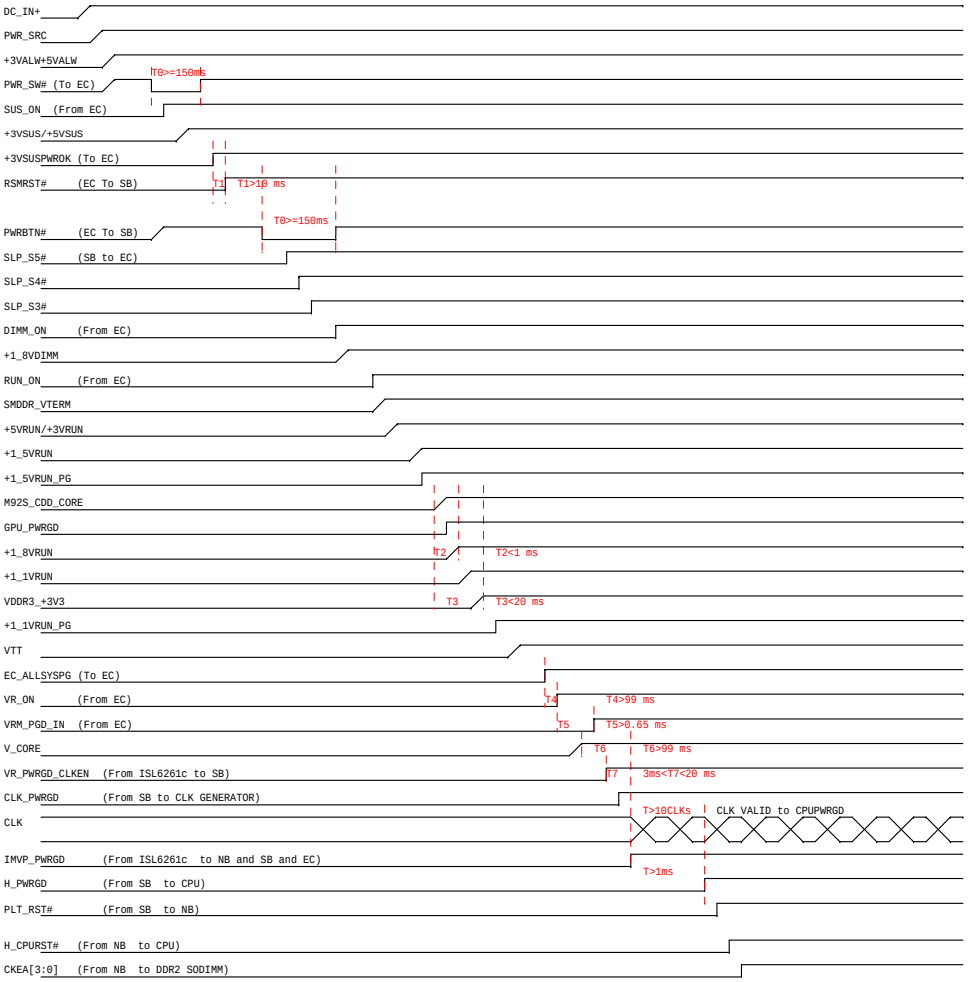
INTEL CANTIGA+ICH9M timing SPEC



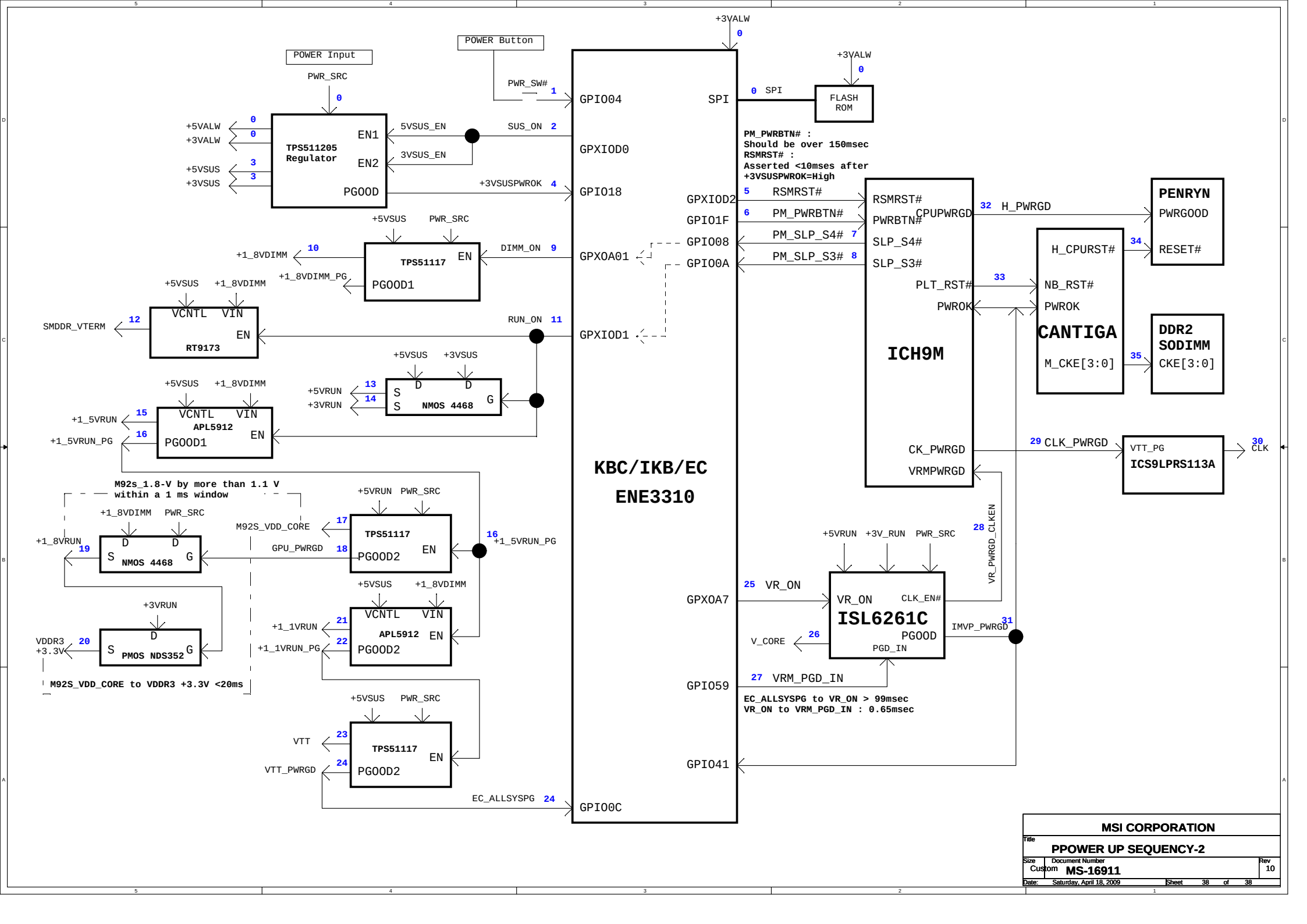
AC S5-S0

EC programming timing

INTEL CANTIGA+ICH9M timing SPEC



MSI CORPORATION		
Title: POWER UP SEQUENCY-1		
Size: Custom	Document Number: MS-16911	Rev: 10
Date: Saturday, April 18, 2009	Sheet 37 of 38	


POWER Input
PWR_SRC
POWER Button
PWR_SW#
+3VALW
SPI
FLASH ROM
TPS511205 Regulator
EN1
EN2
PGOOD
5VSUS_EN
3VSUS_EN
SUS_ON
+3VSUSPWROK
+5VALW
+3VALW
+5VSUS
+3VSUS
GPIO04
GPXIOD0
GPIO18
GPXIOD1
GPIO08
GPIO0A
GPIO1F
GPXIOD2
GPXOA01
GPXOA7
GPIO059
GPIO041
GPIO0C
KBC/IKB/EC
ENE3310
PM_PWRBTN# :
Should be over 150msec
RSMRST# :
Asserted <10mses after
+3VSUSPWROK=High
RSMRST#
PM_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
ICH9M
CPUPWRGD
PWRBTN#
SLP_S4#
SLP_S3#
PLT_RST#
PWROK
CK_PWRGD
VRMPWRGD
H_PWRGD
PENRYN
PWRGOOD
RESET#
H_CPURST#
CANTIGA
NB_RST#
PWROK
M_CKE[3:0]
DDR2 SODIMM
CKE[3:0]
CLK_PWRGD
VTT_PG
ICS9LPRS113A
CLK
TPS51117
EN
PGOOD1
+1_8VDIMM
+1_8VDIMM_PG
DIMM_ON
SMDDR_VTERM
RT9173
VCNTL
VIN
RUN_ON
NMOS 4468
+5VRUN
+3VRUN
APL5912
PGOOD1
+1_5VRUN
+1_5VRUN_PG
M92s_1.8-V by more than 1.1 V
within a 1 ms window
+1_8VRUN
M92S_VDD_CORE
GPU_PWRGD
PGOOD2
+1_5VRUN_PG
PMOS NDS352
VDDR3
+3.3V
+3VRUN
M92S_VDD_CORE to VDDR3 +3.3V <20ms
+1_1VRUN
+1_1VRUN_PG
VTT
VTT_PWRGD
EC_ALLSYSPG
+3V_RUN
VR_ON
CLK_EN#
ISL6261C
PGOOD
PGD_IN
V_CORE
IMVP_PWRGD
VR_PWRGD_CLKEN
EC_ALLSYSPG to VR_ON > 99msec
VR_ON to VRM_PGD_IN : 0.65msec
MSI CORPORATION
PPOWER UP SEQUENCY-2
Custom
MS-16911
Rev
10
Date: Saturday, April 18, 2009
Sheet 38 of 38