Essentials Oak 14 Schematic
Haswell-ULT

2013-4-19
REV : X02

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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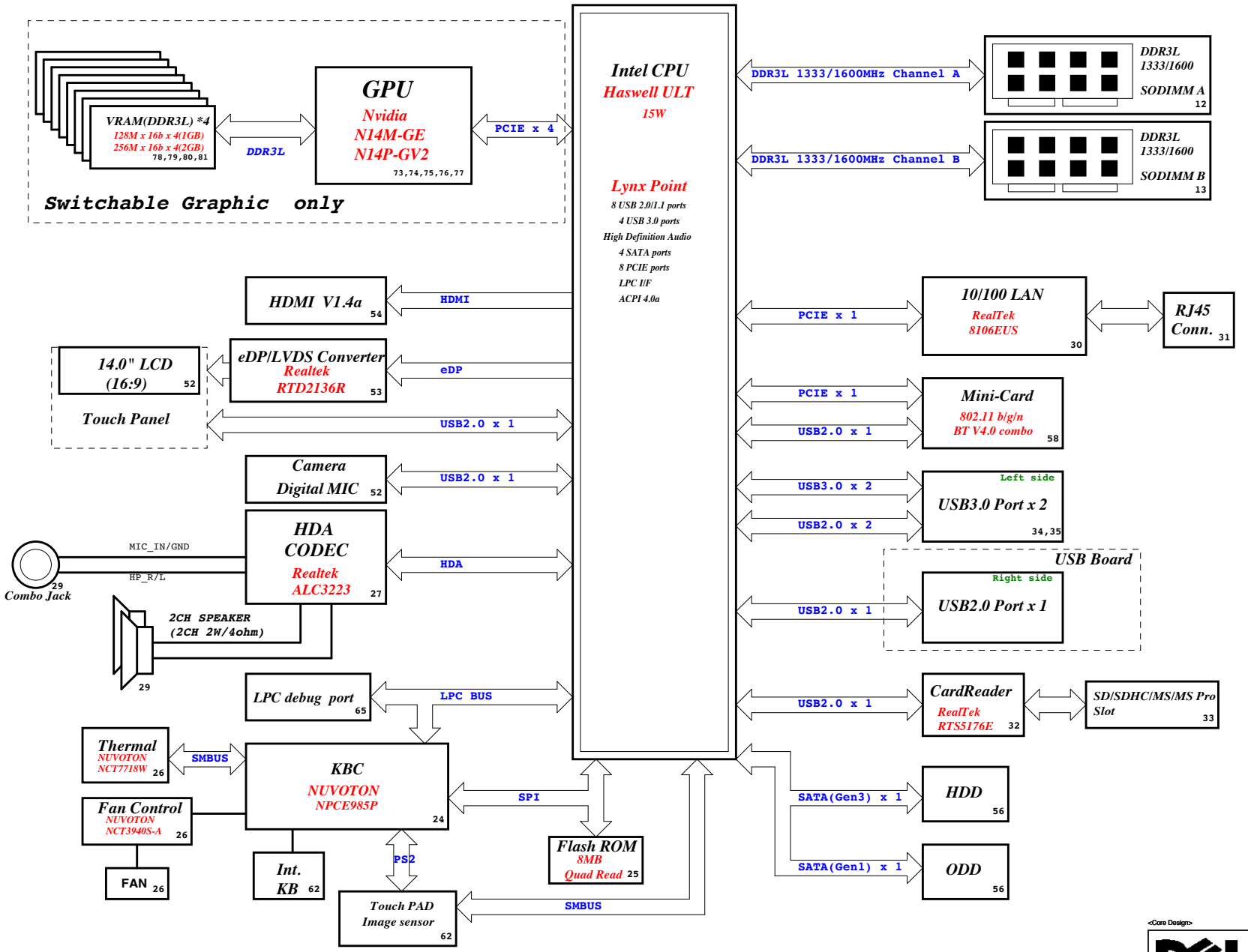
Title: *Cover Page*		
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Friday, April 19, 2013	Sheet 1 of 104	

Project code: 91.44L01.001
PCB P/N : 12314
Revision: X00

Oak14 Block Diagram



CHARGER	
BQ24717	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95813	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS	
TPS51216	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU 1.05V	
RT8237	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0	
TLV70215	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches 36 83

INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	0D675V_S0
VCCP_CPU	3D3V_S0
3D3V_S0	1D05V_VGA_S0
	3D3V_VGA_S0
	1D35V_VGA_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: Block Diagram

Size	Document Number	Rev
C	OAK14 Haswell	X00

Date: Tuesday, February 26, 2013 Sheet 2 of 104

(Blanking)

<Core Design>

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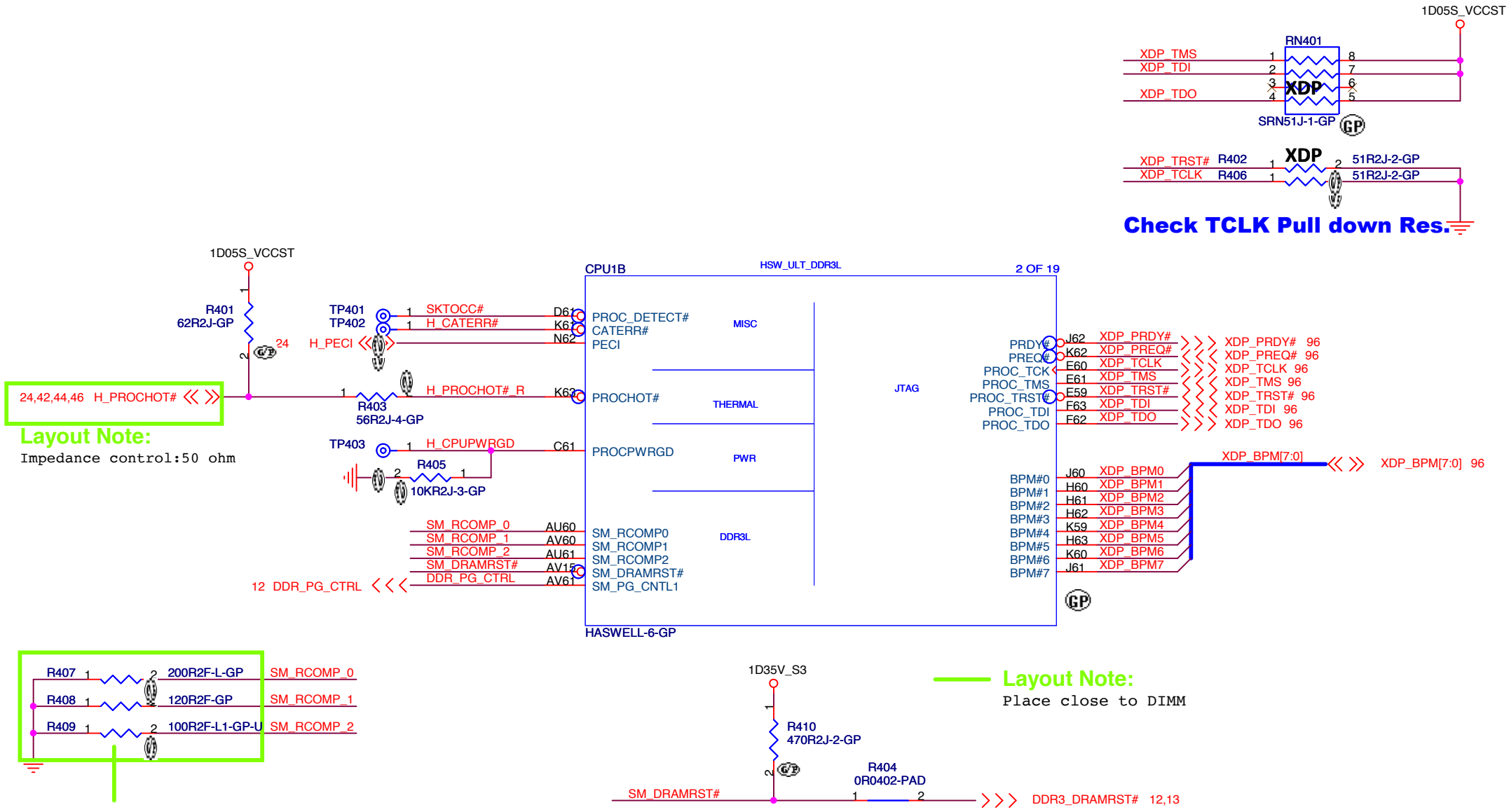
Title

(Reserved)

Size	Document Number	Rev
A3	*OAK14 Haswell*	*X00*

Date: Thursday, January 10, 2013 Sheet 3 of 104

SSID = CPU



<Core Design>

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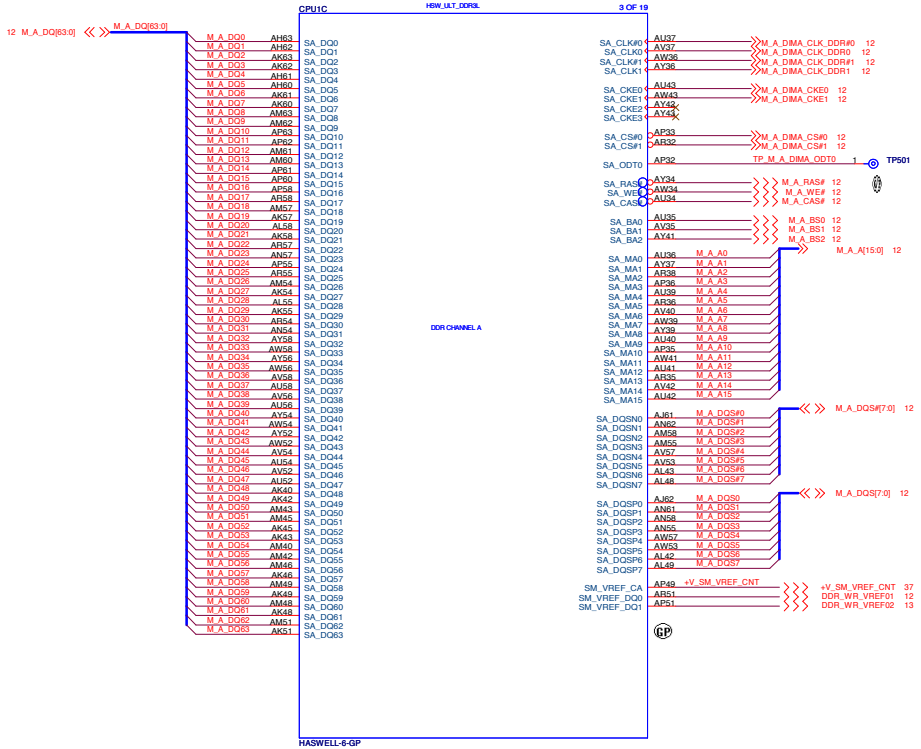
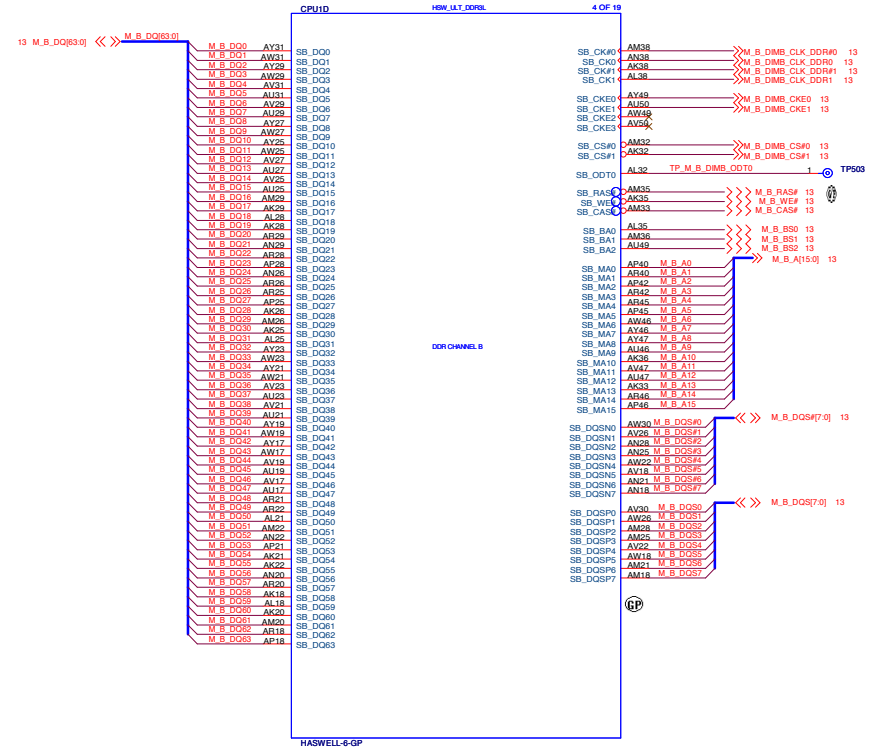
Title: ***CPU (THERMAL/MISC/PM)***

Size	Document Number	Rev
A4	***OAK14 Haswell***	***X00***

Date: Friday, April 12, 2013 Sheet 4 of 104

SSID = CPU





<Core Design>

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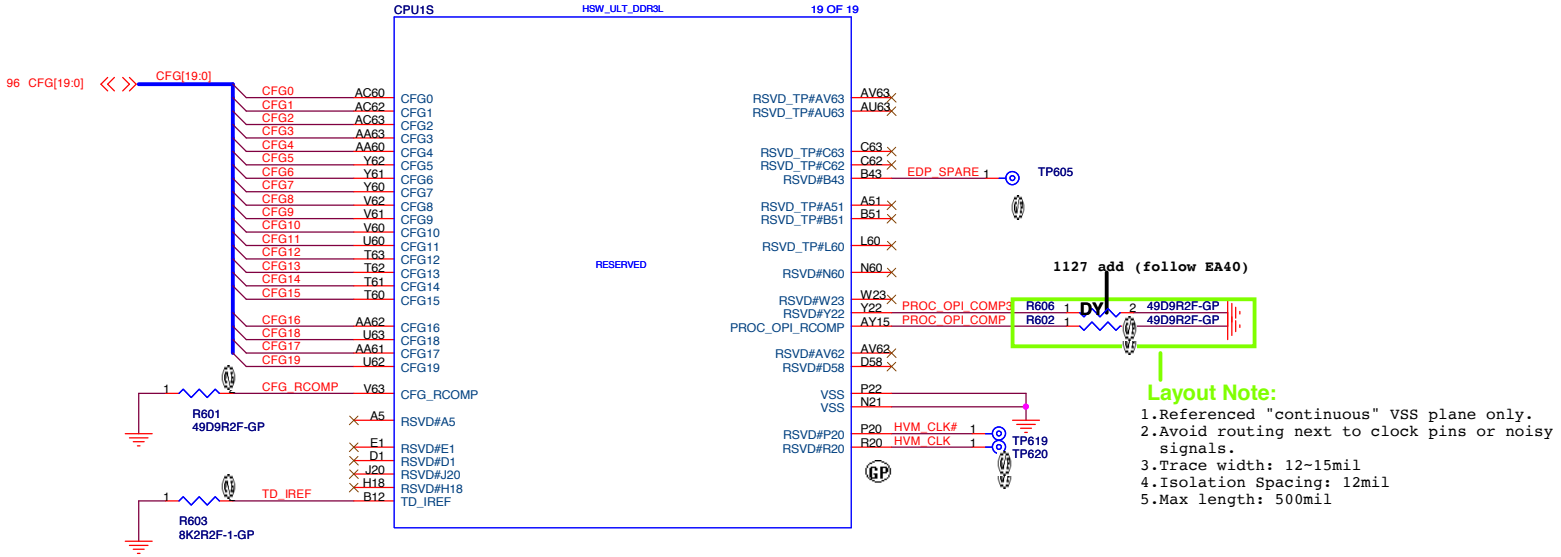
Title: CPU (DDR)

Size	Document Number	Rev
A2	OAK14 Haswell	X00

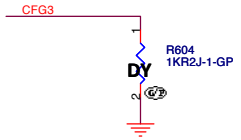
Date: Thursday, March 07, 2013 Sheet 5 of 104

SSID = CPU

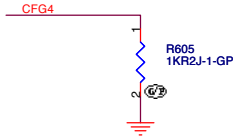


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, March 07, 2013 | Sheet 6 of 104

SSID = CPU

1D05S_VCCST

R703 1 75R2F-2-GP VR_SVID_ALERT#

R704 1 130R2F-1-GP H_CPU_SVIDDAT

1127 130R change to 110R
1203 110R change to 130R

1127 Change net name of R703.2 from VR_SVID_ALERT# to H_CPU_SVIDALRT#

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil

VCC_CORE

R702 100R2F-L1-GP-U

46 VCC_SENSE

TP701 TP_VCCIO_OUT

+VCCIOA_OUT

R701 43R2J-GP

46 VR_SVID_ALERT# H_CPU_SVIDALRT#

46 H_CPU_SVIDCLK H_CPU_SVIDCLK

46 H_CPU_SVIDDAT H_CPU_SVIDDAT

H_VCCST_PWRGD

46 H_VR_ENABLE R710 1 DY 2 10KR2J-3-GP

IMVP_PWRGD_R

96 PWR_DEBUG PWR_DEBUG

1D05S_VCCST R705 1 150R2J-L1-GP-U

1127_modify (follow EA40)

3D3V_S5

1D05S_VCCST

C702 DY SCD1U10V2KX-5GP

U701

NC#1 VCC

A DY

GND Y

74LVC1G07GW-GP

73.01G07.0HG

R706 10KR2J-3-GP DY

36,48 1D05V_VTT_PWRGD

H_VCCST_PWRGD 96

R707 100KR2F-L1-GP

R709 47KR2F-GP

1D05V_S0 R711 1D05S_VCCST

0R0603-PAD-1-GP

C701 SC22U6D3V5MX-2GP

DY

C703 SC1U6D3V2KX-GP

A00 4/8 R711 down size to 0603

1205 Add

24,46 IMVP_PWRGD R713 100KR2F-L1-GP IMVP_PWRGD_R

R712 47KR2F-GP

CPU1L HSW_ULT_DDR3L 12 OF 19

1D35V_S3

L59 RSVD#L59
J58 RSVD#J58

AH26 VDDQ
AJ31 VDDQ
AJ33 VDDQ
AJ37 VDDQ
AN33 VDDQ
AP43 VDDQ
AR48 VDDQ
AY35 VDDQ
AY40 VDDQ
AY44 VDDQ
AY50 VDDQ

VCC_CORE

F59 VCC
N58 RSVD#N58
AC58 RSVD#AC58

E63 VCC_SENSE
AB23 RSVD#AB23
A59 VCCIO_OUT
E20 VCCIOA_OUT
AD23 RSVD#AD23
AA23 RSVD#AA23
AE59 RSVD#AE59

L62 VIDALERT#
N63 VIDSCLK
L63 VIDSOUT
B59 VCCST_PWRGD
F60 VR_EN
C59 VR_READY

D63 VSS
H59 PWR_DEBUG#
P62 VSS
P60 RSVD_TP#P60
P61 RSVD_TP#P61
N59 RSVD_TP#N59
N61 RSVD_TP#N61
T59 RSVD#T59
AD60 RSVD#AD60
AD59 RSVD#AD59
AA59 RSVD#AA59
AE60 RSVD#AE60
AC59 RSVD#AC59
AG58 RSVD#AG58
U59 RSVD#U59
V59 RSVD#V59

1D05S_VCCST

AC22 VCCST
AE22 VCCST
AE23 VCCST

VCC_CORE

AB57 VCC
AD57 VCC
AG57 VCC
C24 VCC
C28 VCC
C32 VCC

HSW ULT POWER

VCC_CORE

VCC C36
VCC C40
VCC C44
VCC C48
VCC C52
VCC C56
VCC E23
VCC E25
VCC E27
VCC E29
VCC E31
VCC E33
VCC E35
VCC E37
VCC E39
VCC E41
VCC E43
VCC E45
VCC E47
VCC E49
VCC F51
VCC F53
VCC F55
VCC F57
VCC F24
VCC F28
VCC F32
VCC F36
VCC F40
VCC F44
VCC F48
VCC F52
VCC F56
VCC G23
VCC G25
VCC G27
VCC G29
VCC G31
VCC G33
VCC G35
VCC G37
VCC G39
VCC G41
VCC G43
VCC G45
VCC G47
VCC G49
VCC G51
VCC G53
VCC G55
VCC G57
VCC H23
VCC J23
VCC K23
VCC K57
VCC L22
VCC M23
VCC M57
VCC P57
VCC U57
VCC W57

HASWELL-6-GP

<Core Design>

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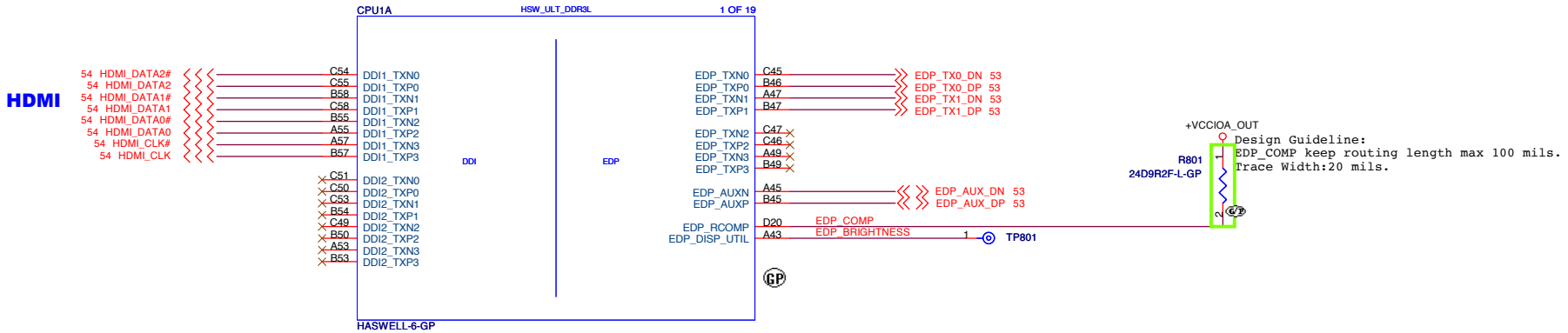
Title: CPU (VCC CORE)

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Monday, April 22, 2013 | Sheet 7 of 104

SSID = CPU



<Core Design>

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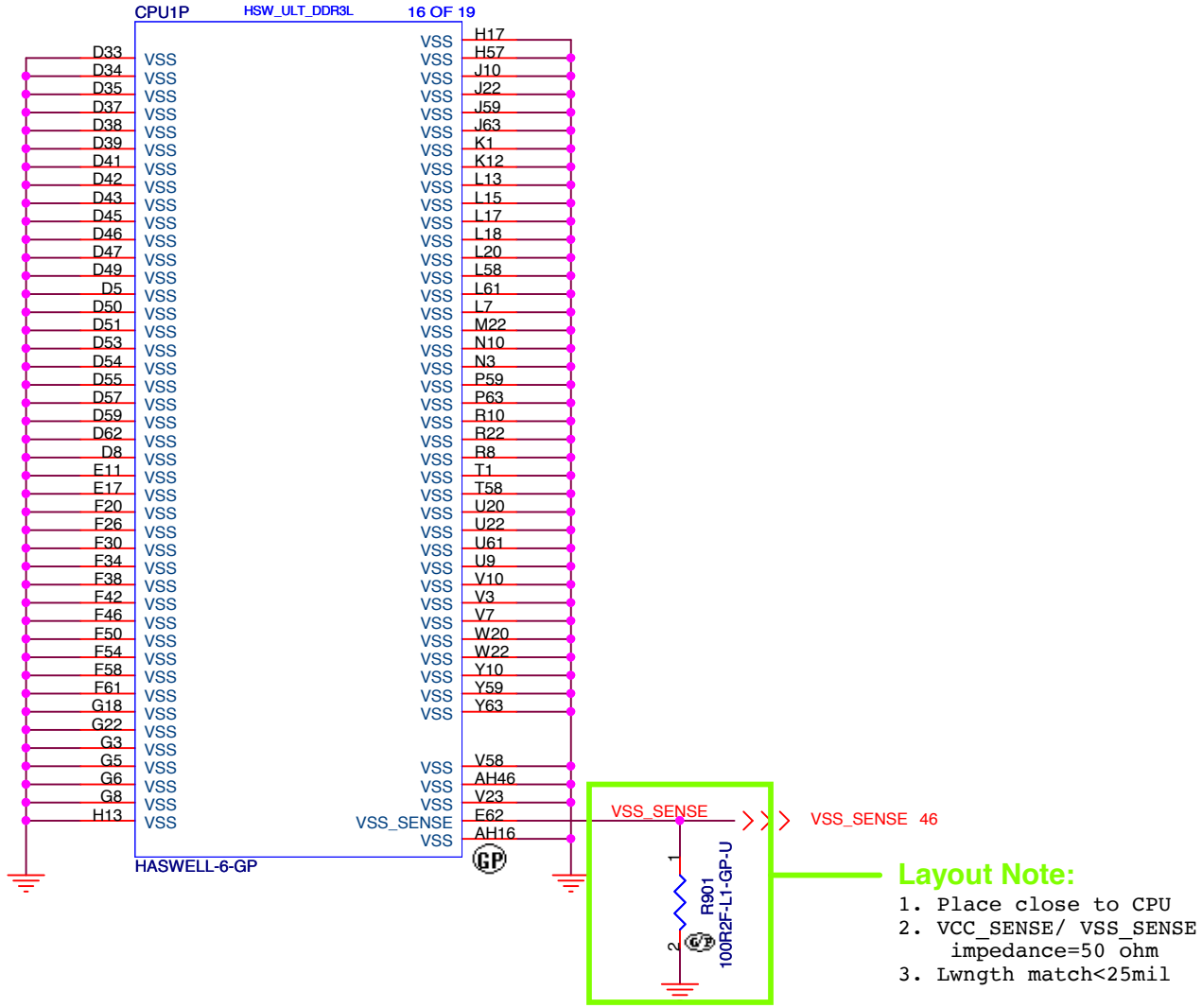
Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	OAK14 Haswell	X00

Date: Thursday, March 07, 2013 Sheet 8 of 104

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil

<Core Design>

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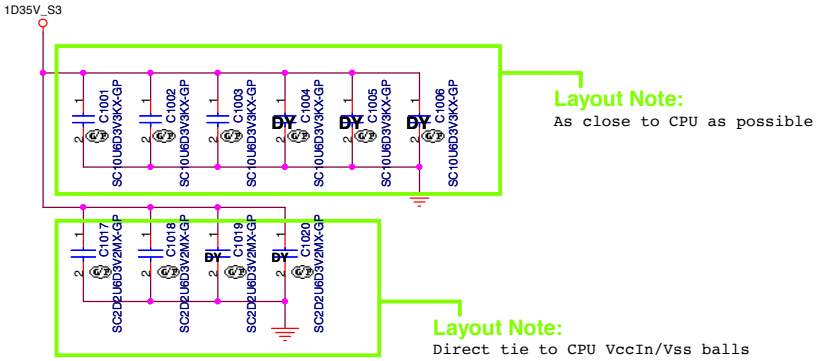
Title	CPU (VSS)	
Size A4	Document Number OAK14 Haswell	Rev X00
Date: Thursday, March 07, 2013	Sheet 9 of 104	

SSID = CPU



<Core Design>

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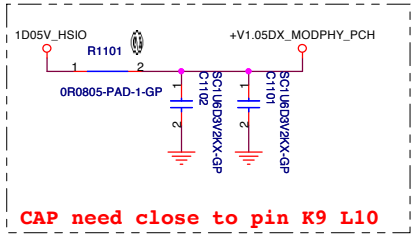
Title: Reserved

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, April 25, 2013 | Sheet 10 of 104

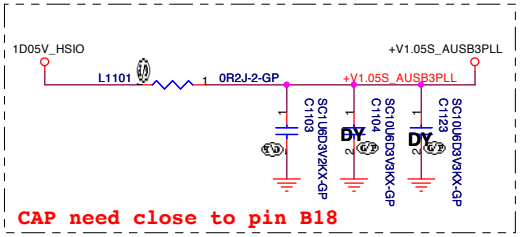
MAX: 1.92A

1.838A



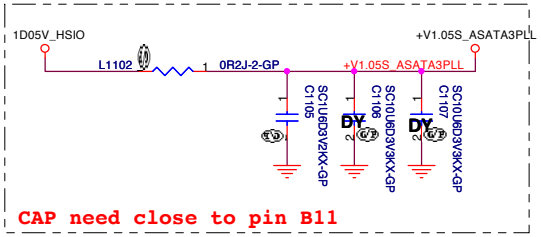
CAP need close to pin K9 L10

41mA



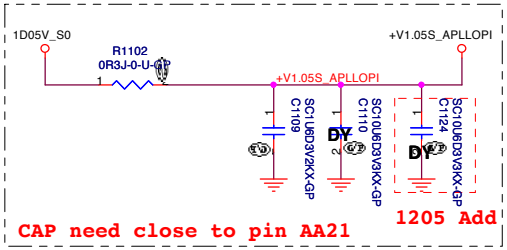
CAP need close to pin B18

42mA



CAP need close to pin B11

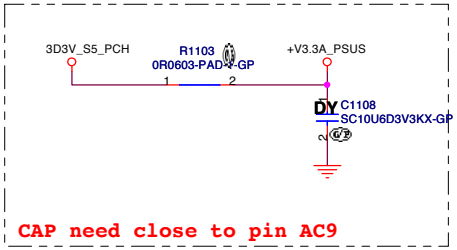
57mA



CAP need close to pin AA21

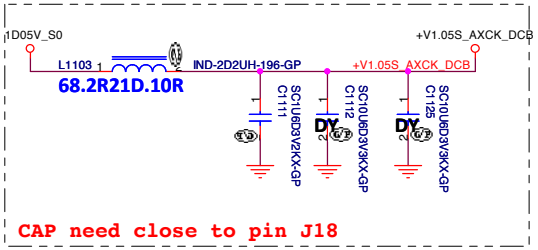
1205 Add

62mA



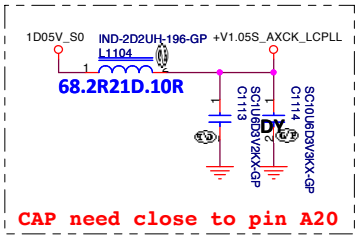
CAP need close to pin AC9

200mA



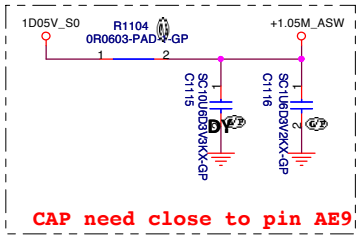
CAP need close to pin J18

31mA



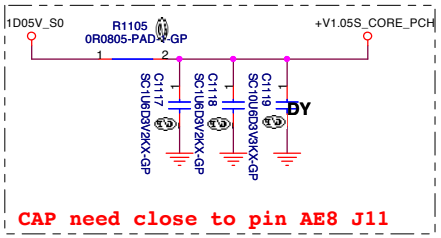
CAP need close to pin A20

658mA



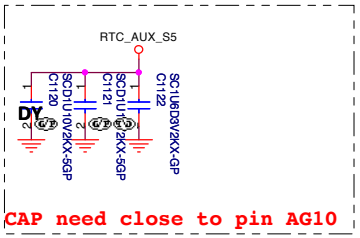
CAP need close to pin AE9

1.632A



CAP need close to pin AE8 J11

1mA



CAP need close to pin AG10

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A3	OAK14 Haswell	X00

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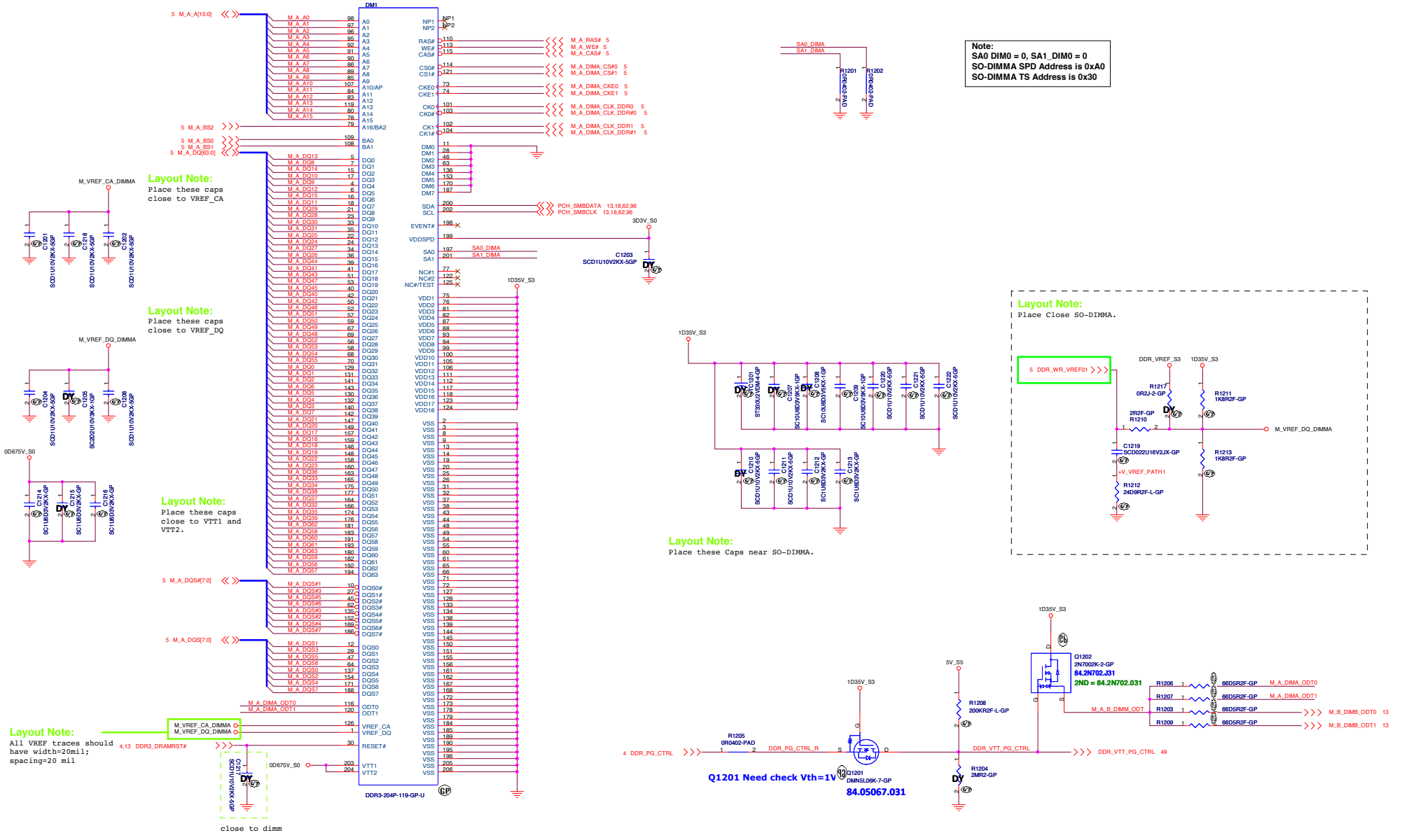
SSID = MEMORY



<Core Design>

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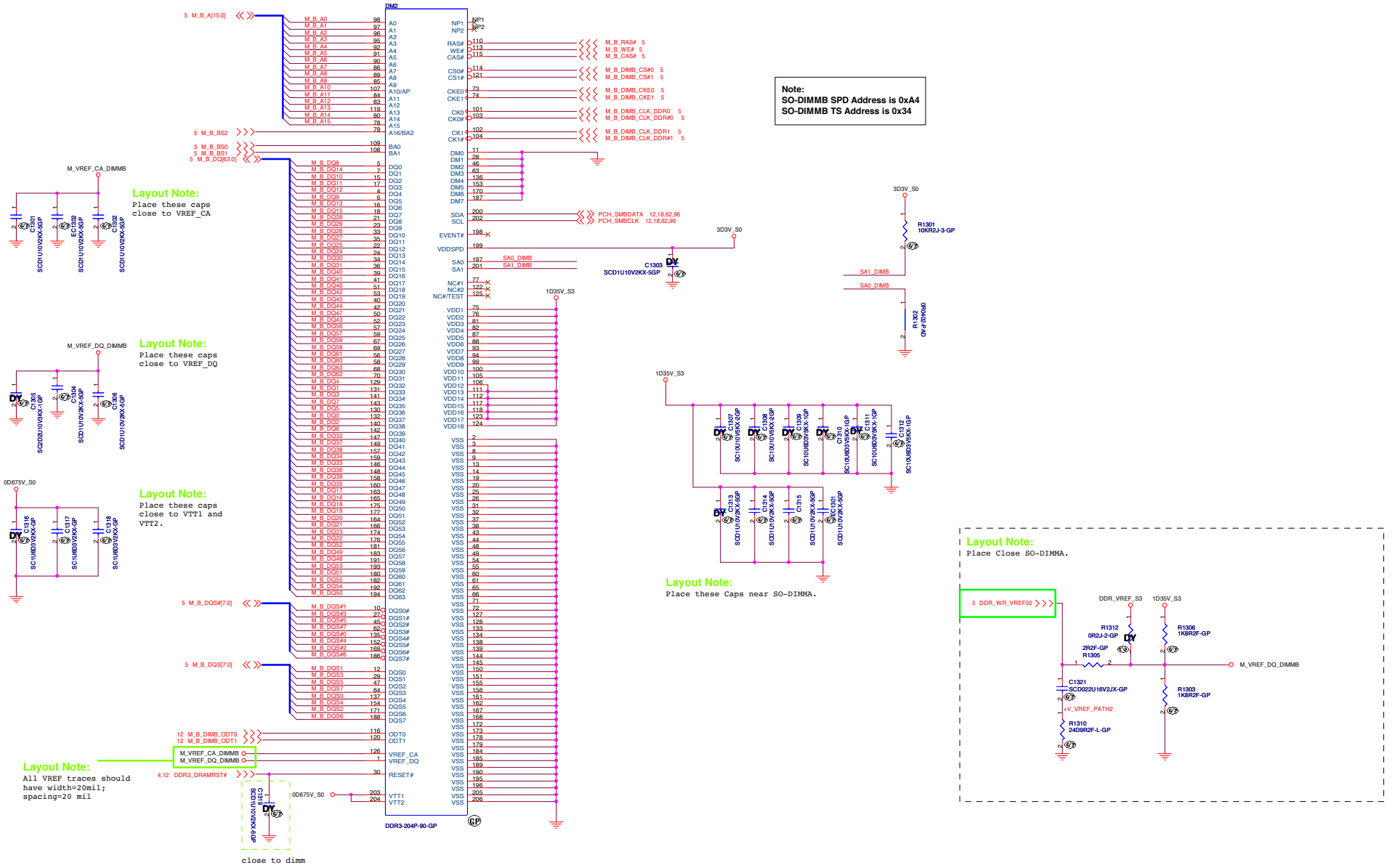
Title: DDR3-SODIMM1

Size: A2 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, April 18, 2013 | Sheet 12 of 104

SSID = MEMORY



<Core Design>

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Title: **DDR3-SODIMM2**

Size: A2 | Document Number: **OAK14 Haswell** | Rev: **X00**

Date: Friday, April 12, 2013 | Sheet 13 of 104

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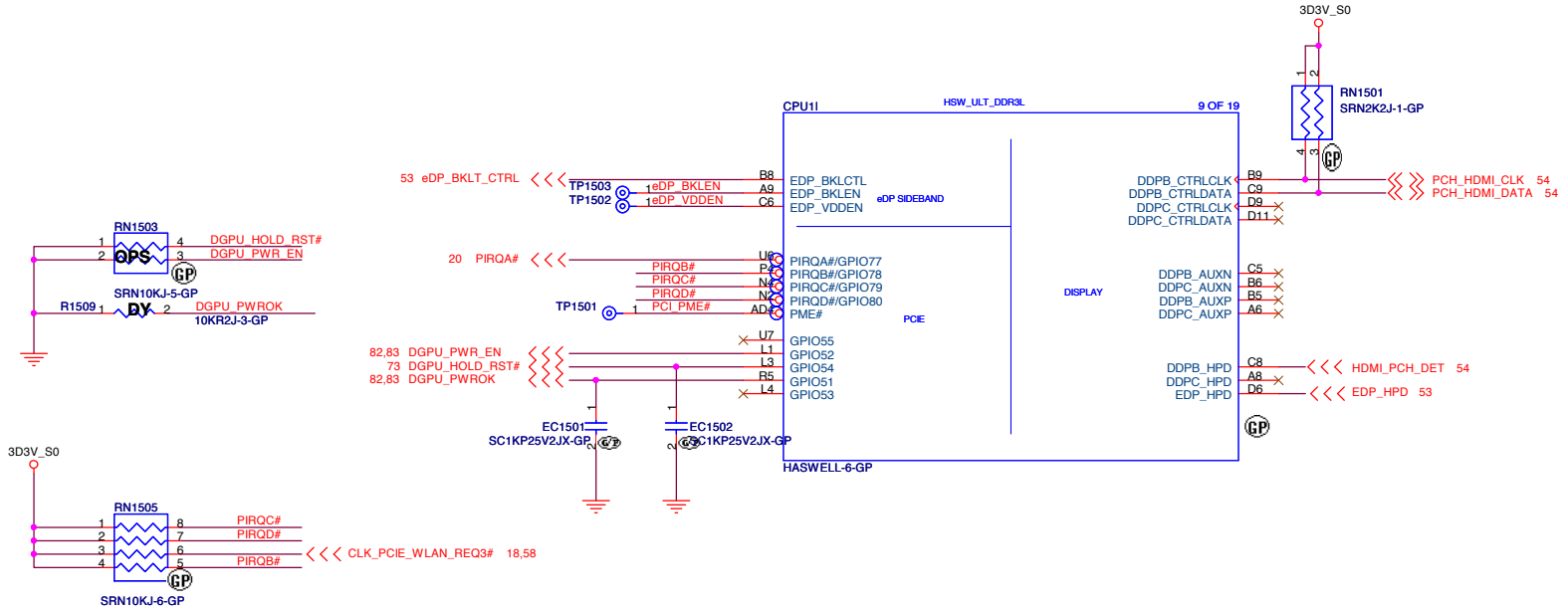
Title	M3	
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Thursday, January 10, 2013	Sheet 14 of 104	

SSID = CPU



<Core Design>

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Title	PCH (EDP/GPIO/DDI)	
Size A3	Document Number OAK14 Haswell	Rev X00
Date: Thursday, March 07, 2013	Sheet 15 of 104	

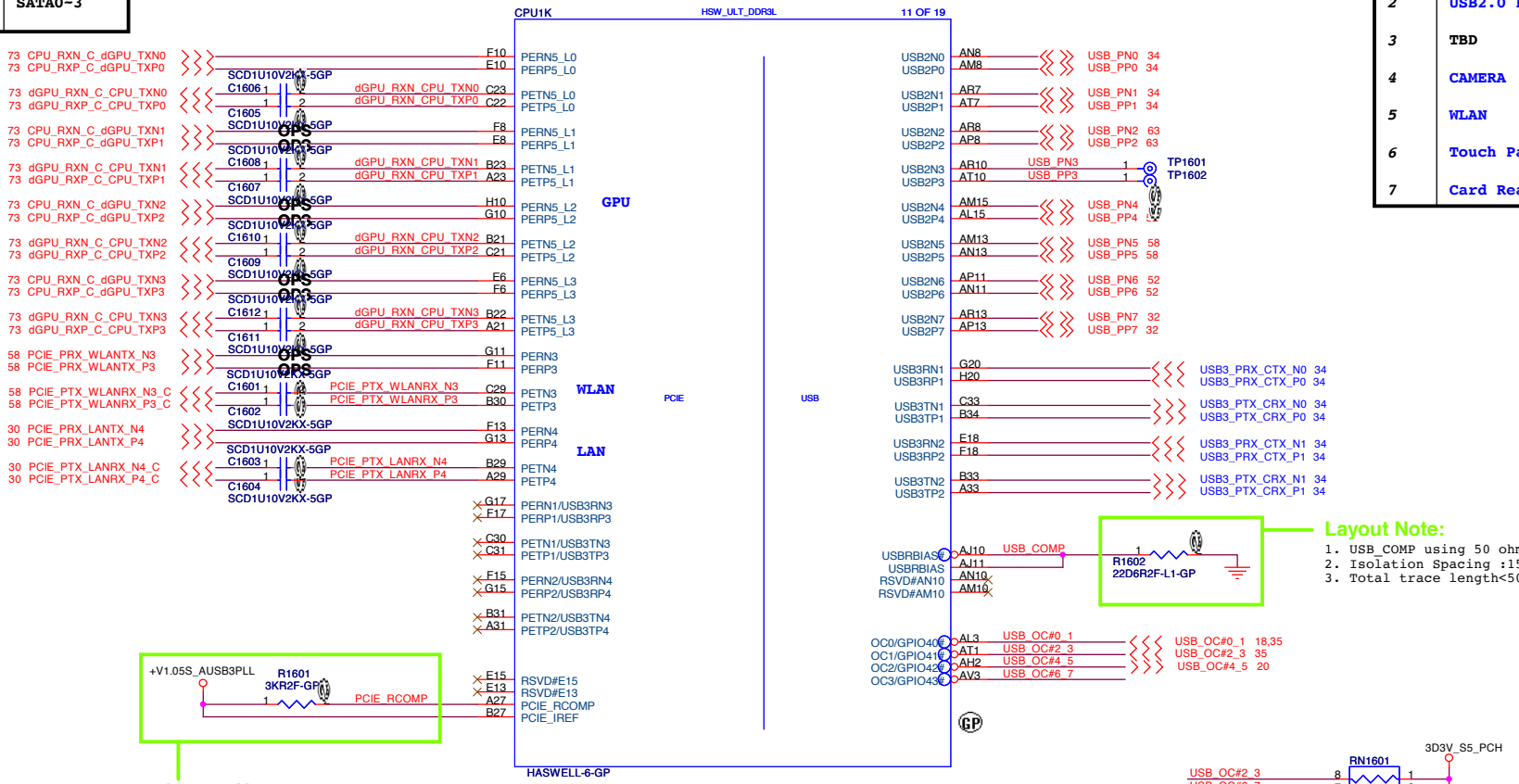
SSID = PCH

PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5(4lane)	GPU	
6(4lane)	TBD	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3
3	TBD
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



<Core Design>

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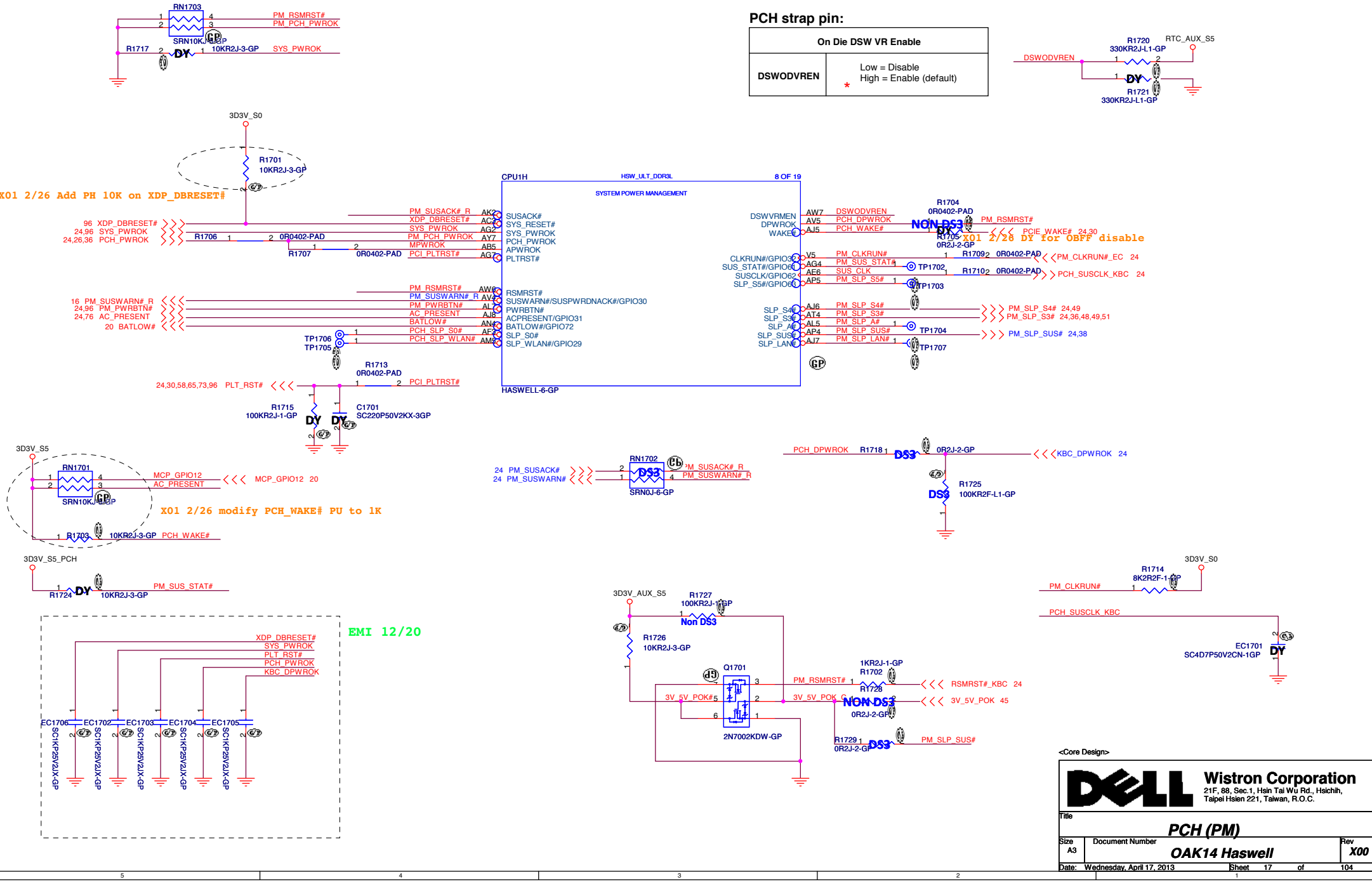
Title	PCH (PCIE/USB)	
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Thursday, March 07, 2013	Sheet 16 of 104	

SSID = PCH



<Core Design>

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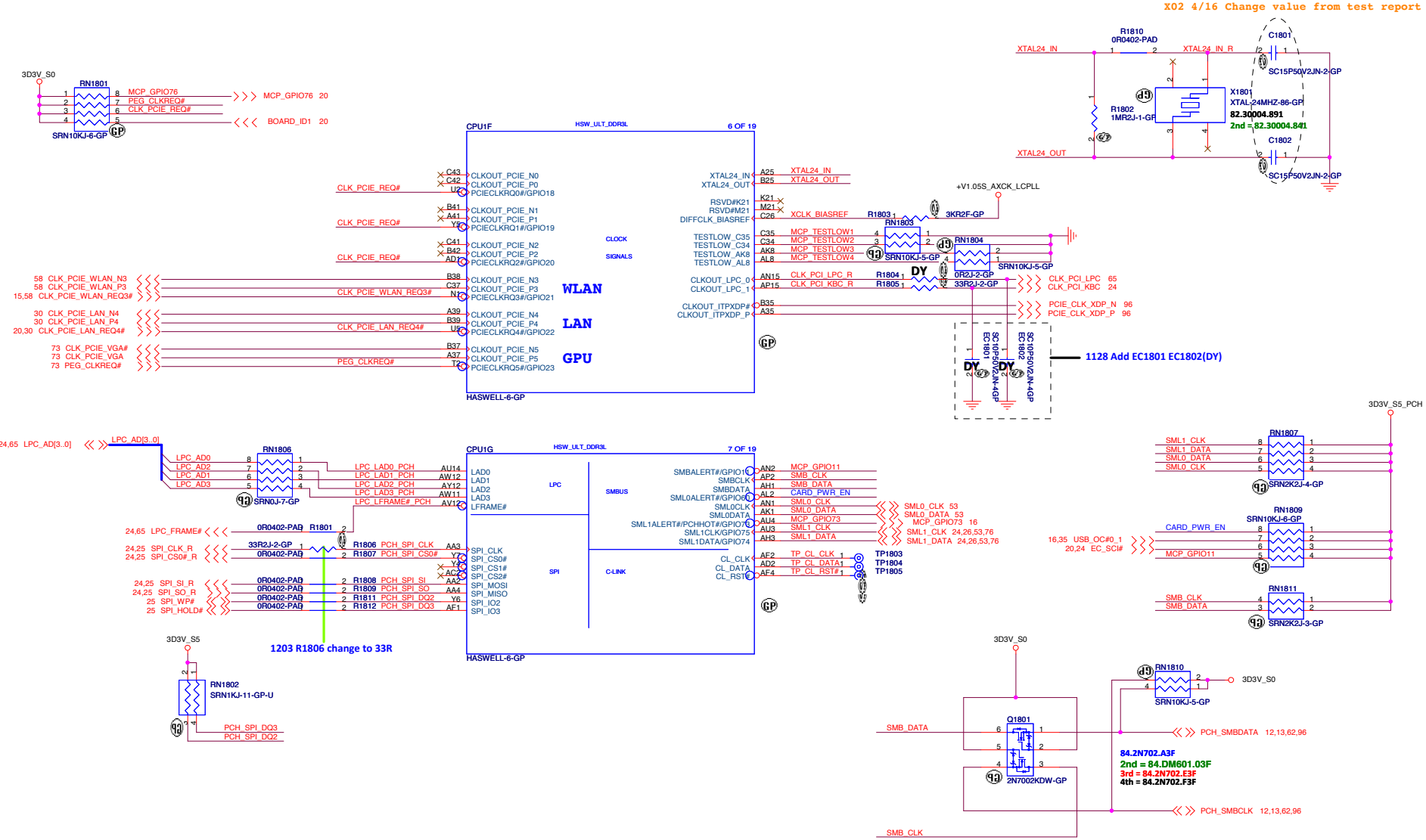
Title	PCH (PM)	
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Wednesday, April 17, 2013	Sheet 17 of 104	

SSID = PCH

X02 4/16 Change value from test report



<Core Design>

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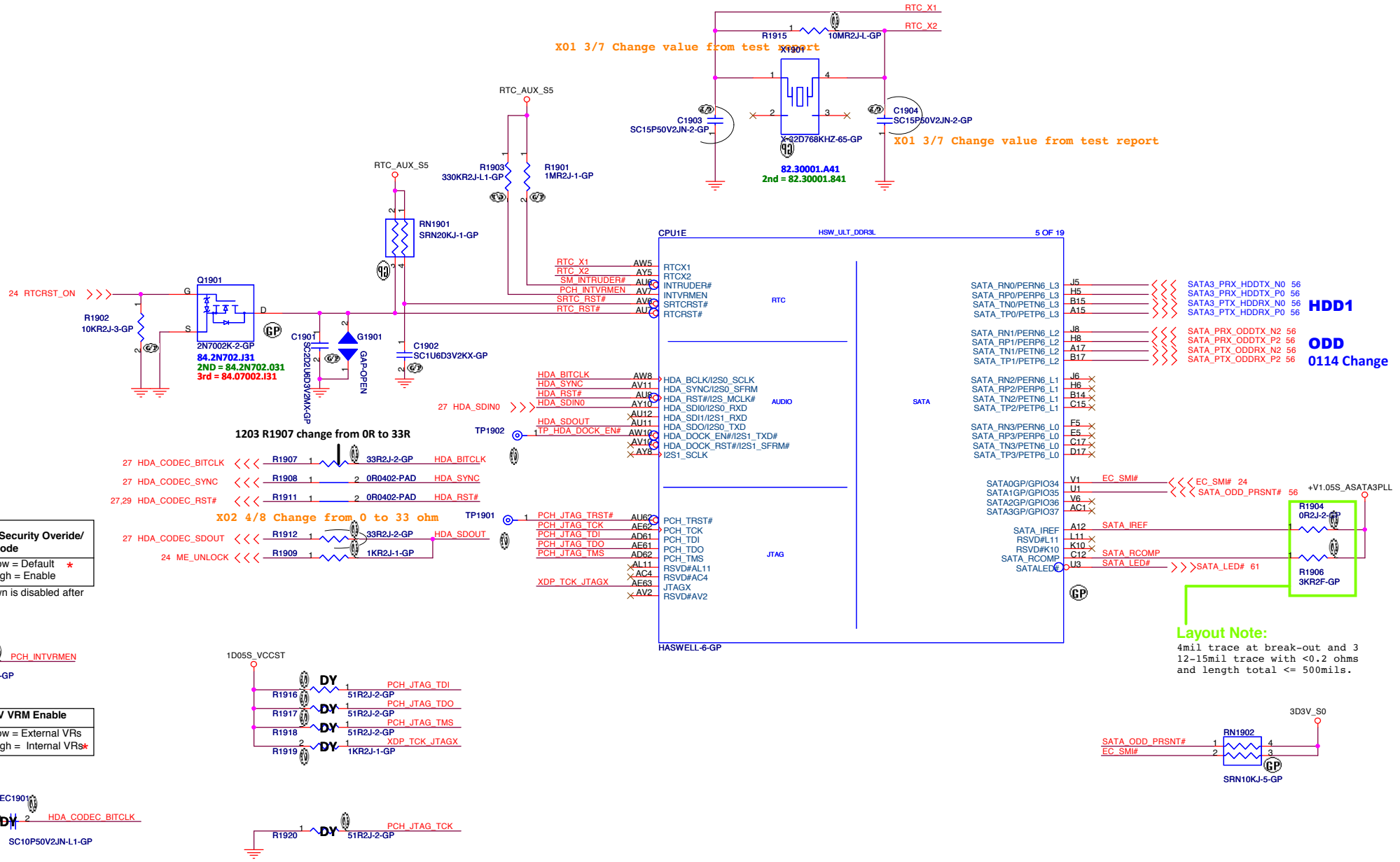
Title: PCH (CLOCK/SMBUS/CL/LPC/SPI)

Size: Custom | Document Number: OAK14 Haswell | Rev: X00

Date: Wednesday, April 17, 2013 | Sheet 18 of 104

SSID = CPU



<Core Design>

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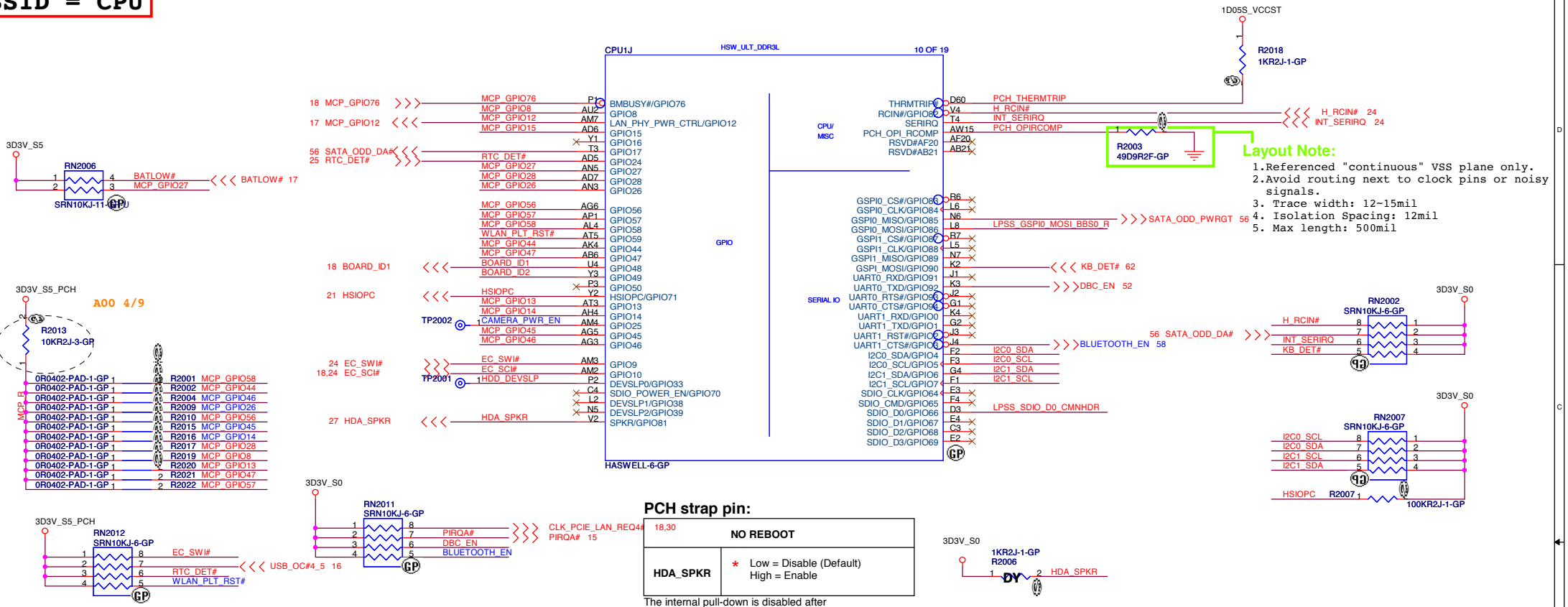
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (RTC/SATA/HDA/JTAG)

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, April 25, 2013 | Sheet 19 of 104

SSID = CPU



PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

3D3V_S0 — R2011 1KR2J-1-GP — DY — LPSS_SDIO_D0_CMNHDR

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

3D3V_S5_PCH — R2014 1KR2J-1-GP — DY — MCP_GPIO15

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

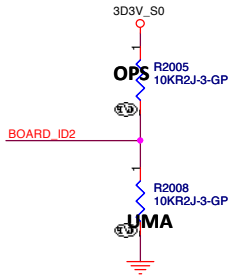
The internal pull-down is disabled after PLTRST# deasserts

3D3V_S0 — R2012 1KR2J-1-GP — DY — LPSS_GSPI0_MOSI_BBS0_R

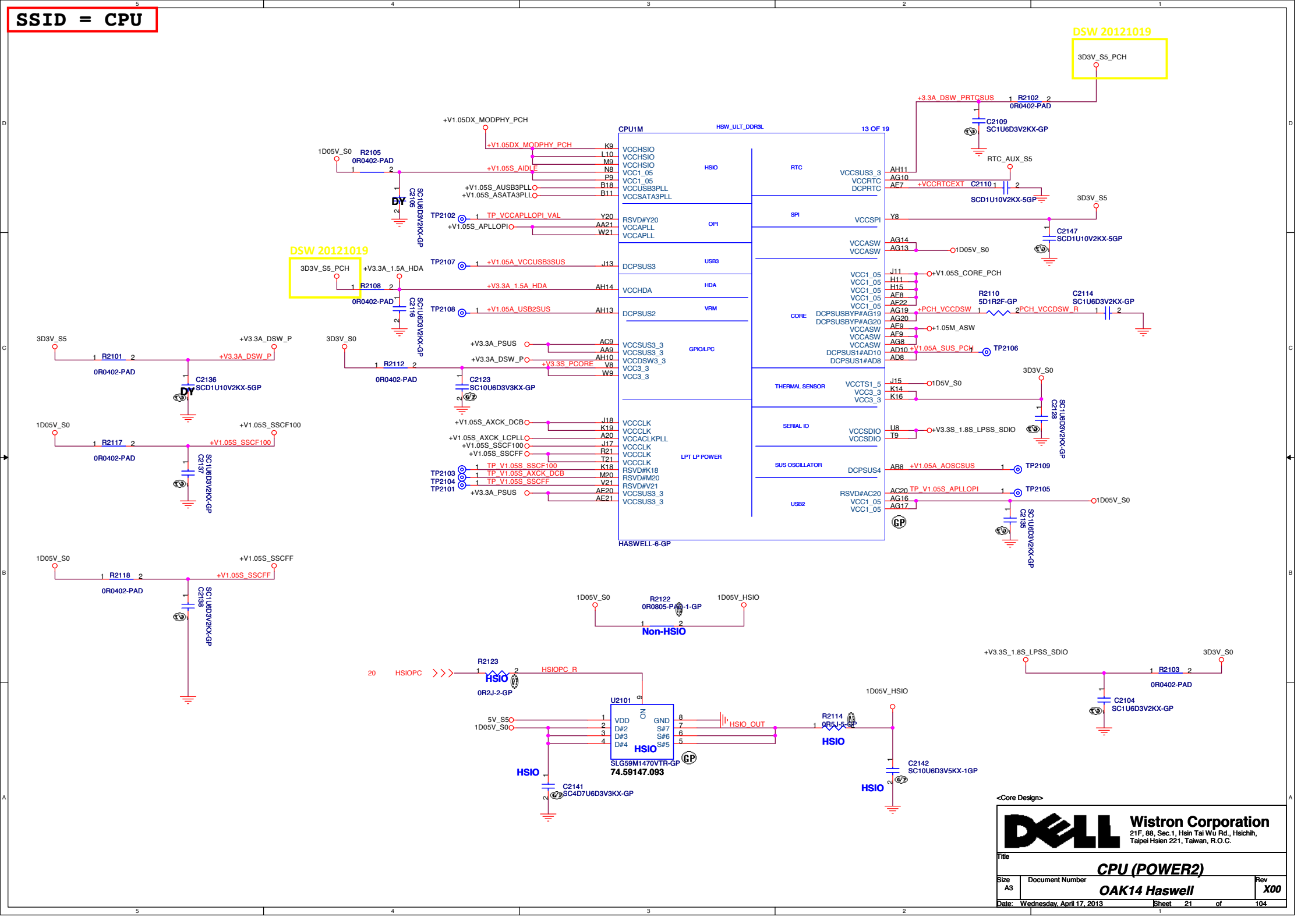
Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
UMA	1	0
DIS	1	1



SSID = CPU



<Core Design>

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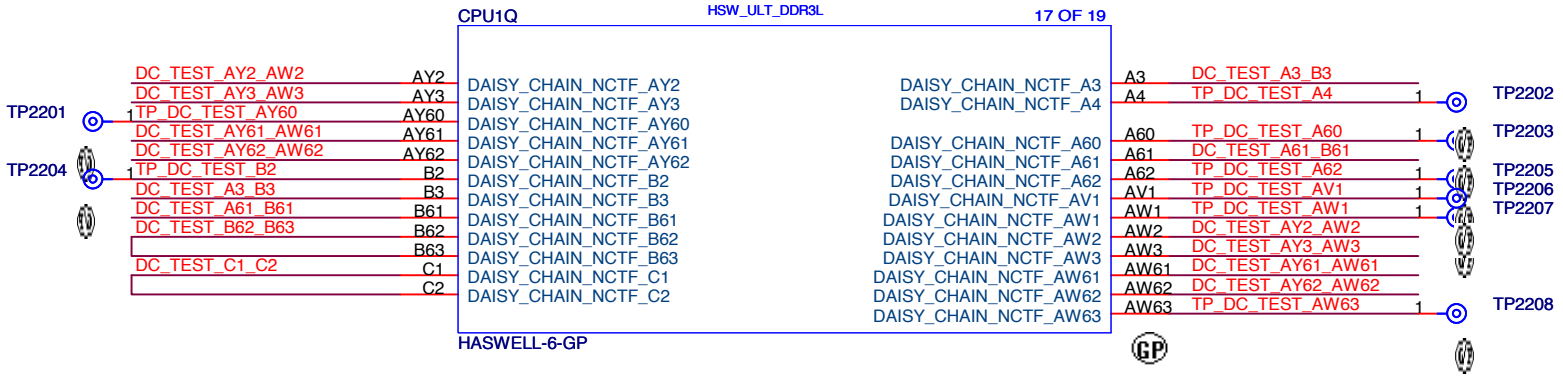
Title: CPU (POWER2)

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Wednesday, April 17, 2013 | Sheet 21 of 104

SSID = PCH



<Core Design>

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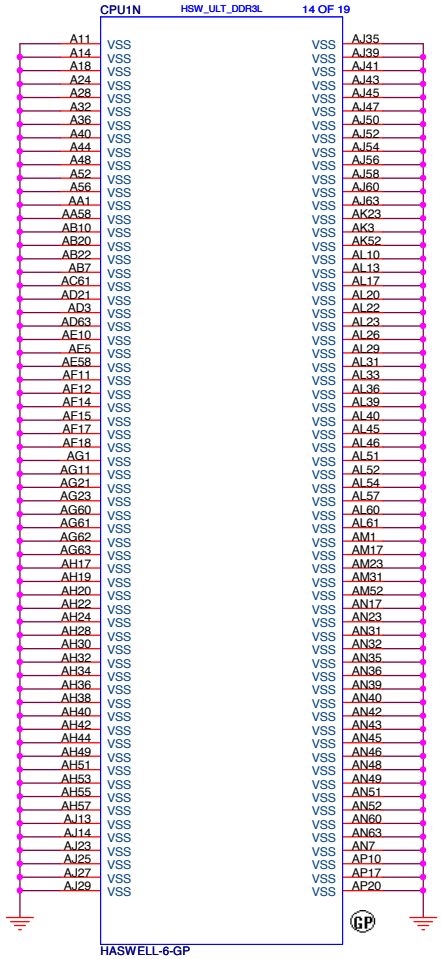
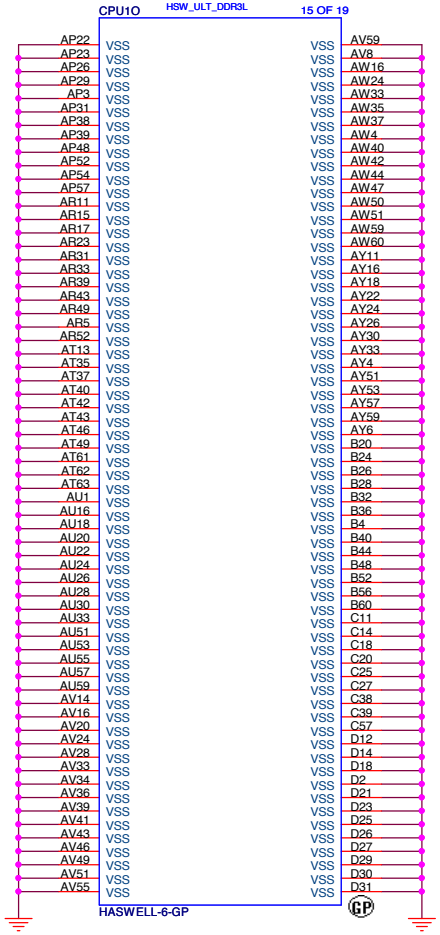
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***OAK14 Haswell***	***X00***

Date: Thursday, January 10, 2013 Sheet 22 of 104

SSID = PCH





<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 23 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

X02 4/8 Change to X02

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
UMA	100.0K	10.0K(64.10025.6D1.)	3.0V
TBD	100.0K	13.7K(64.13725.6D1.)	2.902V
TBD	100.0K	17.8K(64.17825.6D1.)	2.801V
TBD	100.0K	22.1K(64.22125.6D1.)	2.702V
TBD	100.0K	27.0K(64.27025.6D1.)	2.598V
TBD	100.0K	32.4K(64.32425.6D1.)	2.492V
TBD	100.0K	37.4K(64.37425.6D1.)	2.402V
TBD	100.0K	43.2K(64.43225.6D1.)	2.304V
DIS	100.0K	49.9K(64.49925.6D1.)	2.201V
N14M-GE	100.0K	57.6K(64.57625.6D1.)	2.093V
N14P-GV2	100.0K	64.9K(64.64925.6D1.)	2.001V
TBD	100.0K	73.2K(64.73225.6D1.)	1.905V
TBD	100.0K	82.5K(64.82525.6D1.)	1.808V
TBD	100.0K	93.1K(64.93125.6D1.)	1.709V
TBD	100.0K	107K(64.10725.6D1.)	1.594V
TBD	100.0K	120K(64.12035.6D1.)	1.499V
TBD	100.0K	137K(64.13735.6D1.)	1.392V
TBD	100.0K	154K(64.15435.6D1.)	1.299V
TBD	100.0K	200K(64.20035.6D1.)	1.099V
TBD	100.0K	232K(64.23236.6D1.)	0.994V

Layout Note:
Need very close to EC

X01 3/5 move WPAN_LED# from GPIO85 to GPIO93

Layout Note:
Need very close to EC

Power Switch Logic(PSL)

Layout Note:
Need very close to EC
C2422 PDG is 47p

A00 4/9 move PCIE_WAKE# from GPO33 to GPI083

Don't PD

ALL_SYS_PWRGD assert,
delay 10ms; PCH_PWROK assert.
ALL_SYS_PWRGD de-assert,
delay 100ms; SYS_PWROK assert.
LVDS backlight Control from PS8625

eDP backlight Control from Travis
Travis request response time < 1ms

71.00985.C0G

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

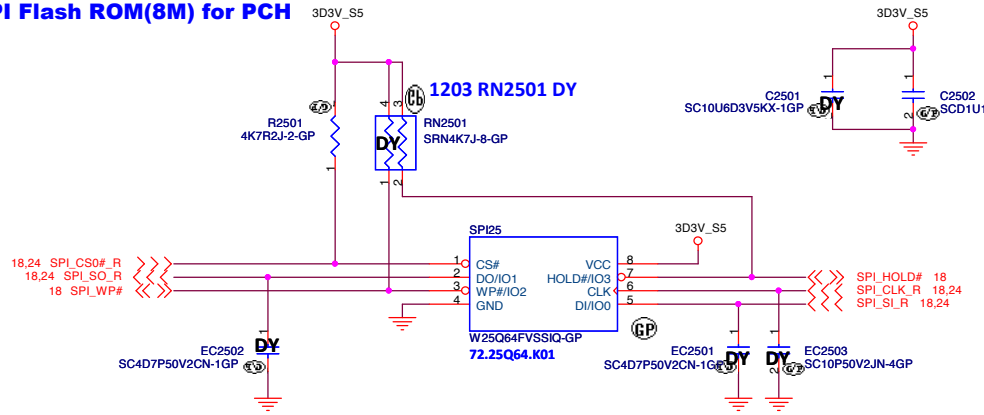
EC_GPIO47 High Active

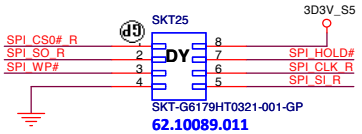
A00 4/3 change R2414 from 100K to 10K

0111 Add

SSID = Flash.ROM

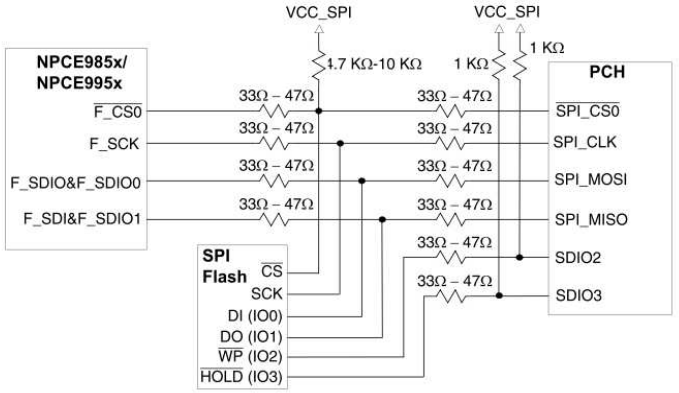
SPI Flash ROM(8M) for PCH





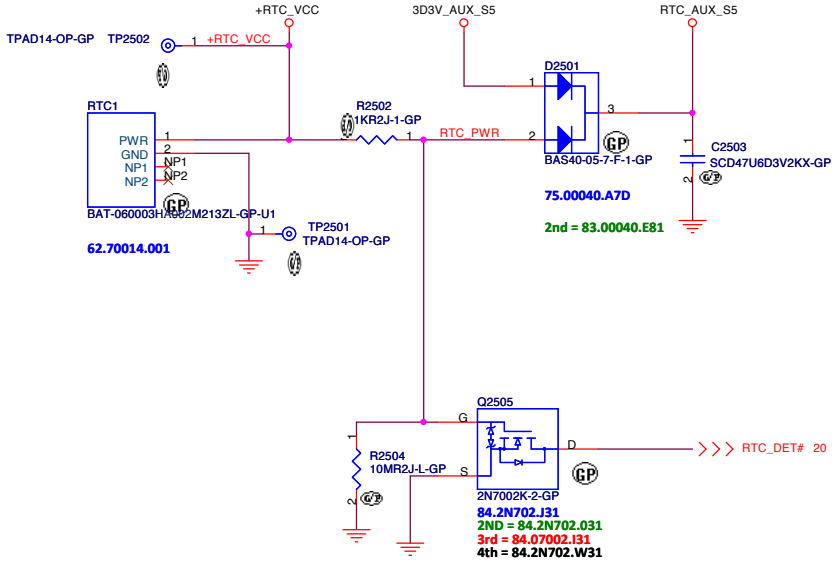
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25Q64.F01	O	O
72.25Q64.D01	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

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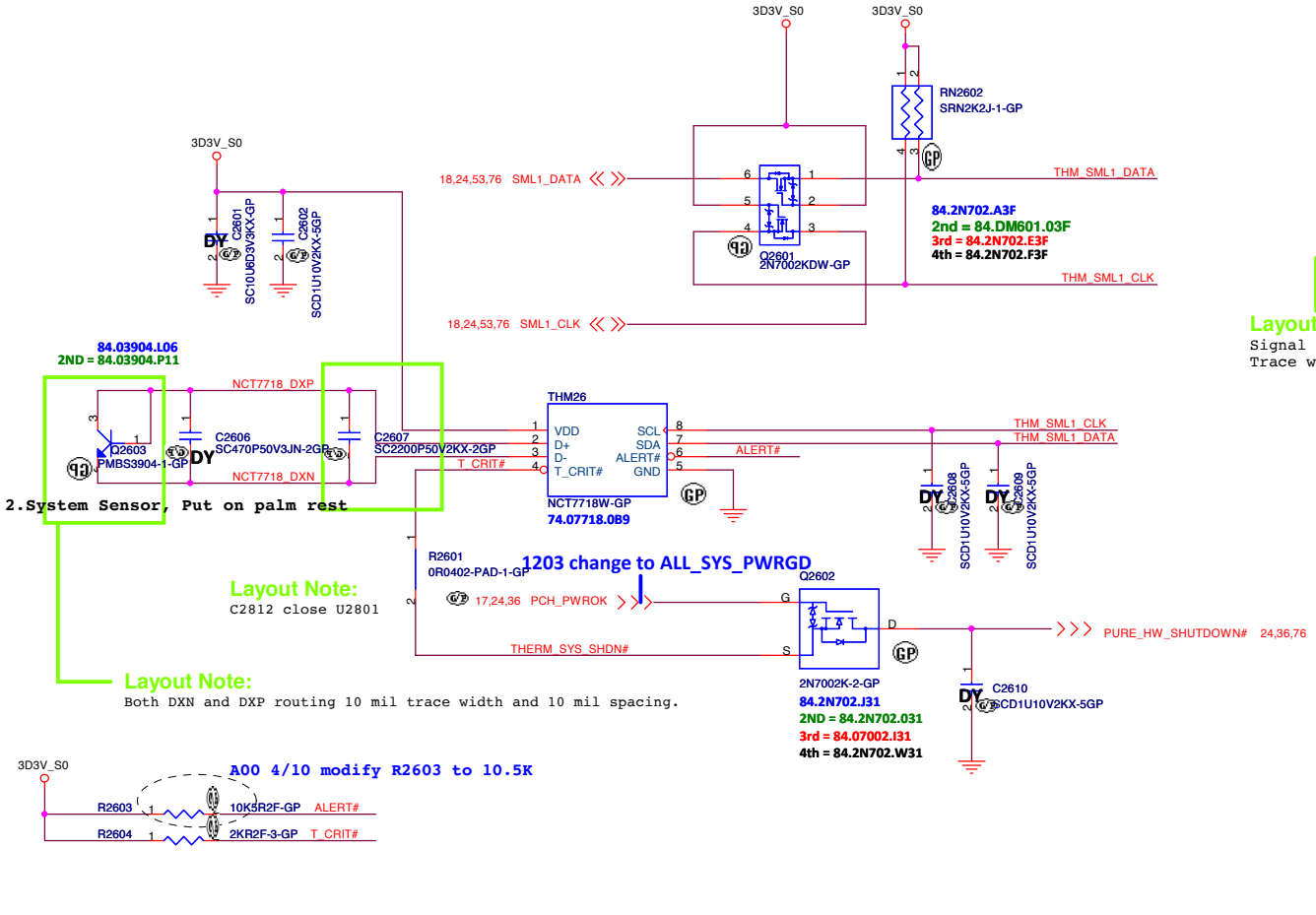
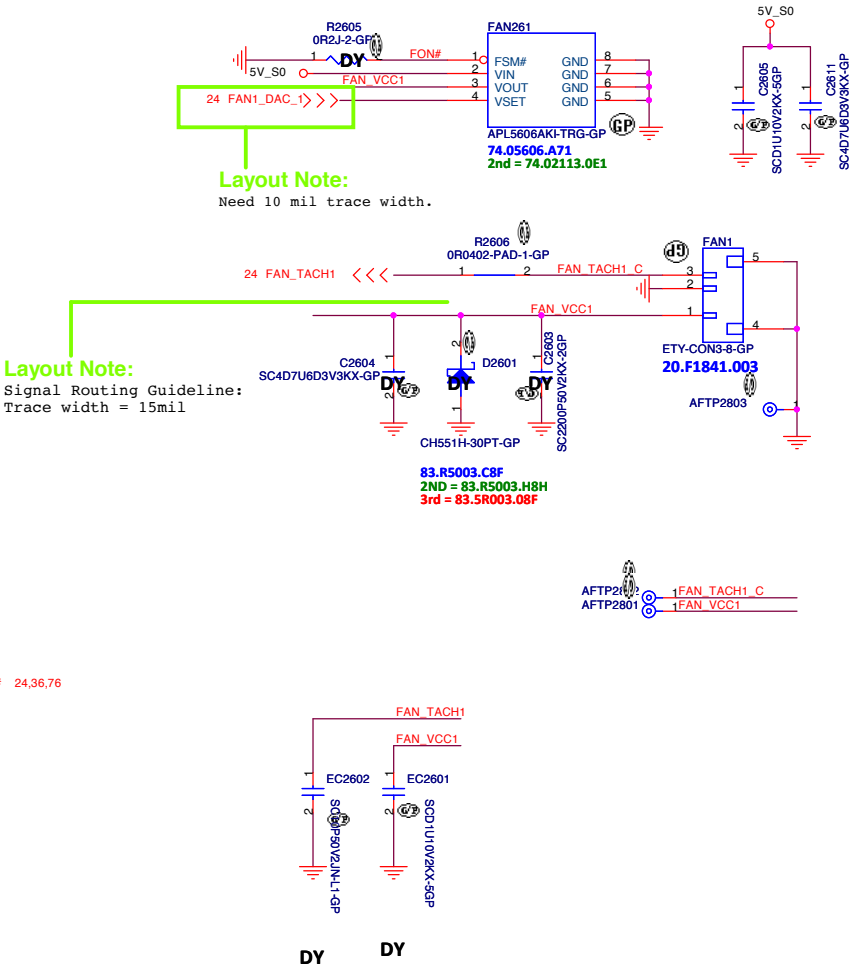
Title: Flash/RTC		
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Thursday, April 25, 2013	Sheet 25 of 104	

SSID = Thermal



Fan controller1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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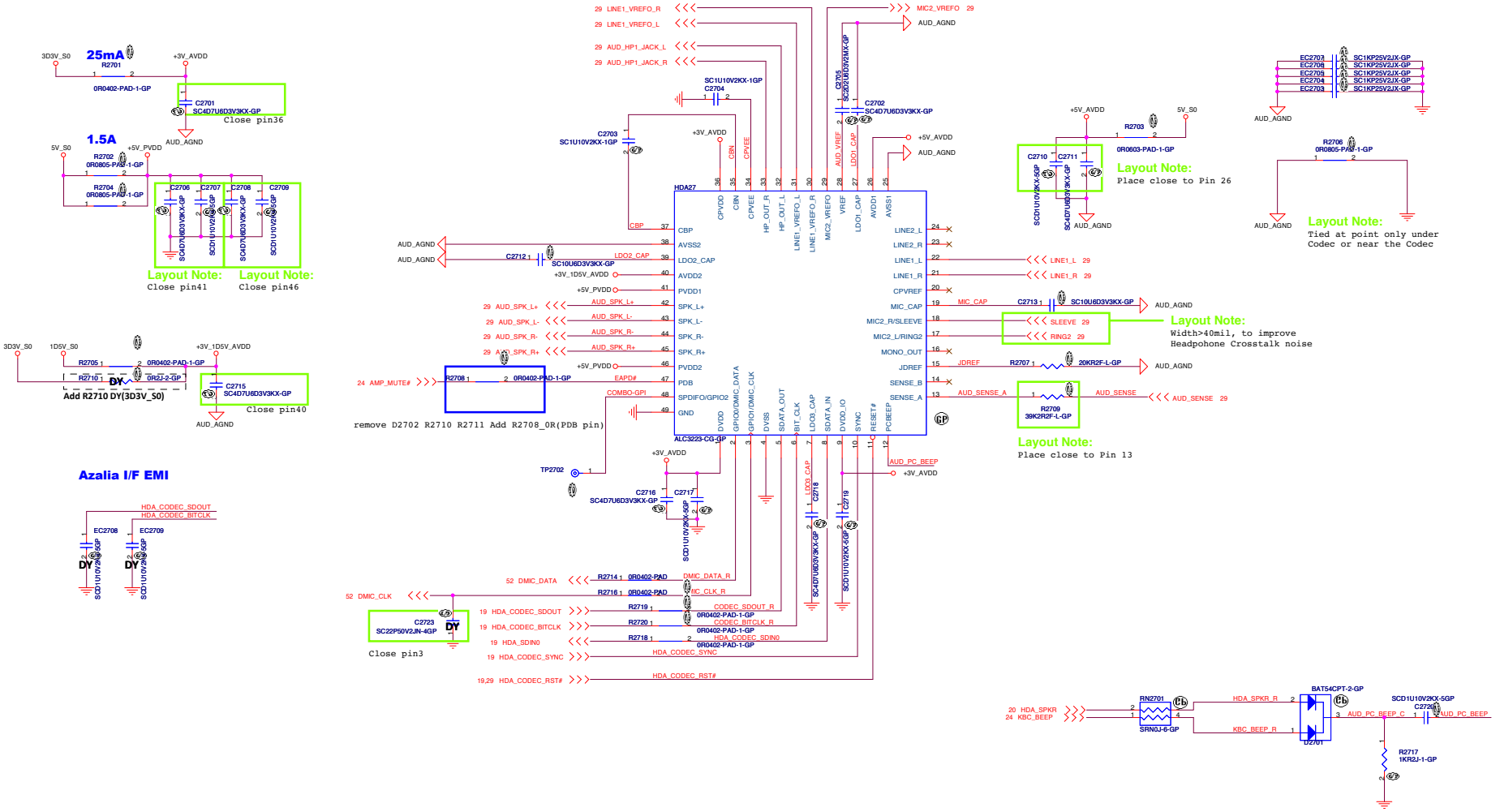
Title: Reserved

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Wednesday, April 17, 2013 | Sheet 26 of 104

SSID = AUDIO


25mA
1.5A
Close pin36
Close pin41
Close pin46
Close pin40
Add R2710 DY(3D3V_S0)
Azalia I/F EMI
HDA27
ALC3223-CG-GP
remove D2702 R2710 R2711 Add R2708_0R(PDB pin)
Close pin3
Layout Note:
Place close to Pin 26
Layout Note:
Tied at point only under Codec or near the Codec
Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Layout Note:
Place close to Pin 13
Wistron Corporation
Audio Codec ALC3221
OAK14 Haswell
X00

(Blanking)

<Core Design>

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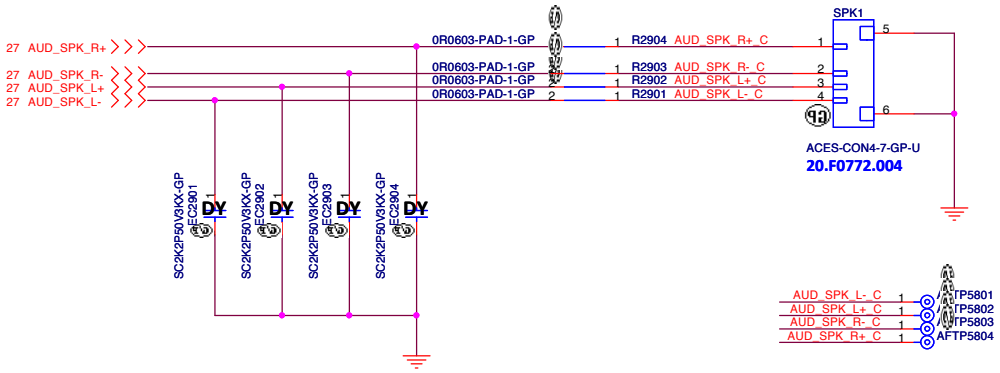
Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 28 of 104

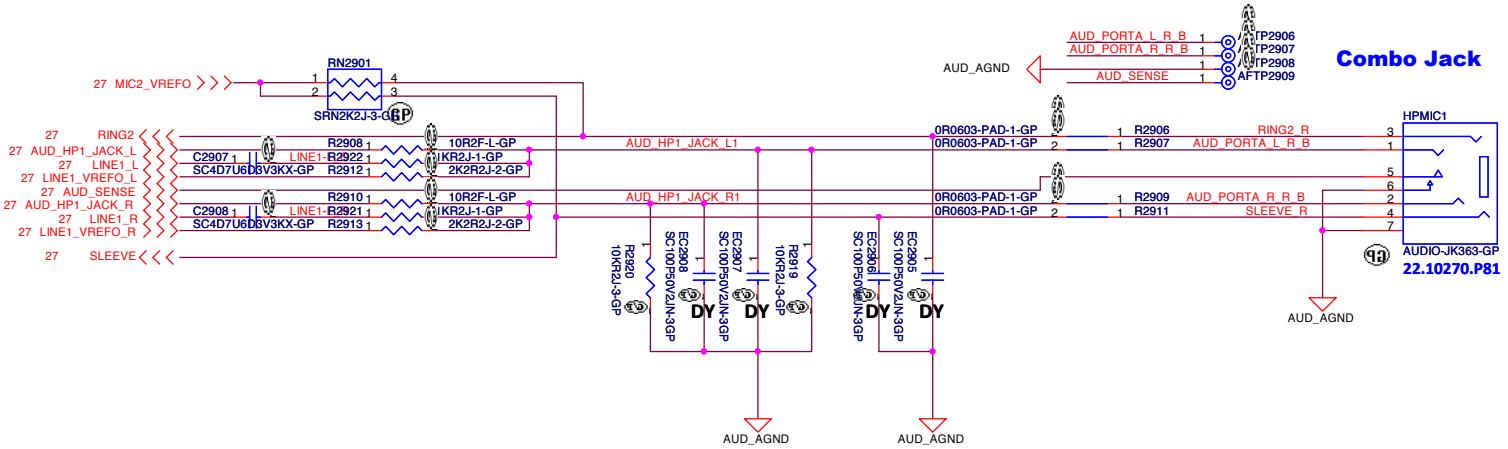
SSID = AUDIO

Speaker

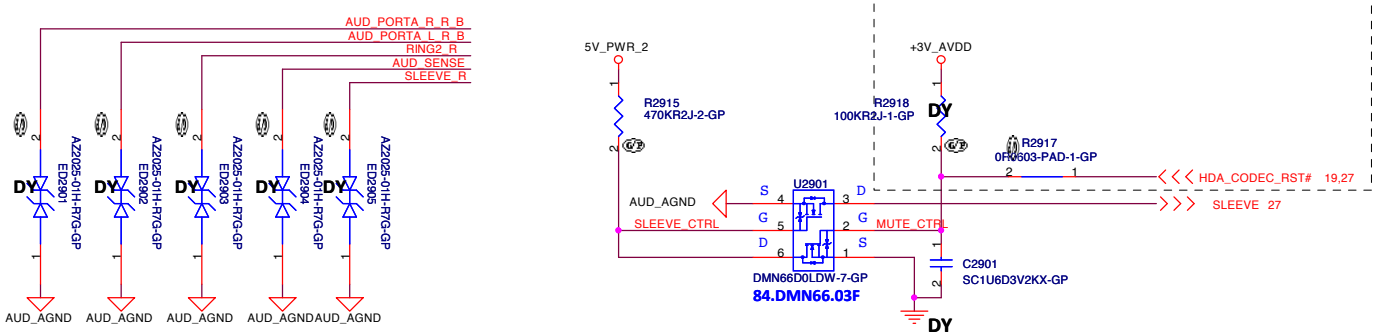


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Combo Jack



1227 modify



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal NCT7718W/Fan Controllor P2793*

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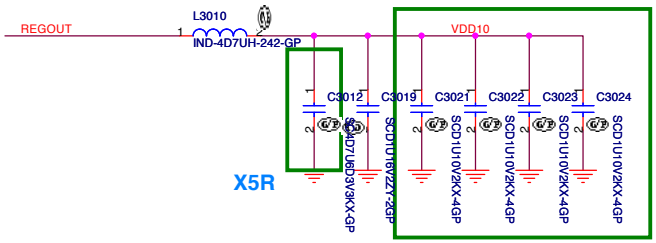
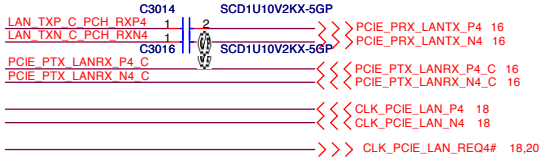
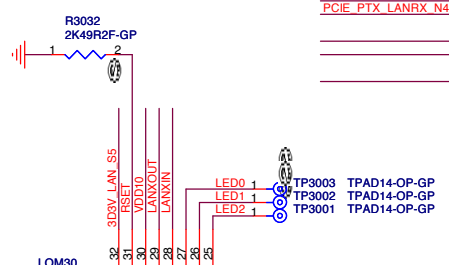
Date: Friday, April 12, 2013 Sheet 29 of 104

LAN CHIP

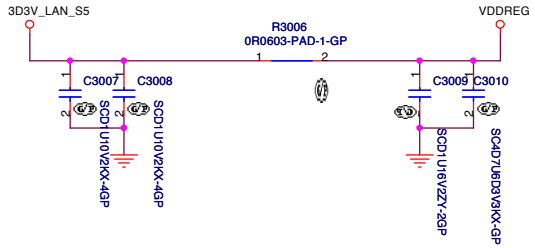
10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30

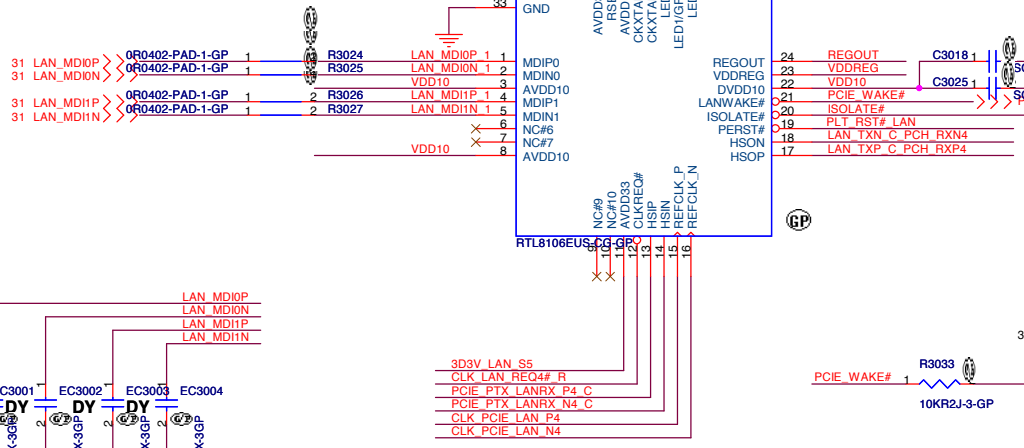


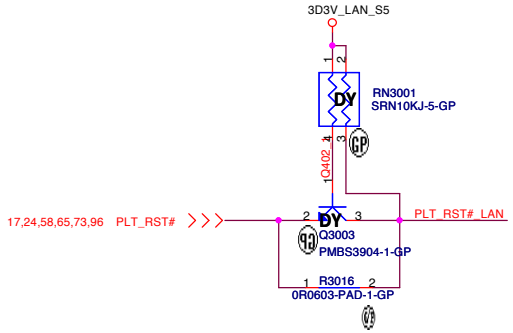


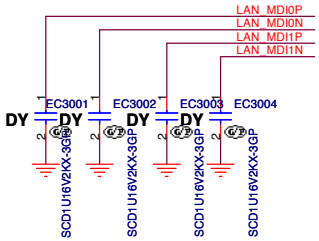


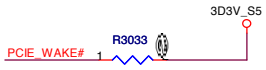
40 mils



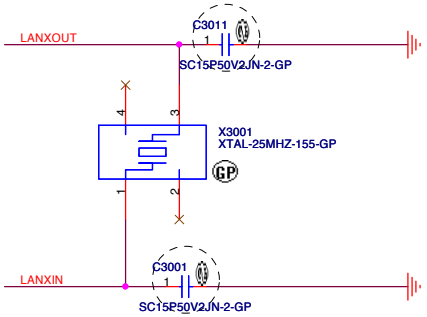


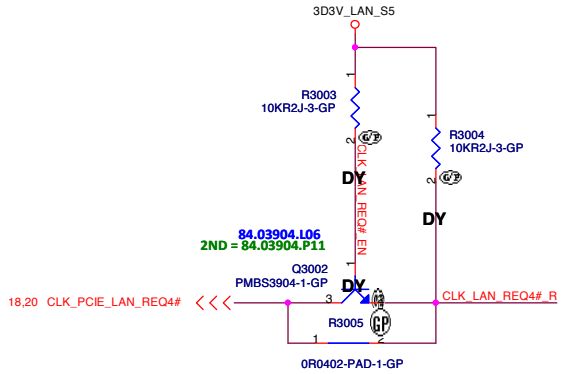




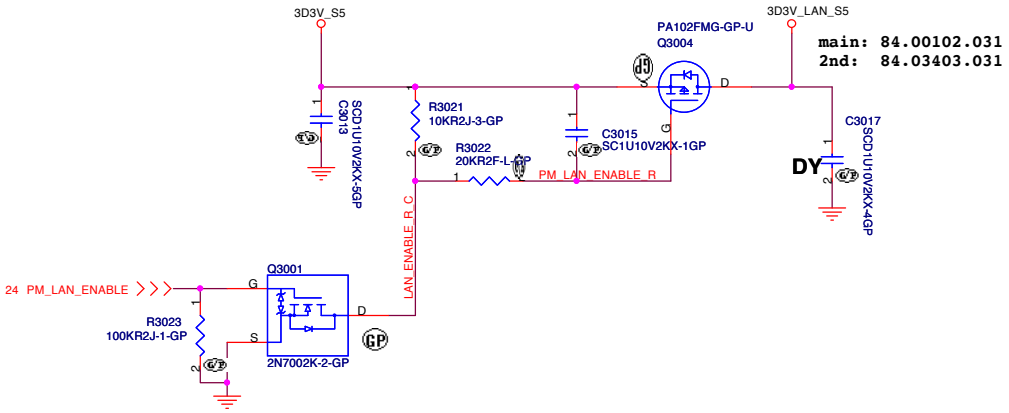


X01 3/7 Change value from test report





251mA



<Core Design>

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Title: LOM

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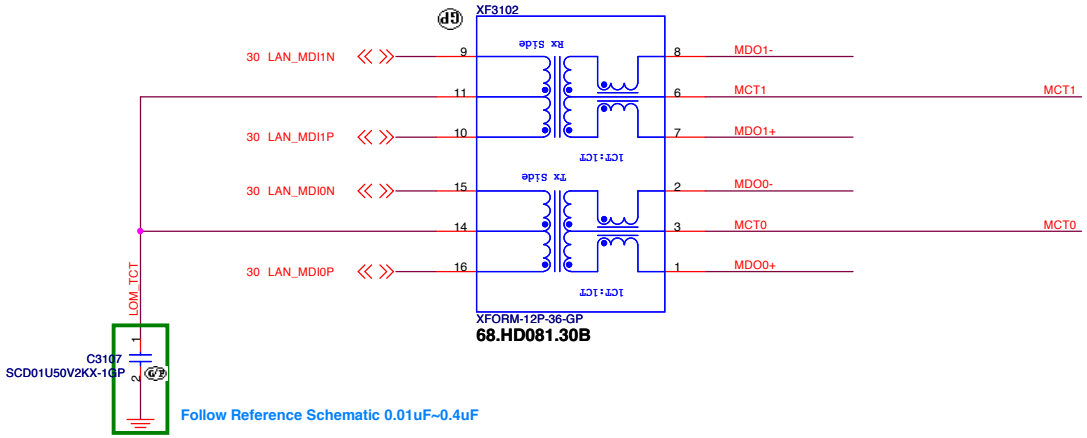
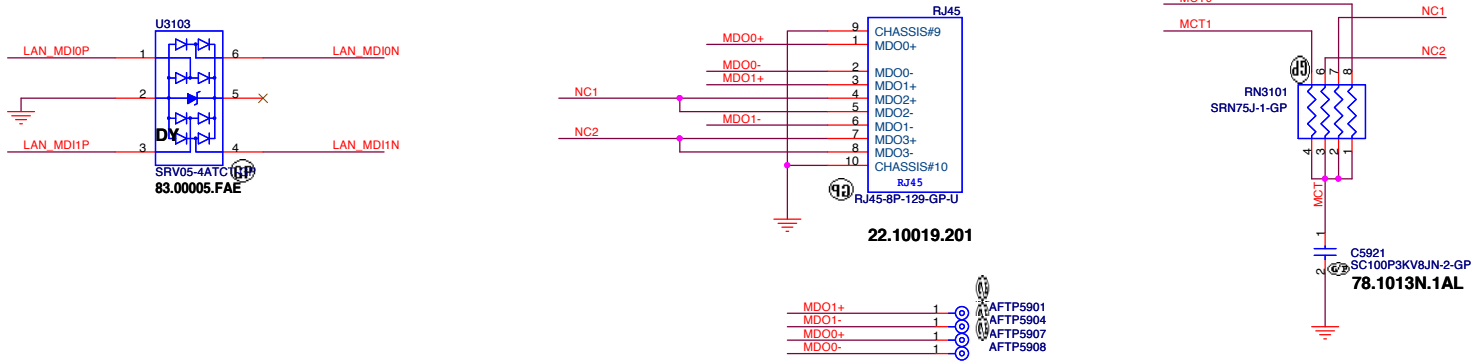
Date: Wednesday, April 17, 2013 Sheet 30 of 104

SSID = LOM

10/100 LAN TransFormer



RJ45 CONN



<Core Design>

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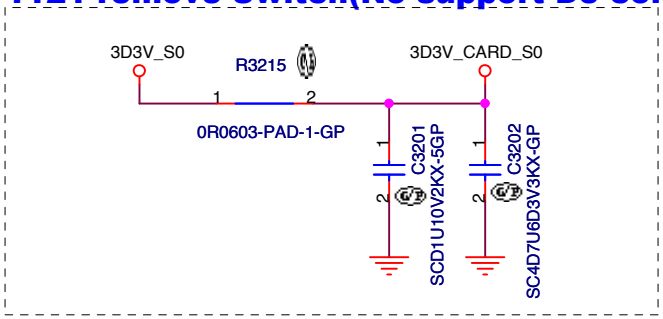
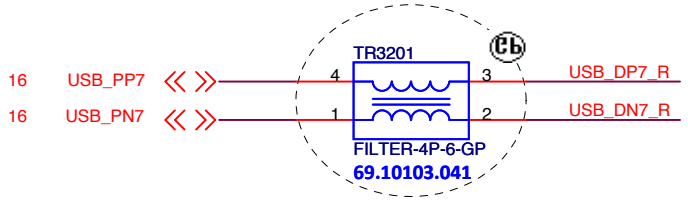
Title	XFOM&RJ45	
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Monday, April 15, 2013	Sheet 31 of 104	

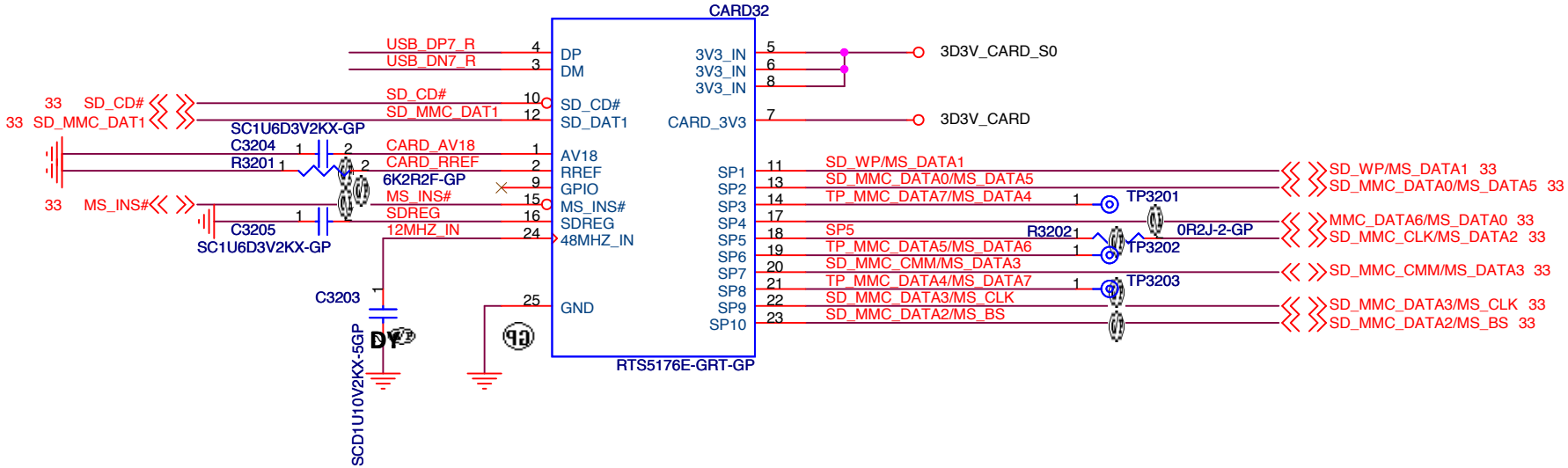
1121 remove Switch(No support D3 cold)





A00 4/10 Add TR3201

Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



<Core Design>

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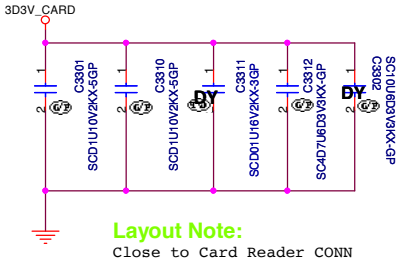
Title: **Card Reader-RTS5176**

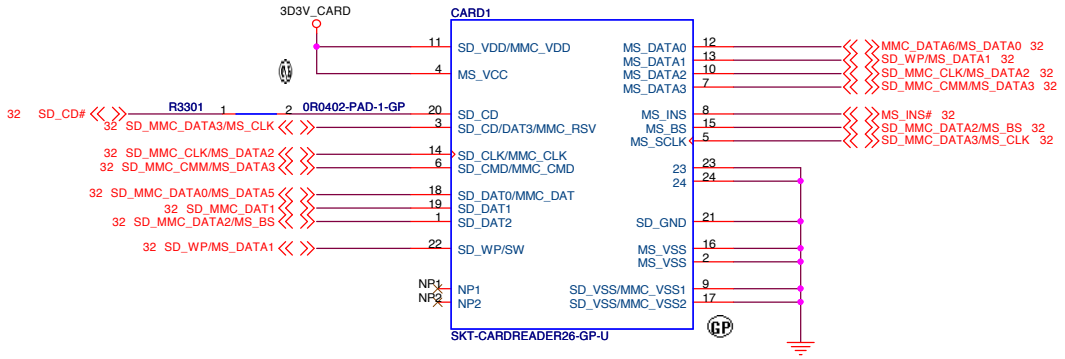
Size	Document Number	Rev
A4	OAK14 Haswell	X00

Date: Wednesday, April 17, 2013 Sheet 32 of 104

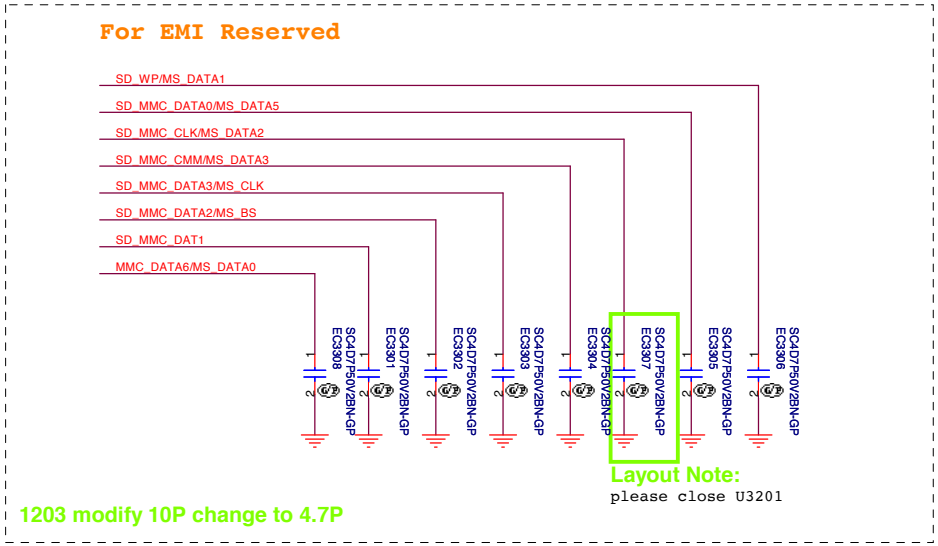
SSID = SDIO



SD/MS/MMC Card Connector



62.10051.C21



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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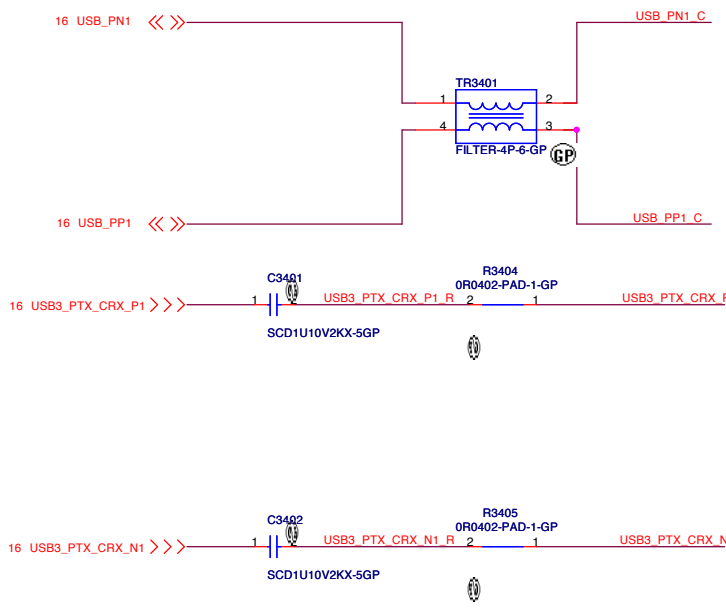
Title: SD/XD/MS/MMC Card CONN

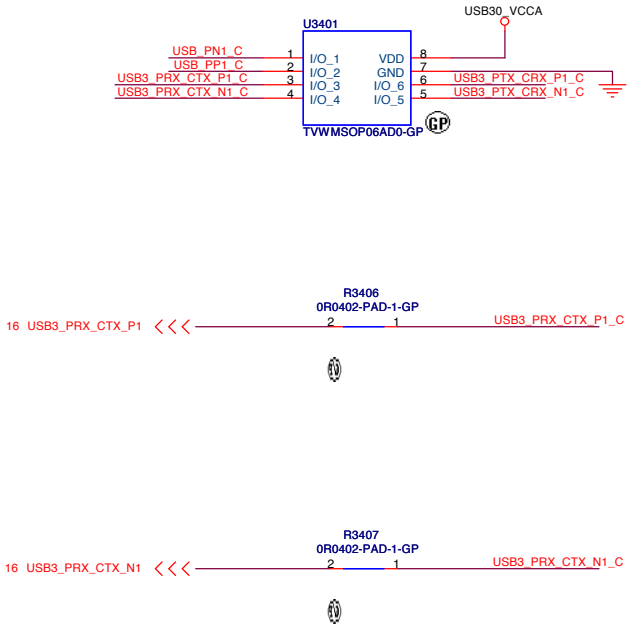
Size	Document Number	Rev
A3	OAK14 Haswell	X00

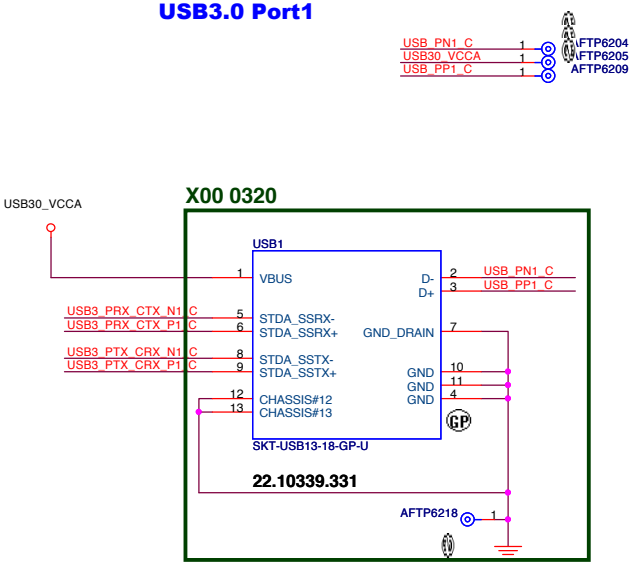
Date: Tuesday, April 16, 2013 Sheet 33 of 104

SSID = USB

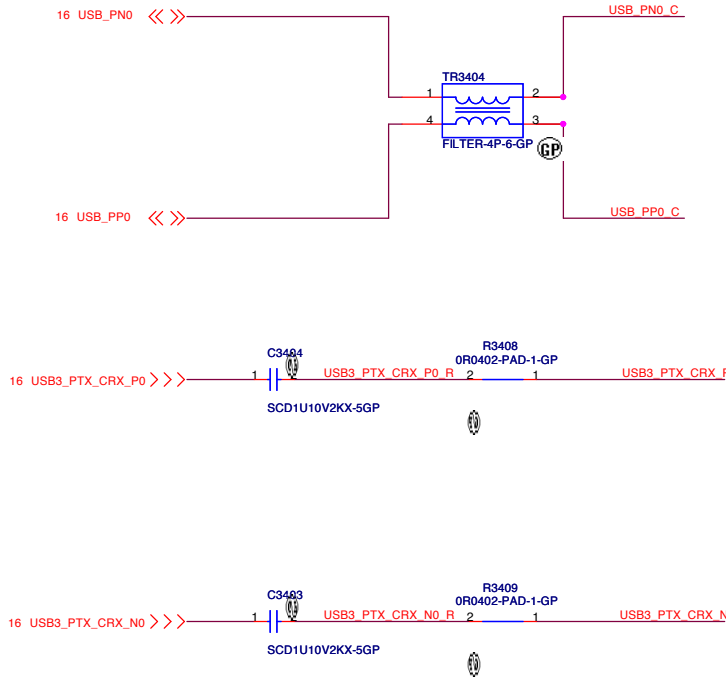
USB3.0 Port1

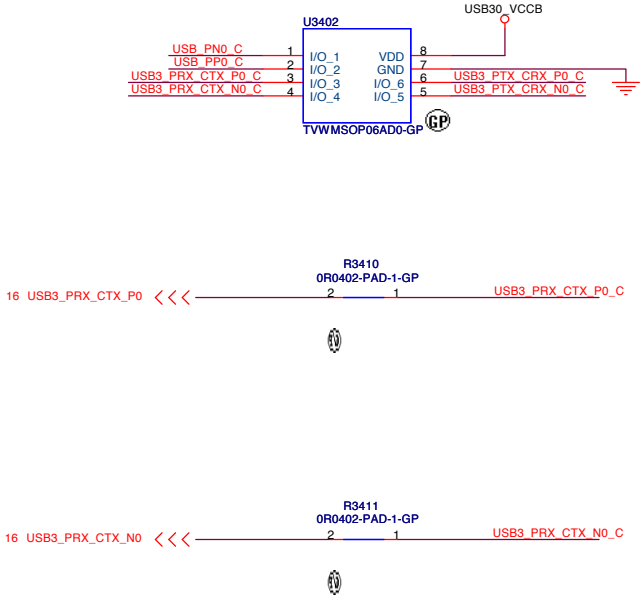


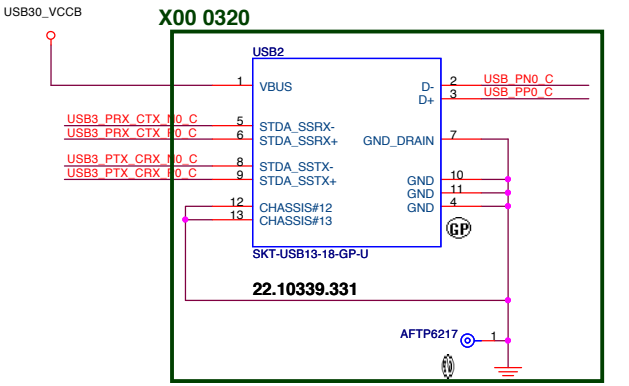




USB3.0 Port2



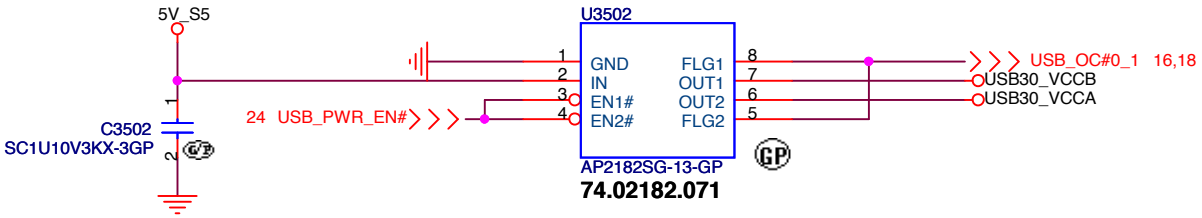


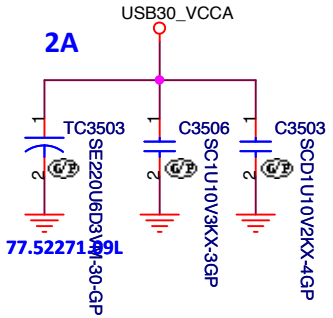


<Core Design>

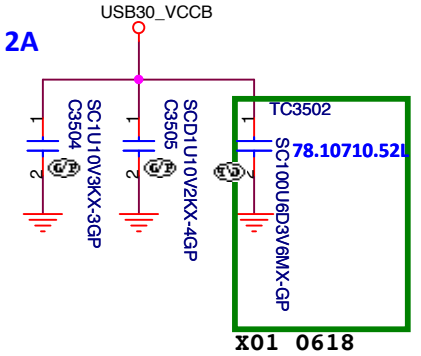
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB 3.0		
Size: A3	Document Number: OAK14 Haswell	Rev: X00
Date: Friday, April 12, 2013	Sheet 34 of 104	



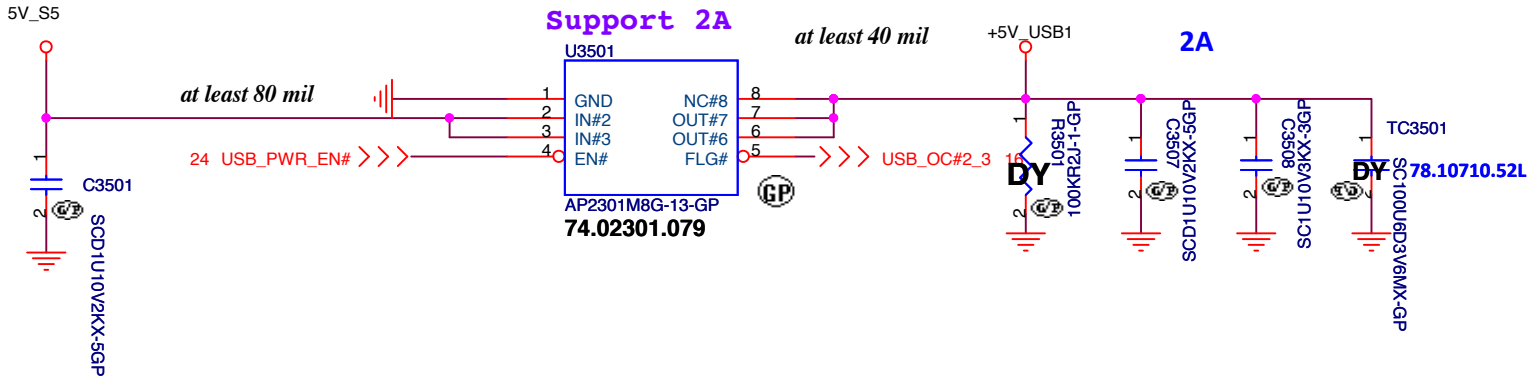


USB3.0 Port1



USB3.0 Port2

Right USB Power x1



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

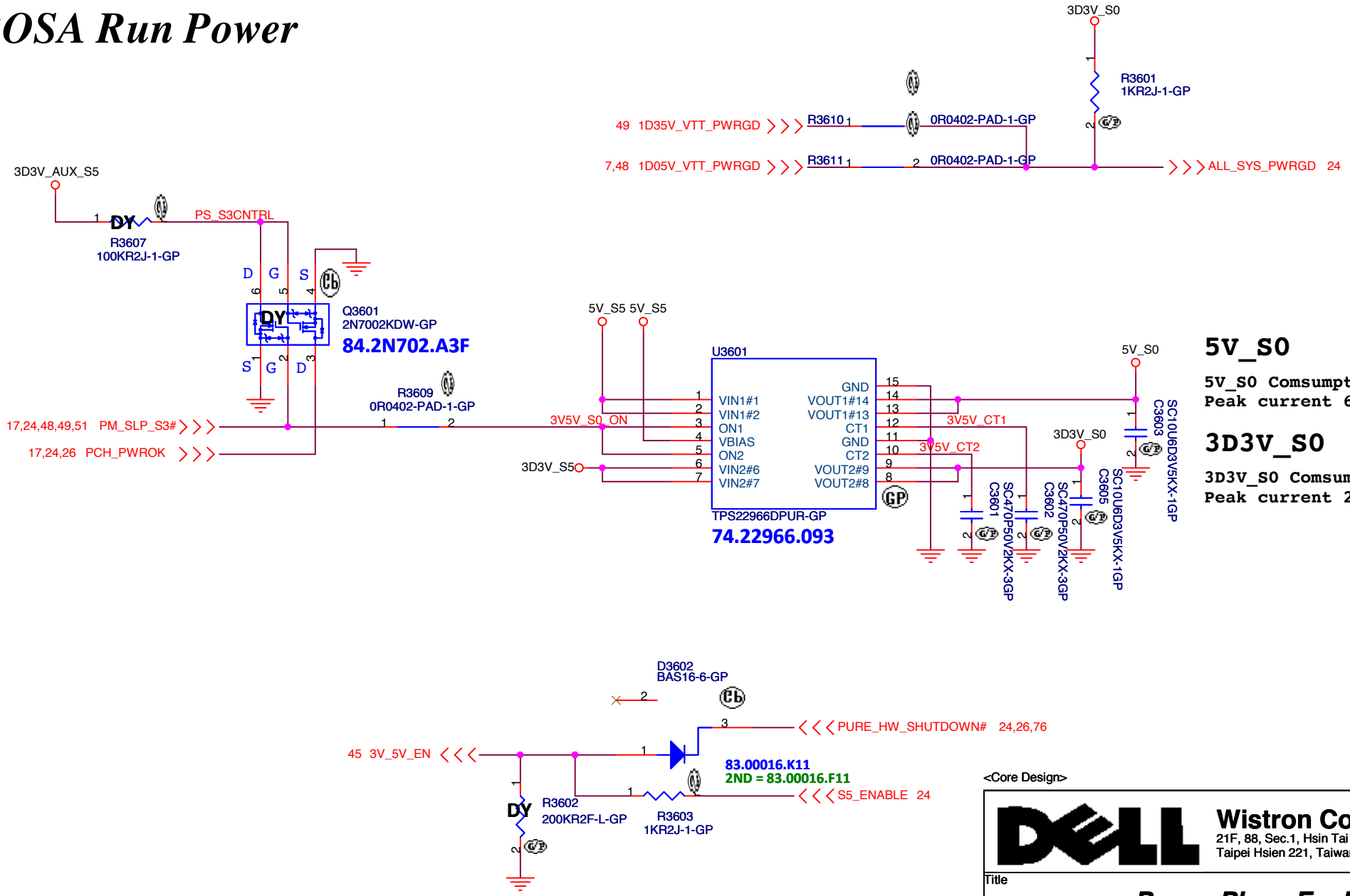
Size	Document Number	Rev
	OAK14 Haswell	***X00***

Date: Monday, April 15, 2013 Sheet 35 of 104

SSID = Reset.Suspend

ROSA Run Power

Power Good



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A4	OAK14 Haswell	X00

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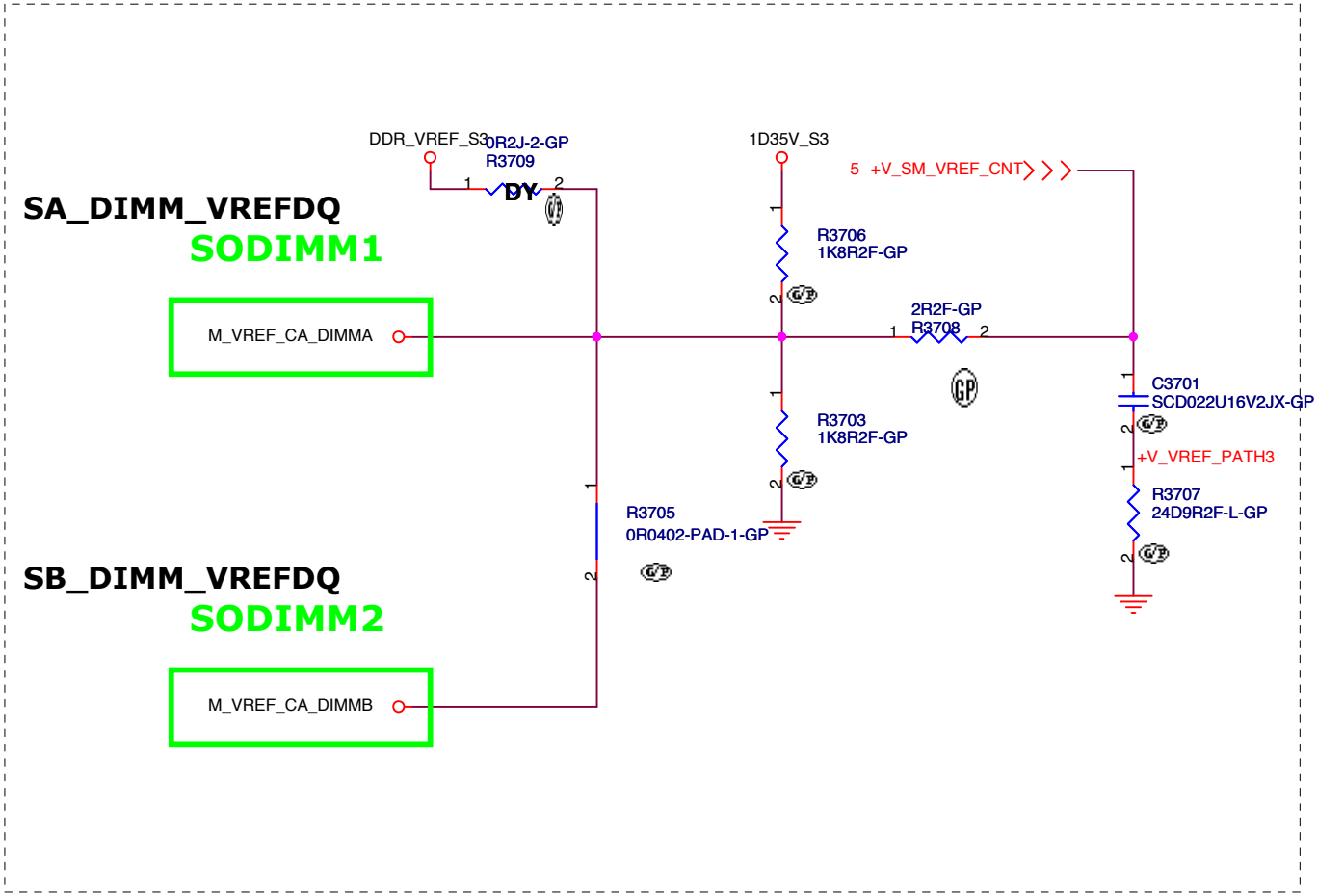
Layout Note:
Place Close SO-DIMM



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
S3 Reduction Circuit

Size	Document Number	Rev
A4	OAK14 Haswell	X00

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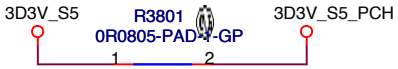
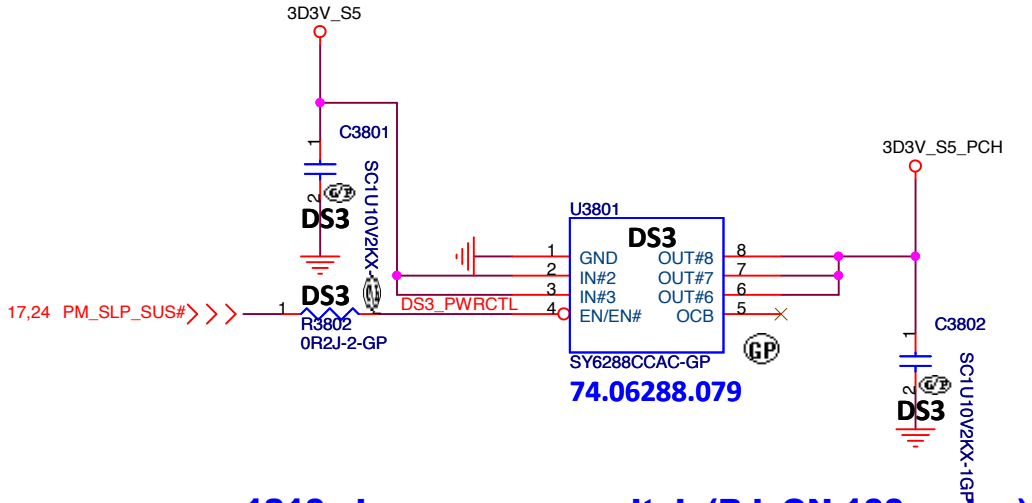


Non DS3



1210 change power switch (RdsON:100m ohm)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DSW***	
Size: A4	Document Number: ***OAK14 Haswell***	Rev: ***X00***
Date: Wednesday, April 17, 2013	Sheet 38 of 104	

SSID = CPU

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (POWER1)

Size	Document Number	Rev
Custom	*OAK14 Haswell*	*X00*

Date: Thursday, January 10, 2013 Sheet 39 of 104

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 40 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 41 of 104

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

DT MODE

Title	DCIN
Size	A3
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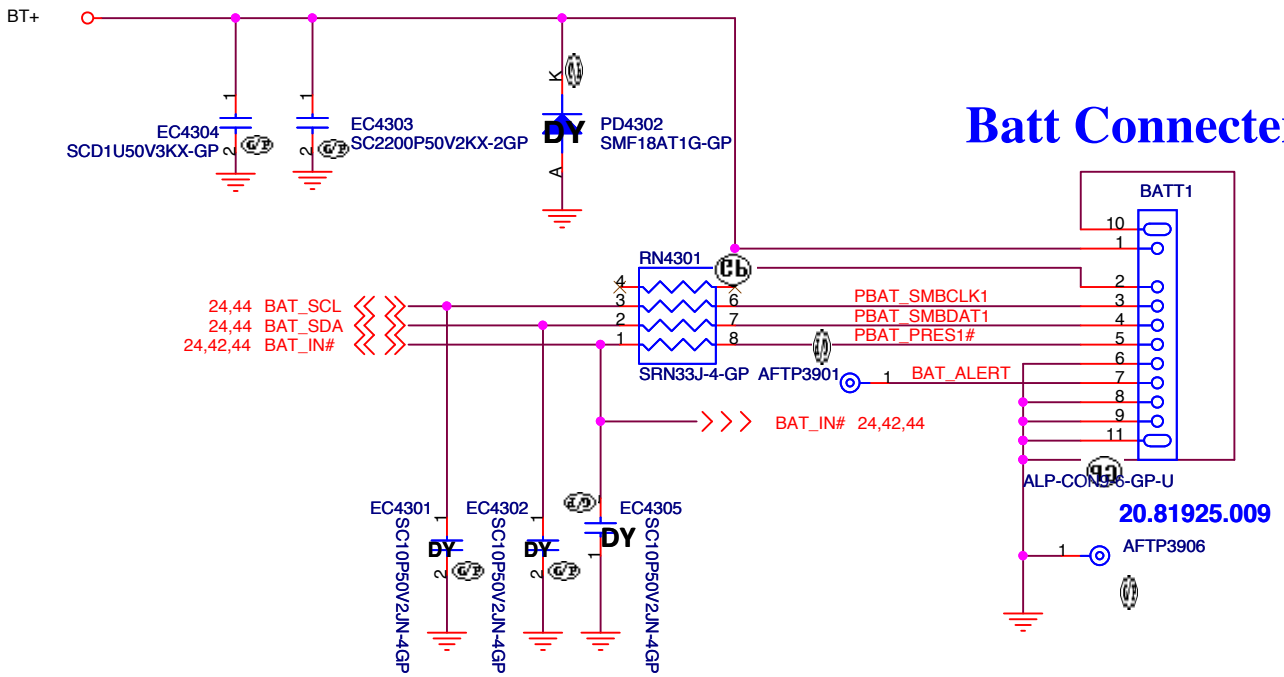
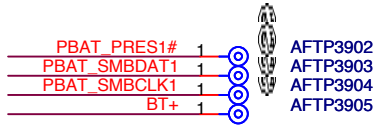
Sheet	42 of 104

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

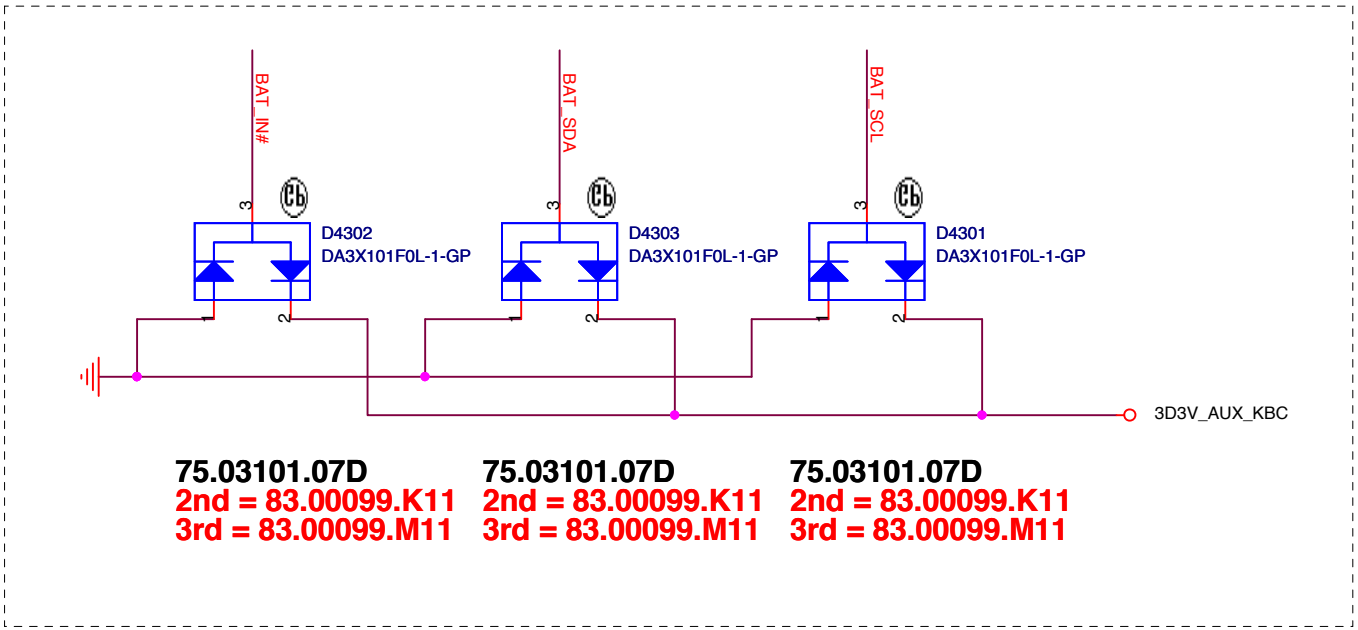
<Core Design>

SSID = PWR.Support





Placement: Close to Batt Connector



75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

<Core Design>

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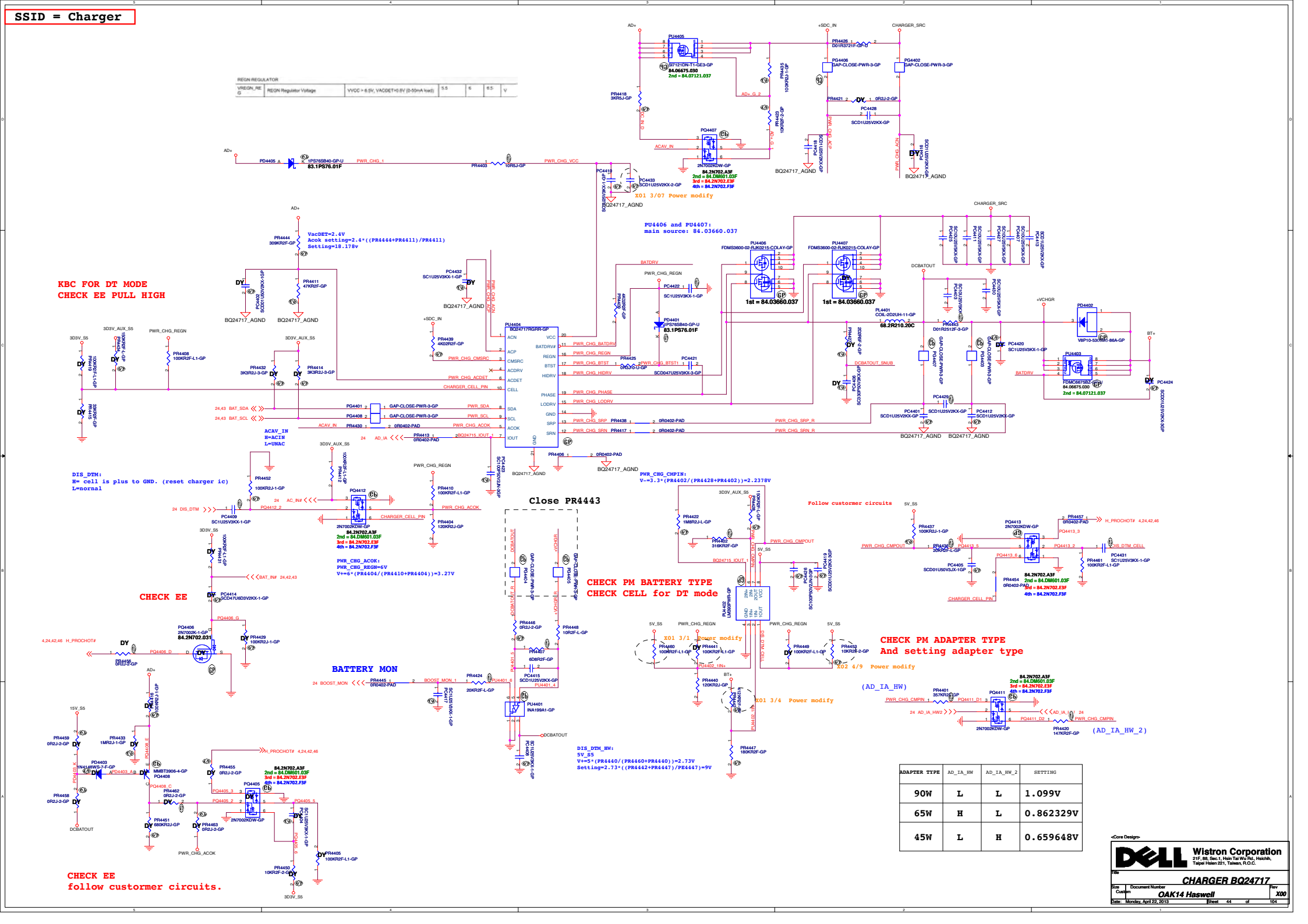
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	OAK14 Haswell	X00

Date: Thursday, March 07, 2013 Sheet 43 of 104

SSID = Charger



REGN REGULATOR						
VREGN_REG	REGN Regulator Voltage	VVCC > 6.5V, VACDET=0.6V (0-50mA load)	5.5	6	6.5	V

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

<Core Design>

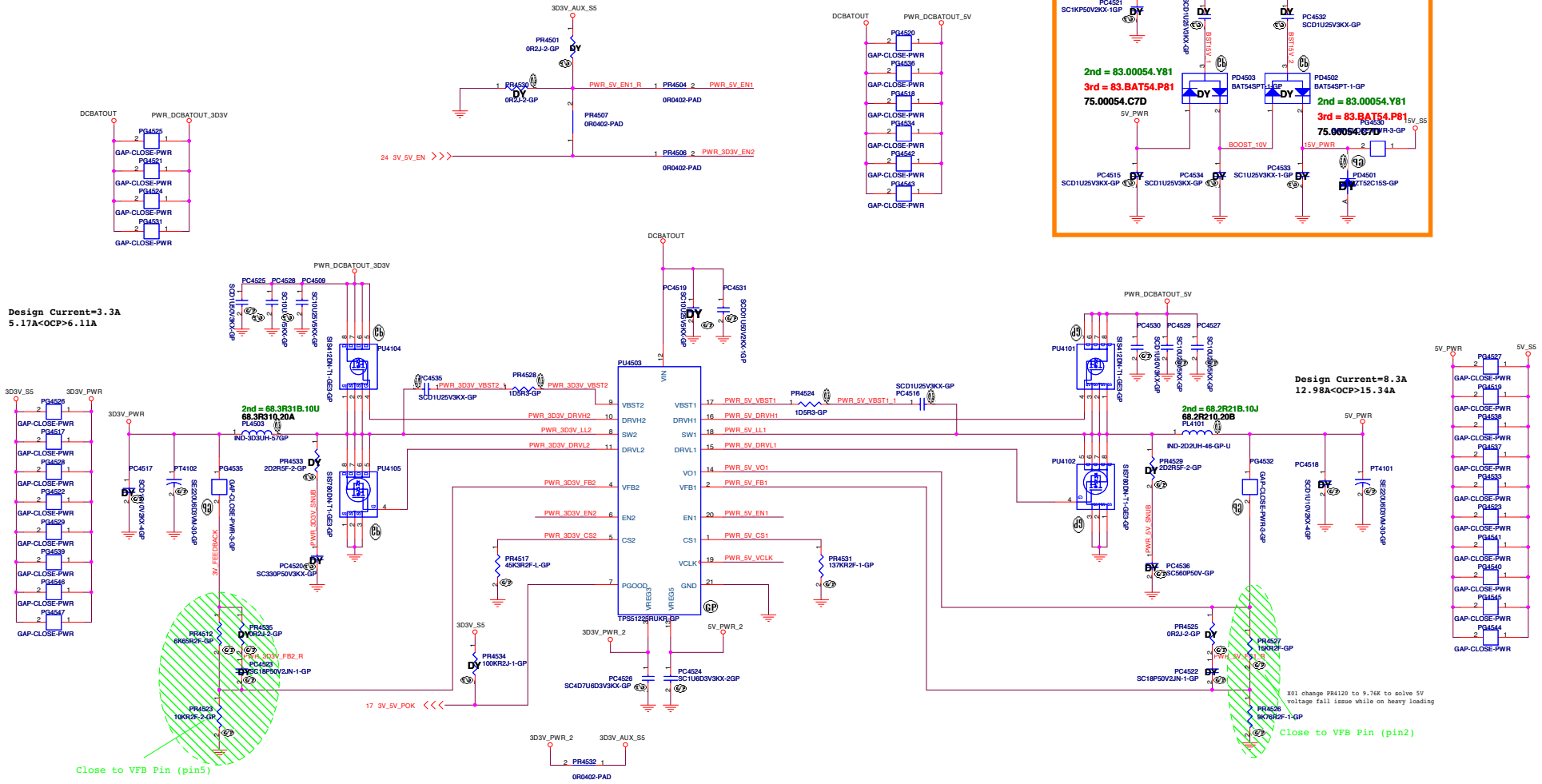
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24717

Size: Custom | Document Number: OAK14 Haswell | Rev: X00

Date: Monday, April 22, 2013 | Sheet 44 of 104

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

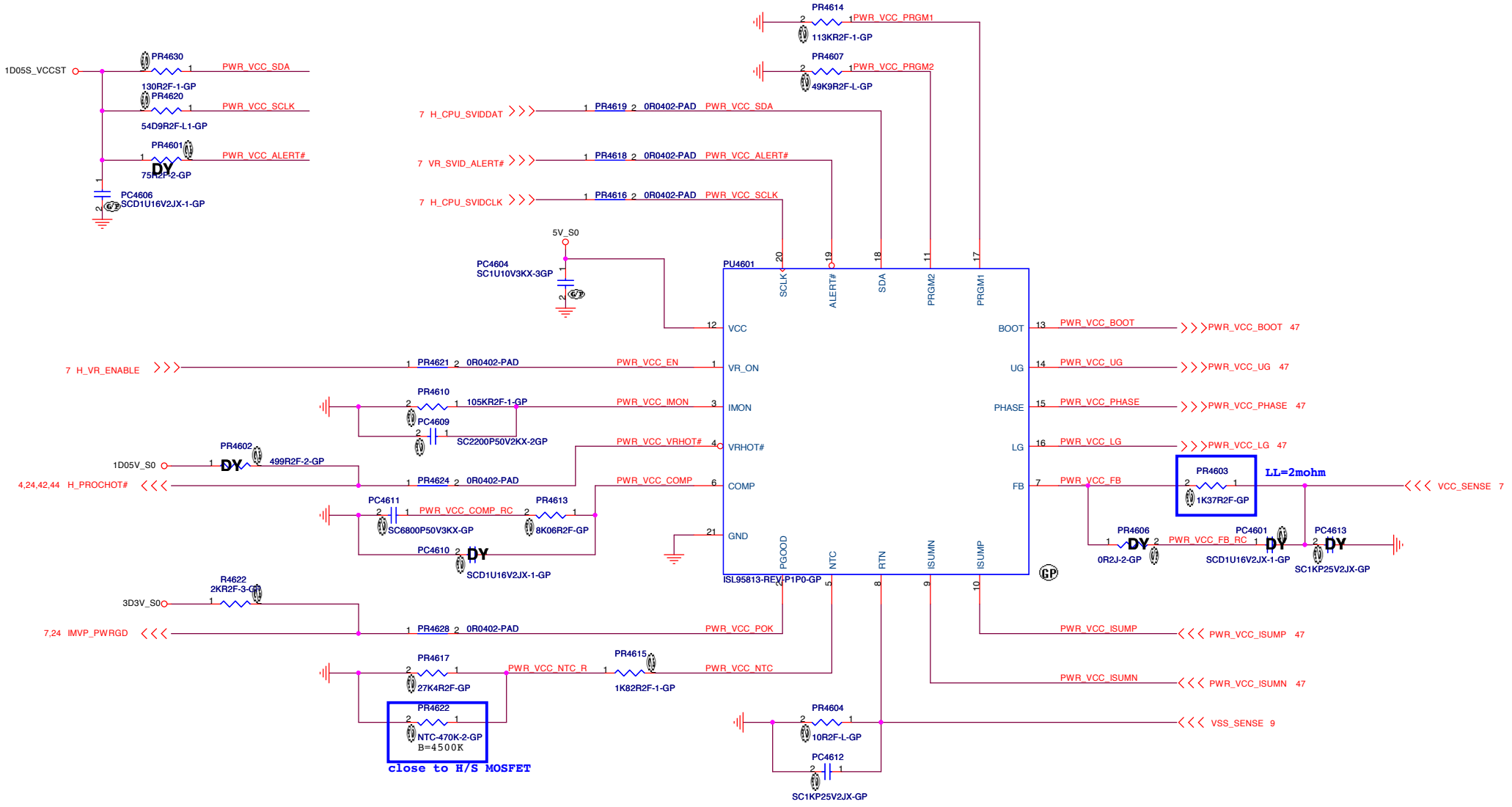
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size: A2 | Document Number: OAK14 Haswell | Rev: X00

Date: Tuesday, April 16, 2013 | Sheet 45 of 104

SSID = CPU.Regulator



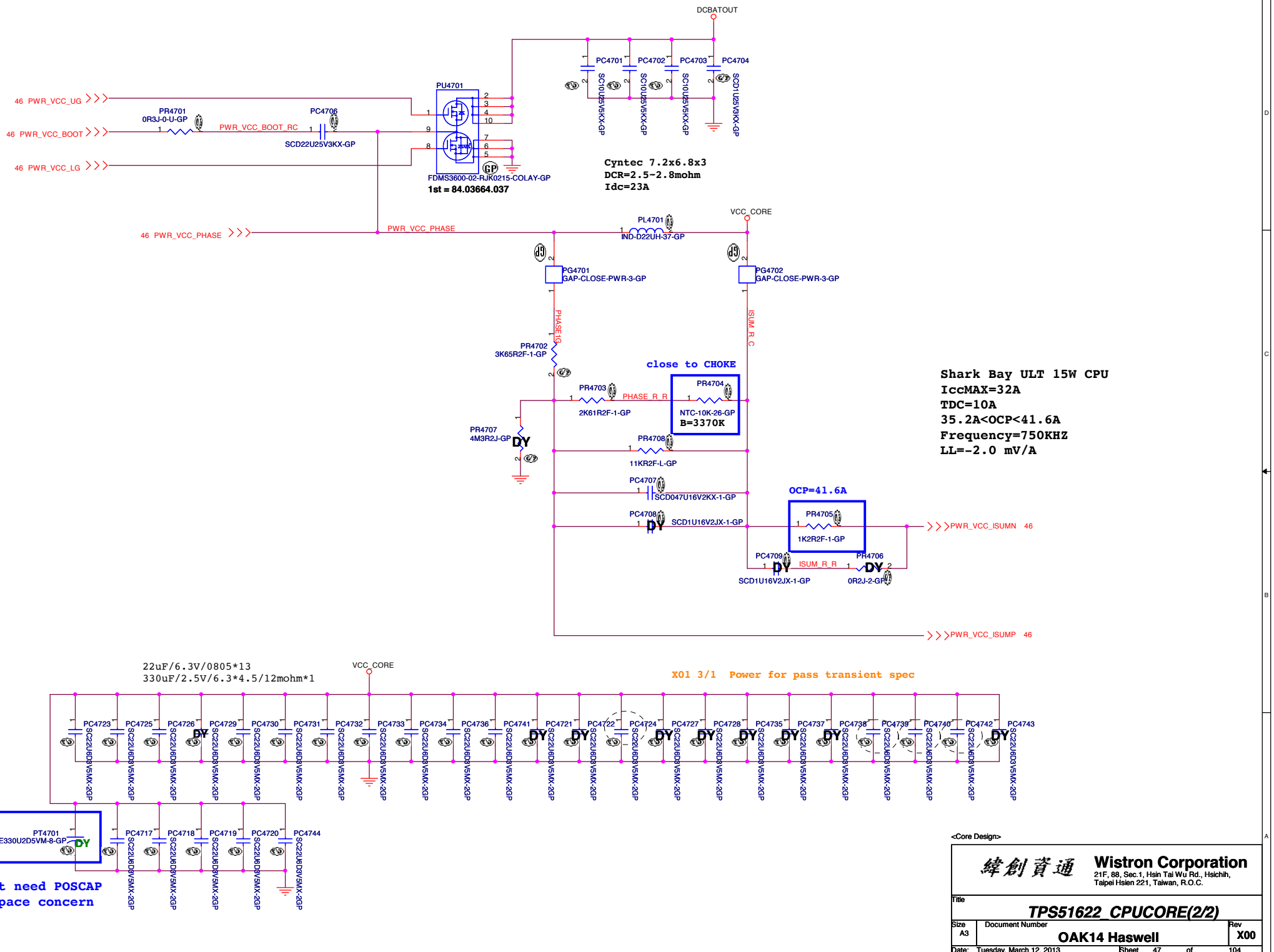
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

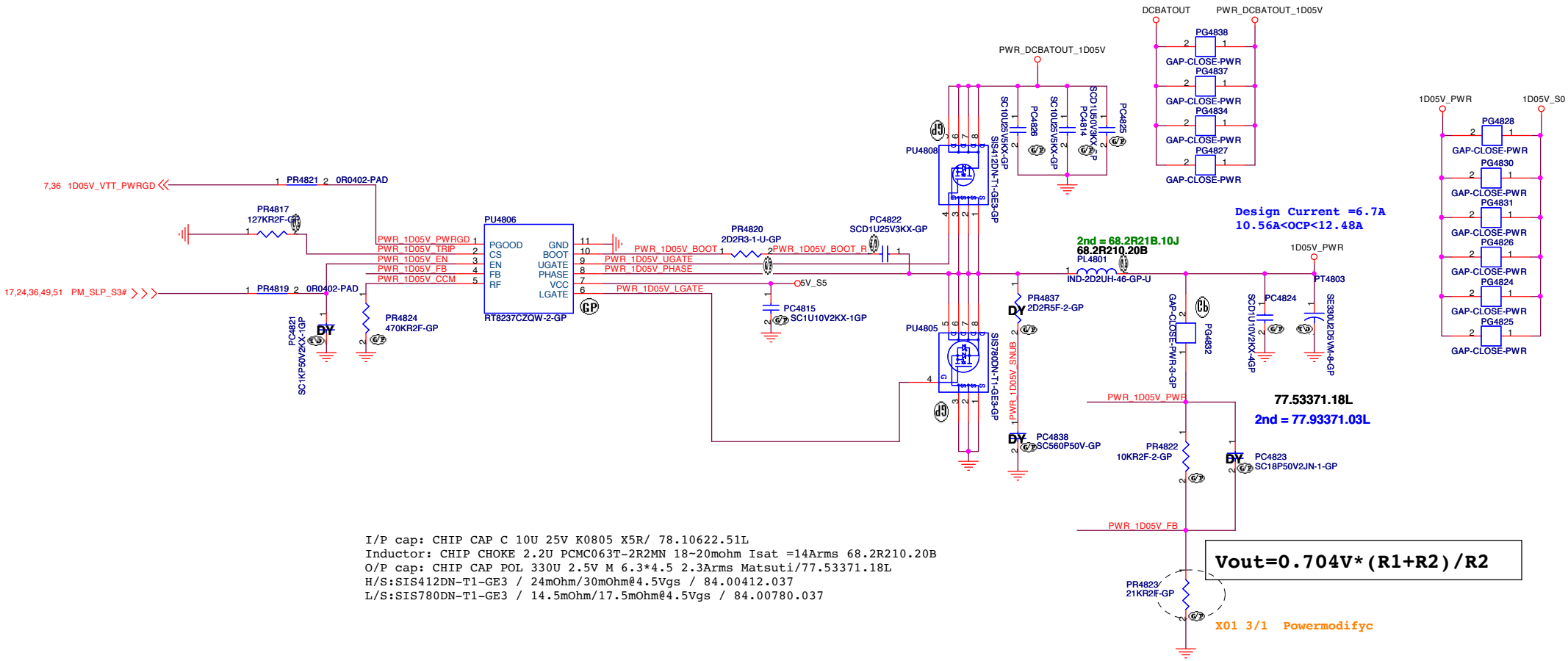
Title: TPS51622_CPUCORE(1/2)

Size	Document Number	Rev
A3	OAK14 Haswell	X00

Date: Thursday, April 18, 2013 Sheet 46 of 104


DCBATOUT
PC4701
PC4702
PC4703
PC4704
SC10U25V5KX-GP
SCD1U25V3KX-GP
PU4701
46 PWR_VCC_UG
46 PWR_VCC_BOOT
46 PWR_VCC_LG
PR4701
0R3J-0-U-GP
PWR_VCC_BOOT_RC
PC4706
SCD22U25V3KX-GP
FDMS3600-02-RJK0215-COLAY-GP
1st = 84.03664.037
Cyntec 7.2x6.8x3
DCR=2.5-2.8mohm
Idc=23A
46 PWR_VCC_PHASE
PWR_VCC_PHASE
PL4701
IND-D22UH-37-GP
VCC_CORE
PG4701
GAP-CLOSE-PWR-3-GP
PG4702
GAP-CLOSE-PWR-3-GP
PHASE1G
ISUM_R_C
PR4702
3K65R2F-1-GP
close to CHOKE
PR4703
PHASE_R_R
2K61R2F-1-GP
PR4704
NTC-10K-26-GP
B=3370K
PR4707
4M3R2J-GP
DY
PR4708
11KR2F-L-GP
PC4707
SCD047U16V2KX-1-GP
PC4708
SCD1U16V2JX-1-GP
OCP=41.6A
PR4705
1K2R2F-1-GP
PWR_VCC_ISUMN 46
PC4709
ISUM_R_R
PR4706
0R2J-2-GP
PWR_VCC_ISUMP 46
Shark Bay ULT 15W CPU
IccMAX=32A
TDC=10A
35.2A<OCP<41.6A
Frequency=750KHZ
LL=-2.0 mV/A
22uF/6.3V/0805*13
330uF/2.5V/6.3*4.5/12mohm*1
VCC_CORE
X01 3/1 Power for pass transient spec
PC4723
PC4725
PC4726
PC4729
PC4730
PC4731
PC4732
PC4733
PC4734
PC4736
PC4741
PC4721
PC4722
PC4724
PC4727
PC4728
PC4735
PC4737
PC4738
PC4739
PC4740
PC4742
PC4743
SC22U6D3V5MX-2GP
PT4701
SE330U2D5VM-8-GP
PC4717
PC4718
PC4719
PC4720
PC4744
SC22U6D3V5MX-3GP
Don't need POSCAP
If space concern
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51622_CPUCORE(2/2)
Size
A3
Document Number
OAK14 Haswell
Rev
X00
Date: Tuesday, March 12, 2013
Sheet 47 of 104

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

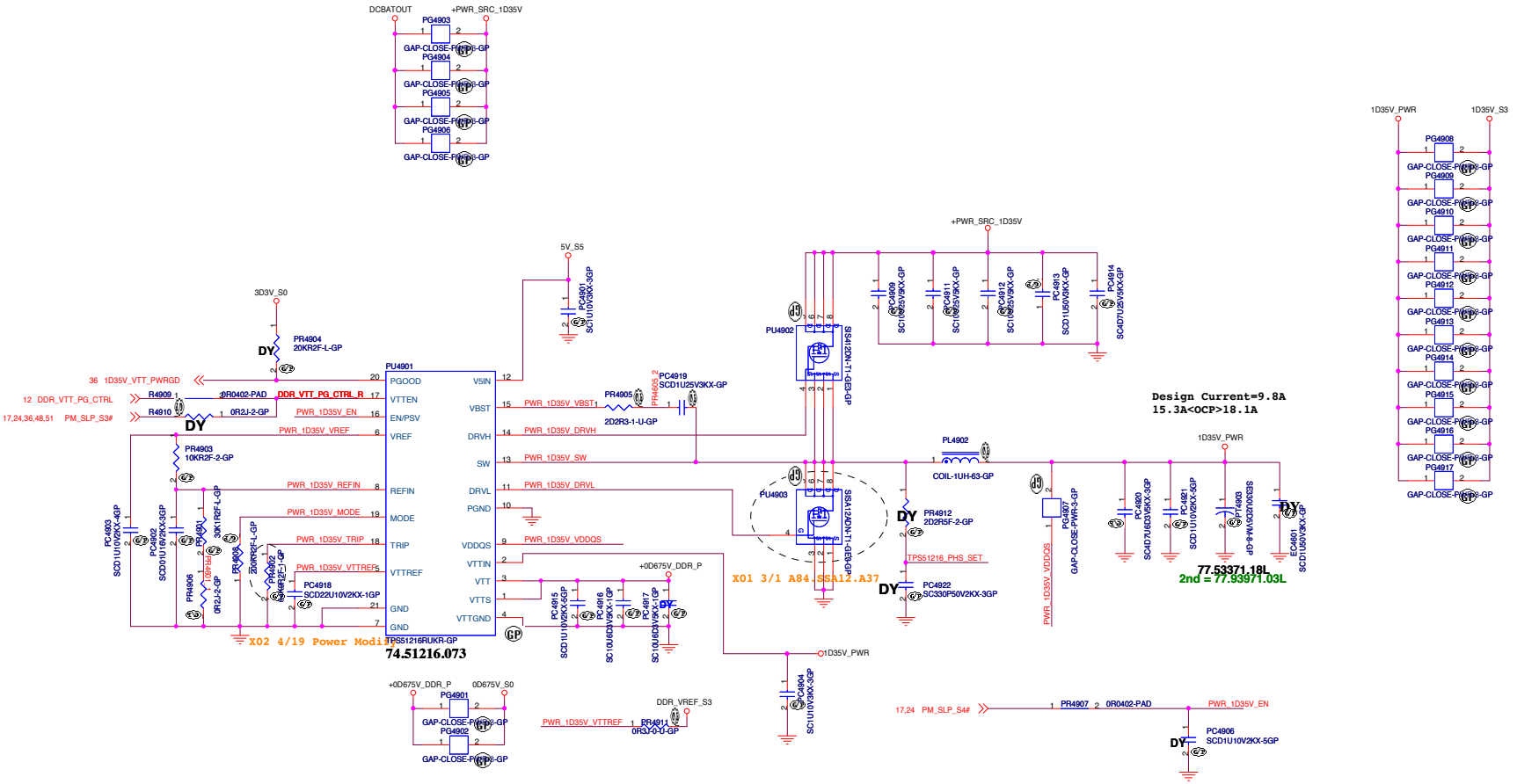
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51367_1D05V***

Size	Document Number	Rev
A3		X00

Date: Monday, April 15, 2013 Sheet 48 of 104

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5~1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24~30mohm @Vgs=4.5V
L/S MOS: FET MOS SIS780DN-T1-GE3 NC POWERPAK 121 / 84.00780.037 / Rds(on)=14.5~17.5mohm @Vgs=4.5V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51367+51206 1D35V & 0D675V

Size: C | Document Number: OAK14 Haswell | Rev: X00

Date: Friday, April 19, 2013 | Sheet 49 of 104

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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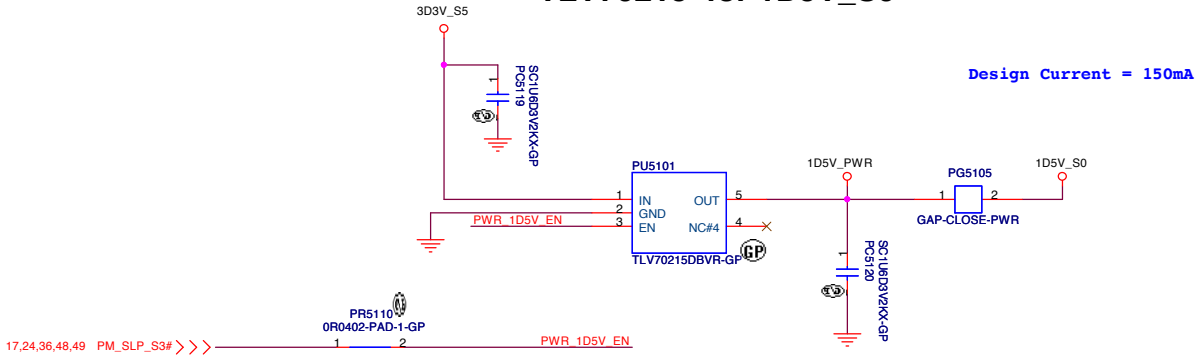
Title: *Reserved*

Size	Document Number	Rev
A3	*OAK14 Haswell*	*X00*

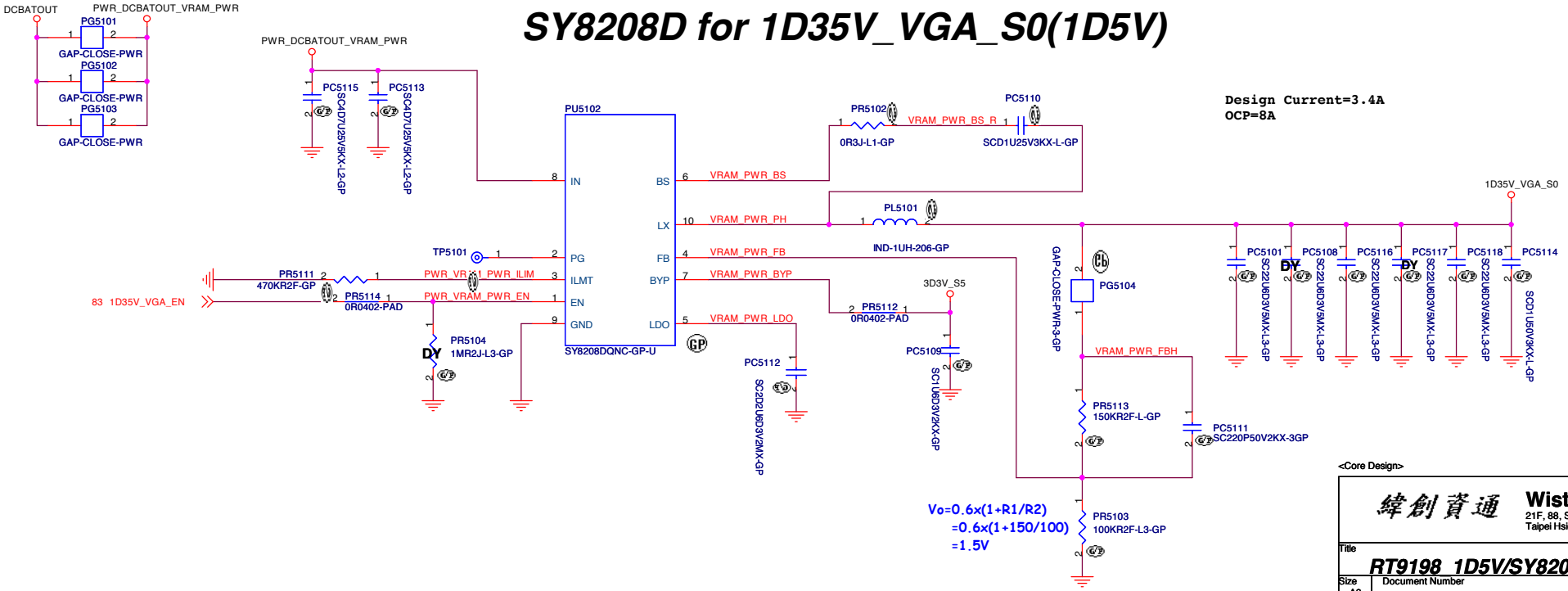
Date: Thursday, January 10, 2013 Sheet 50 of 104

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



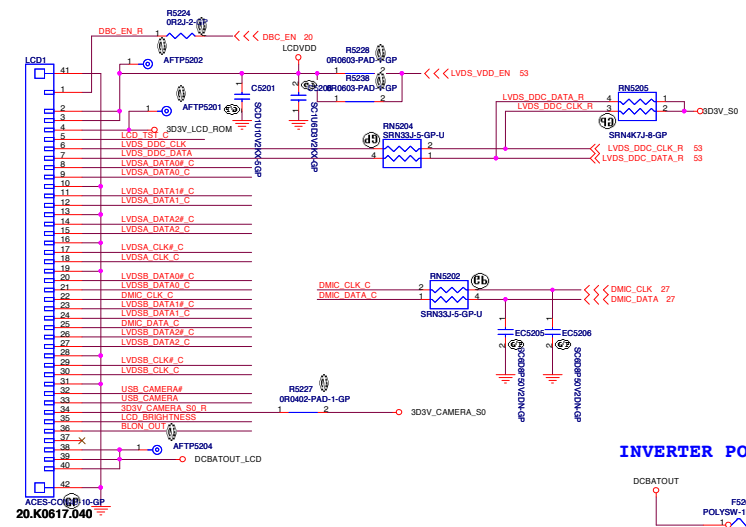
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9198_1D5V/SY8208D_1D5V(VGA)

Size	Document Number	Rev
A3	OAK14 Haswell	X00

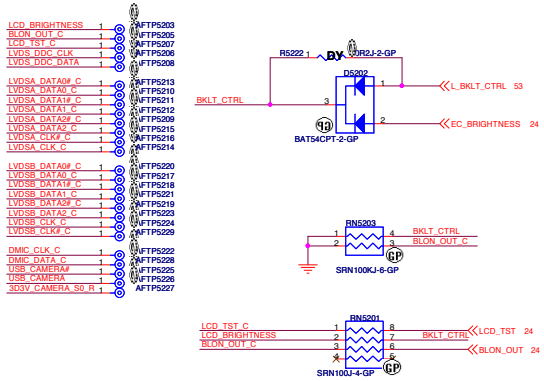
Date: Friday, April 19, 2013 Sheet 51 of 104



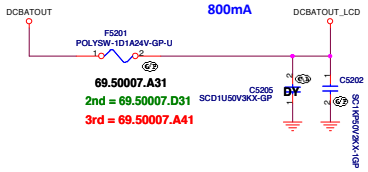
CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

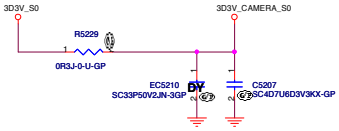
MB Connecter		是否接線	Wire (40 PIN)	FFC(40 PIN)
Pin 10	GND	Y	Pin 10(GND 實體線)	Pin 10 GND
Pin 13	GND	Y	Pin 13(GND 實體線)	Pin 13 GND
Pin 16	GND	Y	Pin 16 (GND實體線)	Pin 16 GND
Pin 19	GND	Y	Camera Module Pin 6 DMIC_GND(實體線)	Pin 19 GND
Pin 22	GND	Y	Camera Module Pin 5 AUD_DMIC_CLK	Pin 22 GND
Pin 25	GND	Y	Camera Module Pin 7 AUD_DMIC_IN0	o
Pin 28	GND	Y	Camera Module Pin 8 CCD GND(實體線)	Pin 28 GND
Pin 31	GND	Y	Pin 31 (實體線)	Pin 31 GND
Pin 32	GND	Y	Camera Module Pin 3 USB_CAMERA#	Pin 32 GND
Pin 33	GND	Y	Camera Module Pin 2 USB_CAMERA	Pin 33 GND
Pin 34	3D3V_CAMERA_S0	Y	Camera Module Pin 4 3D3V_CAMERA_S0	NC(0 ohm DY)

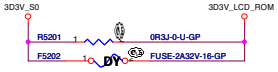
PIN	MB Connecter	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0



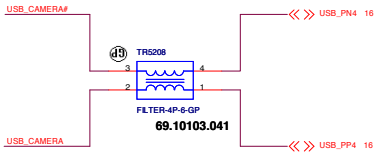
INVERTER POWER



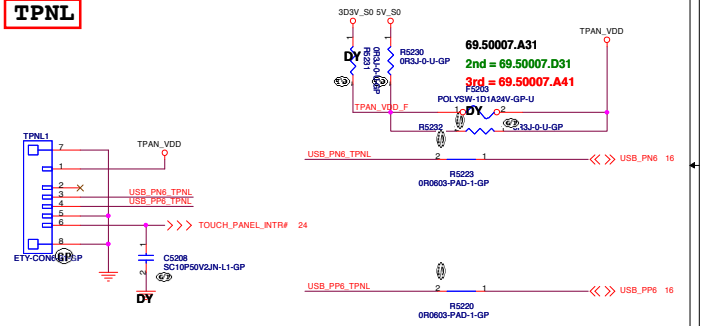




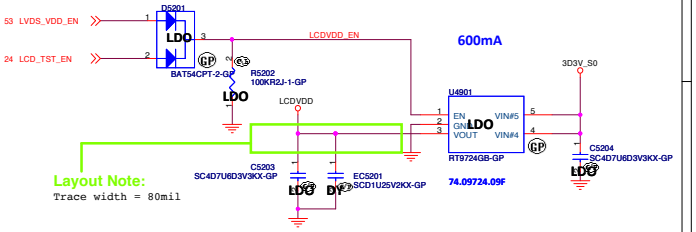
Close to LCD connector



TPNL



LCDVDD



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A2 | Document Number: OAK14 Haswell | Rev: X00

Date: Wednesday, April 17, 2013 | Sheet 52 of 104

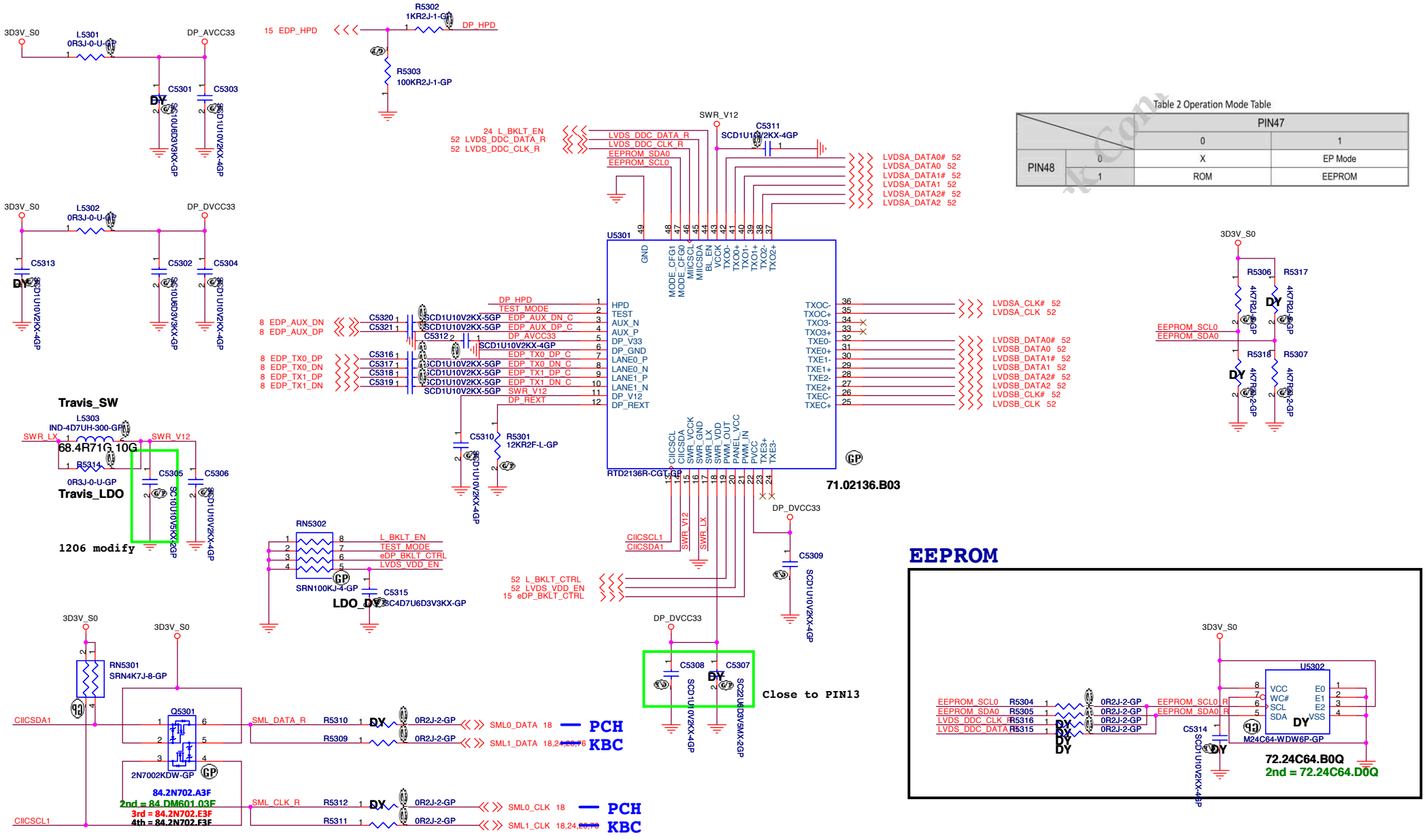


Table 2 Operation Mode Table

		PIN47	
		0	1
PIN48	0	X	EP Mode
	1	ROM	EEPROM

<Core Design>

Wistron Corporation
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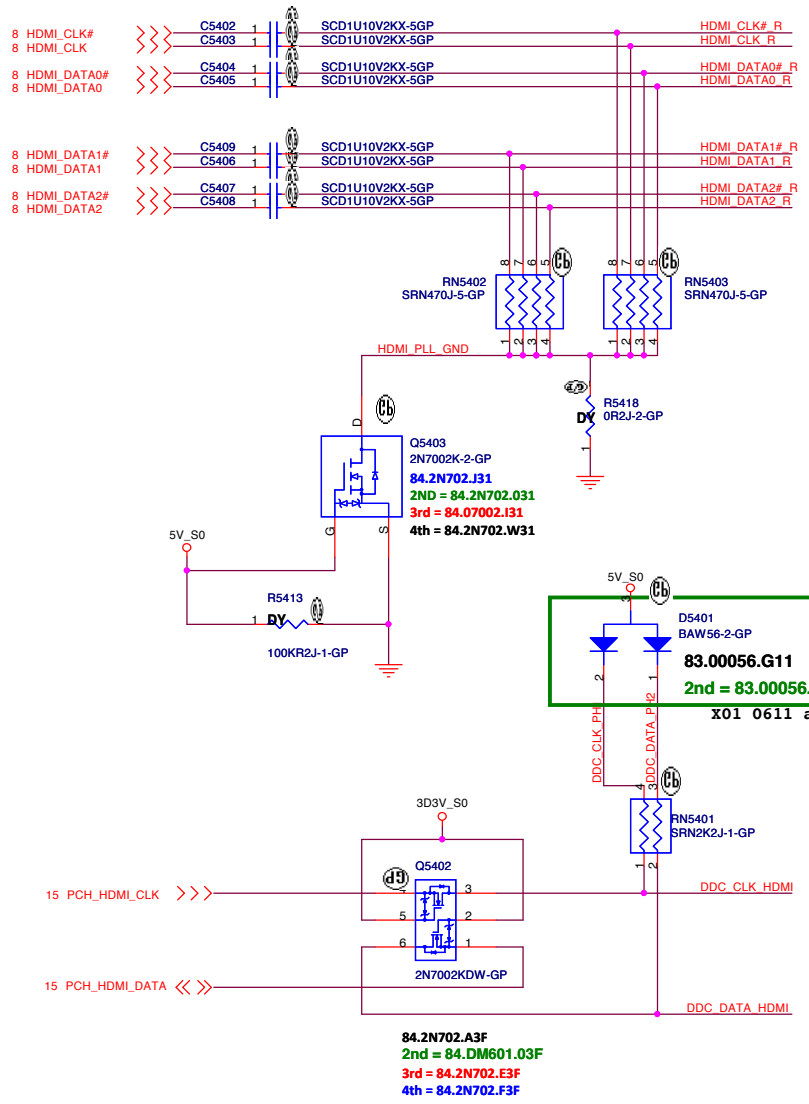
Taipei Hsien 221, Taiwan, R.O.C.

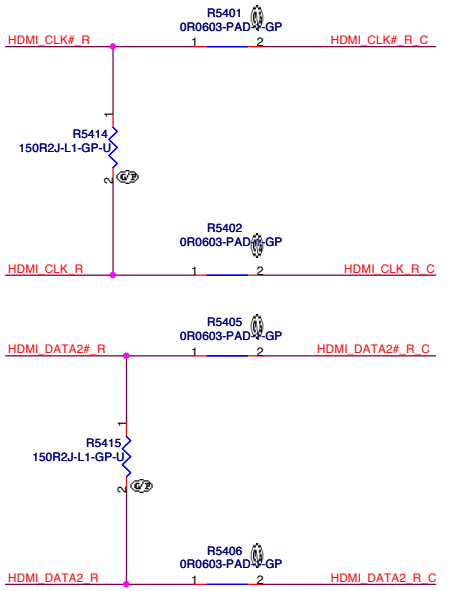
Title: LVDS_Switch

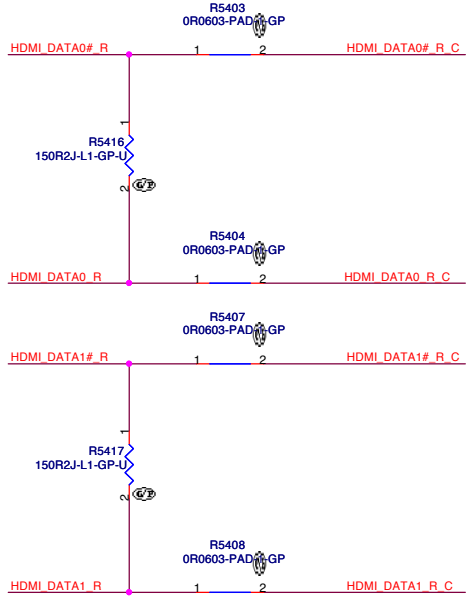
Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Tuesday, April 02, 2013 | Sheet 53 of 104

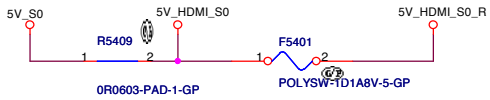
SSID = VIDEO

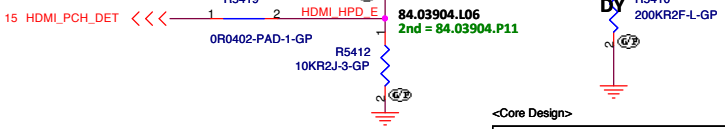


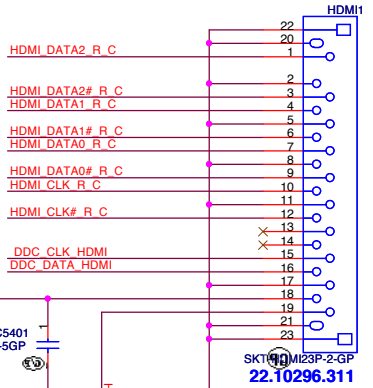




HDMI CONN







<Core Design>

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Title: **HDMI Level Shifter/Connector**		
Size: A3	Document Number: **OAK14 Haswell**	Rev: **X00**
Date: Friday, April 19, 2013	Sheet 54 of 104	

SSID = User.Interface

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

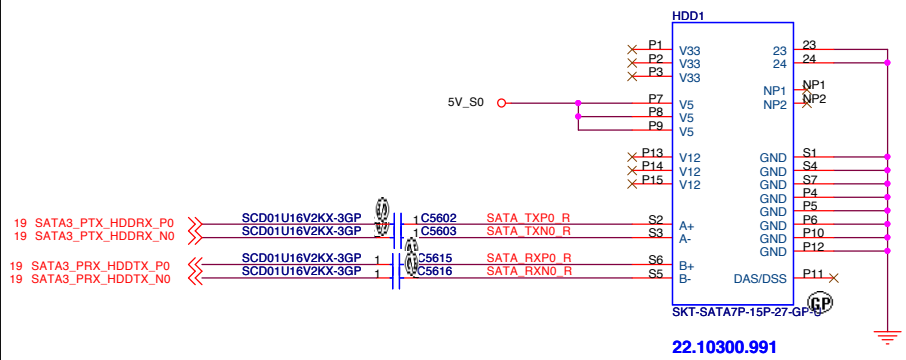
Title: ITP/Fan Connector

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

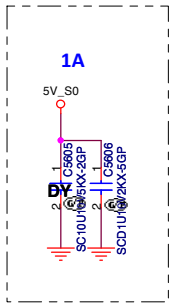
Date: Thursday, January 10, 2013 | Sheet 55 of 104

SSID = SATA

SATA HDD Connector



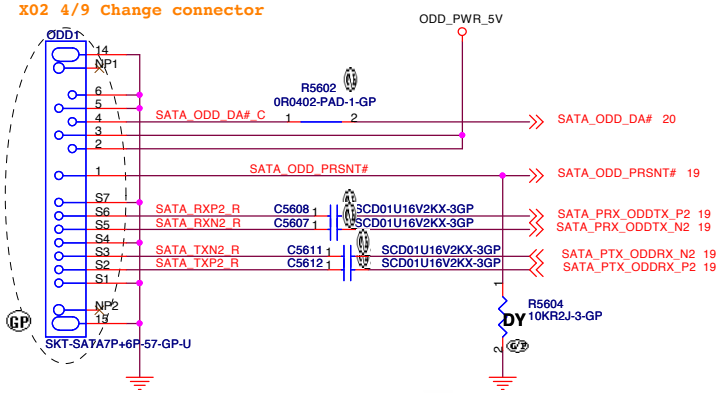
22.10300.991

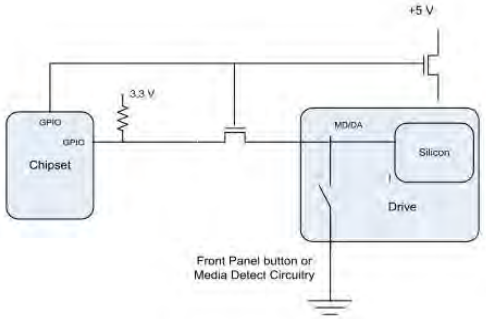


Close to HDD1

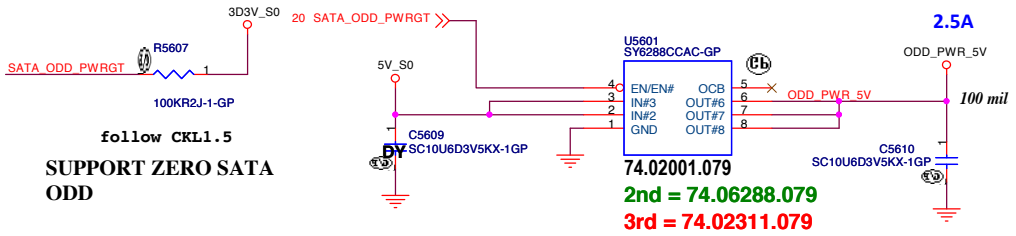
ODD Connector

X02 4/9 Change connector





SATA Zero Power ODD



follow CKL1.5

SUPPORT ZERO SATA ODD

74.02001.079

2nd = 74.06288.079

3rd = 74.02311.079

Current limit
Active High
typ =>2.5A

<Core Design>

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Title	HDD/ODD	
Size A3	Document Number OAK14 Haswell	Rev X00
Date: Thursday, April 18, 2013	Sheet 56 of 104	

SSID = ESATA

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<Core Design>

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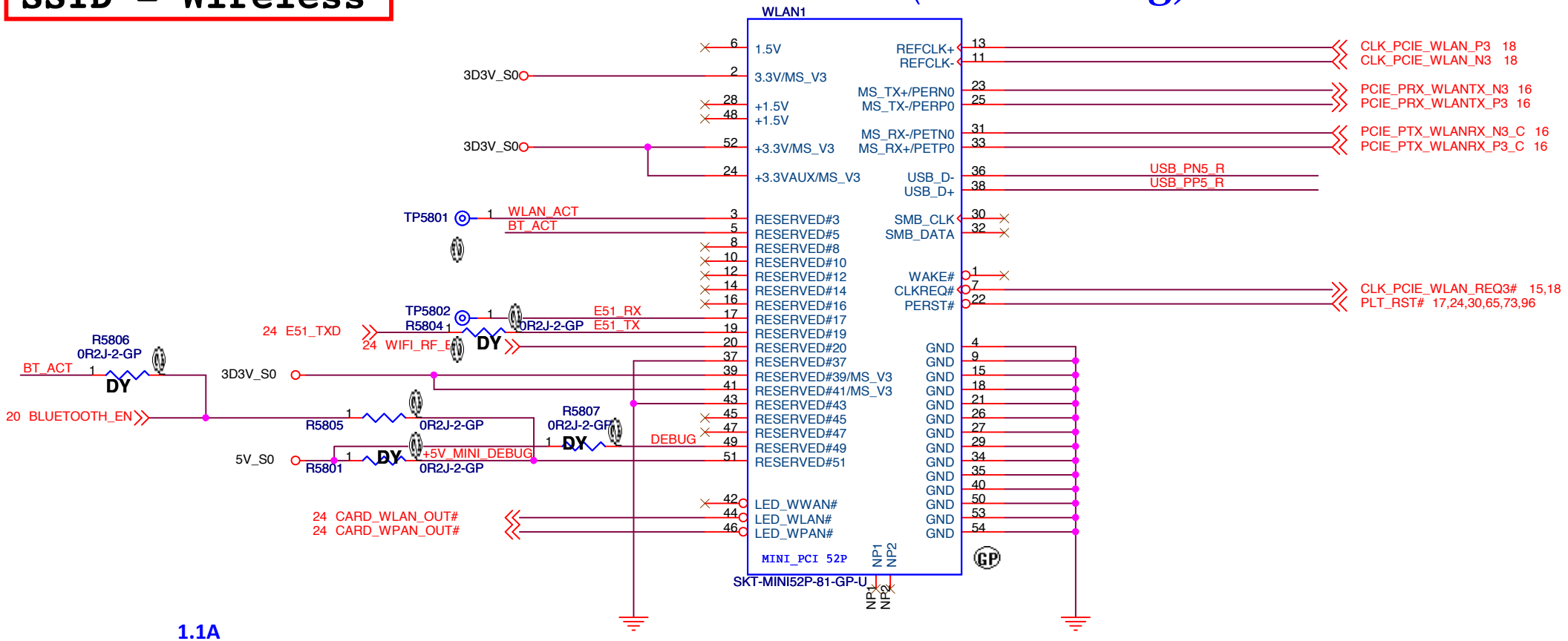
Title: ESATA

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

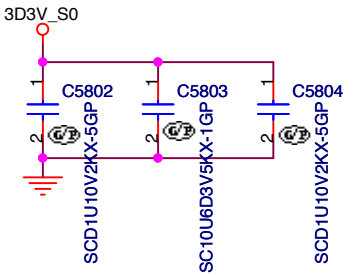
Date: Thursday, January 10, 2013 | Sheet 57 of 104

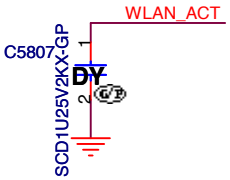
Mini Card Connector(802.11a/b/g)

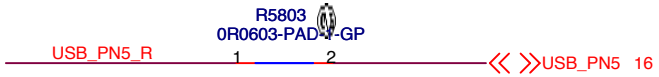
SSID = Wireless

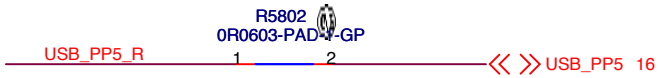


1.1A









<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A4	Document Number: OAK14 Haswell	Rev: X00
Date: Thursday, April 18, 2013	Sheet 58 of 104	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 59 of 104

SSID = PCH

<Core Design>

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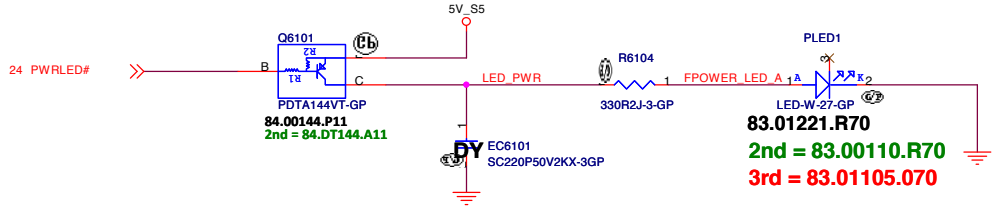
Title: *(Reserved)*

Size	Document Number	Rev
A4	*OAK14 Haswell*	*X00*

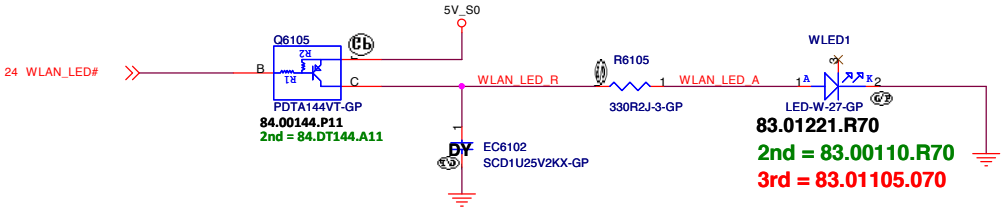
Date: Thursday, January 10, 2013 Sheet 60 of 104

SSID = User.Interface

FRONT POWER LED
Low actived from KBC GPIO

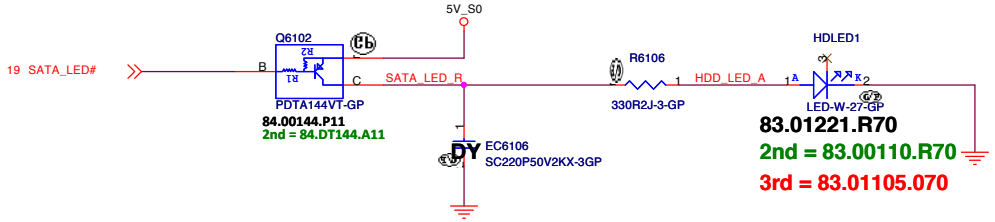


Wireless LED
Low actived from KBC GPIO

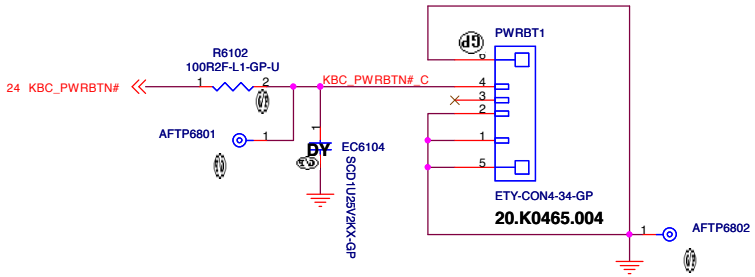


Place EC6806 near WLED1

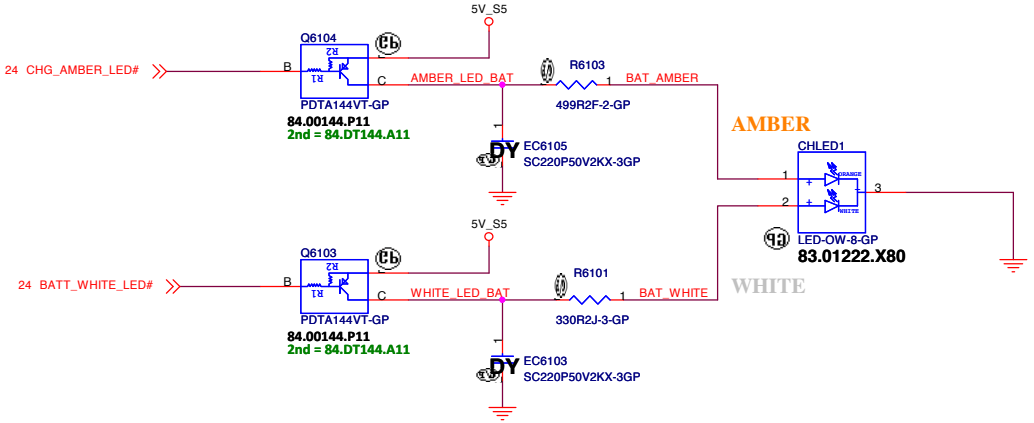
SATA HDD LED(White)
Low actived from PCH GPIO



Power button



Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

<Core Design>

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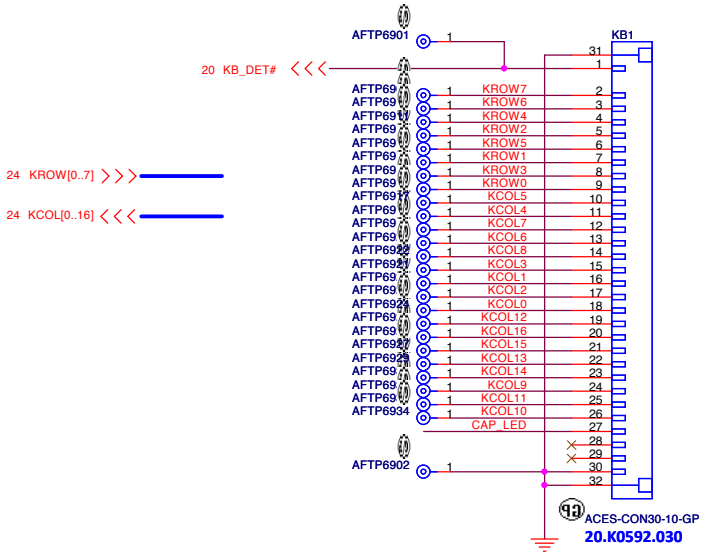
Title	LED Bard/Power Button	
Size A3	Document Number OAK14 Haswell	Rev X00
Date: Thursday, March 07, 2013	Sheet 61 of 104	

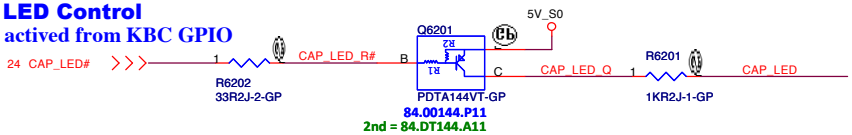
SSID = KBC

Internal Keyboard Connector

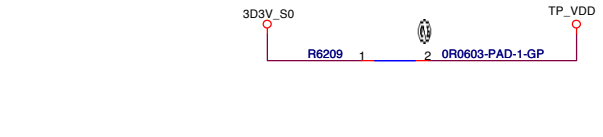


CAP LED Control

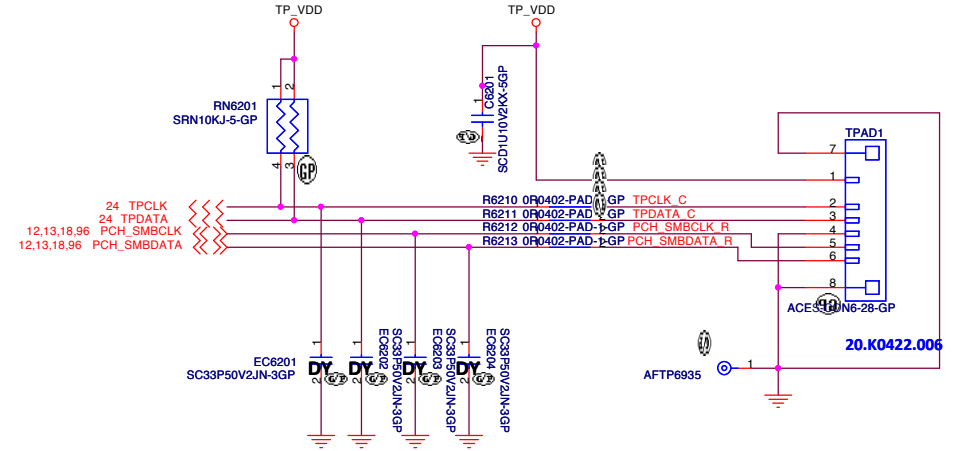
LOW actived from KBC GPIO

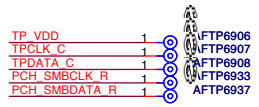


SSID = Touch.Pad



Touch Pad Connector





Refer "PN 510-002792-01 Rev 2 " module spec

Pin number	Pin name
1	VDD
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMBUS_CLK
6	SMBUS_DATA

<Core Design>

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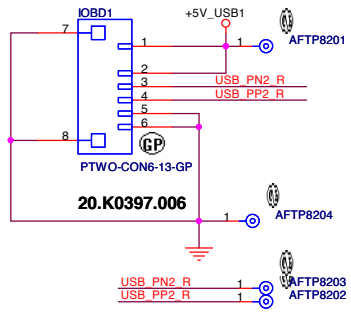
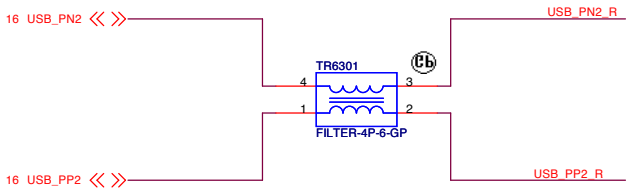
Title: Key Board/Touch Pad

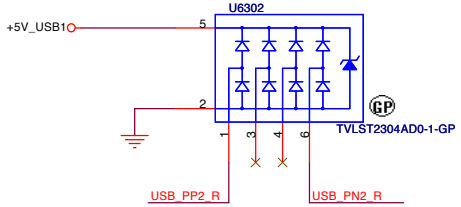
Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Wednesday, April 17, 2013 | Sheet 62 of 104

SSID = User.Interface







<Core Design>

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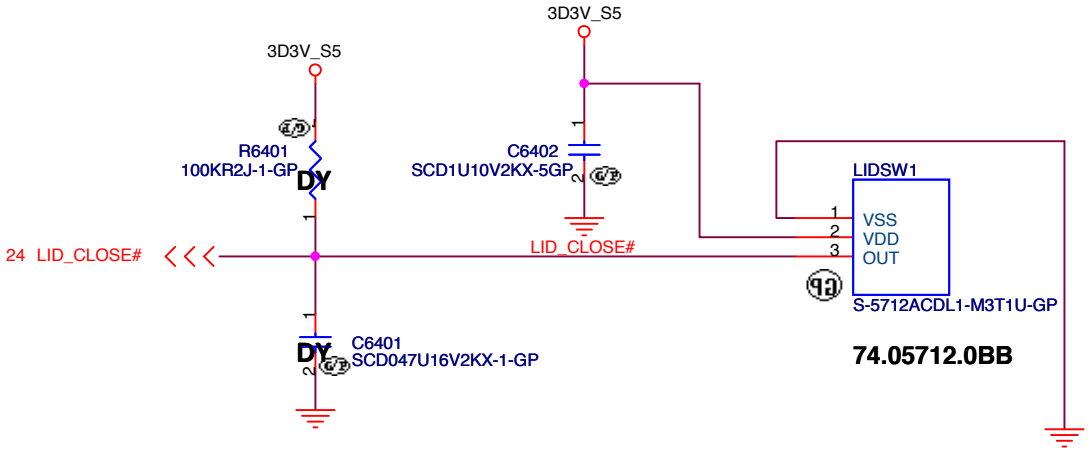
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

Date: Friday, April 12, 2013 | Sheet 63 of 104

SSID = User.Interface



<Core Design>

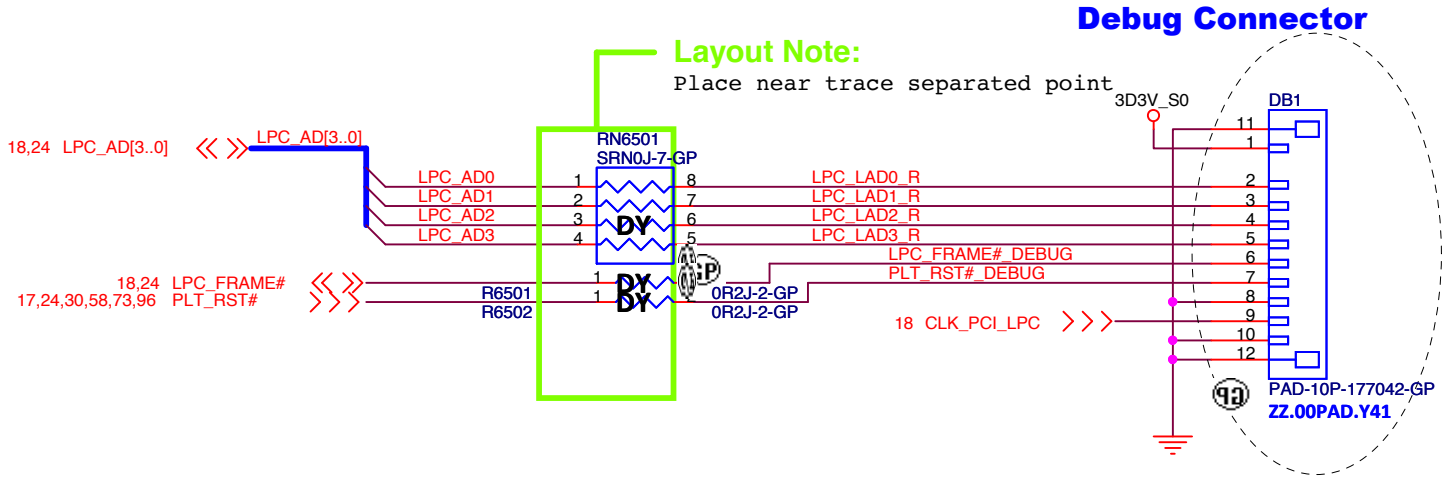
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***OAK14 Haswell***	***X00***

Date: Thursday, March 07, 2013 Sheet 64 of 104

SSID = DEBUG PORT



A00 4/8 DB1 change to dummy pad with sold mask

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*		
Size: A4	Document Number: *OAK14 Haswell*	Rev: *X00*
Date: Monday, April 08, 2013	Sheet 65 of 104	

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*OAK14 Haswell*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 67 of 104

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 PORT

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 70 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*OAK14 Haswell*	*X00*

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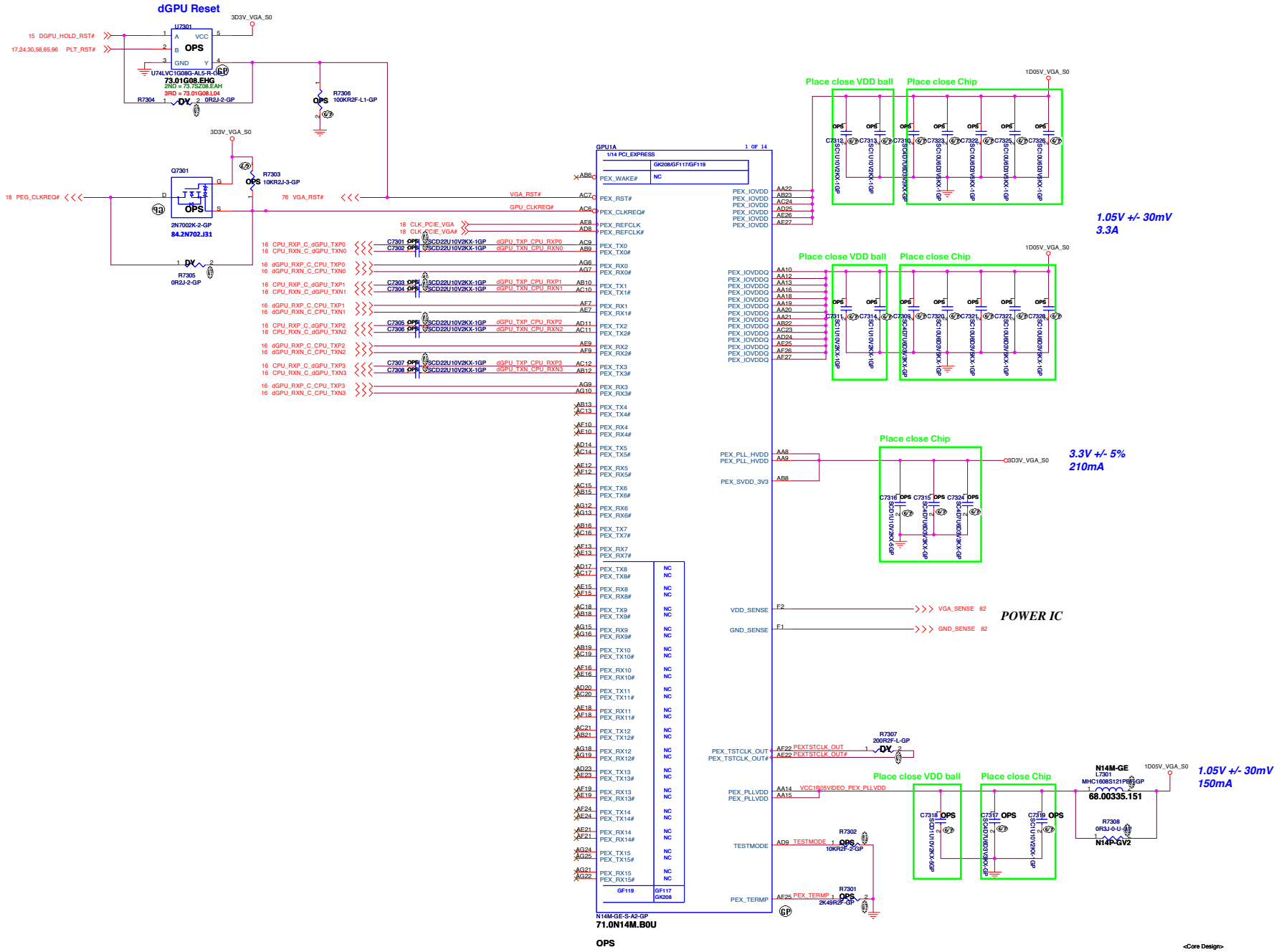
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

Date: Thursday, January 10, 2013 | Sheet 72 of 104



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A2	OAK14 Haswell	X00

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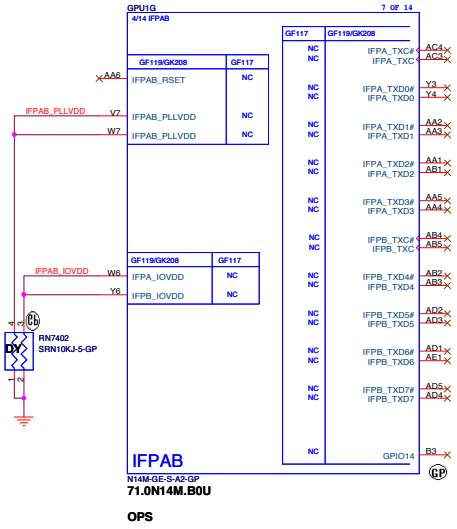
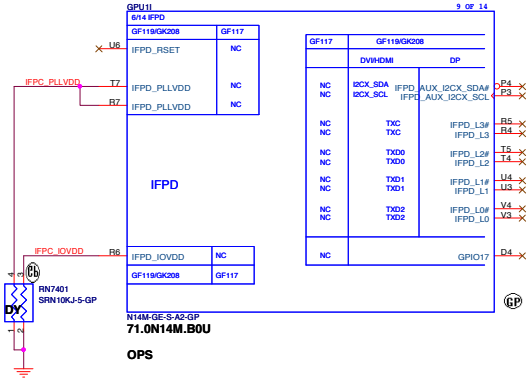
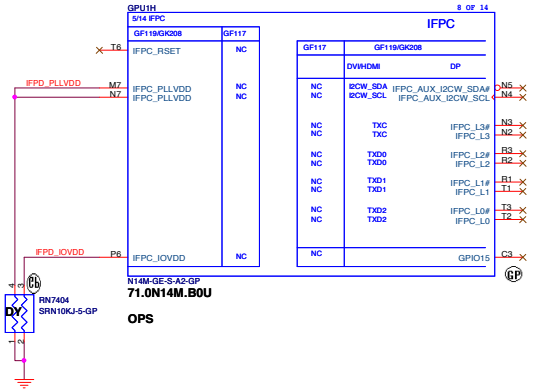
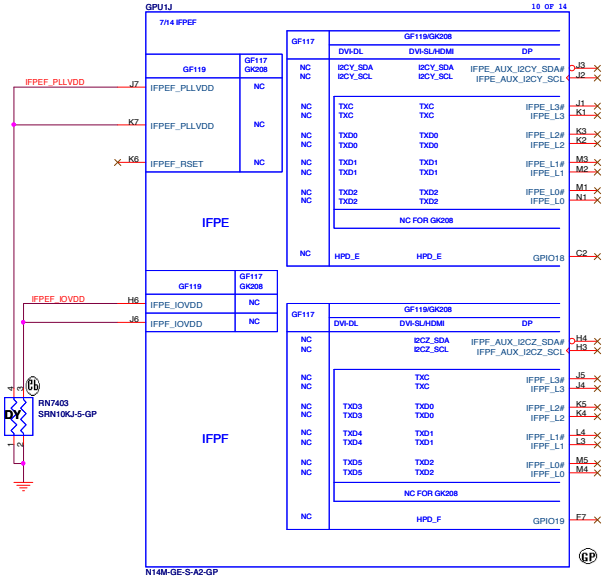
LVDS Interface





HDMI Interface





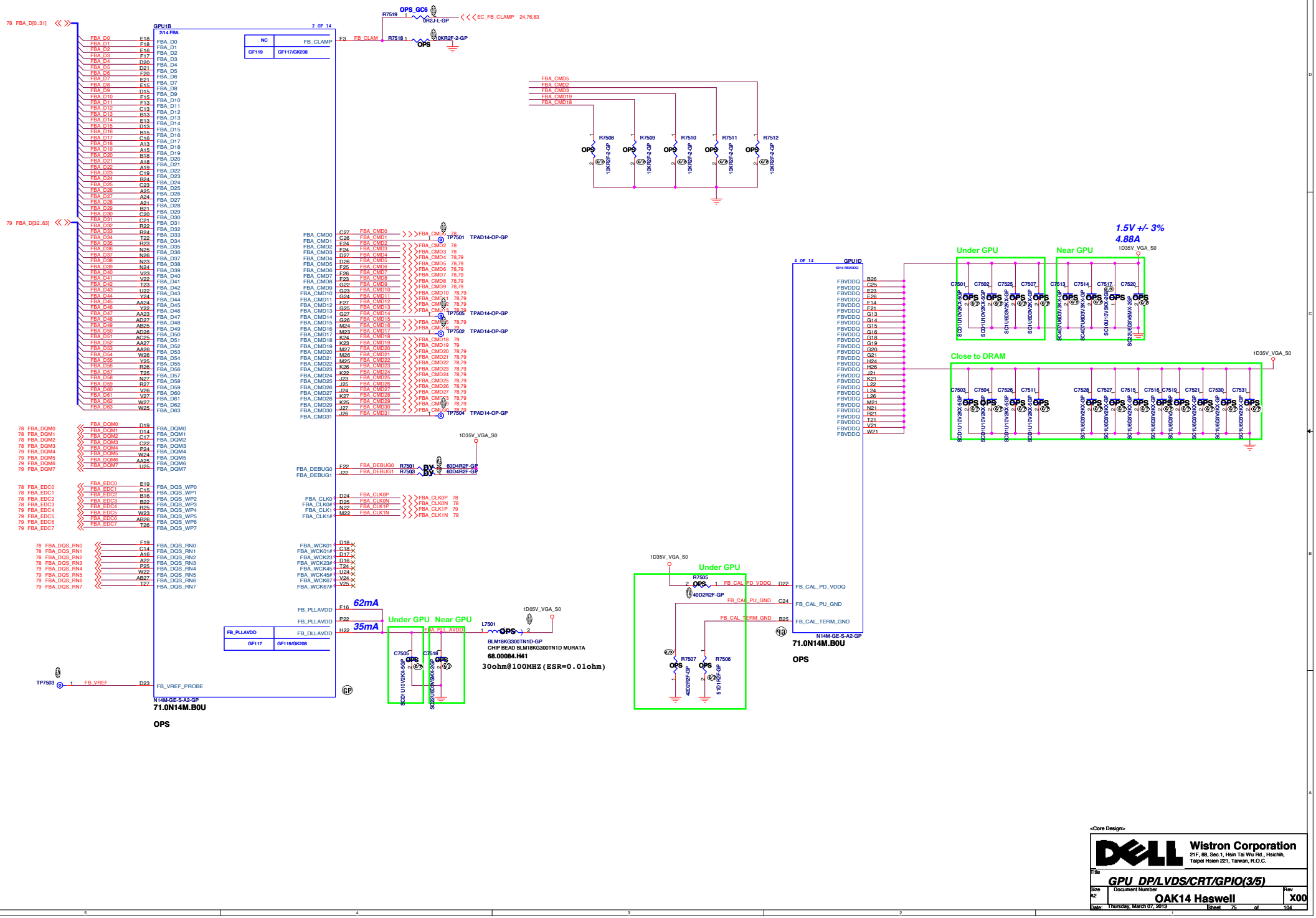
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU Memory(2/5)*

Size: A2 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, January 10, 2013 | Sheet 74 of 104



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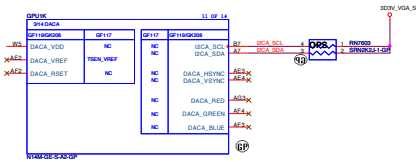
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: OAK14 Haswell | Rev: X00

Date: Thursday, March 07, 2013 | Sheet 75 of 104



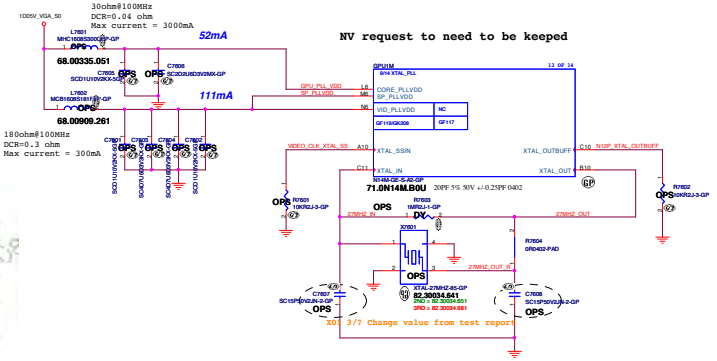


Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

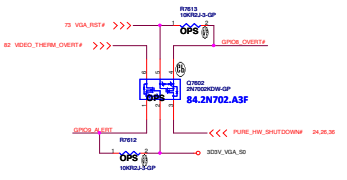
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M*16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready
		0xC	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Post-production candidate

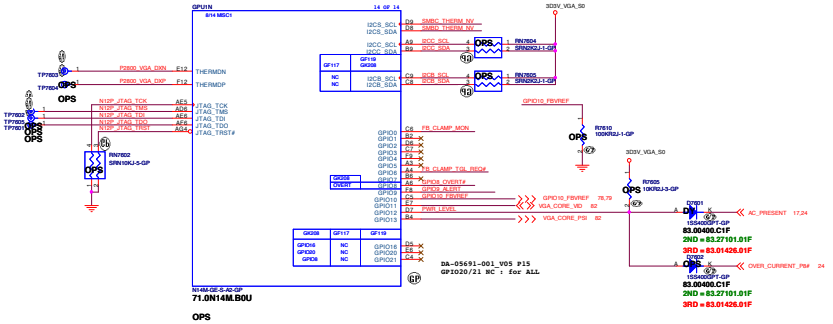
Table 112. GB2-64 and GB4-128 PLL Power Rail Filter - PLL_VDD

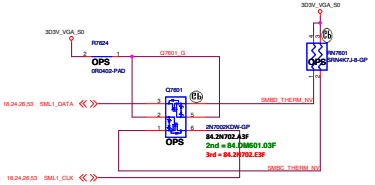
GPU Package Type	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64 and GB4-128	PLL_VDD	100 nF	X7R	0402	1	Under GPU
		22 µF	X7R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR<0.010 for H14E-GE; 0.05 for all others)		0402	1	Near GPU

Table 113. GB2-64, GB4-128, GB2-192 and GB3-256 PLL Power Rail Filter - SP_PLLVDD and VID_PLLVDD Combined

GPU Package Type	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64, GB4-128 and GB3-256	SP_PLLVDD and VID_PLLVDD combined	100 nF	X7R	0402	2	Under GPU
		4.7 µF	X5R	0402	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU







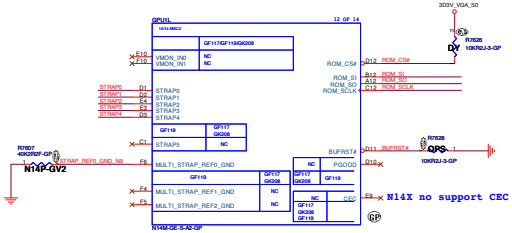


Table 5. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V/ 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready

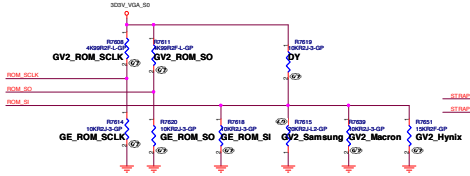
Table 121. Resistance Mapping to Hex Values

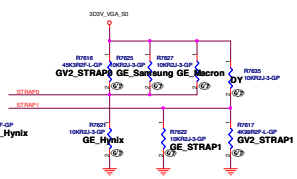
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

N14M-GE, N14P-GV2 Strapping





	N14M-LP	N14M-GS	N14P-GV	N14P-GV2
Chip Part #	GK208-640 (Small package) GK208-740 (Big package)	GK208-630 (Small package) GK208-730 (Big package)	GK208-650 (Small package) GK208-750 (Big package)	GK208-632 (Small package) GK208-732 (Big package)
Device ID	0x1291	0x1290	0x1294	0x1292

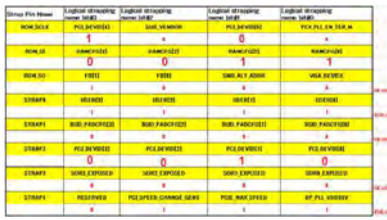
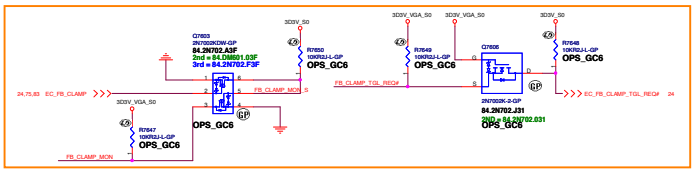
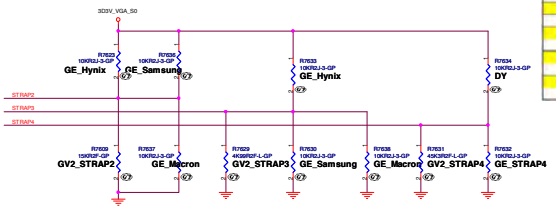
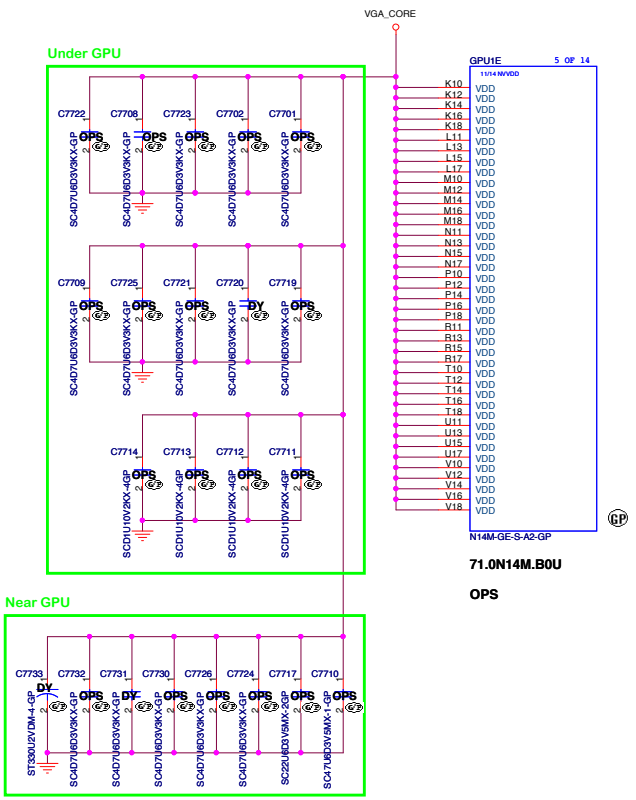


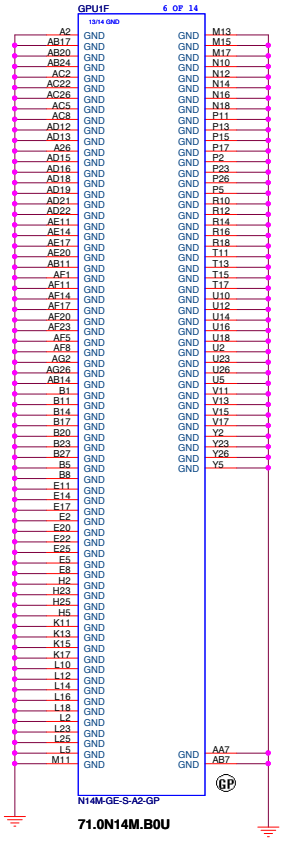
Table 120. Device Specific Strap Mode Selection

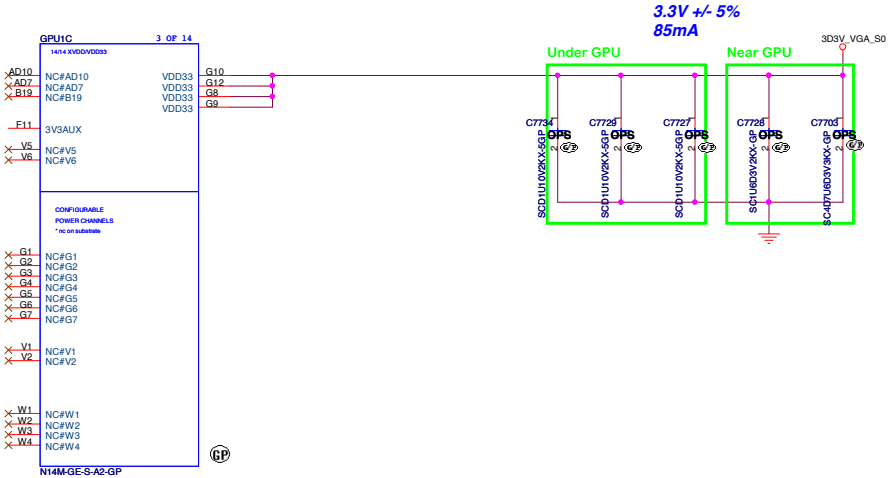
	N14E-GE/-GL	Other N14x GPU's
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Boot's	Multi-Level











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Title: GPU_DPPWR/GND(5/5)

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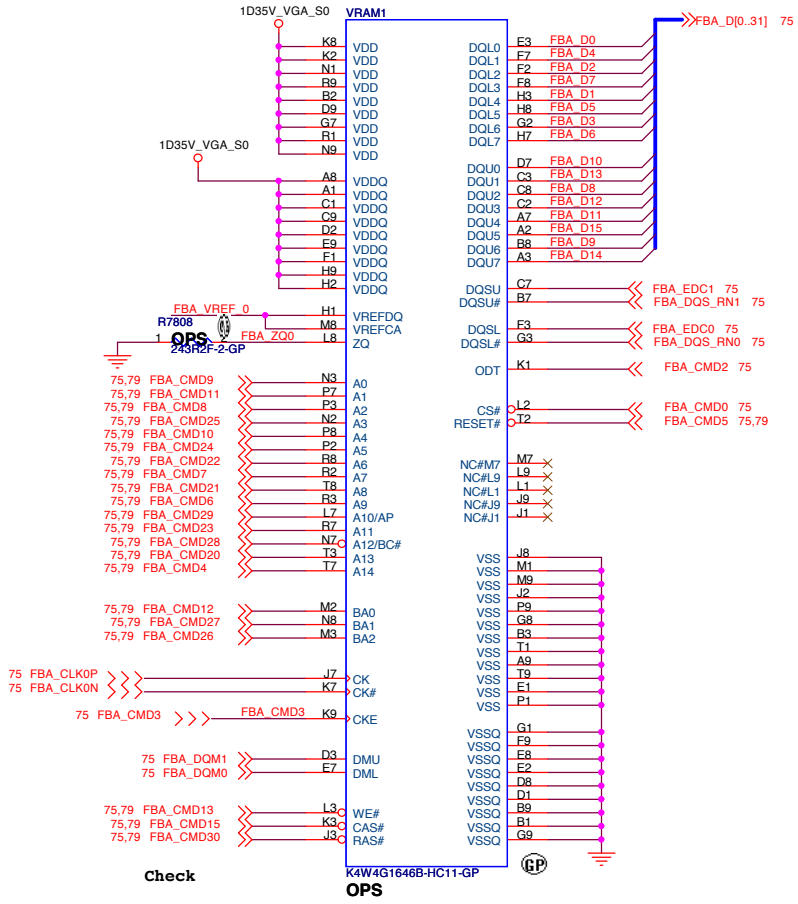
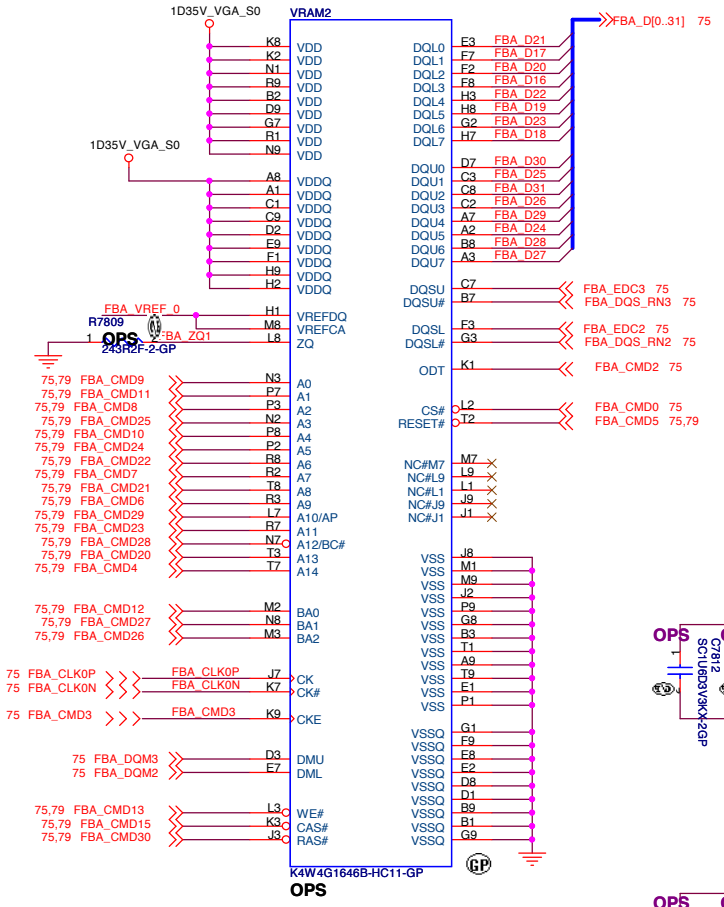
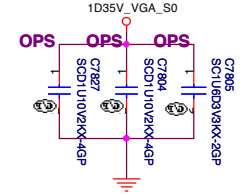
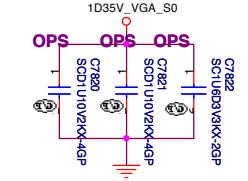




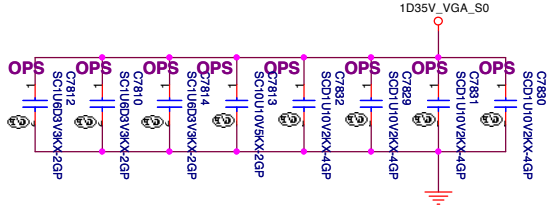
Place close VRAM1 VDD ball



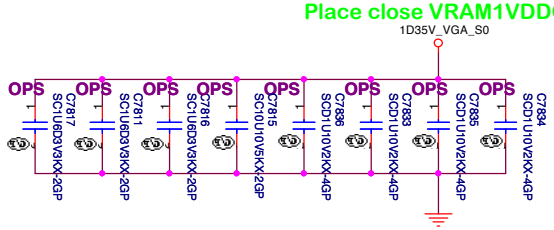
Place close VRAM2 VDD ball



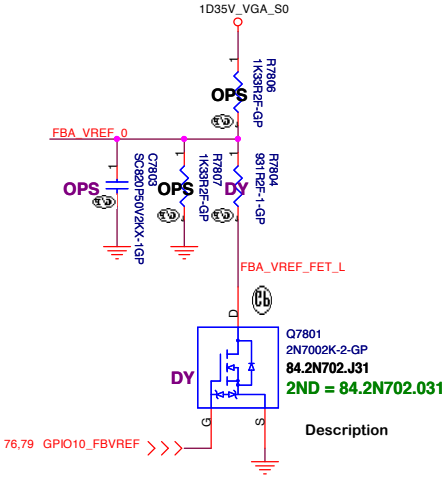
Place close VRAM1VDDQ ball

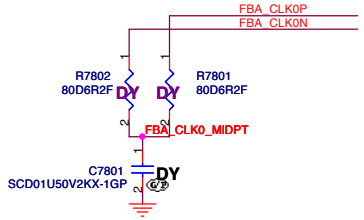


Place close VRAM1VDDQ ball

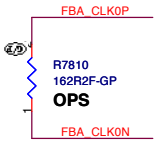


Frame Buffer Patition A-Lower Half





FBCLK Termination place on VRAM side



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

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Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: OAK14 Haswell | Rev: X00

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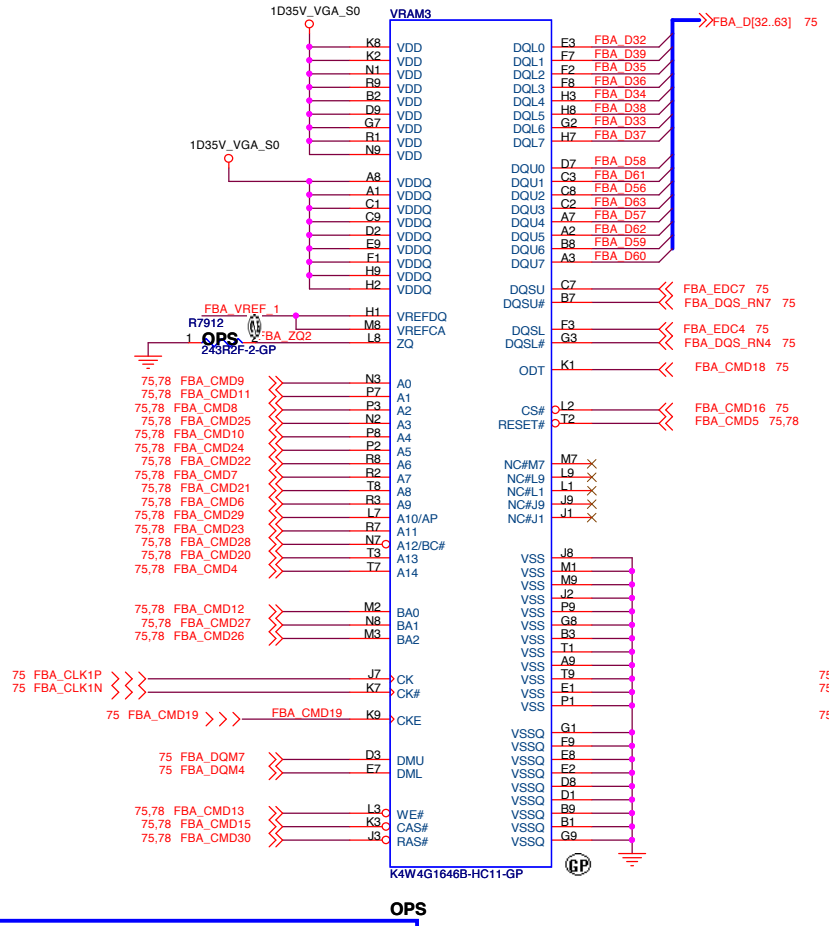
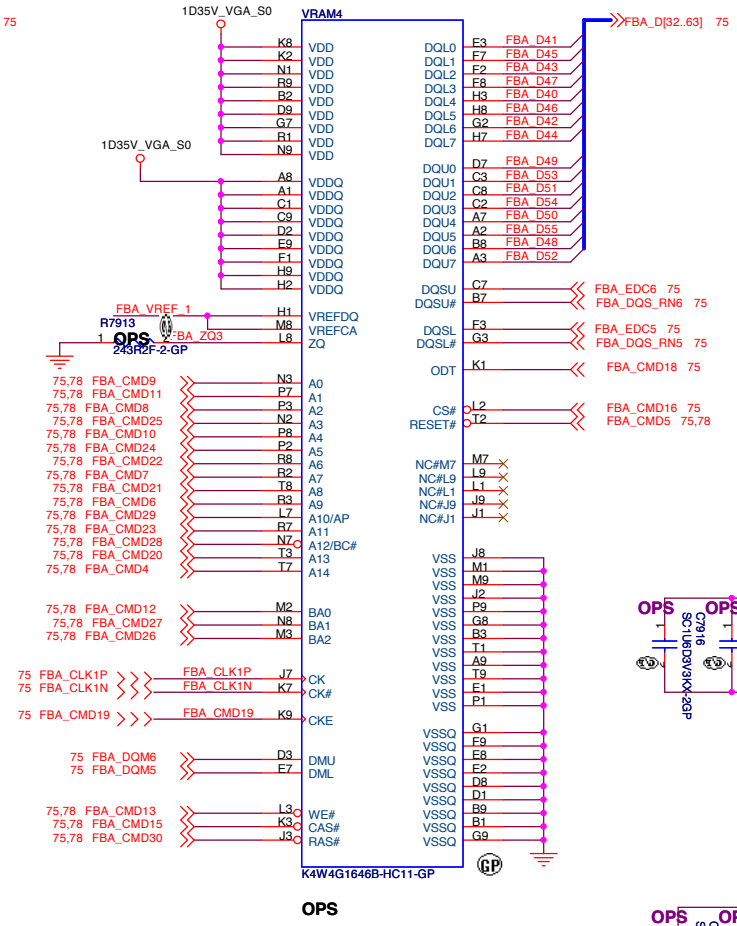
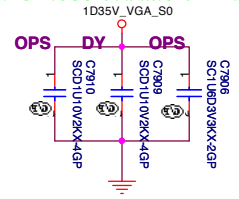
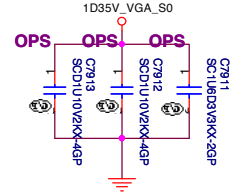




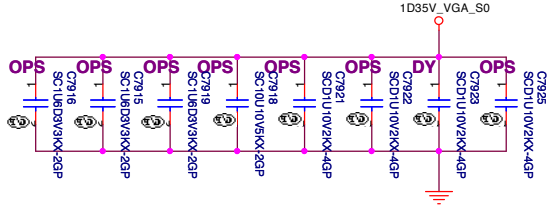
Place close VRAM3 VDD ball



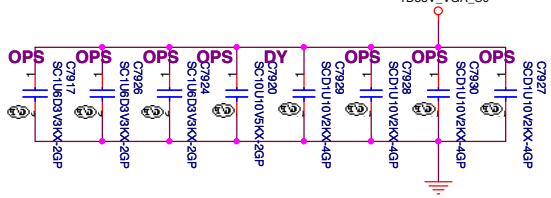
Place close VRAM4 VDD ball



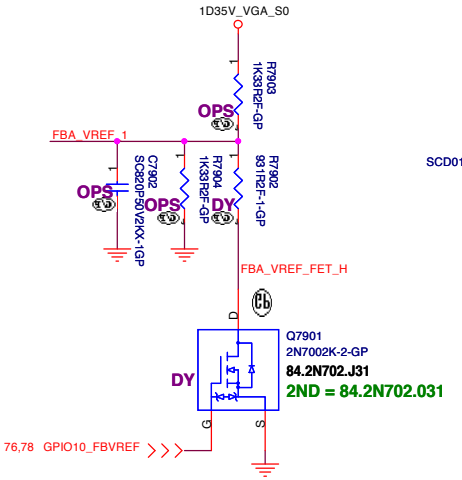
Place close VRAM3 VDDQ ball

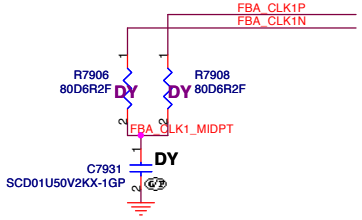


Place close VRAM4 VDDQ ball

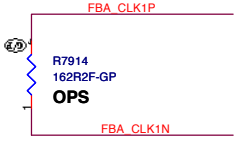


Frame Buffer Patition A-Lower Half





FBCLK Termination place on VRAM side



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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	OAK14 Haswell	X00

Date: Wednesday, April 17, 2013 Sheet 79 of 104

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Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	OAK14 Haswell	X00

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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	OAK14 Haswell	X00

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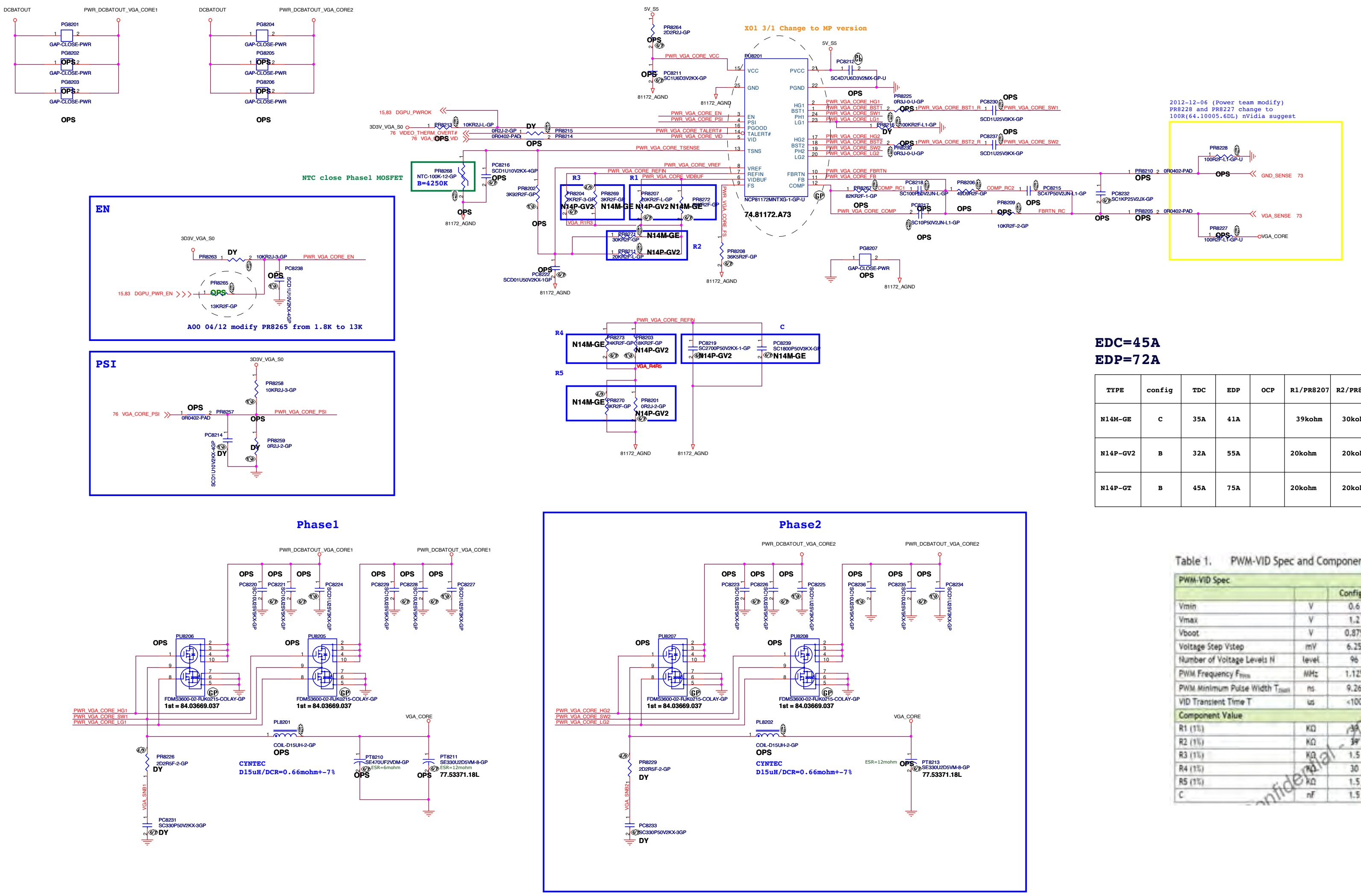


EDC=45A
EDP=72A

TYPE	config	TDC	EDP	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14M-GE	C	35A	41A		39kohm	30kohm	3kohm	24kohm	3kohm	1.8nF
N14P-GV2	B	32A	55A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF
N14P-GT	B	45A	75A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{Dash}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
MOS: Q1: Id=10A,Rdson=9.8~13.2 mohm ; Q2: Id=17A, Rdson=3.6~5.2mohm 84.03669.037
Inductor: CHIP CHOKE 0.22UH PCMB063T-R22MS 2.5~3mohm Isat =34Arms 68.R2210.20C
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L

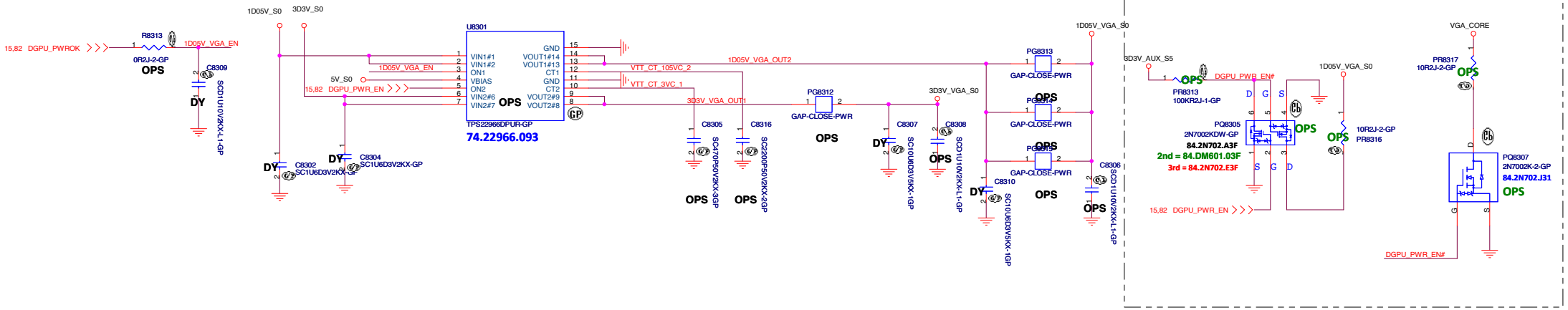
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
MOS: Q1: Id=10A,Rdson=9.8~13.2 mohm ; Q2: Id=17A, Rdson=3.6~5.2mohm 84.03669.037
Inductor: CHIP CHOKE 0.22UH PCMB063T-R22MS 2.5~3mohm Isat =34Arms 68.R2210.20C
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L

3D3V_VGA_S0
1D05V_VGA_S0

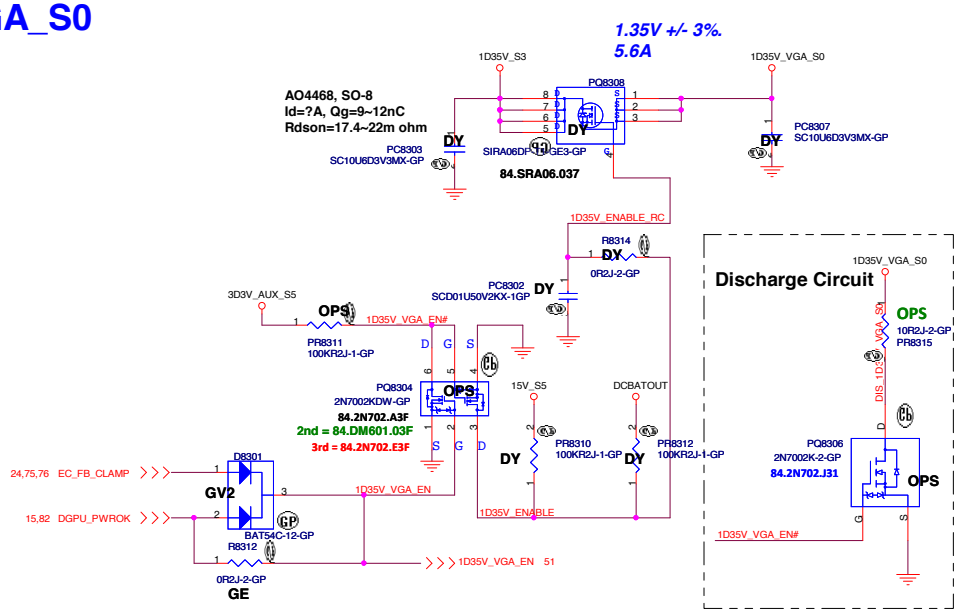
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0

0307 Add Discharge Circuit



1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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Title: DISCRETE VGA POWER
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Title

Reserved

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Title: *Reserved*

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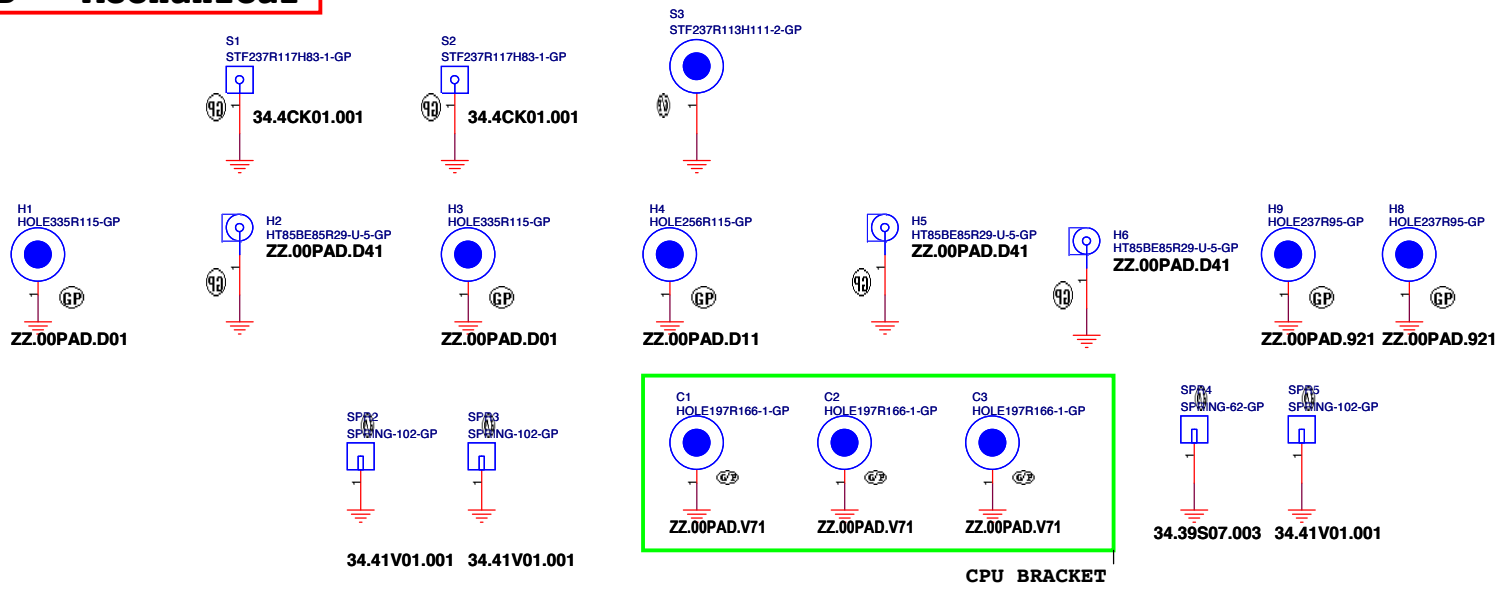
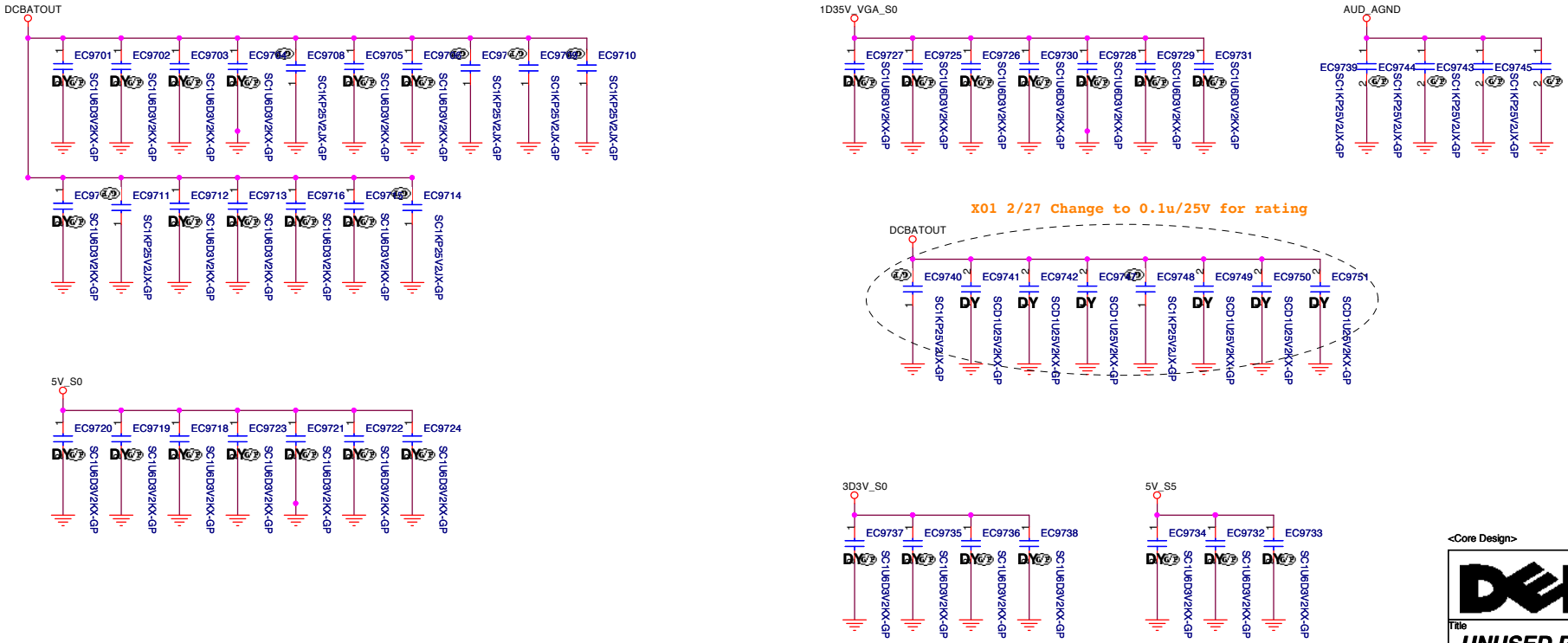
SSID = Mechanical



SSID = EMI



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Title: *UNUSED PARTS/EMI Capacitors*

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Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

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Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

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Title: *Reserved*

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Title: Free Fall Sensor

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *OAK14 Haswell* | Rev: *X00*

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Title: *Reserved*

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Title: Express Card

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Title
LVDS_Switch

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Title: *CRT_Switch*

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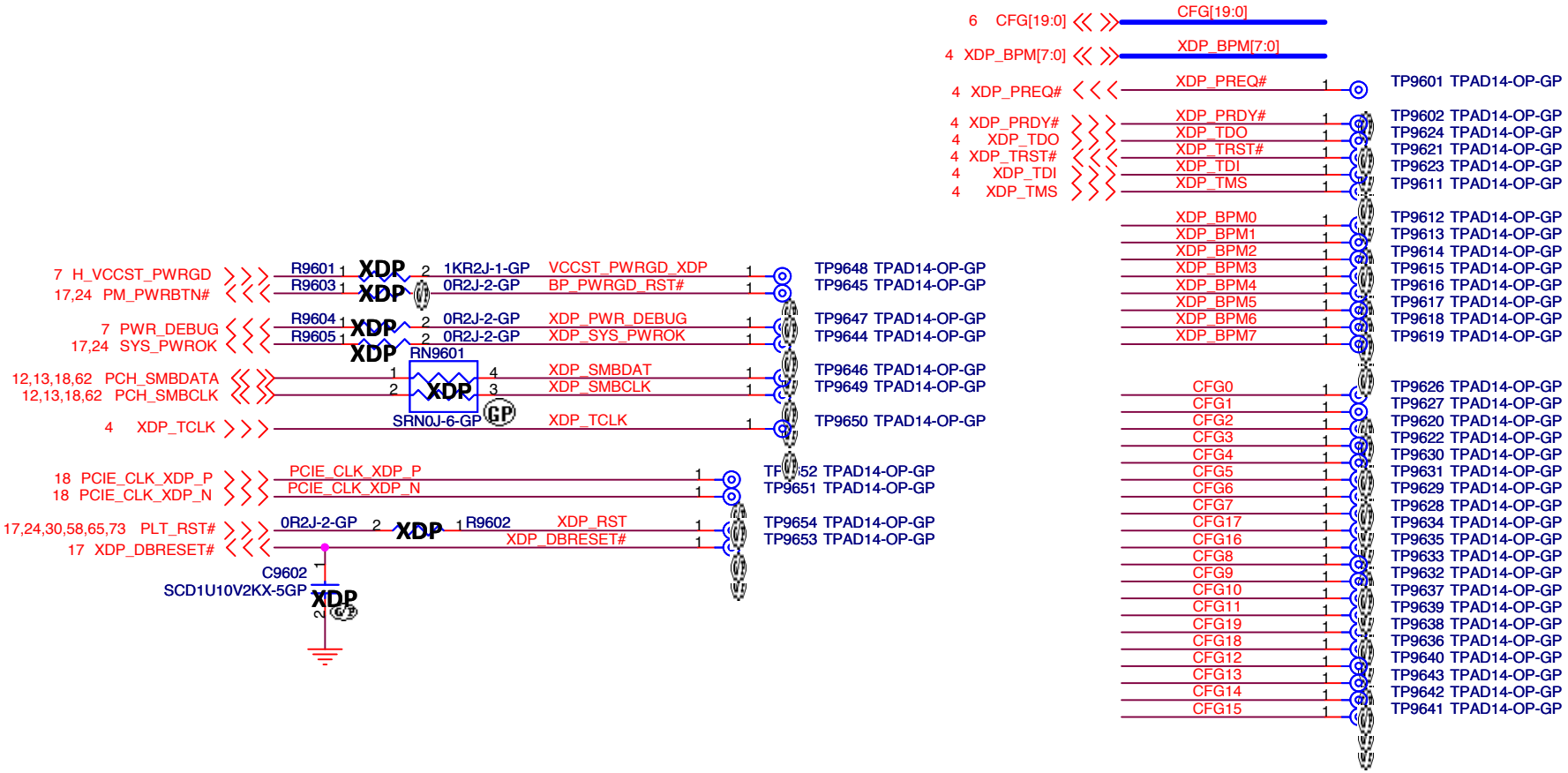
SSID = XDP

CPU XDP



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Title: TOUCH PANEL

Size	Document Number	Rev
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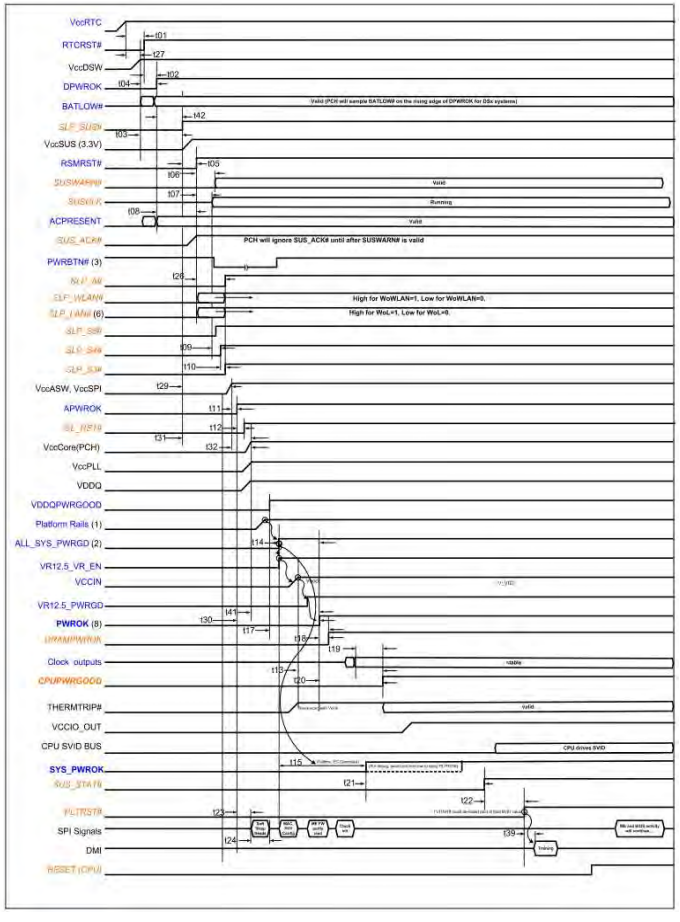
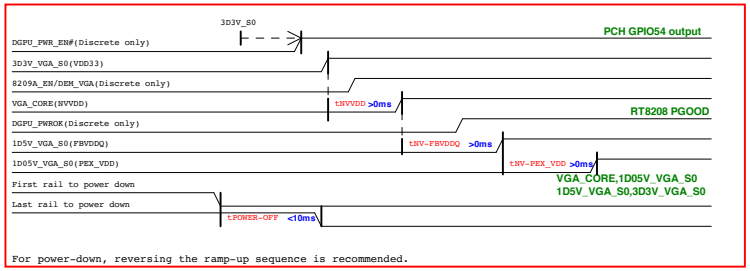
Shark Bay Platform Power Sequence

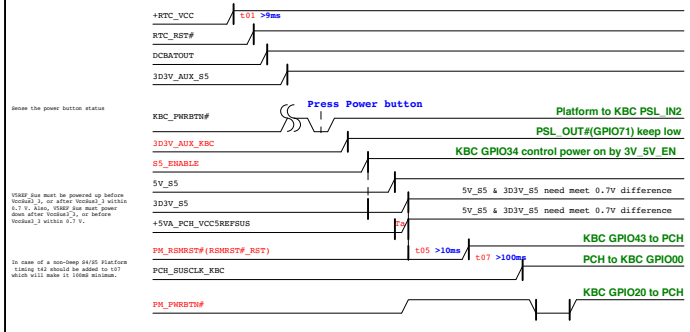


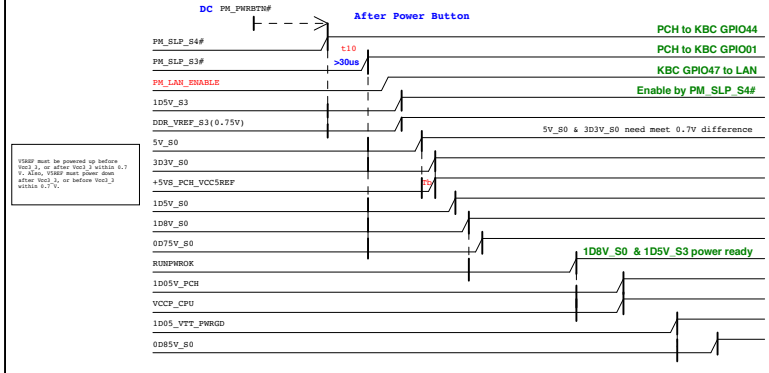
N14P-GT Power-Up/Down Sequence

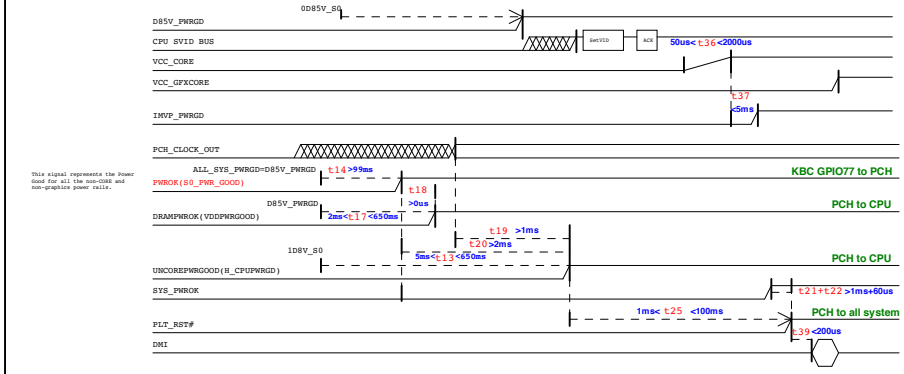


(DC mode)

Red Words: Controlled by EC GPIO







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Title: Power Sequence

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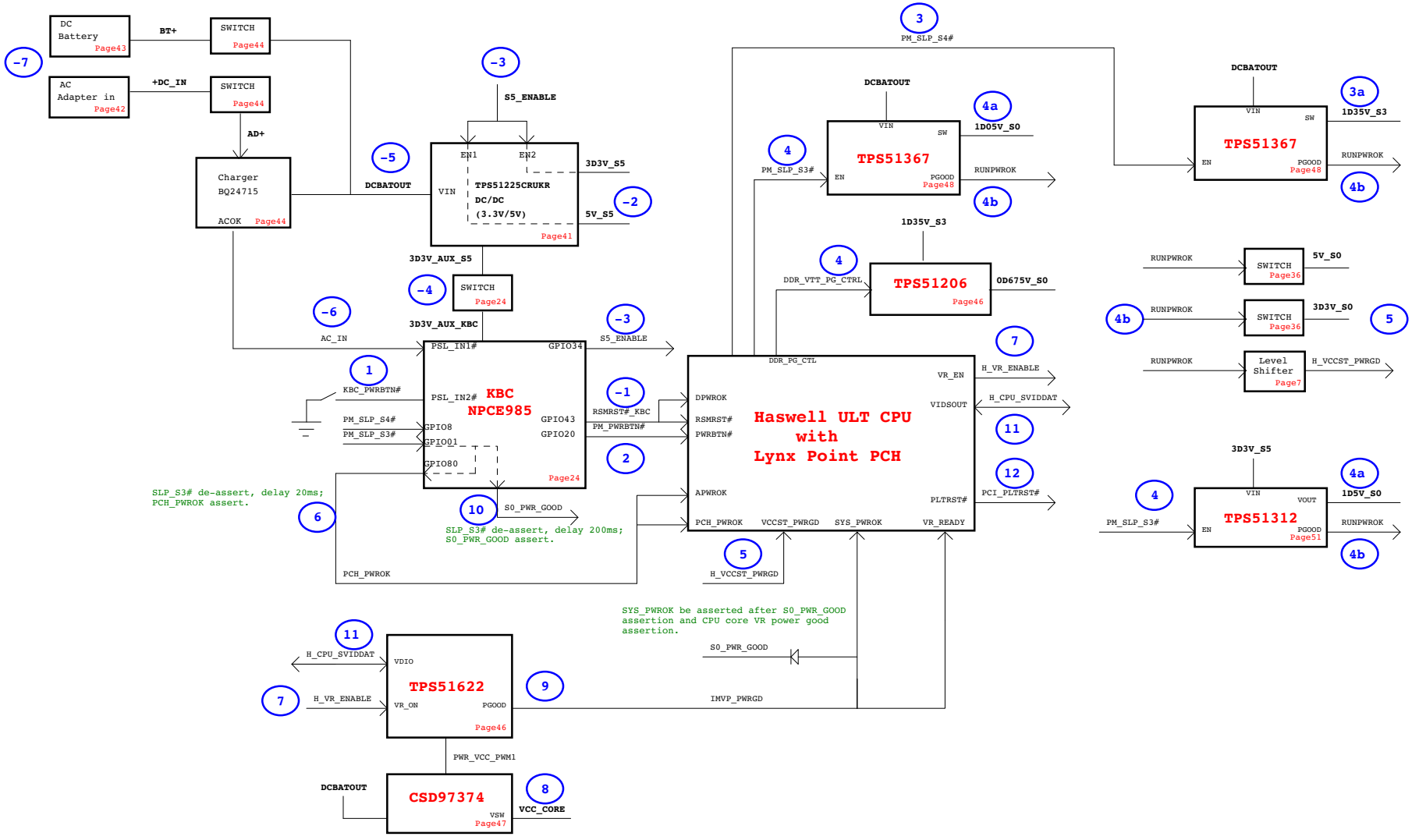
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 9 → 10 → 11 → 12

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Title: Power Sequence Diagram

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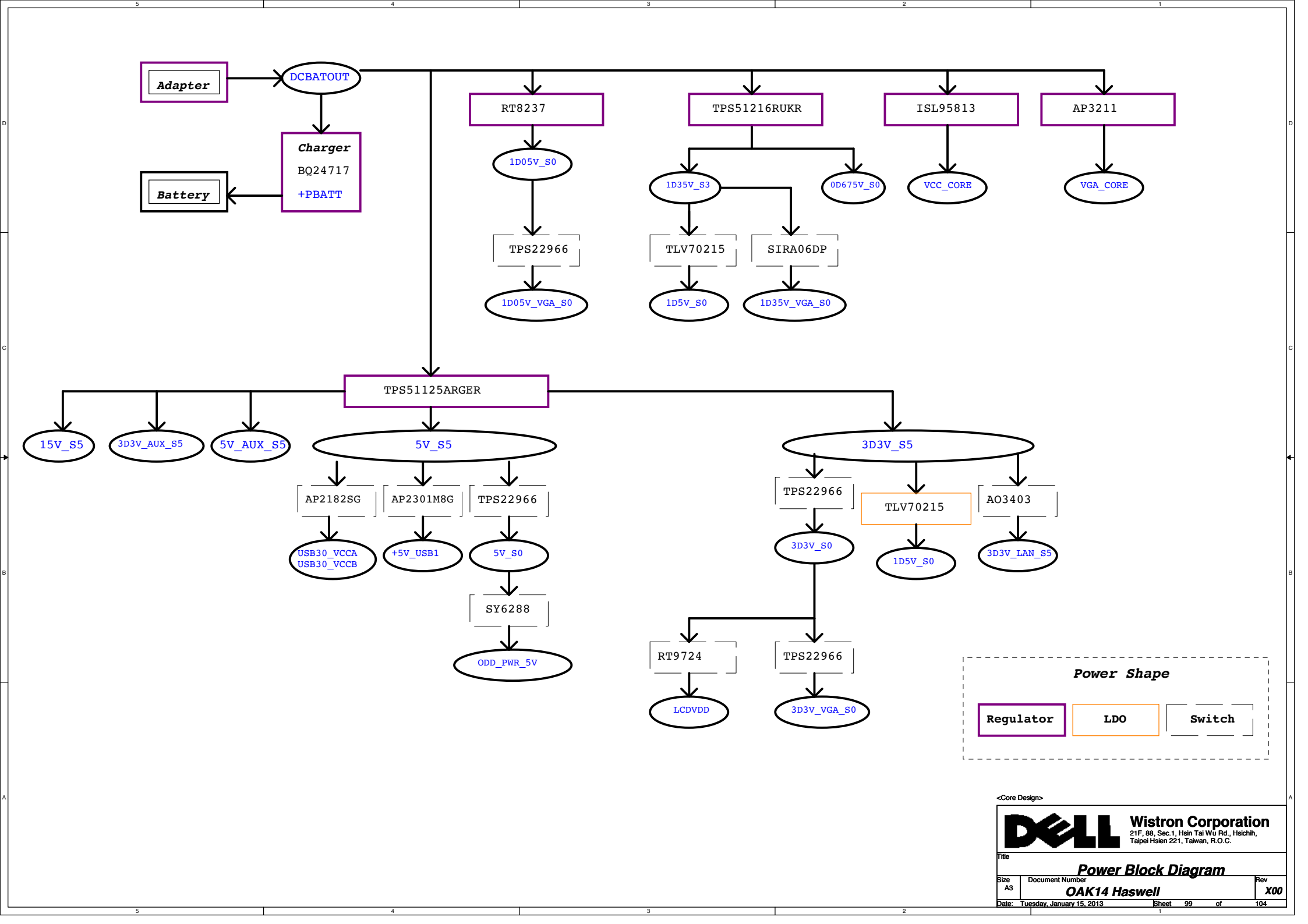

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Title: Power Block Diagram

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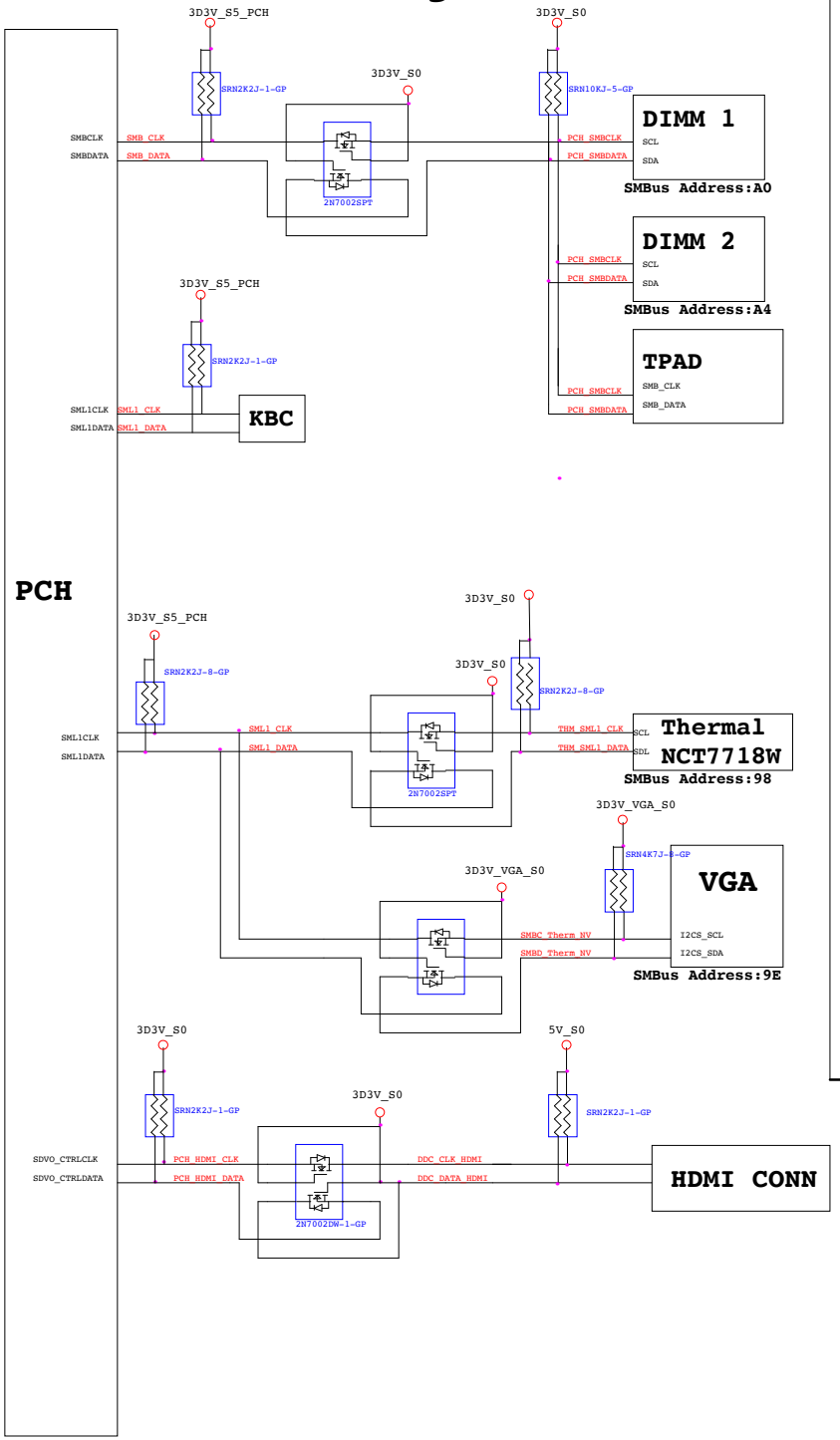
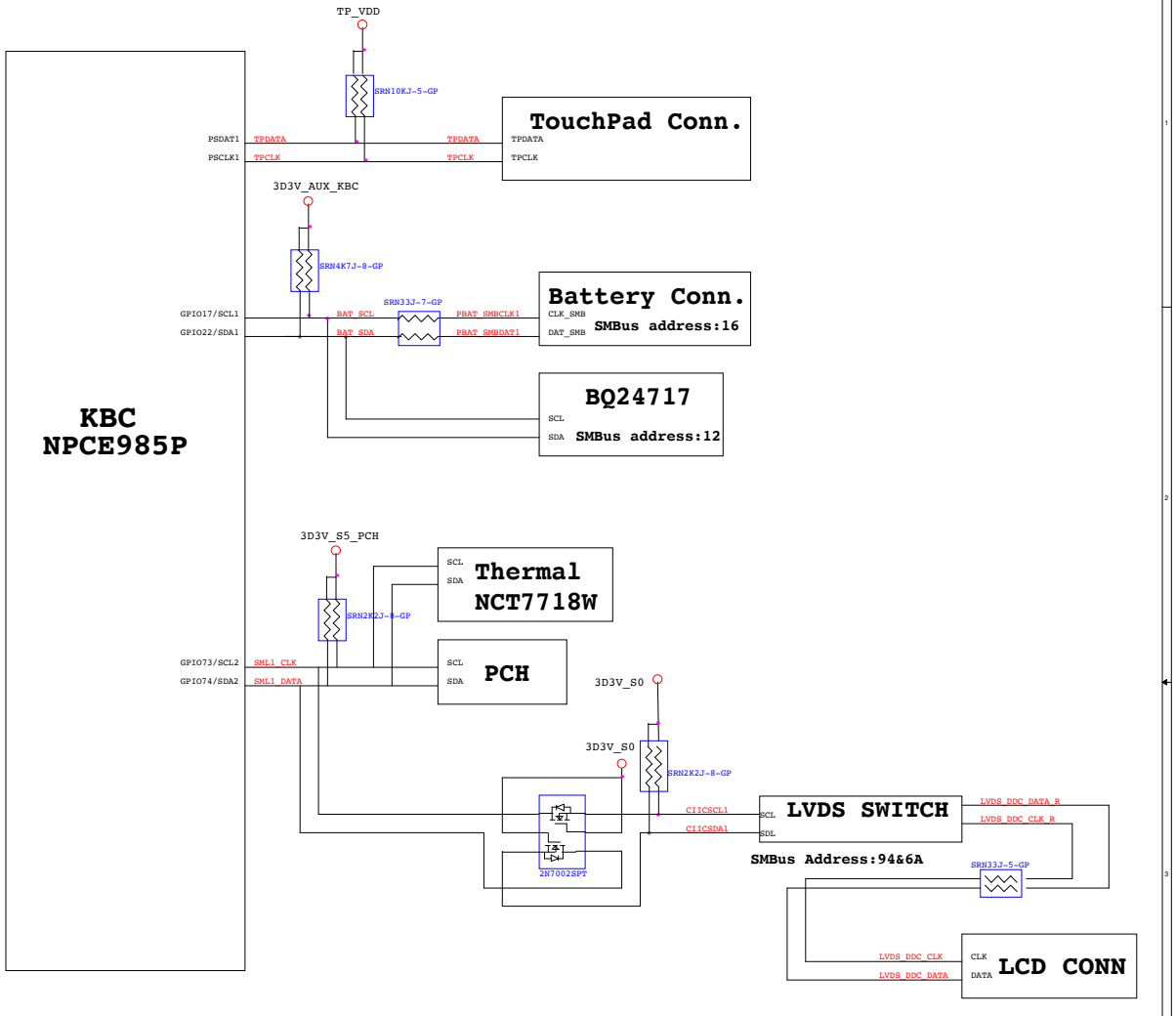
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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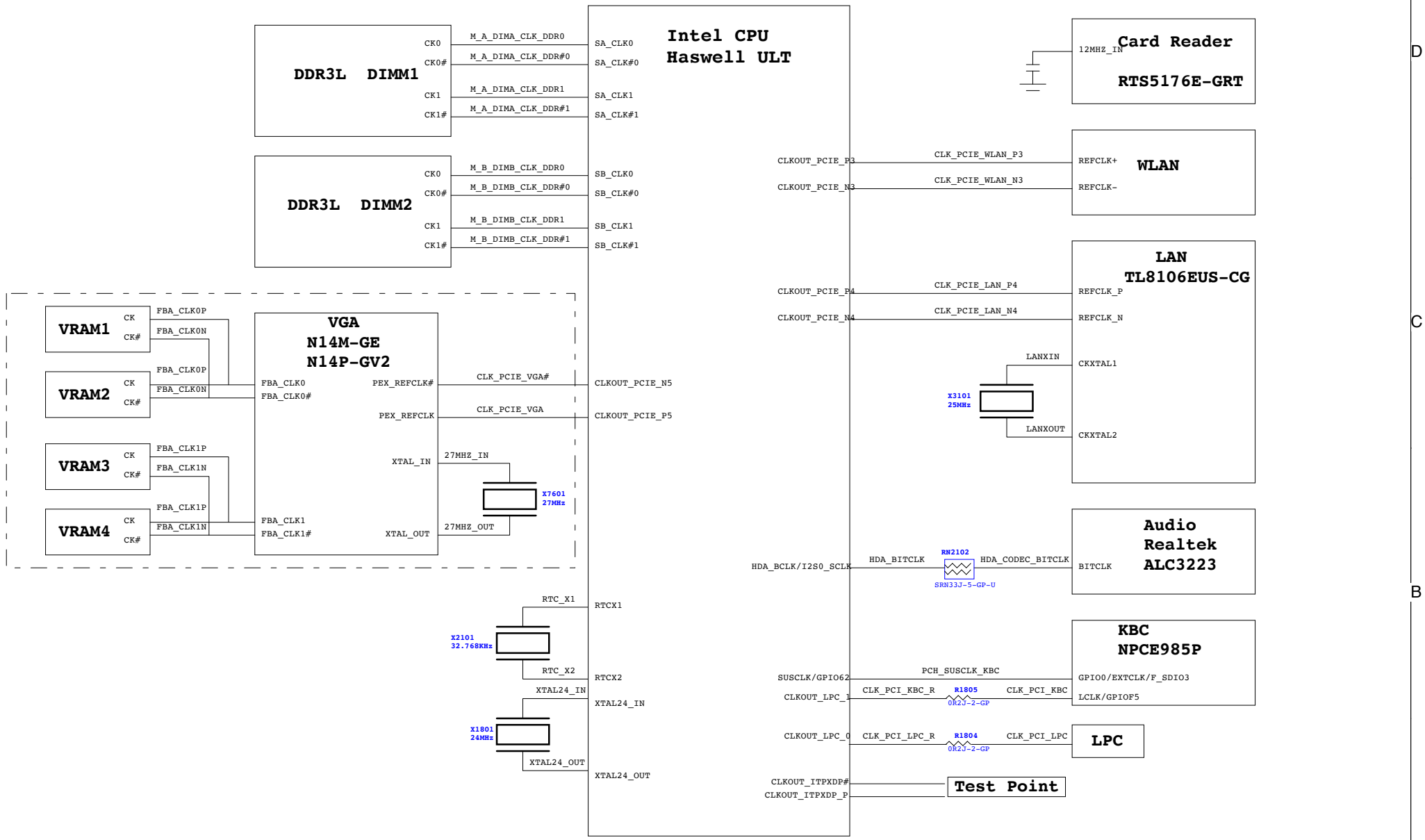
OAK Haswell CLK Block Diagram



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Title: CLK Block Diagram

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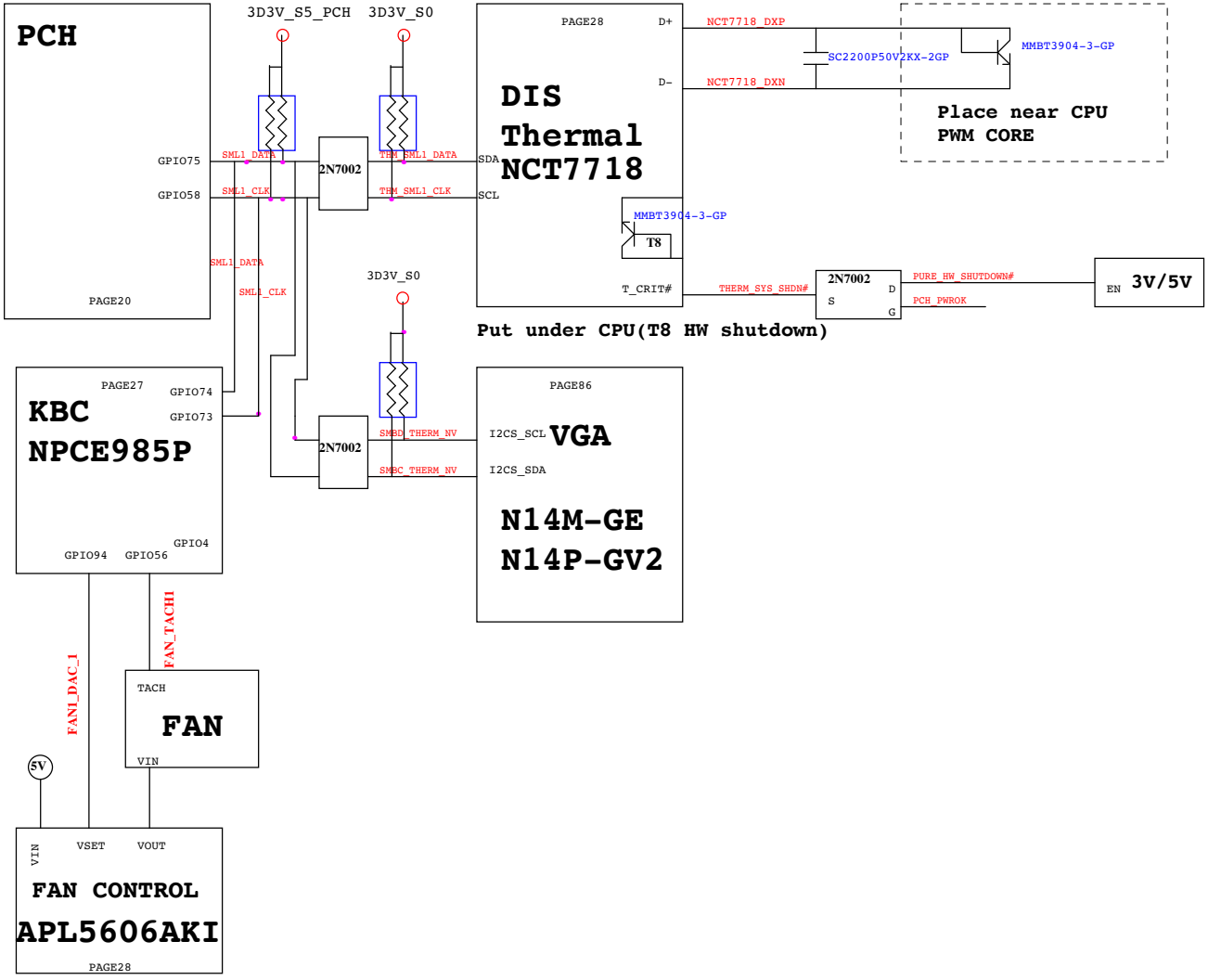
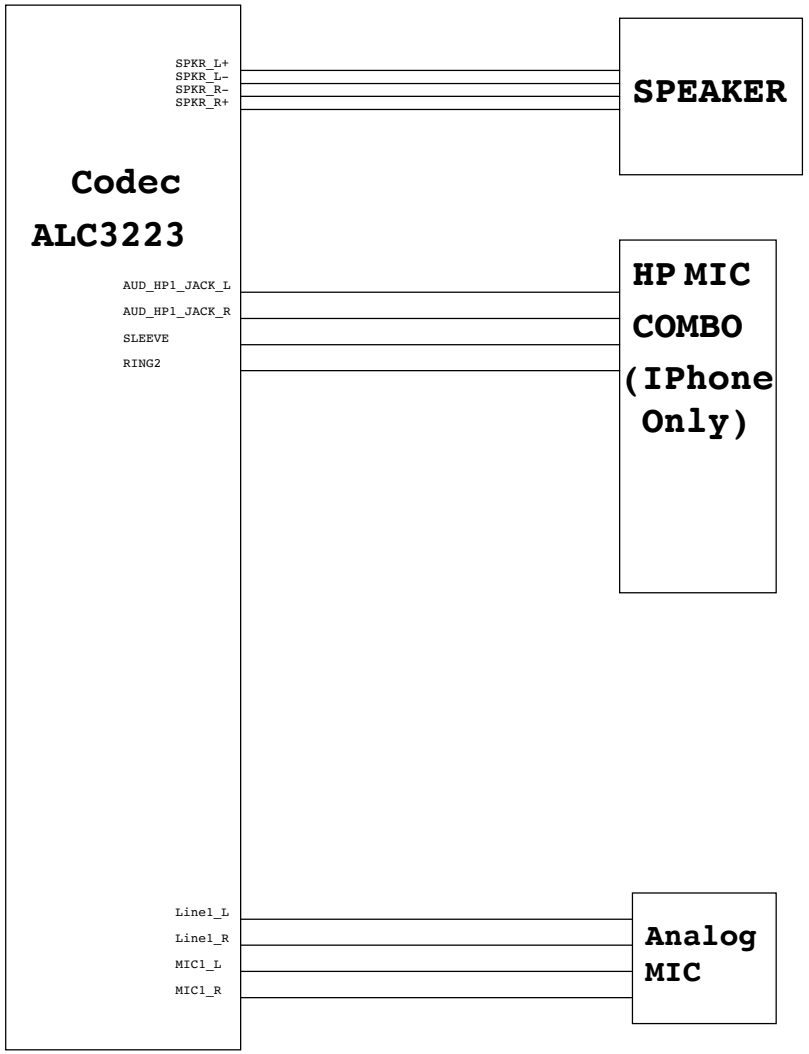
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	2/26	17	XDP_DBRESET# 10K to 3.3V	EE
		2/26	17	PCH_Wake# to 1K and DY R1705	EE

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Title: Change History

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VERSION	DATA	PAGE	Change Iteam

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Title: Change History

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