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A78DG-A2T (RS780D&SB750)

REV 6.0

AMD AM2+

DDR2 X 4 (Dual channel)

PCI-EX16 X 1

PCI-EX1 X 2

PCI X 3

RELTEK 10/100/1000 PCI-E Lan

 映泰股份有限公司 BIOS STAR GROUP			
Title COVER			
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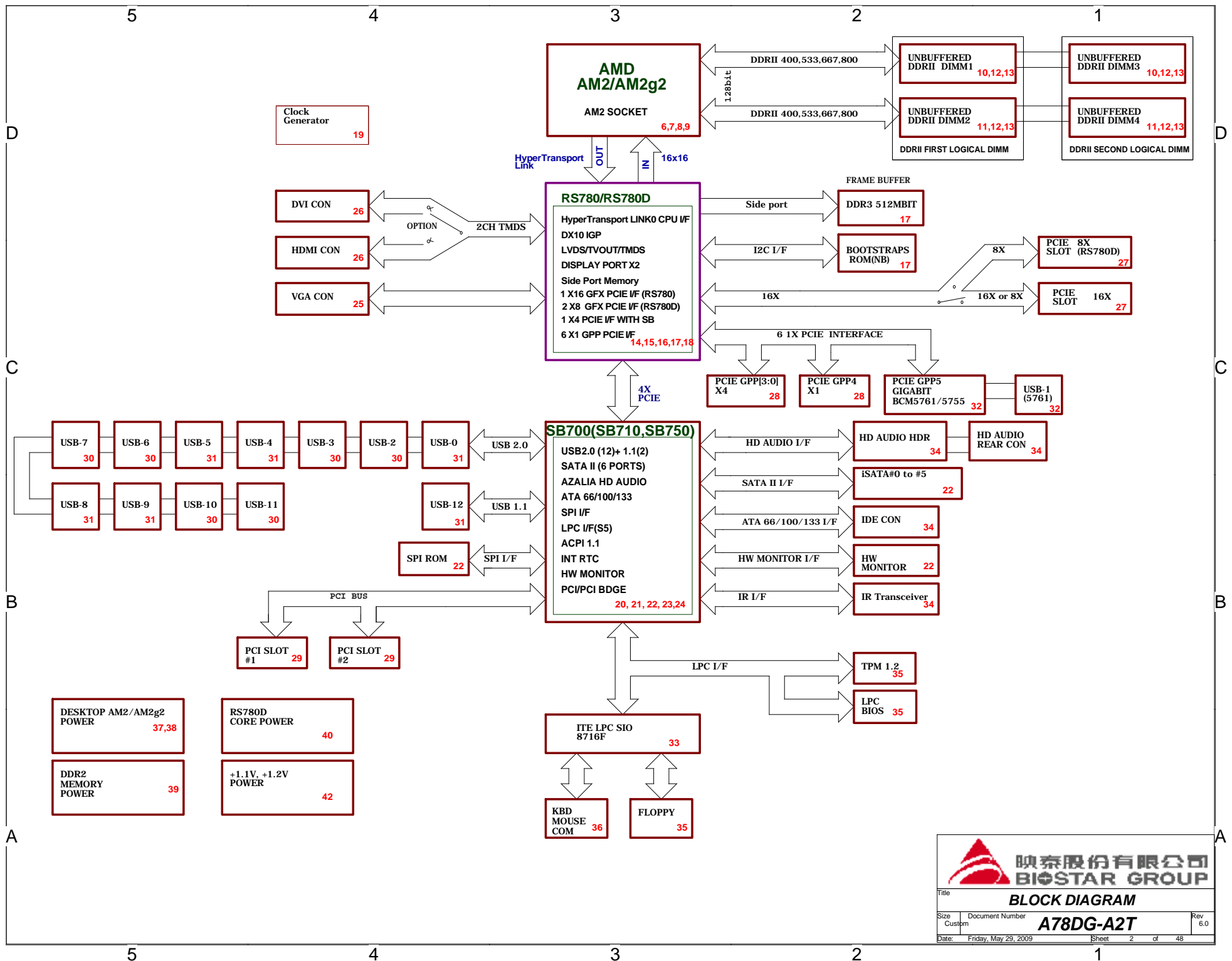
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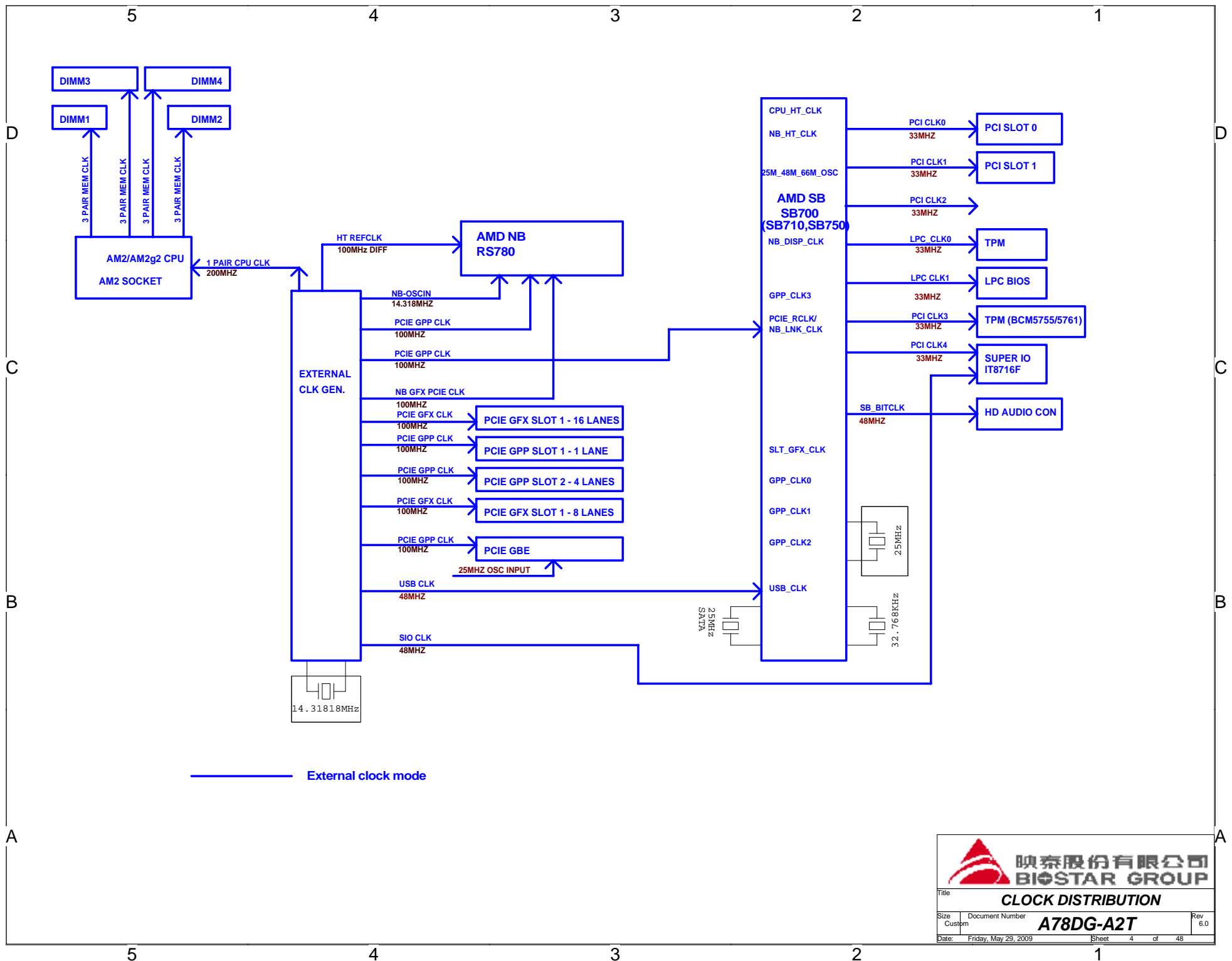
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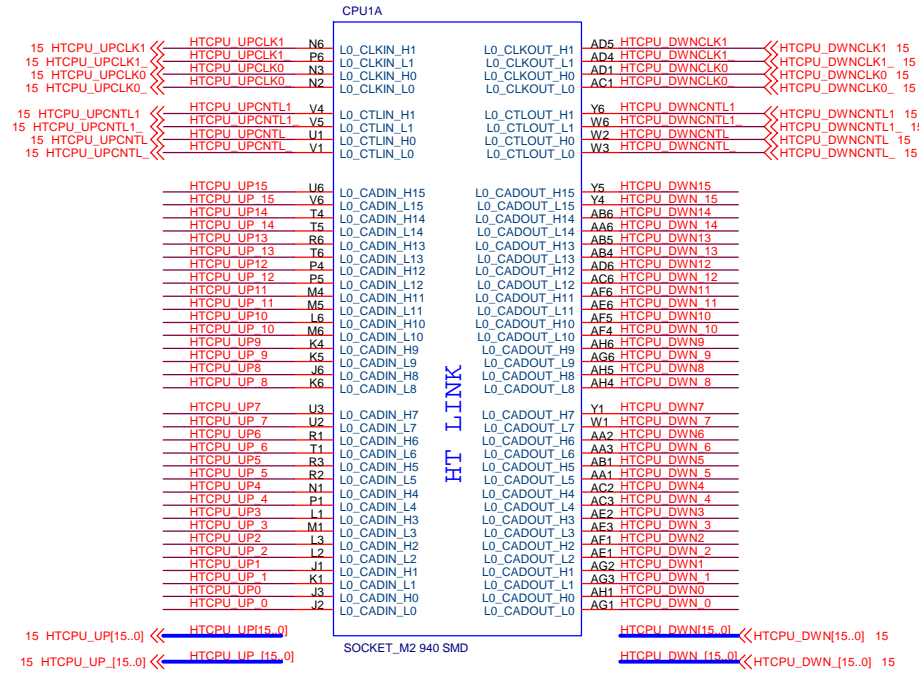
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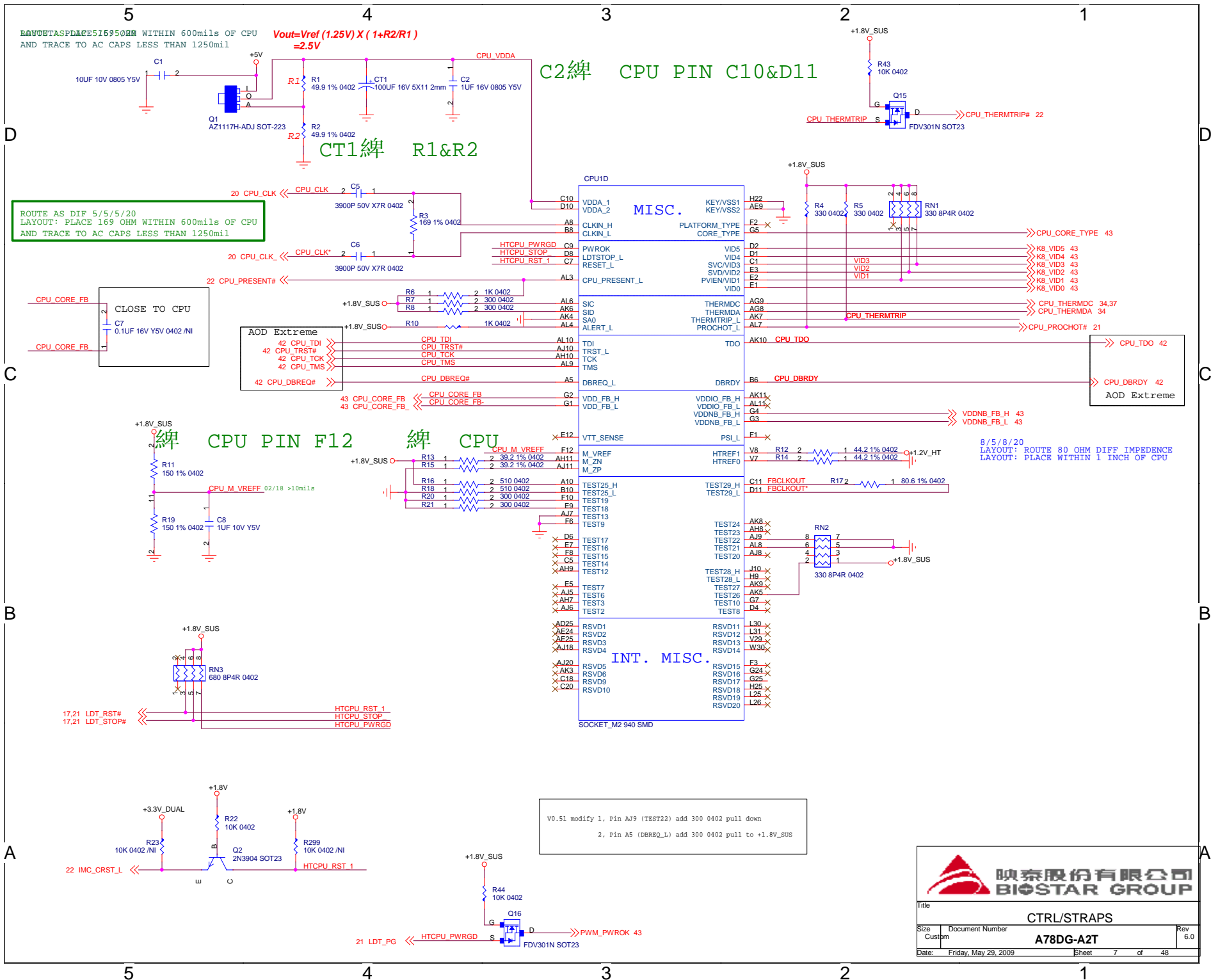
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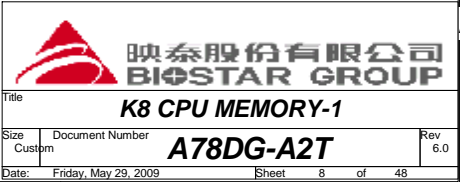


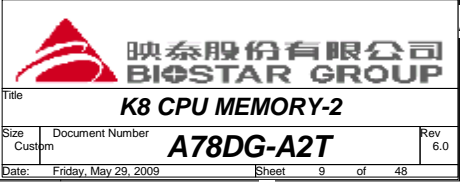


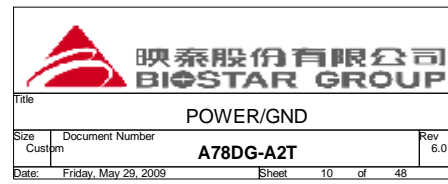
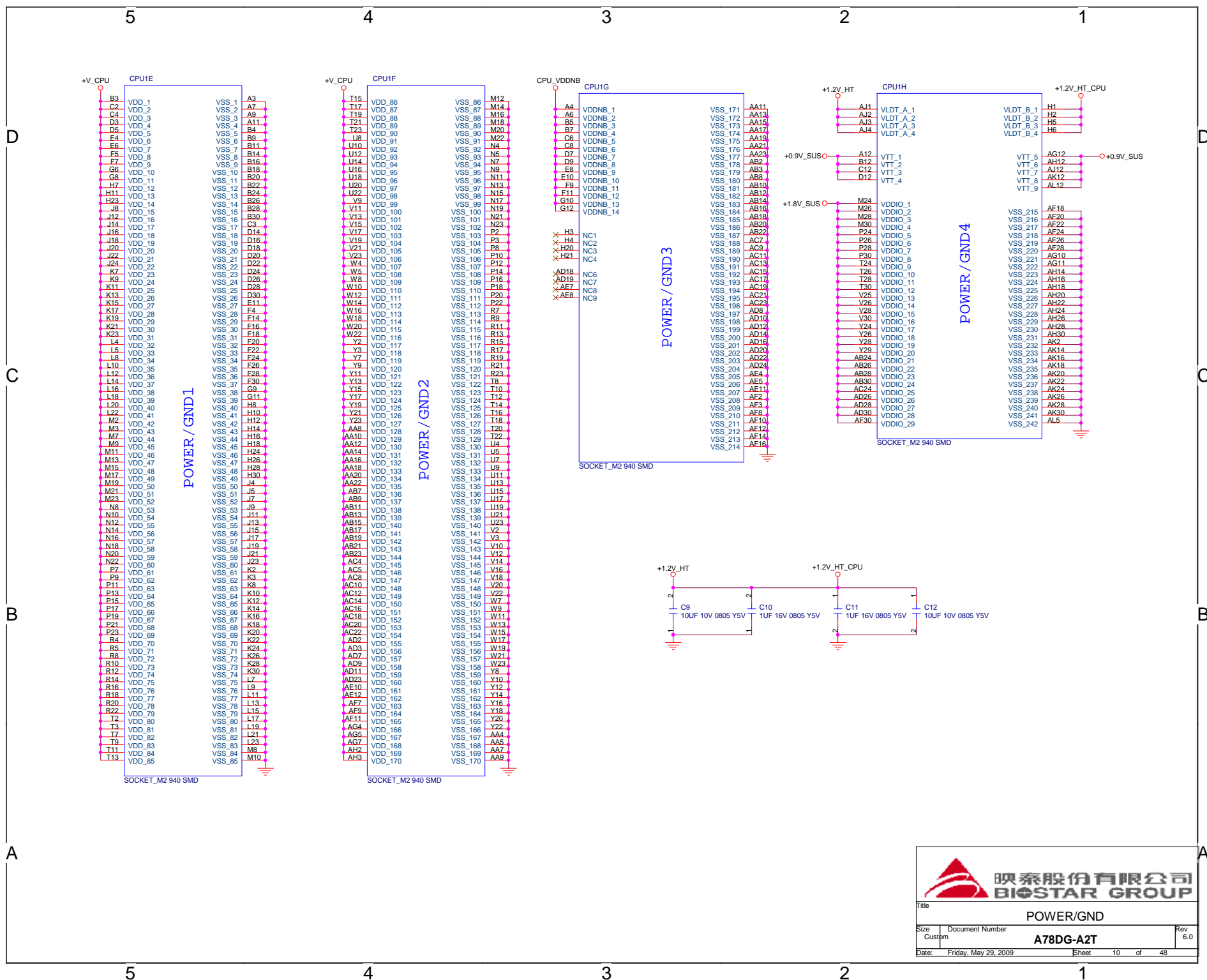
HyperTransport





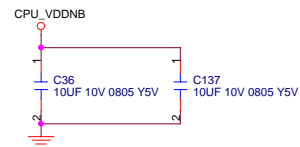
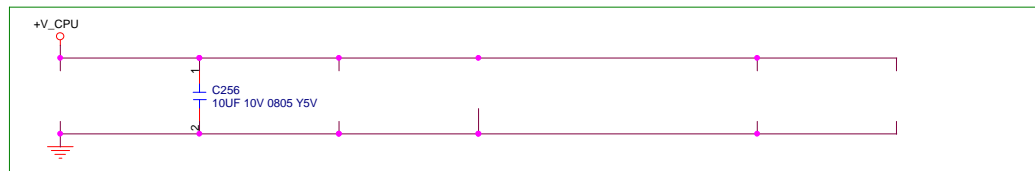
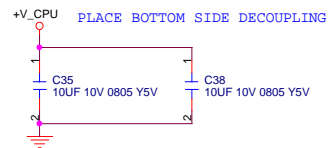
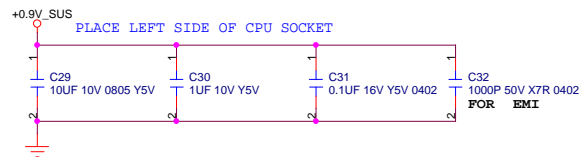
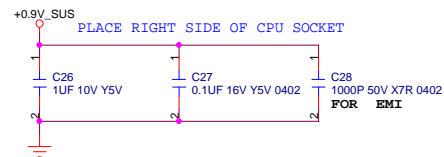
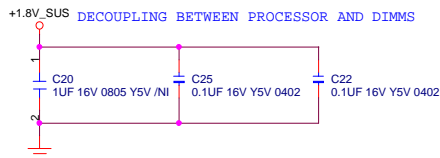
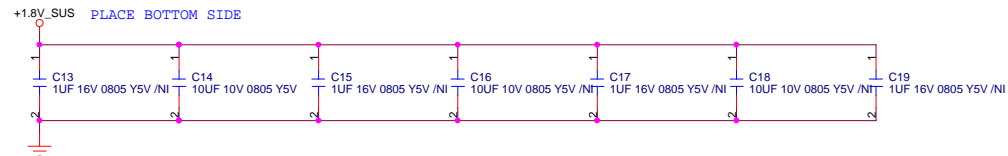


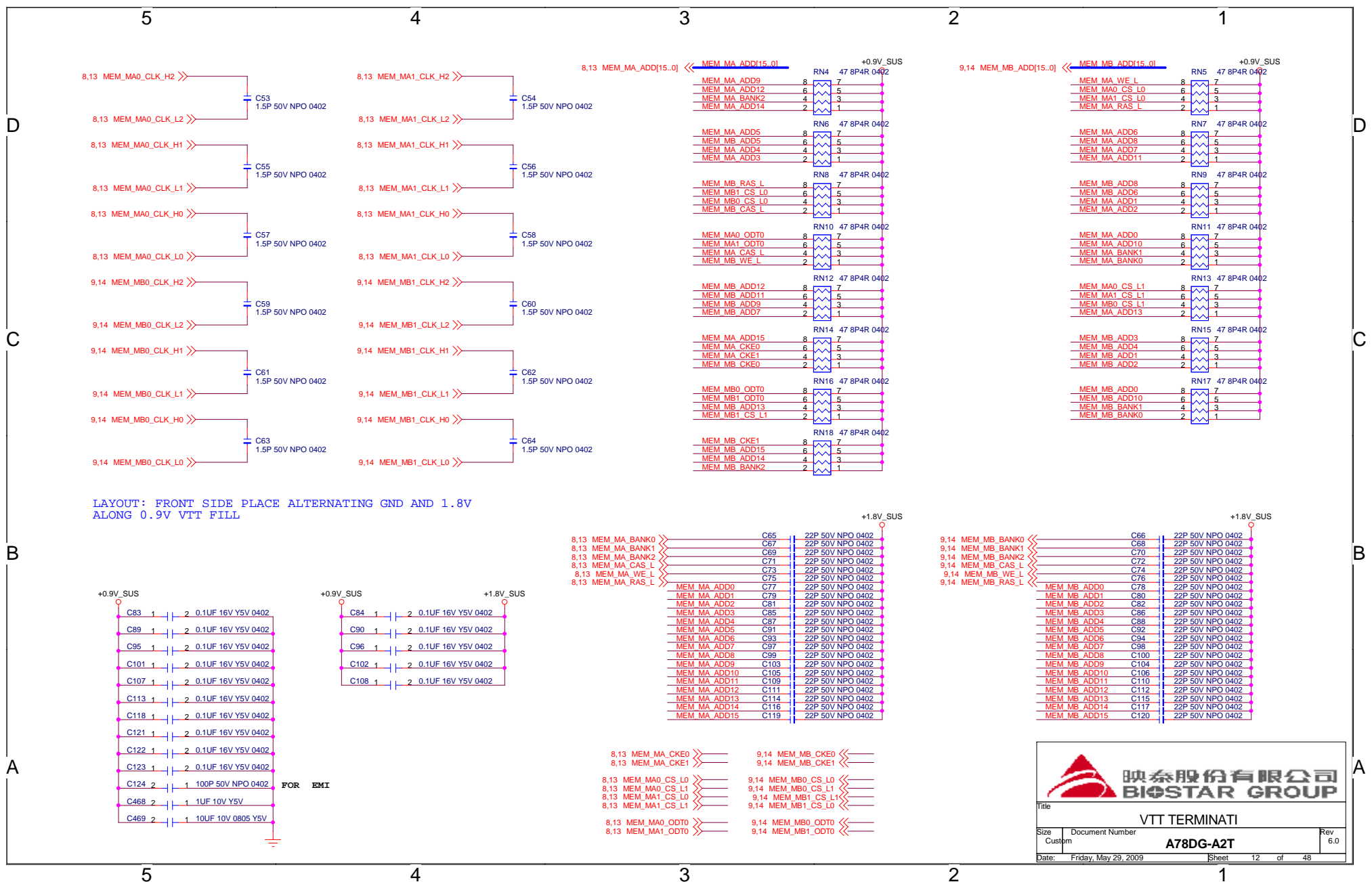


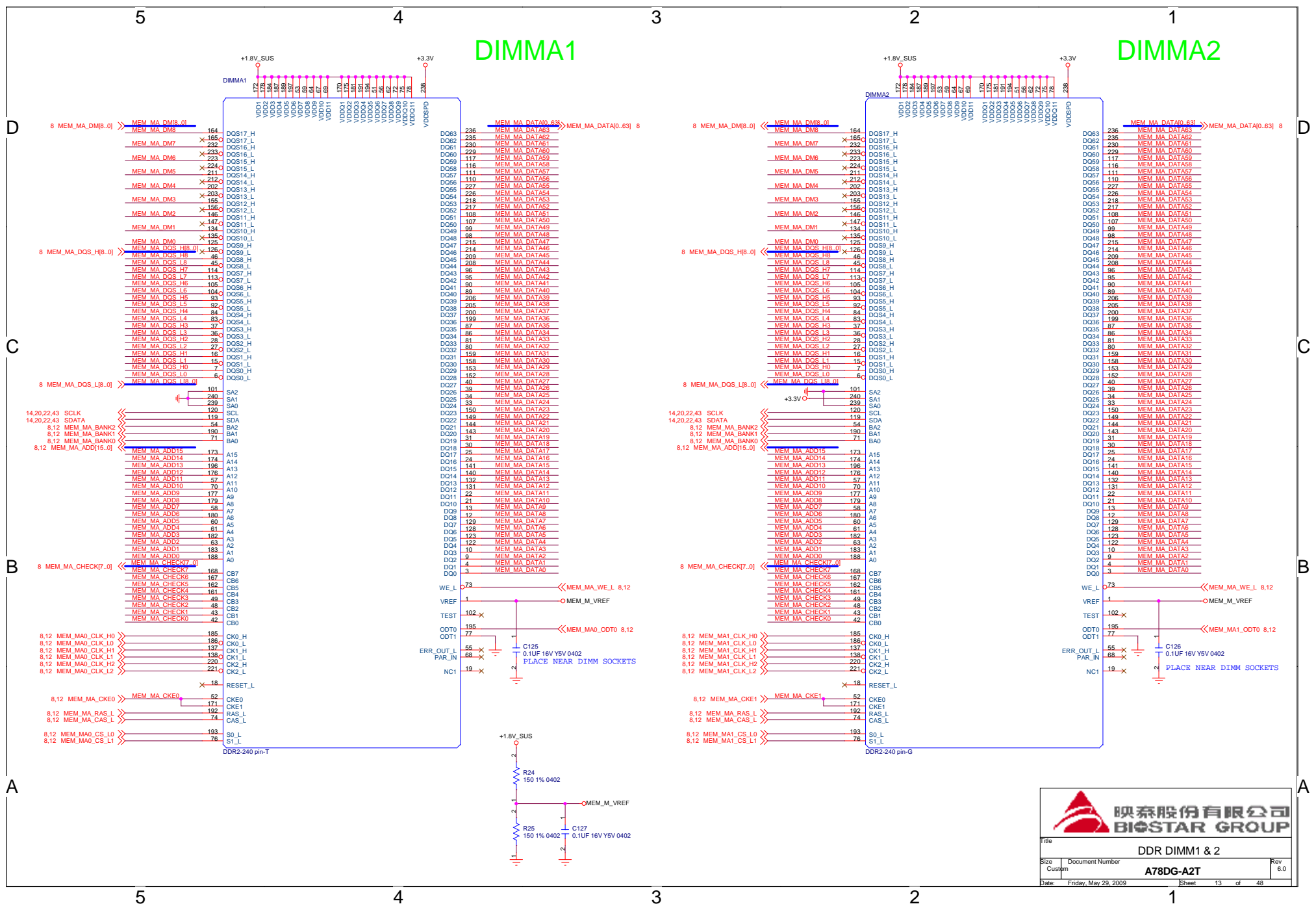


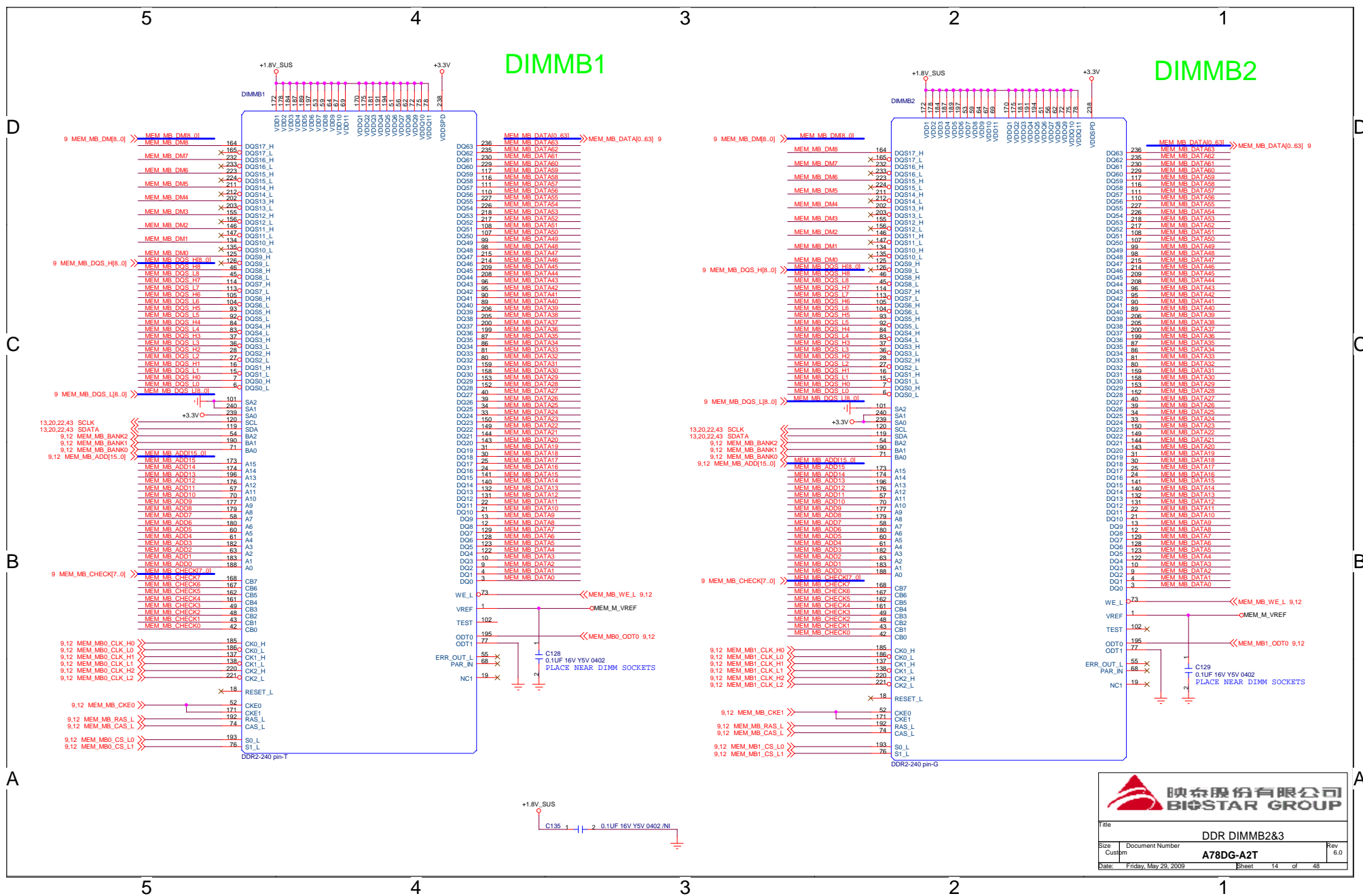
BC 笨 簿 夕 pB 奔 ㊦

02/27 BC249=>NI 02/27 BC250=>NI 02/27 BC251=>NI 02/27 BC252=>NI 02/27 BC253=>NI 02/27 BC254=>NI
02/27 BC262=>NI

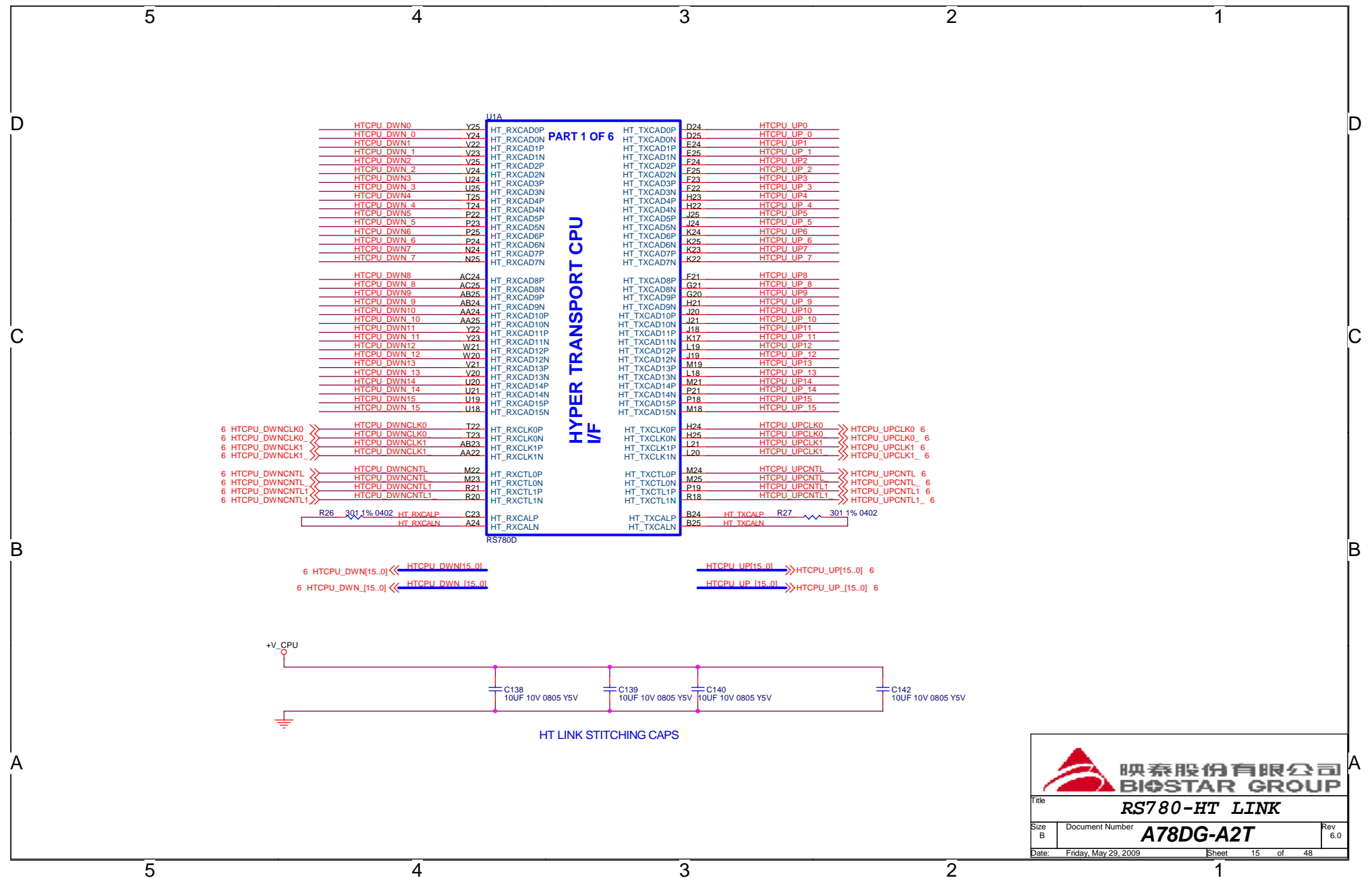


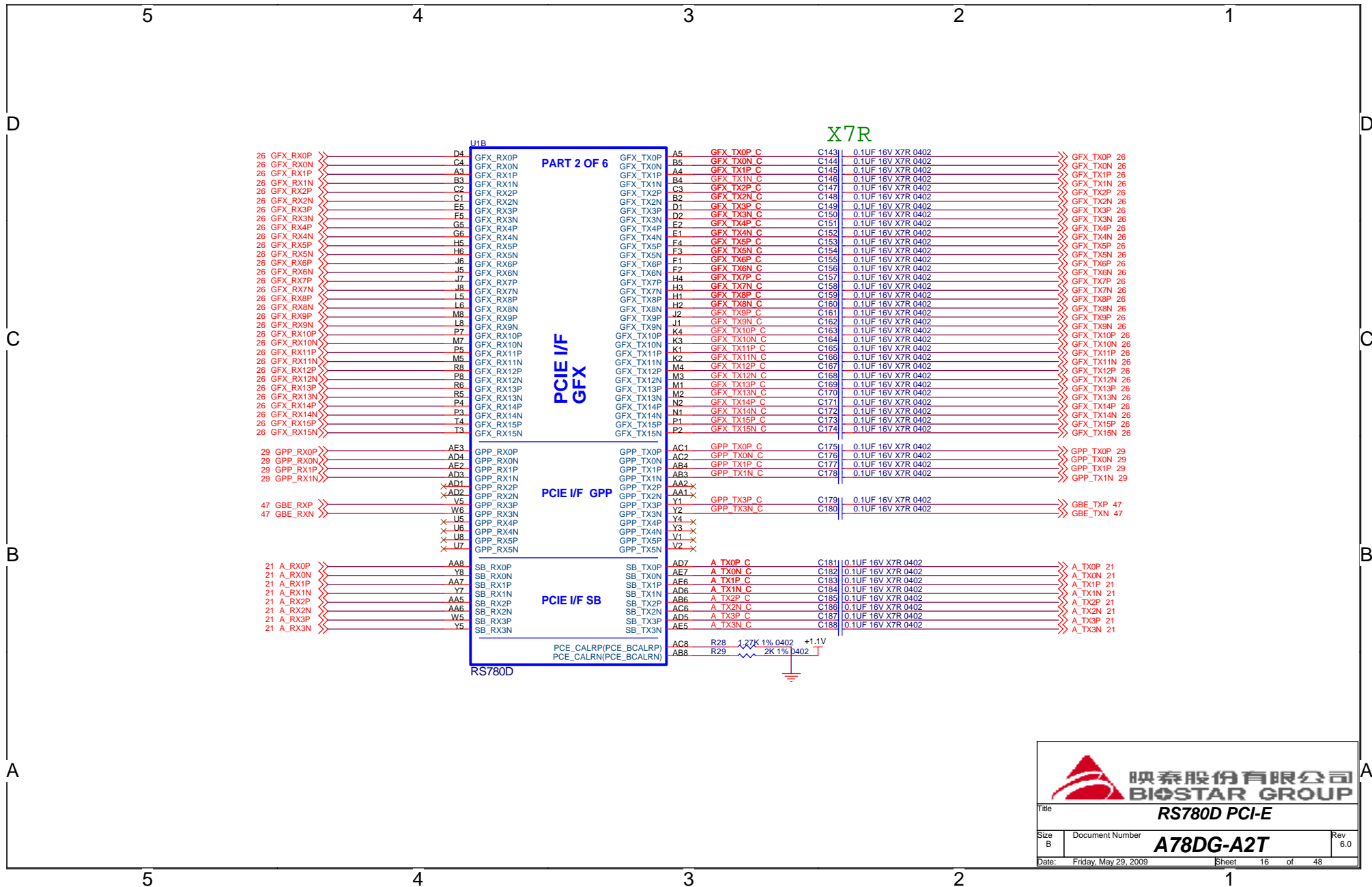


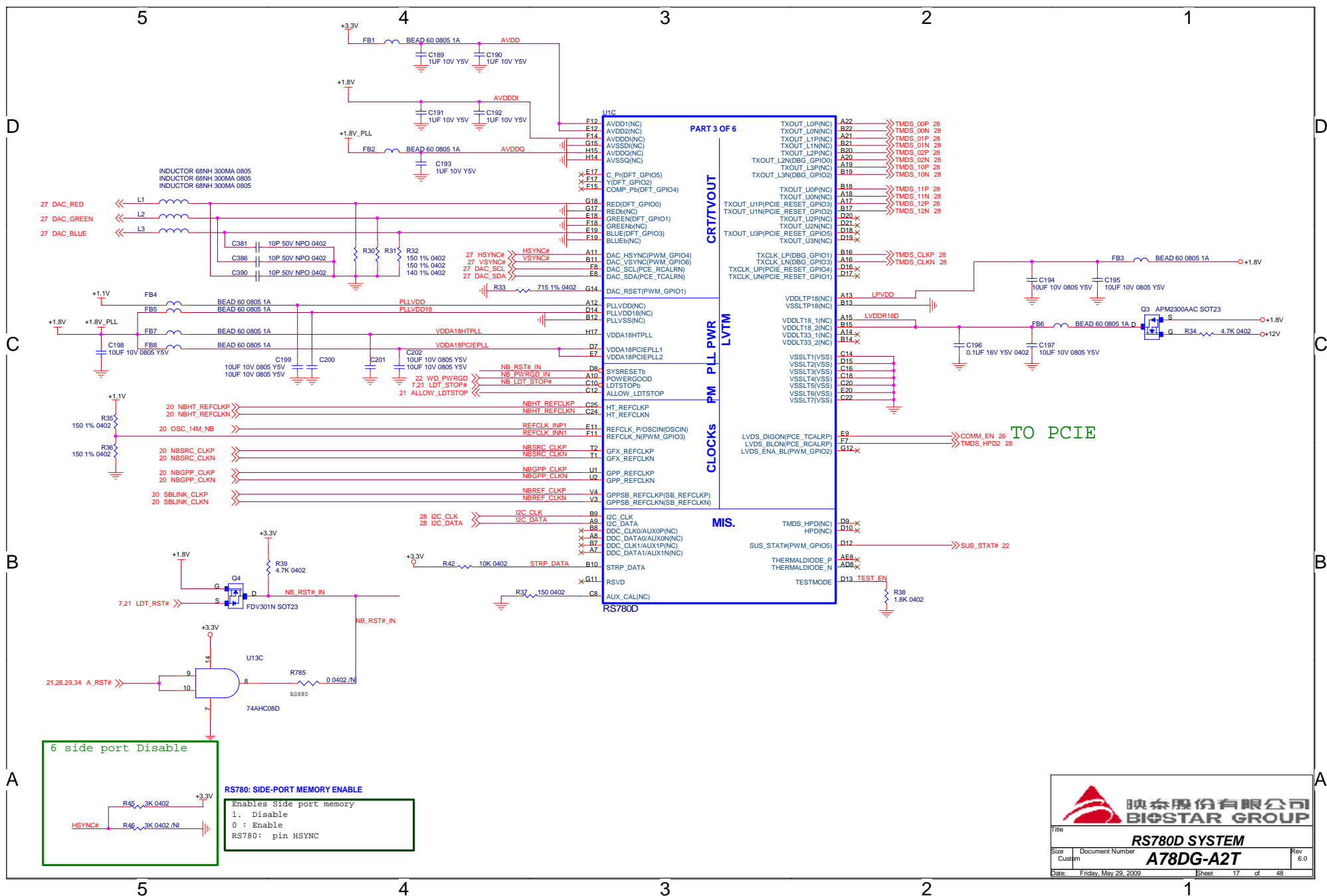


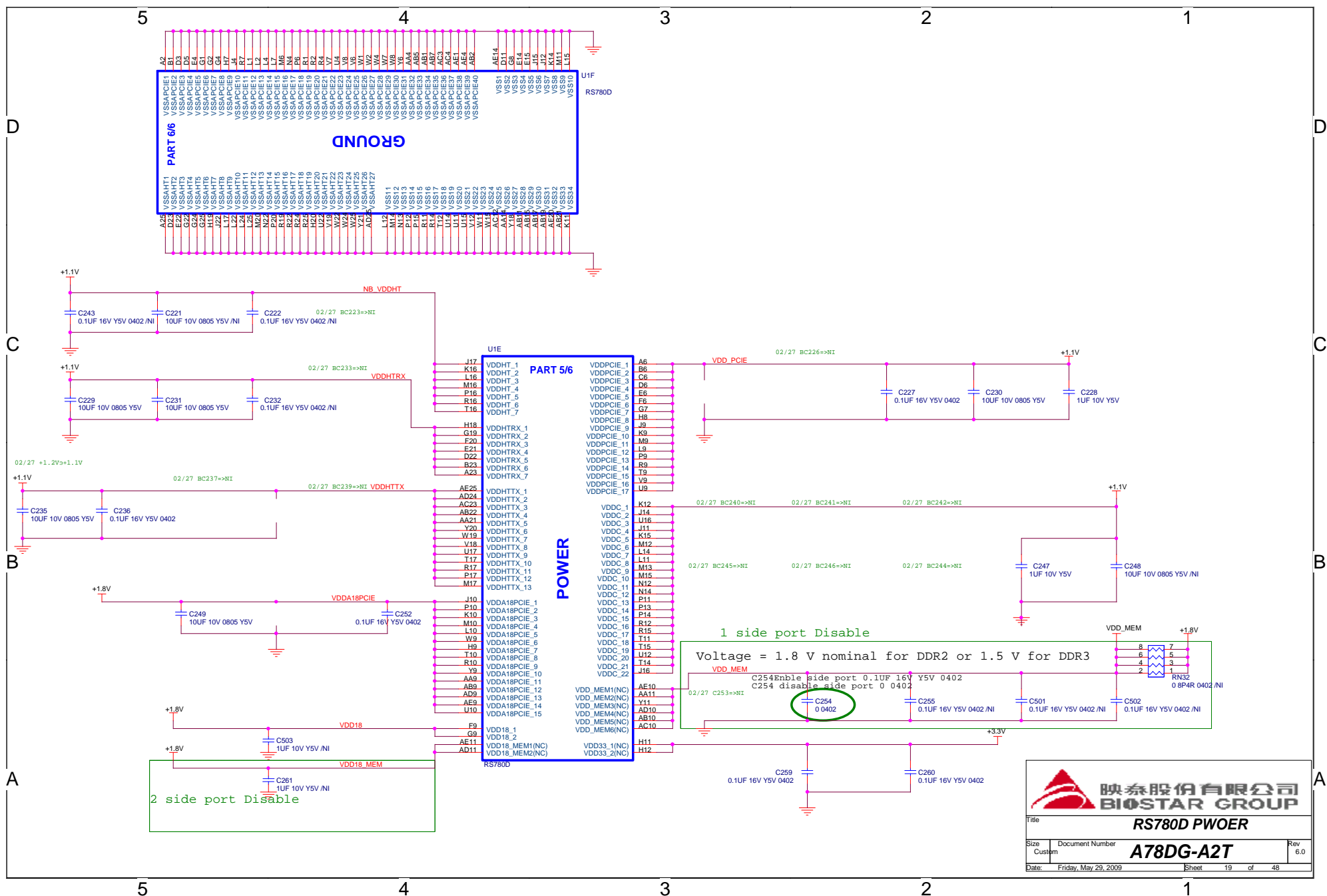


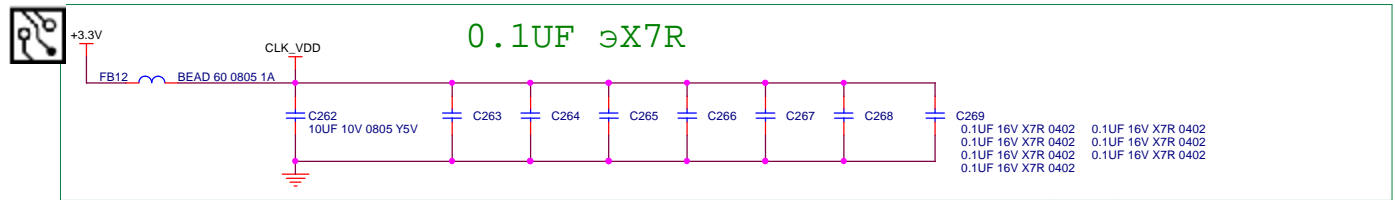
Title				DDR DIMMB2&3			
Size	Document Number						Rev
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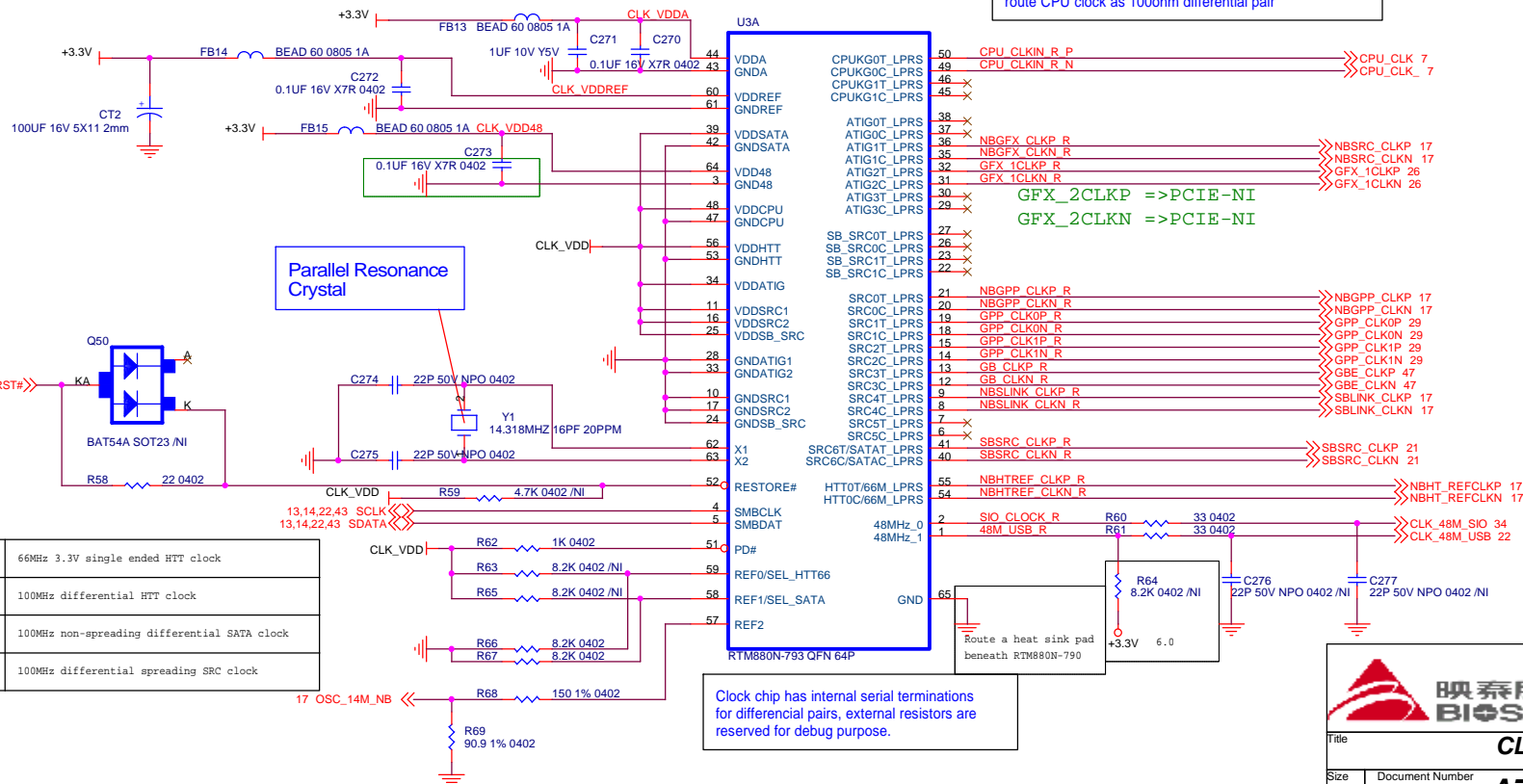






1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE TO U800 AS
POSSIBLE ALL SRCCLKTx AND SRCCLKCx
AS DIFFERENT PAIR RULE
2- PLACE ALL DECOUPLING CAPS CLOSE TO U800
POWER PIN

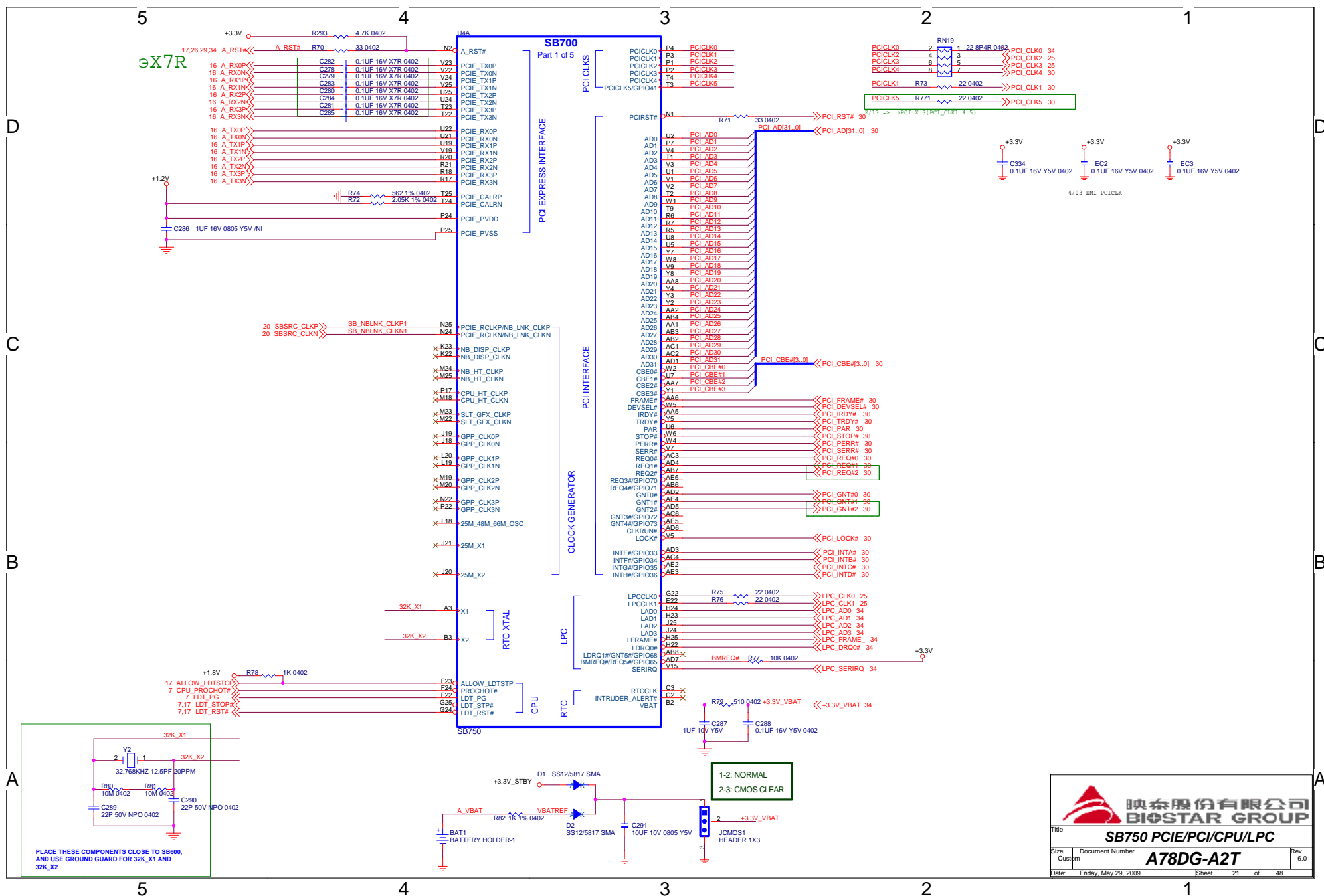
Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

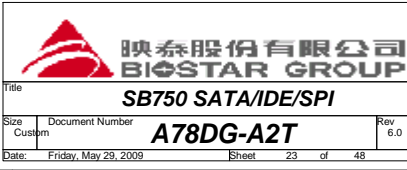


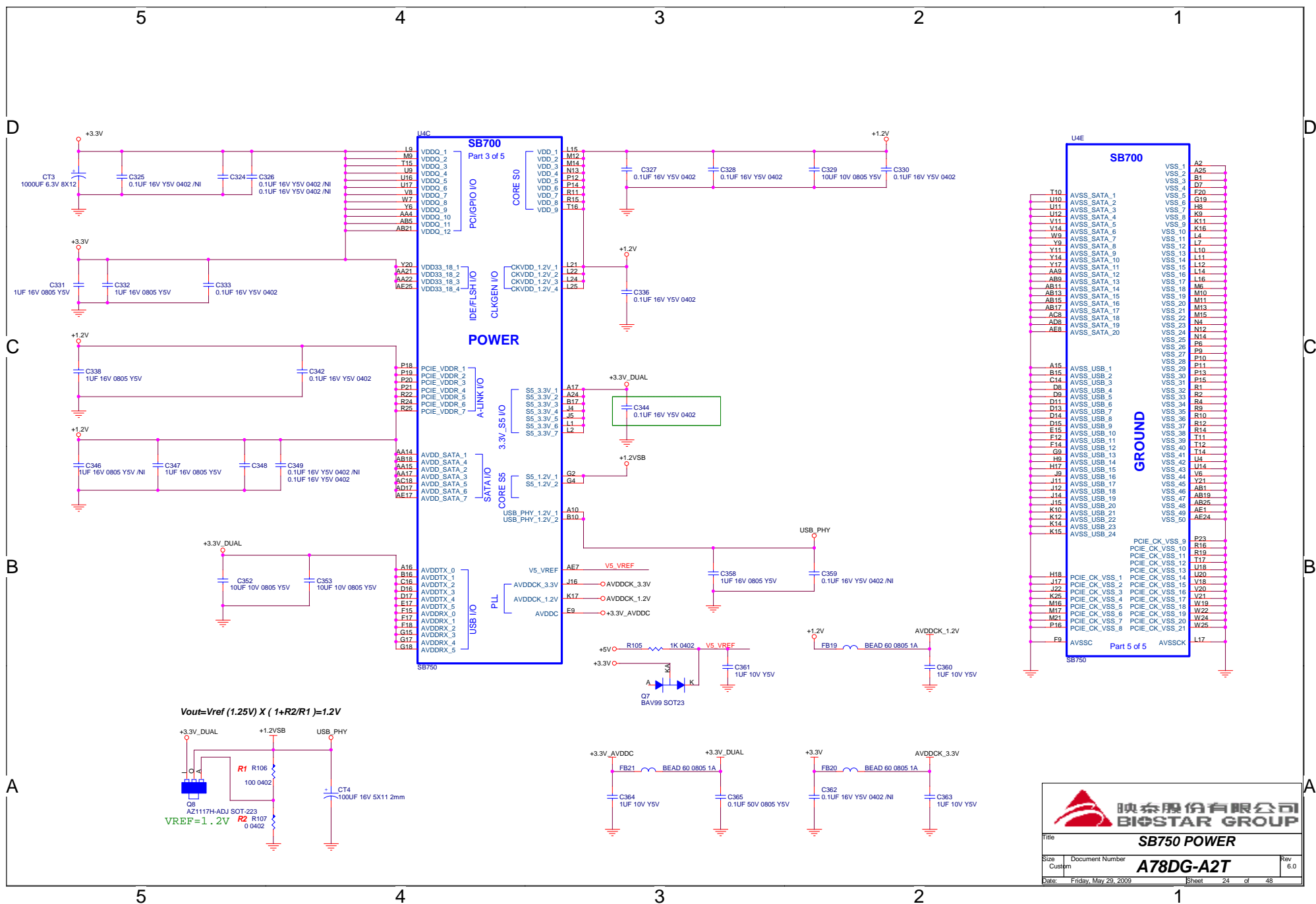
Clock chip has internal serial terminations
for differential pairs, external resistors are
reserved for debug purpose.

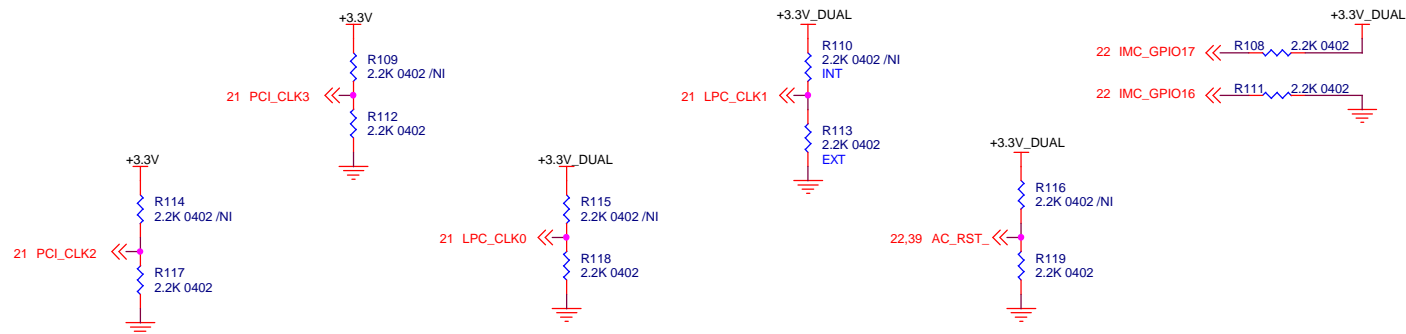


Title			CLOCK GEN
Size	Document Number	A78DG-A2T	
B		Rev 6.0	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED ADO Extreme	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT		

Title

SB750 STRAP

Size

Custom

Document Number

A78DG-A2T

Rev

6.0

Date:

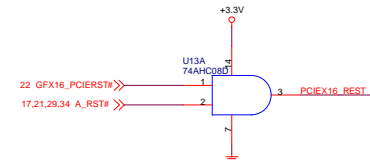
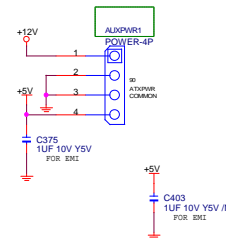
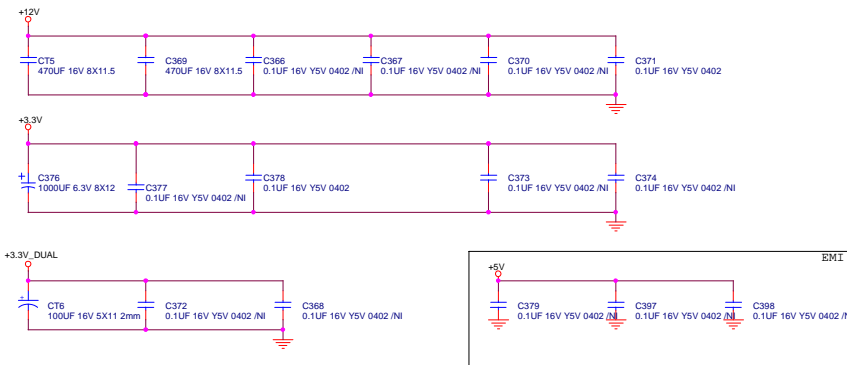
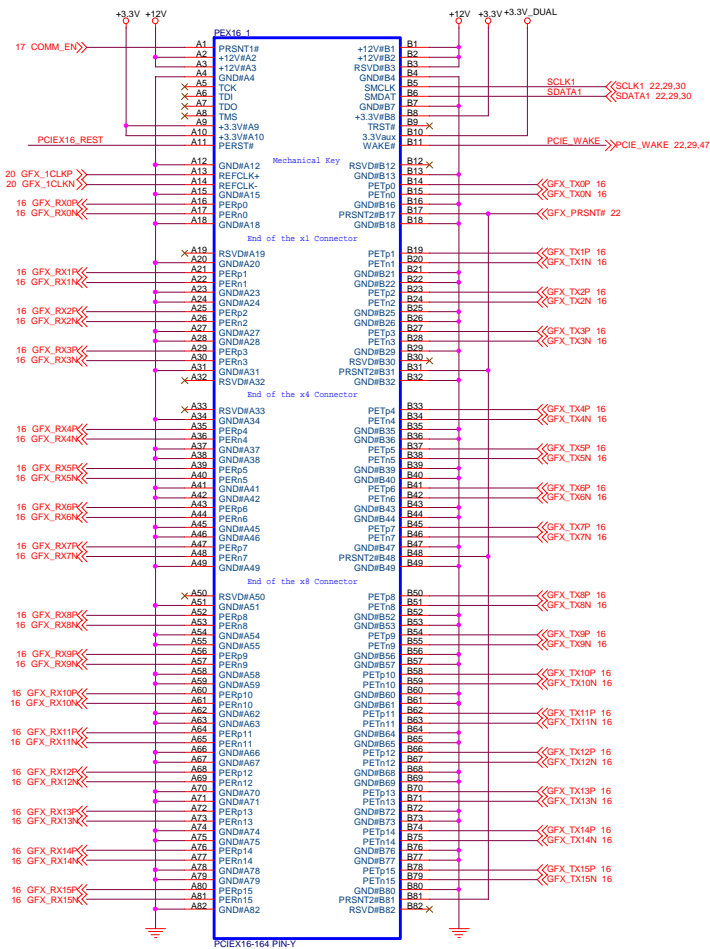
Friday, May 29, 2009

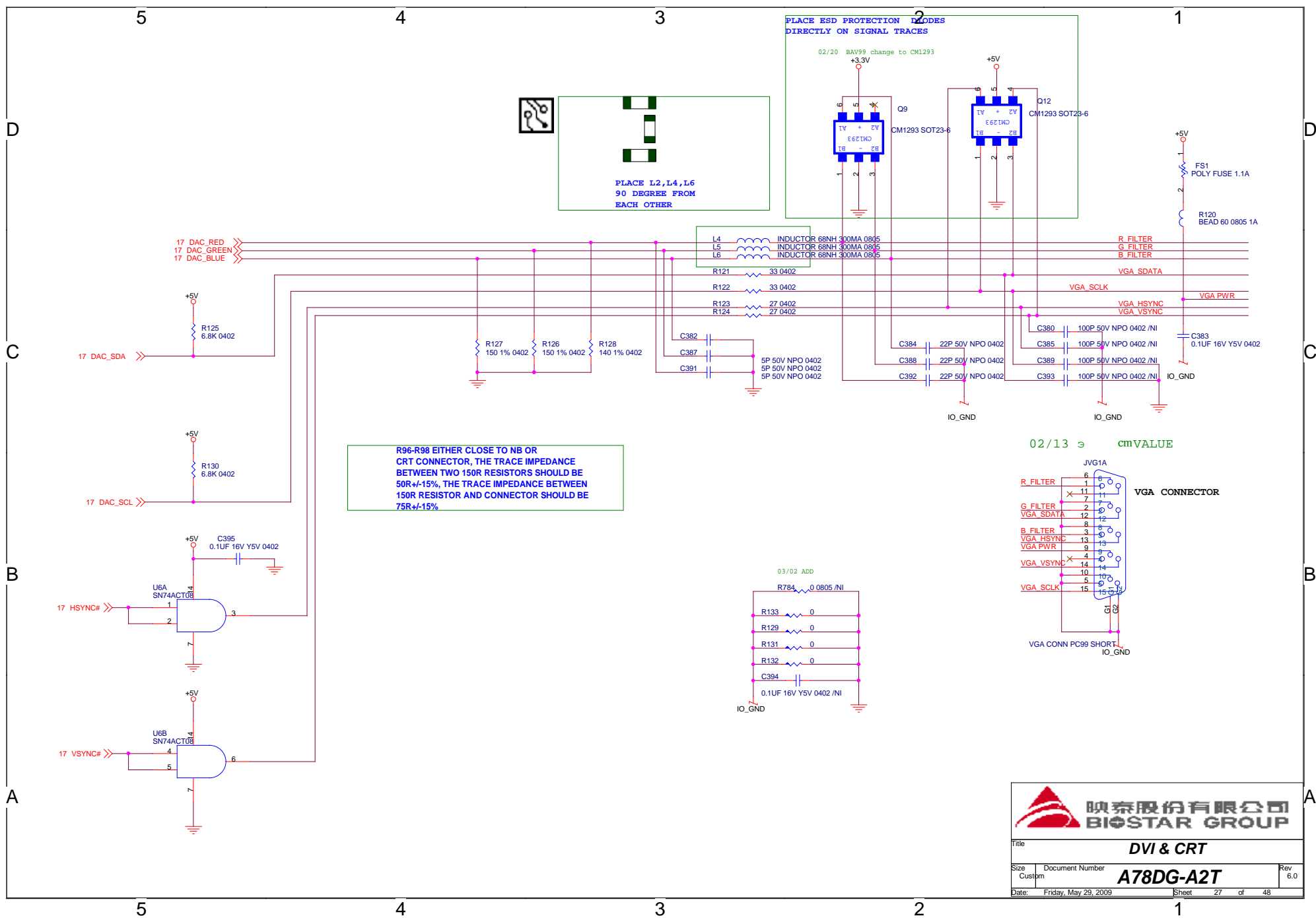
Sheet

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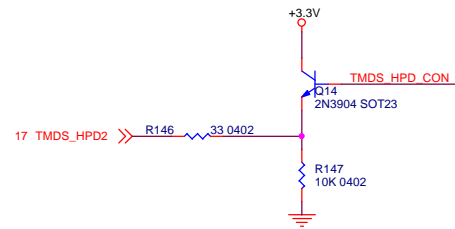
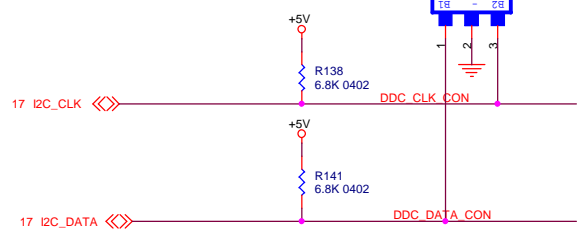
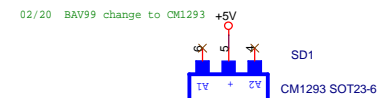
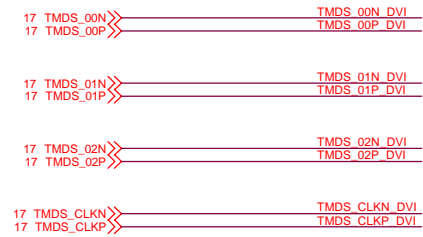
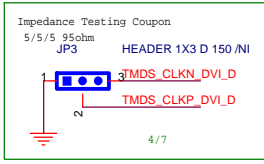
of

48

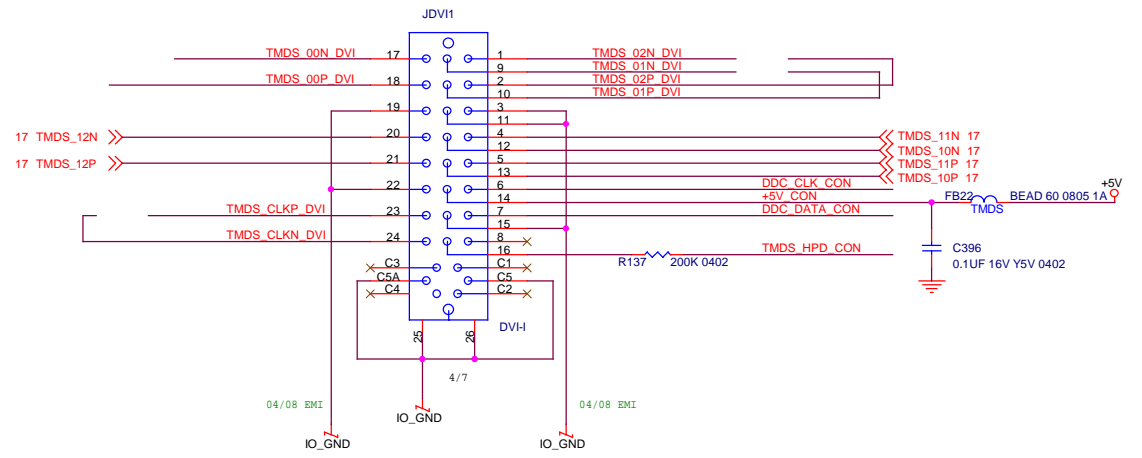




SHARE COMMON PADS
AVIOD STUB



02/13 9



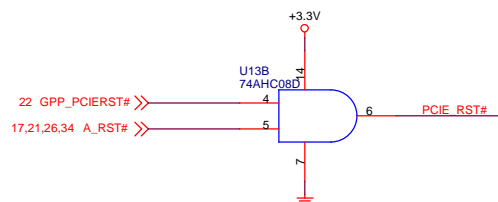
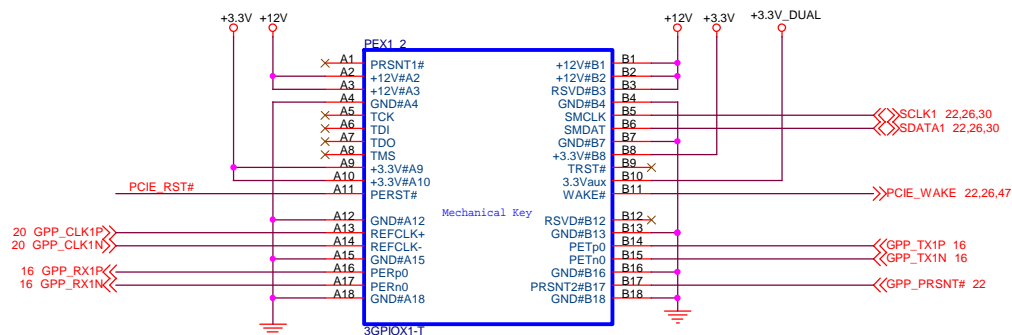
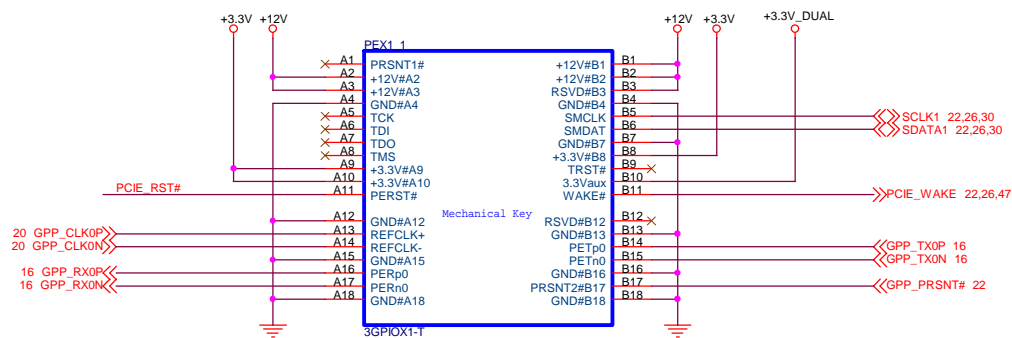
- TMDS_00N_DVI R272 110 1% 0402 /NI TMDS_00P_DVI
- TMDS_01N_DVI R274 110 1% 0402 /NI TMDS_01P_DVI
- TMDS_02N_DVI R273 110 1% 0402 /NI TMDS_02P_DVI

- TMDS_CLKN_DVI R279 110 1% 0402 /NI TMDS_CLKP_DVI

- TMDS_12N R307 110 1% 0402 /NI TMDS_12P
- TMDS_11N R308 110 1% 0402 /NI TMDS_11P
- TMDS_10N R309 110 1% 0402 /NI TMDS_10P

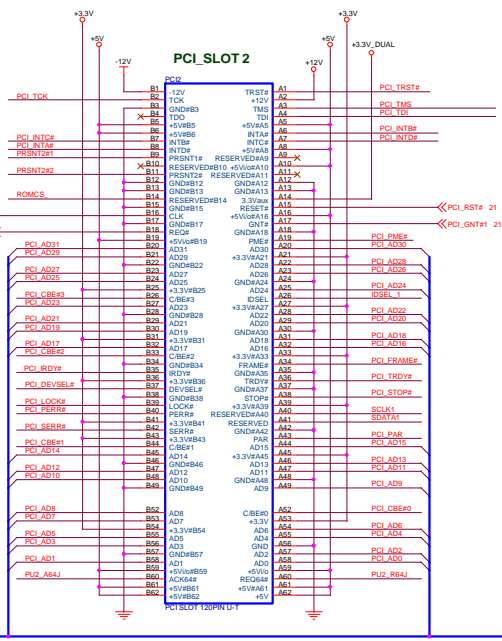
HDMI
02/13 HDMI/NI

Title		DVI/HDMI	
Size B	Document Number	A78DG-A2T	
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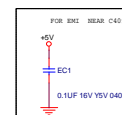
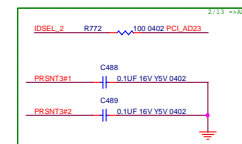
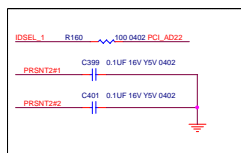
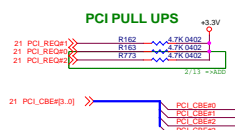
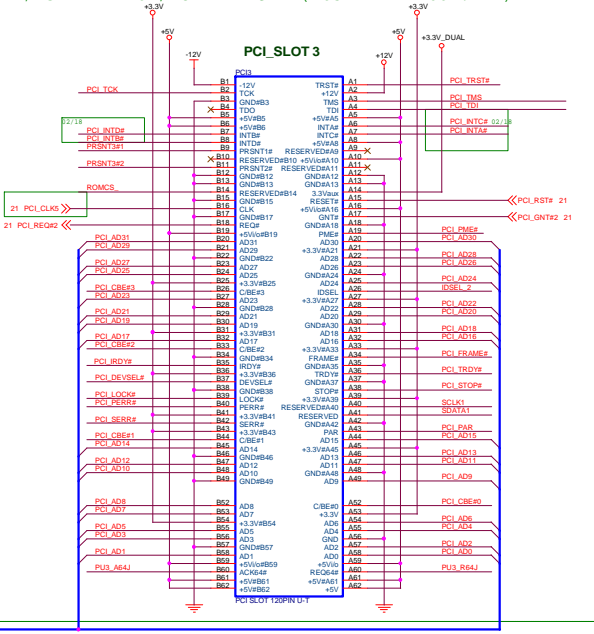


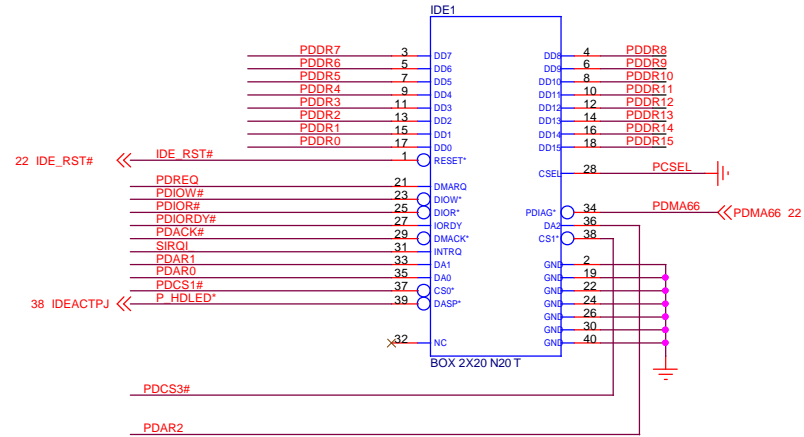
Title PCIE_X1&MDV_SOLT			
Size B	Document Number A78DG-A2T		Rev 6.0
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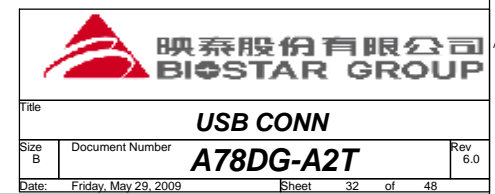
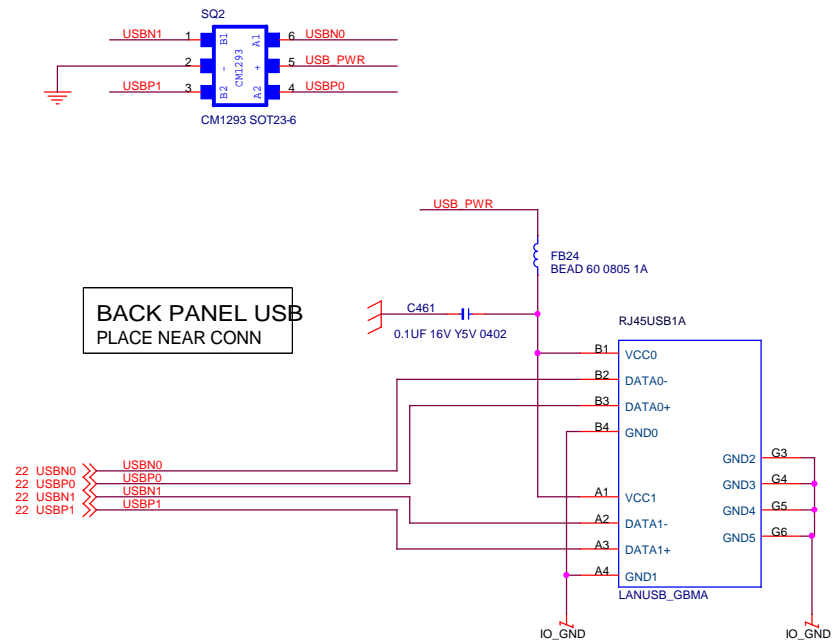
+5V IDSEL:AD22 , INT:BCDA , REQ1 & GNT1 , PCI_CLK4

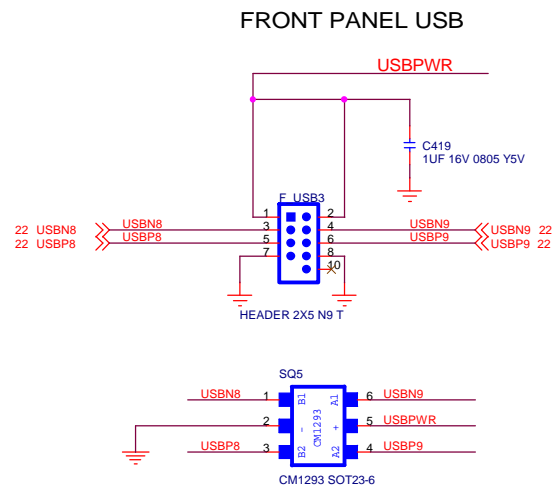
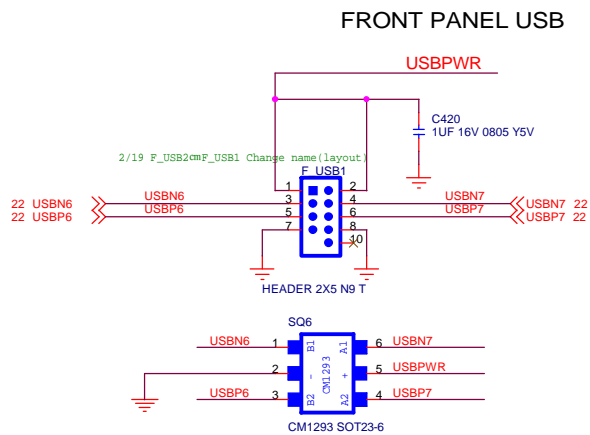
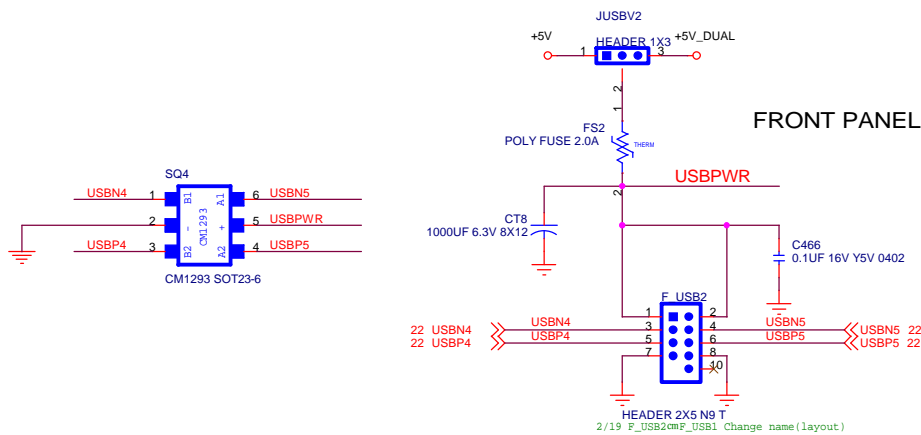


PCI SLOT 3









JP1 : SPI INTERFACE (PIN121)
1 : Disabled
0 : Enabled

JP2 : VID Output Function(PIN122)
1 : Disabled
0 : Enabled

JP3 : Chipset Select (PIN124)
1 : Chip 1
0 : Chip 0

JP4 : PCIRST#1-4 Output Buffer (PIN1)
1 : Open-Drain
0 : Push-Pull

JP7 : WDT to Reset PWROK (PIN46)
1 : Disabled
0 : Enabled

For over-voltage GPIO select

1, Powered By VCCH

2, DIOD8 (Open-Drain)

Pin 20-21 FOR CHIPSET CORE VOLTAGE

Pin 22-23 FOR CPU_VTT

Pin 24-25 FOR CPU VCORE

Pin 26, 27 & 70 FOR MEM. VOLTAGE

CONTROL PWM AUTO PHASE GPIO

+5V_DUAL ○ SR77 4.7K 0402

37 EXT_SPI# << EXT_SPI#

02/13 簡歷

VCPU_NB0 =>NI
VCPU_NB1 =>NI

TO LU2 RTL8111DL-GR LQFP48

PCIE_RST_OUT2# R177 1K 0402

ATX_PWRGD R29 1K 0402 NI

+3.3V SRN2 4.7K 8P4R 0402

EXT_SPI#

35 FAN1

35 FAN_CTL1

35 FAN2

35 FAN3

35 FAN_CTL3

44 PHASE_DETECT4#

44 PHASE_DETECT3#

44 PHASE_DETECT2#

42 VCHIP0

42 VCHIP1

42 VTT_FSB0_VHT0

42 VTT_FSB0_VHT1

42 VDMM2

42 VDMM1

42 VDMM0

35,44,45 ATX_PWRGD

47 PCIE_RST_OUT2#

17,21,26,29 A_RST#

21 LPC_DRQ0#

21 LPC_SERIRQ

21 LPC_FRAME

21 LPC_AD0

21 LPC_AD1

21 LPC_AD2

21 LPC_AD3

22 SIO_KBRST

22 A20GATE

21 PCI_CLK0

20 CLK_48M_SIO

48 95Hz

SR13 4.7K 0402

SR14 4.7K 0402

SRN1 4.7K 8P4R 0402

+5V

38 DEBUG_LED2

38 DEBUG_LED1

CTSS#

RTS#

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SRN1 4.7K 8P4R 0402

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+5V

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38 DEBUG_LED1

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SRN1 4.7K 8P4R 0402

+5V

38 DEBUG_LED2

38 DEBUG_LED1

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Temperature Sensing

TEMPIN1 << CPU_THERM0A 7

SC1 2200P 50V X7R 0402

From CPU Routed by differential

TEMPIN2 << CPU_THERM0C 7,37

NO USE FUNCTION ADD R4 -> 10K

R4

VIN7 SR12 10K 0402

3.3V

TEMPIN2

SC36 2200P 50V X7R 0402

System Thermal sensor

SR61 0.0402 NI

PWRGD_PS << PWRGD_PS 44

02/18

SR61 0.0402 NI

PWRGD_PS << PWRGD_PS 44

02/18

SR61 0.0402 NI

PWRGD_PS << PWRGD_PS 44

02/18

SR61 0.0402 NI

PWRGD_PS << PWRGD_PS 44

02/18

SR61 0.0402 NI

PWRGD_PS << PWRGD_PS 44

02/18

SR61 0.0402 NI

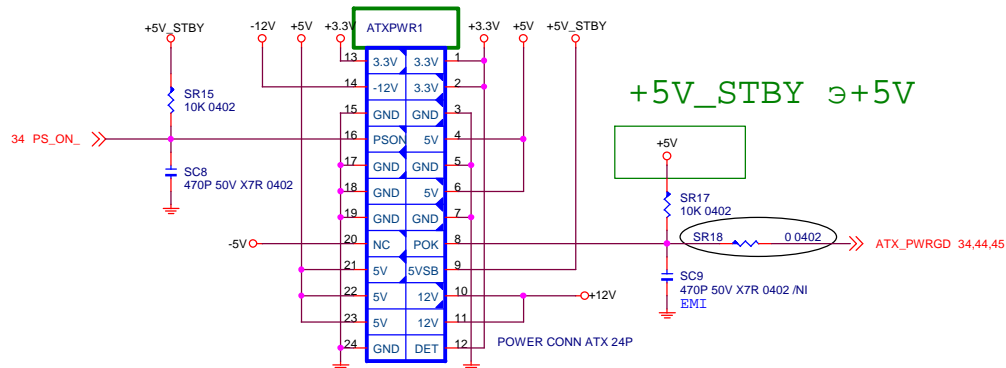
PWRGD_PS << PWRGD_PS 44

02/18

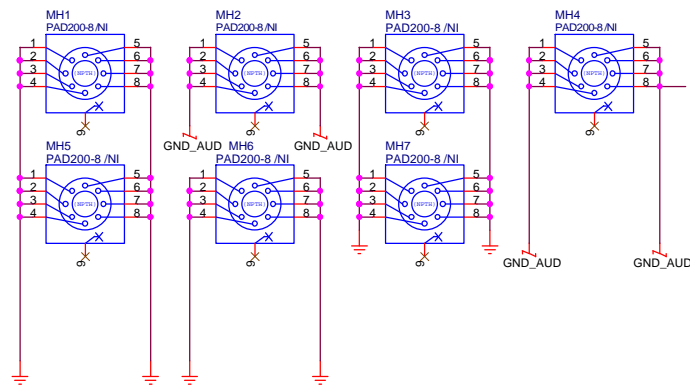
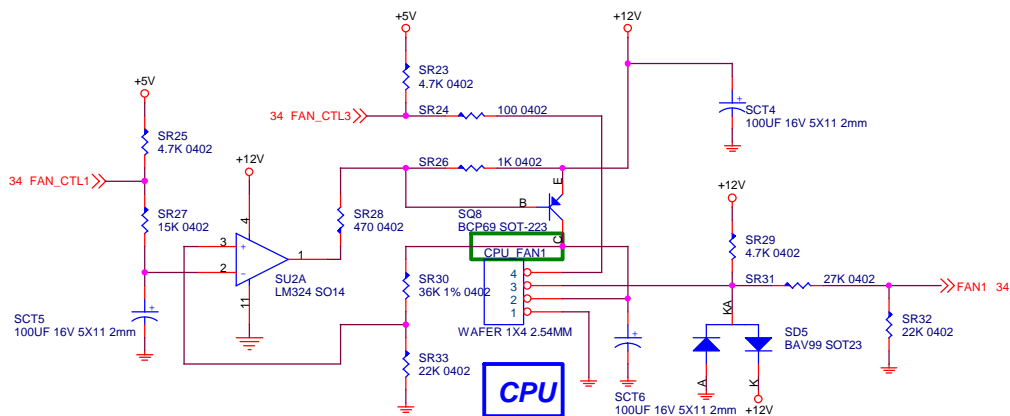
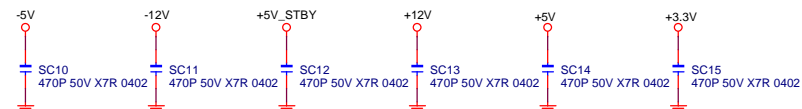
SR61 0.0402 NI

PWR

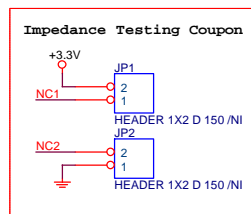
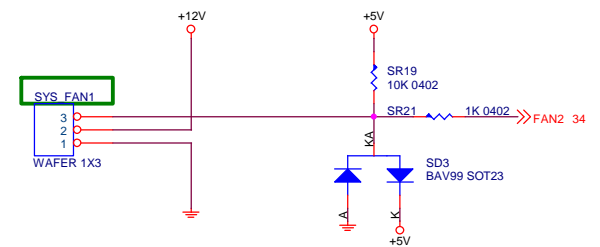
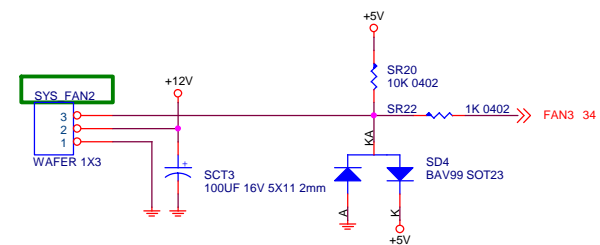
POWER CONNECTOR




EMI POWER CONN DECOUPLING

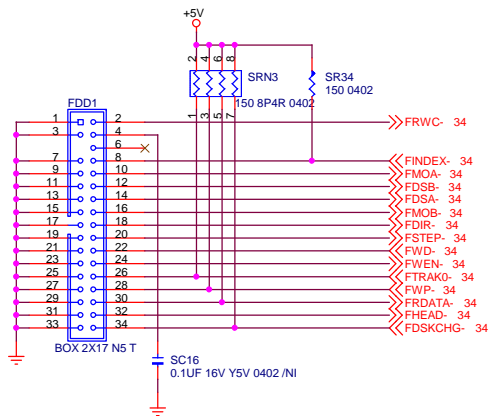


SYSTEM

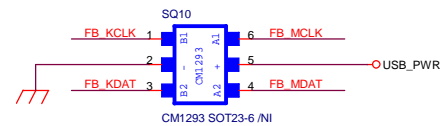
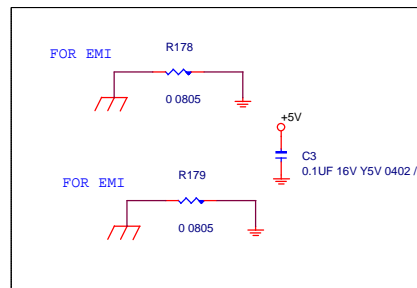
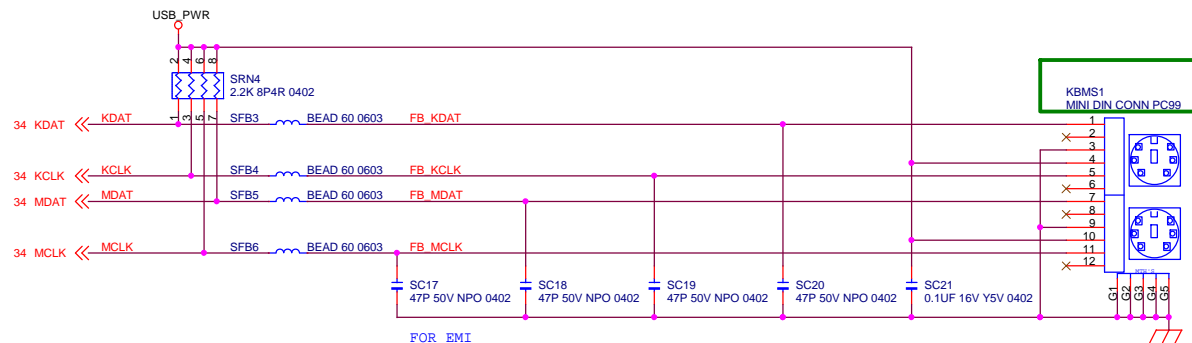


 映泰股份有限公司 BIOSSTAR GROUP		
Title FAN&POWER CONN		
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FLOPPY CONNECTOR



FOR KEYBOARD WITH MOUSE CONN.



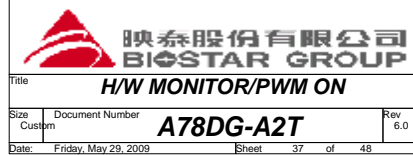
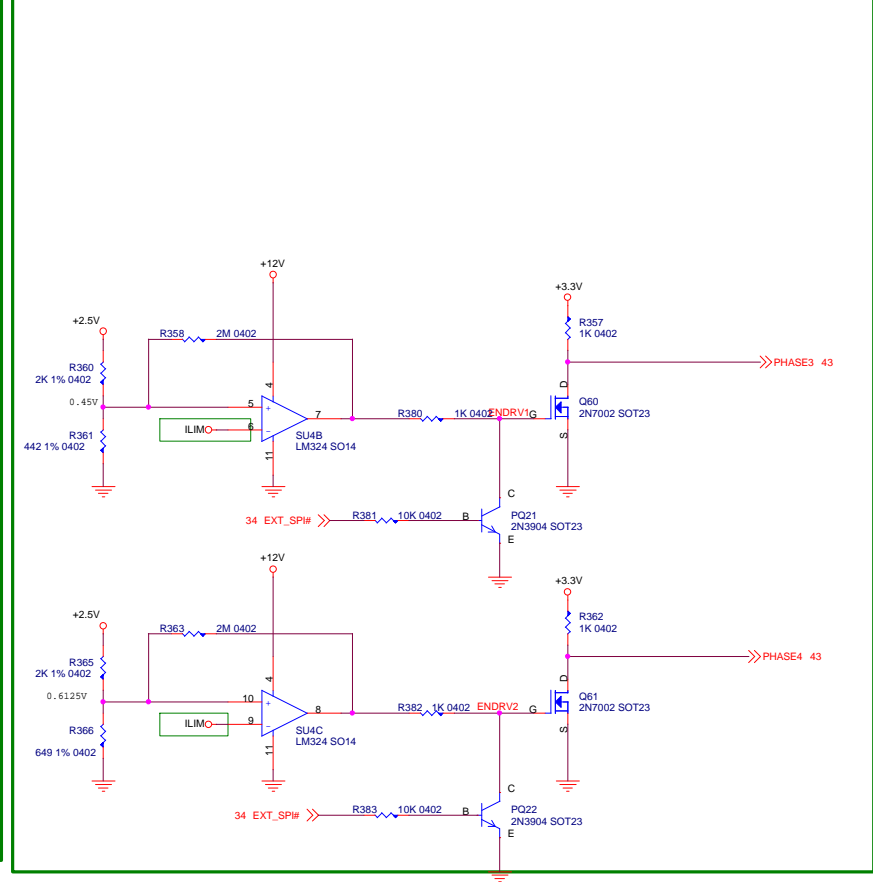
映泰股份有限公司
BIOSTAR GROUP

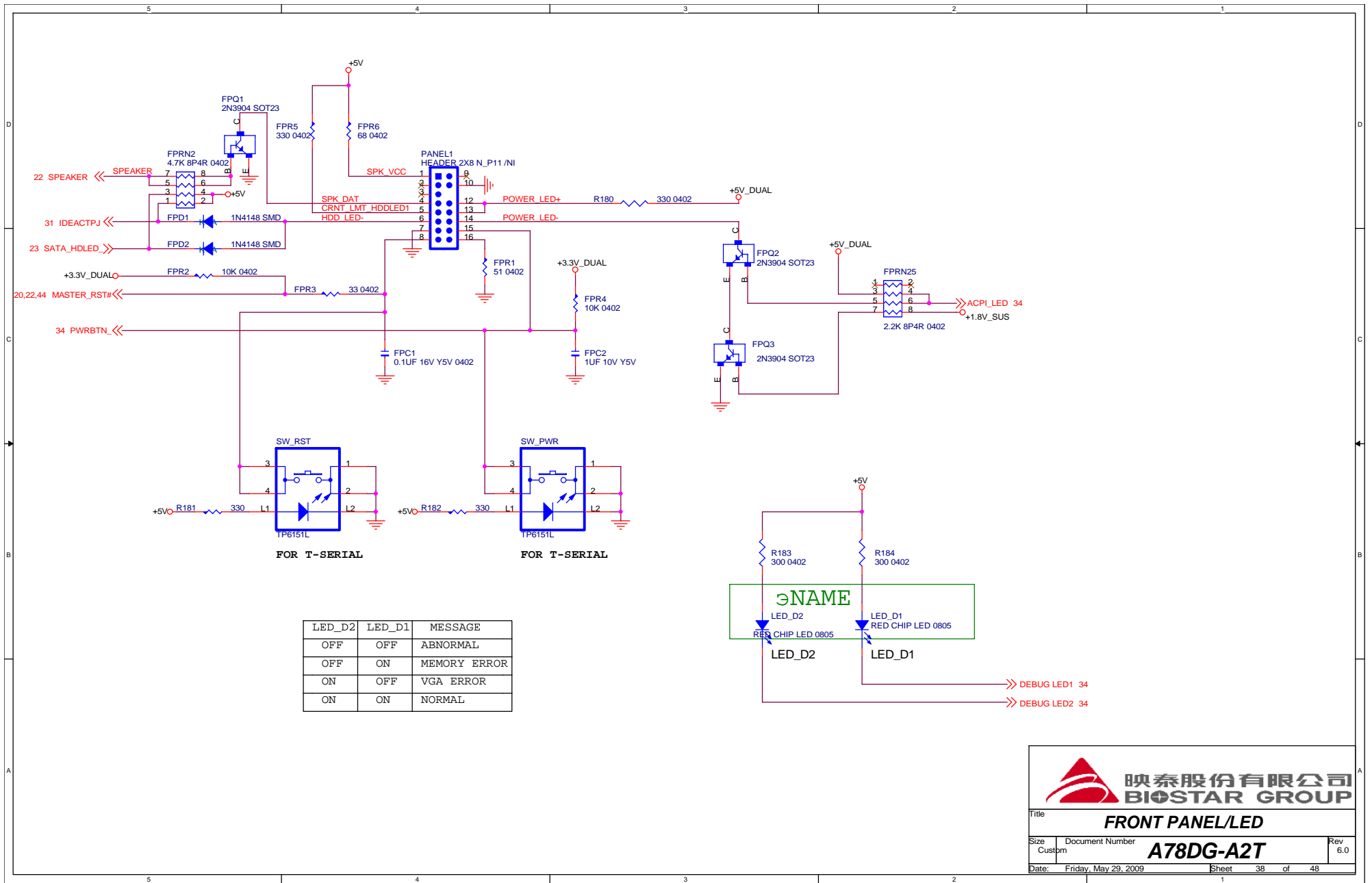
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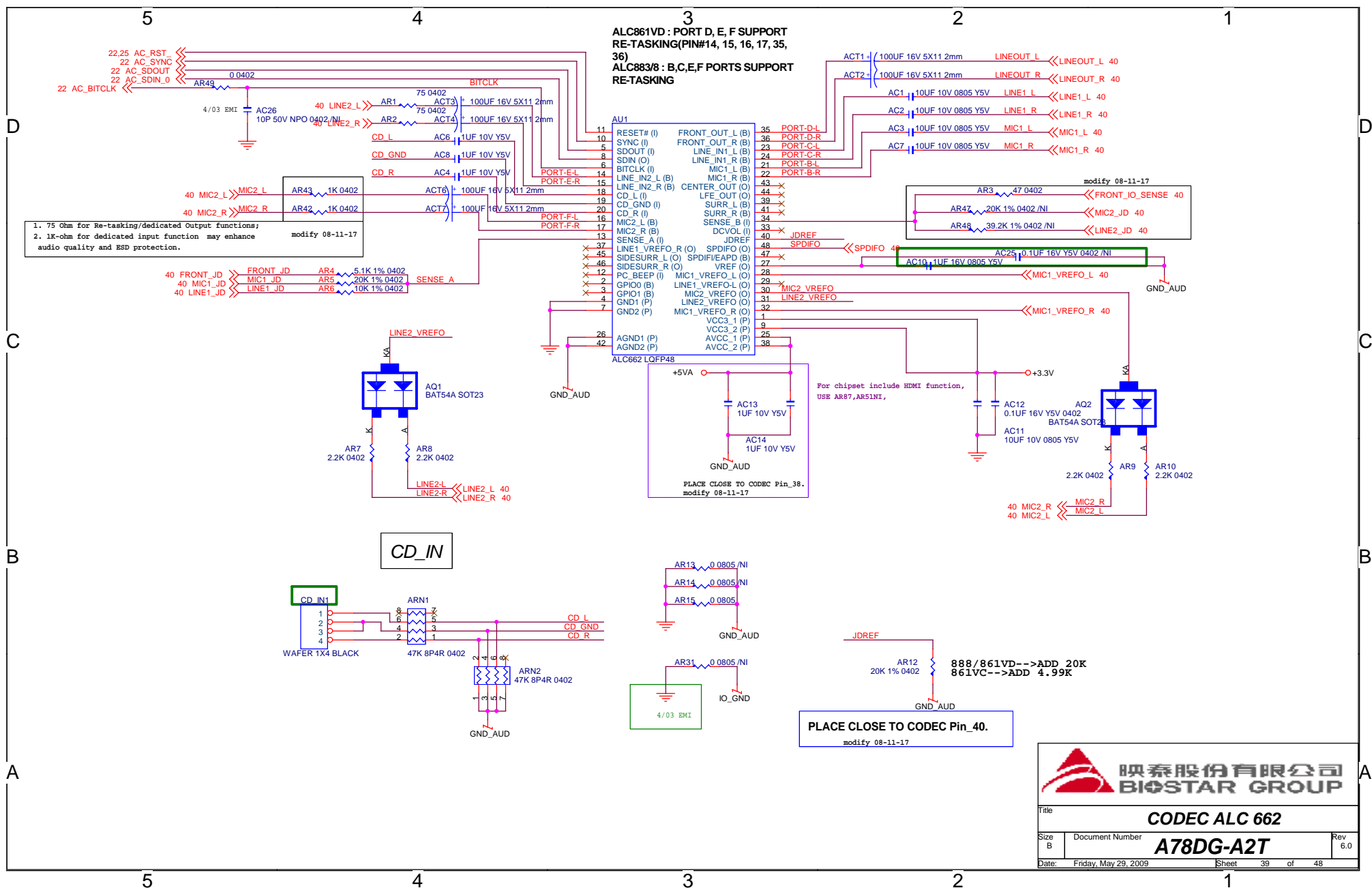
Size: Custom Document Number: **A78DG-A2T** Rev: 6.0

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Voltage Sensing

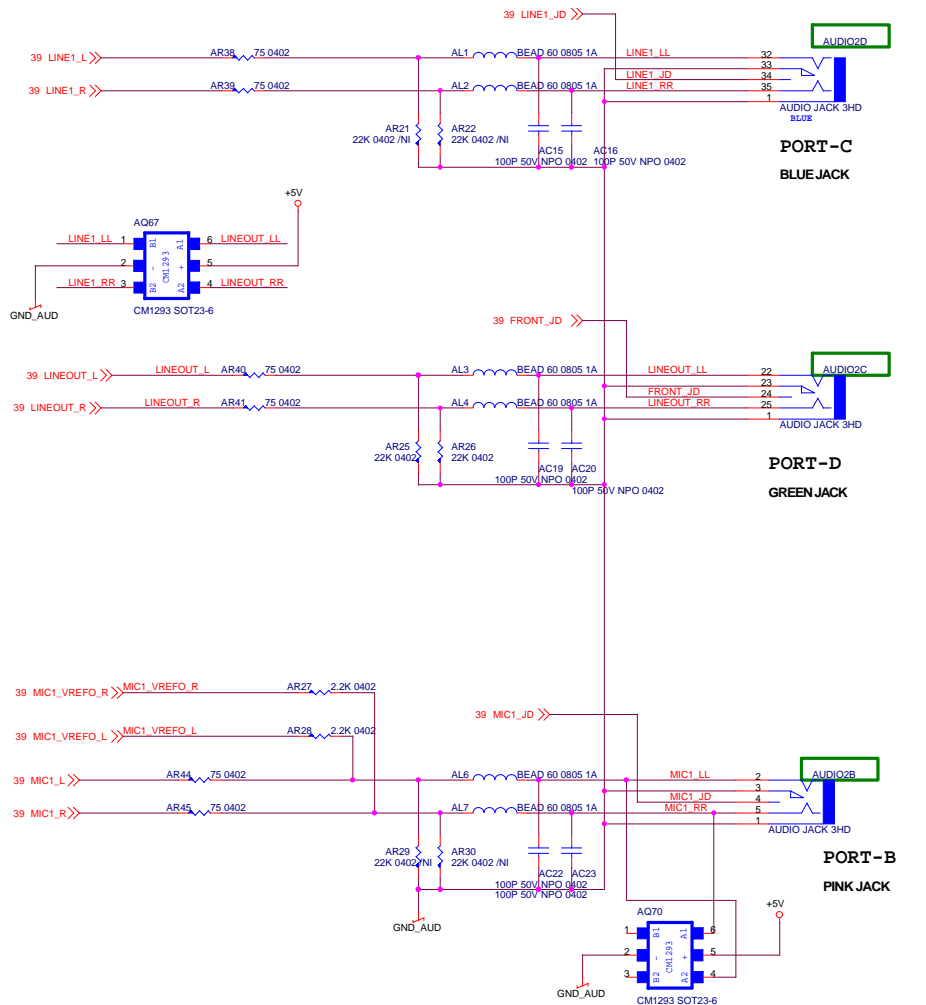






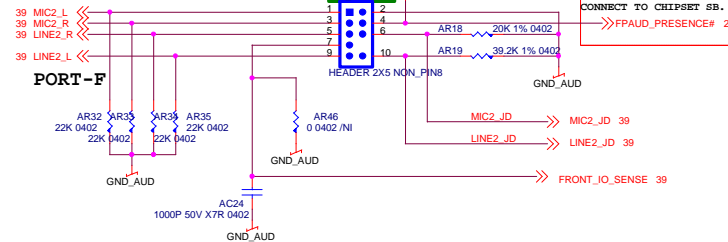
Rear Panel Onboard Analog I/O

P07 : 3-Port & 6-Port Co-lay

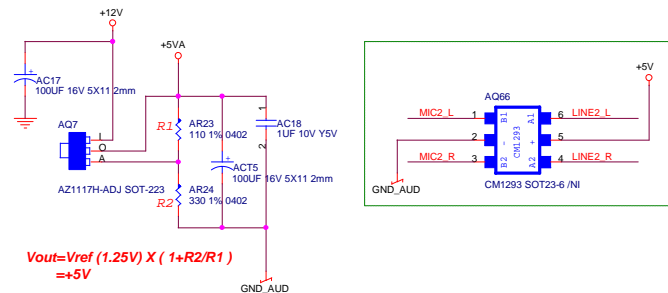


*ALC883/888:B,C,E,F ports support I/P & O/P function.
But A,D,G,H ports not support MIC function.

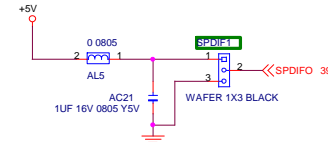
PORT-E



AUDIO ANALOG POWER



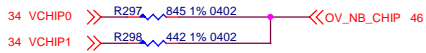
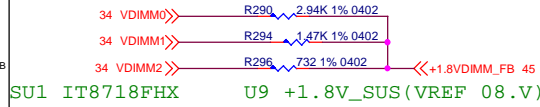
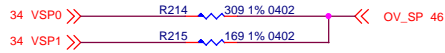
SPDIF OUT



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VCPU_NB0 ==>NI
VCPU_NB1 ==>NI

3/30 1.2V_SB



CPU_NB	VCPU_NB0	VCPU_NB1
Default	1	1
+0.1	0	1
+0.2	1	0
+0.3	0	0

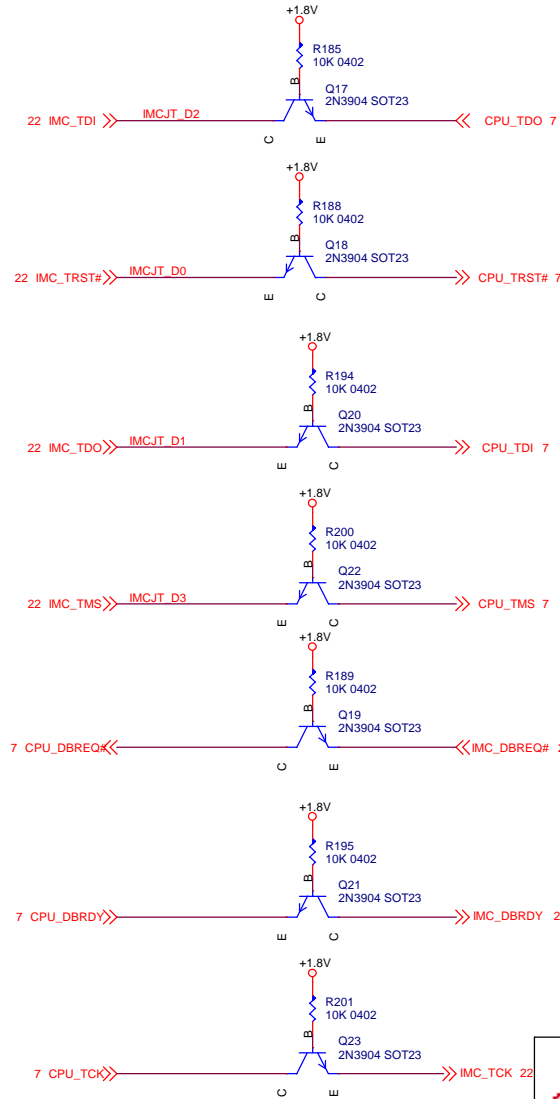
1.2V_SB	VHT0	VHT1
Default 1.23V	1	1
1.32V	0	1
1.43V	1	0
1.53V	0	0

SIDEPORT	VSP0	VSP1
Default 1.8V	1	1
1.9V	0	1
2.0V	1	0
2.1V	0	0

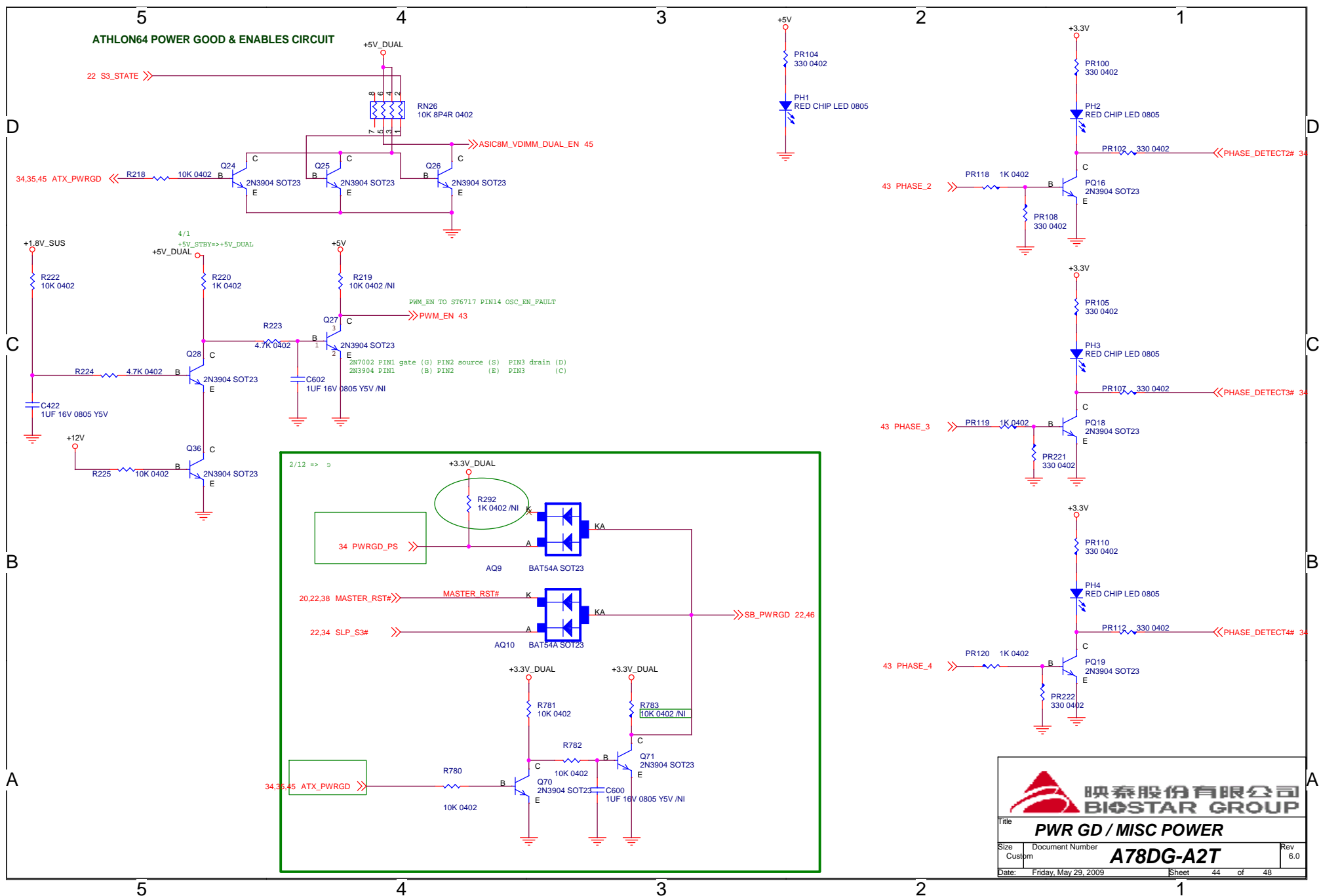
+1.8VDIMM_FB	VDIMM0	VDIMM1	VDIMM2
Default 1.95V	1	1	1
2.05V	0	1	1
2.15V	1	0	1
2.25V	0	0	1
2.35V	1	1	0
2.45V	0	1	0
2.55V	1	0	0
2.65V	0	0	0

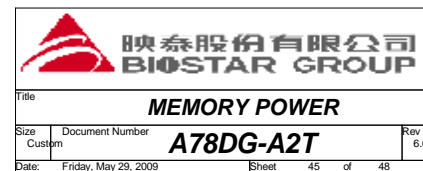
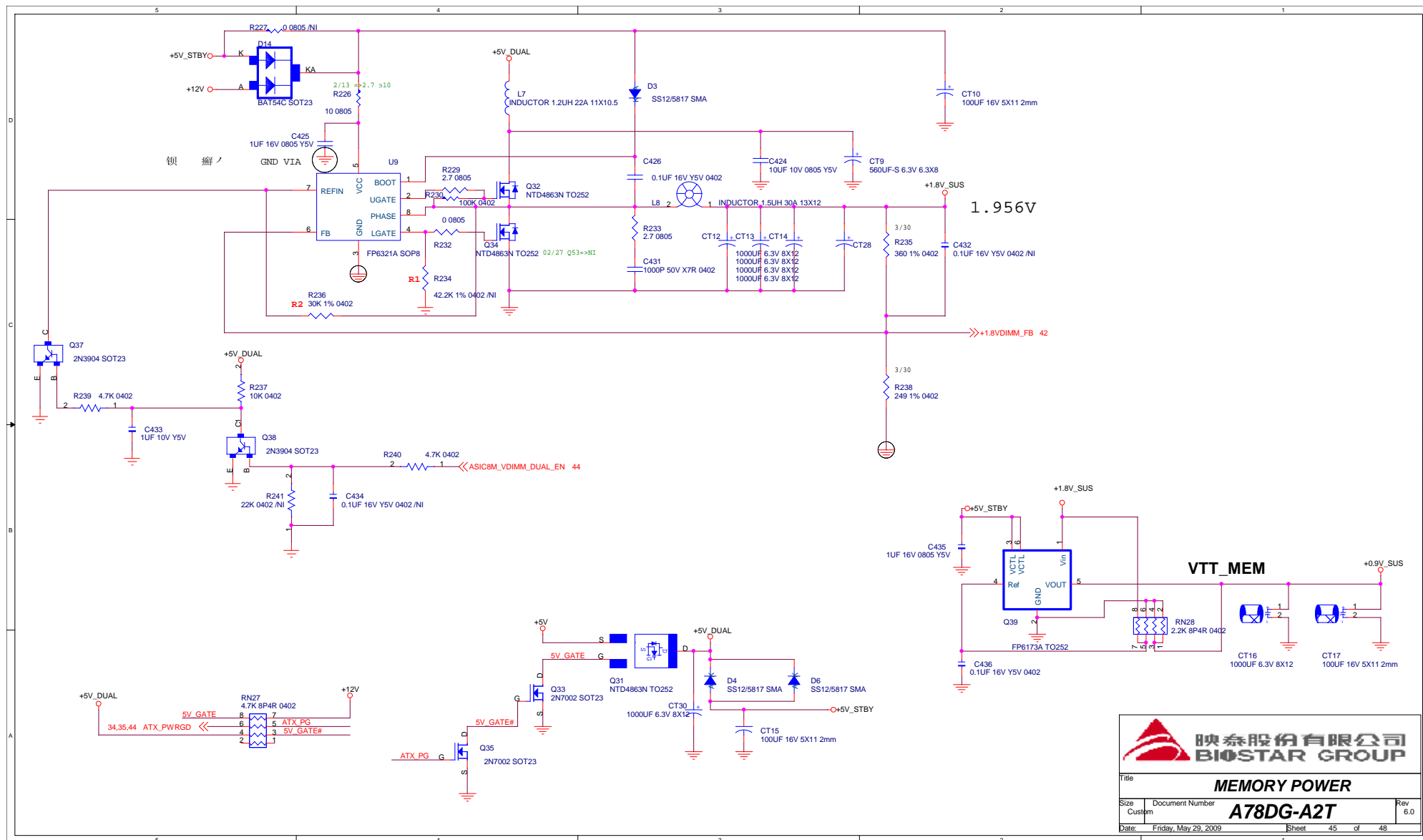
3/30

NB CORE	OV_CHIP1	OV_CHIP0
+1.25V	1	1
+1.35V	0	1
+1.45V	1	0
+1.55V	0	0



Title OVER VOLTAGE & AOD		
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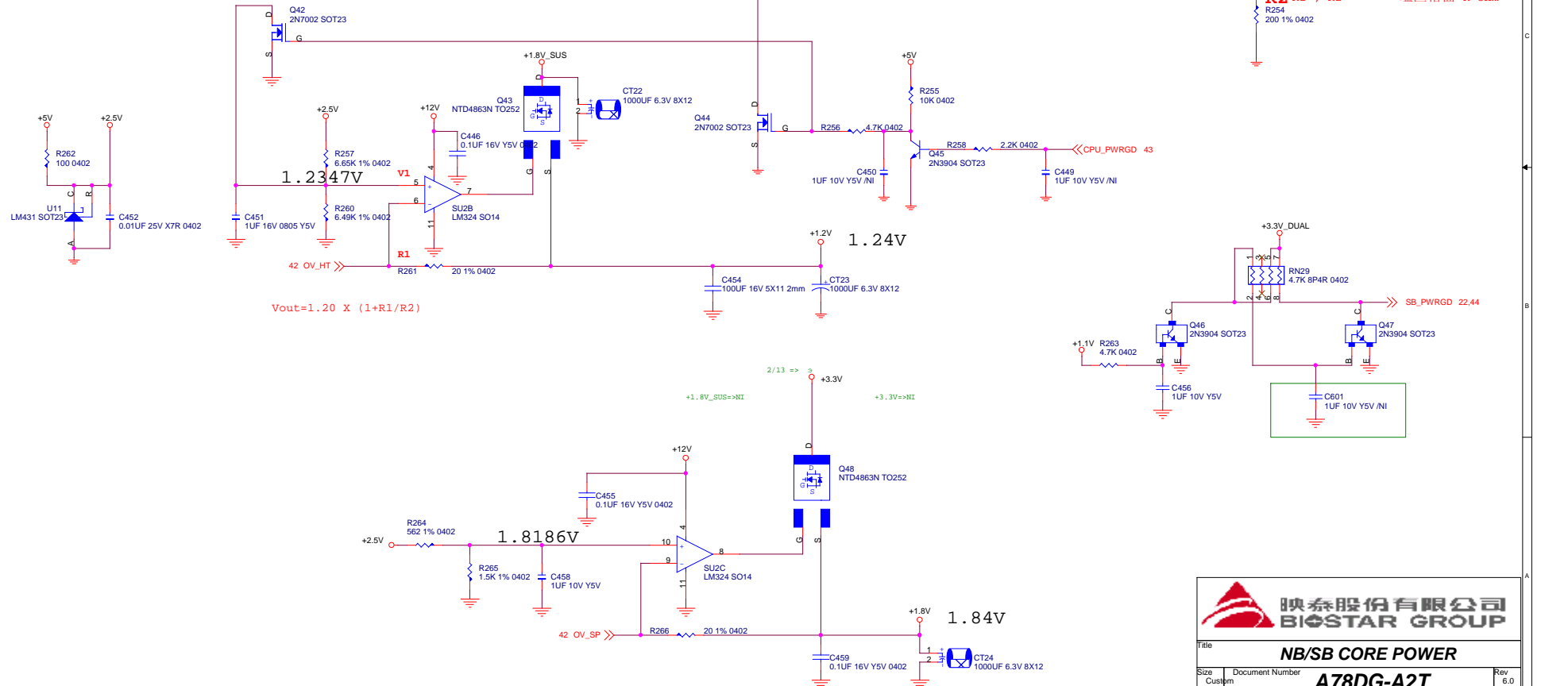


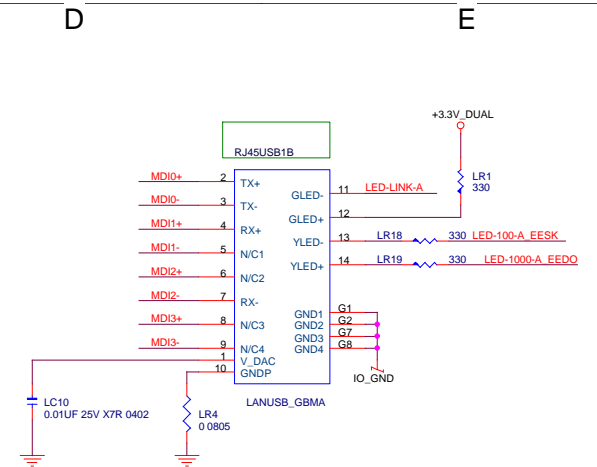
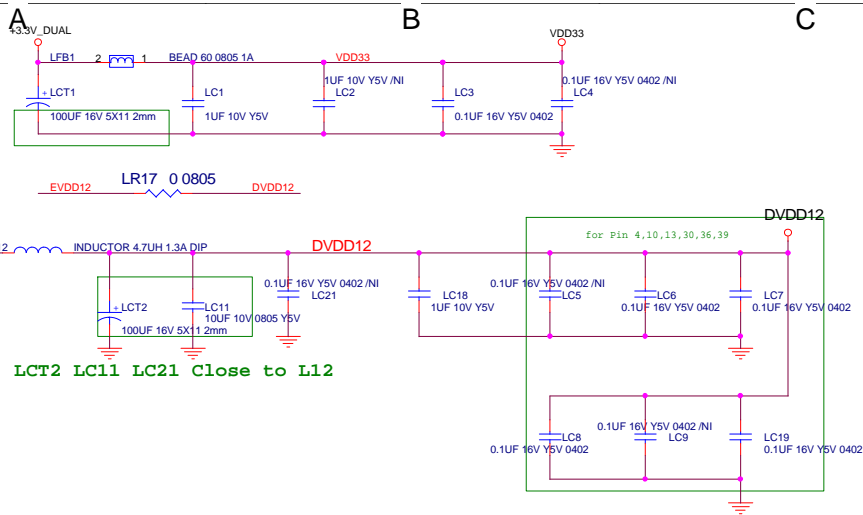


NB/SB +1.1V/+1.2V POWER 1.1V @3A FOR RX780/RS780
NB CORE POWER 1.1V @8A FOR RX780/RS780

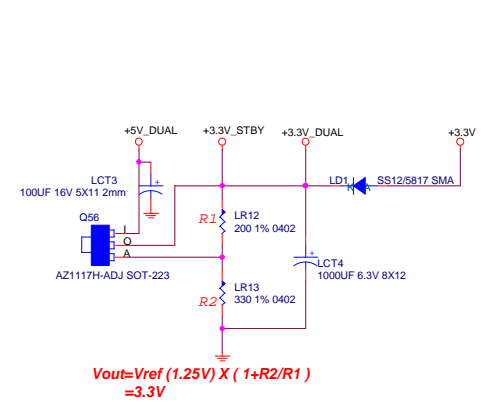
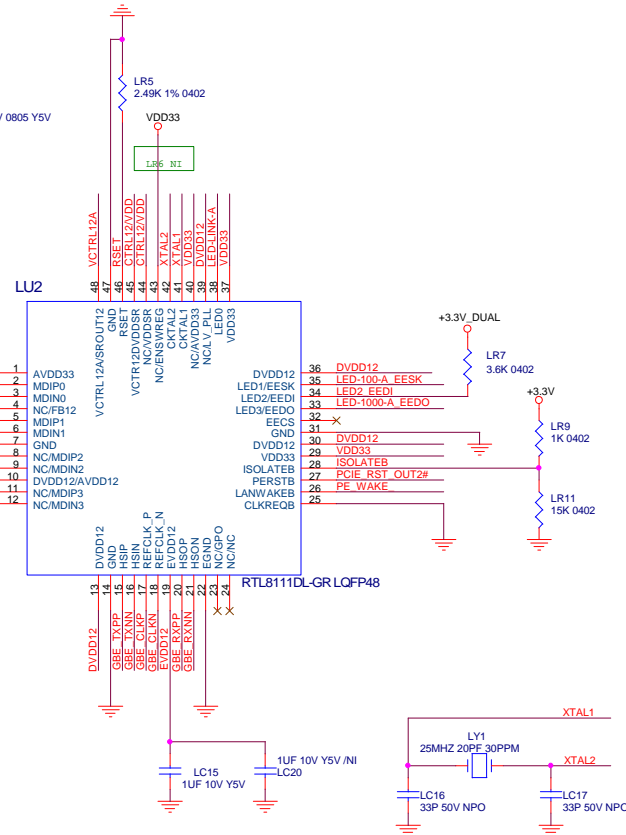
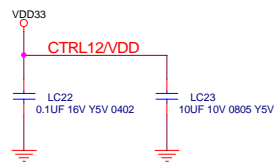
uP6103-->ADD-->RA1, RA2, REMOVE-->RA3, RA4, CA1, DA1
RT9214-->REMOVE-->RA1, RA2, ADD-->RA3, RA4, CA1, DA1

NB
+1.1V @ 8A AMPS MAX





Power domain chart	RTL8111DL
AVDD33	3.3V
DVDD12	1.05V



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