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43	BOM

A78LA-A3S (RS780L&SB710)

REV:6.0

2011/02/09

CPU :

AM3

DDR3 X 4 Dual channel , PCI-Ex16 X 1 , PCI-Ex1 X 2 , PCI X 3 , RTL8111EL PCI-E Lan , AMD AM3

System Chipset :

AMD RS780

AMD SB750

On Board Chip :

Clock Gen. -- RTM880N-793

Azalia Codec -- ALC662

GigaBit Lan -- RealTek RTL8111EL

PWM Controller -- ST6717A

Super I/O -- IT8728

SPI Flash 8Mb

Expansion Slot :

PCI Express x16 Slot * 1

PCI Express x1 Slot * 2

PCI Slot * 3

Heatsink :

NB: NB-NF61

SB: SB SMALL-AMD

MOS: NONE


I/O Pannel :

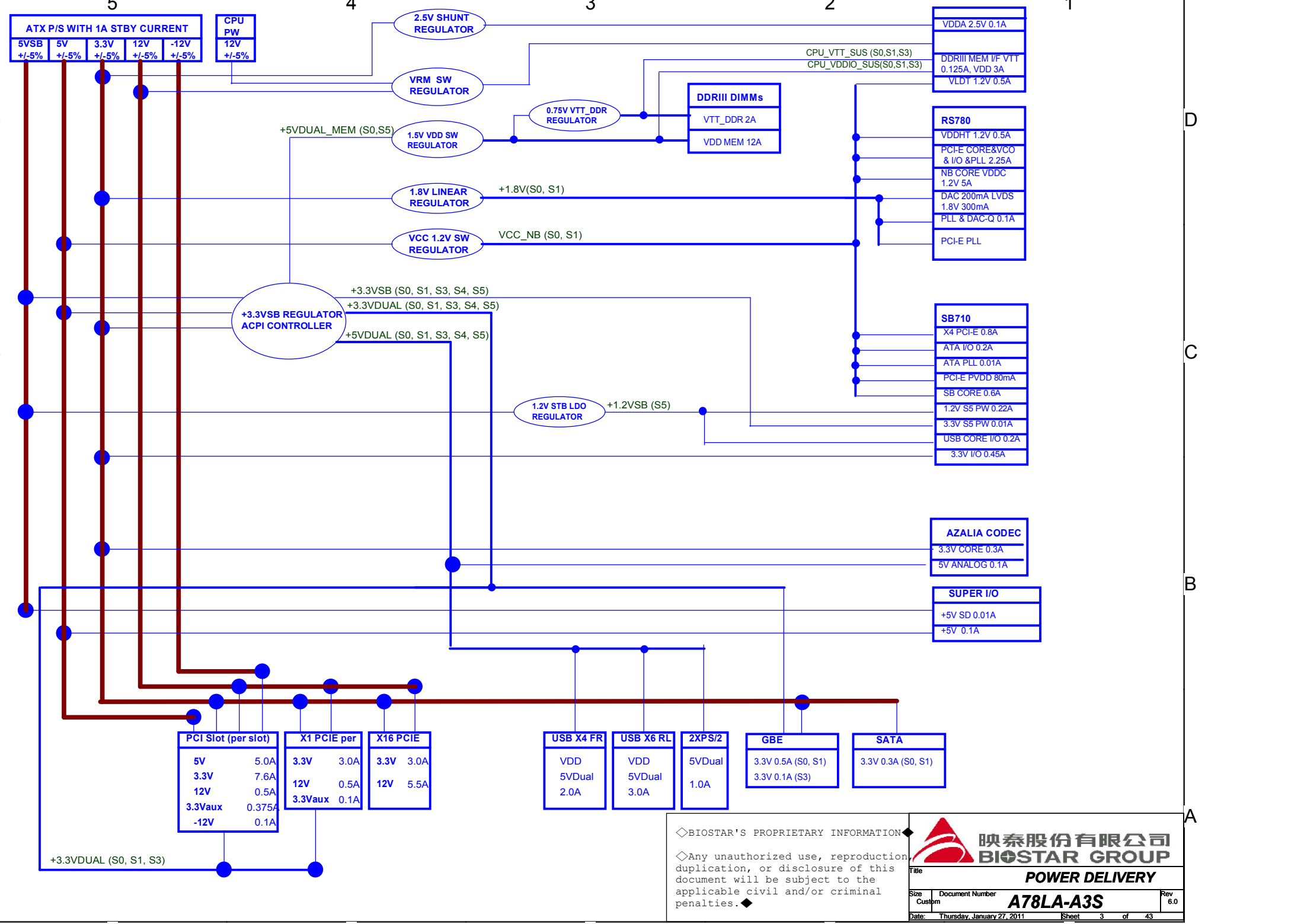
47-RIOBRACKET-68

PCB SIZE :

205.09 X 304.80


1080

HW Engineer:		Date:		
HW Leader:		Date:		
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		Title COVER		
		Size Custom	Document Number A78LA-A3S	Rev 6.0
		Date: Wednesday, February 09, 2011 Sheet 1 of 43		



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Title			POWER DELIVERY	
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5

4

3

2

1

Change list From 6.1 to 6.2

- 1. (PAGE 39) Add CPU_NB low side MOS PQ22
- 2. (PAGE 38) Change MEM POWER control circuit (S3_STATE change to S5)
- 3. (PAGE 40) Change CT23 from 560uF to 270uF
- 4. (PAGE 41) Change CT35 from 560uF to 270uF
- 5. (PAGE 40) Change MEM POWER OV circuit
- 6. (PAGE 39) Change some RES and CAP Value by following TW test report
- 7. (PAGE 22) Change Board ID

D

D

C

C

B


B

A

A

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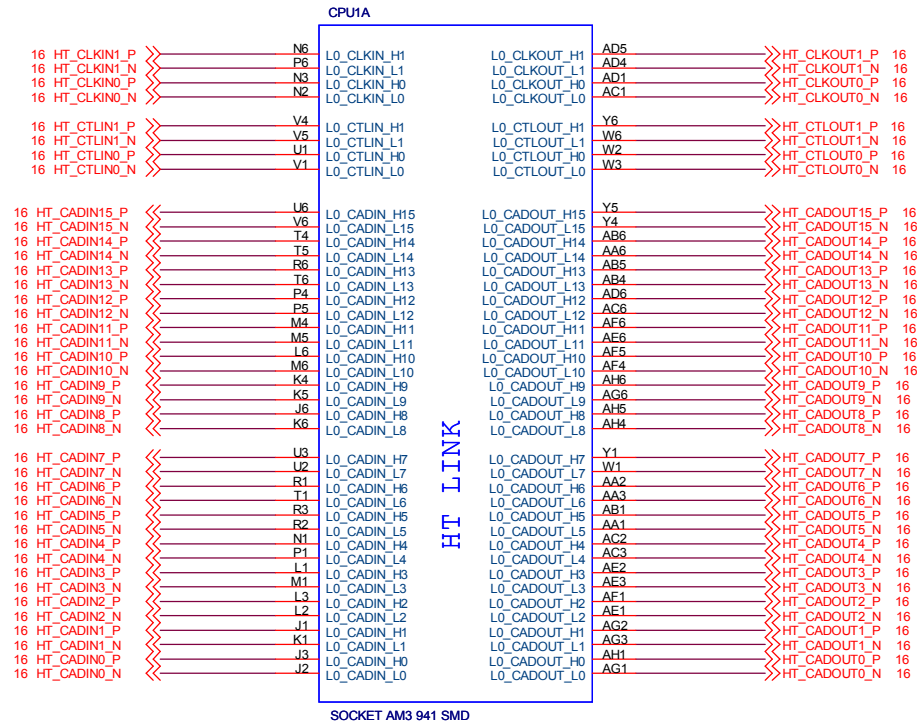
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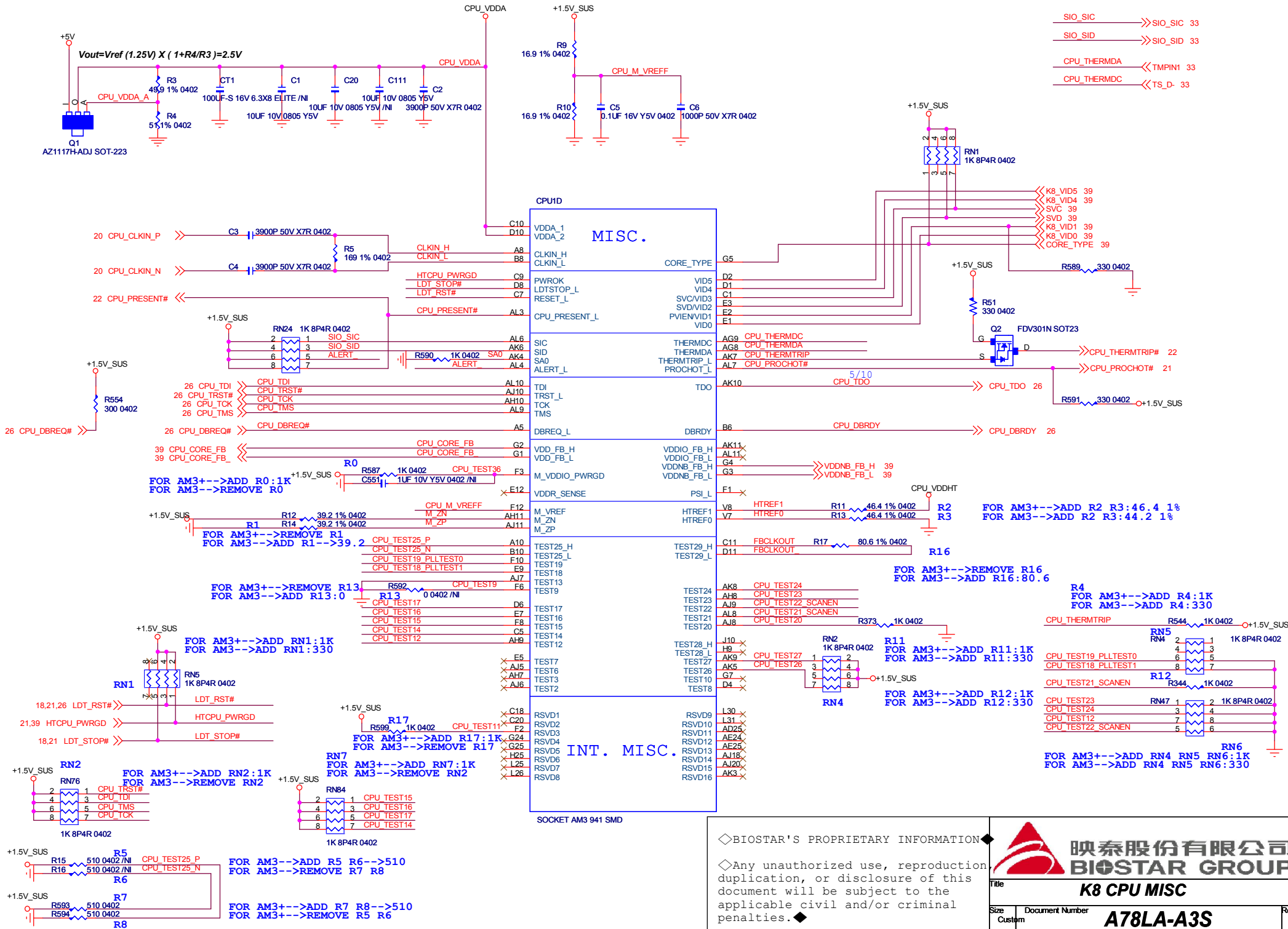
HyperTransport

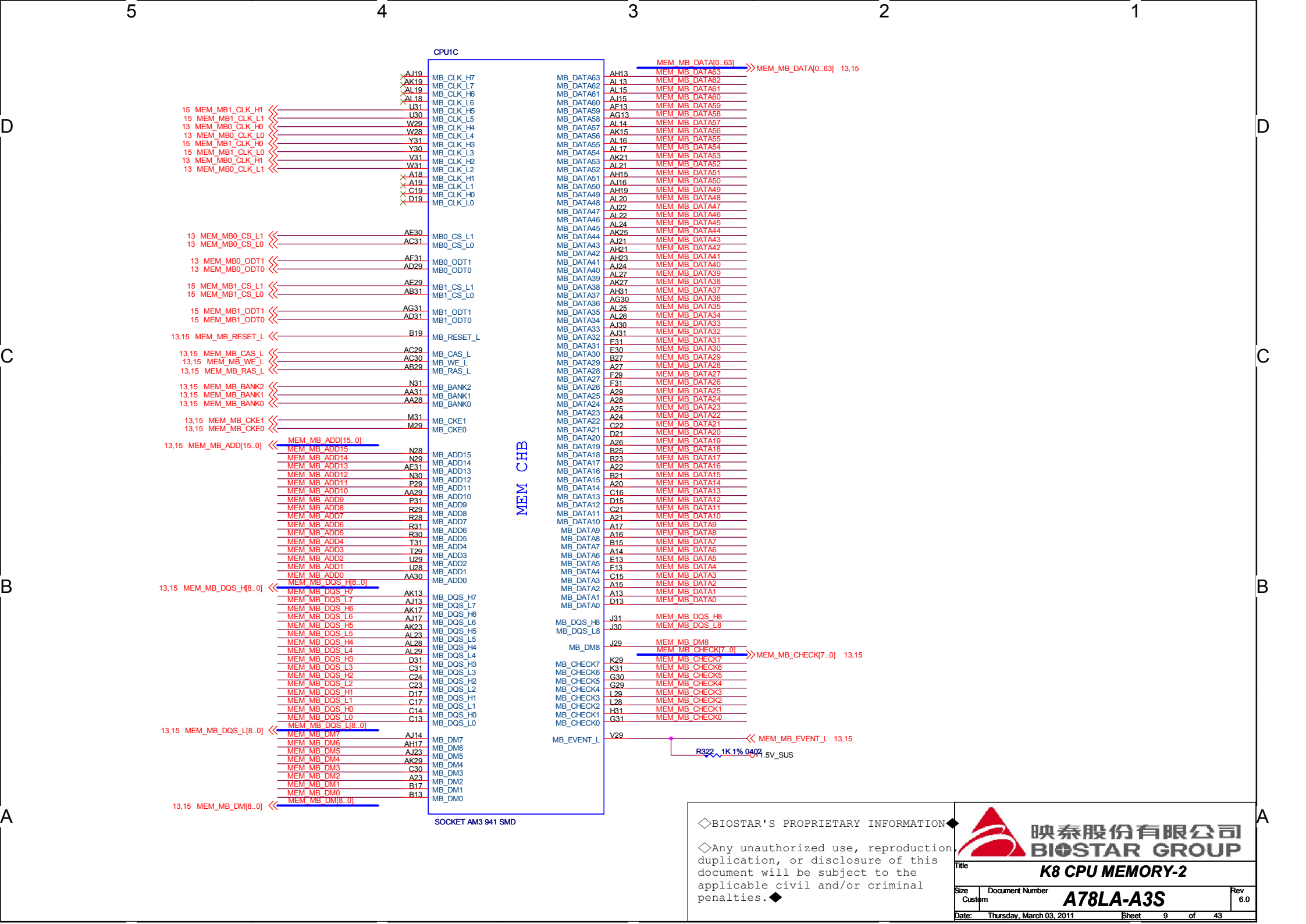


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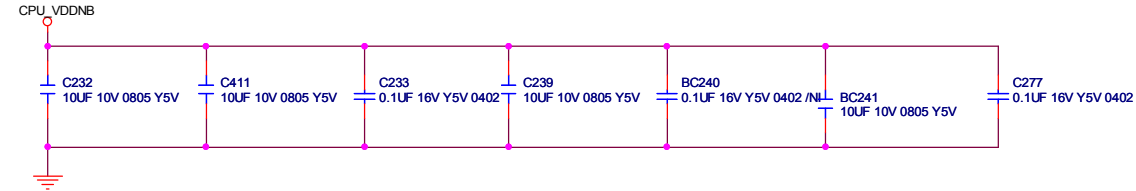
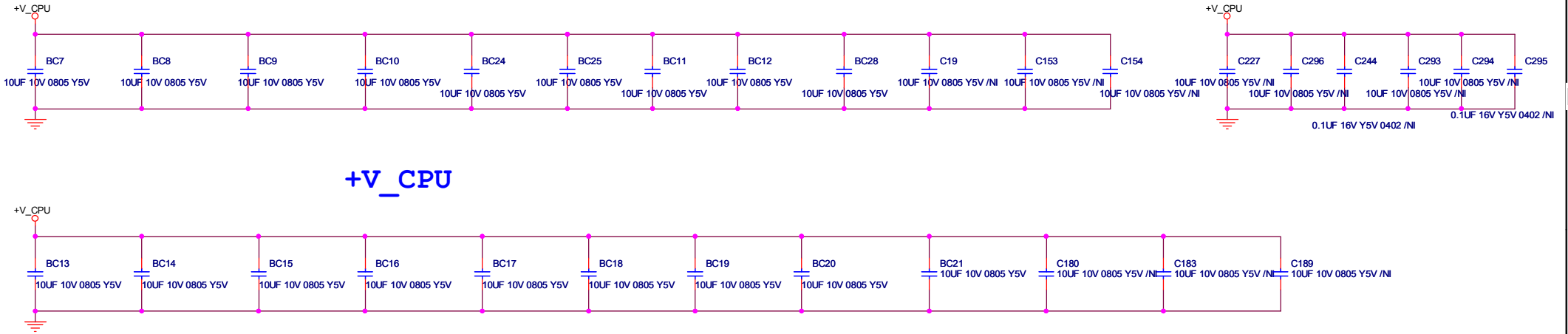
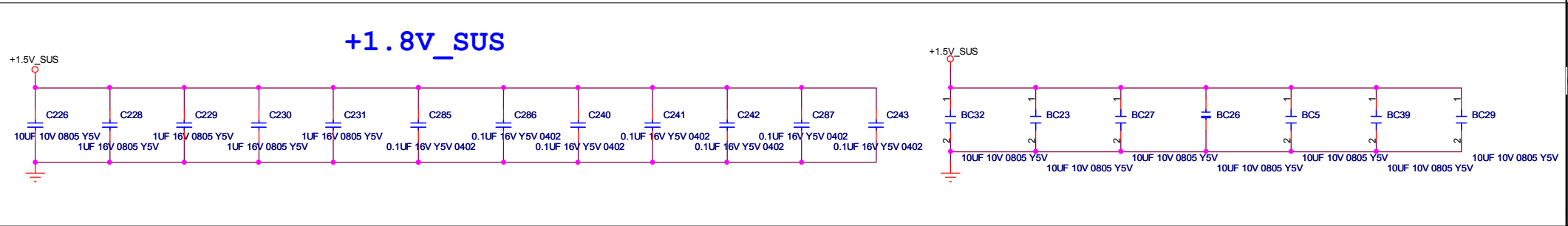
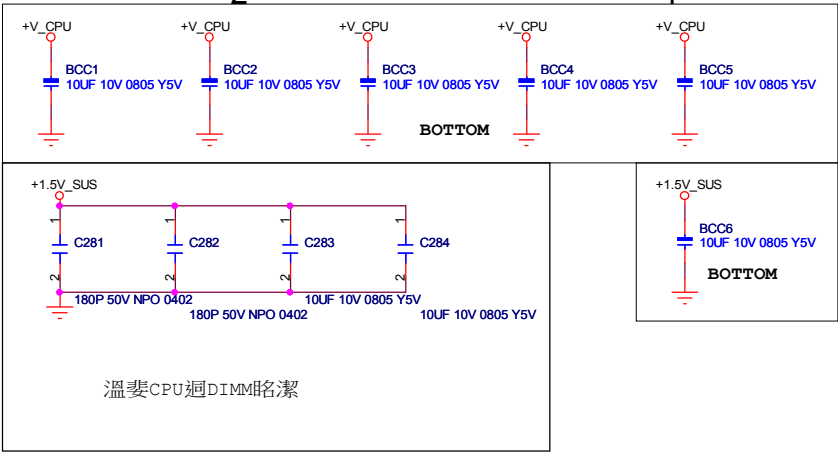
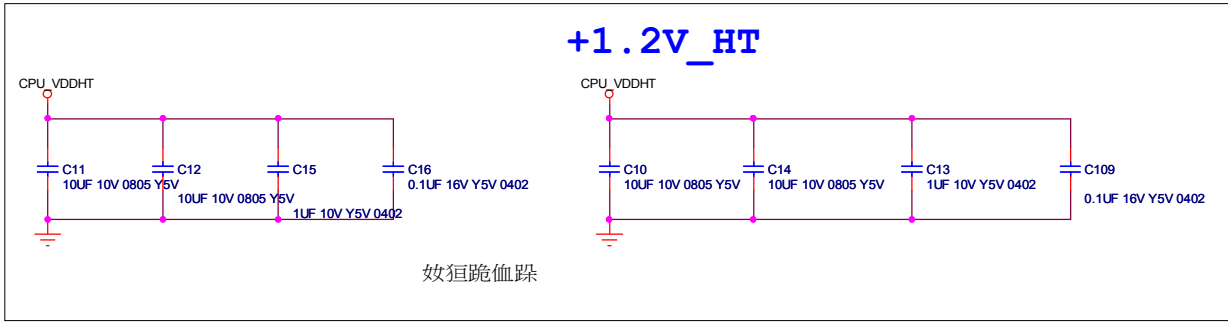




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Title	K8 CPU POWER
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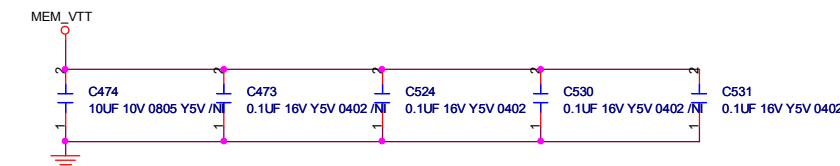
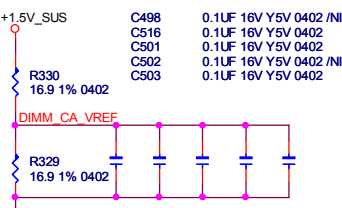
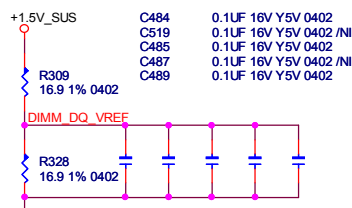
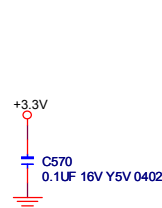
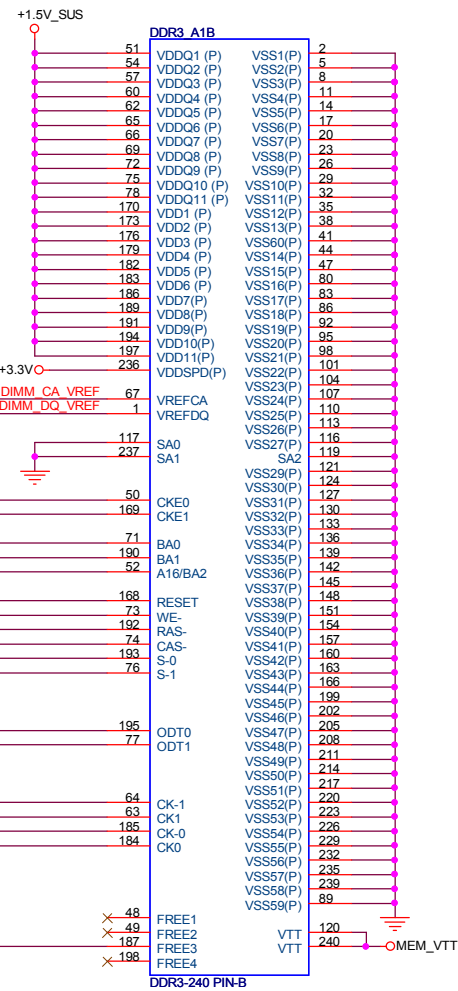
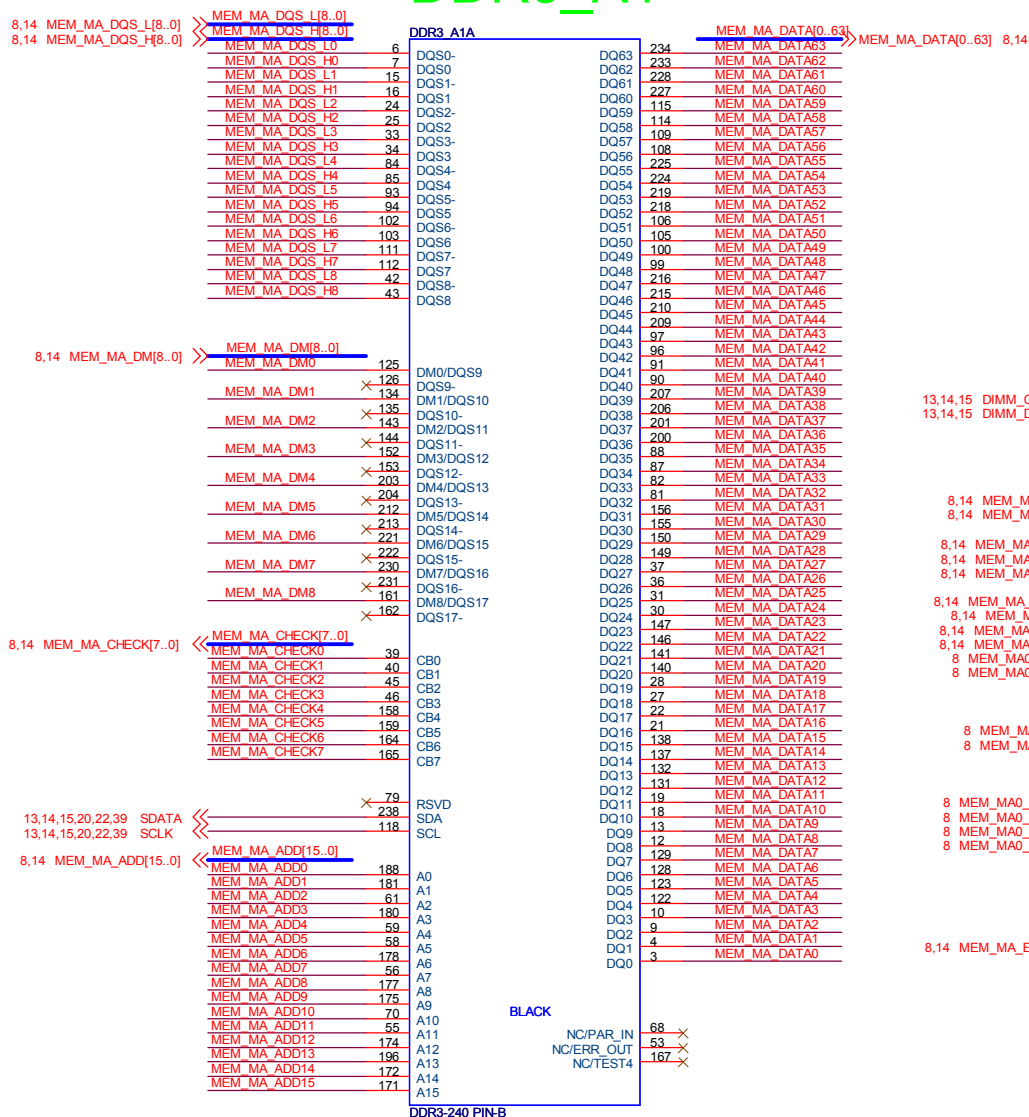
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DDR3_A1



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DDR DIMM-1

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DDR3_B1



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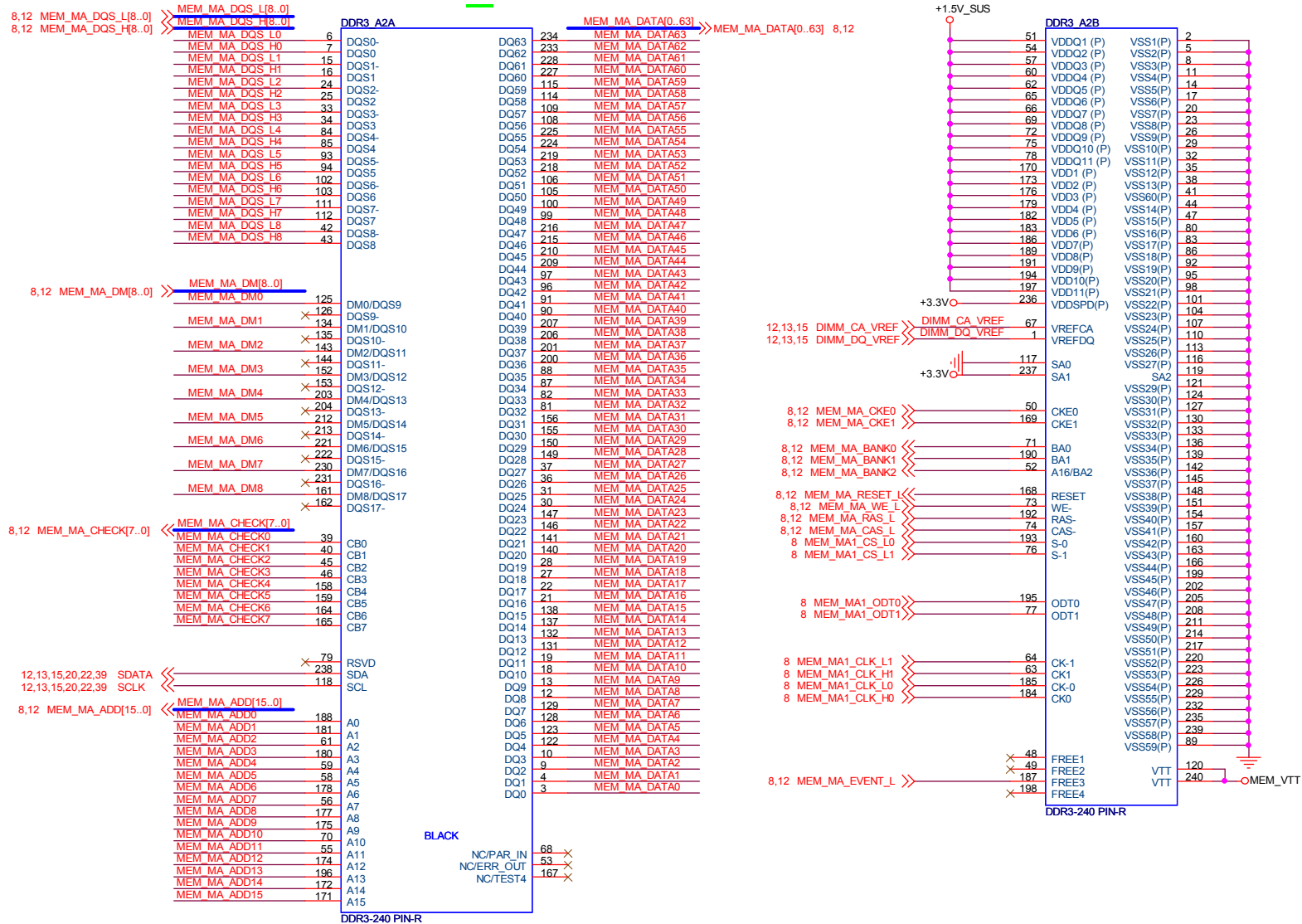
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DDR3_A2



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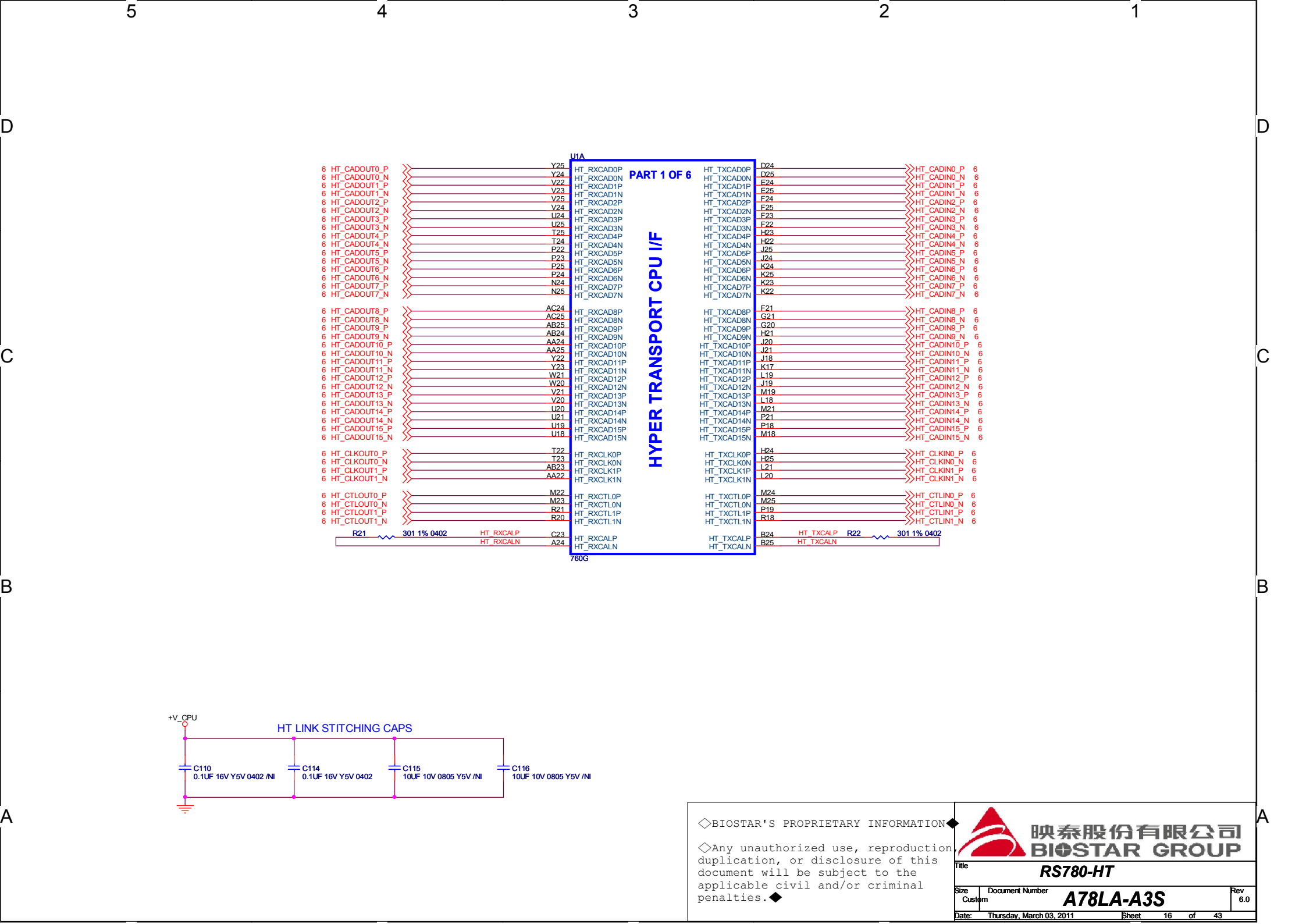
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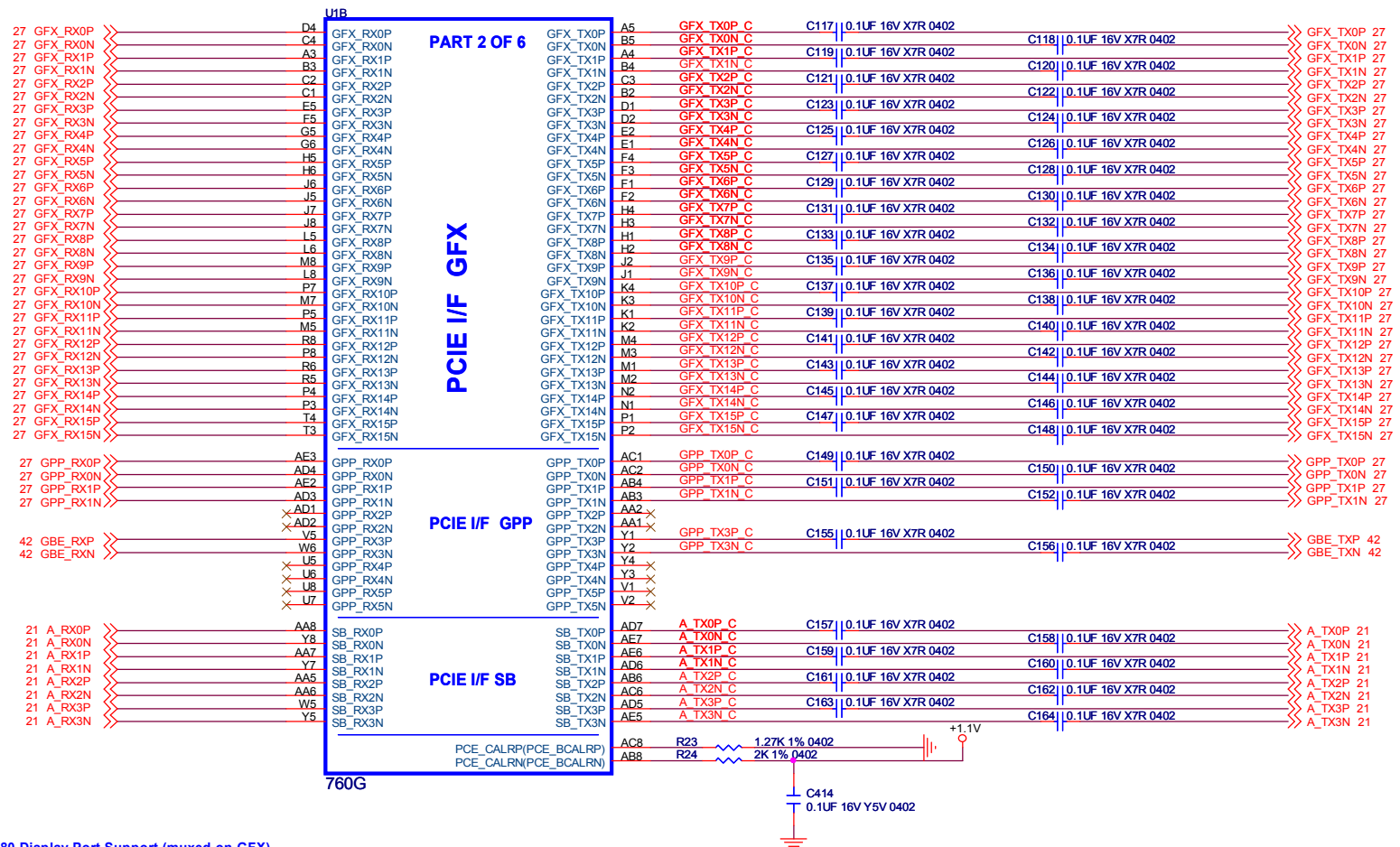
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DDR3-240 PIN-R







RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

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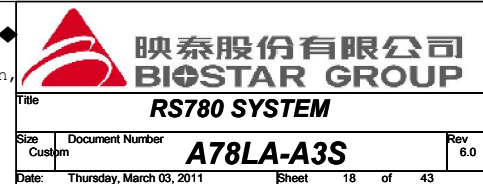
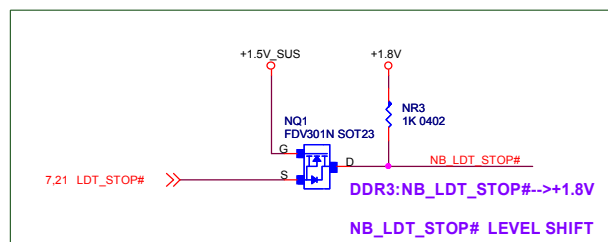
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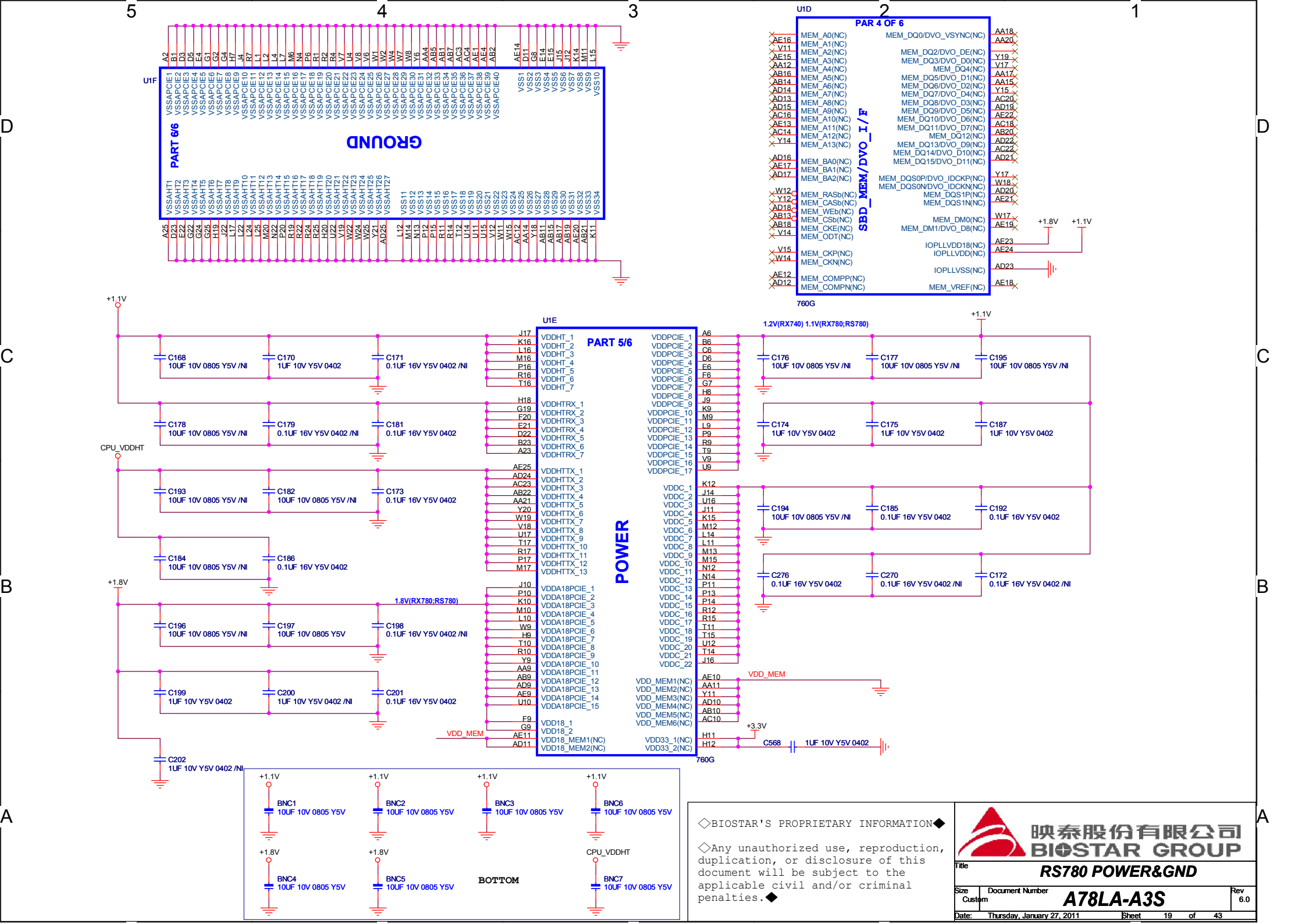
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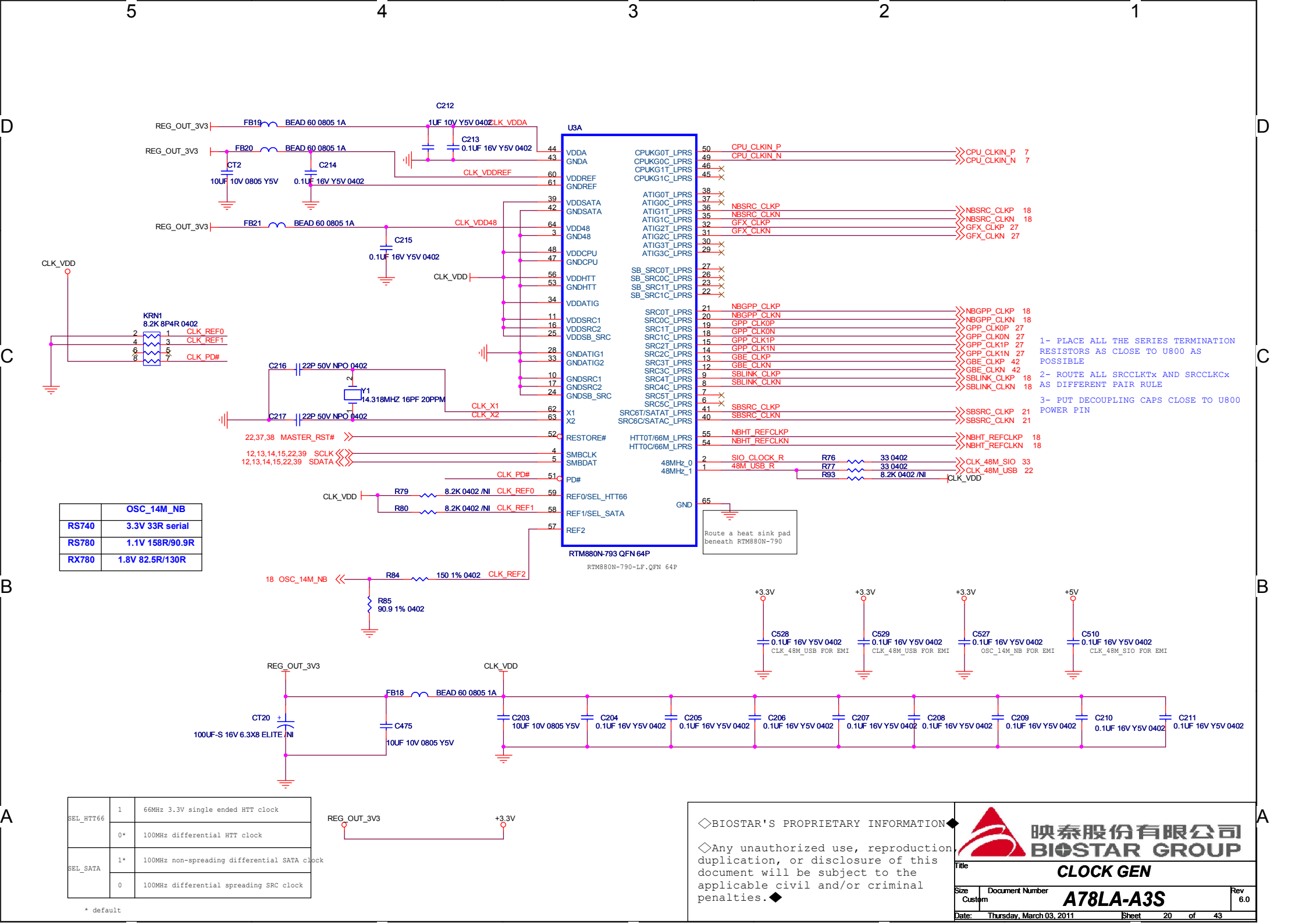
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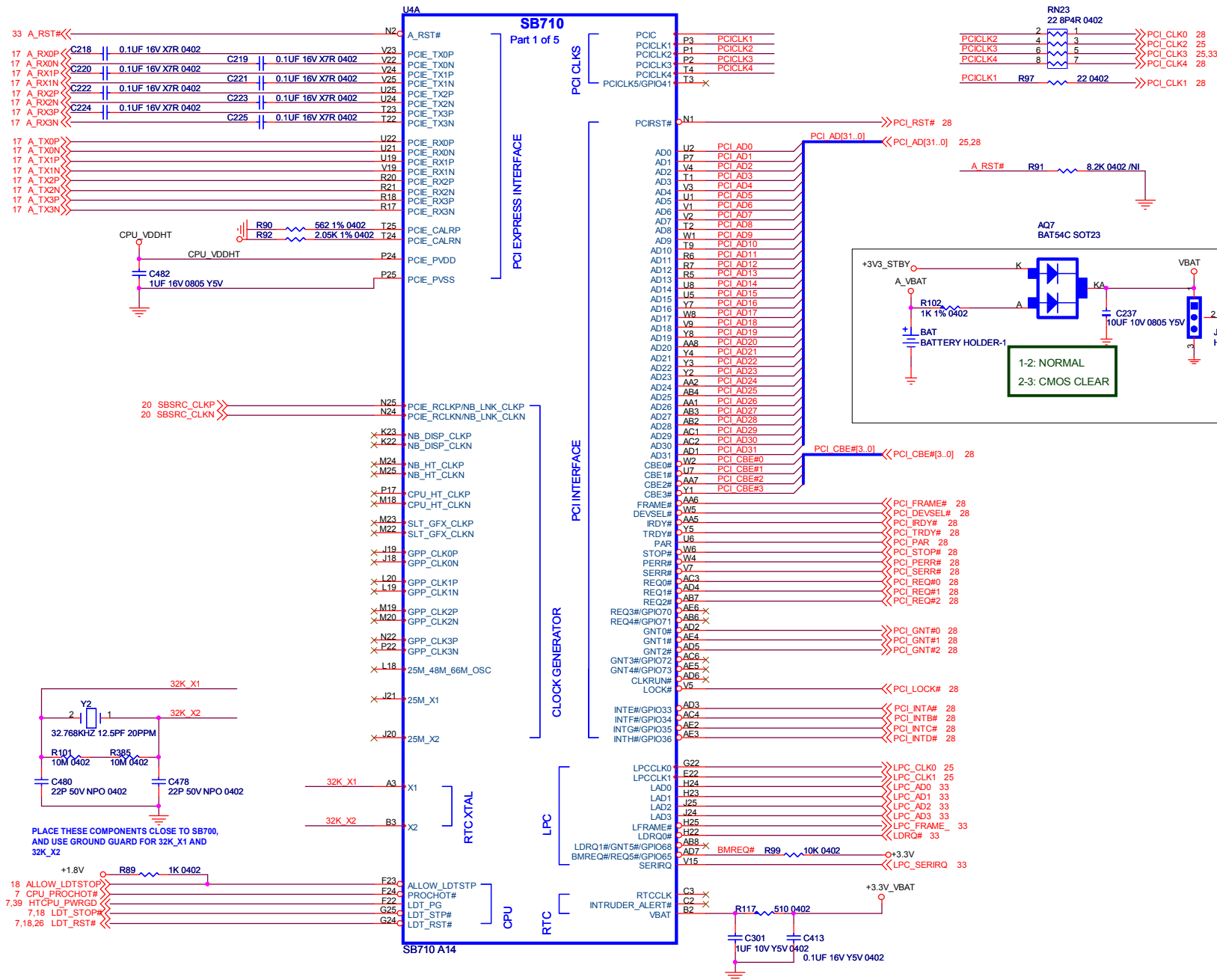
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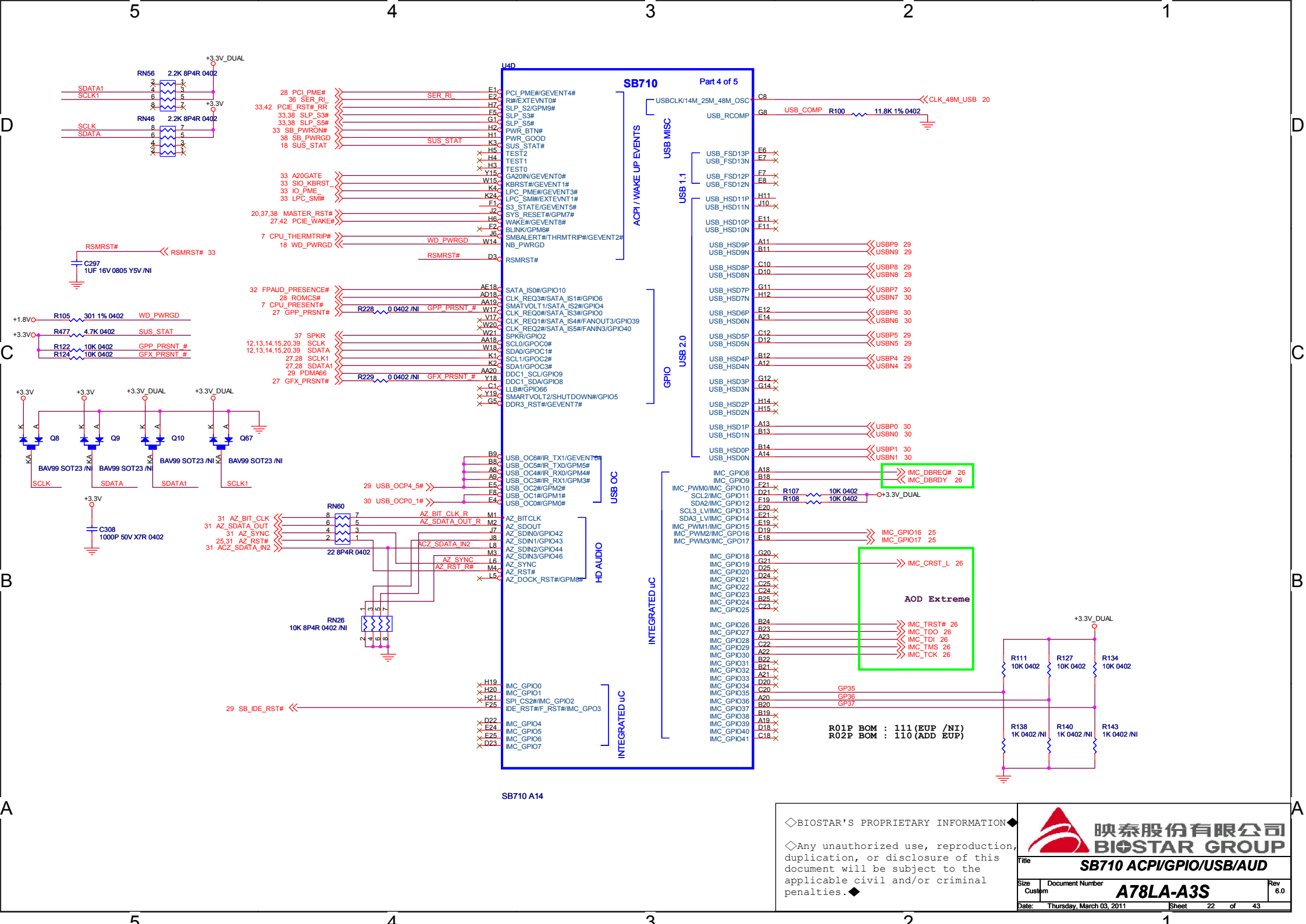
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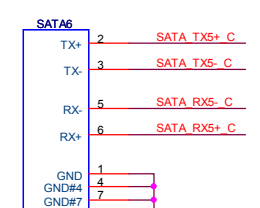
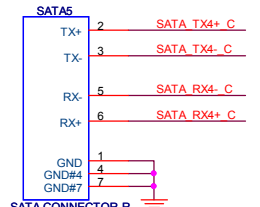
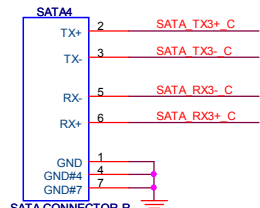
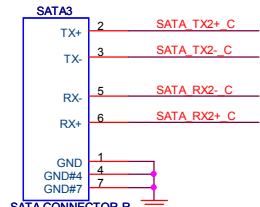
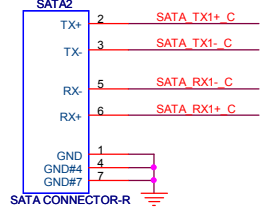
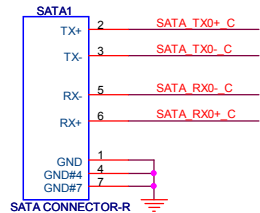
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Size: Custom Document Number: **A78LA-A3S** Rev: 6.0

Date: Thursday, March 03, 2011 Sheet: 21 of 43

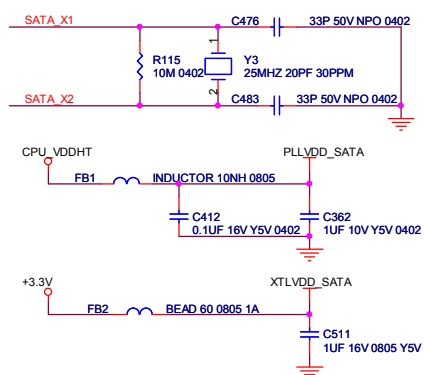


D



PLACE R297 CLOSE TO SB600 BALL

R297 IS 1K 1% FOR XTAL 4.99K 1% FOR INTERNAL CLK



U4B

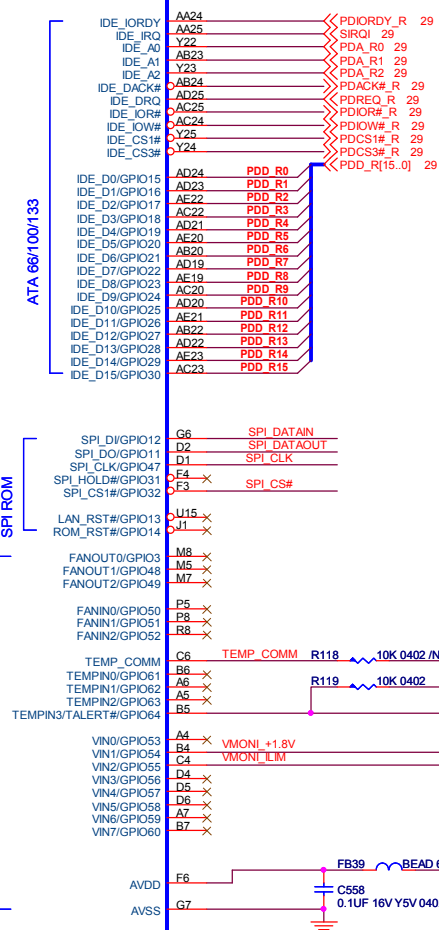
SB710

Part 2 of 5

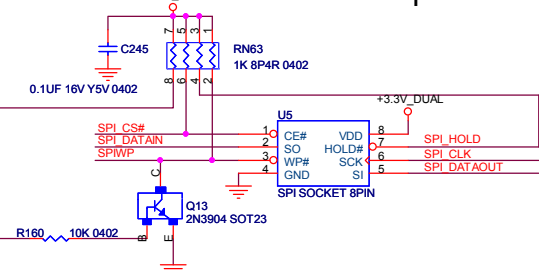
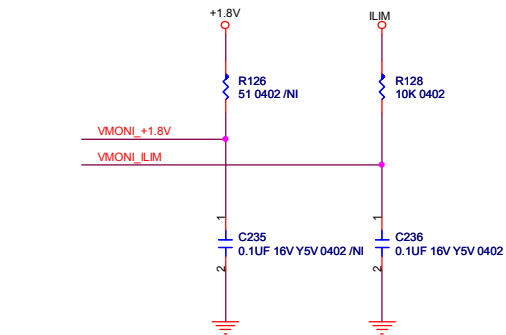
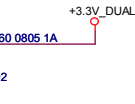
SERIAL ATA

SATA PWR

HW MONITOR



PIN NAME	BIOS
GPIO50 ~ GPIO60	0 OR 1



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SB710 SATA/IDE/SPI

A78LA-A3S

Rev 6.0

Thursday, March 03, 2011

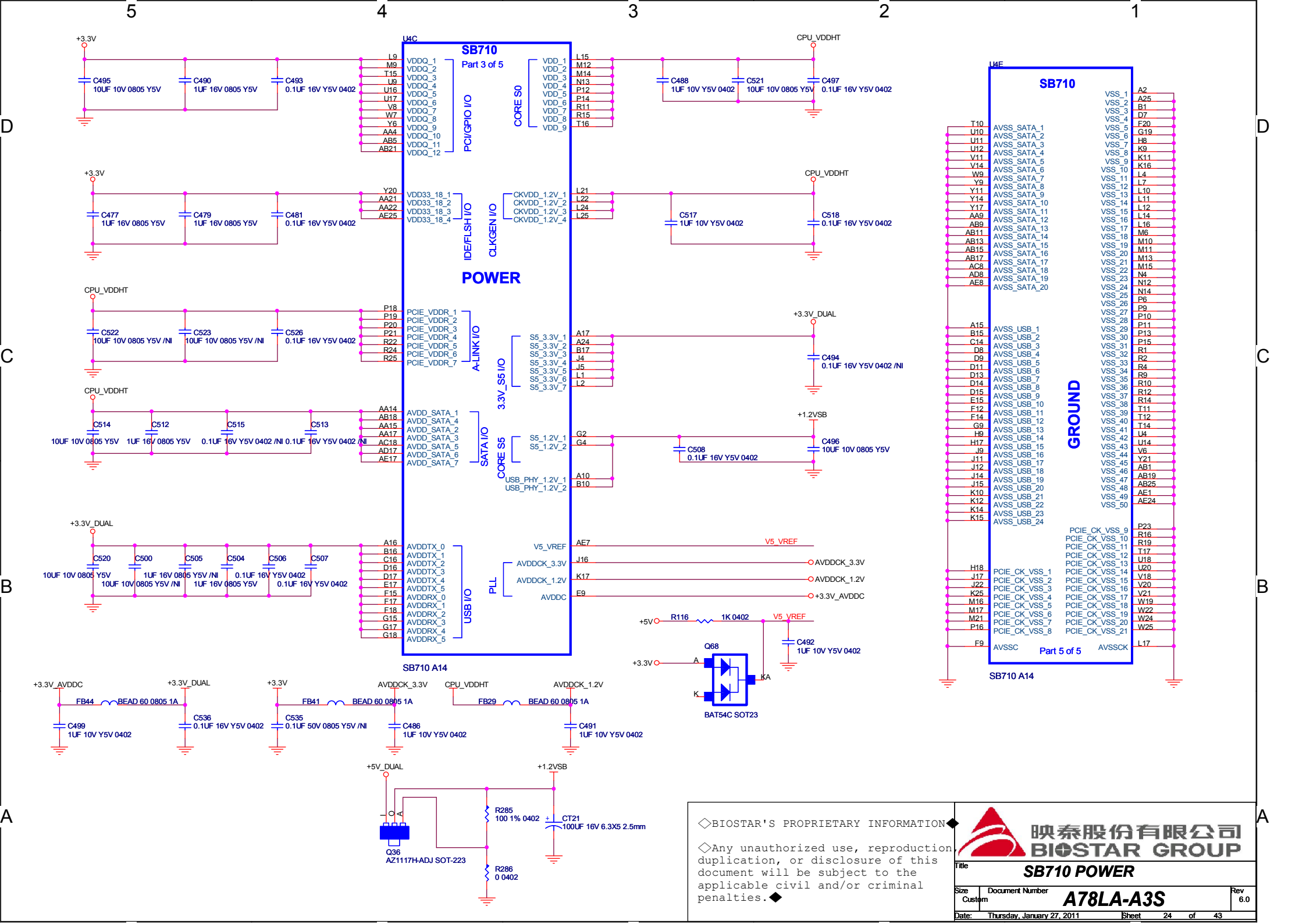
Sheet 23 of 43

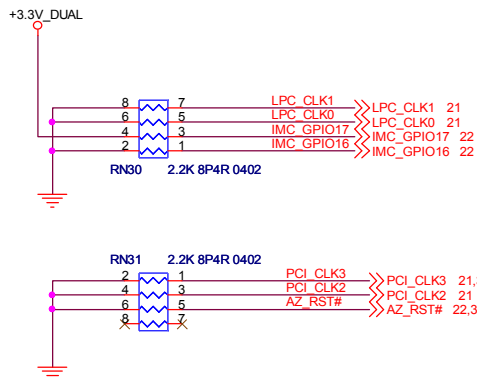
D

C

B

A



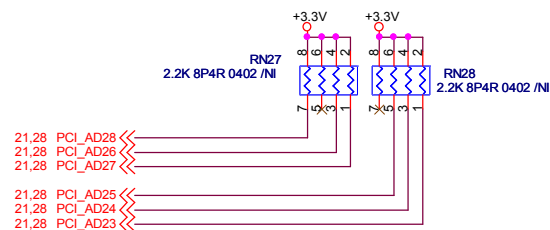


REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	

DEBUG STRAPS



SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

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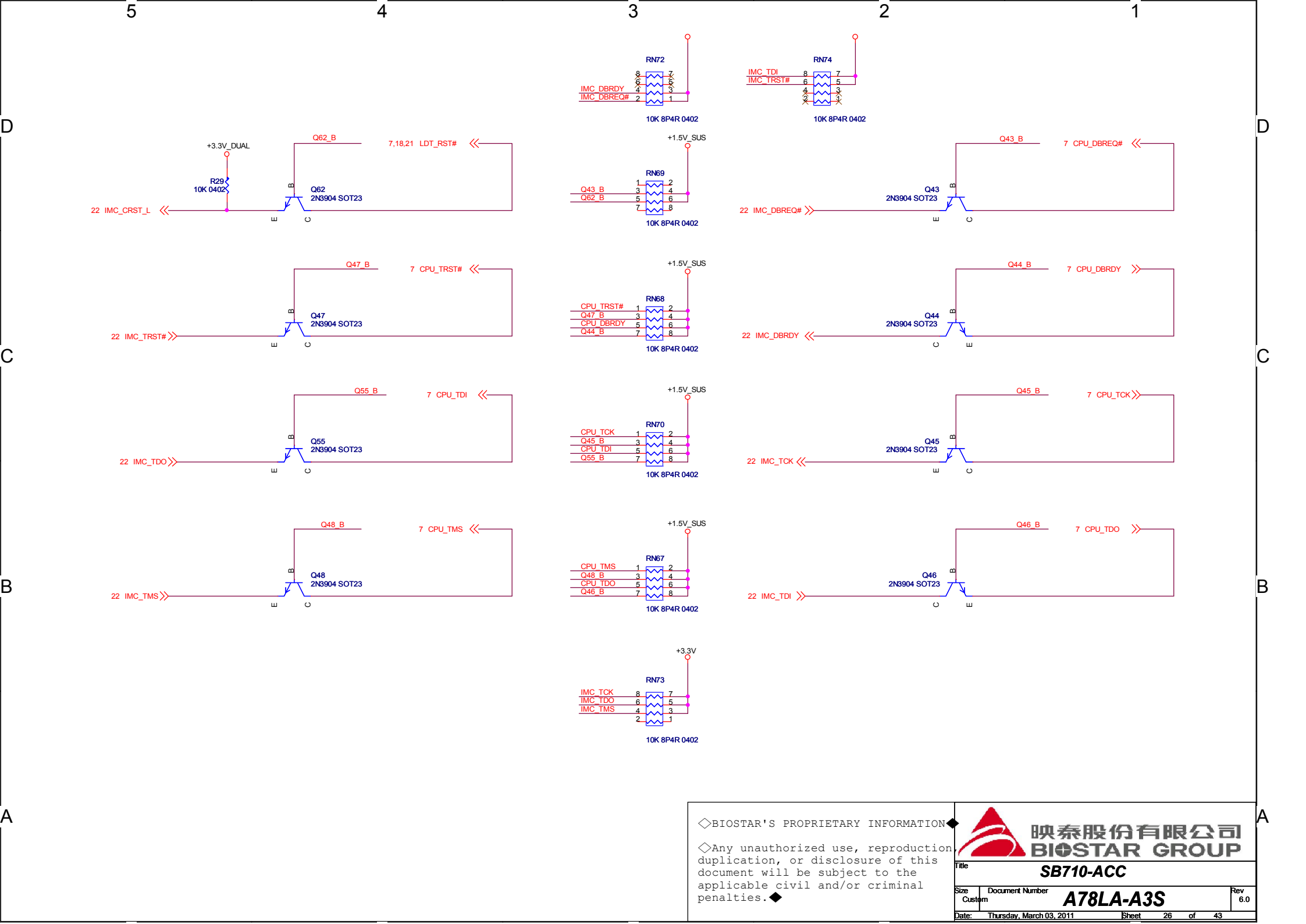
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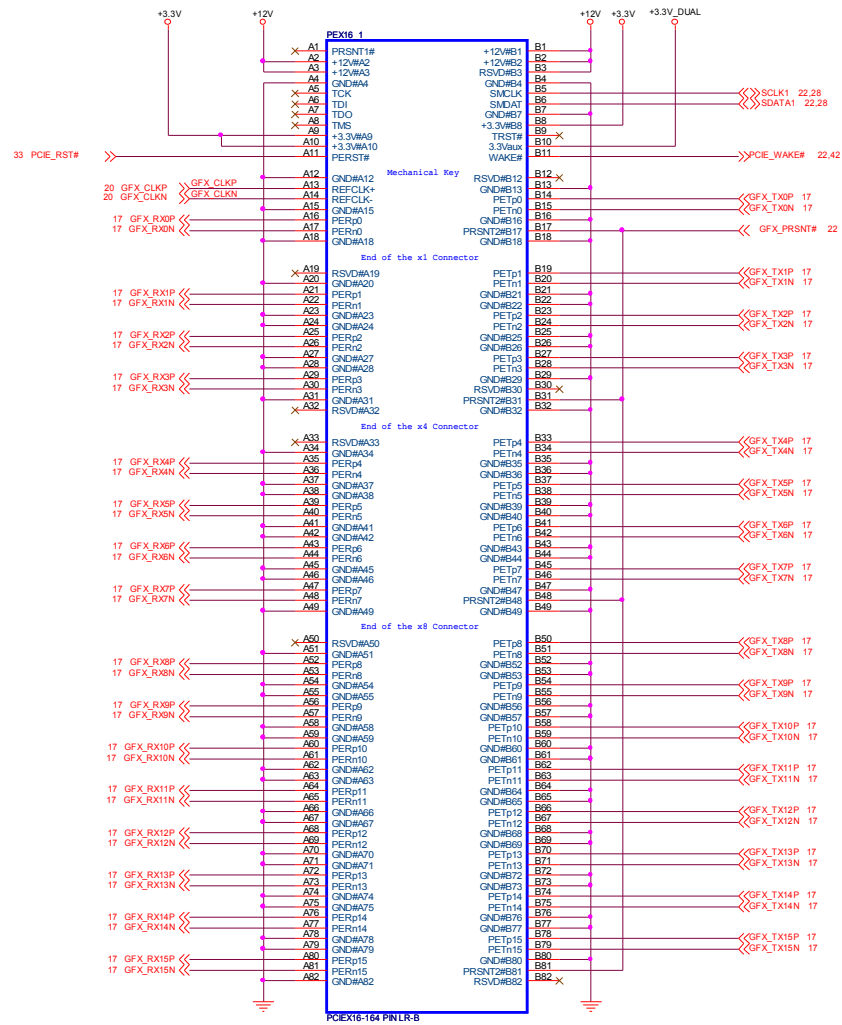
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SB710 STRAP

Size Custom Document Number
A78LA-A3S

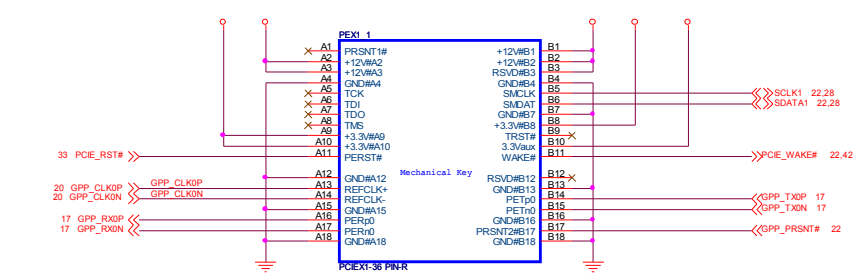
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6.0

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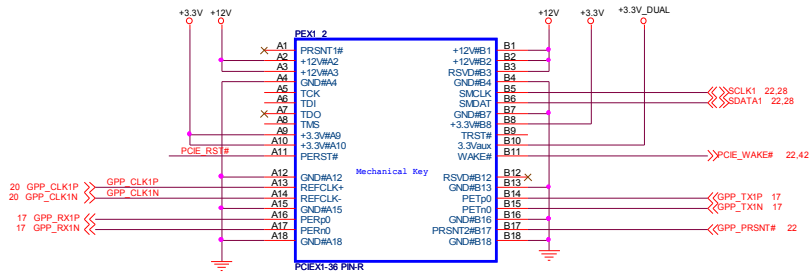
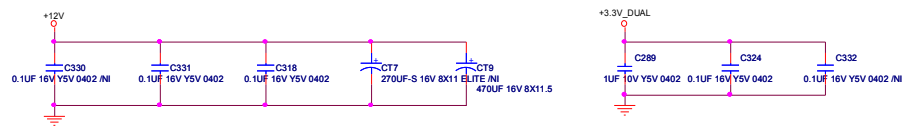




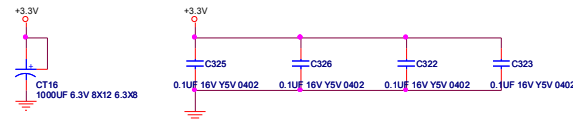
PCIEX16-164 PINLR-B



PCIEX1-36 PINR



PCIEX1-36 PINR



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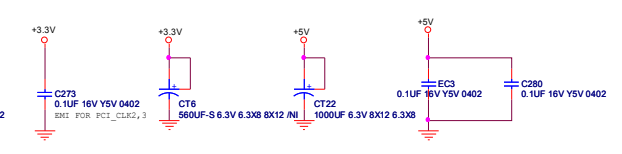
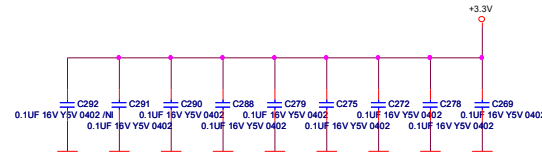
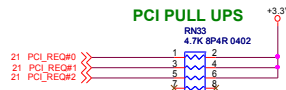
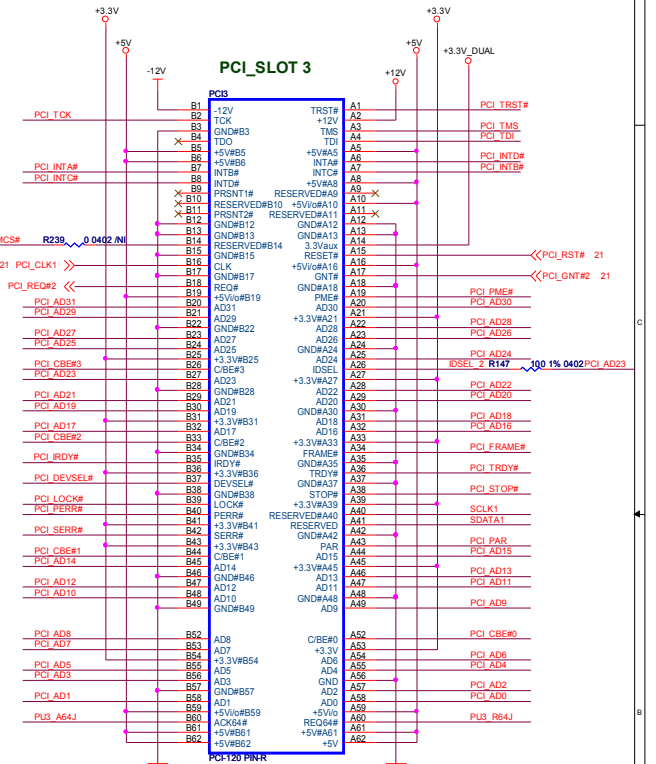
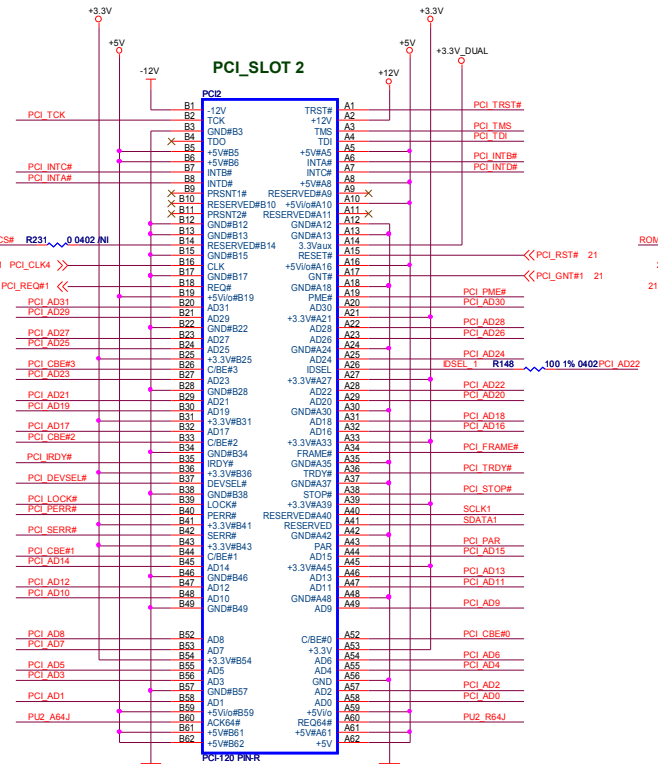
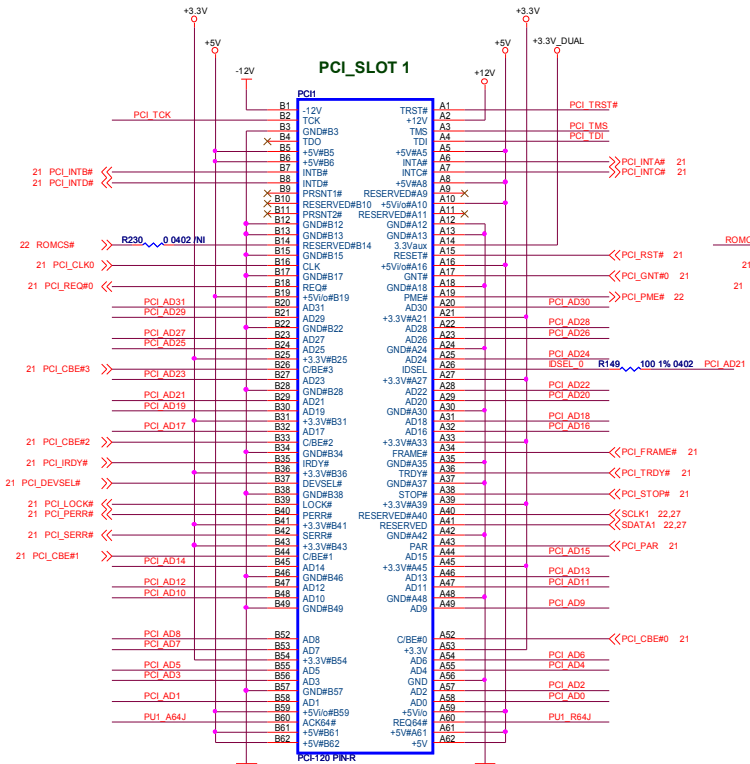
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File: **PCI-E SLOT**
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IDSEL:AD21, INT:ABCD, REQ0 & GNT0, PCI_CLK3

IDSEL:AD22, INT:BCDA, REQ1 & GNT1, PCI_CLK4

IDSEL:AD23, INT:DABC, REQ2 & GNT2, PCI_CLK2



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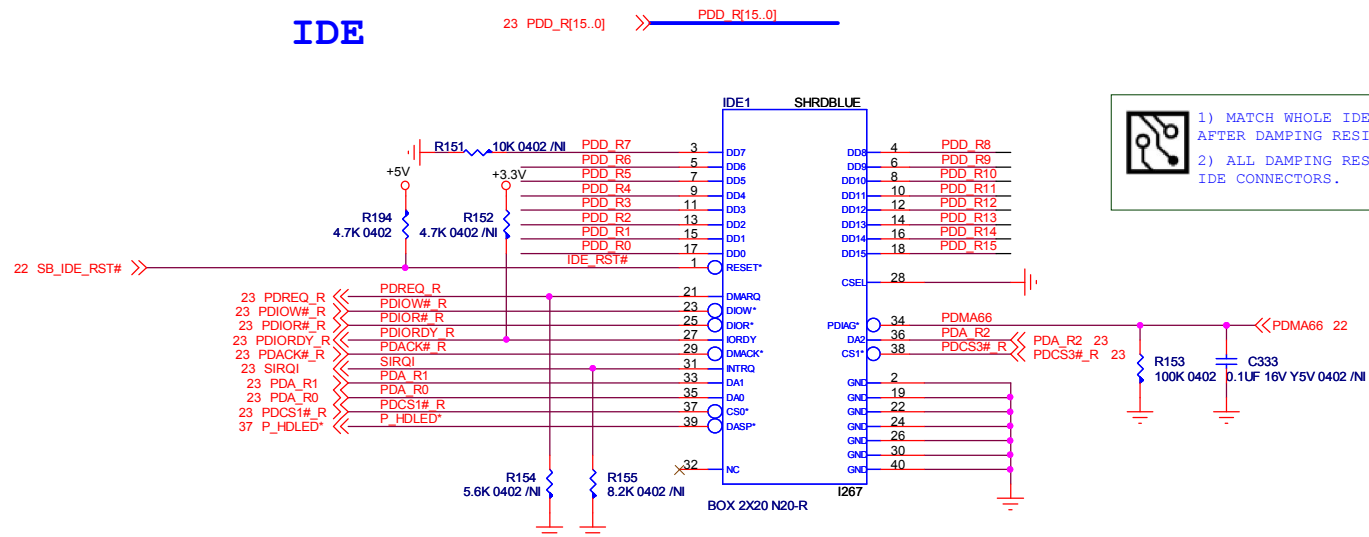
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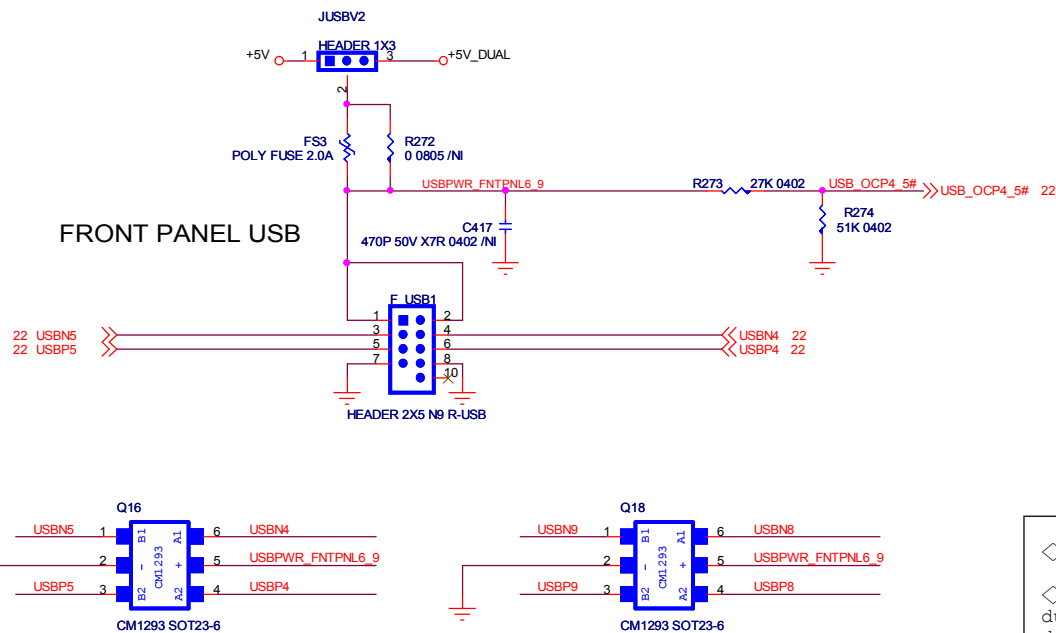
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File Document Number A78LA-A3S	Rev 8.0
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IDE

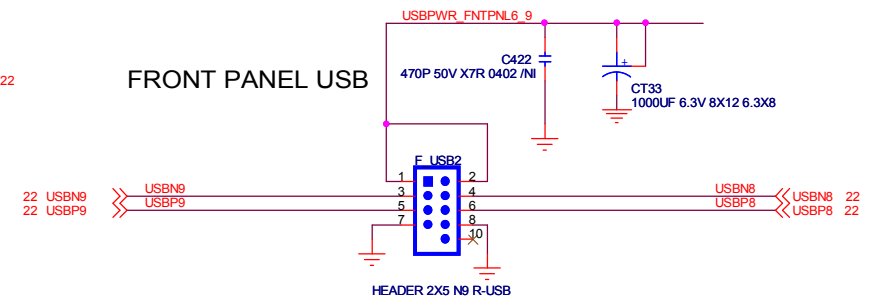


- 1) MATCH WHOLE IDE LINES (BEFORE AND AFTER DAMPING RESISTORS) WITHIN 0.5"
- 2) ALL DAMPING RESISTORS CLOSE TO IDE CONNECTORS.

FORNT USB



FRONT PANEL USB

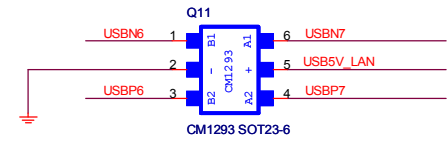
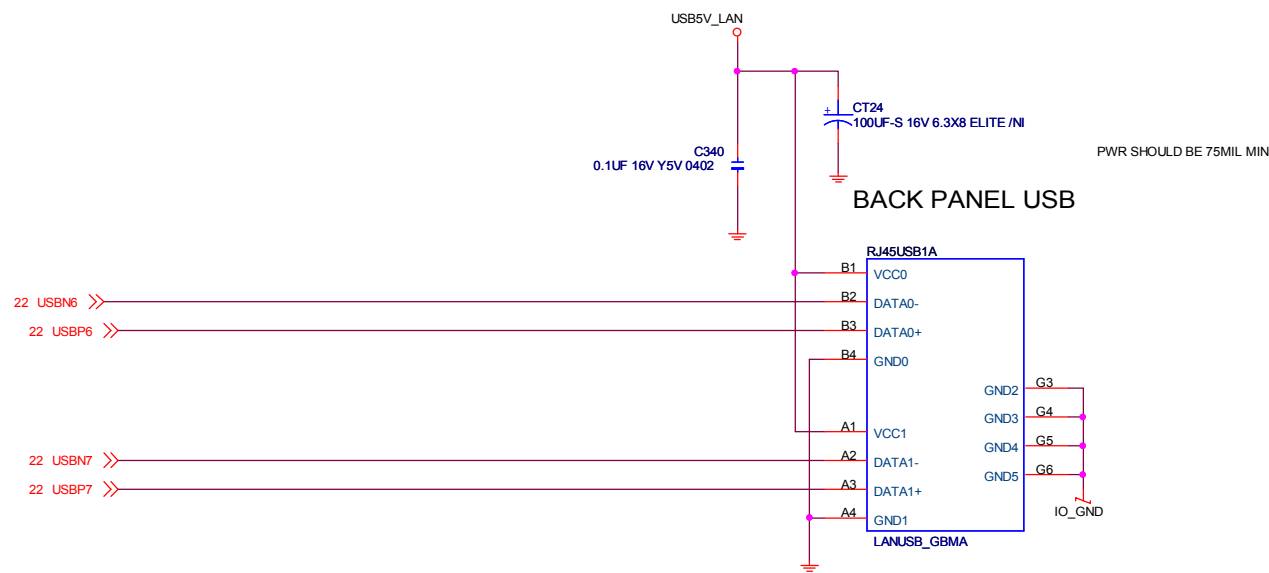


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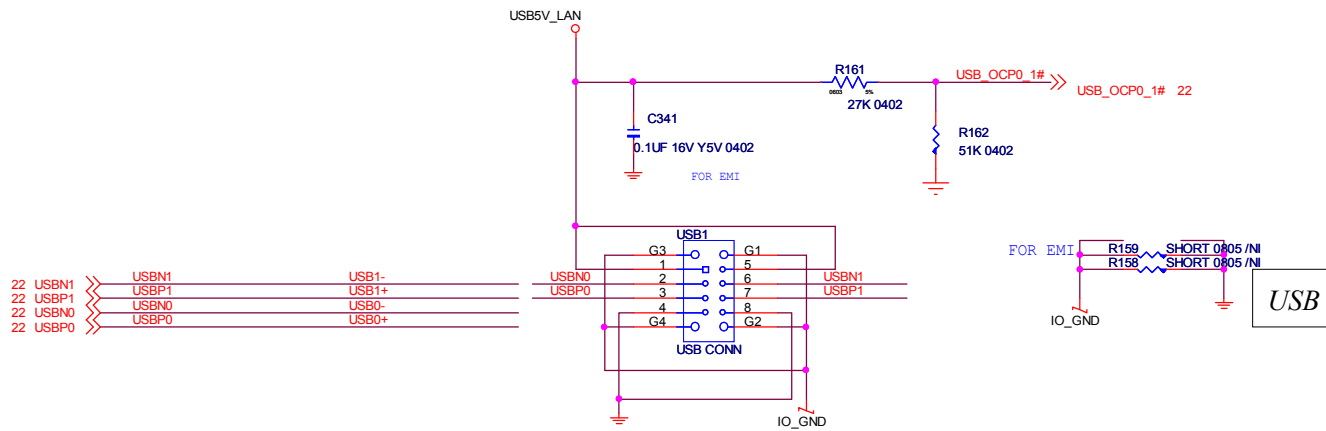
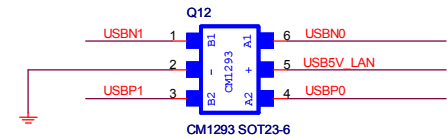
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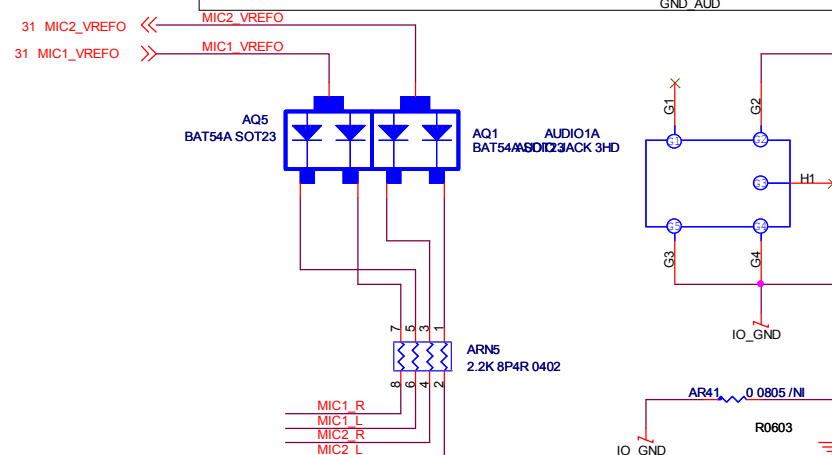
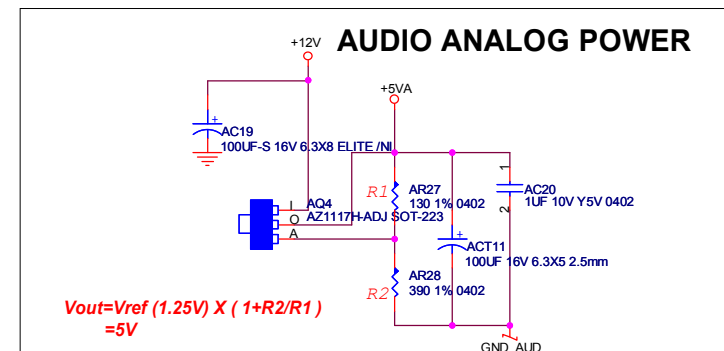
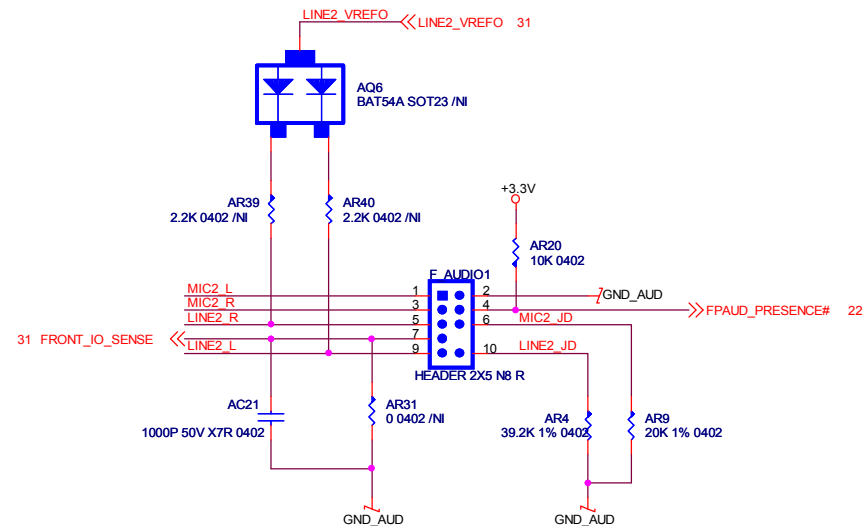
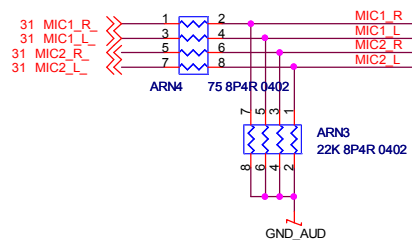
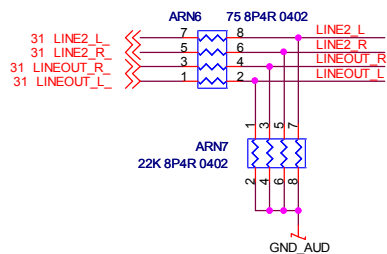
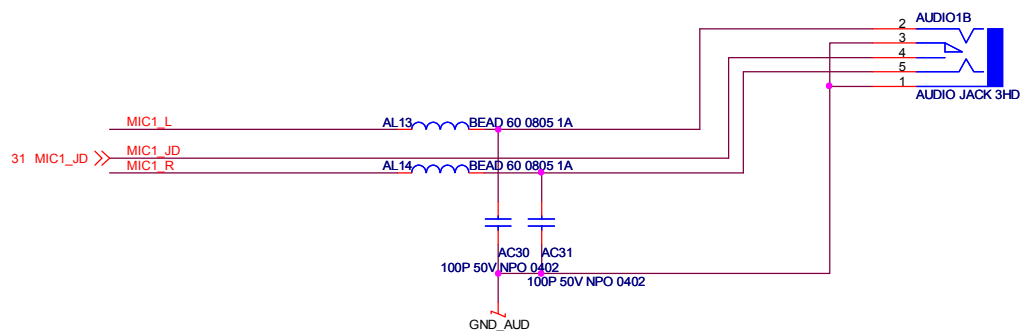
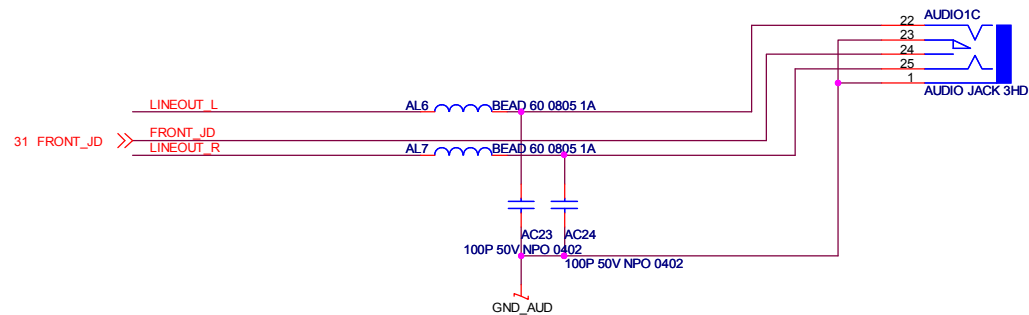
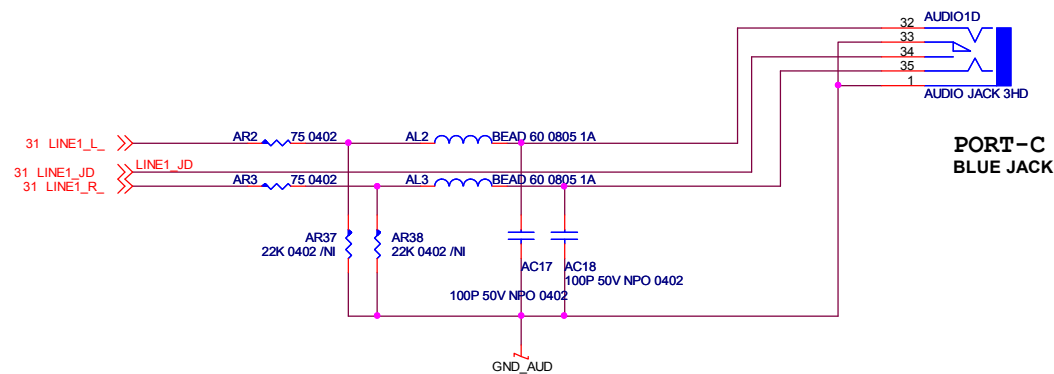
PLACE NEAR CONN



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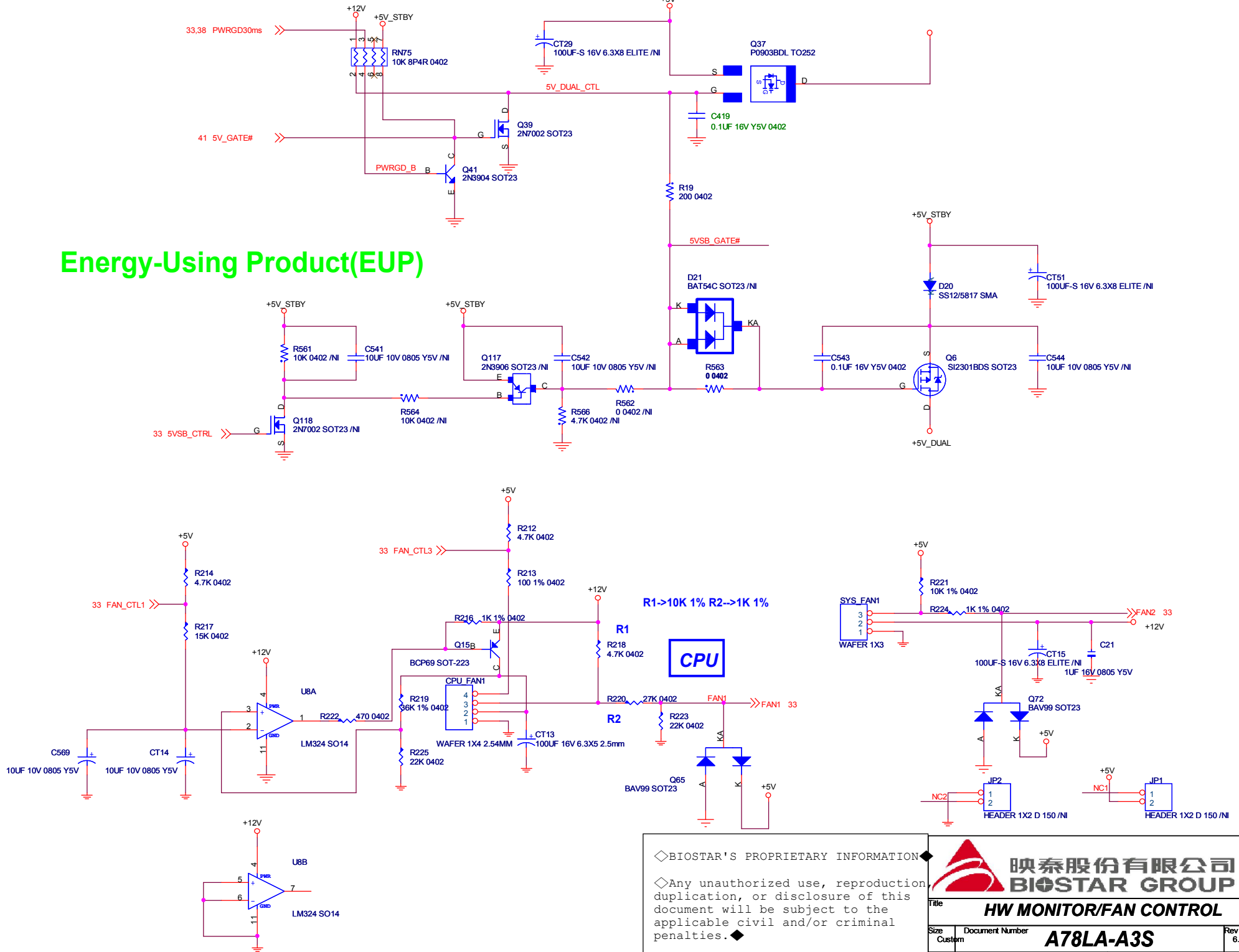
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Title **AUDIO CONNECTOR**

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Energy-Using Product(EUP)



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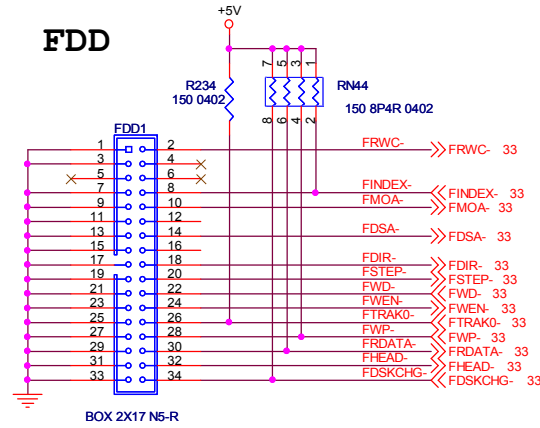
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Title: **HW MONITOR/FAN CONTROL**

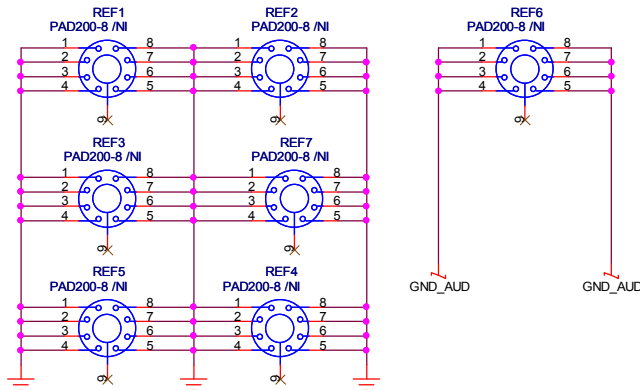
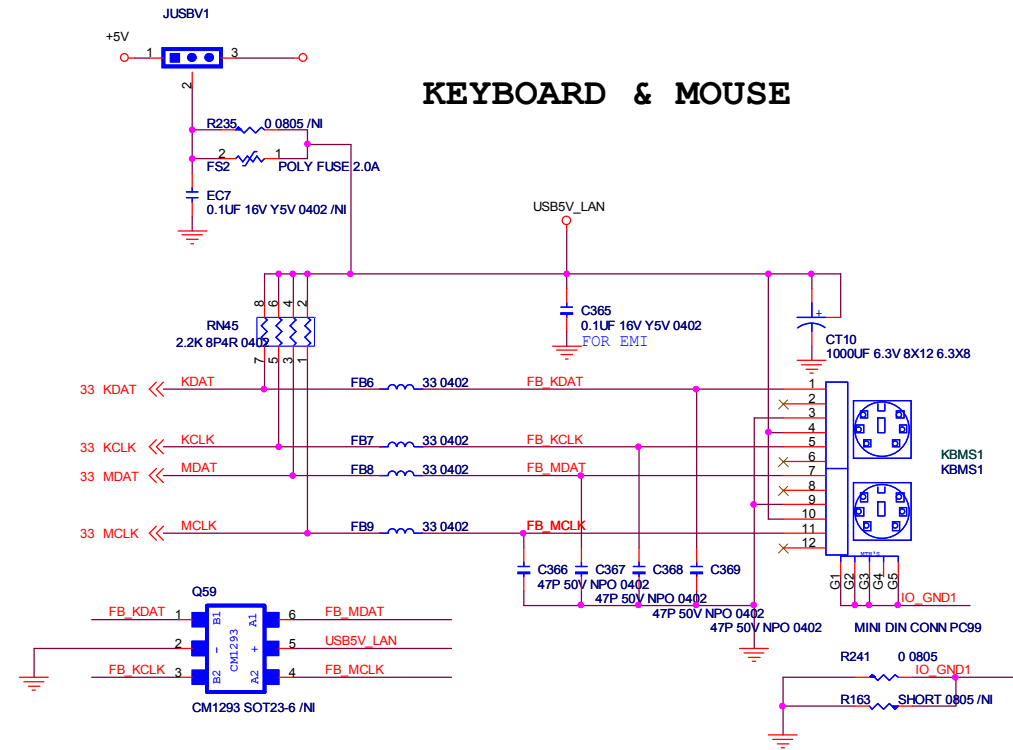
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FDD



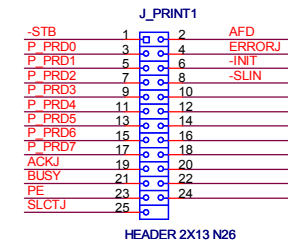
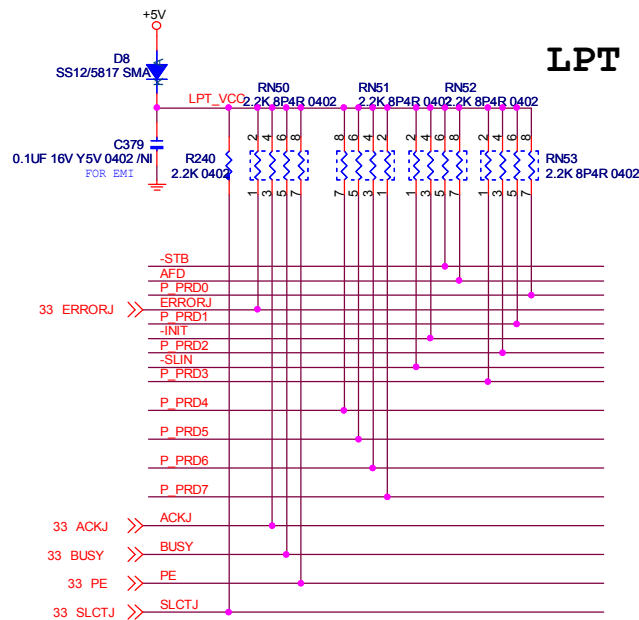
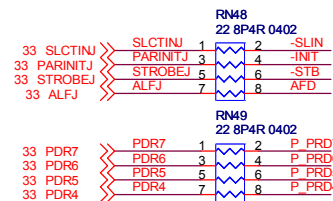
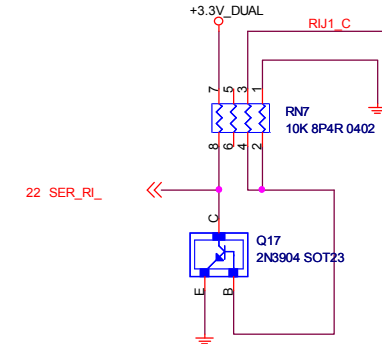
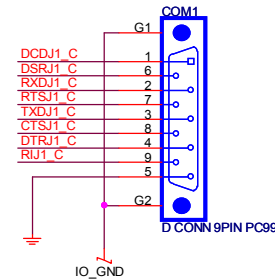
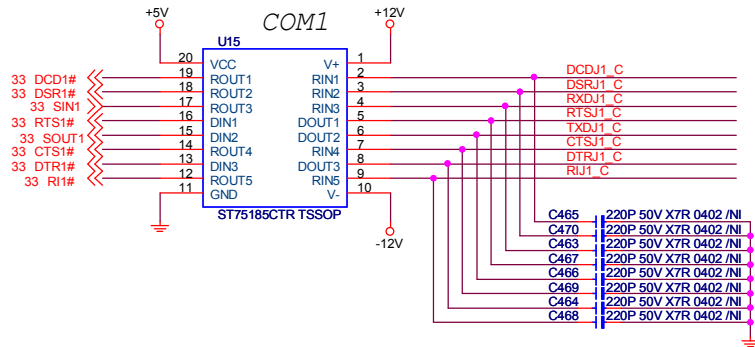
KEYBOARD & MOUSE



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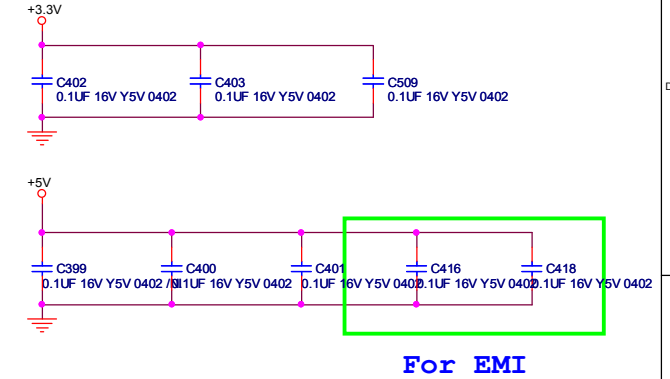
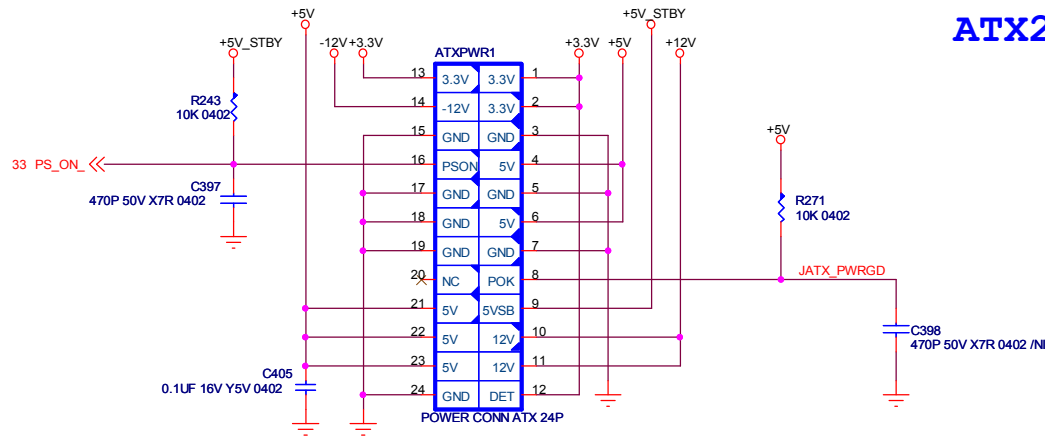
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Title **COM & PRINTER CONNECTOR**

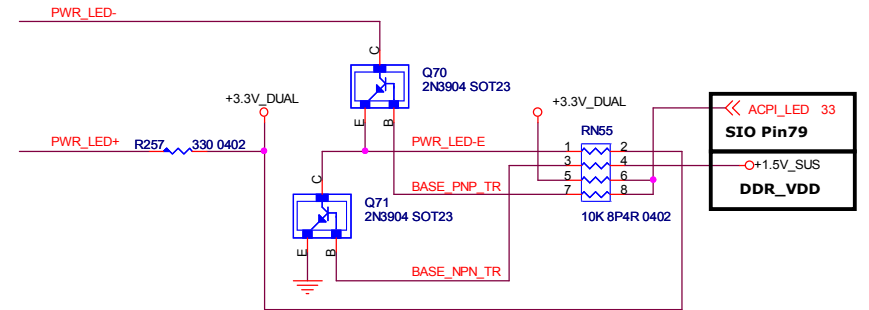
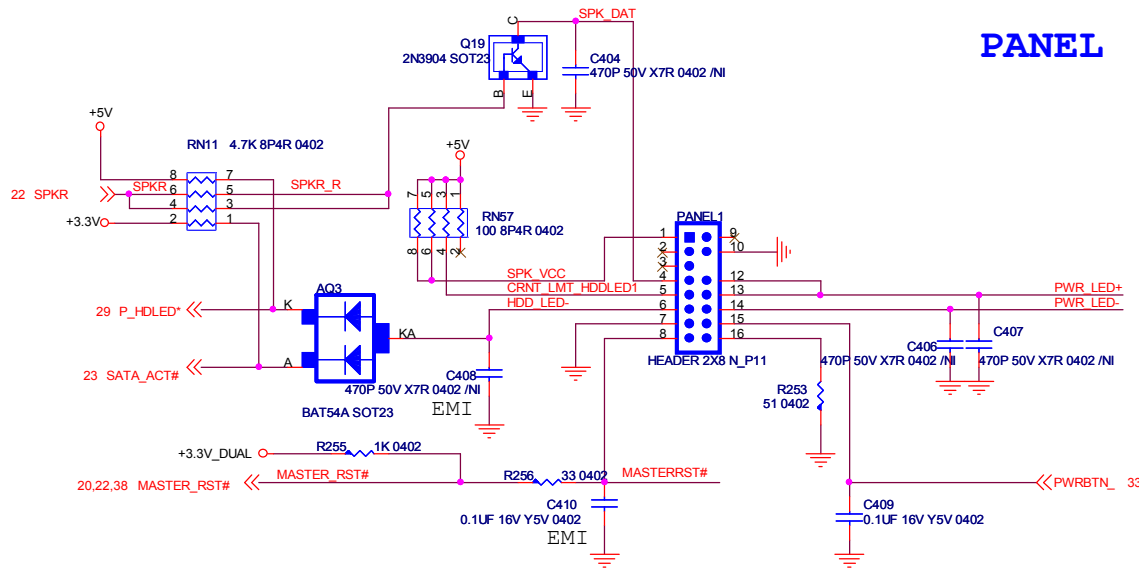
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ATX24



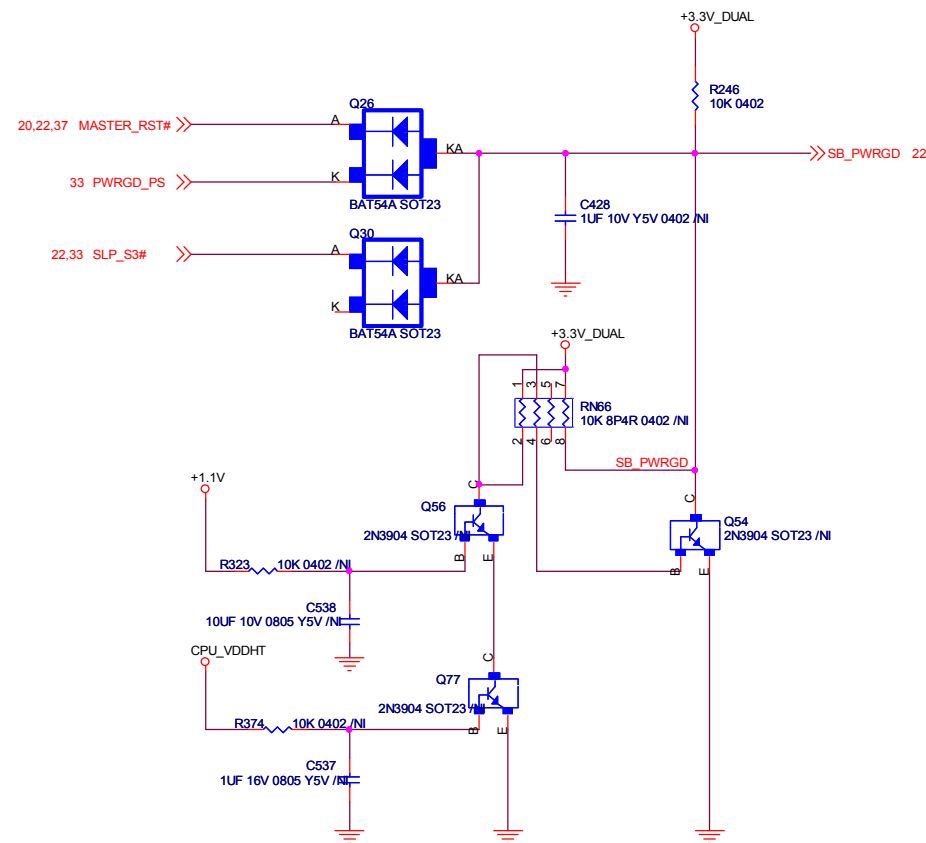
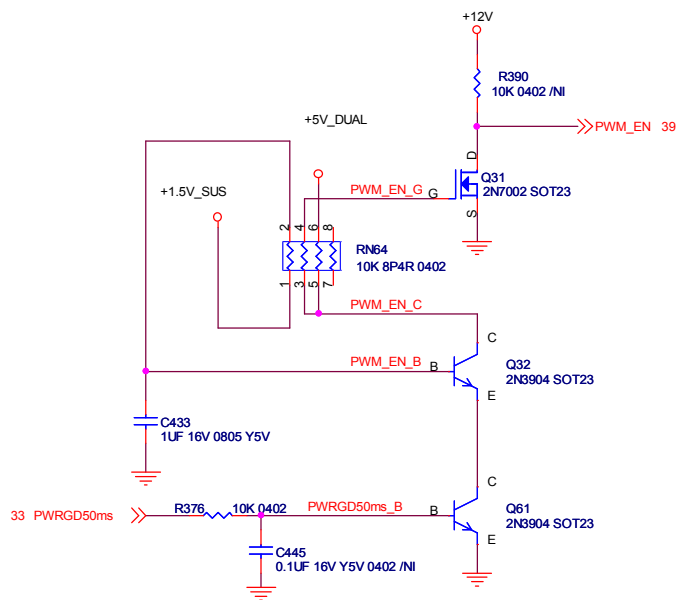
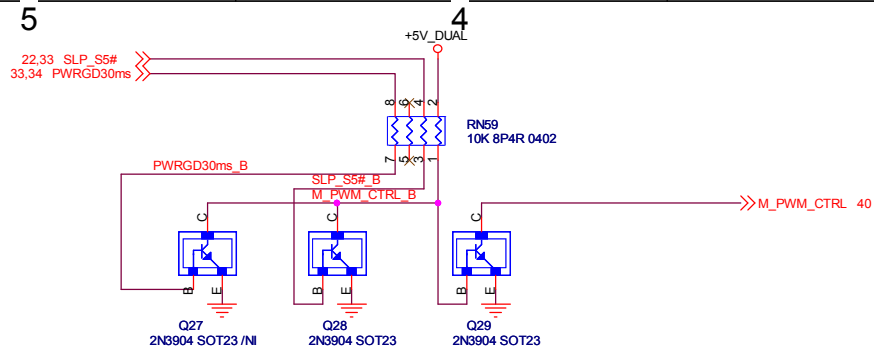
PANEL



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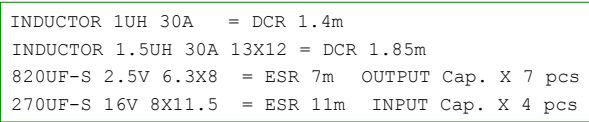
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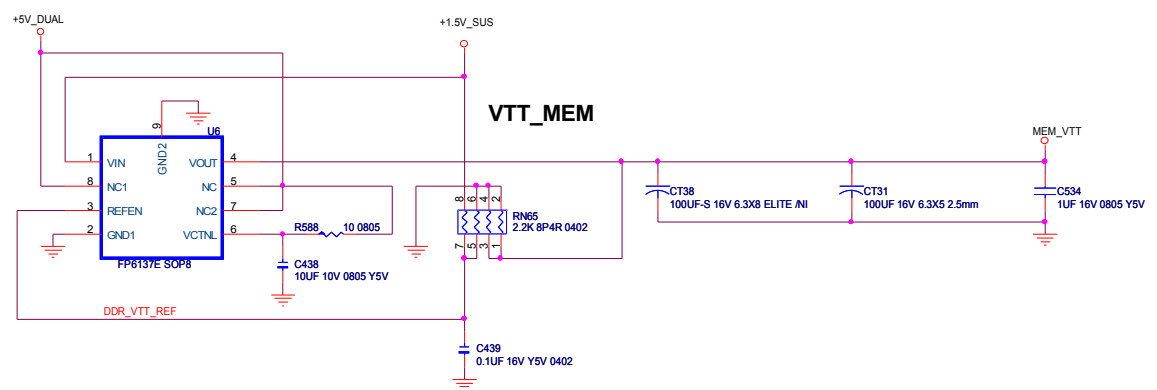
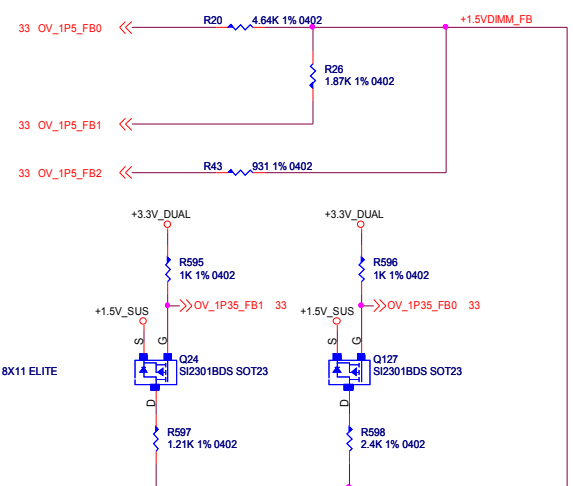
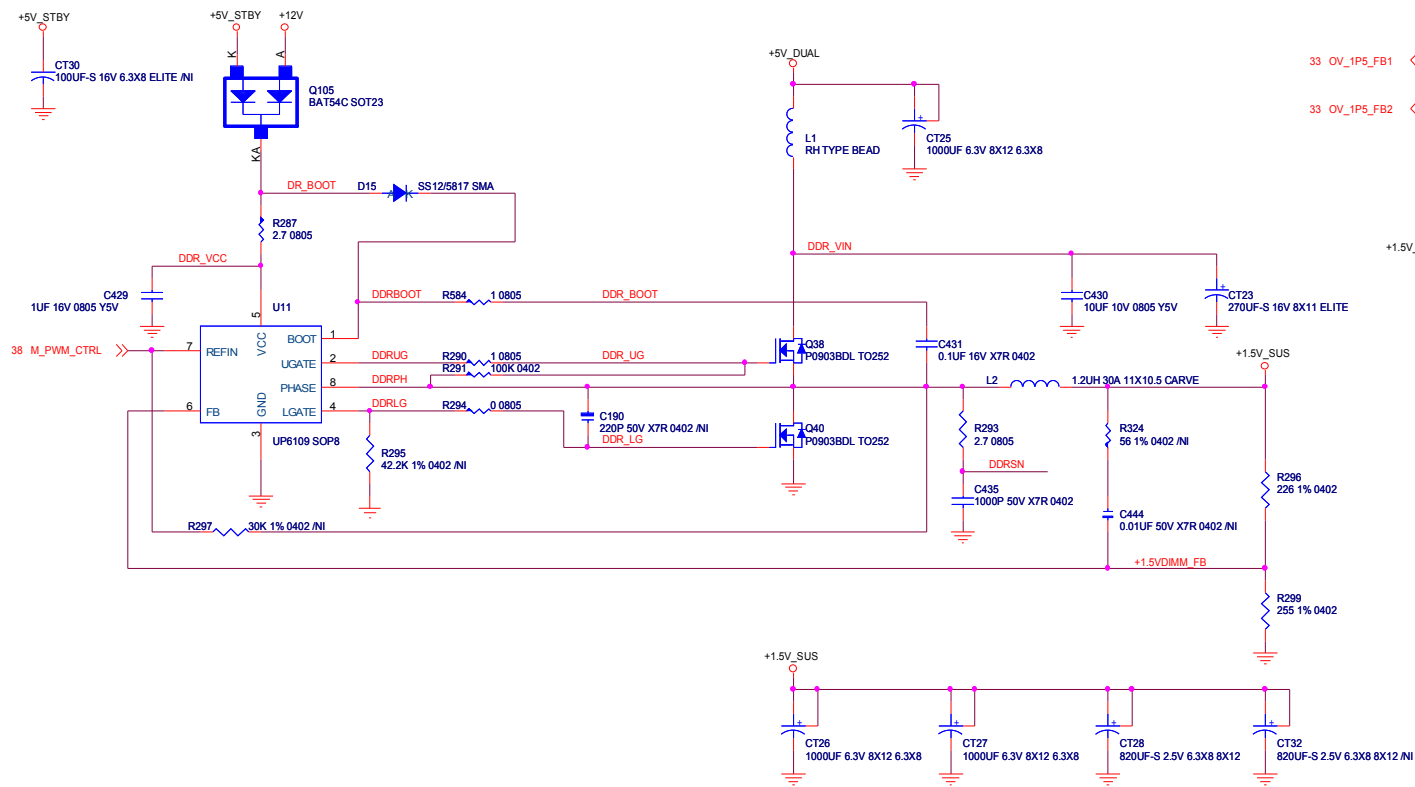
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Title **PWR GD / MISC POWER**

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+1.5V_DIMM_FB	OV_1P35_FB1	OV_1P35_FB0
1.353V	0	0
1.397V	0	1
1.447V	1	0
Default 1.509V	1	1

+1.5V_DIMM_FB	OV_1P5_FB0	OV_1P5_FB1	OV_1P5_FB2
Default 1.509V	1	1	1
1.547V	0	1	1
1.605V	1	0	1
1.644V	0	0	1
1.703V	1	1	0
1.742V	0	1	0
1.799V	1	0	0
1.838V	0	0	0

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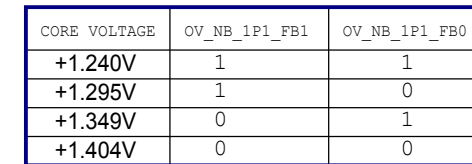
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JUSBV1(1_2)
JUMPER 2P R



3V BATTERY SONY



JUSBV2(1_2)
JUMPER 2P R



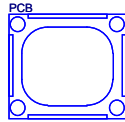
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JUMPER 2P B



SPI W25X80 DIP



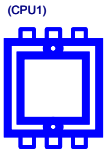
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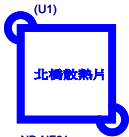
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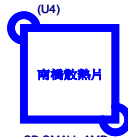
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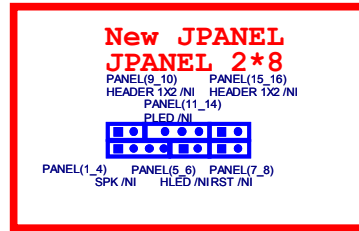
AM2RM-B



NB-NF61




SB SMALL-AMD



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