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A78LC-M3S (RS780L&SB710)

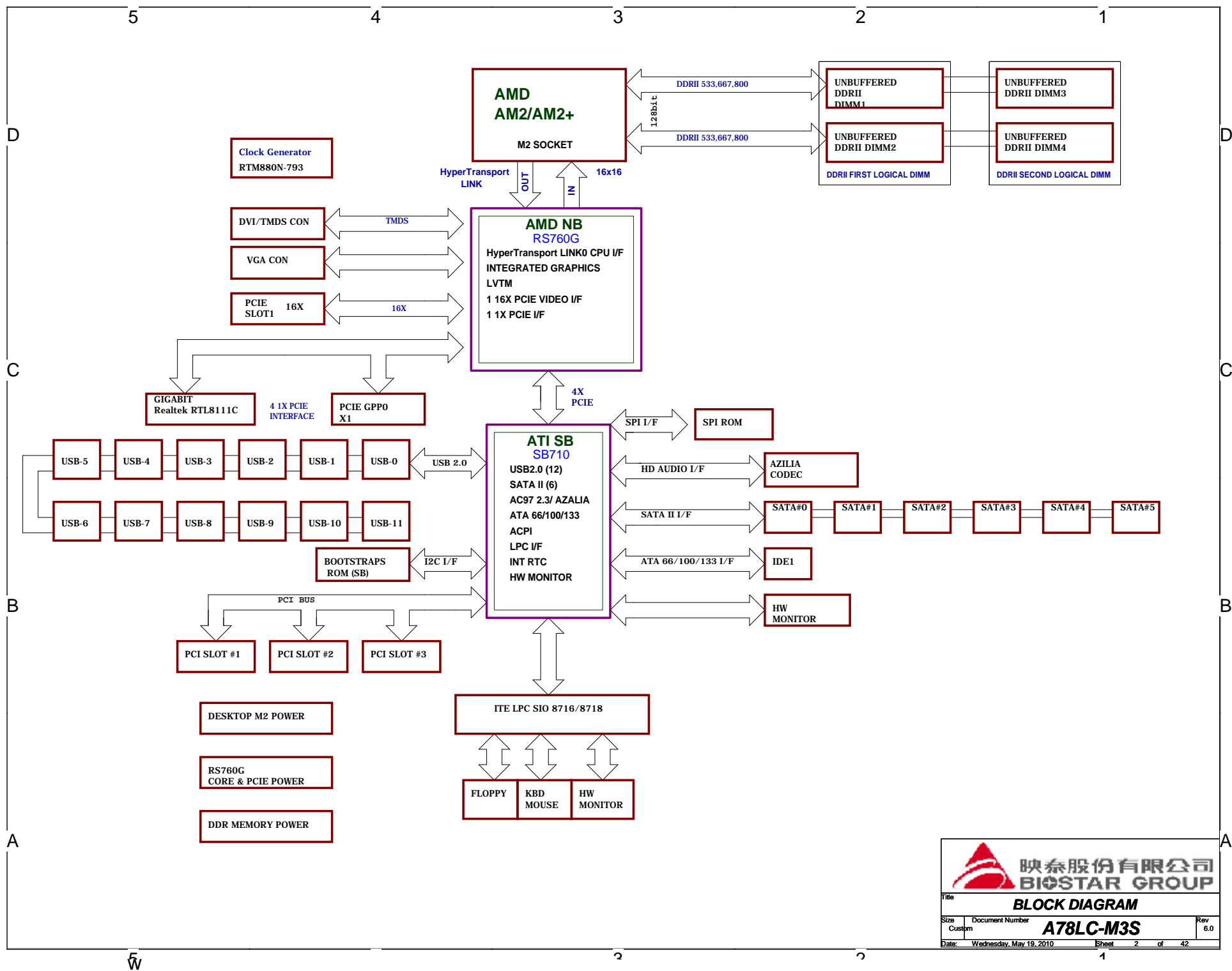
REV 6.0

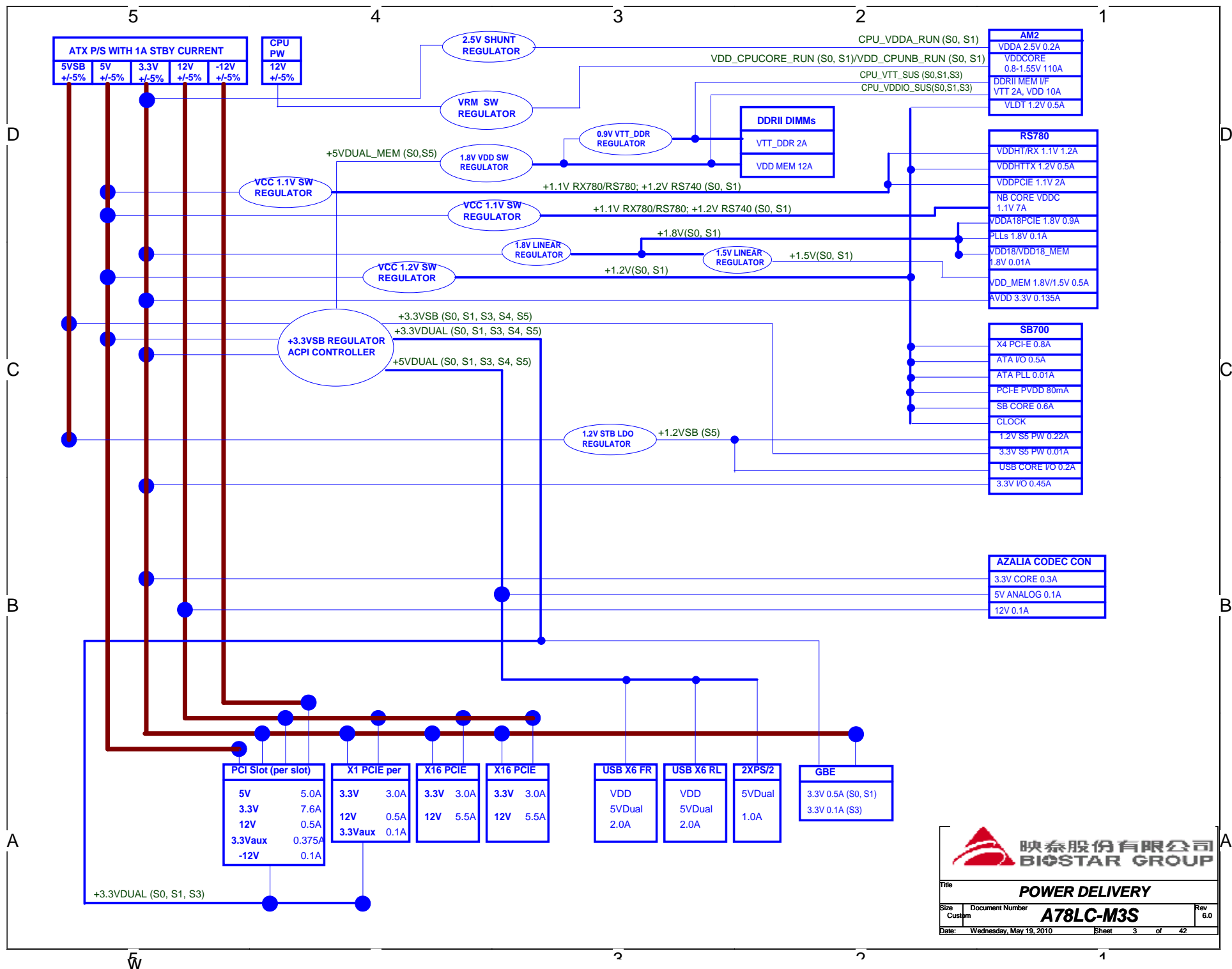
DATE :2010/05/18

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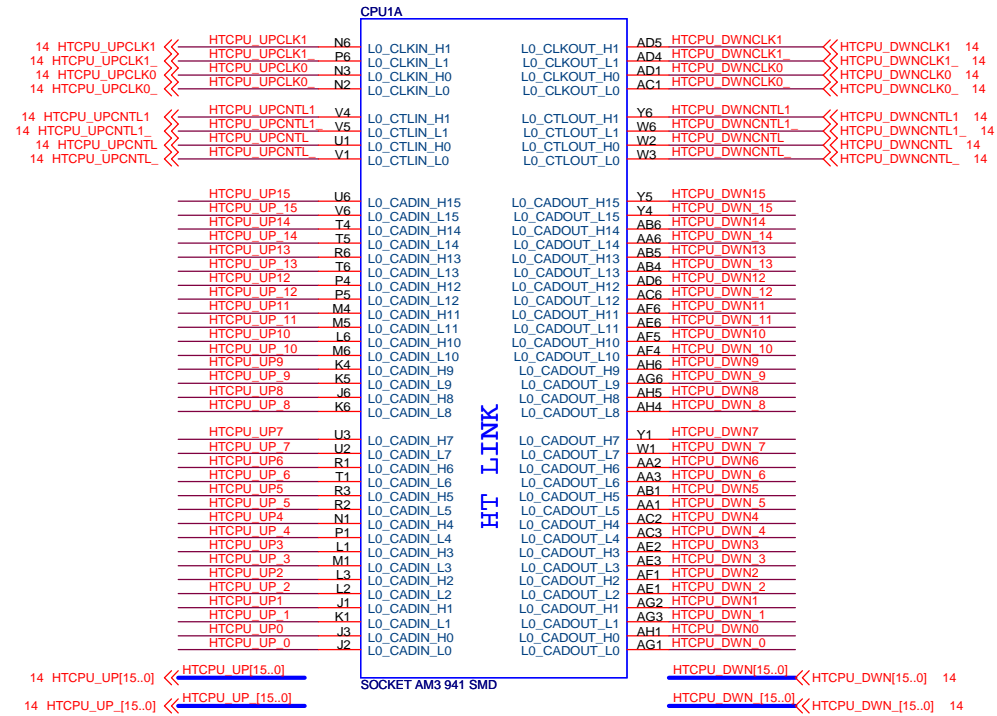
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HyperTransport 3.0



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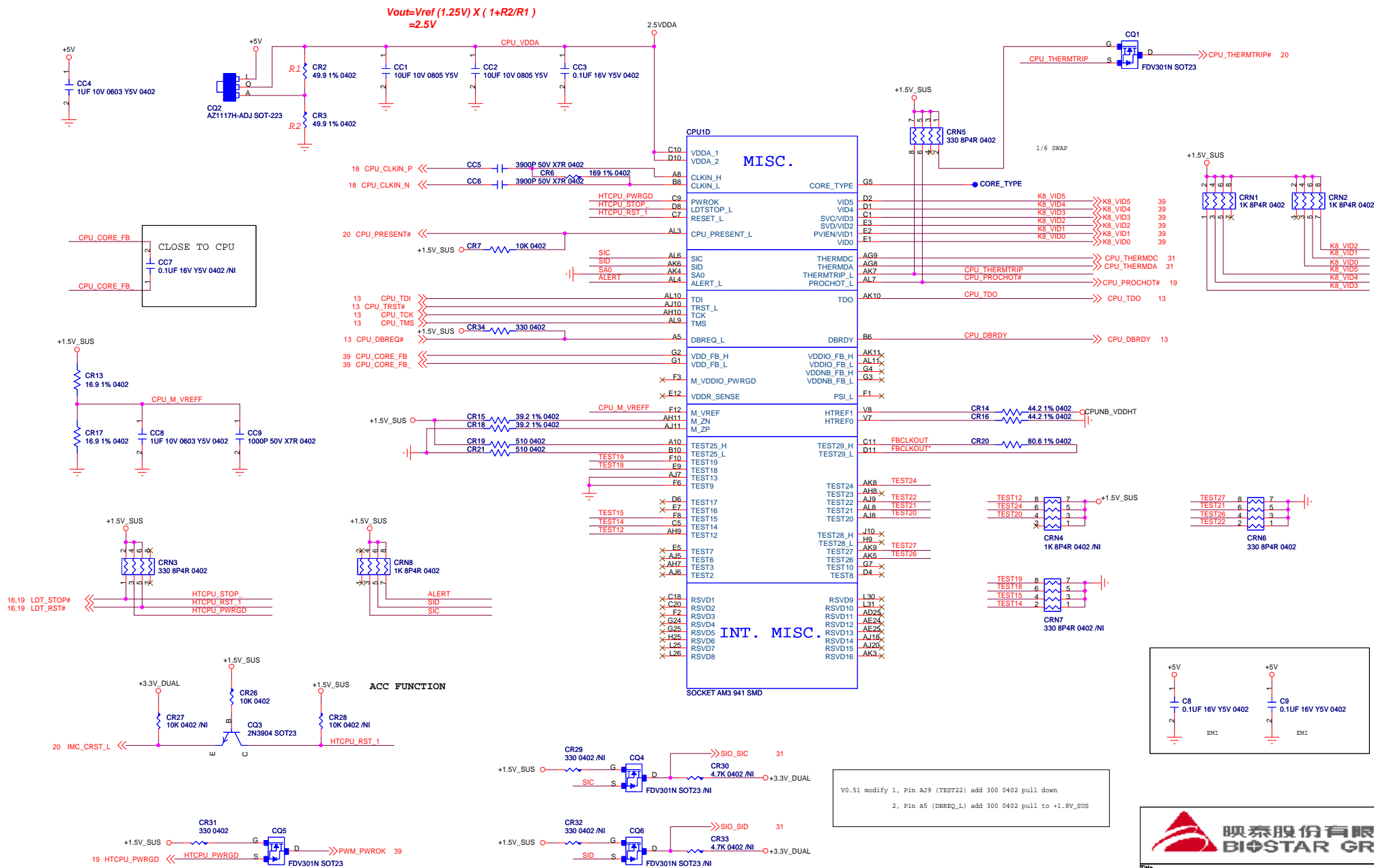
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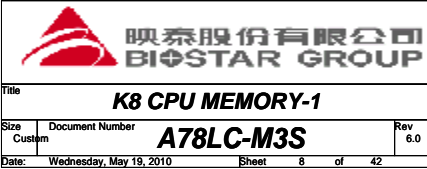
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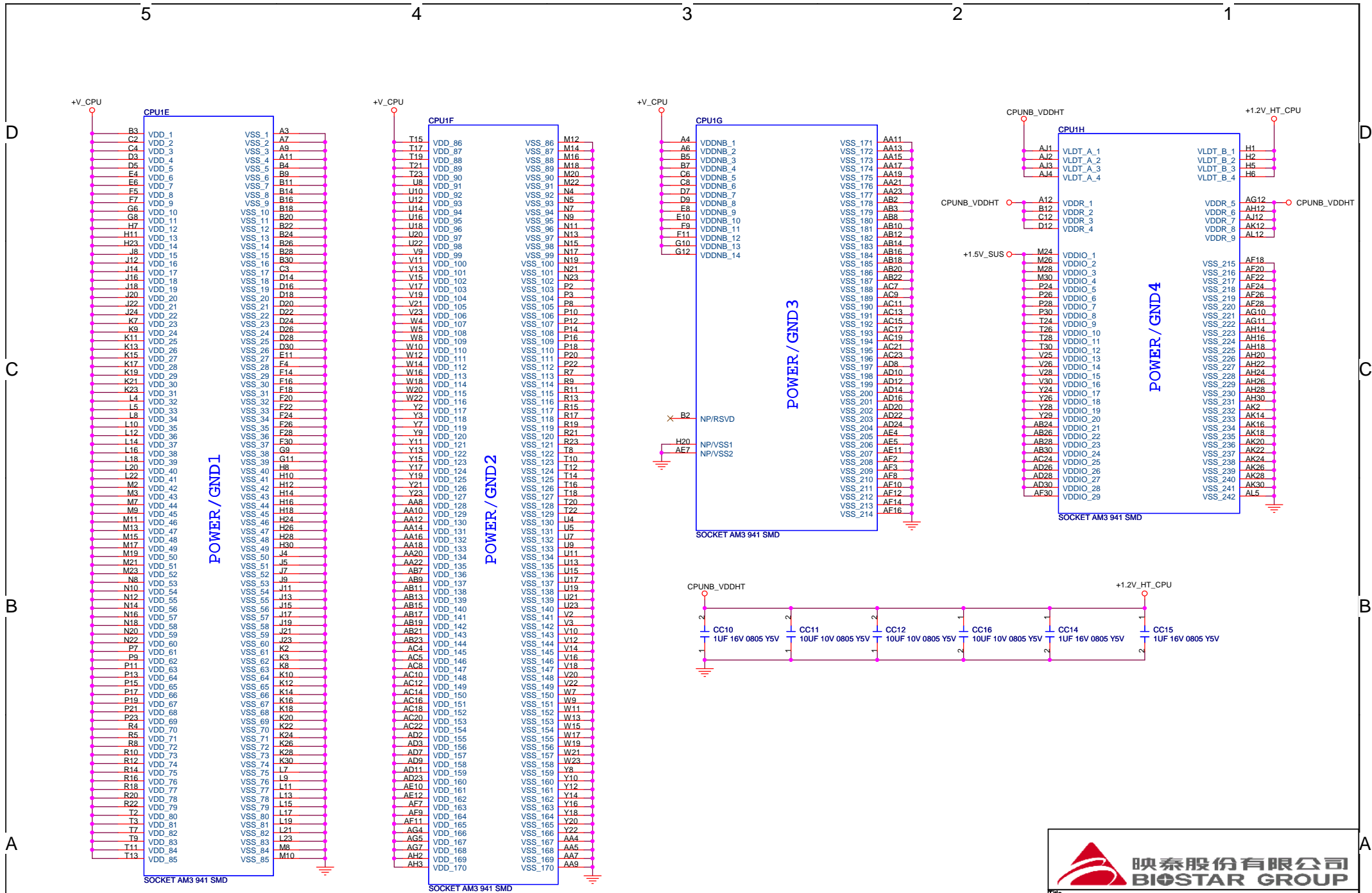
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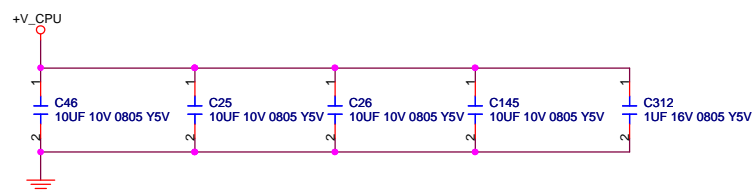
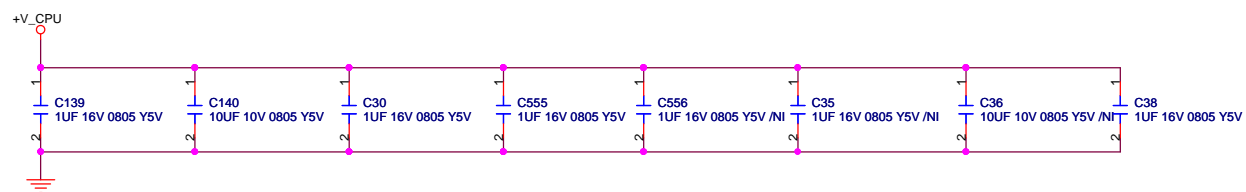
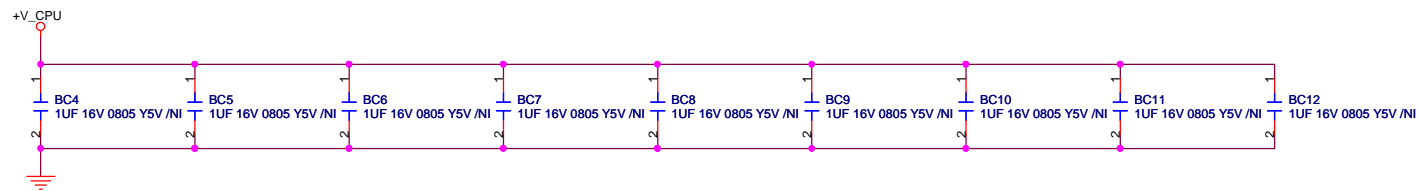
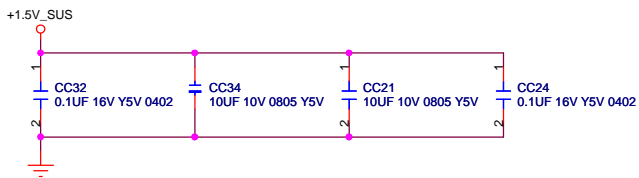
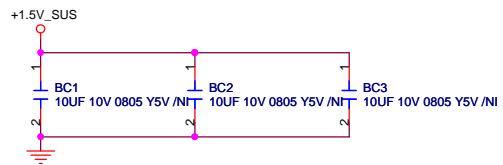
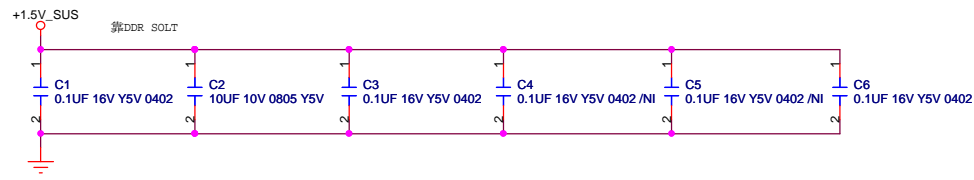
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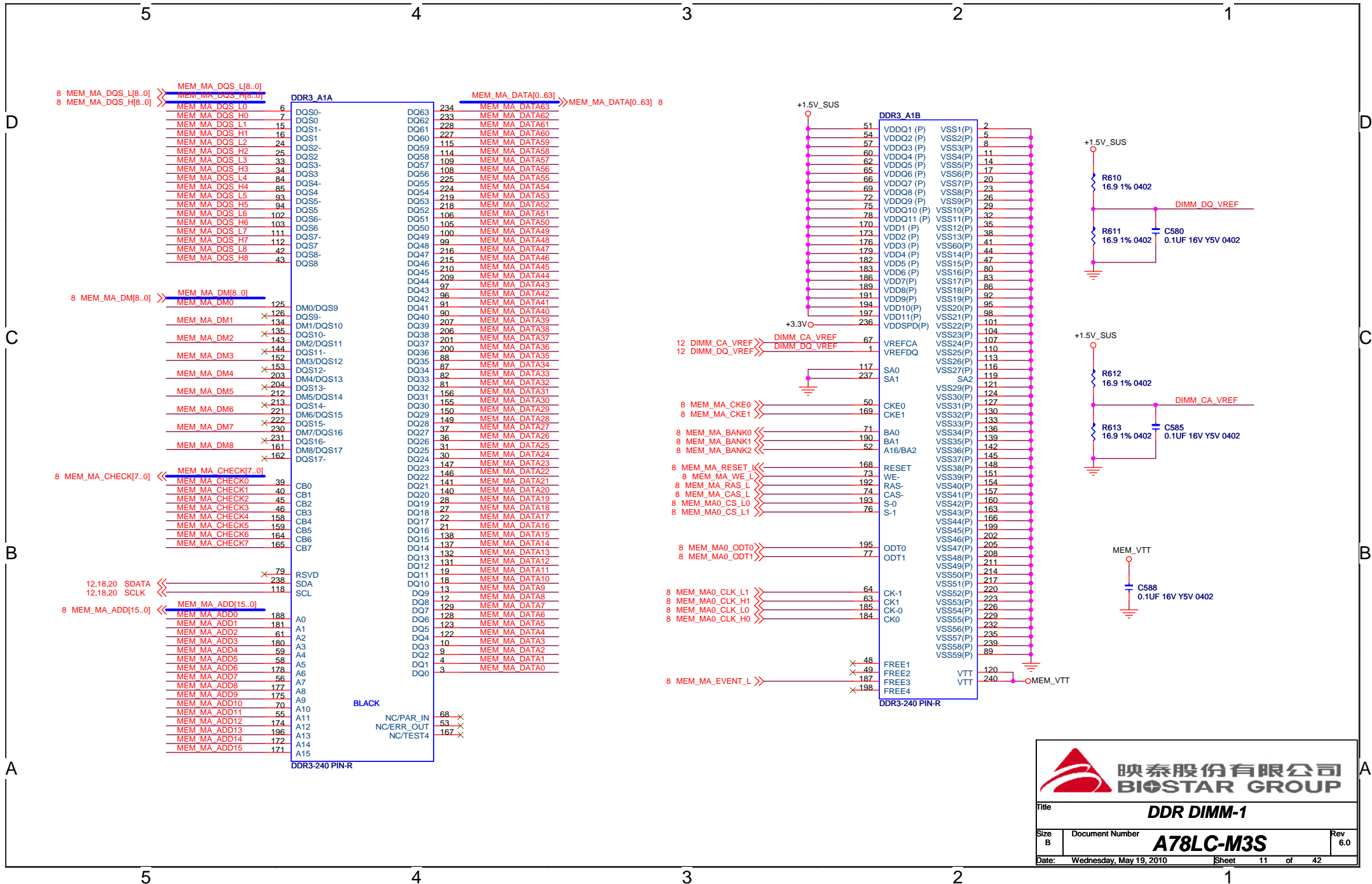


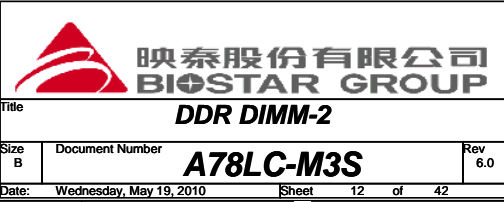






		
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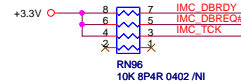
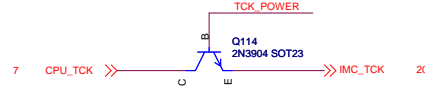
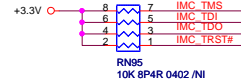
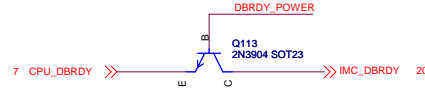
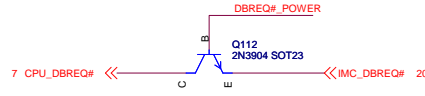
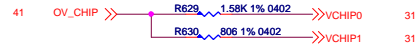
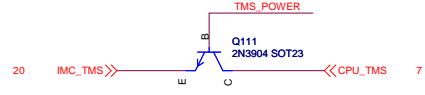
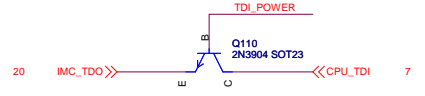
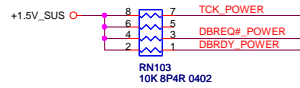
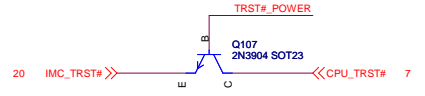
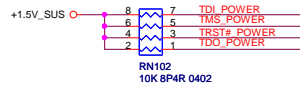
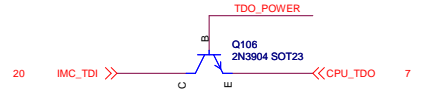
4

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D



+1.5VDIMM_FB	VDIMM0	VDIMM1	VDIMM2
Default 1.509V	1	1	1
1.547V	0	1	1
1.605V	1	0	1
1.644V	0	0	1
1.703V	1	1	0
1.742V	0	1	0
1.799V	1	0	0
1.838V	0	0	0

	OV_NB_1P1_FB0	OV_NB_1P1_FB1
+1.2V / +1.296V	1	1
+1.250V / +1.346V	0	1
+1.299V / +1.403V	1	0
+1.349V / +1.452V	0	0

	OV_SB_1P1_FB0	OV_SB_1P1_FB1
+1.204V	1	1
+1.246V	0	1
+1.284V	1	0
+1.324V	0	0

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Title

OV/ACC FUNCTION

Size

Document Number

Rev

Custom

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6.0

Date:

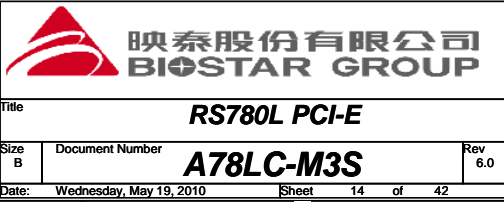
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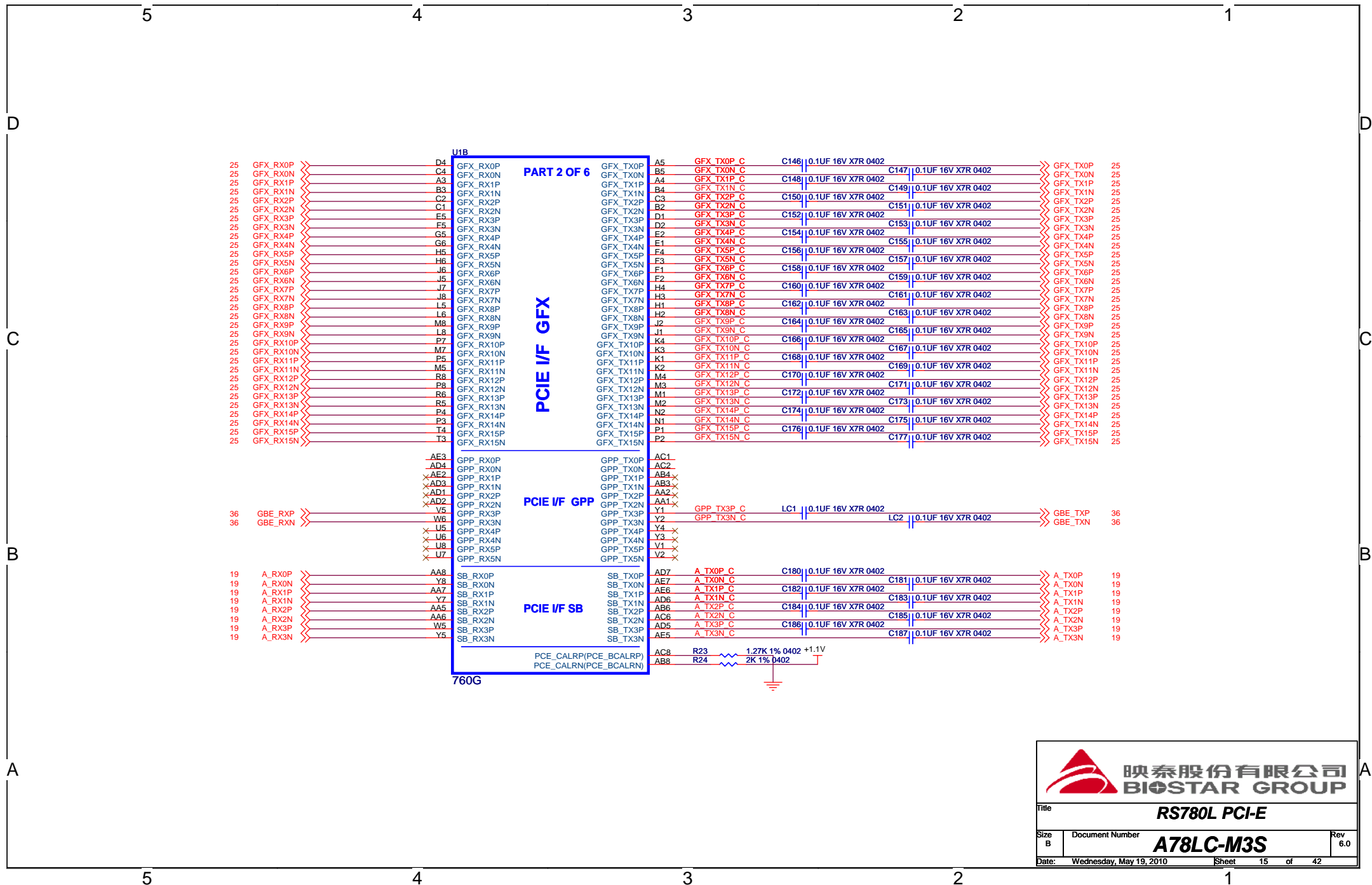
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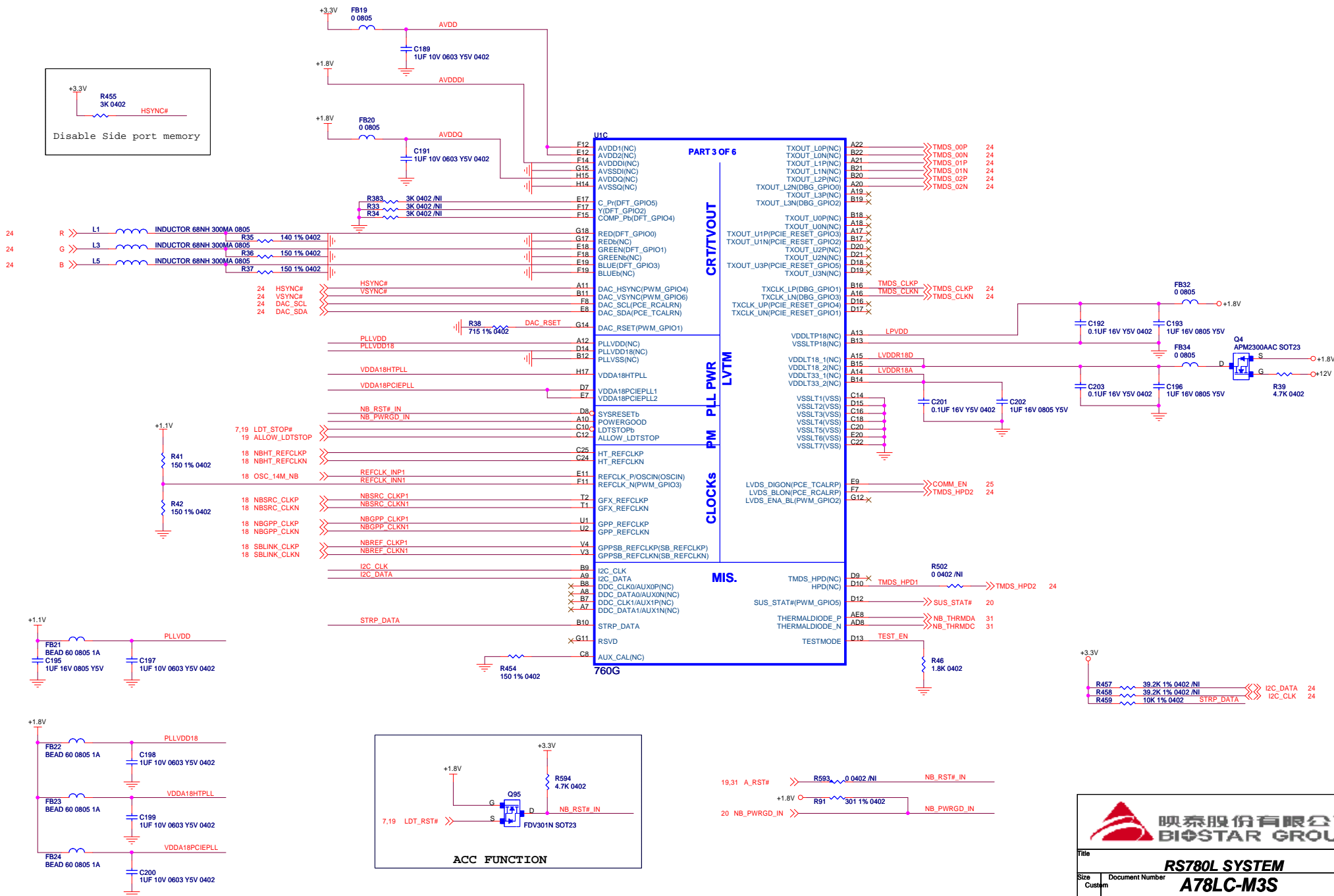
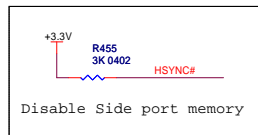
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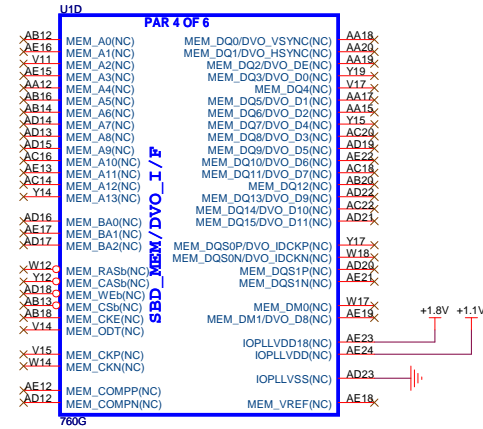
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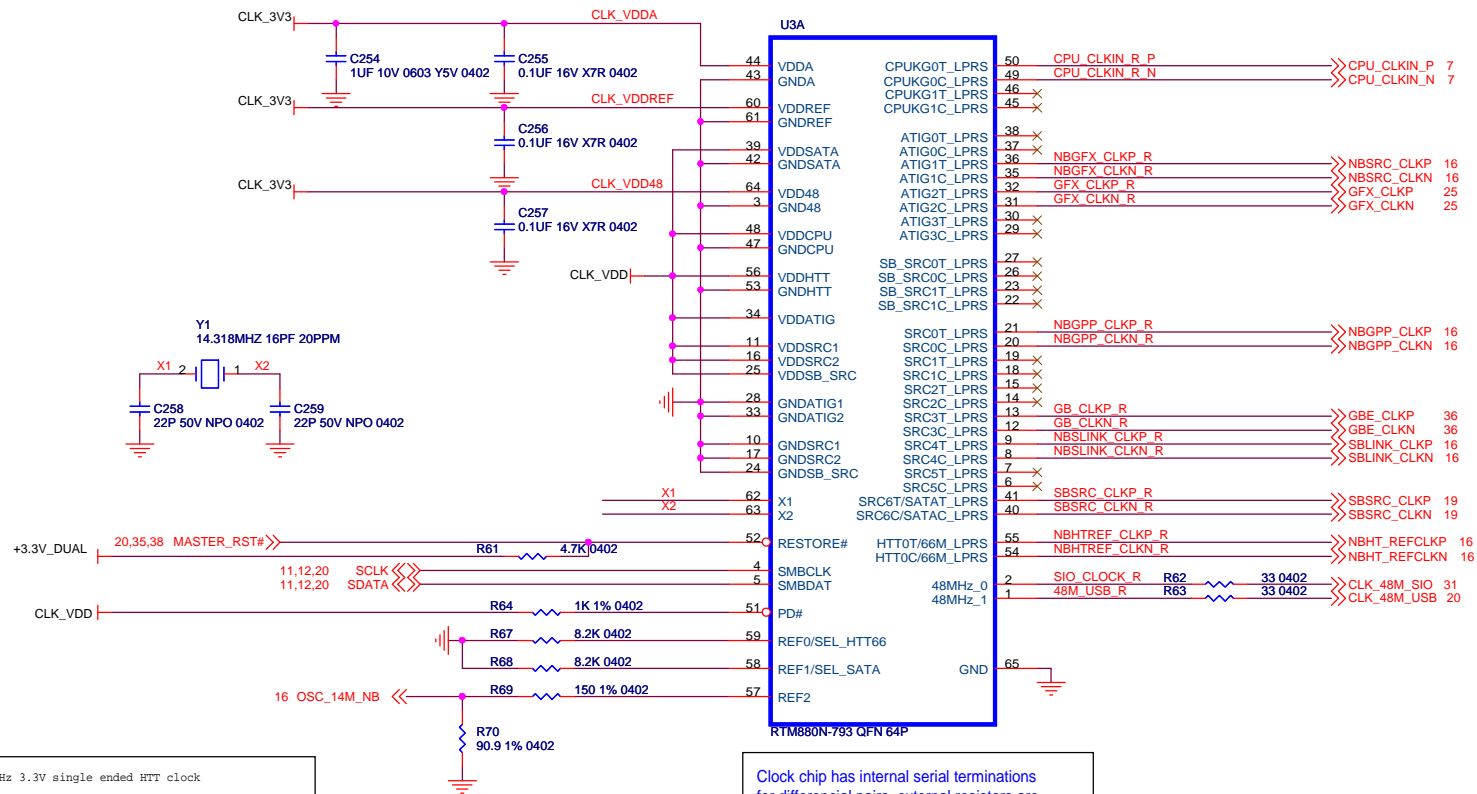
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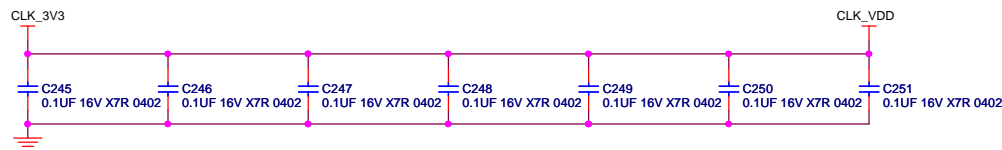
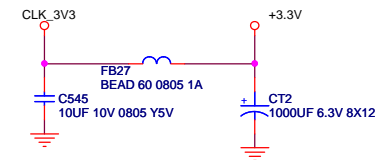





* default

SEL_HTT66	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock

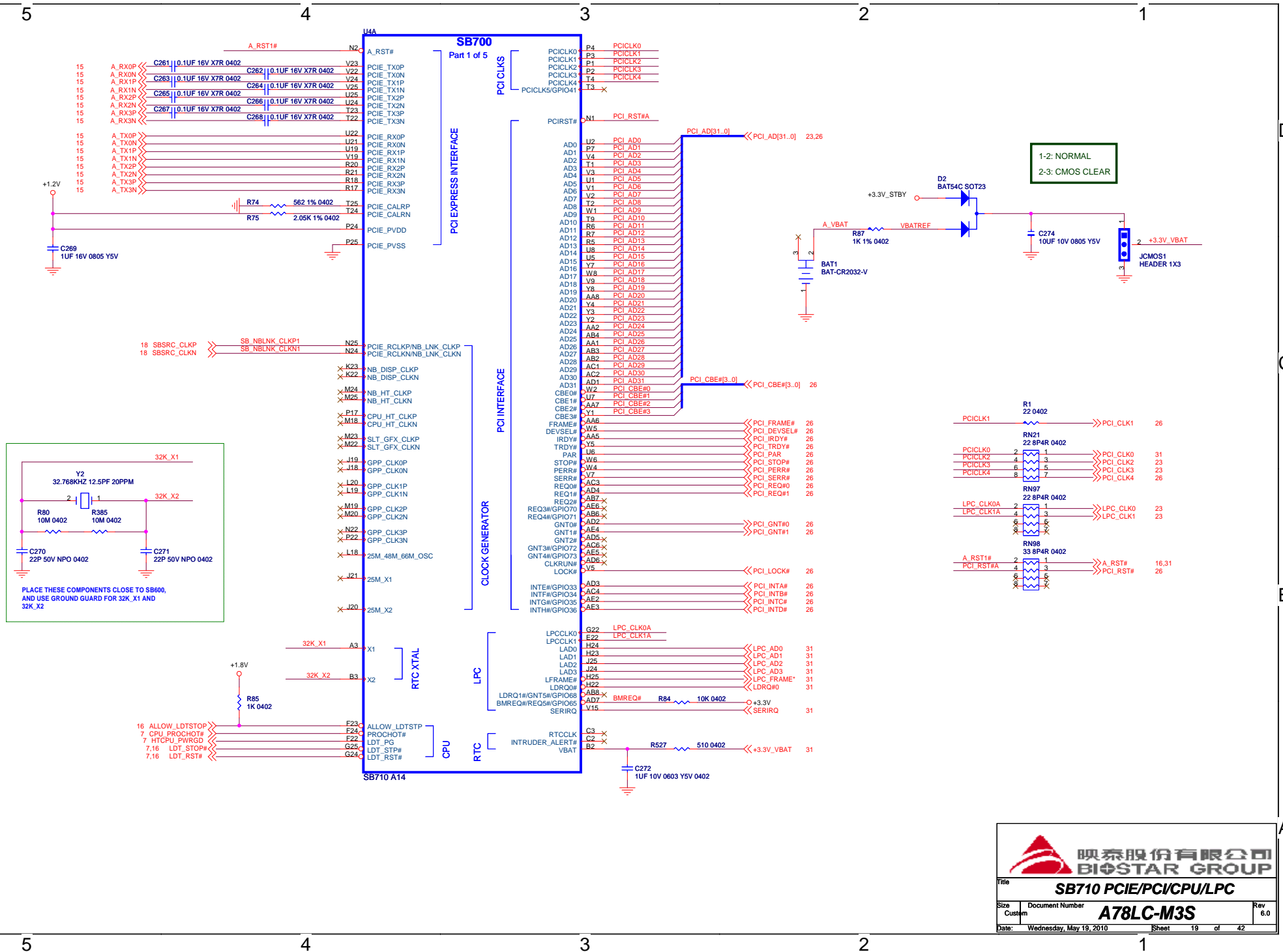
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

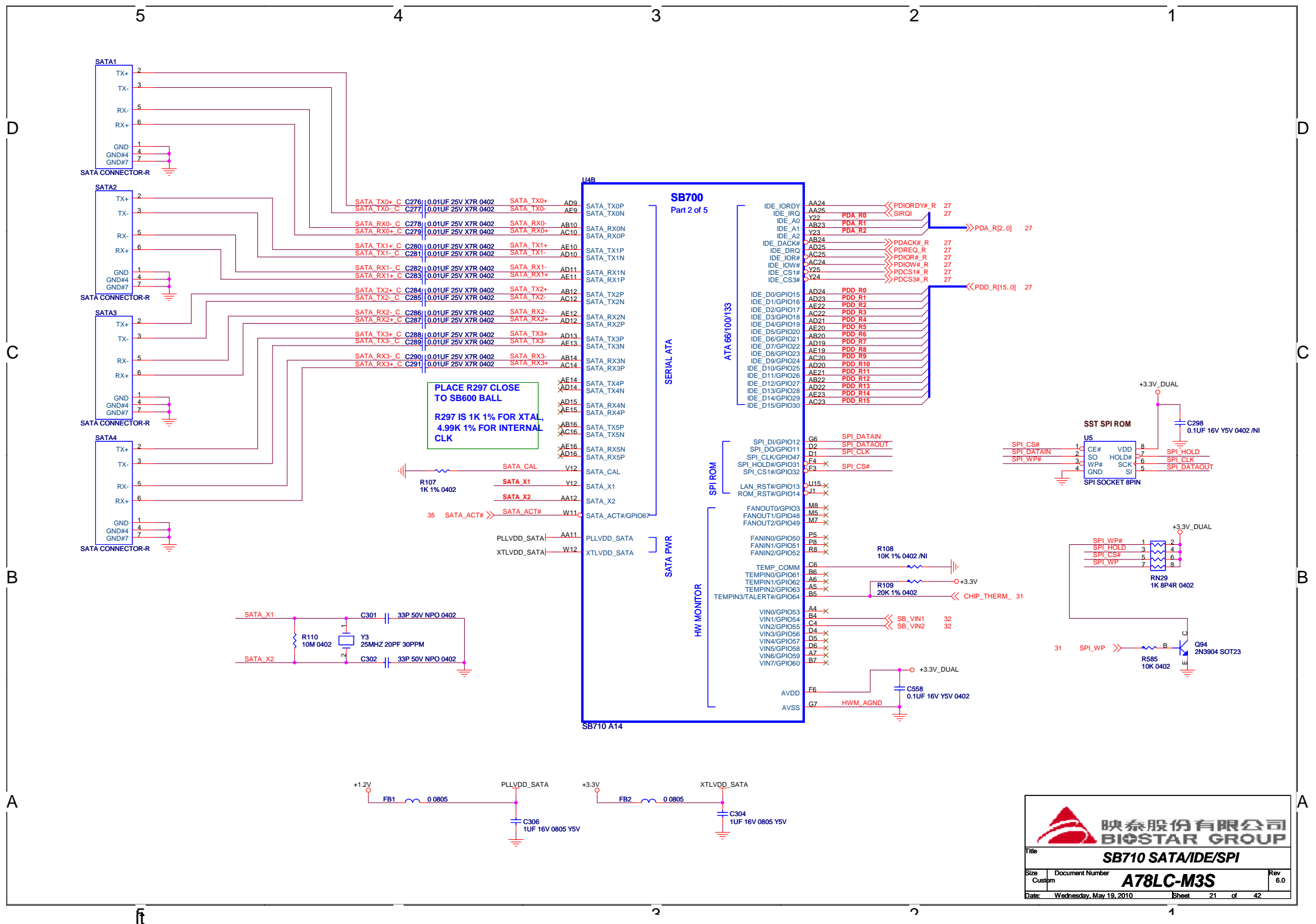


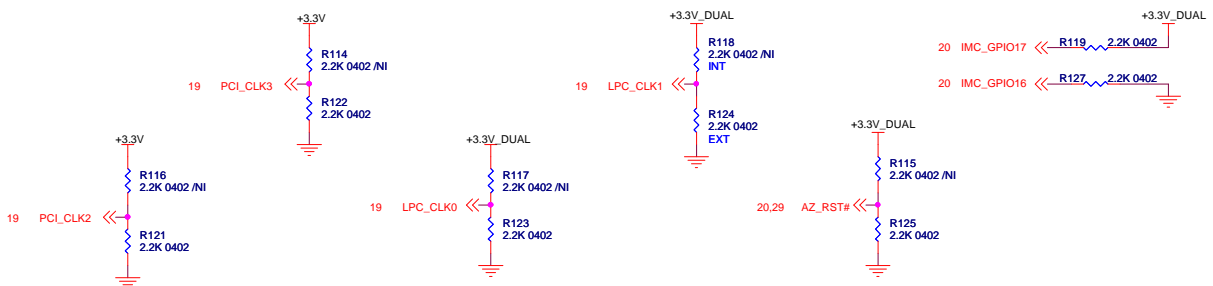


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Title		
CLOCK GEN		
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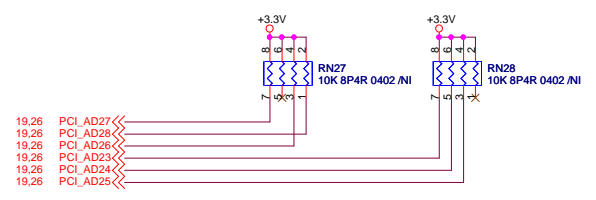
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM	DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT		



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



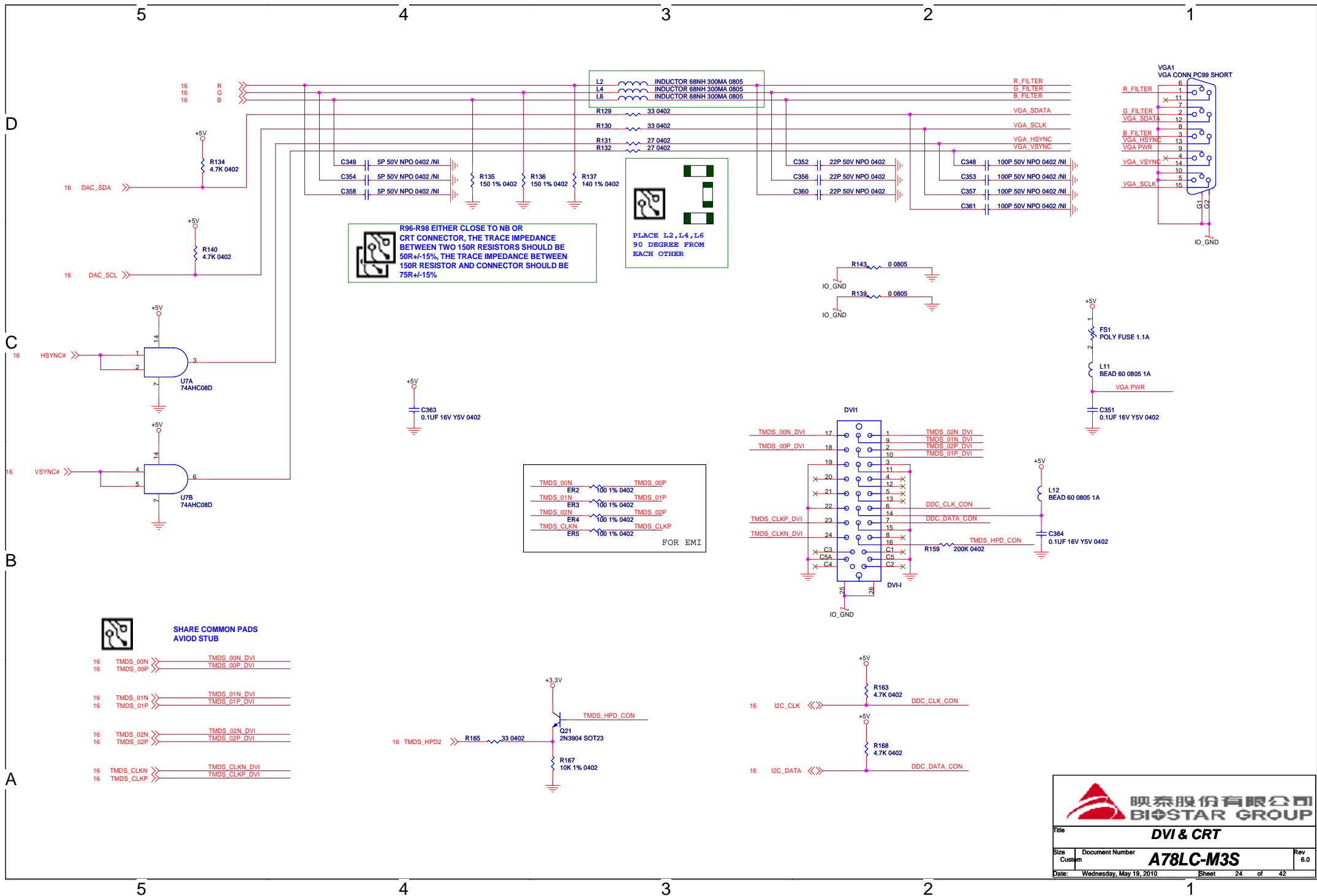
DEBUG STRAPS

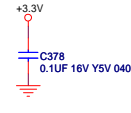
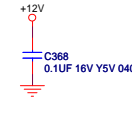
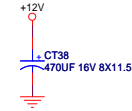
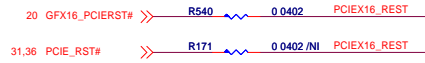
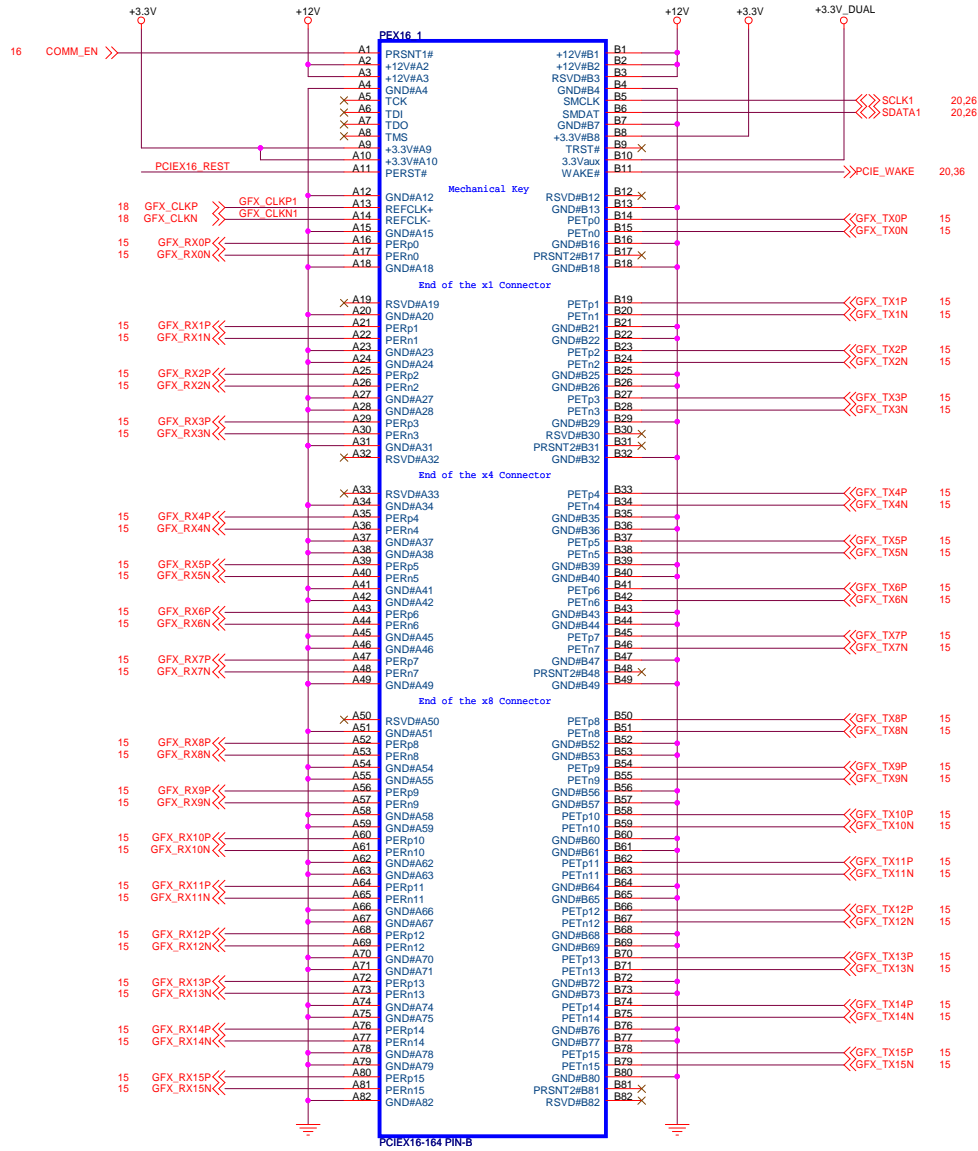
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

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Title SB710 STRAP		
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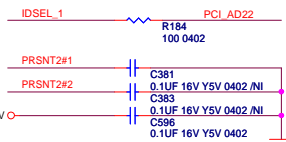
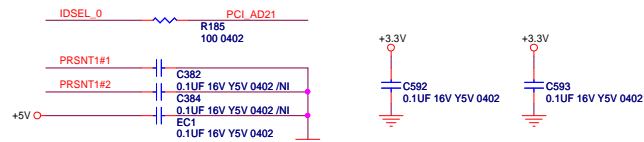
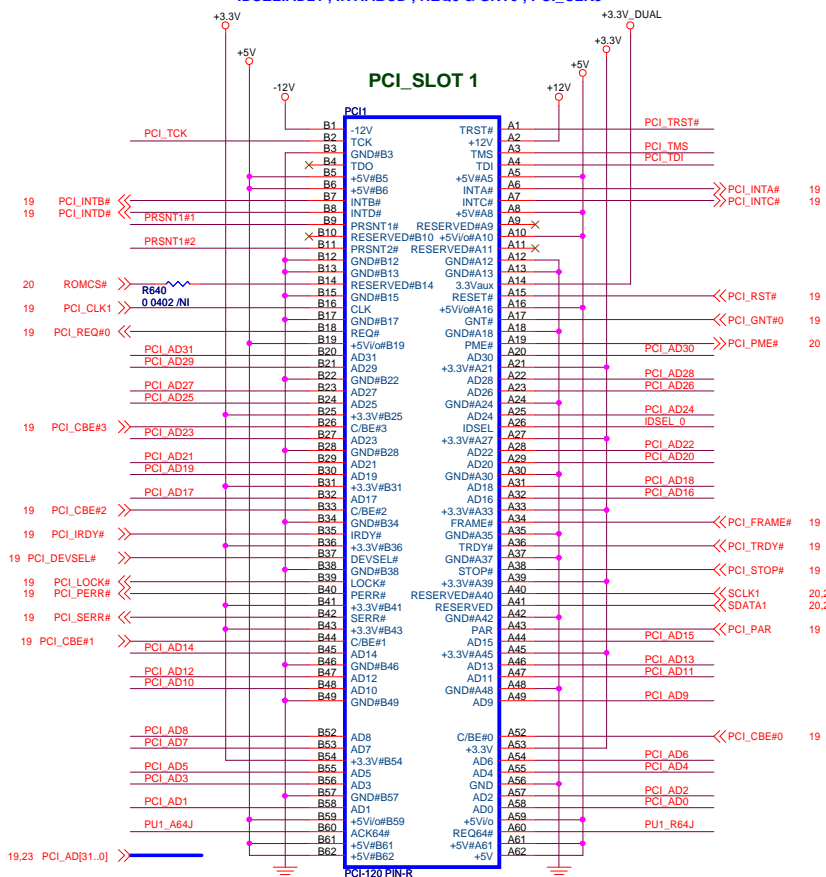


File: **PCI-E SLOT**

Size: Custom	Document Number: A78LC-M3S	Rev: 6.0
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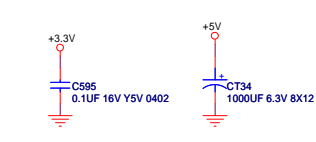
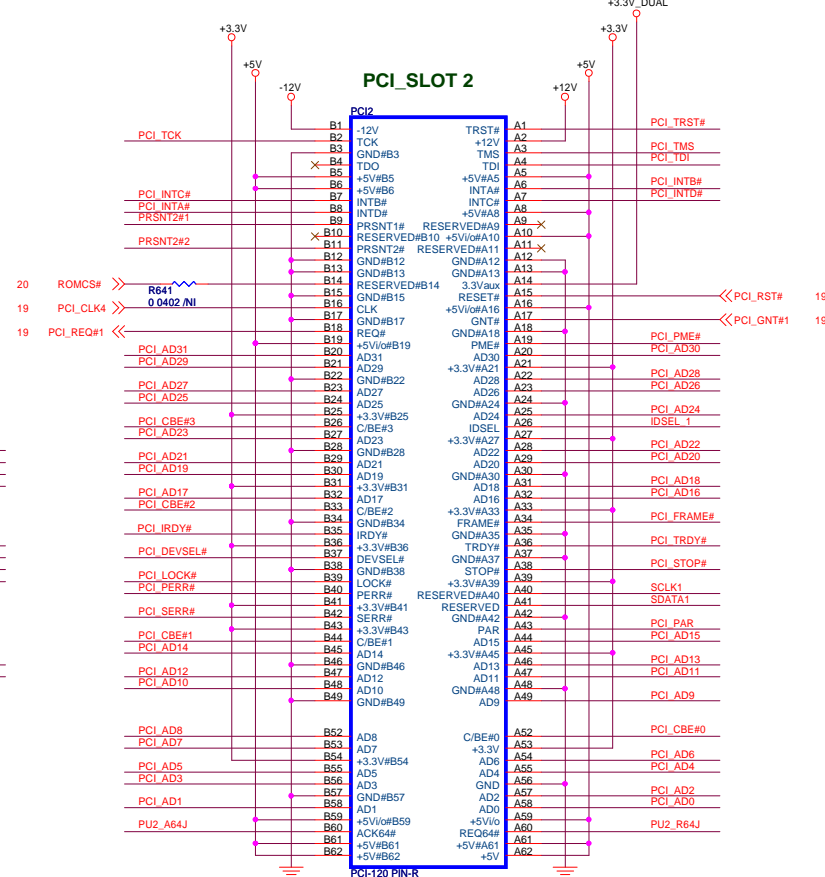
IDSEL:AD21, INT:ABCD, REQ0 & GNT0, PCI_CLK3


PCI_SLOT 1



IDSEL:AD22, INT:BCDA, REQ1 & GNT1, PCI_CLK4

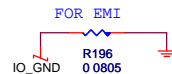
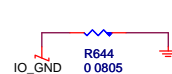
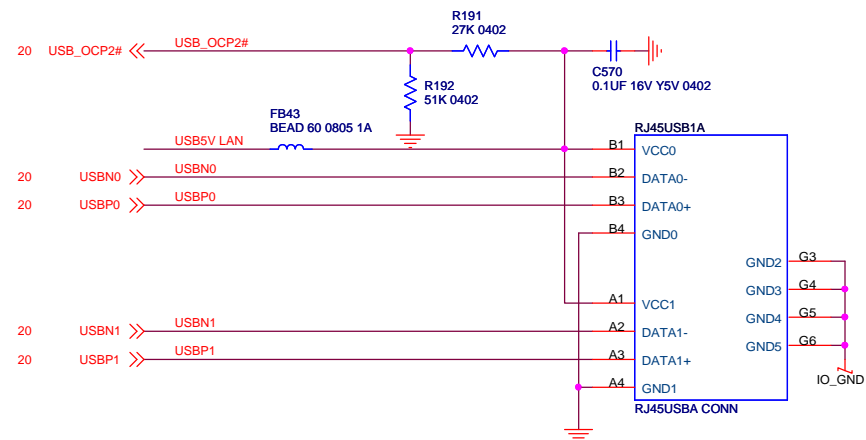
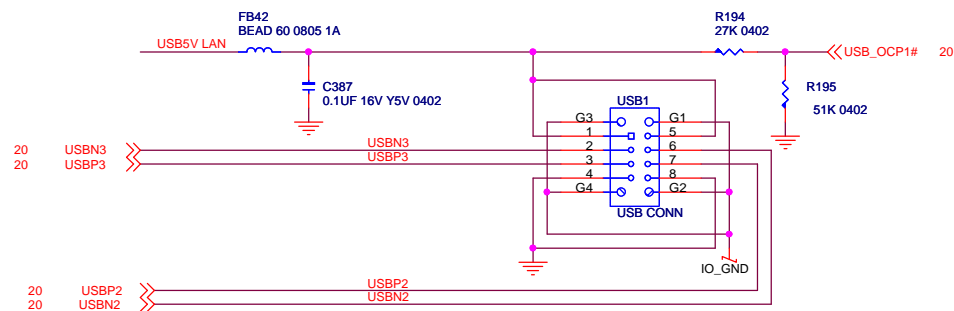
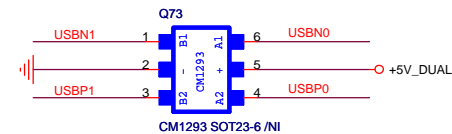
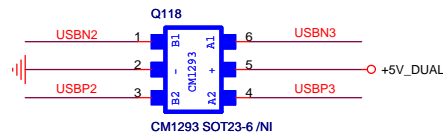
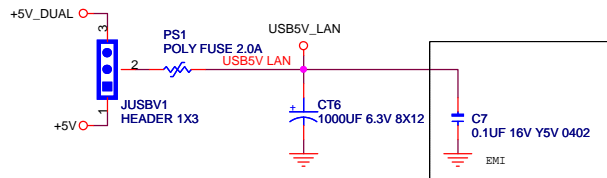
PCI_SLOT 2






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PCI SLOT		
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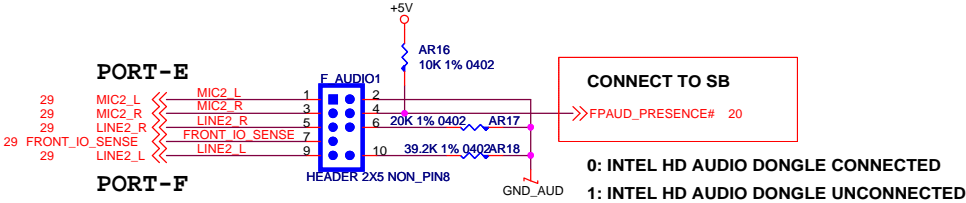
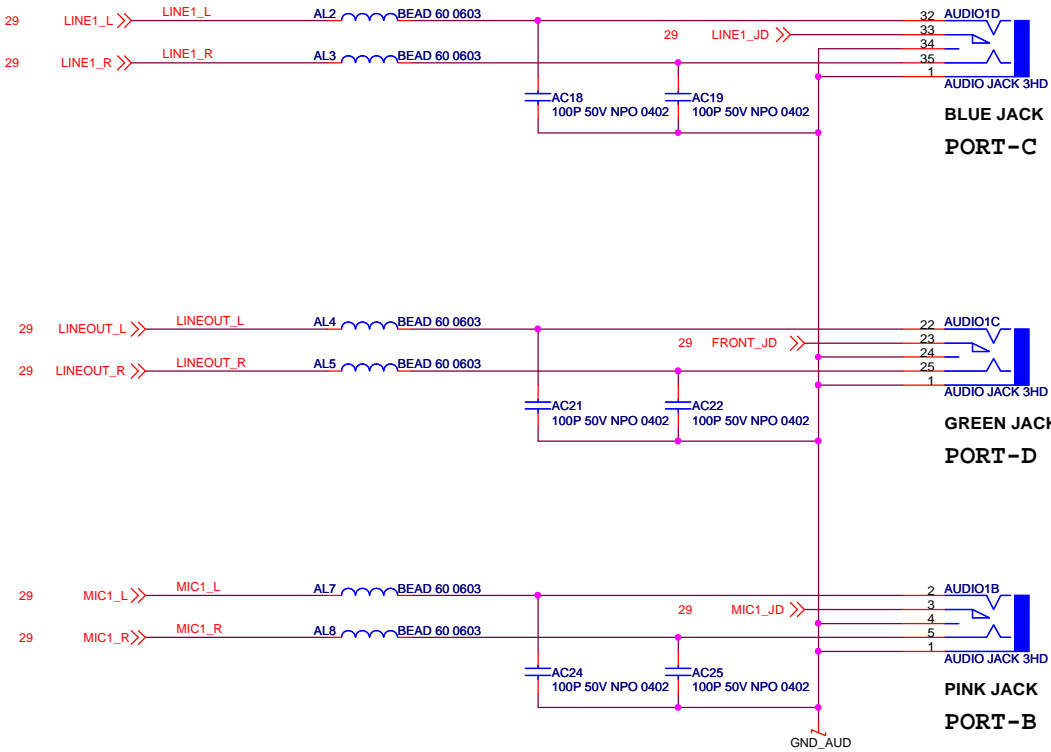




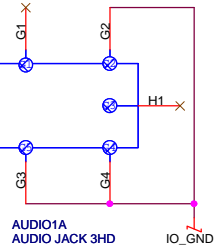
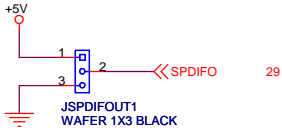
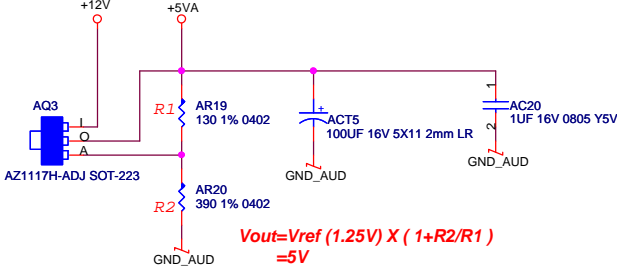
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USB CONN		
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Rear Panel Onboard Analog I/O



AUDIO ANALOG POWER



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BIOSTAR GROUP

Title: **AUDIO CONNECTOR**

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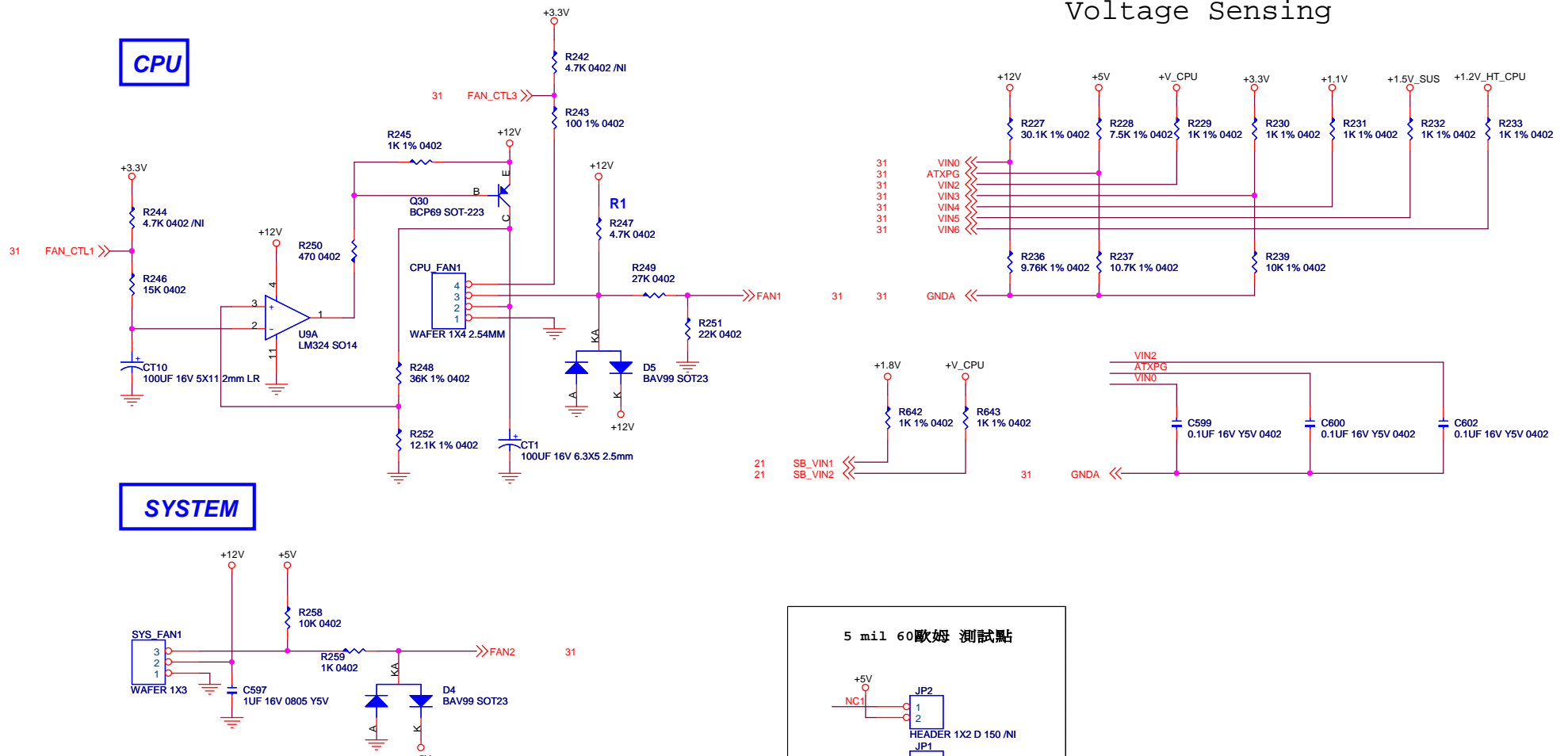
Document Number: **A78LC-M3S**

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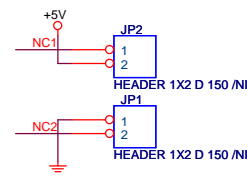
CPU

SYSTEM

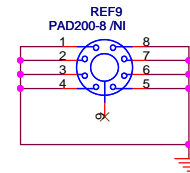
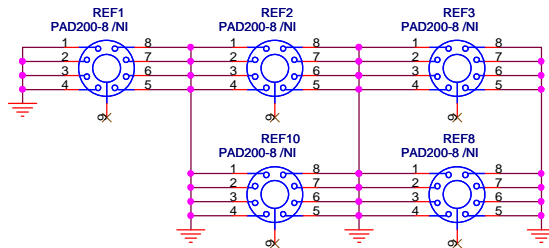
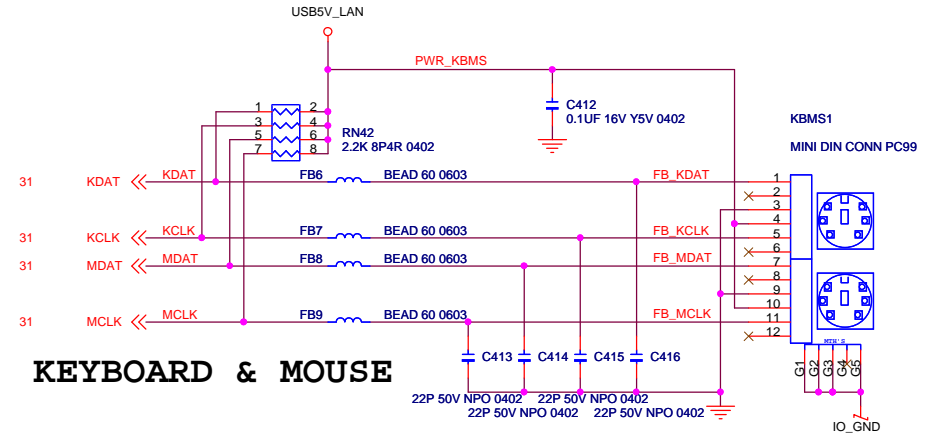
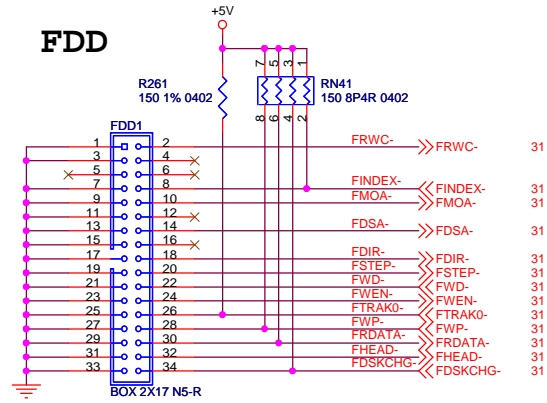
Voltage Sensing



5 mil 60欧姆 测试点

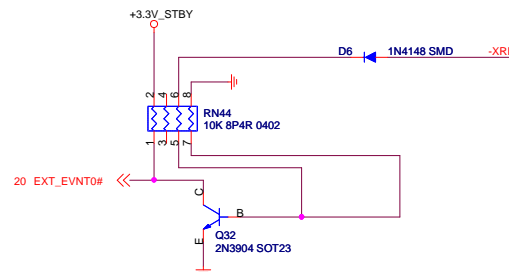
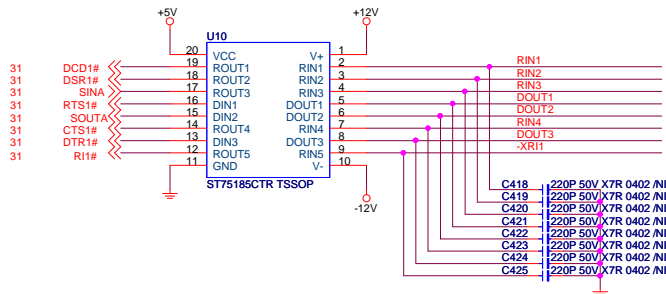


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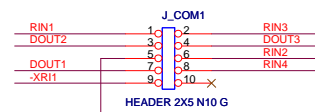


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COM1



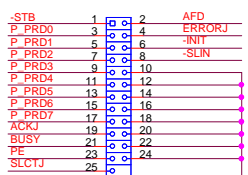
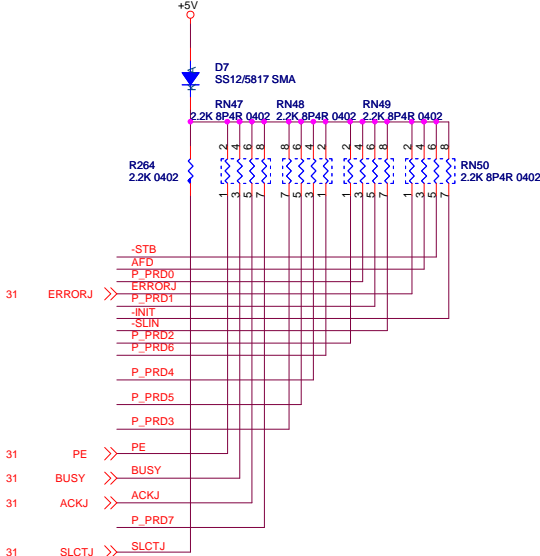
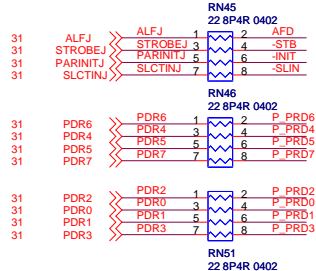
WAKE ON LAN



COM PORT



COM PORT PIN
ASSIGNMENT



J_PRINT1
HEADER 2X13 N26

映泰股份有限公司
BIOSTAR GROUP

Title
COM & PRINTER CONNECTOR

Size
Custom

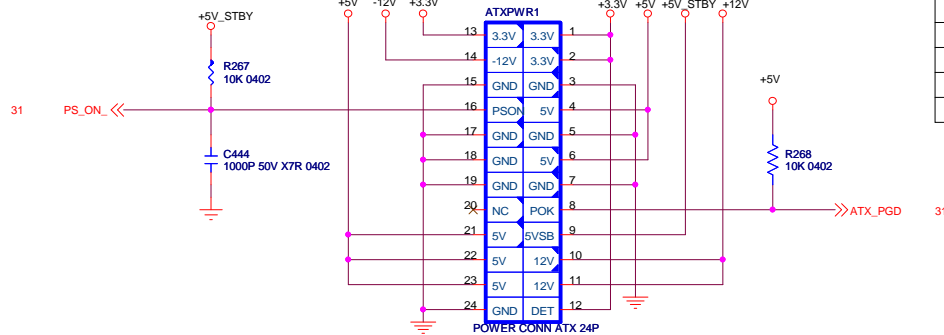
Document Number
A78LC-M3S

Date
Wednesday, May 19, 2010

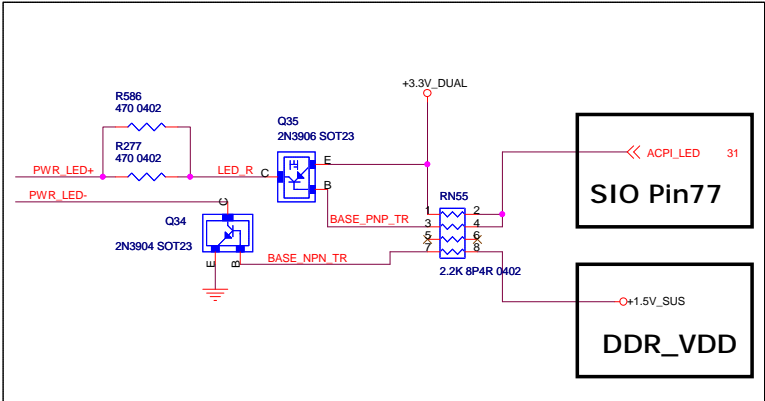
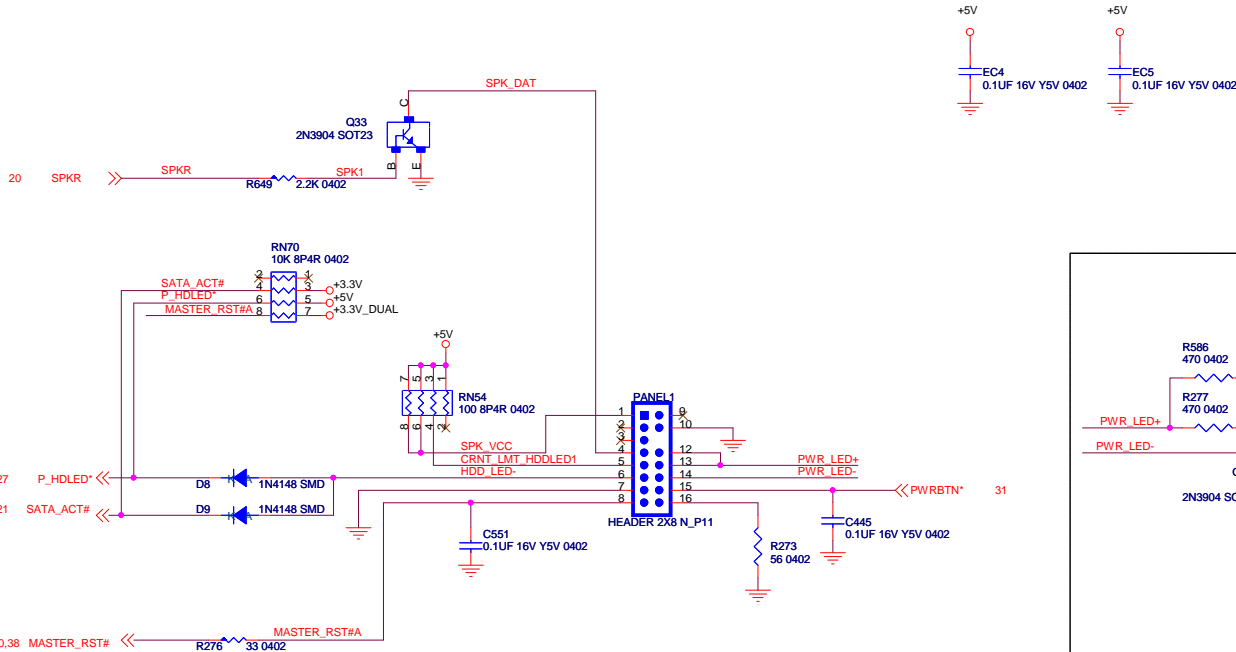
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6.0


5 4 3 2 1



LED_D2	LED_D1	MESSAGE
OFF	OFF	ABNORMAL
OFF	ON	MEMORY ERROR
ON	OFF	VGA ERROR
ON	ON	NORMAL

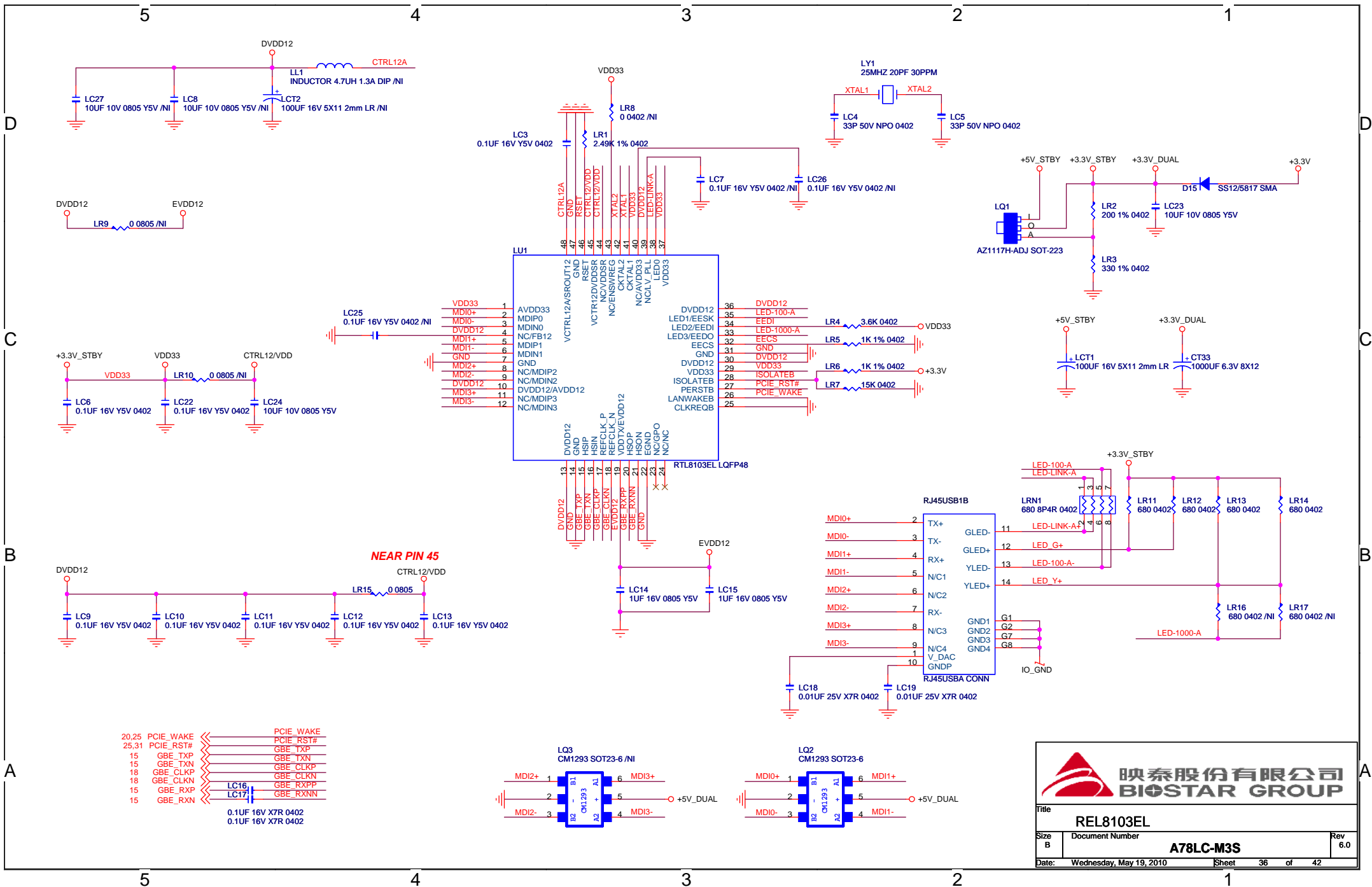


5 4 3 2 1

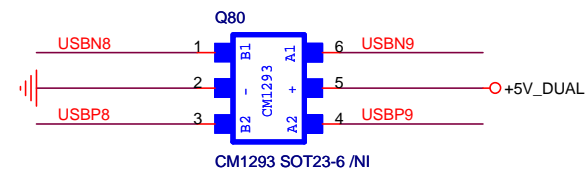
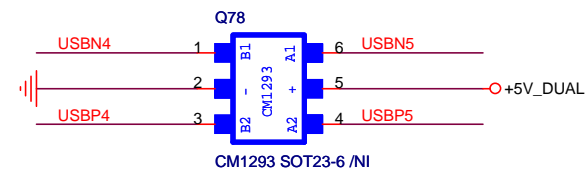
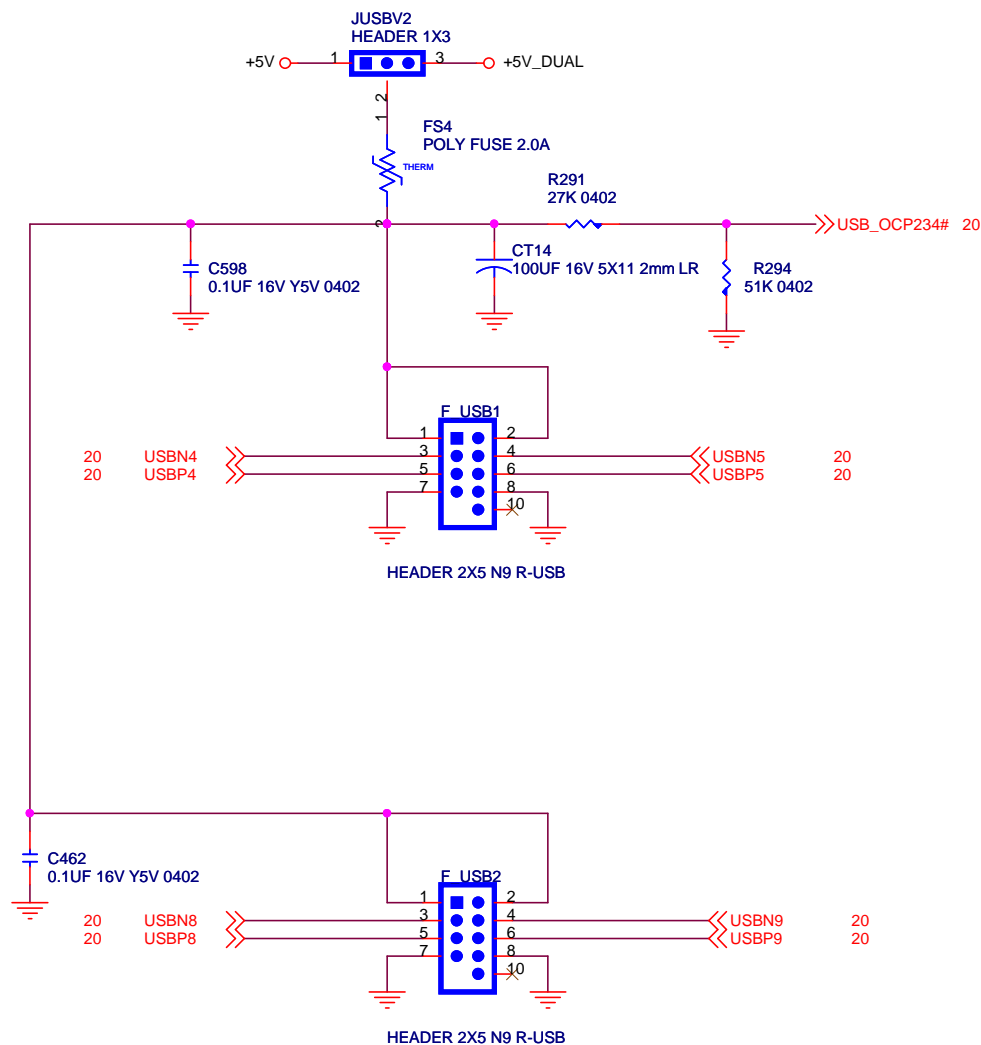



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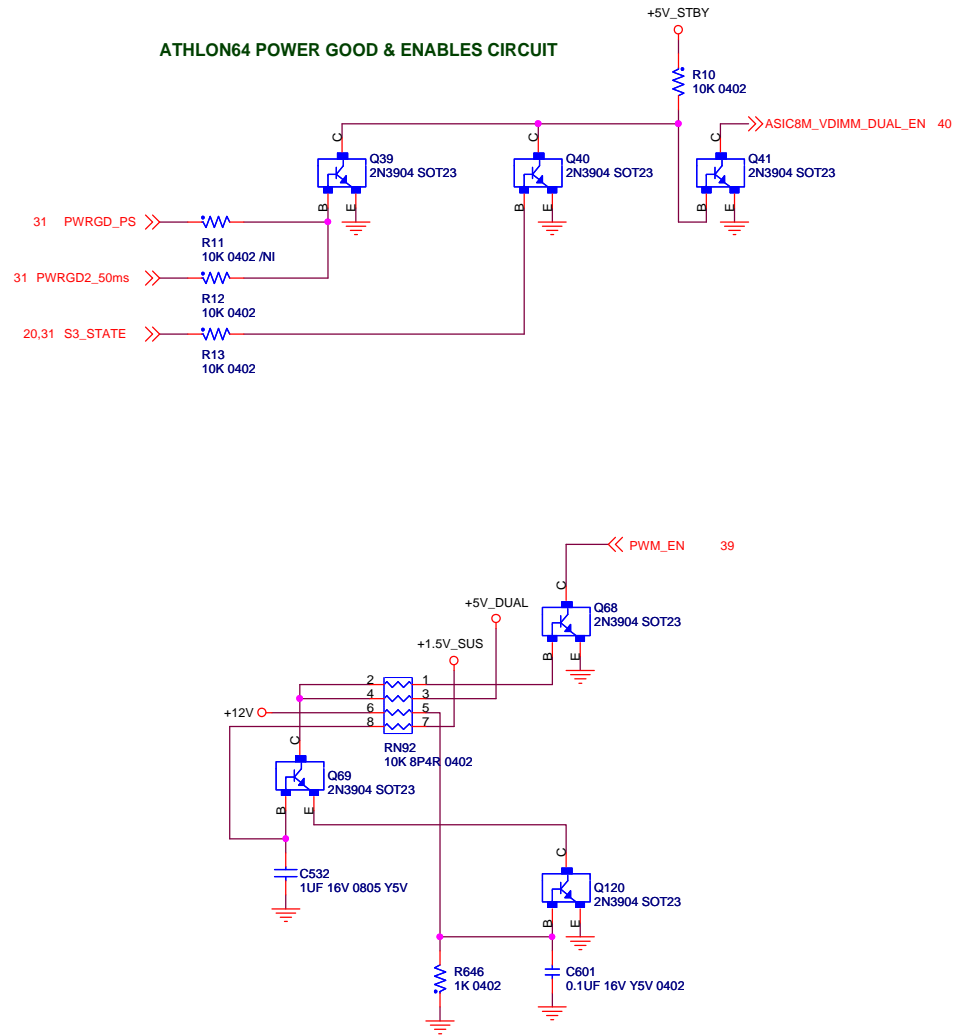


FRONT PANEL USB

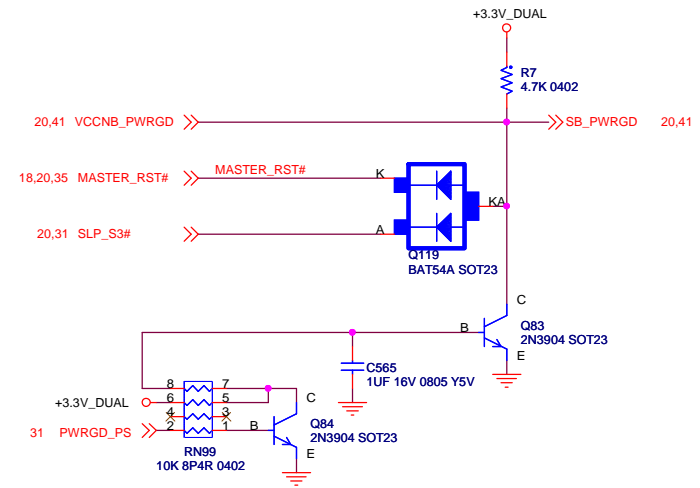


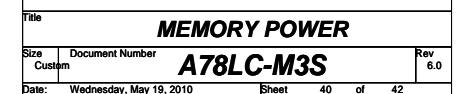
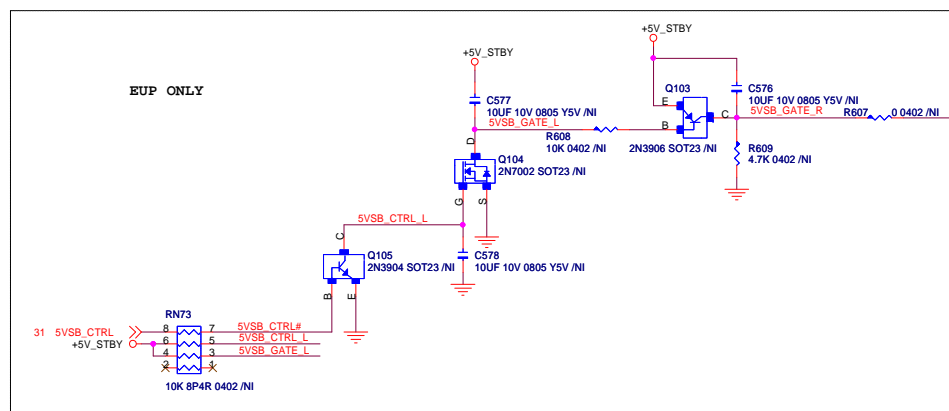
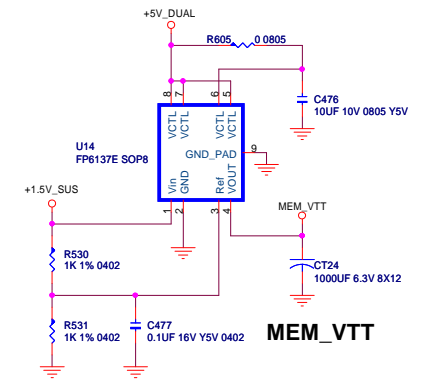
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Title FRONT USB		
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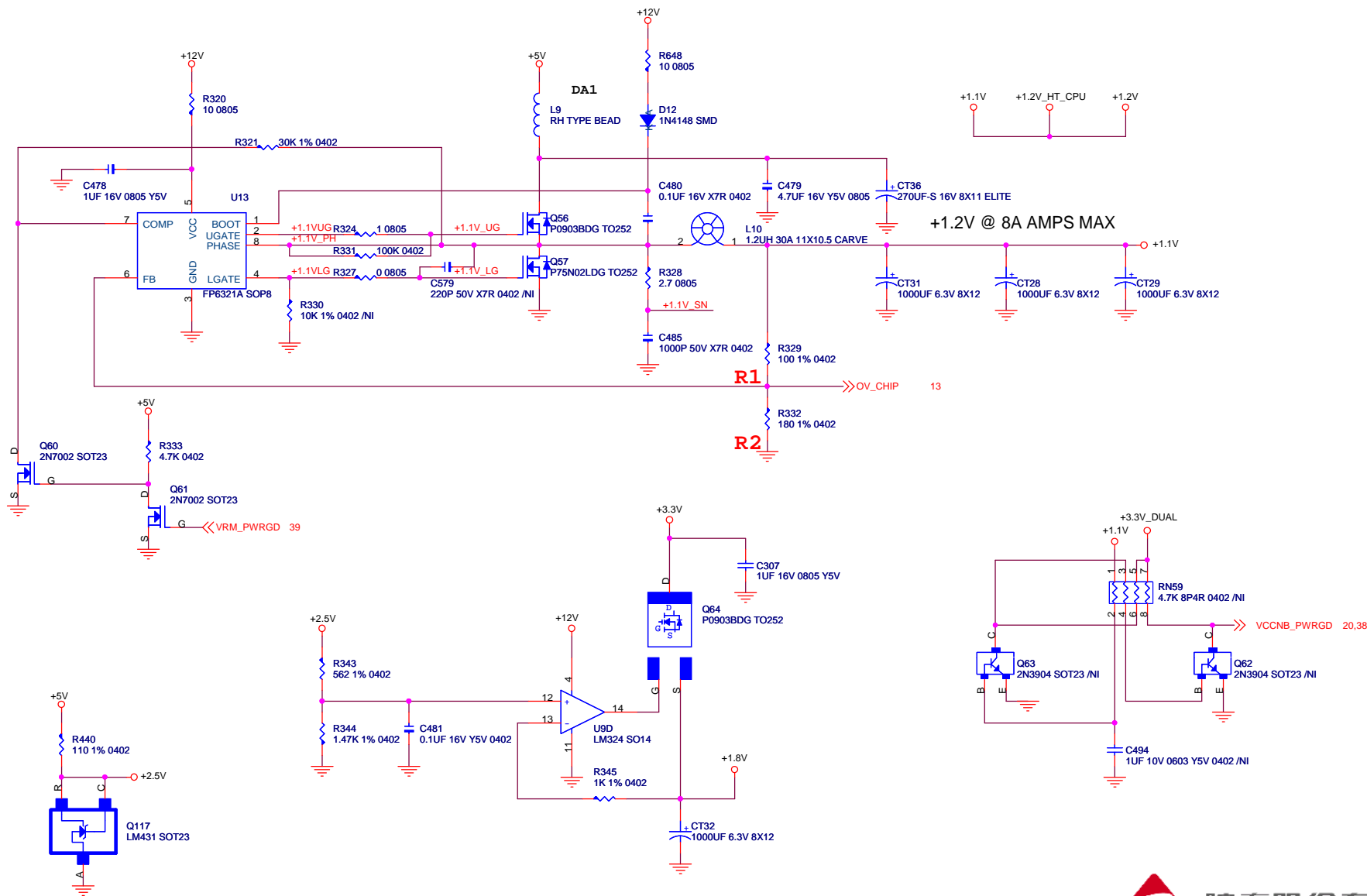
ATHLON64 POWER GOOD & ENABLES CIRCUIT



SB700 POWER GOOD CIRCUIT RS780 POWER GOOD CIRCUIT







Title			NB/SB CORE POWER	
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