PAGE	CONTENTS
1	COVER
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	CLOCK DISTRIBUTION
5	REVISION HISTROY
6-10	SKT 941 K8 AM3 CPU
11	CPU DECOUPLING
12	DDR CLK BYPASS
13	DDR3 DIMM A1
14	DDR3 DIMM B1
15	ADO FUNCTION
16	RS780-HT LINK
17	RS780-PCIE
18	RS780-SYSTEM
19	RS780-PWOER&SBD_MEM
20	CLOCK GEN
21	SB710-PCIE/PCI/CPU/LPC
22	SB710-ACPI/GPIO/USB/AUD
23	SB710-SATA/IDE/HWM/SPI
24	SB710-POWER&DECOUPLING
25	SB710-STRAPS
26	CRT
27	PCI-E 16X SLOT
28	PCI SLOT
29	NONE
30	USB CONN
31	CODEC VT1708B/ALC662
32	AUDIO CONNECTOR
33	SUPER I/O ITE8728
34	FAN CONTROL
35	PS2 CONN
36	COM&LPT CONNECTOR
37	ATX PWR / FRONT PANEL / LED
38	OVER VOLTAGE IC
39	FRONT USB
40	PWRGD / MISC DC-DC
41	VCC_CORE DC-DC CONVER
42	MEMORY POWER
43	NB/SB CORE POWER
44	Realtek RTL8105T
45	BOM

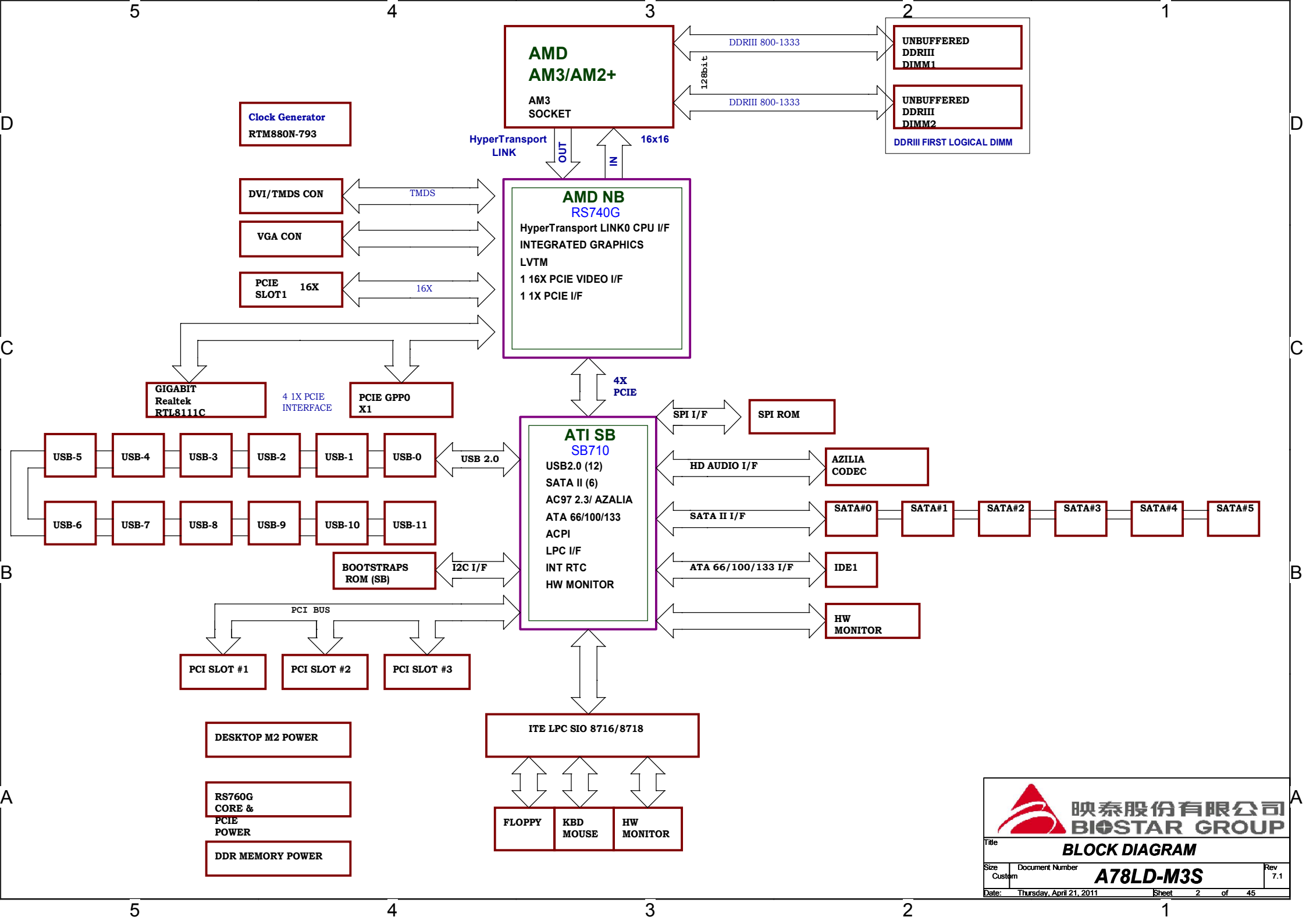
A78LD-M3S (RS780&SB710)

REV 7.1

DDR3 X 2 Dual channel , PCI-Ex16 X 1 , PCI X 1 ,
Realtek 10/100 PCI-E Lan , AMD AM3

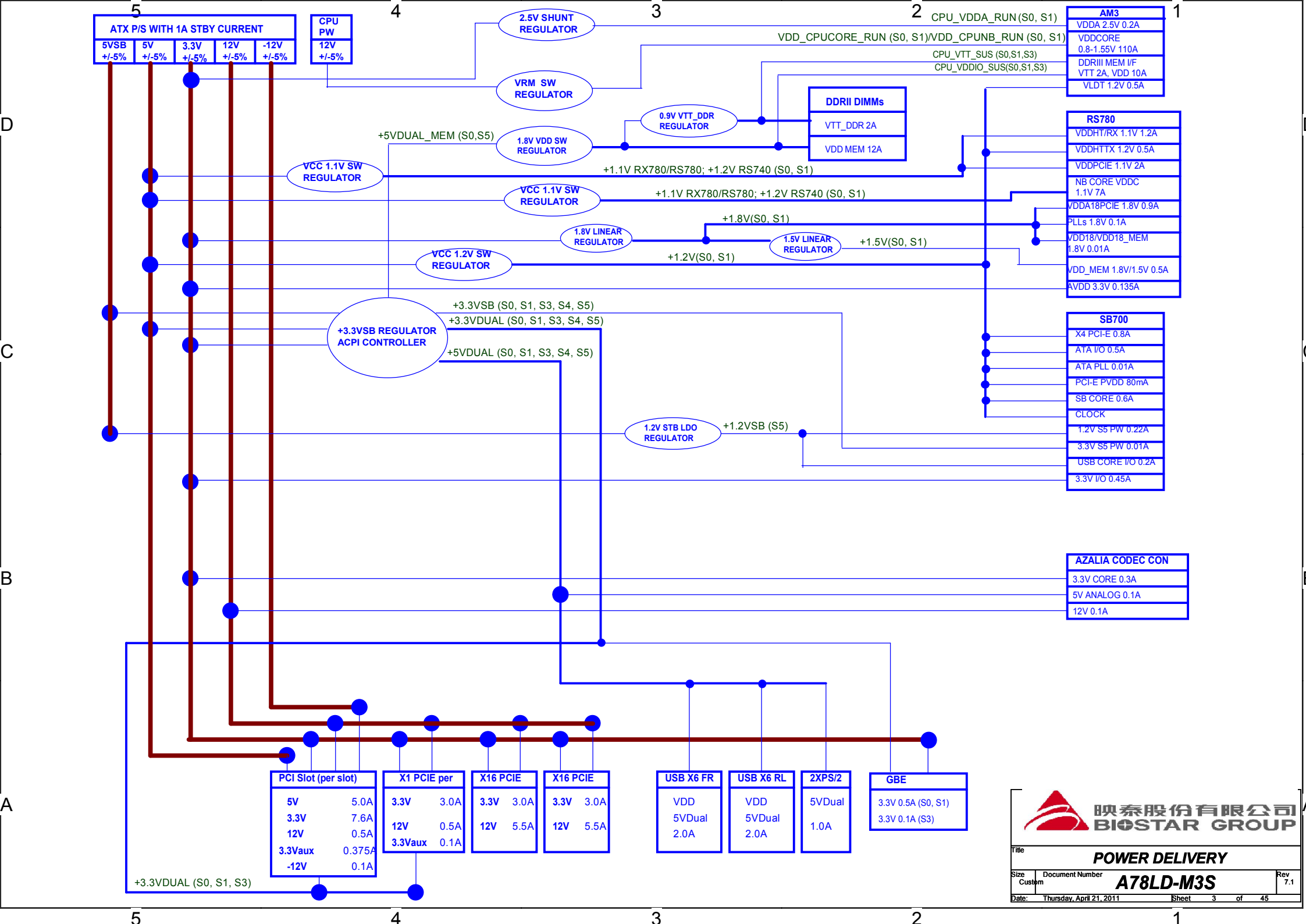
映泰股份有限公司
BIOSTAR GROUP

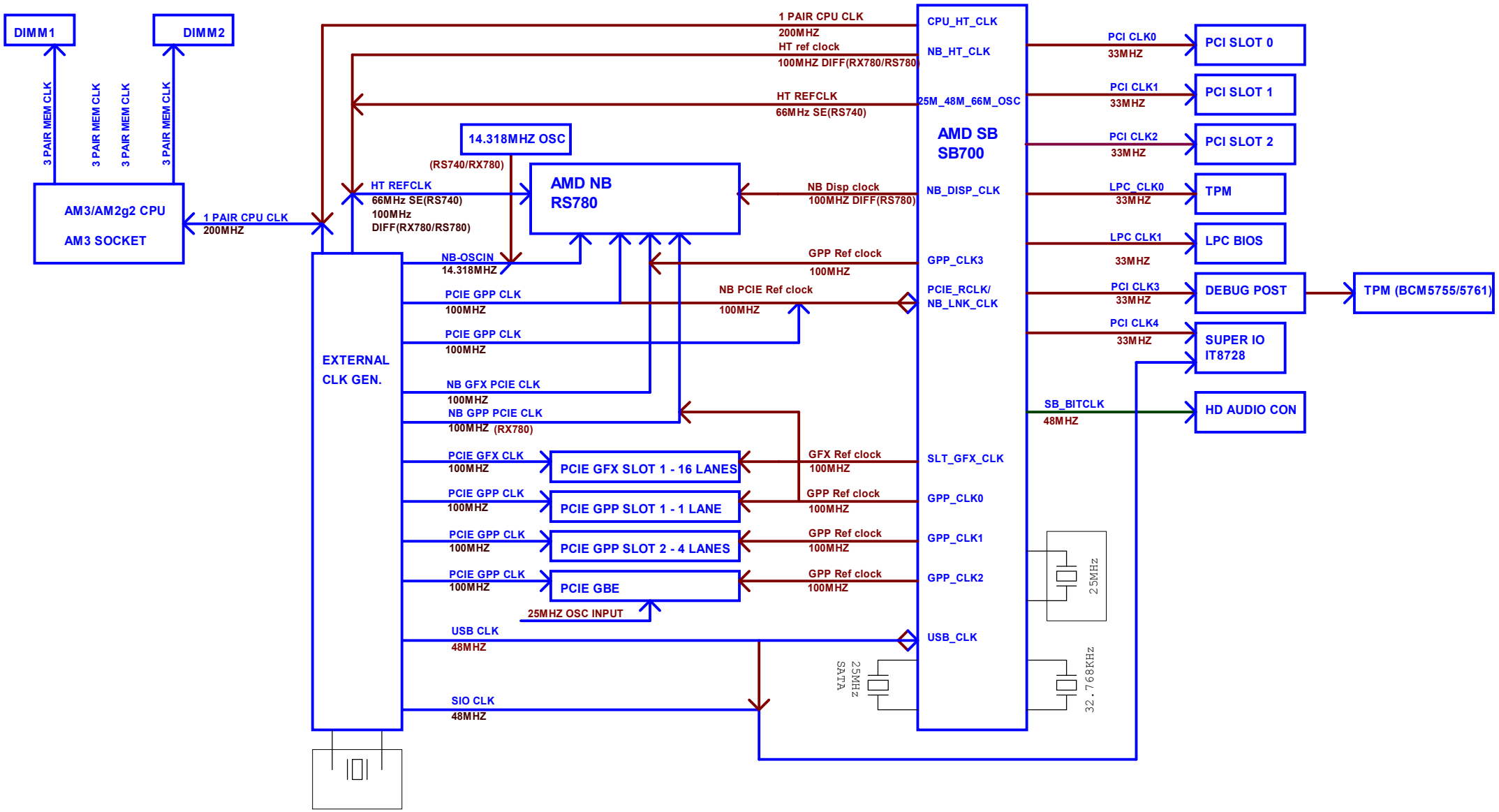
Title	COVER	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 1 of 45	



映泰股份有限公司
BIOSTAR GROUP

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 2 of 45	


ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
CPU PW
12V +/-5%
2.5V SHUNT REGULATOR
CPU_VDDA_RUN (S0, S1)
AM3
VDDA 2.5V 0.2A
VDDCORE 0.8-1.55V 110A
DDRIII MEM I/F VTT 2A, VDD 10A
VLDT 1.2V 0.5A
VDD_CPUCORE_RUN (S0, S1)/VDD_CPUNB_RUN (S0, S1)
CPU_VTT_SUS (S0,S1,S3)
CPU_VDDIO_SUS(S0,S1,S3)
VRM SW REGULATOR
0.9V VTT_DDR REGULATOR
DDRII DIMMs
VTT_DDR 2A
VDD MEM 12A
+5VDUAL_MEM (S0,S5)
1.8V VDD SW REGULATOR
RS780
VDDHT/RX 1.1V 1.2A
VDDHTTX 1.2V 0.5A
VDDPCIE 1.1V 2A
NB CORE VDDC 1.1V 7A
VDDA18PCIE 1.8V 0.9A
PLLs 1.8V 0.1A
VDD18/VDD18_MEM 1.8V 0.01A
VDD_MEM 1.8V/1.5V 0.5A
AVDD 3.3V 0.135A
VCC 1.1V SW REGULATOR
+1.1V RX780/RS780; +1.2V RS740 (S0, S1)
VCC 1.1V SW REGULATOR
+1.1V RX780/RS780; +1.2V RS740 (S0, S1)
+1.8V(S0, S1)
1.8V LINEAR REGULATOR
1.5V LINEAR REGULATOR
+1.5V(S0, S1)
VCC 1.2V SW REGULATOR
+1.2V(S0, S1)
+3.3VSB (S0, S1, S3, S4, S5)
+3.3VDUAL (S0, S1, S3, S4, S5)
+3.3VSB REGULATOR ACPI CONTROLLER
+5VDUAL (S0, S1, S3, S4, S5)
SB700
X4 PCI-E 0.8A
ATA I/O 0.5A
ATA PLL 0.01A
PCI-E PVDD 80mA
SB CORE 0.6A
CLOCK
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A
1.2V STB LDO REGULATOR
+1.2VSB (S5)
AZALIA CODEC CON
3.3V CORE 0.3A
5V ANALOG 0.1A
12V 0.1A
PCI Slot (per slot)
5V 5.0A
3.3V 7.6A
12V 0.5A
3.3Vaux 0.375A
-12V 0.1A
X1 PCIE per
3.3V 3.0A
12V 0.5A
3.3Vaux 0.1A
X16 PCIE
3.3V 3.0A
12V 5.5A
X16 PCIE
3.3V 3.0A
12V 5.5A
USB X6 FR
VDD
5VDual
2.0A
USB X6 RL
VDD
5VDual
2.0A
2XPS/2
5VDual
1.0A
GBE
3.3V 0.5A (S0, S1)
3.3V 0.1A (S3)
+3.3VDUAL (S0, S1, S3)
映泰股份有限公司
BIOSTAR GROUP
Title
POWER DELIVERY
Size
Custom
Document Number
A78LD-M3S
Rev
7.1
Date:
Thursday, April 21, 2011
Sheet
3
of
45



映泰股份有限公司
BIOSTAR GROUP

Title: CLOCK DISTRIBUTION

Size	Document Number	Rev
Custom	A78LD-M3S	7.1

Date: Thursday, April 21, 2011 Sheet 4 of 45

1.Change NB to RS780

2.Change SUPER IO to IT8728

3.Change Codec to VT1708B

4.Change Lan Chip to RTL8105T

5.Remove Floppy Connector

6.Remove SPDIF Out Connector

7.Modify BAT Socket

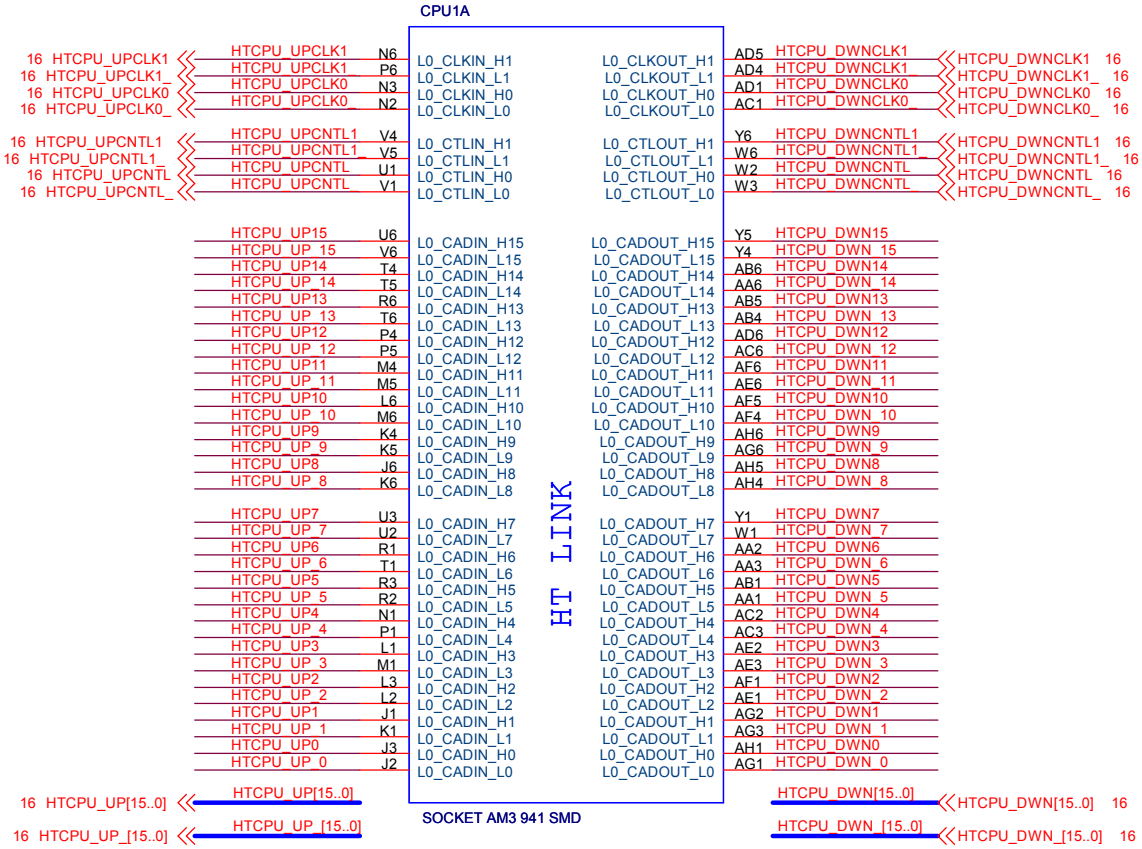
映泰股份有限公司
BIOSTAR GROUP

Title: REVISION HISTORY

Size: Custom | Document Number: A78LD-M3S | Rev: 7.1

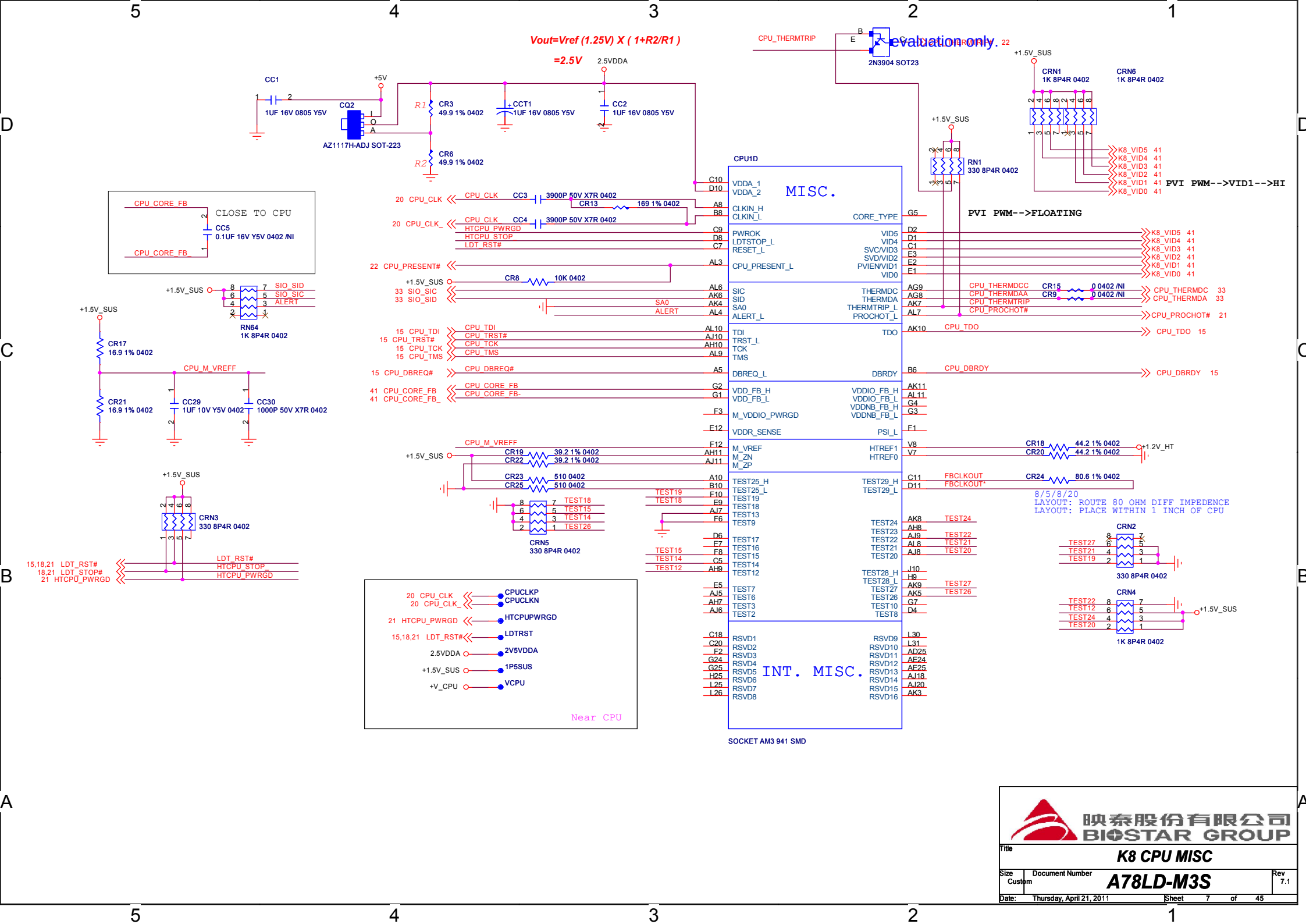
Date: Thursday, April 21, 2011 | Sheet 5 of 45

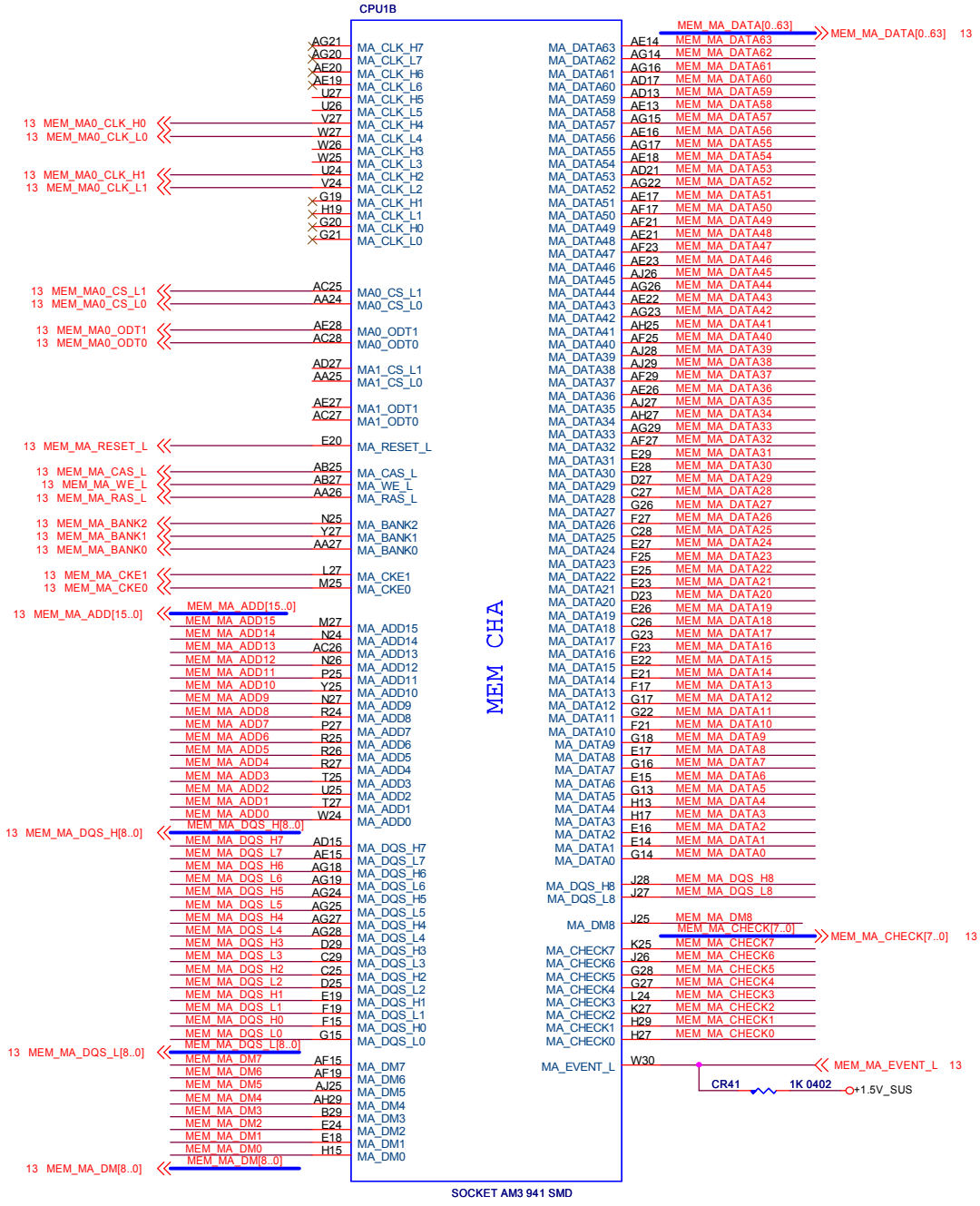
HyperTransport



映泰股份有限公司
BIOSTAR GROUP

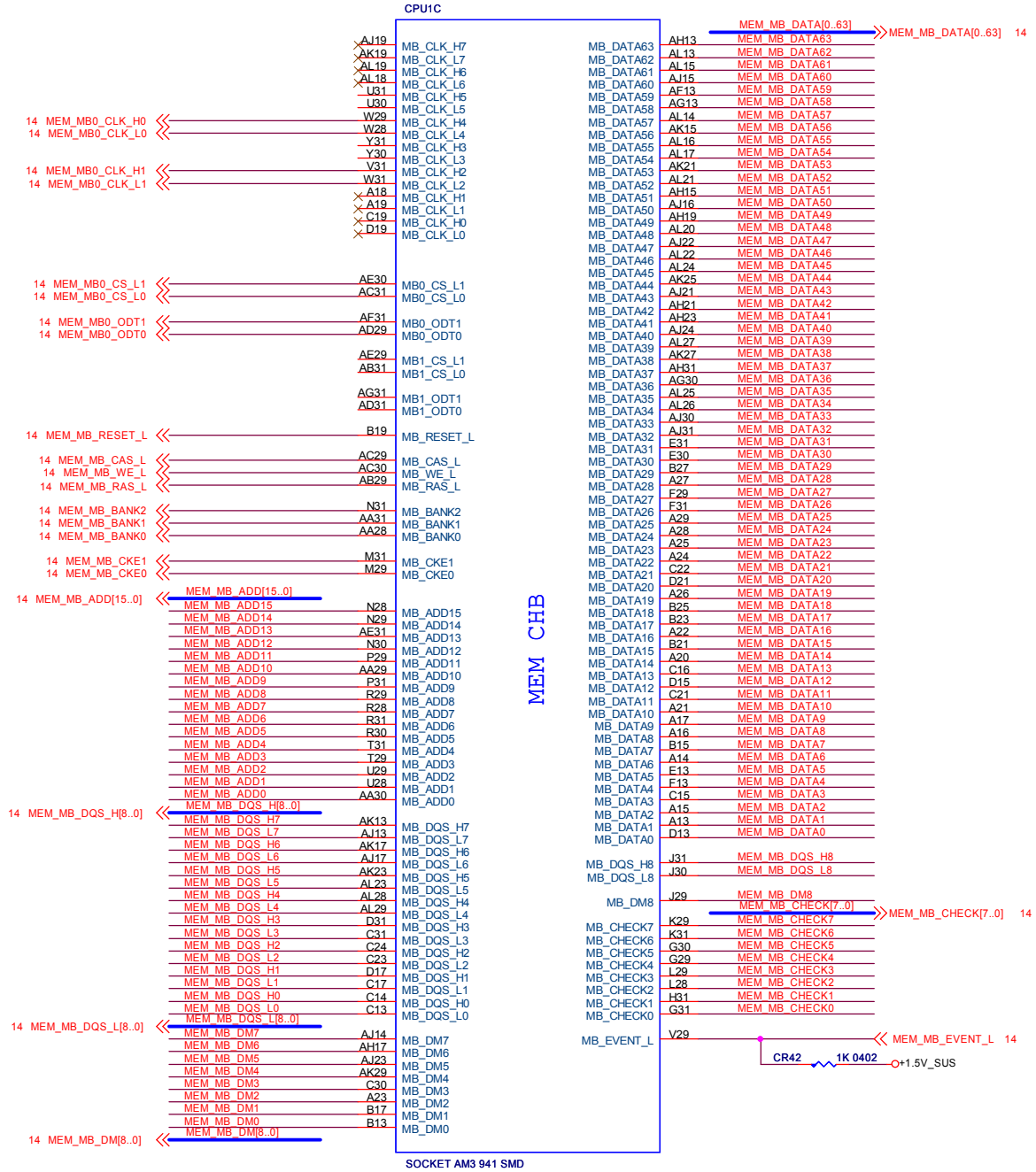
Title	K8 CPU HT	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 6 of 45	


Vout=Vref (1.25V) X (1+R2/R1)
=2.5V
evaluation only.
CPU1D
MISC.
INT. MISC.
SOCKET AM3 941 SMD
CLOSE TO CPU
Near CPU
PVI PWM-->VID1-->HI
PVI PWM-->FLOATING
8/5/8/20
LAYOUT: ROUTE 80 OHM DIFF IMPEDENCE
LAYOUT: PLACE WITHIN 1 INCH OF CPU
AZ1117H-ADJ SOT-223
2N3904 SOT23
RN64
1K 8P4R 0402
CRN5
330 8P4R 0402
CRN3
330 8P4R 0402
CRN1
1K 8P4R 0402
CRN6
1K 8P4R 0402
RN1
330 8P4R 0402
CRN2
330 8P4R 0402
CRN4
1K 8P4R 0402
BIOSTAR GROUP
K8 CPU MISC
A78LD-M3S
Thursday, April 21, 2011



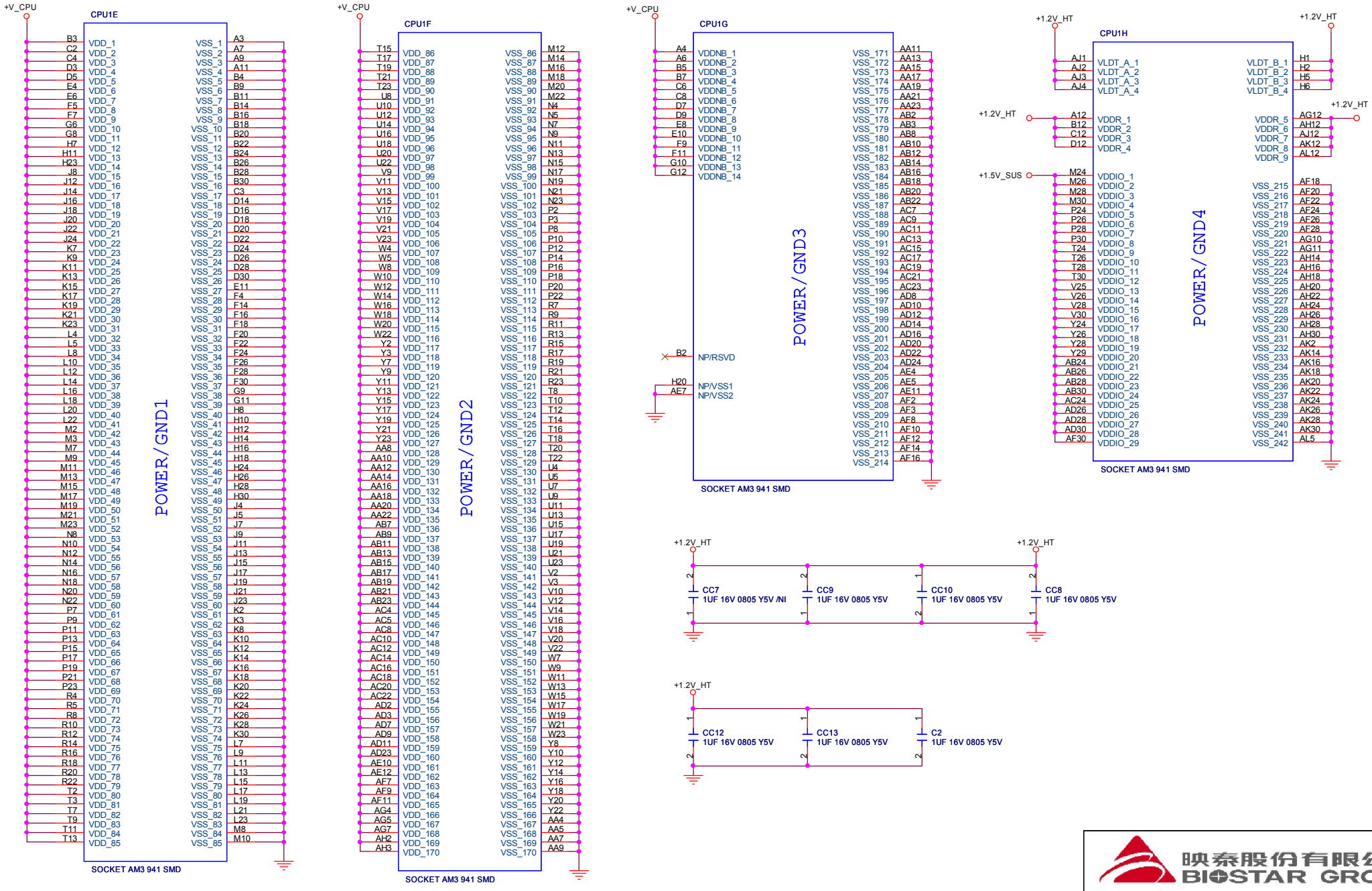
映泰股份有限公司
BIOSTAR GROUP

Title	K8 CPU MEMORY-1	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 8 of 45	



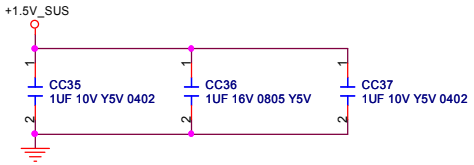
Title	K8 CPU MEMORY-2
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	9 of 45

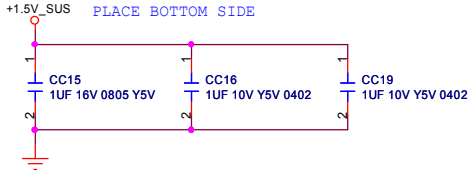
映泰股份有限公司 BIOSTAR GROUP

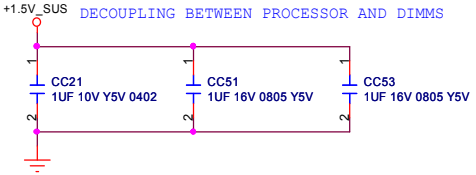


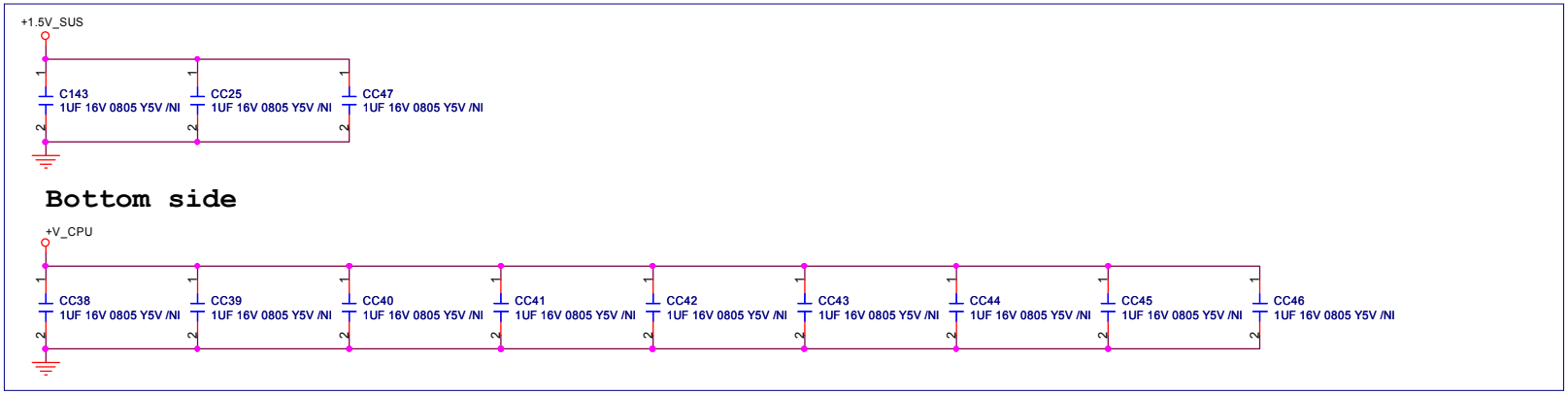
映泰股份有限公司 BIOSTAR GROUP

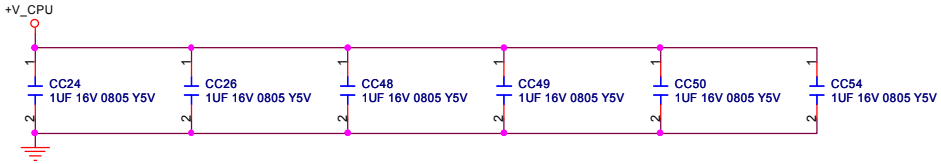
Title	K8 CPU POWER	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 10 of 45	

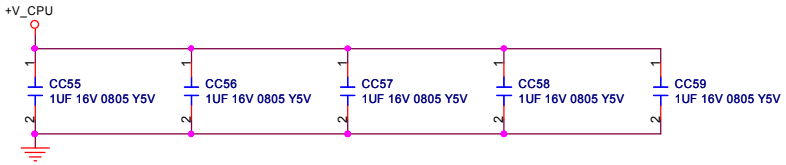












映泰股份有限公司
BIOSTAR GROUP

Title	CPU DECPOULING CAP		
Size: Custom	Document Number: A78LD-M3S		Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 11 of 45		

5 4 3 2 1

D C B A

映泰股份有限公司
BIOSTAR GROUP

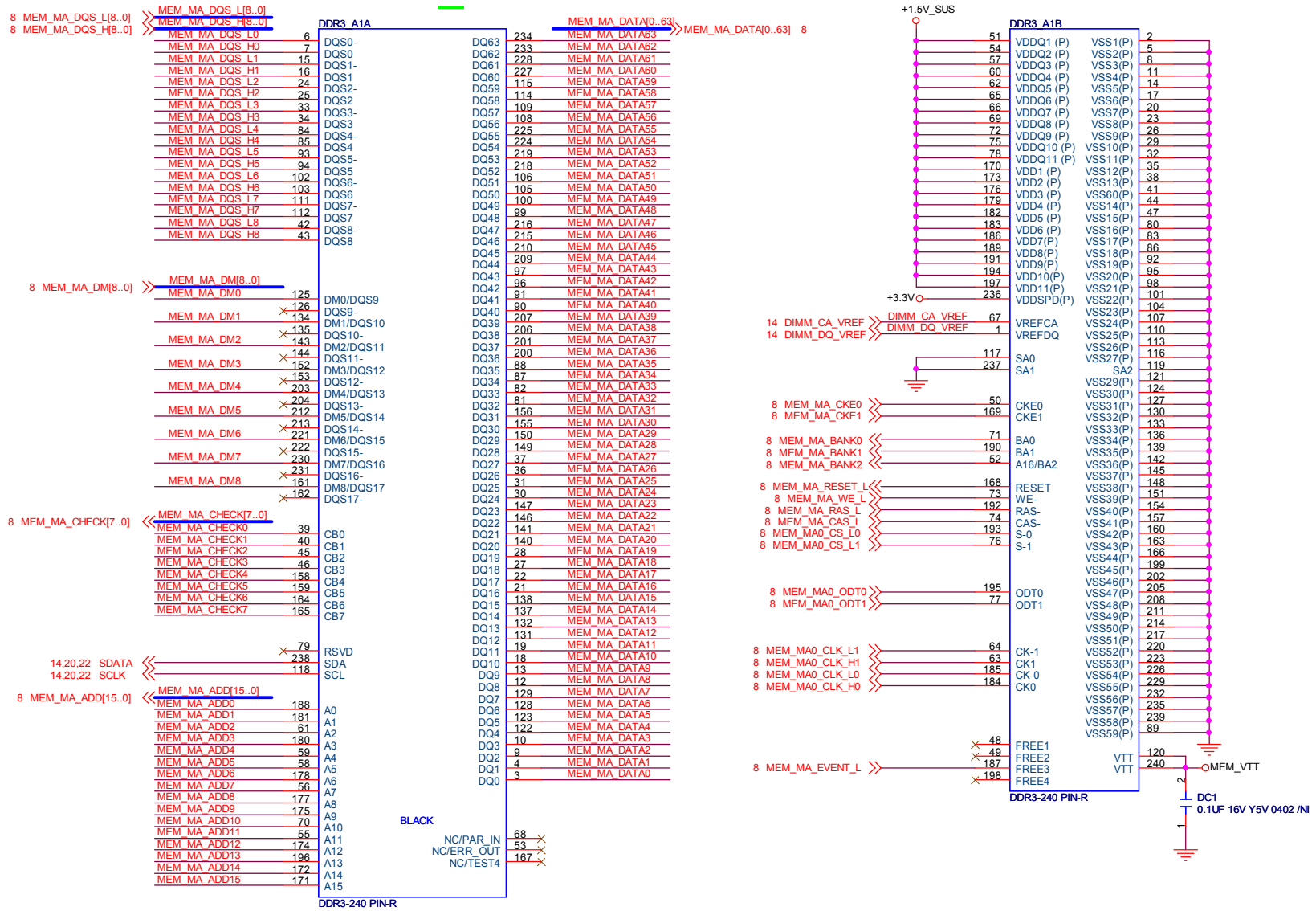
Title: **DDR CAP BYPASS**

Size	Document Number	Rev
Custom	**A78LD-M3S**	7.1

Date: Thursday, April 21, 2011 Sheet 12 of 45

5 4 3 2 1

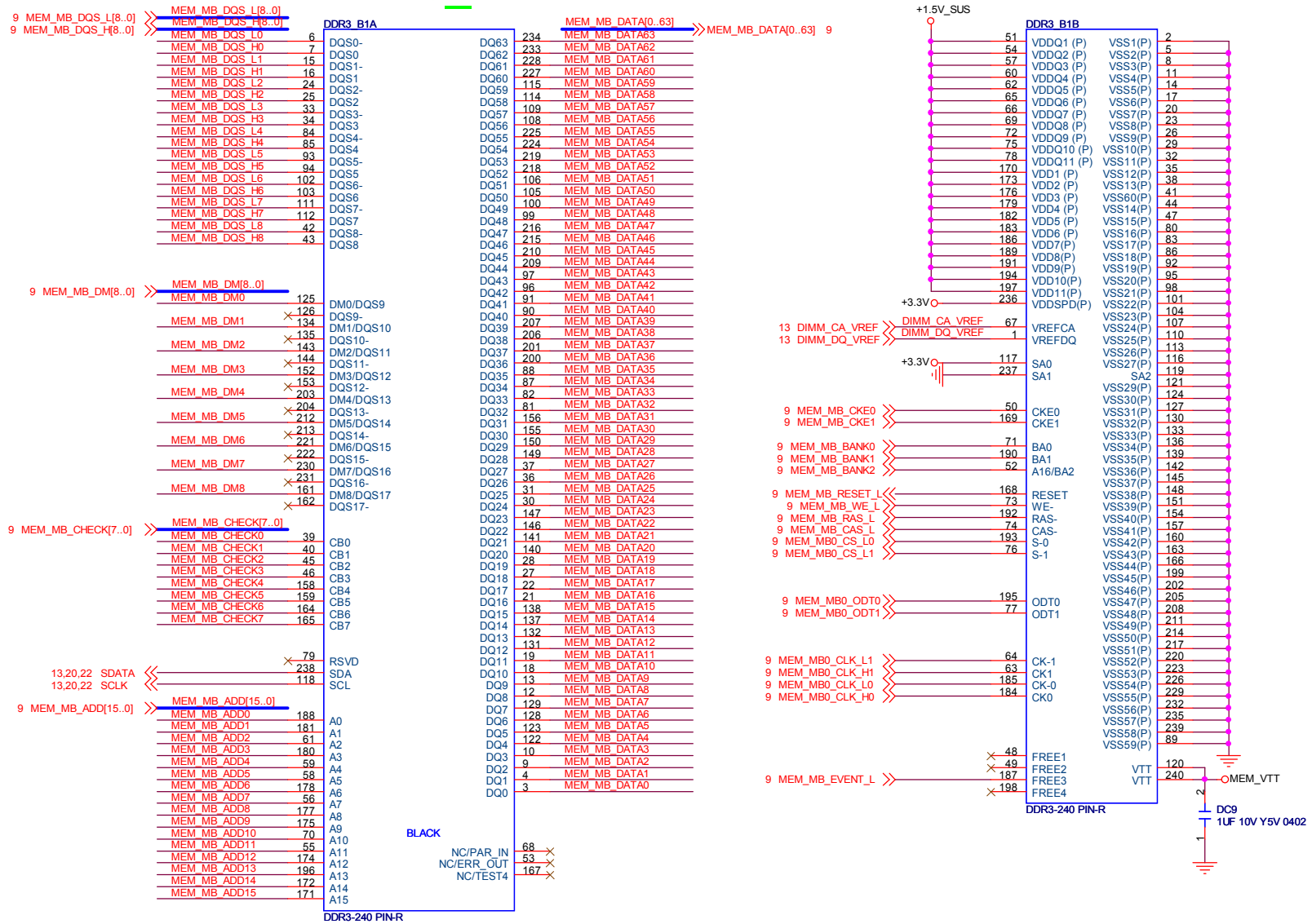
DDR3_A1



映泰股份有限公司
BIOSTAR GROUP

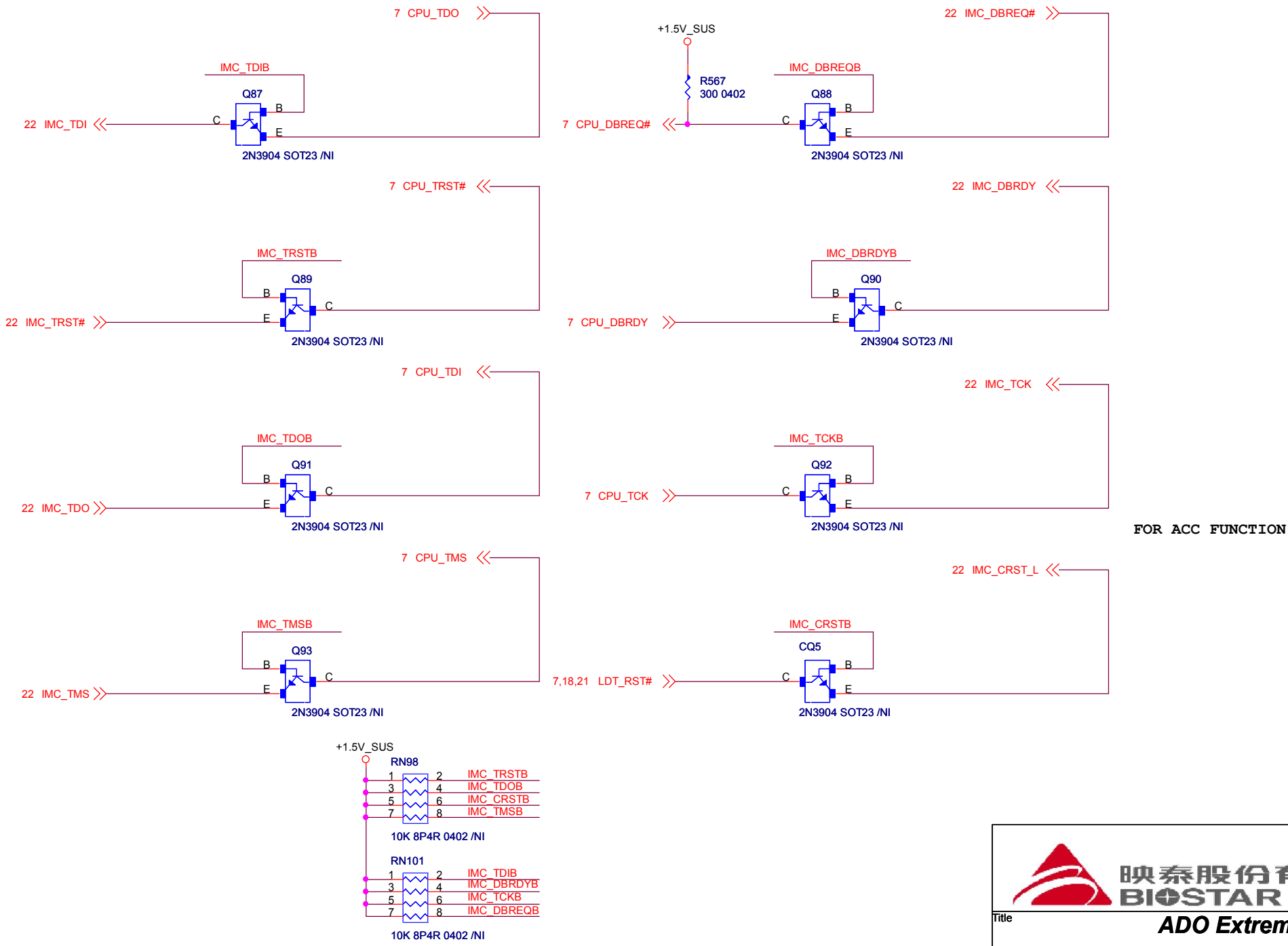
Title	DDR DIMM-1	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 13 of 45	

DDR3_B1



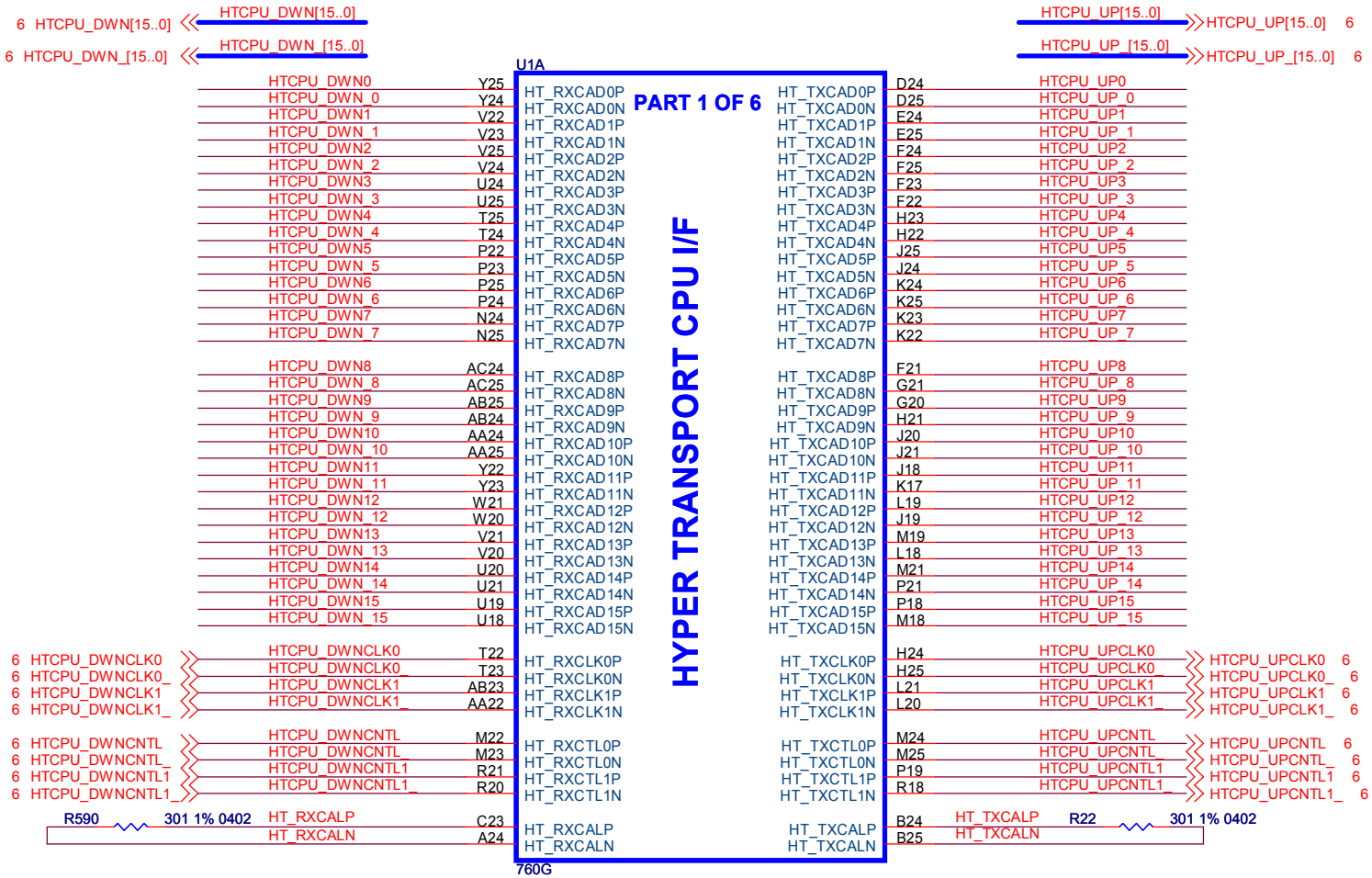
映泰股份有限公司
BIOSTAR GROUP

Title	DDR DIMM-2	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 14 of 45	



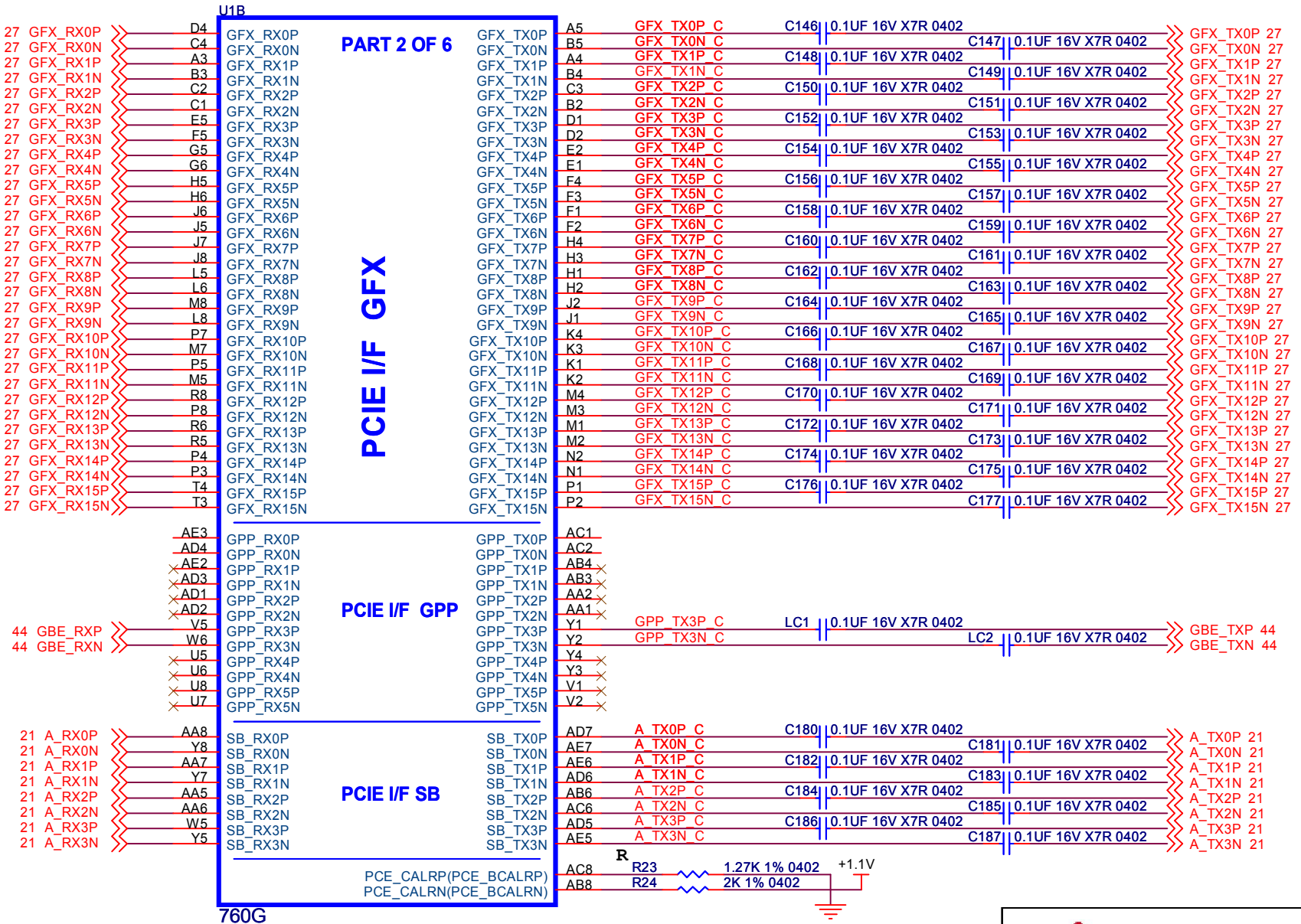
映泰股份有限公司
BIOSTAR GROUP

Title	ADO Extreme	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 15 of 45	



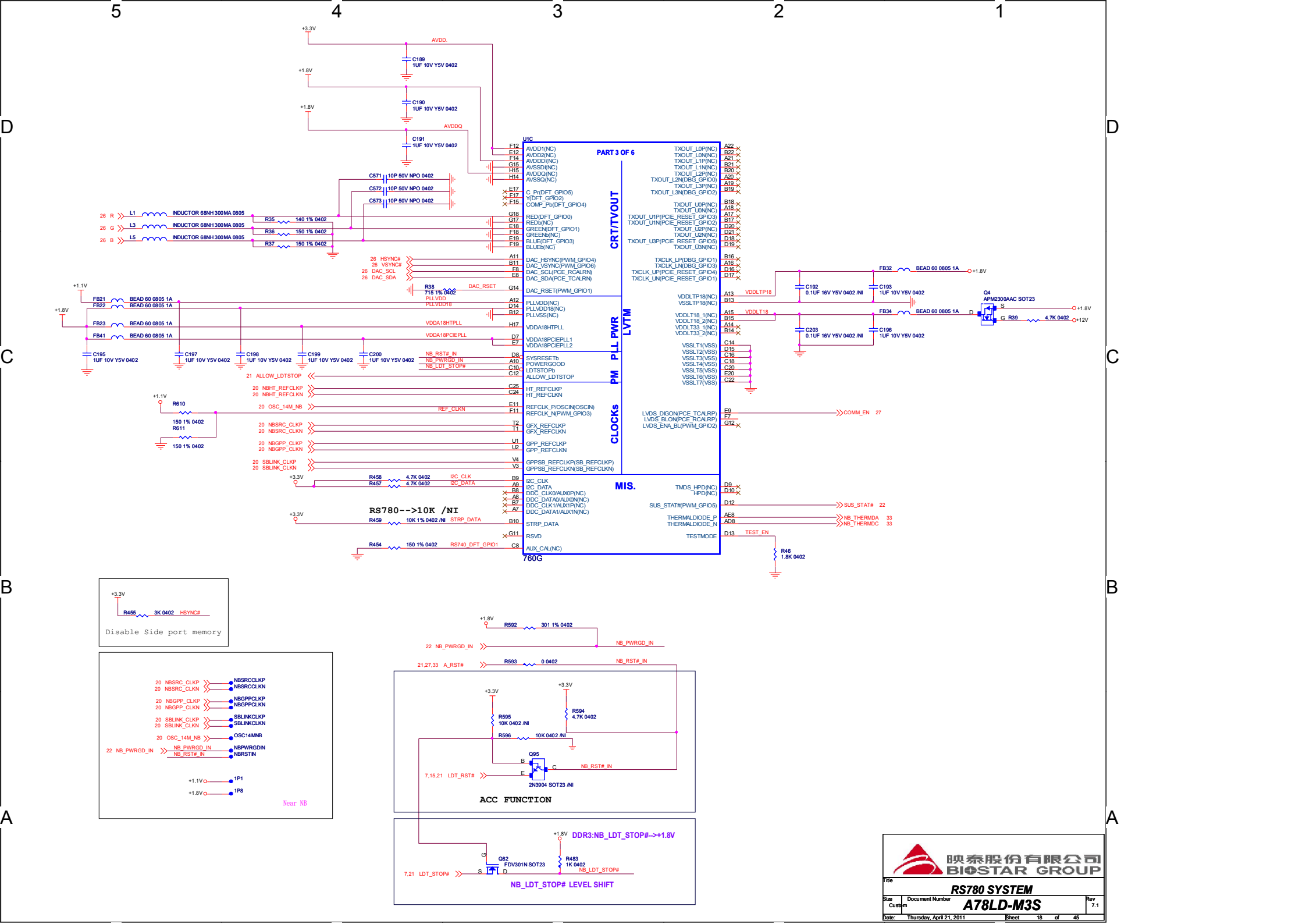
映泰股份有限公司
BIOSTAR GROUP

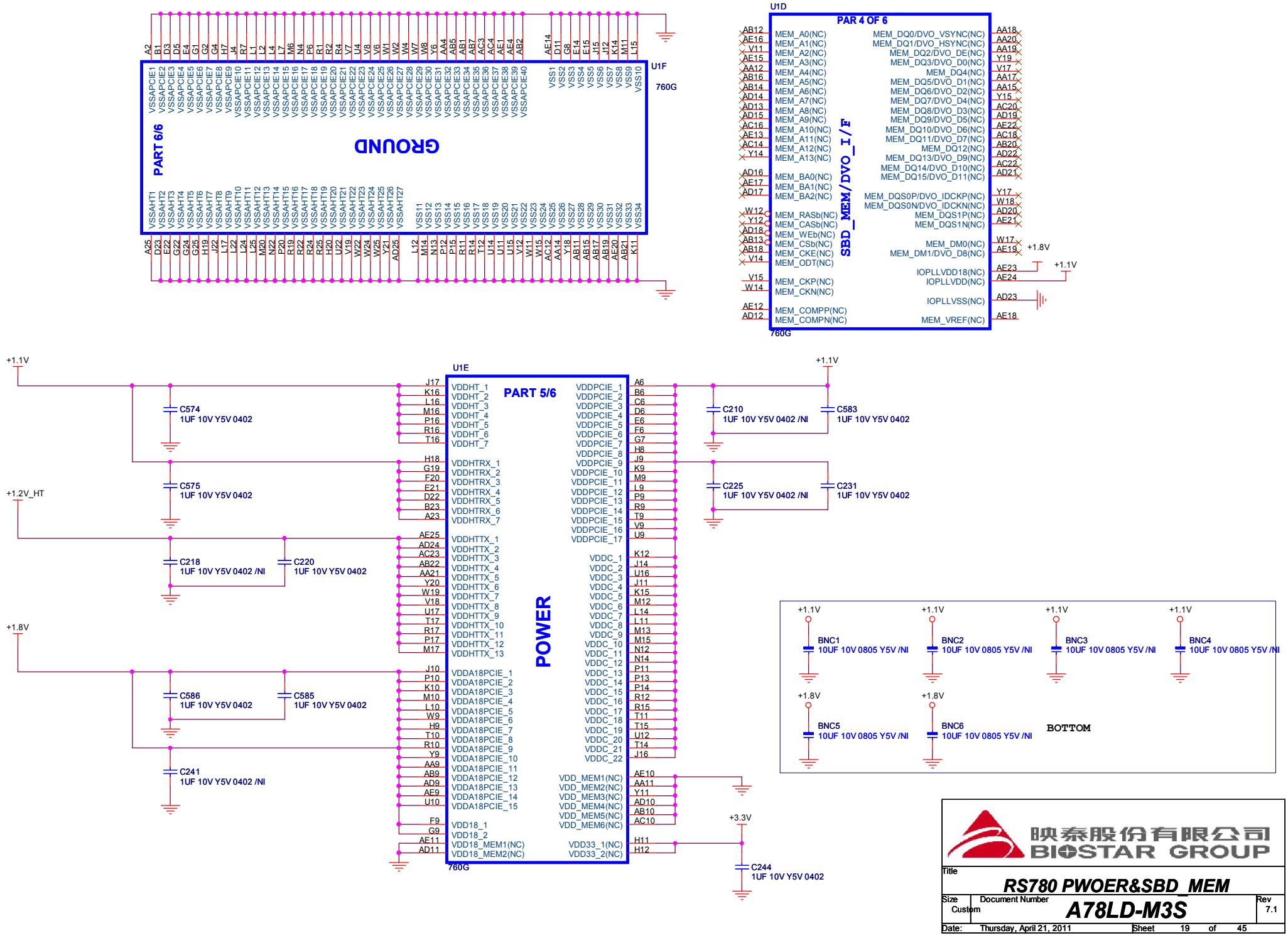
Title	RS780 PCI-E	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 16 of 45	

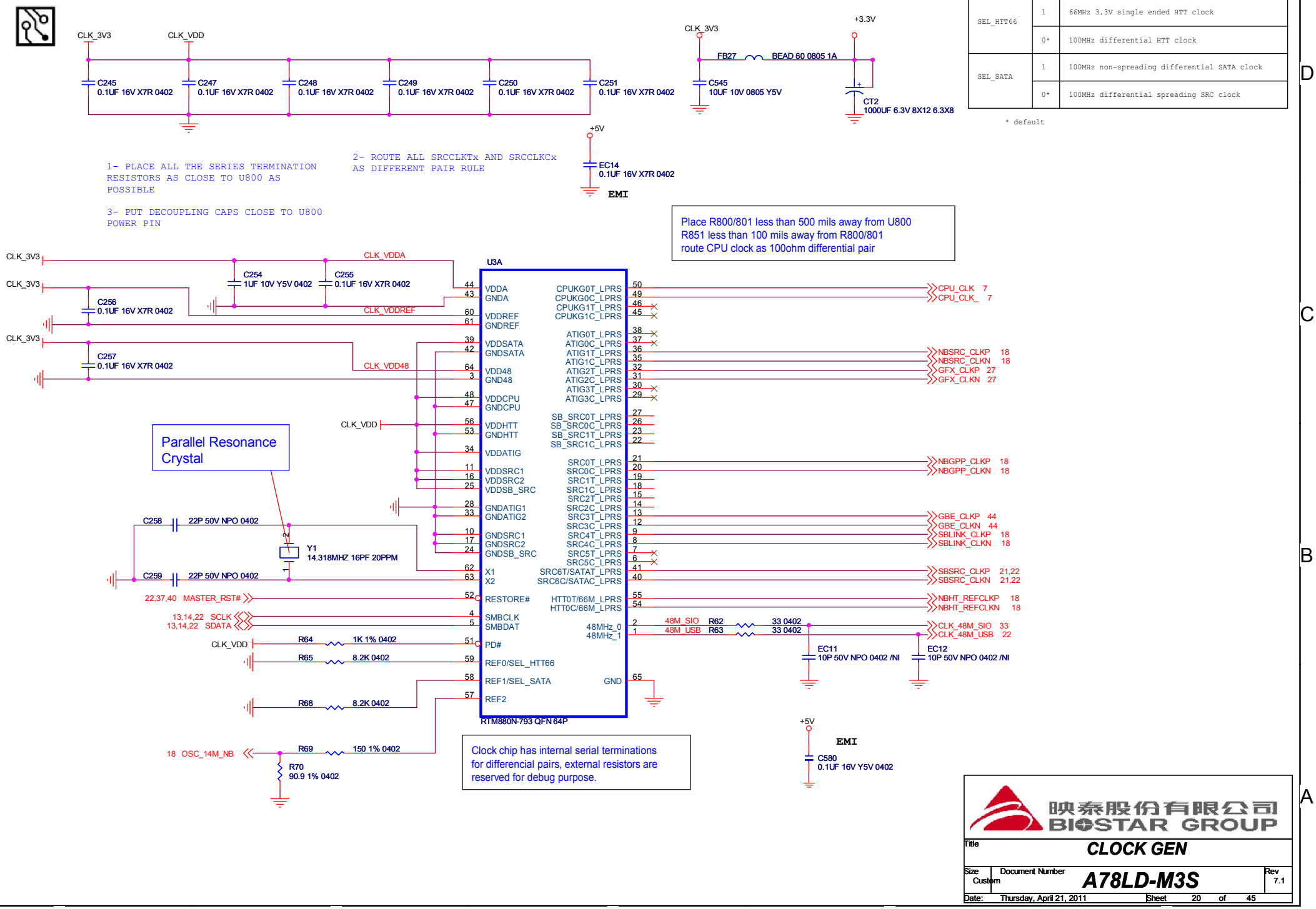


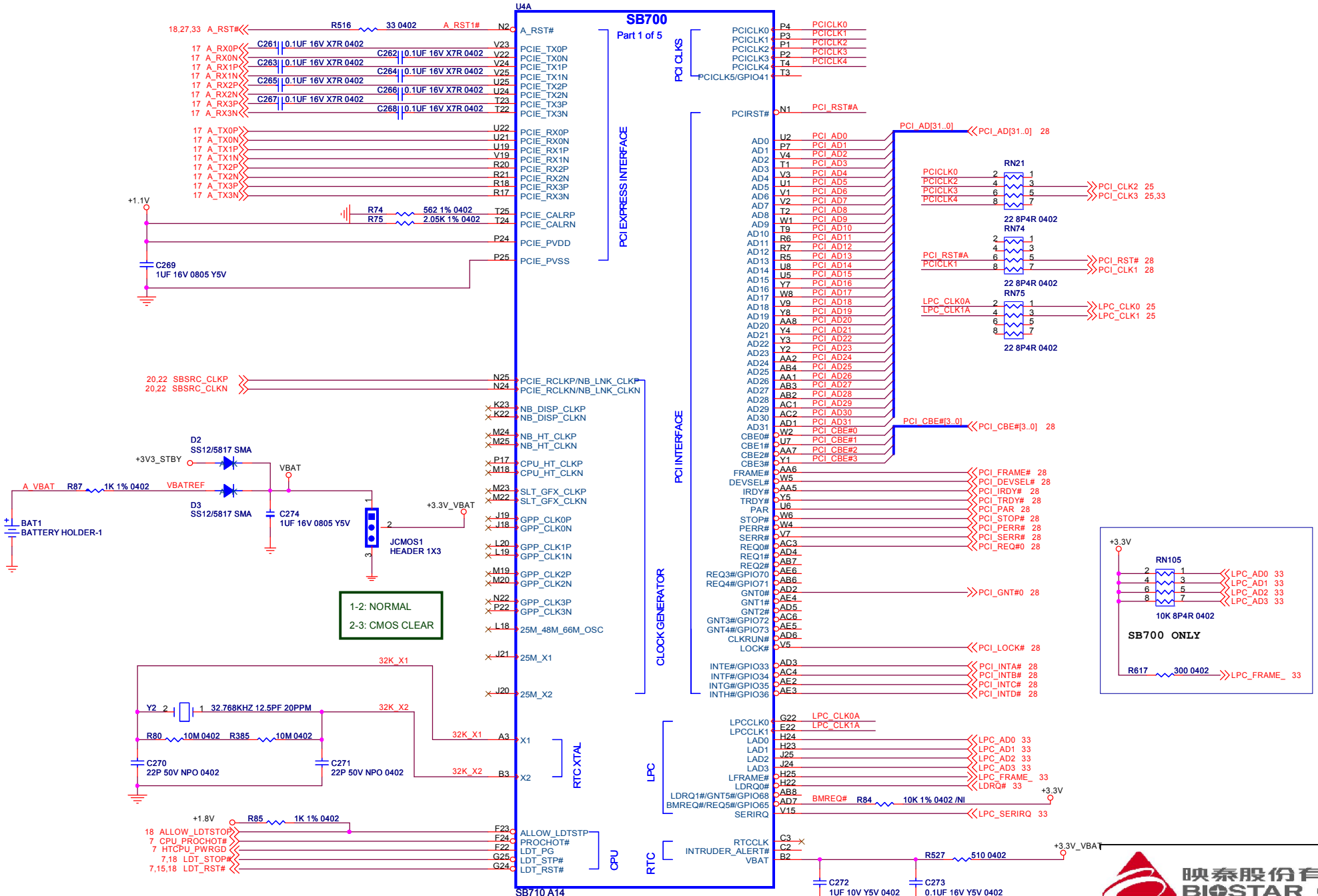
Title	RS780 PCI-E
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	17 of 45

映泰股份有限公司 BIOSTAR GROUP


U1C
PART 3 OF 6
760G
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.
AVDD1(NC)
AVDD2(NC)
AVDD3(NC)
AVSSD(NC)
AVDDQ(NC)
AVSSQ(NC)
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SCL(PCE_RCALRN)
DAC_SDA(PCE_TCALRN)
DAC_RSET(PWM_GPIO1)
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
SYSRESETb
POWERGOOD
LDTSTOPb
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN(OSCIN)
REFCLK_N(PWM_GPIO3)
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
I2C_CLK
I2C_DATA
DDC_CLK0/AUXDP(NC)
DDC_DATA0/AUX0N(NC)
DDC_CLK1/AUX1P(NC)
DDC_DATA1/AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)
TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
VDDLTP18(NC)
VSSLTP18(NC)
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)
LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
TMDS_HPD(NC)
HPD(NC)
SUS_STAT#(PWM_GPIO5)
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
C189 1UF 10V Y5V 0402
C190 1UF 10V Y5V 0402
C191 1UF 10V Y5V 0402
C571 10P 50V NPO 0402
C572 10P 50V NPO 0402
C573 10P 50V NPO 0402
L1 INDUCTOR 68NH 300MA 0805
L3 INDUCTOR 68NH 300MA 0805
L5 INDUCTOR 68NH 300MA 0805
R35 140 1% 0402
R36 150 1% 0402
R37 150 1% 0402
R38 715 1% 0402
FB21 BEAD 60 0805 1A
FB22 BEAD 60 0805 1A
FB23 BEAD 60 0805 1A
FB41 BEAD 60 0805 1A
FB32 BEAD 60 0805 1A
FB34 BEAD 60 0805 1A
C195 1UF 10V Y5V 0402
C197 1UF 10V Y5V 0402
C198 1UF 10V Y5V 0402
C199 1UF 10V Y5V 0402
C200 1UF 10V Y5V 0402
C192 0.1UF 16V Y5V 0402 /NI
C193 1UF 10V Y5V 0402
C203 0.1UF 16V Y5V 0402 /NI
C196 1UF 10V Y5V 0402
Q4 APM2300AAC SOT23
R39 4.7K 0402
R610 150 1% 0402
R611 150 1% 0402
R458 4.7K 0402
R457 4.7K 0402
R459 10K 1% 0402 /NI
R454 150 1% 0402
R46 1.8K 0402
RS780-->10K /NI
R455 3K 0402 HSYNC#
Disable Side port memory
Near NB
R592 301 1% 0402
R593 0 0402
R595 10K 0402 /NI
R594 4.7K 0402
R596 10K 0402 /NI
Q95 2N3904 SOT23 /NI
ACC FUNCTION
Q82 FDV301N SOT23
R483 1K 0402
DDR3:NB_LDT_STOP#-->+1.8V
NB_LDT_STOP# LEVEL SHIFT
映泰股份有限公司
BIOSTAR GROUP
RS780 SYSTEM
A78LD-M3S
Rev 7.1
Thursday, April 21, 2011
Sheet 18 of 45

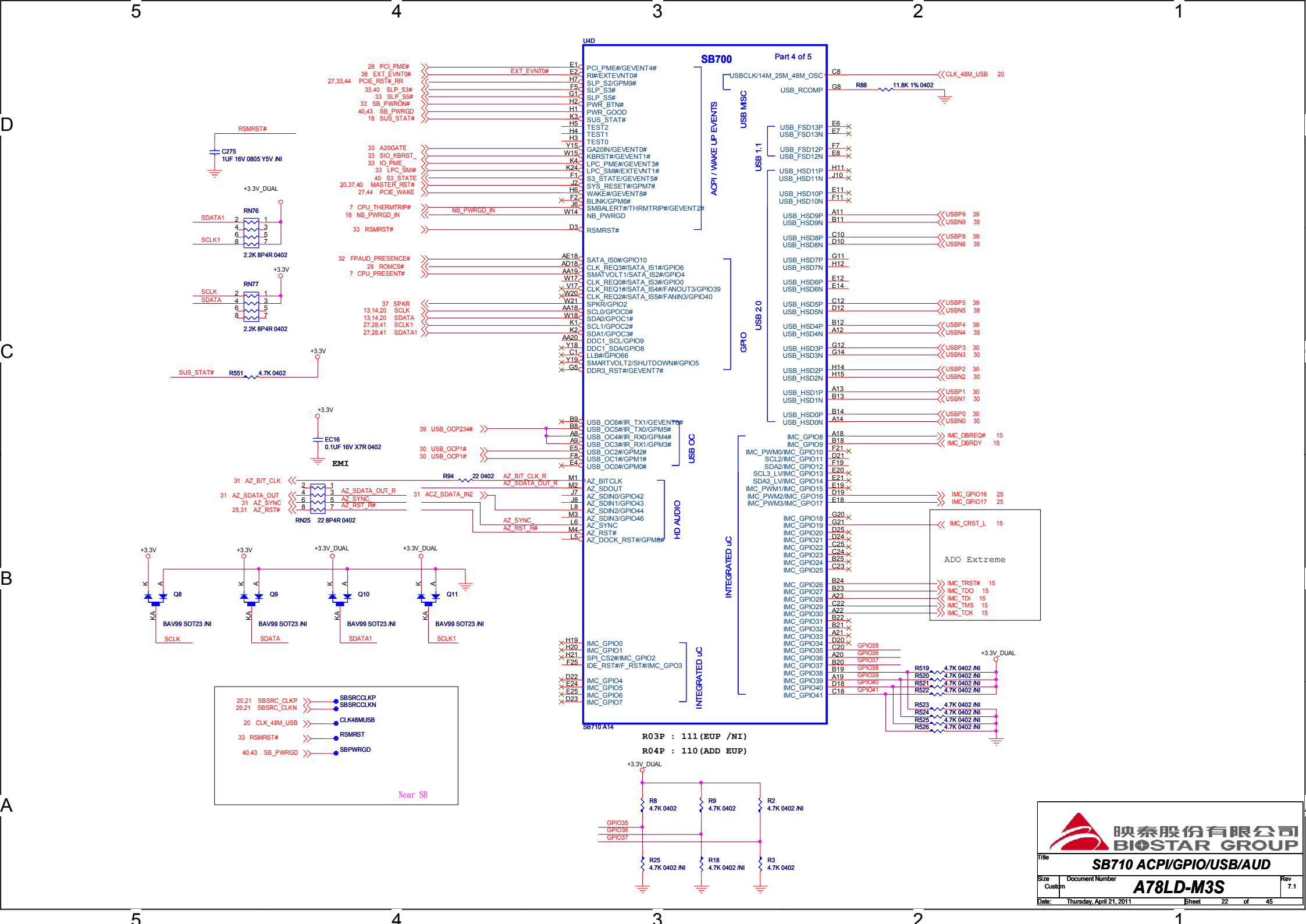

U1F
760G
PART 6/6
GROUND
U1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
760G
U1E
PART 5/6
POWER
760G
+1.1V
+1.2V_HT
+1.8V
+3.3V
C574 1UF 10V Y5V 0402
C575 1UF 10V Y5V 0402
C218 1UF 10V Y5V 0402 /NI
C220 1UF 10V Y5V 0402
C586 1UF 10V Y5V 0402
C585 1UF 10V Y5V 0402
C241 1UF 10V Y5V 0402 /NI
C210 1UF 10V Y5V 0402 /NI
C583 1UF 10V Y5V 0402
C225 1UF 10V Y5V 0402 /NI
C231 1UF 10V Y5V 0402
C244 1UF 10V Y5V 0402
BNC1 10UF 10V 0805 Y5V /NI
BNC2 10UF 10V 0805 Y5V /NI
BNC3 10UF 10V 0805 Y5V /NI
BNC4 10UF 10V 0805 Y5V /NI
BNC5 10UF 10V 0805 Y5V /NI
BNC6 10UF 10V 0805 Y5V /NI
BOTTOM
映泰股份有限公司
BIOSTAR GROUP
Title
RS780 PWOER&SBD_MEM
Size Custom
Document Number
A78LD-M3S
Rev 7.1
Date: Thursday, April 21, 2011
Sheet 19 of 45


CLK_3V3
CLK_VDD
C245 0.1UF 16V X7R 0402
C247 0.1UF 16V X7R 0402
C248 0.1UF 16V X7R 0402
C249 0.1UF 16V X7R 0402
C250 0.1UF 16V X7R 0402
C251 0.1UF 16V X7R 0402
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN
+5V
EC14 0.1UF 16V X7R 0402
EMI
CLK_3V3
FB27 BEAD 60 0805 1A
+3.3V
C545 10UF 10V 0805 Y5V
CT2 1000UF 6.3V 8X12 6.3X8
SEL_HTT66 1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
SEL_SATA 1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
* default
Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair
U3A
VDDA GNDA VDDREF GNDREF VDDSATA GNDSATA VDD48 GND48 VDDCPU GNDCPU VDDHTT GNDHTT VDDATIG VDDSRC1 VDDSRC2 VDDSB_SRC GNDATIG1 GNDATIG2 GNDSRC1 GNDSRC2 GNDSB_SRC X1 X2 RESTORE# SMBCLK SMBDAT PD# REF0/SEL_HTT66 REF1/SEL_SATA REF2
CPUKG0T_LPRS CPUKG0C_LPRS CPUKG1T_LPRS CPUKG1C_LPRS
ATIG0T_LPRS ATIG0C_LPRS ATIG1T_LPRS ATIG1C_LPRS ATIG2T_LPRS ATIG2C_LPRS ATIG3T_LPRS ATIG3C_LPRS
SB_SRC0T_LPRS SB_SRC0C_LPRS SB_SRC1T_LPRS SB_SRC1C_LPRS
SRC0T_LPRS SRC0C_LPRS SRC1T_LPRS SRC1C_LPRS SRC2T_LPRS SRC2C_LPRS SRC3T_LPRS SRC3C_LPRS SRC4T_LPRS SRC4C_LPRS SRC5T_LPRS SRC5C_LPRS SRC6T/SATAT_LPRS SRC6C/SATAC_LPRS
HTT0T/66M_LPRS HTT0C/66M_LPRS
48MHz_0 48MHz_1 GND
RTM880N-793 QFN 64P
CPU_CLK 7
CPU_CLK_ 7
NBSRC_CLKP 18
NBSRC_CLKN 18
GFX_CLKP 27
GFX_CLKN 27
NBGPP_CLKP 18
NBGPP_CLKN 18
GBE_CLKP 44
GBE_CLKN 44
SBLINK_CLKP 18
SBLINK_CLKN 18
SBSRC_CLKP 21,22
SBSRC_CLKN 21,22
NBHT_REFCLKP 18
NBHT_REFCLKN 18
CLK_48M_SIO 33
CLK_48M_USB 22
48M_SIO R62 33 0402
48M_USB R63 33 0402
EC11 10P 50V NPO 0402 /NI
EC12 10P 50V NPO 0402 /NI
C254 1UF 10V Y5V 0402
C255 0.1UF 16V X7R 0402
C256 0.1UF 16V X7R 0402
C257 0.1UF 16V X7R 0402
CLK_VDDA
CLK_VDDREF
CLK_VDD48
Parallel Resonance Crystal
C258 22P 50V NPO 0402
C259 22P 50V NPO 0402
Y1 14.318MHZ 16PF 20PPM
22,37,40 MASTER_RST#
13,14,22 SCLK
13,14,22 SDATA
R64 1K 1% 0402
R65 8.2K 0402
R68 8.2K 0402
R69 150 1% 0402
R70 90.9 1% 0402
18 OSC_14M_NB
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
+5V
EMI
C580 0.1UF 16V Y5V 0402
映泰股份有限公司
BIOSTAR GROUP
Title
CLOCK GEN
Size Custom
Document Number A78LD-M3S
Rev 7.1
Date: Thursday, April 21, 2011
Sheet 20 of 45



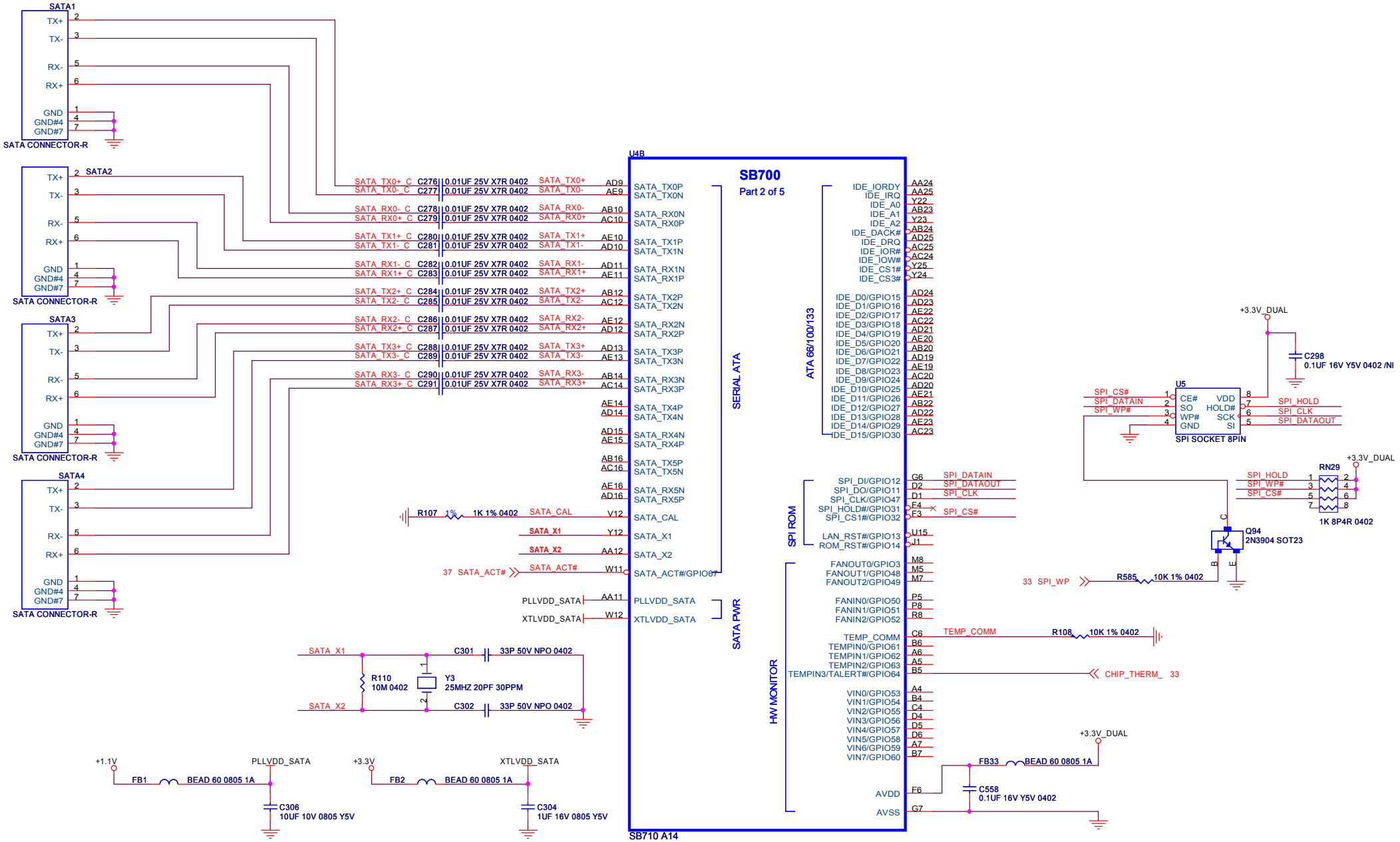
Title	SB710 PCIE/PCI/CPU/LPC
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	21 of 45

映泰股份有限公司 BIOSTAR GROUP



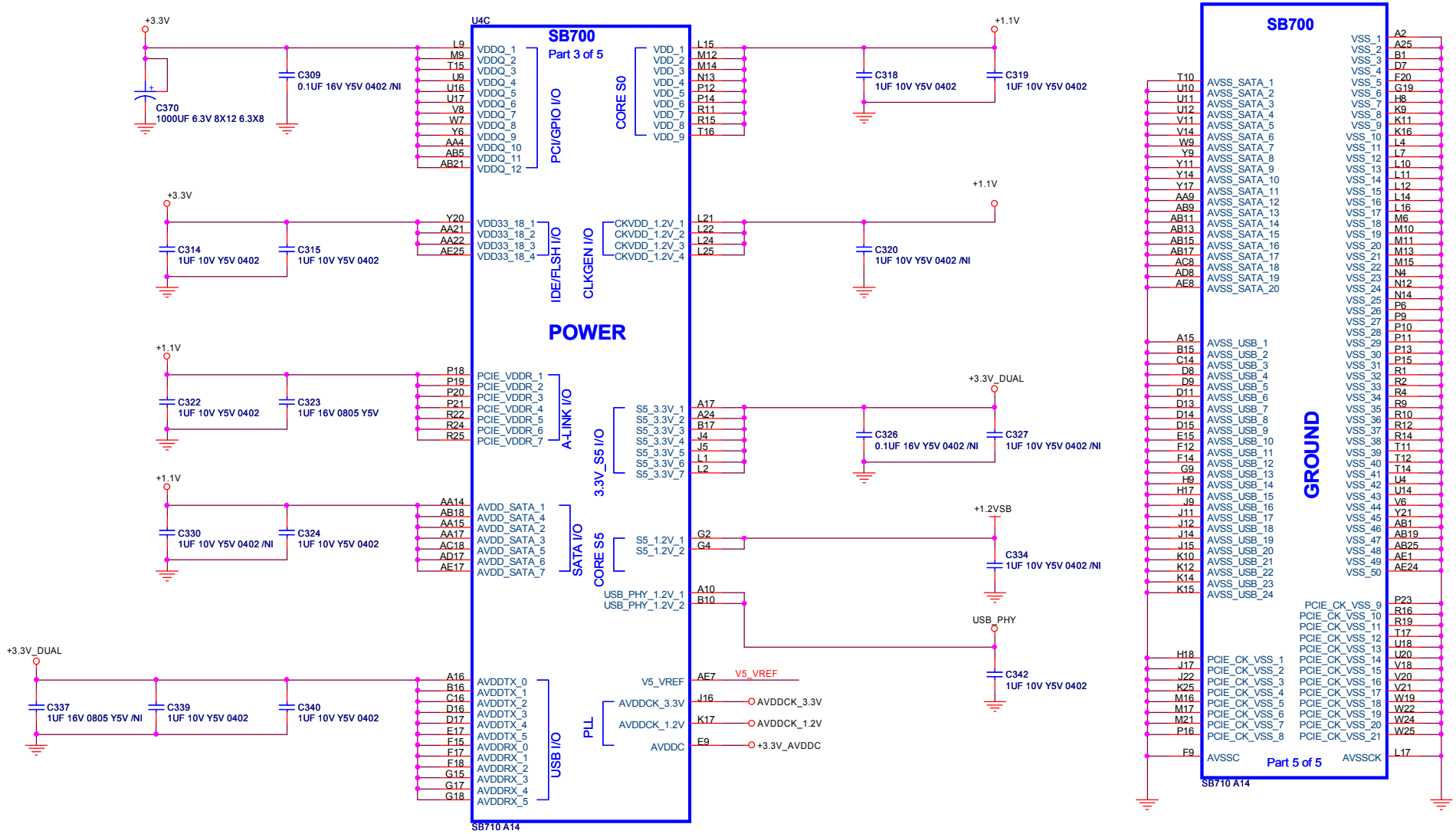
Title	SB710 ACPI/GPIO/USB/AUD
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	22 of 45

映泰股份有限公司 BIOSTAR GROUP

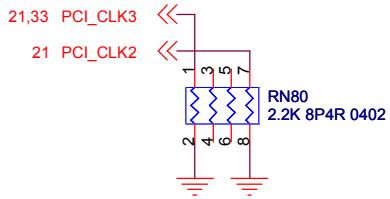


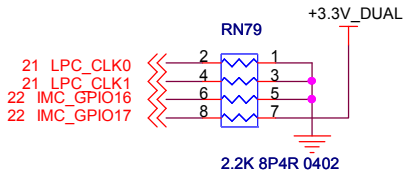
映泰股份有限公司
BIOSTAR GROUP

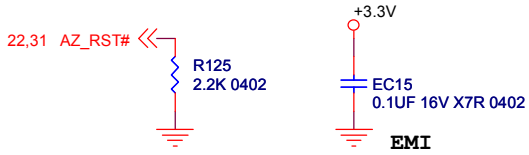
Title	SB710 SATA/IDE/SPI	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 23 of 45	



Title	SB710 POWER
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	24 of 45







REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

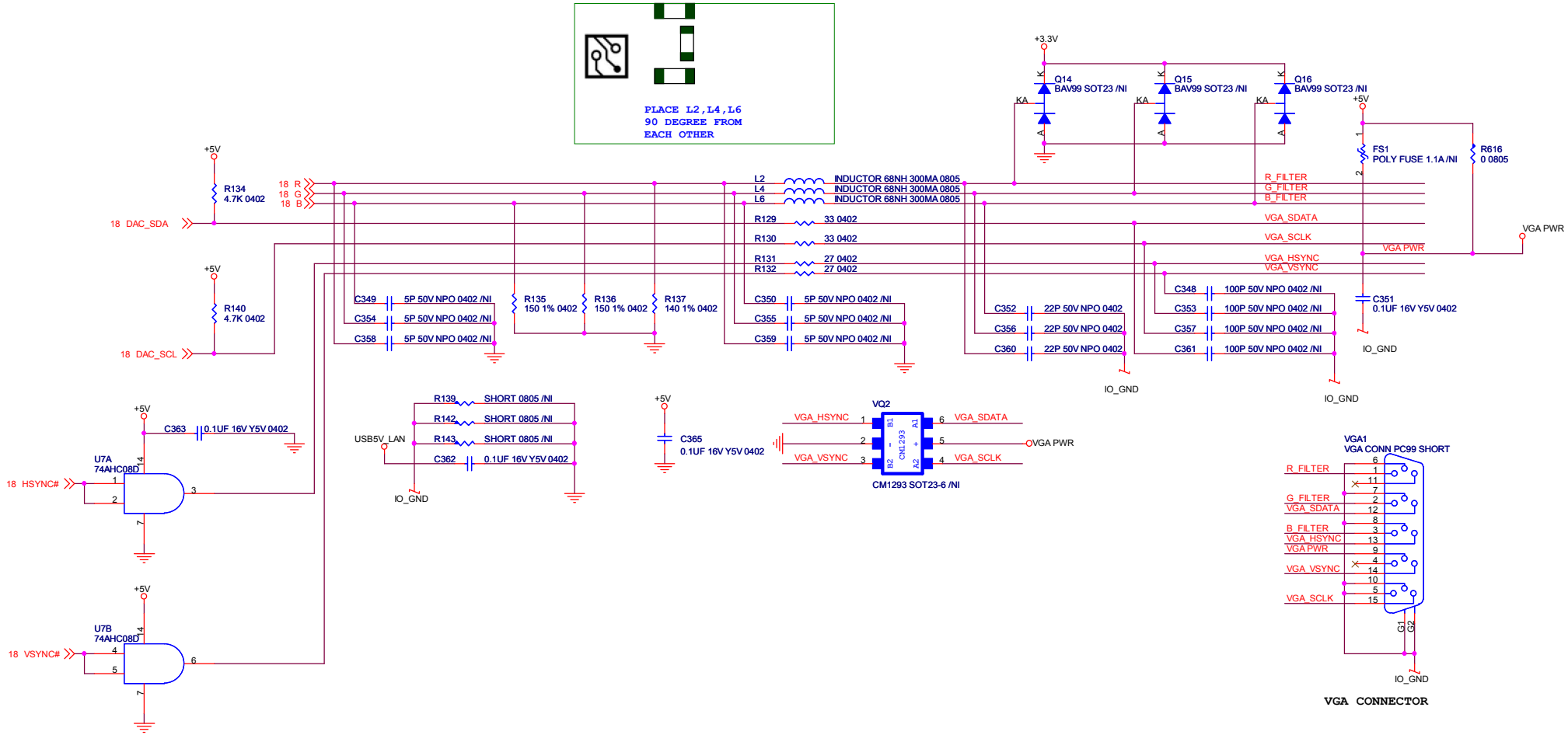
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

映泰股份有限公司 BIOSTAR GROUP

Title: SB710 STRAP

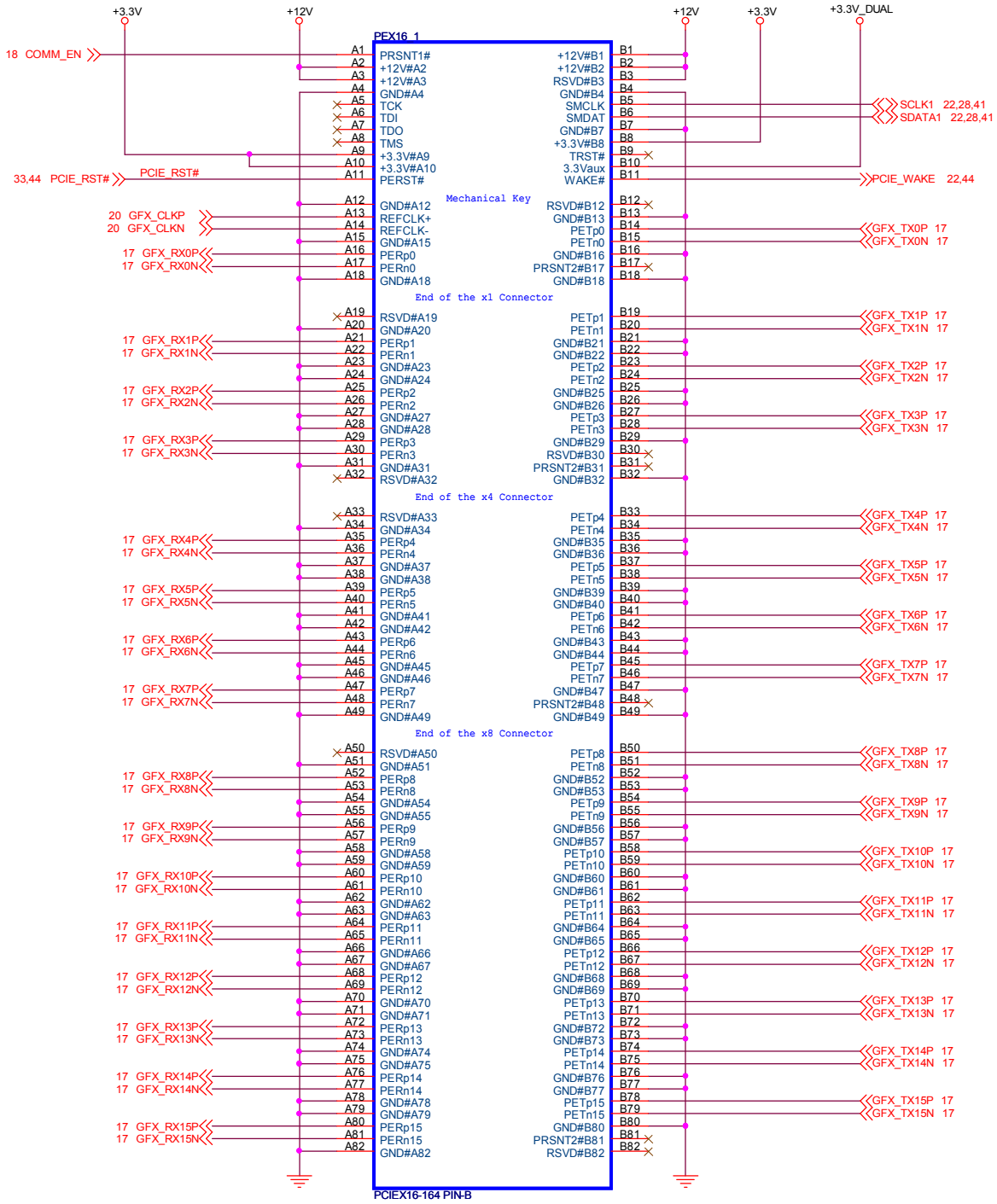
Size: Custom | Document Number: A78LD-M3S | Rev: 7.1

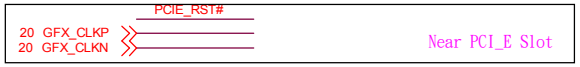
Date: Thursday, April 21, 2011 | Sheet 25 of 45

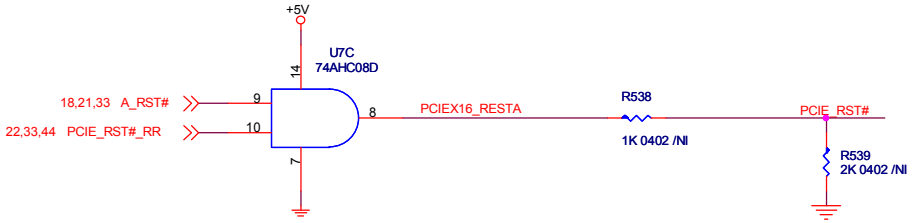


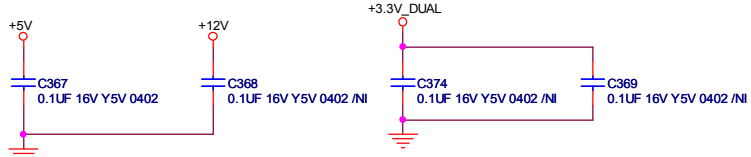
Title	CRT
Size	Custom
Document Number	A78LD-M3S
Rev	7.1
Date:	Thursday, April 21, 2011
Sheet	26 of 45

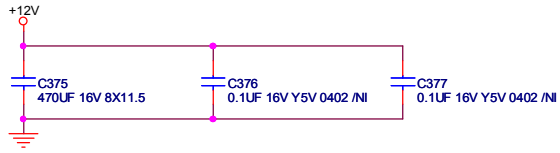
映泰股份有限公司 BIOSTAR GROUP

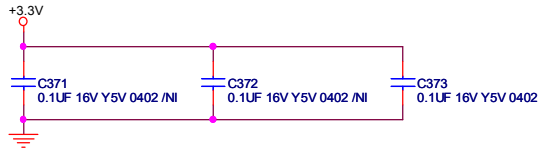


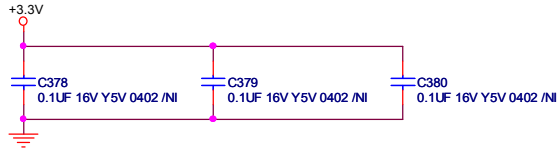












映泰股份有限公司
BIOSTAR GROUP

Title	PCI-E SLOT	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 27 of 45	

IDSEL:AD21 , INT:ABCD , REQ0 & GNT0 , PCI_CLK3

IDSEL:AD22 , INT:BCDA , REQ1 & GNT1 , PCI_CLK4

PCI_SLOT 1

PCI1

PCI-120 PIN-R

CT34
1000UF 6.3V 8X12 6.3X8

RN31
4.7K 8P4R 0402

R182 0 0402 /NI

R185 100 1% 0402

C382 0.1UF 16V Y5V 0402 /NI

C384 0.1UF 16V Y5V 0402 /NI

RN33
8.2K 8P4R 0402

FOR EMI NEAR C382
EC7 0.1UF 16V Y5V 0402 /NI

FOR EMI NEAR RN32
EC8 0.1UF 16V Y5V 0402 /NI

FOR EMI NEAR C409
EC1 0.1UF 16V Y5V 0402

Near PCI Slot

B1	-12V	TRST#	A1
B2	TCK	+12V	A2
B3	GND#B3	TMS	A3
B4	TDO	TDI	A4
B5	+5V#B5	+5V#A5	A5
B6	+5V#B6	INTA#	A6
B7	INTB#	INTC#	A7
B8	INTD#	+5V#A8	A8
B9	PRSNT1#	RESERVED#A9	A9
B10	RESERVED#B10	+5Vi/o#A10	A10
B11	PRSNT2#	RESERVED#A11	A11
B12	GND#B12	GND#A12	A12
B13	GND#B13	GND#A13	A13
B14	RESERVED#B14	3.3Vaux	A14
B15	GND#B15	RESET#	A15
B16	CLK	+5Vi/o#A16	A16
B17	GND#B17	GNT#	A17
B18	REQ#	GND#A18	A18
B19	+5Vi/o#B19	PME#	A19
B20	AD31	AD30	A20
B21	AD29	+3.3V#A21	A21
B22	GND#B22	AD28	A22
B23	AD27	AD26	A23
B24	AD25	GND#A24	A24
B25	+3.3V#B25	AD24	A25
B26	C/BE#3	IDSEL	A26
B27	AD23	+3.3V#A27	A27
B28	GND#B28	AD22	A28
B29	AD21	AD20	A29
B30	AD19	GND#A30	A30
B31	+3.3V#B31	AD18	A31
B32	AD17	AD16	A32
B33	C/BE#2	+3.3V#A33	A33
B34	GND#B34	FRAME#	A34
B35	IRDY#	GND#A35	A35
B36	+3.3V#B36	TRDY#	A36
B37	DEVSEL#	GND#A37	A37
B38	GND#B38	STOP#	A38
B39	LOCK#	+3.3V#A39	A39
B40	PERR#	RESERVED#A40	A40
B41	+3.3V#B41	RESERVED	A41
B42	SERR#	GND#A42	A42
B43	+3.3V#B43	PAR	A43
B44	C/BE#1	AD15	A44
B45	AD14	+3.3V#A45	A45
B46	GND#B46	AD13	A46
B47	AD12	AD11	A47
B48	AD10	GND#A48	A48
B49	GND#B49	AD9	A49
B52	AD8	C/BE#0	A52
B53	AD7	+3.3V	A53
B54	+3.3V#B54	AD6	A54
B55	AD5	AD4	A55
B56	AD3	GND	A56
B57	GND#B57	AD2	A57
B58	AD1	AD0	A58
B59	+5Vi/o#B59	+5Vi/o	A59
B60	ACK64#	REQ64#	A60
B61	+5V#B61	+5V#A61	A61
B62	+5V#B62	+5V	A62

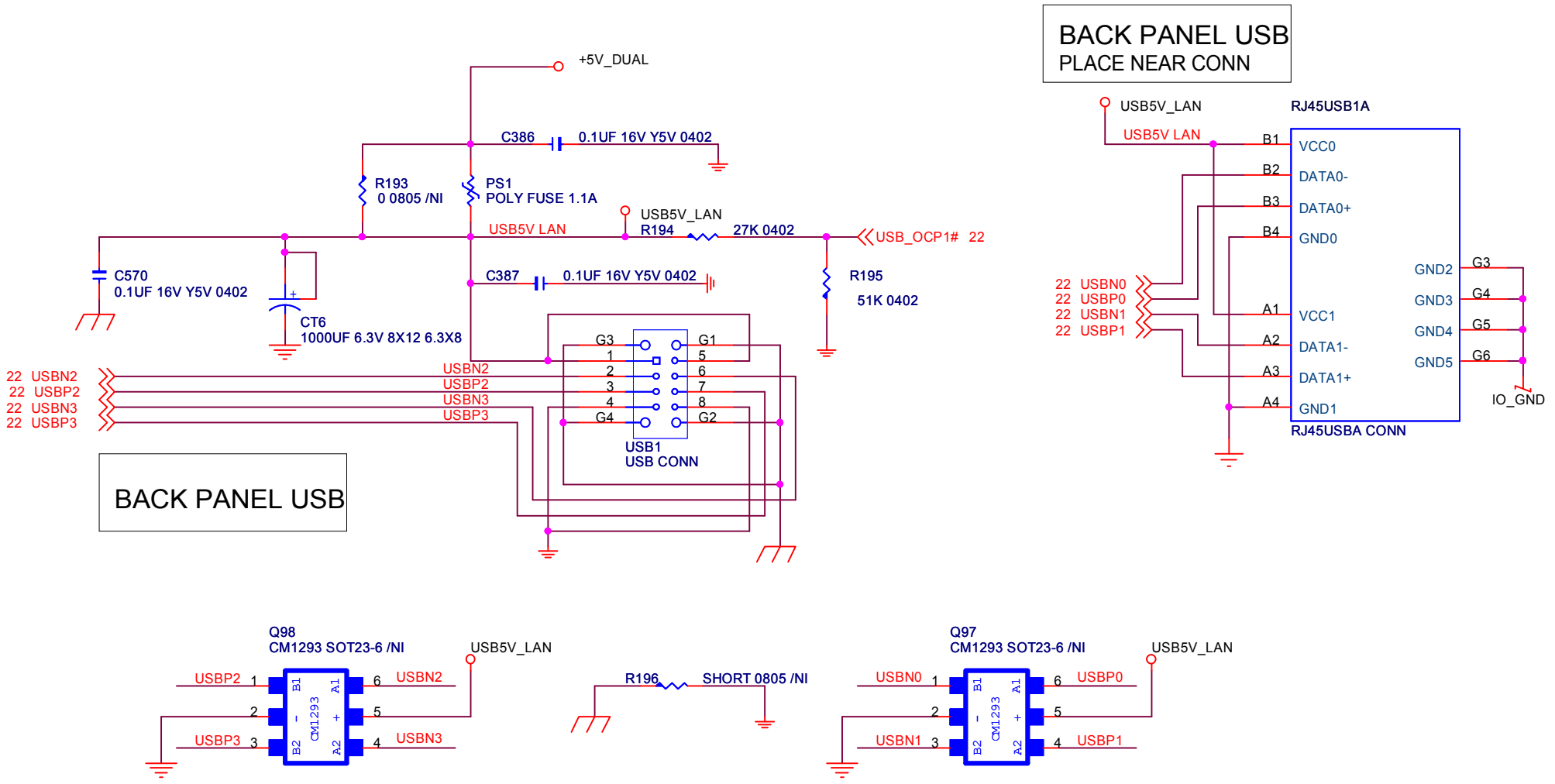
Title: PCI SLOT

Size: Custom | Document Number: A78LD-M3S | Rev: 7.1

Date: Thursday, April 21, 2011 | Sheet 28 of 45

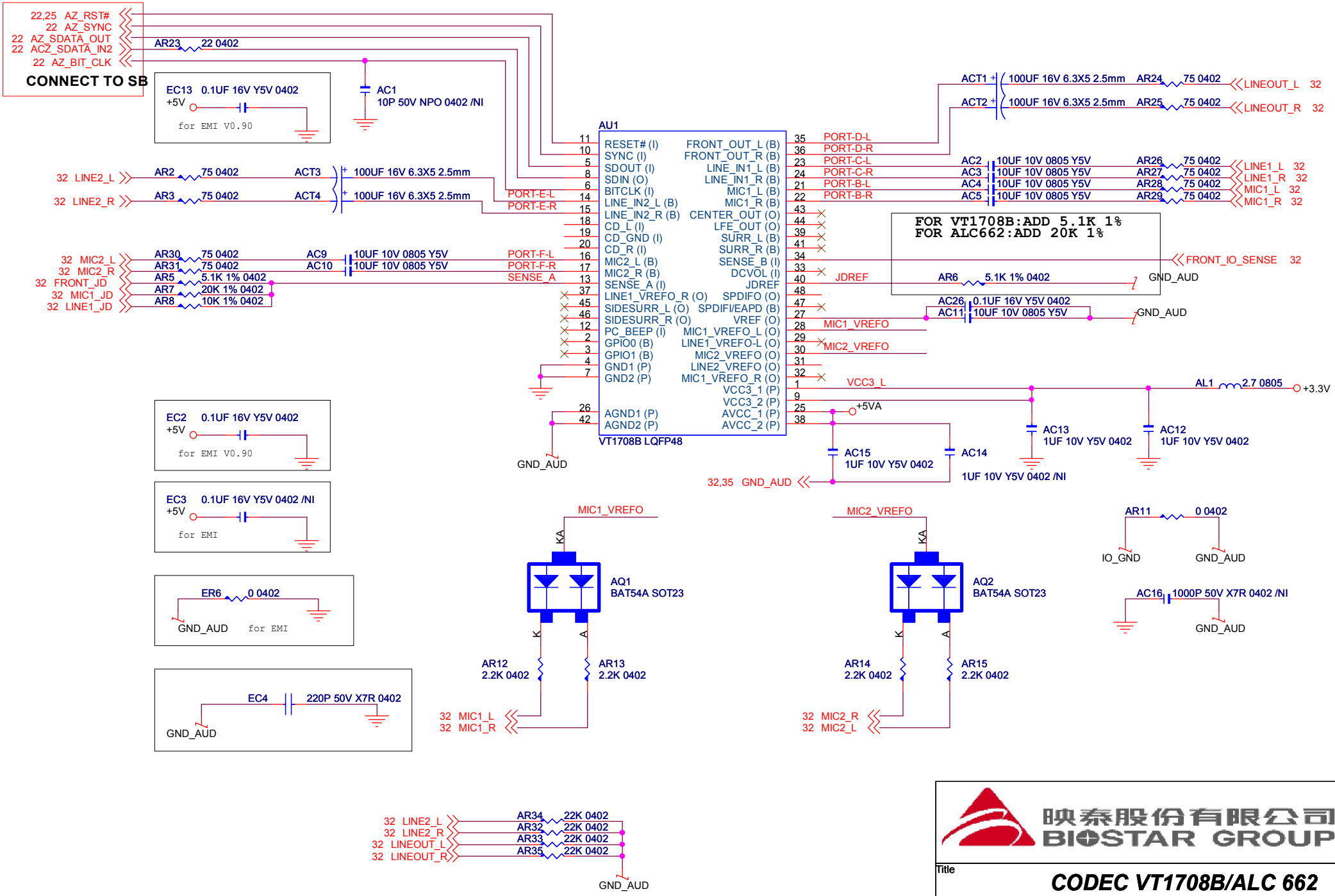
映泰股份有限公司
BIOSTAR GROUP

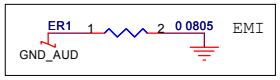
Title	NONE	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 29 of 45	



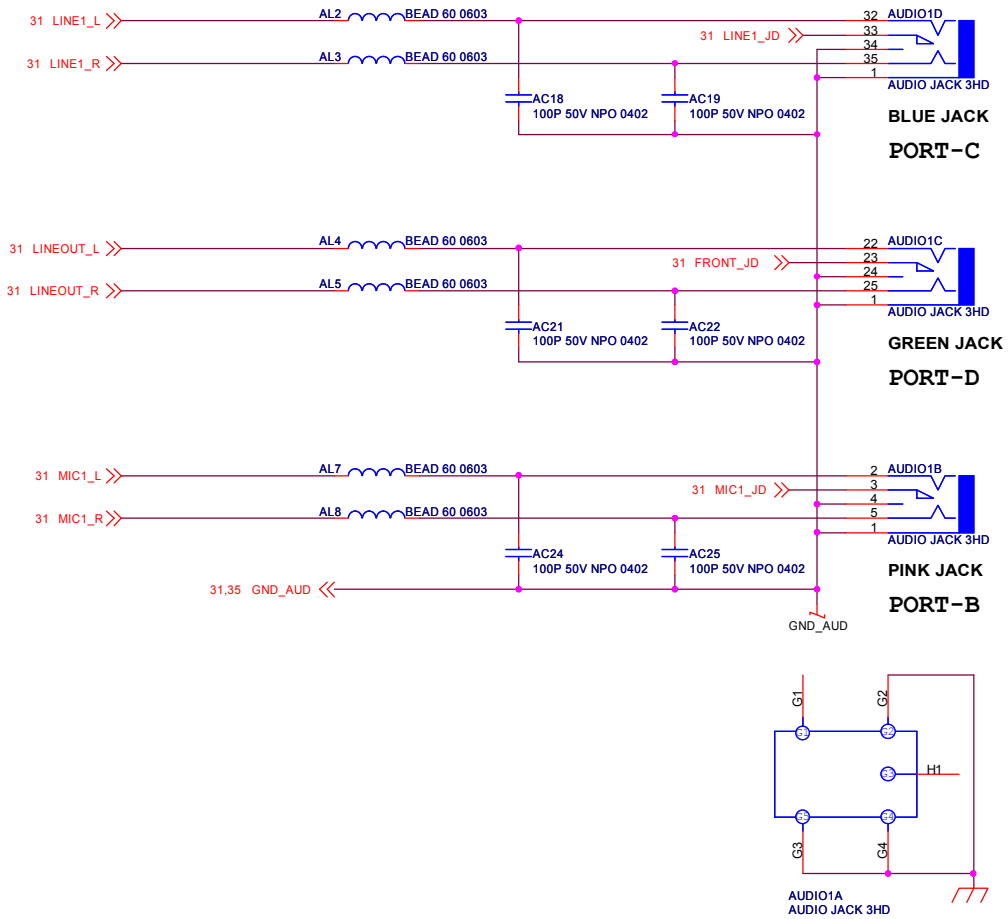
映泰股份有限公司
BIOSTAR GROUP

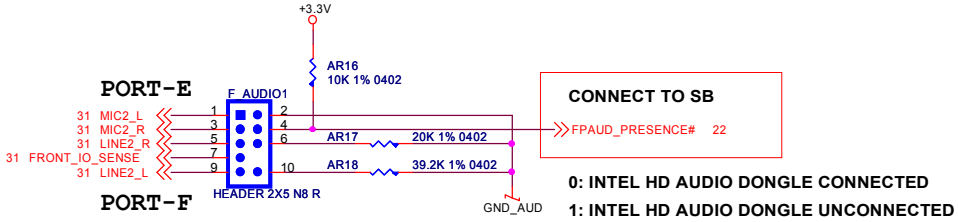
Title	**USB CONN**	
Size: Custom	Document Number: **A78LD-M3S**	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 30 of 45	


22,25 AZ_RST#
22 AZ_SYNC
22 AZ_SDATA_OUT
22 AZ_SDATA_IN2
22 AZ_BIT_CLK
CONNECT TO SB
AR23 22 0402
EC13 0.1UF 16V Y5V 0402
+5V
for EMI V0.90
AC1
10P 50V NPO 0402 /NI
AU1
RESET# (I)
SYNC (I)
SDOUT (I)
SDIN (O)
BITCLK (I)
LINE_IN2_L (B)
LINE_IN2_R (B)
CD_L (I)
CD_GND (I)
CD_R (I)
MIC2_L (B)
MIC2_R (B)
SENSE_A (I)
LINE1_VREFO_R (O)
SIDESURR_L (O)
SIDESURR_R (O)
PC_BEEP (I)
GPIO0 (B)
GPIO1 (B)
GND1 (P)
GND2 (P)
AGND1 (P)
AGND2 (P)
FRONT_OUT_L (B)
FRONT_OUT_R (B)
LINE_IN1_L (B)
LINE_IN1_R (B)
MIC1_L (B)
MIC1_R (B)
CENTER_OUT (O)
LFE_OUT (O)
SURR_L (B)
SURR_R (B)
SENSE_B (I)
DCVOL (I)
JDREF
SPDIFO (O)
SPDIFI/EAPD (B)
VREF (O)
MIC1_VREFO_L (O)
LINE1_VREFO_L (O)
MIC2_VREFO (O)
LINE2_VREFO (O)
MIC1_VREFO_R (O)
VCC3_1 (P)
VCC3_2 (P)
AVCC_1 (P)
AVCC_2 (P)
VT1708B LQFP48
PORT-D-L
PORT-D-R
PORT-C-L
PORT-C-R
PORT-B-L
PORT-B-R
ACT1 100UF 16V 6.3X5 2.5mm
ACT2 100UF 16V 6.3X5 2.5mm
AR24 75 0402
AR25 75 0402
LINEOUT_L 32
LINEOUT_R 32
AC2 10UF 10V 0805 Y5V
AC3 10UF 10V 0805 Y5V
AC4 10UF 10V 0805 Y5V
AC5 10UF 10V 0805 Y5V
AR26 75 0402
AR27 75 0402
AR28 75 0402
AR29 75 0402
LINE1_L 32
LINE1_R 32
MIC1_L 32
MIC1_R 32
32 LINE2_L
32 LINE2_R
AR2 75 0402
AR3 75 0402
ACT3 100UF 16V 6.3X5 2.5mm
ACT4 100UF 16V 6.3X5 2.5mm
PORT-E-L
PORT-E-R
FOR VT1708B:ADD 5.1K 1%
FOR ALC662:ADD 20K 1%
FRONT_IO_SENSE 32
JDREF
AR6 5.1K 1% 0402
GND_AUD
AC26 0.1UF 16V Y5V 0402
AC11 10UF 10V 0805 Y5V
GND_AUD
MIC1_VREFO
MIC2_VREFO
32 MIC2_L
32 MIC2_R
32 FRONT_JD
32 MIC1_JD
32 LINE1_JD
AR30 75 0402
AR31 75 0402
AR5 5.1K 1% 0402
AR7 20K 1% 0402
AR8 10K 1% 0402
AC9 10UF 10V 0805 Y5V
AC10 10UF 10V 0805 Y5V
PORT-F-L
PORT-F-R
SENSE_A
VCC3_L
AL1 2.7 0805
+3.3V
+5VA
AC13 1UF 10V Y5V 0402
AC12 1UF 10V Y5V 0402
AC15 1UF 10V Y5V 0402
AC14 1UF 10V Y5V 0402 /NI
32,35 GND_AUD
GND_AUD
EC2 0.1UF 16V Y5V 0402
+5V
for EMI V0.90
EC3 0.1UF 16V Y5V 0402 /NI
+5V
for EMI
ER6 0 0402
GND_AUD for EMI
EC4 220P 50V X7R 0402
GND_AUD
MIC1_VREFO
KA
AQ1
BAT54A SOT23
K
A
AR12
2.2K 0402
AR13
2.2K 0402
32 MIC1_L
32 MIC1_R
MIC2_VREFO
KA
AQ2
BAT54A SOT23
K
A
AR14
2.2K 0402
AR15
2.2K 0402
32 MIC2_R
32 MIC2_L
AR11 0 0402
IO_GND
GND_AUD
AC16 1000P 50V X7R 0402 /NI
GND_AUD
32 LINE2_L
32 LINE2_R
32 LINEOUT_L
32 LINEOUT_R
AR34 22K 0402
AR32 22K 0402
AR33 22K 0402
AR35 22K 0402
GND_AUD
映泰股份有限公司
BIOSTAR GROUP
Title
CODEC VT1708B/ALC 662
Size
Custom
Document Number
A78LD-M3S
Rev
7.1
Date: Thursday, April 21, 2011
Sheet 31 of 45

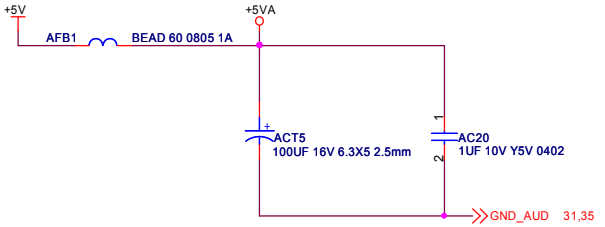


Rear Panel Onboard Analog I/O





AUDIO ANALOG POWER

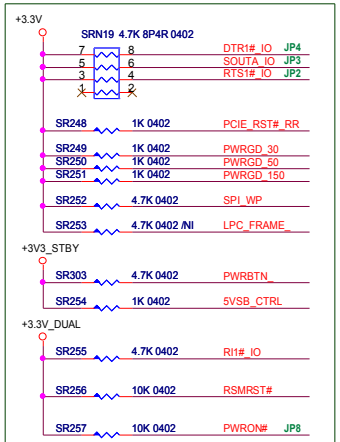


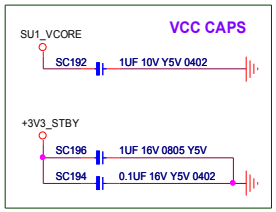
Vout=Vref (1.25V) X (1+R2/R1)
=5V

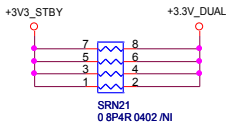
映泰股份有限公司
BIOSTAR GROUP

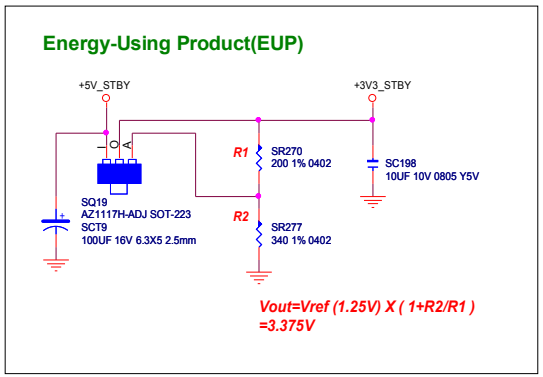
Title	AUDIO CONNECTOR	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 32 of 45	

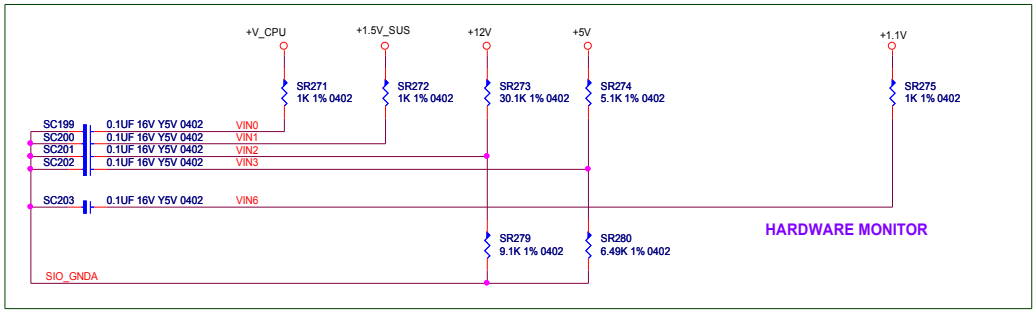
SUPERIO PART: S+Reference

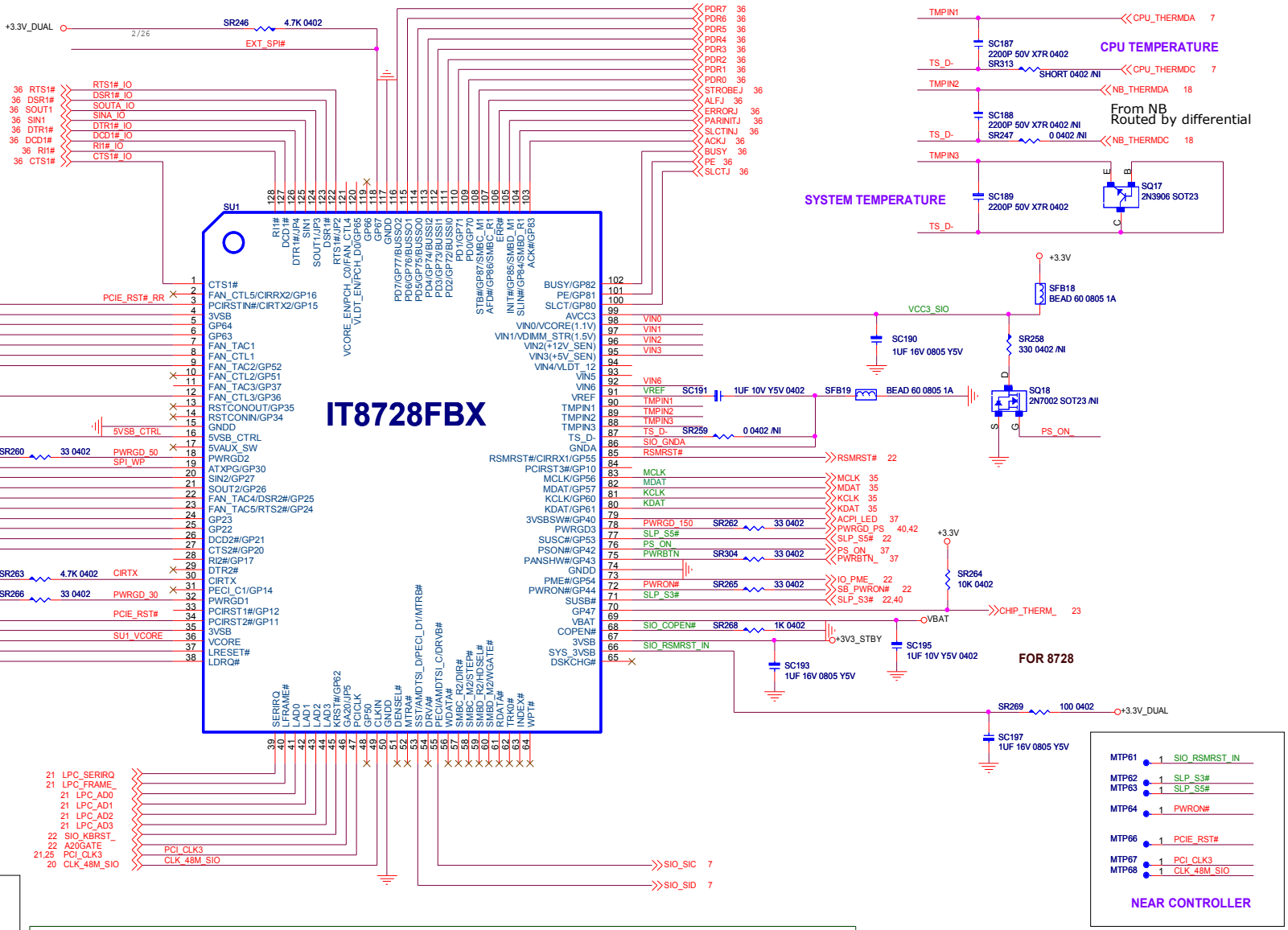






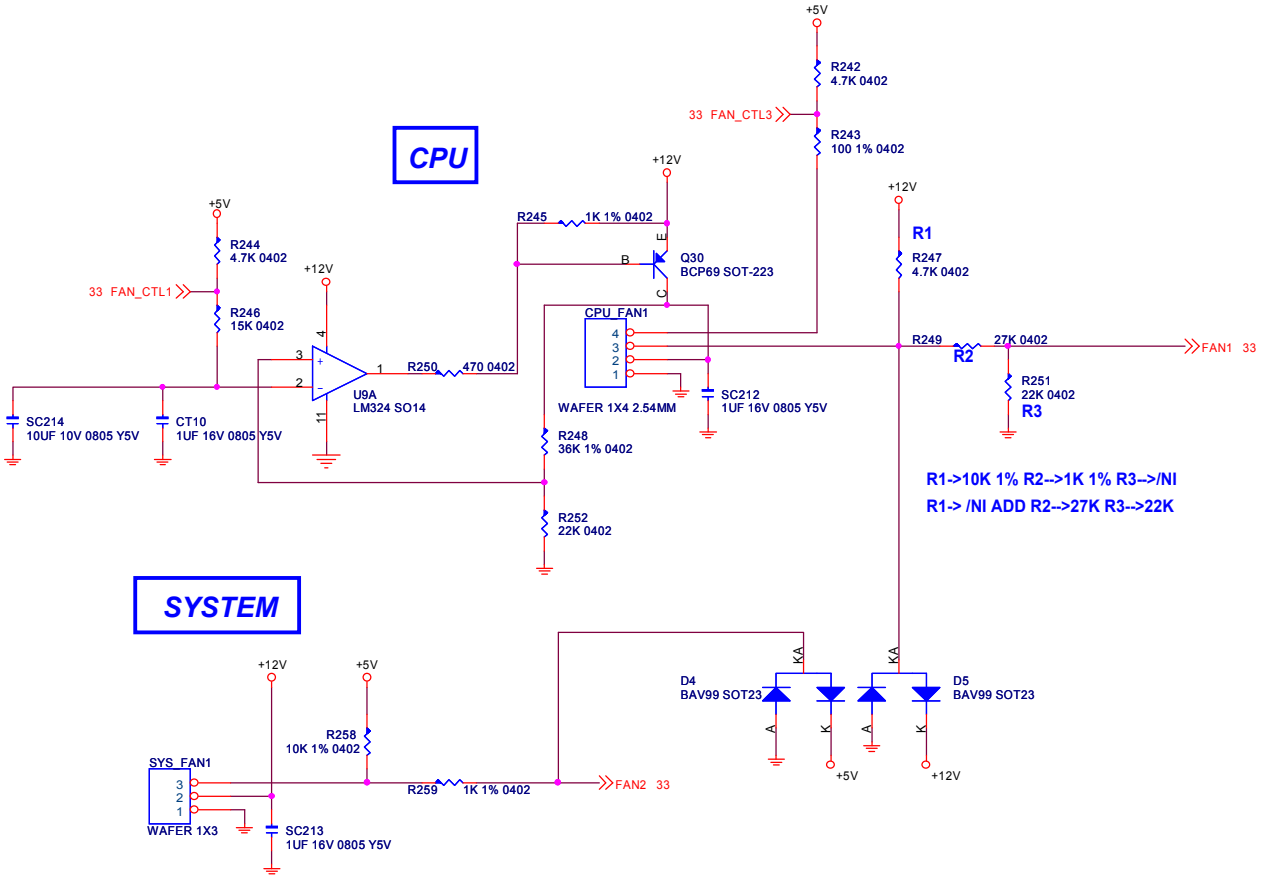




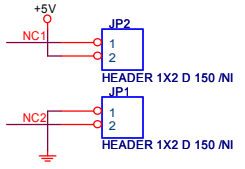


映泰股份有限公司
BIOSTAR GROUP

Title	SUPER I/O ITE 8728	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 33 of 45	



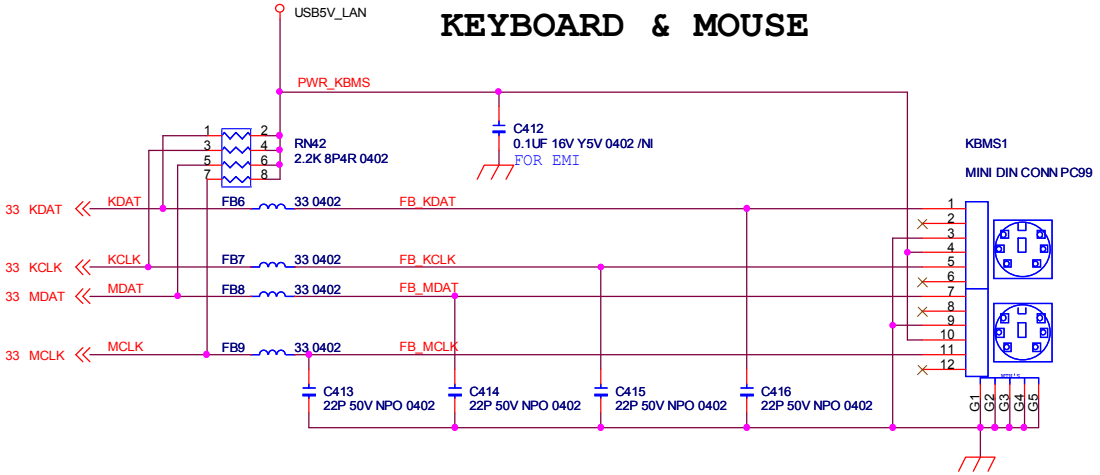
5 mil 60歐姆 測試點

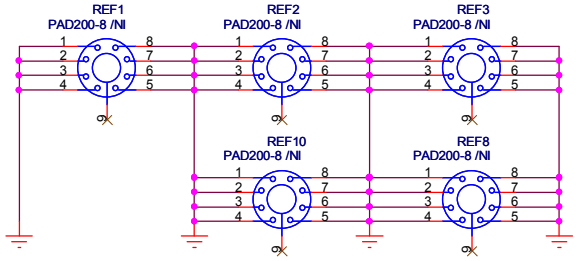


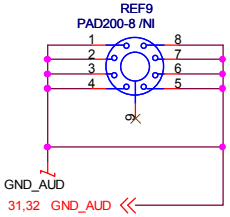
映泰股份有限公司
BIOSTAR GROUP

Title	FAN CONTROL		
Size: Custom	Document Number: A78LD-M3S		Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 34 of 45		

KEYBOARD & MOUSE







映泰股份有限公司
BIOSTAR GROUP

Title	PS2 CONN	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 35 of 45	

COM1

+5V
+12V
U10
ST75185CTR TSSOP /NI
-12V

33 DCD1#
33 DSR1#
33 SIN1
33 RTS1#
33 SOUT1
33 CTS1#
33 DTR1#
33 RI1#

RIN1
RIN2
RIN3
DOUT1
DOUT2
RIN4
DOUT3
-XRI1

C418 220P 50V X7R 0402 /NI
C419 220P 50V X7R 0402 /NI
C420 220P 50V X7R 0402 /NI
C421 220P 50V X7R 0402 /NI
C422 220P 50V X7R 0402 /NI
C423 220P 50V X7R 0402 /NI
C424 220P 50V X7R 0402 /NI
C425 220P 50V X7R 0402 /NI

+3.3V_DUAL
-XRI1
RN44
10K 8P4R 0402 /NI
22 EXT_EVNT0#
Q32
2N3904 SOT23 /NI
D6
1N4148 SMD /NI

WAKE ON LAN

J_COM1
HEADER 2X5 N10 G /NI

RIN1
DOUT2
DOUT1
-XRI1
RIN3
DOUT3
RIN2
RIN4

COM PORT

COM PORT PIN ASSIGNMENT

RN45
22 8P4R 0402
33 STROBEJ
33 ALFJ
33 PARINITJ
33 SLCTINJ
STROBEJ
ALFJ
PARINITJ
SLCTINJ
-STB
AFD
-INIT
-SLIN

RN46
22 8P4R 0402
33 PDR7
33 PDR6
33 PDR5
33 PDR4
PDR7
PDR6
PDR5
PDR4
P_PRD7
P_PRD6
P_PRD5
P_PRD4

RN51
22 8P4R 0402
33 PDR3
33 PDR2
33 PDR1
33 PDR0
PDR3
PDR2
PDR1
PDR0
P_PRD3
P_PRD2
P_PRD1
P_PRD0

+5V
D7
SS12/5817 SMA
C426
0.1UF 16V Y5V 0402 /NI
FOR EMI
R264
2.2K 0402
RN47
2.2K 8P4R 0402
RN48
2.2K 8P4R 0402
RN49
2.2K 8P4R 0402
RN50
2.2K 8P4R 0402

33 SLCTJ
33 ACKJ
33 BUSY
33 PE
33 ERRORJ
SLCTJ
P_PRD7
ACKJ
BUSY
PE
P_PRD4
P_PRD5
P_PRD6
P_PRD3
-STB
P_PRD2
P_PRD1
P_PRD0
ERRORJ
AFD
-INIT
-SLIN

+5V
FOR EMI near R265
EC10
1000P 50V X7R 0402 /NI
R265
SHORT 0805 /NI
IO_GND
R266
SHORT 0805 /NI
IO_GND

J_PRINT1
HEADER 2X13 N26

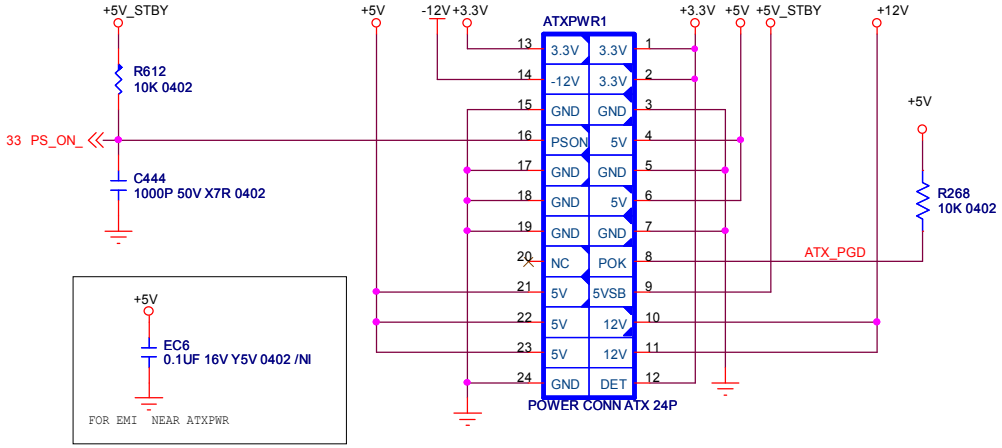
-STB
P_PRD0
P_PRD1
P_PRD2
P_PRD3
P_PRD4
P_PRD5
P_PRD6
P_PRD7
ACKJ
BUSY
PE
SLCTJ
AFD
ERRORJ
-INIT
-SLIN

映泰股份有限公司
BIOSTAR GROUP

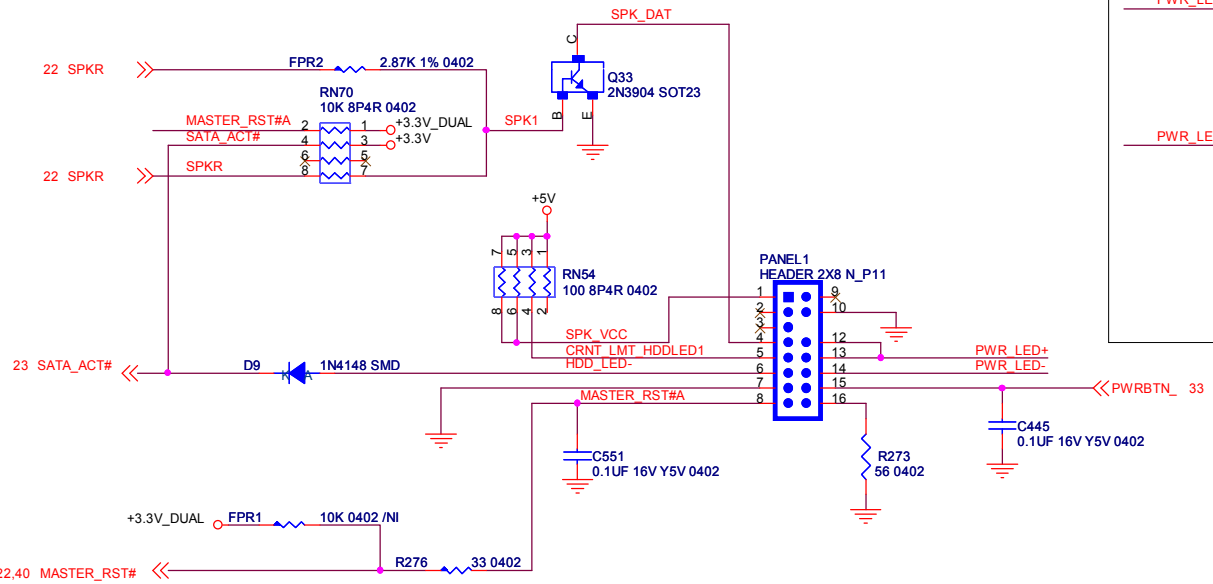
Title
COM & PRINTER CONNECTOR

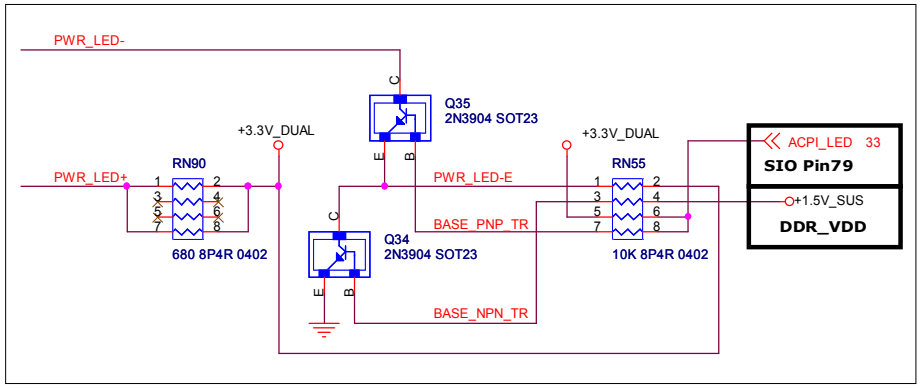
Size	Document Number	Rev
Custom	A78LD-M3S	7.1

Date: Thursday, April 21, 2011 Sheet 36 of 45



LED_D2	LED_D1	MESSAGE
OFF	OFF	ABNORMAL
OFF	ON	MEMORY ERROR
ON	OFF	VGA ERROR
ON	ON	NORMAL



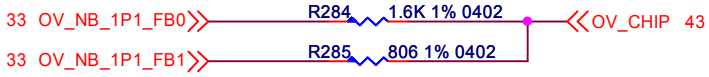


映泰股份有限公司
BIOSTAR GROUP

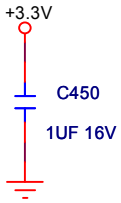
Title: ATX PWR / FRONT PANEL

Size	Document Number	Rev
Custom	A78LD-M3S	7.1

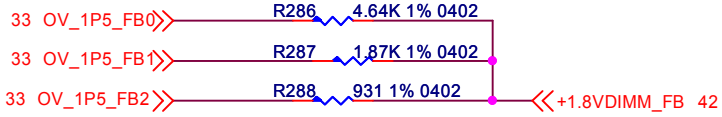
Date: Thursday, April 21, 2011 Sheet 37 of 45



CORE VOLTAGE	OV_NB_1P1_FB1	OV_NB_1P1_FB0
+1.240V	1	1
+1.295V	1	0
+1.349V	0	1
+1.404V	0	0



DUAL +3.3V



+1.5VDIMM_FB	VDIMM0	VDIMM1	VDIMM2
Default 1.509V	1	1	1
1.547V	0	1	1
1.605V	1	0	1
1.644V	0	0	1
1.703V	1	1	0
1.742V	0	1	0
1.799V	1	0	0
1.838V	0	0	0

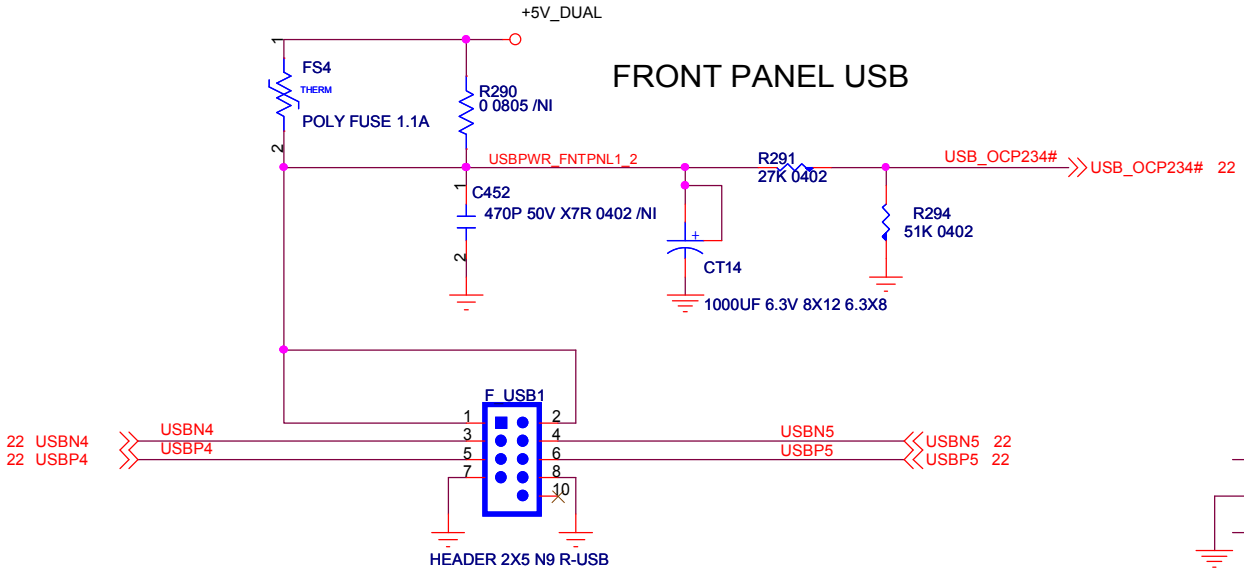
0V_VCORE	OV_VCORE0	OV_VCORE1
Default V_CPU	1	1
+3.3%	0	1
+6.6%	1	0
+10%	0	0

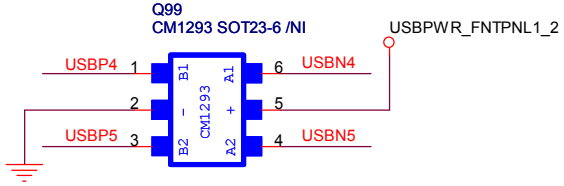
映泰股份有限公司
BIOSTAR GROUP

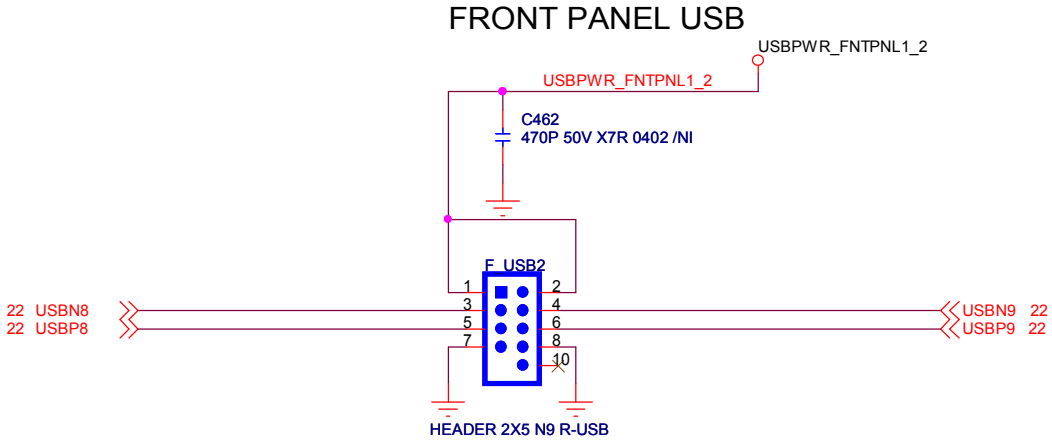
Title: OVER VOLTAGE

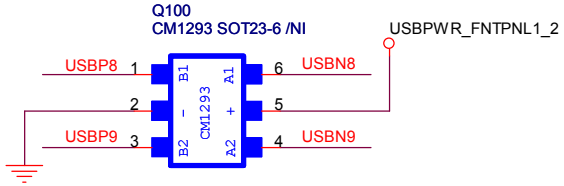
Size: Custom | Document Number: A78LD-M3S | Rev: 7.1

Date: Thursday, April 21, 2011 | Sheet 38 of 45





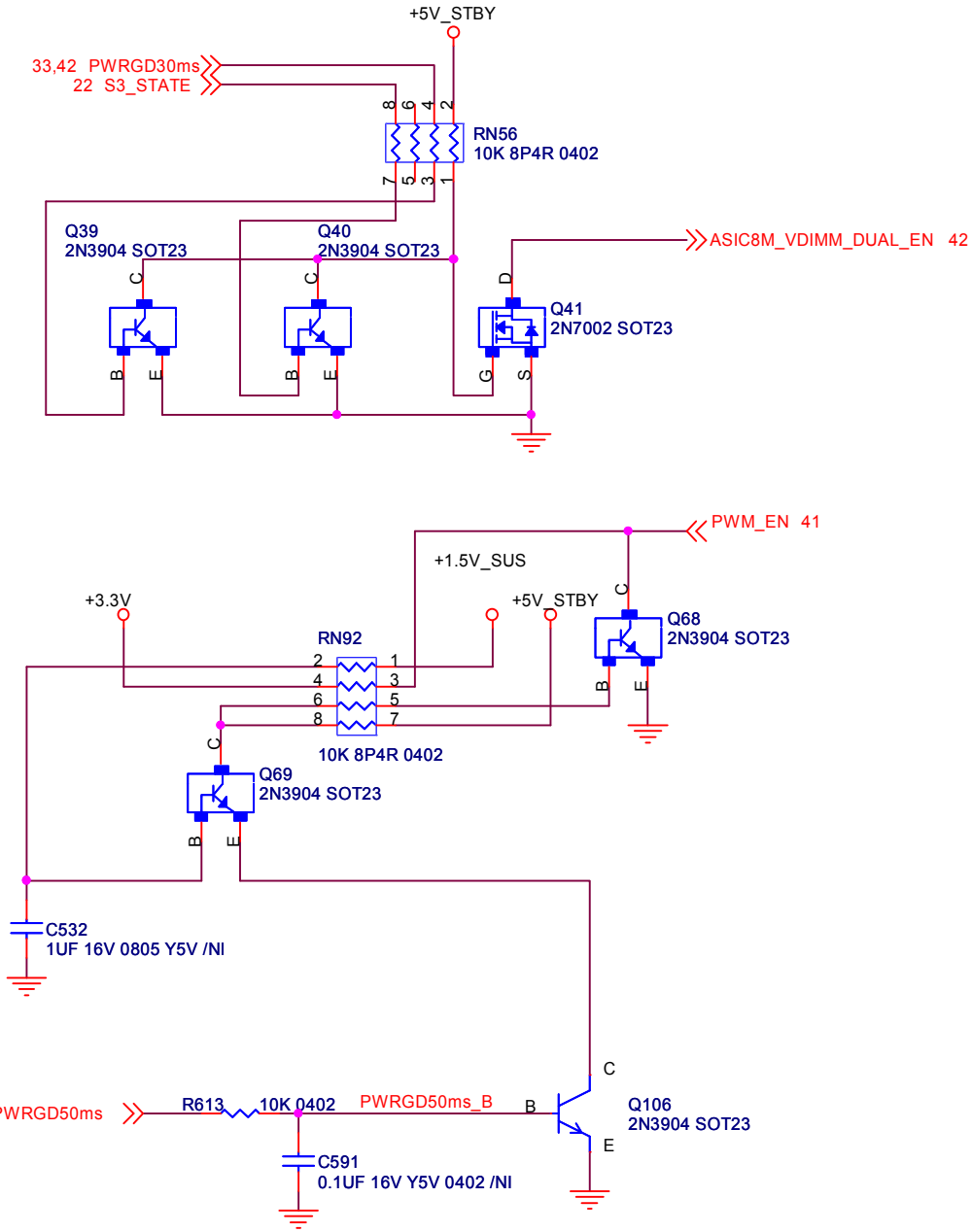


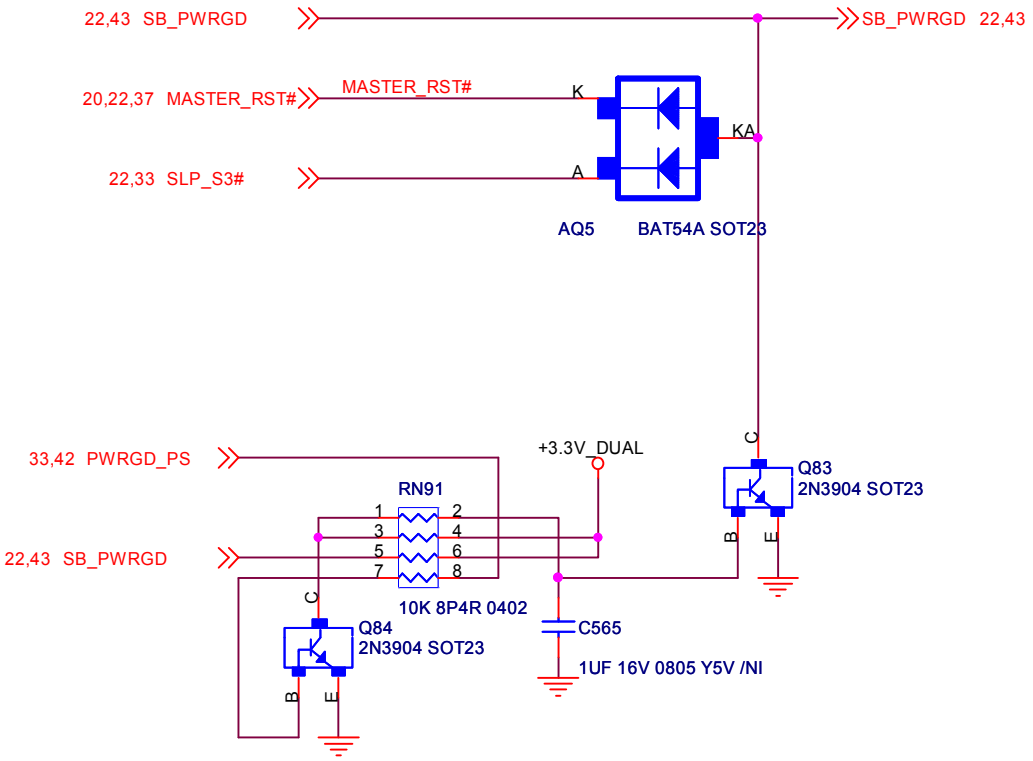


映泰股份有限公司
BIOSTAR GROUP

Title	FRONT USB	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 39 of 45	

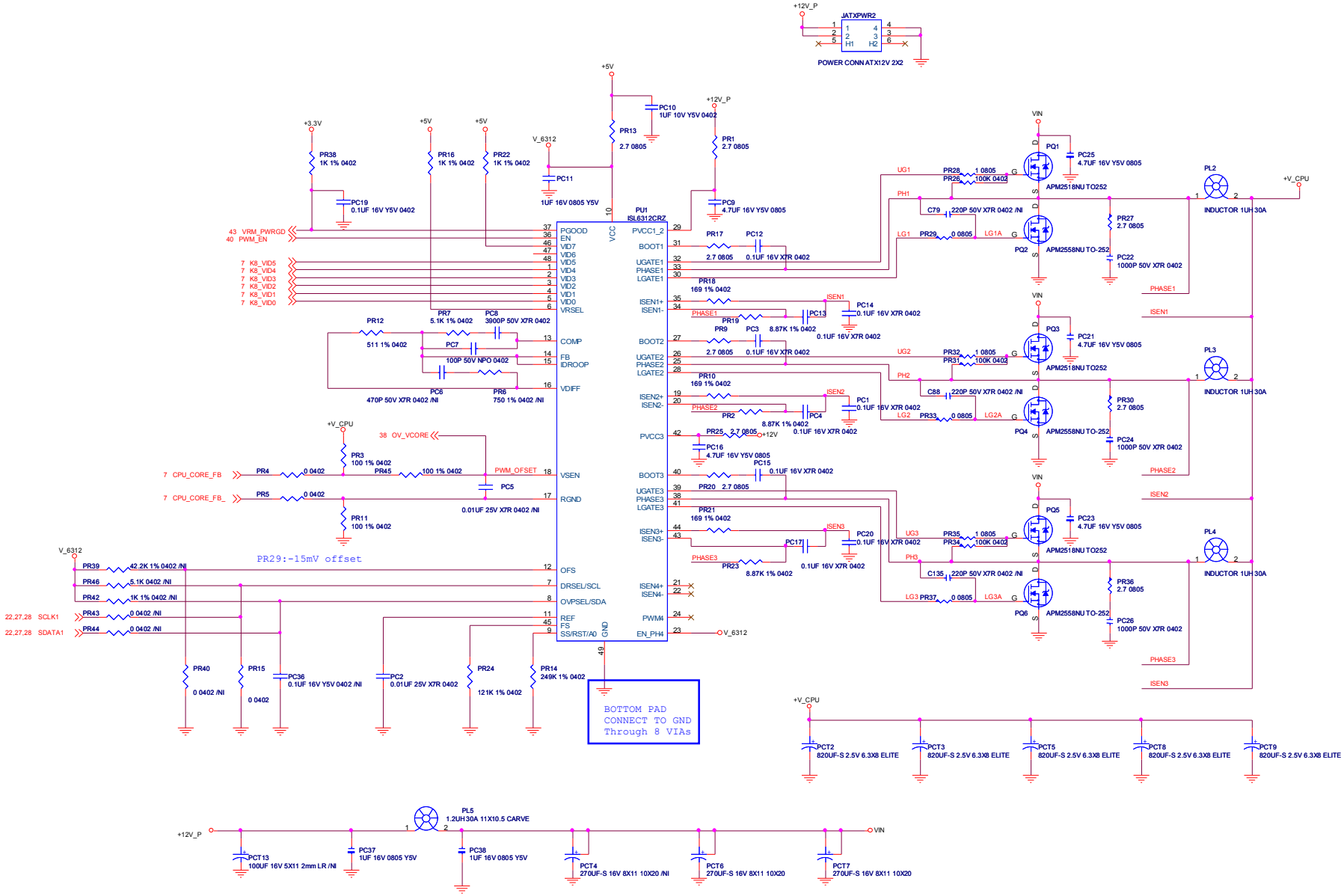
ATHLON64 POWER GOOD & ENABLES CIRCUIT





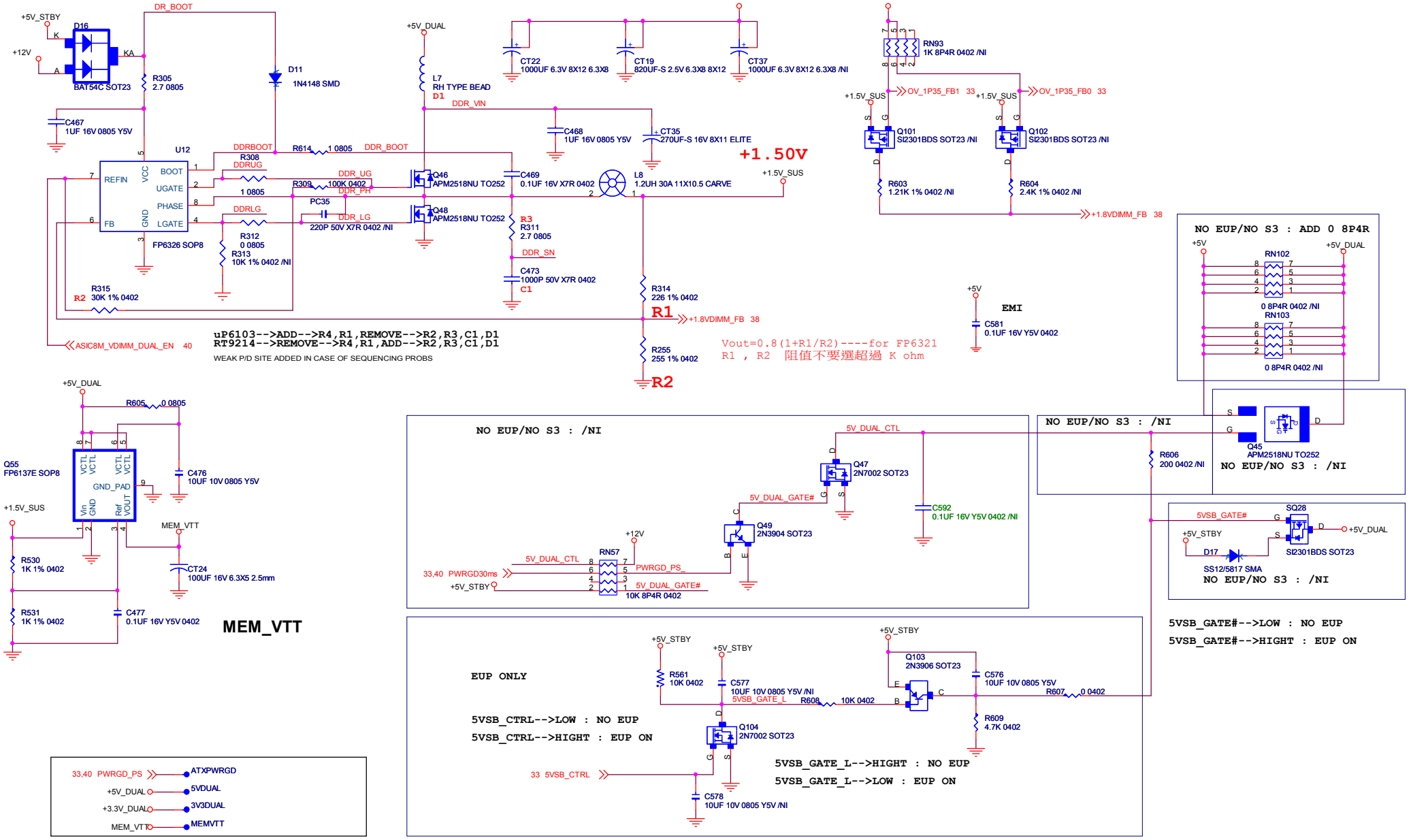
映泰股份有限公司
BIOSTAR GROUP

Title	PWR GD / MISC POWER	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 40 of 45	



映泰股份有限公司
BIOSTAR GROUP

Title	VCORE POWER SUPPLY	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 41 of 45	



映泰股份有限公司
BIOSTAR GROUP

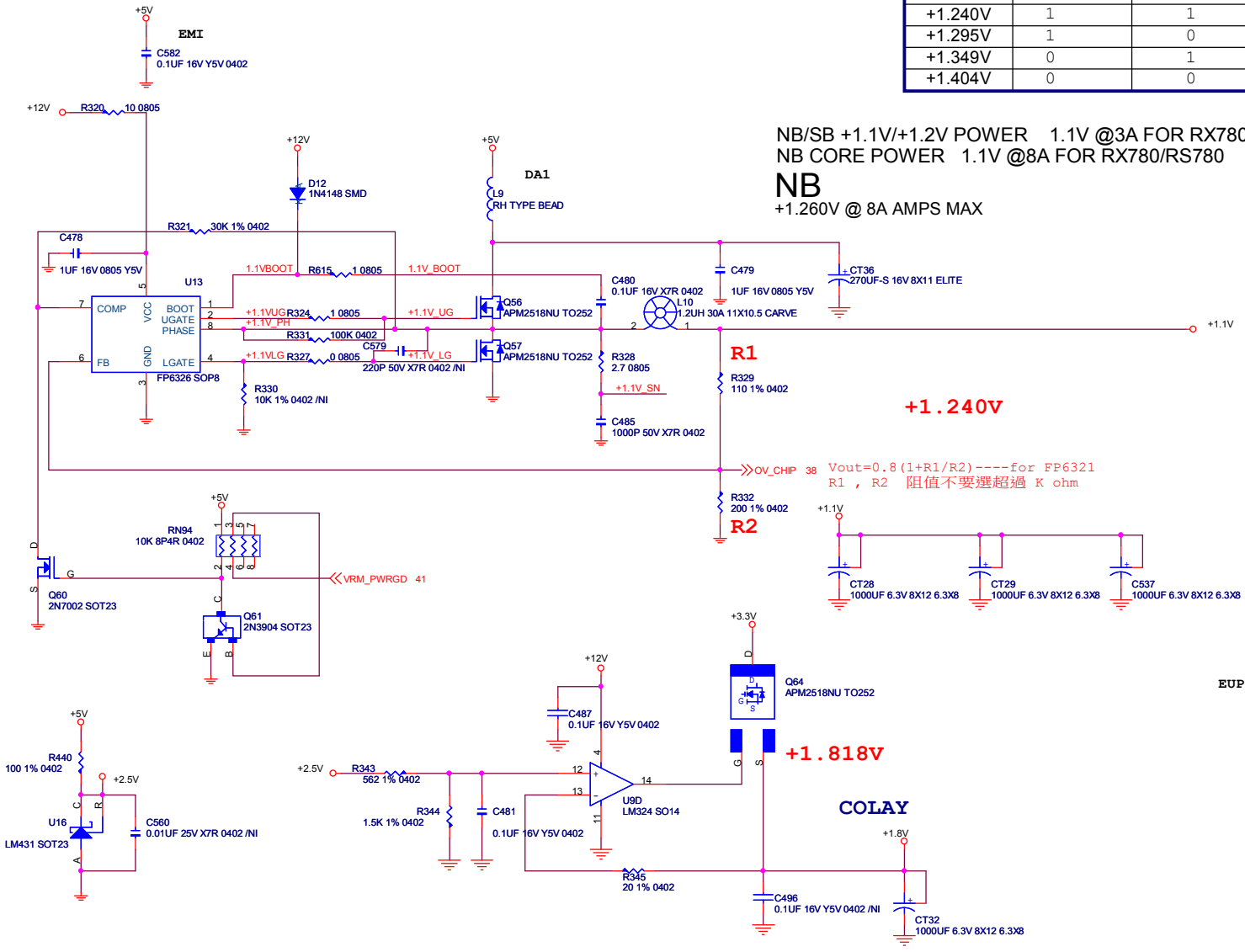
Title	MEMORY POWER	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 42 of 45	

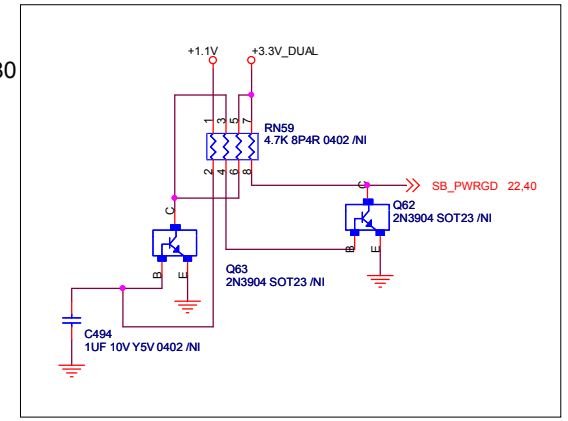
CORE VOLTAGE	OV_NB_1P1_FB1	OV_NB_1P1_FB0
+1.240V	1	1
+1.295V	1	0
+1.349V	0	1
+1.404V	0	0

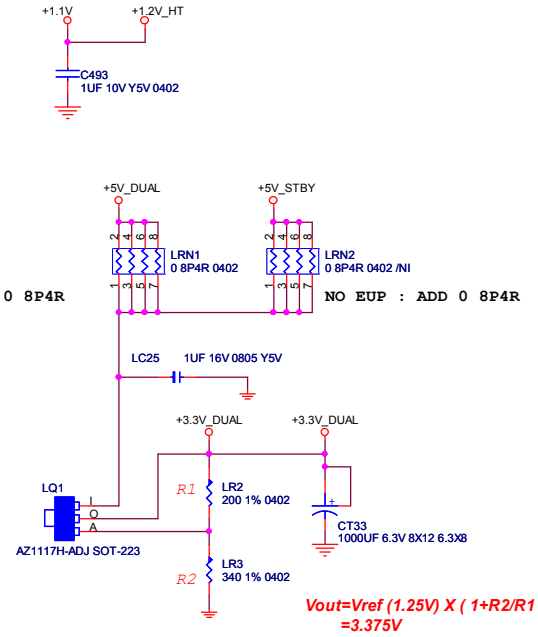
NB/SB +1.1V/+1.2V POWER 1.1V @3A FOR RX780/RS780
NB CORE POWER 1.1V @8A FOR RX780/RS780

NB

+1.260V @ 8A AMPS MAX

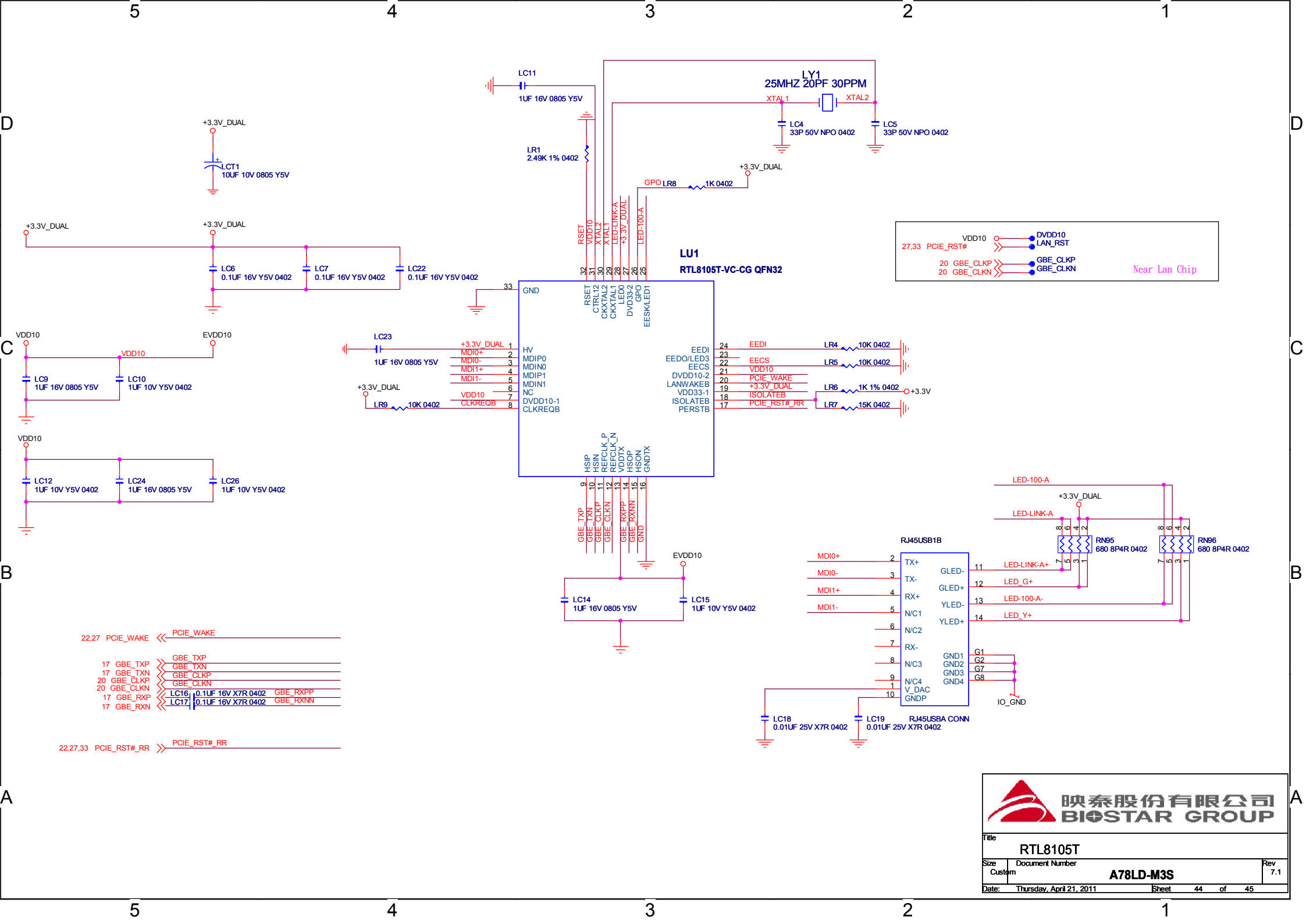






映泰股份有限公司
BIOSTAR GROUP

Title	NB/SB CORE POWER	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 43 of 45	



映泰股份有限公司
BIOSTAR GROUP

Title	RTL8105T	
Size: Custom	Document Number: A78LD-M3S	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 44 of 45	

(BAT1)

電池

3V BATTERY SONY

JUSBV1(1_2)
JUMPER 2P R /NI

JUSBV2(1_2)
JUMPER 2P R /NI

JCMOS1(1_2)
JUMPER 2P B

(Y2)
X'TAL WIRE

(U5)

FLASH ROM

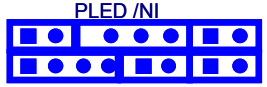
SPI MX25L8005 DIP

New JPANEL1
JPANEL1 2*8

PANEL1(9_10)
HEADER 1X2 /NI

PANEL1(15_16)
HEADER 1X2 /NI

PANEL1(11_14)
PLED /NI



PANEL1(1_4)
SPK /NI

PANEL1(7_8)
RST /NI

PANEL1(5_6)
HLED /NI

LB1

LB1

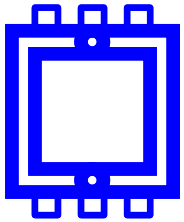
A780L M2G+-LB1 /NI

PCB

PCB

A78LD-M3S VER7.1

(CPU1)



AM2RM-B

(PCB)

泡棉

POLON 235X182

(U1)

北橋散熱片

NBHS-A74GC

(U4)

南橋散熱片

SB SMALL-AMD

映泰股份有限公司
BIOSTAR GROUP

Title	**BOM**	
Size: Custom	Document Number: **A78LD-M3S**	Rev: 7.1
Date: Thursday, April 21, 2011	Sheet 45 of 45	