

PAGE	CONTENTS
1	COVER
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	CLOCK DISTRIBUTION
5	REVISION HISTROY
6-10	SKT 941 K8 AM3 CPU
11	CPU DECOUPLING
12	DDR CLK BYPASS
13	DDR3 DIMM A1
14	DDR3 DIMM B1
15	ADO FUNCTION
16	RS780-HT LINK
17	RS780-PCIE
18	RS780-SYSTEM
19	RS780-PWOER&SBD_MEM
20	CLOCK GEN
21	SB710-PCIE/PCI/CPU/LPC
22	SB710-ACPI/GPIO/USB/AUD
23	SB710-SATA/IDE/HWM/SPI
24	SB710-POWER&DECOUPLING
25	SB710-STRAPS
26	CRT
27	PCI-E 16X SLOT
28	PCI SLOT
29	NONE
30	USB CONN
31	CODEC VT1708B/ALC662
32	AUDIO CONNECTOR
33	SUPER I/O ITE8728
34	FAN CONTROL
35	PS2 CONN
36	COM&LPT CONNECTOR
37	ATX PWR / FRONT PANEL / LED
38	OVER VOLTAGE IC
39	FRONT USB
40	PWRGD / MISC DC-DC
41	VCC_CORE DC-DC CONVER
42	MEMORY POWER
43	NB/SB CORE POWER
44	Realtek RTL8105T
45	BOM

A78LD-M3S (RS780&SB710)

REV 7.1

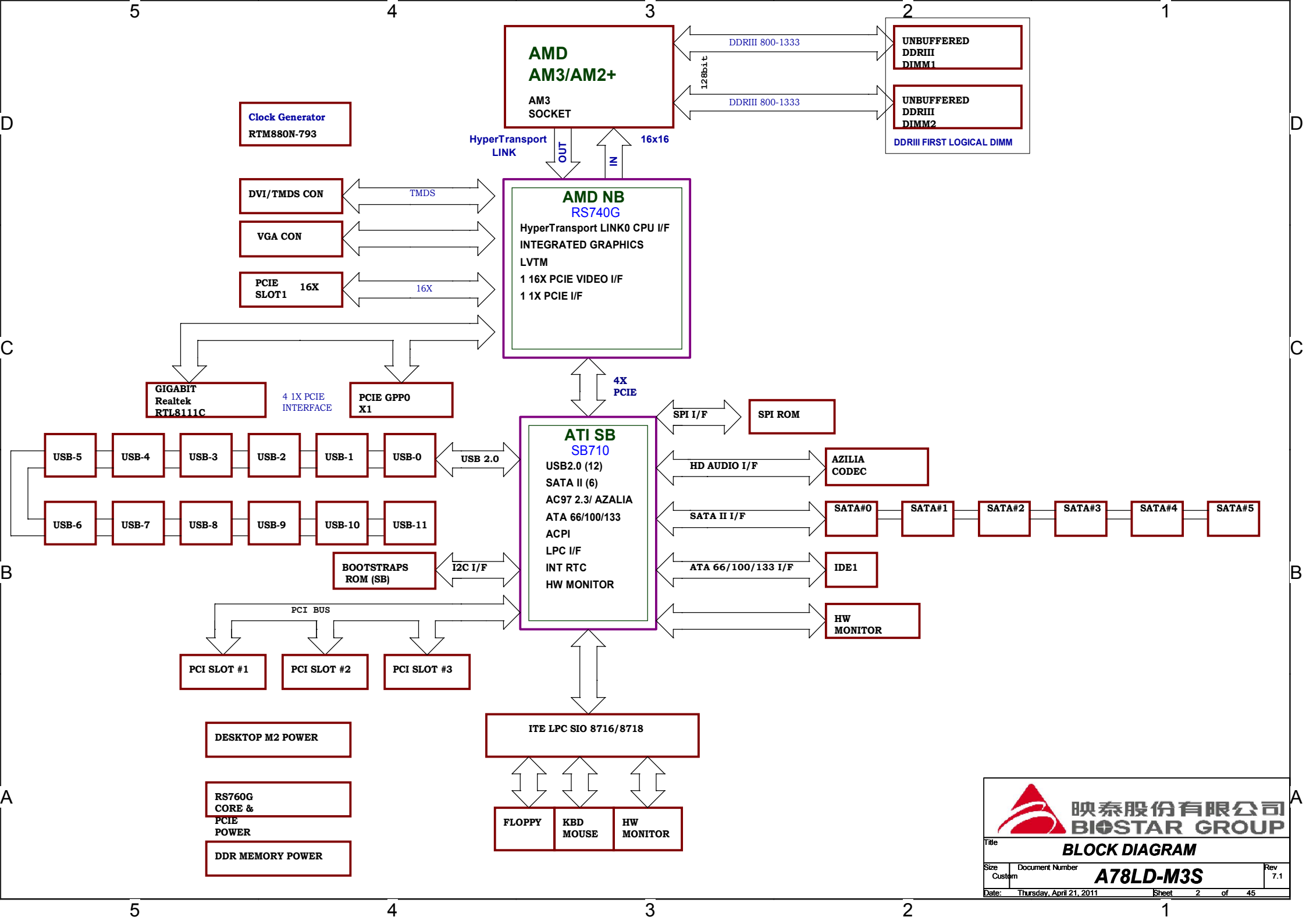
**DDR3 X 2 Dual channel , PCI-Ex16 X 1 , PCI X 1 ,
Realtek 10/100 PCI-E Lan , AMD AM3**

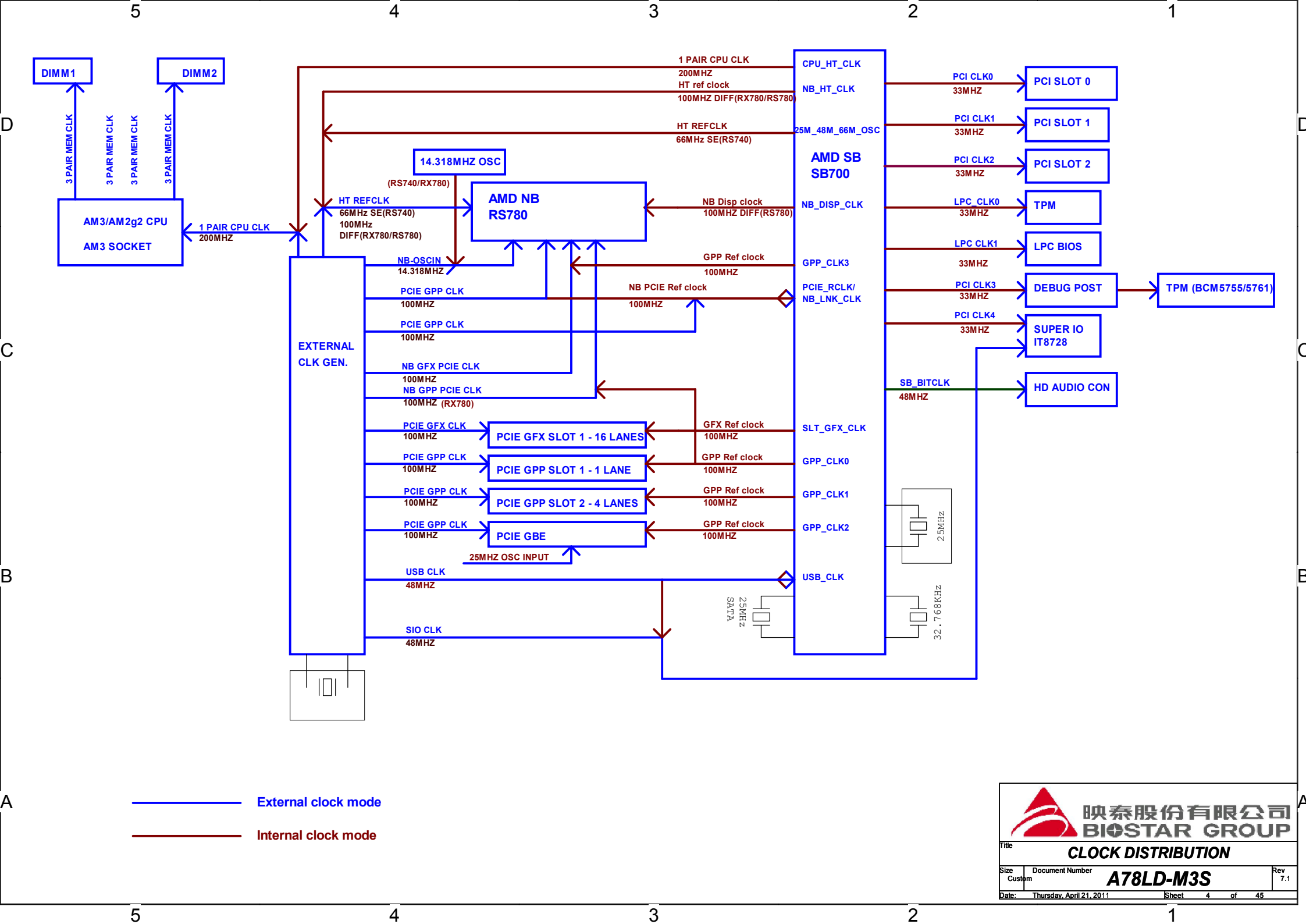
DATE :2011/04/21

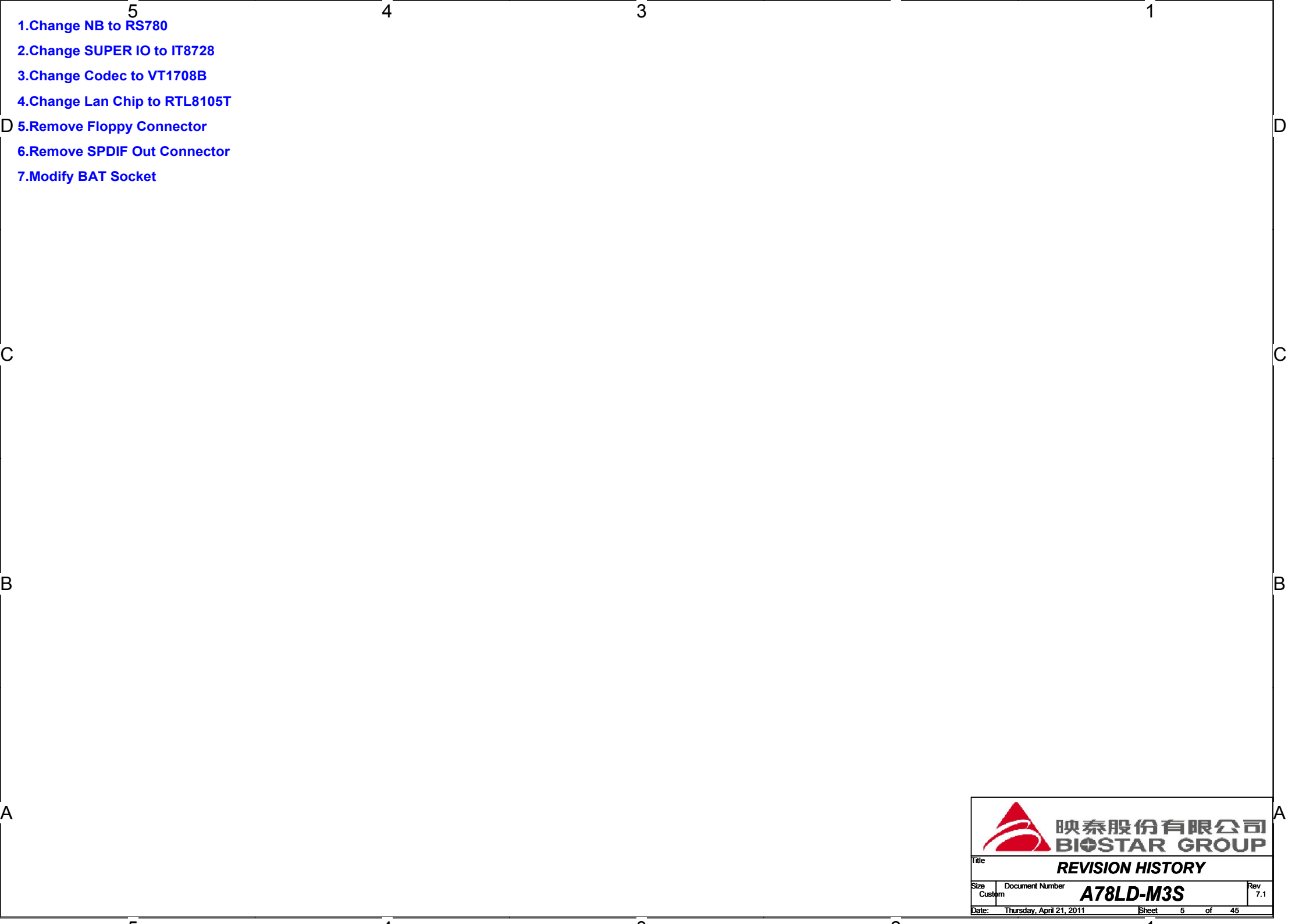
『BIOSTAR'S PROPRIETARY INFORMATION』

『Any unauthorized use, reproduction, duplication,
or disclosure of this document will be subject to
the applicable civil and/or criminal penalties.』


			
映泰股份有限公司 BIOSTAR GROUP			
Title COVER			
Size Custom	Document Number A78LD-M3S		Rev 7.1
Date: Thursday, April 21, 2011			
Sheet		1 of 45	







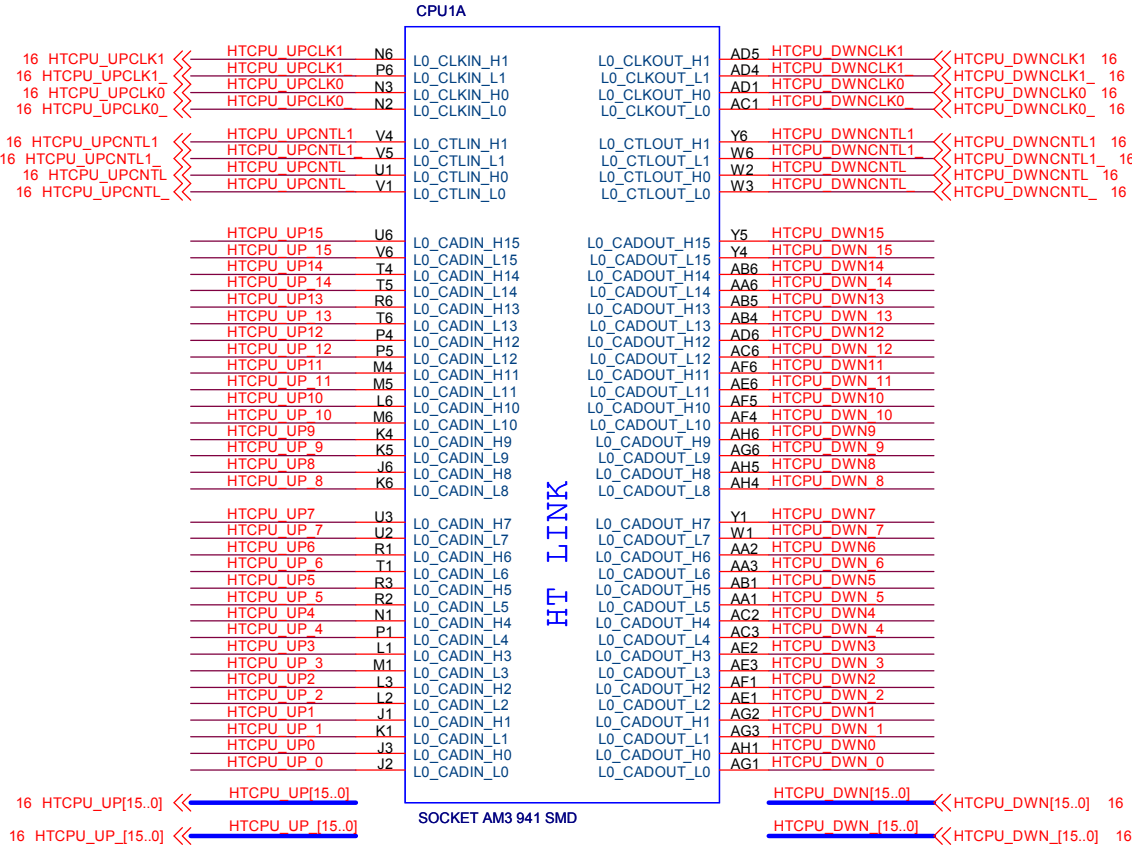
- 1.Change NB to RS780
- 2.Change SUPER IO to IT8728
- 3.Change Codec to VT1708B
- 4.Change Lan Chip to RTL8105T
- 5.Remove Floppy Connector
- 6.Remove SPDIF Out Connector
- 7.Modify BAT Socket

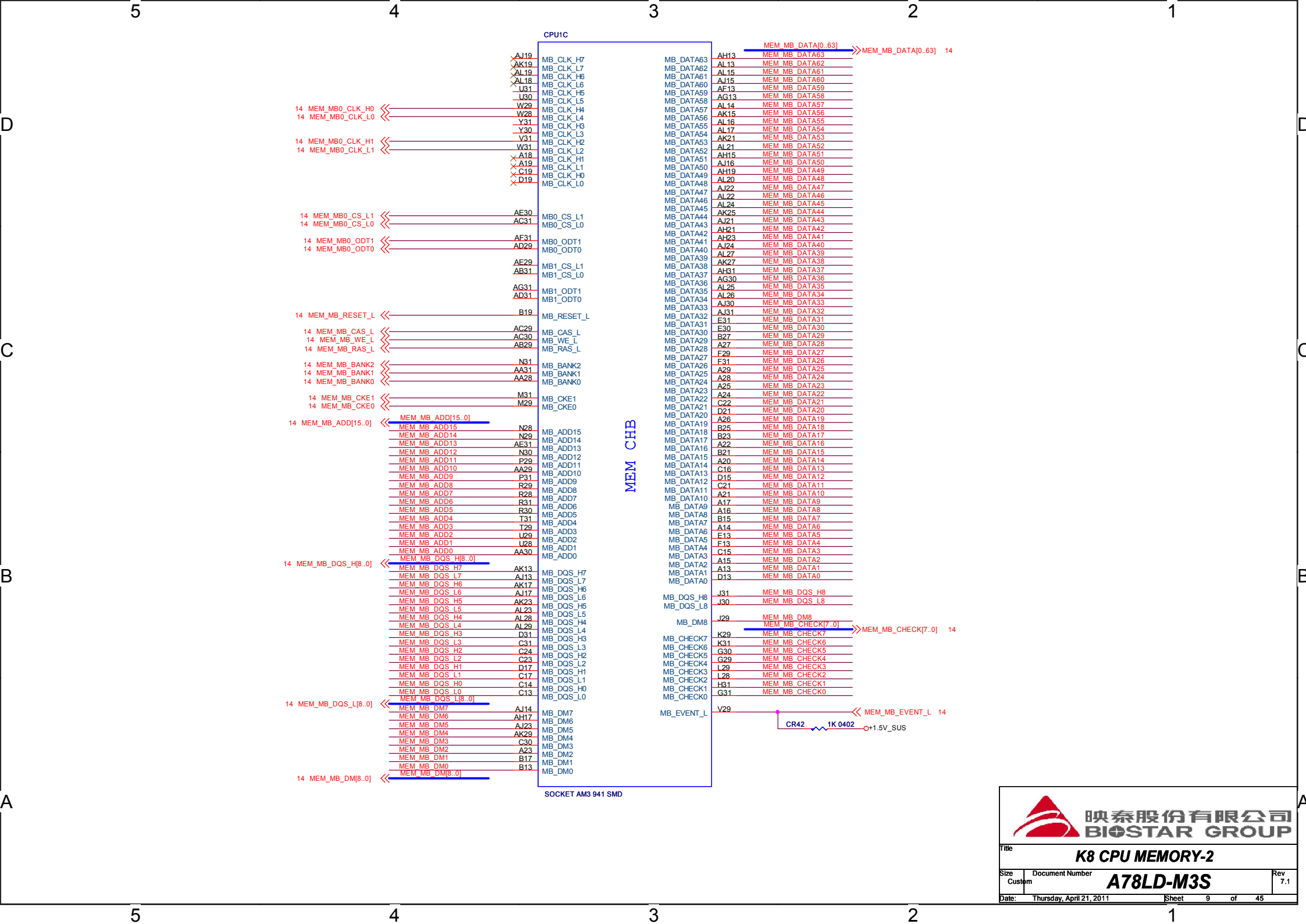


映泰股份有限公司
BIOSTAR GROUP

Title			REVISION HISTORY		
Size	Document Number	A78LD-M3S			Rev
Custom					7.1
Date:	Thursday, April 21, 2011			Sheet	5 of 45

HyperTransport



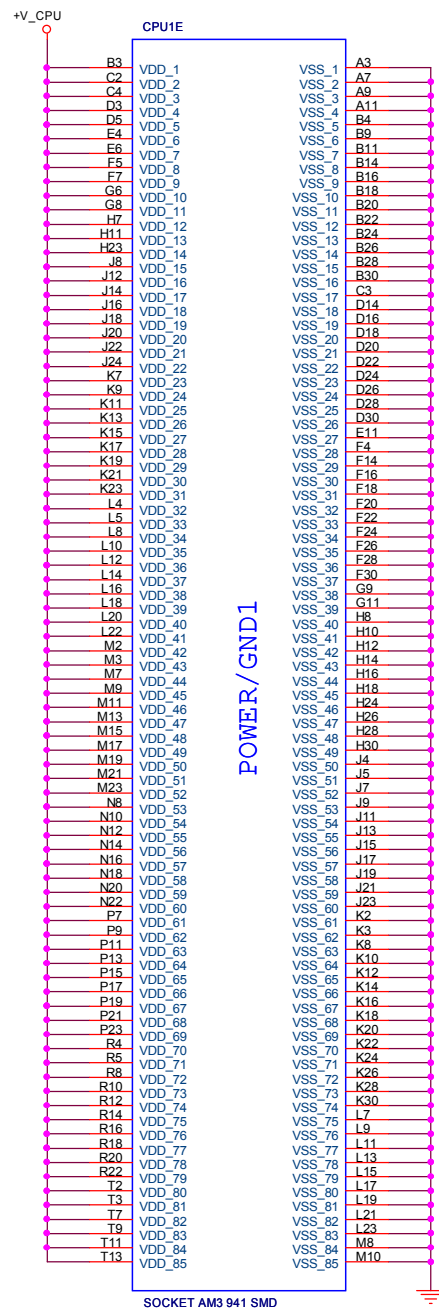


D

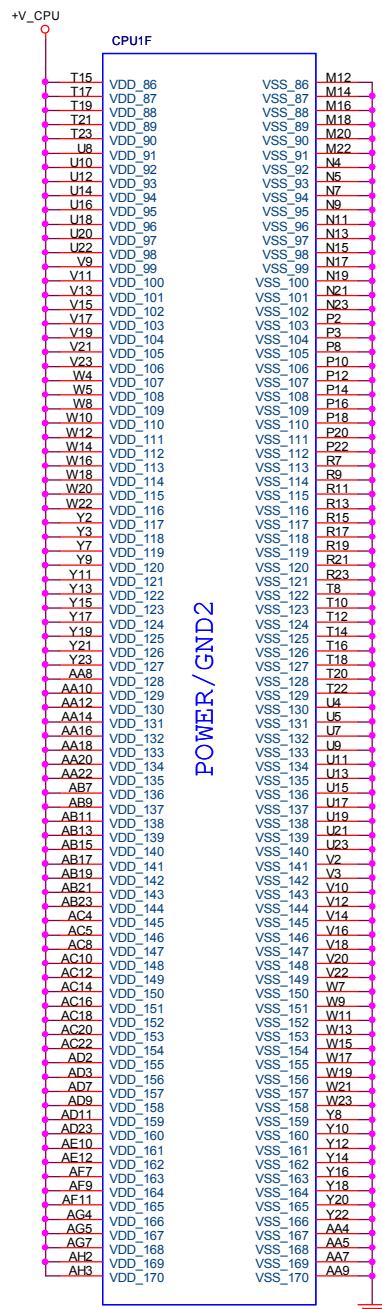
C

B

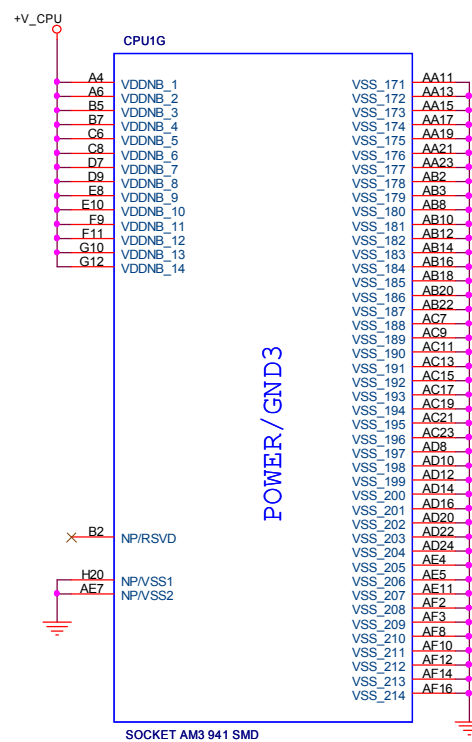
A



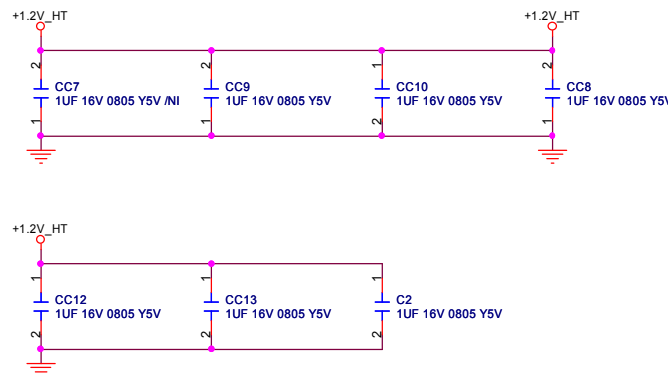
SOCKET AM3 941 SMD



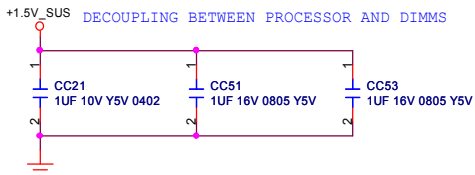
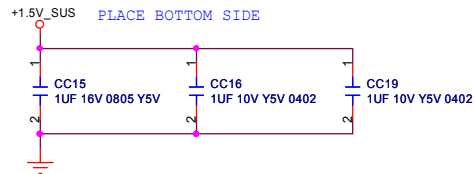
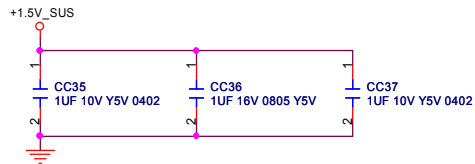
SOCKET AM3 941 SMD



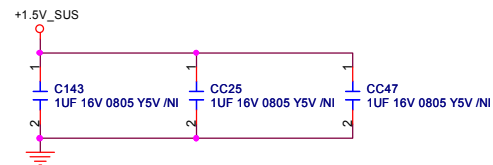
SOCKET AM3 941 SMD



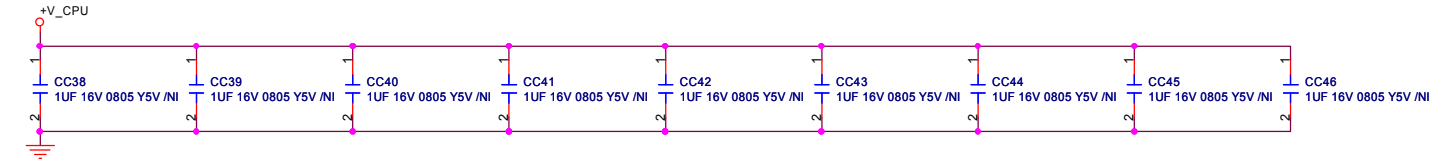
D



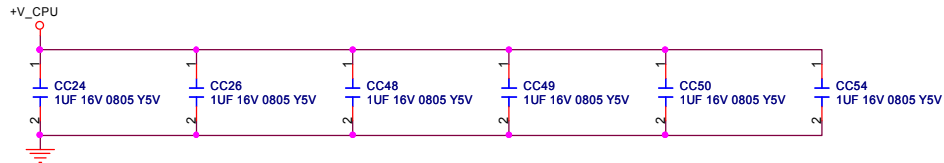
C



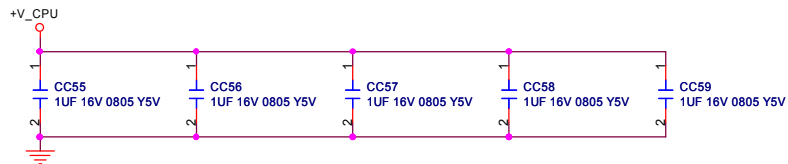
Bottom side



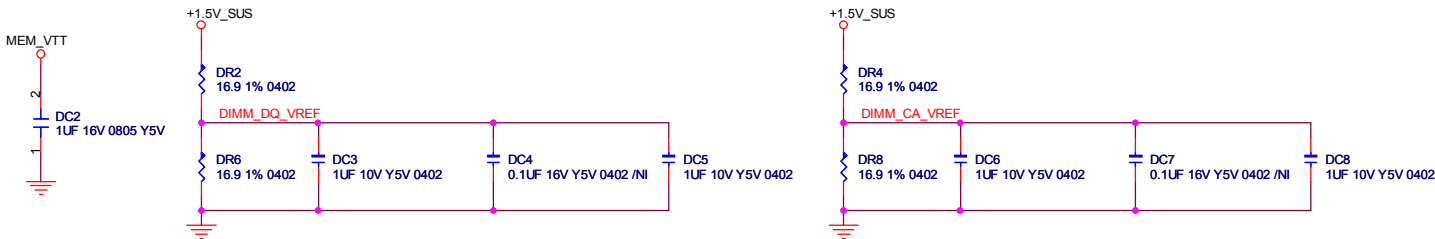
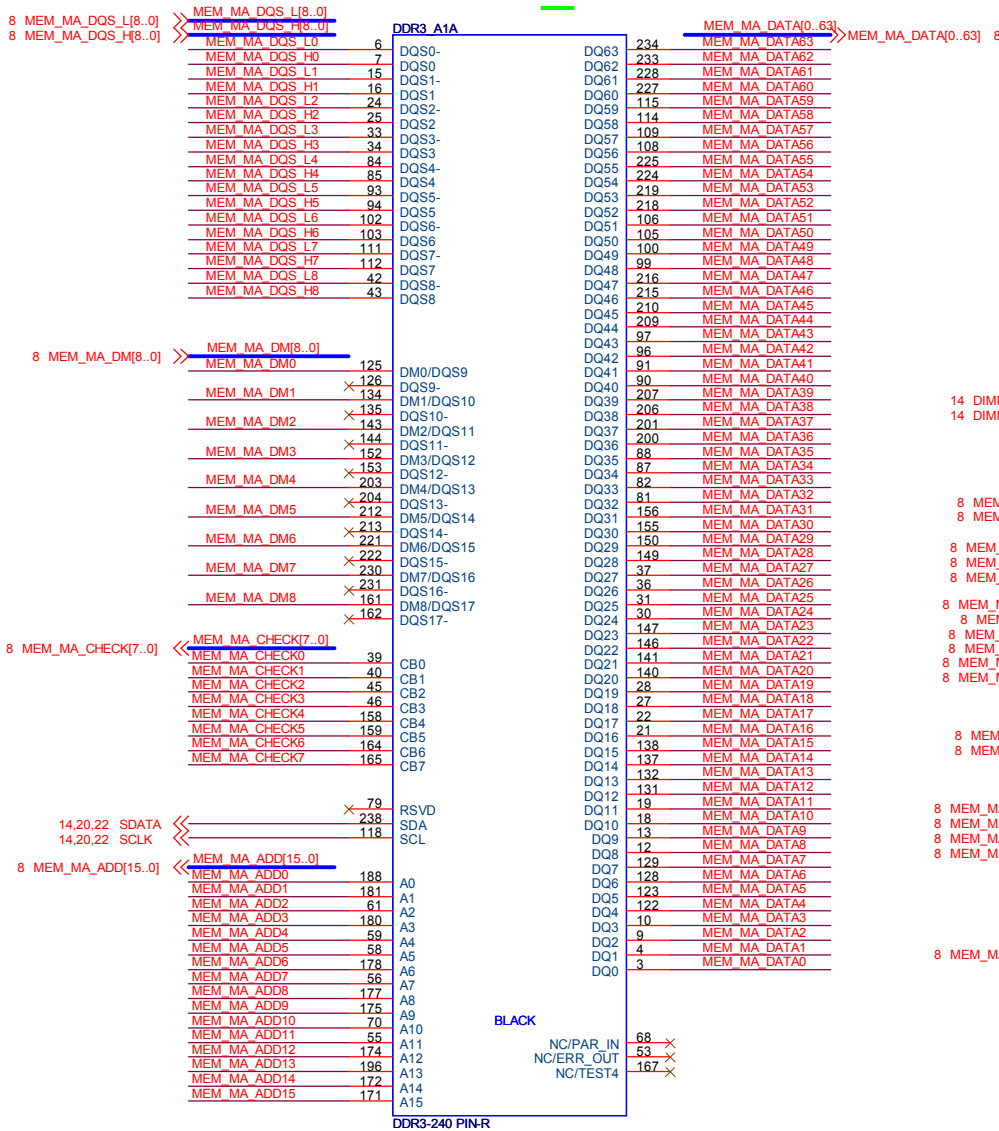
B



A



DDR3_A1



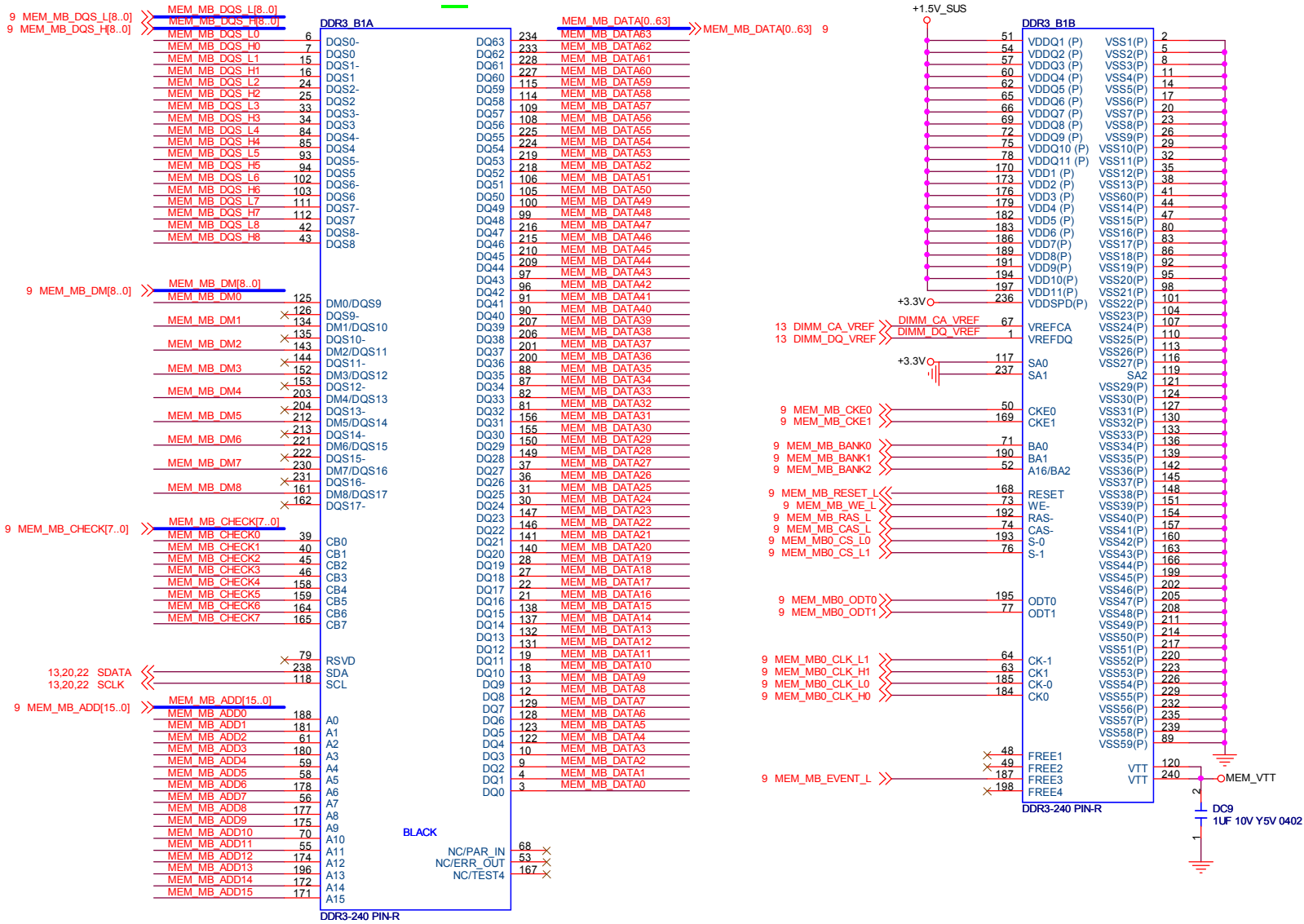
映泰股份有限公司
BIOSTAR GROUP

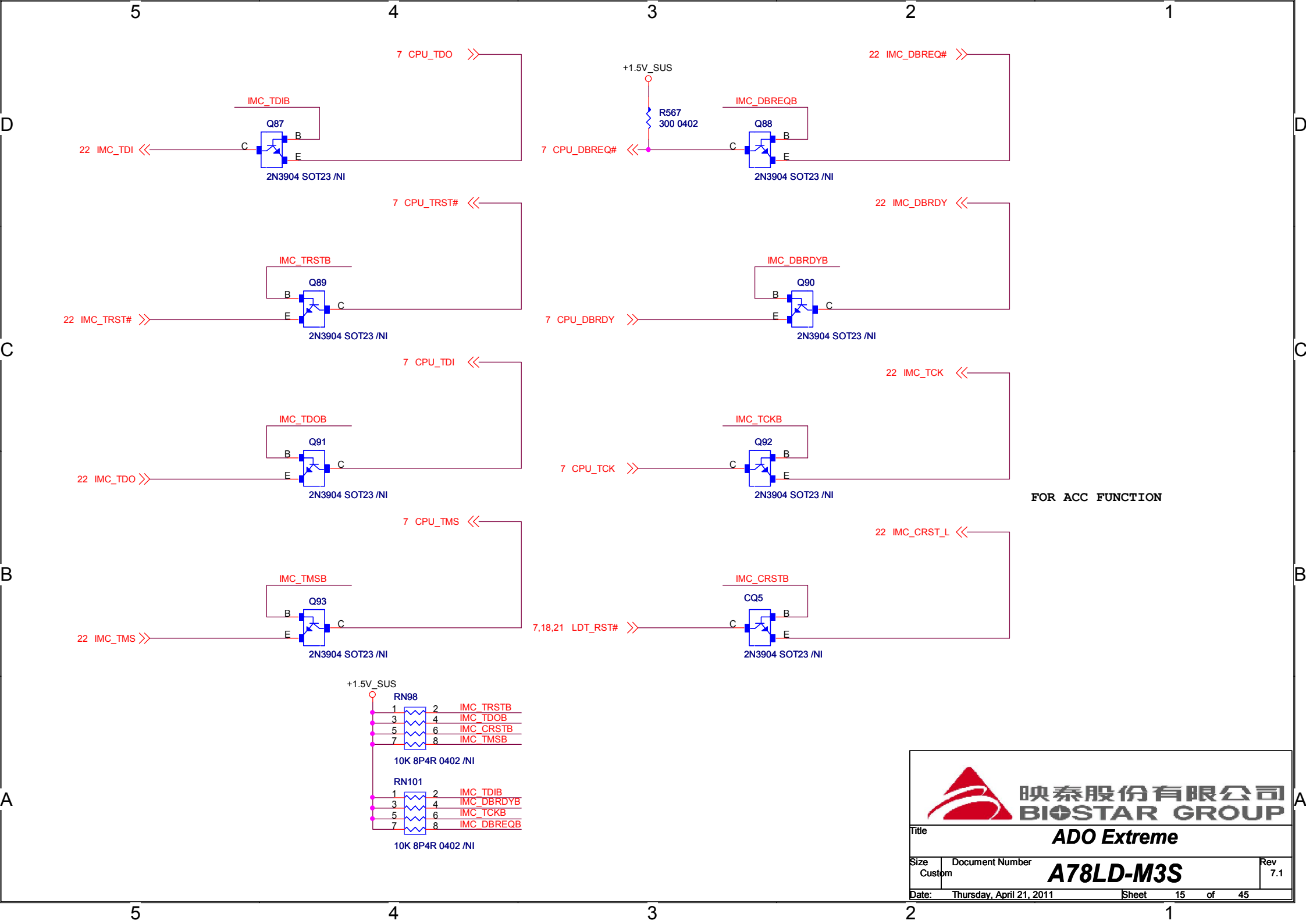
Title: **DDR DIMM-1**

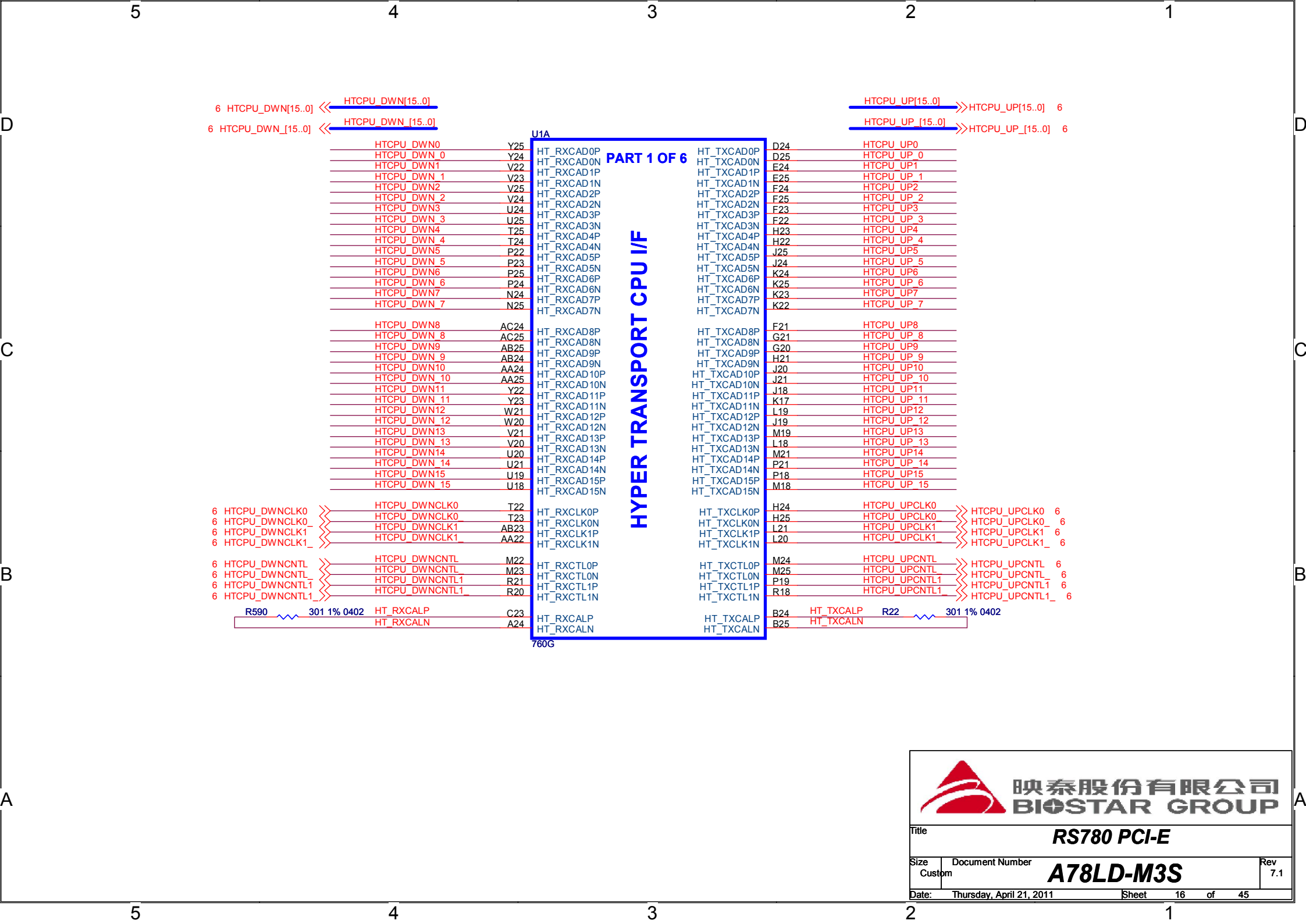
Size: Custom Document Number: **A78LD-M3S** Rev: 7.1

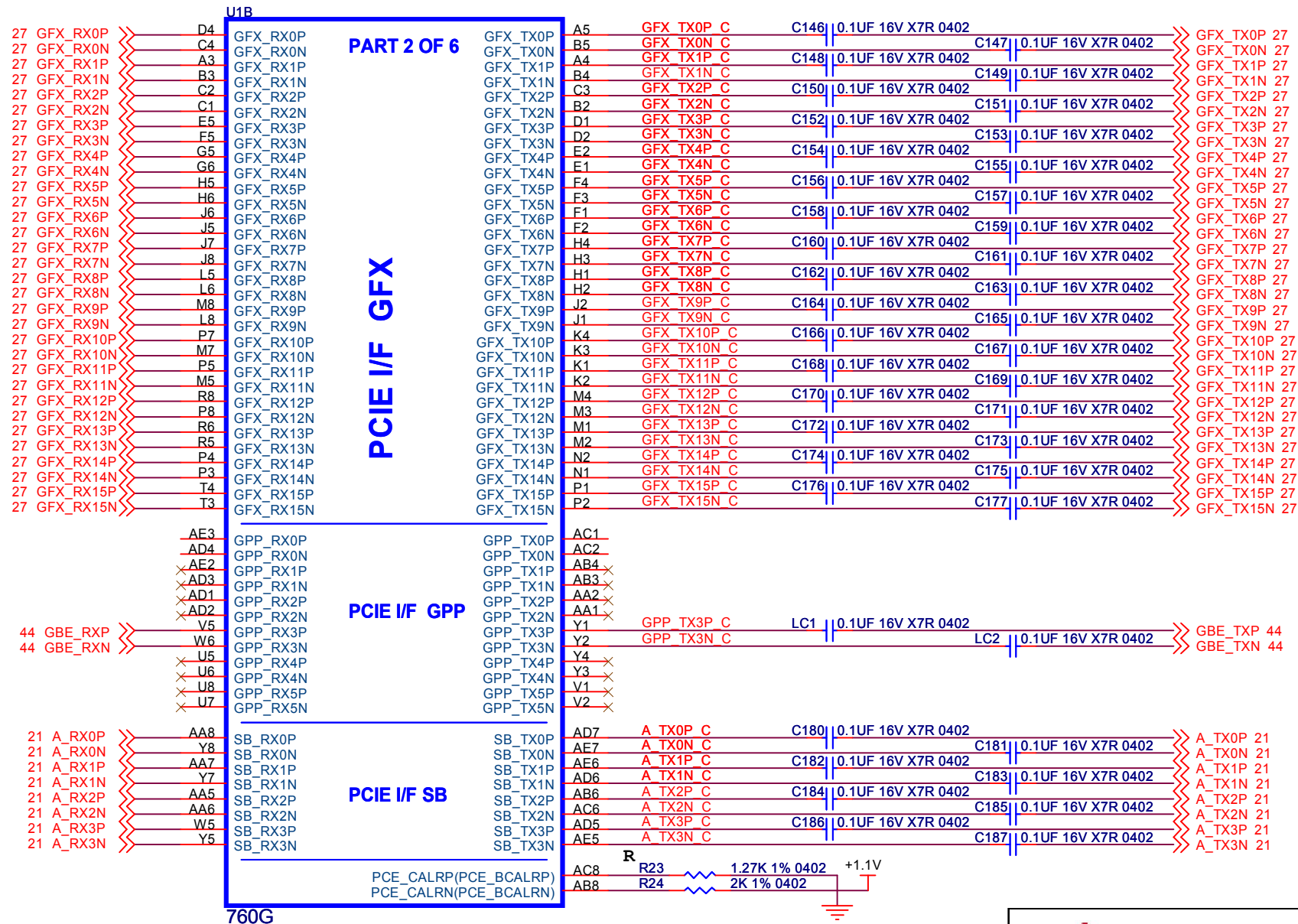
Date: Thursday, April 21, 2011 Sheet: 13 of 45

DDR3_B1

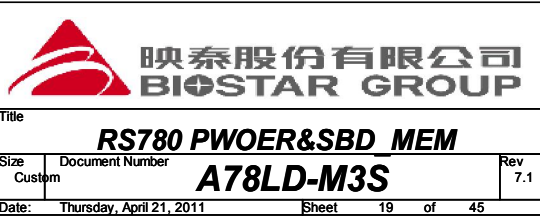


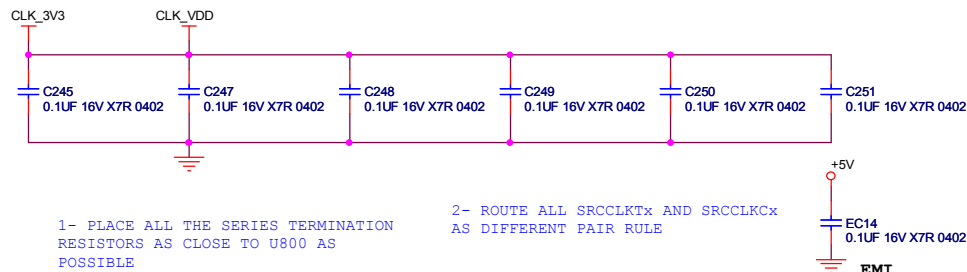






Title			RS780 PCI-E	
Size	Document Number	A78LD-M3S		Rev
Custom				7.1
Date:	Thursday, April 21, 2011	Sheet	17	of 45



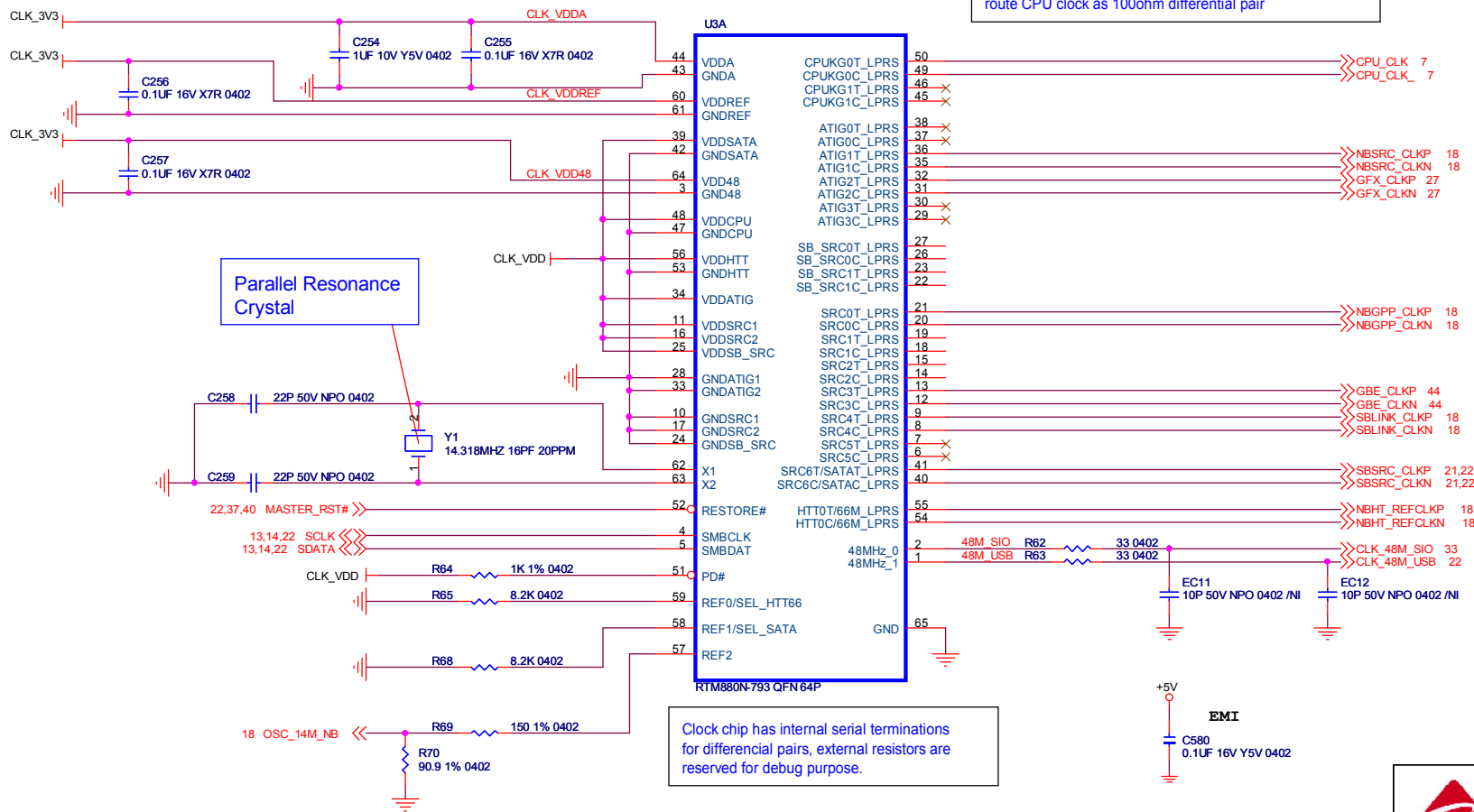


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Parallel Resonance Crystal

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

SEL_HTT66	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock

* default

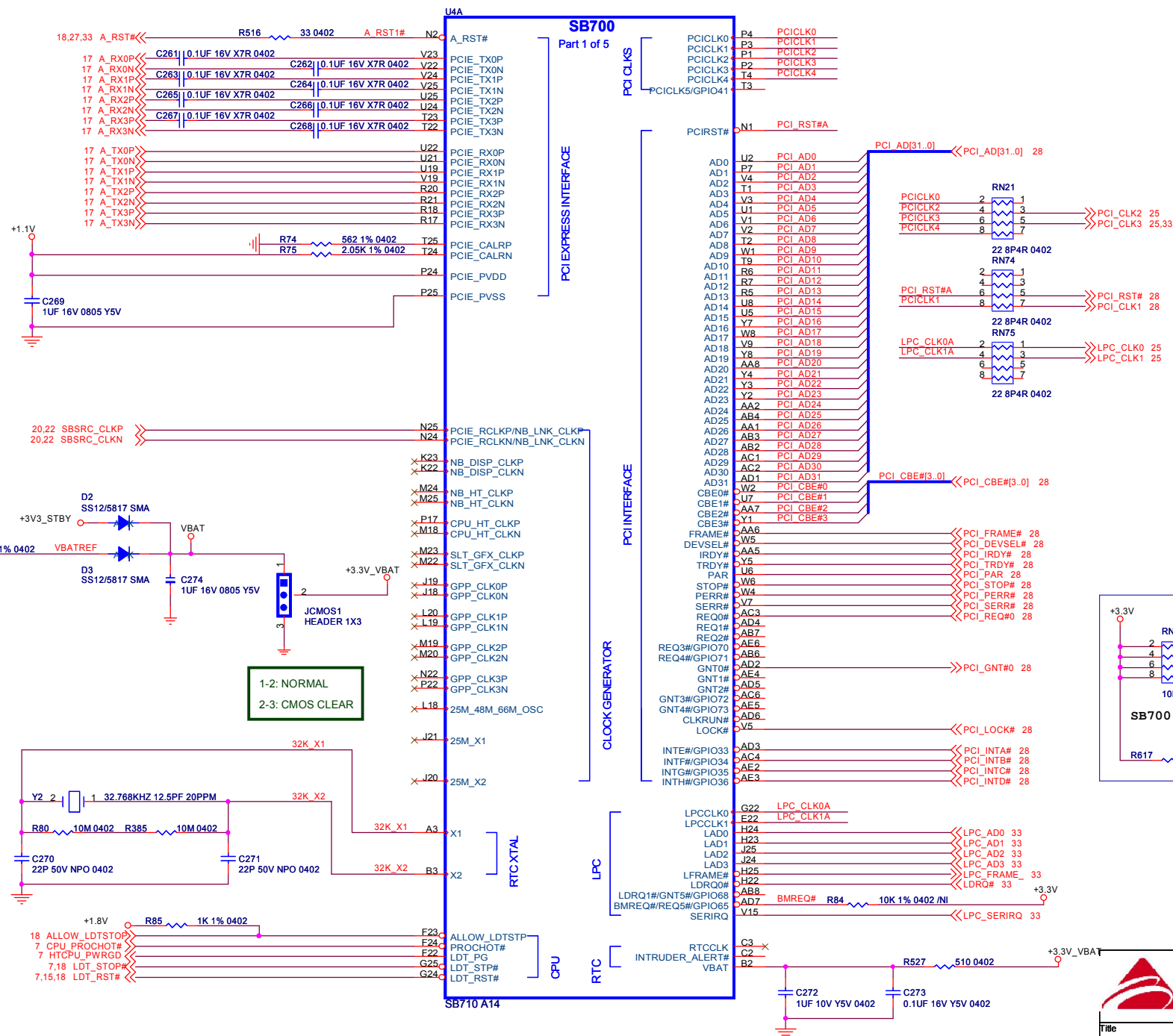
Title			
CLOCK GEN			
Size	Document Number	Rev	
Custom	A78LD-M3S	7.1	
Date:	Thursday, April 21, 2011	Sheet	20 of 45

D

C

B

A

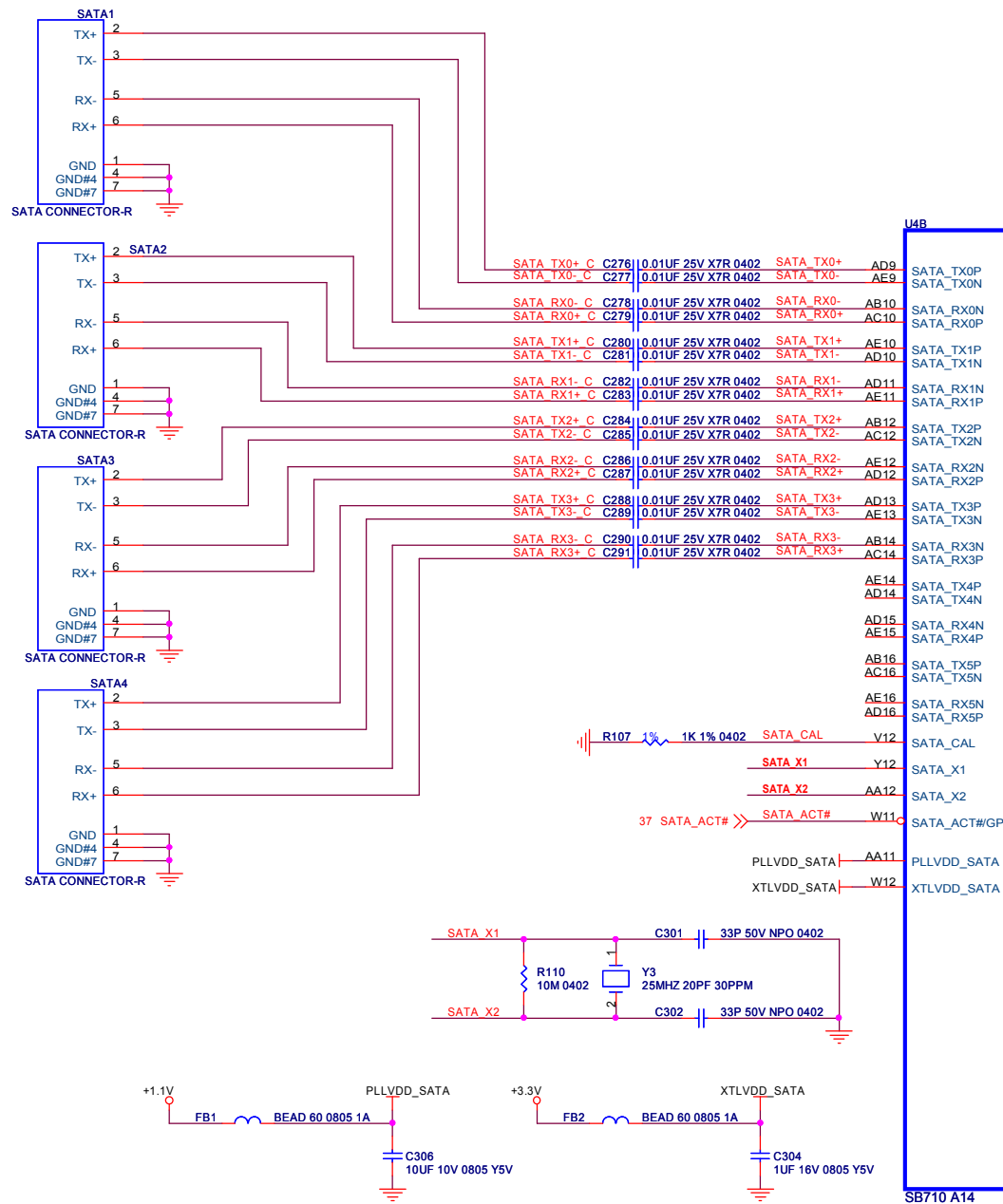


D

C

B

A



U4B

SB700
Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR

SB710 A14

IDE_IORDY AA24

IDE_IRQ AA25

IDE_A0 Y22

IDE_A1 AB23

IDE_A2 Y23

IDE_DACK# AB24

IDE_DRQ AD25

IDE_IOR# AC25

IDE_IOW# AC24

IDE_CS1# Y25

IDE_CS3# Y24

IDE_D0/GPIO15 AD24

IDE_D1/GPIO16 AD23

IDE_D2/GPIO17 AE22

IDE_D3/GPIO18 AC22

IDE_D4/GPIO19 AD21

IDE_D5/GPIO20 AE20

IDE_D6/GPIO21 AB20

IDE_D7/GPIO22 AD19

IDE_D8/GPIO23 AC20

IDE_D9/GPIO24 AD20

IDE_D10/GPIO25 AE21

IDE_D11/GPIO26 AB22

IDE_D12/GPIO27 AD22

IDE_D13/GPIO28 AE23

IDE_D14/GPIO29 AC23

IDE_D15/GPIO30

SPI ROM

HW MONITOR

SPI_DI/GPIO12 G6 SPI_DATAIN

SPI_DO/GPIO11 D2 SPI_DATAOUT

SPI_CLK/GPIO47 D1 SPI_CLK

SPI_HOLD#/GPIO31 E4 SPI_CS#

SPI_CS1#/GPIO32 E3

LAN_RST#/GPIO13 U15

ROM_RST#/GPIO14 J1

FANOUT0/GPIO3 M8

FANOUT1/GPIO48 M5

FANOUT2/GPIO49 M7

FANIN0/GPIO50 P5

FANIN1/GPIO51 P8

FANIN2/GPIO52 R8

TEMP_COMM C6 TEMP_COMM R108 10K 1% 0402

TEMPINO/GPIO61 B6

TEMPIN1/GPIO62 A6

TEMPIN2/GPIO63 A5

TEMPIN3/TALERT#/GPIO64 B5

VIN0/GPIO53 A4

VIN1/GPIO54 B4

VIN2/GPIO55 C4

VIN3/GPIO56 D5

VIN4/GPIO57 D6

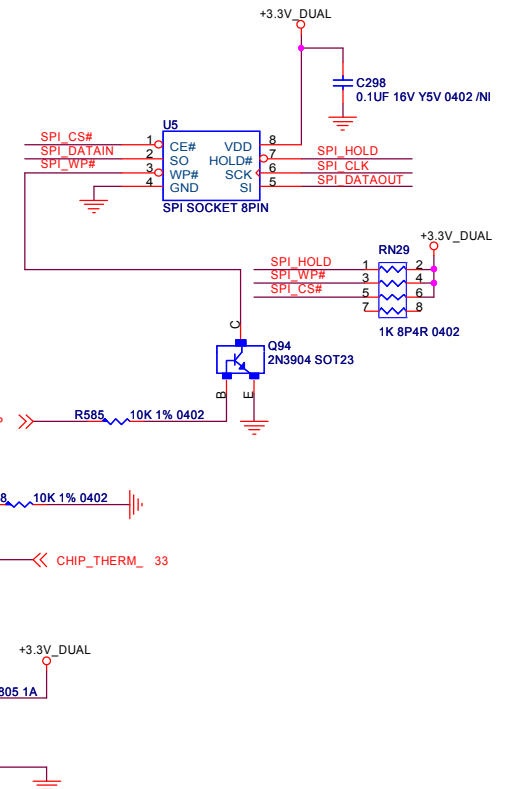
VIN5/GPIO58 A7

VIN6/GPIO59 A7

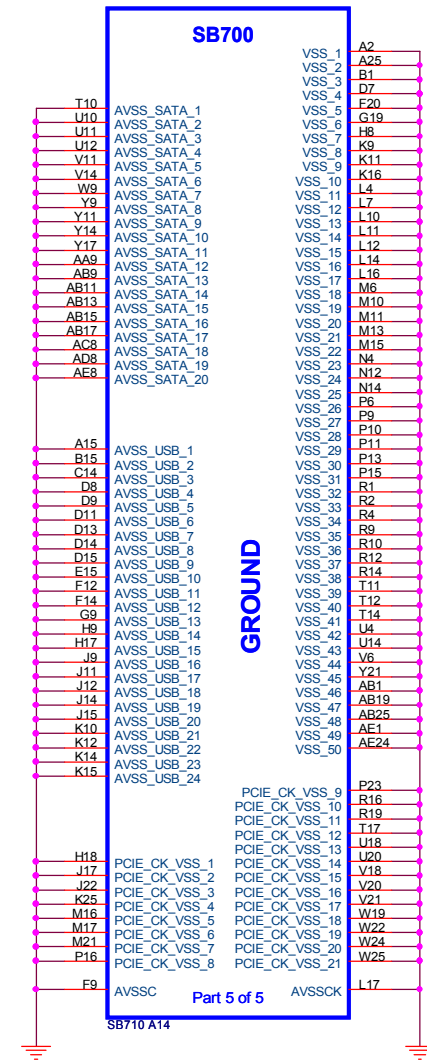
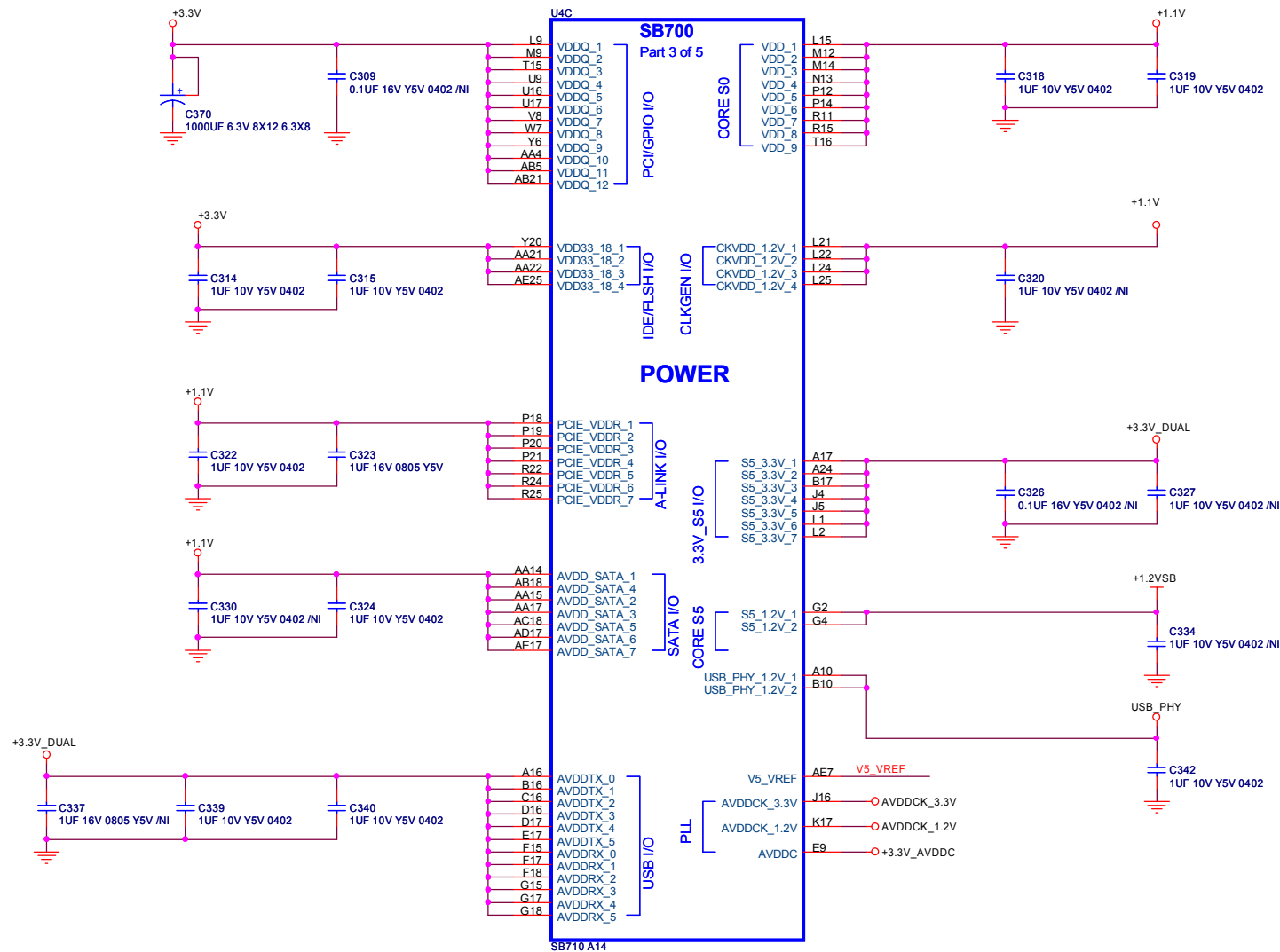
VIN7/GPIO60 B7

AVDD F6

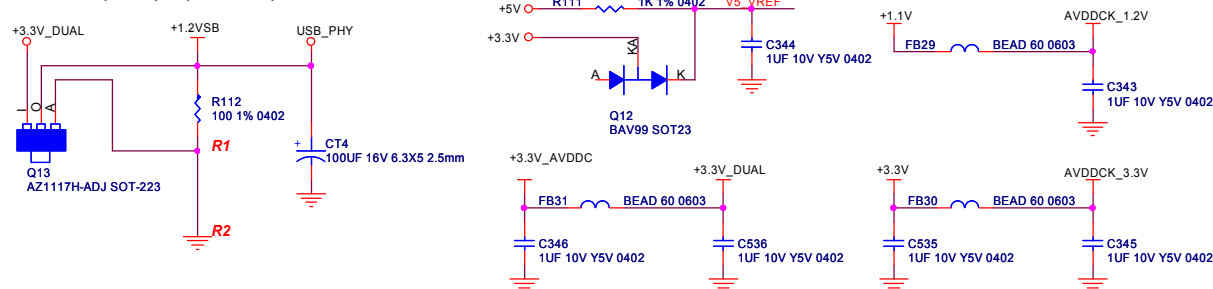
AVSS G7



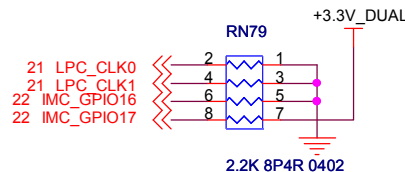
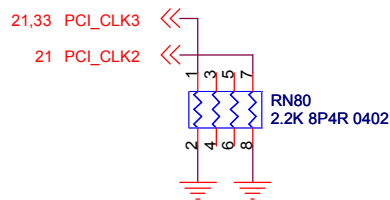
Title			SB710 SATA/IDE/SPI
Size	Document Number	A78LD-M3S	
Custom			Rev 7.1
Date:	Thursday, April 21, 2011	Sheet 23	of 45



$$V_{out}=V_{ref} (1.25V) \times (1+R_2/R_1)=1.2V$$



Title		SB710 POWER	
Size	Document Number		Rev
Custom	A78LD-M3S		7.1
Date:	Thursday, April 21, 2011	Sheet	24 of 45



REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	

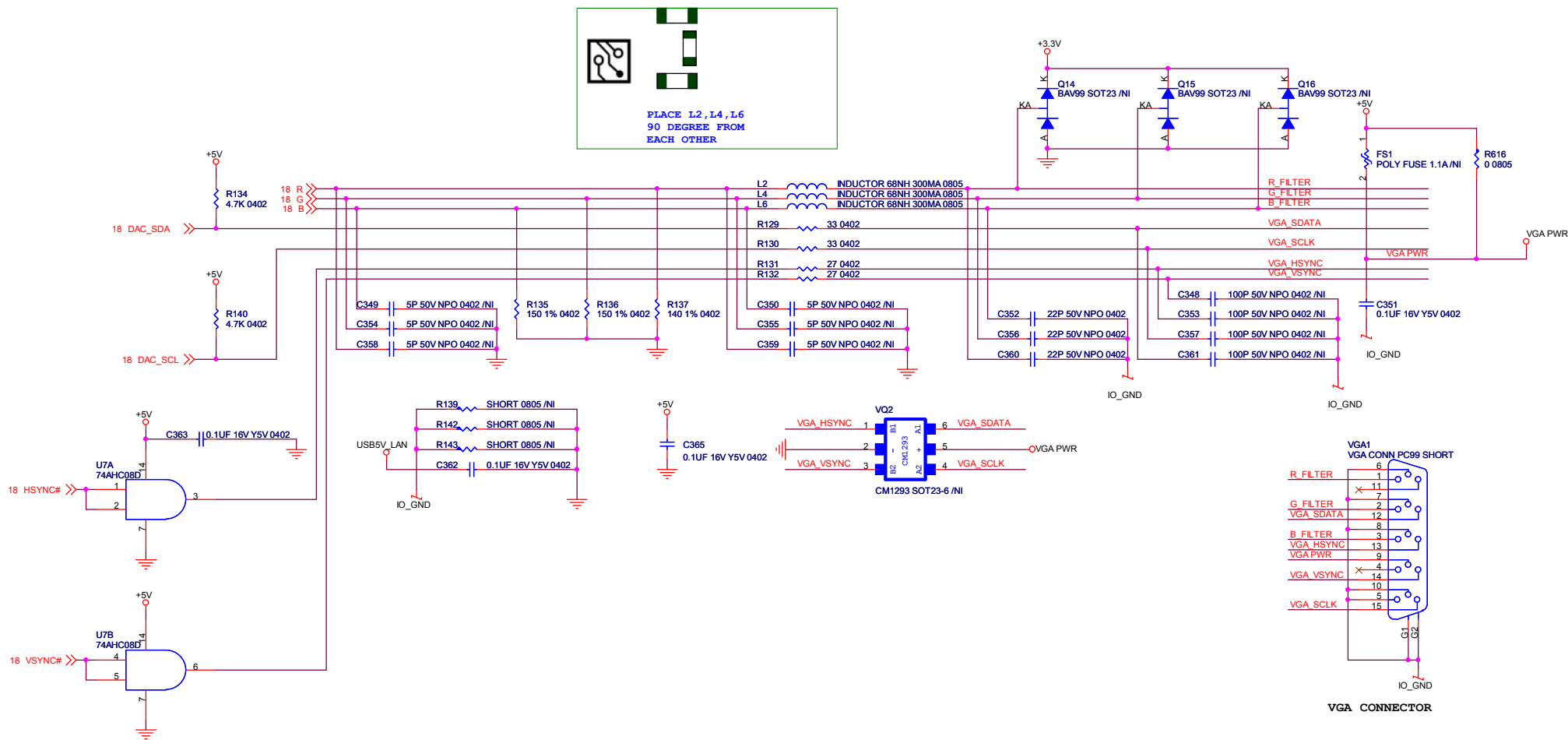
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

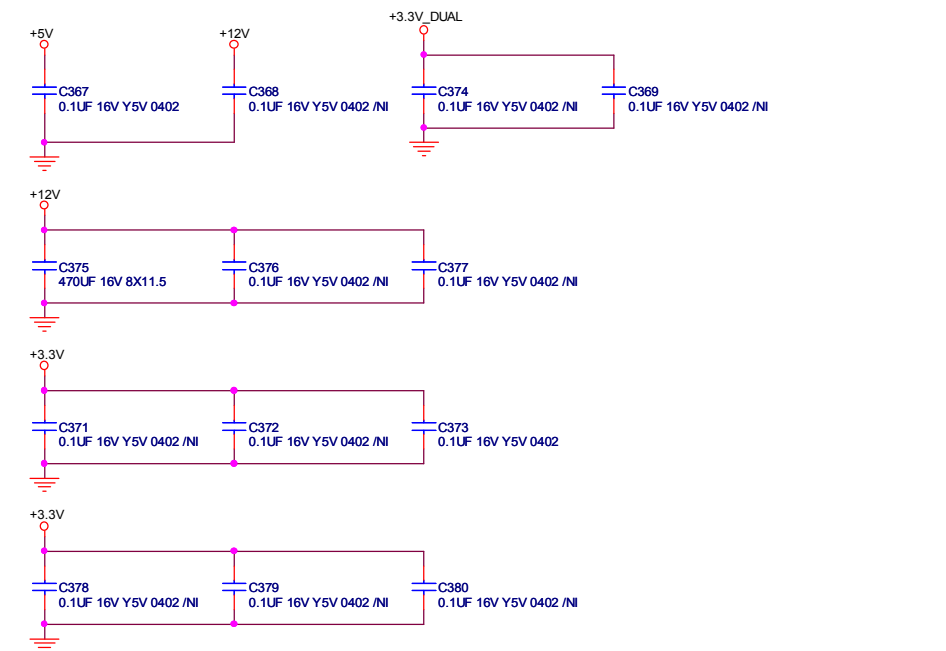
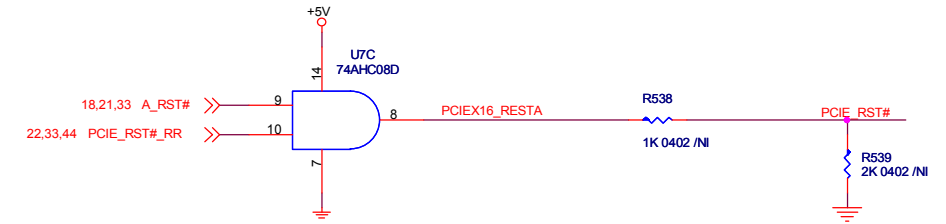
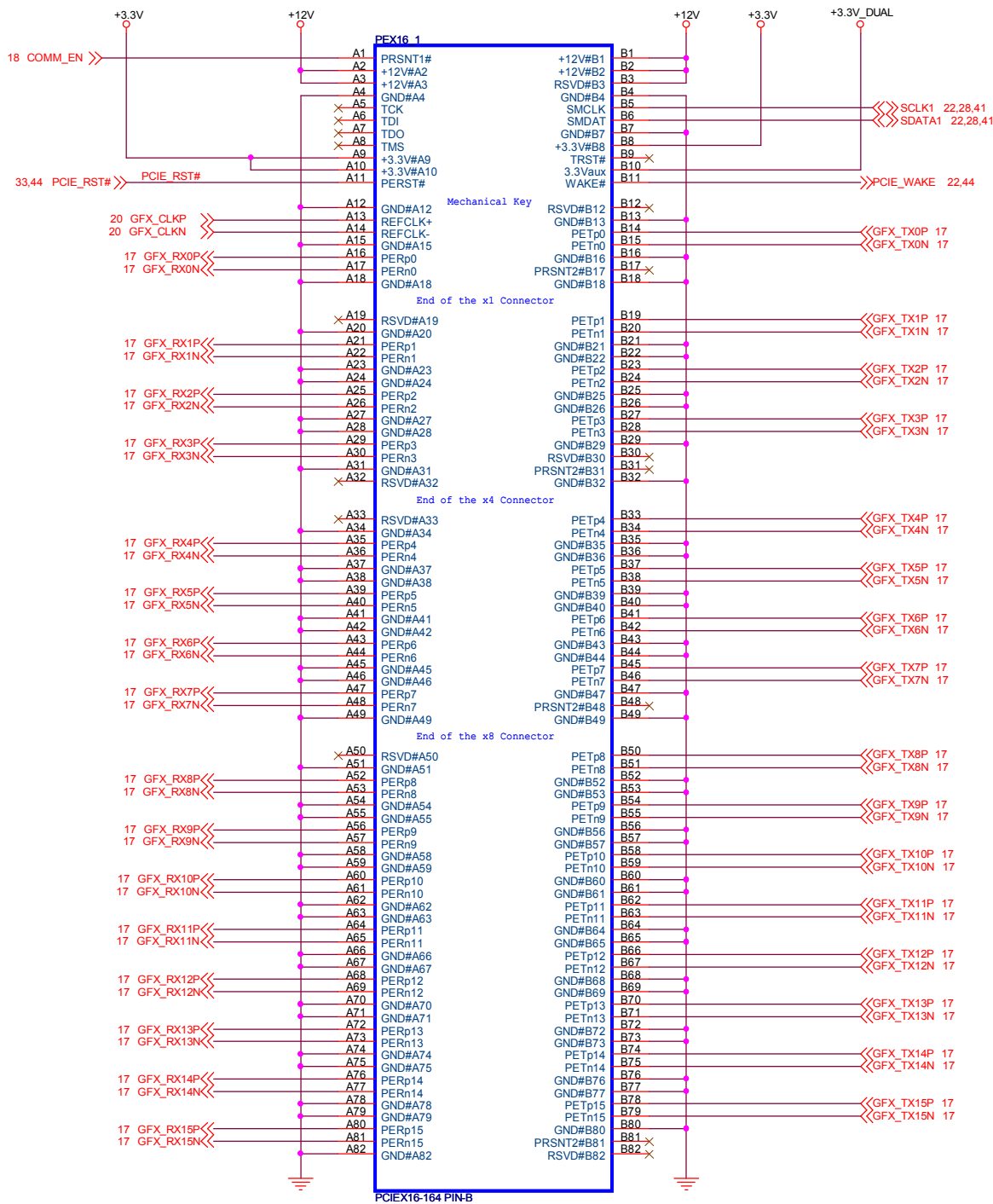
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

		
Title SB710 STRAP		
Size Custom	Document Number A78LD-M3S	Rev 7.1
Date: Thursday, April 21, 2011	Sheet 25 of 45	





映泰股份有限公司
BIOSTAR GROUP

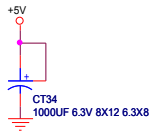
PCI-E SLOT

A78LD-M3S

Rev 7.1

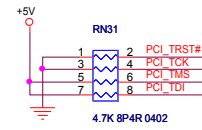
Thursday, April 21, 2011

Sheet 27 of 45

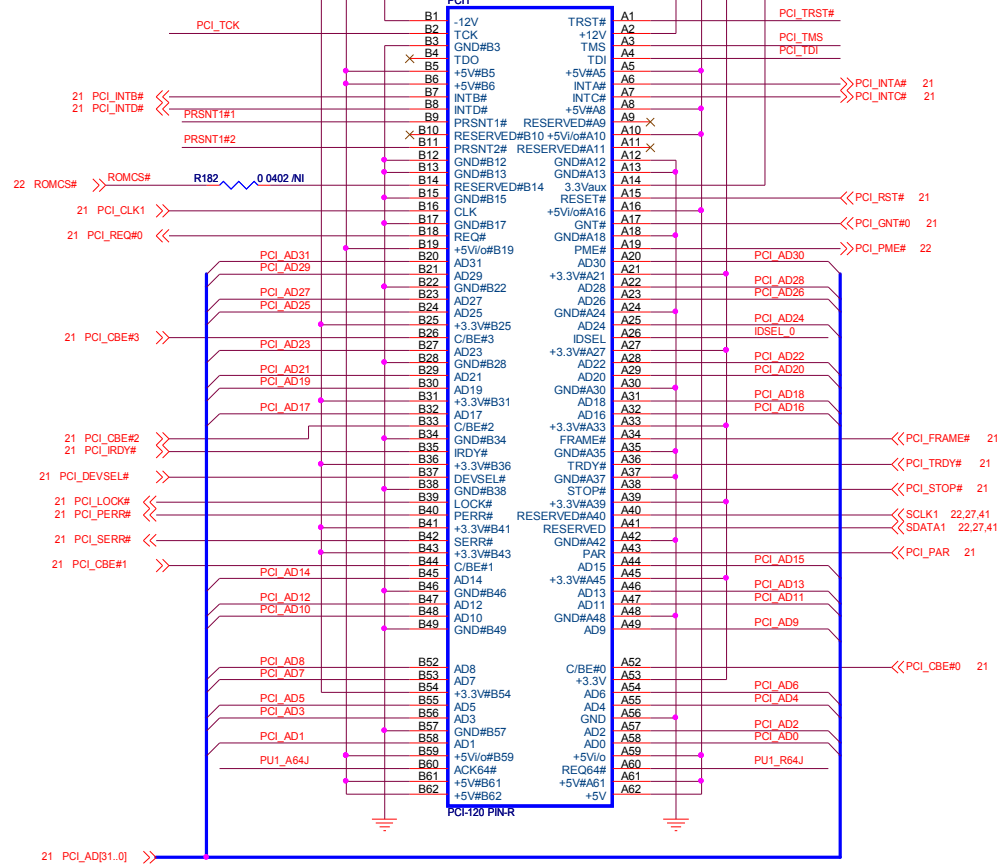


IDSEL:AD21 , INT:ABCD , REQ0 & GNT0 , PCI_CLK3

PCI_SLOT 1



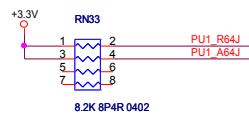
IDSEL:AD22 , INT:BCDA , REQ1 & GNT1 , PCI_CLK4



IDSEL_0 R185 100 1% 0402 PCI_AD21

PRSN1#1 C382 0.1UF 16V Y5V 0402 /NI

PRSN1#2 C384 0.1UF 16V Y5V 0402 /NI

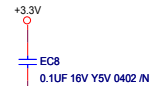


21 PCI_CBE#3.0] >> PCI_CBE#0
PCI_CBE#1
PCI_CBE#2
PCI_CBE#3

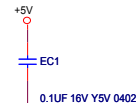
FOR EMI NEAR C382



FOR EMI NEAR RN32



FOR EMI NEAR C409

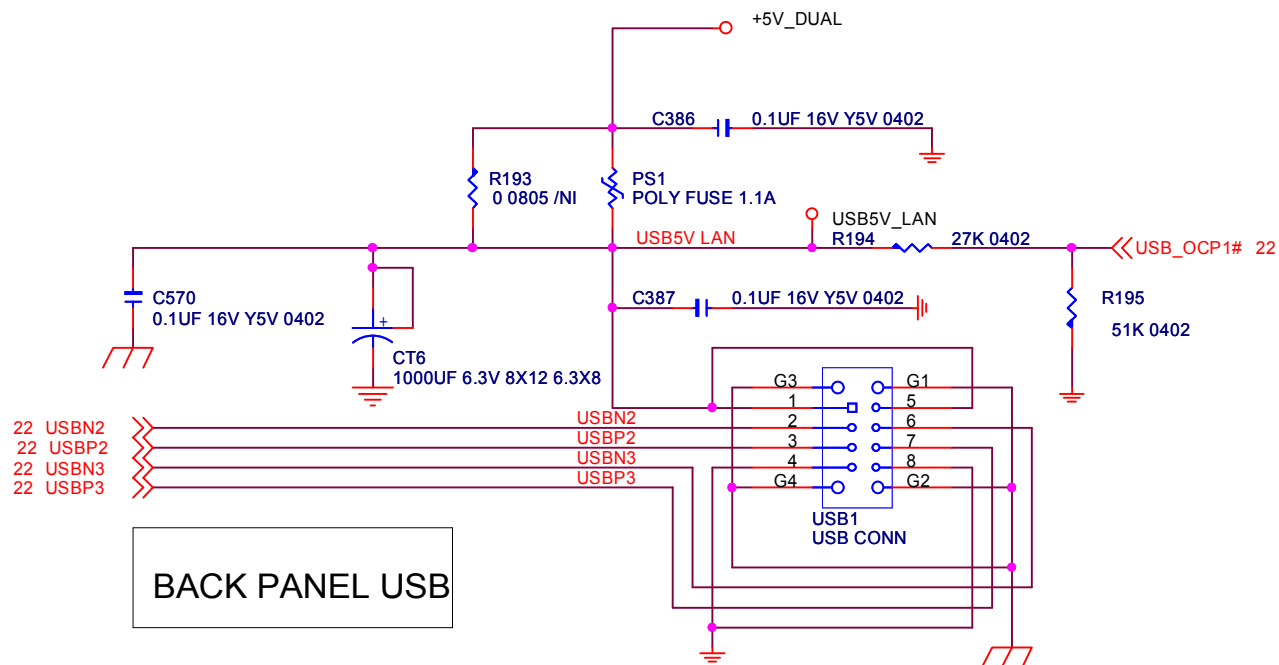


21 PCI_CLK1 >>
21 PCI_RST# >>

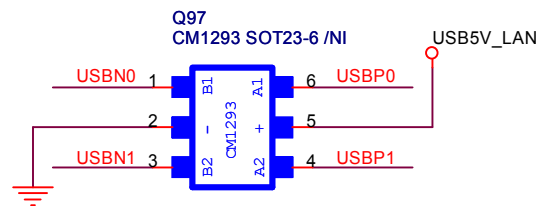
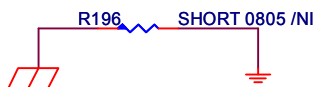
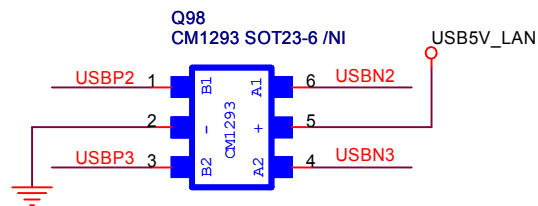
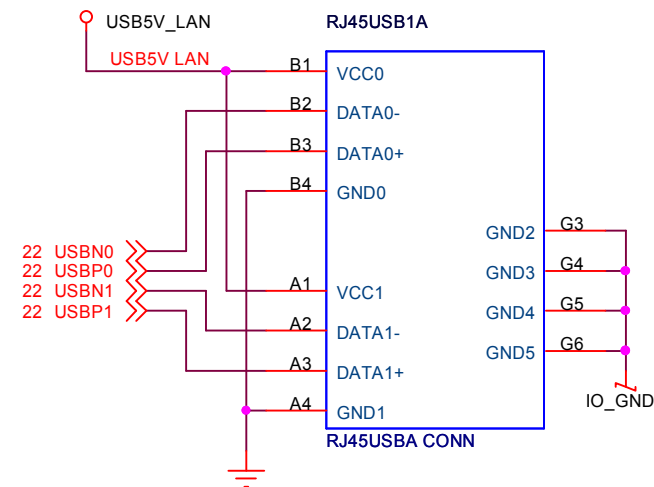
Near PCI Slot




Title			PCI SLOT
Size	Document Number	Rev	
Custom	A78LD-M3S	7.1	
Date:	Thursday, April 21, 2011	Sheet	28 of 45



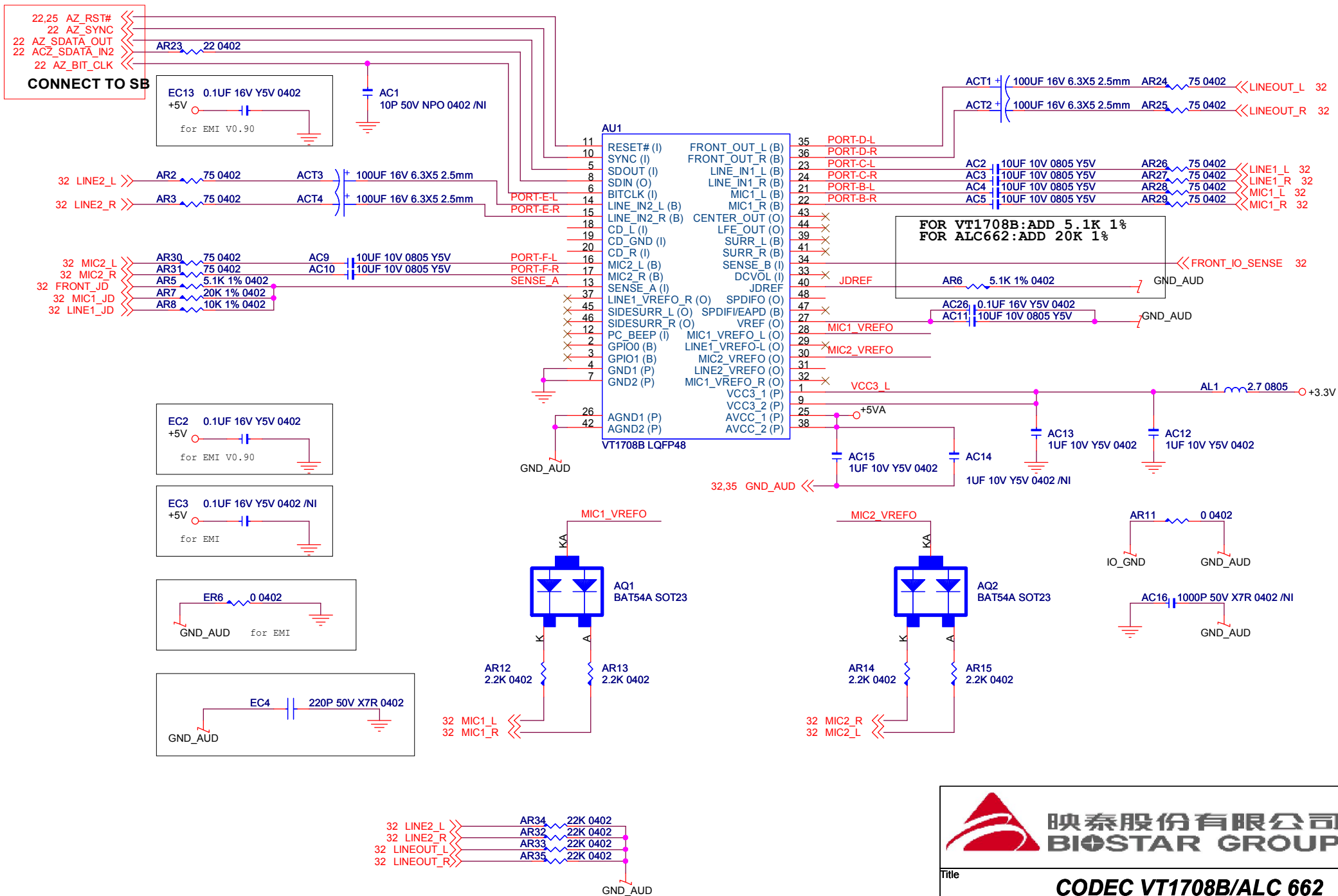
BACK PANEL USB
PLACE NEAR CONN

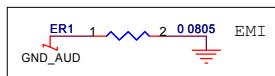




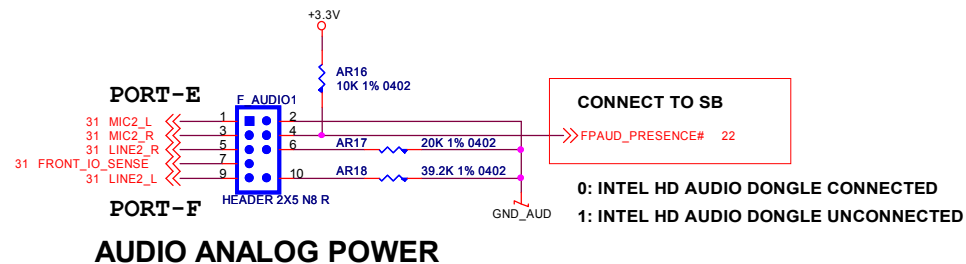
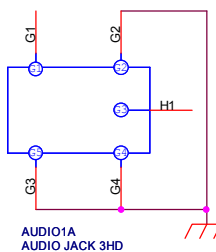
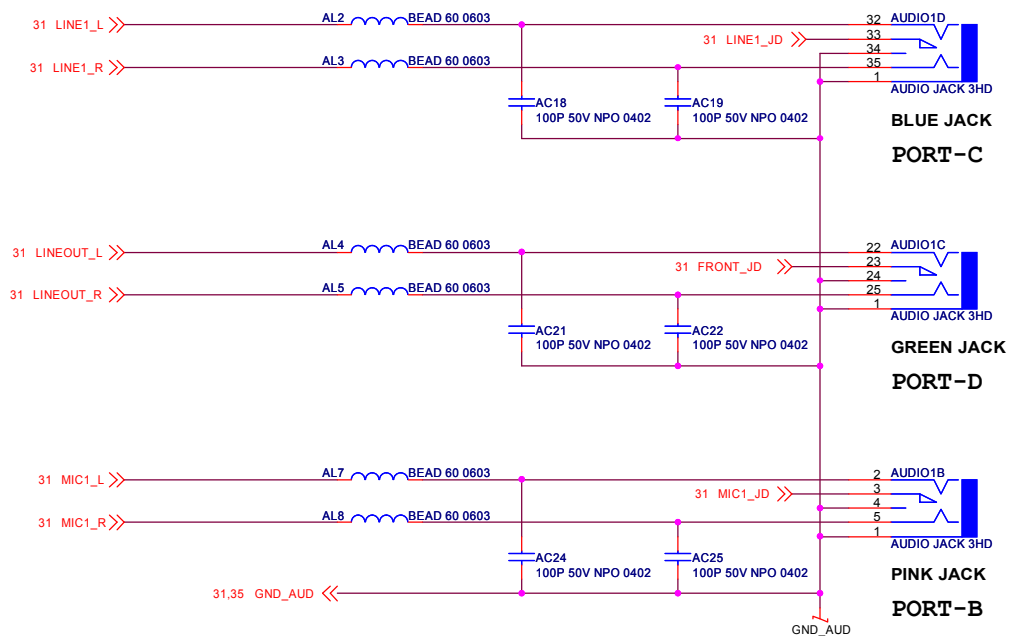
映泰股份有限公司
BIOSAR GROUP

Title		
USB CONN		
Size	Document Number	Rev
Custom	A78LD-M3S	7.1
Date:	Thursday, April 21, 2011	Sheet 30 of 45





Rear Panel Onboard Analog I/O



PORT-E

31 MIC2_L
31 MIC2_R
31 LINE2_R
31 FRONT_IO_SENSE
31 LINE2_L

PORT-F

HEADER 2X5 N8 R

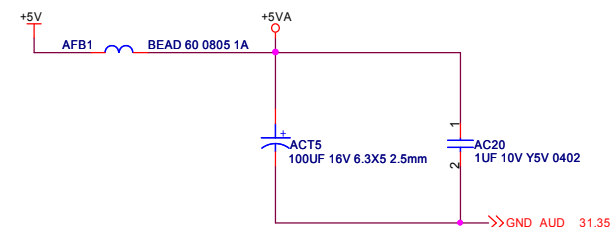
CONNECT TO SB

FPAUD_PRESENCE# 22

0: INTEL HD AUDIO DONGLE CONNECTED

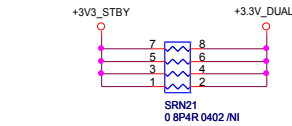
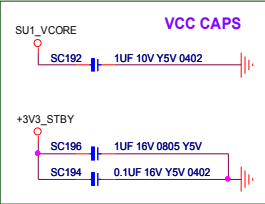
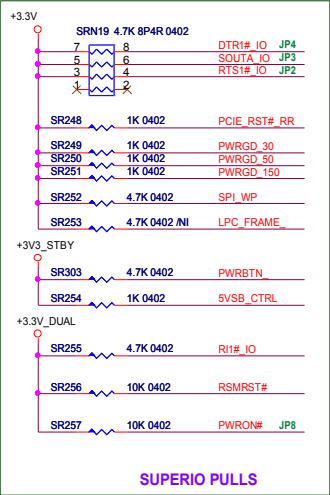
1: INTEL HD AUDIO DONGLE UNCONNECTED

AUDIO ANALOG POWER

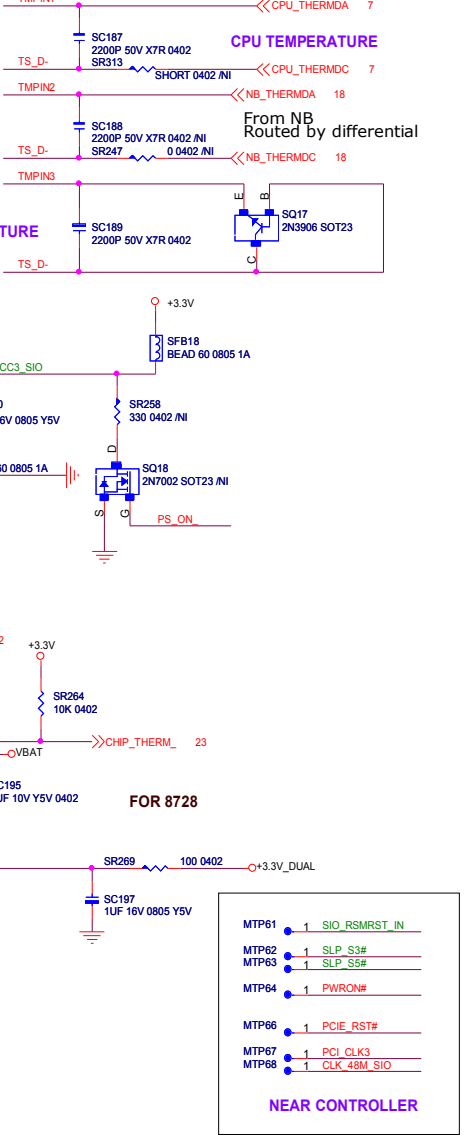
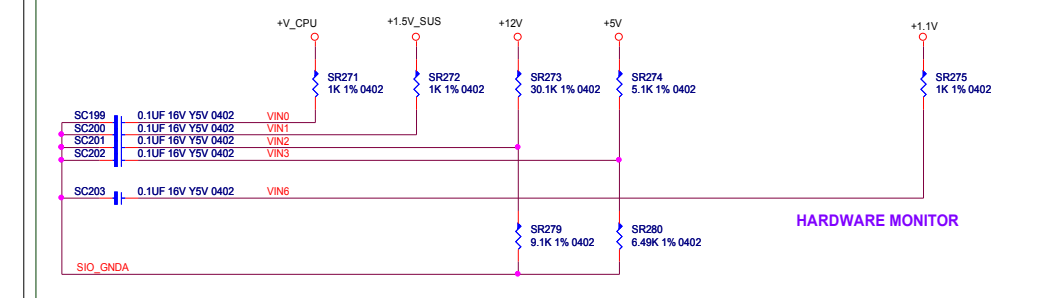
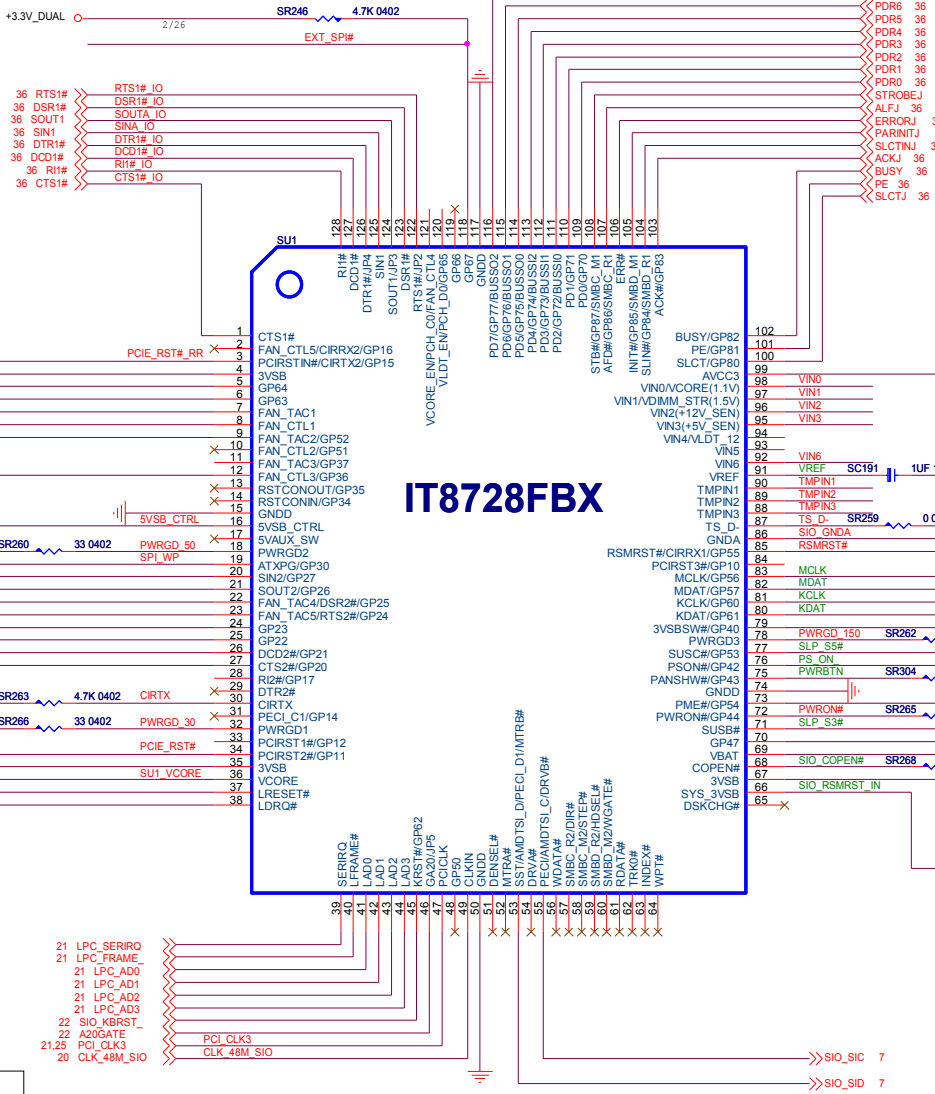
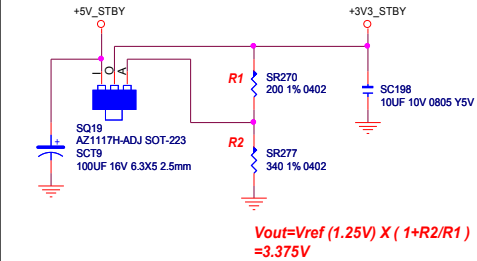


$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 5V$$

SUPERIO PART: S+Reference



Energy-Using Product(EUP)

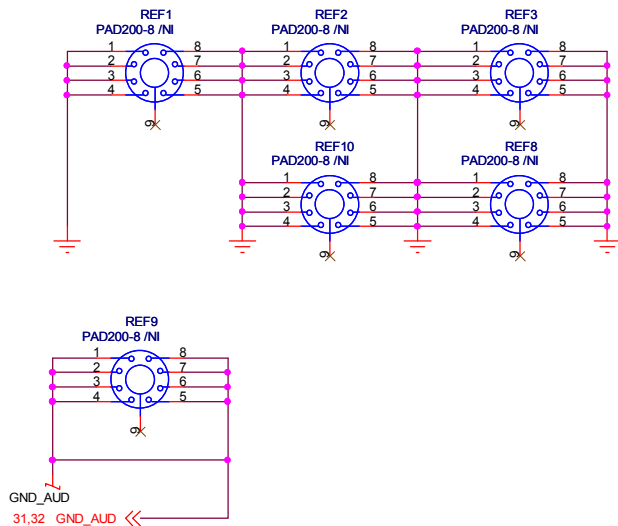
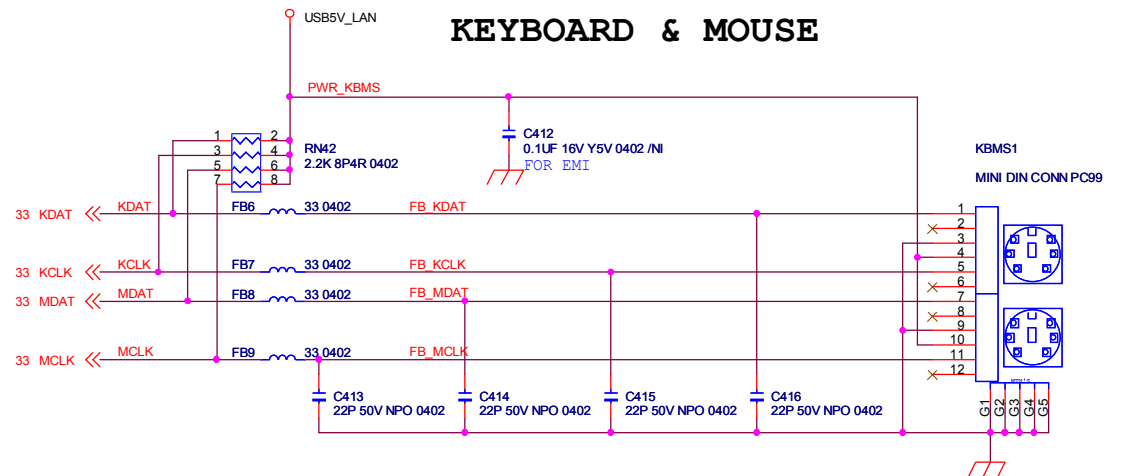


◇BIOSTAR'S PROPRIETARY INFORMATION◇

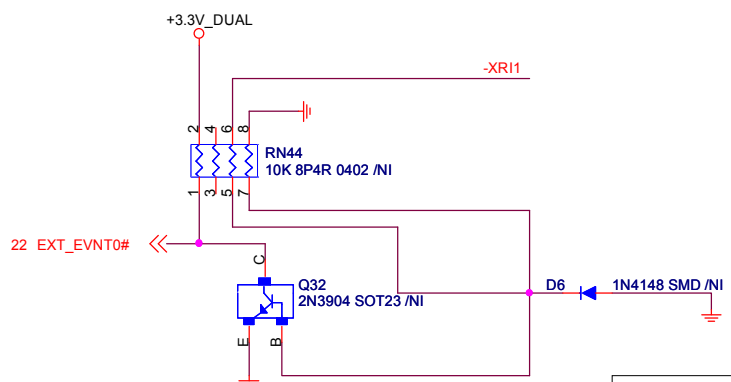
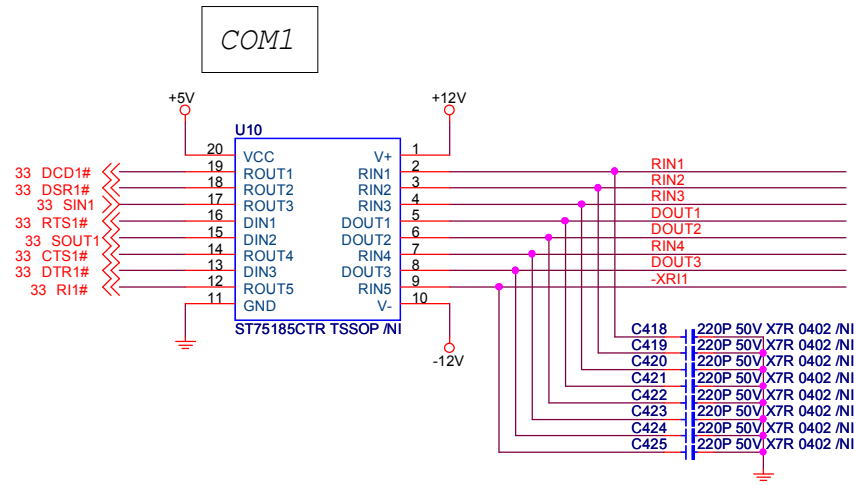
◇Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◇



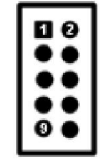
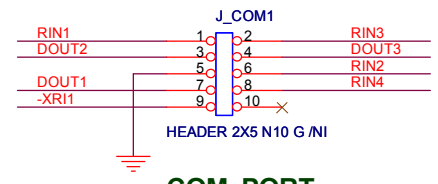
Title			SUPER I/O ITE 8728		
Size	Document Number	A78LD-M3S			Rev
Custom					7.1
Date:	Thursday, April 21, 2011	Sheet	33	of	45



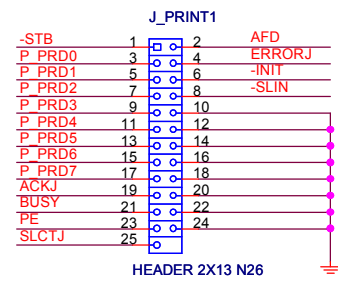
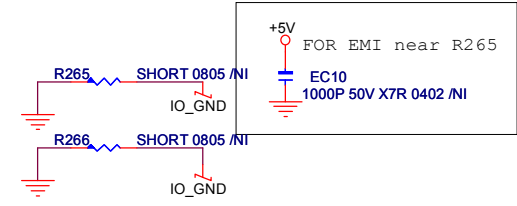
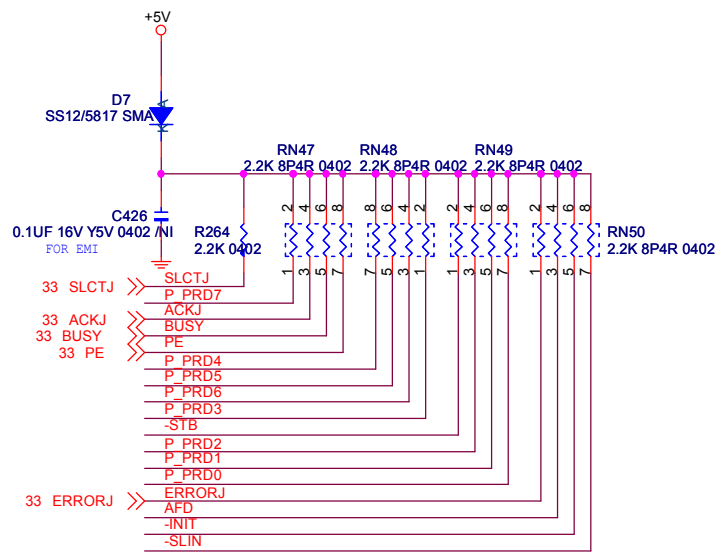
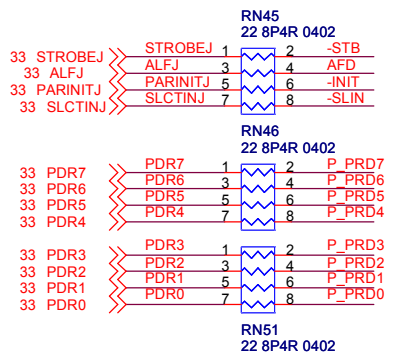
		Title	
		PS2 CONN	
Size	Document Number	Rev	
Custom		A78LD-M3S 7.1	
Date:	Thursday, April 21, 2011	Sheet	35 of 45




WAKE ON LAN



COM PORT PIN ASSIGNMENT



 映泰股份有限公司
BIOSSTAR GROUP

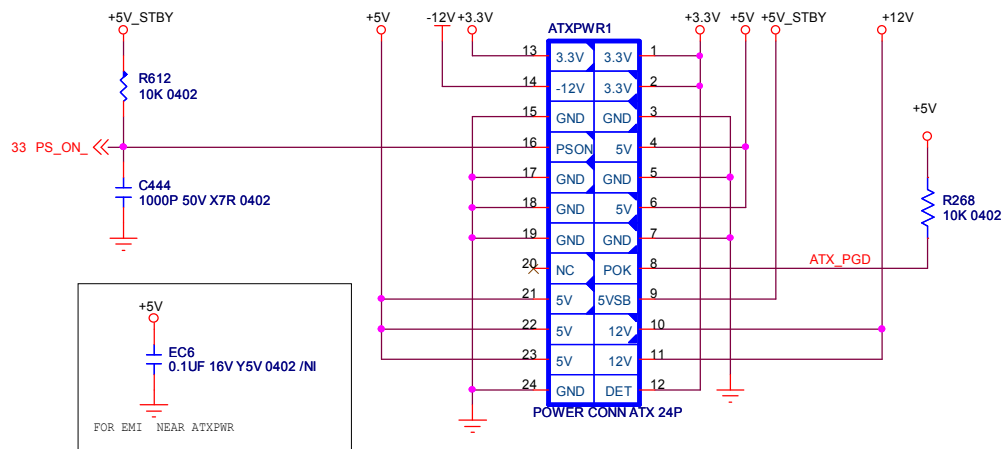
Title

COM & PRINTER CONNECTOR

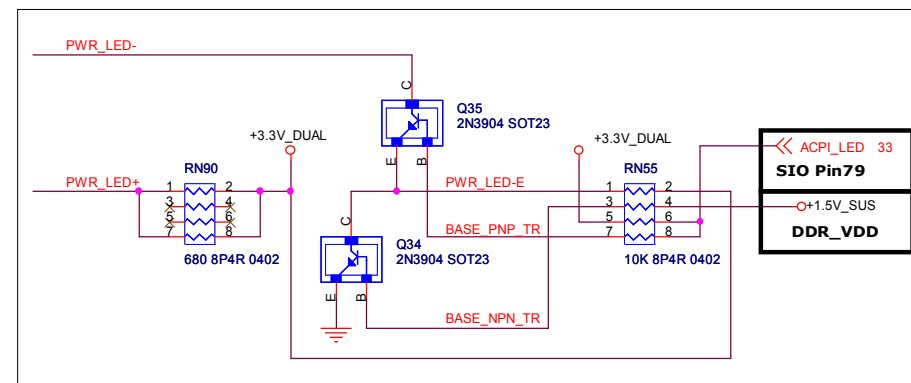
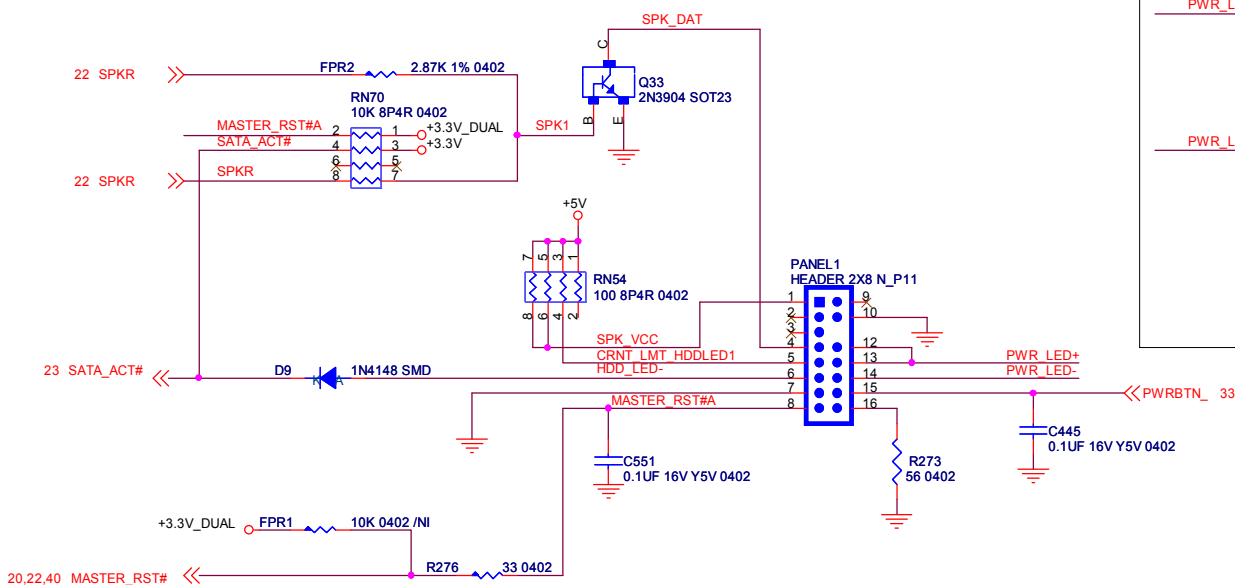
Size Custom Document Number

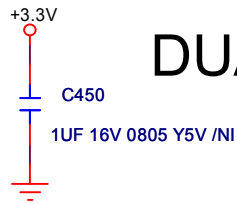
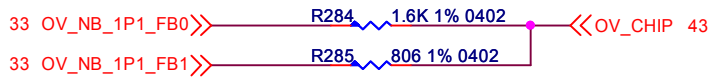
A78LD-M3S

Date: Thursday, April 21, 2011 Sheet 36 of 45 Rev 7.1

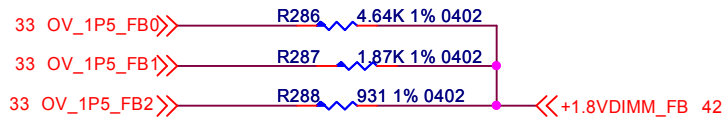


LED_D2	LED_D1	MESSAGE
OFF	OFF	ABNORMAL
OFF	ON	MEMORY ERROR
ON	OFF	VGA ERROR
ON	ON	NORMAL






DUAL +3.3V



CORE VOLTAGE	OV_NB_1P1_FB1	OV_NB_1P1_FB0
+1.240V	1	1
+1.295V	1	0
+1.349V	0	1
+1.404V	0	0

+1.5VDIMM_FB	VDIMM0	VDIMM1	VDIMM2
Default 1.509V	1	1	1
1.547V	0	1	1
1.605V	1	0	1
1.644V	0	0	1
1.703V	1	1	0
1.742V	0	1	0
1.799V	1	0	0
1.838V	0	0	0

OV_VCORE	OV_VCORE0	OV_VCORE1
Default V_CPU	1	1
+3.3%	0	1
+6.6%	1	0
+10%	0	0



映泰股份有限公司
BIOSTAR GROUP

Title

OVER VOLTAGE

Size

Document Number

Rev

Custom

A78LD-M3S

7.1

Date:

Thursday, April 21, 2011

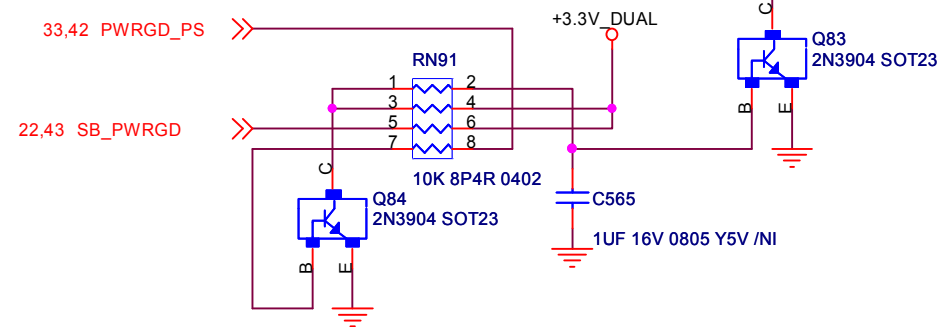
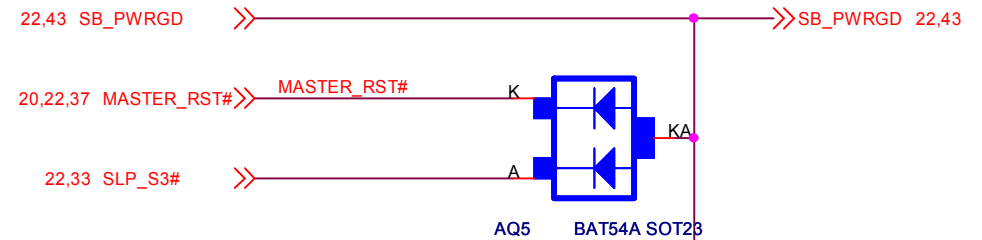
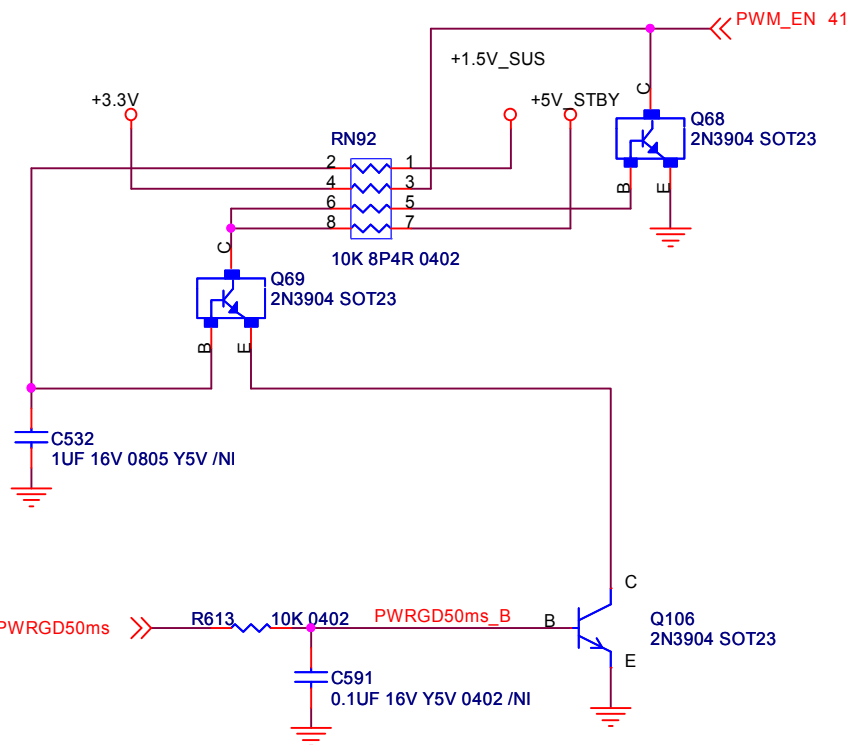
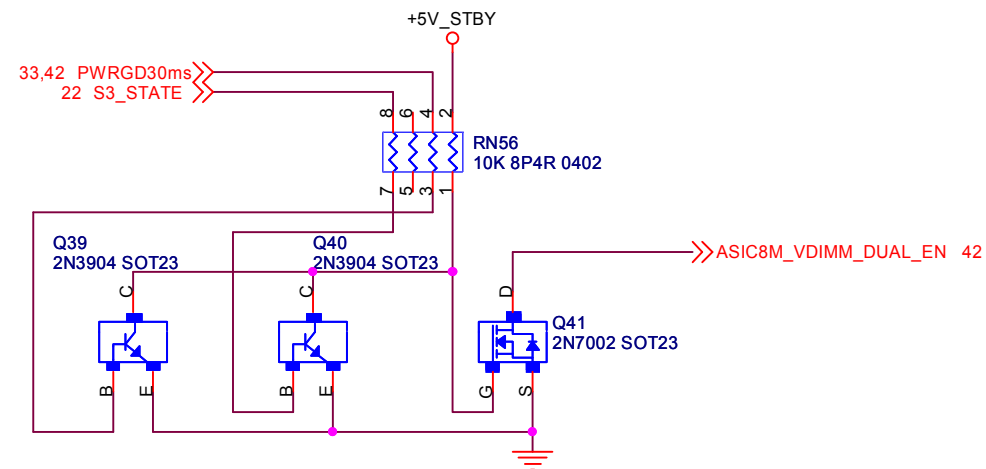
Sheet


38

of

45

ATHLON64 POWER GOOD & ENABLES CIRCUIT

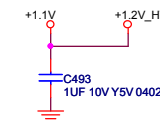
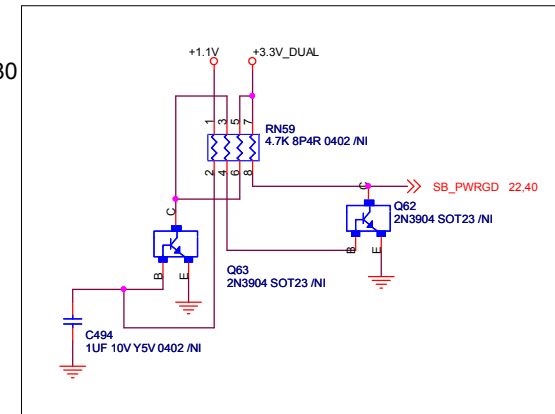
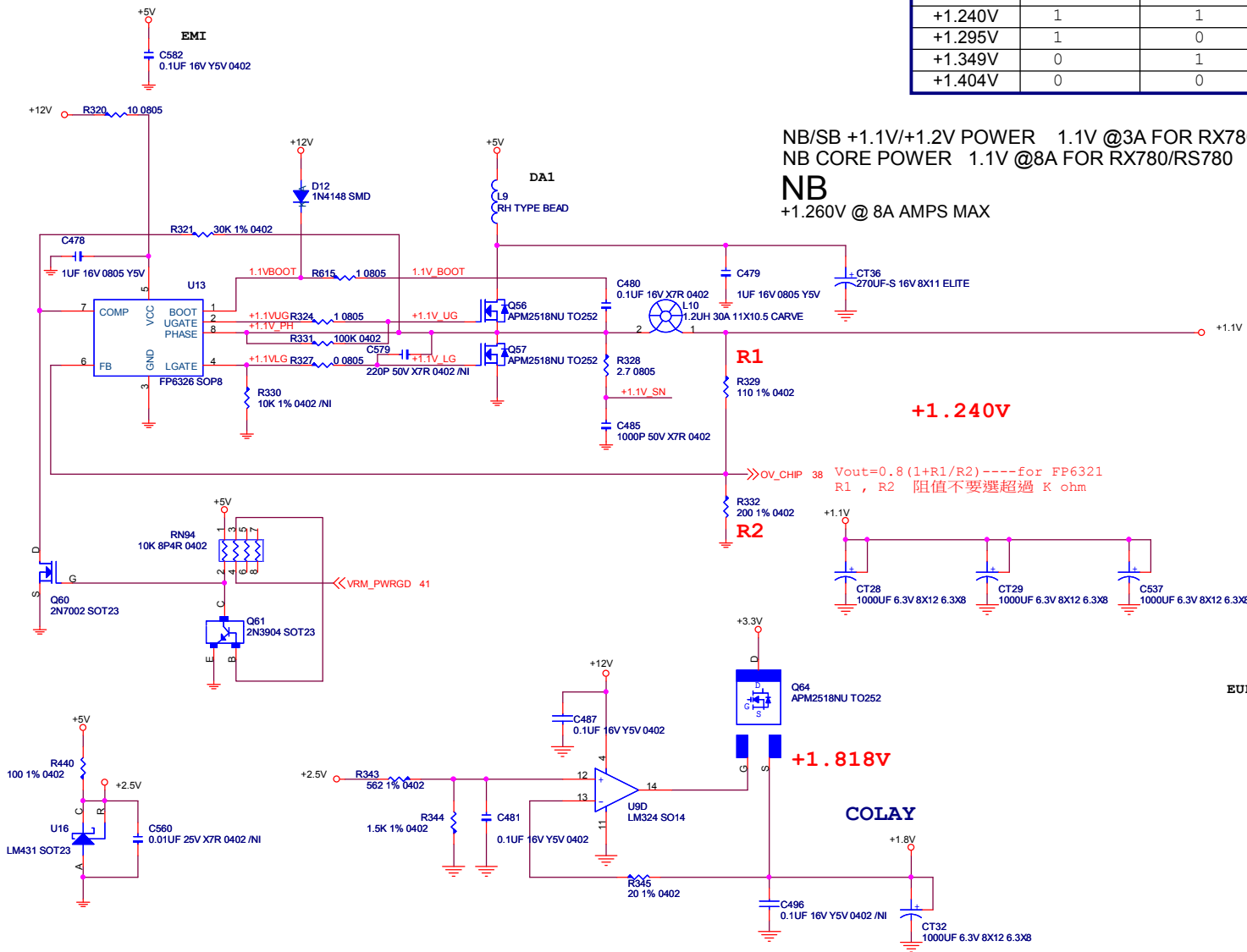


 映泰股份有限公司 BI+STAR GROUP		
Title PWR GD / MISC POWER		
Size Custom	Document Number A78LD-M3S	Rev 7.1
Date: Thursday, April 21, 2011		
Sheet 40 of 45		

CORE VOLTAGE	OV_NB_1P1_FB1	OV_NB_1P1_FB0
+1.240V	1	1
+1.295V	1	0
+1.349V	0	1
+1.404V	0	0

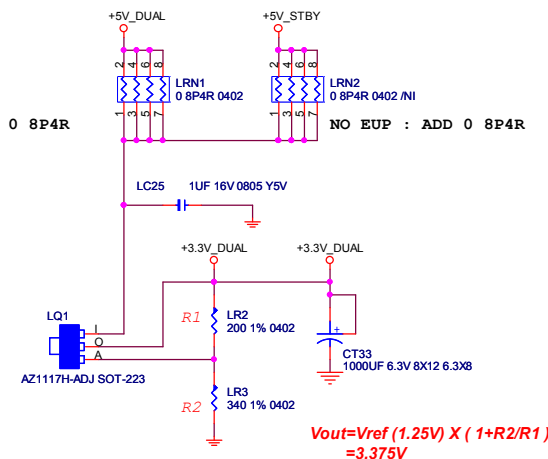
NB/SB +1.1V/+1.2V POWER 1.1V @3A FOR RX780/RS780
NB CORE POWER 1.1V @8A FOR RX780/RS780

NB
+1.260V @ 8A AMPS MAX



EUP : ADD 0 8P4R

NO EUP : ADD 0 8P4R



$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 3.375V$$

