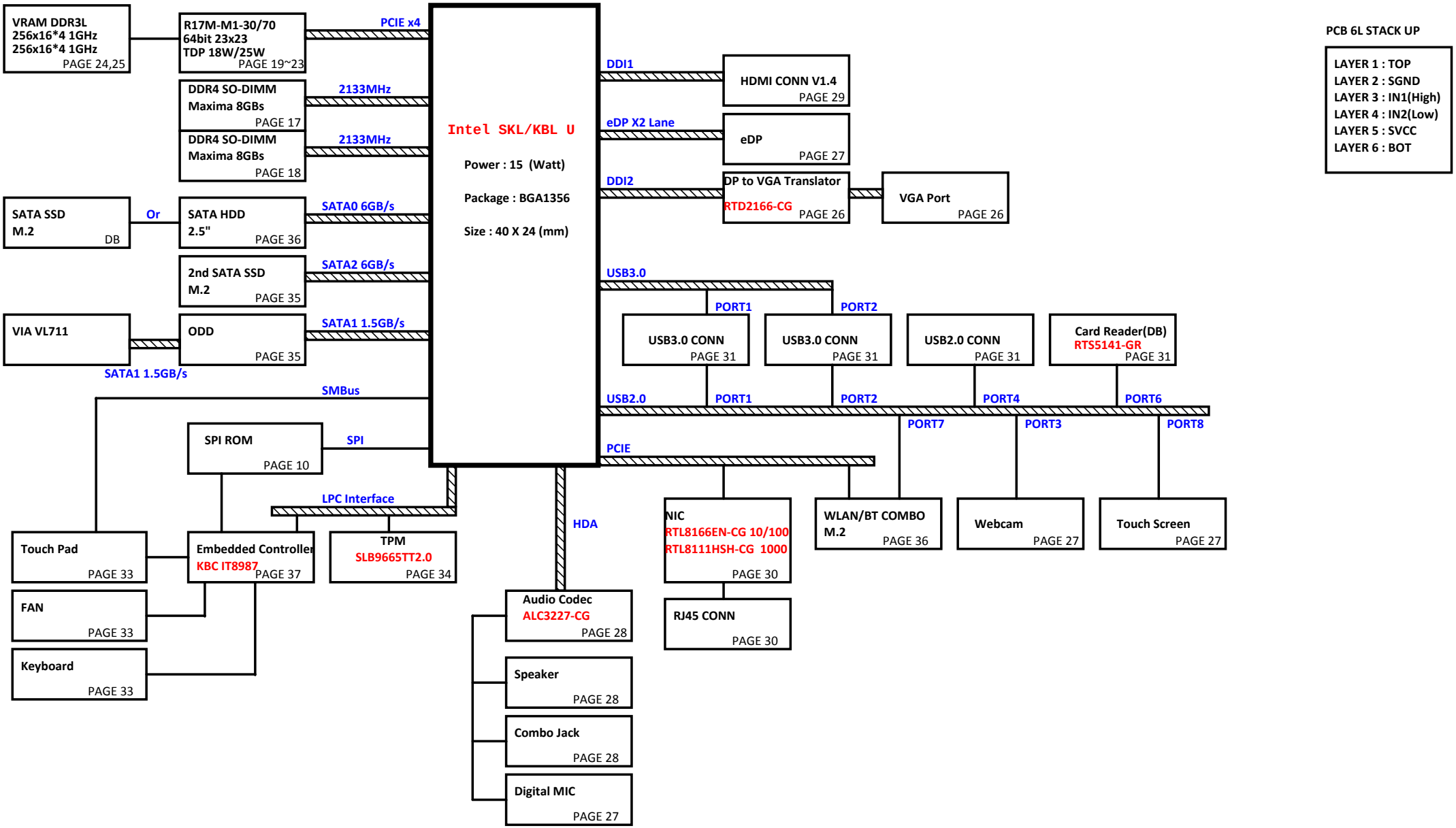
Intel SKL-U/KBL-U Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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+3V <4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+1.0V <4,37,42,43>
+VCCSTPLL <4,5,6,9,42>

HDMI

<29> IN_D2# → IN_D2# E55
<29> IN_D2 → IN_D2 F55
<29> IN_D1# → IN_D1# E58
<29> IN_D1 → IN_D1 F58
<29> IN_D0# → IN_D0# F53
<29> IN_D0 → IN_D0 G53
<29> IN_CLK# → IN_CLK# F56
<29> IN_CLK → IN_CLK G56

<26> DDI1_TX0_N → DDI1_TX0_N C50
<26> DDI1_TX0_P → DDI1_TX0_P D50
<26> DDI1_TX1_N → DDI1_TX1_N C52
<26> DDI1_TX1_P → DDI1_TX1_P D52

U1A — SKL_ULT ? — Need apply PN

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3] — DDI
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 <27>
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 <27>
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 <27>
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 <27>
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN <27>
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP <27>
EDP_DISP_UTIL B52

DISPLAY SIDEBANDS

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN F48 → INT_DDI1_AUXN <26>
DDI2_AUXP G48 → INT_DDI1_AUXP <26>
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E18/DDPB_CTRLCLK L13
GPP_E19/DDPB_CTRLDATA L12
GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N8
GPP_E22/DDPD_CTRLCLK N11
GPP_E23/DDPD_CTRLDATA N12
EDP_RCOMP E52

GPP_E13/DDPB_HPD0 L9 HDMI_HPD_CON → HDMI_HPD_CON <29>
GPP_E14/DDPC_HPD1 L7 DDI1_HPD_CON → DDI1_HPD_CON <26>
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD <27>

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON <27>
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM <27>
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON <27>

*SKL_ULT
REV = 1
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?

SI

+3VO — R9055 2.2K_4 — DDPC_CTRLDATA
TP3 — 1DDPD_CTRLDATA
+VCCIO — R3 24.9_1%_4 — EDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

ULT_EDP_HPD — R2 100K_4

<37,43> H_PROCHOT# — R4 499/F_4 — <37> EC_PECI, <37> PM_THRMTRIP#

U1D — SKL_ULT ? — Need apply PN

CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63
SKTOCC# A65

CPU MISC

BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5

PROC_POPIRCOMP AT16
PCH_OPIRCOMP AU16
OPCE_RCOMP H66
OPC_RCOMP H65

JTAG

PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU
PROC_TRST# B59 PROC_TEST#

PCH_JTAG_TCK B56 JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH
PCH_JTAG_TDO A56 JTAG_TDO_PCH
PCH_JTAG_TMS C59 JTAG_TMS_PCH
PCH_TRST# C61 XDP_TRST#_CPU
JTAGX A59 JTAGX_PCH

*SKL_ULT
REV = 1
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?

+VCCSTPLL — R6 *49.9/F_4 — CATERR#

+1.0V
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

R8 49.9/F_4 PROC_POPIRCOMP
R11 49.9/F_4 PCH_OPI_RCOMP
R12 49.9/F_4 EDRAM_OPIO_RCOMP
R14 49.9/F_4 EOPIO_RCOMP

XDP_TRST#_CPU R863 *0_4/S PROC_TEST#

Close to EC

+VCCSTPLL — PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A
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SkyLake ULT Processor (DDR4)

<17> M_A_DQSN[7:0]
<17> M_A_DQSP[7:0]
<18> M_B_DQSN[7:0]
<18> M_B_DQSP[7:0]
<17> M_A_DQ[63:0]
<18> M_B_DQ[63:0]

+1.2VSUS <6,17,18,40,42>

Need apply PN

U1B — SKL_ULT — *SKL_ULT REV = 1 — 2 OF 20

M_A_DQ0	AL71	DDR0_DQ[0]	
M_A_DQ1	AL68	DDR0_DQ[1]	
M_A_DQ2	AN68	DDR0_DQ[2]	
M_A_DQ3	AN69	DDR0_DQ[3]	
M_A_DQ4	AL70	DDR0_DQ[4]	
M_A_DQ5	AL69	DDR0_DQ[5]	
M_A_DQ6	AN70	DDR0_DQ[6]	
M_A_DQ7	AN71	DDR0_DQ[7]	
M_A_DQ8	AR70	DDR0_DQ[8]	
M_A_DQ9	AR68	DDR0_DQ[9]	
M_A_DQ10	AU71	DDR0_DQ[10]	
M_A_DQ11	AU68	DDR0_DQ[11]	
M_A_DQ12	AR71	DDR0_DQ[12]	
M_A_DQ13	AR69	DDR0_DQ[13]	
M_A_DQ14	AU70	DDR0_DQ[14]	
M_A_DQ15	AU69	DDR0_DQ[15]	
M_B_DQ0	AF65	DDR1_DQ[0]/DDR0_DQ[16]	
M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	
M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	
M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	
M_B_DQ4	AF66	DDR1_DQ[4]/DDR0_DQ[20]	
M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	
M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	
M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]	
M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]	
M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	
M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	
M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	
M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	
M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]	
M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]	
M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	
M_A_DQ16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	
M_A_DQ17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	
M_A_DQ18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	
M_A_DQ19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	
M_A_DQ20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	
M_A_DQ21	AY65	DDR0_DQ[21]/DDR0_DQ[37]	
M_A_DQ22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	
M_A_DQ23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	
M_A_DQ24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	
M_A_DQ25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	
M_A_DQ26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	
M_A_DQ27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	
M_A_DQ28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	
M_A_DQ29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	
M_A_DQ30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	
M_A_DQ31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	
M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	
M_B_DQ17	AT64	DDR1_DQ[17]/DDR0_DQ[49]	
M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	
M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	
M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	
M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]	
M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]	
M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	
M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]	
M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]	
M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	
M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	
M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]	
M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]	
M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]	
M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]	

		DDR0_CKN[0]	AU53
		DDR0_CKP[0]	AT53
		DDR0_CKN[1]	AU55
		DDR0_CKP[1]	AT55
		DDR0_CKE[0]	BA56
		DDR0_CKE[1]	BB56
		DDR0_CKE[2]	AW56
		DDR0_CKE[3]	AY56
		DDR0_CS#[0]	AU45
		DDR0_CS#[1]	AU43
		DDR0_ODT[0]	AT45
		DDR0_ODT[1]	AT43
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]		BA51	M_A_A5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]		BB54	M_A_A9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]		BA52	M_A_A6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]		AW52	M_A_A8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]		AY55	M_A_A7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]		AW54	M_A_BG#0
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]		BA54	M_A_A12
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]		BA55	M_A_A11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#		AY54	M_A_A15
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]		AU46	M_A_BG#1
		AU48	M_A_A13
		AT46	M_A_CAS#
		AU50	M_A_WE#
		AU52	M_A_RAS#
		AY51	M_A_BS#0
		AT48	M_A_A2
		AT50	M_A_BS#1
		BB50	M_A_A1
		AY50	M_A_A0
		BA50	M_A_A3
		BB52	M_A_A4
		DDR0_DQSN[0]	AM70
		DDR0_DQSP[0]	AM69
		DDR0_DQSN[1]	AT69
		DDR0_DQSP[1]	AT70
DDR1_DQSN[0]/DDR0_DQSN[2]		AH66	M_B_DQSN0
DDR1_DQSP[0]/DDR0_DQSP[2]		AH65	M_B_DQSP0
DDR1_DQSN[1]/DDR0_DQSN[3]		AG69	M_B_DQSN1
DDR1_DQSP[1]/DDR0_DQSP[3]		AG70	M_B_DQSP1
DDR0_DQSN[2]/DDR0_DQSN[4]		BA64	M_A_DQSN2
DDR0_DQSP[2]/DDR0_DQSP[4]		AY64	M_A_DQSP2
DDR0_DQSN[3]/DDR0_DQSN[5]		AY60	M_A_DQSN3
DDR0_DQSP[3]/DDR0_DQSP[5]		BA60	M_A_DQSP3
DDR1_DQSN[2]/DDR0_DQSN[6]		AR66	M_B_DQSN2
DDR1_DQSP[2]/DDR0_DQSP[6]		AR65	M_B_DQSP2
DDR1_DQSN[3]/DDR0_DQSN[7]		AR61	M_B_DQSN3
DDR1_DQSP[3]/DDR0_DQSP[7]		AR60	M_B_DQSP3
DDR0_ALERT#		AW50	M_A_ALERT#
DDR0_PAR		AT52	M_A_PARITY
DDR_VREF_CA		AY67	SM_VREF
DDR0_VREF_DQ		BA68	SMDDR_VREF_DQ0_M3
DDR1_VREF_DQ		BA67	SMDDR_VREF_DQ1_M3
DDR_VTT_CNTL		AW67	DDR_VTT_CNTL

NIL-DDR CH - A

M_A_CLKN0	<17>
M_A_CLKP0	<17>
M_A_CLKN1	<17>
M_A_CLKP1	<17>
M_A_CKE0	<17>
M_A_CKE1	<17>
M_A_CS#0	<17>
M_A_CS#1	<17>
M_A_DIM0_ODT0	<17>
M_A_DIM0_ODT1	<17>
M_A_A5	<17>
M_A_A9	<17>
M_A_A6	<17>
M_A_A8	<17>
M_A_A7	<17>
M_A_BG#0	<17>
M_A_A12	<17>
M_A_A11	<17>
M_A_ACT#	<17>
M_A_BG#1	<17>
M_A_A13	<17>
M_A_CAS#	<17>
M_A_WE#	<17>
M_A_RAS#	<17>
M_A_BS#0	<17>
M_A_A2	<17>
M_A_BS#1	<17>
M_A_A10	<17>
M_A_A1	<17>
M_A_A0	<17>
M_A_A3	<17>
M_A_A4	<17>
M_A_ALERT#	<17>
M_A_PARITY	<17>
SM_VREF	<17>
SMDDR_VREF_DQ1_M3	<18>
DDR_VTT_CNTL	<18>

20mils width

U1C — SKL_ULT — *SKL_ULT REV = 1 — 3 OF 20

Need apply PN

M_A_DQ32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	
M_A_DQ33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	
M_A_DQ34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	
M_A_DQ35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	
M_A_DQ36	BB39	DDR0_DQ[36]/DDR1_DQ[4]	
M_A_DQ37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	
M_A_DQ38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	
M_A_DQ39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	
M_A_DQ40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	
M_A_DQ41	AW35	DDR0_DQ[41]/DDR1_DQ[9]	
M_A_DQ42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	
M_A_DQ43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	
M_A_DQ44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	
M_A_DQ45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	
M_A_DQ46	BA33	DDR0_DQ[46]/DDR1_DQ[14]	
M_A_DQ47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	
M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	
M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	
M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	
M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	
M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	
M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	
M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]	
M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]	
M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	
M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]	
M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	
M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	
M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	
M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	
M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	
M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	
M_A_DQ48	AY31	DDR0_DQ[48]/DDR1_DQ[32]	
M_A_DQ49	AW31	DDR0_DQ[49]/DDR1_DQ[33]	
M_A_DQ50	AY29	DDR0_DQ[50]/DDR1_DQ[34]	
M_A_DQ51	AW29	DDR0_DQ[51]/DDR1_DQ[35]	
M_A_DQ52	BB31	DDR0_DQ[52]/DDR1_DQ[36]	
M_A_DQ53	BA31	DDR0_DQ[53]/DDR1_DQ[37]	
M_A_DQ54	BA29	DDR0_DQ[54]/DDR1_DQ[38]	
M_A_DQ55	BB29	DDR0_DQ[55]/DDR1_DQ[39]	
M_A_DQ56	AY27	DDR0_DQ[56]/DDR1_DQ[40]	
M_A_DQ57	AW27	DDR0_DQ[57]/DDR1_DQ[41]	
M_A_DQ58	AY25	DDR0_DQ[58]/DDR1_DQ[42]	
M_A_DQ59	AW25	DDR0_DQ[59]/DDR1_DQ[43]	
M_A_DQ60	BB27	DDR0_DQ[60]/DDR1_DQ[44]	
M_A_DQ61	BA27	DDR0_DQ[61]/DDR1_DQ[45]	
M_A_DQ62	BA25	DDR0_DQ[62]/DDR1_DQ[46]	
M_A_DQ63	BB25	DDR0_DQ[63]/DDR1_DQ[47]	
M_B_DQ48	AU27	DDR1_DQ[48]	
M_B_DQ49	AT27	DDR1_DQ[49]	
M_B_DQ50	AT25	DDR1_DQ[50]	
M_B_DQ51	AU25	DDR1_DQ[51]	
M_B_DQ52	AP27	DDR1_DQ[52]	
M_B_DQ53	AN27	DDR1_DQ[53]	
M_B_DQ54	AN25	DDR1_DQ[54]	
M_B_DQ55	AP25	DDR1_DQ[55]	
M_B_DQ56	AT22	DDR1_DQ[56]	
M_B_DQ57	AU22	DDR1_DQ[57]	
M_B_DQ58	AU21	DDR1_DQ[58]	
M_B_DQ59	AT21	DDR1_DQ[59]	
M_B_DQ60	AN22	DDR1_DQ[60]	
M_B_DQ61	AP22	DDR1_DQ[61]	
M_B_DQ62	AP21	DDR1_DQ[62]	
M_B_DQ63	AN21	DDR1_DQ[63]	

NIL-DDR CH - B

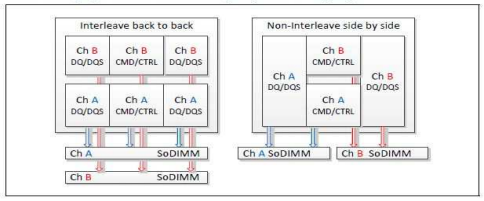
		DDR1_CKN[0]	AN45
		DDR1_CKN[1]	AN46
		DDR1_CKP[0]	AP45
		DDR1_CKP[1]	AP46
		DDR1_CKE[0]	AN56
		DDR1_CKE[1]	AP55
		DDR1_CKE[2]	AN55
		DDR1_CKE[3]	AP53
		DDR1_CS#[0]	BB42
		DDR1_CS#[1]	AY42
		DDR1_ODT[0]	BA42
		DDR1_ODT[1]	AW42
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]		AY48	M_B_A5
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]		AP50	M_B_A9
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]		BA48	M_B_A6
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]		BB48	M_B_A8
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]		AP48	M_B_A7
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]		AP52	M_B_BG#0
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]		AN50	M_B_A12
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]		AN48	M_B_A11
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#		AN53	M_B_ACT#
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]		AN52	M_B_BG#1
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]		BA43	M_B_A13
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]		AY43	M_B_CAS#
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]		AY44	M_B_WE#
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]		AW44	M_B_RAS#
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]		BB44	M_B_BS#0
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]		AY47	M_B_A2
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]		BA44	M_B_BS#1
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]		AW46	M_B_A10
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]		AY46	M_B_A1
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]		BA46	M_B_A0
DDR1_MA[3]		BB46	M_B_A3
DDR1_MA[4]		BA47	M_B_A4
DDR0_DQSN[4]/DDR1_DQSN[0]		BA38	M_A_DQSN4
DDR0_DQSP[4]/DDR1_DQSP[0]		AY38	M_A_DQSP4
DDR0_DQSN[5]/DDR1_DQSN[1]		AY34	M_A_DQSN5
DDR0_DQSP[5]/DDR1_DQSP[1]		BA34	M_A_DQSP5
DDR0_DQSN[4]/DDR1_DQSN[2]		AT38	M_B_DQSN4
DDR1_DQSP[4]/DDR1_DQSP[2]		AR38	M_B_DQSP4
DDR1_DQSN[5]/DDR1_DQSN[3]		AT32	M_B_DQSN5
DDR1_DQSP[5]/DDR1_DQSP[3]		AR32	M_B_DQSP5
DDR0_DQSN[6]/DDR1_DQSN[4]		BA30	M_A_DQSN6
DDR0_DQSP[6]/DDR1_DQSP[4]		AY30	M_A_DQSP6
DDR0_DQSN[7]/DDR1_DQSN[5]		AY26	M_A_DQSN7
DDR0_DQSP[7]/DDR1_DQSP[5]		BA26	M_A_DQSP7
DDR1_DQSN[6]		AR25	M_B_DQSN6
DDR1_DQSP[6]		AR27	M_B_DQSP6
DDR1_DQSN[7]		AT22	M_B_DQSN7
DDR1_DQSP[7]		AR21	M_B_DQSP7
DDR1_ALERT#		AN43	M_B_ALERT#
DDR1_PAR		AP43	M_B_PARITY
DRAM_RESET#		AT13	SM_DRAMRST#
DDR_RCOMP[0]		AR18	SM_RCOMP_0
DDR_RCOMP[1]		AT18	SM_RCOMP_1
DDR_RCOMP[2]		AU18	SM_RCOMP_2

M_B_CLKN0	<18>
M_B_CLKN1	<18>
M_B_CLKP0	<18>
M_B_CLKP1	<18>
M_B_CKE0	<18>
M_B_CKE1	<18>
M_B_CS#0	<18>
M_B_CS#1	<18>
M_B_DIM0_ODT0	<18>
M_B_DIM0_ODT1	<18>
M_B_A5	<18>
M_B_A9	<18>
M_B_A6	<18>
M_B_A8	<18>
M_B_A7	<18>
M_B_BG#0	<18>
M_B_A12	<18>
M_B_A11	<18>
M_B_ACT#	<18>
M_B_BG#1	<18>
M_B_A13	<18>
M_B_CAS#	<18>
M_B_WE#	<18>
M_B_RAS#	<18>
M_B_BS#0	<18>
M_B_A2	<18>
M_B_BS#1	<18>
M_B_A10	<18>
M_B_A1	<18>
M_B_A0	<18>
M_B_A3	<18>
M_B_A4	<18>
M_B_ALERT#	<18>
M_B_PARITY	<18>

20mils width

+1.2VSUS
R24 470/F_4
R25 121/F_4
R26 80.6/F_4
R27 100/F_4
DDR3_DRAMRST# <17,18>

Interleave (IL) and Non-Interleave (NIL) Modes Mapping



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 -- SKYLAKE 2/15(DDR4 I/F)	1A

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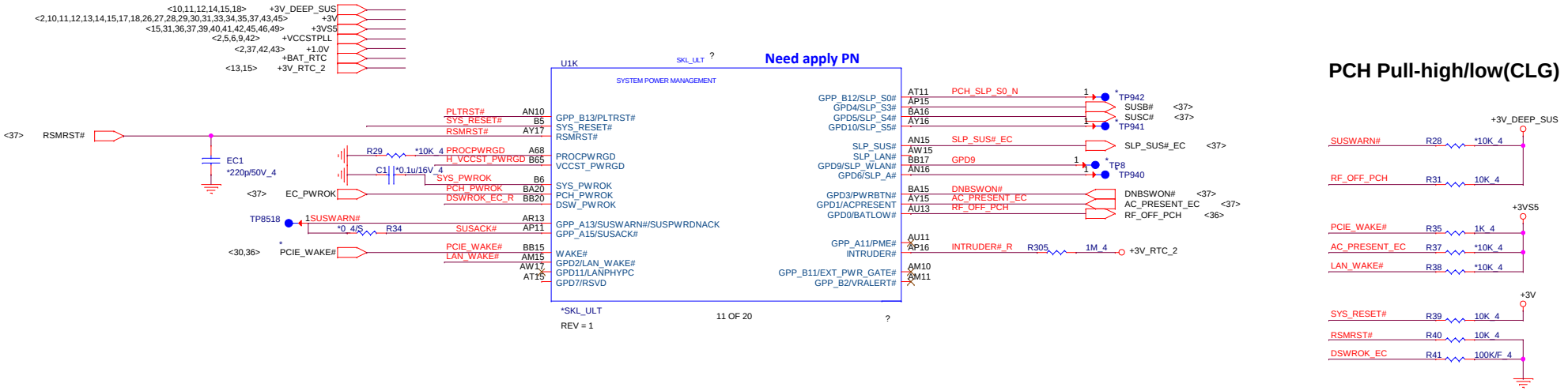
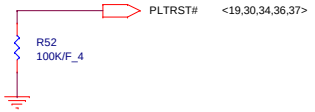


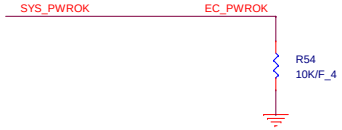
For DS3 Sequence

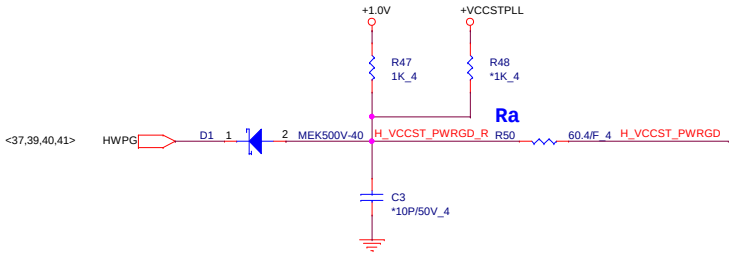
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

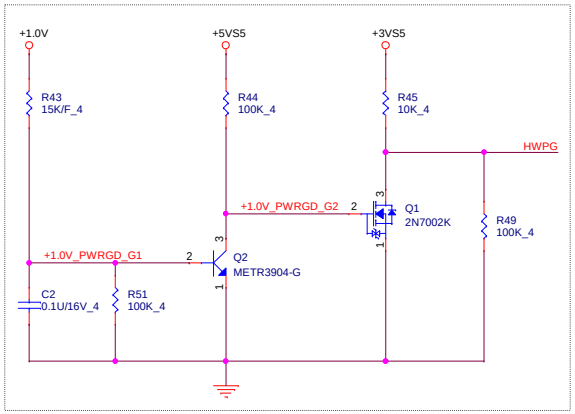


System PWR_OK(CLG)

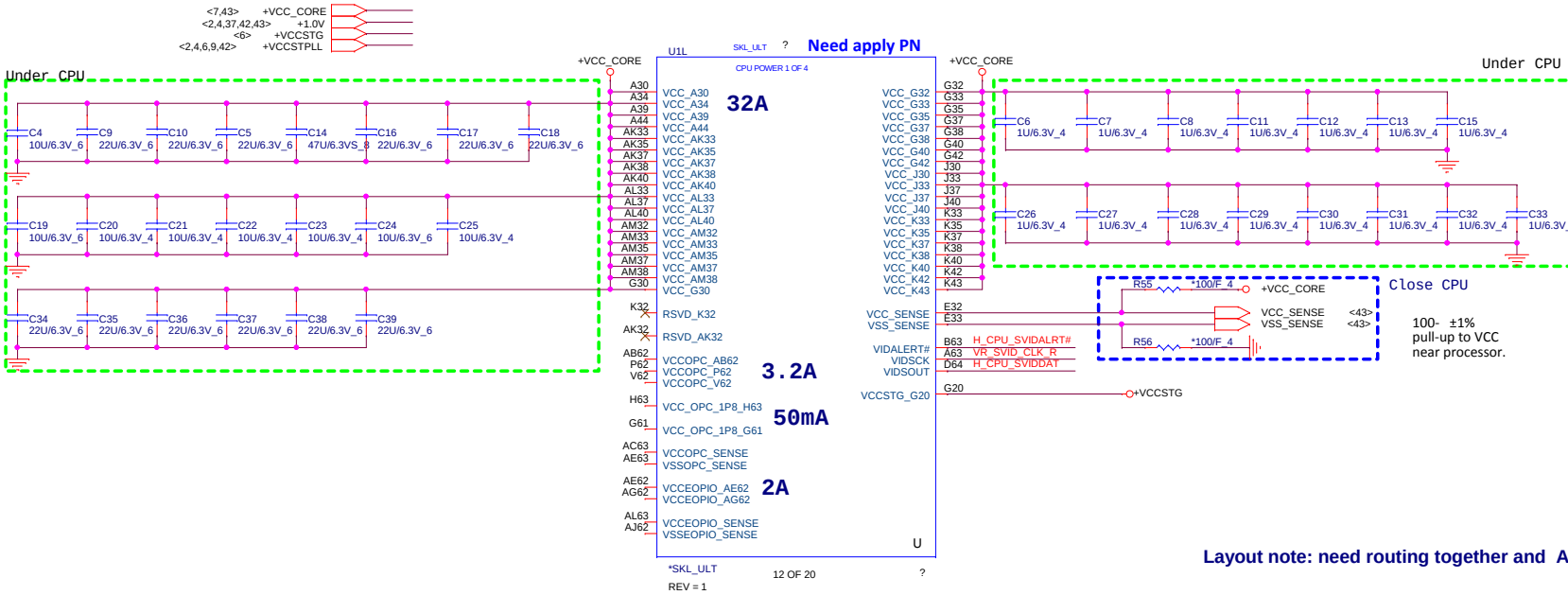


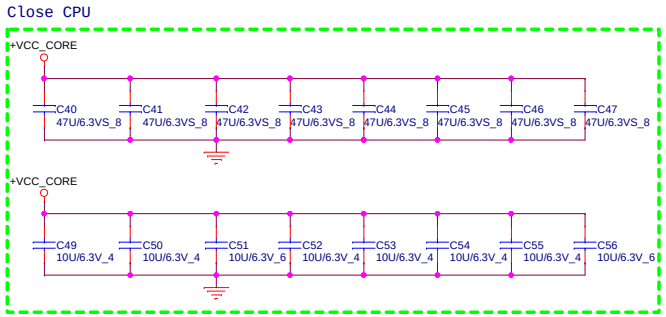


Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

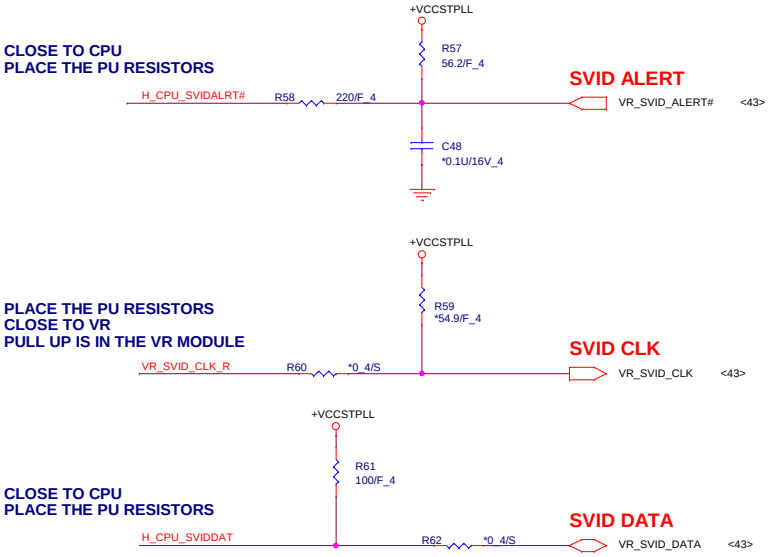


NB5	**PROJECT : 0P1B** Quanta Computer Inc.	
Size: Custom	Document Number: **04 -- SKYLAKE 3/15(PowerManger)**	Rev: 1A
Date: Wednesday, March 08, 2017	Sheet 4 of 51	





Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE 4/15 (POWER-1)	1A

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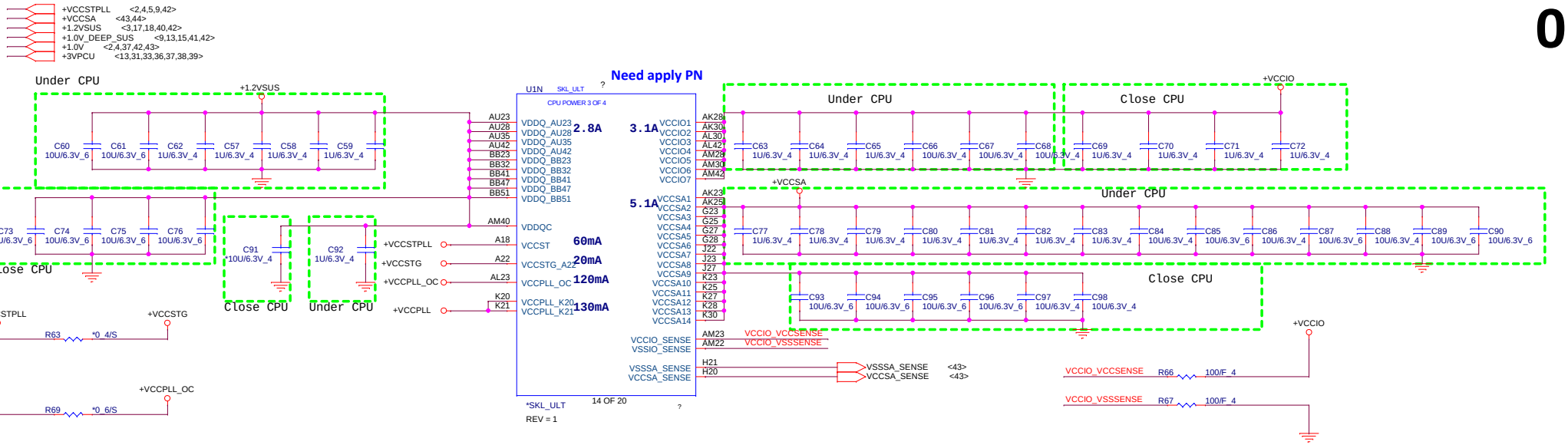
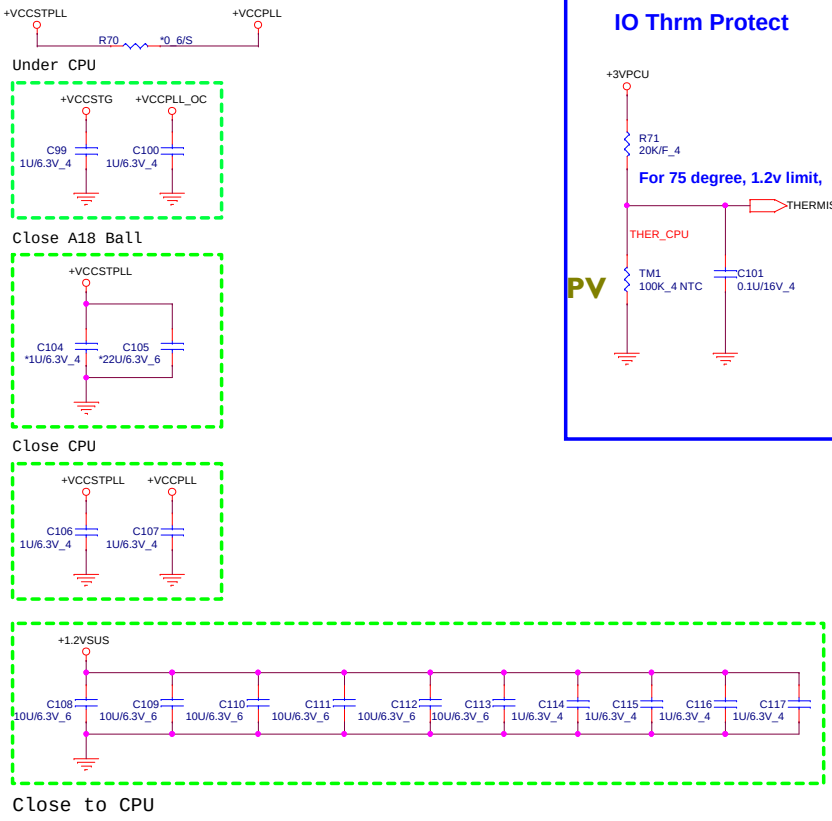
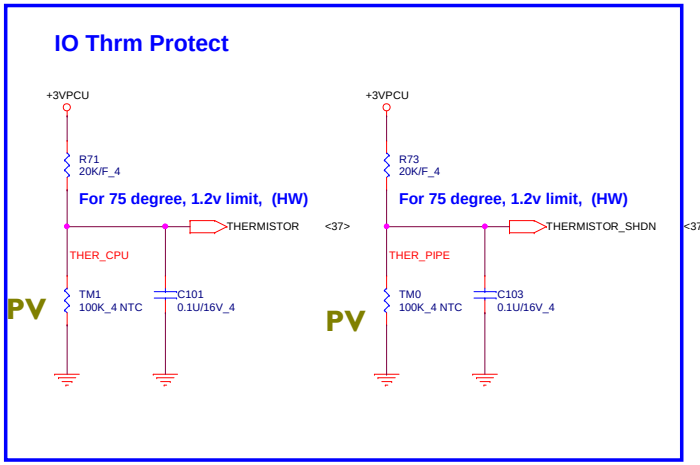




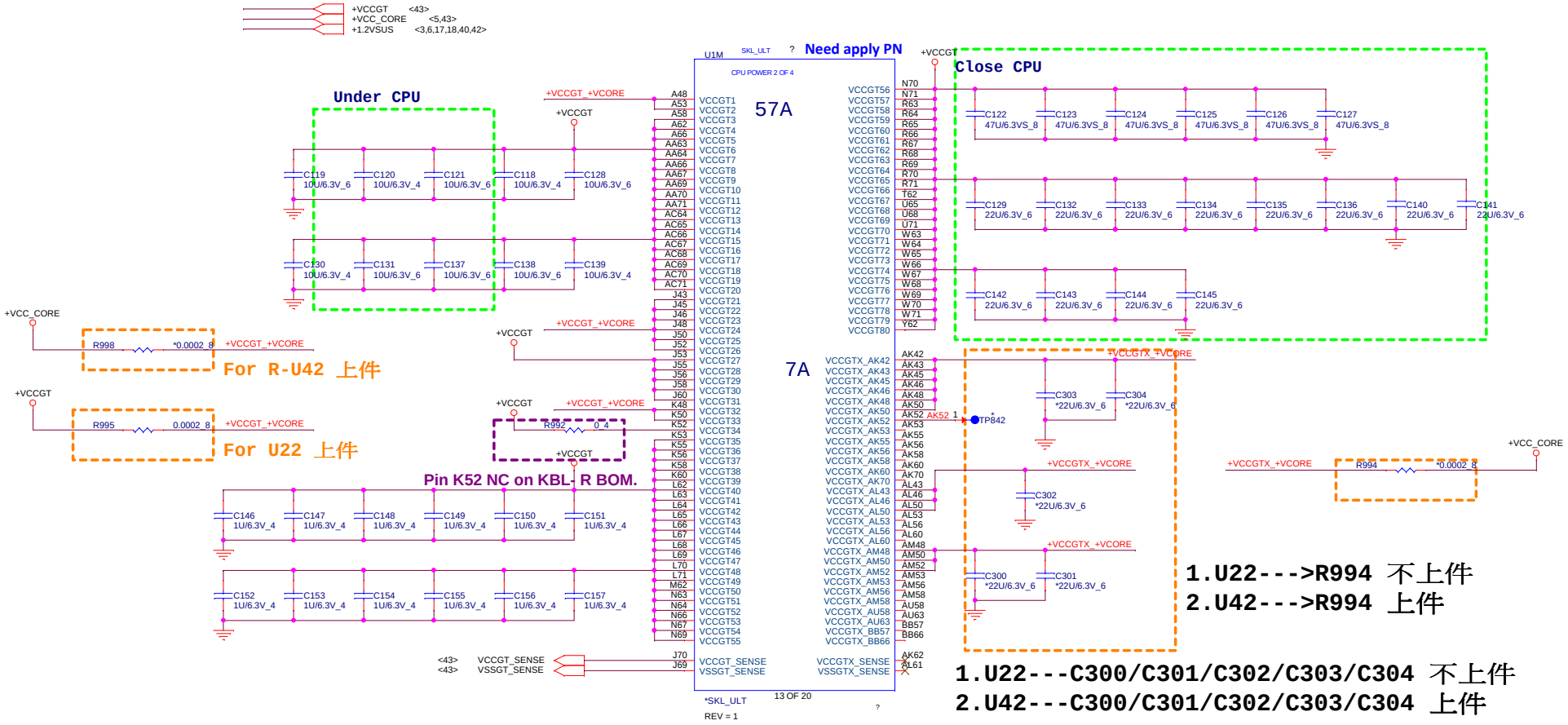


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYLAKE 5/15 (POWER-2)	1A
Date: Wednesday, March 08, 2017	Sheet 6 of 51	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	07 -- SKYLAKE 6/15 (POWER-3)	1A

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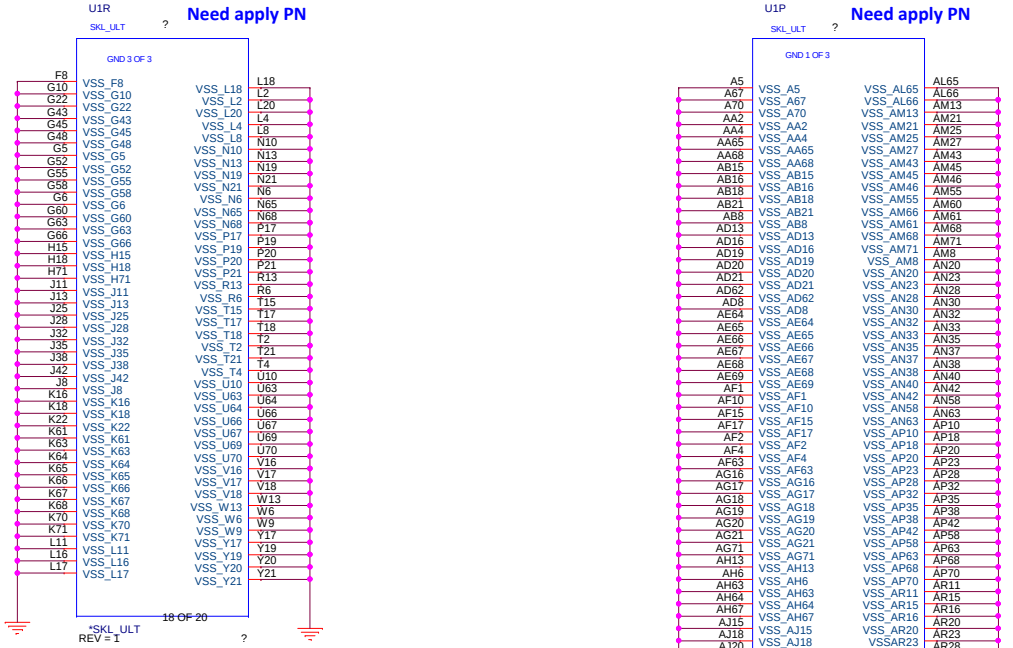
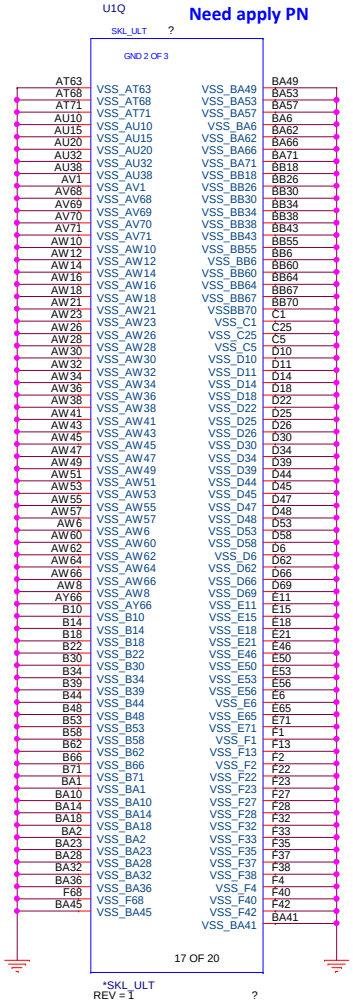
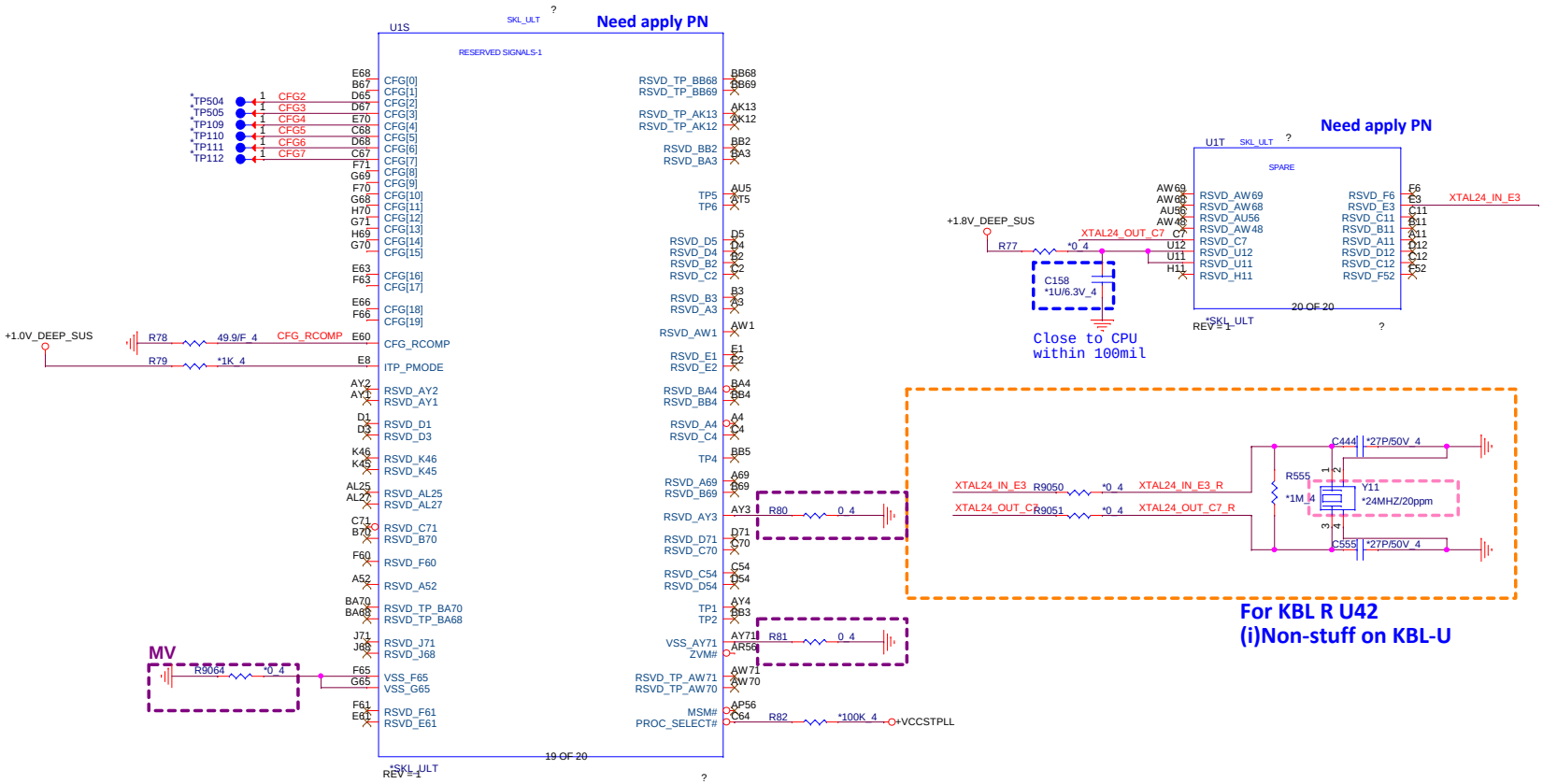




NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A
Date: Wednesday, March 08, 2017	Sheet 8 of 51	



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

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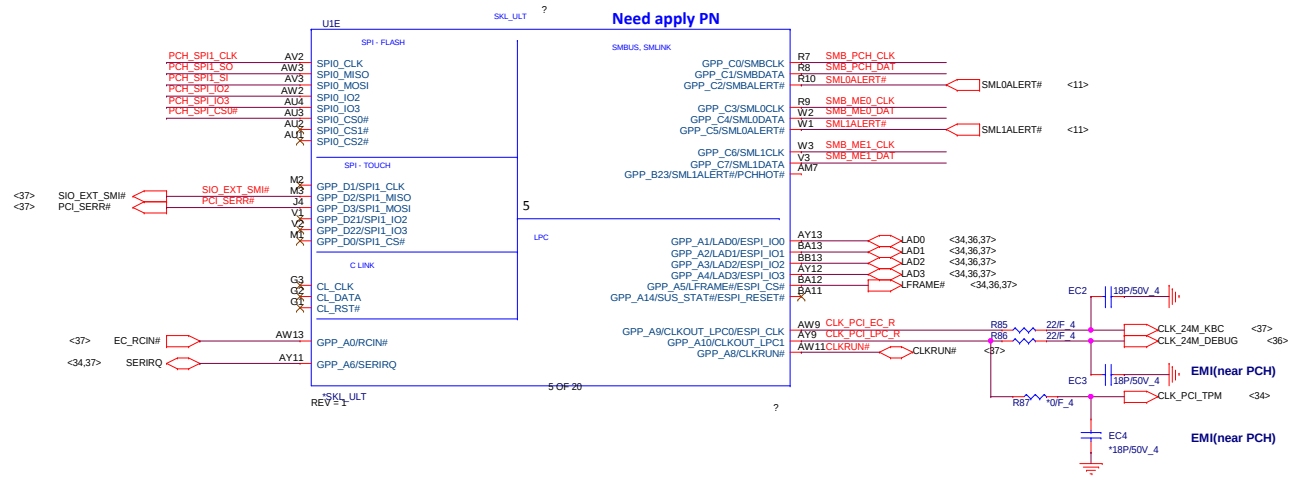
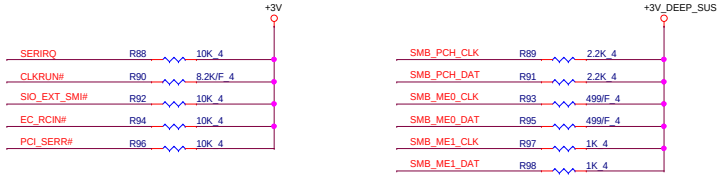
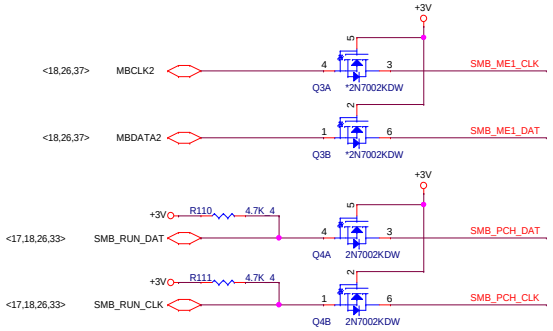
+3V_DEEP_SUS <4,11,12,14,15,18>
+3V <2,4,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+5V <26,27,28,29,33,35,36,45>
+1.0V <2,4,37,42,43>
+3VS5 <4,15,31,36,37,39,40,41,42,45,46,49>



GPIO Pull UP



SMBus/Pull-up(CLG)



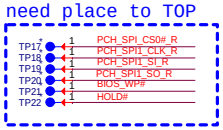
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

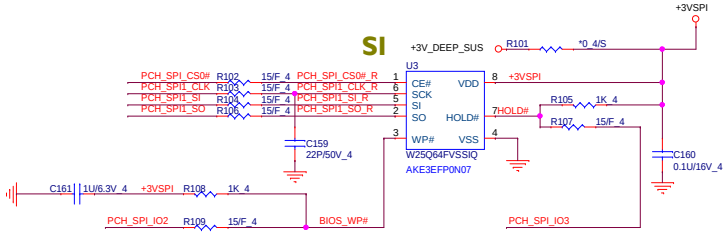
PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)



NB5
PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE 09/15(SPI/LPC/SM)	1A
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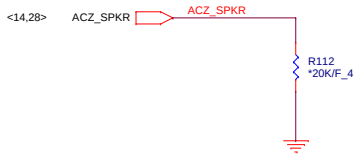
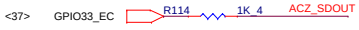
Functional Strap Definitions

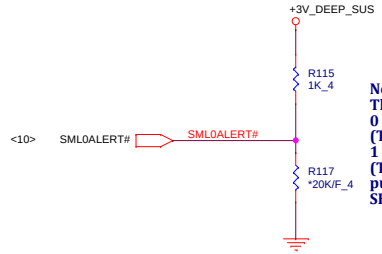
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



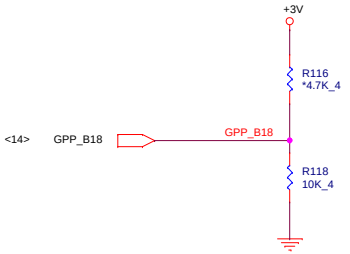
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

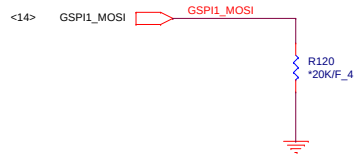




No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

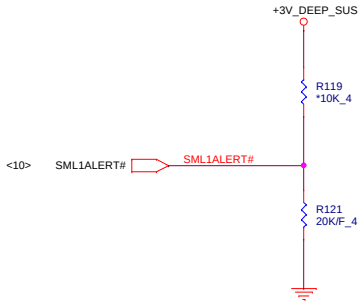


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

NB5	**PROJECT : 0P1B** Quanta Computer Inc.		
	Size: Custom	Document Number: **11 -- SKYLAKE 10/15(HDA)**	Rev: 1A
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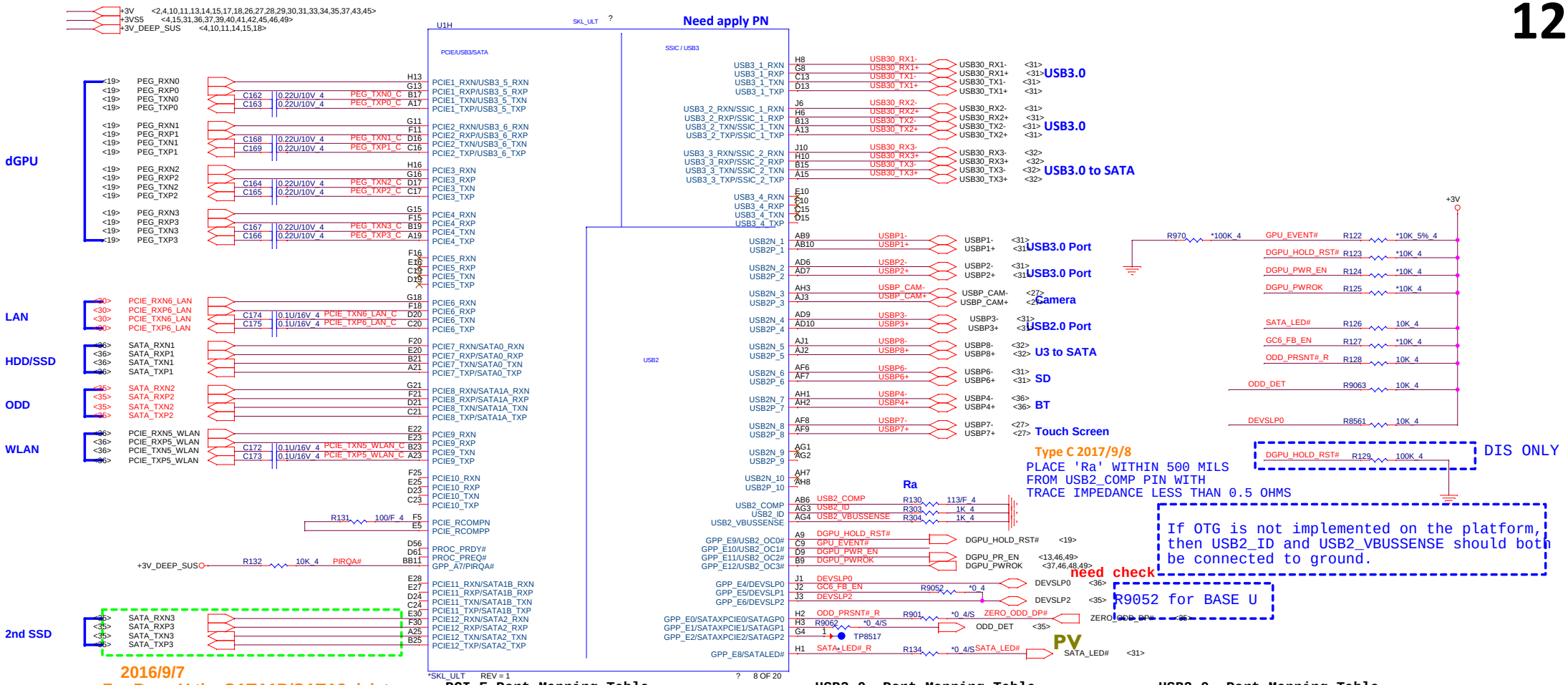

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	Un-used
Port4	dGPU	Port3	WLAN
Port5		Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD/SSD		
Port8	ODD		
Port9	WLAN		
Port10			
Port11			
Port12	2nd SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB
PORT-2	USB3.0 MB
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB
PORT-2	Cobime USB3.0 MB
PORT-3	Webcam
PORT-4	USB2.0 Small Board
PORT-5	USB3.0 to SATA
PORT-6	SD Card
PORT-7	WLAN (BT)
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A
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NB5

+3V_RTC_2 <4,15>
+BAT_RTC
+1.8V_DEEP_SUS <9,15,41,49>
+3V <2,4,10,11,12,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>

VGA
<19> CLK_GFX_N
<19> CLK_GFX_P
CLK_VGA_N
CLK_VGA_P
PCIE_CLKREQ_VGA#

WLAN
<36> CLK_PCIE_WLANN
<36> CLK_PCIE_WLANP
<36> PCIE_CLKREQ_WLAN#
CLK_PCIE_WLANN
CLK_PCIE_WLANP
PCIE_CLKREQ_WLAN#

LAN
<30> CLK_PCIE_LANN
<30> CLK_PCIE_LANP
<30> PCIE_CLKREQ_LAN#
CLK_PCIE_LANN
CLK_PCIE_LANP
PCIE_CLKREQ_LAN#

PCIE_CLKREQ_CR#
PCIE_CLKREQ_SSD#
PCIE_CLKREQ5#

1005 SWAP CLK RQ Port

U1J SKL_ULT ? Need apply PN
CLOCK SIGNALS
D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#
F43 CLKOUT_ITPXDP_N
E43 CLKOUT_ITPXDP_P
BA17 GPD8/SUSCLK
E37 XTAL24_IN
E35 XTAL24_OUT
E42 XCLK_BIASREF
AM18 RTC_X1
AM20 RTC_X2
AN18 SRTC_RST#
AM16 RTC_RST#
TBT
10 OF 20
*SKL_ULT REV = 1

+1.0V_DEEP_SUS
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

CLK_REQ/Strap Pin(CLG)
+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

GPU CLK REQ
DIS: Stuff
UMA: No Stuff
*PCIE_CLKREQ_VGA#
<12,46,49> DGPU_PR_EN
R850 30K_1%_4
Q850 METR5213-G
C850 0.47u/6.3V_4
R9056 *10K_4

U1I SKL_ULT ? Need apply PN
CSI-2
A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3
C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A33 CSI2_DN6
B33 CSI2_DP6
A32 CSI2_DN7
B32 CSI2_DP7
A29 CSI2_DN8
B29 CSI2_DP8
C29 CSI2_DN9
D29 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11
C37 CSI2_CLKN0
D37 CSI2_CLKP0
C32 CSI2_CLKN1
D32 CSI2_CLKP1
C29 CSI2_CLKN2
D29 CSI2_CLKP2
C26 CSI2_CLKN3
D26 CSI2_CLKP3
E13 CSI2_COMP
B7 GPP_D4/FLASHTRIG
R143 100/F_4
EMMC
AP2 GPP_F13/EMMC_DATA0
AP1 GPP_F14/EMMC_DATA1
AP3 GPP_F15/EMMC_DATA2
AN3 GPP_F16/EMMC_DATA3
AN1 GPP_F17/EMMC_DATA4
AN2 GPP_F18/EMMC_DATA5
AM4 GPP_F19/EMMC_DATA6
AM1 GPP_F20/EMMC_DATA7
AM2 GPP_F21/EMMC_RCLK
AM3 GPP_F22/EMMC_CLK
AP4 GPP_F12/EMMC_CMD
AT1 EMMC_RCOMP
R144 200/F_4
9 OF 20
*SKL_ULT REV = 1

RTC Clock 32.768KHz

C177 15P/50V_4
RTC_X1
Y1 32.768KHZ/20ppm
R147 10M_4
C179 15P/50V_4
RTC_X2

RTC Circuitry(RTC)

30mils
+3V_RTC_2
TP8521
RTC Power trace width 20mils.
+3V_RTC_0
R150 1K_4
+3VPCU
+3V_RTC11
D2 BAT54CW-7-F
C181 1U/6.3V_4
RTC1 RTC Battery
R146 20K/F_4
R149 20K/F_4
C178 1U/6.3V_4
C182 1U/6.3V_4
RTC_RST#
SRTC_RST#
R152 *0_6
R151 10K_4
R153 10K_4
EC_RTC_RST
Q5A 2N7002KDW
Q5B 2N7002KDW
R9061 *0_4
EC_SRTC_RST
PV

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

XTAL24_IN R9048 40.2_4 XTAL24_IN_R
XTAL24_OUT R9049 40.2_4 XTAL24_OUT_R
R148 1M_4
C176 27P/50V_4
Y2 24MHZ/20ppm
C180 27P/50V_4
PV

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Document Number 13 -- SKYLAKE 12/15 (CLK/EMMC)
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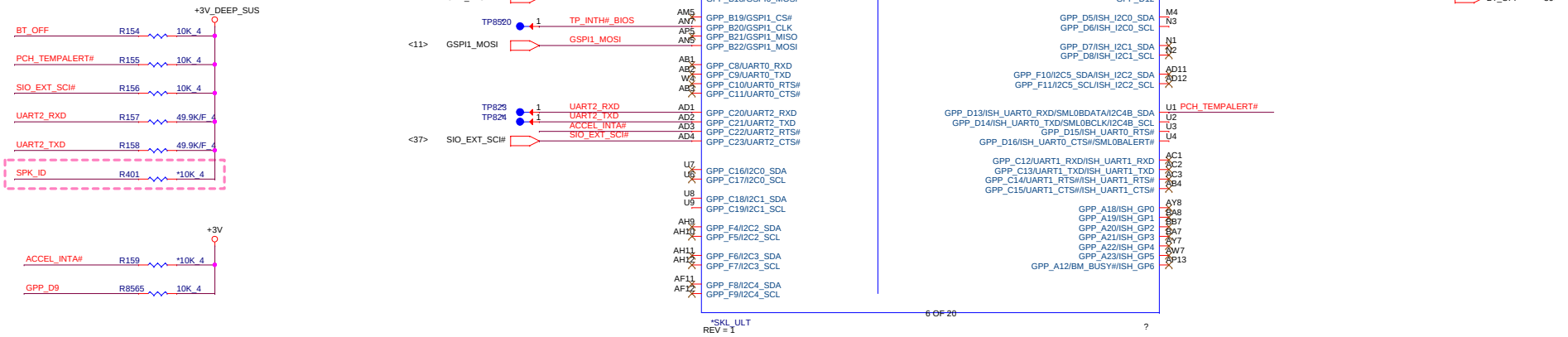
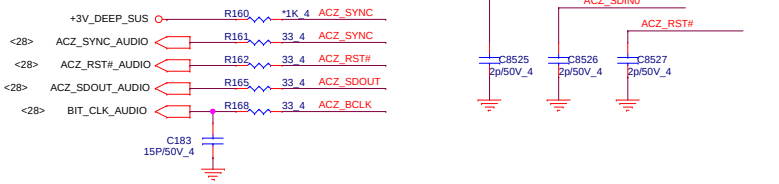
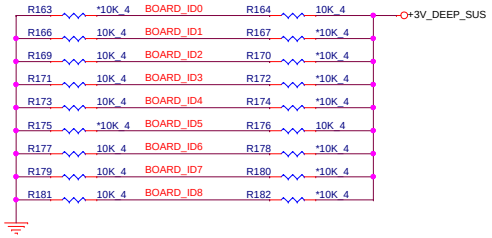
Skylake (GPIO)

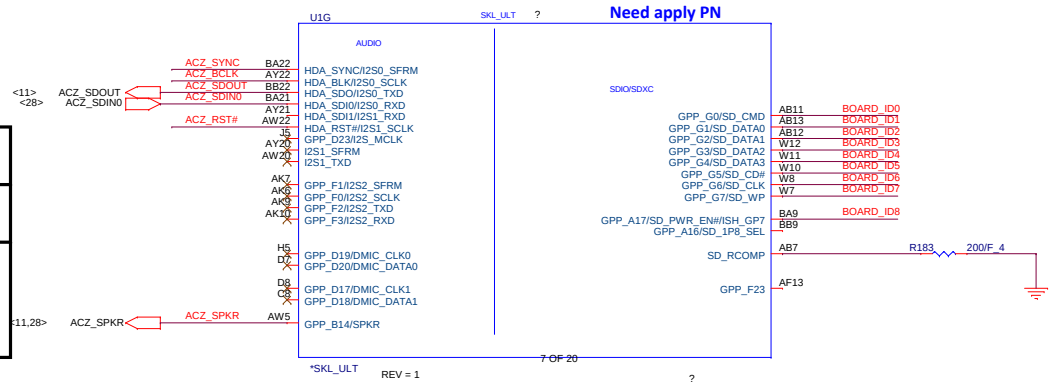
+3V <2,4,10,11,12,13,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+3V_DEEP_SUS <4,10,11,12,15,18>



HDA Bus(CLG)







Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	00 SKL U 01 KBL U 10 Base U 11 KBL R(4+2)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS

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Custom	14 – SKYLAKE 13/15 (GPIO)	1A
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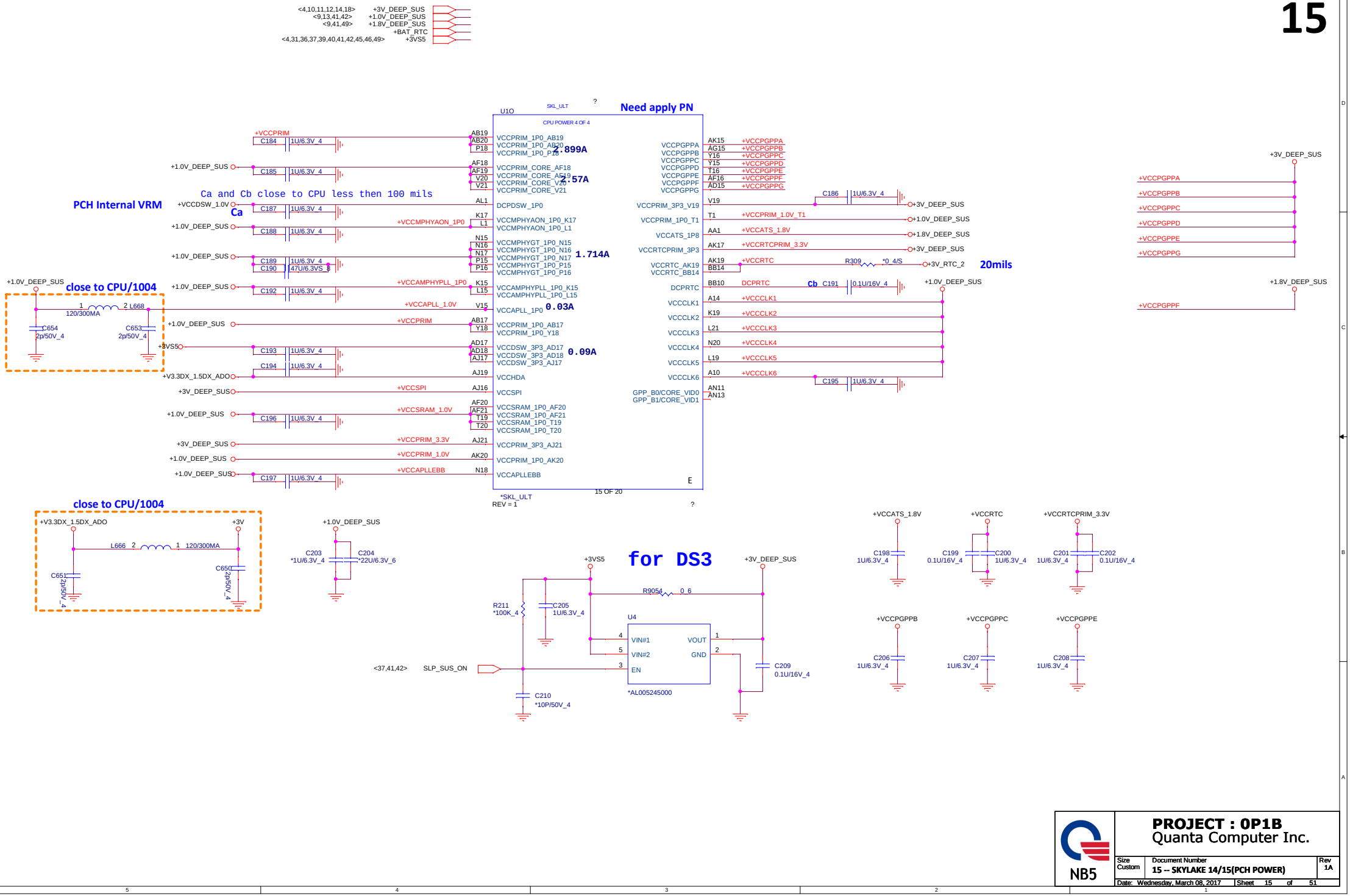

<4,10,11,12,14,18>	+3V_DEEP_SUS
<9,13,41,42>	+1.0V_DEEP_SUS
<9,41,49>	+1.8V_DEEP_SUS
	+BAT_RTC
<4,31,36,37,39,40,41,42,45,46,49>	+3VS5

+VCCPRIM	C184 1U/6.3V_4	AB19, AB20, P18	VCCPRIM_1P0_AB19, VCCPRIM_1P0_AB20, VCCPRIM_1P0_P18
+1.0V_DEEP_SUS	C185 1U/6.3V_4	AF18, AF19, V20, V21	VCCPRIM_CORE_AF18, VCCPRIM_CORE_AF19, VCCPRIM_CORE_V20, VCCPRIM_CORE_V21
+VCCDSW_1.0V	C187 1U/6.3V_4	AL1	DCPDSW_1P0
+1.0V_DEEP_SUS	C188 1U/6.3V_4	K17, L1	VCCMPHYAON_1P0_K17, VCCMPHYAON_1P0_L1
+1.0V_DEEP_SUS	C189 1U/6.3V_4, C190 47U/6.3VS_8	N15, N16, N17, P15, P16	VCCMPHYGT_1P0_N15, VCCMPHYGT_1P0_N16, VCCMPHYGT_1P0_N17, VCCMPHYGT_1P0_P15, VCCMPHYGT_1P0_P16
+1.0V_DEEP_SUS	C192 1U/6.3V_4	K15, L15	VCCAMPHYPLL_1P0_K15, VCCAMPHYPLL_1P0_L15
+VCCAPLL_1.0V		V15	VCCAPLL_1P0
+1.0V_DEEP_SUS		AB17, Y18	VCCPRIM_1P0_AB17, VCCPRIM_1P0_Y18
+3VS5	C193 1U/6.3V_4, C194 1U/6.3V_4	AD17, AD18, AJ17	VCCDSW_3P3_AD17, VCCDSW_3P3_AD18, VCCDSW_3P3_AJ17
+V3.3DX_1.5DX_ADO		AJ19	VCCHDA
+3V_DEEP_SUS		AJ16	VCCSPI
+1.0V_DEEP_SUS	C196 1U/6.3V_4	AF20, AF21, T19, T20	VCCSRAM_1P0_AF20, VCCSRAM_1P0_AF21, VCCSRAM_1P0_T19, VCCSRAM_1P0_T20
+3V_DEEP_SUS		AJ21	VCCPRIM_3P3_AJ21
+1.0V_DEEP_SUS		AK20	VCCPRIM_1P0_AK20
+1.0V_DEEP_SUS	C197 1U/6.3V_4	N18	VCCAPLLEBB

VCCPGPPA	AK15	+VCCPGPPA
VCCPGPPB	AG15	+VCCPGPPB
VCCPGPPC	Y16	+VCCPGPPC
VCCPGPPD	Y15	+VCCPGPPD
VCCPGPPE	T16	+VCCPGPPE
VCCPGPPF	AF16	+VCCPGPPF
VCCPGPPG	AD15	+VCCPGPPG
VCCPRIM_3P3_V19	V19	C186 1U/6.3V_4 → +3V_DEEP_SUS
VCCPRIM_1P0_T1	T1	+VCCPRIM_1.0V_T1 → +1.0V_DEEP_SUS
VCCATS_1P8	AA1	+VCCATS_1.8V → +1.8V_DEEP_SUS
VCCRTCPRIM_3P3	AK17	+VCCRTCPRIM_3.3V → +3V_DEEP_SUS
VCCRTC_AK19	AK19	+VCCRTC R309 *0_4/S → +3V_RTC_2
VCCRTC_BB14	BB14	
DCPRTC	BB10	DCPRTC Cb C191 0.1U/16V_4 → +1.0V_DEEP_SUS
VCCCLK1	A14	+VCCCLK1
VCCCLK2	K19	+VCCCLK2
VCCCLK3	L21	+VCCCLK3
VCCCLK4	N20	+VCCCLK4
VCCCLK5	L19	+VCCCLK5
VCCCLK6	A10	+VCCCLK6 C195 1U/6.3V_4
GPP_B0/CORE_VID0	AN11	
GPP_B1/CORE_VID1	AN13	

+3V_DEEP_SUS: +VCCPGPPA, +VCCPGPPB, +VCCPGPPC, +VCCPGPPD, +VCCPGPPE, +VCCPGPPG

+1.8V_DEEP_SUS: +VCCPGPPF

+1.0V_DEEP_SUS	1 — L668 120/300MA — 2	
	C654 2p/50V_4	C653 2p/50V_4
+V3.3DX_1.5DX_ADO	1 — L666 120/300MA — 2	+3V
	C651 2p/50V_4	C650 2p/50V_4
+1.0V_DEEP_SUS	C203 *1U/6.3V_4	C204 *22U/6.3V_6

+3VS5	R211 *100K_4	C205 1U/6.3V_4
+3V_DEEP_SUS	R9054 0_6	
U4	VIN#1 (4), VIN#2 (5), EN (3)	VOUT (1), GND (2)
<37,41,42> SLP_SUS_ON		
	C210 *10P/50V_4	C209 0.1U/16V_4

+VCCATS_1.8V	C198 1U/6.3V_4	
+VCCRTC	C199 0.1U/16V_4	C200 1U/6.3V_4
+VCCRTCPRIM_3.3V	C201 1U/6.3V_4	C202 0.1U/16V_4
+VCCPGPPB	C206 1U/6.3V_4	
+VCCPGPPC	C207 1U/6.3V_4	
+VCCPGPPE	C208 1U/6.3V_4	

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Quanta Computer Inc.

Size	Document Number	Rev
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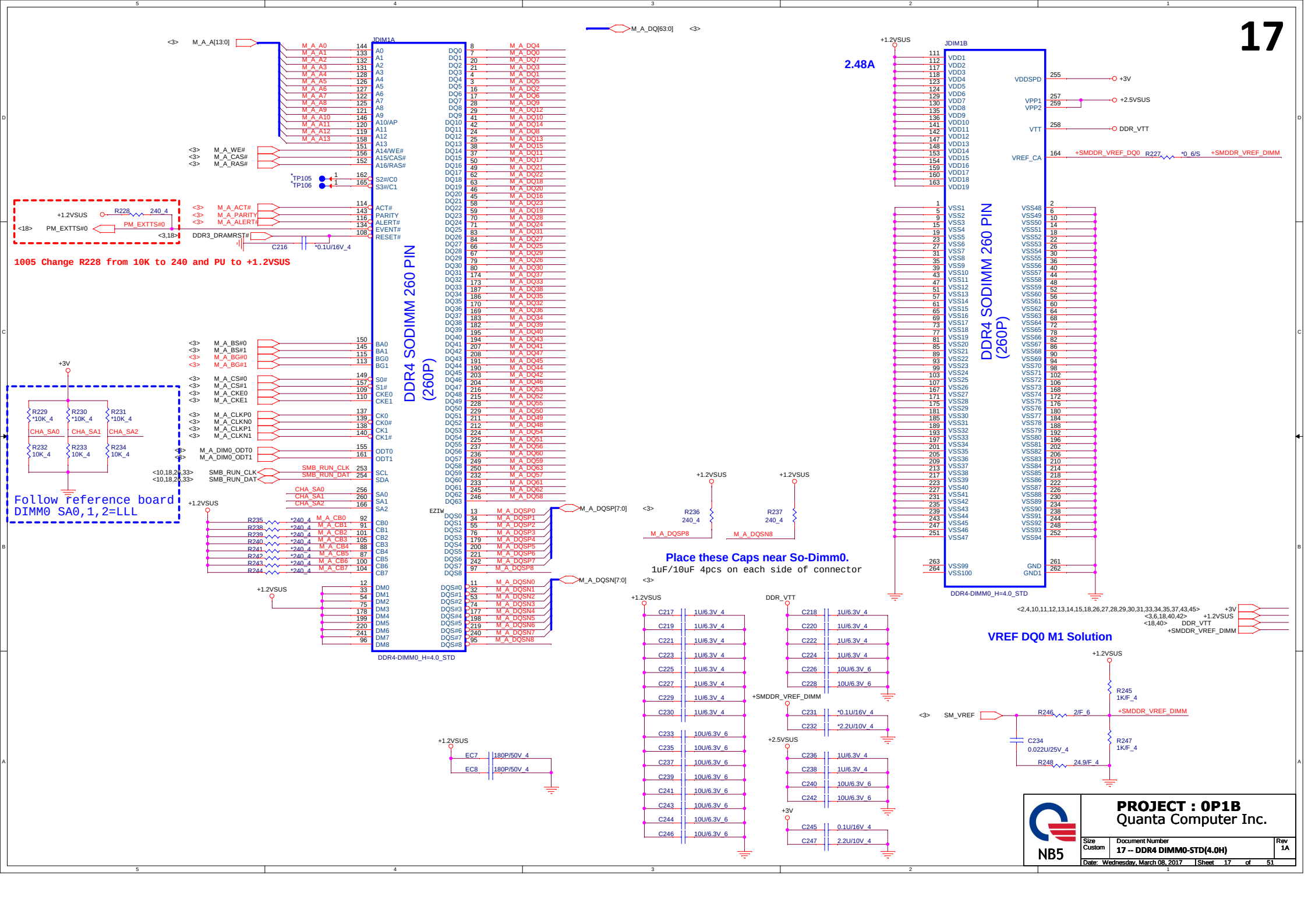
del XDP


JDIM1A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
M_A_DQ[63:0]
M_A_A[13:0]
M_A_DQSP[7:0]
M_A_DQSN[7:0]
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : 0P1B
Quanta Computer Inc.
NB5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
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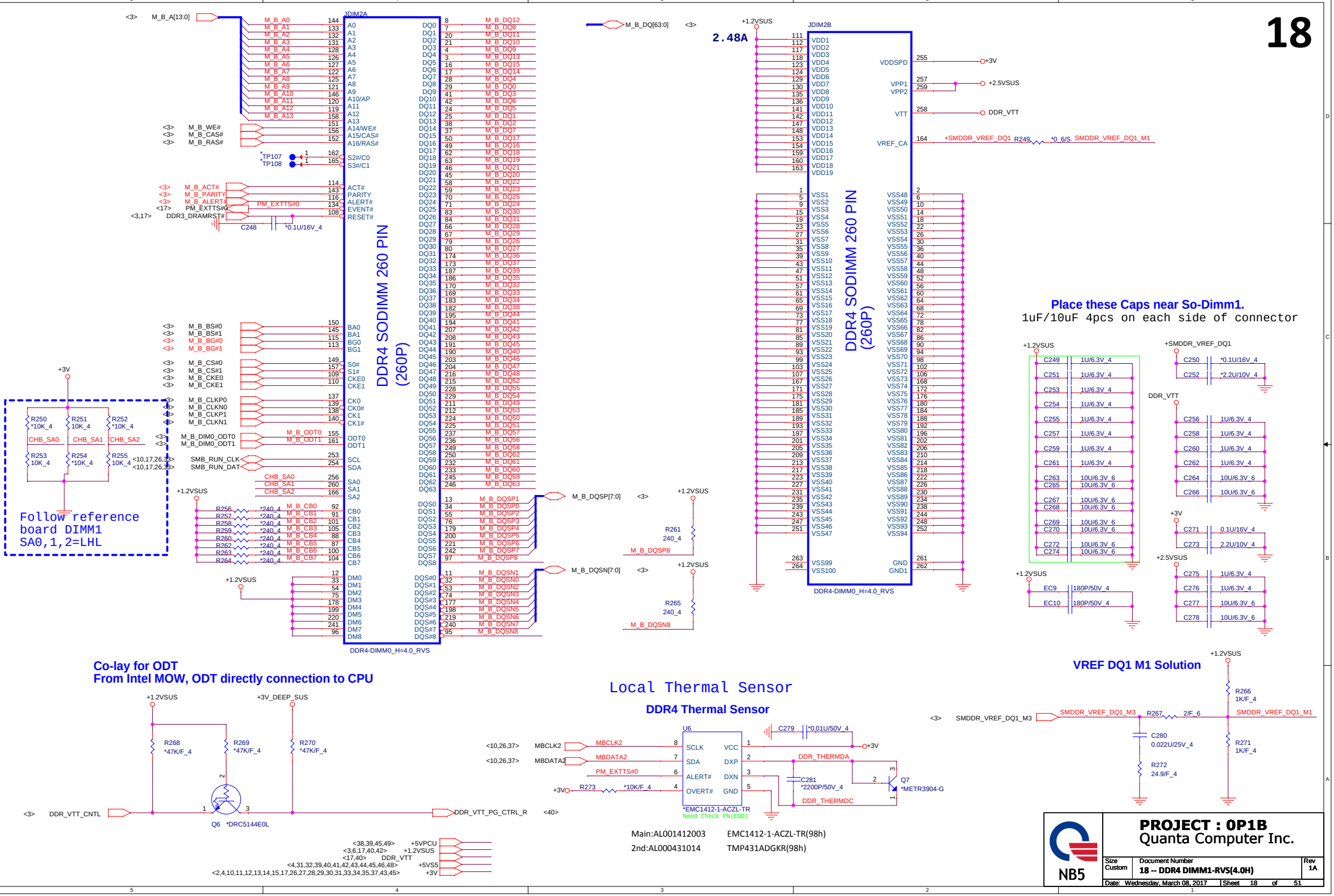

Main:AL001412003 EMC1412-1-ACZL-TR(98h)

2nd:AL000431014 TMP431ADGKR(98h)

NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size: Custom	Document Number: 18 -- DDR4 DIMM1-RVS(4.0H)	Rev: 1A
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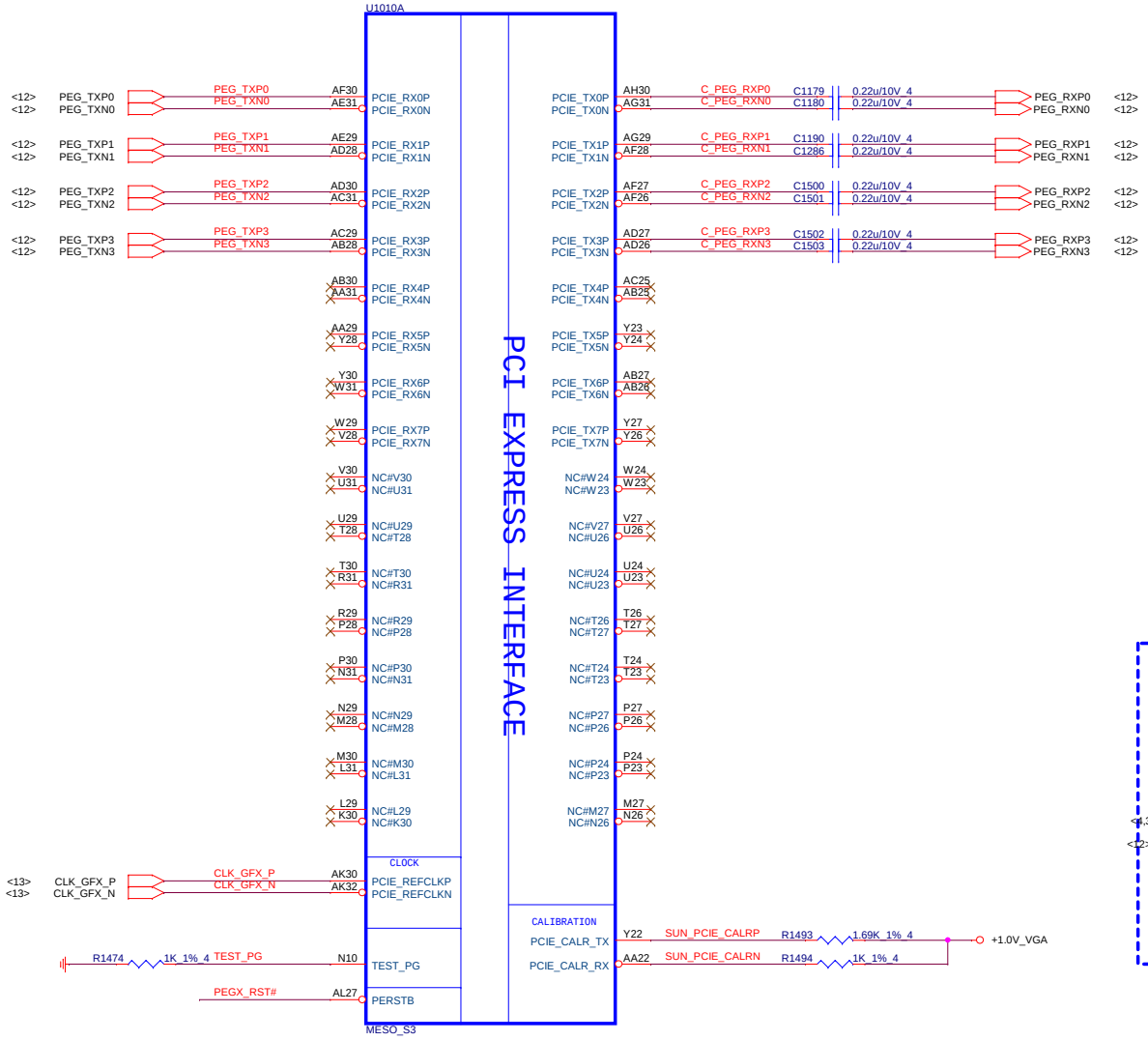

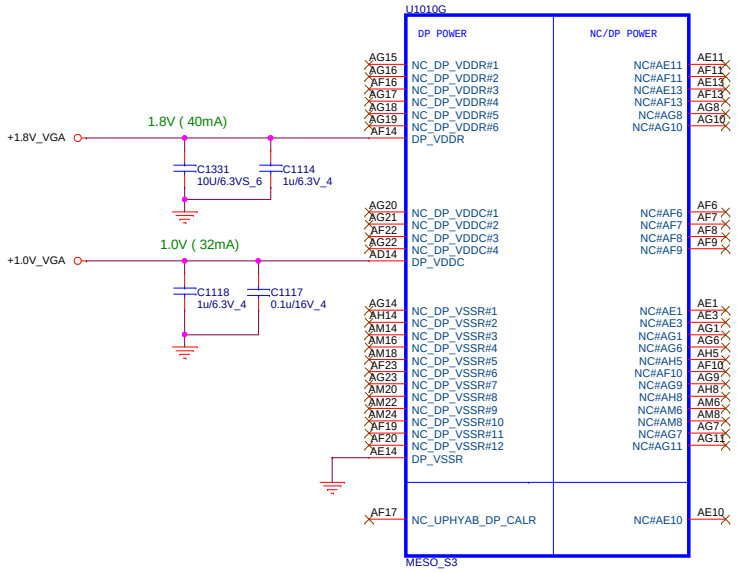

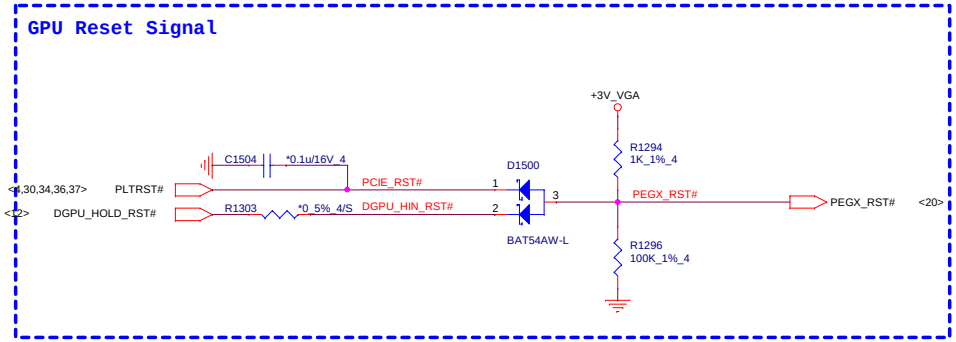

NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size	Document Number M1-70_S3_PCIE/DP POWER	Rev 1A
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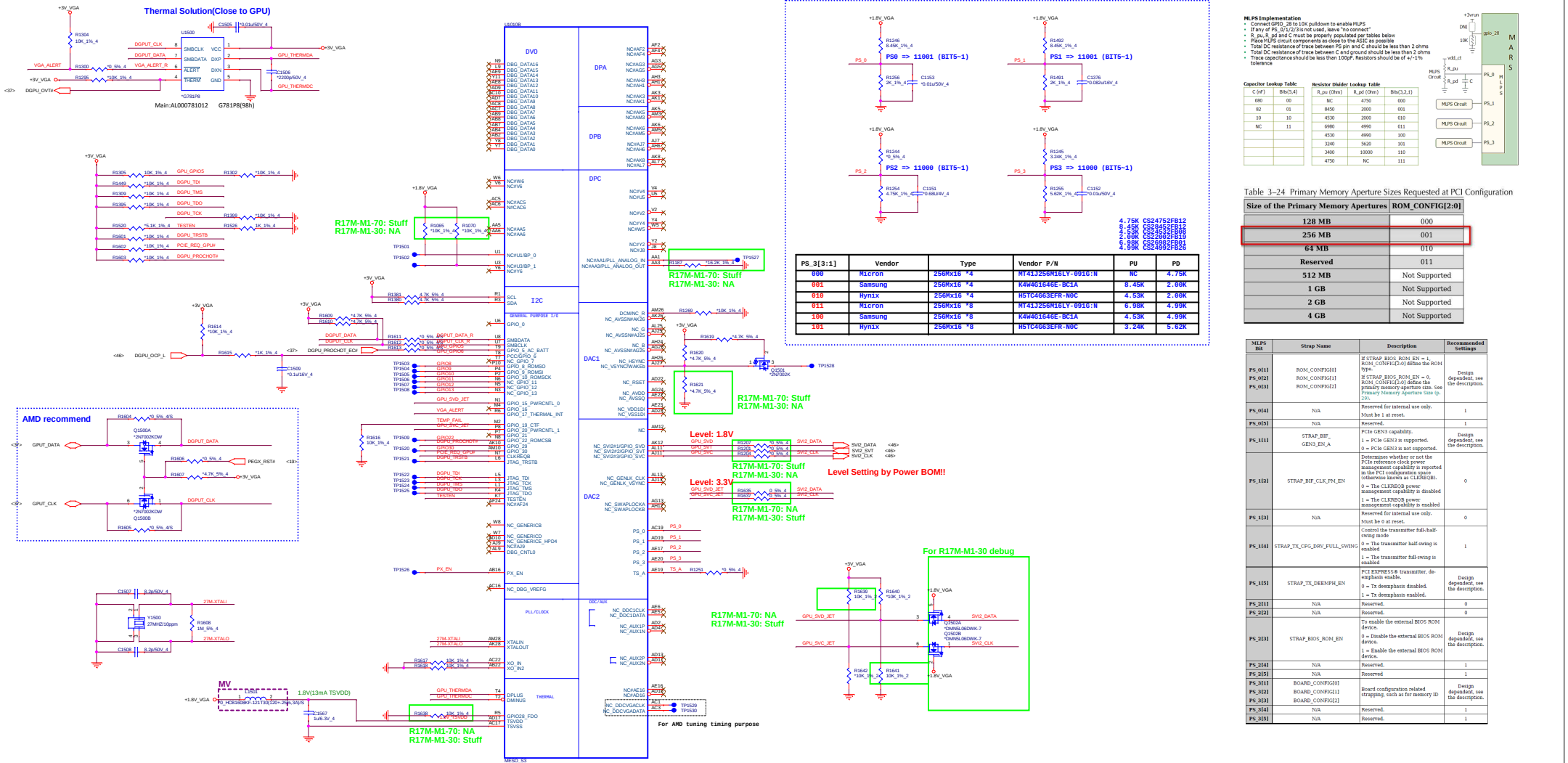


PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Micron	256Mx16 *4	MT41J256M16LY-091G:N	NC	4.75K
001	Samsung	256Mx16 *4	K4W4G1646E-BC1A	8.45K	2.00K
010	Hynix	256Mx16 *4	H5TC4G63EFR-N0C	4.53K	2.00K
011	Micron	256Mx16 *8	MT41J256M16LY-091G:N	6.98K	4.99K
100	Samsung	256Mx16 *8	K4W4G1646E-BC1A	4.53K	4.99K
101	Hynix	256Mx16 *8	H5TC4G63EFR-N0C	3.24K	5.62K

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

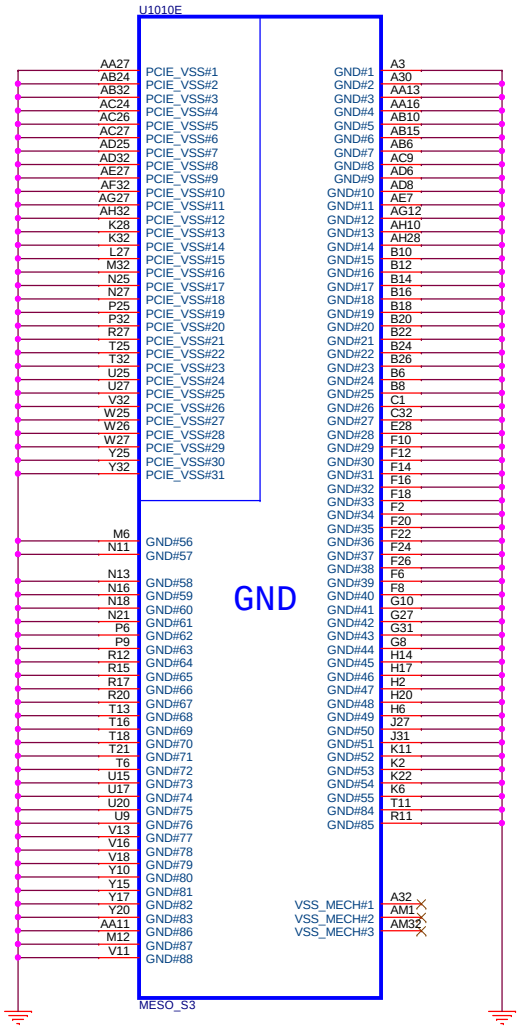
Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Table 3–24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

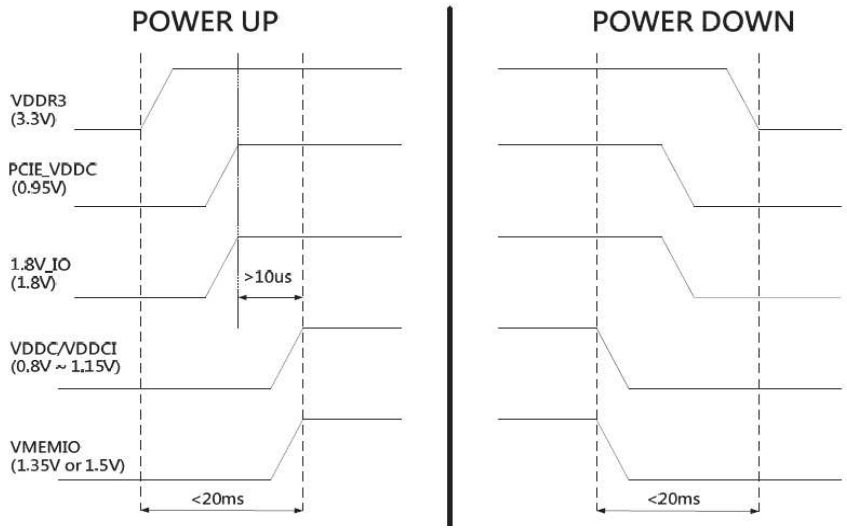
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

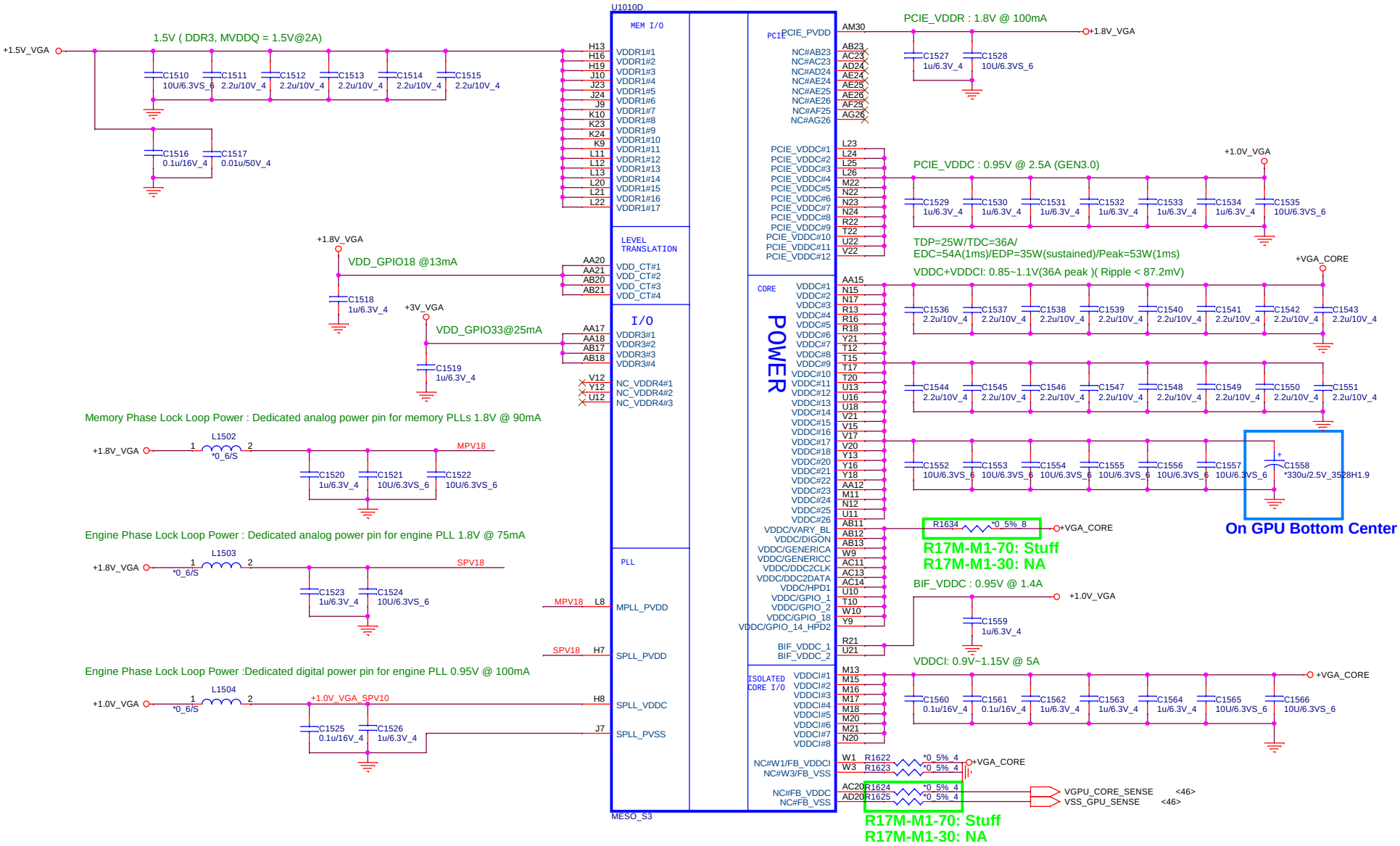
POWER UP / POWER DOWN SEQUENCE



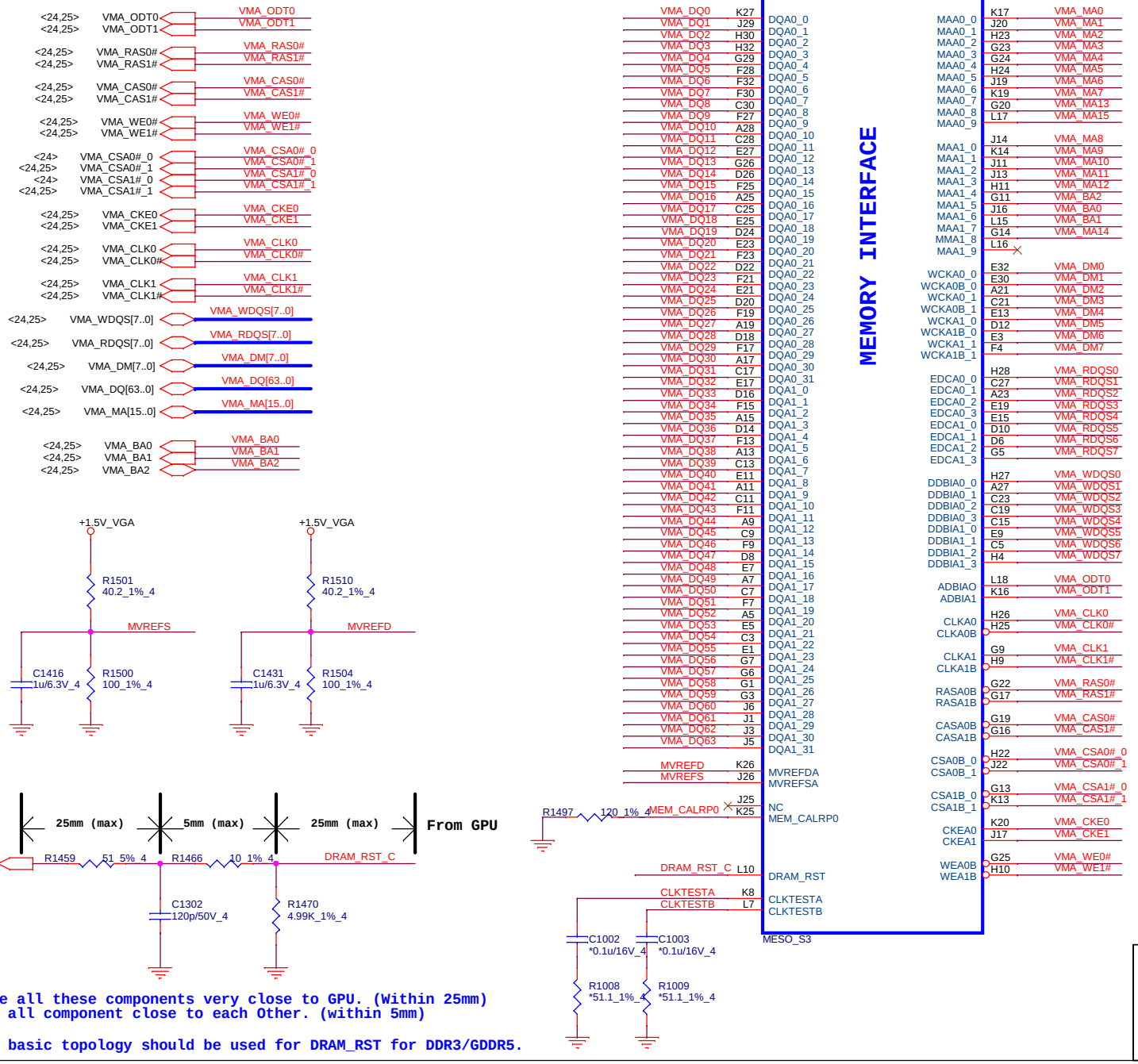
NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	1A
Date: Wednesday, March 08, 2017	Sheet 21 of 51	



NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size	Document Number M1-70_S3_POWER	Rev 1A
Date: Wednesday, March 08, 2017	Sheet 22 of 51	



Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)

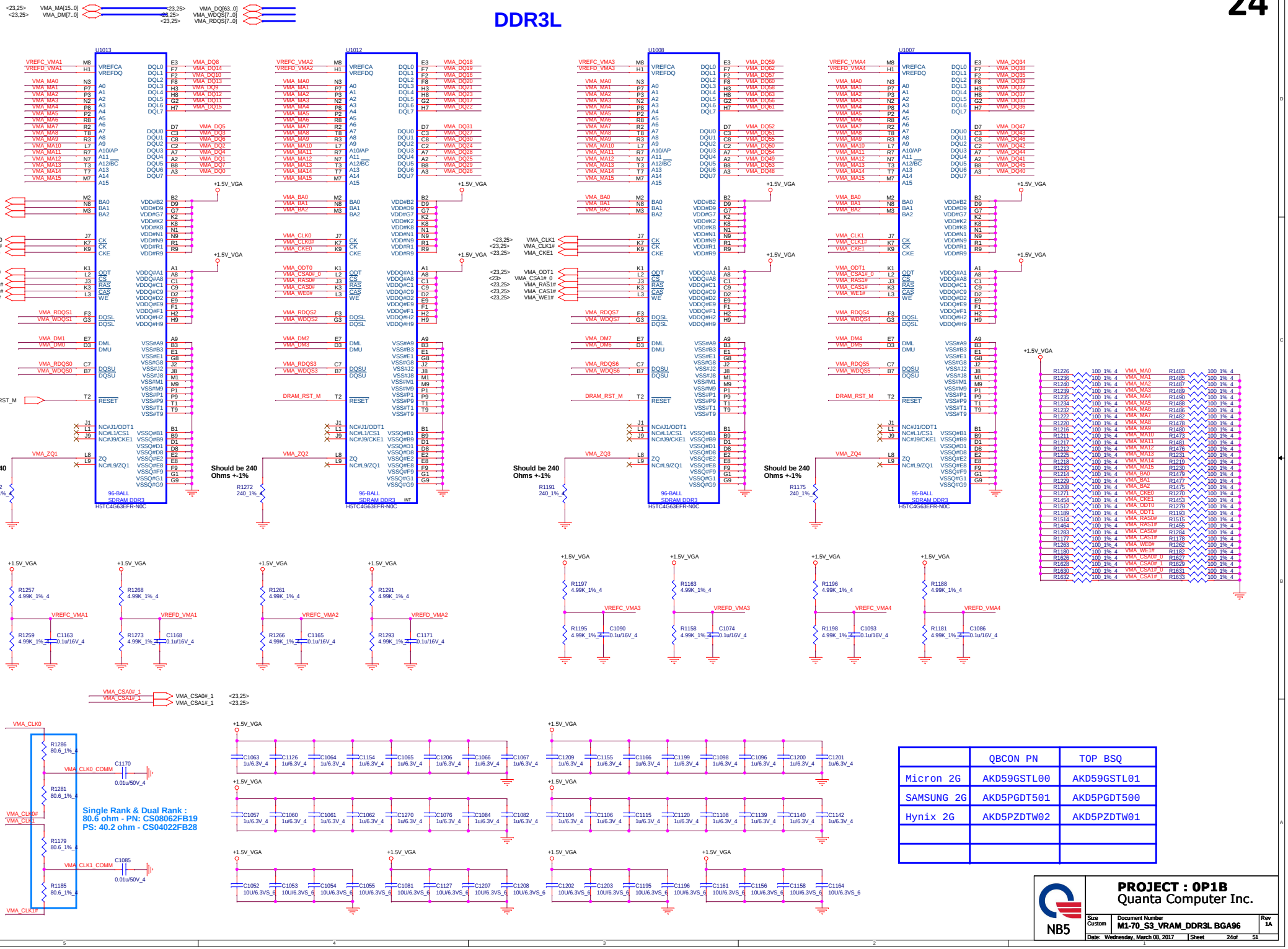
This basic topology should be used for DRAM_RST for DDR3/GDDR5.

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_MEM	1A
Date: Wednesday, March 08, 2017	Sheet 23 of 51	

DDR3L



	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01

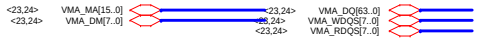
NB5

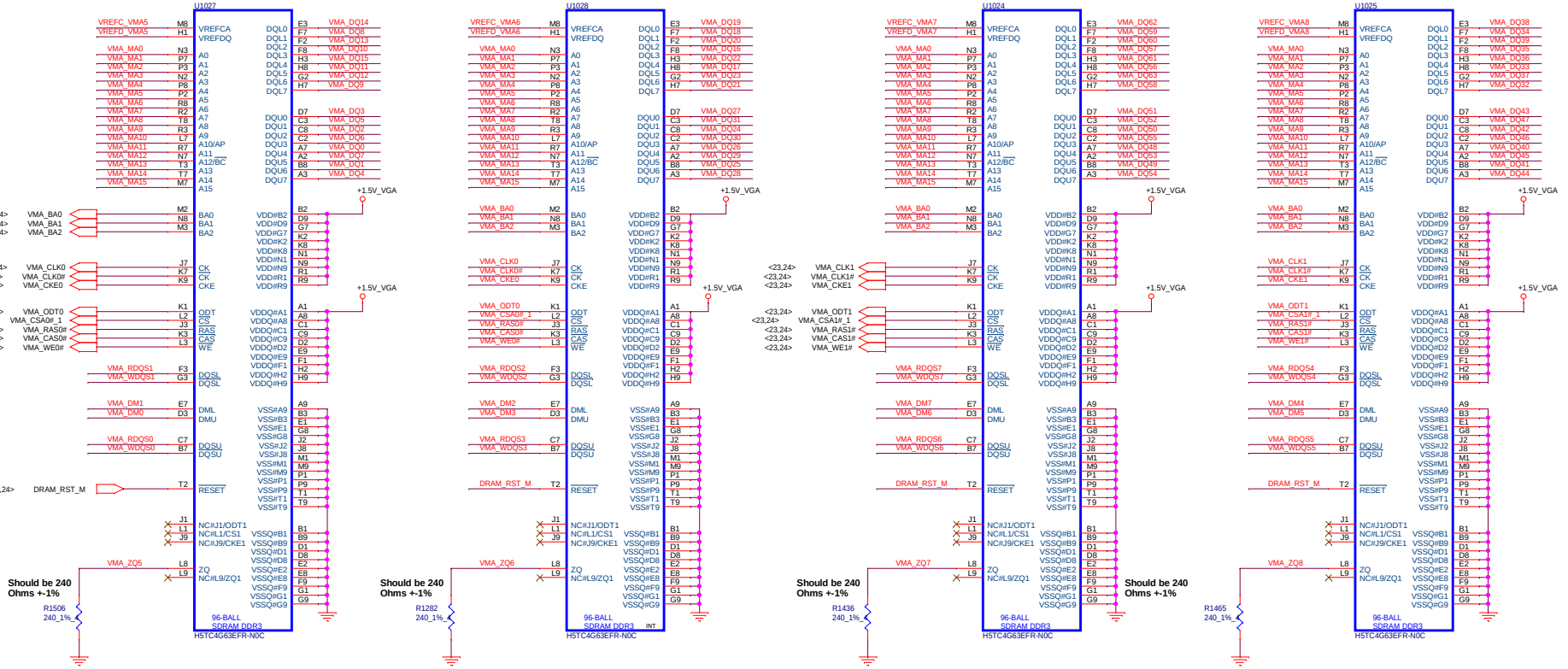
PROJECT : 0P1B
Quanta Computer Inc.

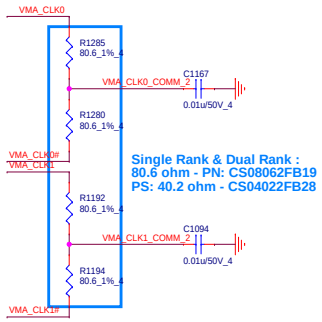
Size	Document Number	Rev
Custom	M1-70_S3_VRAM_DDR3L BGA96	1A

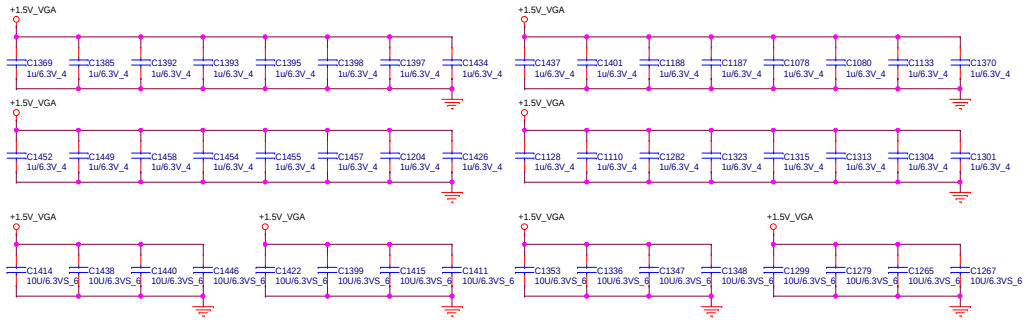
Date: Wednesday, March 08, 2017 | Sheet 24of 51

DDR3L









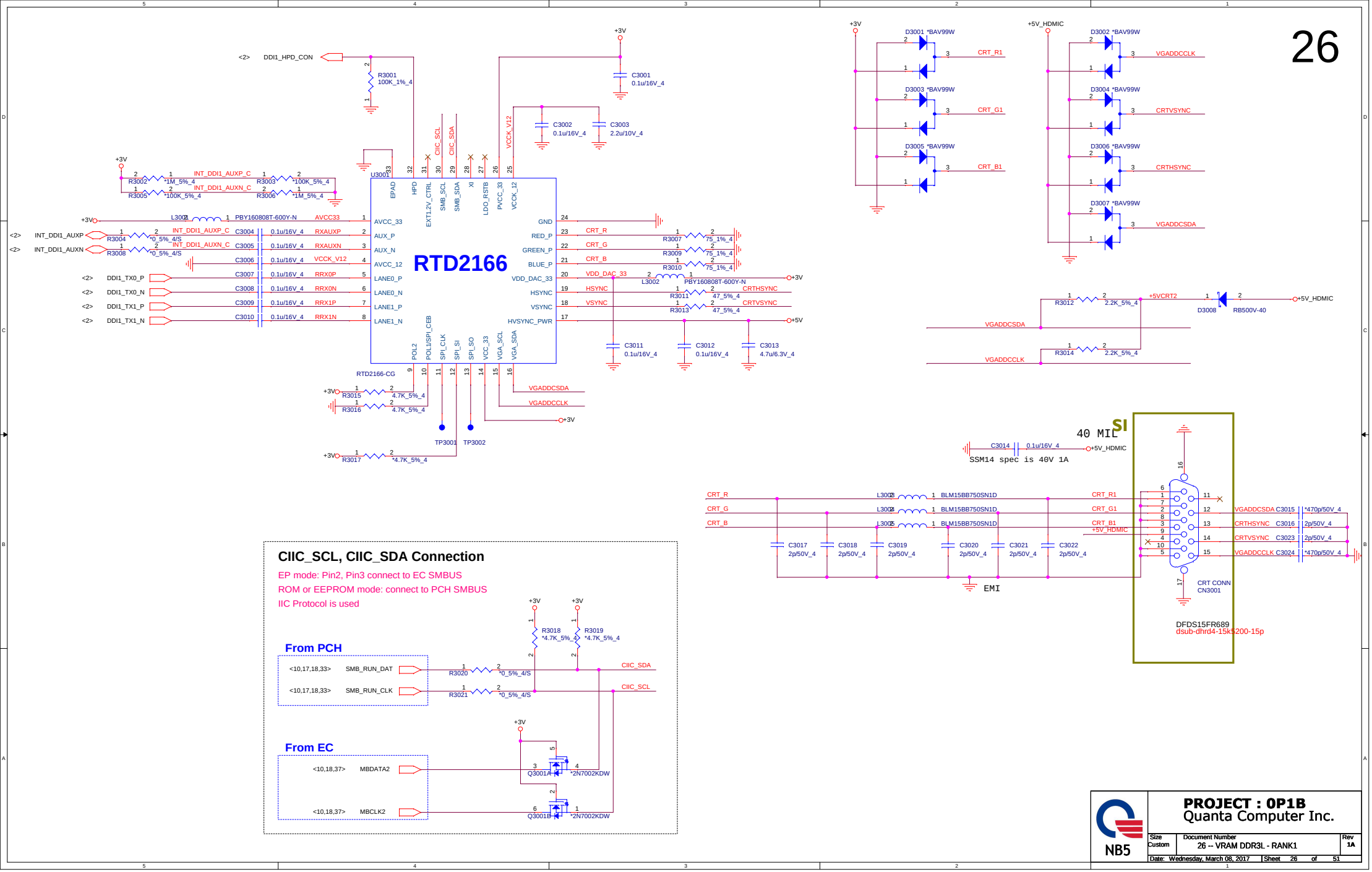
	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01

PROJECT : 0P1B
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	M1-70_S3_VRAM_DDR3L BGA96	1A

Date: Wednesday, March 08, 2017 | Sheet 25of 51



CIIC_SCL, CIIC_SDA Connection

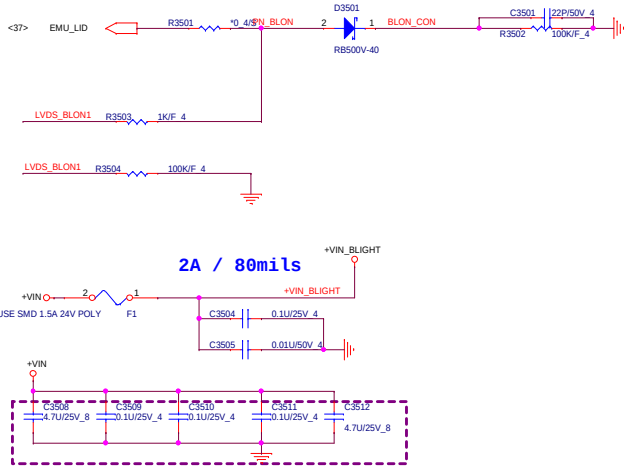
EP mode: Pin2, Pin3 connect to EC SMBUS

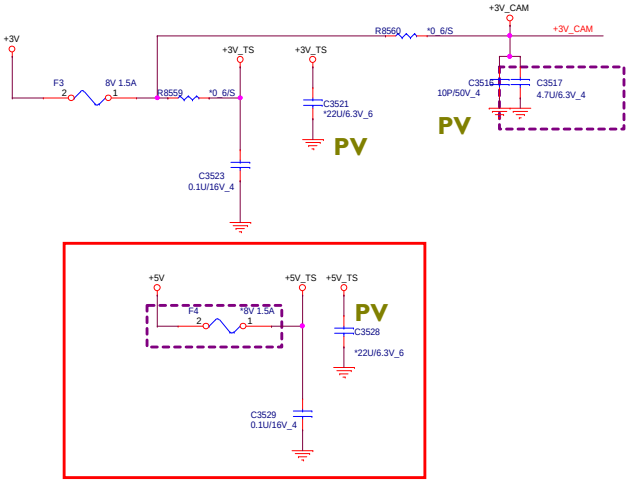
ROM or EEPROM mode: connect to PCH SMBUS

IIC Protocol is used

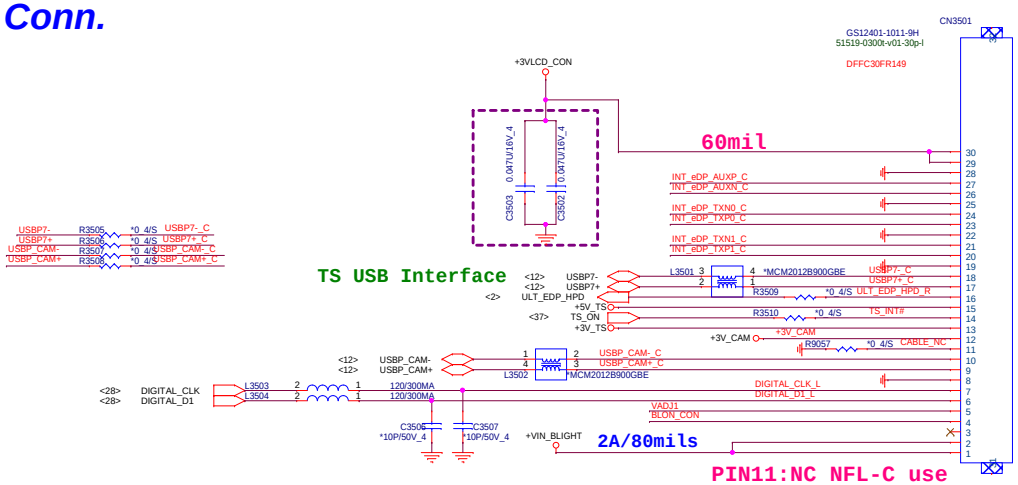
NB5	PROJECT : 0P1B Quanta Computer Inc.		
	Size: Custom	Document Number: 26 -- VRAM DDR3L - RANK1	Rev: 1A
	Date: Wednesday, March 08, 2017	Sheet 26 of 51	

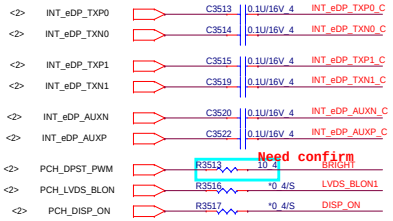
LID Switch

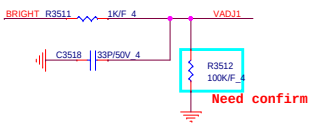


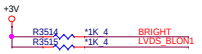


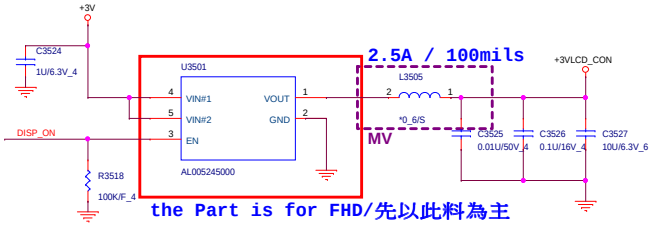
eDP Conn.





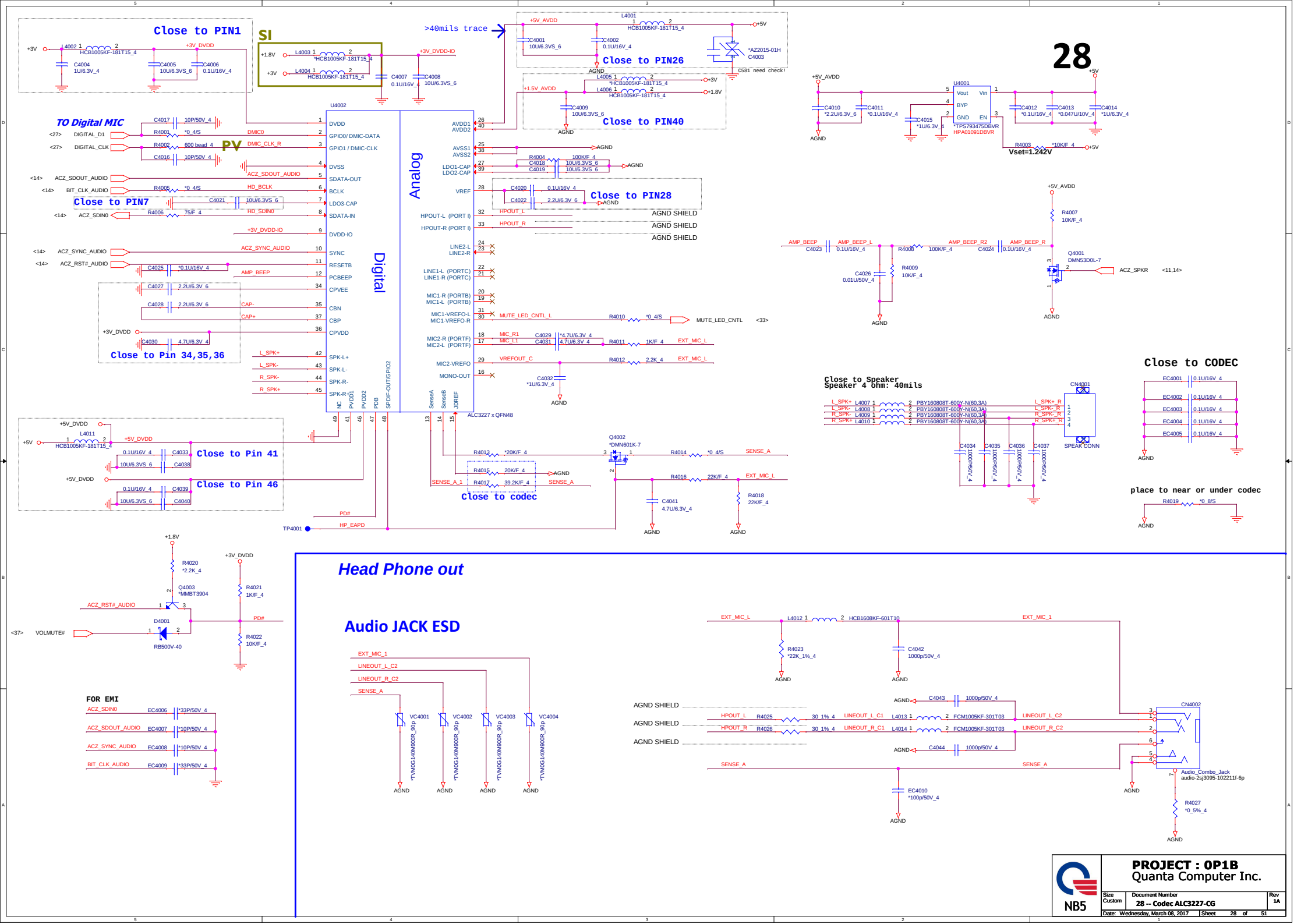




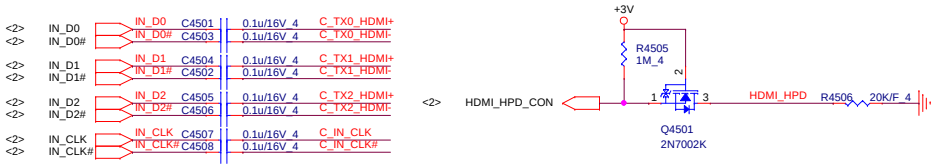


PROJECT :	0P1B
Quanta Computer Inc.	
Size: Custom	Document Number: 27 -- eDP CONN/LID/CAM/D-MIC/TS
Rev: 1A	
Date: Wednesday, March 08, 2017	Sheet 27 of 51

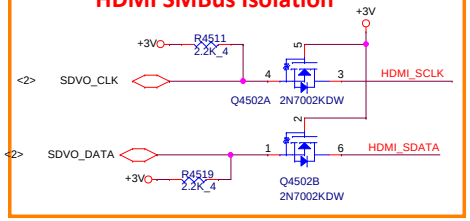
NB5


28
Close to PIN1
SI
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN28
Close to PIN7
Close to Pin 34,35,36
Close to Pin 41
Close to Pin 46
close to codec
TO Digital MIC
PV
Analog
Digital
ALC3227 x QFN48
Vset=1.242V
Close to CODEC
Close to Speaker
Speaker 4 ohm: 40mils
place to near or under codec
Head Phone out
Audio JACK ESD
FOR EMI
AGND SHIELD
PROJECT : 0P1B
Quanta Computer Inc.
NB5
Document Number
28 -- Codec ALC3227-CG
Date: Wednesday, March 08, 2017
Sheet 28 of 51

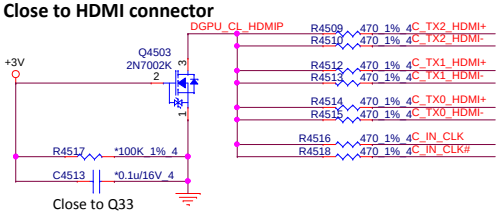
HDMI CONN



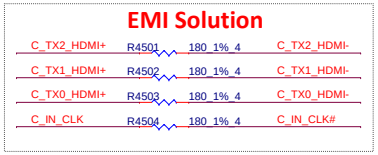
HDMI SMBus Isolation

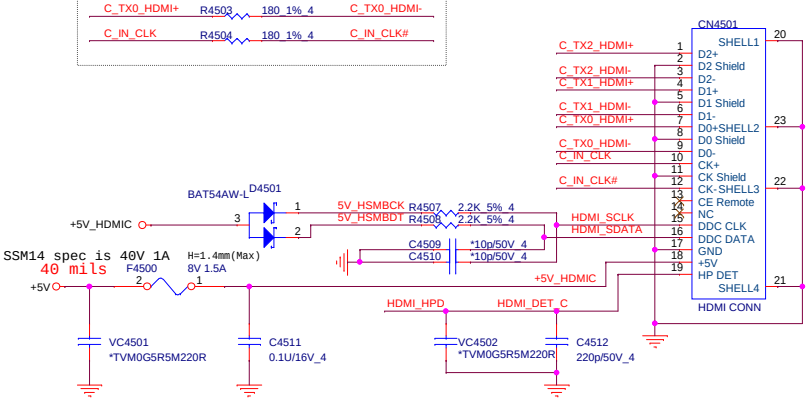


Close to HDMI connector



EMI Solution





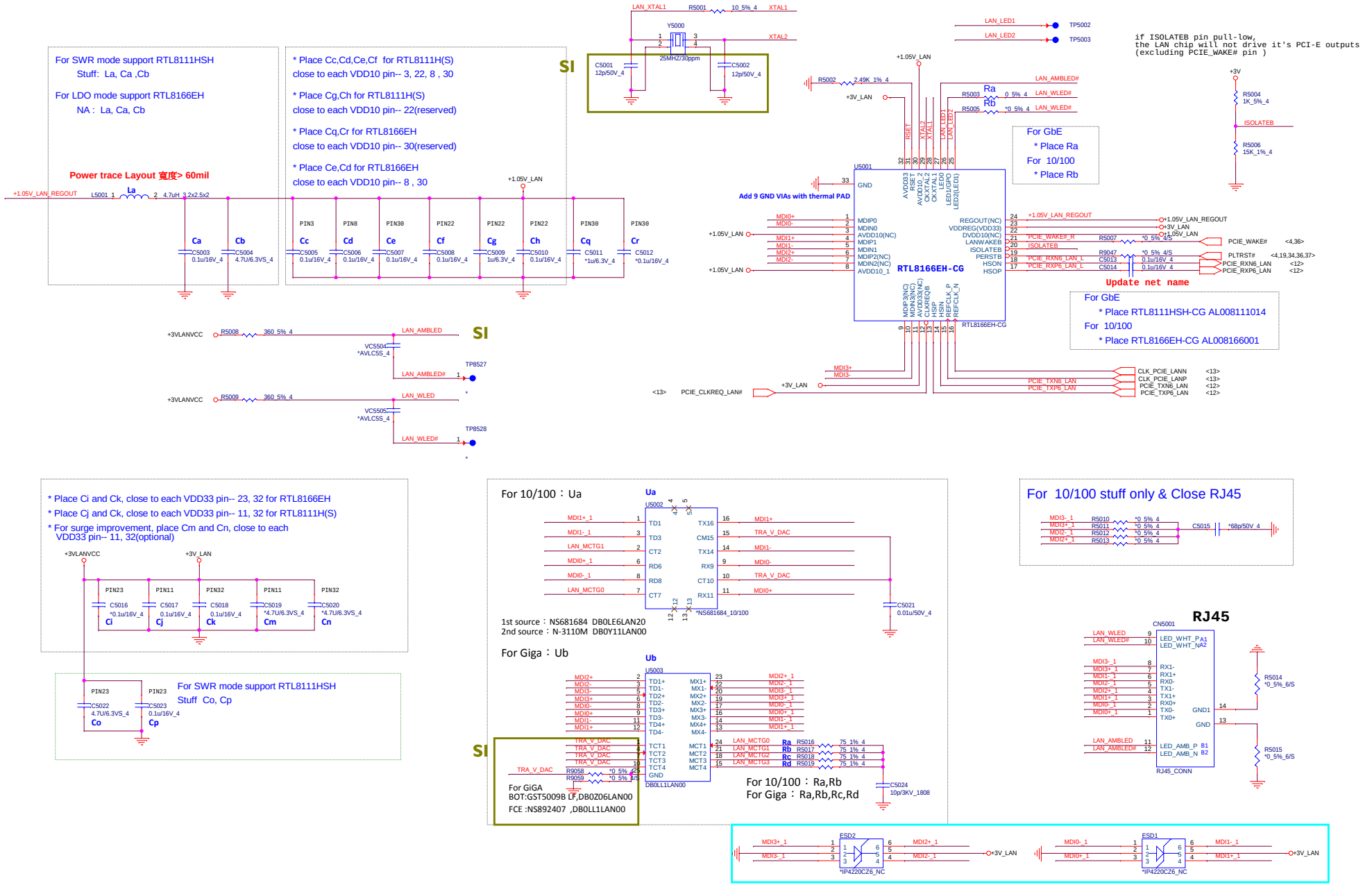
NB5

PROJECT : 0P1B
Quanta Computer Inc.

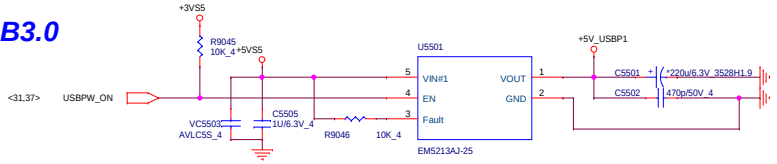
Size	Document Number	Rev
Custom	29 – HDMI/AMP HPA022642RTJR	1A

Date: Wednesday, March 08, 2017 | Sheet 29 of 51

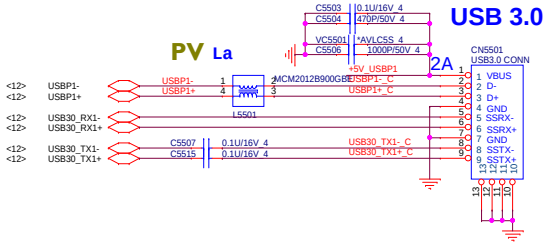
LAN RTL8166EH/RTL8111HSH

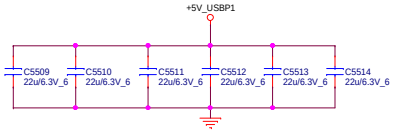


USB3.0



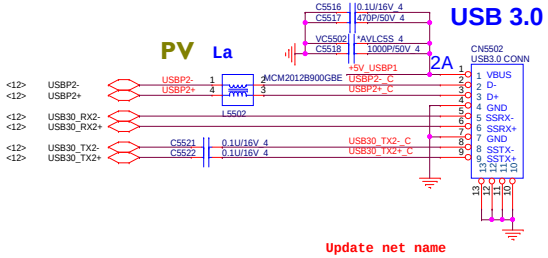
USB 2.0/3.0 Combo





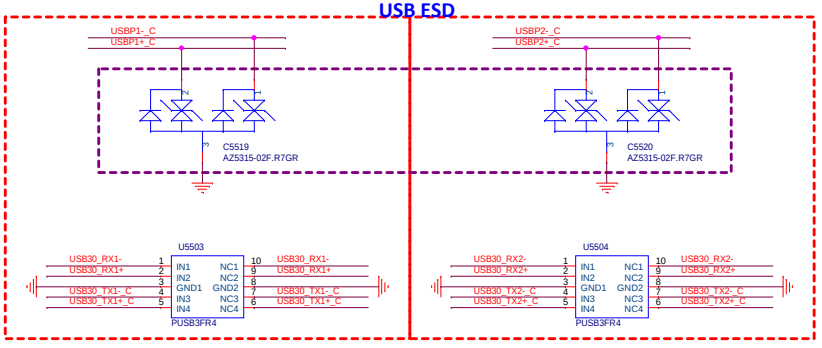
UART for Win7 WHQL DEBUG

USB 2.0/3.0 Combo



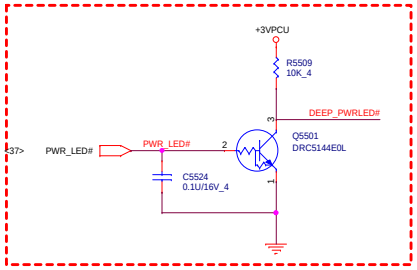
Update net name

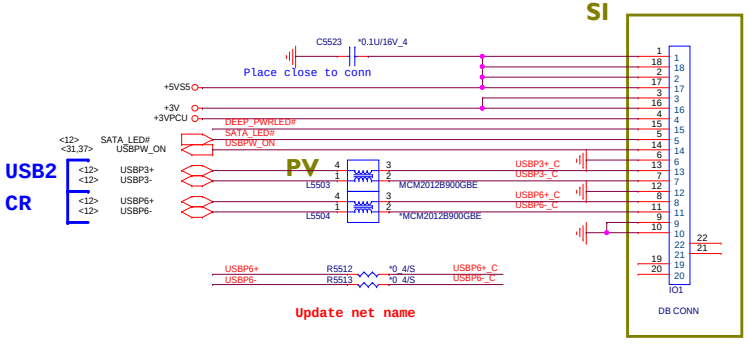
USB ESD



Update net name

Daughter Board

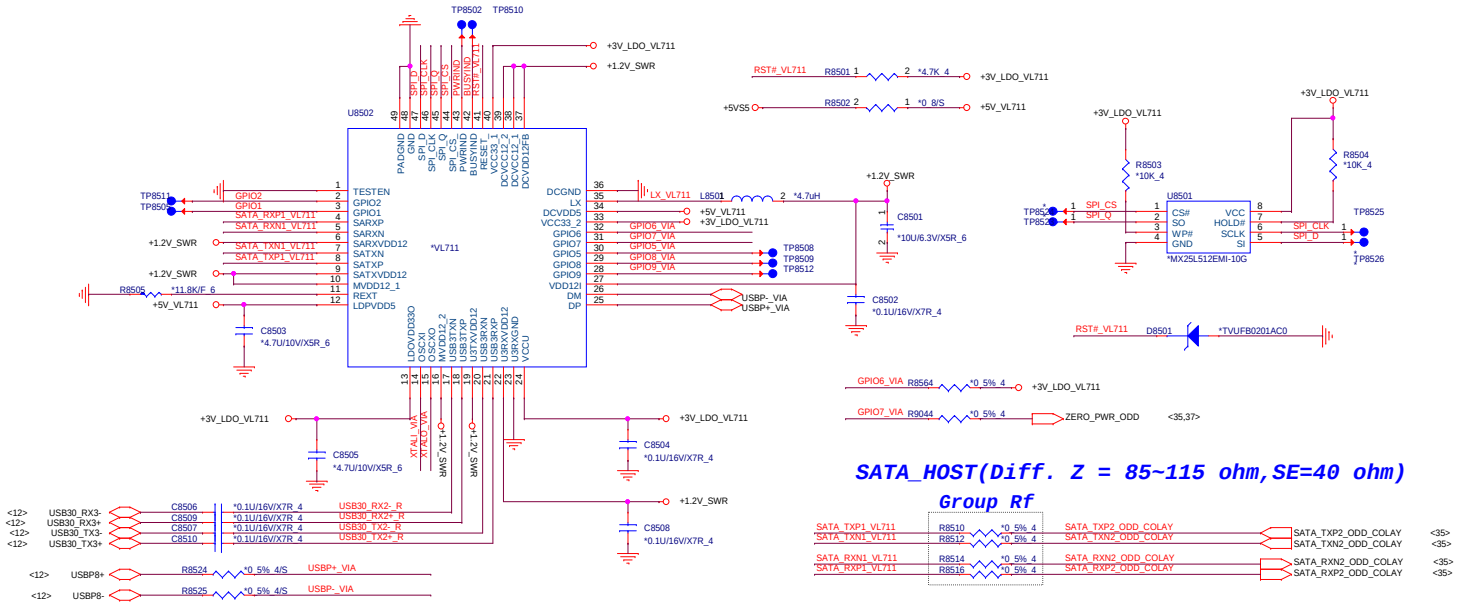




Update net name

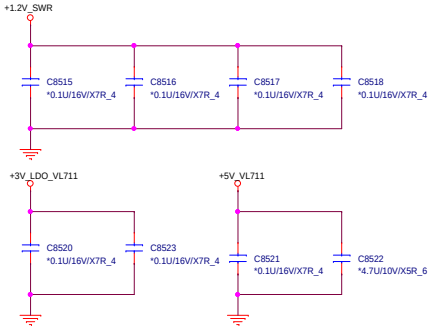
NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size C	Document Number 31 – USB SW & TYPE-C -TPS25810	Rev 1A
Date: Wednesday, March 08, 2017	Sheet 31 of 51	

USB3 to SATA VL711



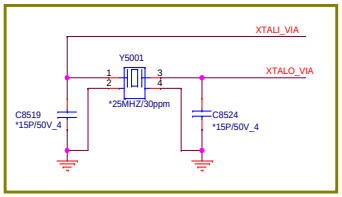
SATA_HOST(Diff. Z = 85~115 ohm,SE=40 ohm)

Group Rf



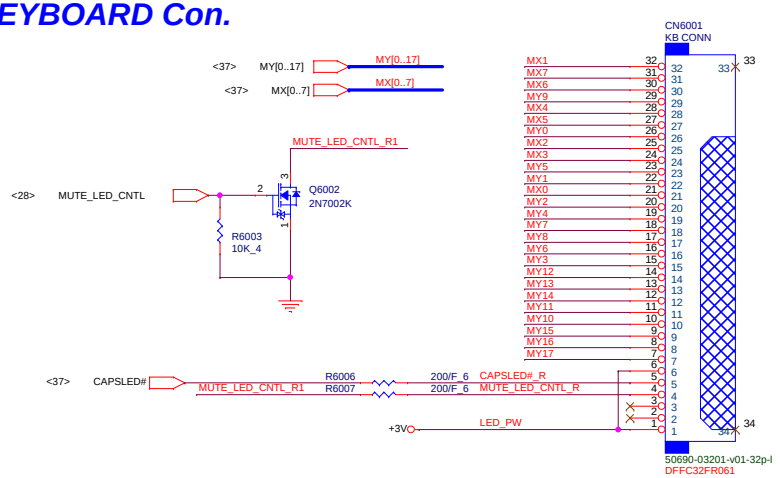
X'tal 25MHz

SI

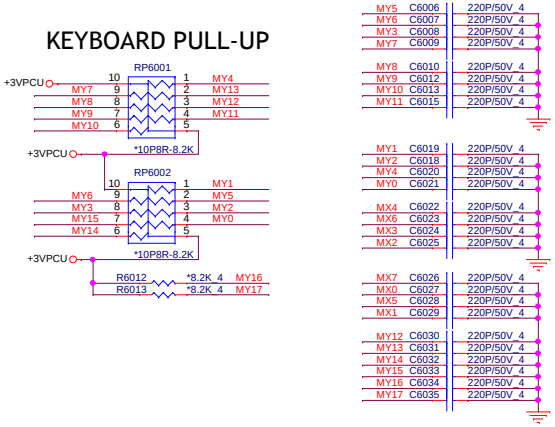


NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size C	Document Number 32 – USB SW & TYPE-C -TPS25810	Rev 1A
Date: Wednesday, March 08, 2017	Sheet 32 of 51	

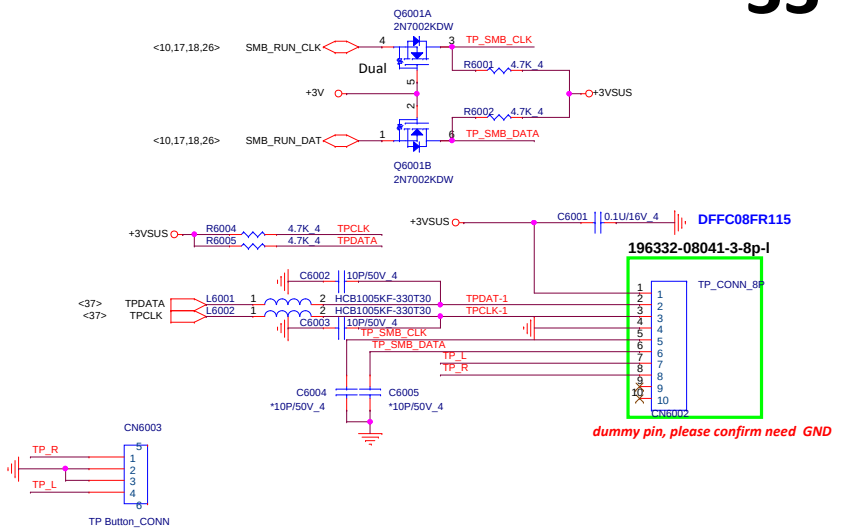
KEYBOARD Con.



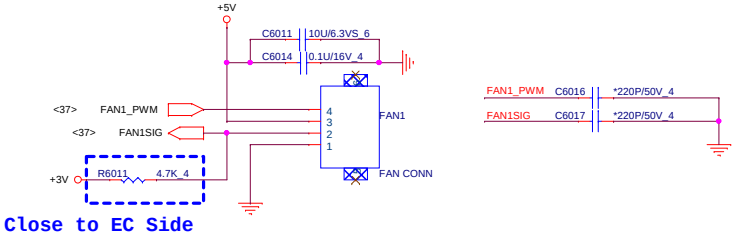
KEYBOARD PULL-UP



Touch Pad Connector



FAN

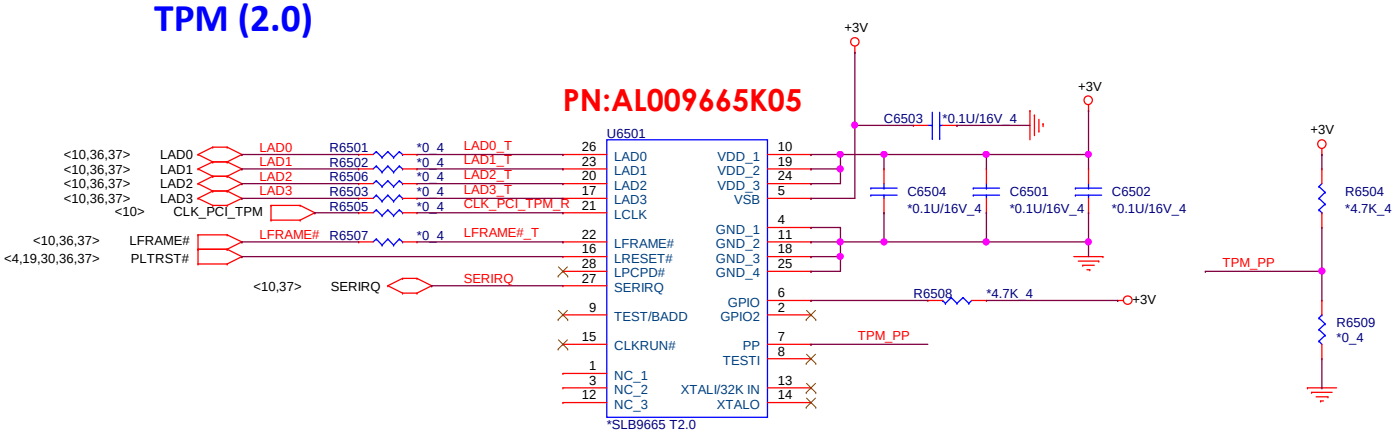


Power Button

NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size: Custom	Document Number: 33 -- KB/TP/FAN	Rev: 1A
Date: Wednesday, March 08, 2017	Sheet 33 of 51	

TPM (2.0)

PN:AL009665K05



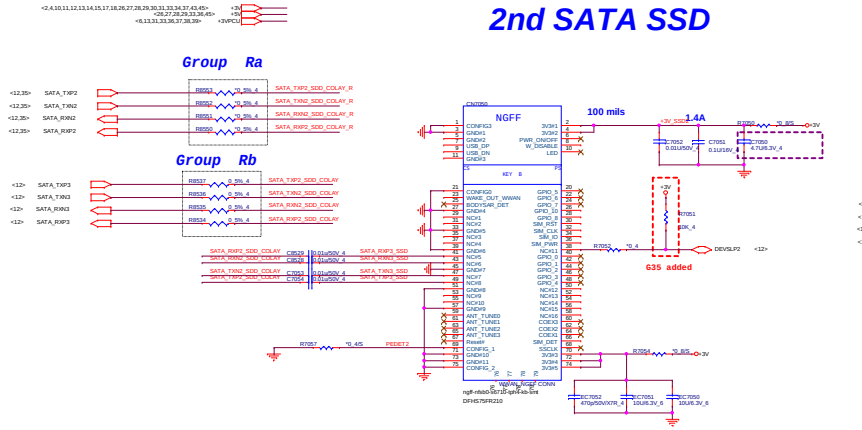
H1 *H-TC276IBC197D154P2
H25 *H-TC276IBC197D154P2
H24 h-tc237ic170d130pt
H30 *PAD-BALL276-NP
H26 *H-TC276IBC197D154P2
H27 *H-TC276IBC197D154P2
H7 *H-C237D130P2
H8 *H-IC276BC315D154PB
H28 *H-TC276IBC197D154P2
H29 *H-TC276IBC197D154P2
H4 *PAD-BALL276-NP
H32 *H-CT315B400SI178D158P2
H2 *H-C237D130P2
H3 *H-IC276BC315D154PB
H31 *H-IC276BC315D154PB
PAD1 *SPAD-RE315X59NP
PAD2 *SPAD-RE537X138NP

NB5

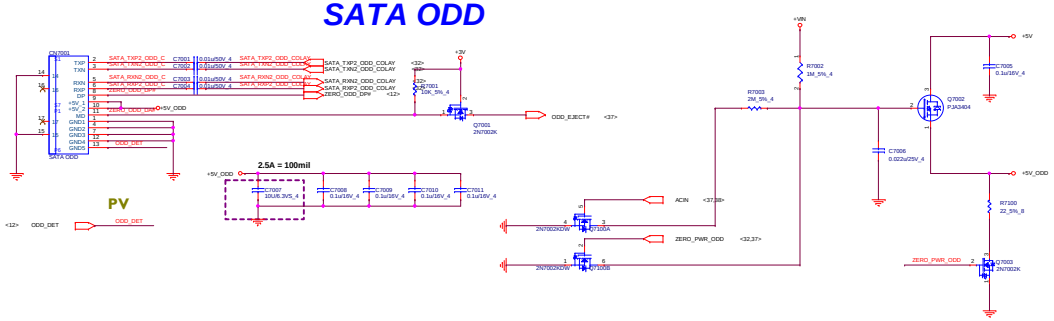
PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
B	34 -- TPM/G-Sensor/IR CAM	1A
Date: Wednesday, March 08, 2017	Sheet 34 of 51	

2nd SATA SSD



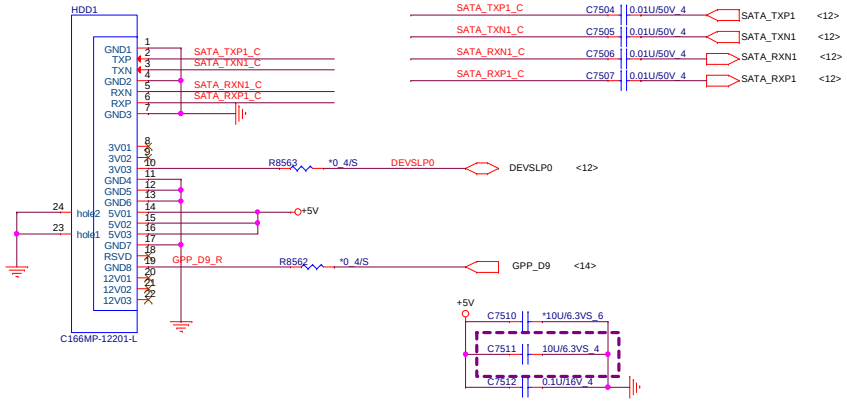
SATA ODD



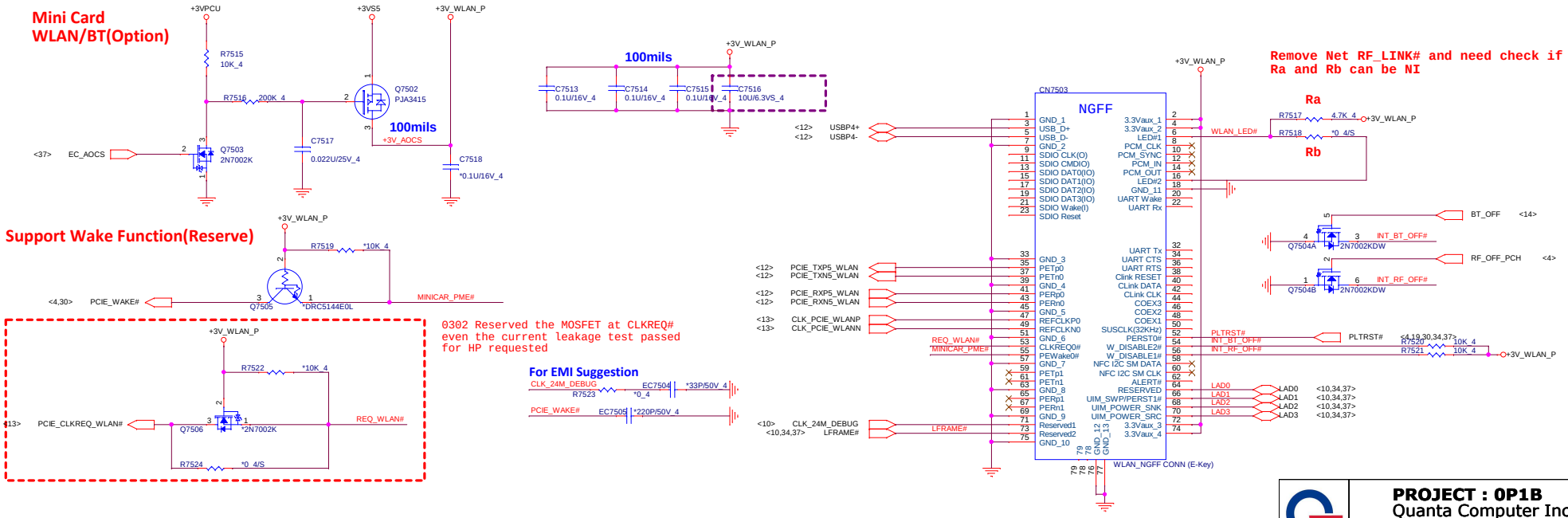
PROJECT : 0P1B	
Quanta Computer Inc.	
Size: Custom	Document Number: 35 – SSD_ODD_EMMC_ASM1153
Date: Wednesday, March 08, 2017	Sheet 35 of 35

HDD

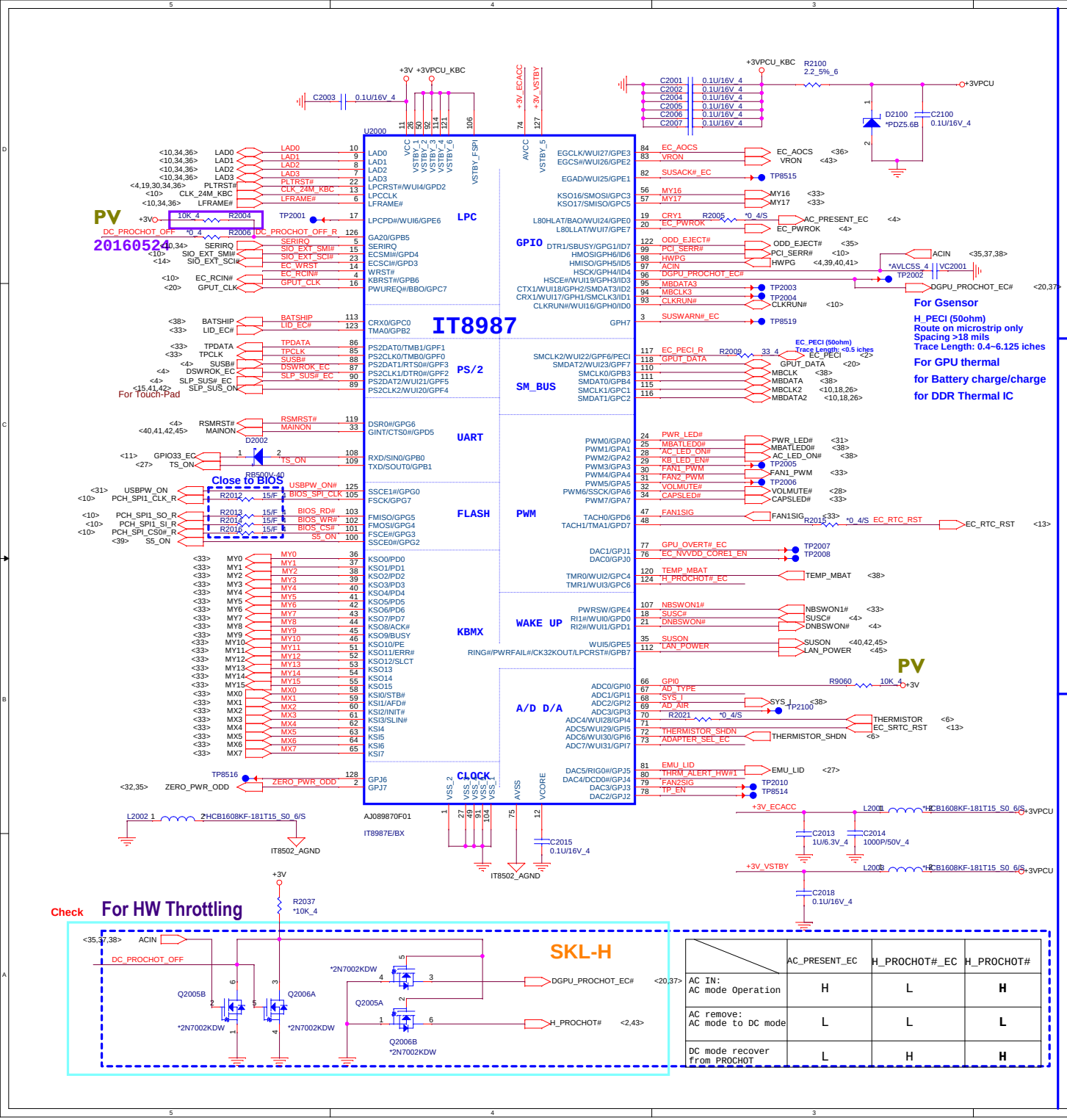
SATA HDD

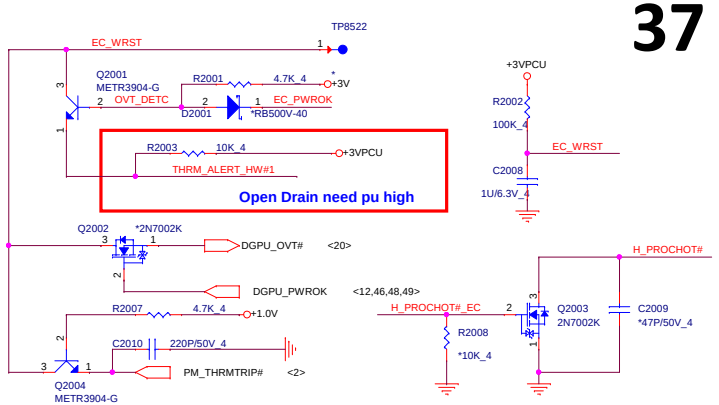


WLAN



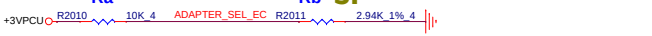
NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size: Custom	Document Number: 36 -- HDD/WLAN(NGFF)	Rev: 1A
Date: Wednesday, March 08, 2017	Sheet 36 of 51	





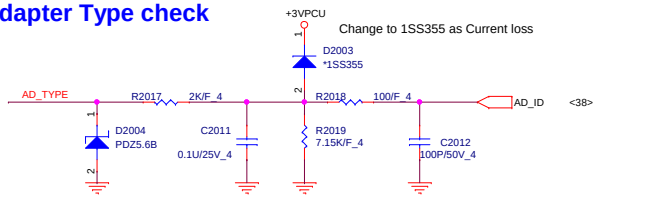
Adapter select for EC

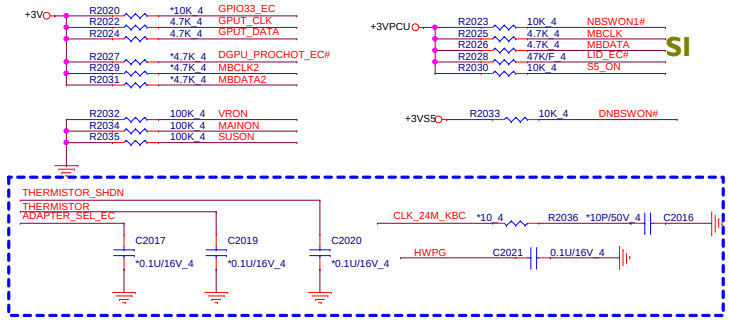
Ra Rb SI



	Ra	Rb	ADAPTER_SEL_EC	BOM
150W	10K(CS31002FB26)	100K(CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K	2.25V	
90W	10K(CS31002FB26)	8.33K	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

Adapter Type check



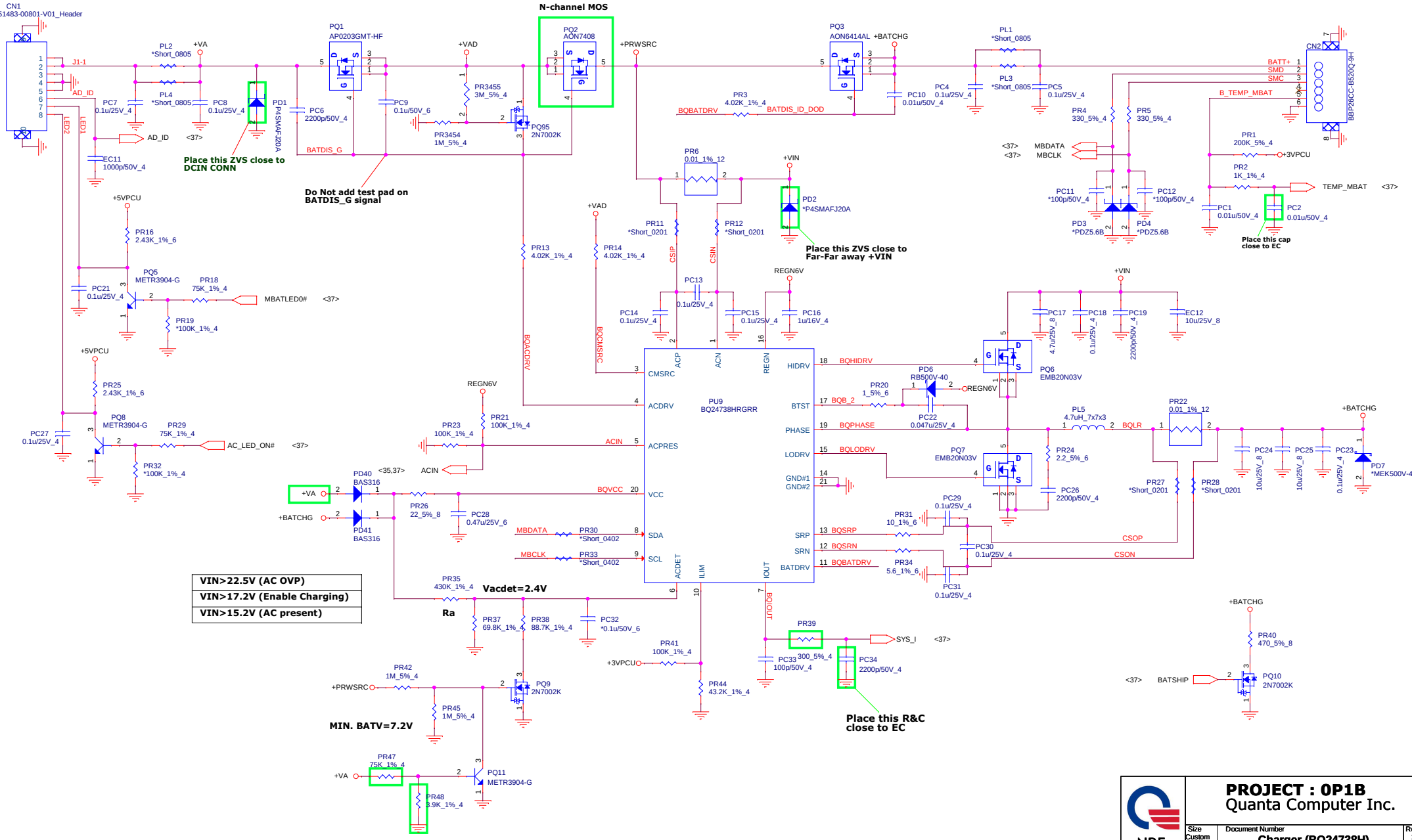


CLOSE to EC Pin

+3VPCU <6,13,31,33,36,37,38,39>
+5VPCU <39,45,49>
+BAT_RTC
+VIN <27,35,39,40,41,43,44,46,47,48,50>
+3VPCU <6,13,31,33,36,37,38,39>

ADP=65W

14"



NB5	PROJECT : 0P1B Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (BQ24738H)	Rev: 1A
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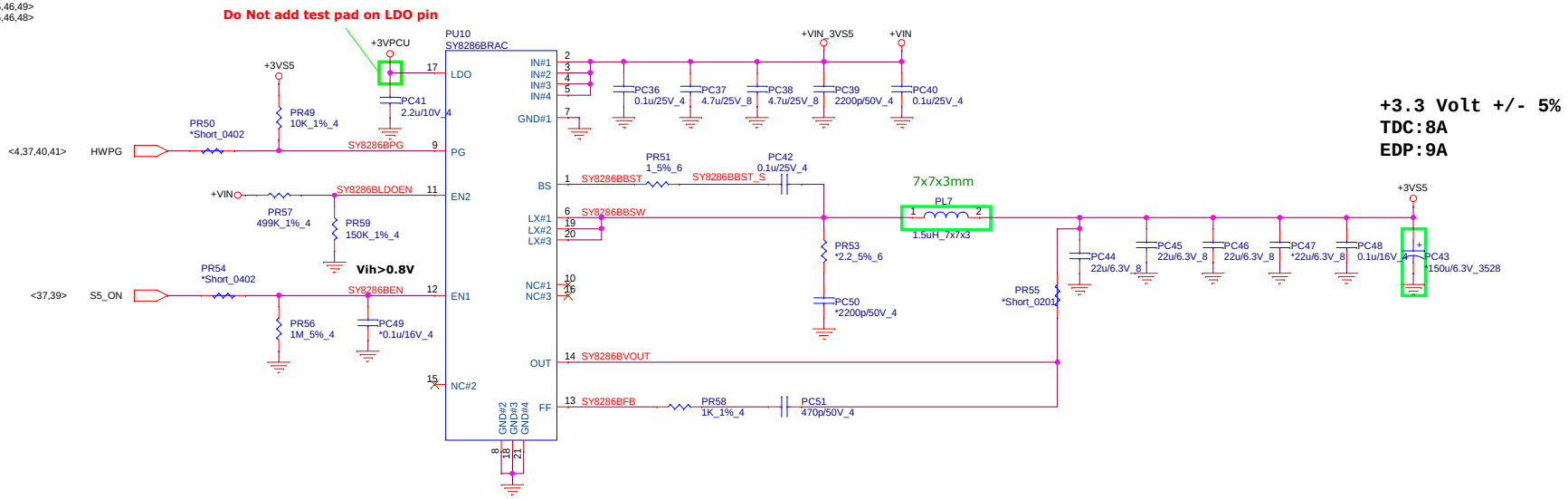
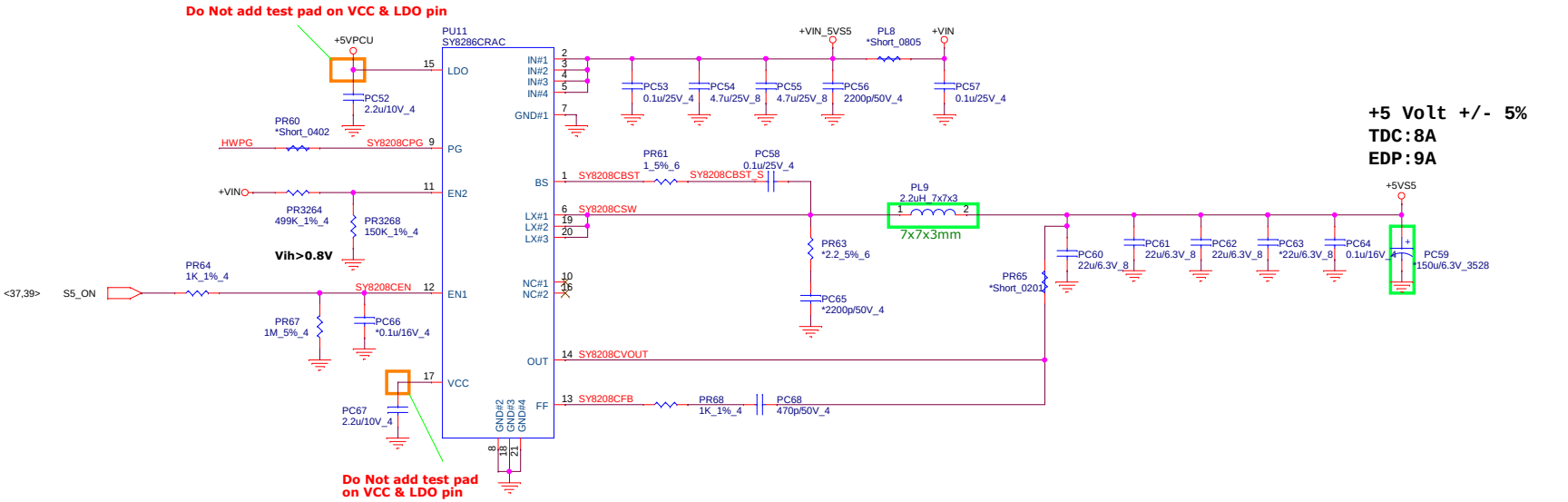
DC/DC +3VS5/+5VS5

+VIN <27,35,38,40,41,43,44,46,47,48,50>
+3VS5 <4,15,31,36,37,40,41,42,45,46,49>
+5VS5 <4,31,32,40,41,42,43,44,45,46,48>
+3VPCU <6,13,31,33,36,37,38>
+5VPCU <38,45,49>



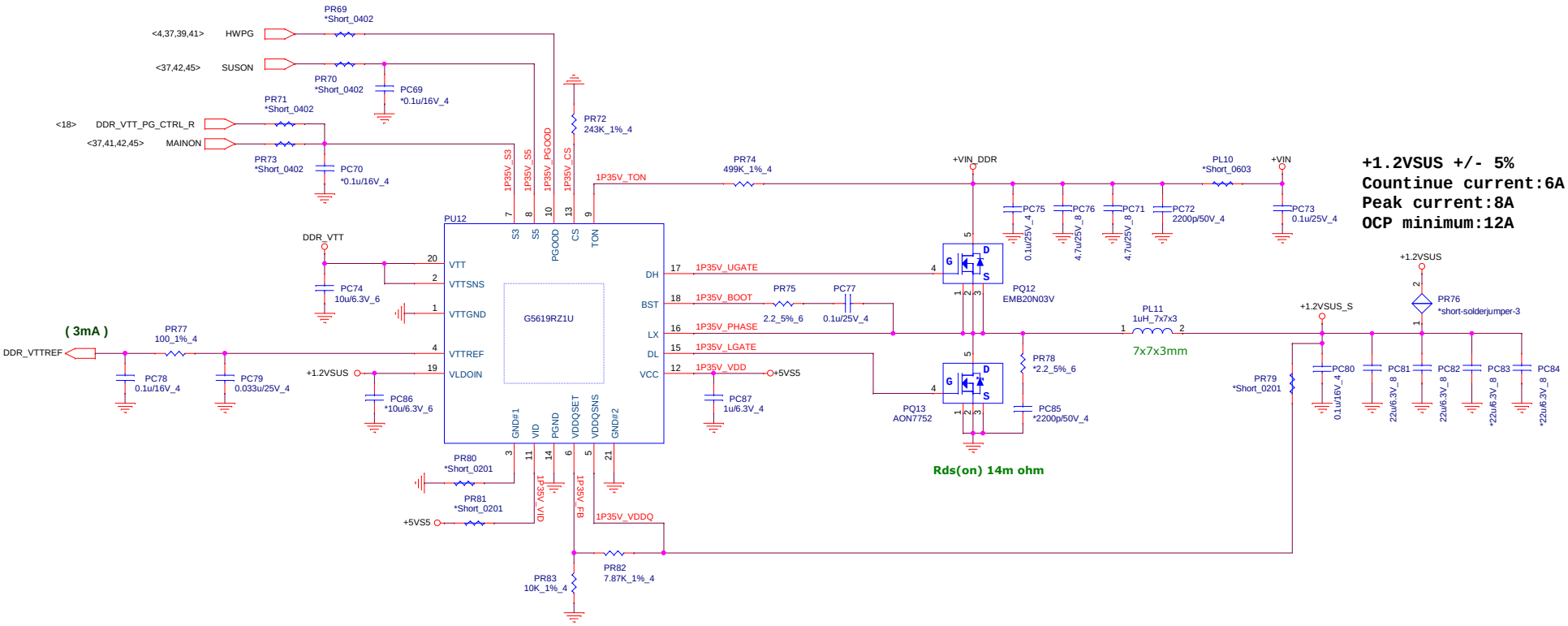


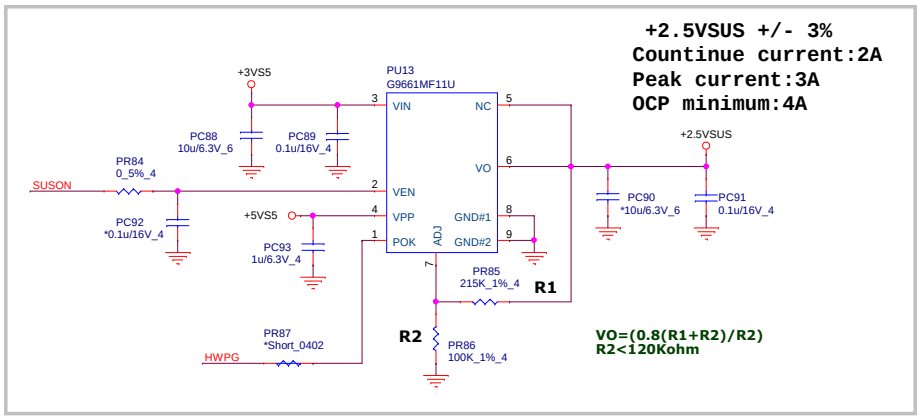
NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Wednesday, March 08, 2017	Sheet 39 of 51	

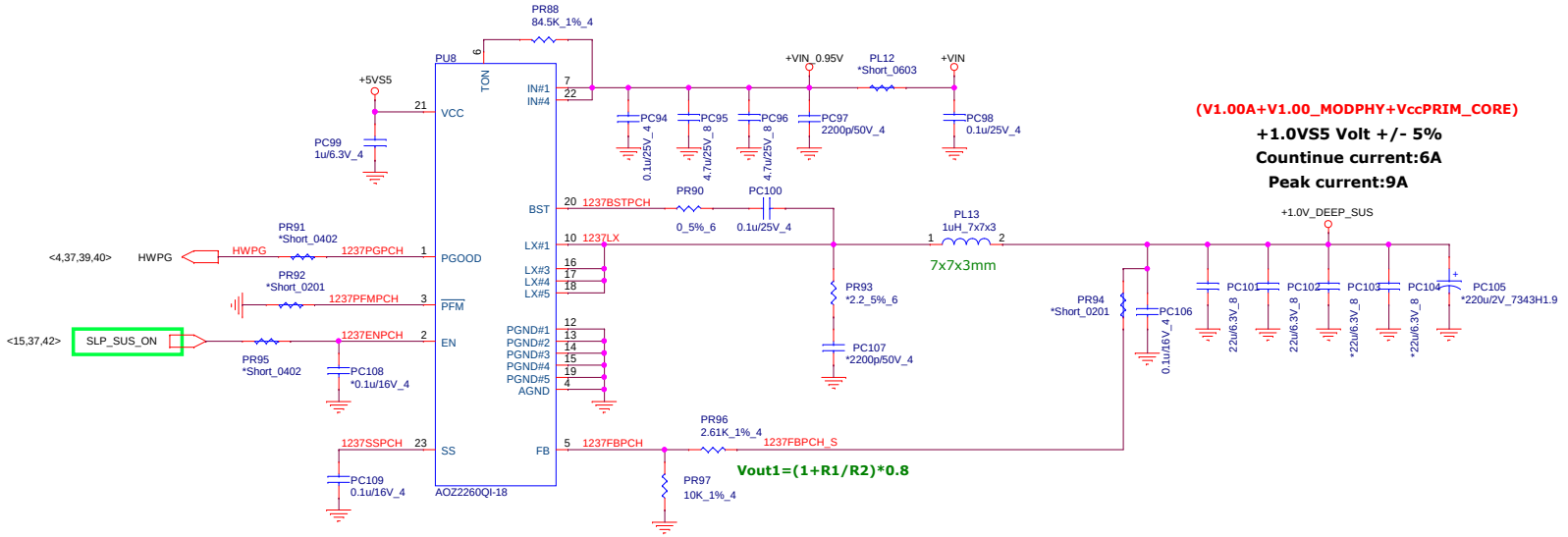
+VIN <27,35,38,39,41,43,44,46,47,48,50>
+5VS5 <4,31,32,39,41,42,43,44,45,46,48>
+1.2VSUS <3,6,17,18,42>
DDR_VTT <17,18>

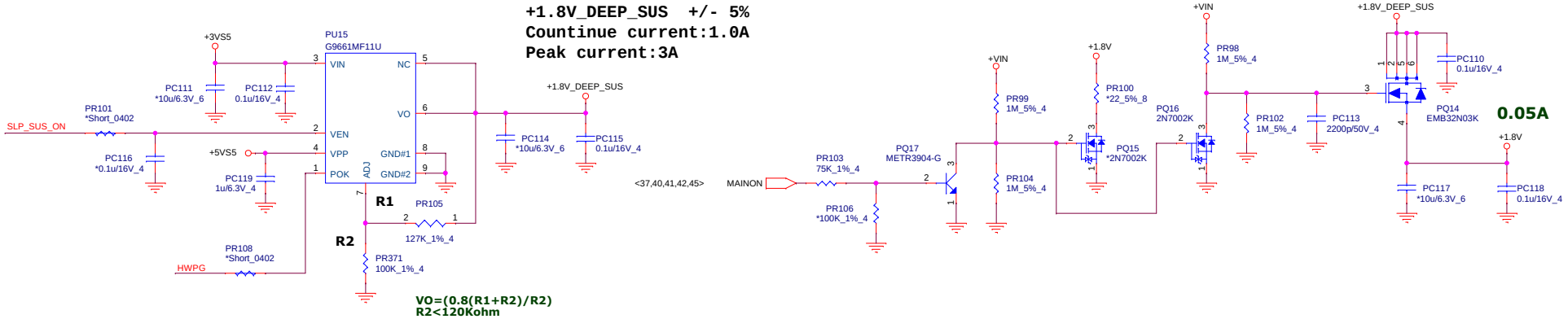




NB5	PROJECT : 0P1B Quanta Computer Inc.		
	Size	Document Number DDR4 (G5619RZ1U)	Rev 1A 1A
	Date: Wednesday, March 08, 2017	Sheet 40 of 51	

+VIN <27,35,38,39,40,43,44,46,47,48,50>
+3VS5 <4,15,31,36,37,39,40,42,45,46,49>
+5VS5 <4,31,32,39,40,42,43,44,45,46,48>
+1.0V_DEEP_SUS <9,13,15,42>
+1.8V_DEEP_SUS <9,15,49>
MAINON <37,40,41,42,45>
+1.5V





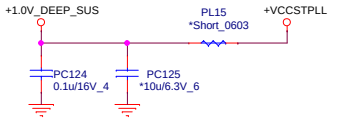
NB5	PROJECT : 0P1B Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V/+1.8V_DEEP_SUS	Rev: 1A
Date: Wednesday, March 08, 2017	Sheet 41 of 51	

+1.0V <2,4,37,43>
+3VS5 <4,15,31,36,37,39,40,41,45,46,49>
+5VS5 <4,31,32,39,40,41,43,44,45,46,48>
+VCCIO <2,6>
+1.2VSUS <3,6,17,18,40>
+VCCSTPLL <2,4,5,6,9>
+1.0V_DEEP_SUS <9,13,15,41>
+1.2V_VCCPLL_OC <6>
MAINON <37,40,41,45>

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

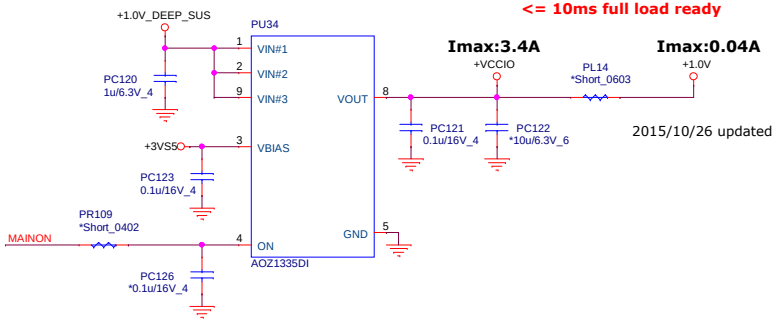
Imax:0.24A



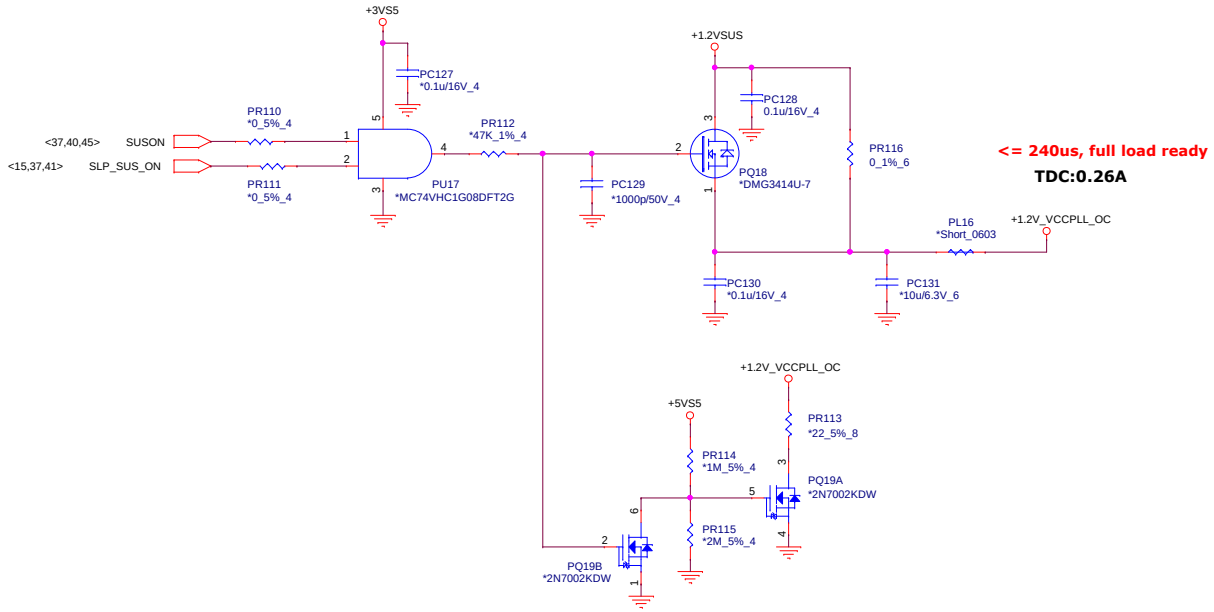
Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**



2015/10/26 updated



<= 240us, full load ready
TDC:0.26A

NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
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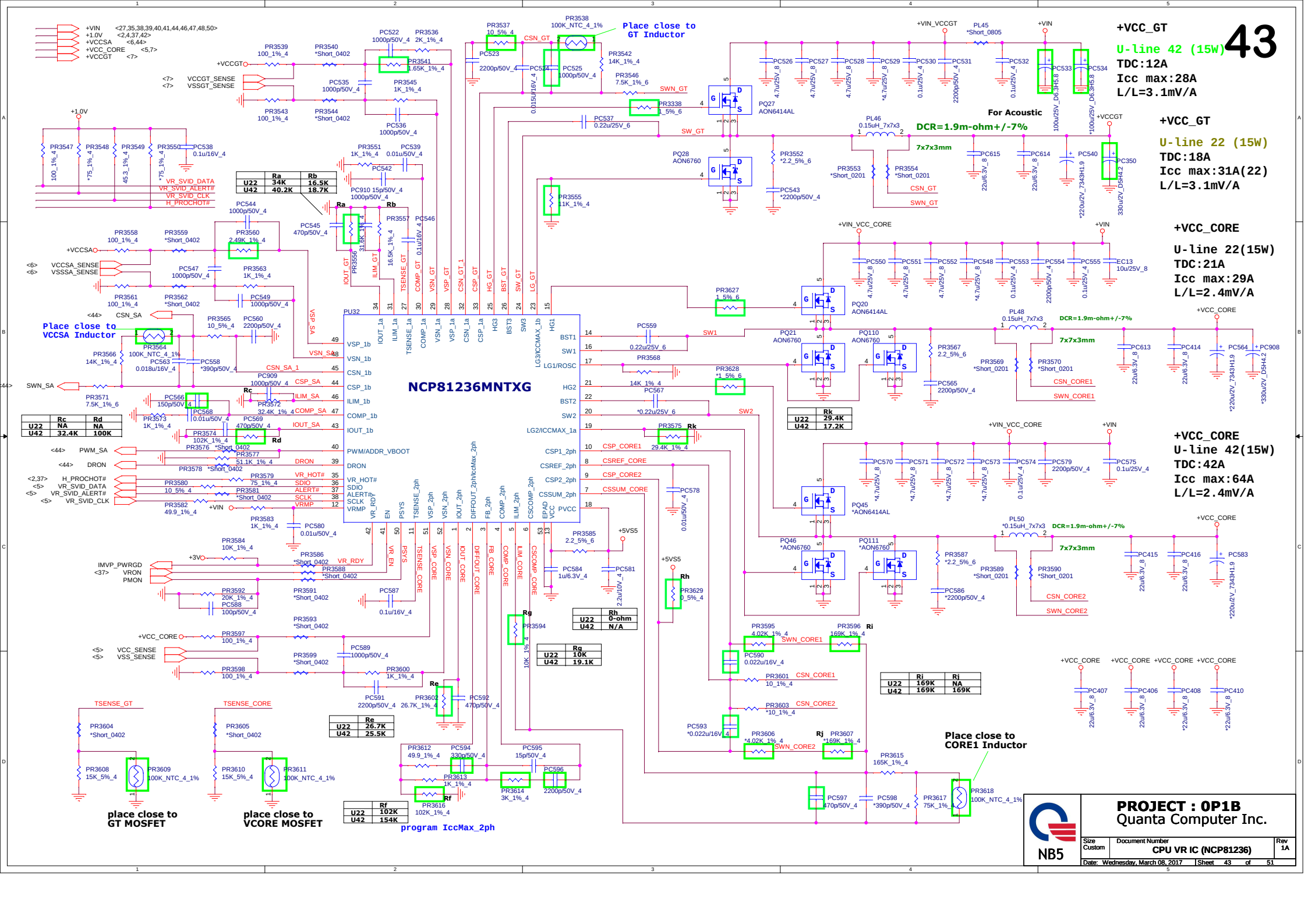
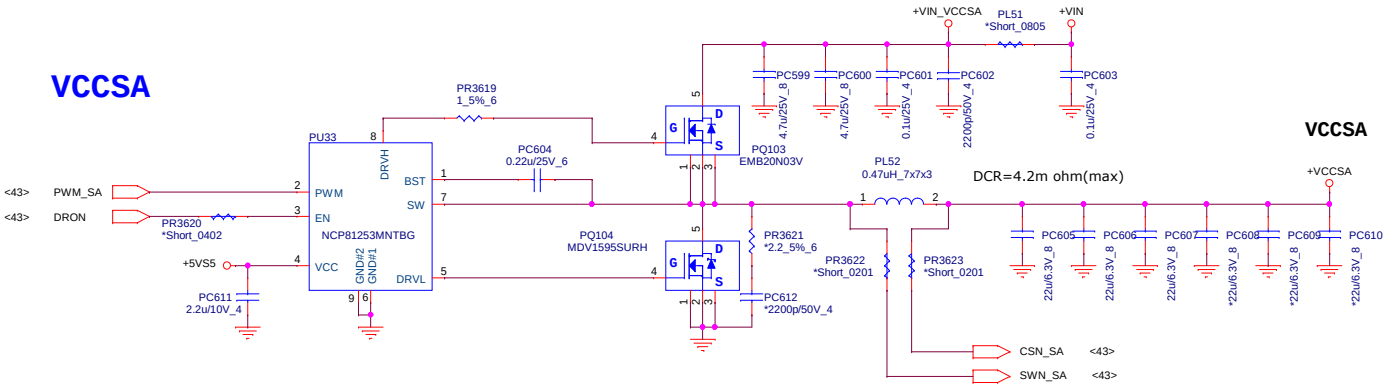

+VCC_GT
U-line 42 (15W)
TDC:12A
Icc max:28A
L/L=3.1mV/A
43
+VCC_GT
U-line 22 (15W)
TDC:18A
Icc max:31A(22)
L/L=3.1mV/A
+VCC_CORE
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A
+VCC_CORE
U-line 42(15W)
TDC:42A
Icc max:64A
L/L=2.4mV/A
NCP81236MNTXG
Place close to GT Inductor
Place close to VCCSA Inductor
Place close to CORE1 Inductor
For Acoustic
DCR=1.9m-ohm+/-7%
7x7x3mm
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
PROJECT : 0P1B
Quanta Computer Inc.
NB5
CPU VR IC (NCP81236)
Wednesday, March 08, 2017



NB5	**PROJECT : 0P1B** Quanta Computer Inc.	
Size: Custom	Document Number: +VCCSA (NCP81253)	Rev: 1A
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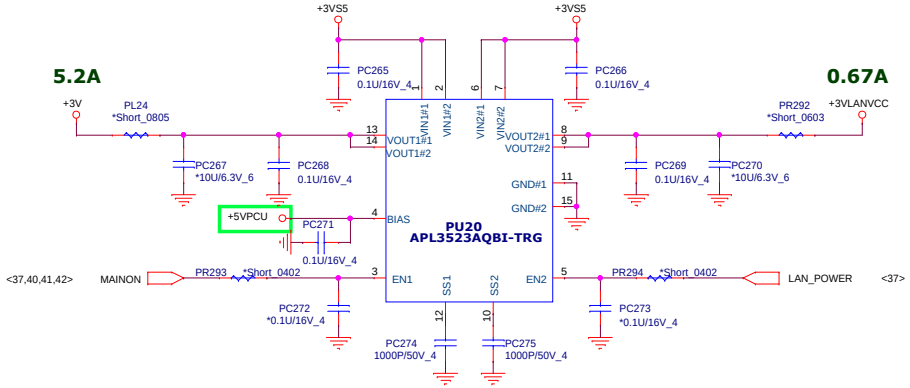
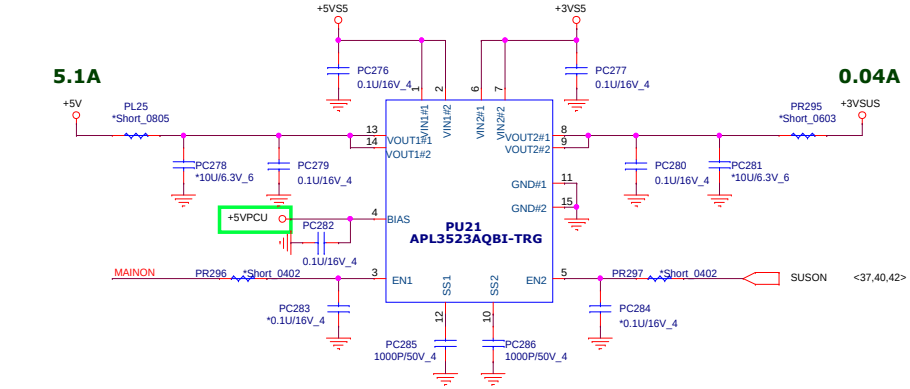
+3V <2,4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43>
+5V <26,27,28,29,33,35,36>
+VIN <27,35,38,39,40,41,43,44,46,47,48,50>
+3VS5 <4,15,31,36,37,39,40,41,42,46,49>
+5VS5 <4,31,32,39,40,41,42,43,44,46,48>
+3VSUS <33>
+5VPCU <38,39,49>
+3VLANVCC <30>





NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
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R17M-M1-70

+1.8V_VGA

PR3457 *10K_1%_4
PR3458 *10K_1%_4
PC449 *0.1u/16V_4
3662SVC
3662SVD
PR1210 *10K_1%_4
PR1208 *10K_1%_4

VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

8899VCC
PR3456 4.7_5%_4
+5VS5
PC448 2.2u/10V_4
8899PVCC
PR3459 *Short_0402
+5VS5
PC450 2.2u/10V_4
+VIN_GPU
PC451 0.1u/25V_4
PR1209 4.7_5%_4
PR3465 1_5%_6

PU16
RT3662EBGQW

NC 22
VCC 14
PVCC 27
VIN 1
UGATE1 24 3662UGATE1 3662UGATE1_G <47>
BOOT1 23 3662BOOT1 PC452 0.1u/25V_4
PHASE1 25 3662LX1 3662LX1 <47>
LGATE1 26 3662LGATE1 3662LGATE1 <47>
ISEN1P 7 3662ISEN1P_1
ISEN1N 8 3662ISEN1N_1 PR3478 *Short_0402
UGATE2 30 3662UGATE2 PR3481 1_5%_6 3662UGATE2_G <47>
BOOT2 31 3662BOOT2 PC457 0.1u/25V_4
PHASE2 29 3662LX2 3662LX2 <47>
LGATE2 28 3662LGATE2 3662LGATE2 <47>
ISEN2P 5 3662ISEN2P_1
ISEN2N 6 3662ISEN2N_1
COMP 3 3662COMPA
FB 4 3662FBA
VSEN 21 PR3500 *Short_0402
RGND 2
GND 33

SET1 11 3662SET1 VREF_PINSET PR1201 10K_1%_4 PR1204 48.7K_1%_4 PR1205 10K_1%_4 PR1206 2.94K_1%_4
TSEN 10 3662TSEN VREF_PINSET PR3470 60.4K_1%_4 PR3471 6.04K_1%_4 PR3472 60.4K_1%_4 PR3473 10K_1%_4 PR3474 23.7K_1%_4 PR3464 100K_NTC_4_1%
EN 32 3662EN <12,13,49> DGPU_PR_EN <48> 3662EN PD16 RB500V-40 PR3476 10K_1%_4 PC454 0.47u/6.3V_4
Put close to VGACORE HOT SPOT
Vih=2V
VDDIO 19 3662VDDIO +3V_VGA PR3479 2.2_5%_6 +1.8V_VGA PR3480 *2.2_5%_6 PC456 1u/6.3V_4
R17M-M1-30
R17M-M1-70
PWROK 15 3662PWROK DGPU_PWROK PR3483 *Short_0201
SVC 16 3662SVC <20> SVI2_CLK PR3485 *Short_0201
SVD 17 3662SVD <20> SVI2_DATA PR3486 *Short_0201
SVT 18 3662SVT <20> SVI2_SVT PR3488 *Short_0201
PGOOD 20 3662PGOOD <12,37,48,49> DGPU_PWROK +3VS5 PR3491 10K_1%_4 PR1207 *Short_0201
VRHOT_L 9 3662VRHOT +3VS5 PR3493 *10K_1%_4 <20> DGPU_OCP_L PR3494 *Short_0402
IMON 12 PR3499 100K_NTC_4_1% PR3497 6.98K_1%_4 PC462 *100p/50V_4 VREF_PINSET
VREF_PINSET 13 PR3502 14K_1%_4 PR3503 11K_1%_4 PR3504 3.9_1%_4 PC464 0.47u/6.3V_4

Put close to VGACORE hot sport PHASE 1
R1
R2
R3

	1 Phase setting	
R1		
R2		
R3		

PR3475 3.3K_1%_4
PC453 0.47u/6.3V_4
PR3477 357_1%_4
PC455 0.1u/16V_4
3662ISEN1P <47>
3662ISEN1N <47>

PR3484 3.3K_1%_4
PC458 0.47u/6.3V_4
PR3487 357_1%_4
PC459 0.1u/16V_4
PR3489 0_5%_4
3662ISEN2P <47>
3662ISEN2N <47>
Unstuff
1 Phase setting
PR3490 *10K_1%_2 +5VS5 stuff 1 Phase setting

PC460 39p/50V_4
PC461 270p/50V_4
PR3495 56.2K_1%_4
PR3492 10K_1%_4
R4
+VGA_CORE
PR3498 10_1%_4
VGPU_CORE_SENSE_SRC
PC463 *82p/50V_4
VSS_GPU_SENSE_SRC
VGPU_CORE_SENSE <22>
VSS_GPU_SENSE <22>
PR3506 10_1%_4

	1 Phase setting	
R4		

NB5

PROJECT : 0P1B
Quanta Computer Inc.

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Custom	EC ENE KB9027B	1A

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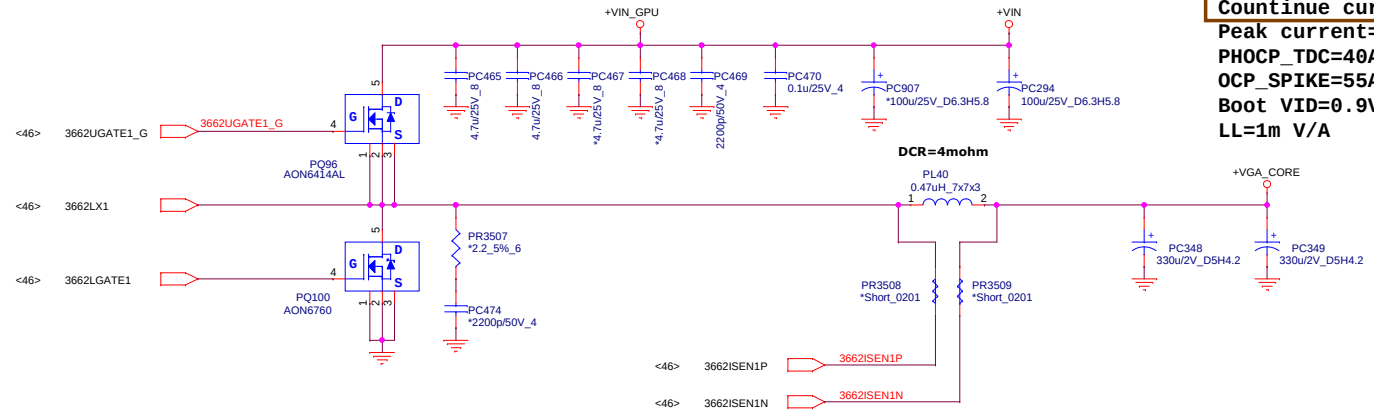
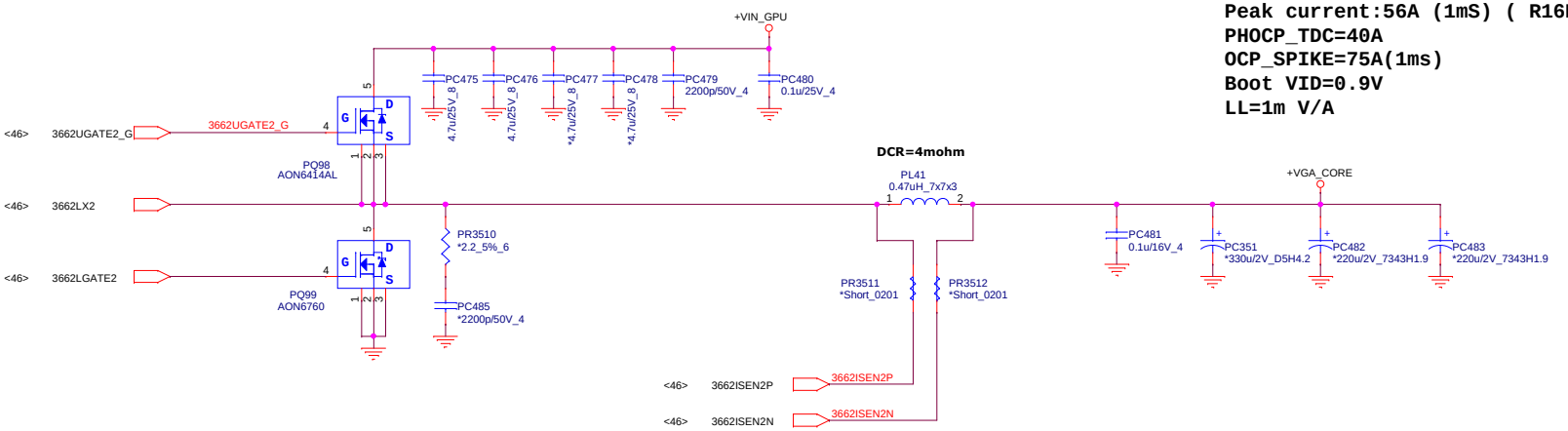
VGACORE (R17M-M1-30_ 25W/38W(1ms))
Countinue current:28A
Peak current=38A (1ms)
PHOCP_TDC=40A (soft-start only)
OCP_SPIKE=55A(1ms)
Boot VID=0.9V
LL=1m V/A



VGACORE (R16M-M2-50_ 37W/56W(1ms))
Countinue current:40A (R16M-M2-50)
Peak current:56A (1mS) (R16M-M2-50)
PHOCP_TDC=40A
OCP_SPIKE=75A(1ms)
Boot VID=0.9V
LL=1m V/A



NB5

PROJECT : 0P1B
Quanta Computer Inc.

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Custom	EC ENE KB9027B	1A

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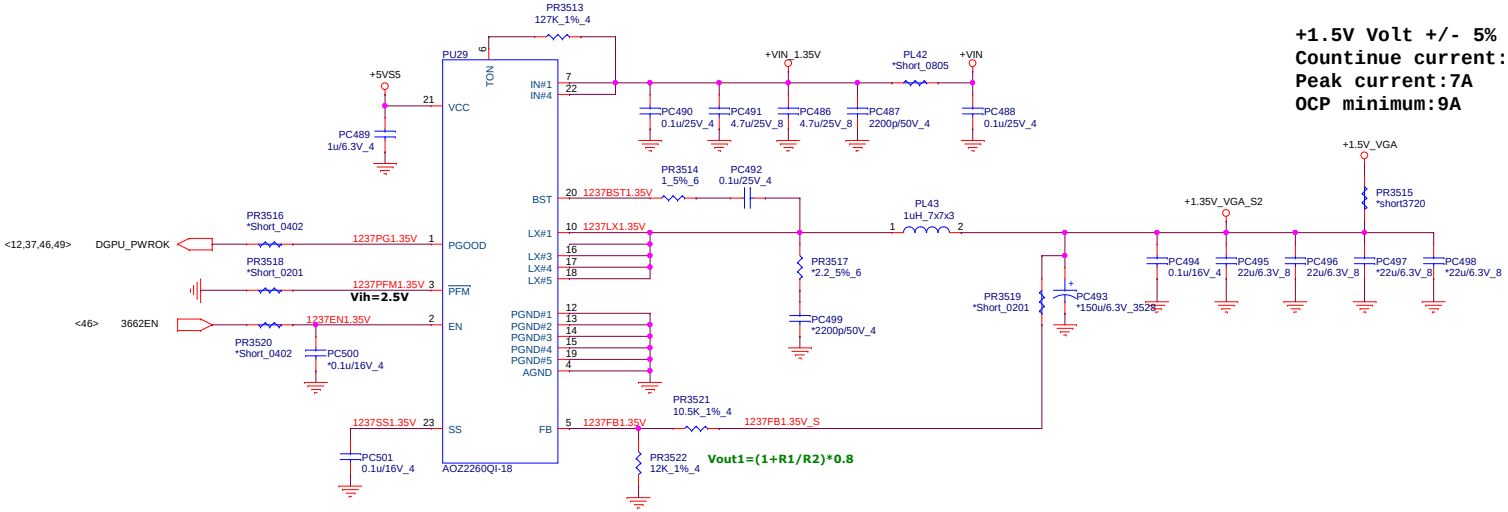

+1.5V Volt +/- 5%
Countinue current:6A
Peak current:7A
OCP minimum:9A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

NB5

PROJECT : 0P1B
Quanta Computer Inc.

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Custom	EC ENE KB9027B	1A

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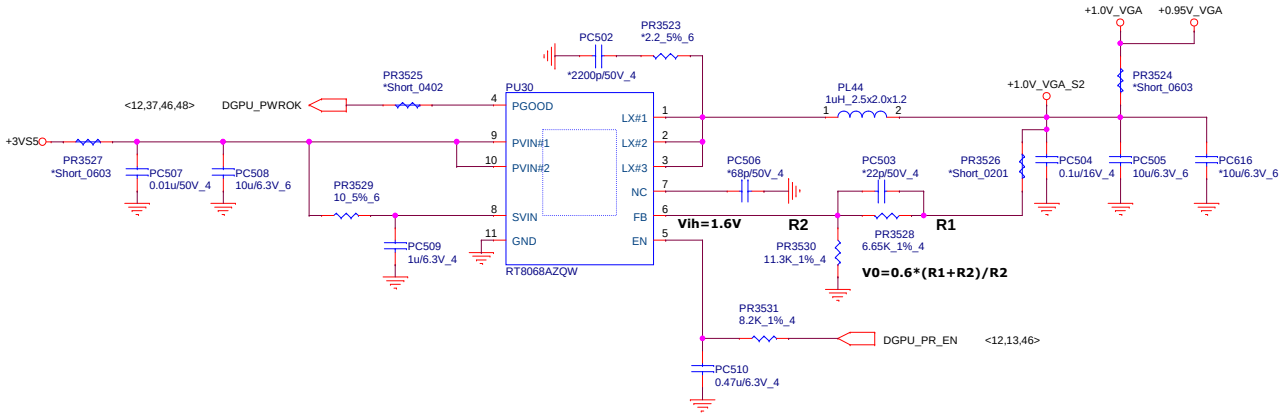
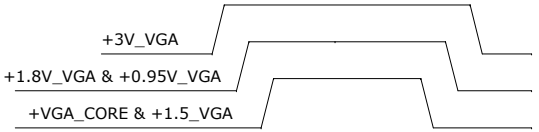
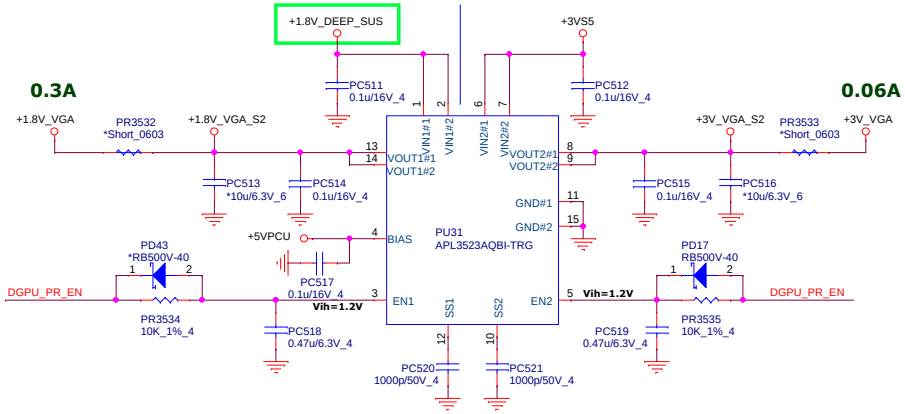
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A





PUT COLSE TO +1.8V power.



PROJECT : 0P1B
Quanta Computer Inc.

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Size	Document Number	Rev
Custom	EC ENE KB9027B	1A

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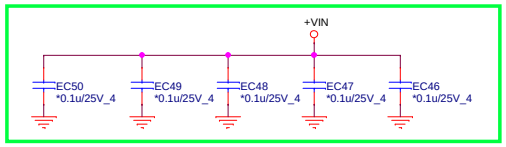
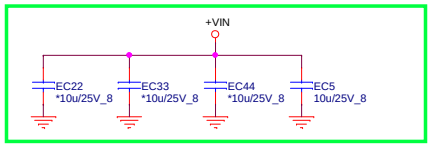
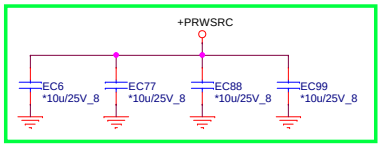


EMI request for ISN



EMI request for ISN



NB5

PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI solution	1A
		1A

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