
msi
MOTHERBOARD
Z97S SLI
Krait Edition
Z97S SLI
Krait Edition
msi
msi
Z97S SLI Krait Edition
msi

MS-7922

ATX

Ver:2.0

Intel -Shark Bay plamform Z97

CPU:

Marswell LGA1150

System Chipset:

Lynx Point Z97

Onboard Chip:

HD Audio Codec:ALC892

LAN-Intel 218 - Reatek 8111G

SIO:Fintek NTC6792D

Flash ROM: SPI 64 MB/128MB

Main Memory:

*DDRIII (800/1066/1333MHz) * 4 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12.5 -UP1649-8-2=6phase

Expansion Slots:

*PCI Express (X16) Slot *3-2=1*

*PCI Express (X1) Slot * 3*

*PCI Express (X8) Slot * 1*

*PCI Express (X1) Slot * 1*

*PCI Slot * 2*

Other:

SATA Express

SATA3.0 x6 (PCH)

*REAR USB2.0 *2*

*FRONT USB2.0 *4*

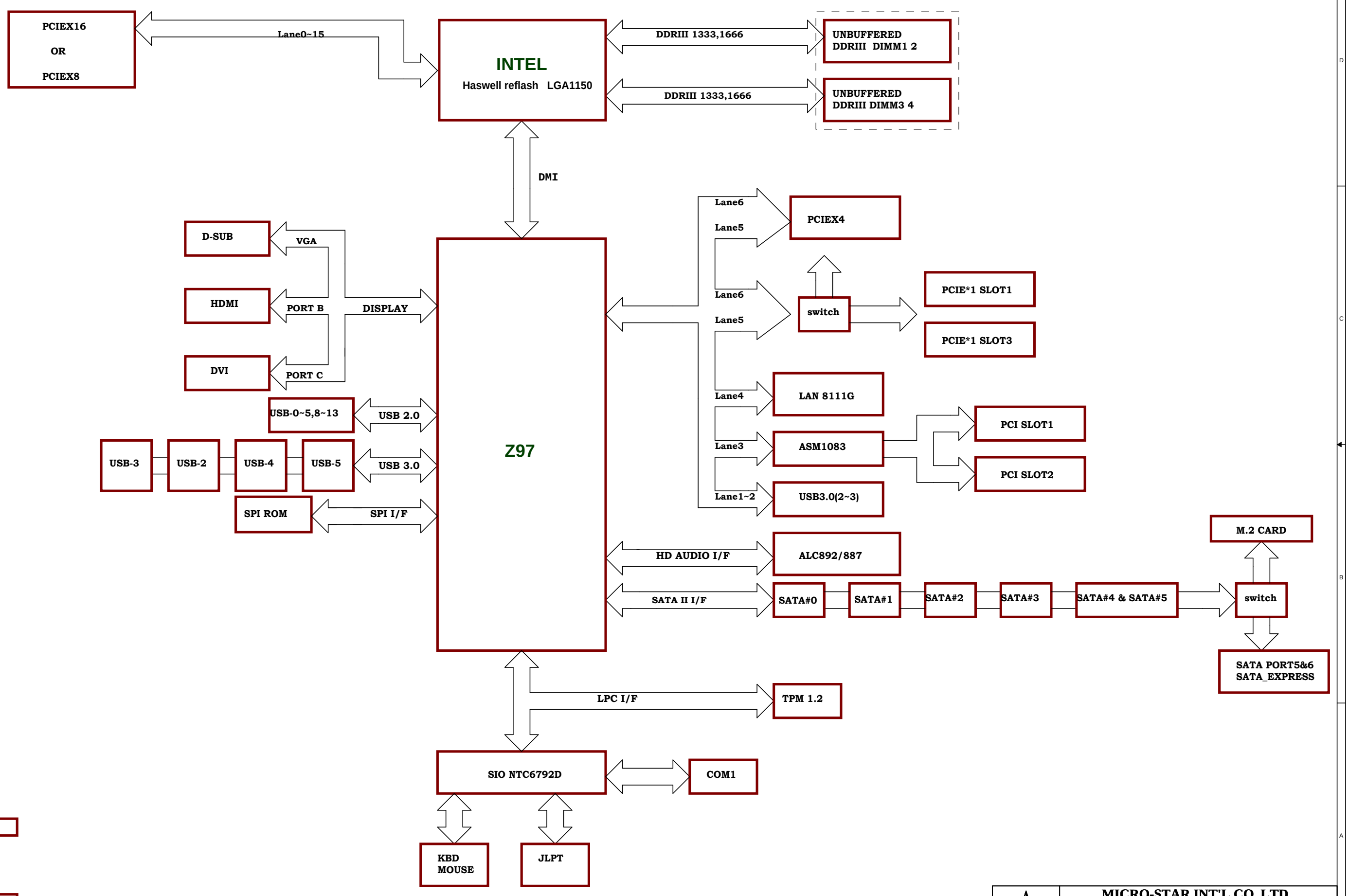
*REAR USB3.0 *4*

*FRONT USB3.0 *2*

*REAL USB3.1 *2 remove*

MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: Cover Sheet	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 1 of 49	

MS-7922 Block Diagram



Slot Sequence:

PCIE X1

PCIE X16

PCIE X1

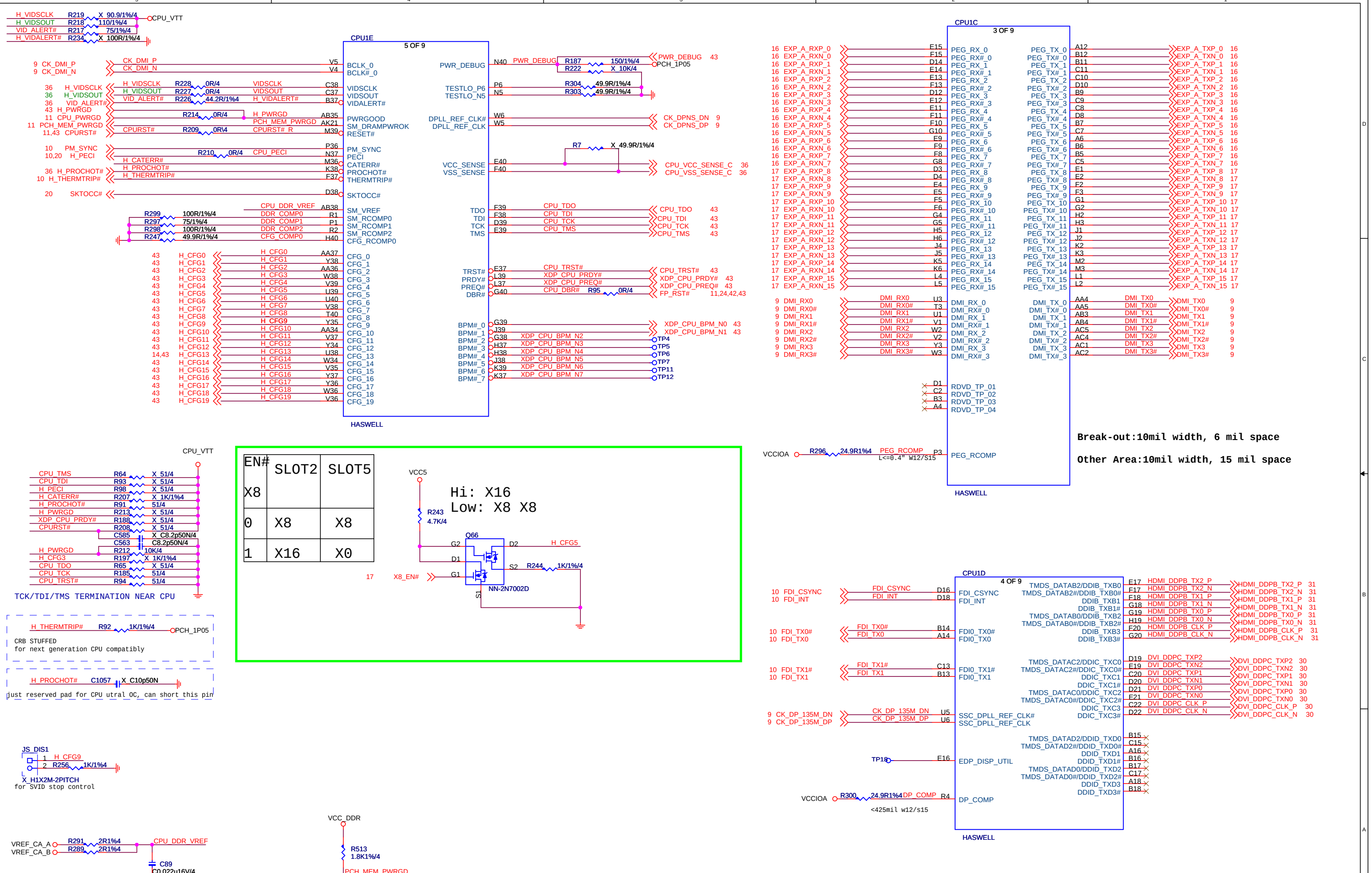
PCIE X1

PCIE X8

PCI

PCI

MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: Block Diagram	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 2 of 49	



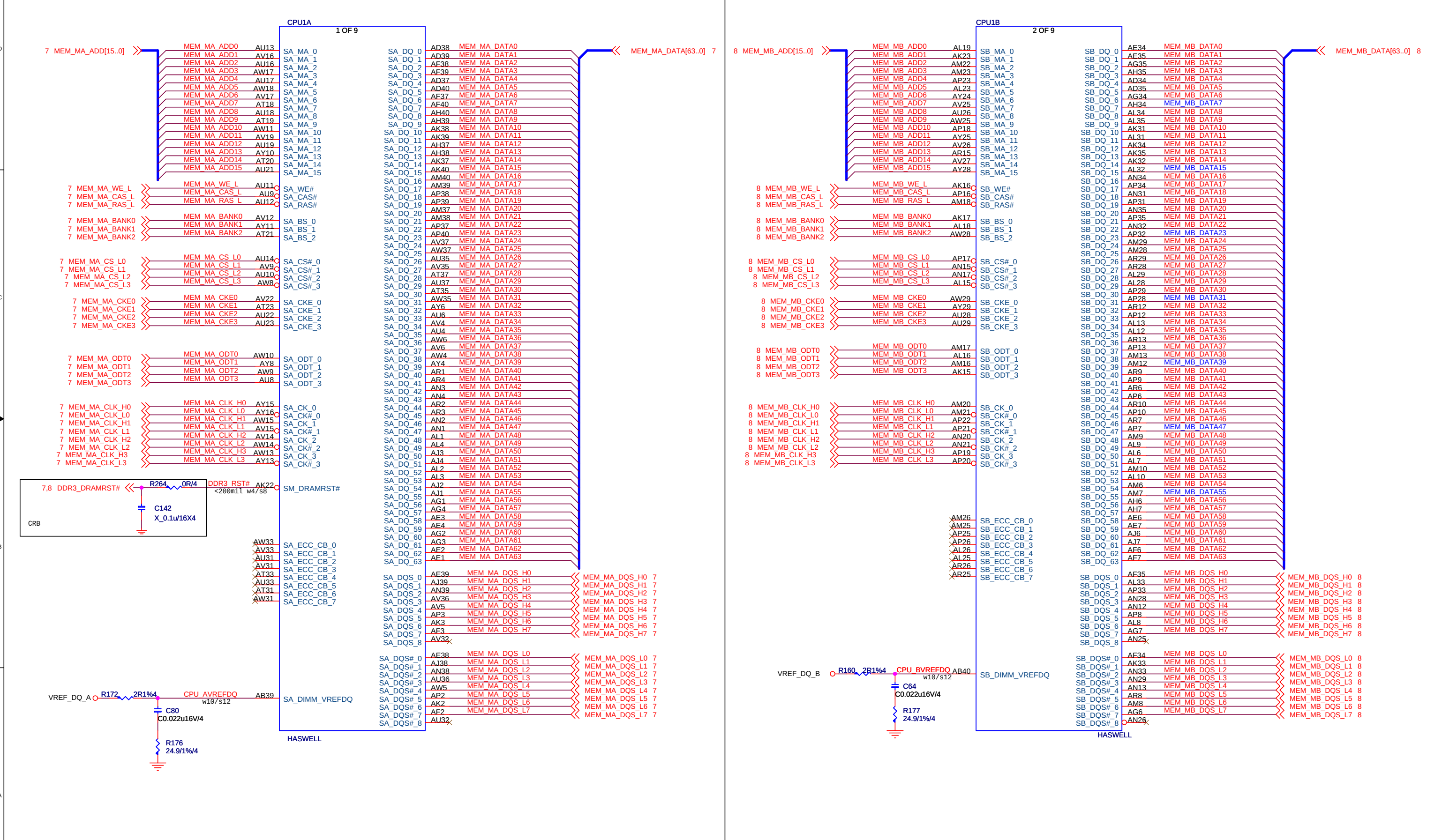
EN#	SLOT2	SLOT5
X8		
0	X8	X8
1	X16	X0

MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	CPU-CNTL/CLK/MISC	2.0

Date: Wednesday, July 16, 2014 | Sheet 3 of 49

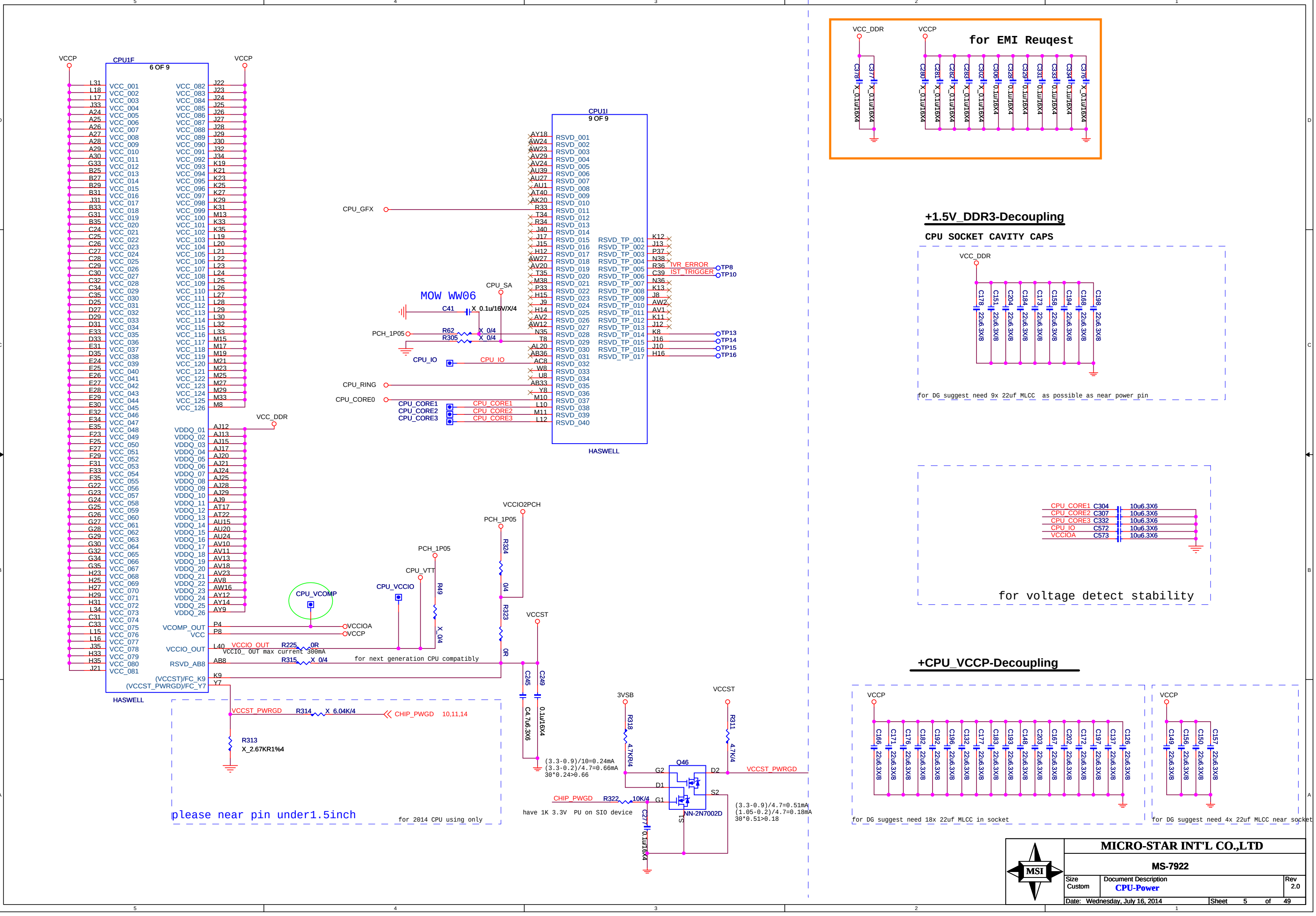


MICRO-STAR INT'L CO.,LTD

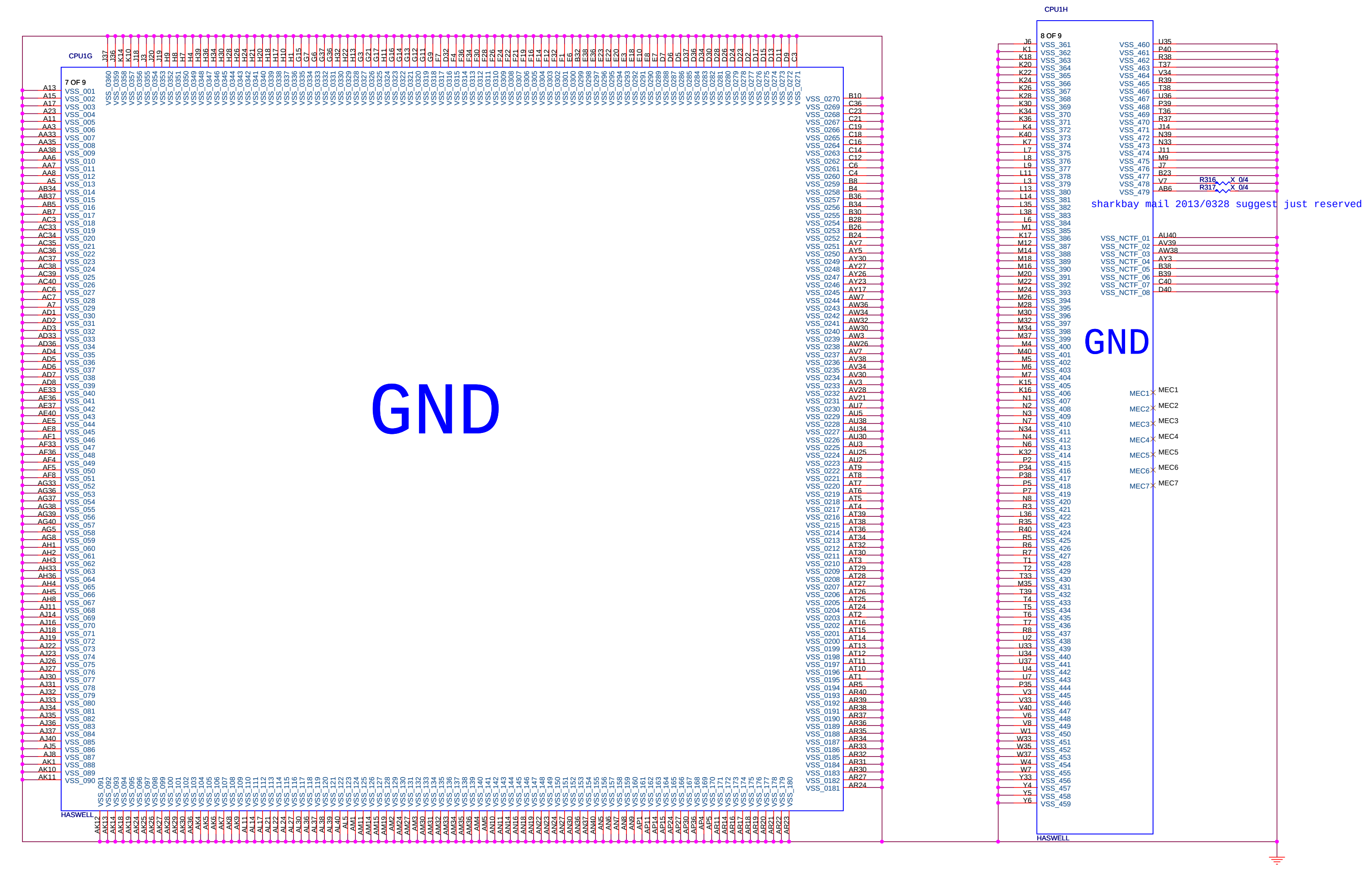
MS-7922

Size	Document Description	Rev
Custom	CPU-Memory	2.0

Date: Wednesday, July 16, 2014 Sheet 4 of 49



CPU1F
6 OF 9
HASWELL
CPU1I
9 OF 9
MOW WW06
for EMI Reuqest
+1.5V_DDR3-Decoupling
CPU SOCKET CAVITY CAPS
for DG suggest need 9x 22uf MLCC as possible as near power pin
for voltage detect stability
+CPU_VCCP-Decoupling
for DG suggest need 18x 22uf MLCC in socket
for DG suggest need 4x 22uf MLCC near socket
VCCIO_ OUT max current 300mA
for next generation CPU compatibly
please near pin under1.5inch
for 2014 CPU using only
have 1K 3.3V PU on SIO device
(3.3-0.9)/10=0.24mA
(3.3-0.2)/4.7=0.66mA
30*0.24>0.66
(3.3-0.9)/4.7=0.51mA
(1.05-0.2)/4.7=0.18mA
30*0.51>0.18
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
CPU-Power
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 5 of 49

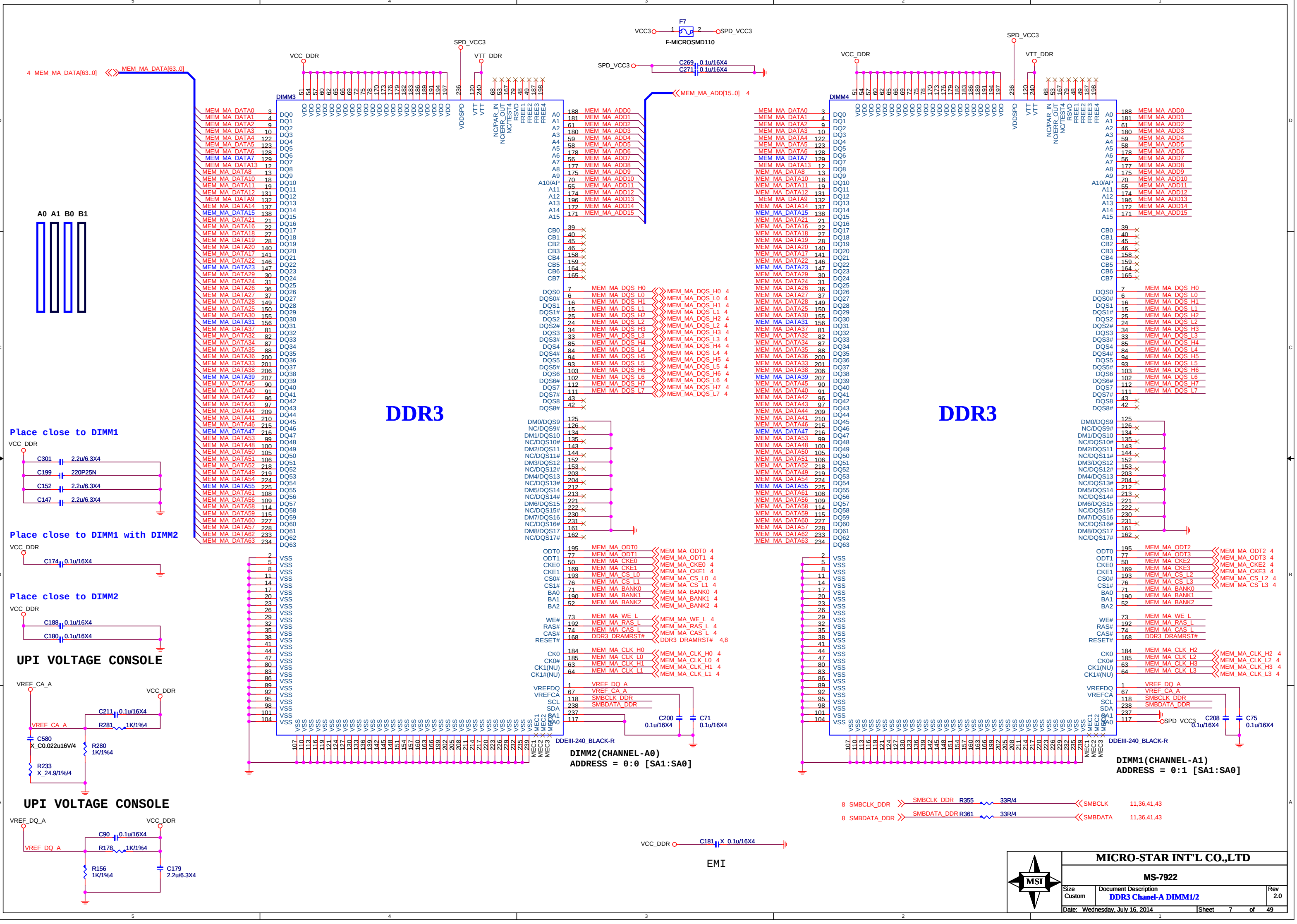


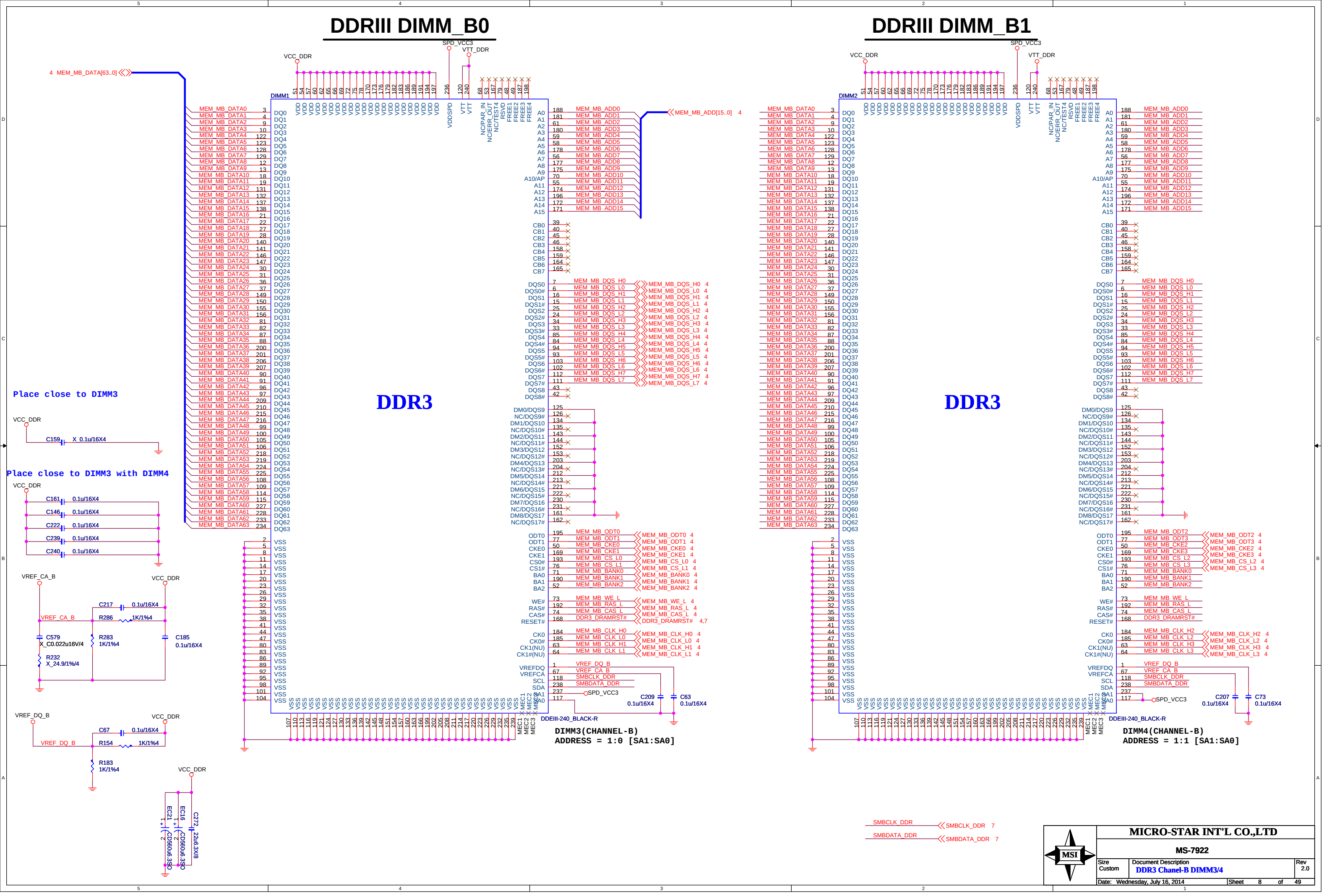
MICRO-STAR INT'L CO.,LTD

MS-7922

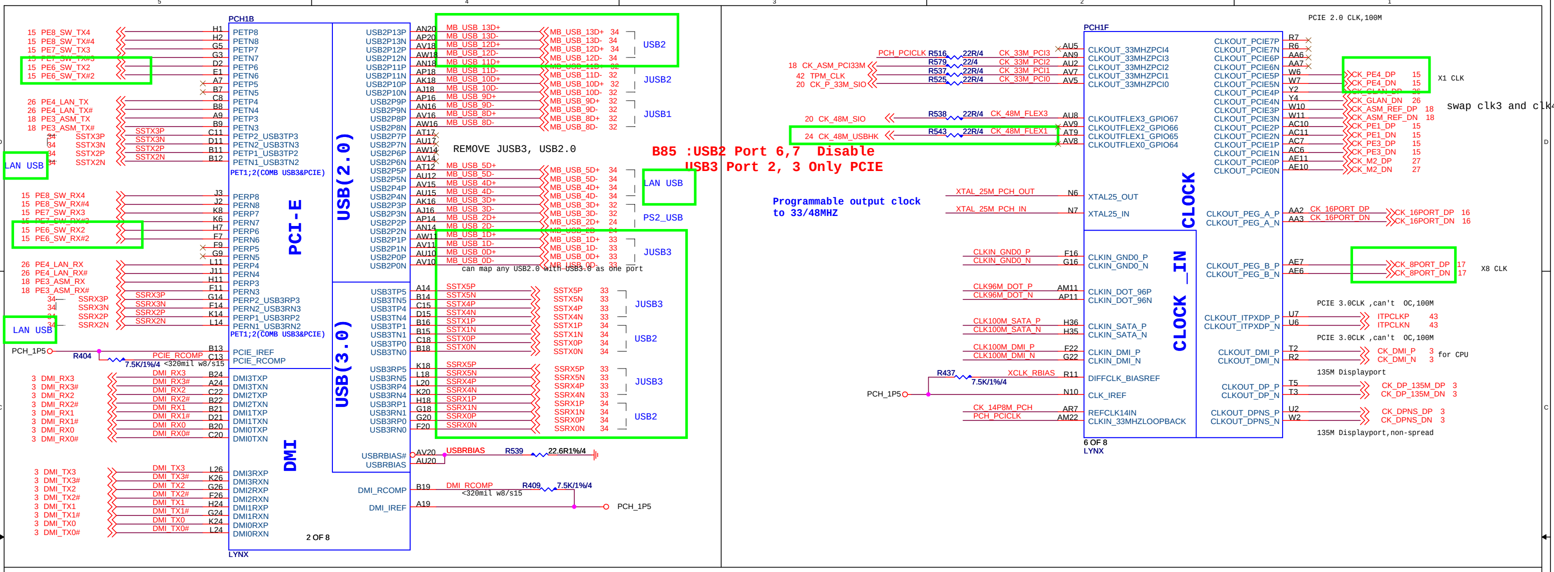
Size	Document Description	Rev
Custom	CPU-GND	2.0

Date: Wednesday, July 16, 2014 Sheet 6 of 49

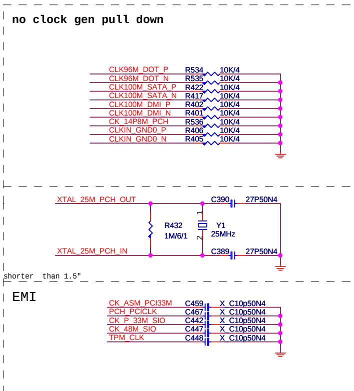

DDR3
DDR3
DIMM3
DIMM4
Place close to DIMM1
Place close to DIMM1 with DIMM2
Place close to DIMM2
UPI VOLTAGE CONSOLE
UPI VOLTAGE CONSOLE
DIMM2(CHANNEL-A0)
ADDRESS = 0:0 [SA1:SA0]
DIMM1(CHANNEL-A1)
ADDRESS = 0:1 [SA1:SA0]
DDEIII-240_BLACK-R
F-MICROSMD110
EMI
MICRO-STAR INT'L CO.,LTD
MS-7922
Document Description
DDR3 Chanel-A DIMM1/2
Size
Custom
Rev
2.0
Date: Wednesday, July 16, 2014
Sheet 7 of 49



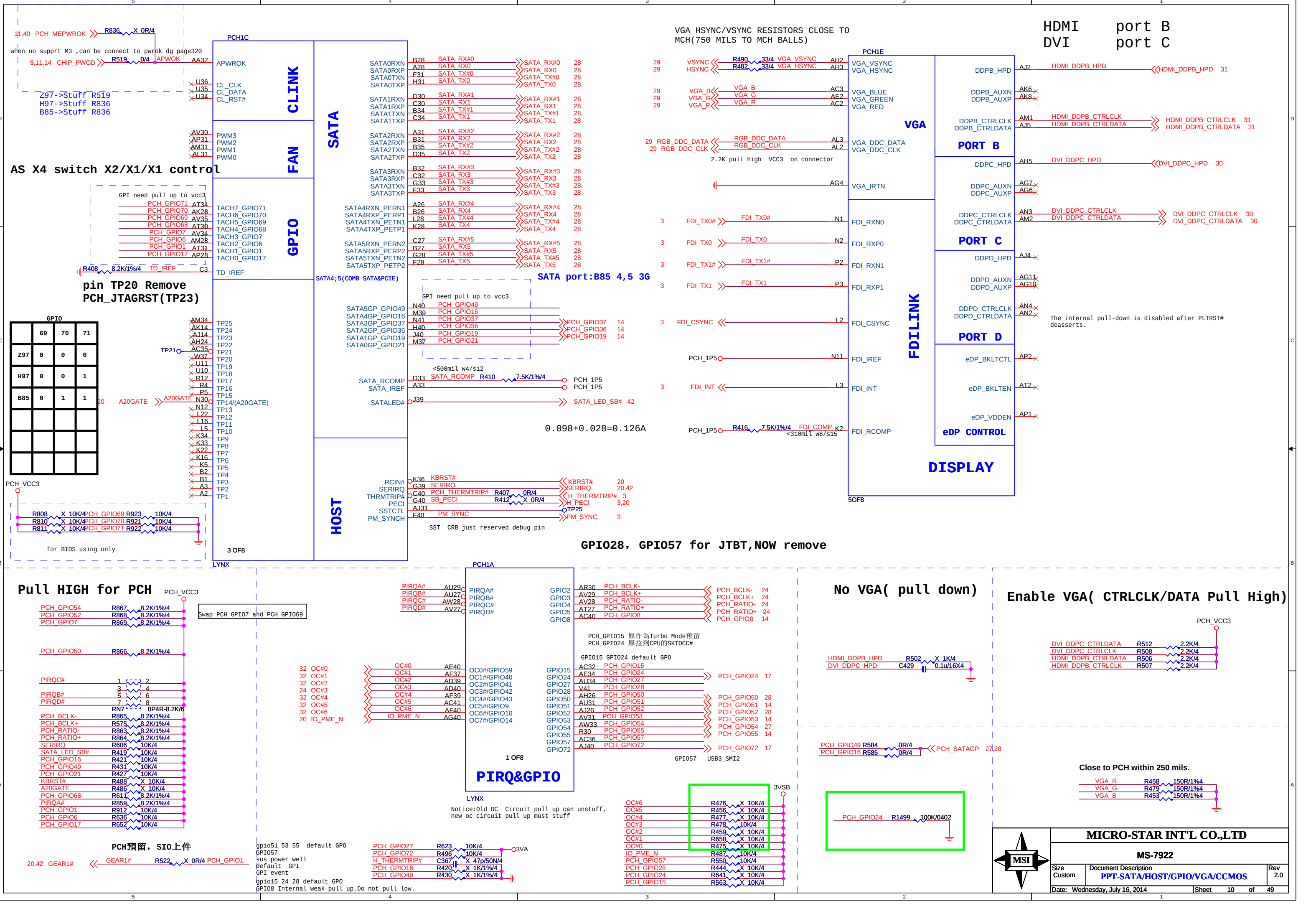
DDRIII DIMM_B0
DDRIII DIMM_B1
DDR3
DDR3
Place close to DIMM3
Place close to DIMM3 with DIMM4
DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
DDEIII-240_BLACK-R
4 MEM_MB_DATA[63..0]
MEM_MB_ADD[15..0] 4
VCC_DDR
SPD_VCC3
VTT_DDR
VREF_CA_B
VREF_DQ_B
SMBCLK_DDR
SMBDATA_DDR
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
DDR3 Chanel-B DIMM3/4
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 8 of 49



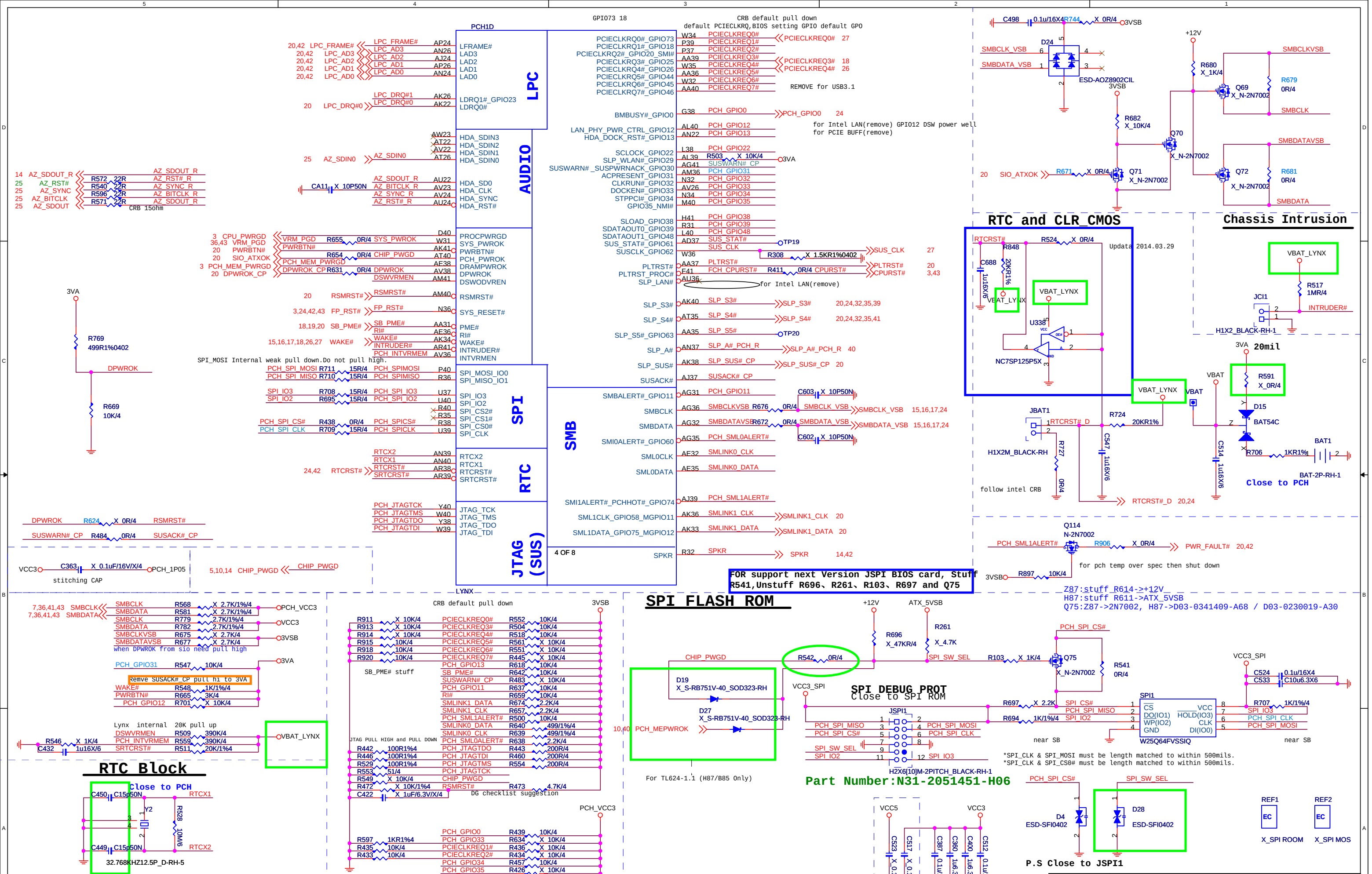
PCIE CLK BUFFER(remove)



MICRO-STAR INT'L CO.,LTD			
MS-7922			
Size Custom	Document Description PPT-PCI/E/DMI/CLK/USB20		Rev 2.0
Date: Wednesday, July 16, 2014	Sheet 9	of 49	



HDMI port B
DVI port C
VGA HSYNC/VSYNC RESISTORS CLOSE TO MCH(750 MILS TO MCH BALLS)
when no supprt M3 ,can be connect to pwrok dg page320
Z97->Stuff R519
H97->Stuff R836
B85->Stuff R836
AS X4 switch X2/X1/X1 control
GPI need pull up to vcc3
pin TP20 Remove
PCH_JTAGRST(TP23)
GPIO
69 70 71
Z97 0 0 0
H97 0 0 1
B85 0 1 1
for BIOS using only
CLINK
FAN
GPIO
SATA
HOST
SATA4;5(COMB SATA&PCIE)
SATA port:B85 4,5 3G
GPI need pull up to vcc3
<500mil w4/s12
0.098+0.028=0.126A
SST CRB just reserved debug pin
GPIO28, GPIO57 for JTBT,NOW remove
2.2K pull high VCC3 on connector
VGA
PORT B
PORT C
PORT D
eDP CONTROL
FDILINK
DISPLAY
<310mil w8/s15
The internal pull-down is disabled after PLTRST# deasserts.
Pull HIGH for PCH
Swap PCH_GPIO7 and PCH_GPIO69
PCH预留，SIO上件
PCH_GPIO15 原作為Turbo Mode预留
PCH_GPIO24 原拉到CPU的SKTOCC#
GPIO15 GPIO24 default GPO
PIRQ&GPIO
Notice:Old OC Circuit pull up can unstuff, new oc circuit pull up must stuff
gpio51 53 55 default GPO
GPIO57
sus power well
default GPI
GPI event
gpio15 24 28 default GPO
GPIO8 Internal weak pull up.Do not pull low.
GPIO57 USB3_SMI2
No VGA(pull down)
Enable VGA(CTRLCLK/DATA Pull High)
Close to PCH within 250 mils.
MICRO-STAR INT'L CO.,LTD
MS-7922
Document Description
PPT-SATA/HOST/GPIO/VGA/CCMOS
Size Custom
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 10 of 49

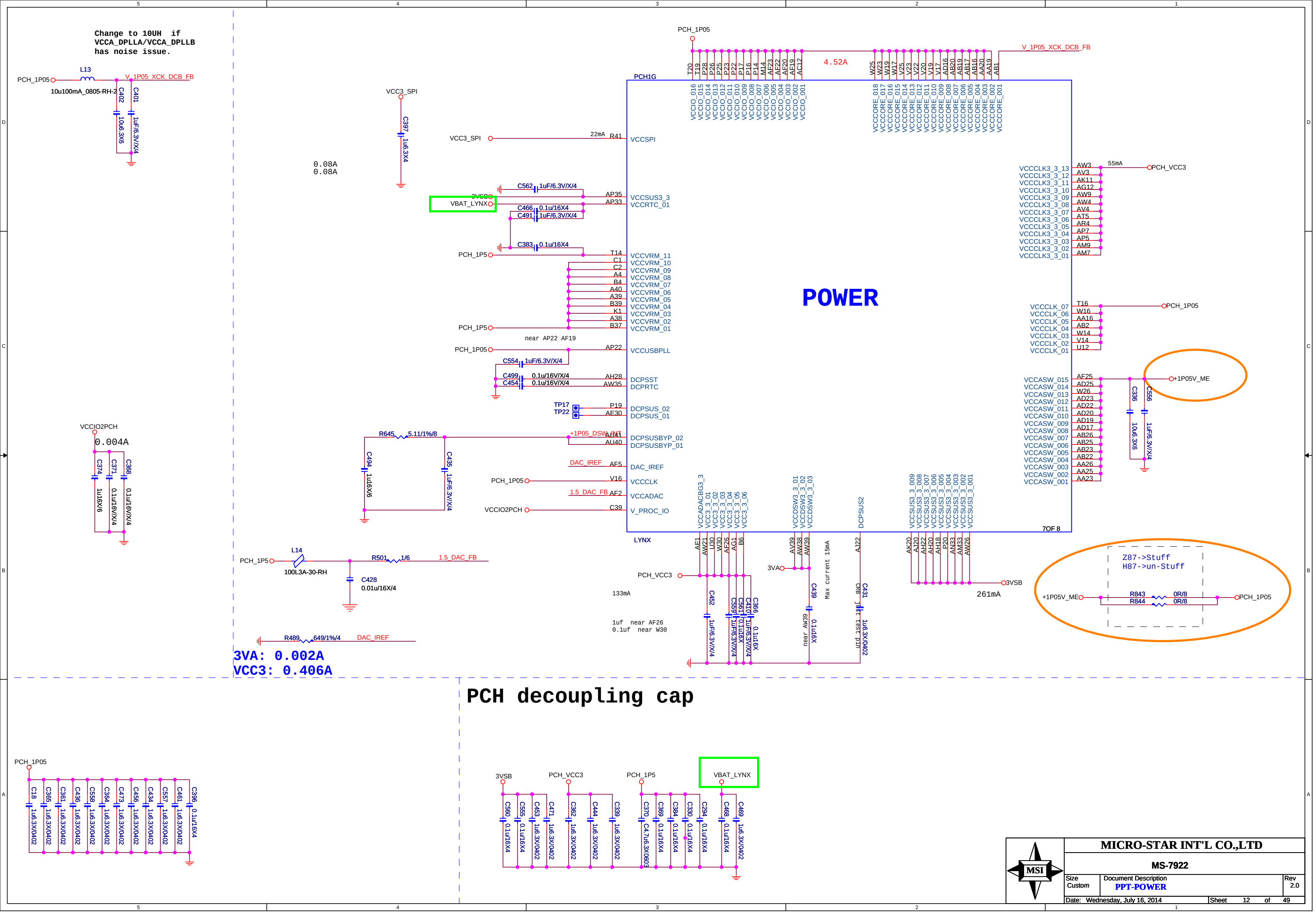


MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	PPT-SMB/LPC/AUDIO/RTC/SPI	2.0

Date: Wednesday, July 16, 2014 Sheet 11 of 49

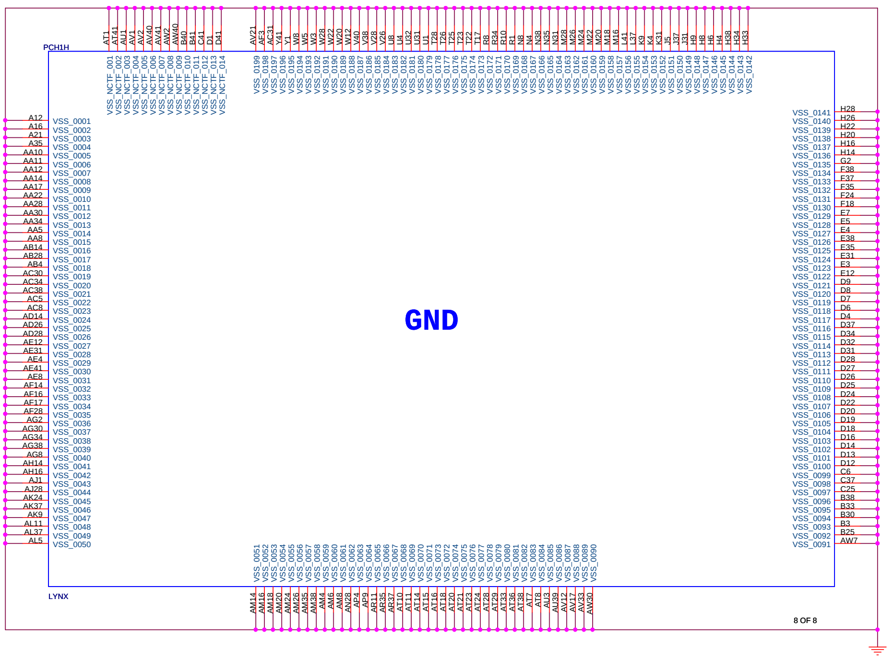


MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	PPT-POWER	2.0

Date: Wednesday, July 16, 2014 Sheet 12 of 49



MICRO-STAR INT'L CO.,LTD			
MS-7922			
Size: Custom	Document Description: PPT-GND/NVRAM/USB30		Rev: 2.0
Date: Wednesday, July 16, 2014		Sheet 13 of 49	

PCH Straps

Internal pull-DOWN

SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

11,42 SPKR — SPKR — R505 X 1K/4 — PCH_VCC3

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

10 PCH_GPIO51, 10 PCH_GPIO19 — PCH_GPIO51 R499 X 10K/4; PCH_GPIO19 R415 10K/4; PCH_GPIO51 R576 X 1K/4; PCH_GPIO19 R423 X 1K/4 — PCH_VCC3

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

10 PCH_GPIO55 — PCH_GPIO55 R521 X 4.7K/4

Internal pull-up

Connect to ground with 1k Ohm pull-down resistor.

10 PCH_GPIO53 — PCH_GPIO53 R600 X 1K/4

10 PCH_GPIO8 — PCH_GPIO8 — R741 X 1K/4 PCH_VCC3; R609 1K/4 3VSB; R455 1K/4

Internal pull-up
follow TPE ,in fact just need pull up only

30((3.3-0.95)10=7.05mA
(1.05-0.2)/1=0.85mA

3VSB R617 10K/4; PCH_GPIO8 R593 10K/4; Q68 NN-CMKT3904; R582 1K/4 H_CFG13 — H_CFG13 3,43

30((3.3/2)-0.95)10=2.1mA
(3.3-0.2)10=0.31mA

JME1 H1X2M-2PITCH — R704 1K/4 — 3VSB; AZ_SDOUT_R — AZ_SDOUT_R 11

SIO_5VSB — R698 47K/4; +12V — R699 47K/4 — Q76 NN-2N7002D (G2, D2, D1, S2, G1, S1)

20 ME_DIS# — SIO GPIO default GPI

Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

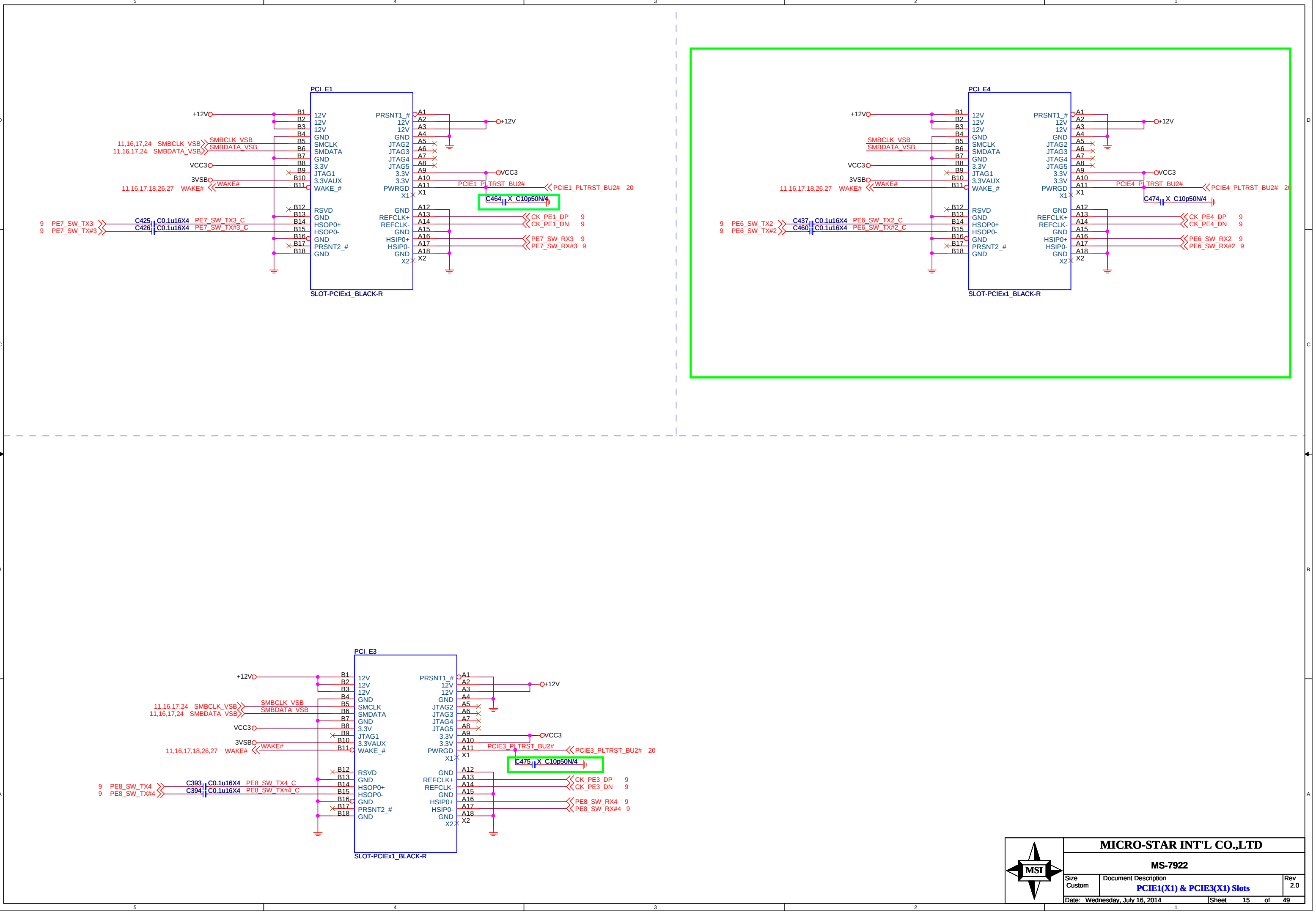
10 PCH_GPIO36 — PCH_GPIO36 R414 X 1K/4; R413 X 10K/1%4 — PCH_VCC3

Internal weak pull down. Do not pull high.

10 PCH_GPIO37 — PCH_GPIO37 R544 X 1K/4 3VSB; R429 1K/4 PCH_VCC3; R428 X 10K/1%4

GPIO37 Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

J1 H1X2M-2PITCH — CHIP_PWGD 5,10,11

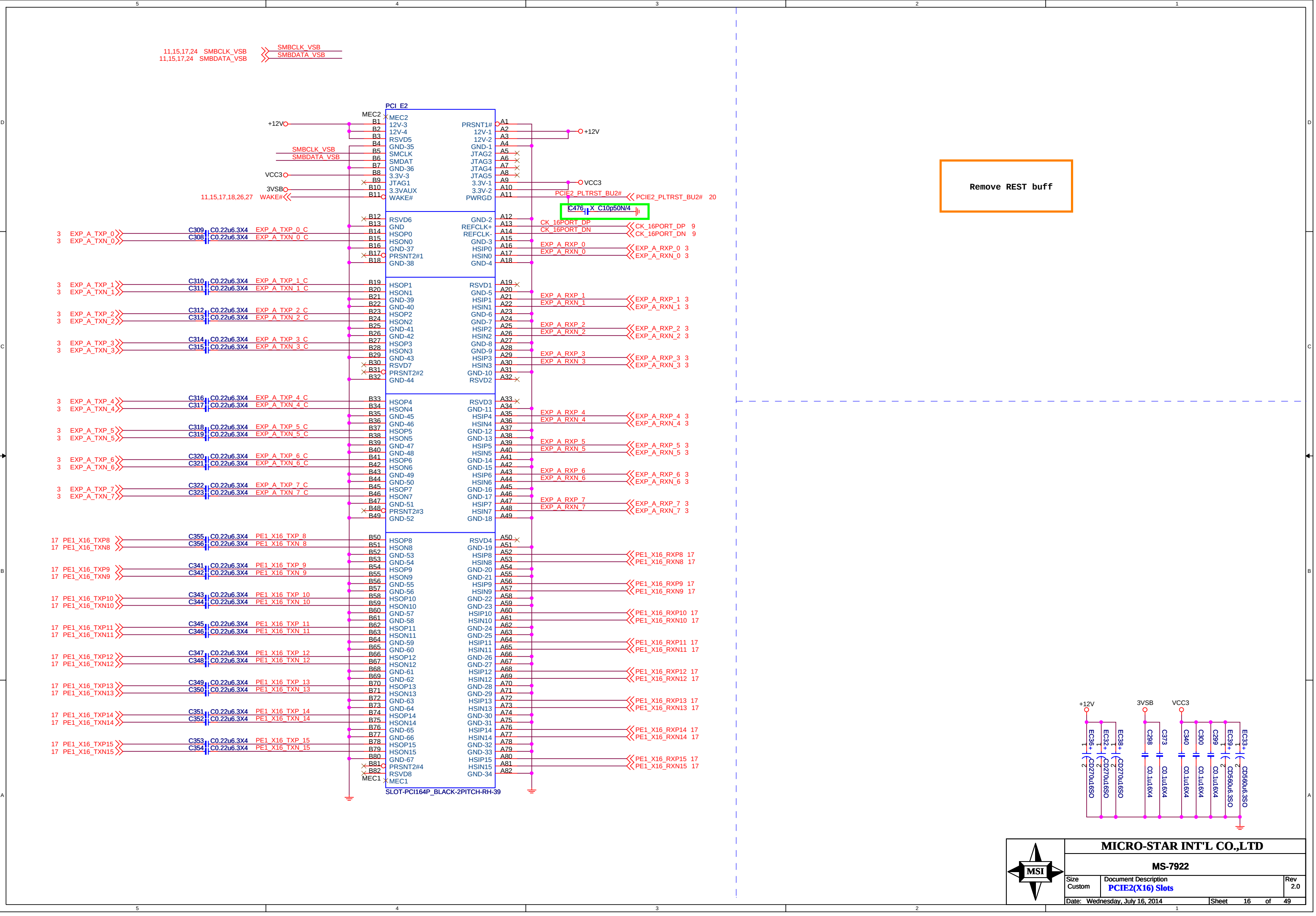


MICRO-STAR INT'L CO.,LTD

MS-7922

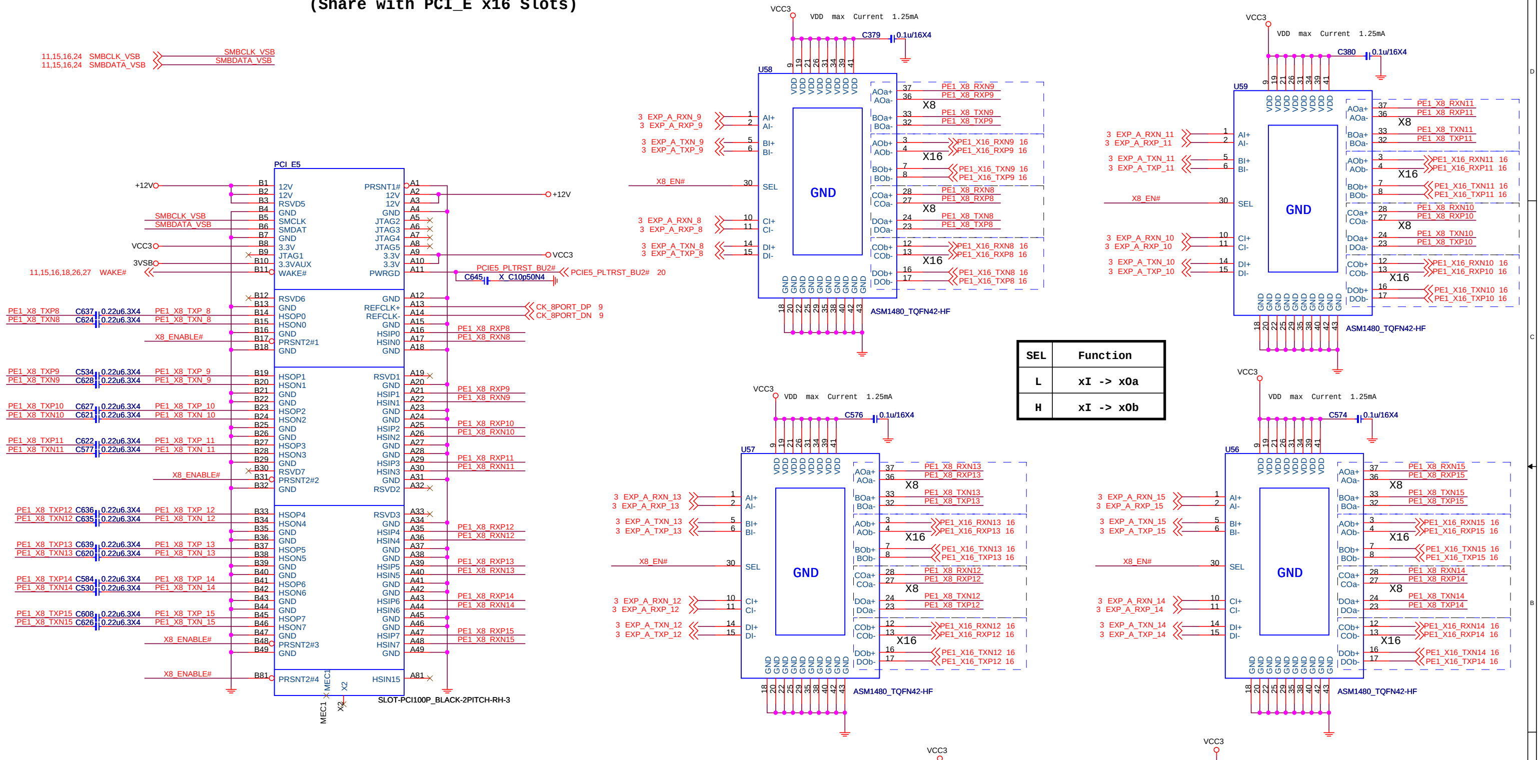
Size	Document Description	Rev
Custom	PCIE1(X1) & PCIE3(X1) Slots	2.0

Date: Wednesday, July 16, 2014 | Sheet 15 of 49



Remove REST buff
PCI_E2
SLOT-PCI164P_BLACK-2PITCH-RH-39
C476 X_C10p50N/4
PCIE2_PLTRST_BU2#
MICRO-STAR INT'L CO.,LTD
MS-7922
Size
Custom
Document Description
PCIE2(X16) Slots
Rev
2.0
Date: Wednesday, July 16, 2014
Sheet 16 of 49

PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



SEL	Function
L	xI -> xOa
H	xI -> xOb

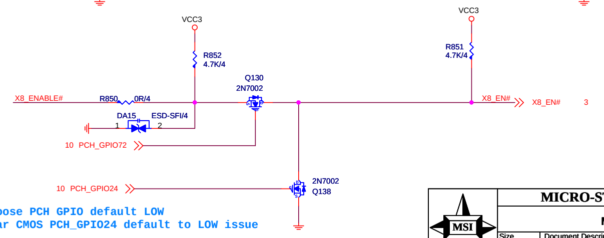
GPIO72

0: BIOS MODE
1: HW MODE

If USE HW MODE (Default)
PCH_GPIO24 programming to GPI
PCH_GPIO72 programming GPO

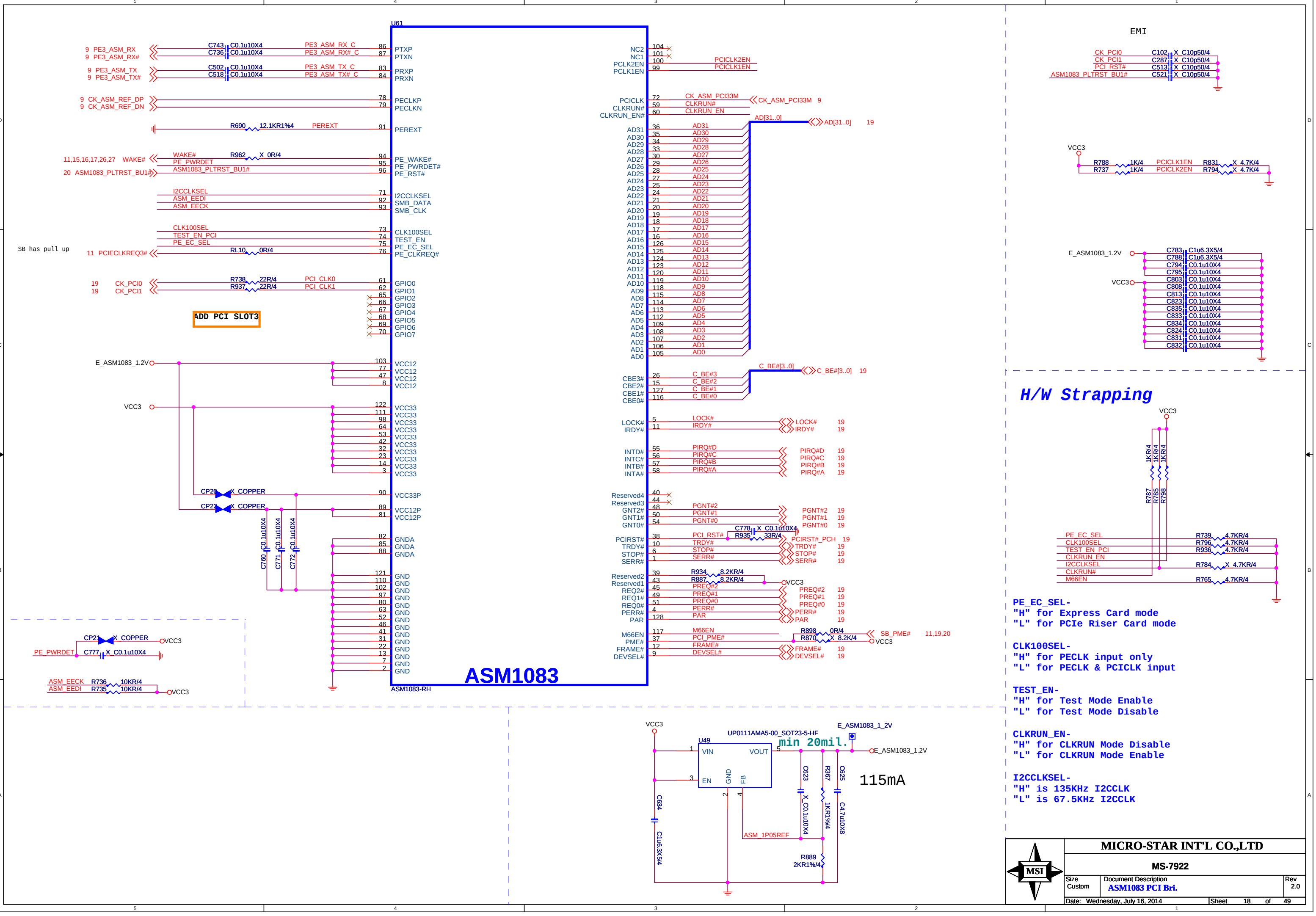
If USE BIOS MODE
PCH_GPIO24 & PCH_GPIO72
programming to GPO

PCH / Status	GPIO24	GPIO72
AUTO	GPI	1
16,0,0	0	0
8,8,0	1	0



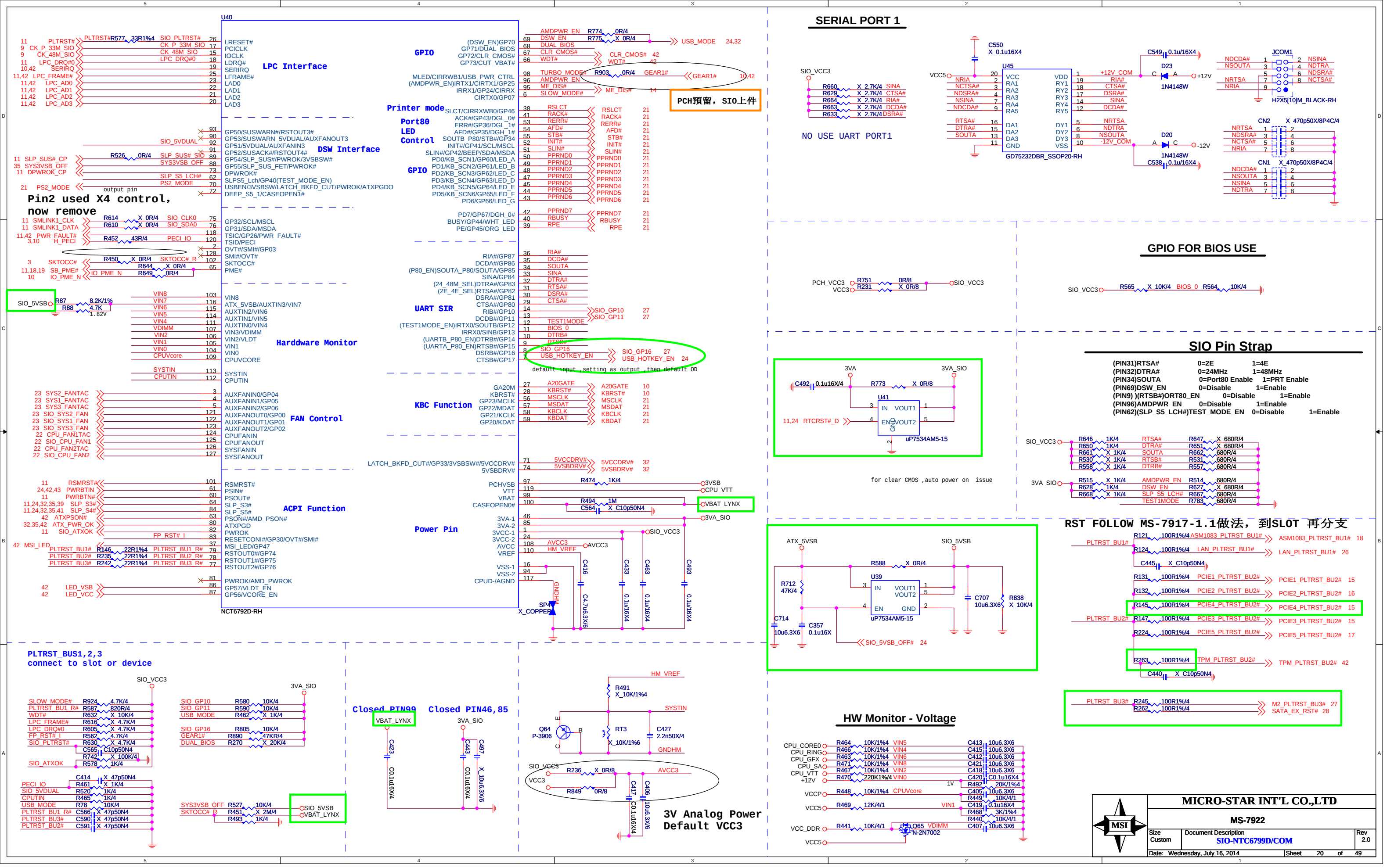
Please choose PCH GPIO default LOW
Patch Clear CMOS PCH_GPIO24 default to LOW issue

MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: PCIE(X8) slots	Rev 2.0
Date: Wednesday, July 16, 2014	Sheet 17 of 49	

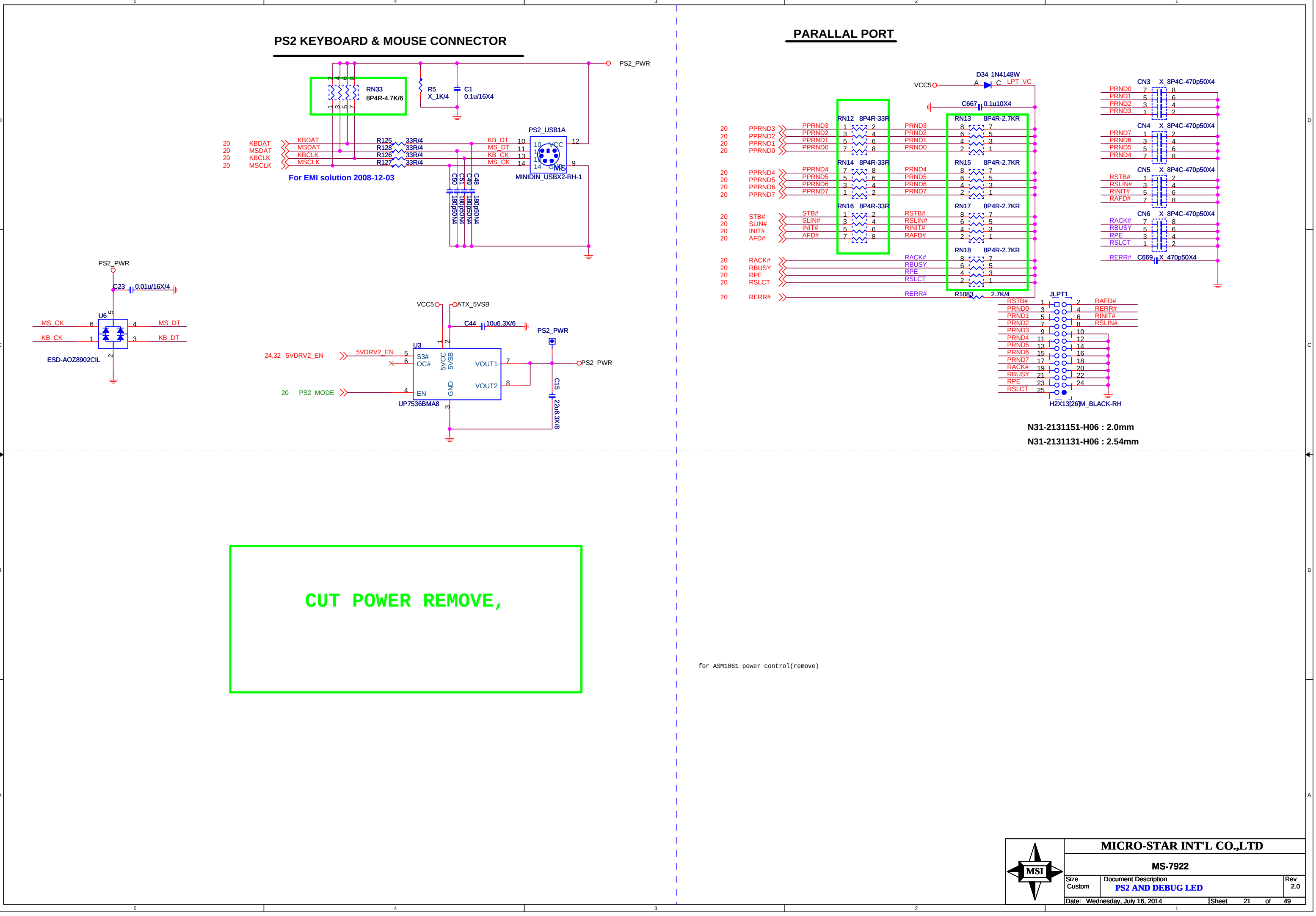


ASM1083
U61
ASM1083-RH
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC12
VCC33
VCC33P
VCC12P
GNDA
GND
NC2
NC1
PCLK2EN
PCLK1EN
PCICLK
CLKRUN#
CLKRUN_EN#
AD31 … AD0
CBE3#
CBE2#
CBE1#
CBE0#
LOCK#
IRDY#
INTD#
INTC#
INTB#
INTA#
Reserved4
Reserved3
GNT2#
GNT1#
GNT0#
PCIRST#
TRDY#
STOP#
SERR#
Reserved2
Reserved1
REQ2#
REQ1#
REQ0#
PERR#
PAR
M66EN
PME#
FRAME#
DEVSEL#
9 PE3_ASM_RX
9 PE3_ASM_RX#
9 PE3_ASM_TX
9 PE3_ASM_TX#
9 CK_ASM_REF_DP
9 CK_ASM_REF_DN
11,15,16,17,26,27 WAKE#
20 ASM1083_PLTRST_BU1#
SB has pull up
11 PCIECLKREQ3#
19 CK_PCI0
19 CK_PCI1
ADD PCI SLOT3
E_ASM1083_1.2V
VCC3
CP20 X_COPPER
CP22 X_COPPER
CP21 X_COPPER
PE_PWRDET
ASM_EECK
ASM_EEDI
CK_ASM_PCI33M 9
AD[31..0] 19
C_BE#[3..0] 19
SB_PME# 11,19,20
EMI
H/W Strapping
UP0111AMA5-00_SOT23-5-HF
U49
VIN
VOUT
EN
GND
FB
min 20mil.
115mA
ASM_1P05REF
E_ASM1083_1_2V
PE_EC_SEL-
"H" for Expres Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
MICRO-STAR INT'L CO.,LTD
MSI
MS-7922
Size Custom
Document Description
ASM1083 PCI Bri.
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 18 of 49


PCI1
SLOT-PCI120P_BLACK-RH
PCI2
SLOT-PCI120P_BLACK-RH
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
PCI PULL-UP / DOWN RESISTORS
RN32 8P4R-8.2K/6
RN22 8P4R-8.2K/6
RN31 8P4R-8.2K/6
RN20 8P4R-8.2K/6
Swap net PIRQ#B and net PIRQ#C
AD[31..0]
C_BE#[3..0]
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description PCIx2 Slots
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 19 of 49

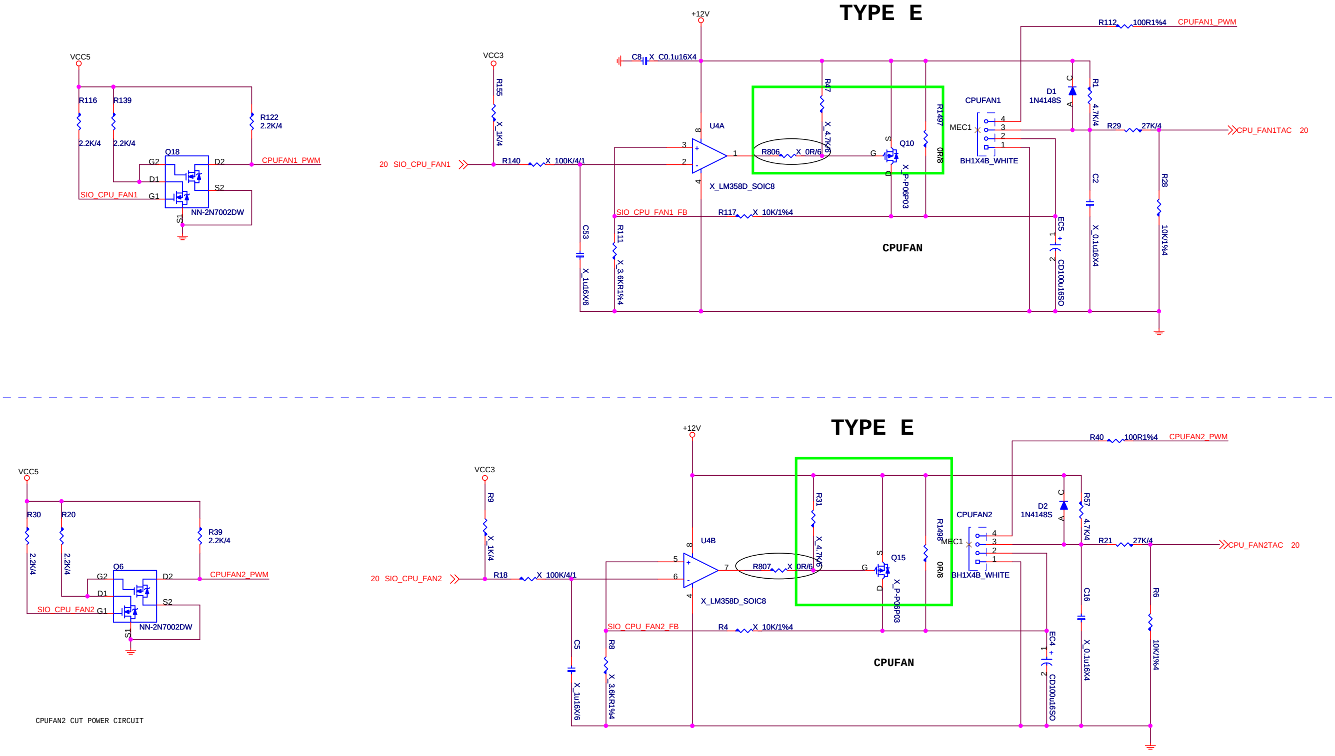


U40
LPC Interface
GPIO
Printer mode
Port80
LED
Control
DSW Interface
Pin2 used X4 control, now remove
Hardware Monitor
FAN Control
UART SIR
KBC Function
ACPI Function
Power Pin
NCT6792D-RH
PCH預留，SIO上件
default input ,setting as output ,then default 0D
SERIAL PORT 1
NO USE UART PORT1
GD75232DBR_SSOP20-RH
H2X5[10]M_BLACK-RH
GPIO FOR BIOS USE
SIO Pin Strap
(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9)(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable
for clear CMOS ,auto power on issue
RST FOLLOW MS-7917-1.1做法，到SLOT 再分支
PLTRST_BUS1,2,3
connect to slot or device
Closed PIN99
Closed PIN46,85
3V Analog Power
Default VCC3
HW Monitor - Voltage
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description SIO-NTC6799D/COM
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 20 of 49



PS2 KEYBOARD & MOUSE CONNECTOR
PS2_PWR
RN33
8P4R-4.7K/6
R5
X_1K/4
C1
0.1u/16X4
KBDAT
MSDAT
KBCLK
MSCLK
R125
R128
R126
R127
33R/4
KB_DT
MS_DT
KB_CK
MS_CK
PS2_USB1A
MINIDIN_USBX2-RH-1
For EMI solution 2008-12-03
C50
C51
C49
C48
180p50N4
C23
0.01u/16X/4
U6
ESD-AOZ8902CIL
VCC5
ATX_5VSB
C44
10u6.3X/6
U3
UP7536BMA8
S3#
OC#
EN
5VCC
5VSB
GND
VOUT1
VOUT2
5VDRV2_EN
PS2_MODE
C15
22u6.3X/8
PARALLAL PORT
D34 1N4148W
LPT_VC
C667 0.1u10X4
RN12 8P4R-33R
RN14 8P4R-33R
RN16 8P4R-33R
RN13 8P4R-2.7KR
RN15 8P4R-2.7KR
RN17 8P4R-2.7KR
RN18 8P4R-2.7KR
R1083 2.7K/4
PPRND0
PPRND1
PPRND2
PPRND3
PPRND4
PPRND5
PPRND6
PPRND7
STB#
SLIN#
INIT#
AFD#
RACK#
RBUSY
RPE
RSLCT
RERR#
PRND0
PRND1
PRND2
PRND3
PRND4
PRND5
PRND6
PRND7
RSTB#
RSLIN#
RINIT#
RAFD#
CN3 X_8P4C-470p50X4
CN4 X_8P4C-470p50X4
CN5 X_8P4C-470p50X4
CN6 X_8P4C-470p50X4
C669 X_470p50X4
JLPT1
H2X13[26]M_BLACK-RH
N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm
CUT POWER REMOVE,
for ASM1061 power control(remove)
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
PS2 AND DEBUG LED
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 21 of 49

FAN-COUNTROL CIRCUIT

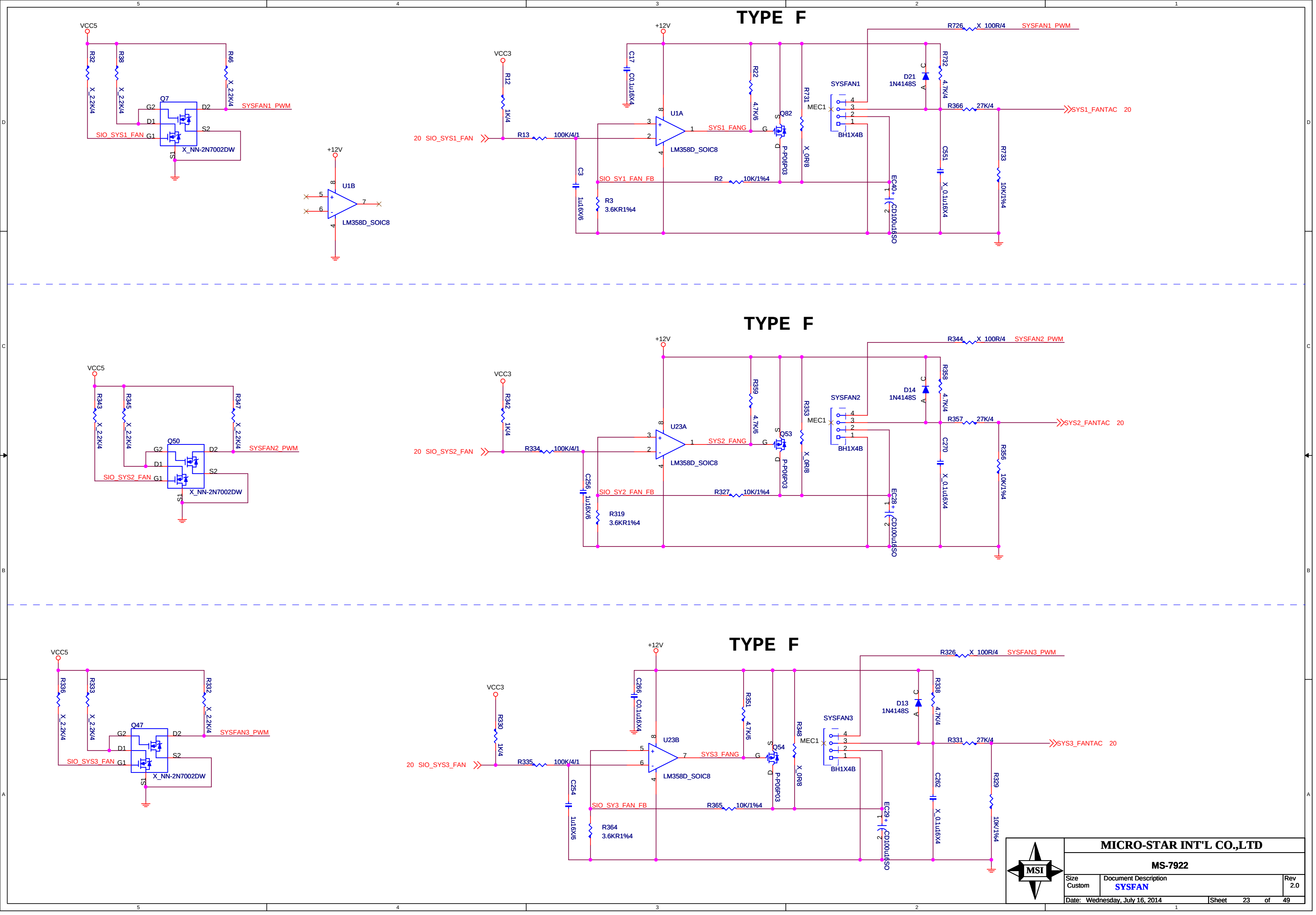


MICRO-STAR INT'L CO.,LTD

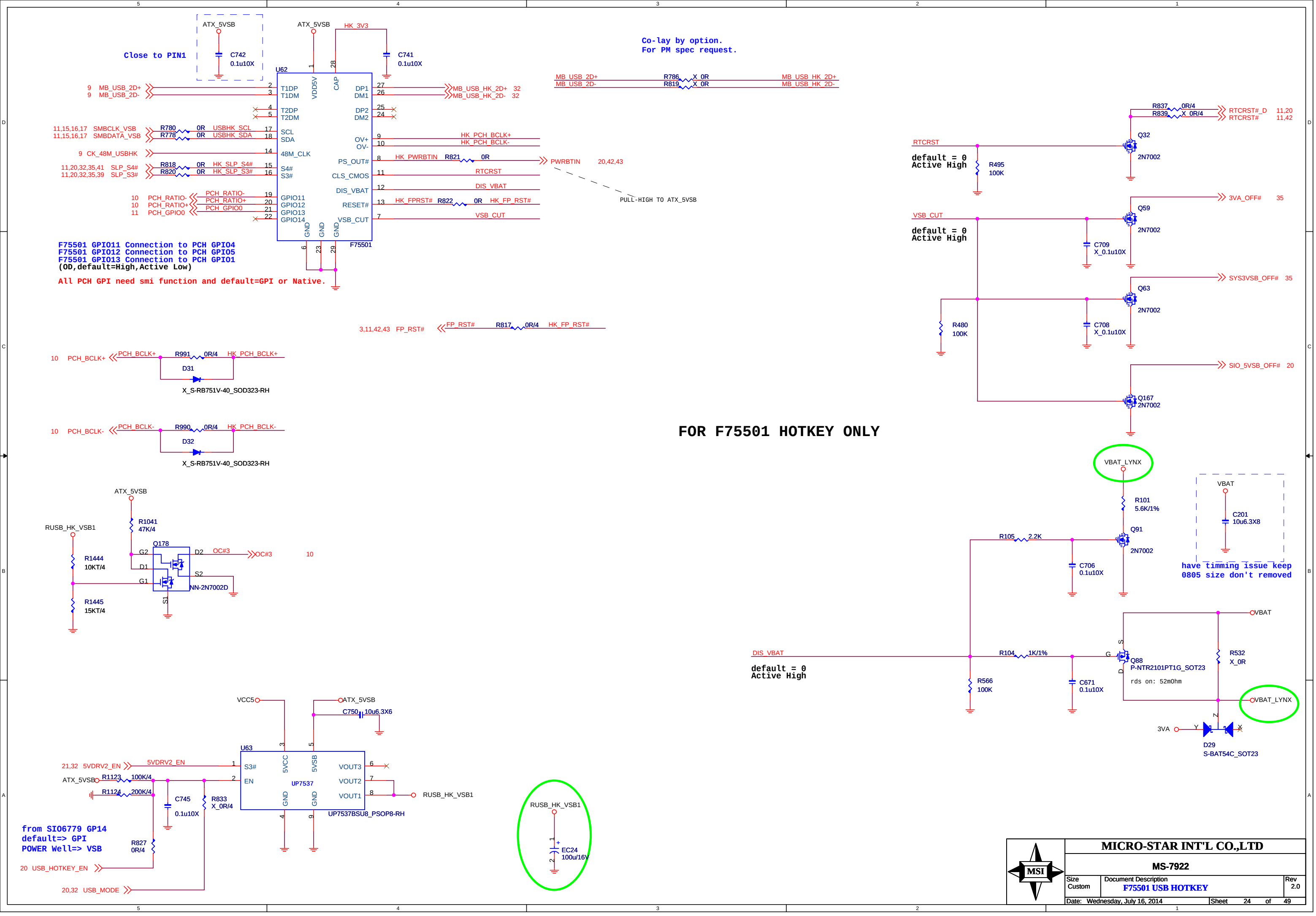
MS-7922

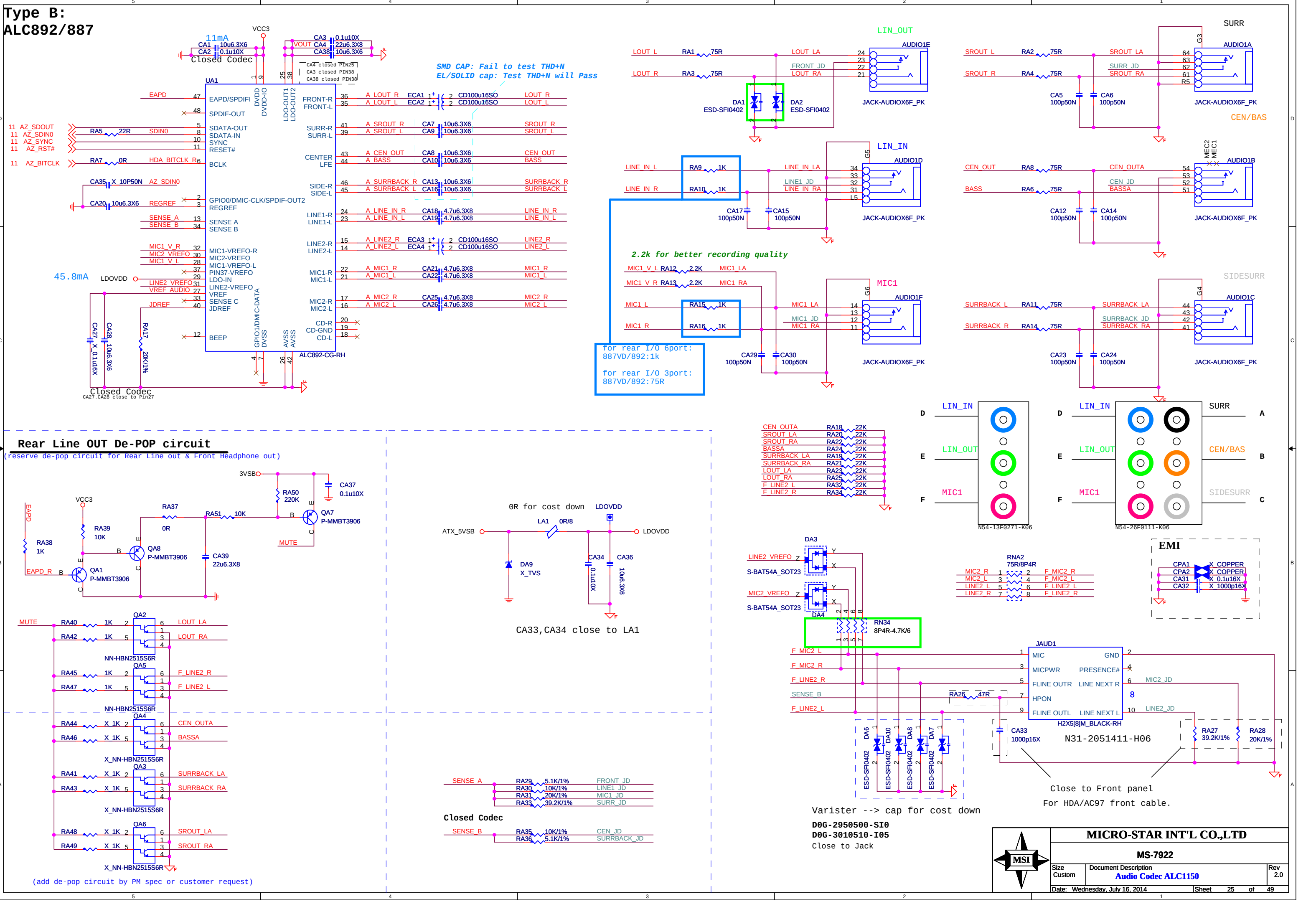
Size	Document Description	Rev
Custom	CPU FAN	2.0

Date: Wednesday, July 16, 2014 | Sheet 22 of 49



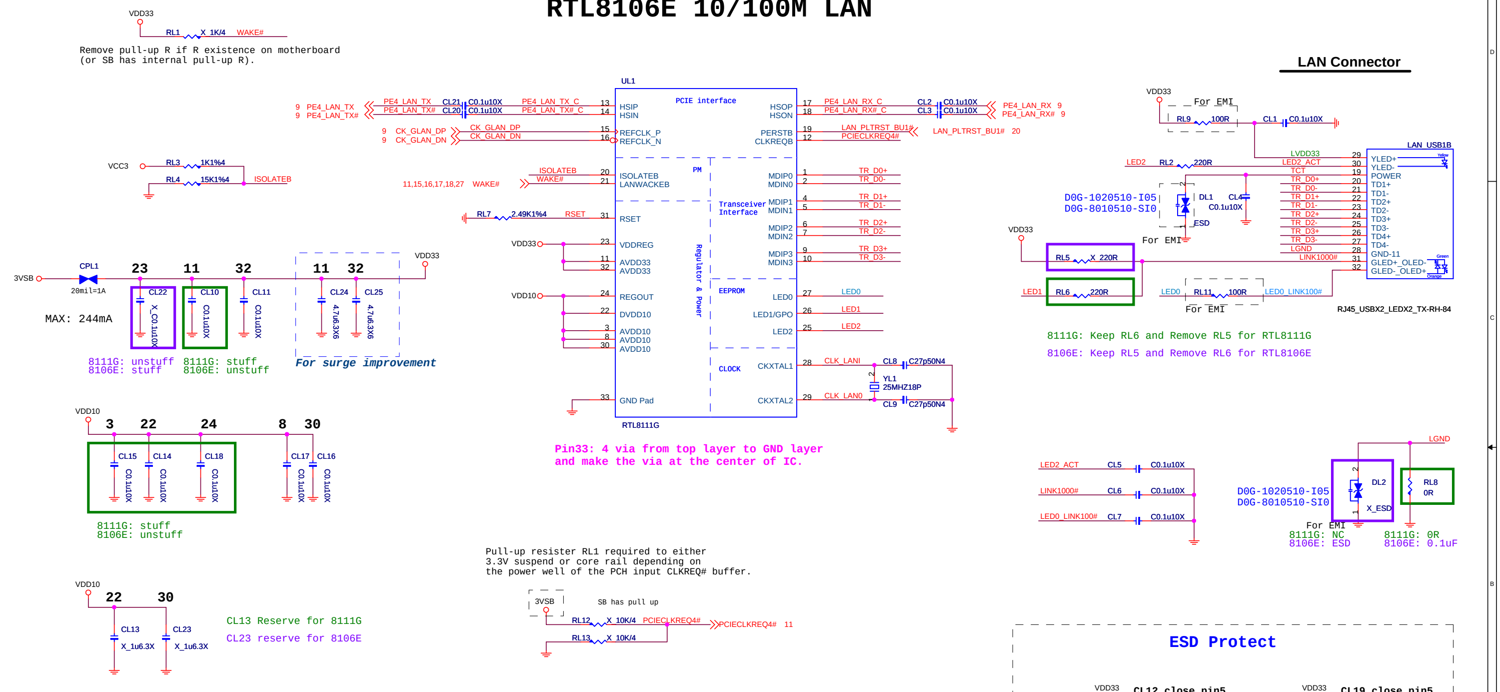
TYPE F
TYPE F
TYPE F
VCC5
+12V
VCC3
SIO_SYS1_FAN
SIO_SYS2_FAN
SIO_SYS3_FAN
SYSFAN1_PWM
SYSFAN2_PWM
SYSFAN3_PWM
SYS1_FANTAC
SYS2_FANTAC
SYS3_FANTAC
LM358D_SOIC8
X_NN-2N7002DW
BH1X4B
1N4148S
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
SYSFAN
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 23 of 49

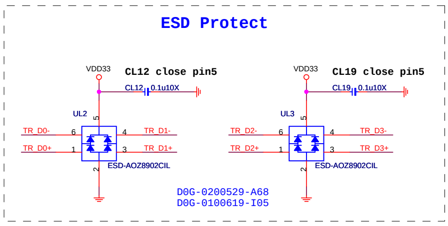

Close to PIN1
Co-lay by option.
For PM spec request.
F75501 GPIO11 Connection to PCH GPIO4
F75501 GPIO12 Connection to PCH GPIO5
F75501 GPIO13 Connection to PCH GPIO1
(OD,default=High,Active Low)
All PCH GPI need smi function and default=GPI or Native.
PULL-HIGH TO ATX_5VSB
default = 0
Active High
FOR F75501 HOTKEY ONLY
have timming issue keep
0805 size don't removed
rds on: 52mOhm
from SIO6779 GP14
default=> GPI
POWER Well=> VSB
U62
F75501
U63
UP7537
UP7537BSU8_PSOP8-RH
X_S-RB751V-40_SOD323-RH
NN-2N7002D
P-NTR2101PT1G_SOT23
S-BAT54C_SOT23
MICRO-STAR INT'L CO.,LTD
MS-7922
Size
Custom
Document Description
F75501 USB HOTKEY
Rev
2.0
Date: Wednesday, July 16, 2014
Sheet 24 of 49


Type B:
ALC892/887
11mA
Closed Codec
SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass
CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38
ALC892-CG-RH
45.8mA
LDOVDD
Closed Codec
CA27,CA28 close to Pin27
LIN_OUT
SURR
CEN/BAS
LIN_IN
MIC1
SIDESURR
2.2k for better recording quality
for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R
JACK-AUDIOX6F_PK
N54-13F0271-K06
N54-26F0111-K06
EMI
Rear Line OUT De-POP circuit
(reserve de-pop circuit for Rear Line out & Front Headphone out)
0R for cost down
ATX_5VSB
LDOVDD
CA33,CA34 close to LA1
(add de-pop circuit by PM spec or customer request)
Closed Codec
RN34
8P4R-4.7K/6
JAUD1
H2X5[8]M_BLACK-RH
N31-2051411-H06
Close to Front panel
For HDA/AC97 front cable.
Varister --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
Audio Codec ALC1150
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 25 of 49

RTL8111G Giga LAN

RTL8106E 10/100M LAN





8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

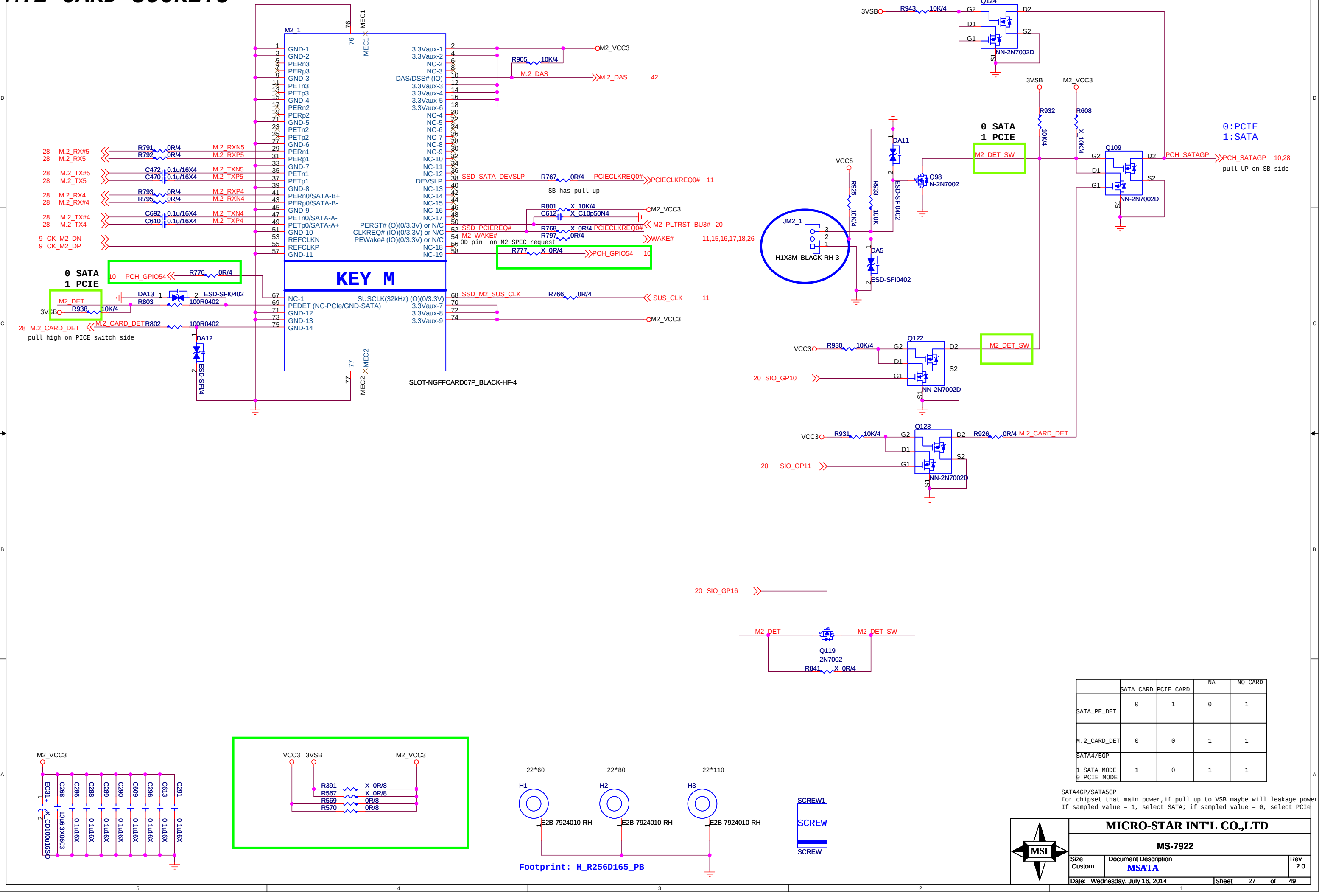
MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	Intel Clvrkville I217V / I218V PHY	2.0

Date: Wednesday, July 16, 2014 Sheet 26 of 49

M.2 CARD SOCKET3



	SATA CARD	PCIE CARD	NA	NO CARD
SATA_PE_DET	0	1	0	1
M.2_CARD_DET	0	0	1	1
SATA4/5GP 1 SATA MODE 0 PCIE MODE	1	0	1	1

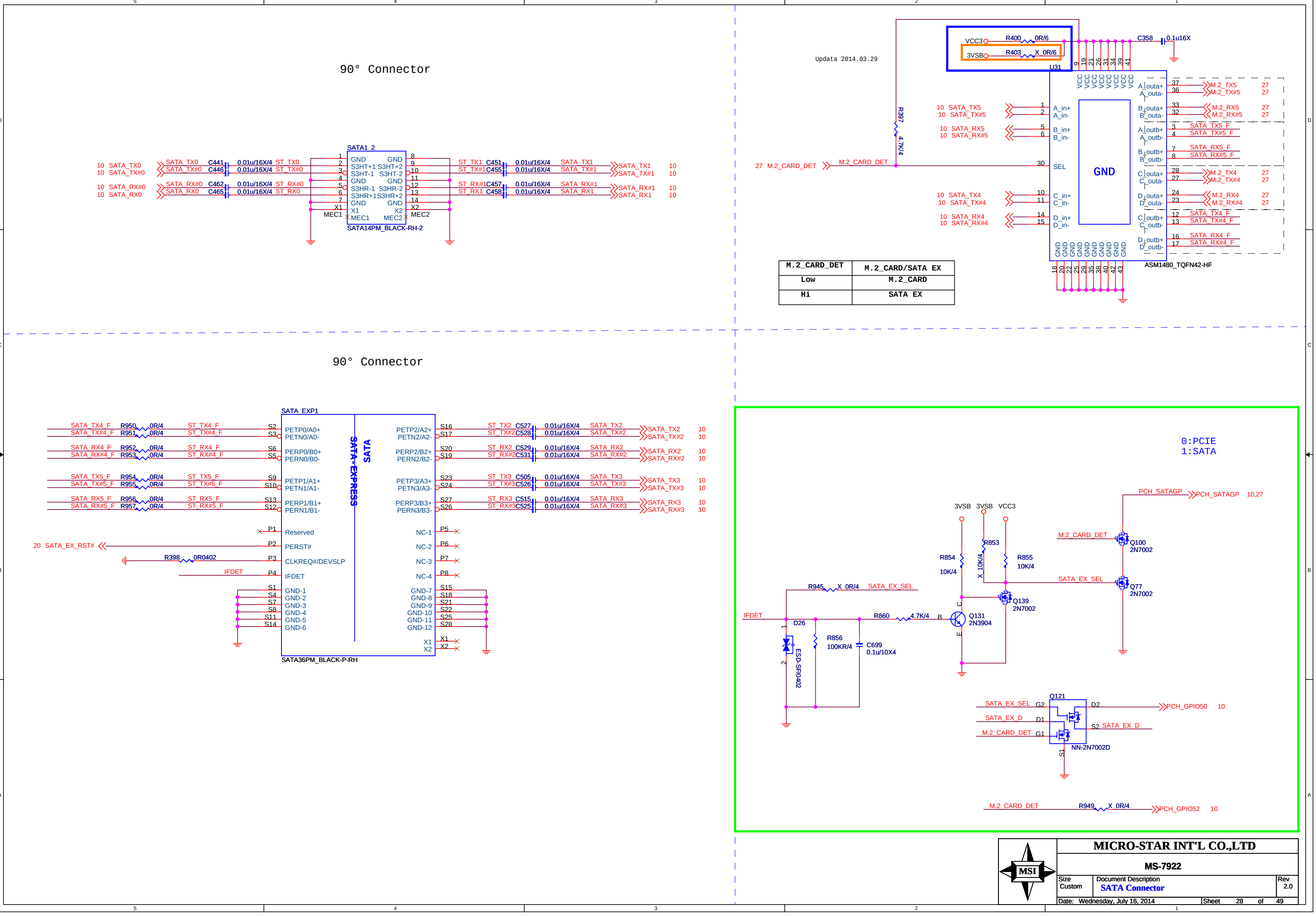
SATA4GP/SATA5GP
for chipset that main power,if pull up to VSB maybe will leakage power
If sampled value = 1, select SATA; if sampled value = 0, select PCIe

MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	MSATA	2.0

Date: Wednesday, July 16, 2014 Sheet 27 of 49



M.2_CARD_DET	M.2_CARD/SATA EX
Low	M.2_CARD
Hi	SATA EX

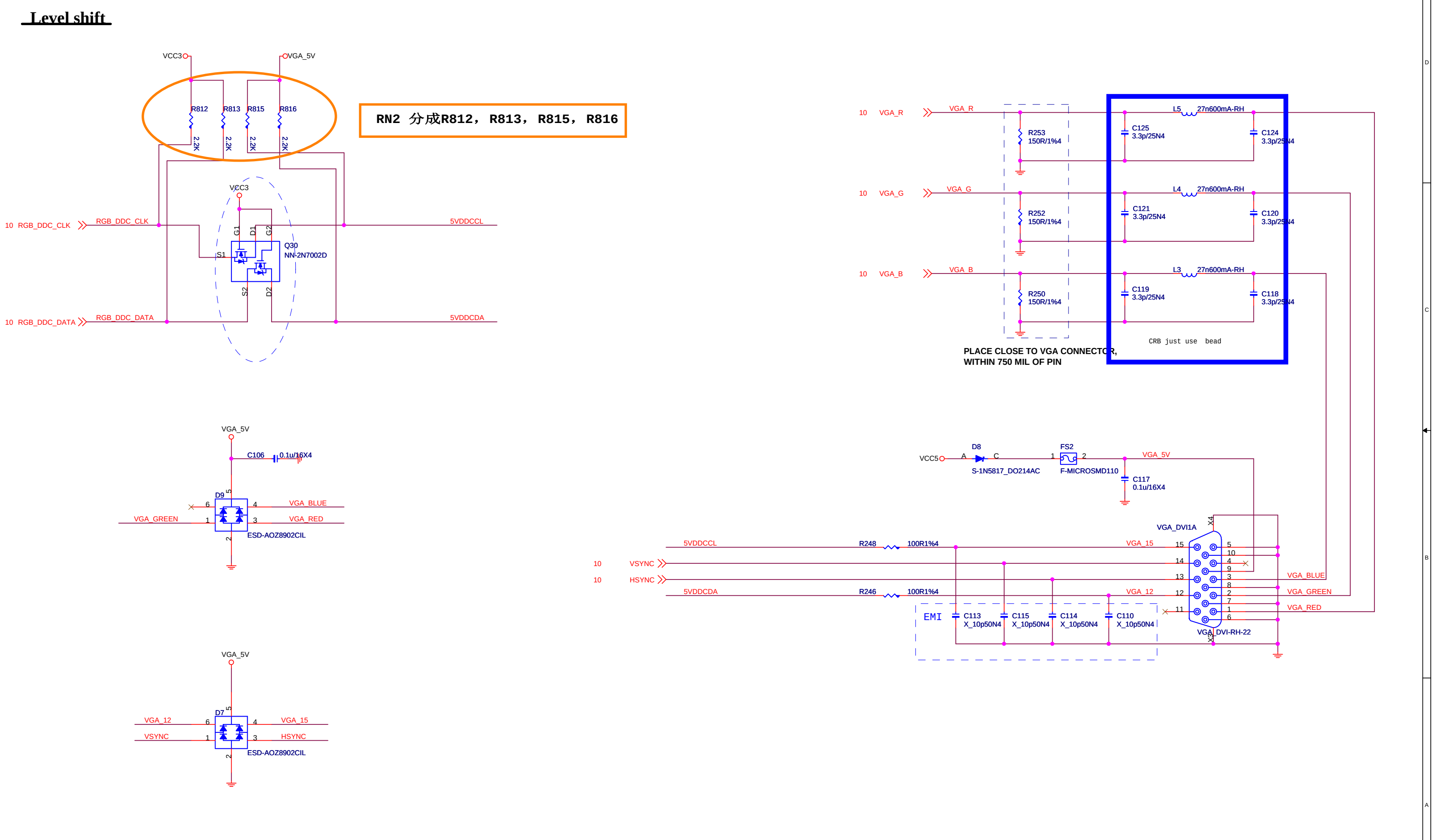
MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	SATA Connector	2.0

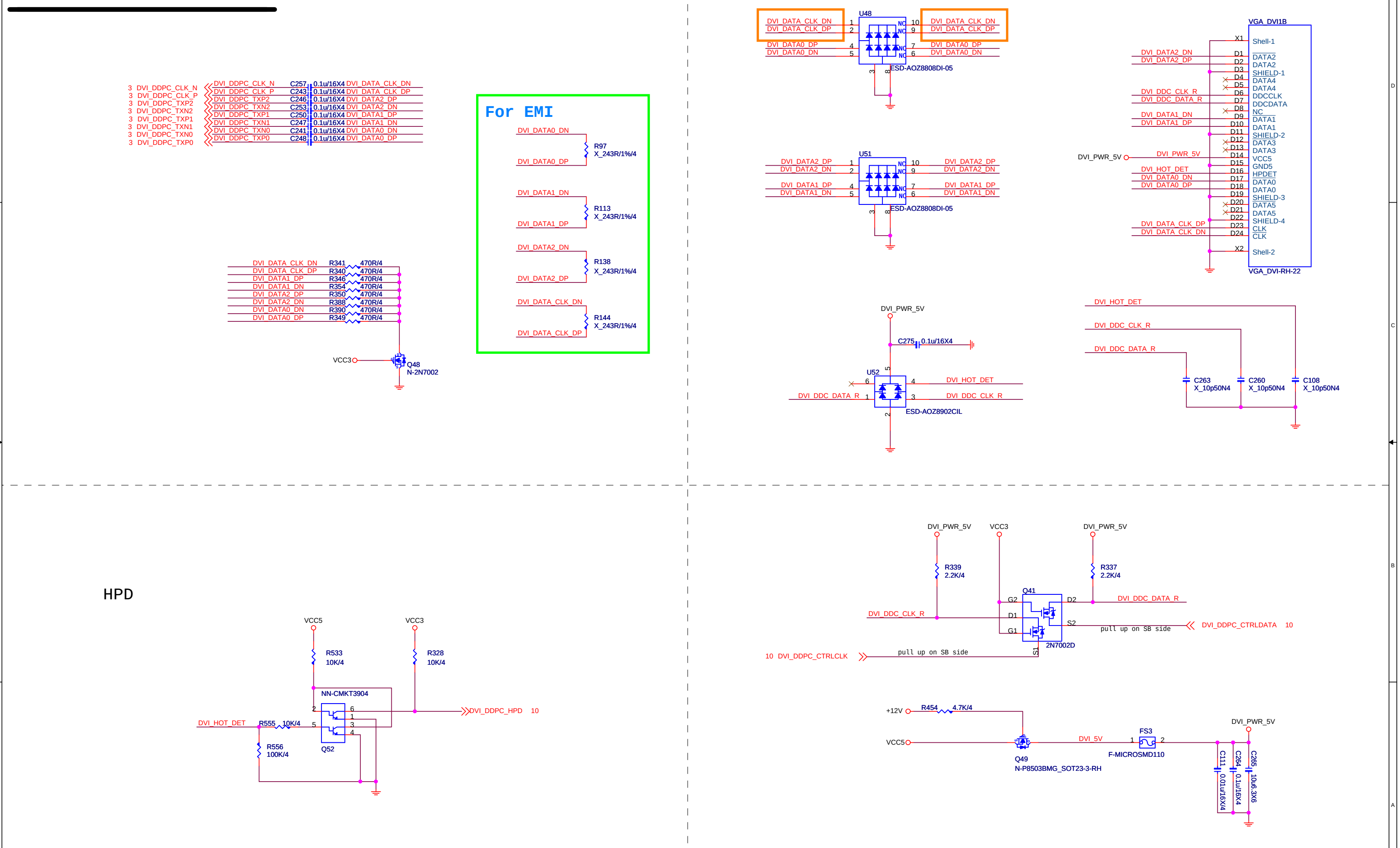
Date: Wednesday, July 16, 2014 Sheet 28 of 49

D-Sub

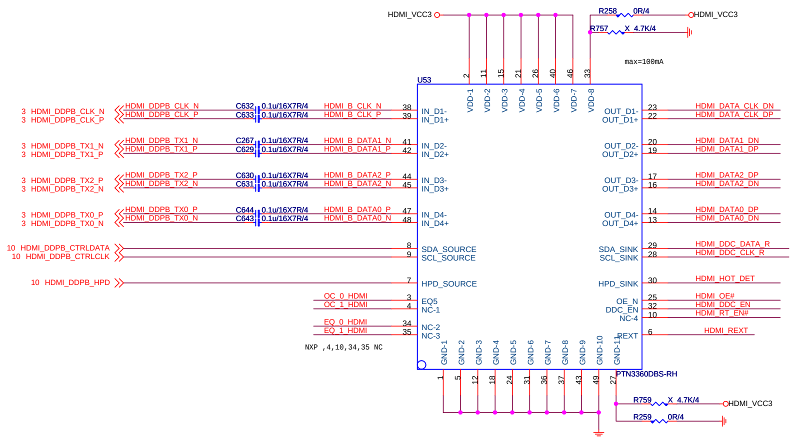


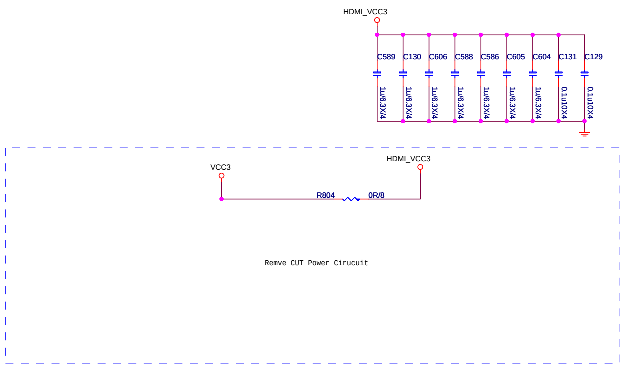
MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: VGA Connector	Rev 2.0
Date: Wednesday, July 16, 2014	Sheet 29 of 49	

DVI level shifter



MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: DVI transfer	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 30 of 49	

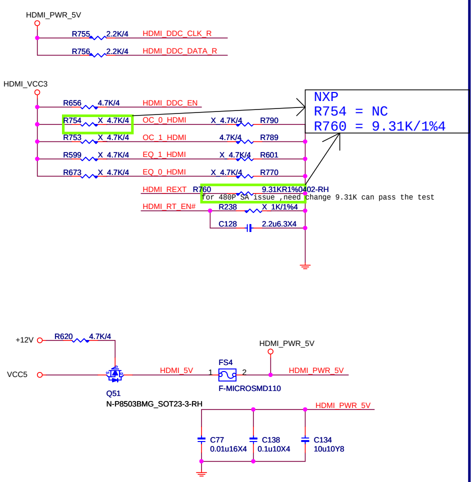




	"0"	"1"	note
HDMI_DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

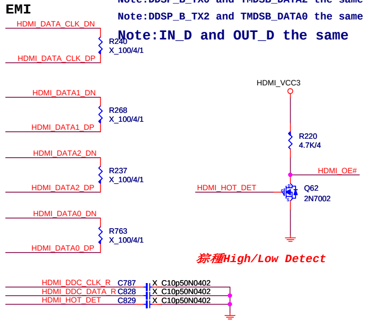


EMI

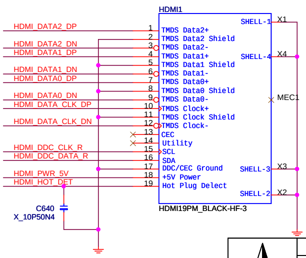
Note:DDSP_B_TX0 and TMDSB_DATA2 the same

Note:DDSP_B_TX2 and TMDSB_DATA0 the same

Note:IN_D and OUT_D the same



Note:Reserve RN4;RN5 for EMI



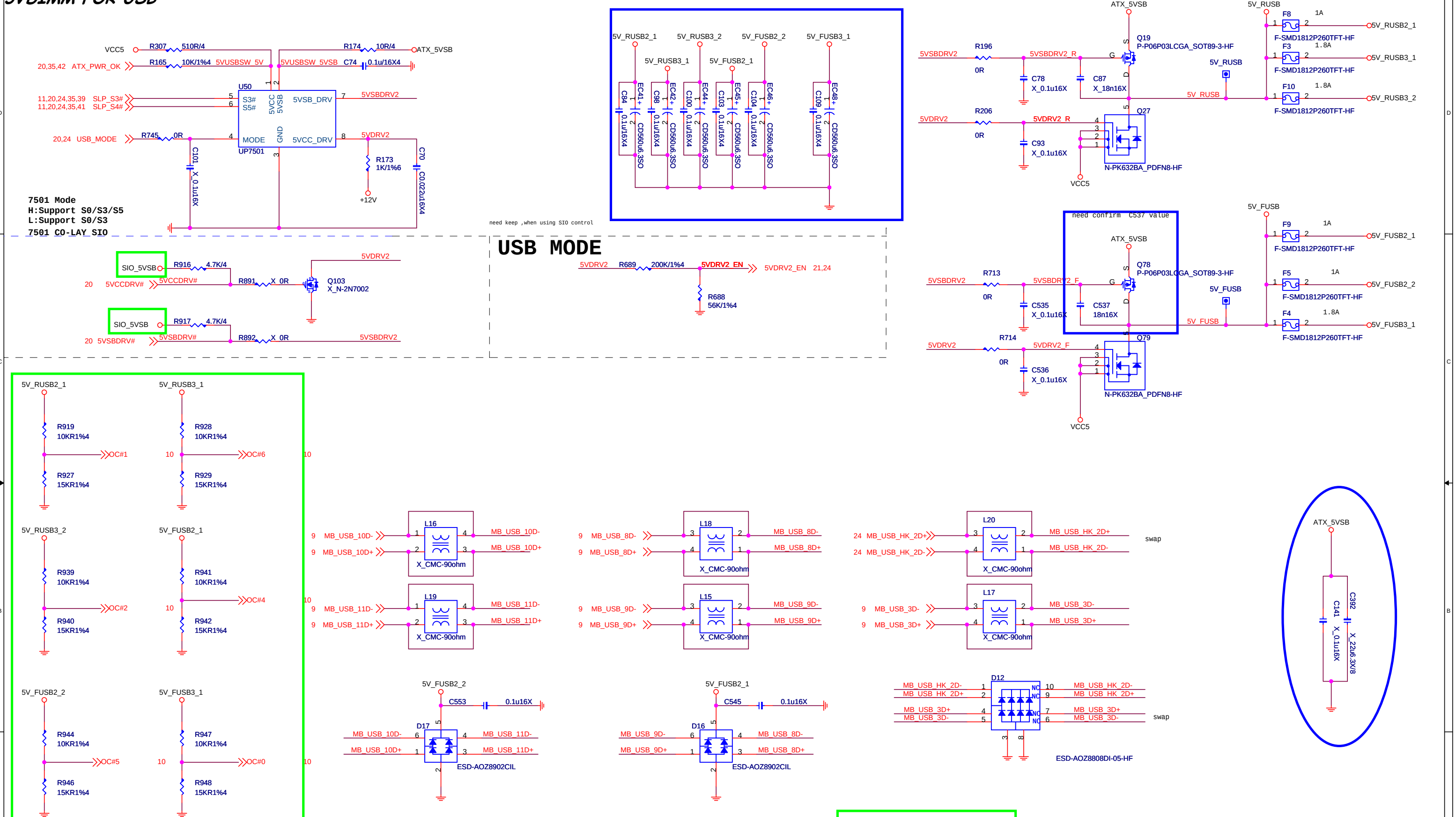
MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	HDMI Connector	2.0

Date: Wednesday, July 16, 2014 Sheet 31 of 49

5VDIMM FOR USB



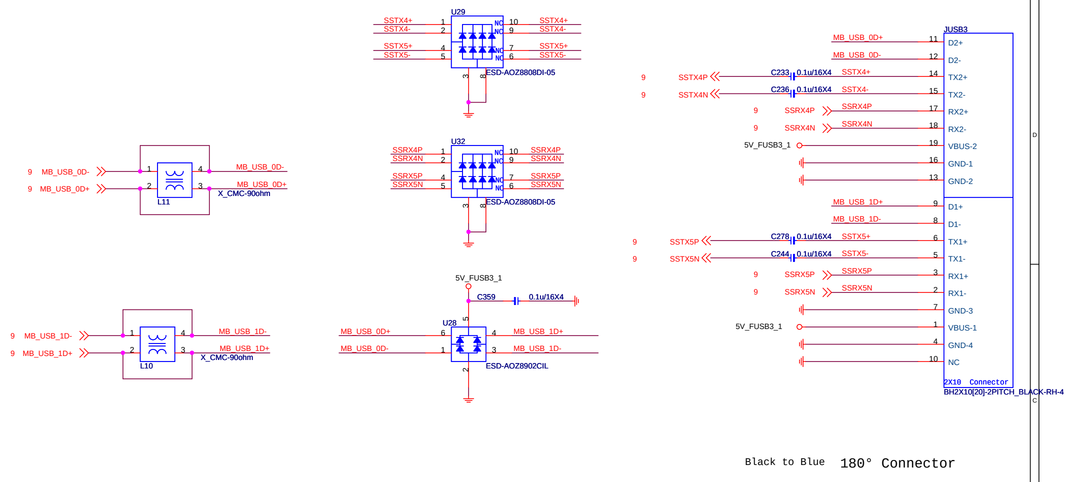
USB Location	USB Power	USB Port	OC PIN
PS2_USB1	5V_RUSB2_1	2/3	OC#1
USB2	5V_RUSB3_1	13/12	OC#6
LAN_USB	5V_RUSB3_2	0/1	OC#2
JUSB3	5V_FUSB3_1	4/5	OC#0
JUSB2	5V_FUSB2_2	10/11	OC#5
JUSB1	5V_FUSB2_1	8/9	OC#4

MICRO-STAR INT'L CO.,LTD

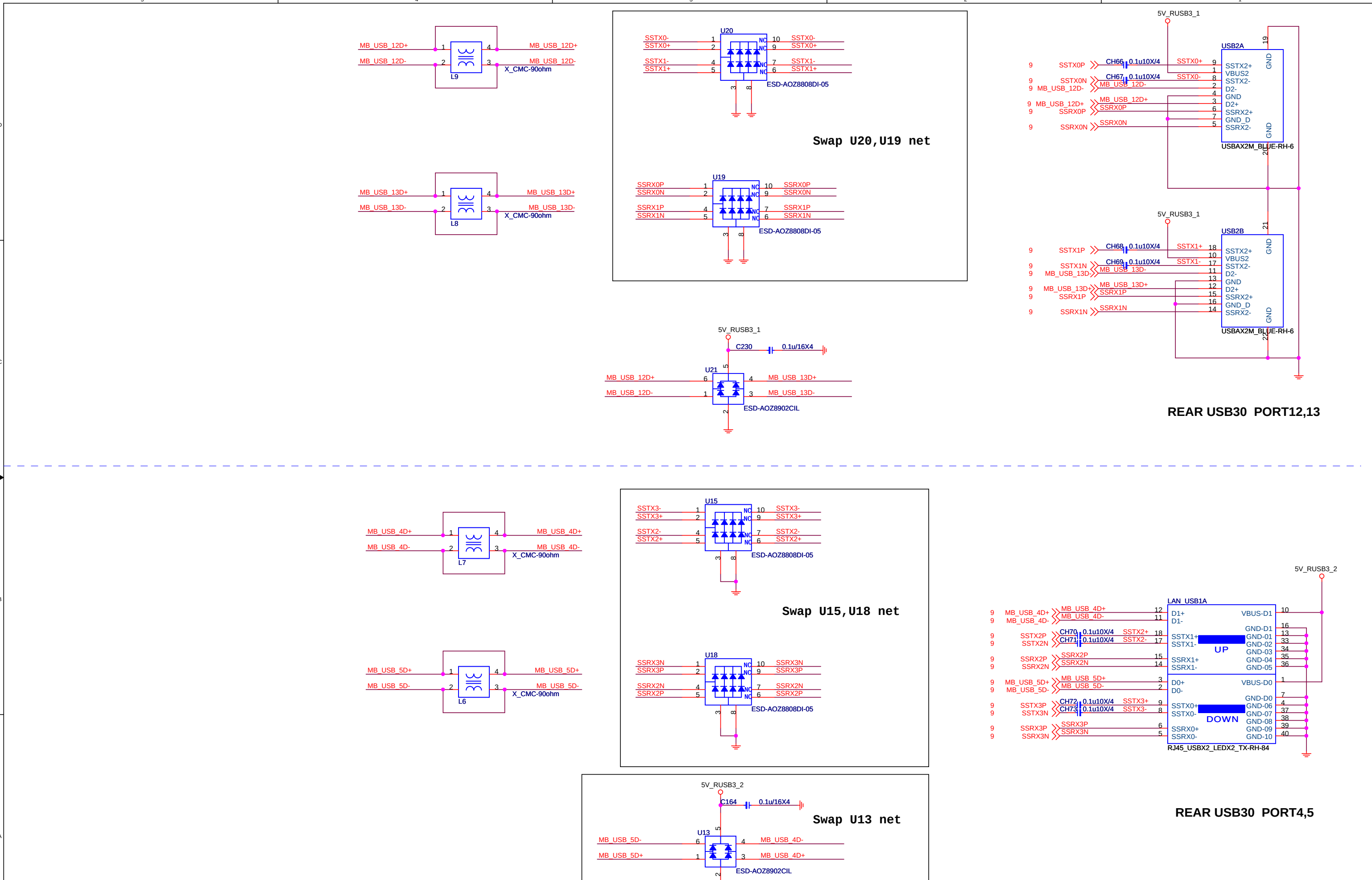
MS-7922

Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	2.0

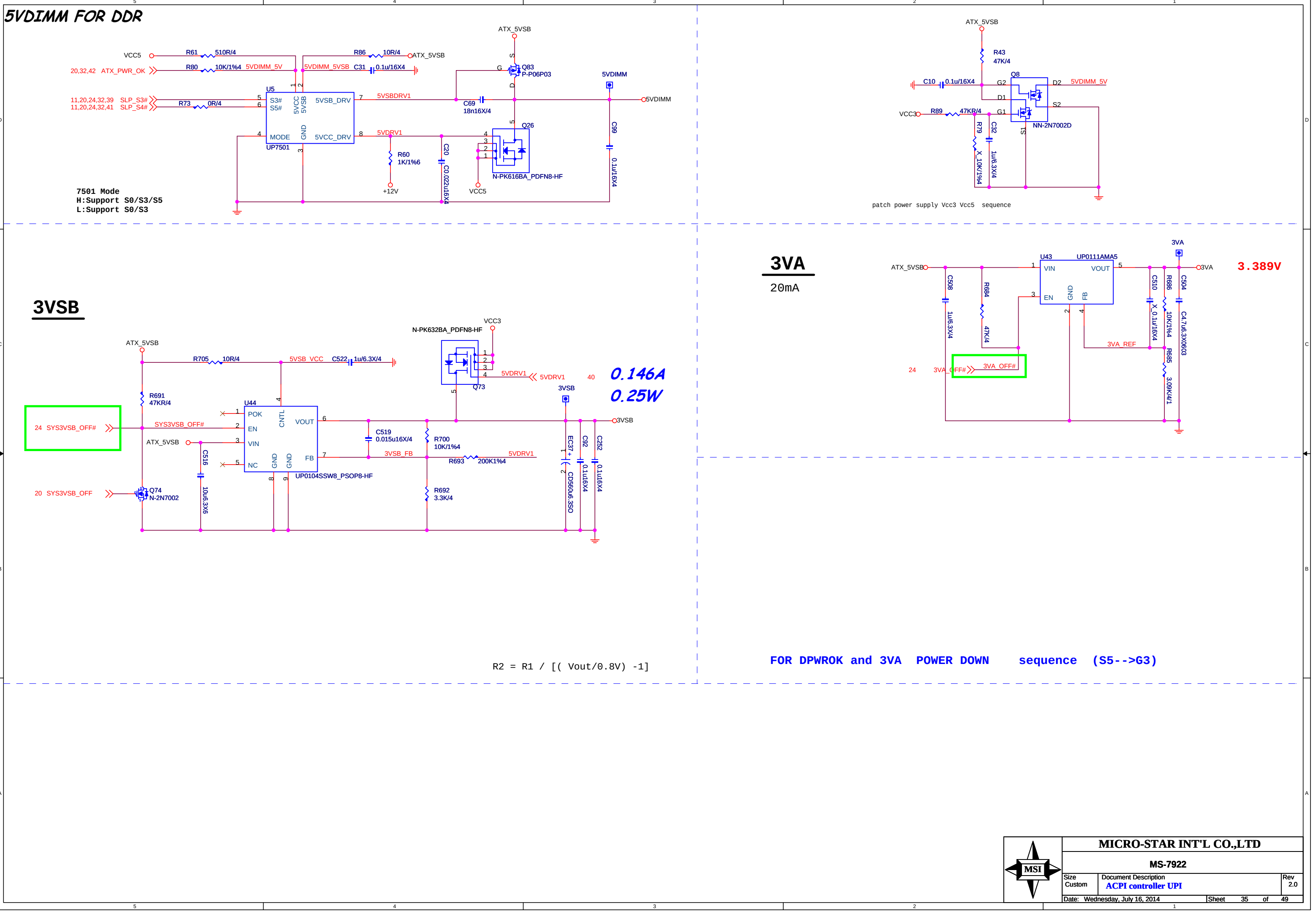
Date: Wednesday, July 16, 2014 Sheet 32 of 49



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7922	
Size: Custom	Document Description: FRONT USB3.0 -IUSB4/JUSB5	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 33 of 49	



MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: REAR USB3.0 -USB2/LANUSB	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 34 of 49	

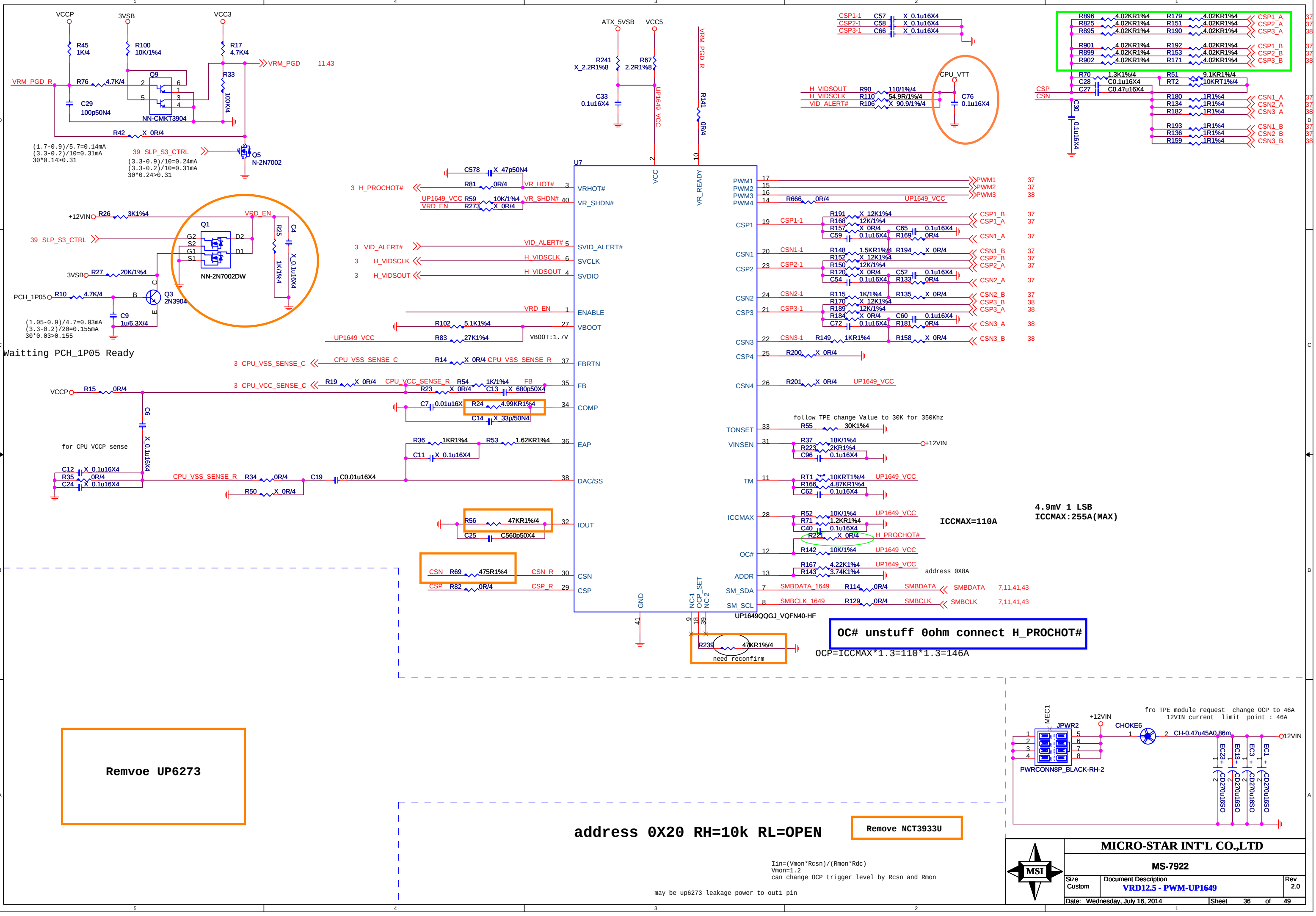


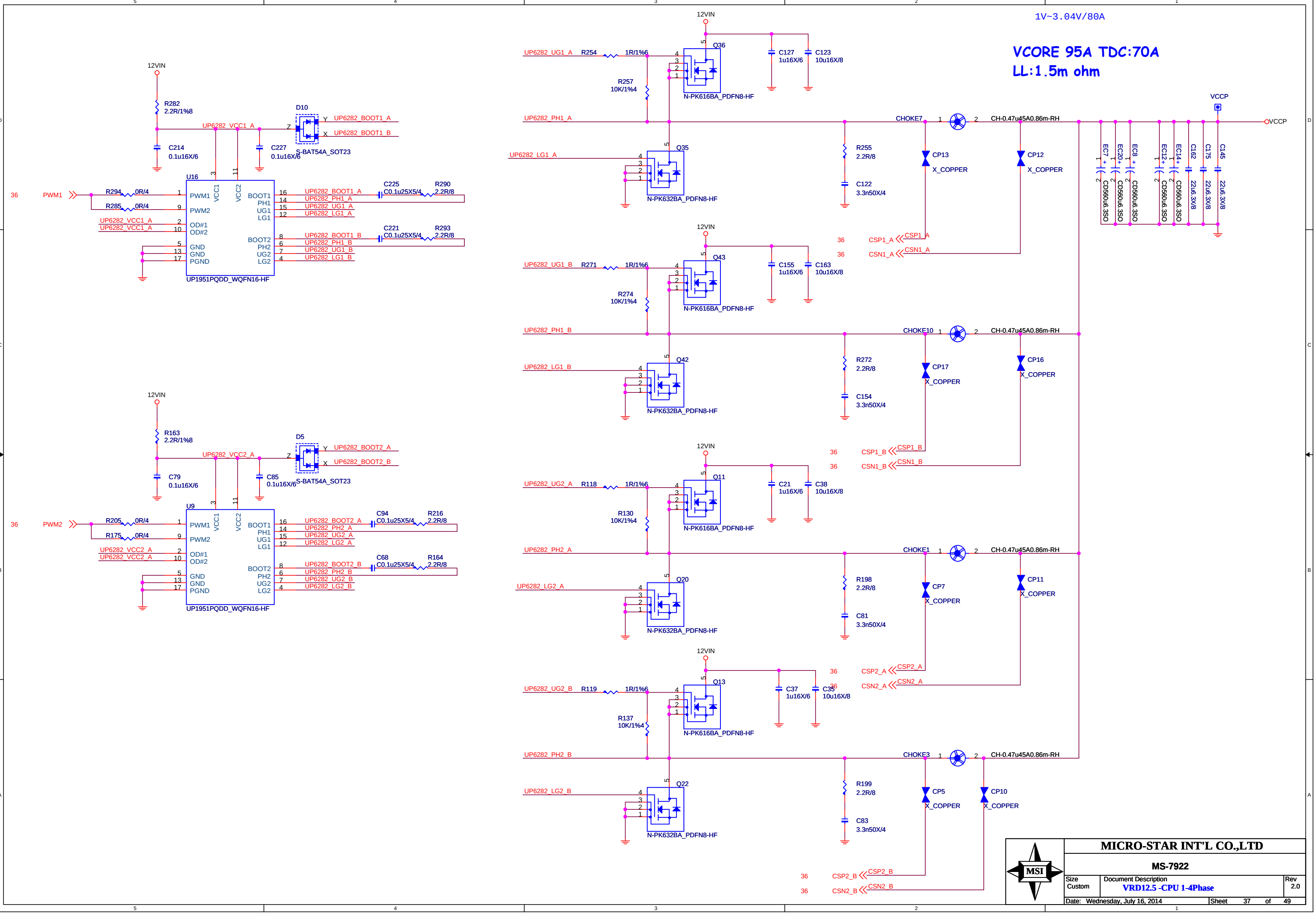
MICRO-STAR INT'L CO.,LTD

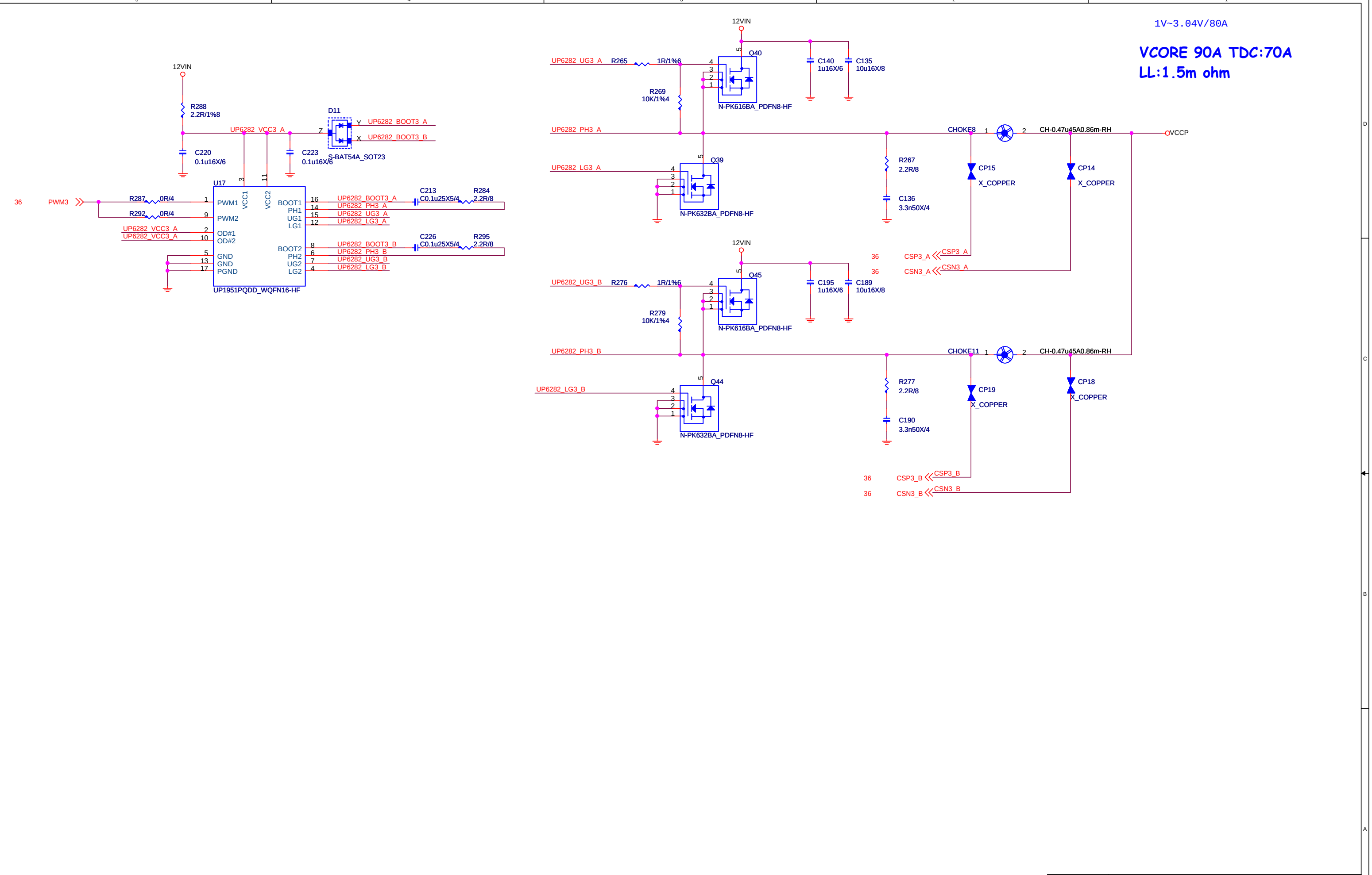
MS-7922

Size	Document Description	Rev
Custom	ACPI controller UPI	2.0

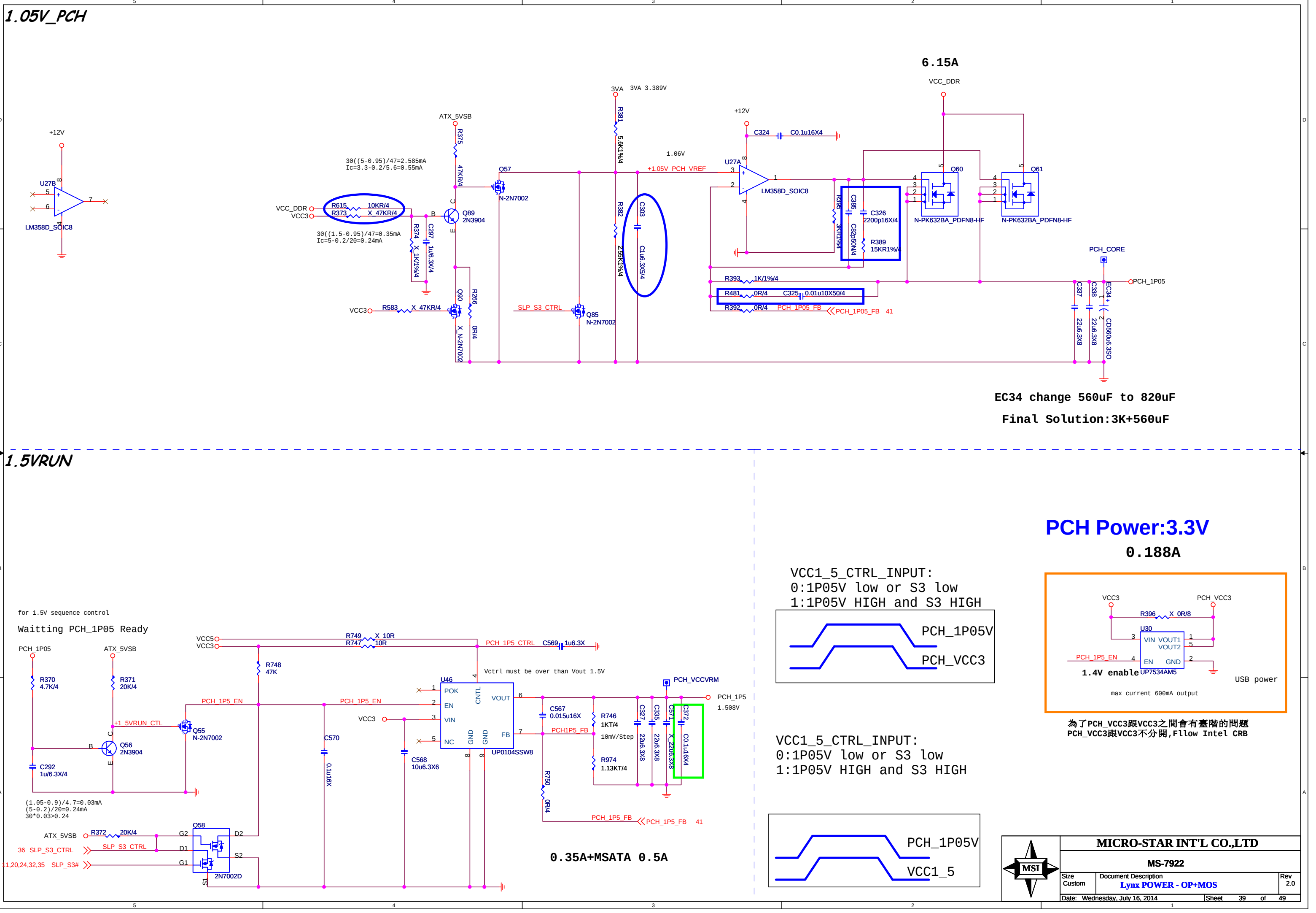
Date: Wednesday, July 16, 2014 | Sheet 35 of 49

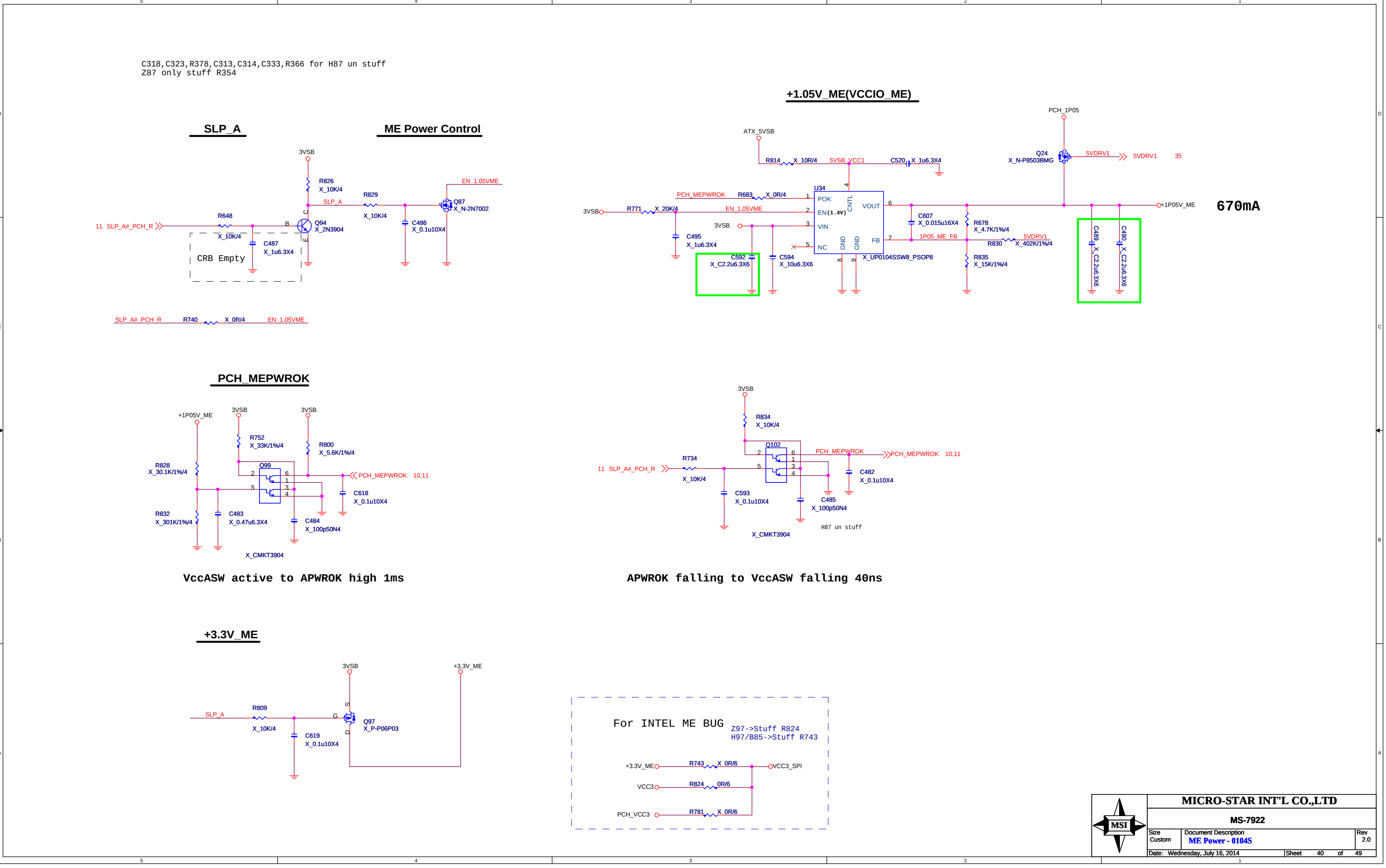

Waitting PCH_1P05 Ready
(1.7-0.9)/5.7=0.14mA
(3.3-0.2)/10=0.31mA
30*0.14>0.31
(3.3-0.9)/10=0.24mA
(3.3-0.2)/10=0.31mA
30*0.24>0.31
(1.05-0.9)/4.7=0.03mA
(3.3-0.2)/20=0.155mA
30*0.03>0.155
for CPU VCCP sense
VBOOT:1.7V
follow TPE change Value to 30K for 350Khz
4.9mV 1 LSB
ICCMAX:255A(MAX)
ICCMAX=110A
address 0X8A
need reconfirm
OC# unstuff 0ohm connect H_PROCHOT#
OCP=ICCMAX*1.3=110*1.3=146A
U7
UP1649QQGJ_VQFN40-HF
fro TPE module request change OCP to 46A
12VIN current limit point : 46A
PWRCONN8P_BLACK-RH-2
Remvoe UP6273
address 0X20 RH=10k RL=OPEN
Remove NCT3933U
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon
may be up6273 leakage power to out1 pin
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
VRD12.5 - PWM-UP1649
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 36 of 49


1V~3.04V/80A
VCORE 95A TDC:70A
LL:1.5m ohm
12VIN
R282
2.2R/1%8
D10
UP6282_VCC1_A
UP6282_BOOT1_A
UP6282_BOOT1_B
C214
0.1u16X/6
C227
0.1u16X/6
S-BAT54A_SOT23
U16
PWM1
R294
0R/4
R285
0R/4
PWM2
OD#1
OD#2
GND
PGND
VCC1
VCC2
BOOT1
PH1
UG1
LG1
BOOT2
PH2
UG2
LG2
UP1951PQDD_WQFN16-HF
UP6282_PH1_A
UP6282_UG1_A
UP6282_LG1_A
UP6282_PH1_B
UP6282_UG1_B
UP6282_LG1_B
C225
C0.1u25X5/4
R290
2.2R/8
C221
C0.1u25X5/4
R293
2.2R/8
R163
2.2R/1%8
D5
UP6282_VCC2_A
UP6282_BOOT2_A
UP6282_BOOT2_B
C79
0.1u16X/6
C85
0.1u16X/6
U9
R205
0R/4
R175
0R/4
UP6282_PH2_A
UP6282_UG2_A
UP6282_LG2_A
UP6282_PH2_B
UP6282_UG2_B
UP6282_LG2_B
C94
C0.1u25X5/4
R216
2.2R/8
C68
C0.1u25X5/4
R164
2.2R/8
R254
1R/1%6
R257
10K/1%4
Q36
N-PK616BA_PDFN8-HF
C127
1u16X/6
C123
10u16X/8
Q35
N-PK632BA_PDFN8-HF
CHOKE7
CH-0.47u45A0.86m-RH
R255
2.2R/8
C122
3.3n50X/4
CP13
X_COPPER
CP12
X_COPPER
VCCP
EC7
EC20
EC8
EC12
EC14
CD560u6.3SO
C162
C175
C145
22u6.3X/8
CSP1_A
CSN1_A
R271
1R/1%6
R274
10K/1%4
Q43
C155
1u16X/6
C163
10u16X/8
CHOKE10
Q42
R272
2.2R/8
C154
3.3n50X/4
CP17
CP16
CSP1_B
CSN1_B
R118
1R/1%6
R130
10K/1%4
Q11
C21
1u16X/6
C38
10u16X/8
CHOKE1
Q20
R198
2.2R/8
C81
3.3n50X/4
CP7
CP11
CSP2_A
CSN2_A
R119
1R/1%6
R137
10K/1%4
Q13
C37
1u16X/6
C35
10u16X/8
CHOKE3
Q22
R199
2.2R/8
C83
3.3n50X/4
CP5
CP10
CSP2_B
CSN2_B
MICRO-STAR INT'L CO.,LTD
MS-7922
Size
Custom
Document Description
VRD12.5 -CPU 1-4Phase
Rev
2.0
Date: Wednesday, July 16, 2014
Sheet 37 of 49



MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: VRD12.5 -CPU 5-6Phase	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 38 of 49	


1.05V_PCH
6.15A
VCC_DDR
3VA 3.389V
+12V
ATX_5VSB
U27B
LM358D_SOIC8
30((5-0.95)/47=2.585mA
Ic=3.3-0.2/5.6=0.55mA
VCC_DDR
VCC3
R615 10KR/4
R373 X_47KR/4
30((1.5-0.95)/47=0.35mA
Ic=5-0.2/20=0.24mA
R375 47KR/4
Q89 2N3904
R374 X_1K/1%/4
C297 1u6.3X/4
Q57 N-2N7002
R583 X_47KR/4
Q90 X_N-2N7002
R266 0R/4
SLP_S3_CTRL
Q85 N-2N7002
R381 5.6K1%/4
R382 2.55K1%/4
C303 C1u6.3X5/4
1.06V
+1.05V_PCH_VREF
U27A
LM358D_SOIC8
C324 C0.1u16X4
R390 3KR1%/4
C385 C82p50N/4
C326 2200p16X/4
R389 15KR1%/4
Q60 N-PK632BA_PDFN8-HF
Q61 N-PK632BA_PDFN8-HF
PCH_CORE
PCH_1P05
R393 1K/1%/4
R481 0R/4
C325 0.01u10X50/4
R392 0R/4
PCH_1P05_FB
C337 22u6.3X8
C338 22u6.3X8
EC34 CD560u6.3SO
EC34 change 560uF to 820uF
Final Solution:3K+560uF
1.5VRUN
PCH Power:3.3V
0.188A
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
PCH_1P05V
PCH_VCC3
VCC3
PCH_VCC3
R396 X_0R/8
U30
VIN VOUT1
VOUT2
EN GND
PCH_1P5_EN
1.4V enable
UP7534AM5
USB power
max current 600mA output
為了PCH_VCC3跟VCC3之間會有臺階的問題
PCH_VCC3跟VCC3不分開,Fllow Intel CRB
for 1.5V sequence control
Waitting PCH_1P05 Ready
PCH_1P05
ATX_5VSB
R370 4.7K/4
R371 20K/4
Q56 2N3904
C292 1u/6.3X/4
+1_5VRUN_CTL
Q55 N-2N7002
(1.05-0.9)/4.7=0.03mA
(5-0.2)/20=0.24mA
30*0.03>0.24
VCC5
VCC3
R749 X_10R
R747 10R
PCH_1P5_CTRL
C569 1u6.3X
R748 47K
PCH_1P5_EN
Vctrl must be over than Vout 1.5V
U46
POK
EN
VIN
NC
CNTL
VOUT
FB
GND
UP0104SSW8
C570 0.1u16X
C568 10u6.3X6
C567 0.015u16X
R746 1KT/4
10mV/Step
R974 1.13KT/4
PCH1P5_FB
R750 0R/4
PCH_1P5_FB
PCH_VCCVRM
PCH_1P5
1.508V
C327 22u6.3X8
C335 22u6.3X8
C571 X_22u6.3X8
C372 C0.1u16X4
Q58
2N7002D
ATX_5VSB
R372 20K/4
SLP_S3_CTRL
SLP_S3#
0.35A+MSATA 0.5A
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
PCH_1P05V
VCC1_5
MICRO-STAR INT'L CO.,LTD
MS-7922
Size Custom
Document Description
Lynx POWER - OP+MOS
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 39 of 49


C318,C323,R378,C313,C314,C333,R366 for H87 un stuff
Z87 only stuff R354
SLP_A
ME Power Control
+1.05V_ME(VCCIO_ME)
3VSB
R826
X_10K/4
SLP_A
R829
X_10K/4
EN_1.05VME
Q87
X_N-2N7002
C486
X_0.1u10X4
R648
X_10K/4
11 SLP_A#_PCH_R
Q94
X_2N3904
C487
X_1u6.3X4
CRB Empty
SLP_A#_PCH_R
R740
X_0R/4
EN_1.05VME
ATX_5VSB
R814
X_10R/4
5VSB_VCC1
C520
X_1u6.3X4
PCH_1P05
Q24
X_N-P8503BMG
5VDRV1
5VDRV1 35
PCH_MEPWROK
R683
X_0R/4
U34
POK
EN (1.4V)
VIN
NC
CNTL
VOUT
FB
GND
GND
3VSB
R771
X_20K/4
EN_1.05VME
C495
X_1u6.3X4
3VSB
C592
X_C2.2u6.3X6
C594
X_10u6.3X6
X_UP0104SSW8_PSOP8
C607
X_0.015u16X4
1P05_ME_FB
R678
X_4.7K/1%/4
R830
X_402K/1%/4
5VDRV1
R835
X_15K/1%/4
+1P05V_ME
670mA
C489
X_C2.2u6.3X6
C490
X_C2.2u6.3X6
PCH_MEPWROK
+1P05V_ME
3VSB
3VSB
R752
X_33K/1%/4
R800
X_5.6K/1%/4
Q99
PCH_MEPWROK 10,11
R828
X_30.1K/1%/4
C618
X_0.1u10X4
R832
X_301K/1%/4
C483
X_0.47u6.3X4
C484
X_100p50N4
X_CMKT3904
VccASW active to APWROK high 1ms
3VSB
R834
X_10K/4
Q102
PCH_MEPWROK
PCH_MEPWROK 10,11
R734
11 SLP_A#_PCH_R
X_10K/4
C482
X_0.1u10X4
C593
X_0.1u10X4
C485
X_100p50N4
H87 un stuff
X_CMKT3904
APWROK falling to VccASW falling 40ns
+3.3V_ME
3VSB
+3.3V_ME
SLP_A
R809
X_10K/4
Q97
X_P-P06P03
C619
X_0.1u10X4
For INTEL ME BUG
Z97->Stuff R824
H97/B85->Stuff R743
+3.3V_ME
R743
X_0R/6
VCC3_SPI
VCC3
R824
0R/6
PCH_VCC3
R781
X_0R/6
MSI
MICRO-STAR INT'L CO.,LTD
MS-7922
Size
Custom
Document Description
ME Power - 0104S
Rev
2.0
Date: Wednesday, July 16, 2014
Sheet 40 of 49

DDR Power:1.5V

DDR3_1.5V 4.2A+12A+1.1A+5A=22.3A

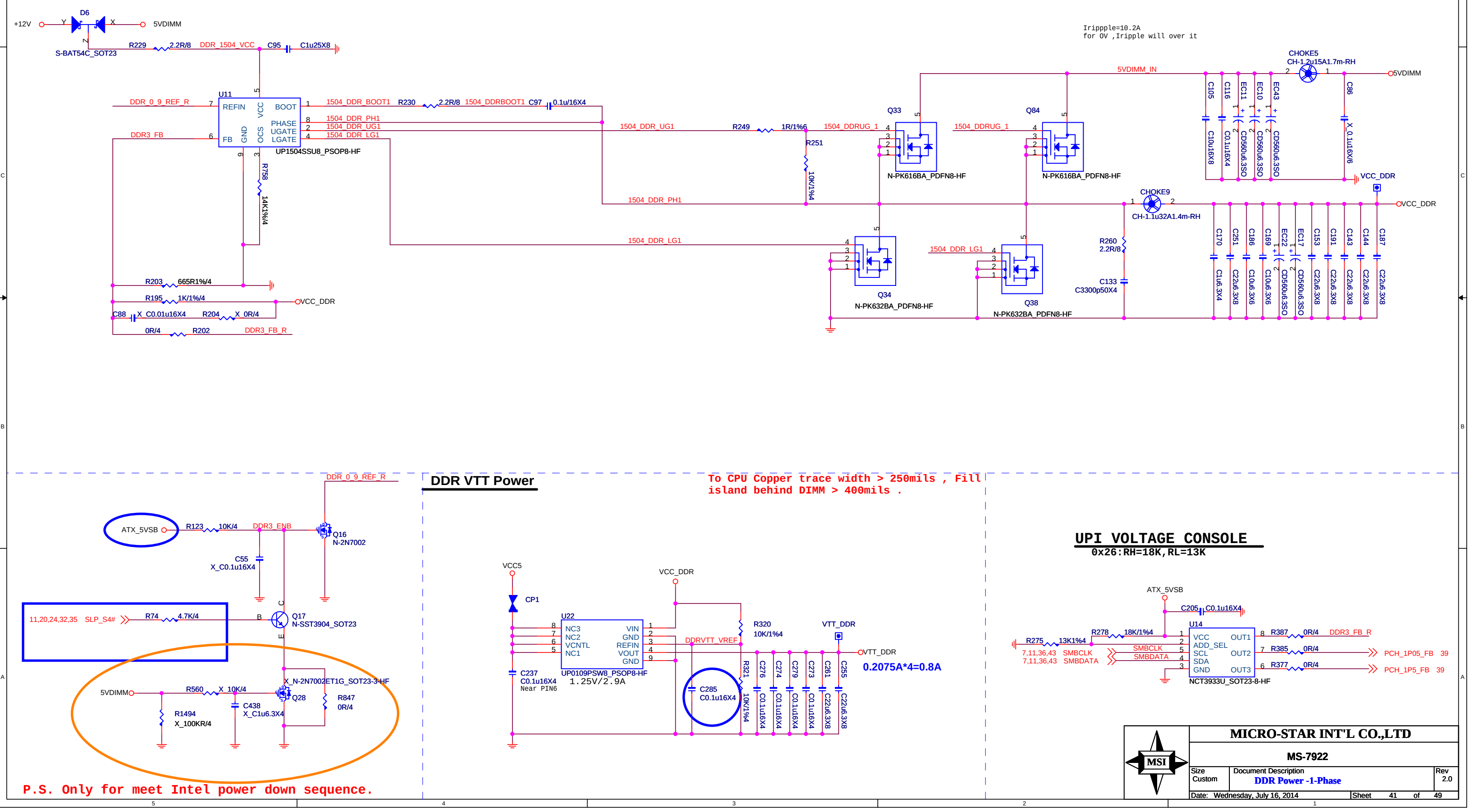
4.2A FOR CPU

12A FOR 4DIMM

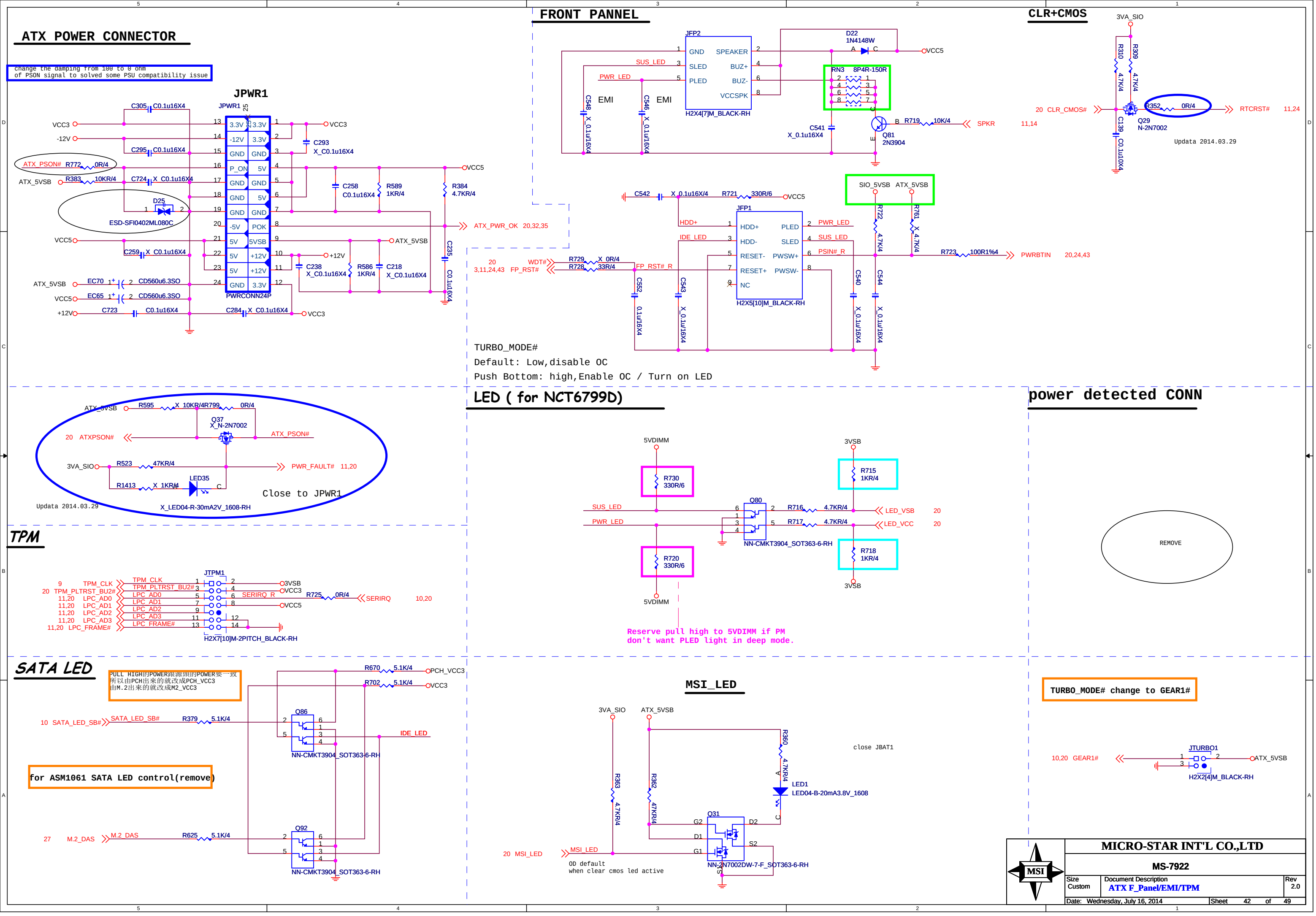
1.1A FOR DDR VTT

5A FOR PCH

*OCP ((5*10v6*R758/(3.4/2)m ohm=36.47A>22.3*1.5A*

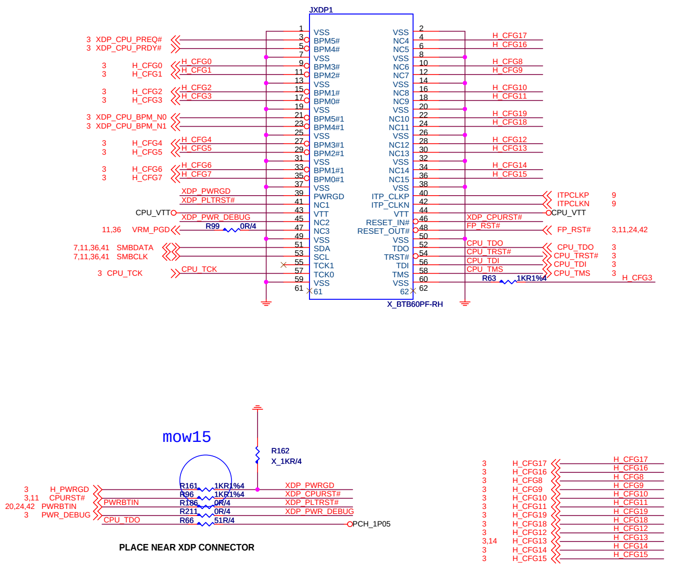


MICRO-STAR INT'L CO.,LTD			
MS-7922			
Size: Custom	Document Description: DDR Power -1-Phase		Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 41	of 49	



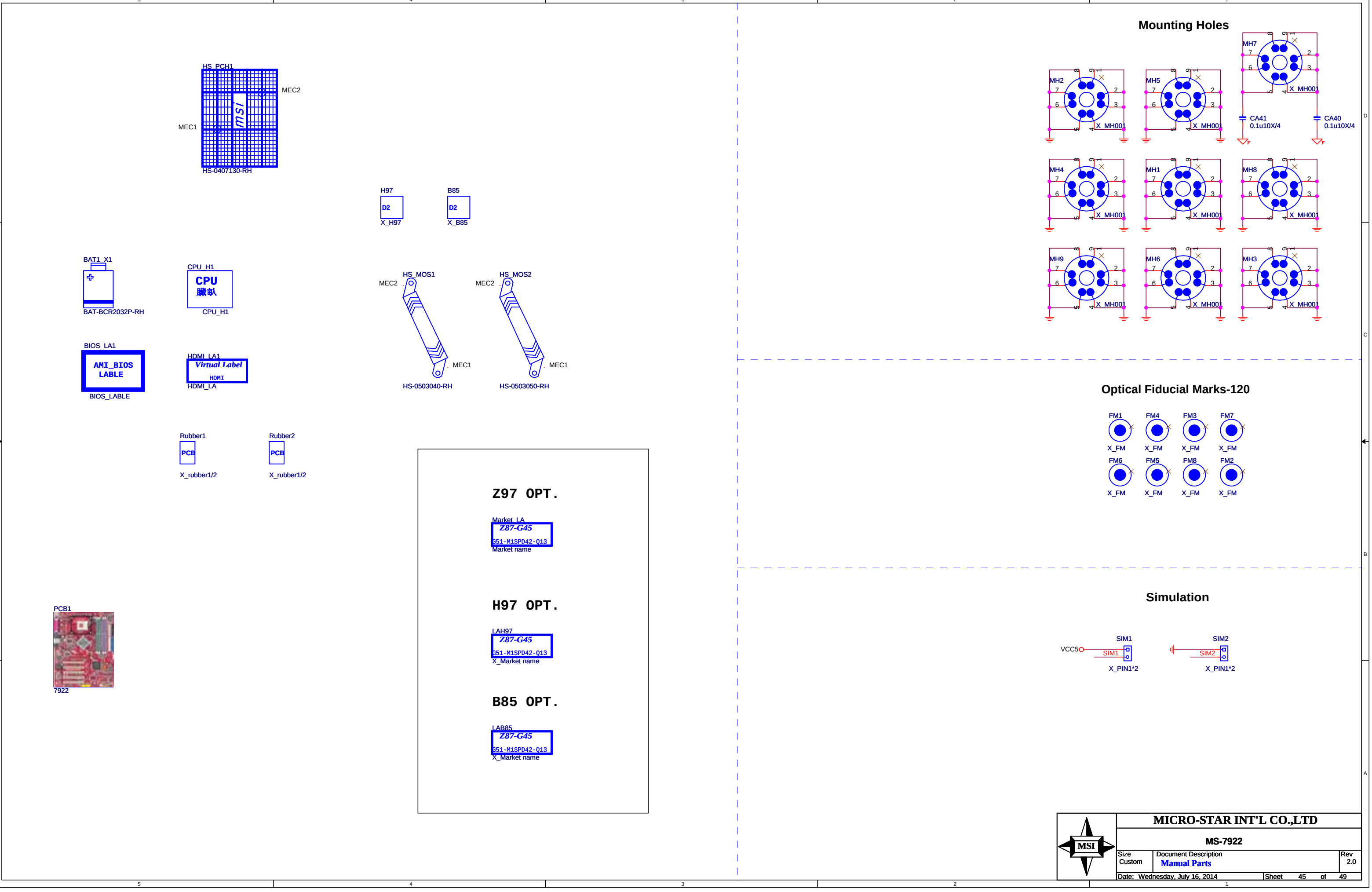
ATX POWER CONNECTOR
change the damping from 100 to 0 ohm
of PSON signal to solved some PSU compatibility issue
JPWR1
PWRCONN24P
ESD-SFI0402ML080C
ATX_PWR_OK 20,32,35
FRONT PANNEL
JFP2
H2X4[7]M_BLACK-RH
D22 1N4148W
RN3 8P4R-150R
Q81 2N3904
SPKR 11,14
EMI
JFP1
H2X5[10]M_BLACK-RH
PWRBTIN 20,24,43
TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED
CLR+CMOS
CLR_CMOS#
RTCRST# 11,24
Q29 N-2N7002
Updata 2014.03.29
Q37 X_N-2N7002
ATX_PSON#
PWR_FAULT# 11,20
LED35
X_LED04-R-30mA2V_1608-RH
Close to JPWR1
Updata 2014.03.29
TPM
JTPM1
H2X7[10]M-2PITCH_BLACK-RH
SERIRQ 10,20
LED (for NCT6799D)
Q80
NN-CMKT3904_SOT363-6-RH
LED_VSB 20
LED_VCC 20
Reserve pull high to 5VDIMM if PM
don't want PLED light in deep mode.
power detected CONN
REMOVE
SATA LED
PULL HIGH的POWER跟测到的POWER要一致
所以由PCH出来的就改成PCH_VCC3
由M.2出来的就改成M2_VCC3
for ASM1061 SATA LED control(remove)
Q86
Q92
NN-CMKT3904_SOT363-6-RH
IDE_LED
M.2_DAS
MSI_LED
close JBAT1
LED1 LED04-B-20mA3.8V_1608
Q31 NN-2N7002DW-7-F_SOT363-6-RH
OD default
when clear cmos led active
TURBO_MODE# change to GEAR1#
JTURBO1
H2X2[4]M_BLACK-RH
MICRO-STAR INT'L CO.,LTD
MS-7922
Document Description
ATX F_Panel/EMI/TPM
Rev 2.0
Date: Wednesday, July 16, 2014
Sheet 42 of 49

Reserve debug port 5020



MICRO-STAR INT'L CO.,LTD		
MS-7922		
Size: Custom	Document Description: XDP debug port	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 43 of 49	

MICRO-STAR INT'L CO.,LTD	
MS-7922	
Size: Custom	Document Description: EMI CAP	Rev: 2.0
Date: Wednesday, July 16, 2014	Sheet 44 of 49



MICRO-STAR INT'L CO.,LTD

MS-7922

Size	Document Description	Rev
Custom	Manual Parts	2.0

Date: Wednesday, July 16, 2014 | Sheet 45 of 49