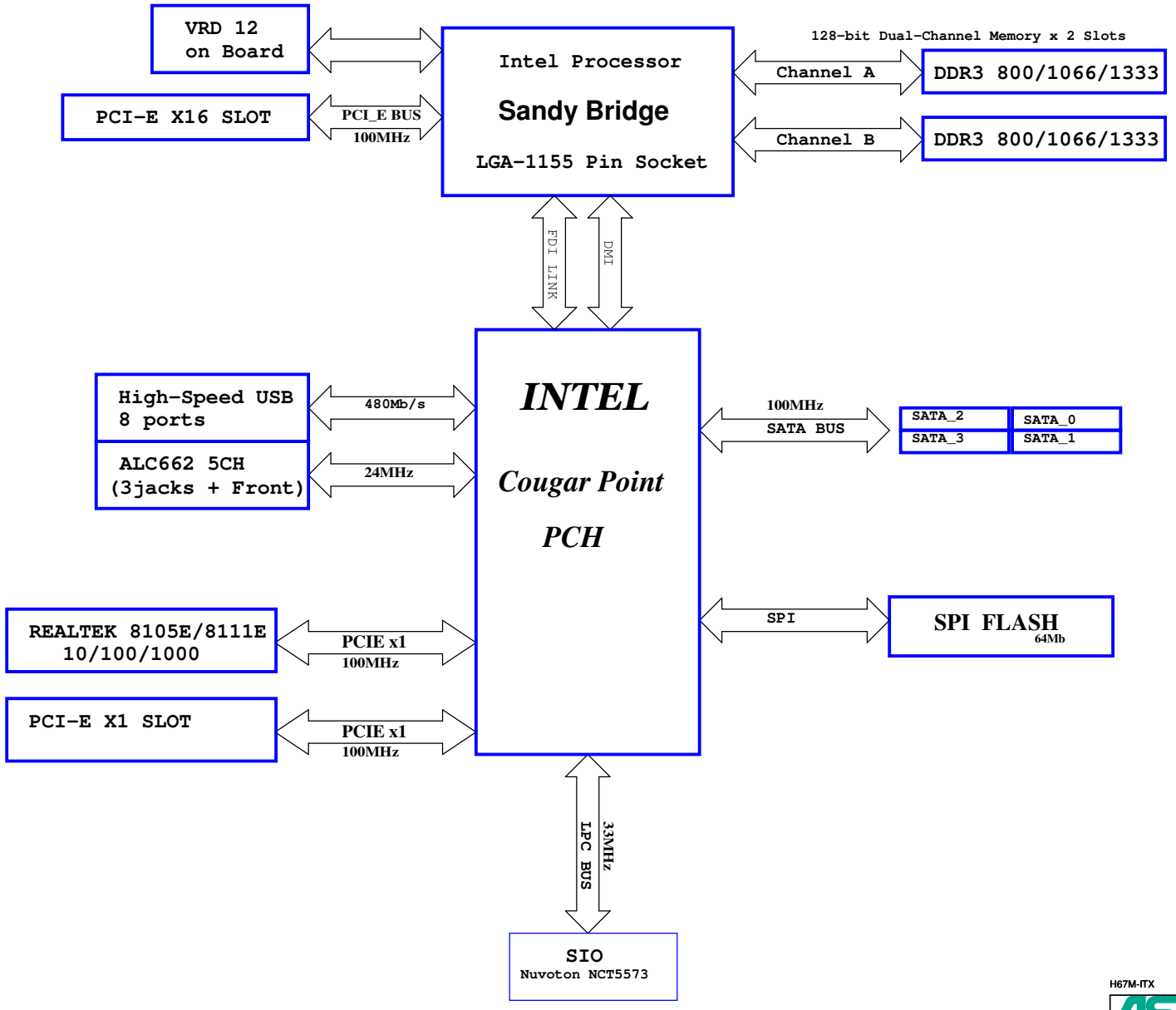
H67M-VS3 R1.02
H61M-VG3 R1.02

Draft



H67M-ITX

ASRock Inc.

Title : Block Diagram

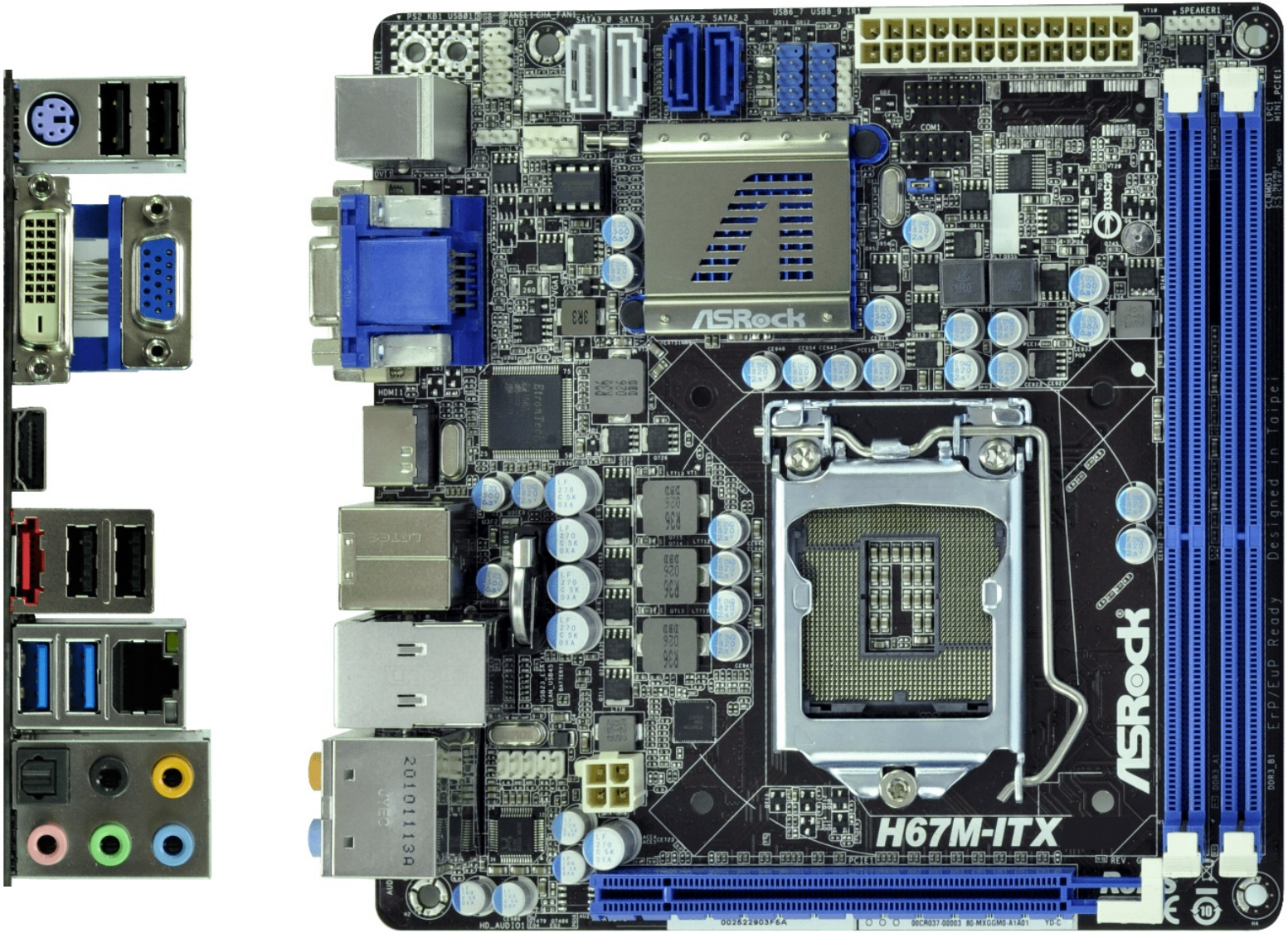
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 1 of 47

Schematics Change History

Version	Date	Comments
H61M-VS3 1.00	2012/09/14	Primary release



H67M-ITX

ASRock Inc.

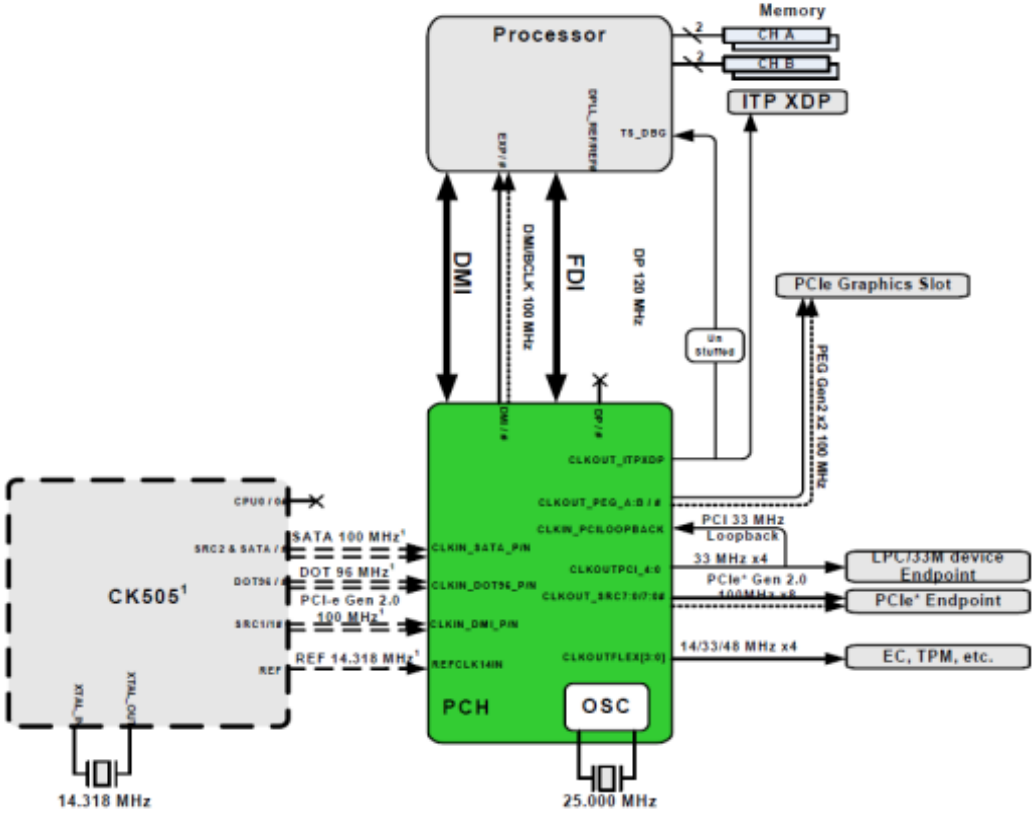
Title : Change History

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 2 of 47

Full Integrated Clock Mode



1. CK505 and PCH input clock sources indicated are Buffer Through mode back-up routes only and can be un-stuffed when in full clock integration mode

H67M-ITX

ASRock Inc.

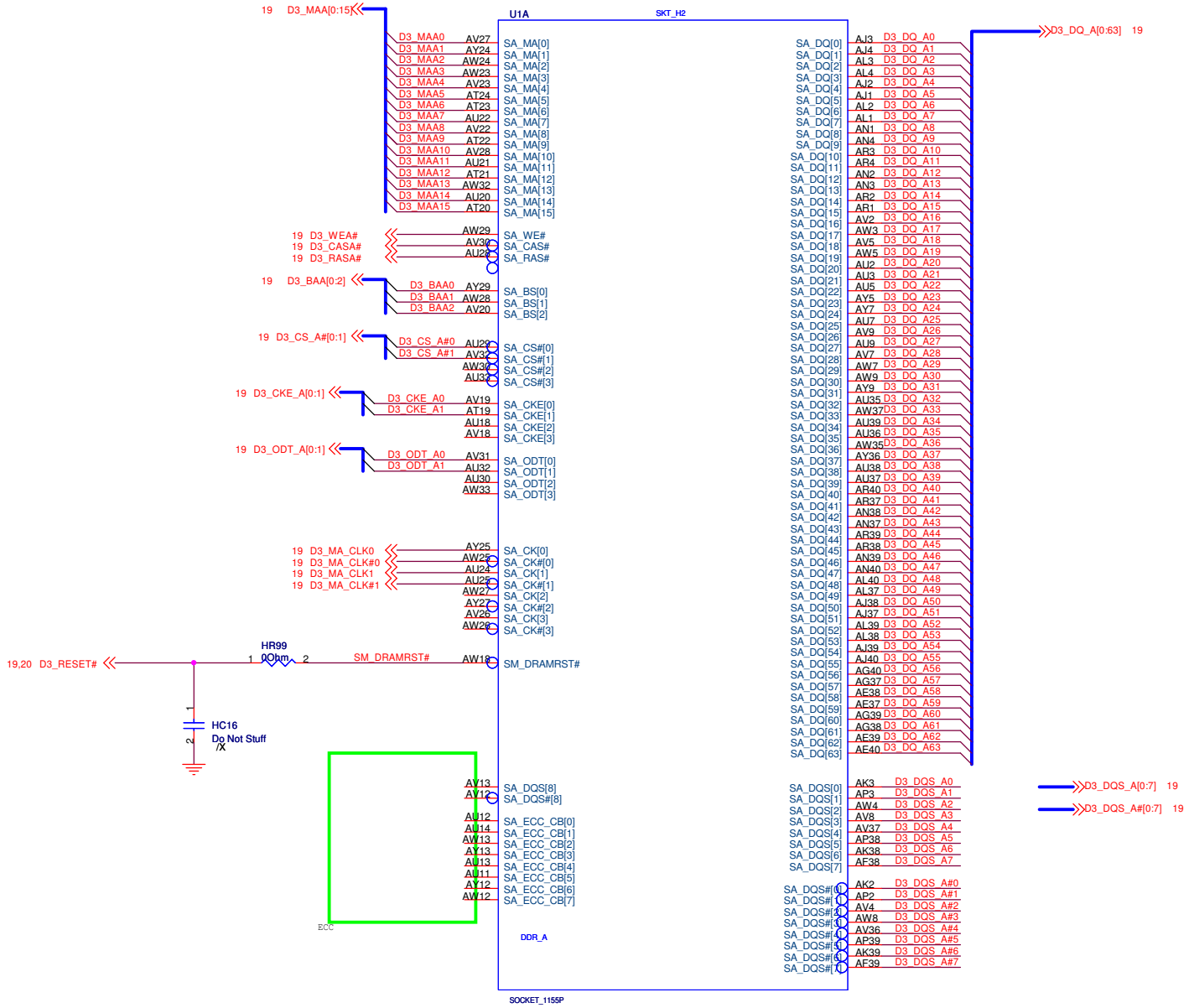
Title : Clock Distribution

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 3 of 47

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



H67M-ITX

ASRock Inc.

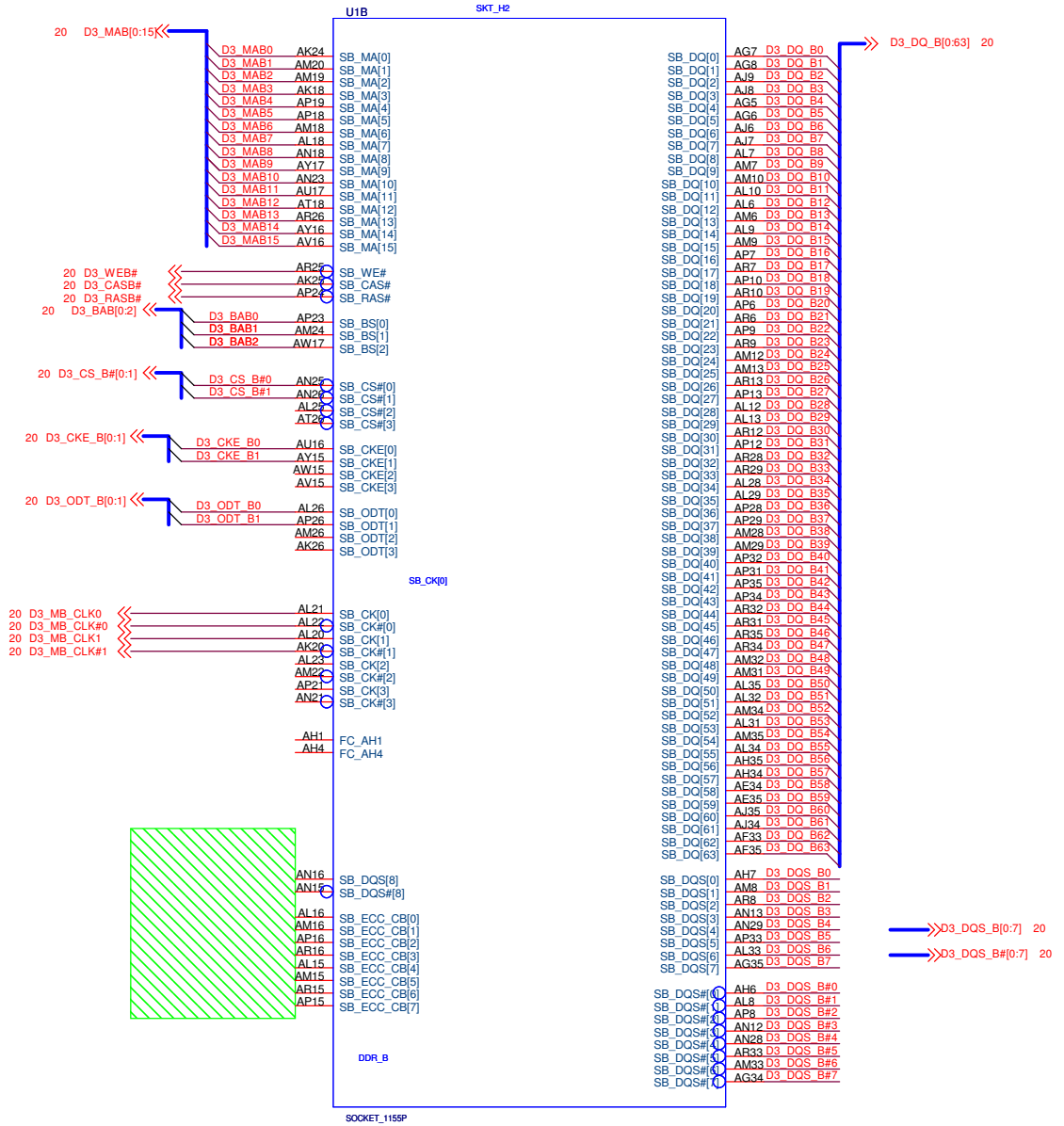
Title : MEM CTRL CHA

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 4 of 47

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



H67M-ITX

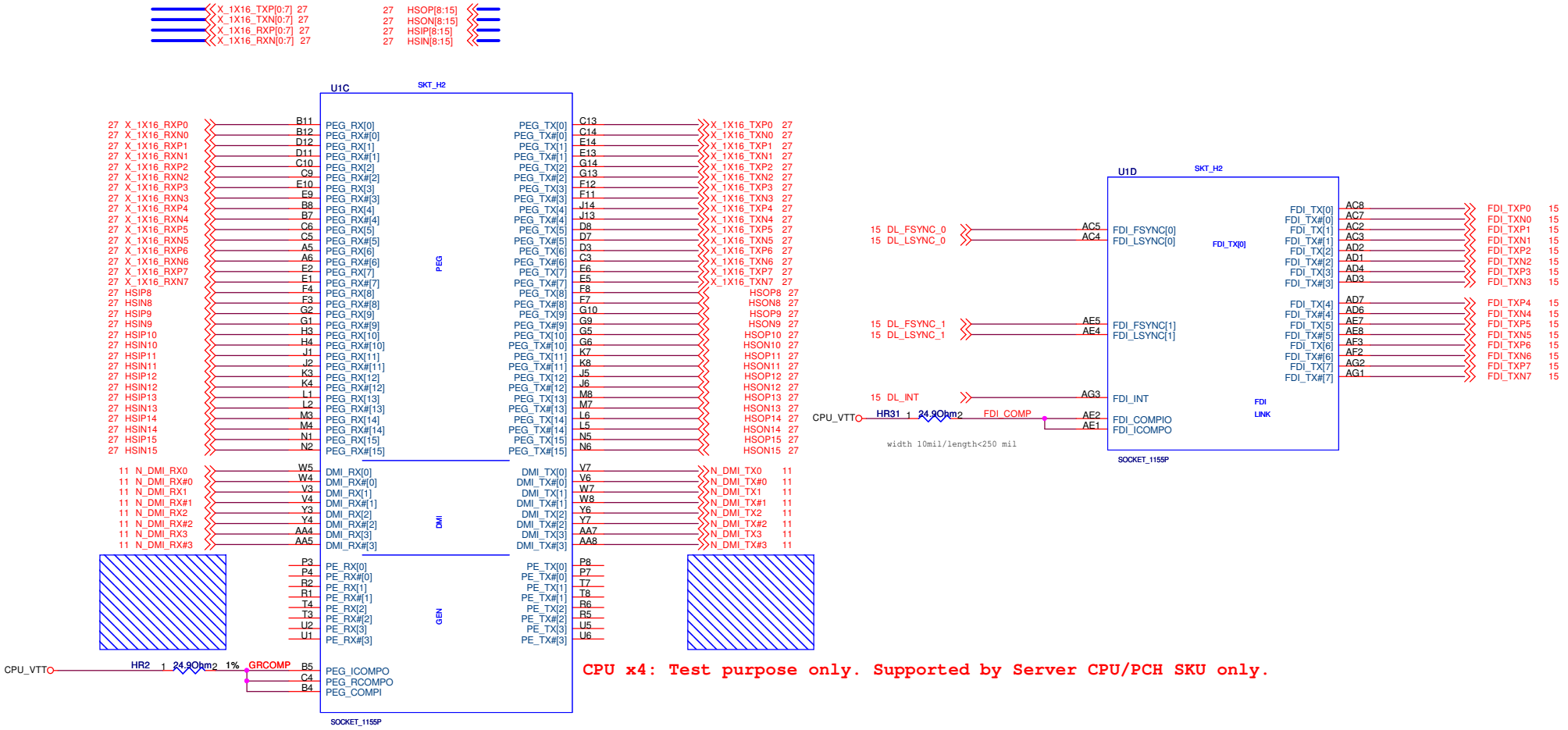
ASRock Inc.

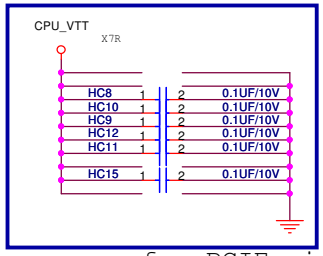
Title : MEM CTRL CHB

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 5 of 47





for PCIE signal trans-layer decoupling capacitors!!!
Place near trans-layer vias for PCIe lanes.

H67M-ITX

ASRock Inc.

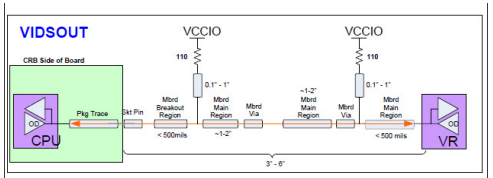
Title : CPU - PEG/FDI

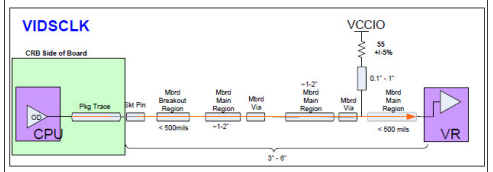
Engineer: Isaac Lee

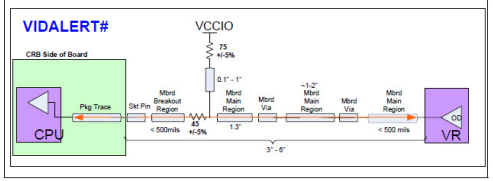
Size	Project Name	Rev
A3	H67M-ITX	1.03

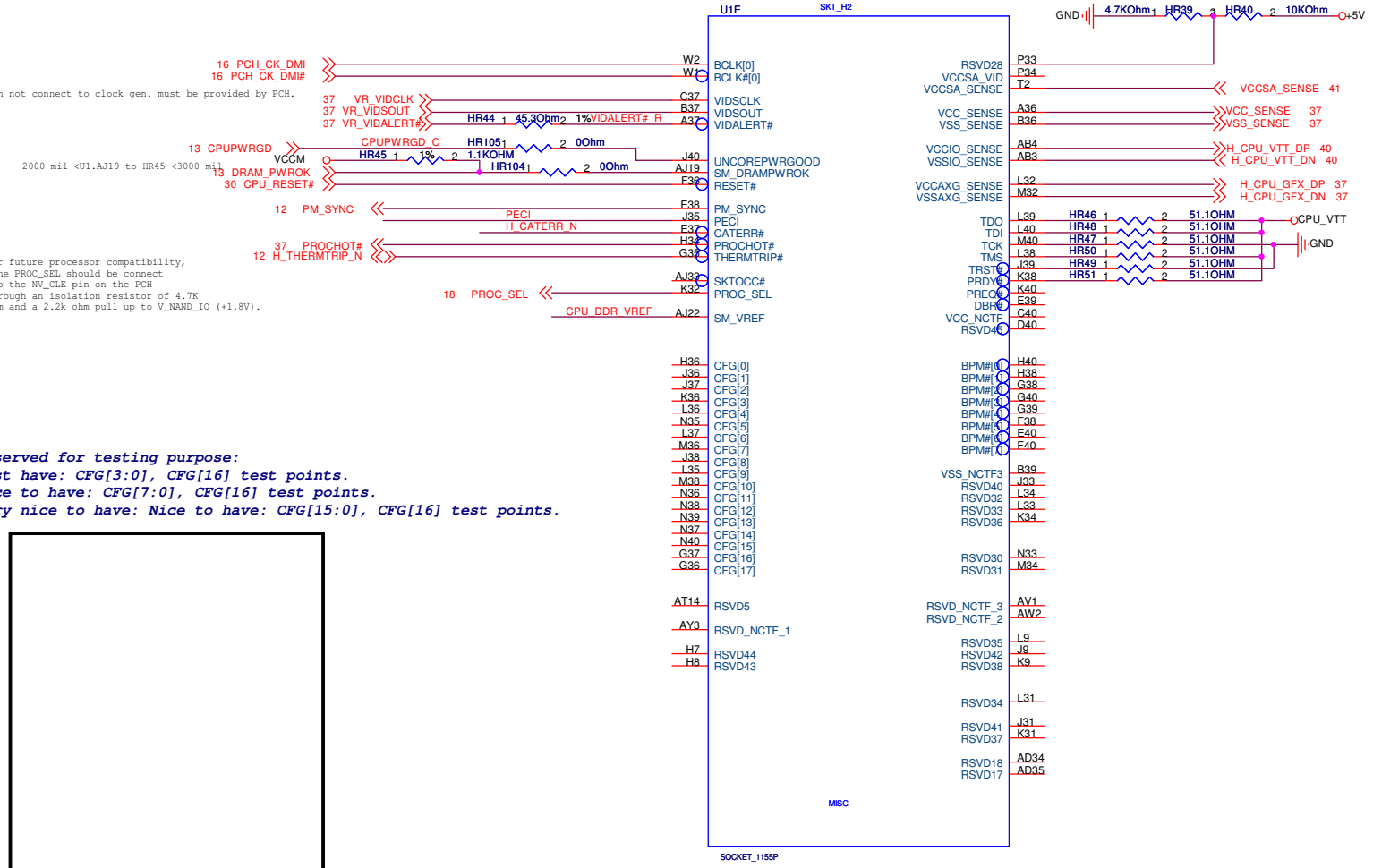
Date: Wednesday, December 19, 2012 Sheet 6 of 47

SVID Placement needs to pay attention for pull up resistors. See PDG page 330

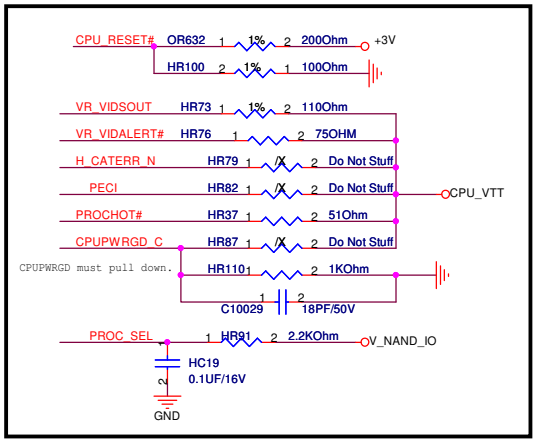


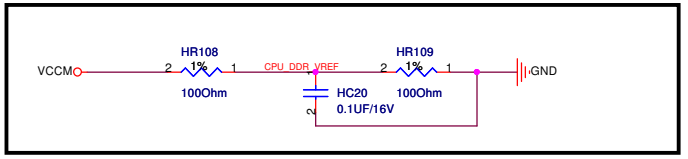


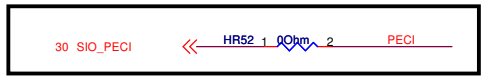




Reserved for testing purpose:
Must have: CFG[3:0], CFG[16] test points.
Nice to have: CFG[7:0], CFG[16] test points.
Very nice to have: Nice to have: CFG[15:0], CFG[16] test points.







H67M-ITX

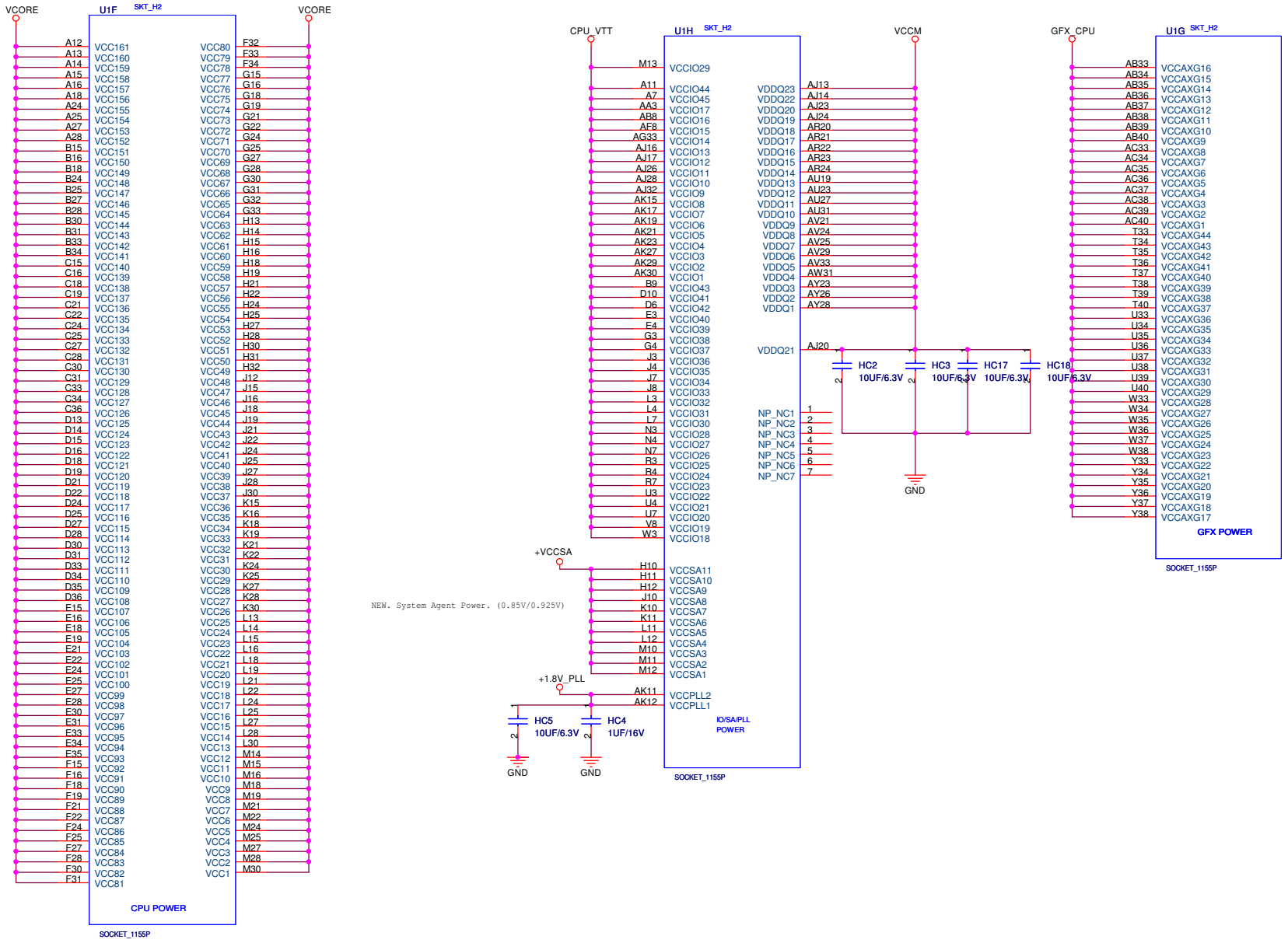
ASRock Inc.

Title : CPU-MISC

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 7 of 47



H67M-ITX

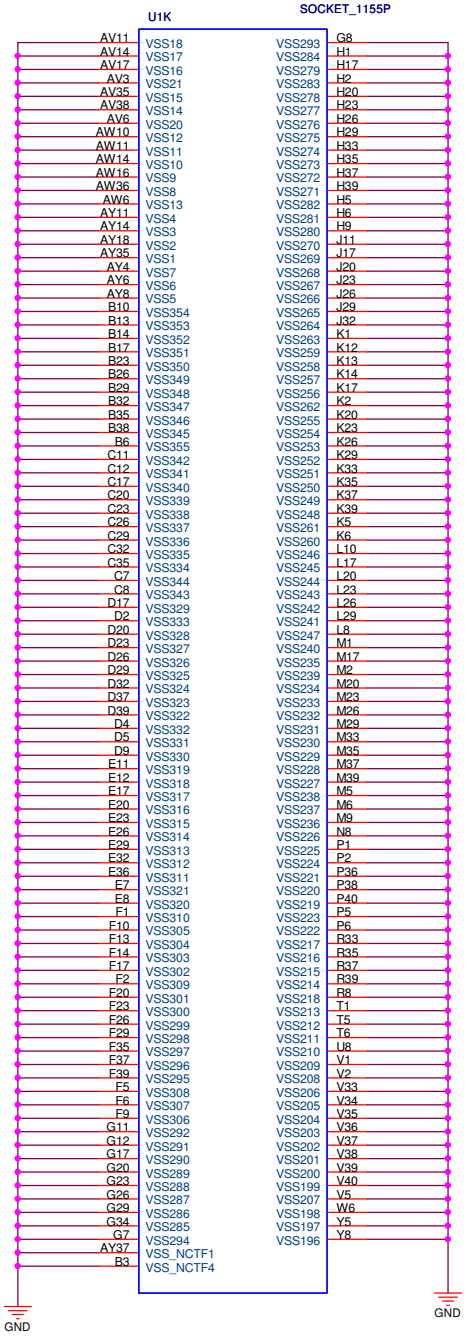
ASRock Inc.

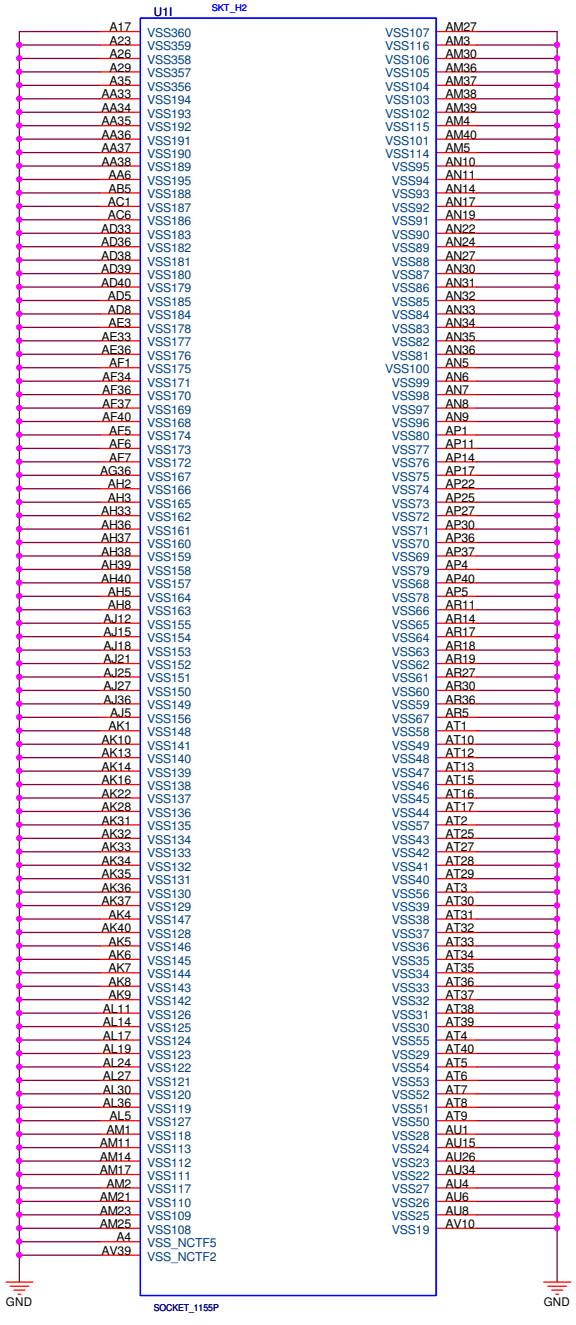
Title : CPU - Power

Engineer: Isaac Lee

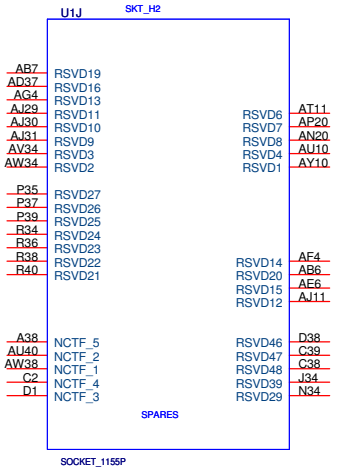
Size	Project Name	Rev
A3	H67M-ITX	1.03

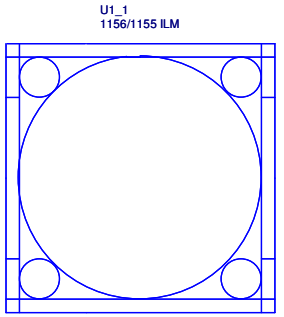
Date: Wednesday, December 19, 2012 Sheet 8 of 47





All reserved. No connected.





H67M-ITX

ASRock Inc.

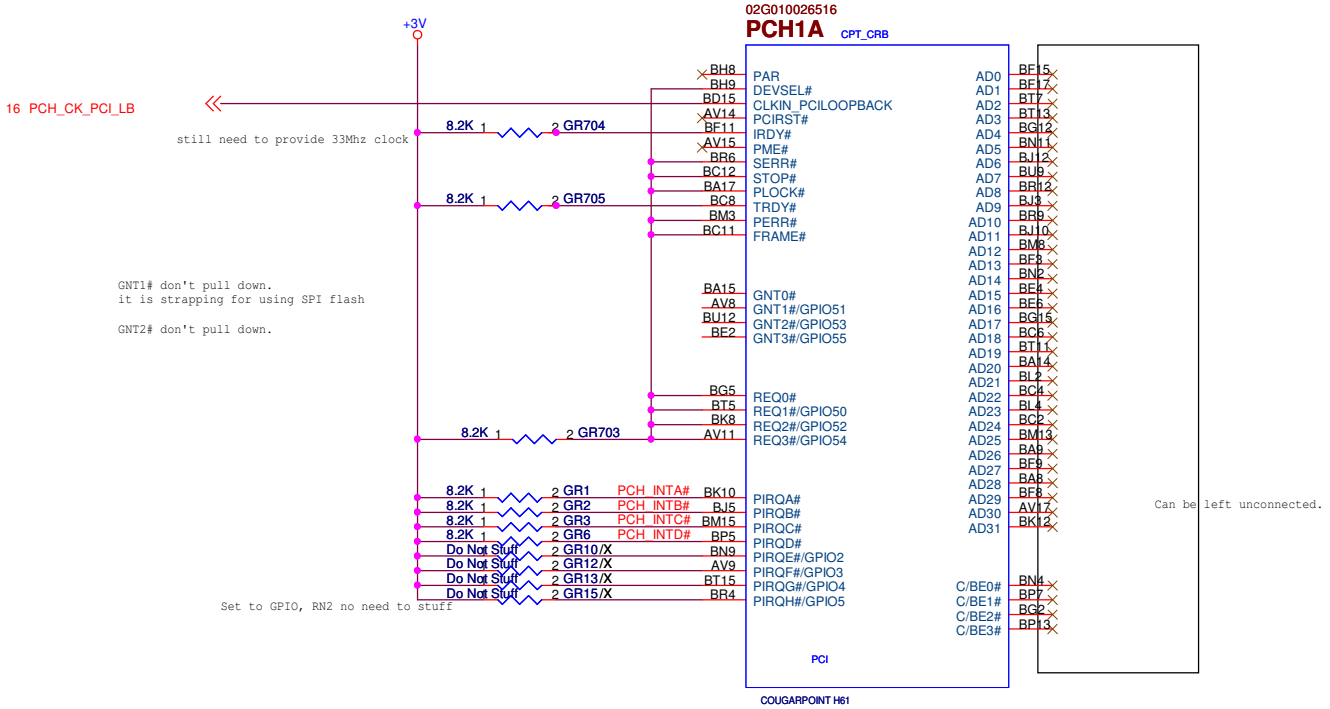
Title : CPU - GND

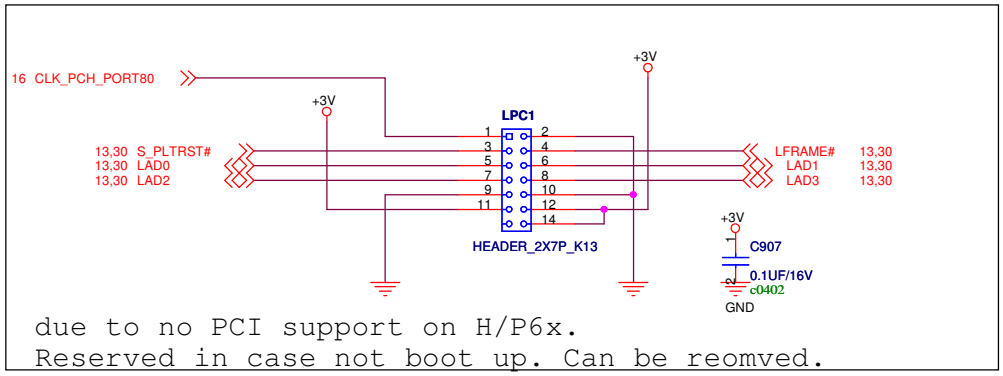
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 9 of 47

H67/P67 do not support PCI. Check PCI solution!!!





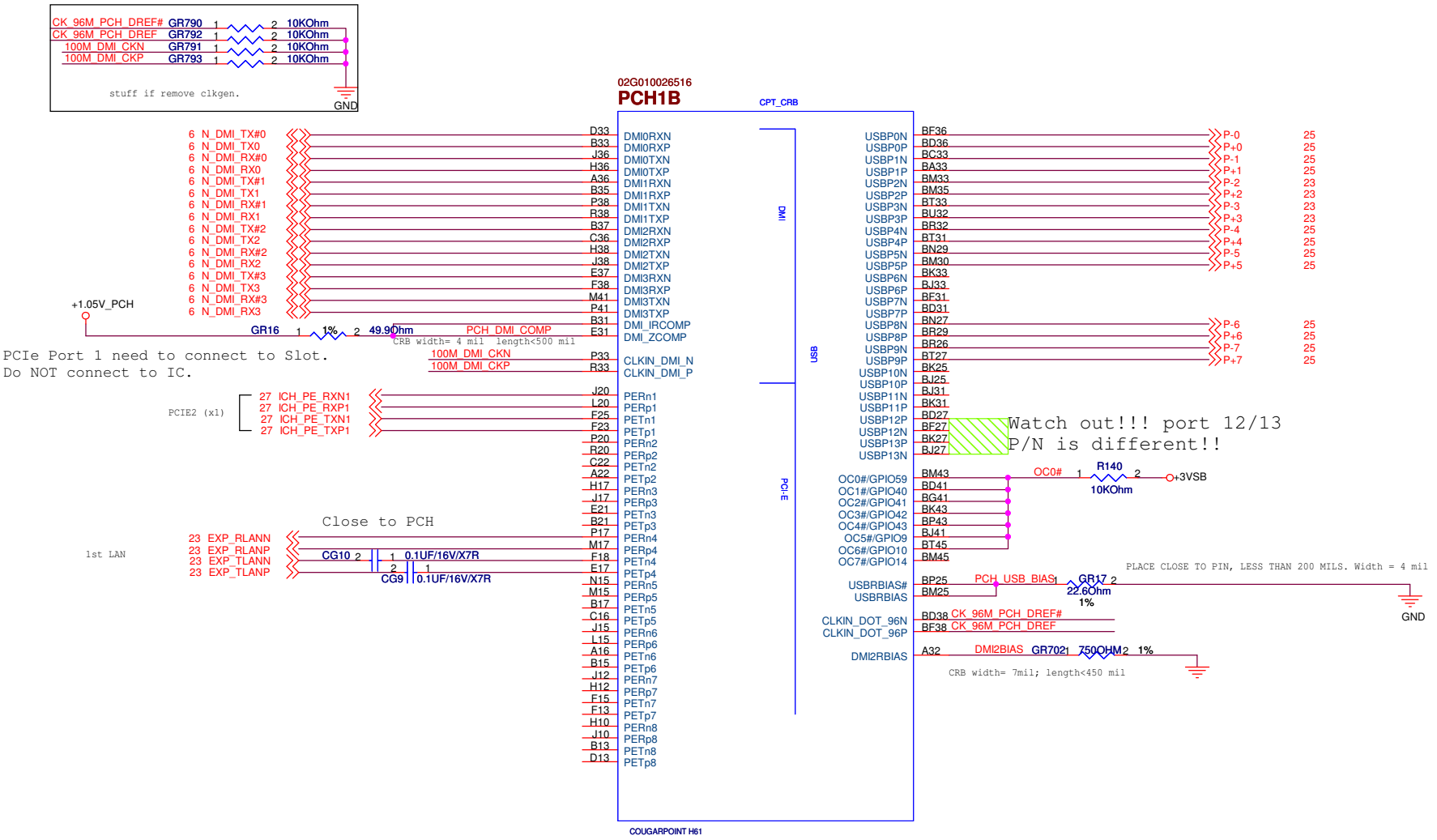
H67M-ITX

ASRock Title : PCH - PCI/LPC

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 10 of 47



H67M-ITX

ASRock Title : PCH - PCIE/DMI/USB

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 11 of 47

02G010026516

PCH1C

CPT_CRB

CL_CLK1 BA50
CL_DATA1 BF50
CL_RST1# BF49
13,30,32 O_PWROK
connect to PCH PWROK if no support M3.
APWROK BC46

PWM0 BN21
PWM1 BT21
PWM2 BM20
PWM3 BN19

PCH_GPIO17 BT17
PCH_GPIO1 BR19
29 FP_PRES# BA22
BR16
PCH_GPIO68 BU16
PCH_GPIO69 BM18
PCH_GPIO70 BN17
PCH_GPIO71 BP15
TACH0/GPIO17
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71

BC43 SST
BA53 SCLOCK/GPIO22
BE54 SLOAD/GPIO38
BF55 SDATAOUT0/GPIO39
AW53 SDATAOUT1/GPIO48

AY20 NC_1

SATA0RXN AC56 — SATA_RXN0 22
SATA0RXP AB55 — SATA_RXP0 22
SATA0TXN AE46 — SATA_TXN0 22
SATA0TXP AE44 — SATA_TXP0 22
SATA1RXN AA53 — SATA_RXN1 22
SATA1RXP AA56 — SATA_RXP1 22
SATA1TXN AG49 — SATA_TXN1 22
SATA1TXP AG47 — SATA_TXP1 22

SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55

SATA2

H61 can not support port 2 & 3

SATA4RXN AN49 — SATA_RXN4 22
SATA4RXP AN50 — SATA_RXP4 22
SATA4TXN AT50 — SATA_TXN4 22
SATA4TXP AT49 — SATA_TXP4 22
SATA5RXN AT46 — SATA_RXN5 22
SATA5RXP AT44 — SATA_RXP5 22
SATA5TXN AV50 — SATA_TXP5 22
SATA5TXP AV49 — SATA_TXN5 22

CLKIN_SATA_N AF55 — CK_100M_SATA#
CLKIN_SATA_P AG56 — CK_100M_SATA

SATALED# BF57 — GR18 1 2 8.2KOhm — +3V
SATAICOMPI AJ55
SATAICOMPO AJ53 — SATA2_COMP — GR19 1 1% 2 37.4Ohm within 500 mil — SATA_ACT# 22 — +1.05V_PCH

SATA0GP/GPIO21 BC54 — PCH_GPIO21 — BIOS_WP# 13
SATA1GP/GPIO19 AY52
SATA2GP/GPIO36 BB55
SATA3GP/GPIO37 BG53
SATA4GP/GPIO16 AU56
SATA5GP/GPIO49 BA56

GPIO19 don't pull down.
it is strapping for using SPI flash

GPIO36/GPIO37 do not pull high

+1.05V_PCH

SATA3COMPI AE54 — SATA3_COMP
SATA3RCOMPO AE52 — GR709 1% 2 49.9Ohm within 500 mil

TP16 AE50

SATA3RBIAS AC52 — SATA3_BIAS — GR710 1% 2 750OHM

GR20 1 2 8.2KOhm
GR65 1 2 8.2KOhm — +3V

A20GATE BB57 — A20GATE 30
INIT3_3V# BN56
RCIN# BG56 — O_KB_RST# 30
SERIRQ AV52 — SERIRQ# 30
THRMTRIP# E56 — H_THERMTRIP_N 7
PECI H48
PMSYNCH F55 — PM_SYNC 7

COUGARPOINT H61

+3V
GR21 1 2 8.2KOhm FP_PRES#
GR23 1 2 8.2KOhm PCH_GPIO17
GR24 1 2 8.2KOhm PCH_GPIO1
GR25 1 2 8.2KOhm PCH_GPIO68
GR26 1 2 8.2KOhm PCH_GPIO69
GR31 1 2 8.2KOhm PCH_GPIO70
GR32 1 2 8.2KOhm PCH_GPIO71
GR22 1 2 8.2KOhm PCH_GPIO21
GND

CK_100M_SATA# GR795 1 2 10KOhm
CK_100M_SATA GR794 1 2 10KOhm
stuff if remove clkgen.
GND

CPU_VTT
H_THERMTRIP_N
GC66 1 /X2 Do Not Stuff GND
Must near PCH
Pull up needs to stuff.

Serial IRQ pull up at SIO side.

H67M-ITX

ASRock Title : PCH - SATA/HOST

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 12 of 47

	HIGH	LOW
GPIO8(IPU)	BTM	FCIM

Enable Internal VRM

GPIO28	High
HDA_SYNC	Low

02G010026516

PCH1D

COUGARPOINT H61

LDRQ1#/GPIO23, FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, LDRQ0#, FWH4/LFRAME#, HDA_BCLK, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_SYNC, SPI_MOSI, SPI_MISO, SPI_CS0#, SPI_CLK, SPI_CS1#, RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, PWROK, RSMRST#, INTVRMEN, DPWROK, DSWVRMEN, SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/PCHHOT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

BMBUSY#/GPIO0, CLKRUN#/GPIO32, HDA_DOCK_EN#/GPIO33, STP_PCI#/GPIO34, GPIO35, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, HDA_DOCK_RST#/GPIO13, GPIO15, GPIO24/MEM_LED, GPIO28, SLP_LAN#/GPIO29, PCIECLKRQ2#/GPIO20, PCIECLKRQ5#/GPIO44, PCIECLKRQ6#/GPIO45, PCIECLKRQ7#/GPIO46, GPIO57, SYS_PWROK, RI#, PLTRST#, WAKE#, SLP_A#, SLP_S3#, SLP_S4#, SLP_S5#/GPIO63, SUS_STAT#/GPIO61, SUSCLK/GPIO62, BATLOW#/GPIO72, SUSACK#, SUSWARN#/SUSPWRDNACK/GPIO30, DRAMPWROK, GPIO27, GPIO31, SLP_SUS#, PWRBTN#, SYS_RESET#, SPKR, PROCPWRGD, TP12, JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS

PM_GPIO(DSW), JTAG(ISIS)

LAD0 10,30 LAD1 10,30 LAD2 10,30 LAD3 10,30 LFRAME# 10,30

28 ACZ_BITCLK — RACZ_BITCLK — 33Ohm GR46 — R_RACZ_BITCLK

28 ACZ_RST# — 33Ohm GR41 — R_ACZ_RST#

28 ACZ_SDIN0 — 33Ohm GR679 — EOT NEAR AUDIO CODEC

GC7 /X Do Not Stuff — Near SB — GND

28 ACZ_SDOUT — 33Ohm GR51 — R_ACZ_SDOUT

28 ACZ_SYNC — 33Ohm GR52 — R_ACZ_SYNC

F1_SPI_MOSI_R, F1_SPI_MISO, F1_SPI_CS#_R, F1_SPI_CLK_R

S_ICH_RTCX1, S_ICH_RTCX2

33 RTCRST# — GR11 20KOhm 1% — S_SRST#

+BAT_3V — GR29 1MOhm — S_INTRUDER#

12,30,32 O_PWROK, 30 RSMRST# — GR720 /X Do Not Stuff — DPWROK, INTVRMEN, DSWVRMEN

+3VSB — GR34 10K — SMBALERT

31 SMB_CLK, 31 SMB_DATA — GR721 2.2KOhm, GR722 2.2KOhm

O_PME# 30

PWM_PG 37 — GR28 8.2KOhm — +3VSB

S_PLTRST# 10,30 — GR27 1KOhm 1% — +3VSB — WAKE# 23,27

NEW!! Need to check!!

SLP_S3# 30, SLP_S4# 30

for measurement only.

SUSWARN# — GR796 10KOhm — +3VSB_A

DRAM_PWROK 7

gpio 27 can not use for led blinking function on CPT.

SLP_SUS# — 0Ohm GR798 — O_PWRBTN# 30

SYS_RESET — RESETCON# 30,32

SPKR — SB_SPKR 28

CPUPWRGD 7

Pull High/Low

DSWVRMEN GR729 392KOhm, INTVRMEN GR33 392KOhm — +BAT_3V

PWM_PG 0.1UF/16V GC63

RSMRST# 0.022UF/16V GC64

O_PWROK GR732 10KOhm

R_ACZ_SYNC GR727 1KOhm

Flash descriptor overide

DPWROK DELAY

+3VSB_A — GR726 100KOhm — DPWROK — GC72 1UF/16V — GND

FET Control

ATX+5VSB — GR776 8.2KOhm /X — GR778 220KOhm /X — SLP_SUS_FET

SLP_SUS# — GR777 220KOhm /X — GQ17 PMBS3904

GC801 1UF/6.3V /X — GND

GC802 1UF/6.3V /X — GND

unstuff all if using SIO's function!

ATX+5VSB — Q811 Do Not Stuff /X — R8487 0Ohm

SLP_SUS_FET — +5VSB

+3VSB_A — Q812 Do Not Stuff /X — R8491 0Ohm

SLP_SUS_FET — +3VSB

SPI ROM

F1_SPI_CS#_R — F1_SPI_CS#

F1_SPI_MOSI_R — F1_SPI_MOSI

F1_SPI_MISO — F1_SPI_MISO

F1_SPI_CLK_R — F1_SPI_CLK

SPI_MOSI do not pull high

U3_1 SPI 32Mb

+3V — 0.1UF/16V GC2 — GR4 8.2KOhm

U3 SOCK8: CE# VDD, SO HOLD#, WP# SCK, VSS SI

F1_SPI_CS#, F1_SPI_MISO, R_SPI_WP#

12 BIOS_WP# — GR7 0Ohm

SPI_HOLD1#, F1_SPI_CLK, F1_SPI_MOSI

+3V — GR5 8.2KOhm

GC3 0.1UF/16V c0402 — GC65 0.1UF/16V c0402

RTC

S_ICH_RTCX1 — GR14 10MOhm — S_ICH_RTCX2

GY1 32.768KHZ

GC5 10PF/50V — GC6 10PF/50V

S_SRST# — GC4 1UF/10V c0603 — GND

GY1_1 JUMPER_WIRE 0.5*6.3*4*6.3mm

RTCX1 and RTCX2 width=4,Length=<1

Case Open

CI1 HEADER_1X2P — CASEOPEN — S_INTRUDER#

OC1 0.1UF/16V — GND

H67M-ITX

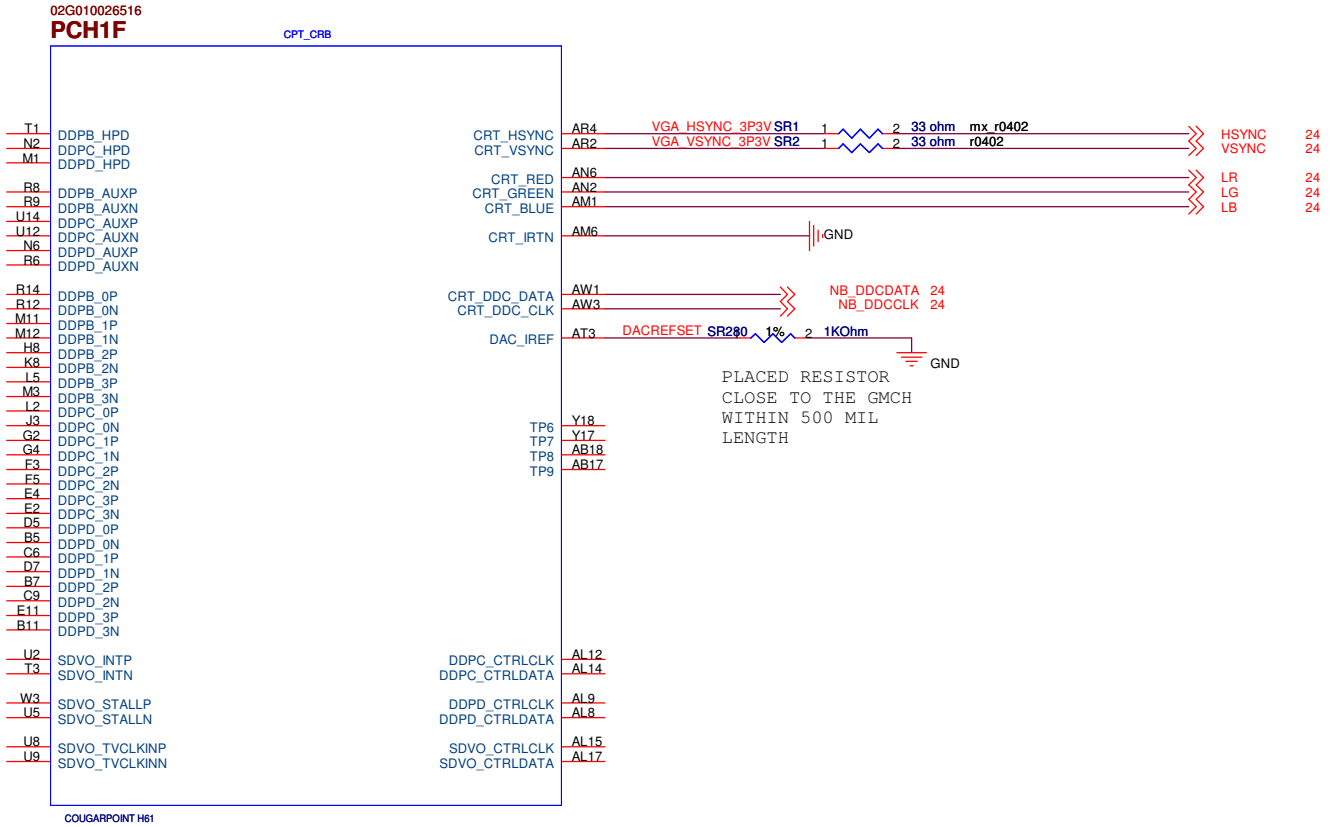
ASRock Inc.

Title : Audio/MISC

Engineer: Isaac Lee

Size	Project Name	Rev
Custom	H67M-ITX	1.03

Date: Monday, December 24, 2012 Sheet 13 of 47



All AC couple capacitors put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following

Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

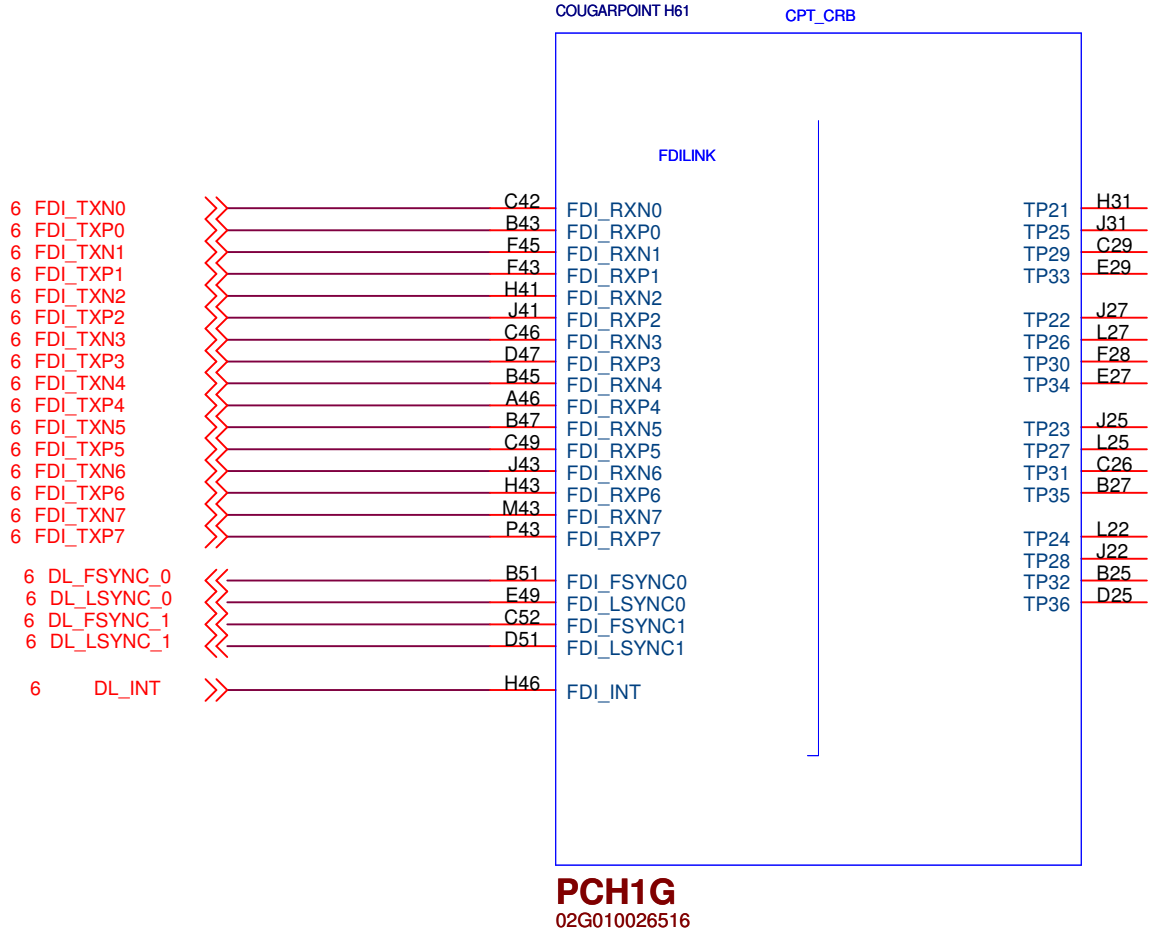
H67M-ITX

ASRock Title : PCH - Display

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 14 of 47



H67M-ITX

ASRock Title : PCH - FDI

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 15 of 47

FLEX CLK HAS RULE OF USING.
SEE PDG PAGE 191 FOR DETAILS.

02G010026516

PCH1H

CPT_CRB

30 PCH_CK_33M_SIO — GR736 1 2 22Ohm — AT11 CLKOUT_PCI0
10 CLK_PCH_PORT80 — GR773 1 2 22Ohm — AN14 CLKOUT_PCI1
10 PCH_CK_PCI_LB — GR770 1 2 22Ohm — AT12 CLKOUT_PCI2
AT17 CLKOUT_PCI3
AT14 CLKOUT_PCI4

AT9 CLKOUTFLEX0/GPIO64
BA5 CLKOUTFLEX1/GPIO65
23 PCH_25M — RG31 1 r0402 2 0Ohm LAN_25M — AW5 CLKOUTFLEX2/GPIO66
30 PCH_CK_48M_SIO — BA2 CLKOUTFLEX3/GPIO67

+1.05V_PCH — 90.9Ohm 2 1% 1 GR43 — AL2 XCLK_RCOMP

AN8 REFCLK14IN

14Mhz no need to connect by using internal clock.

GR797 10KOhm

Flex 0, 1, 2, 3 : Check ME setting!!

AJ5 XTAL25_OUT
AJ3 XTAL25_IN

1MOhm GR45
GX1 25Mhz
GC12 27PF/50V
GC13 27PF/50V

CLKIN_GND1_N — R27 — GR756 1 2 10KOhm
CLKIN_GND1_P — P27 — GR757 1 2 10KOhm
CLKIN_GND0_N — W53 — GR759 1 2 10KOhm
CLKIN_GND0_P — V52 — GR758 1 2 10KOhm

CLKOUT_ITPXDP_N R52
CLKOUT_ITPXDP_P N52

CLKOUT_PCIE7N AE2
CLKOUT_PCIE7P AF1

CLKOUT_DMI_N P31 — PCH_CK_DMI# 7
CLKOUT_DMI_P R31 — PCH_CK_DMI 7

CPU

CLKOUT_DP_N N56
CLKOUT_DP_P M55
unused for PCH platform

CLKOUT_PCIE0N AE6 — PCH_ECLK_PCIE2# 27
CLKOUT_PCIE0P AC6 — PCH_ECLK_PCIE2 27

PCIE x1 Slot

CLKOUT_PCIE1N AA5
CLKOUT_PCIE1P W5

CLKOUT_PCIE2N AB12 — PCH_ECLK_LAN# 23
CLKOUT_PCIE2P AB14 — PCH_ECLK_LAN 23

LAN

CLKOUT_PCIE3N AB9
CLKOUT_PCIE3P AB8

CLKOUT_PCIE4N Y9
CLKOUT_PCIE4P Y8

CLKOUT_PCIE5N AF3
CLKOUT_PCIE5P AG2

CLKOUT_PCIE6N AB3
CLKOUT_PCIE6P AA2

CLKOUT_PEG_A_N AG8 — PCH_ECLK_X16# 27
CLKOUT_PEG_A_P AG9 — PCH_ECLK_X16 27

PCIE x16 Slot

CLKOUT_PEG_B_N AE12
CLKOUT_PEG_B_P AE11

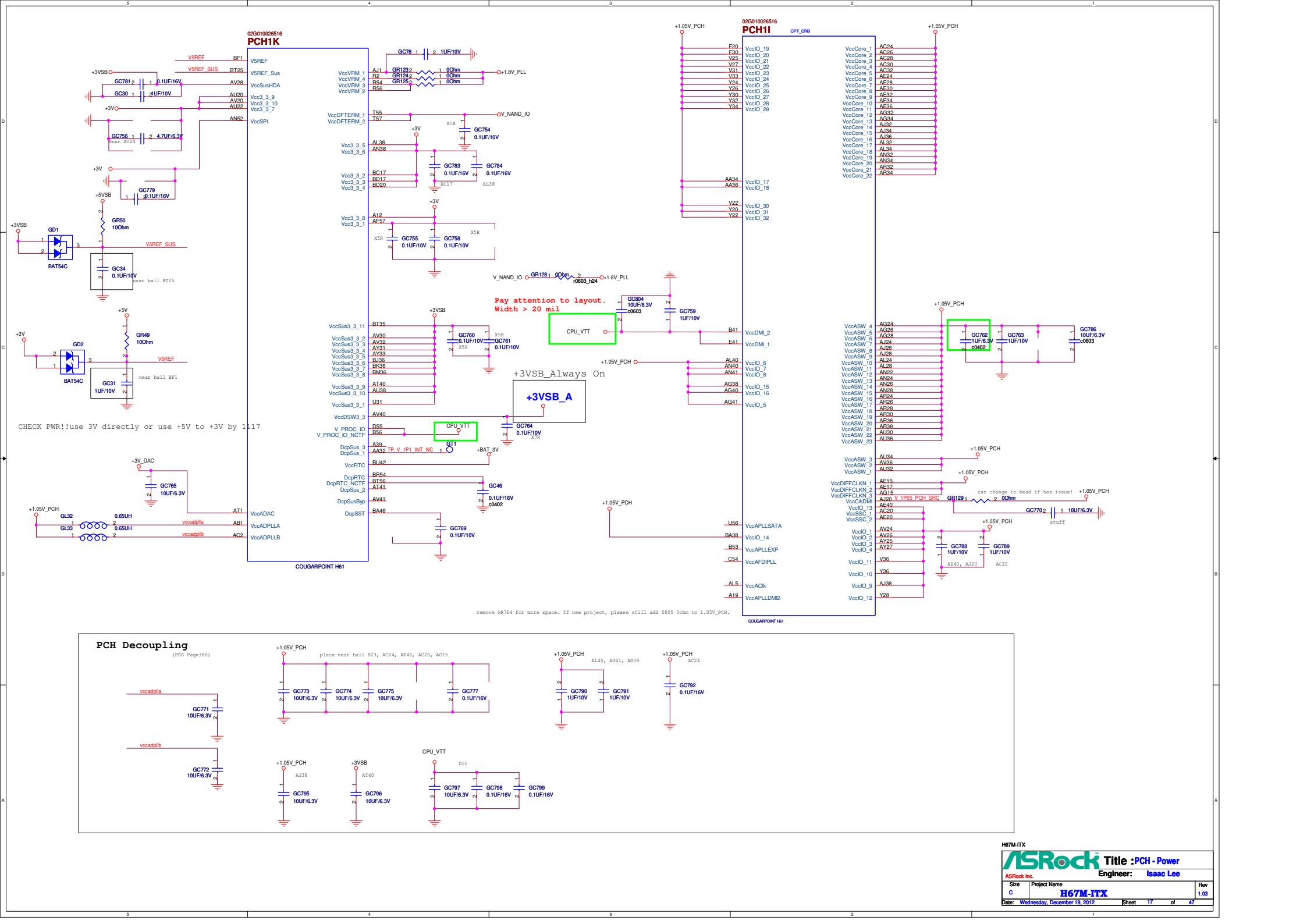
COUGARPOINT H61

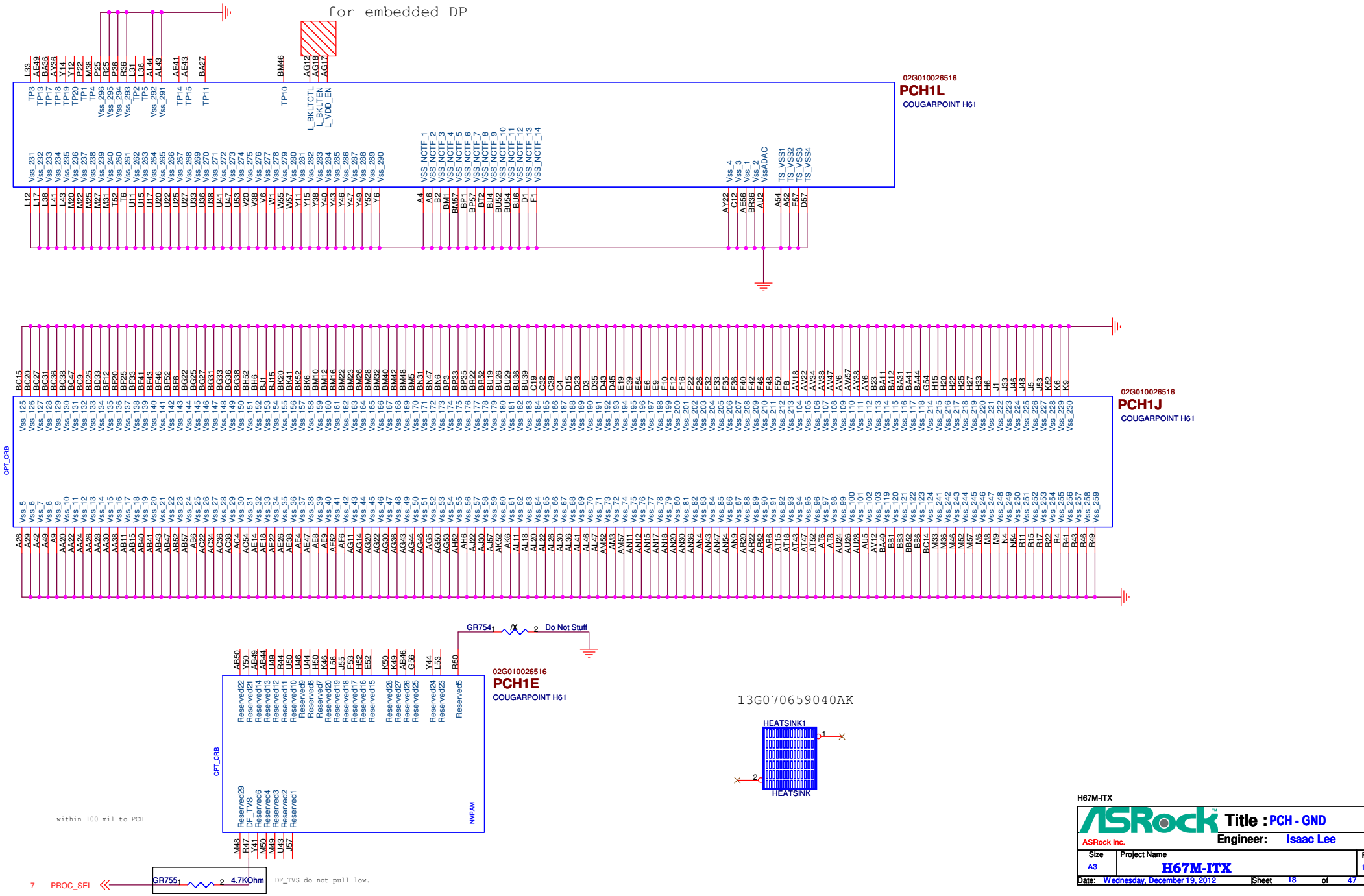
H67M-ITX

ASRock Title :PCH - CLK
ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 16 of 47


02G010026516
PCH1K
COUGARPOINT H61
02G010026516
PCH1I
CPT_CRB
COUGARPOINT H61
Pay attention to layout.
Width > 20 mil
+3VSB_Always On
+3VSB_A
CPU_VTT
CHECK PWR!!use 3V directly or use +5V to +3V by 1117
remove GR764 for more space. If new project, please still add 0805 0ohm to 1.05V_PCH.
can change to bead if has issue!
PCH Decoupling
(PDG Page366)
place near ball B23, AC24, AE40, AC20, AG15
AL40, AG41, AG38
AC24
AJ38
AT40
D55
ASRock
Title :PCH - Power
ASRock Inc.
Engineer: Isaac Lee
H67M-ITX
Size C
Project Name H67M-ITX
Rev 1.03
Date: Wednesday, December 19, 2012
Sheet 17 of 47



H67M-ITX

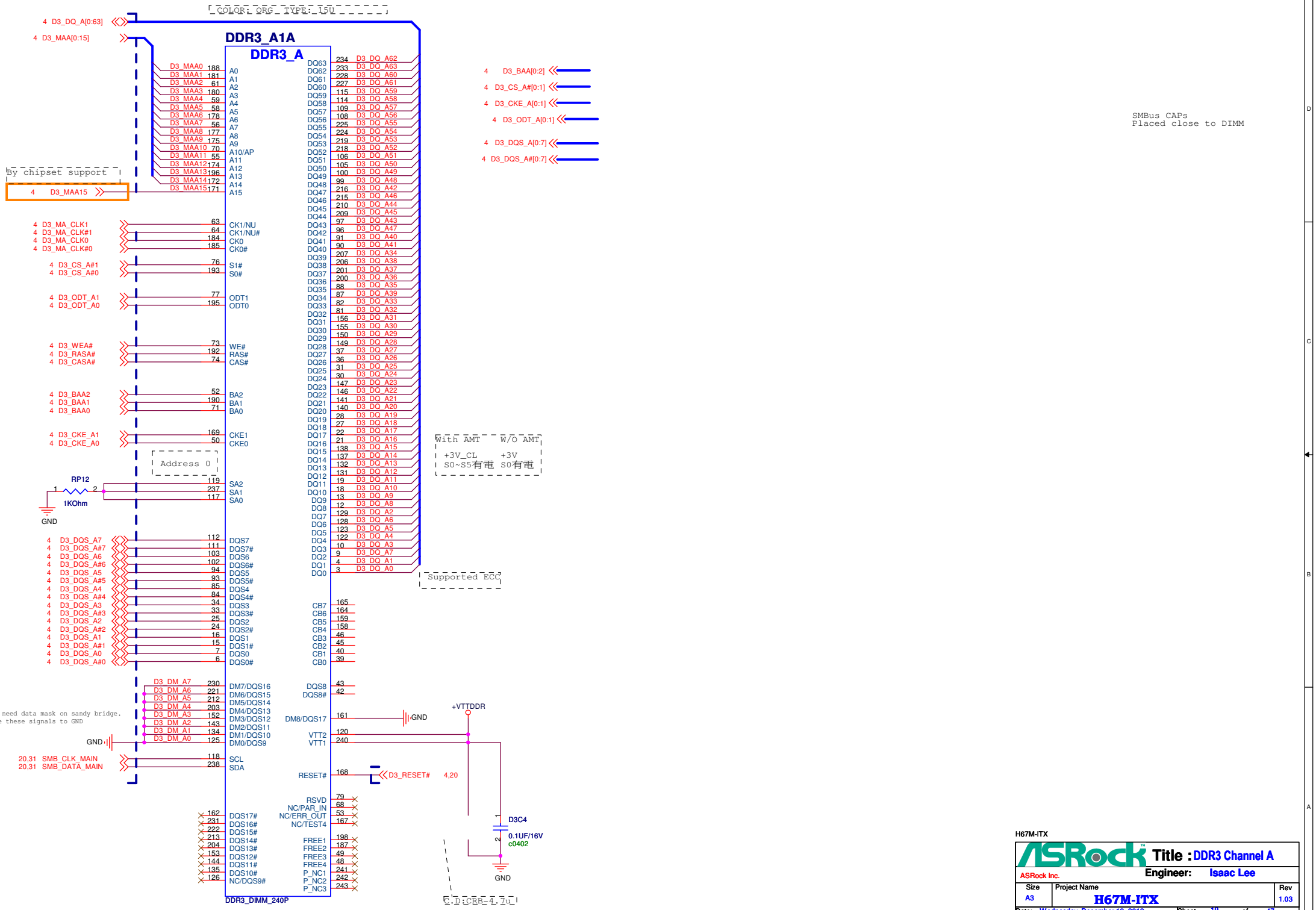
ASRock Inc.

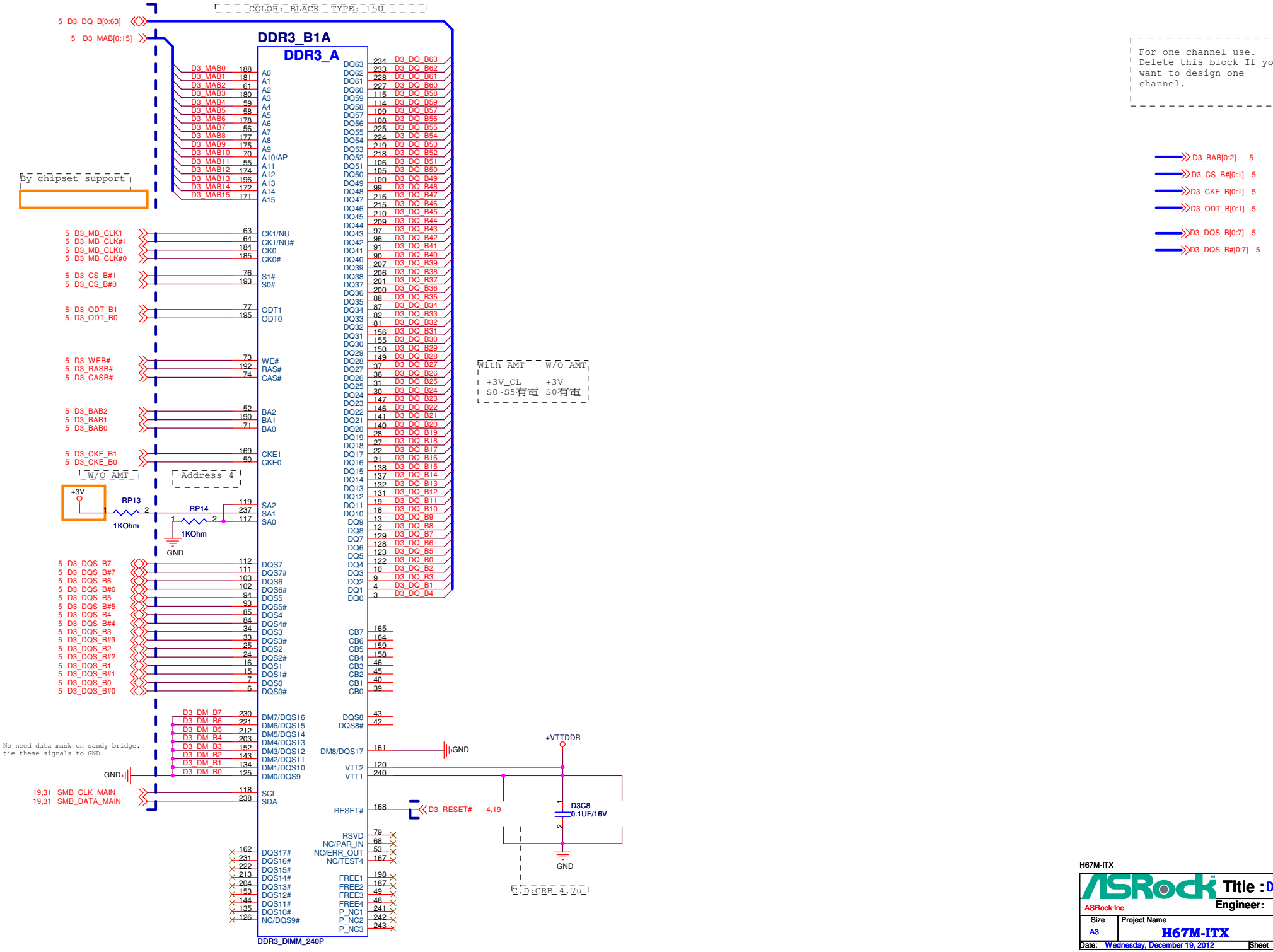
Title : PCH - GND

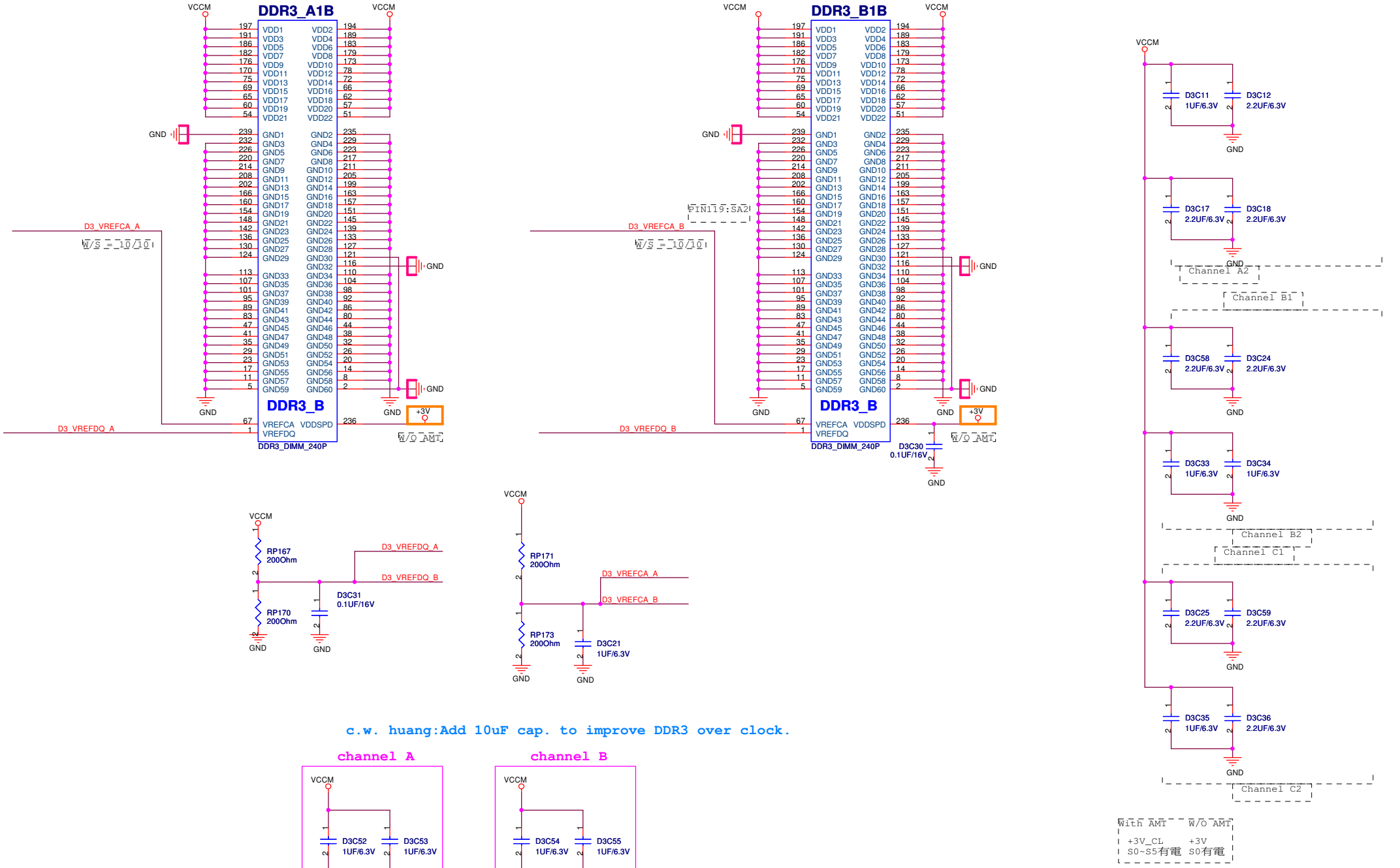
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 18 of 47


COLOR: ORG TYPE: 15U
DDR3_A1A
DDR3_A
4 D3_DQ_A[0:63]
4 D3_MAA[0:15]
By chipset support
4 D3_MAA15
4 D3_MA_CLK1
4 D3_MA_CLK#1
4 D3_MA_CLK0
4 D3_MA_CLK#0
4 D3_CS_A#1
4 D3_CS_A#0
4 D3_ODT_A1
4 D3_ODT_A0
4 D3_WEA#
4 D3_RASA#
4 D3_CASA#
4 D3_BAA2
4 D3_BAA1
4 D3_BAA0
4 D3_CKE_A1
4 D3_CKE_A0
Address 0
RP12
1KOhm
GND
4 D3_DQS_A7
4 D3_DQS_A#7
4 D3_DQS_A6
4 D3_DQS_A#6
4 D3_DQS_A5
4 D3_DQS_A#5
4 D3_DQS_A4
4 D3_DQS_A#4
4 D3_DQS_A3
4 D3_DQS_A#3
4 D3_DQS_A2
4 D3_DQS_A#2
4 D3_DQS_A1
4 D3_DQS_A#1
4 D3_DQS_A0
4 D3_DQS_A#0
No need data mask on sandy bridge.
tie these signals to GND
GND
20,31 SMB_CLK_MAIN
20,31 SMB_DATA_MAIN
DDR3_DIMM_240P
4 D3_BAA[0:2]
4 D3_CS_A#[0:1]
4 D3_CKE_A[0:1]
4 D3_ODT_A[0:1]
4 D3_DQS_A[0:7]
4 D3_DQS_A#[0:7]
With AMT W/O AMT
+3V_CL +3V
S0~S5有電 S0有電
Supported ECC
+VTTDDR
GND
D3_RESET# 4,20
D3C4
0.1UF/16V
c0402
GND
C_D:CRB_4.7u
SMBus CAPs
Placed close to DIMM
H67M-ITX
ASRock
Title : DDR3 Channel A
ASRock Inc.
Engineer: Isaac Lee
Size A3
Project Name H67M-ITX
Rev 1.03
Date: Wednesday, December 19, 2012
Sheet 19 of 47


COLOR: BLACK TYPE: 15U
DDR3_B1A
DDR3_A
5 D3_DQ_B[63:0]
5 D3_MAB[0:15]
By chipset support
5 D3_MB_CLK1
5 D3_MB_CLK#1
5 D3_MB_CLK0
5 D3_MB_CLK#0
5 D3_CS_B#1
5 D3_CS_B#0
5 D3_ODT_B1
5 D3_ODT_B0
5 D3_WEB#
5 D3_RASB#
5 D3_CASB#
5 D3_BAB2
5 D3_BAB1
5 D3_BAB0
5 D3_CKE_B1
5 D3_CKE_B0
W/O AMT
Address 4
+3V
RP13
1KOhm
RP14
1KOhm
GND
5 D3_DQS_B7
5 D3_DQS_B#7
5 D3_DQS_B6
5 D3_DQS_B#6
5 D3_DQS_B5
5 D3_DQS_B#5
5 D3_DQS_B4
5 D3_DQS_B#4
5 D3_DQS_B3
5 D3_DQS_B#3
5 D3_DQS_B2
5 D3_DQS_B#2
5 D3_DQS_B1
5 D3_DQS_B#1
5 D3_DQS_B0
5 D3_DQS_B#0
D3_DM_B7
D3_DM_B6
D3_DM_B5
D3_DM_B4
D3_DM_B3
D3_DM_B2
D3_DM_B1
D3_DM_B0
No need data mask on sandy bridge.
tie these signals to GND
GND
19,31 SMB_CLK_MAIN
19,31 SMB_DATA_MAIN
DDR3_DIMM_240P
With AMT
+3V_CL
S0~S5有電
W/O AMT
+3V
S0有電
For one channel use.
Delete this block If you want to design one channel.
D3_BAB[0:2] 5
D3_CS_B#[0:1] 5
D3_CKE_B[0:1] 5
D3_ODT_B[0:1] 5
D3_DQS_B[0:7] 5
D3_DQS_B#[0:7] 5
+VTTDDR
D3_RESET# 4,19
D3C8
0.1UF/16V
GND
C_D:CRB_4.7u
H67M-ITX
ASRock
Title : DDR3 Channel B
ASRock Inc.
Engineer: Isaac Lee
Size A3
Project Name H67M-ITX
Rev 1.03
Date: Wednesday, December 19, 2012
Sheet 20 of 47



H67M-ITX

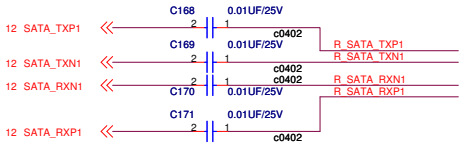
ASRock Inc.

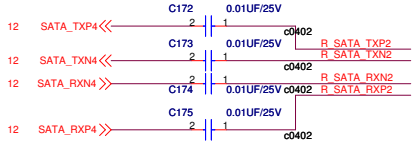
Title : DDR3 (Power)

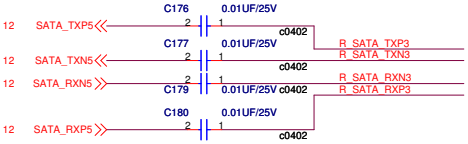
Engineer: Isaac Lee

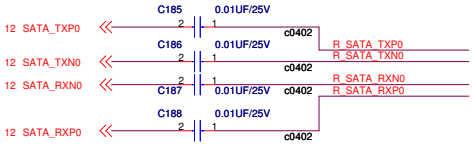
Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 21 of 47



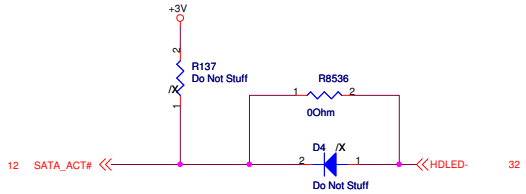




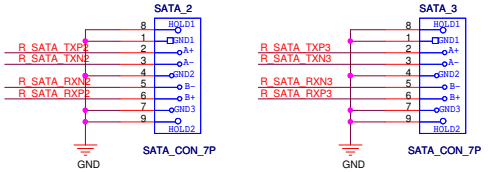


SATA3 & SATA LED

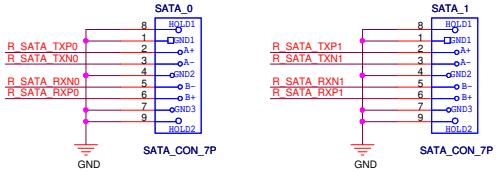
1.00 Internal Pull UP
1.00 If need pul up, check +3.3V or +5V



INTEL SATA2



INTEL SATA3



Check SATA Port Name with leaders!!!

H67M-ITX

ASRock Inc.

Title : SATA3/SATA2 / ESATA

Engineer: Isaac Lee

Size	Project Name	Rev
Custom	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 22 of 47

pin12,27,39,42,47,48 for RTL8111E
pin27,39,42,47,48 for RTL8105E

+3VSB
CG35 0.1UF/16V
CG36 0.1UF/16V
CG44 0.1UF/16V
CG53 0.1UF/16V
CG55 0.1UF/16V
CG60 Do Not Stuff /X/for 8105E
VDD33

RG26 0Ohm
AVDD33_REG
CG51 4.7UF/6.3V c0805_h57
CG56 0.1UF/16V

REGOUT
LG5 4.7UH
CG50 4.7UF/6.3V c0805_h57
RG24 0Ohm
CG52 0.1UF/16V
L_EVDD10
RG23 0Ohm
for pin 21
EVDD10
CG48 0.1UF/16V
CG49 1UF/16V c0603

pin3,6,9,13,29,41,45 for RTL8111E
pin3,13,29,45 for RTL8105E
VDD10
CG20 0.1UF/16V
CG21 Do Not Stuff /X/for 8105E
CG22 Do Not Stuff /X/for 8105E
CG23 0.1UF/16V
CG24 0.1UF/16V
CG25 Do Not Stuff /X/for 8105E
CG61 0.1UF/16V

VDD33
RG12 1KOhm 1%
GPO
LAN_SMBDATA
RG27 10KOhm 1%
When using EFUSE/BIOS patch without ASF function

UG5
GND2
MDIP_0 MDIN_0 VDD10 MDIP_1 MDIN_1 VDD10 MDIP_2 MDIN_2 VDD10 MDIP_3 MDIN_3 VDD33
MDIP0 MDIN0 AVDD10_1 MDIP1 MDIN1 AVDD10_2 MDIP2 MDIN2 AVDD10_3 MDIP3 MDIN3 AVDD33_1
AVDD33_2 AVDD33_3 RSET AVDD10_4 CKXTAL2 CKXTAL1 AVDD33_4 DVDD10_3 LED_0 DVDD33_2 GPO/SMBALERT LED1/EESK
REGOUT VDDREG1 VDDREG2 ENSWREG EEDI LED3/EEDO EECS DVDD10_2 LANWAKEB DVDD33_1 ISOLATEB PERSTB
REGOUT AVDD33_REG AVDD33_REG ENSWREG EEDI BLK_TXRX EECS VDD10 WAKE# 13,27 VDD33 ISOLATEB LAN_PLTRST#_IC
RG22 0Ohm r0402 PLTRST#_IC 30
DVDD10_1 SMBCLK SMBDATA CLKREQB HSIP HSIN REFCLK_P REFCLK_N LED0_0 HSOP HSON GND1
RTL8105E-VB-GR

Enable Swithch regulator
VDD33
RG21 0Ohm r0402

LED3 for Activity
LED0,1 for link

CLKREQB RG20 10KOhm 1%
/X WAKE# RG29 Do Not Stuff
LAN_SMBCLK RG28 10KOhm 1%
EEDI RG3 10KOhm 1%
EECS RG16 10KOhm 1%

RTSET RG2 2.49KOhm 1%
RG2 close to Lan Chip Pin#46

X3 25Mhz
PH25M1 PH25M2
/X CG39 27PF/50V
/X CG38 27PF/50V

Close to Lan Chip
HSIP HSIN
EXP_TLANP 11
EXP_TLANN 11
HSON HSOP
CG11 0.1UF/16V
CG12 0.1UF/16V
EXP_RLANN 11
EXP_RLANP 11
PCH_ECLK_LAN# 16
PCH_ECLK_LAN 16

+3V
RG10 1KOhm 1%
ISOLATEB
RG11 15KOhm 1%

11 P+2 LP+2
11 P-2 LP-2
11 P+3 LP+3
11 P-3 LP-3

CLED1 BLK_TXRX 150PF/50V
CLED2 LINK_100# 150PF/50V
CLED3 LINK_1000# 150PF/50V
GND

LAN_USB01 P/R:
10/100: 12G142333224
1000 :12G14263322WAK

LAN_USB23
LANGND30 LANGND28 LANGND27 LANGND29
ACTLEDP ACTLEDN
RG33 249Ohm
RG34 249Ohm
LINK_1000#
LINK_100#
RLED7 Do Not Stuff /
RLED6 Do Not Stuff /
+3VSB

SBV0123
LP-3 LP+3 LP-2 LP+2
USB_VCC1 USB_VCC2 2P- 2P+ 1P- 1P+ USB_GND1 USB_GND2
LAN_CON_USB
CT TD4- TD4+ TD3- TD3+ TD2- TD2+ TD1- TD1+ VCT
MDIN_3 MDIP_3 MDIN_2 MDIP_2 MDIN_1 MDIP_1 MDIN_0 MDIP_0 LAN_VCT
LR6 0Ohm /GLAN
LC18 0.1UF/16V
GND

USBGND26 USBGND24 USBGND23 USBGND25
LILEDN LILEDP
BLK_TXRX RLED5 Do Not Stuff /
LILEDP RLED8 330OHM
LC20 / Do Not Stuff c0402
+3VSB GND

10/100 LAN connector
Pin 19 (Active LED+) : +3VSB
Pin 20 (Active LED-) : LED3
Pin 21 (Link LED+) : LED0
Pin 22 (Link LED-) : LED1

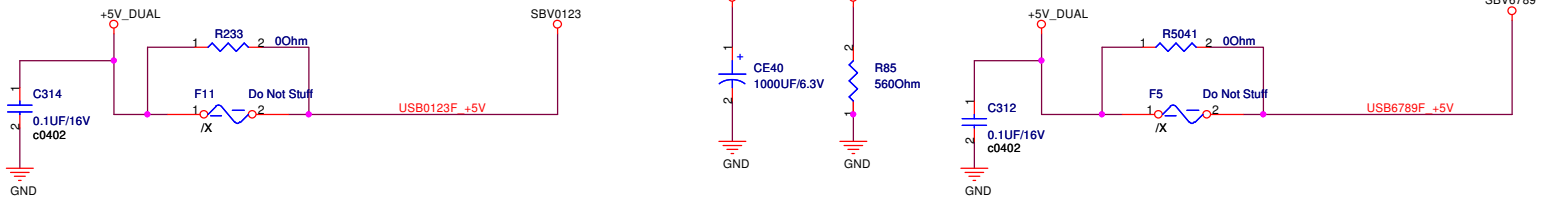
Left LED:
1. YELLOW : Activity
Right LED:
1. Green : 100Mbps
2. No Light : 10Mbps
LAN
USB1
USB2

PH25M1 RG30 r0402 0Ohm PCH_25M 16

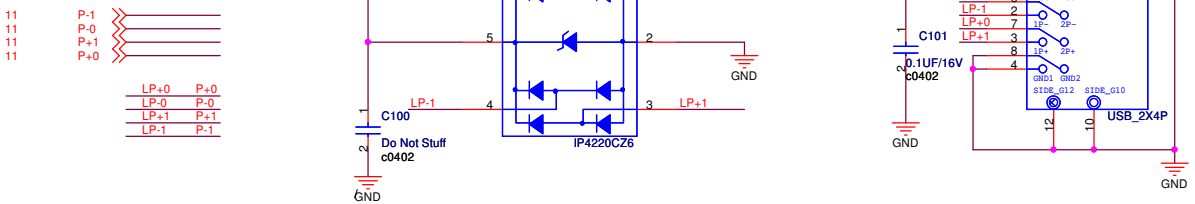
UD3
LP-3 LP+3 LP-2 LP+2
+5V_DUAL
C102 0.1UF/16V c0402
GND
IP4220CZ6

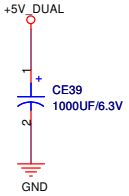
bom
ASRock Title : LAN RTL8105E
ASRock Inc. Engineer: Chia-Wei Chang
Size Custom | Project Name H61M-HVS | Rev 1.00
Date: Tuesday, May 07, 2013 | Sheet 23 of 41

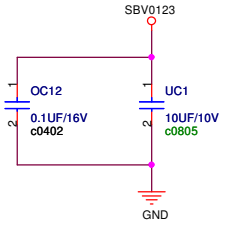
USB Power

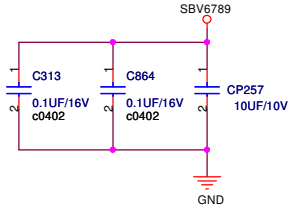


USB 0,1

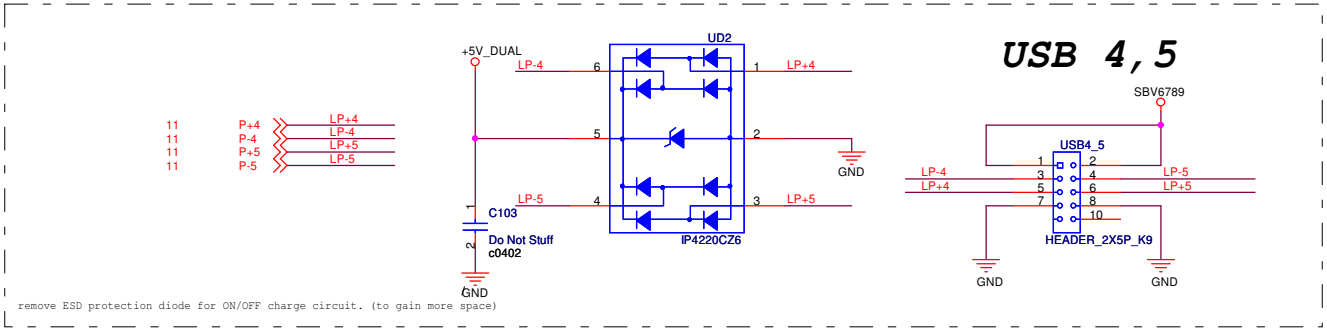




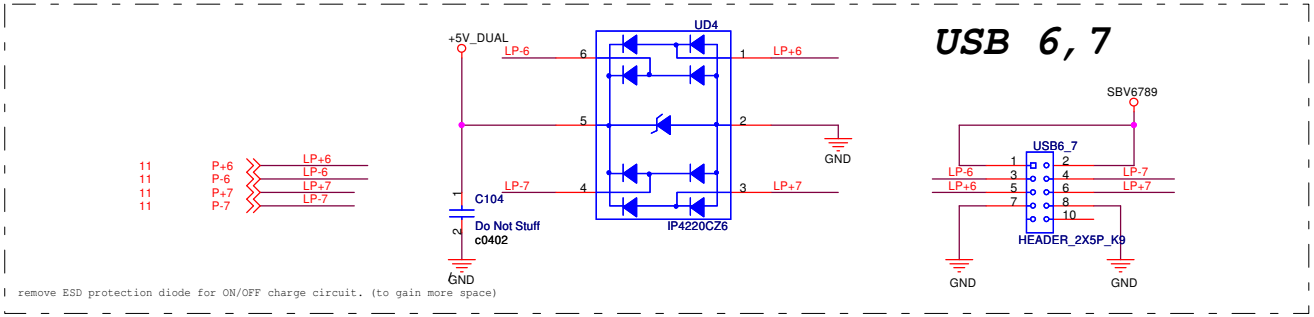




USB 4,5



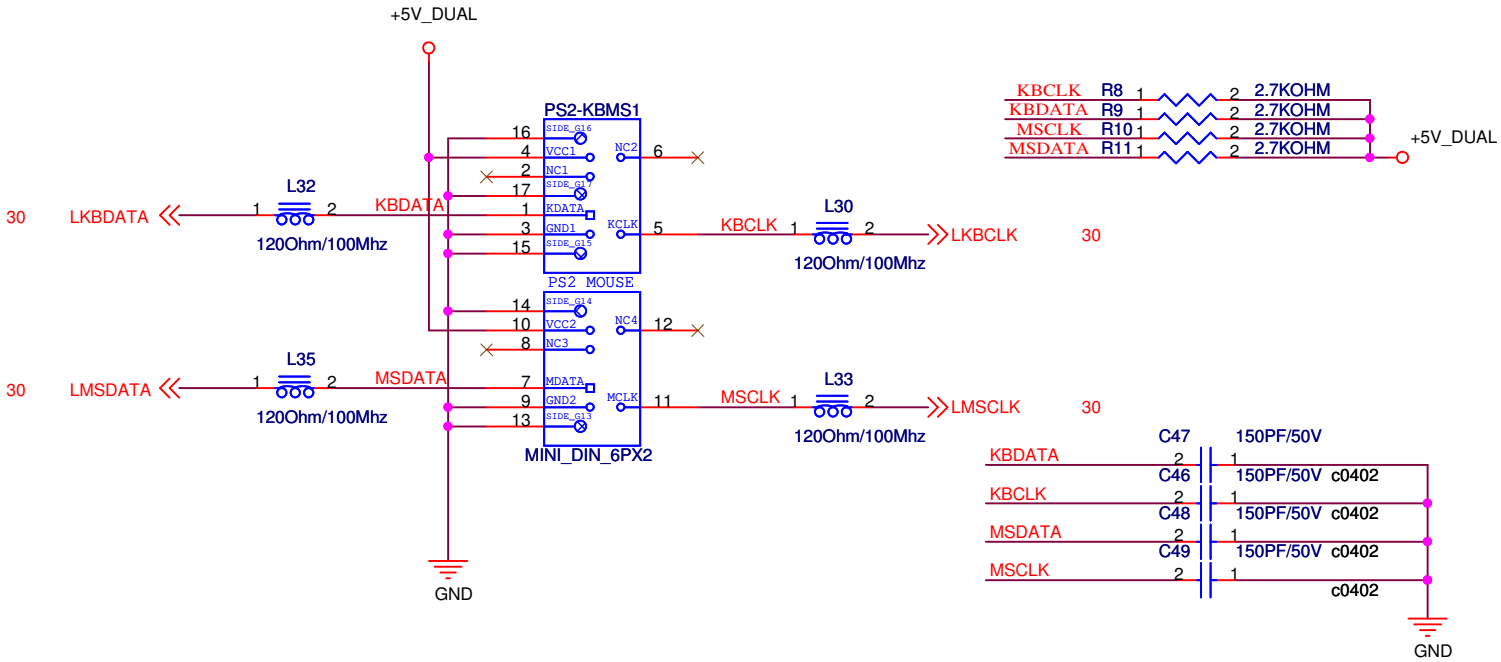
USB 6,7



H67M-ITX

ASRock Inc.	Title : USB Port	
	Engineer: Isaac Lee	
Size: A3	Project Name: H67M-ITX	Rev: 1.03
Date: Wednesday, December 19, 2012	Sheet 25 of 47	

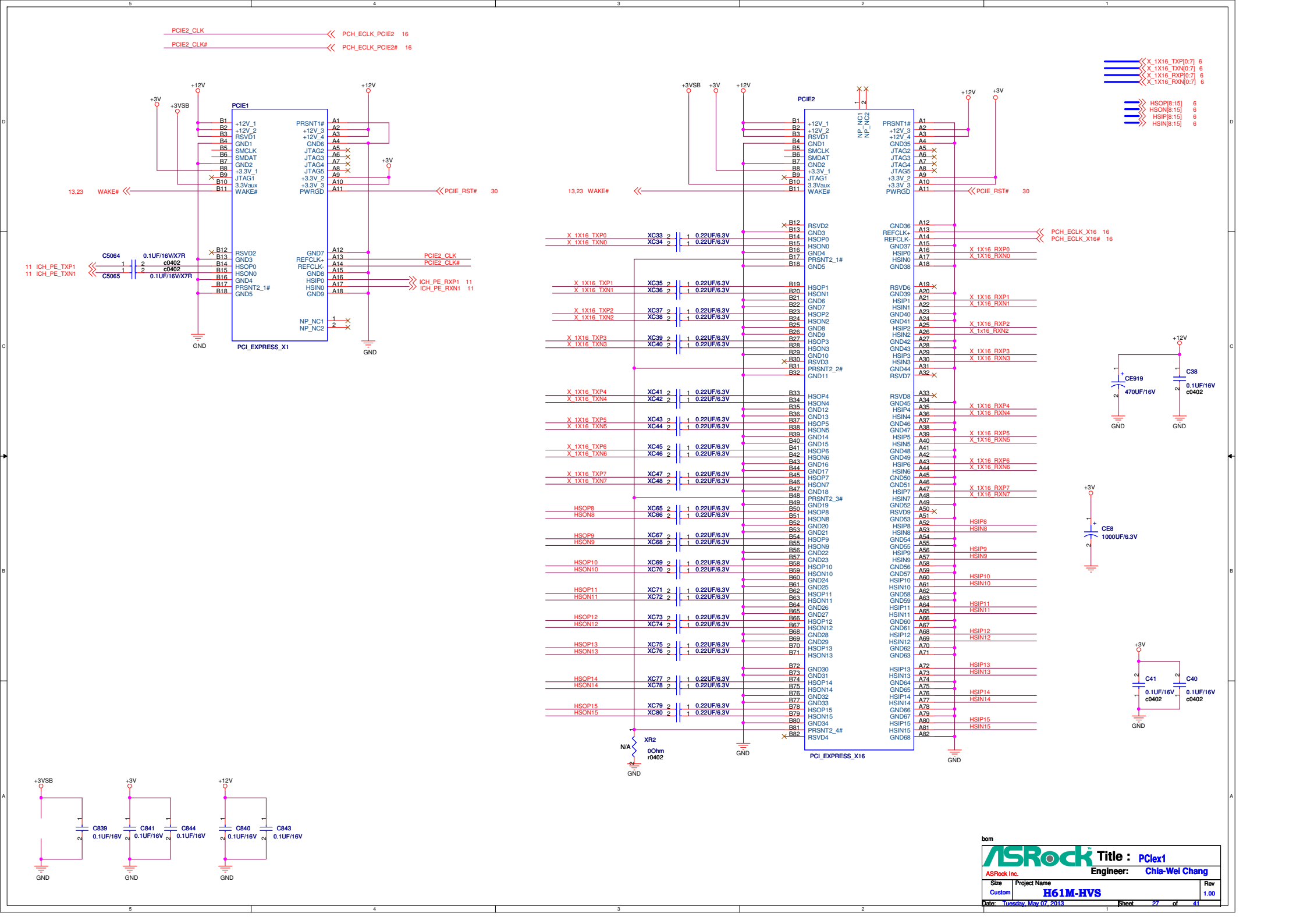
*Modify LMSCLK & LKBDATA



remove ESD protection diode for ON/OFF charge circuit. (to gain more space)

H67M-ITX

ASRock Inc.	Title : KB & MS	
	Engineer: Isaac Lee	
Size: A4	Project Name: H67M-ITX	Rev: 1.03
Date: Wednesday, December 19, 2012	Sheet 26 of 47	



bom

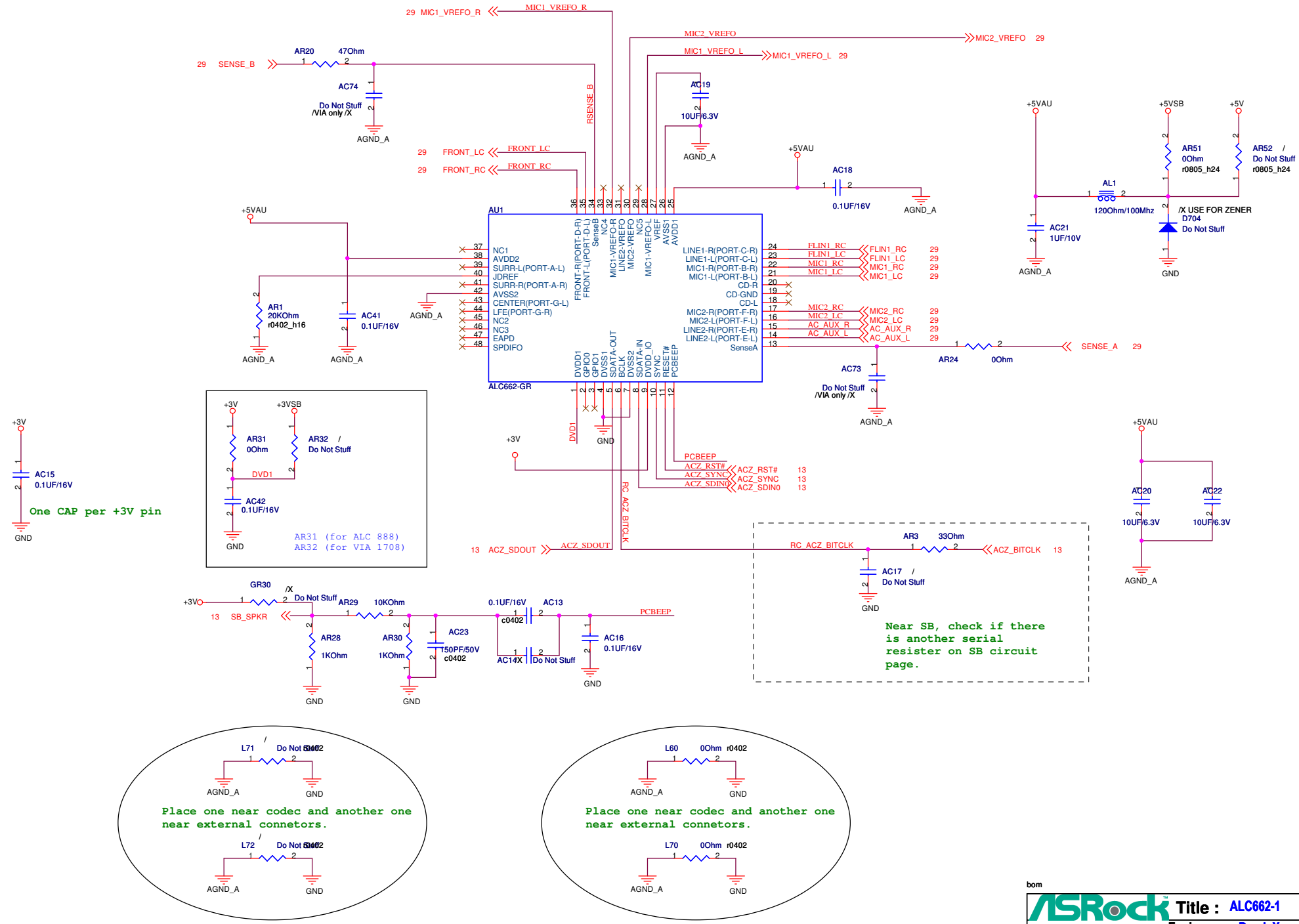
ASRock Inc.

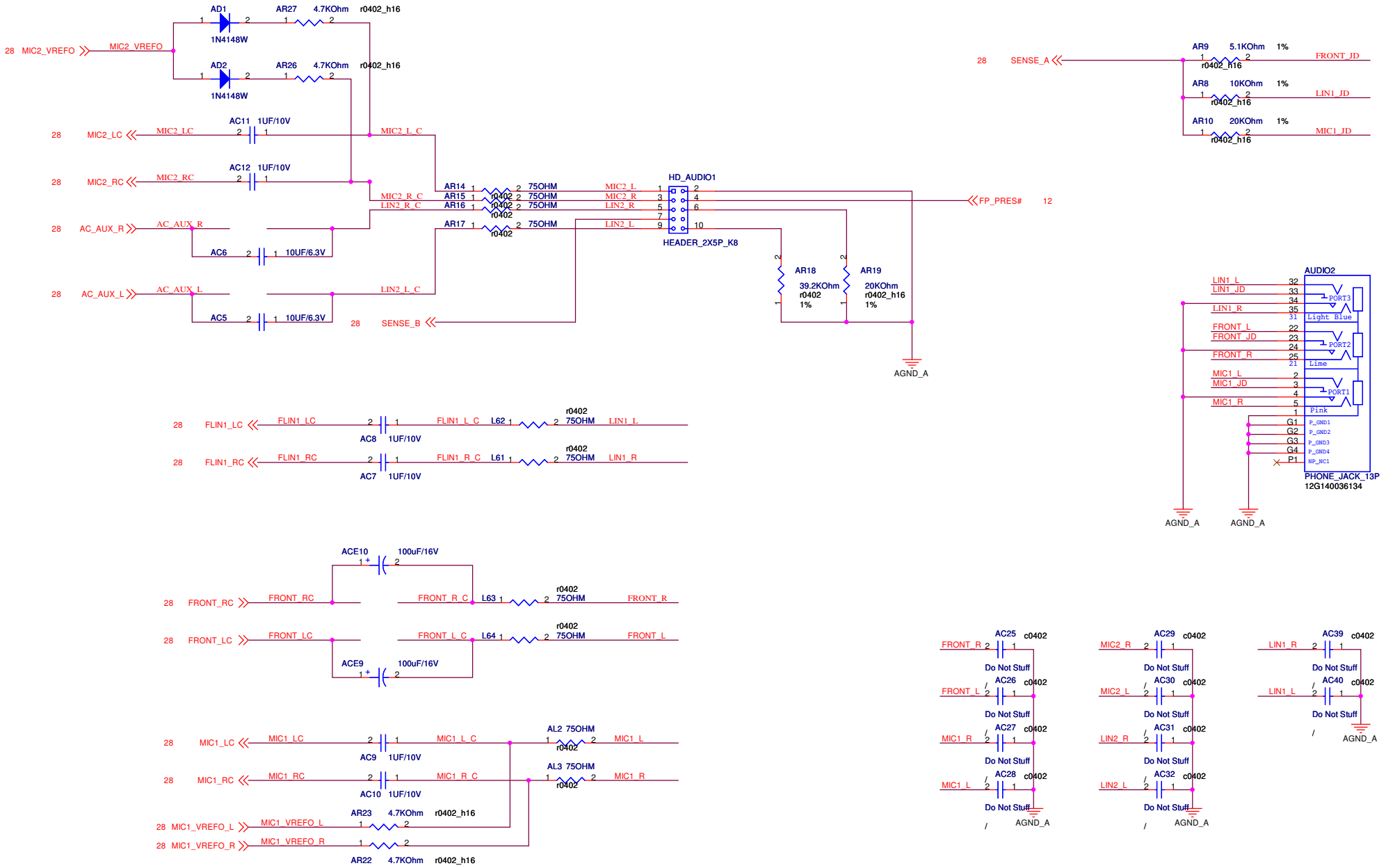
Title : PCIex1

Engineer: Chia-Wei Chang

Size	Project Name	Rev
Custom	H61M-HVS	1.00

Date: Tuesday, May 07, 2013 Sheet 27 of 41


AU1
ALC662-GR
NC1
AVDD2
SURR-L(PORT-A-L)
JDREF
SURR-R(PORT-A-R)
AVSS2
CENTER(PORT-G-L)
LFE(PORT-G-R)
NC2
NC3
EAPD
SPDIFO
FRONT-R(PORT-D-R)
FRONT-L(PORT-D-L)
SenseB
NC4
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
NC5
MIC1-VREFO-L
VREF
AVSS1
AVDD1
LINE1-R(PORT-C-R)
LINE1-L(PORT-C-L)
MIC1-R(PORT-B-R)
MIC1-L(PORT-B-L)
CD-R
CD-GND
CD-L
MIC2-R(PORT-F-R)
MIC2-L(PORT-F-L)
LINE2-R(PORT-E-R)
LINE2-L(PORT-E-L)
SenseA
DVDD1
GPDO
GPDI
DVSS1
SDATA-OUT
BCLK
DVSS2
SDATA-IN
DVDD_IO
SYNC
RESET#
PCBEEP
MIC1_VREFO_R
MIC2_VREFO
MIC1_VREFO_L
RSENSE_B
FRONT_LC
FRONT_RC
FLIN1_RC
FLIN1_LC
MIC1_RC
MIC1_LC
MIC2_RC
MIC2_LC
AC_AUX_R
AC_AUX_L
SENSE_A
ACZ_RST#
ACZ_SYNC
ACZ_SDIN0
ACZ_SDOUT
RC_ACZ_BITCLK
ACZ_BITCLK
AR1 20KOhm r0402_h16
AC41 0.1UF/16V
AC74 Do Not Stuff /VIA only /X
AC19 10UF/6.3V
AC18 0.1UF/16V
AC73 Do Not Stuff /VIA only /X
AR24 0Ohm
AR20 47Ohm
AL1 120Ohm/100Mhz
AR51 0Ohm r0805_h24
AR52 / Do Not Stuff r0805_h24
/X USE FOR ZENER D704 Do Not Stuff
AC21 1UF/10V
AC15 0.1UF/16V
One CAP per +3V pin
AR31 0Ohm
AR32 / Do Not Stuff
AC42 0.1UF/16V
AR31 (for ALC 888)
AR32 (for VIA 1708)
AC20 10UF/6.3V
AC22 10UF/6.3V
AR3 33Ohm
AC17 / Do Not Stuff
Near SB, check if there is another serial resister on SB circuit page.
GR30 /X Do Not Stuff
AR29 10KOhm
AR28 1KOhm
AR30 1KOhm
AC23 150PF/50V c0402
AC13 0.1UF/16V c0402
AC14X Do Not Stuff
AC16 0.1UF/16V
SB_SPKR
L71 / Do Not Stuff 0402
L72 / Do Not Stuff 0402
Place one near codec and another one near external connetors.
L60 0Ohm r0402
L70 0Ohm r0402
Place one near codec and another one near external connetors.
bom
ASRock Inc.
Title : ALC662-1
Engineer: Derek Y
Size A3
Project Name 847PV3
Rev 1.00
Date: Tuesday, May 07, 2013
Sheet 28 of 41



bom

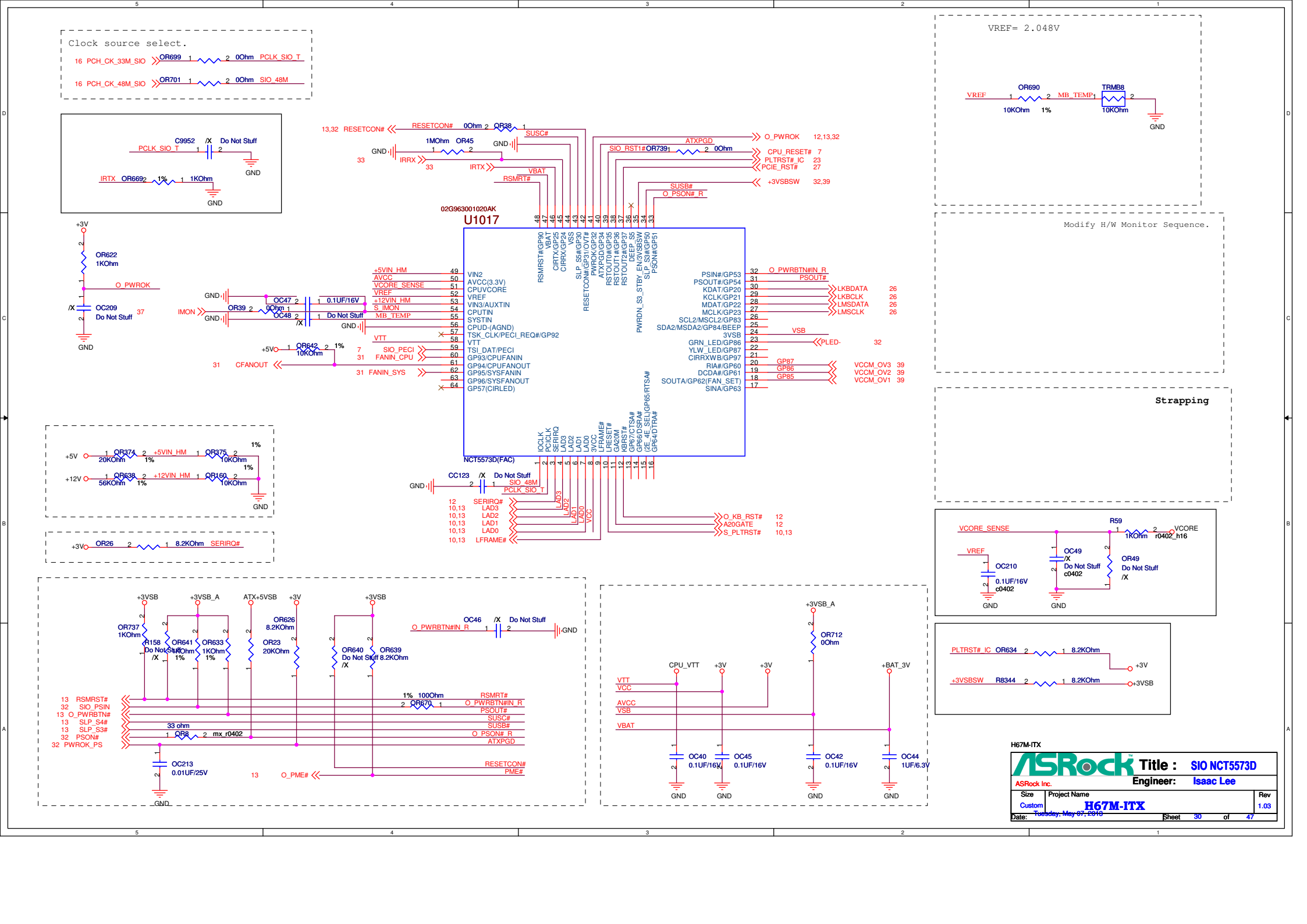
ASRock Inc.

Title : ALC662-2

Engineer: Derek Y

Size	Project Name	Rev
A3	847PV3	1.00

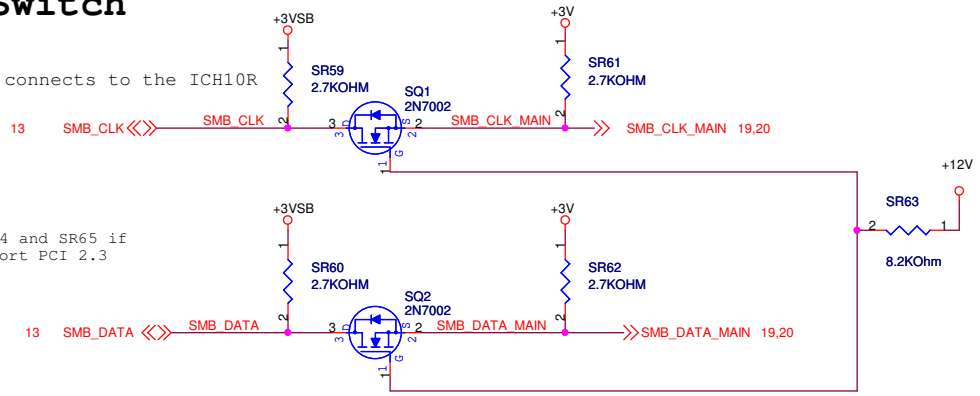
Date: Tuesday, May 07, 2013 Sheet 29 of 41


Clock source select.
16 PCH_CK_33M_SIO
OR699 1 2 0Ohm PCLK_SIO_T
16 PCH_CK_48M_SIO
OR701 1 2 0Ohm SIO_48M
C9952 /X Do Not Stuff
PCLK_SIO_T
IRTX OR669 2 1% 1 1KOhm
GND
VREF= 2.048V
VREF
OR690
MB_TEMP
TRMB8
10KOhm 1%
10KOhm
Modify H/W Monitor Sequence.
Strapping
02G963001020AK
U1017
NCT5573D(FAC)
13,32 RESETCON#
RESETCON# 0Ohm OR38
SUSC#
1MOhm OR45
IRRX
IRTX
VBAT
RSMRT#
ATXPGD
SIO_RST1# OR739 0Ohm
O_PWROK 12,13,32
CPU_RESET# 7
PLTRST#_IC 23
PCIE_RST# 27
+3VSBSW 32,39
SUSB#
O_PSON#_R
+3V
OR622 1KOhm
O_PWROK
/X OC209 Do Not Stuff 37
IMON
OR39 0Ohm
OC47 0.1UF/16V
OC48 /X Do Not Stuff
MB_TEMP
+5VIN_HM
VCORE_SENSE
VREF
+12VIN_HM
S_IMON
VTT
SIO_PECI 7
FANIN_CPU 31
CFANOUT 31
FANIN_SYS 31
+5V OR642 10KOhm 1%
VIN2
AVCC
AVCC(3.3V)
CPUVCORE
VREF
VIN3/AUXTIN
CPUTIN
SYSTIN
CPUD-(AGND)
TSK_CLK/PECI_REQ#/GP92
VTT
TSI_DAT/PECI
GP93/CPUFANIN
GP94/CPUFANOUT
GP95/SYSFANIN
GP96/SYSFANOUT
GP57(CIRLED)
PSIN#/GP53
PSOUT#/GP54
KDAT/GP20
KCLK/GP21
MDAT/GP22
MCLK/GP23
SCL2/MSCL2/GP83
SDA2/MSDA2/GP84/BEEP
3VSB
GRN_LED/GP86
YLW_LED/GP87
CIRRXWB/GP97
RIA#/GP60
DCDA#/GP61
SOUTA/GP62(FAN_SET)
SINA/GP63
O_PWRBTN#IN_R
PSOUT#
LKBDATA 26
LKBCLK 26
LMSDATA 26
LMSCLK 26
VSB
PLED- 32
GP87
GP86
GP85
VCCM_OV3 39
VCCM_OV2 39
VCCM_OV1 39
RSMRST#/GP90
VBAT
CIRTX/GP25
CIRRX/GP24
VSS
SLP_S5#/GP30
PWROK/GP32
ATXPGD/GP34
RSTOUT0#/GP35
RSTOUT1#/GP36
RSTOUT2#/GP37
DEEP_S5
PWRDN_S3_STBY_EN/3VSBSW
SLP_S3#/GP50
PSON#/GP51
IOCLK
PCICLK
SERIRQ
LAD3
LAD2
LAD1
LAD0
3VCC
LFRAME#
LRESET#
GA20M
KBRST#
GP67/CTSA#
GP66/DSRA#
(2E_4E_SEL)GP65/RTSA#
GP64/DTRA#
CC123 /X Do Not Stuff
SIO_48M
PCLK_SIO_T
12 SERIRQ#
10,13 LAD3
10,13 LAD2
10,13 LAD1
10,13 LAD0
10,13 LFRAME#
O_KB_RST# 12
A20GATE 12
S_PLTRST# 10,13
+5V OR374 20KOhm 1% +5VIN_HM OR375 10KOhm 1%
+12V OR638 56KOhm 1% +12VIN_HM OR160 10KOhm 1%
+3V OR26 8.2KOhm SERIRQ#
VCORE_SENSE
VREF
OC210 0.1UF/16V c0402
R59 1KOhm r0402_h16 VCORE
OC49 /X Do Not Stuff c0402
OR49 Do Not Stuff /X
PLTRST#_IC OR634 8.2KOhm +3V
+3VSBSW R8344 8.2KOhm +3VSB
+3VSB
+3VSB_A
ATX+5VSB
+3V
OR737 1KOhm
R158 Do Not Stuff /X
OR641 1% OR633 1KOhm 1%
OR626 8.2KOhm
OR23 20KOhm
OR640 Do Not Stuff /X
OR639 8.2KOhm
OC46 /X Do Not Stuff
O_PWRBTN#IN_R
13 RSMRST#
32 SIO_PSIN
13 O_PWRBTN#
13 SLP_S4#
13 SLP_S3#
32 PSON#
32 PWROK_PS
33 ohm
OR8 mx_r0402
1% 100Ohm OR670
RSMRT#
O_PWRBTN#IN_R
PSOUT#
SUSC#
SUSB#
O_PSON#_R
ATXPGD
RESETCON#
PME#
OC213 0.01UF/25V
13 O_PME#
+3VSB_A
OR712 0Ohm
CPU_VTT
+3V
+3V
+BAT_3V
VTT
VCC
AVCC
VSB
VBAT
OC40 0.1UF/16V
OC45 0.1UF/16V
OC42 0.1UF/16V
OC44 1UF/6.3V
GND
H67M-ITX
ASRock
Title : SIO NCT5573D
ASRock Inc.
Engineer: Isaac Lee
Size Custom
Project Name H67M-ITX
Rev 1.03
Date: Tuesday, May 07, 2013
Sheet 30 of 47

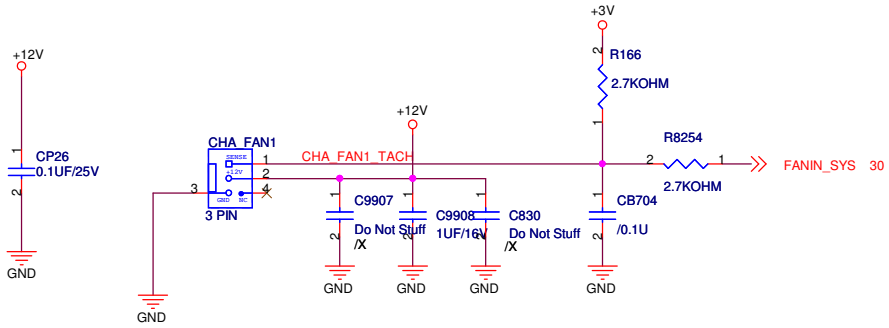
1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.
SMB_CLK and SMB_DATA for Standby device.
SMB_CLK_MAIN and SMB_DATA_MAIN for Main power device.

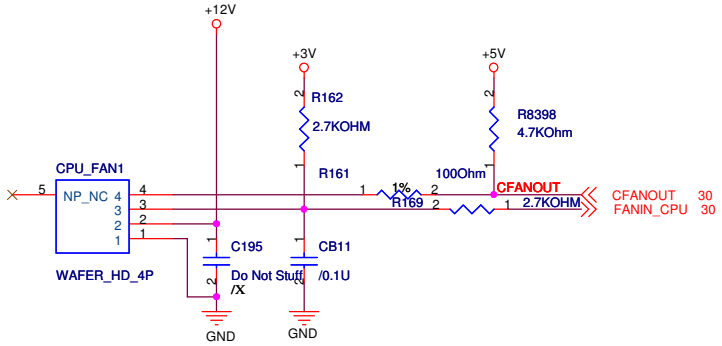
SMBus Switch

SMB_CLK and SMB_DATA connects to the ICH10R



SMB_CLK_PCI and SMB_DATA_PCI connects to the PCIE slot





H67M-ITX

ASRock Inc.

Title : SMBUS SWITCH,FAN

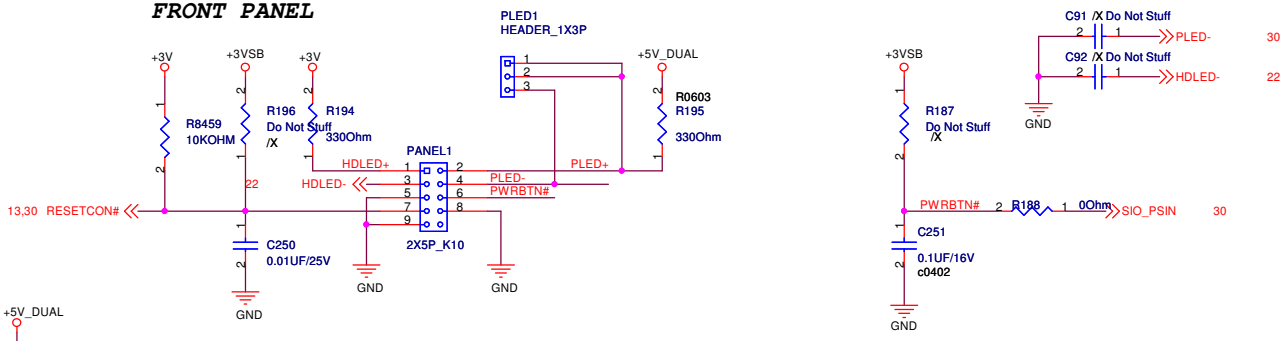
Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

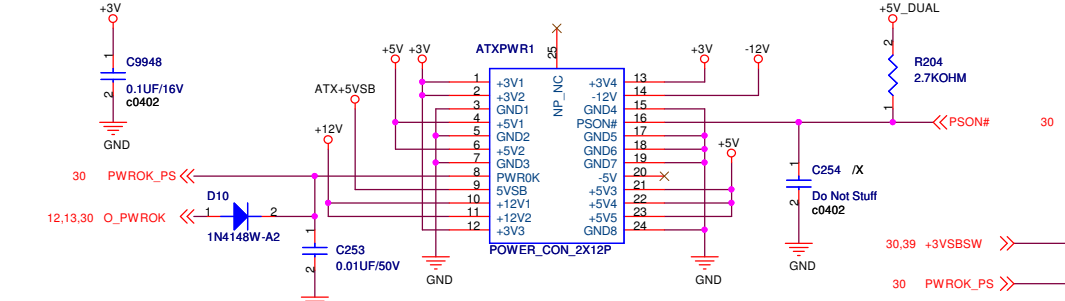
Date: Tuesday, May 07, 2013 Sheet 31 of 47

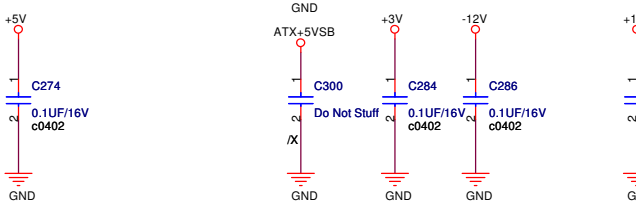
RING_IN

FRONT PANEL



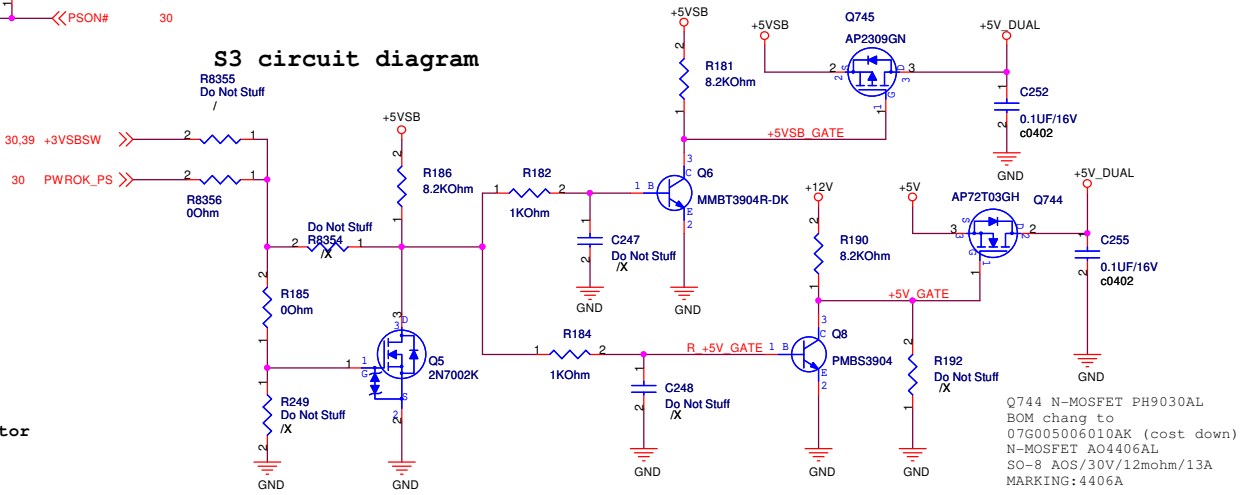
ATXPWR CONN





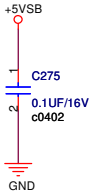
*Around the ATX Power Connector

S3 circuit diagram



Q744 N-MOSFET PH9030AL
BOM chang to
07G005006010AK (cost down)
N-MOSFET AO4406AL
SO-8 AOS/30V/12mohm/13A
MARKING:4406A

Logic IC : R190 = 2.7K, Q8 = 2N7002
BJT : R190 = 8.2K, Q8 = 3904, R192
= uninstall

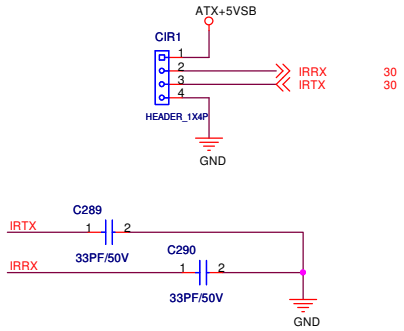


bom

ASRock Inc.	Title : POK_DUALSW_ENASUS	
	Engineer: Isaac Lee	
Size: A3	Project Name: H67M-ITX	Rev: 1.03
Date: Tuesday, May 07, 2013	Sheet 32 of 41	

COM

IR

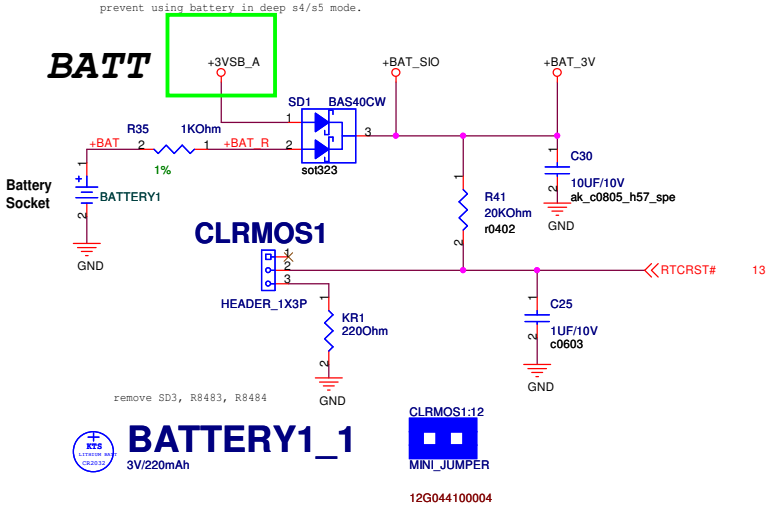


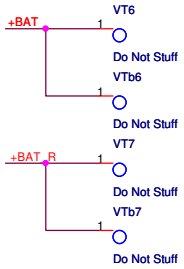
Wifi

prevent using battery in deep s4/s5 mode.

prevent using battery in deep s4/s5 mode.

BATT





H67M-ITX

ASRock Inc.

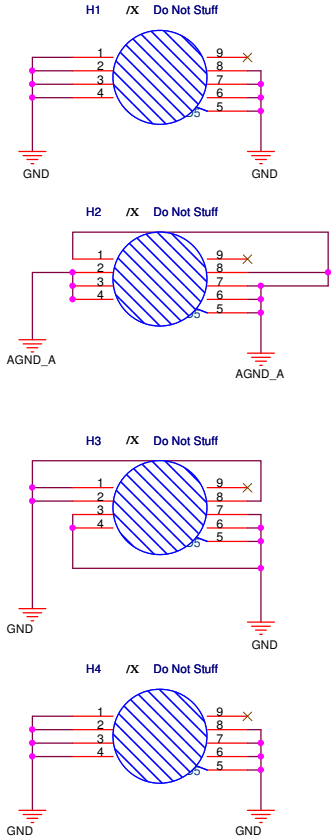
Title : IO CONNECTOR

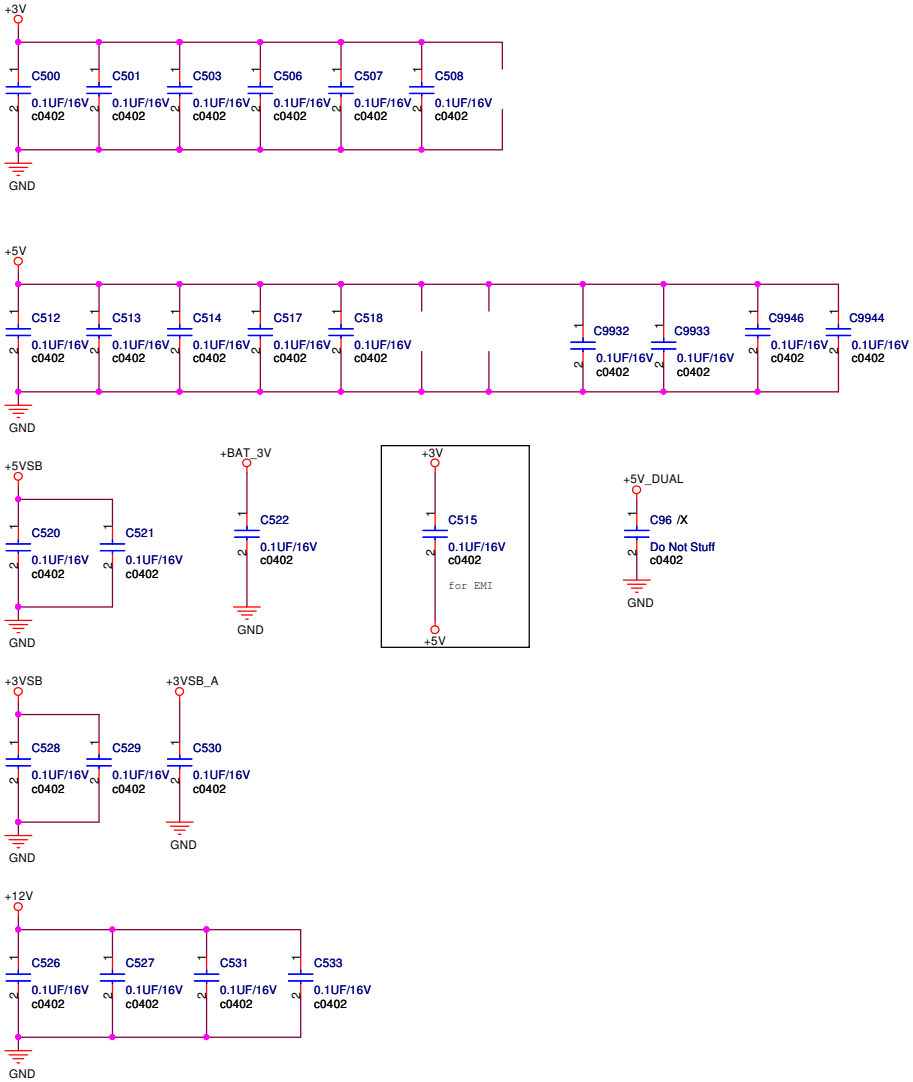
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 33 of 47

SCREW_HOLE





H67M-ITX

ASRock Inc.

Title : MECHANICAL

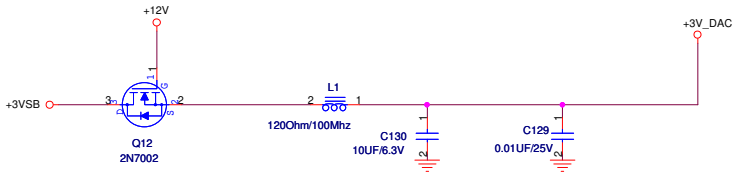
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

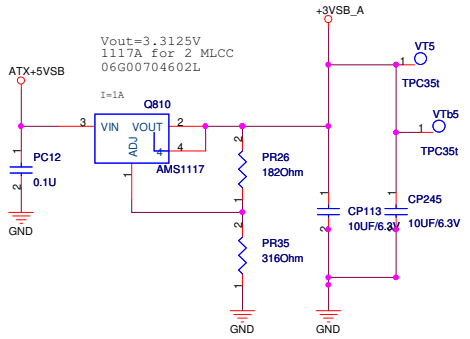
Date: Wednesday, December 19, 2012 Sheet 34 of 47

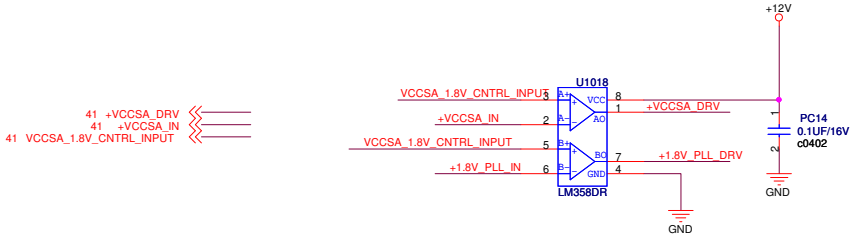
Soft Start - PCH

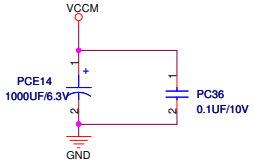
+3.3V_DAC



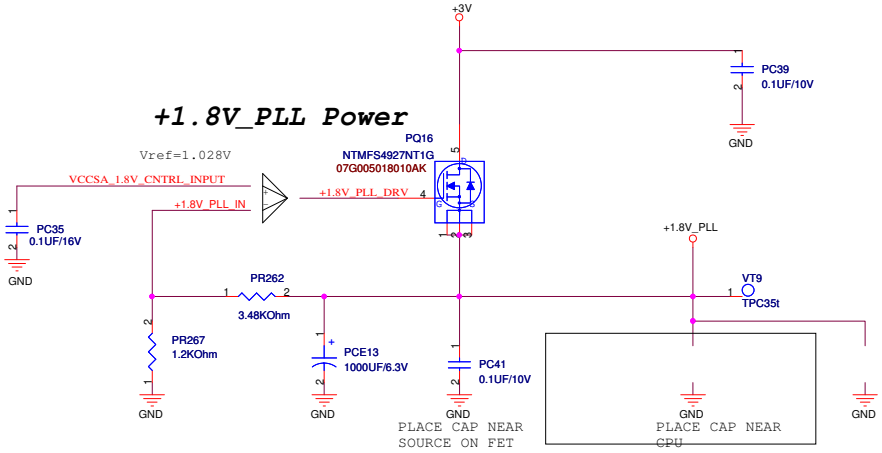
+3VSB_A

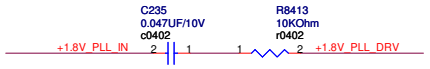






+1.8V_PLL Power





bom

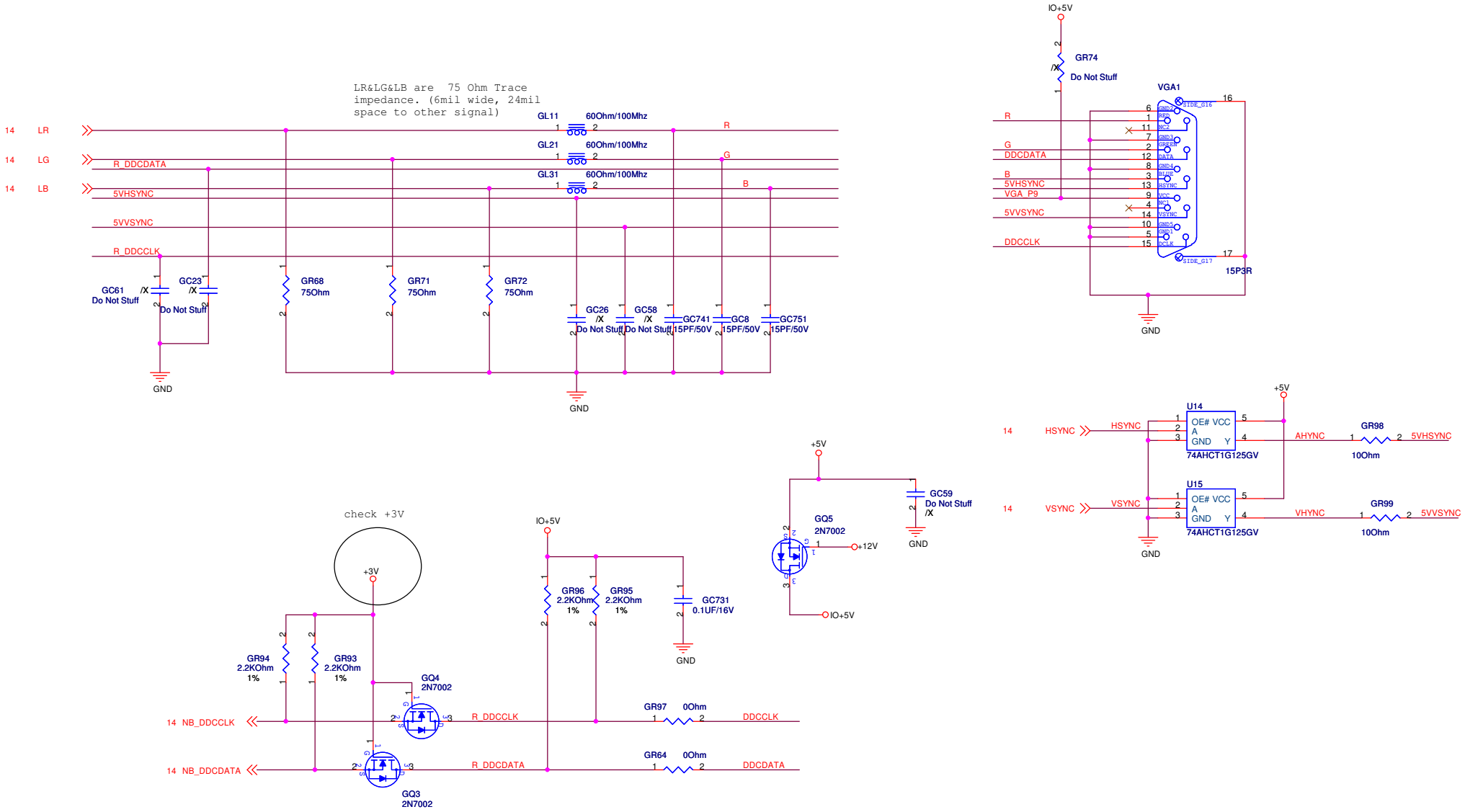
ASRock Inc.

Title : DC_DC

Engineer: Isaac Lee

Size	Project Name	Rev
Custom	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 35 of 41



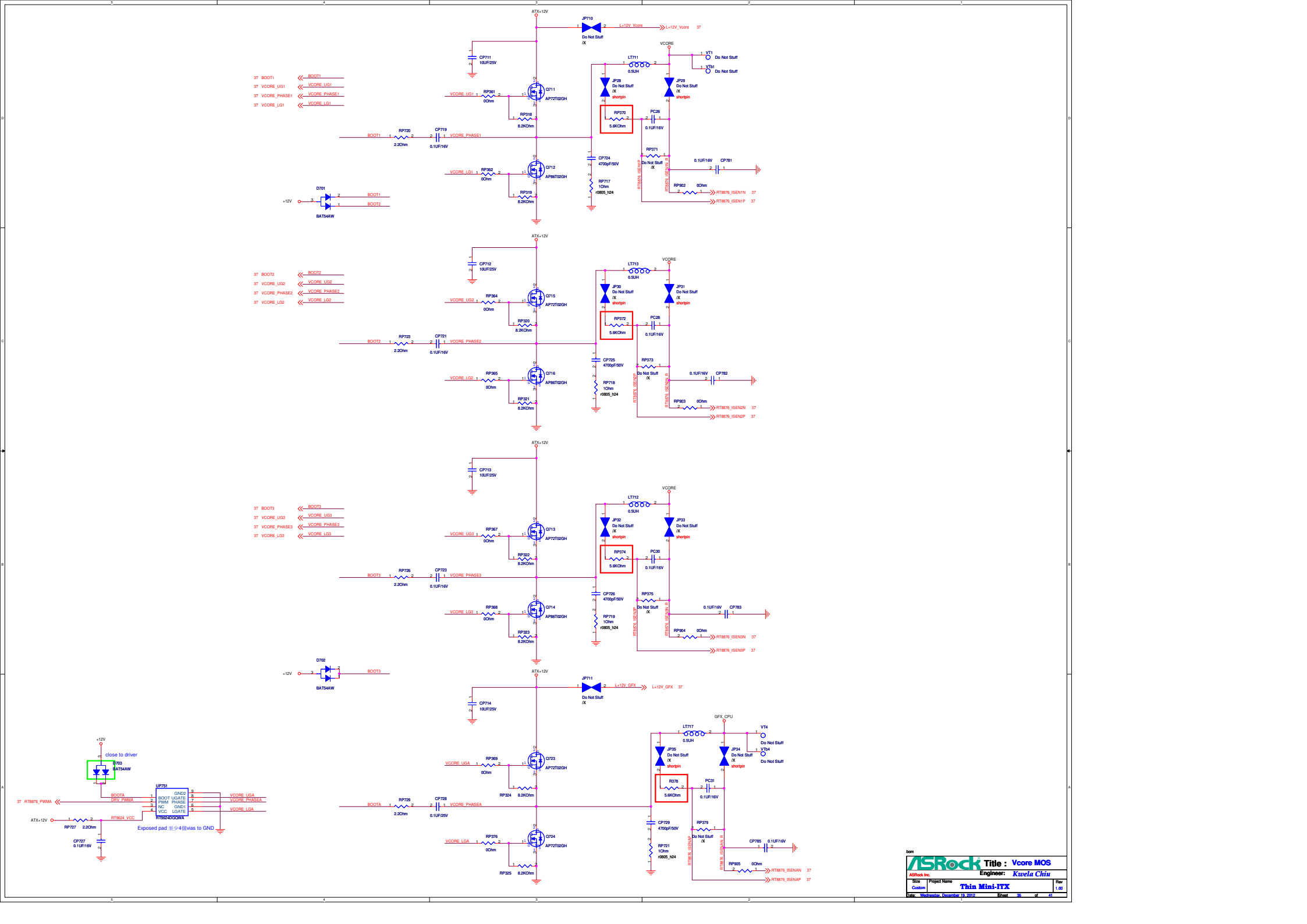
H67M-ITX

ASRock Title : VGA CONNECTOR

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 35 of 47



bom

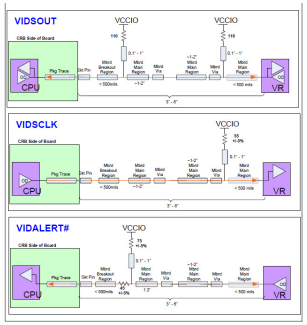
ASRock Inc.

Title : Vcore MOS

Engineer: Kwela Chiu

Size	Project Name	Rev
Custom	Thin Mini-ITX	1.00

Date: Wednesday, December 19, 2012 Sheet 36 of 41



bom use 10G212180314010
RES 180K OHM 1/16W (0402) 1%

bom use 10G212300314010
RES 300K OHM 1/16W (0402) 1%

bom use 10G212133314010
RES 133K OHM 1/16W (0402) 1%

ICCMAX : 80A*19.6mV=1.568V

bom use 10G212240314010
RES 240K OHM 1/16W (0402) 1%

bom use 10G212270314010
RES 270K OHM 1/16W (0402) 1%

VGT: 50A OCP setting
48*50A*1.05m=2.52V

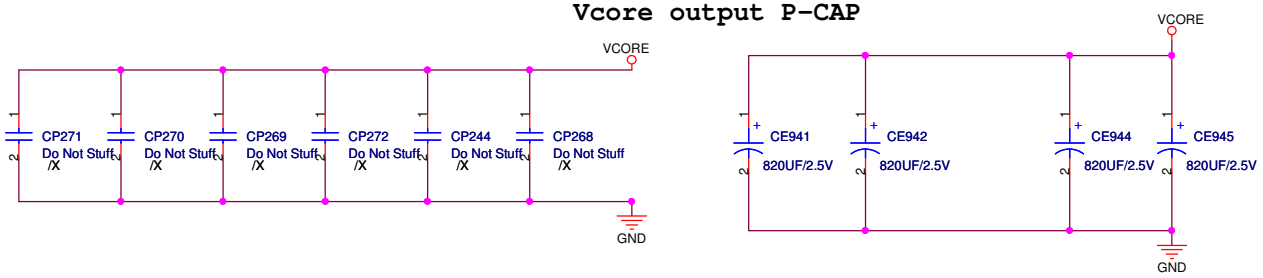
Vcore: 40A OCP setting/per phase
48*40A*1.05m=2.01V

1.77m ohm=10" 1.05m*15k/R

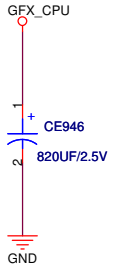
3.81m ohm=20" 1.05m*15k/R

bom			
ASRock Inc.	Title : PWM RT8859		
	Engineer: Kwela Chiu		
Size: Custom	Project Name: Thin Mini-ITX		Rev: 1.00
Date: Tuesday, May 07, 2013	Sheet 37 of 41		

Vcore output P-CAP

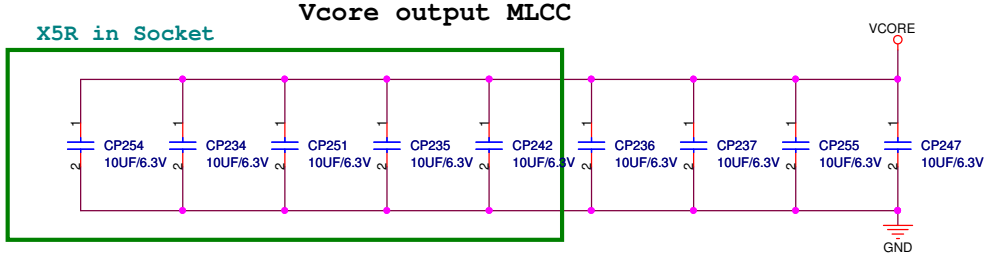


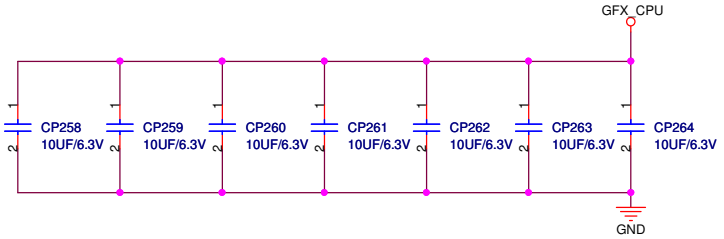
GFX output P-CAP

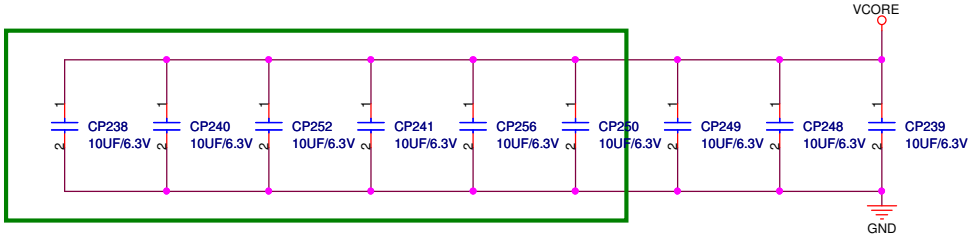


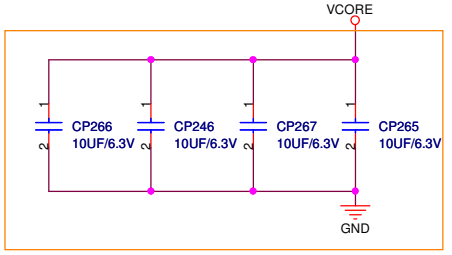
Vcore output MLCC

X5R in Socket



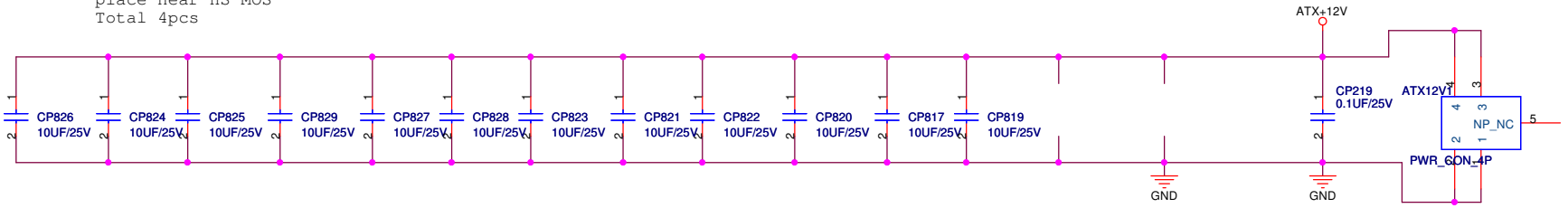






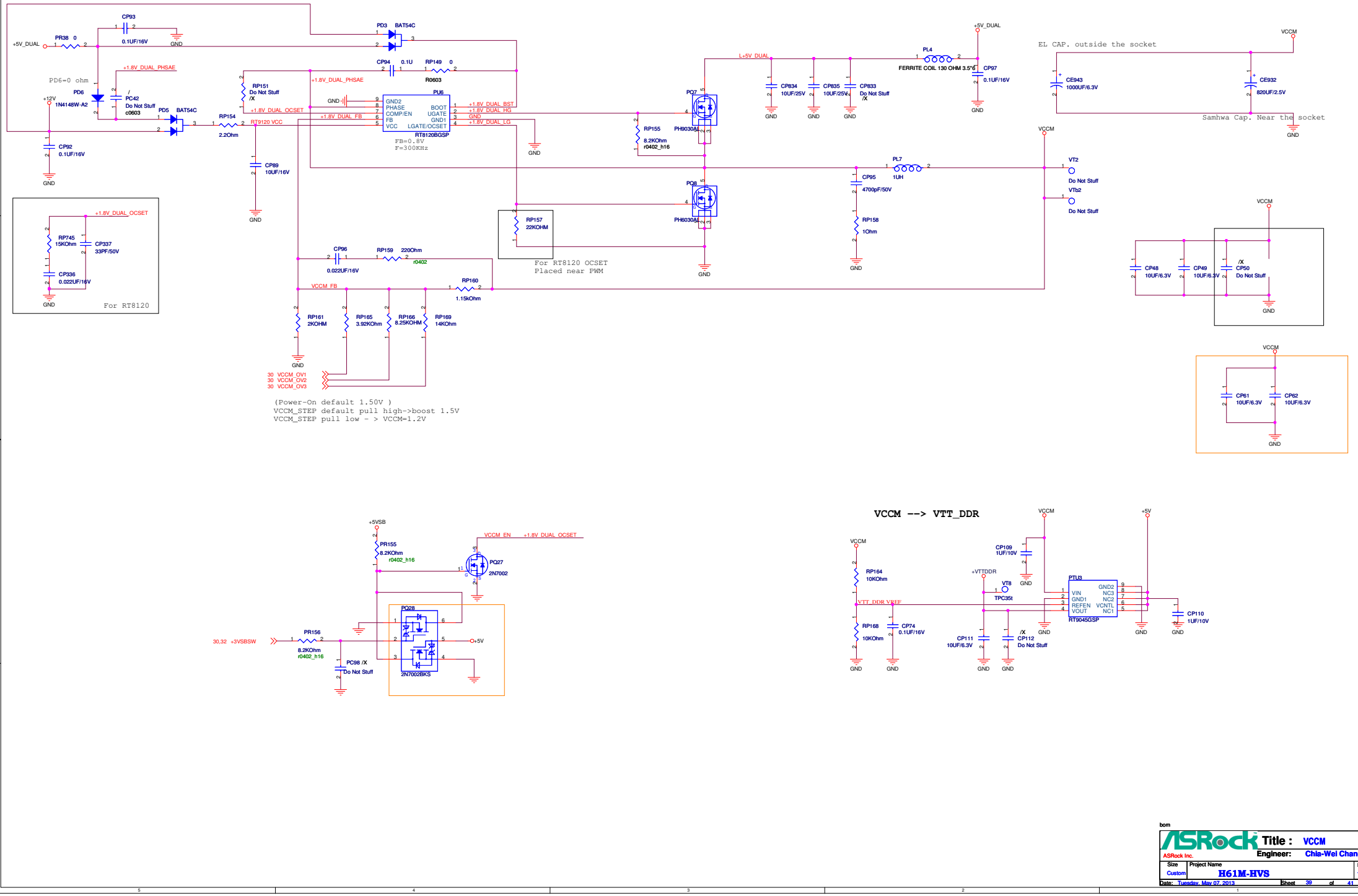
Vcore Input P-CAP

place near HS MOS
Total 4pcs



bom

ASRock Inc.	Title : VCORE	
	Engineer: Isaac Lee	
Size: B	Project Name: H67M-ITX	Rev: 1.03
Date: Tuesday, May 07, 2013	Sheet 38 of 41	



bom

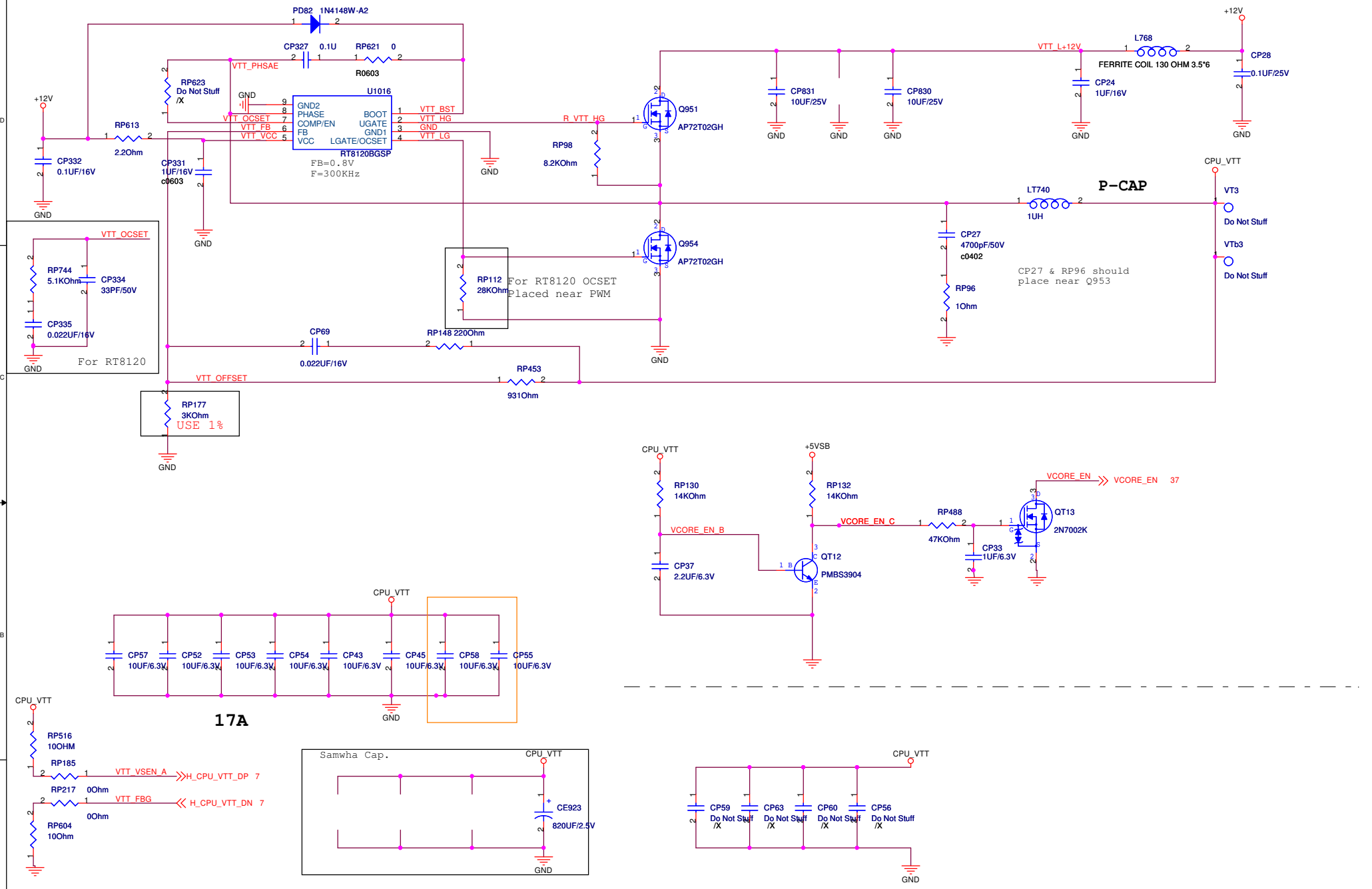
ASRock Inc.

Title : VCCM

Engineer: Chia-Wei Chang

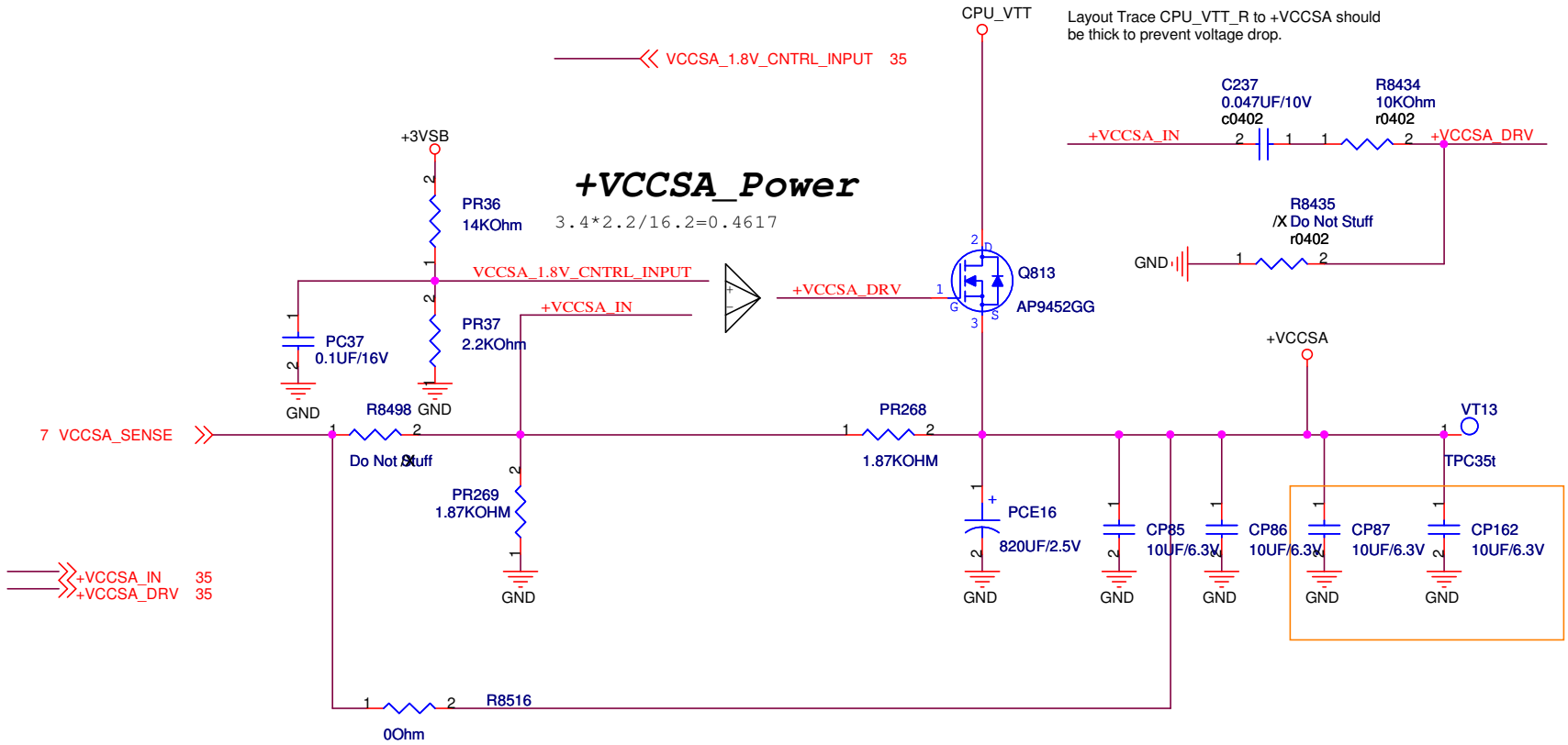
Size	Project Name	Rev
Custom	H61M-HVS	1.00

Date: Tuesday, May 07, 2013 Sheet 39 of 41



bom

ASRock Inc.	Title : VTT	
	Engineer: Chia-Wei Chang	
Size: A3	Project Name: H61M-HVS	Rev: 1.00
Date: Tuesday, May 07, 2013	Sheet 40 of 41	



bom

ASRock Inc.	Title : VTT	
	Engineer: Chia-Wei Chang	
Size: Custom	Project Name: H61M-HVS	Rev: 1.00
Date: Wednesday, December 19, 2012	Sheet 41 of 41	