PAGE	TITLE	Quantity
01	COVER PAGE	
02	BLOCK DIAGRAM	
03	CPU (PCIE/DMI)	
04	CPU (DDI/EDP)	
05	CPU (DDR)	
06	CPU (SVID/CFG/JTAG/CLK)	
07	CPU (VCORE/VCCGT)	
08	CPU (CCSA/VCCIO/VDDQ/RSVD)	
09	CPU (VSS)	
10	CPU (Power CAP)	
11	CPU (Power Cap2)	
12	DDR (DDR4-CHA)	
13	DDR (DDR4-CHB)	
14	DDR (RSVD) (DDR4-CHA1)	
15	PCH (SPI/UART/I2C)	
16	PCH (DMI/PCI-E/USB)DDI GP	
17	PCH (PCI-E/SATA)	
18	PCH (CLOCK/CL)	
19	PCH (USB/ESPI)	
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)	
21	PCH (POWER1)	
22	PCH (POWER2) PCH Strap	
23	PCH Power CAP	
24	ECIO (ITE8732F_CX)	
25	Flash&RTC	
26	INT IO (Thermal/FAN)	
27	AUDIO (RSVD) (ALC286)	
28	Audio (RSVD) (AMP)	
29	Audio (RSVD HP/SPK/MICJack)	
30	Audio (RSVD)	
31	LAN (RTL8111GA)	
32	RJ45&Transformer (R)	
33	Card reader (R)	
34	USB3 Redriver(PI3EQX1012C)	
35	USB (RSVD)	
36	USB (USB Power Switch)	
37	USB (HEADER CAM/TOUCH)	
38	USB (USB30 PORT)	
39	Sequence (RSVD)	
40	Sequence (Power Plane EN)	
41	Sequence (Power5V&3.3V)	
42	INT IO (RSVD)	
43	INT IO (DCIN JACK)	
44	Power (OZ554 LED Converter)	
45	Power (5V/3D3V RT6575D)	
46	Power (NCP81203 CPUCORE1/1)	
47	Power (NCP1151 CPUCORE1/2)	
48	Power (NCP81151 CPUVGT1/3)	
49	Power (NCP1589A DCDC12V)	
50	Power (RT8231A VDDQ/VTT)	
51	Power (RT8237C_PCH1P0V)	
52	Power (RT8237C VCC SA)	
53	Power (RT8237C VCC IO)	
54	Power (LDO 1P5V 2P5V)	

PAGE	TITLE	Quantity
55	LVDS Connector	
56	HDMI IN	
57	HDMI OUT	
58	DVI/CRT (R)	
59	Display switch (R)	
60	HDD/ODD	
61	Mini PCIE Card TV Tuner (R)	
62	WLAN and BT--NGFF	
63	SSD-NGFF	
64	PWR BT/Side Key/LED	
65	Stand off&EMI Cap&DUMMY BOM	
66	IO Board	
67	COM (R)	
68	Debug	
69	LPT (R)	
70	G sensor (R)	
71	Thunderbolt (R)	
72	Thunderbolt (R)	
73	Thunderbolt (R)	
74	Thunderbolt (R)	
75	Thunderbolt (R)	
76	GPU (1/5): PEG	
77	GPU (2/5): DIGITALOUT	
78	GPU (3/5): VRAM I/F	
79	GPU (4/5): GPIO/STRAP	
80	GPU (5/5): PWR/GND	
81	VRAM1 (1/2)	
82	VRAM2 (3/4)	
83	VRAM3 (5/6)	
84	VRAM4 (7/8)	
85	GPU CORE NVVDD(RT8812AGQW)	
86	DISCRETE VGA POWER	
87	GPU Switch (R)	
88	GPU Switch (R)	
89	GPU others (R)	
90	NFC (R)	
91	TPM (R)	
92	PS2 (R)	
93	Express Card (R)	
94	Smart Card (R)	
95	Scalar-RTD2506S	
96	Scalar Power	
97	Inter LAN (R)	
98	LAN Switch (R)	
99	XDP&ITP	
100	Table of Content	
101	GPIO table	
102	POWER SEQUENCE	
103	Power Block Diagram	
104	SMBUS table	
105	CLOCK MAP	
106	RESET Flow CHART	
107	Change History	

Model: AIO, Petra238i
SCH Ver: 1A
PCB Ver:1A
PCB NumSAber:17567
PCB P/N:
3PD0BD010001

PCB BOARD SIZE
6 Layers
237mmX182mm

BOM Configuration
Unmount : (R_)
GPU:(G_)
(N17S_)
(N16S_)
NonGPU : (U_)
Hynix VRAM:(H_)
MICRON VRAM:(M_)
CPU 62 :(S62_)
NONS62:(NONS62_)
Modern Standby :
(MS_)
(NONMS_)
Modern Standby Test:
(MST_)

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: COVER PAGE

Size	Document Number	Rev
C	Consumer AIO Petra238i	1A

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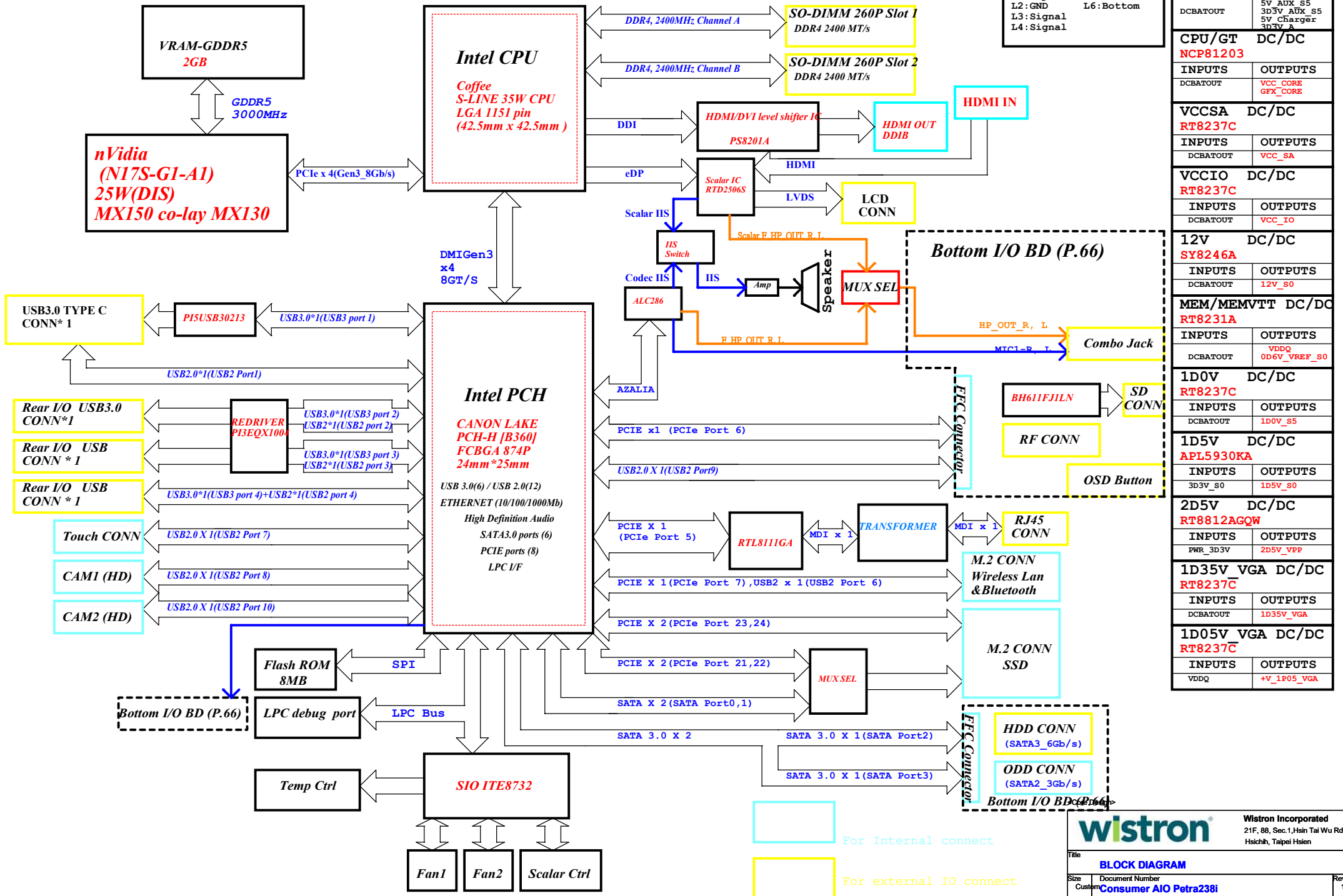
Petra238i Block Diagram (GPU)



PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Bottom
L3:Signal	
L4:Signal	

5V/3D3V DC/DC
RT6575D

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A

CPU/GT DC/DC
NCP81203

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE GFX_CORE

VCCSA DC/DC
RT8237C

INPUTS	OUTPUTS
DCBATOUT	VCC_SA

VCCIO DC/DC
RT8237C

INPUTS	OUTPUTS
DCBATOUT	VCC_IO

12V DC/DC
SY8246A

INPUTS	OUTPUTS
DCBATOUT	12V_S0

MEM/MEMVTT DC/DC
RT8231A

INPUTS	OUTPUTS
DCBATOUT	VDDQ 0D6V_VREF_S0

1D0V DC/DC
RT8237C

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

1D5V DC/DC
APL5930KA

INPUTS	OUTPUTS
3D3V_S0	1D5V_S0

2D5V DC/DC
RT8812AGQW

INPUTS	OUTPUTS
PWR_3D3V	2D5V_VPP

1D35V_VGA DC/DC
RT8237C

INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA

1D05V_VGA DC/DC
RT8237C

INPUTS	OUTPUTS
VDDQ	+V_1P05_VGA

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: BLOCK DIAGRAM

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76 PEG_RXP3
76 PEG_RXN3
76 PEG_RXP2
76 PEG_RXN2
76 PEG_RXP1
76 PEG_RXN1
76 PEG_RXP0
76 PEG_RXN0
76 PEG_C_TXP3
76 PEG_C_TXN3
76 PEG_C_TXP2
76 PEG_C_TXN2
76 PEG_C_TXP1
76 PEG_C_TXN1
76 PEG_C_TXP0
76 PEG_C_TXN0

DMI
16 DMI_IT_MR_DP[0..3]
16 DMI_IT_MR_DN[0..3]
16 DMI_MT_IR_DP[0..3]
16 DMI_MT_IR_DN[0..3]

CPU1C 3 OF 12
Lake-S

B8	PEG_RXP_0	PEG_TXP_0	A5
B7	PEG_RXN_0	PEG_TXN_0	A6
C7	PEG_RXP_1	PEG_TXP_1	B4
C6	PEG_RXN_1	PEG_TXN_1	B5
D6	PEG_RXP_2	PEG_TXP_2	C3
D5	PEG_RXN_2	PEG_TXN_2	C4
E5	PEG_RXP_3	PEG_TXP_3	D2
E4	PEG_RXN_3	PEG_TXN_3	D3
F6	PEG_RXP_4	PEG_TXP_4	E1
F5	PEG_RXN_4	PEG_TXN_4	E2
G5	PEG_RXP_5	PEG_TXP_5	F2
G4	PEG_RXN_5	PEG_TXN_5	F3
H6	PEG_RXP_6	PEG_TXP_6	G1
H5	PEG_RXN_6	PEG_TXN_6	G2
J5	PEG_RXP_7	PEG_TXP_7	H2
J4	PEG_RXN_7	PEG_TXN_7	H3
K6	PEG_RXP_8	PEG_TXP_8	J1
K5	PEG_RXN_8	PEG_TXN_8	J2
L5	PEG_RXP_9	PEG_TXP_9	K2
L4	PEG_RXN_9	PEG_TXN_9	K3
M6	PEG_RXP_10	PEG_TXP_10	L1
M5	PEG_RXN_10	PEG_TXN_10	L2
N5	PEG_RXP_11	PEG_TXP_11	M2
N4	PEG_RXN_11	PEG_TXN_11	M3
P6	PEG_RXP_12	PEG_TXP_12	N1
P5	PEG_RXN_12	PEG_TXN_12	N2
R5	PEG_RXP_13	PEG_TXP_13	P2
R4	PEG_RXN_13	PEG_TXN_13	P3
T6	PEG_RXP_14	PEG_TXP_14	R2
T5	PEG_RXN_14	PEG_TXN_14	R1
U5	PEG_RXP_15	PEG_TXP_15	T2
U4	PEG_RXN_15	PEG_TXN_15	T3
L7	PEG_RCOMP		

PEG_RXP3 PEG_RXN3 — PEG_TXP3 PEG_TXN3 — C301 C302 SCD22U10V2KX-1GP — PEG_C_TXP3 PEG_C_TXN3
PEG_RXP2 PEG_RXN2 — PEG_TXP2 PEG_TXN2 — C303 C304 SCD22U10V2KX-1GP — PEG_C_TXP2 PEG_C_TXN2
PEG_RXP1 PEG_RXN1 — PEG_TXP1 PEG_TXN1 — C305 C306 SCD22U10V2KX-1GP — PEG_C_TXP1 PEG_C_TXN1
PEG_RXP0 PEG_RXN0 — PEG_TXP0 PEG_TXN0 — C308 C307 SCD22U10V2KX-1GP — PEG_C_TXP0 PEG_C_TXN0

VCC_IO
R302
24D9R2F-L-GP
PEG_RCOMP_CPU

DMI_IT_MR_DP0	Y3	DMI_RXP_0	DMI_TXP_0 AC2 — DMI_MT_IR_DP0
DMI_IT_MR_DN0	Y4	DMI_RXN_0	DMI_TXN_0 AC1 — DMI_MT_IR_DN0
DMI_IT_MR_DP1	AA4	DMI_RXP_1	DMI_TXP_1 AD3 — DMI_MT_IR_DP1
DMI_IT_MR_DN1	AA5	DMI_RXN_1	DMI_TXN_1 AD2 — DMI_MT_IR_DN1
DMI_IT_MR_DP2	AB4	DMI_RXP_2	DMI_TXP_2 AE2 — DMI_MT_IR_DP2
DMI_IT_MR_DN2	AB3	DMI_RXN_2	DMI_TXN_2 AE1 — DMI_MT_IR_DN2
DMI_IT_MR_DP3	AC4	DMI_RXP_3	DMI_TXP_3 AF2 — DMI_MT_IR_DP3
DMI_IT_MR_DN3	AC5	DMI_RXN_3	DMI_TXN_3 AF3 — DMI_MT_IR_DN3

SKYLAKE-1,SKL-S,LAKE-S

reverse at PCH side

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU(PCIE/DMI)
Size: Custom
Document Number: Consumer AIO Petra238i
Rev: 1A
Date: Wednesday, July 25, 2018
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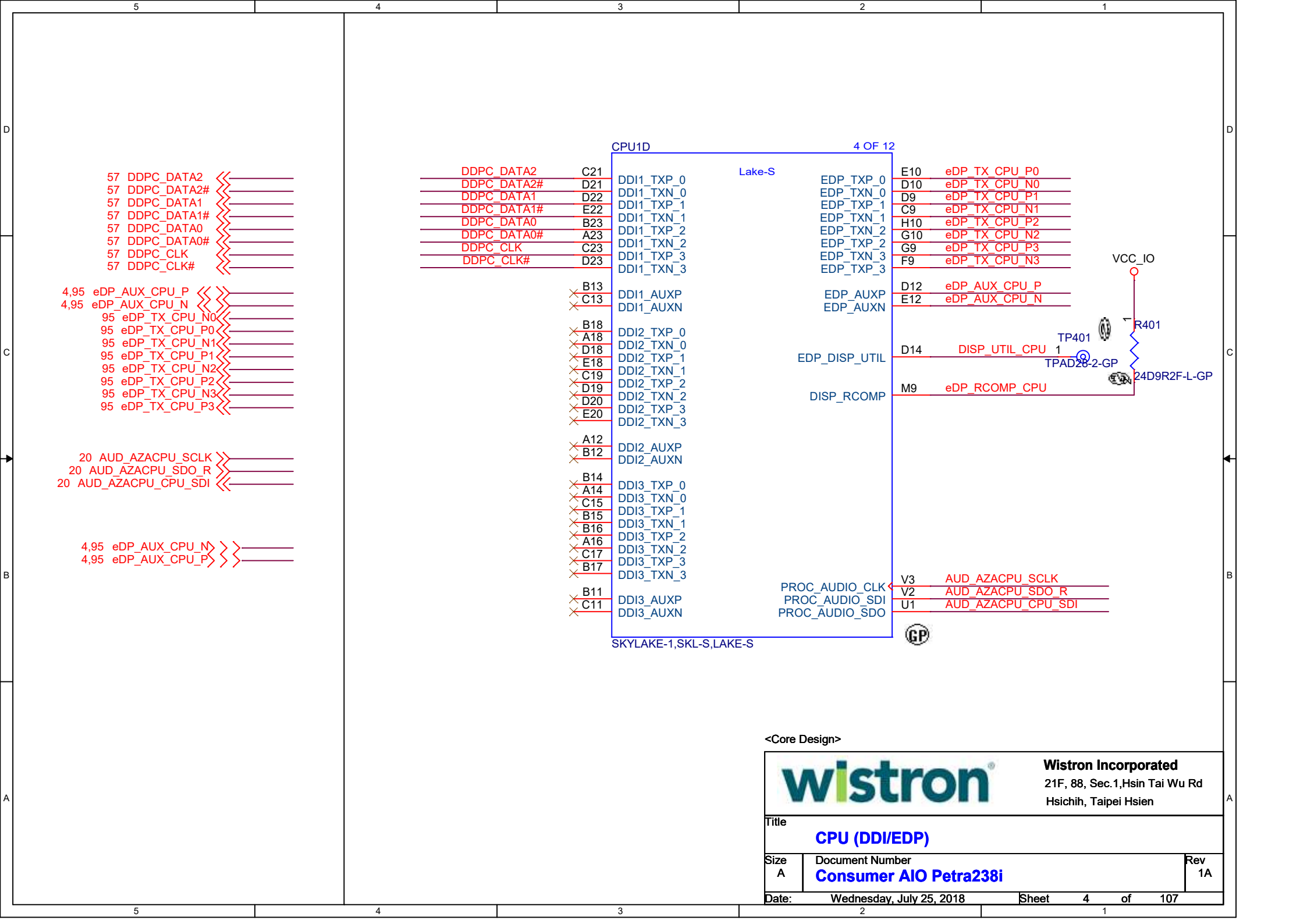

<Core Design>

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
CPU (DDI/EDP)

Size	Document Number	Rev
A	**Consumer AIO Petra238i**	1A

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12 M_A_DQ[63..0]
12 M_A_A[13..0]
12 M_A_DQS_DP[7..0]
12 M_A_DQS_DN[7..0]
12 M_A_BA[1..0]
12 M_A_BG[1..0]
12 M_A_CS#[1..0]
13 M_B_DQ[63..0]
13 M_B_A[13..0]
13 M_B_DQS_DP[7..0]
13 M_B_DQS_DN[7..0]
13 M_B_BA[1..0]
13 M_B_BG[1..0]
12 M_A_CLK0
12 M_A_CLK#0
12 M_A_CLK1
12 M_A_CLK#1
12 M_A_ACT#
12 M_A_ODT0
12 M_A_ODT1
12 M_A_CKE0
12 M_A_CKE1
12 M_A_CAS#
12 M_A_WE#
12 M_A_RAS#
12 M_A_ALERT#
12 M_A_PAR
13 M_B_CLK0
13 M_B_CLK#0
13 M_B_CLK1
13 M_B_CLK#1
13 M_B_CS#1
13 M_B_CS#0
13 M_B_ODT1
13 M_B_ODT0
13 M_B_CKE1
13 M_B_CKE0
13 M_B_WE#
13 M_B_RAS#
13 M_B_CAS#
13 M_B_VREF_DQ
12 M_A_VREF_CA
13 M_B_ACT#
13 M_B_PAR
13 M_B_ALERT#
CPU1A
1 OF 12
Lake-S
DDR0_DQ_0/DDR0_DQ_0
DDR0_DQ_1/DDR0_DQ_1
DDR0_DQ_2/DDR0_DQ_2
DDR0_DQ_3/DDR0_DQ_3
DDR0_DQ_4/DDR0_DQ_4
DDR0_DQ_5/DDR0_DQ_5
DDR0_DQ_6/DDR0_DQ_6
DDR0_DQ_7/DDR0_DQ_7
DDR0_DQ_8/DDR0_DQ_8
DDR0_DQ_9/DDR0_DQ_9
DDR0_DQ_10/DDR0_DQ_10
DDR0_DQ_11/DDR0_DQ_11
DDR0_DQ_12/DDR0_DQ_12
DDR0_DQ_13/DDR0_DQ_13
DDR0_DQ_14/DDR0_DQ_14
DDR0_DQ_15/DDR0_DQ_15
DDR0_DQ_16/DDR0_DQ_32
DDR0_DQ_17/DDR0_DQ_33
DDR0_DQ_18/DDR0_DQ_34
DDR0_DQ_19/DDR0_DQ_35
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DDR0_DQ_23/DDR0_DQ_39
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DDR0_DQ_26/DDR0_DQ_42
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DDR0_DQ_28/DDR0_DQ_44
DDR0_DQ_29/DDR0_DQ_45
DDR0_DQ_30/DDR0_DQ_46
DDR0_DQ_31/DDR0_DQ_47
DDR0_DQ_32/DDR1_DQ_0
DDR0_DQ_33/DDR1_DQ_1
DDR0_DQ_34/DDR1_DQ_2
DDR0_DQ_35/DDR1_DQ_3
DDR0_DQ_36/DDR1_DQ_4
DDR0_DQ_37/DDR1_DQ_5
DDR0_DQ_38/DDR1_DQ_6
DDR0_DQ_39/DDR1_DQ_7
DDR0_DQ_40/DDR1_DQ_8
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DDR0_ALERT#
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M_A_DQS_DP5
M_A_DQS_DP6
M_A_DQS_DP7
DDR CHANNEL A
SKYLAKE-1,SKL-S,LAKE-S
CPU1B
2 OF 12
Lake-S
DDR1_DQ_0/DDR0_DQ_16
DDR1_DQ_1/DDR0_DQ_17
DDR1_DQ_2/DDR0_DQ_18
DDR1_DQ_3/DDR0_DQ_19
DDR1_DQ_4/DDR0_DQ_20
DDR1_DQ_5/DDR0_DQ_21
DDR1_DQ_6/DDR0_DQ_22
DDR1_DQ_7/DDR0_DQ_23
DDR1_DQ_8/DDR0_DQ_24
DDR1_DQ_9/DDR0_DQ_25
DDR1_DQ_10/DDR0_DQ_26
DDR1_DQ_11/DDR0_DQ_27
DDR1_DQ_12/DDR0_DQ_28
DDR1_DQ_13/DDR0_DQ_29
DDR1_DQ_14/DDR0_DQ_30
DDR1_DQ_15/DDR0_DQ_31
DDR1_DQ_16/DDR1_DQ_32
DDR1_DQ_17/DDR1_DQ_33
DDR1_DQ_18/DDR1_DQ_34
DDR1_DQ_19/DDR1_DQ_35
DDR1_DQ_20/DDR1_DQ_36
DDR1_DQ_21/DDR1_DQ_37
DDR1_DQ_22/DDR1_DQ_38
DDR1_DQ_23/DDR1_DQ_39
DDR1_DQ_24/DDR1_DQ_40
DDR1_DQ_25/DDR1_DQ_41
DDR1_DQ_26/DDR1_DQ_42
DDR1_DQ_27/DDR1_DQ_43
DDR1_DQ_28/DDR1_DQ_44
DDR1_DQ_29/DDR1_DQ_45
DDR1_DQ_30/DDR1_DQ_46
DDR1_DQ_31/DDR1_DQ_47
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DDR1_DQ_63/DDR1_DQ_63
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DDR1_ECC_1
DDR1_ECC_2
DDR1_ECC_3
DDR1_ECC_4
DDR1_ECC_5
DDR1_ECC_6
DDR1_ECC_7
DDR1_CKP_0
DDR1_CKN_0
DDR1_CKP_1
DDR1_CKN_1
DDR1_CKP_2
DDR1_CKN_2
DDR1_CKP_3
DDR1_CKN_3
DDR1_CKE_0
DDR1_CKE_1
DDR1_CKE_2
DDR1_CKE_3
DDR1_CS#_0
DDR1_CS#_1
DDR1_CS#_2
DDR1_CS#_3
DDR1_ODT_0
DDR1_ODT_1
DDR1_ODT_2
DDR1_ODT_3
DDR1_MA_16
DDR1_MA_14
DDR1_MA_15
DDR1_BA_0
DDR1_BA_1
DDR1_BG_0
DDR1_MA_0
DDR1_MA_1
DDR1_MA_2
DDR1_MA_3
DDR1_MA_4
DDR1_MA_5
DDR1_MA_6
DDR1_MA_7
DDR1_MA_8
DDR1_MA_9
DDR1_MA_10
DDR1_MA_11
DDR1_MA_12
DDR1_MA_13
DDR1_BG_1
DDR1_ACT#
DDR1_PAR
DDR1_ALERT#
DDR1_DQSN_0/DDR0_DQSN_2
DDR1_DQSN_1/DDR0_DQSN_3
DDR1_DQSN_2/DDR0_DQSN_6
DDR1_DQSN_3/DDR0_DQSN_7
DDR1_DQSN_4/DDR1_DQSN_2
DDR1_DQSN_5/DDR1_DQSN_3
DDR1_DQSN_6/DDR1_DQSN_6
DDR1_DQSN_7/DDR1_DQSN_7
DDR1_DQSP_0/DDR0_DQSP_2
DDR1_DQSP_1/DDR0_DQSP_3
DDR1_DQSP_2/DDR0_DQSP_6
DDR1_DQSP_3/DDR0_DQSP_7
DDR1_DQSP_4/DDR1_DQSP_2
DDR1_DQSP_5/DDR1_DQSP_3
DDR1_DQSP_6/DDR1_DQSP_6
DDR1_DQSP_7/DDR1_DQSP_7
DDR1_DQSP_8/DDR1_DQSP_8
DDR1_DQSN_8/DDR1_DQSN_8
M_B_CLK0
M_B_CLK#0
M_B_CLK1
M_B_CLK#1
M_B_CKE0
M_B_CKE1
M_B_CS#0
M_B_CS#1
M_B_ODT0
M_B_ODT1
M_B_BA0
M_B_BA1
M_B_BG0
M_B_RAS#
M_B_WE#
M_B_CAS#
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BG1
M_B_ACT#
M_B_PAR
M_B_ALERT#
M_B_DQS_DN0
M_B_DQS_DN1
M_B_DQS_DN2
M_B_DQS_DN3
M_B_DQS_DN4
M_B_DQS_DN5
M_B_DQS_DN6
M_B_DQS_DN7
M_B_DQS_DP0
M_B_DQS_DP1
M_B_DQS_DP2
M_B_DQS_DP3
M_B_DQS_DP4
M_B_DQS_DP5
M_B_DQS_DP6
M_B_DQS_DP7
DDR CHANNEL B
SKYLAKE-1,SKL-S,LAKE-S
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
M_A_VREF_CA
M_A_VREF_DQ
M_B_VREF_DQ
TP501
<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
CPU_(DDR4 CHANNEL A)
Size
Custom
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6,99 XDP_PCUDEBUG3

99 CFG[0..15]
99 SKL_PCUSTB_0_DP
99 SKL_PCUSTB_0_DN
99 SKL_PCUSTB_1_DP
99 SKL_PCUSTB_1_DN

99 BPM_CPU_N0
99 BPM_CPU_N1

99 H_TDO
99 H_TDI
99 H_TMS
20,99 H_TCK

65,99 H_TRST_N
99 H_PREQ_N
99 H_PRDY_N

46 VIDSCK_VR1
46 VIDSOUT_VR1
46 VIDALERT#_VR1

18 CPU_BCLK_PCH
18 CPU_BCLK_PCH#
18 CPU_PCIBCLK_PCH
18 CPU_PCIBCLK_PCH#
18 CPU_CLK24M_PCH
18 CPU_CLK24M_PCH#

24,43 PROCHOT#_SIO

65 CPU_VCCST_PWRGD_R
46 PROCHOT#_R
50 DDR_VTT_CNTL

40,99 CPU_VCCST_PWRGD
20,65,99 H_PWRGD
17,65,99 PLTRST_CPU_N
17 PM_SYNC_CPU
17 PM_DOWN_PCH
17,24 PECI_CPU
17,79 THERMTRIP#_CPU_R
17 H_SKTOCC_N

20 PCH_JTAG_TDO
20 PCH_JTAG_TDI
20 PCH_JTAG_TMS
21 H_TRST_N_R

6,99 XDP_PCUDEBUG3

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted. — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation. — 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-Processor Line only and test point may be placed on the board for them.

1V_VCCST_VCCPLL_S3
R6037 (R_) 10KR2J-3-GP
R6038 1KR2F-3-GP
PROCHOT#_SIO_B
PROCHOT#_SIO
Q6001 LMBT3904LT1G-GP
PROCHOT#_R
R6039 0R0402-PAD-2-GP
-1 Layout modify

CPU1E
Lake-S
5 OF 12
SKYLAKE-1,SKL-S,LAKE-S

CPU_BCLK_PCH W5 BCLKP
CPU_BCLK_PCH# W4 BCLKN
CPU_PCIBCLK_PCH W1 PCI_BCLKP
CPU_PCIBCLK_PCH# W2 PCI_BCLKN
CPU_CLK24M_PCH K9 CLK24P
CPU_CLK24M_PCH# J9 CLK24N

VIDALERT#_VR1 R6001 220R2J-L2-GP VIDALERT#_CPU E39 VIDALERT#
VIDSCK_VR1 E38 VIDSCK
VIDSOUT_VR1 E40 VIDSOUT
PROCHOT#_R R6002 499R2F-2-GP PROCHOT#_CPU C39 PROCHOT#
DDR_VTT_CNTL AC36
H_SKTOCC_N AC38 SKTOCC#
CPU_VCCST_PWRGD R6003 6K04R2F-GP
R6004 2K8R2F-GP CPU_VCCST_PWRGD_R U2 VCCST_PWRGD
H_PWRGD F8 PROCPWRGD
PLTRST_CPU_N E7 RESET#
PM_SYNC_CPU E8 PM_SYNC
PM_DOWN_PCH R6005 20R2F-GP PM_DOWN_CPU D8 PM_DOWN
PECI_CPU G7 PECI
THERMTRIP#_CPU_R R6006 0R0402-PAD-2-GP THERMTRIP#_CPU D11 THERMTRIP#
-1 Layout modify short pad
C6001 SCD1U16V2KX-3DLGP (R_)
C6002 SCD1U16V2KX-3DLGP (R_)
SKL_CNL_N AB36 PROC_SELECT#
TP6002
CATERR#_CPU D13 CATERR#
CFG_RCOMP M11 CFG_RCOMP
R6007 49D9R2F-GP

CFG_0 H15 CFG0 R6008 1KR2J-1-GP
CFG_1 F15 CFG1 R6009 1KR2J-1-GP
CFG_2 F16 CFG2 R6010 1KR2J-1-GP
CFG_3 H16 CFG3 R6011 1KR2J-1-GP
CFG_4 F19 CFG4 R6012 1KR2J-1-GP
CFG_5 H18 CFG5 R6013 1KR2J-1-GP
CFG_6 G21 CFG6 R6014 1KR2J-1-GP
CFG_7 H20 CFG7 R6015 1KR2J-1-GP
CFG_8 G16 CFG8 R6016 1KR2J-1-GP
CFG_9 E16 CFG9 R6017 1KR2J-1-GP
CFG_10 F17 CFG10 R6018 1KR2J-1-GP
CFG_11 H17 CFG11 R6019 1KR2J-1-GP
CFG_12 G20 CFG12 R6020 1KR2J-1-GP
CFG_13 F20 CFG13 R6021 1KR2J-1-GP
CFG_14 F21 CFG14 R6022 1KR2J-1-GP
CFG_15 H19 CFG15 R6023 1KR2J-1-GP
SB

CFG_17 F14 SKL_PCUSTB_0_DP
CFG_16 E14 SKL_PCUSTB_0_DN
CFG_19 F18 SKL_PCUSTB_1_DP
CFG_18 G18 SKL_PCUSTB_1_DN

BPM#_0 D16 BPM_CPU_N0
BPM#_1 D17 BPM_CPU_N1
BPM#_2 G14 TP_CPU_G14 TP6003
BPM#_3 H14 TP_CPU_H14 TP6004

PROC_TDO H13 H_TDO
PROC_TDI G12 H_TDI
PROC_TMS F13 H_TMS
PROC_TCK F11 H_TCK
PROC_TRST# F12 H_TRST_N
PROC_PREQ# B9 H_PREQ_N
PROC_PRDY# B10 H_PRDY_N

H_TRST_N R6024 0R0402-PAD-2-GP H_TRST_N_R
H_TDO R6025 0R0402-PAD-2-GP PCH_JTAG_TDO
H_TDI R6026 0R0402-PAD-2-GP PCH_JTAG_TDI
H_TMS R6027 0R0402-PAD-2-GP PCH_JTAG_TMS
-1 Layout modify short pad

VCC_IO
SKL_CNL_N R6029 2 (R_) 1 10KR2J-3-GP
1V_VCCST_VCCPLL_S3
VIDSCK_VR1 R6030 1 (R_) 45D3R2F-L-GP
VIDALERT#_VR1 R6031 1 56R2F-1-GP
VIDSOUT_VR1 R6032 1 100R2J-2-GP
PROCHOT#_CPU R6033 1 (R_) 2 75R2F-2-GP
SB
3D3V_S5
H_SKTOCC_N R6034 1 10KR2J-3-GP
H_TCK R6035 1 51R2F-2-GP
H_TRST_N R6036 (R_) 1 51R2F-2-GP
CFG3 R6028 1 1KR2J-1-GP XDP_PCUDEBUG3

<Core Design>

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Wistron Incorporated
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Hsichih, Taipei Hsien

Title: CPU (SVID/CFG/JTAG/CLK)
Size: B
Document Number: Consumer AIO Petra238i
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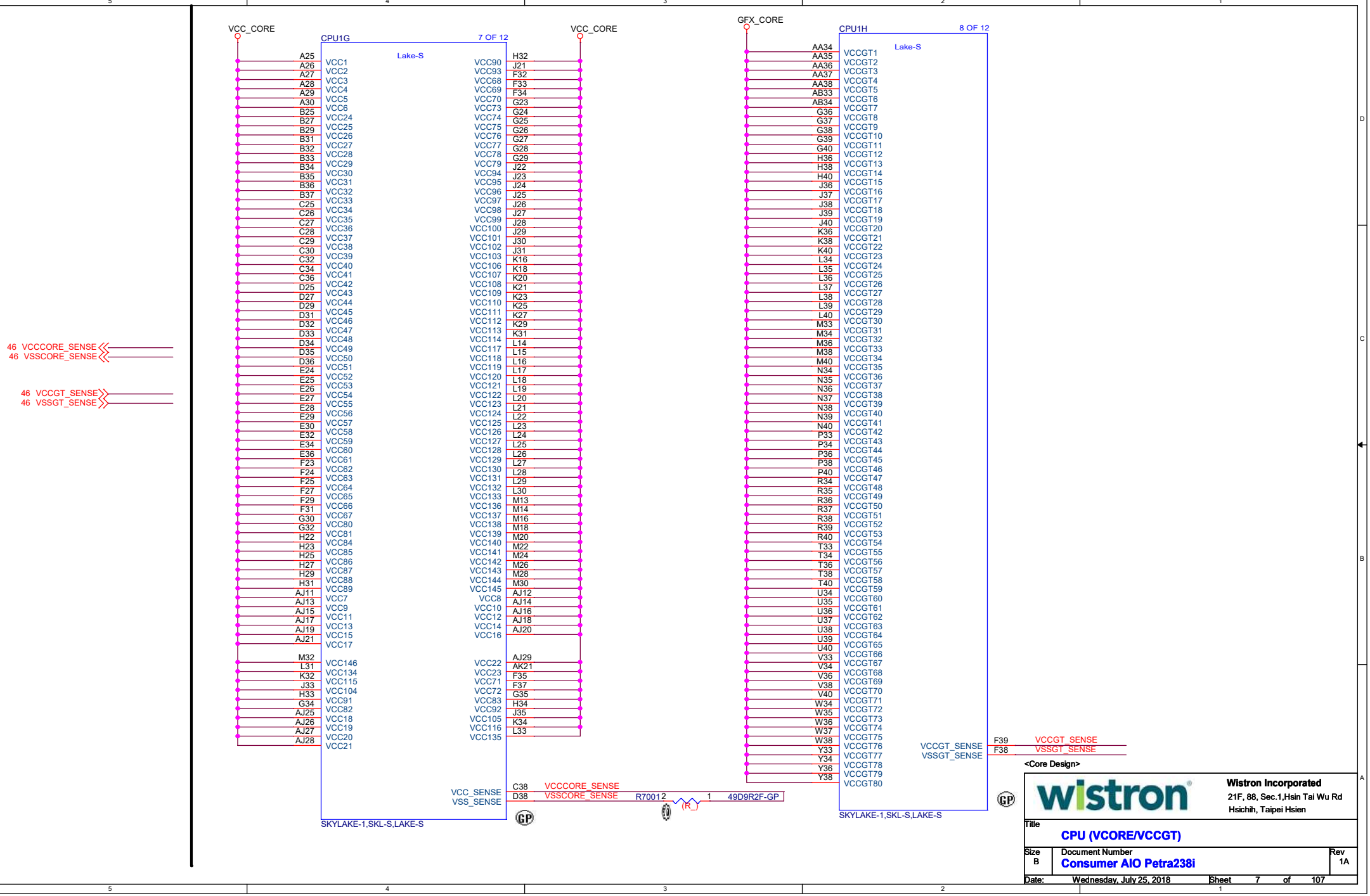

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU (VCORE/VCCGT)

Size: B | Document Number: Consumer AIO Petra238i | Rev: 1A

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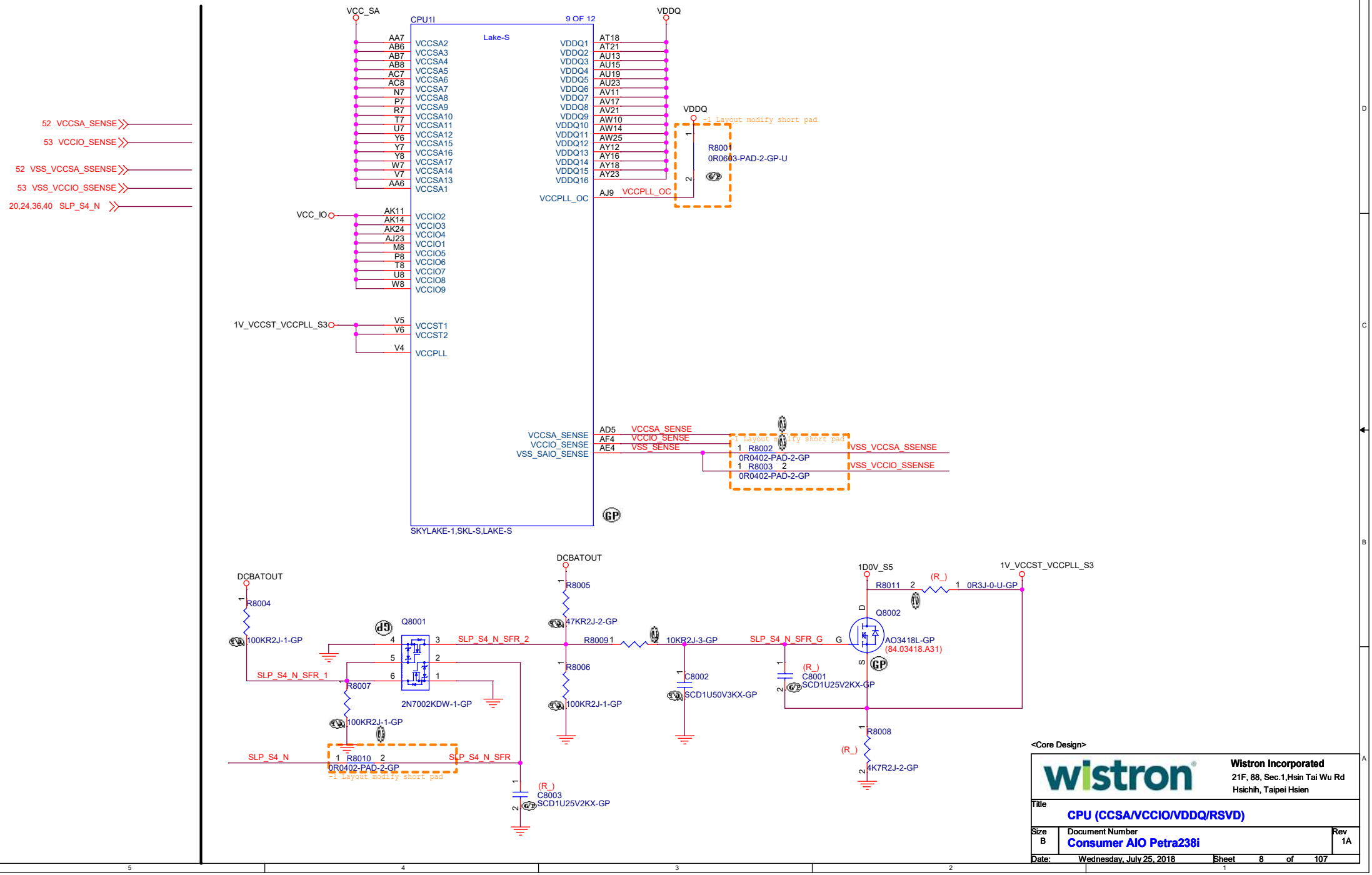
52 VCCSA_SENSE
53 VCCIO_SENSE
52 VSS_VCCSA_SSENSE
53 VSS_VCCIO_SSENSE
20,24,36,40 SLP_S4_N
VCC_SA
CPU1I
9 OF 12
Lake-S
VDDQ
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8
VCCSA9
VCCSA10
VCCSA11
VCCSA12
VCCSA15
VCCSA16
VCCSA17
VCCSA14
VCCSA13
VCCSA1
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15
VDDQ16
VCCPLL_OC
AJ9 VCCPLL_OC
R8001
0R0603-PAD-2-GP-U
-1 Layout modify short pad
VCC_IO
VCCIO2
VCCIO3
VCCIO4
VCCIO1
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCIO9
1V_VCCST_VCCPLL_S3
VCCST1
VCCST2
VCCPLL
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
AD5 VCCSA_SENSE
AF4 VCCIO_SENSE
AE4 VSS_SENSE
R8002
R8003
0R0402-PAD-2-GP
VSS_VCCSA_SSENSE
VSS_VCCIO_SSENSE
SKYLAKE-1,SKL-S,LAKE-S
DCBATOUT
R8004
100KR2J-1-GP
Q8001
2N7002KDW-1-GP
SLP_S4_N_SFR_1
SLP_S4_N_SFR_2
R8007
100KR2J-1-GP
R8005
47KR2J-2-GP
R8006
100KR2J-1-GP
R80091
10KR2J-3-GP
C8002
SCD1U50V3KX-GP
SLP_S4_N_SFR_G
1D0V_S5
R8011
0R3J-0-U-GP
1V_VCCST_VCCPLL_S3
Q8002
AO3418L-GP
(84.03418.A31)
C8001
SCD1U25V2KX-GP
R8008
4K7R2J-2-GP
SLP_S4_N
R8010
0R0402-PAD-2-GP
SLP_S4_N_SFR
C8003
SCD1U25V2KX-GP
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
CPU (CCSA/VCCIO/VDDQ/RSVD)
Size B
Document Number
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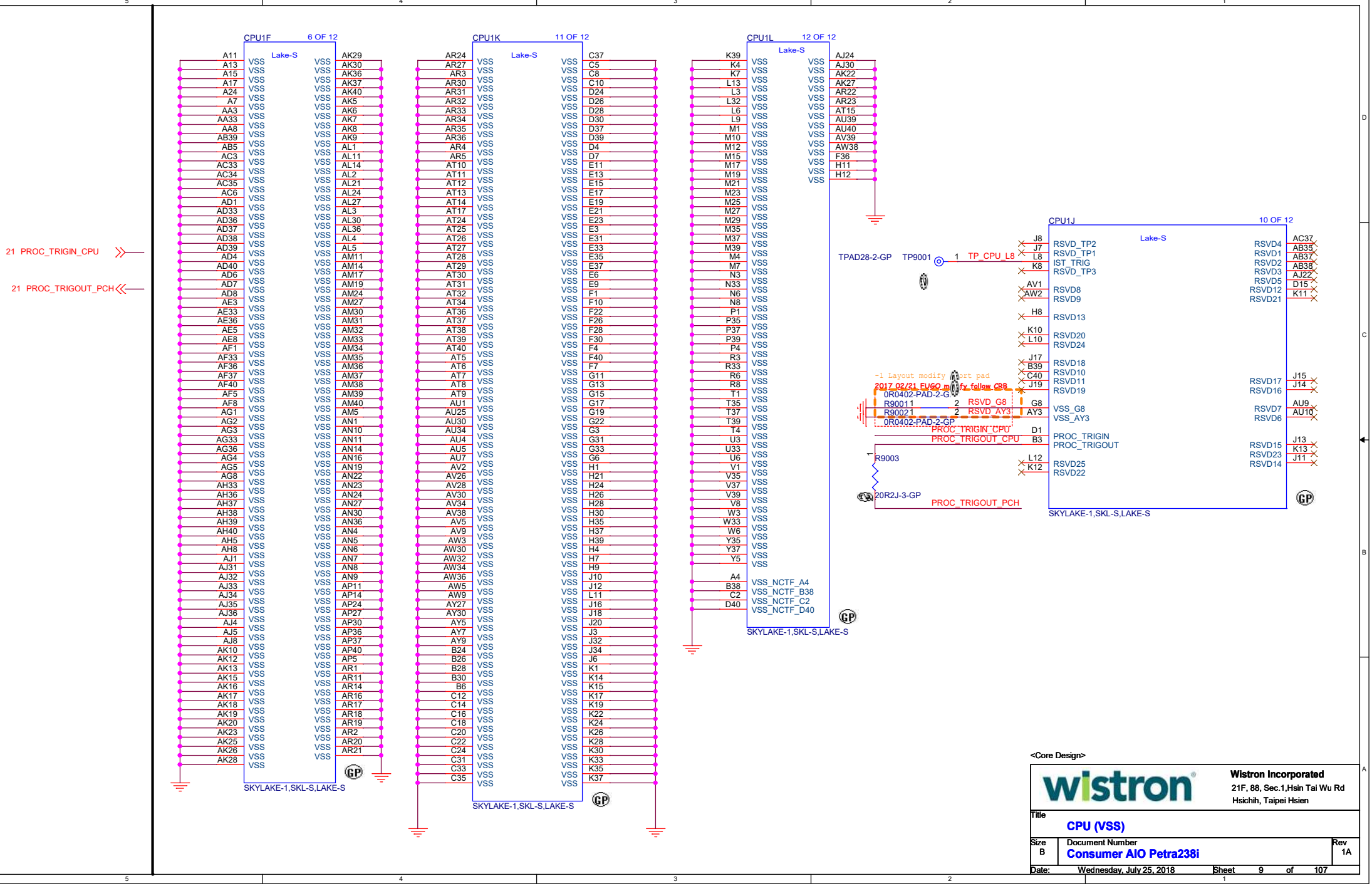
CPU1F
6 OF 12
Lake-S
SKYLAKE-1,SKL-S,LAKE-S
CPU1K
11 OF 12
Lake-S
SKYLAKE-1,SKL-S,LAKE-S
CPU1L
12 OF 12
Lake-S
SKYLAKE-1,SKL-S,LAKE-S
VSS_NCTF_A4
VSS_NCTF_B38
VSS_NCTF_C2
VSS_NCTF_D40
CPU1J
10 OF 12
Lake-S
SKYLAKE-1,SKL-S,LAKE-S
RSVD_TP2
RSVD_TP1
IST_TRIG
RSVD_TP3
RSVD8
RSVD9
RSVD13
RSVD20
RSVD24
RSVD18
RSVD10
RSVD11
RSVD19
VSS_G8
VSS_AY3
PROC_TRIGIN
PROC_TRIGOUT
RSVD25
RSVD22
RSVD4
RSVD1
RSVD2
RSVD3
RSVD5
RSVD12
RSVD21
RSVD17
RSVD16
RSVD7
RSVD6
RSVD15
RSVD23
RSVD14
TPAD28-2-GP
TP9001
TP_CPU_L8
-1 Layout modify short pad
2017 02/21 FUGO modify follow CRB
0R0402-PAD-2-G
R90011
R90021
RSVD_G8
RSVD_AY3
0R0402-PAD-2-GP
PROC_TRIGIN_CPU
PROC_TRIGOUT_CPU
R9003
20R2J-3-GP
PROC_TRIGOUT_PCH
21 PROC_TRIGIN_CPU
21 PROC_TRIGOUT_PCH
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
CPU (VSS)
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B
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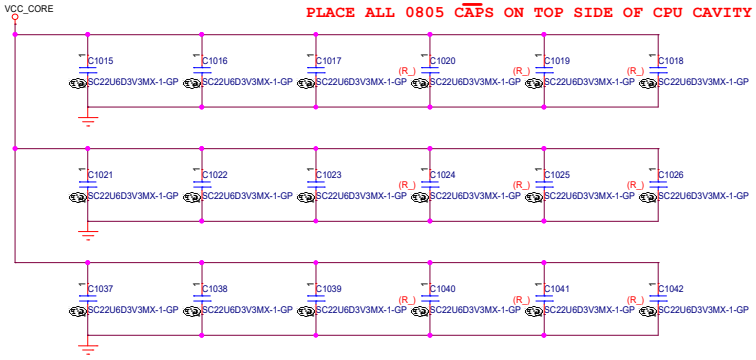
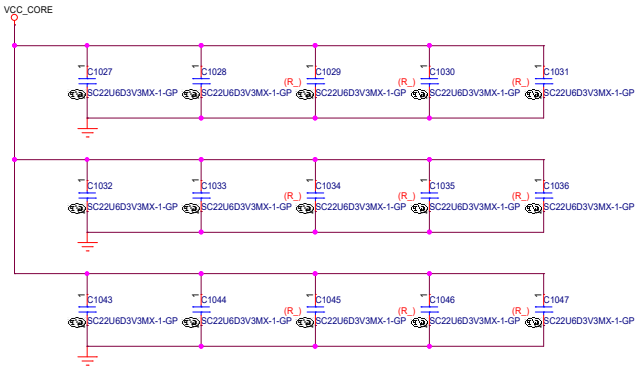
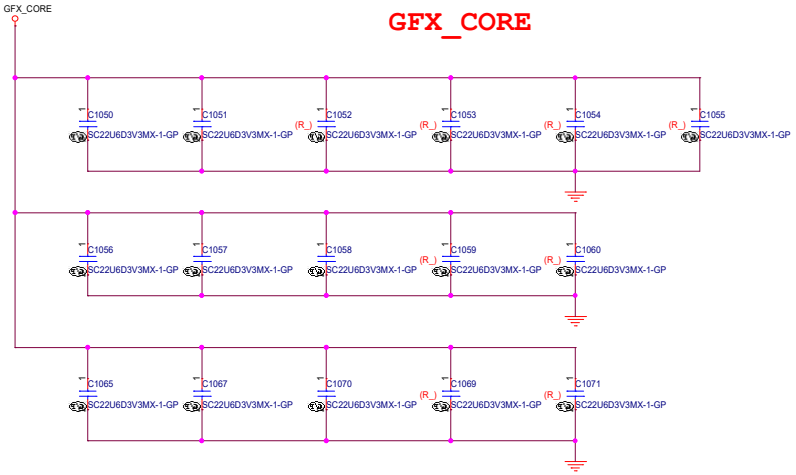
VCC_CORE

PLACE ALL 0805 CAPS ON TOP SIDE OF CPU CAVITY

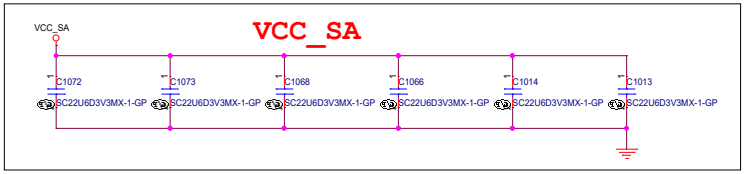




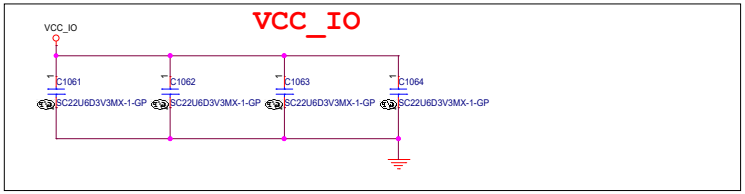
GFX_CORE



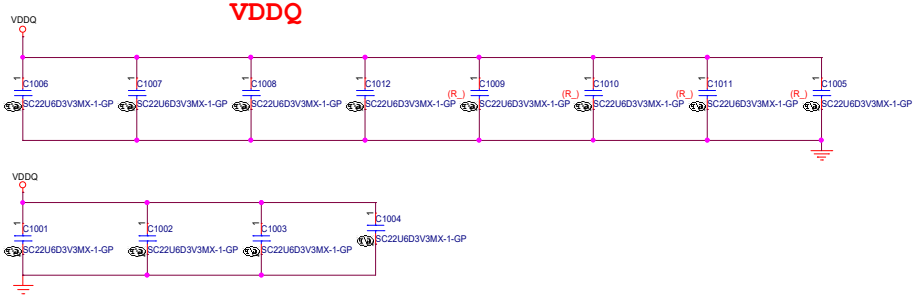
VCC_SA



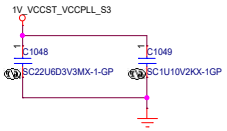
VCC_IO



VDDQ



1V_VCCST_VCCPLL_S3



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU Power CAP

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU Power CAP2

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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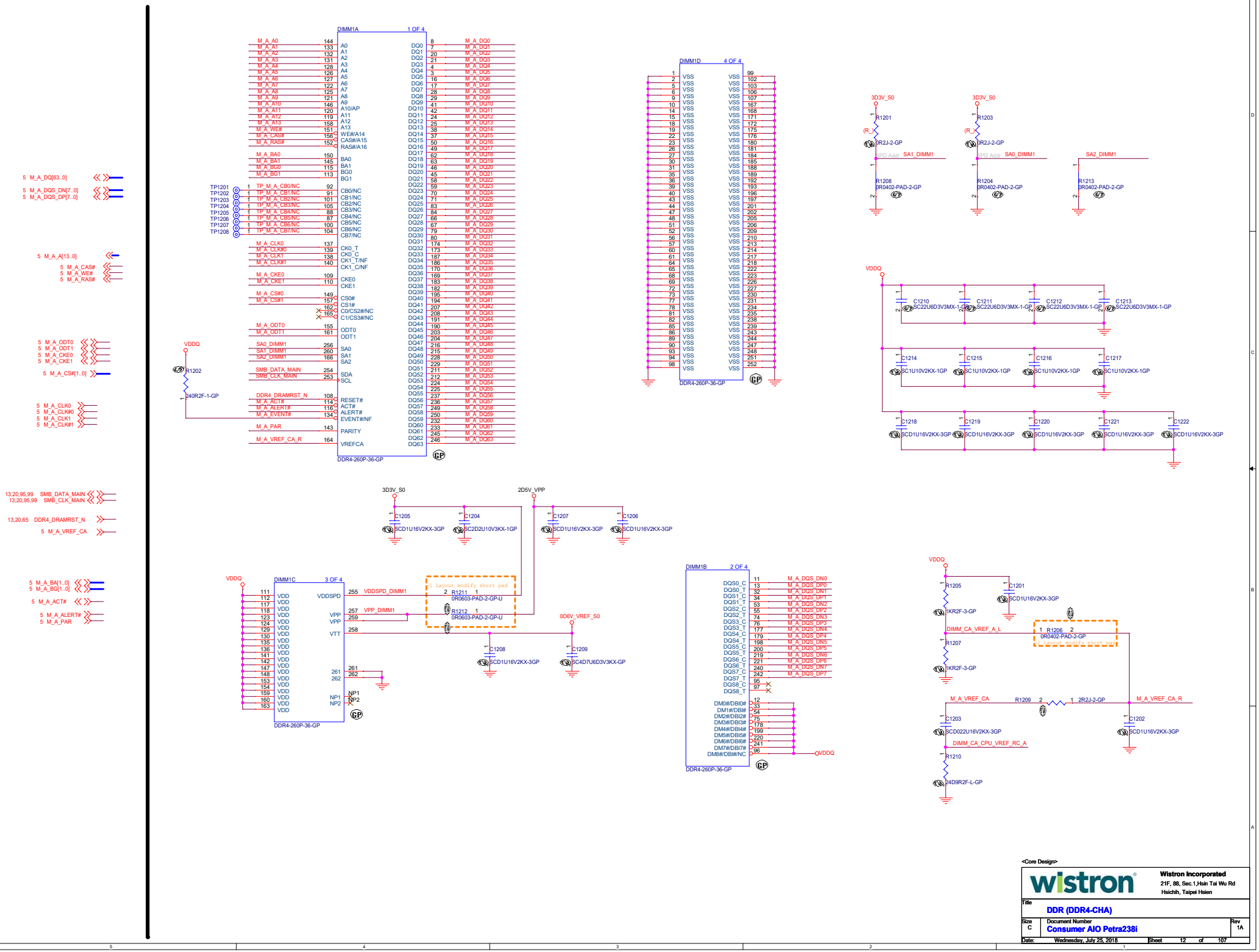
DIMM1A
1 OF 4
DDR4-260P-36-GP
DIMM1D
4 OF 4
DDR4-260P-36-GP
DIMM1C
3 OF 4
DDR4-260P-36-GP
DIMM1B
2 OF 4
DDR4-260P-36-GP
3D3V_S0
SA1_DIMM1
SA0_DIMM1
SA2_DIMM1
VDDQ
2D5V_VPP
0D6V_VREF_S0
DIMM_CA_VREF_A_L
DIMM_CA_CPU_VREF_RC_A
M_A_VREF_CA
M_A_VREF_CA_R
SMB_DATA_MAIN
SMB_CLK_MAIN
DDR4_DRAMRST_N
M_A_VREF_CA
VDDSPD_DIMM1
VPP_DIMM1
1 Layout modify short pad
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
DDR (DDR4-CHA)
Consumer AIO Petra238i
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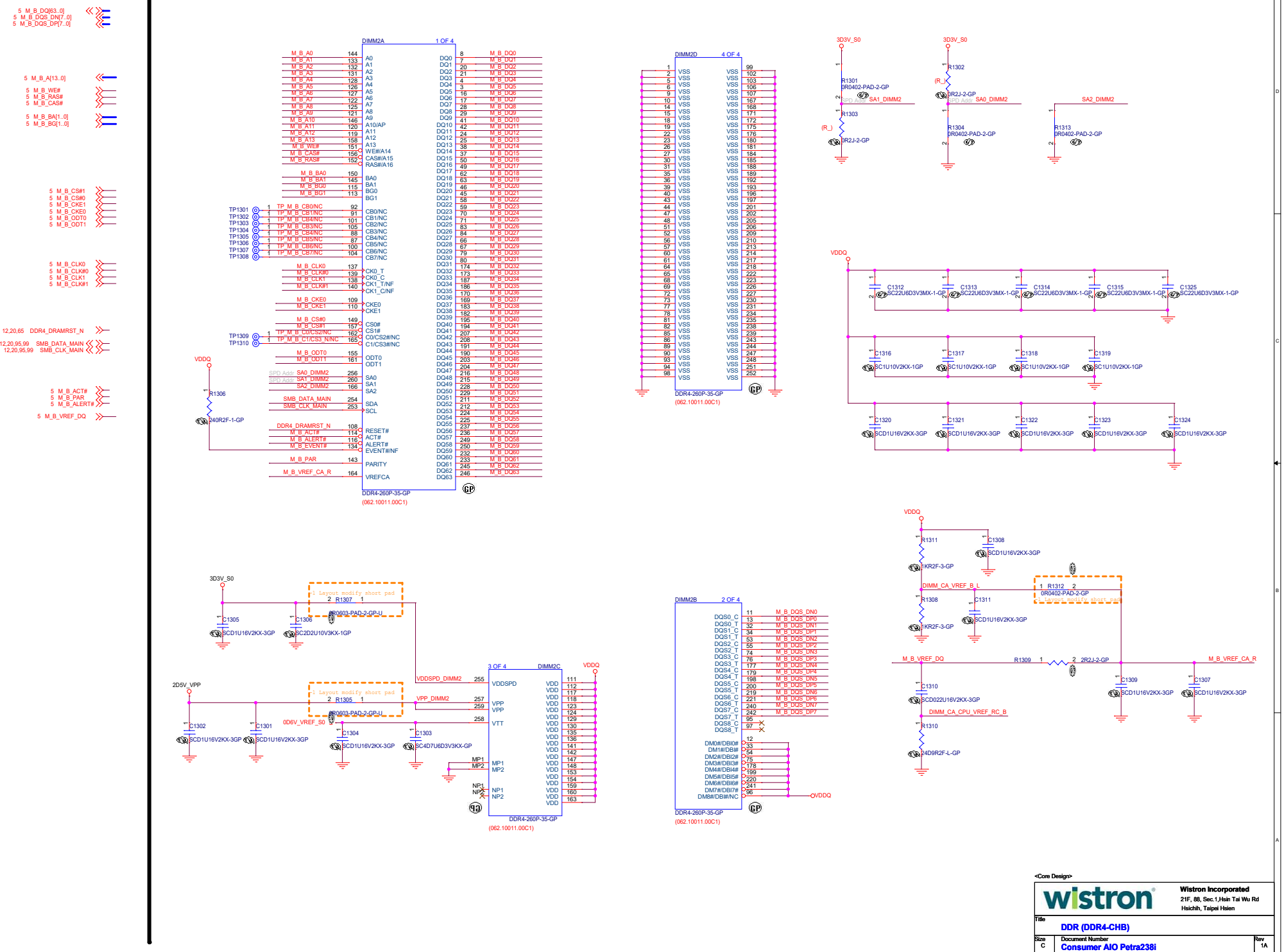
5 M_B_DQ[63..0]
5 M_B_DQS_DN[7..0]
5 M_B_DQS_DP[7..0]
5 M_B_A[13..0]
5 M_B_WE#
5 M_B_RAS#
5 M_B_CAS#
5 M_B_BA[1..0]
5 M_B_BG[1..0]
5 M_B_CS#1
5 M_B_CS#0
5 M_B_CKE1
5 M_B_CKE0
5 M_B_ODT0
5 M_B_ODT1
5 M_B_CLK0
5 M_B_CLK#0
5 M_B_CLK1
5 M_B_CLK#1
12,20,65 DDR4_DRAMRST_N
12,20,95,99 SMB_DATA_MAIN
12,20,95,99 SMB_CLK_MAIN
5 M_B_ACT#
5 M_B_PAR
5 M_B_ALERT#
5 M_B_VREF_DQ
DIMM2A
1 OF 4
DDR4-260P-35-GP
(062.10011.00C1)
DIMM2D
4 OF 4
DDR4-260P-35-GP
(062.10011.00C1)
3D3V_S0
R1301 0R0402-PAD-2-GP
R1302 0R2J-2-GP
R1303 0R2J-2-GP
R1304 0R0402-PAD-2-GP
R1313 0R0402-PAD-2-GP
SA1_DIMM2
SA0_DIMM2
SA2_DIMM2
VDDQ
C1312 SC22U6D3V3MX-1-GP
C1313 SC22U6D3V3MX-1-GP
C1314 SC22U6D3V3MX-1-GP
C1315 SC22U6D3V3MX-1-GP
C1325 SC22U6D3V3MX-1-GP
C1316 SC1U10V2KX-1GP
C1317 SC1U10V2KX-1GP
C1318 SC1U10V2KX-1GP
C1319 SC1U10V2KX-1GP
C1320 SCD1U16V2KX-3GP
C1321 SCD1U16V2KX-3GP
C1322 SCD1U16V2KX-3GP
C1323 SCD1U16V2KX-3GP
C1324 SCD1U16V2KX-3GP
R1306 240R2F-1-GP
TP1301 TP_M_B_CB0/NC
TP1302 TP_M_B_CB1/NC
TP1303 TP_M_B_CB4/NC
TP1304 TP_M_B_CB3/NC
TP1305 TP_M_B_CB4/NC
TP1306 TP_M_B_CB5/NC
TP1307 TP_M_B_CB6/NC
TP1308 TP_M_B_CB7/NC
TP1309 TP_M_B_C0/CS2/NC
TP1310 TP_M_B_C1/CS3_N/NC
SPD Addr SA0_DIMM2
SPD Addr SA1_DIMM2
SPD Addr SA2_DIMM2
SMB_DATA_MAIN
SMB_CLK_MAIN
DDR4_DRAMRST_N
M_B_ACT#
M_B_ALERT#
M_B_EVENT#
M_B_PAR
M_B_VREF_CA_R
3D3V_S0
C1305 SCD1U16V2KX-3GP
C1306 SC2D2U10V3KX-1GP
1 Layout modify short pad
R1307 0R0603-PAD-2-GP-U
2D5V_VPP
C1302 SCD1U16V2KX-3GP
C1301 SCD1U16V2KX-3GP
R1305 0R0603-PAD-2-GP-U
0D6V_VREF_S0
C1304 SCD1U16V2KX-3GP
C1303 SC4D7U6D3V3KX-GP
VDDSPD_DIMM2
VPP_DIMM2
3 OF 4
DIMM2C
VDDSPD
VPP
VTT
MP1
MP2
NP1
NP2
DIMM2B
2 OF 4
DM8#/DBI#/NC
VDDQ
DDR4-260P-35-GP
(062.10011.00C1)
R1311 1KR2F-3-GP
C1308 SCD1U16V2KX-3GP
DIMM_CA_VREF_B_L
R1312 0R0402-PAD-2-GP
R1308 1KR2F-3-GP
C1311 SCD1U16V2KX-3GP
M_B_VREF_DQ
R1309 2R2J-2-GP
M_B_VREF_CA_R
C1310 SCD022U16V2KX-3GP
C1309 SCD1U16V2KX-3GP
C1307 SCD1U16V2KX-3GP
DIMM_CA_CPU_VREF_RC_B
R1310 24D9R2F-L-GP
<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
DDR (DDR4-CHB)
Size C
Document Number
Consumer AIO Petra238i
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Date: Wednesday, July 25, 2018
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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR (RSVD) (DDR4-CHA1)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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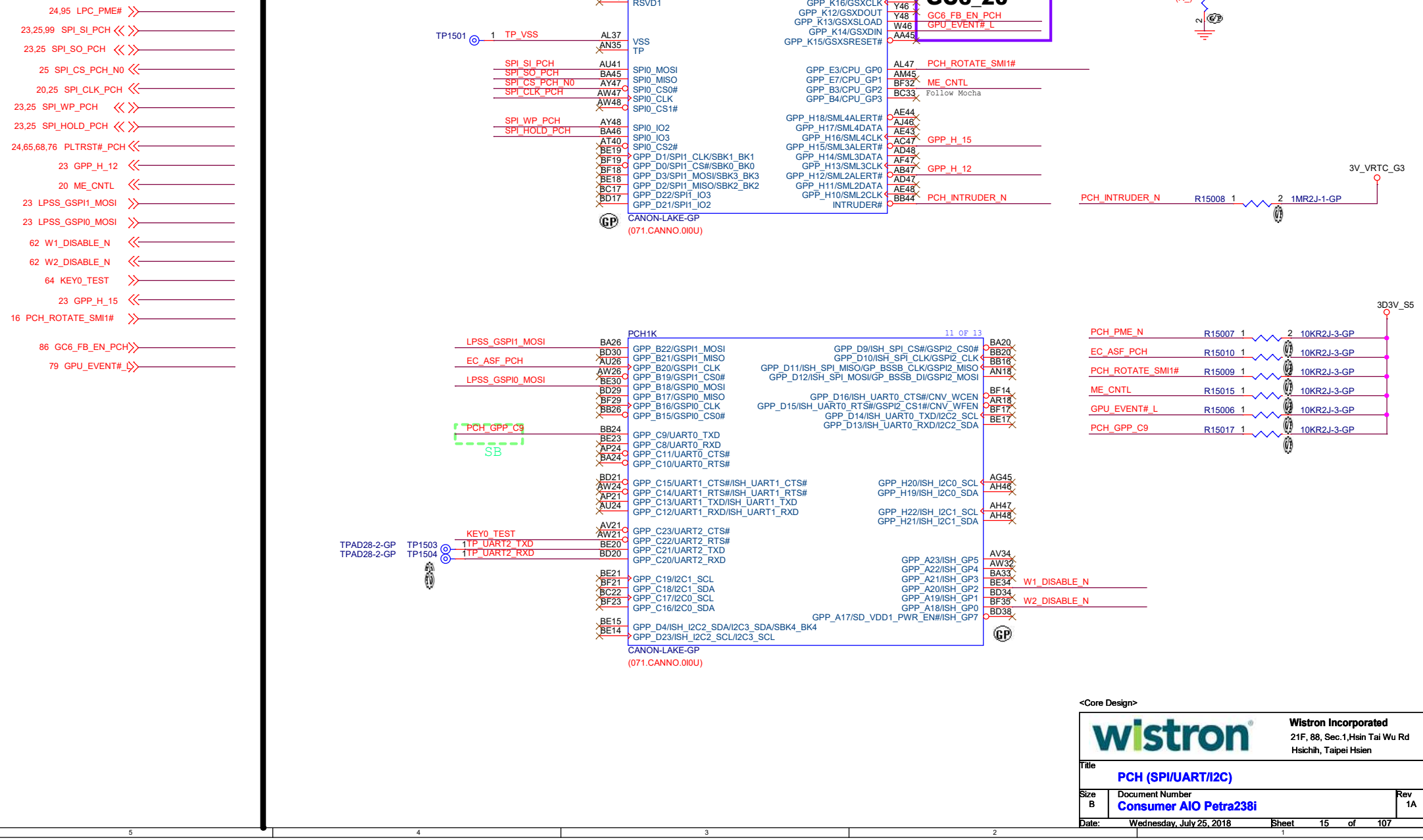
24,95 LPC_PME#
23,25,99 SPI_SI_PCH
23,25 SPI_SO_PCH
25 SPI_CS_PCH_N0
20,25 SPI_CLK_PCH
23,25 SPI_WP_PCH
23,25 SPI_HOLD_PCH
24,65,68,76 PLTRST#_PCH
23 GPP_H_12
20 ME_CNTL
23 LPSS_GSPI1_MOSI
23 LPSS_GSPI0_MOSI
62 W1_DISABLE_N
62 W2_DISABLE_N
64 KEY0_TEST
23 GPP_H_15
16 PCH_ROTATE_SMI1#
86 GC6_FB_EN_PCH
79 GPU_EVENT#_L
LPC_PME#
1 R15011 2
0R0402-PAD-2-GP
-1 Layout modify short pad
PCH_PME_N
PCH1A
1 OF 13
BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
R15 R13 RSVD2 RSVD1
TP1501 1 TP_VSS
AL37 AN35 VSS TP
SPI_SI_PCH AU41 SPI0_MOSI
SPI_SO_PCH BA45 SPI0_MISO
SPI_CS_PCH_N0 AY47 SPI0_CS0#
SPI_CLK_PCH AW47 SPI0_CLK
AW48 SPI0_CS1#
SPI_WP_PCH AY48 SPI0_IO2
SPI_HOLD_PCH BA46 SPI0_IO3
AT40 SPI0_CS2#
BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2
CANON-LAKE-GP
(071.CANNO.0I0U)
AV29 GPP_B13/PLTRST#
Y47 GPP_K16/GSXCLK
Y46 GPP_K12/GSXDOUT
Y48 GPP_K13/GSXSLOAD
W46 GPP_K14/GSXDIN
AA45 GPP_K15/GSXRESET#
GC6_20
GC6_FB_EN_PCH
GPU_EVENT#_L
AL47 GPP_E3/CPU_GP0
AM45 GPP_E7/CPU_GP1
BF32 GPP_B3/CPU_GP2
BC33 GPP_B4/CPU_GP3
Follow Mocha
AE44 GPP_H18/SML4ALERT#
AJ46 GPP_H17/SML4DATA
AE43 GPP_H16/SML4CLK
AC47 GPP_H15/SML3ALERT#
AD48 GPP_H14/SML3DATA
AF47 GPP_H13/SML3CLK
AB47 GPP_H12/SML2ALERT#
AD47 GPP_H11/SML2DATA
AE48 GPP_H10/SML2CLK
BB44 INTRUDER#
PLTRST#_PCH
PCH_ROTATE_SMI1#
ME_CNTL
GPP_H_15
GPP_H_12
PCH_INTRUDER_N
(R_) R15016 100KR2J-1-GP
3V_VRTC_G3
PCH_INTRUDER_N R15008 1 2 1MR2J-1-GP
3D3V_S5
PCH1K
11 OF 13
LPSS_GSPI1_MOSI BA26 GPP_B22/GSPI1_MOSI
BD30 GPP_B21/GSPI1_MISO
EC_ASF_PCH AU26 GPP_B20/GSPI1_CLK
AW26 GPP_B19/GSPI1_CS0#
LPSS_GSPI0_MOSI BE30 GPP_B18/GSPI0_MOSI
BD29 GPP_B17/GSPI0_MISO
BF29 GPP_B16/GSPI0_CLK
BB26 GPP_B15/GSPI0_CS0#
PCH_GPP_C9 BB24 GPP_C9/UART0_TXD
SB
BE23 GPP_C8/UART0_RXD
AP24 GPP_C11/UART0_CTS#
BA24 GPP_C10/UART0_RTS#
BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD
AV21 GPP_C23/UART2_CTS#
KEY0_TEST AW21 GPP_C22/UART2_RTS#
TPAD28-2-GP TP1503 1 TP_UART2_TXD BE20 GPP_C21/UART2_TXD
TPAD28-2-GP TP1504 1 TP_UART2_RXD BD20 GPP_C20/UART2_RXD
BE21 GPP_C19/I2C1_SCL
BF21 GPP_C18/I2C1_SDA
BC22 GPP_C17/I2C0_SCL
BF23 GPP_C16/I2C0_SDA
BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE14 GPP_D23/ISH_I2C2_SCL/I2C3_SCL
CANON-LAKE-GP
(071.CANNO.0I0U)
BA20 GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
BB20 GPP_D10/ISH_SPI_CLK/GSPI2_CLK
BB16 GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
AN18 GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
BF14 GPP_D16/ISH_UART0_CTS#/CNV_WCEN
AR18 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
BF17 GPP_D14/ISH_UART0_TXD/I2C2_SCL
BE17 GPP_D13/ISH_UART0_RXD/I2C2_SDA
AG45 GPP_H20/ISH_I2C0_SCL
AH46 GPP_H19/ISH_I2C0_SDA
AH47 GPP_H22/ISH_I2C1_SCL
AH48 GPP_H21/ISH_I2C1_SDA
AV34 GPP_A23/ISH_GP5
AW32 GPP_A22/ISH_GP4
BA33 GPP_A21/ISH_GP3
BE34 GPP_A20/ISH_GP2
BD34 GPP_A19/ISH_GP1
BF35 GPP_A18/ISH_GP0
BD38 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
W1_DISABLE_N
W2_DISABLE_N
PCH_PME_N R15007 1 2 10KR2J-3-GP
EC_ASF_PCH R15010 1 10KR2J-3-GP
PCH_ROTATE_SMI1# R15009 1 10KR2J-3-GP
ME_CNTL R15015 1 10KR2J-3-GP
GPU_EVENT#_L R15006 1 10KR2J-3-GP
PCH_GPP_C9 R15017 1 10KR2J-3-GP
<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
PCH (SPI/UART/I2C)
Size B
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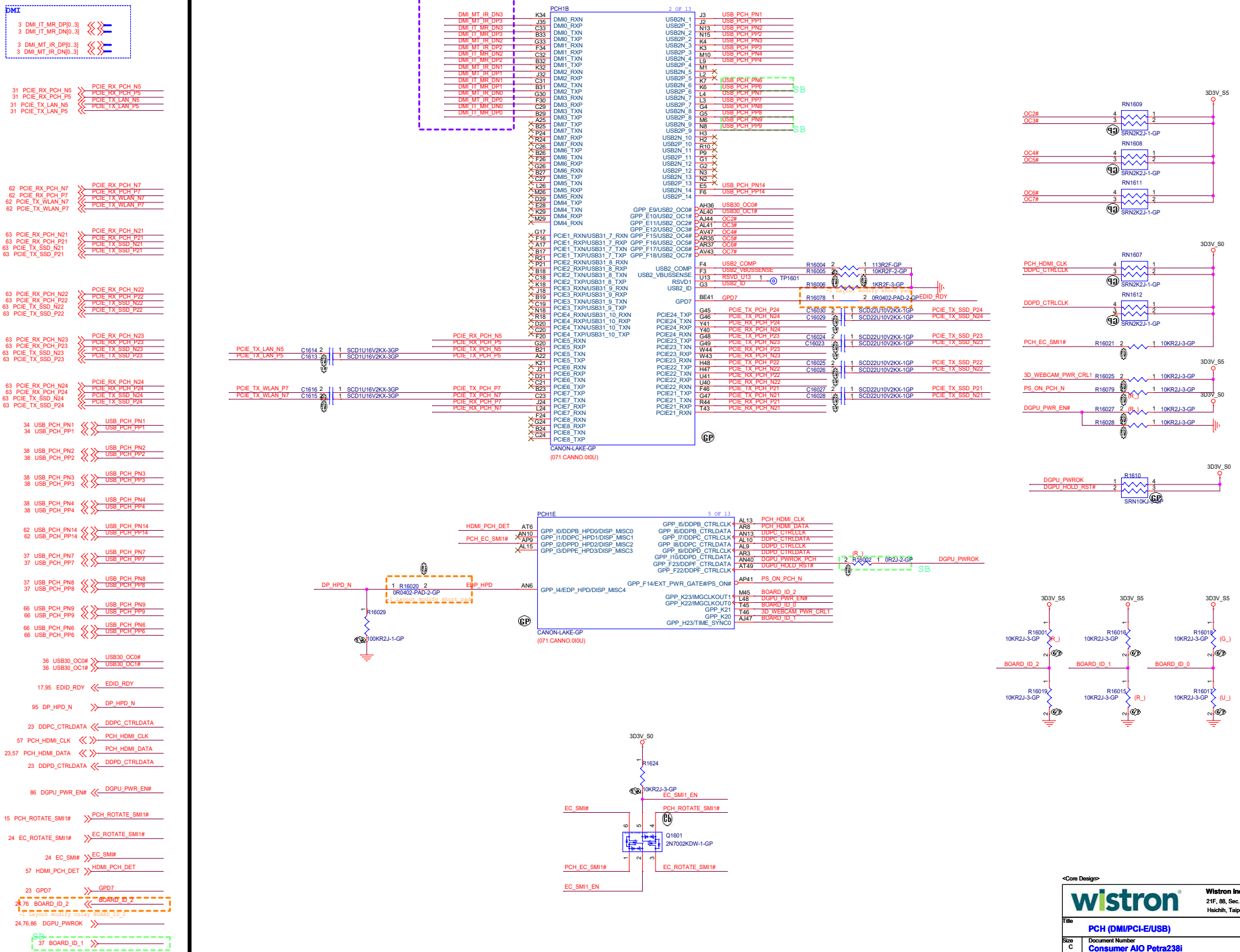
reverse folllow CRB



<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (DMI/PCI-E/USB)

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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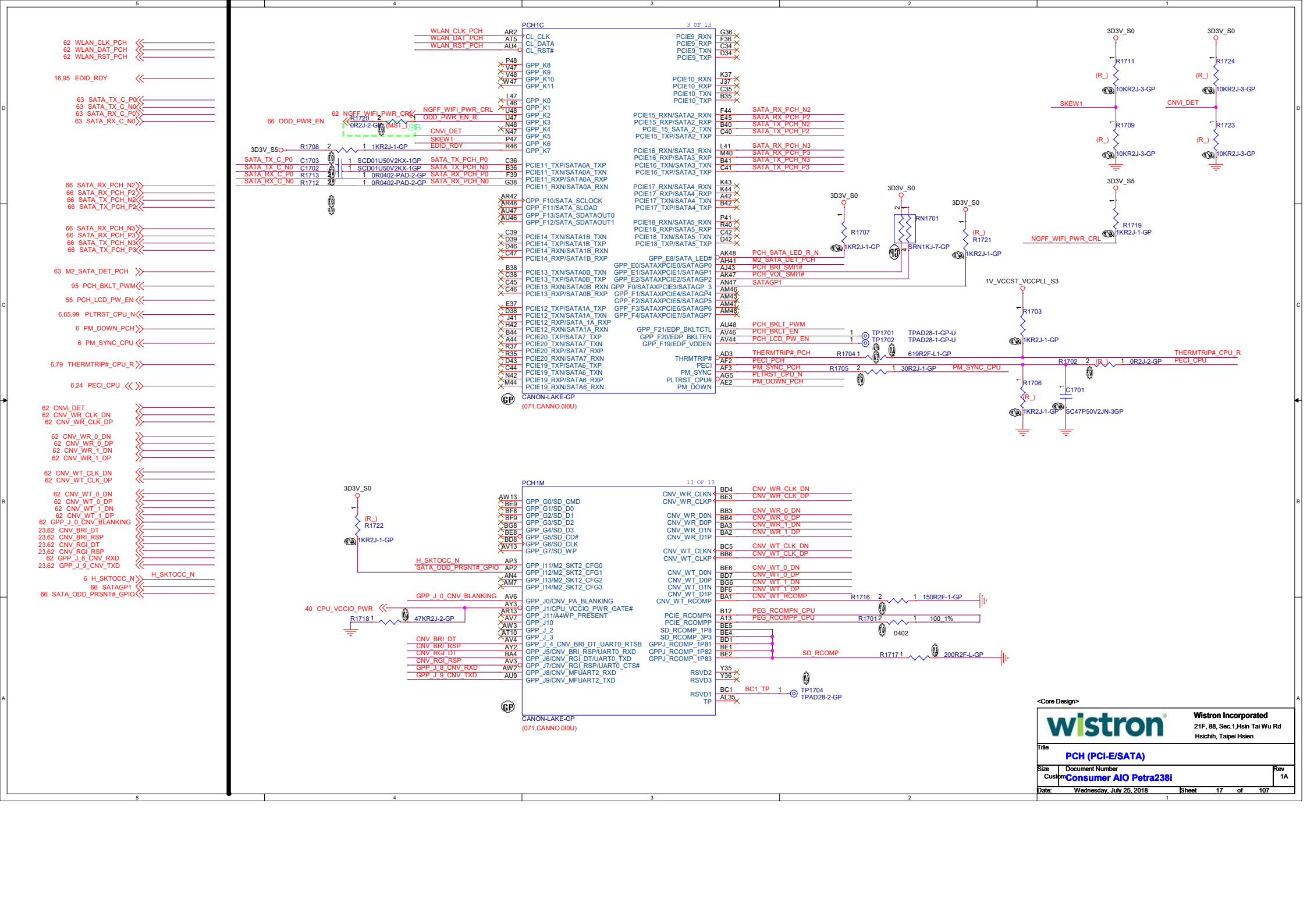
PCH1C
3 OF 13
CANON-LAKE-GP
(071.CANNO.0I0U)
PCH1M
13 OF 13
CANON-LAKE-GP
(071.CANNO.0I0U)
WLAN_CLK_PCH
WLAN_DAT_PCH
WLAN_RST_PCH
EDID_RDY
SATA_TX_C_P0
SATA_TX_C_N0
SATA_RX_C_P0
SATA_RX_C_N0
SATA_RX_PCH_N2
SATA_RX_PCH_P2
SATA_TX_PCH_N2
SATA_TX_PCH_P2
SATA_RX_PCH_N3
SATA_RX_PCH_P3
SATA_TX_PCH_N3
SATA_TX_PCH_P3
M2_SATA_DET_PCH
PCH_BKLT_PWM
PCH_LCD_PW_EN
PLTRST_CPU_N
PM_DOWN_PCH
PM_SYNC_CPU
THERMTRIP#_CPU_R
PECI_CPU
CNVi_DET
CNV_WR_CLK_DN
CNV_WR_CLK_DP
CNV_WR_0_DN
CNV_WR_0_DP
CNV_WR_1_DN
CNV_WR_1_DP
CNV_WT_CLK_DN
CNV_WT_CLK_DP
CNV_WT_0_DN
CNV_WT_0_DP
CNV_WT_1_DN
CNV_WT_1_DP
GPP_J_0_CNV_BLANKING
CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
GPP_J_8_CNV_RXD
GPP_J_9_CNV_TXD
H_SKTOCC_N
SATAGP1
SATA_ODD_PRSNT#_GPIO
NGFF_WIFI_PWR_CRL
ODD_PWR_EN
SKEW1
3D3V_S0
3D3V_S5
1V_VCCST_VCCPLL_S3
CPU_VCCIO_PWR
SD_RCOMP
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
<Core Design>
PCH (PCI-E/SATA)
Consumer AIO Petra238i
Size: Custom
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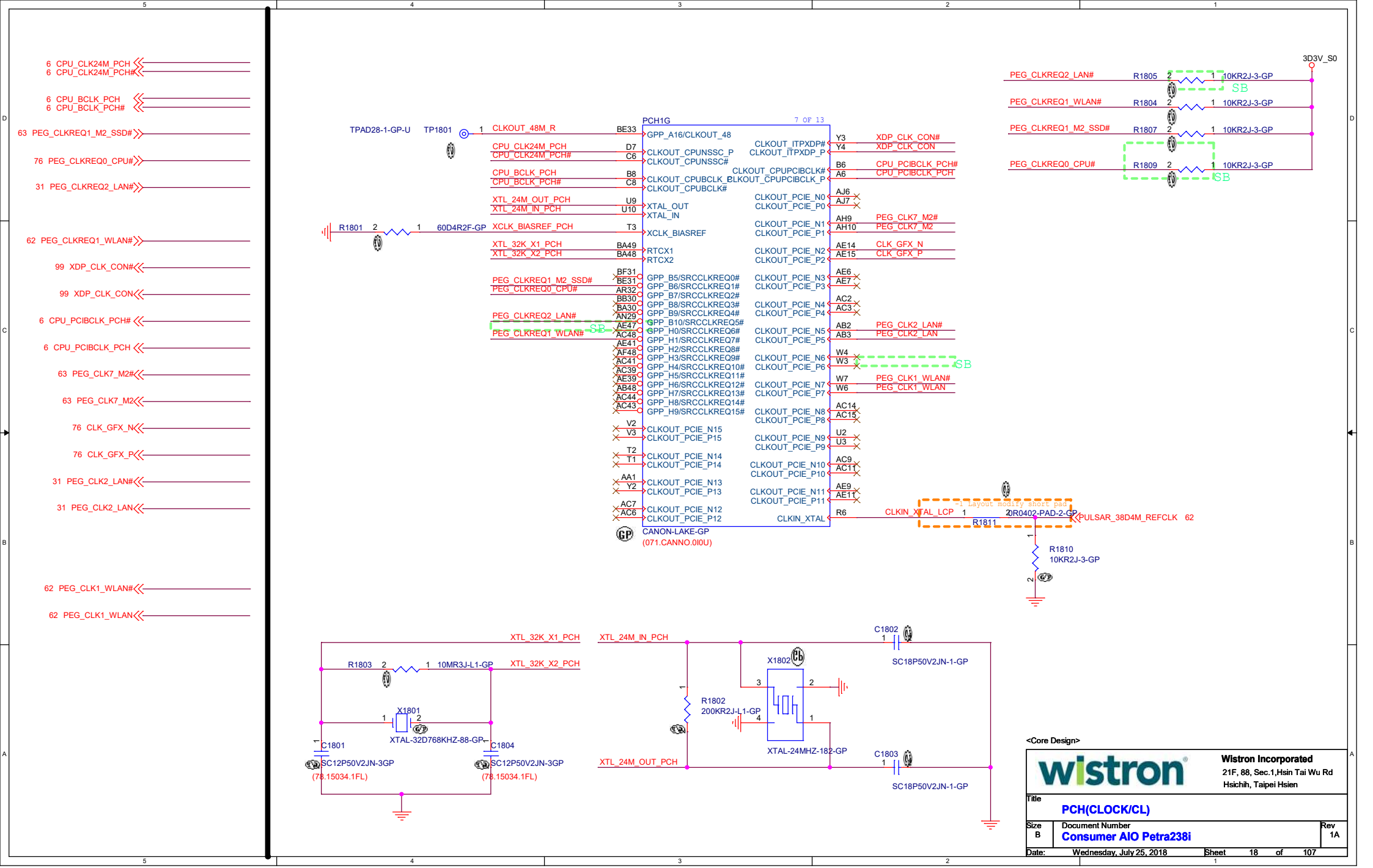
6 CPU_CLK24M_PCH
6 CPU_CLK24M_PCH#
6 CPU_BCLK_PCH
6 CPU_BCLK_PCH#
63 PEG_CLKREQ1_M2_SSD#
76 PEG_CLKREQ0_CPU#
31 PEG_CLKREQ2_LAN#
62 PEG_CLKREQ1_WLAN#
99 XDP_CLK_CON#
99 XDP_CLK_CON
6 CPU_PCIBCLK_PCH#
6 CPU_PCIBCLK_PCH
63 PEG_CLK7_M2#
63 PEG_CLK7_M2
76 CLK_GFX_N
76 CLK_GFX_P
31 PEG_CLK2_LAN#
31 PEG_CLK2_LAN
62 PEG_CLK1_WLAN#
62 PEG_CLK1_WLAN
TPAD28-1-GP-U
TP1801
PCH1G
7 OF 13
CANON-LAKE-GP
(071.CANNO.0I0U)
R1801 60D4R2F-GP
R1803 10MR3J-L1-GP
X1801 XTAL-32D768KHZ-88-GP
C1801 SC12P50V2JN-3GP (78.15034.1FL)
C1804 SC12P50V2JN-3GP (78.15034.1FL)
X1802 XTAL-24MHZ-182-GP
R1802 200KR2J-L1-GP
C1802 SC18P50V2JN-1-GP
C1803 SC18P50V2JN-1-GP
R1805 10KR2J-3-GP
R1804 10KR2J-3-GP
R1807 10KR2J-3-GP
R1809 10KR2J-3-GP
R1810 10KR2J-3-GP
R1811 2R0402-PAD-2-GP
3D3V_S0
SB
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title
PCH(CLOCK/CL)
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Consumer AIO Petra238i
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34 USB30_TX_R_N1
34 USB30_TX_R_P1
34 USB31_RX_C_N1
34 USB31_RX_C_P1

38 USB30_TX_CMC_N2
38 USB30_TX_CMC_P2
38 USB30_RX_PCH_N2
38 USB30_RX_PCH_P2

38 USB30_TX_CMC_P3
38 USB30_TX_CMC_N3
38 USB30_RX_PCH_P3
38 USB30_RX_PCH_N3

38 USB30_TX_CMC_P4
38 USB30_TX_CMC_N4
38 USB30_RX_PCH_P4
38 USB30_RX_PCH_N4

63 SSD_SATA_DEVSLP
66 HDD_SATA_DEVSLP
SB

24,68 LPC_AD_SIO_P0
24,68 LPC_AD_SIO_P1
24,68 LPC_AD_SIO_P2
24,68 LPC_AD_SIO_P3
24,68 LPC_FRAME#_SIO
24 LPC_SERIRQ_PCH
24 KBRST#

68 CLK_LPC_PORT80
24 CLK_PCICLK_SIO
24 CLK_CLKIN_SIO

USB30_TX_R_N1 C1901 2 1 SCD1U16V2KX-3GP USB30_TX_PCH_N1 F9
USB30_TX_R_P1 C1902 2 1 SCD1U16V2KX-3GP USB30_TX_PCH_P1 F7
USB31_RX_C_N1 C1909 2 1 SCD1U16V2KX-3GP USB30_RX_PCH_N1 D11
USB31_RX_C_P1 C1910 2 1 SCD1U16V2KX-3GP USB30_RX_PCH_P1 C11
USB30_TX_CMC_N2 C1903 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_N2 C3
USB30_TX_CMC_P2 C1904 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_P2 D4
USB30_RX_PCH_N2 B9
USB30_RX_PCH_P2 C9

USB30_TX_CMC_P3 C1905 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_P3 G12
USB30_TX_CMC_N3 C1906 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_N3 F11
USB30_RX_PCH_P3 C10
USB30_RX_PCH_N3 B10

USB30_TX_CMC_P4 C1907 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_P4 C14
USB30_TX_CMC_N4 C1908 2 1 SCD22U10V2KX-1GP USB30_TX_PCH_N4 B14
USB30_RX_PCH_P4 J15
USB30_RX_PCH_N4 K16

PCH1F 6 OF 13

USB31_1_TXN		GPP_A1/LAD0/ESPI_IO0	BB39 LPC_AD_SIO_P0
USB31_1_TXP		GPP_A2/LAD1/ESPI_IO1	AW37 LPC_AD_SIO_P1
USB31_1_RXN		GPP_A3/LAD2/ESPI_IO2	AV37 LPC_AD_SIO_P2
USB31_1_RXP		GPP_A4/LAD3/ESPI_IO3	BA38 LPC_AD_SIO_P3
USB31_2_TXN			
USB31_2_TXP			
USB31_2_RXN		GPP_A5/LFRAME#/ESPI_CS0#	BE38 LPC_FRAME#_PCH
USB31_2_RXP		GPP_A6/SERIRQ/ESPI_CS1#	AW35 LPC_SERIRQ_PCH
		GPP_A7/PIRQA#/ESPI_ALERT0#	BA36 LPC_PIRQ_A
		GPP_A0/RCIN#/ESPI_ALERT1#	BE39 KBRST#
		GPP_A14/SUS_STAT#/ESPI_RESET#	BF38 SUS_STAT_N
USB31_6_TXN	C17		
USB31_6_TXP	C16		
USB31_6_RXN	G14		
USB31_6_RXP	F14	GPP_A9/CLKOUT_LPC0/ESPI_CLK	BB36 CLK_PCICLK_SIO_R
USB31_5_TXN	C15	GPP_A10/CLKOUT_LPC1	BB34 CLK_LPC_PORT80_R
USB31_5_TXP	B15		
USB31_5_RXN	J13	GPP_K19/SMI#	T48
USB31_5_RXP	K13	GPP_K18/NMI#	T47
USB31_3_TXP			
USB31_3_TXN		GPP_E6/SATA_DEVSLP2	AH40 HDD_SATA_DEVSLP
USB31_3_RXP		GPP_E5/SATA_DEVSLP1	AH35
USB31_3_RXN		GPP_E4/SATA_DEVSLP0	AL48 SSD_SATA_DEVSLP
		GPP_F9/SATA_DEVSLP7	AP47
USB31_4_TXP		GPP_F8/SATA_DEVSLP6	AN37
USB31_4_TXN		GPP_F7/SATA_DEVSLP5	AN46
USB31_4_RXP		GPP_F6/SATA_DEVSLP4	AR47
USB31_4_RXN		GPP_F5/SATA_DEVSLP3	AP48

CANON-LAKE-GP
(071.CANNO.0I0U)

SB

R1903 1 2 33R2J-2-GP LPC_FRAME#_SIO
R1904 2 1 22R2J-2-GP CLK_CLKIN_SIO
R1905 2 1 22R2J-2-GP CLK_LPC_PORT80
R1906 2 1 22R2J-2-GP CLK_PCICLK_SIO

CLK_CLKIN_SIO EC1901 2 (R_) 1 NEAR PCH SC27P50V2JN-2-GP
CLK_PCICLK_SIO EC1902 2 (R_) 1 NEAR PCH SC27P50V2JN-2-GP

Reserved for MOW WW37

SUS_STAT_N R1907 1 (R_) 2 100KR2J-1-GP

3D3V_S0

RN1901
LPC_SERIRQ_PCH 4
KBRST# 3
1
2
SRN10KJ-5-GP

RN1902
LPC_AD_SIO_P0 4
LPC_AD_SIO_P2 3
1
2
SRN10KJ-5-GP

RN1903
LPC_AD_SIO_P1 4
LPC_AD_SIO_P3 3
1
2
SRN10KJ-5-GP

LPC_FRAME#_SIO R1901 2 (R_) 1 10KR2J-3-GP

3D3V_S5

LPC_PIRQ_A R1902 2 1 10KR2J-3-GP

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (USB/ESPI)
Size: B
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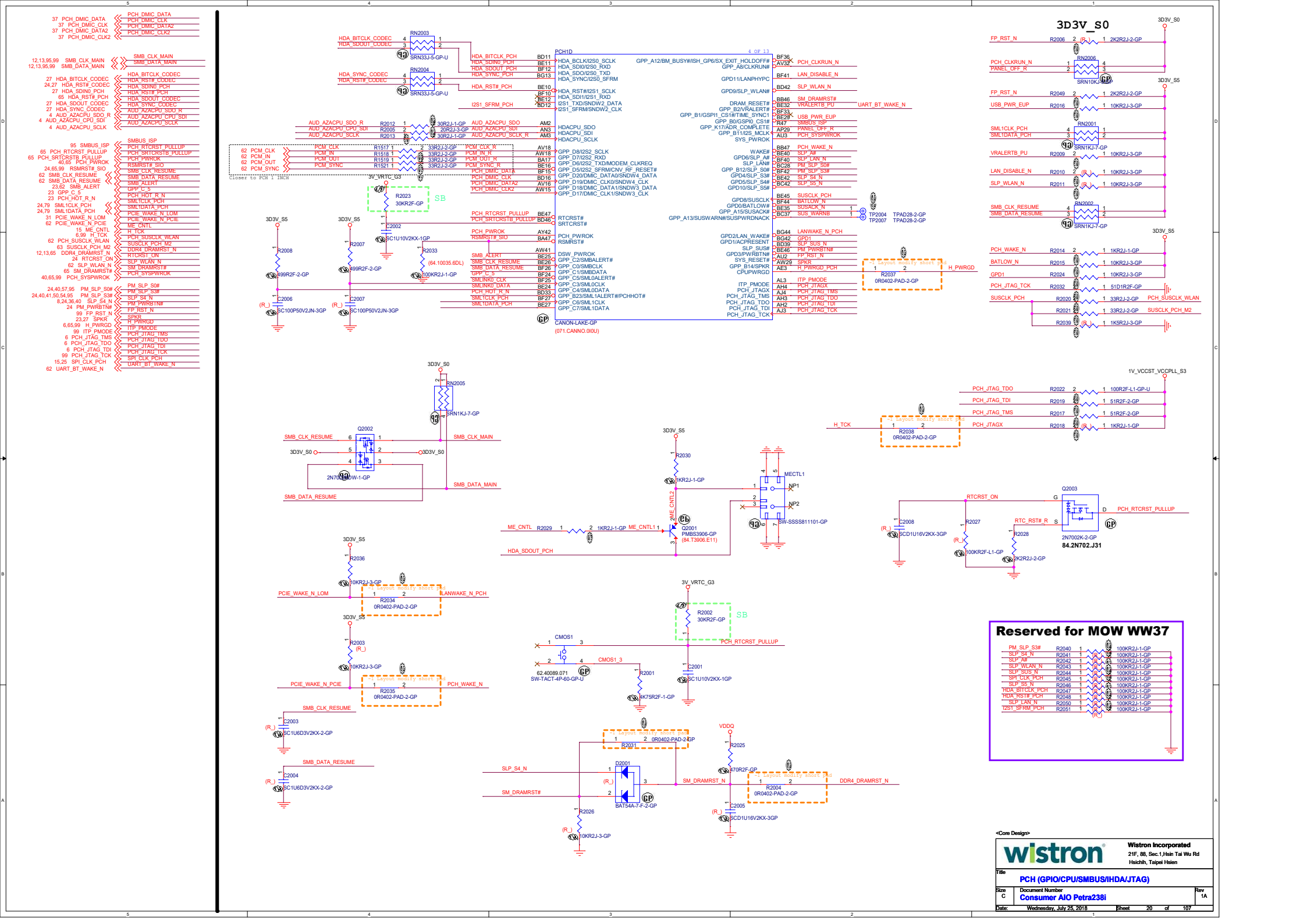
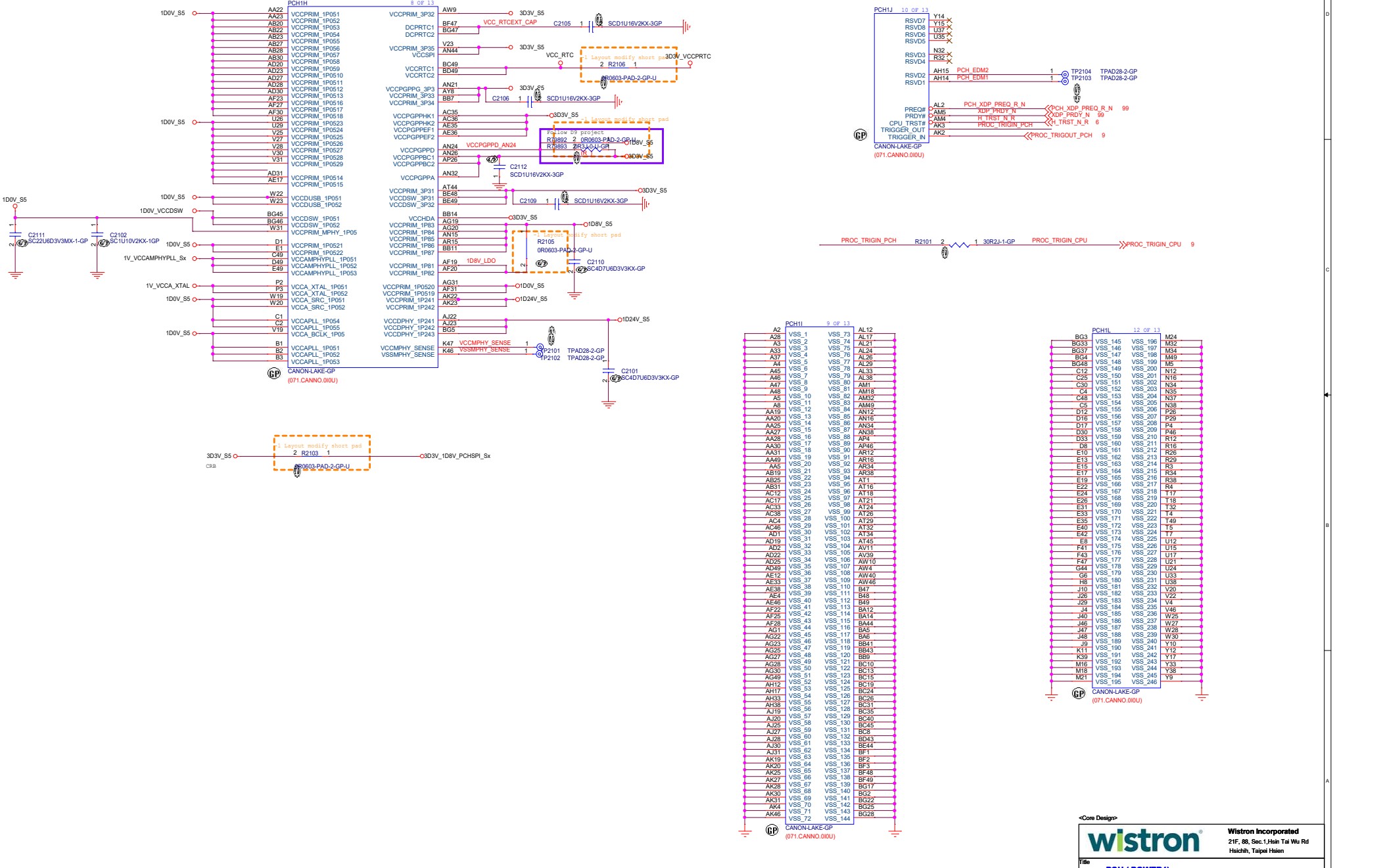

3D3V_S0
Reserved for MOW WW37
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
PCH (GPIO/CPU/SMBUS/IHDA/JTAG)
Consumer AIO Petra238i
Wednesday, July 25, 2018
84.2N702.J31



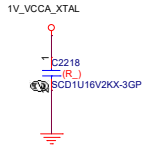
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

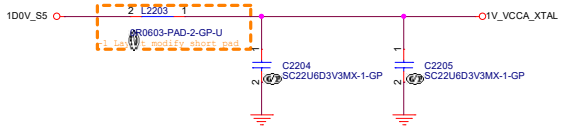
Title: PCH (POWER1)

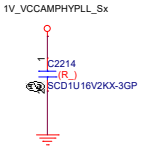
Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 21 of 107

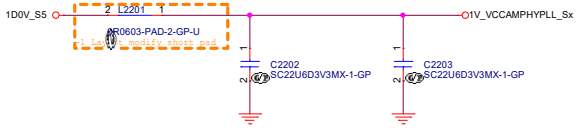


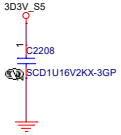
DESIGN NOTE:
BOAED CAP FOR VCCAMPHYPLL
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN C49、D49、E49



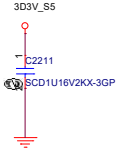


DESIGN NOTE:
BOAED CAP FOR VCCAMPHYPLL
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN C49、D49、E49

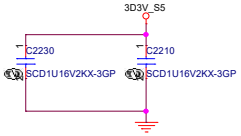




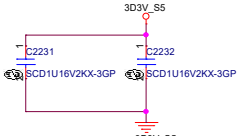
DESIGN NOTE:
EDGE CAP FOR VCCDSW
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BE48 AND BE49



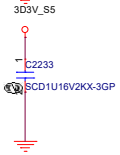
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AE35 AND AE36



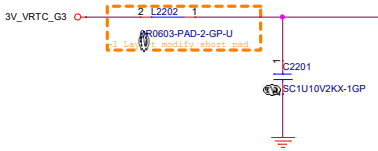
DESIGN NOTE:
EDGE CAP FOR VCCPGPPHK
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AC35 AND AC36

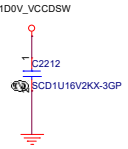


DESIGN NOTE:
EDGE CAP FOR VCCPGPPBC
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN26 AND AP26



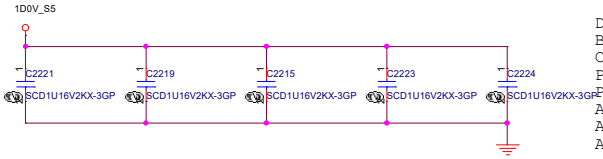
DESIGN NOTE:
EDGE CAP FOR VCCPRIM
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AY8 AND BB7



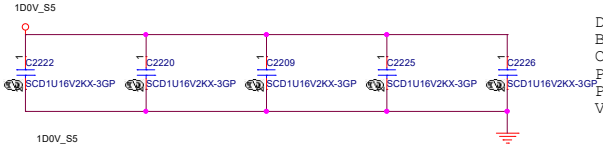


DESIGN NOTE:
BOAED CAP FOR VCCDSW
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BG45、BG46

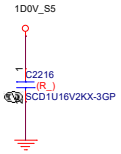
DESIGN NOTE:
EDGE CAP FOR VCCSPI
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN44



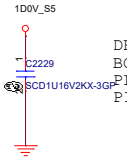
DESIGN NOTE:
BOAED CAP FOR VCCPRIM
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AA22、AA23、AB20、AB22、
AB23、AB27、AB28、AB30、
AD20、AD23、AD27、AD28、
AD30、AF23、AF27、AF30



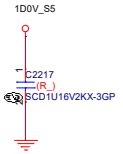
DESIGN NOTE:
BOAED CAP FOR VCCPRIM
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U26、U29、V25、V27、
V28、V30、V31



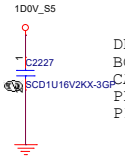
DESIGN NOTE:
BOAED CAP FOR VCCDUSB
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN W22、W23



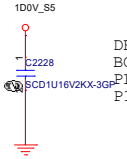
DESIGN NOTE:
BOAED CAP FOR VCCAPLL
PLACE 3~5MM FROM PACKAGE EDGE
PIN B1、B2、B3



DESIGN NOTE:
BOAED CAP FOR VCCPRIM
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN D1、E1



DESIGN NOTE:
BOAED CAP FOR VCCA_SRC
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN W19、W20



DESIGN NOTE:
BOAED CAP FOR VCCAPLL
PLACE 3~5MM FROM PACKAGE EDGE
PIN C1、C2

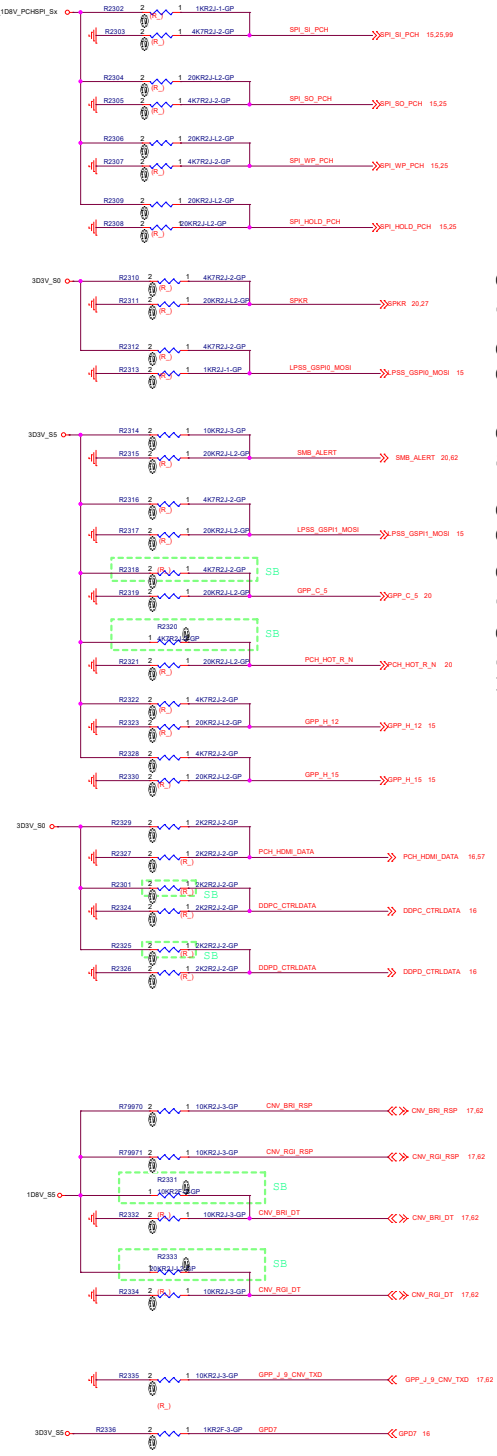
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (POWER&CAP)

Size: Custom | Document Number: Consumer AIO Petra238I | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 22 of 107



SPI0_MOSI

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI0_MISO

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI0_IO2

CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI_HOLD_PCH

PERSONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

GPP_B14
SPKR

TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED
LOW:TOP SWAP DISABLED(DEFAULT)
PCH HAS INTERNAL WEAK PD

CAD NOTE:
USE 3 PAD

GPP_B18
GSPI0_MOSI

NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

GPP_C2
SMBALERT#

TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD

GPP_B22
GSPI1_MOSI

BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
THERE IS A WEAK 15OK PU ON THIS NET
PCH HAS INTERNAL WEAK PD

GPP_C5
SM0ALERT#

ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

GPP_B23
SML1ALERT#
PCHHOT#

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB

ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACHED FLASH SHARING
PCH HAS INTERNAL WEAK PD

GPP_H12
SML2ALERT#

GPP_H15
SML3ALERT#

- GPP_H_15 is JTAG ODT strap. This will be corrected by stuffing external 4.7K PU resistor (R9260).
  - Not implementing this PU may impact ITP debug although we do have external pull ups for JTAG on the RVP.

GPP_I6
DDPB_CTRLDATA
GPP_I8
DDPC_CTRLDATA
GPP_I10
DDPD_CTRLDATA

GPP_F23

- GPP_F23 is connected to 10K PU and it is used as GPIO_WiFi_SSD_RESET

HDA_SDO
I2S0_TXD

GPP_H17
DPPF_CTRLDATA

- GPP_H_17 is muxed with SML4_DATA and not DDPF_CTRLDATA.
  GPP_H_17 is not a PCH strap in the latest CNP-H pinlist description.

GPP_J4
CNV_BRI_DT
UART0_RTS#

GPP_J6
CNV_RGI_DT
UART0_TXD

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

GPD7

XTAL INPUT MODE
HIGH:XTAL INPUT IS DIFFERENTIAL
LOW:XTAL INPUT IS SINGLE-ENDED
PCH HAS INTERNAL 20K PD

HDA_SDO
I2S0_TXD

ME disable

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SM0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_C-TRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_C-TRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH_(STRAP)

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 23 of 107

AMP

27 AMP_MUTE_SIO

LPC

19 LPC_SERIRQ_PCH
19,68 LPC_AD_SIO_P0
19,68 LPC_AD_SIO_P1
19,68 LPC_AD_SIO_P2
19,68 LPC_AD_SIO_P3
19,68 LPC_FRAME#_SIO
15,95 LPC_PME#

Power Manager

20,65,99 RSMRST#_SIO
20,40,41,50,54,95 PM_SLP_S3#
8,20,39,40 SLP_S4_N
64,99 PWRBTN_IN
20 PM_PWRBTN#
15,65,68,76 PLTRST#_PCH
40,43 S0_PWR_GOOD
16,76,86 DGPU_PWROK
40,48 IMVP8_EN

Panel ID

66,95 PNL_ID2
66,95 PNL_ID1
66,95 PNL_ID0

CLOCK

19 CLK_CLKIN_SIO
19 CLK_PCICLK_SIO

SMBUS

20,79 SML1CLK_PCH
20,79 SML1DATA_PCH

66 SMBCLK2_SIO
66 SMBDAT2_SIO

HW Monitor

26 CPU_FANTACH1
26 CPU_FANCTL1

6,43 PROCHOT#_ECIO

Codec

PECI

6,17 PECI_CPU

Others Function

20,40,57,95 PM_SLP_S5#
20 RTCRST_ON
6,43 PROCHOT#_SIO
62 LAN_EN_PWR_SIO
56,95 DET_HDMI#
59 SCALAR_EN
34 1012C_EN1
41,66 CTRL0_EUP
16 EC_SMI#
16 EC_ROTATE_SMI1#
64 TURN_OFF_PWM
55,66 BKLT_EN
36 EC_USB_POWER_EN
19 RSRST#
64 SUBLED_N
25 SPI_WP_R_N
20,27 HDA_RST#_CODEC
62 PCIE_WLAN_WAKE#
31 PLTRST_LAN
63 PLT_M2_SSD_RST#
62 PLT_WLAN_RST#
16,76 SIO_DGPU_HOLD_RST#
95 SIO_UART1_RX
95 SIO_UART1_TX
34 CONF1_SCL1
34 CONF2_SDA1
49 ECIO_12V_EN
37 TOUCH_CT

16,76 BOARD_ID_2

To SB 3/5 EUP control

3D3V_A
R24068 10KR2J-3-GP
CTRL0_EUP
Q24003 2N7002K-2-GP
R24047 10KR2J-3-GP
EC_EUP_EN
C24022 SCD1U16V2KX-3GP
R24054 0R0402-PAD-2-GP
CTRL0
D24001 AZ5125-02S-R7G-GP
C24005 SCD1U16V2KX-3GP
SB

Power Good 3V

0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms

3D3V_S0
R24015 1KR2J-1-GP
S0_PWR_GOOD
R24016 0R0402-PAD-2-GP
PWROK3_1_R
R24009 33R2J-2-GP
R24022 10KR2J-L2-GP
C24003 SC100P50V2JN-3GP
C24010 SCD1U16V2KX-3GP
C24013 SCD1U16V2KX-3GP
C24012 SC2D2U6D3V2MX-GP
D24003 AZ5123-01H-GP
EC2401 SC27P50V2JN-2-GP

HDMI IN DET

Connect High
Normal Low
R24005 100KR2J-1-GP
Q24001 2N7002K-2-GP
R24007 10KR2J-3-GP
DET_HDMI#
HDMI_IN_DET#_R
R24006 100KR2J-1-GP
(63.10234.10L)
Connect Low
Normal High

ECIO SPI ROM

U2402
W25X10CLSNIG-GP
(72.25106.601)
R24050 10KR2J-3-GP
R24051 10KR2J-3-GP
R24052 10KR2J-3-GP
R24038 10KR2J-3-GP
R24039 10KR2J-3-GP
R24040 10KR2J-3-GP
C24007 SCD1U16V2KX-3GP
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash

HW Monitor Thermal

SIO_VREF
R24063 10KR2F-2-GP
REMOTE1+
R24091
R24090
R24062 10KR2F-2-GP
DIMM_TMPIN2
R2402
NTC-10K-27-GP-U
C24025 SCD1U16V2KX-3GP
R24033 10KR2F-2-GP
GPU_PIN3_R
R24034
C24026 SCD1U16V2KX-3GP
Layout Note: place it near CPU VORE MOS
Layout Note: place it near PCH
Layout Note: place it near GPU
REMINE LAYOUT
R24044 0R0402-PAD-2-GP

HW Monitor Voltage

VCC_CORE
HM_VCCP_R
R24037 10KR2F-2-GP
HM_VCCP
G24001 COPPER-CLOSE-GP-U
C24017 SCD1U16V2KX-3GP
VDDQ
SIO_VIN1
R24070 10KR2F-2-GP
C24027 SCD1U16V2KX-3GP
SIO_VIN4
R24045 6K49R2F-1-GP
R24046 10KR2F-2-GP
C24019 SCD1U16V2KX-3GP
SIO_VIN2
R24042 56KR2F-GP
R24043 10KR2F-2-GP
C24018 SCD1U16V2KX-3GP
SIO_VIN5
R24048 17K8R2F-GP
R24049 10KR2F-2-GP
C24020 SCD1U16V2KX-3GP
SIO_VIN3
R24053 17K8R2F-GP
R24024 10KR2F-2-GP
C24021 SCD1U16V2KX-3GP

For AC OFF SEQUENCE

3D3V_S5
R24059 (63.47234.1DL)
PWRGD_PS_L1
R24058 100KR2J-1-GP
DCBATOUT
Q2402 2N7002KDW-1-GP
R24057 10KR2J-L2-GP
PWRGD_PS_L2
C24023 SCD1U16V2KX-3GP
R24073 0R0402-PAD-2-GP
R24061 (63.10334.1DL)
SIO_ATXPG

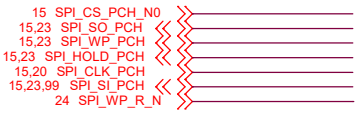
PWRBT Signal

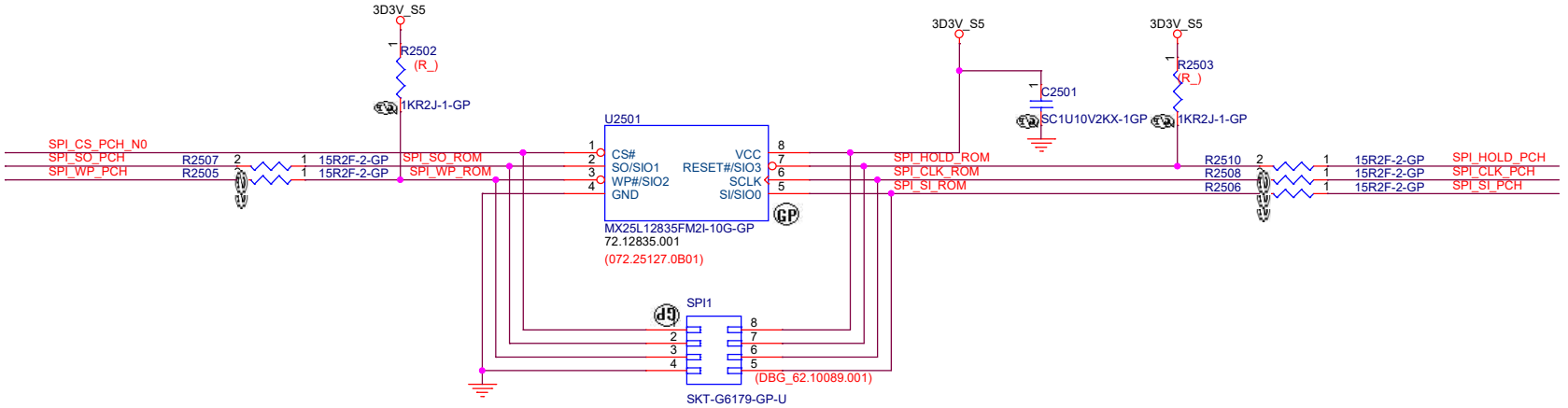
PB_IN_N_1
R24026 0R0402-PAD-2-GP
PWRBTN_IN
R24027 10KR2J-2-GP
SW_ON_N_SIO
R24025 0R0402-PAD-2-GP
PM_PWRBTN#

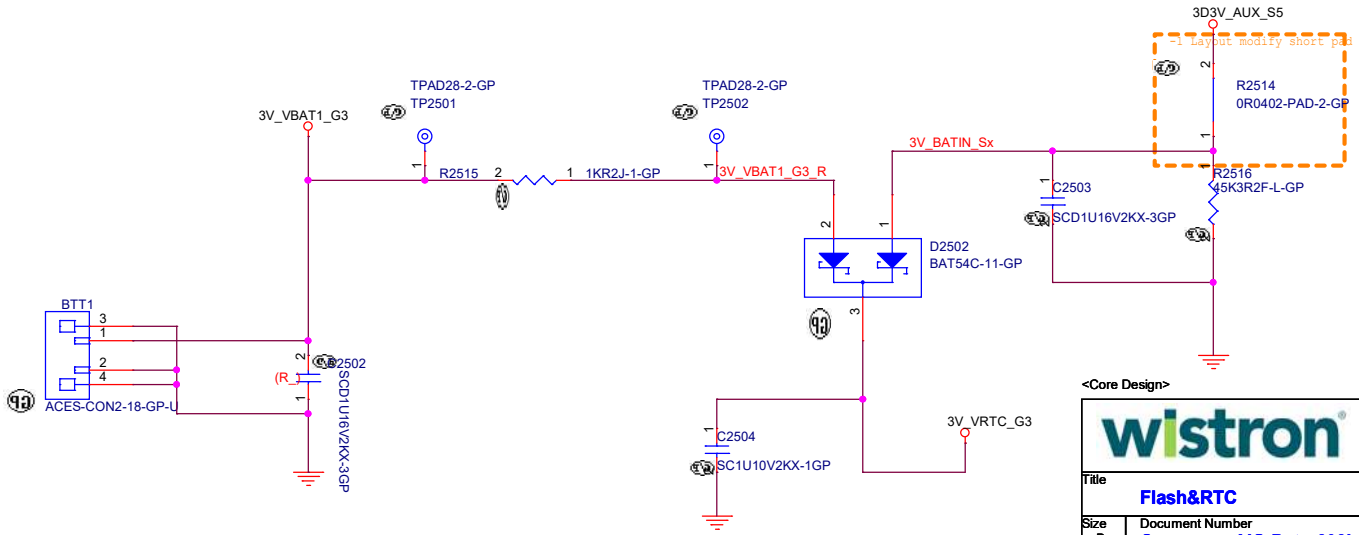
<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: SIO ITE8732F-CX
Size: C
Custom
Document Number: Consumer AIO Petra238I
Rev: 1A
Date: Wednesday, July 25, 2018
Sheet 24 of 107







<Core Design>

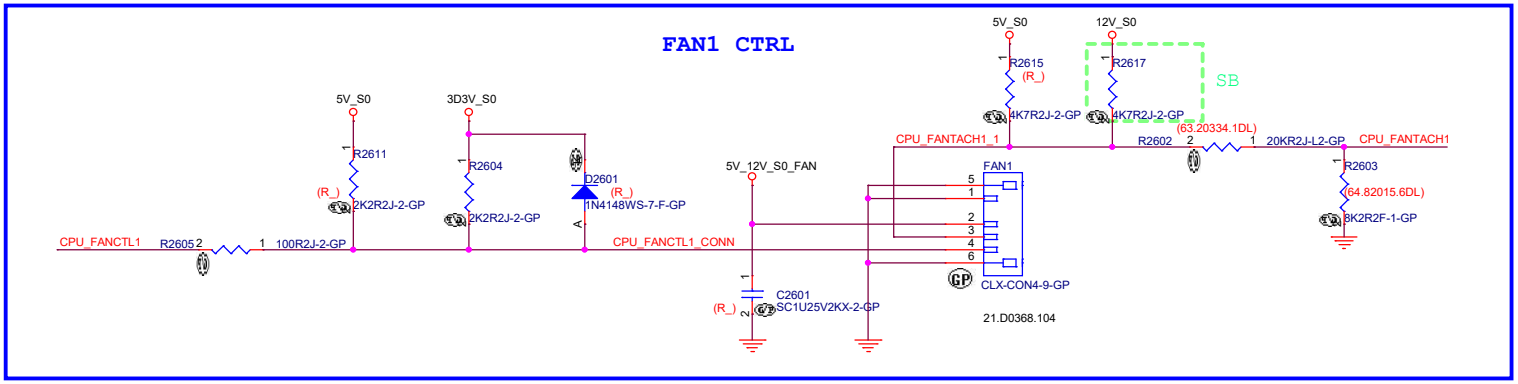
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Flash&RTC

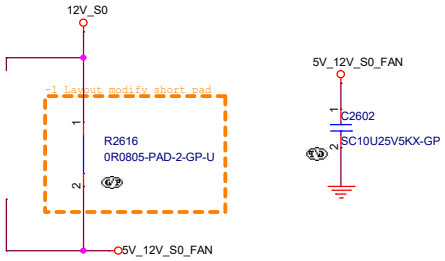
Size: B | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 25 of 107



24 CPU_FANCTL1

24 CPU_FANTACH1



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thermal & FAN

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 26 of 107

AUDIO I2S BUS to I2C Switch

95 I2S_OUT_R
95 I2S_BCLK_R
95 I2S_MCLK_R
95 I2S_LRCK_R

PCH SPKR

20,23 SPKR

HDA

20 HDA_BITCLK_CODEC
20,24 HDA_RST#_CODEC
20 HDA_SDIN0_PCH
20 HDA_SDOUT_CODEC
20 HDA_SYNC_CODEC

DMIC

37 DMIC_DATA2
37 DMIC_CLK2
37 DMIC_DATA
37 DMIC_CLK

F_HPO_Switch Siganl

HP LINE OUT TO MUX SEL

DB board Siganl

66 FM_L_CODEC
66 FM_R_CODEC
66 JD_HP
66 MIC_VREFL
66 COMBO_JACK

EC I2C Control

24,27 AMP_MUTE_SIO

95 SCALAR_HP_OUT_R_2
95 SCALAR_HP_OUT_L_2
95 PC_MONITOR_SW
66 F_HPO_L*
66 F_HPO_L
66 F_HPO_R*
F_HPO_R

Near AVDD1 and AVDD2 power source point

Tied at one point only under Codec or near the Codec

Moat

Analog Moat | Digital Moat

Digital_ground

Analog_ground

Moat

PG2701 Place at Codec bottom side.

PG2702 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

HP Out Switch

+3D3V_SCALAR_PWR

L:Monitor H: PC

Vmin = Vin - 5.5V

HP Source SEL

Combo Audio Jack

5V_S0

Add this Filter to avoid other components clips be influenced

ALC286_PVDD1

ALC286_PVDD2

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

Close to codec PIN

IIS out to Switch

I2S_OUT_R
I2S_BCLK_R
I2S_MCLK_R
I2S_LRCK_R

IISC From IC Codec ALC286 Layout Resistor Closed IC

3D3V_S0

+AUD_DVDD_1

DVDD-IO

V_5_CODEC

AUDIO1

ALC286-VC1-CG-GP

(071.0286M.0003)

Front Combo MIC in

RSVD to control

Front HP sense

NC for fixed type headset

AGND/DGND moat:

AGND

DGND

ALC286-VC1-CG-GP

***1.8V power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Pls make sure that switching frequency operates at out-band(Over 20KHz).

1D8V_CODECS0

Near codec

Modified to AGND 2015-8-15

20121011_aPisa_SB Charles Modify

ALC286 spec sequence requirement:

V

t

5v

3.3V

1.8V

1.2V

2.25V

0.75v

>1.65V

AVDD1/PVDD

DVDD

PD pin

VREF

AVDD2/CPVDD

LDO3

T1

T2

T1>=0mS

T2<=5mS

PWR_1D8V

Iomax=0.21A

<Core Design>

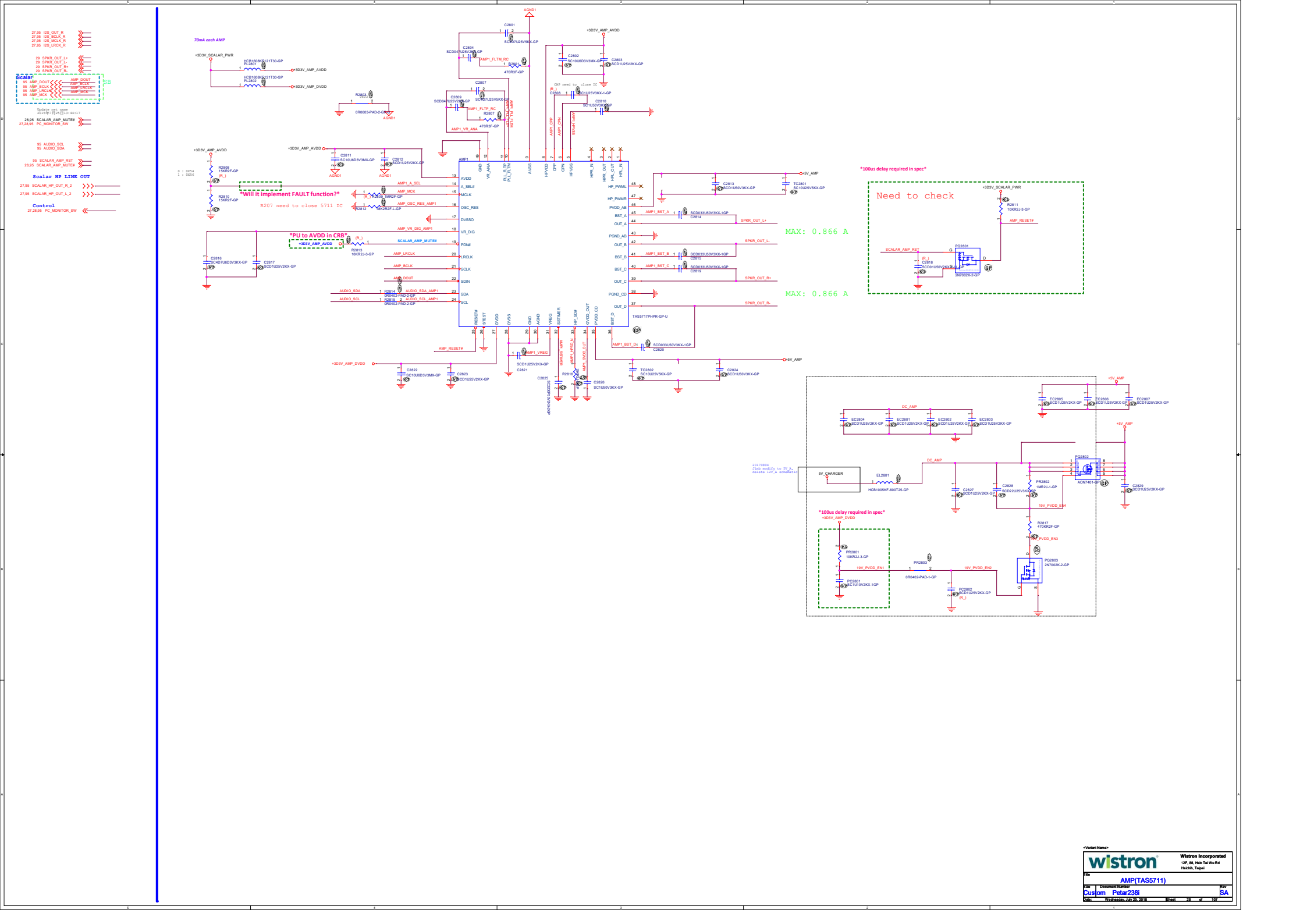
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO_ALC269Q

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 27 of 107


Scalar
Scalar HP LINE OUT
Control
70mA each AMP
Will it implement FAULT function?
R207 need to close 5711 IC
PU to AVDD in CRB
MAX: 0.866 A
MAX: 0.866 A
100us delay required in spec
Need to check
100us delay required in spec
TAS5717PHPR-GP-U
DC_AMP
5V_CHARGER
Wistron Incorporated
AMP(TAS5711)
Custom
Petar238i

28 SPKR_OUT_L+
28 SPKR_OUT_L-
28 SPKR_OUT_R+
28 SPKR_OUT_R-

LC need to close AMP IC

PBY201209T-221Y-N
Z=220 ohm,Rdc=0.05 ohm
I=3A ,0805

SPKR_OUT_L+ — L2901 HCB2012KF-800T50-GP-U — SPKR_OUT_L+_C — C2901 SC1KP50V2KX-1GP
SPKR_OUT_L- — L2902 HCB2012KF-800T50-GP-U — SPKR_OUT_L-_C — C2903 SC1KP50V2KX-1GP
SPKR_OUT_R+ — L2903 HCB2012KF-800T50-GP-U — SPKR_OUT_R+_C — C2907 SC1KP50V2KX-1GP
SPKR_OUT_R- — L2904 HCB2012KF-800T50-GP-U — SPKR_OUT_R-_C — C2908 SC1KP50V2KX-1GP

PBY201209T-221Y-N
Z=220 ohm,Rdc=0.05 ohm
I=3A ,0805

To select appropriate beads
2015年7月25日17:20:56

SPK1 ACES-CON4-85-GP

D2901 AZ5125-02S-R7GP (R_)
SPKR_OUT_L+_C
SPKR_OUT_L-_C

D2902 AZ5125-02S-R7GP (R_)
SPKR_OUT_R+_C
SPKR_OUT_R-_C

SPKR_OUT_L+ — R2901 (64.22R05L) 18R3F-GP — SPKR_OUT_L+_CR — C2902 SC330P50V2KX-3GP
SPKR_OUT_L- — R2902 (64.22R05L) 18R3F-GP — SPKR_OUT_L-_CR — C2904 SC330P50V2KX-3GP
SPKR_OUT_R+ — R2903 (64.22R05L) 18R3F-GP — SPKR_OUT_R+_CR — C2905 SC330P50V2KX-3GP
SPKR_OUT_R- — R2904 (64.22R05L) 18R3F-GP — SPKR_OUT_R-_CR — C2906 SC330P50V2KX-3GP

Need to check Pin define

<Variant Name>

wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Audio Speak&Woofer
Size: B | Document Number: Petar238i | Rev: SA
Date: Wednesday, July 25, 2018 | Sheet 29 of 107

RSVD

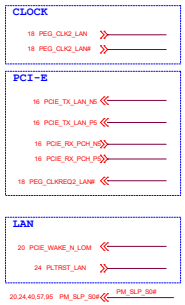
<Variant Name>

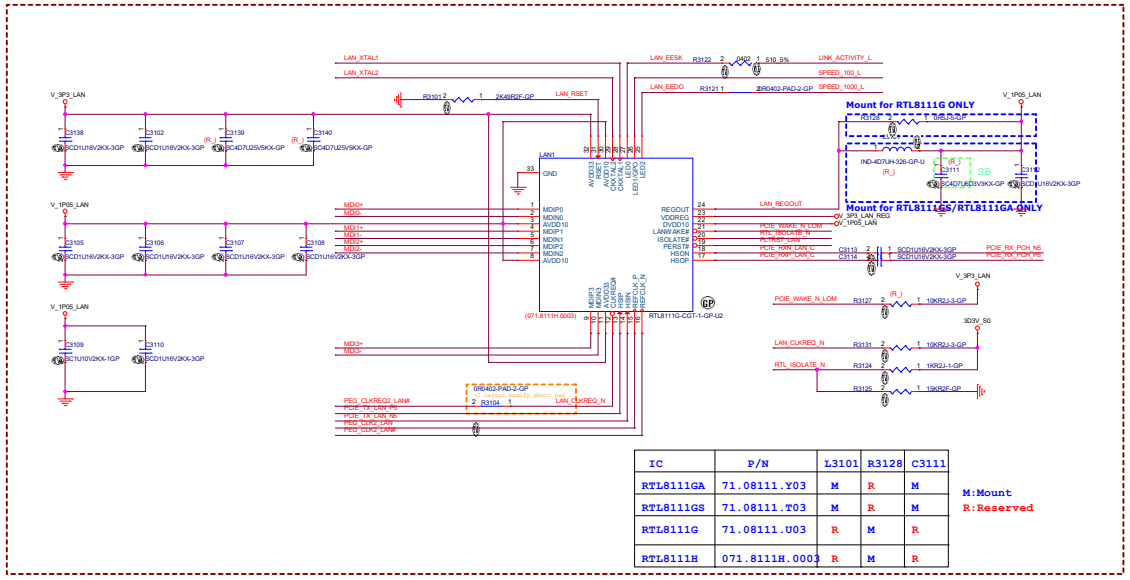
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Audio Speak&Woofer

Size	Document Number	Rev
B	Consumer AIO Petra238i	1A

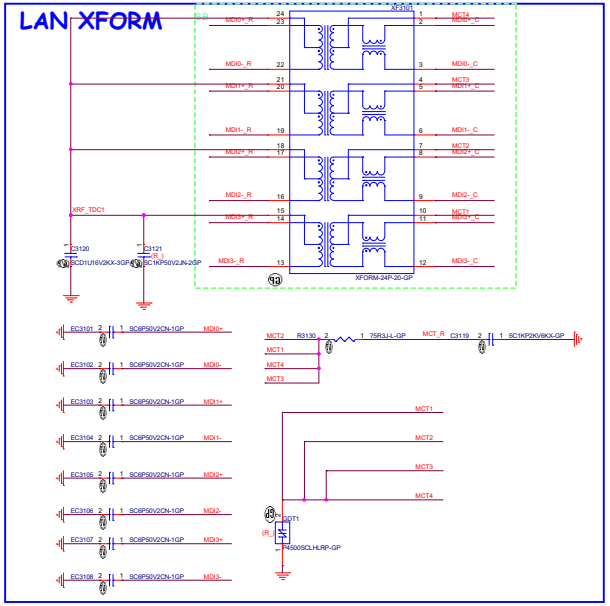
Date: Wednesday, July 25, 2018 Sheet 30 of 105

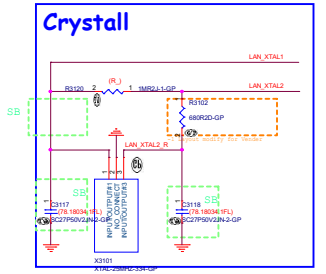


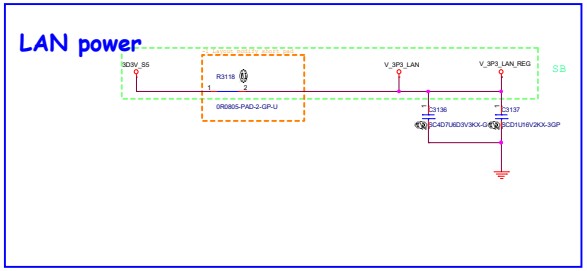


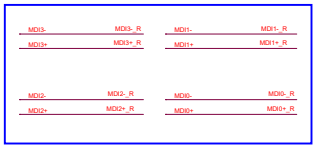
IC	P/N	L3101	R3128	C3111
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R
RTL8111H	071.8111H.0003	R	M	R

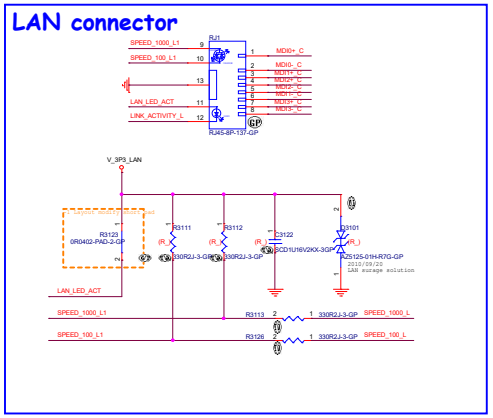
M:Mount
R:Reserved

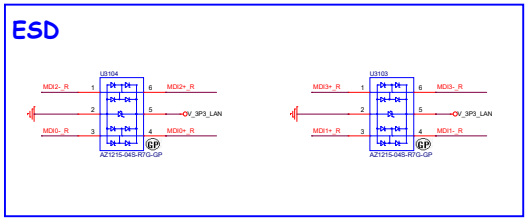


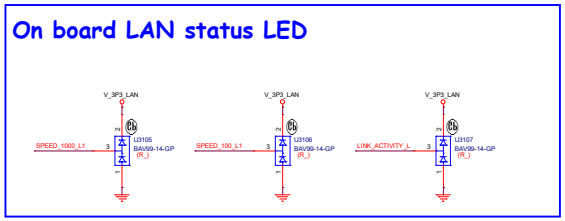












Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RJ45&Transformer

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 32 of 107

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

Card reader BH611FJ1LN

Size	Document Number	Rev
C	Consumer AIO Petra238i	1A

Date: Wednesday, July 25, 2018 Sheet 33 of 107

USB3.1 PCH signal

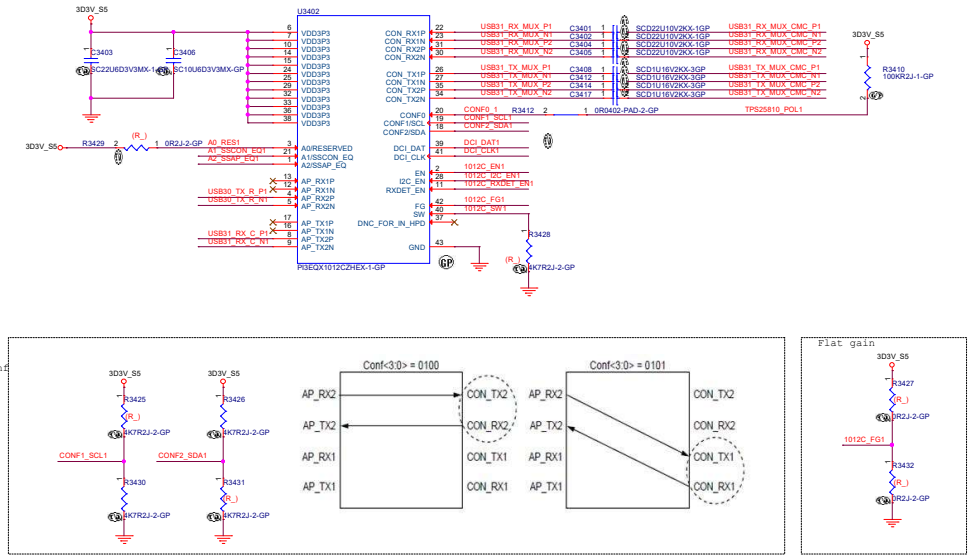
19 USB30_TX_R_N1
19 USB30_TX_R_P1
19 USB31_RX_C_N1
19 USB31_RX_C_P1

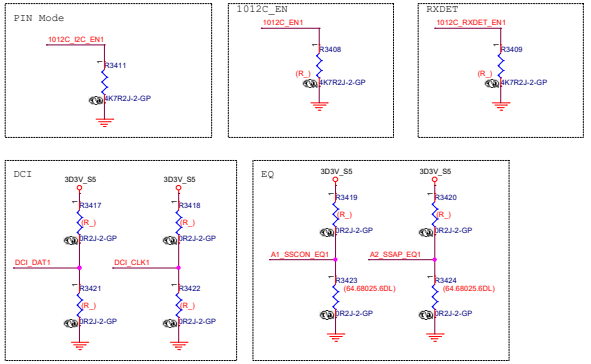
USB2.0 Siganl

16 USB_PCH_PN1
16 USB_PCH_PP1

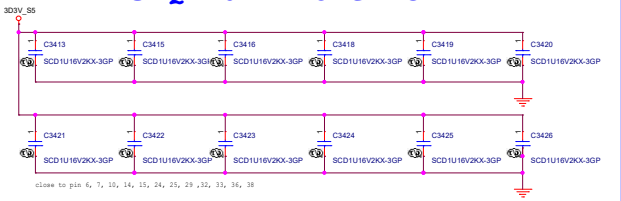
Control Siganl

24 1012C_EN1
36 USB_EN
24 CONF1_SCL1
24 CONF2_SDA1



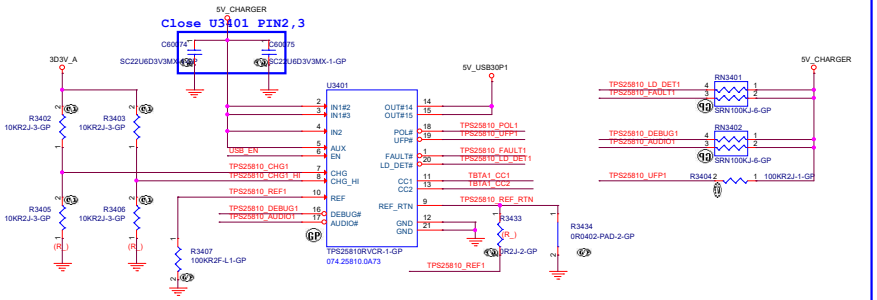


PI3EQX1012 Power CAP

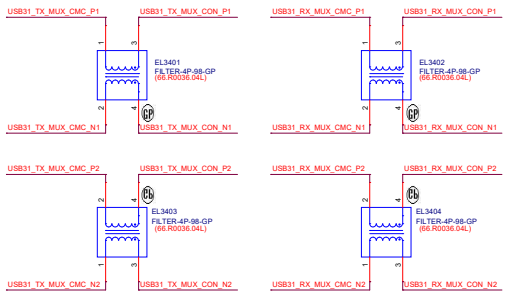


Front USB3.1 Type C Channel Configuration

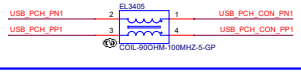
Close U3401 PIN2,3



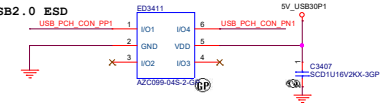
USB3.1 EMI



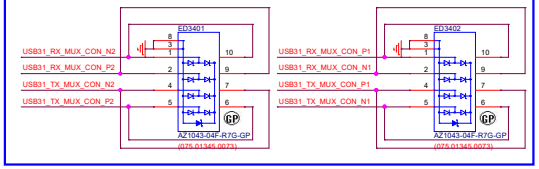
USB2.0 EMI



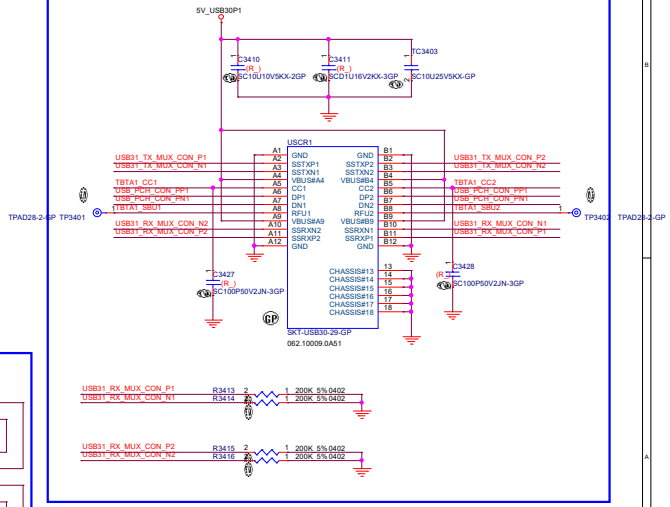
USB2.0 ESD



USB3.1 ESD



USB3.0 Type C connector



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB MUX Switch PI5USB30213

Size	Document Number	Rev
Custom	Consumer AIO Petra238I	1A

Date: Wednesday, July 25, 2018 Sheet 34 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB_Redrive_(R)

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 35 of 107

USB over current siganl

16 USB30_OC0#

16,36 USB30_OC1#

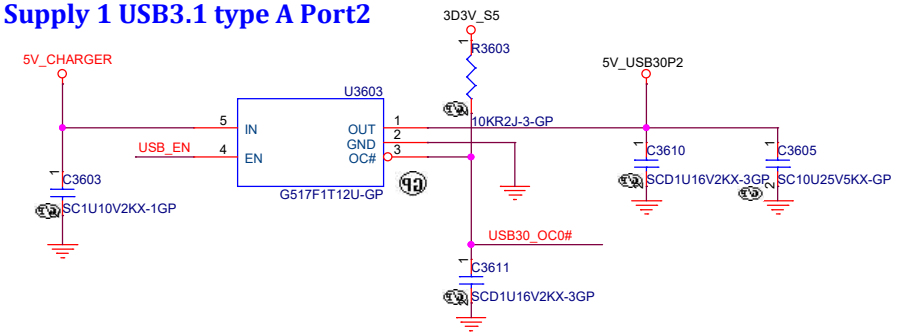
USB power control siganl

8,20,24,40 SLP_S4_N

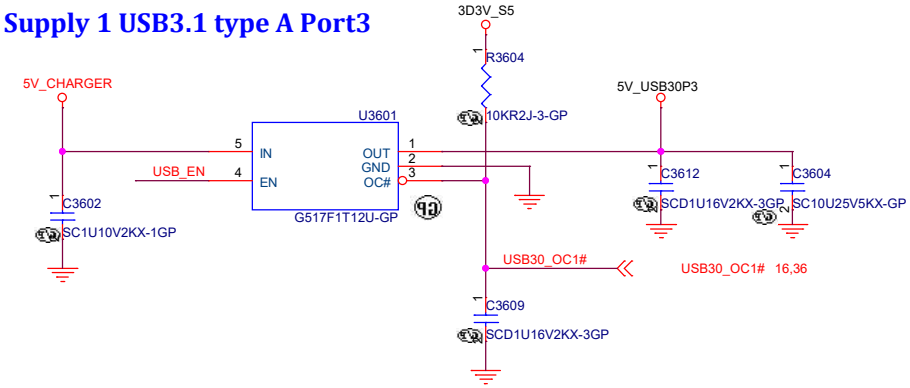
24 EC_USB_POWER_EN

34 USB_EN

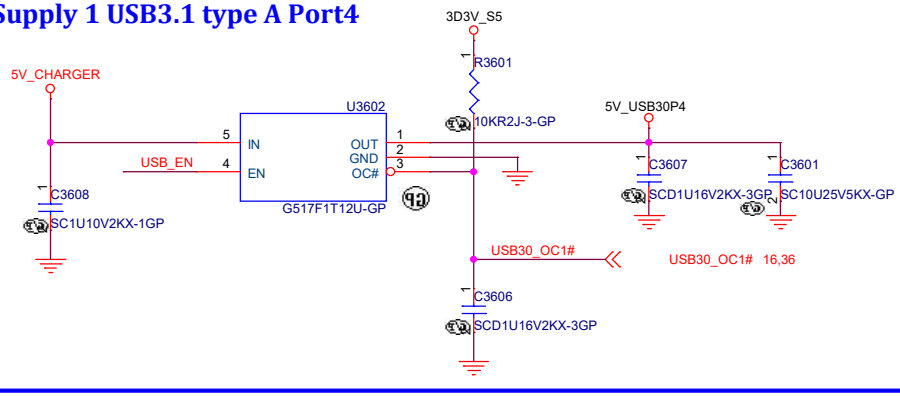
Supply 1 USB3.1 type A Port2



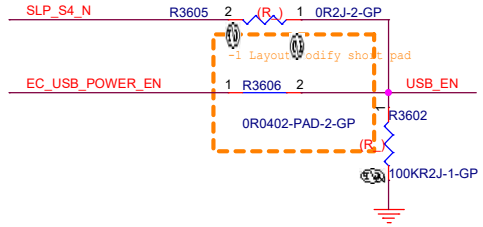
Supply 1 USB3.1 type A Port3



Supply 1 USB3.1 type A Port4



USB3.1 Power control



<Core Design>

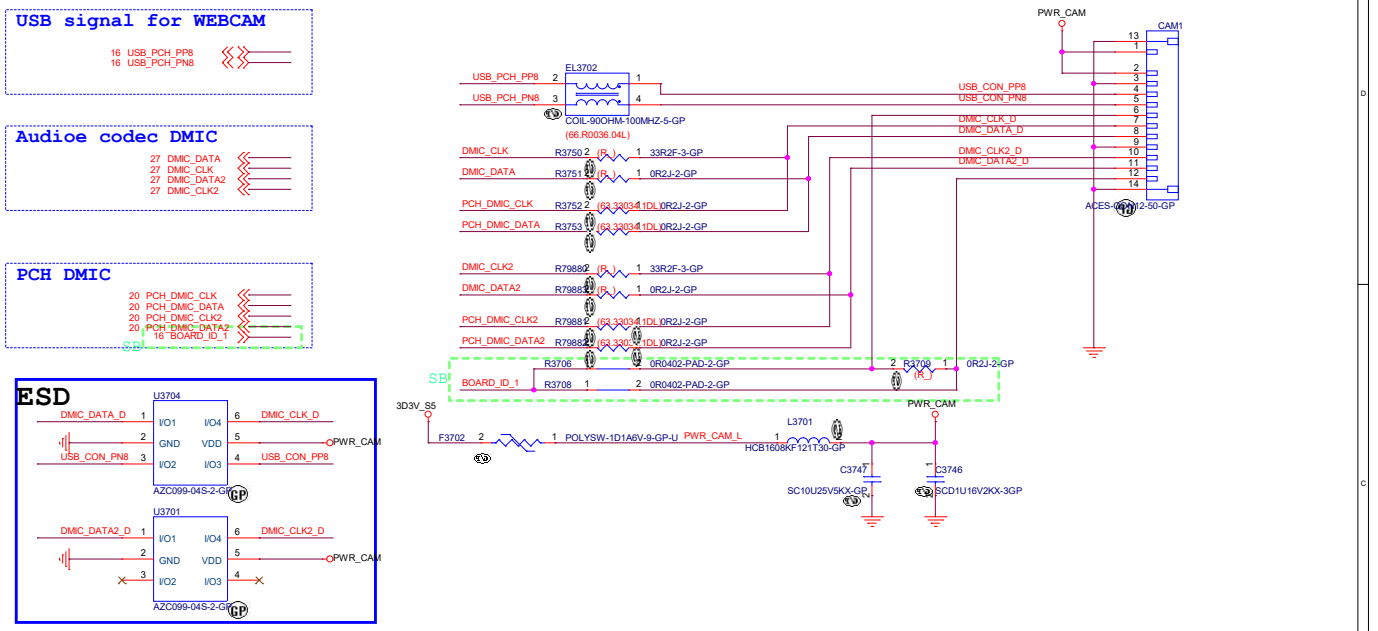
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Switch power

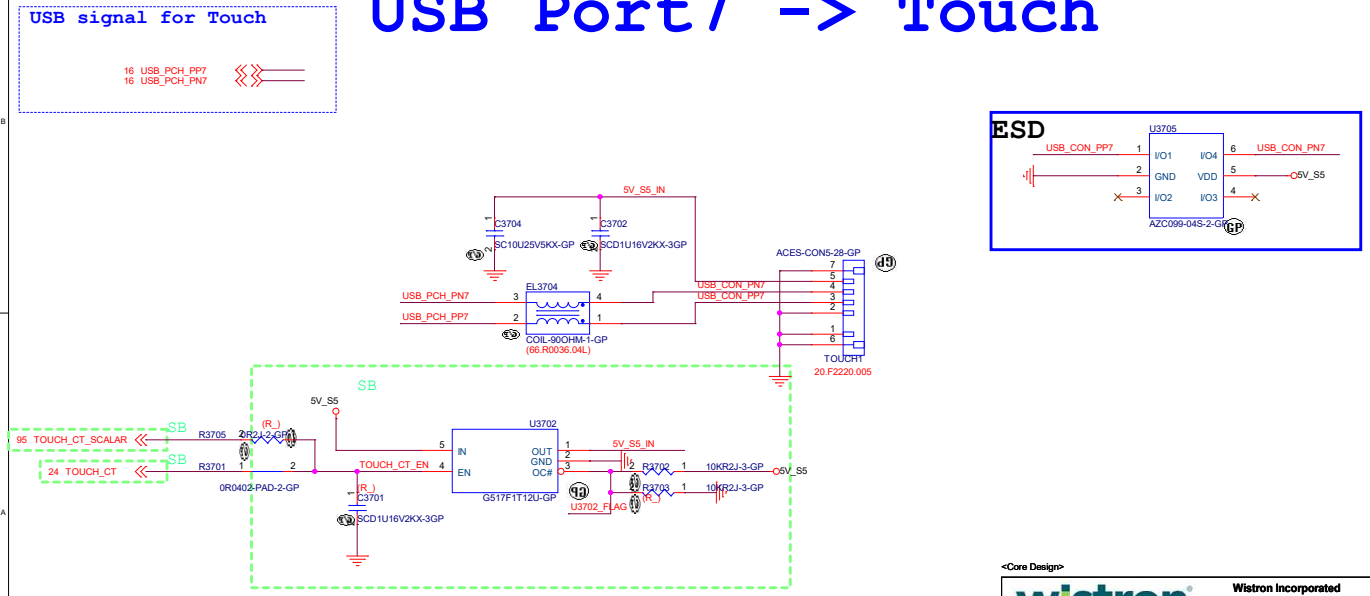
Size: B | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 36 of 107

USB Port8 -> WEBCAM



USB Port7 -> Touch



<Core Design>

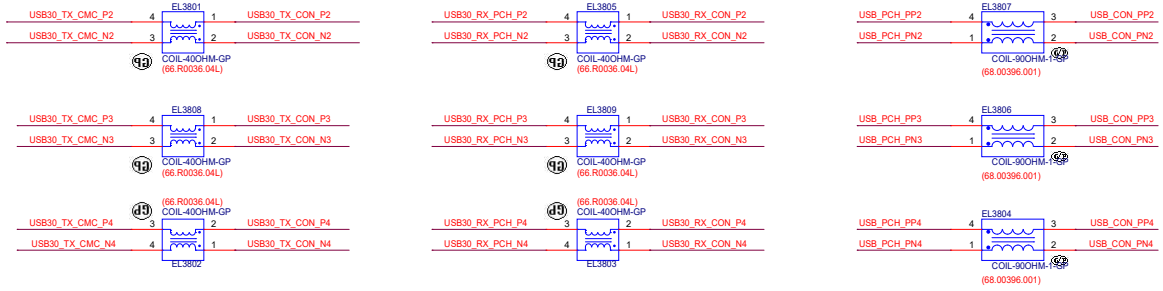
wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	USB20_FRONT HEADER
Size: Custom	Document Number: Consumer AIO Petra238i
Rev	1A
Date: Wednesday, July 25, 2018	Sheet 37 of 107

USB 3.1 signal

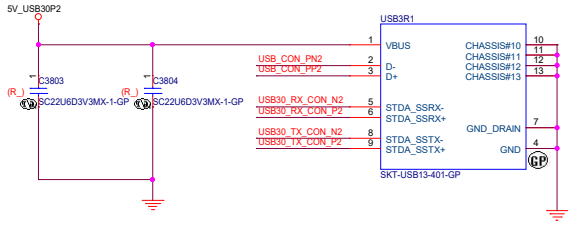
19 USB30_RX_PCH_N2
19 USB30_RX_PCH_P2
19 USB30_TX_CMC_N2
19 USB30_TX_CMC_P2
19 USB30_RX_PCH_N3
19 USB30_RX_PCH_P3
19 USB30_TX_CMC_N3
19 USB30_TX_CMC_P3
19 USB30_TX_CMC_N4
19 USB30_TX_CMC_P4
19 USB30_RX_PCH_N4
19 USB30_RX_PCH_P4

USB 2.0 signal

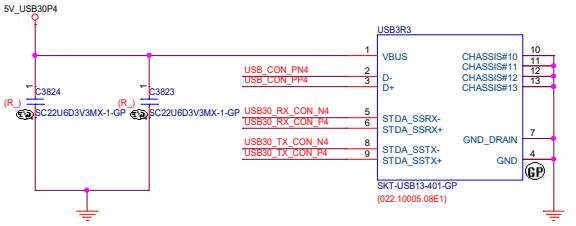
16 USB_PCH_PP2
16 USB_PCH_PN2
16 USB_PCH_PP3
16 USB_PCH_PN3
16 USB_PCH_PP4
16 USB_PCH_PN4



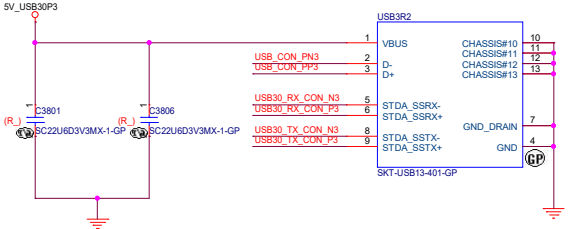
USB3.1 REAR PORT1



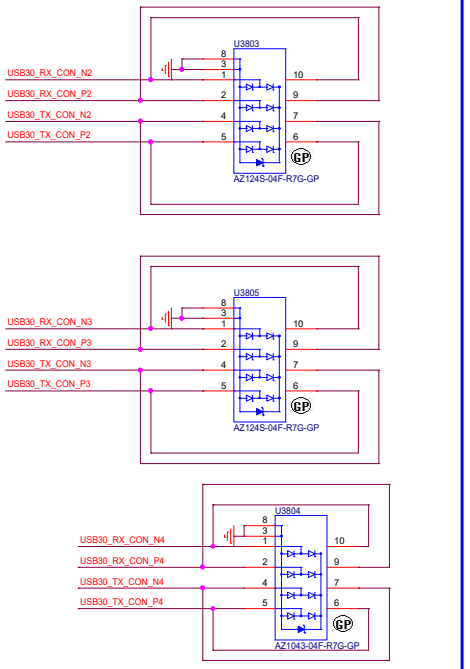
USB3.1 REAR PORT3



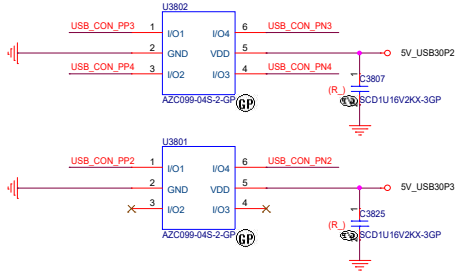
USB3.1 REAR PORT2



ESD



ESD



USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_REAR PORT

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 38 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: USB30_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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50 VTT_EN

50 VDDQ_EN

54 VPP_EN

54 P2V5_VPP_PG

8,20,24,36 SLP_S4_N

50 DDR_VTT_CNTL_CPU

53 VCCIO_EN

50 PWR_VDDQ_PG

40,46 VCORE_PG

52 VCCSA_PG

6,99 CPU_VCCST_PWRGD

20,65 PCH_PWROK

24,43 S0_PWR_GOOD

40,46 VCORE_PG

20,24,41,50,54,95 PM_SLP_S3#

20,65,99 PCH_SYSPWROK

24,48 IMVP8_EN

40,53 VCCIO_PWRGD

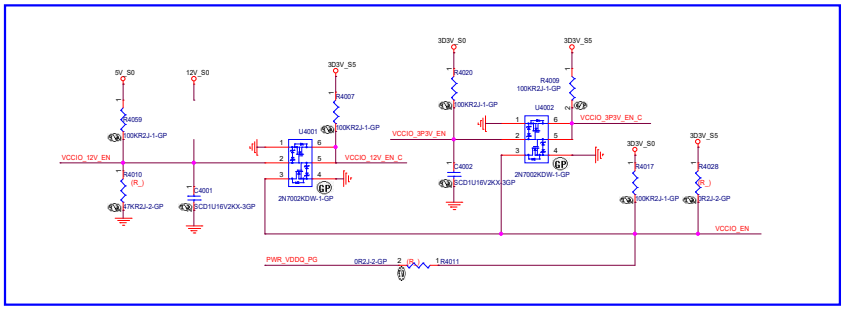
40,53 VCCIO_PWRGD

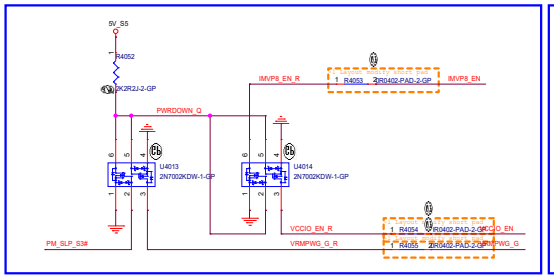
40,46 VCORE_PG

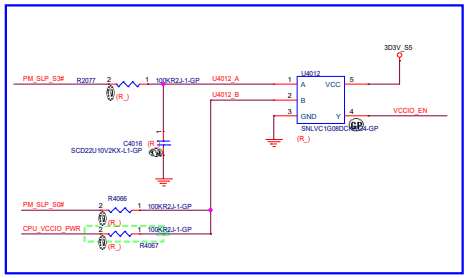
52 VCCSA_EN

20,24,57,95 PM_SLP_S0#

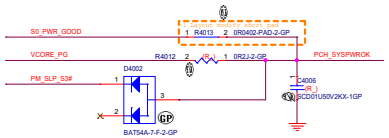
17 CPU_VCCIO_PWR

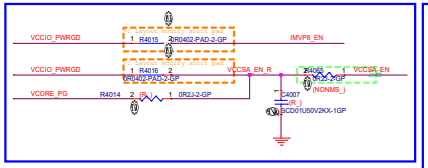


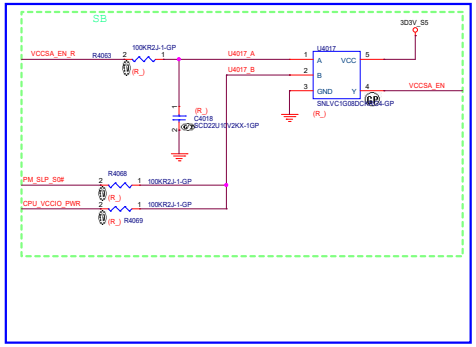




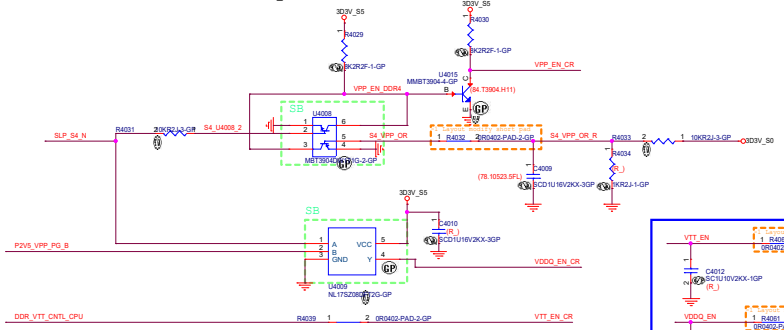
Power Sequence

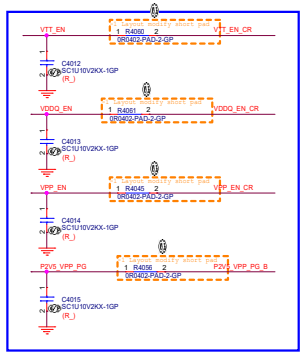


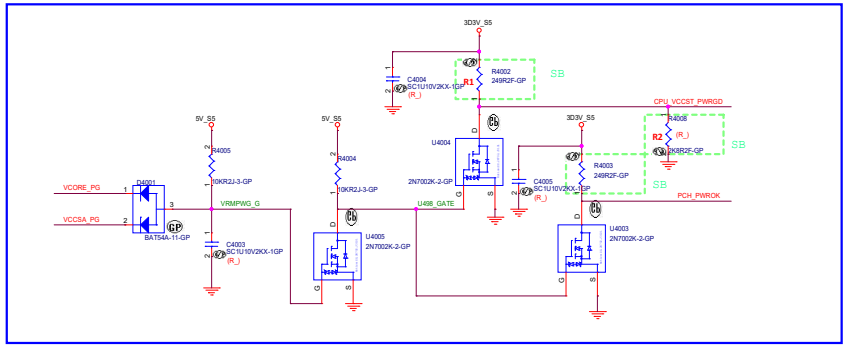




2014/11/11 DDR4 Sequence







<Core Design>

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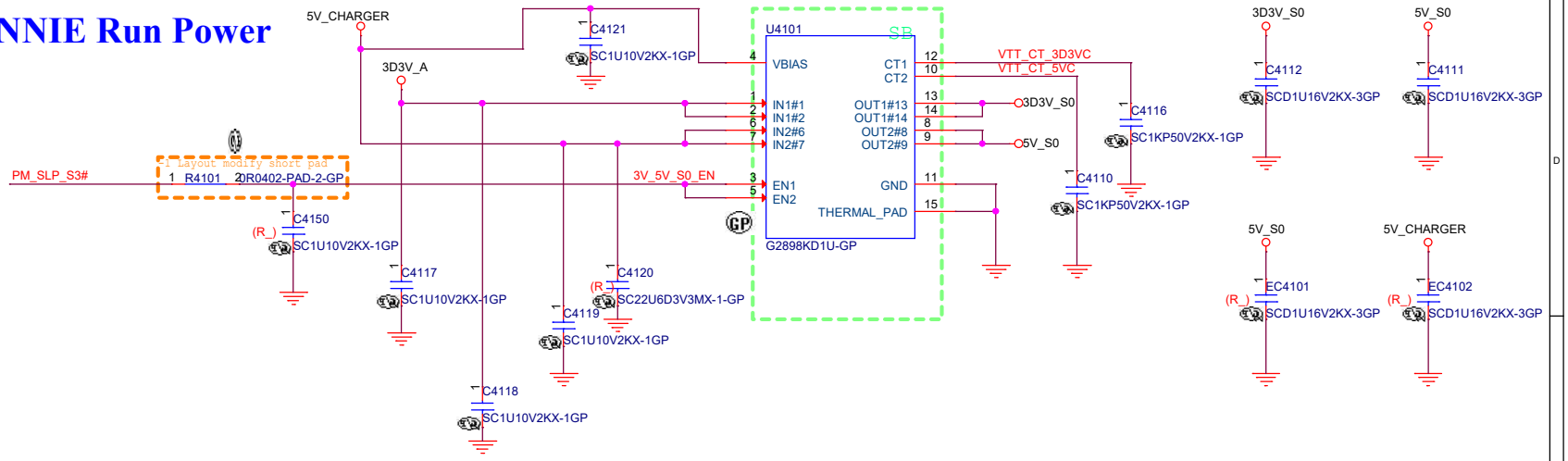
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Power Plane EN Sequence

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 40 of 107

ANNIE Run Power

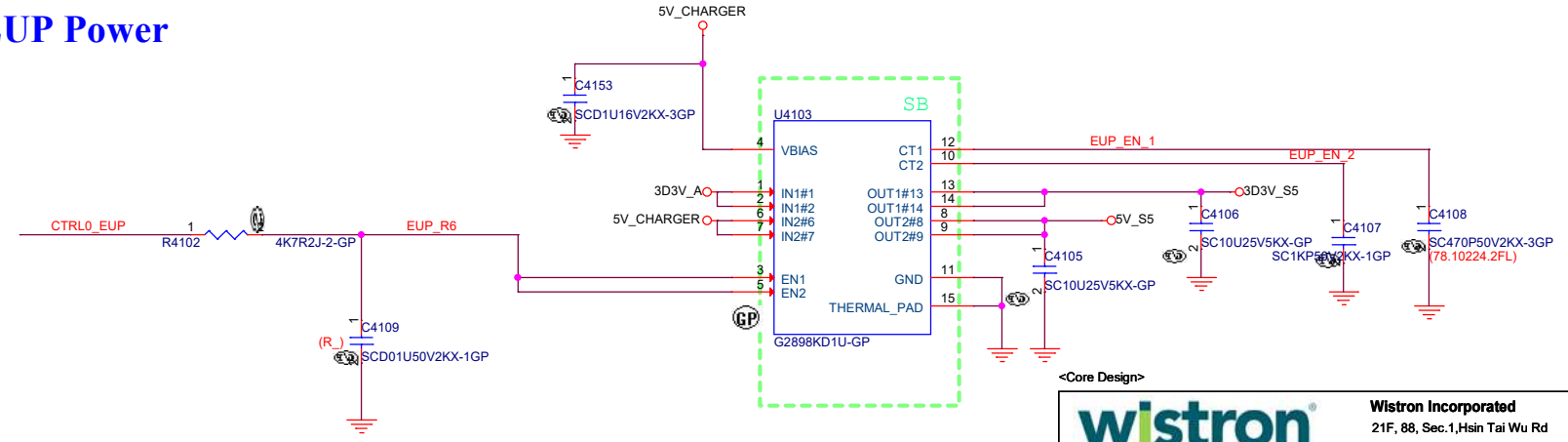


20,24,40,50,54,95 PM_SLP_S3#

17,40 CPU_VCCIO_PWR

20,24,40,57,95 PM_SLP_S0#

EUP Power



24,66 CTRL0_EUP

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Switch power_DS3

Size: B | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 41 of 107

RSVD

<Core Design>

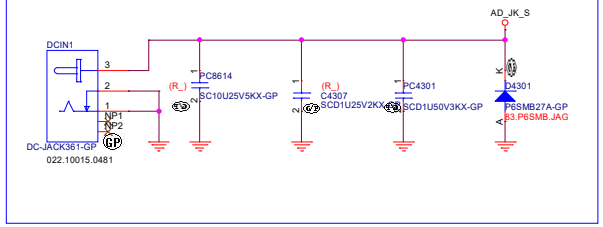
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: RSVD

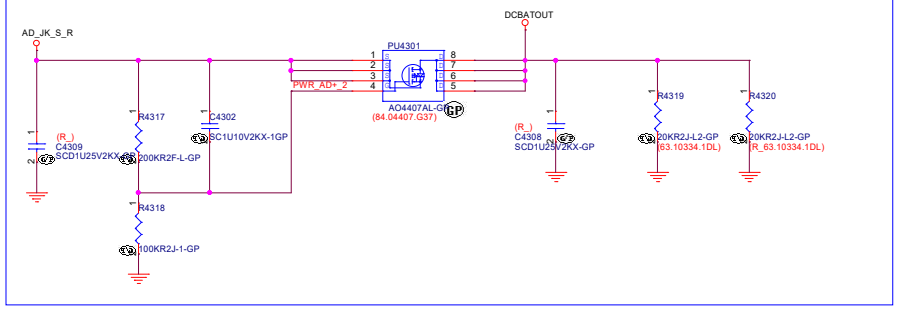
Size: B | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 42 of 107

ANNIE solution



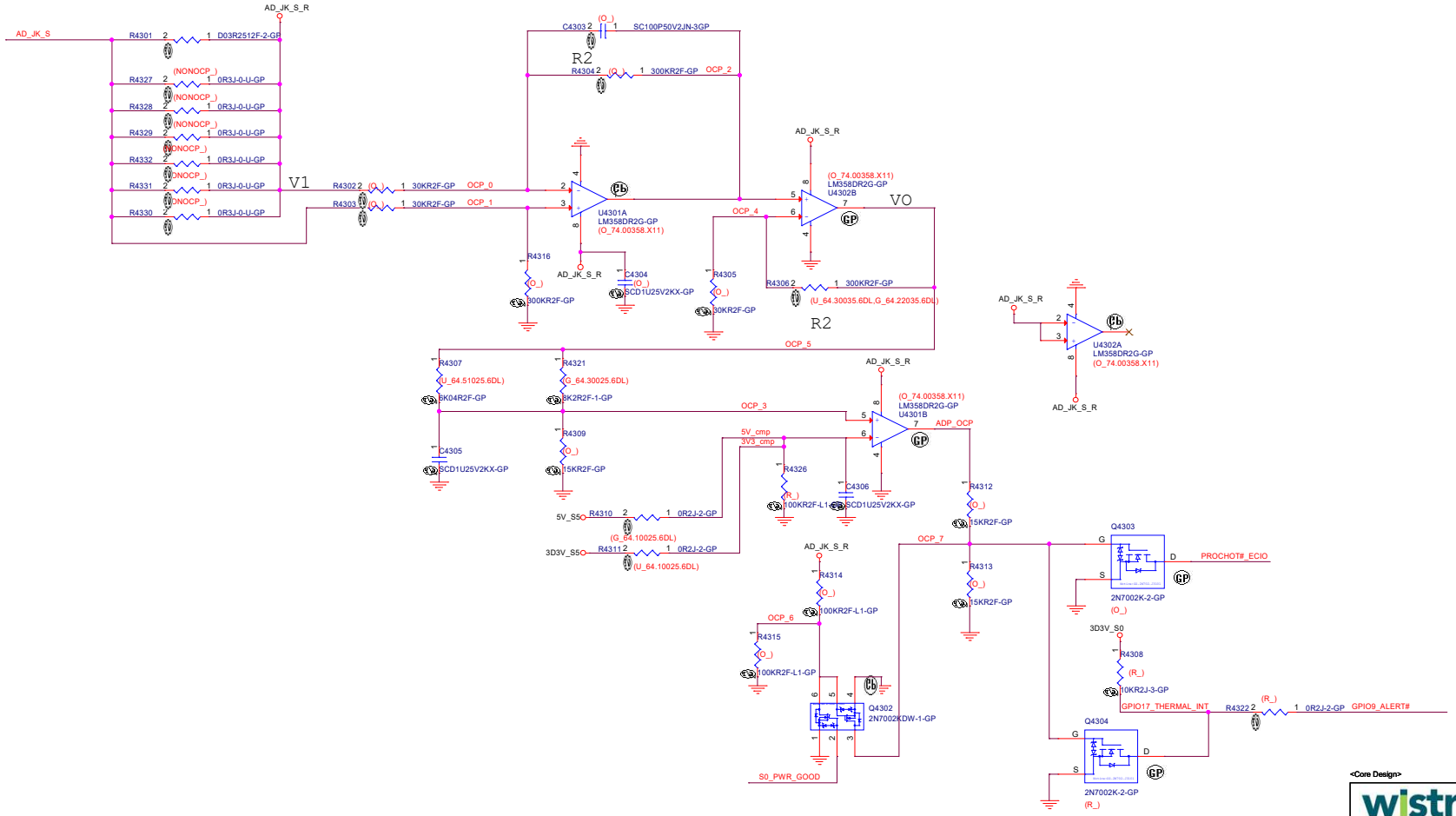
DCBATOUT switch



6,24 PROCHOT#_ECIO

79 GPIO9_ALERT#

24,40 S0_PWR_GOOD



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DCIN JACK(BATT Conn)

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 43 of 107

RSVD

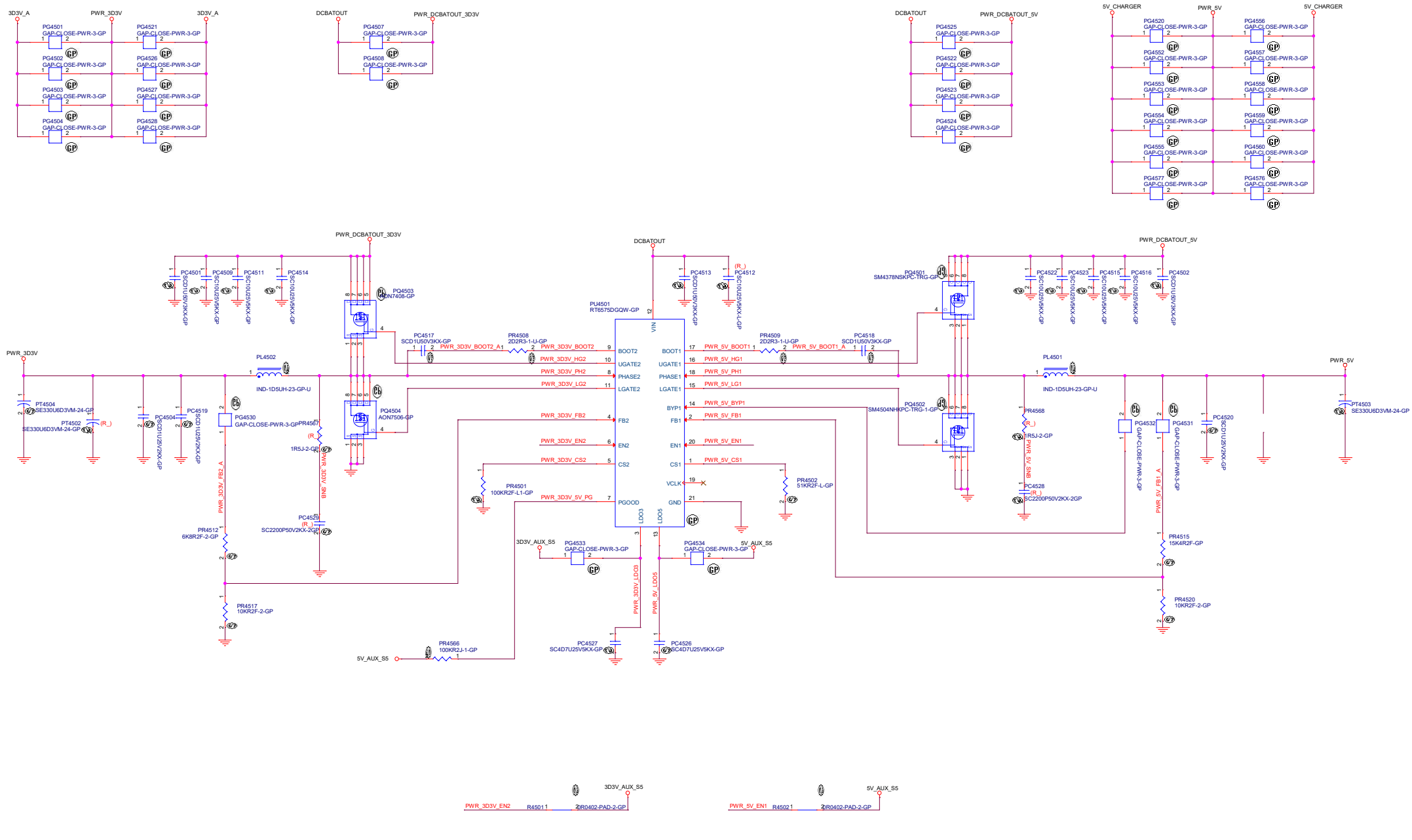
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
OZ554A LED Converter

Size: Custom
Document Number: Consumer AIO Petra238I
Rev: 1A

Date: Wednesday, July 25, 2018 Sheet 44 of 107



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: 5V/3D3V(RT6575D)

Size: A2 | Document Number: Consumer AIO Petra238I | Rev: 1A

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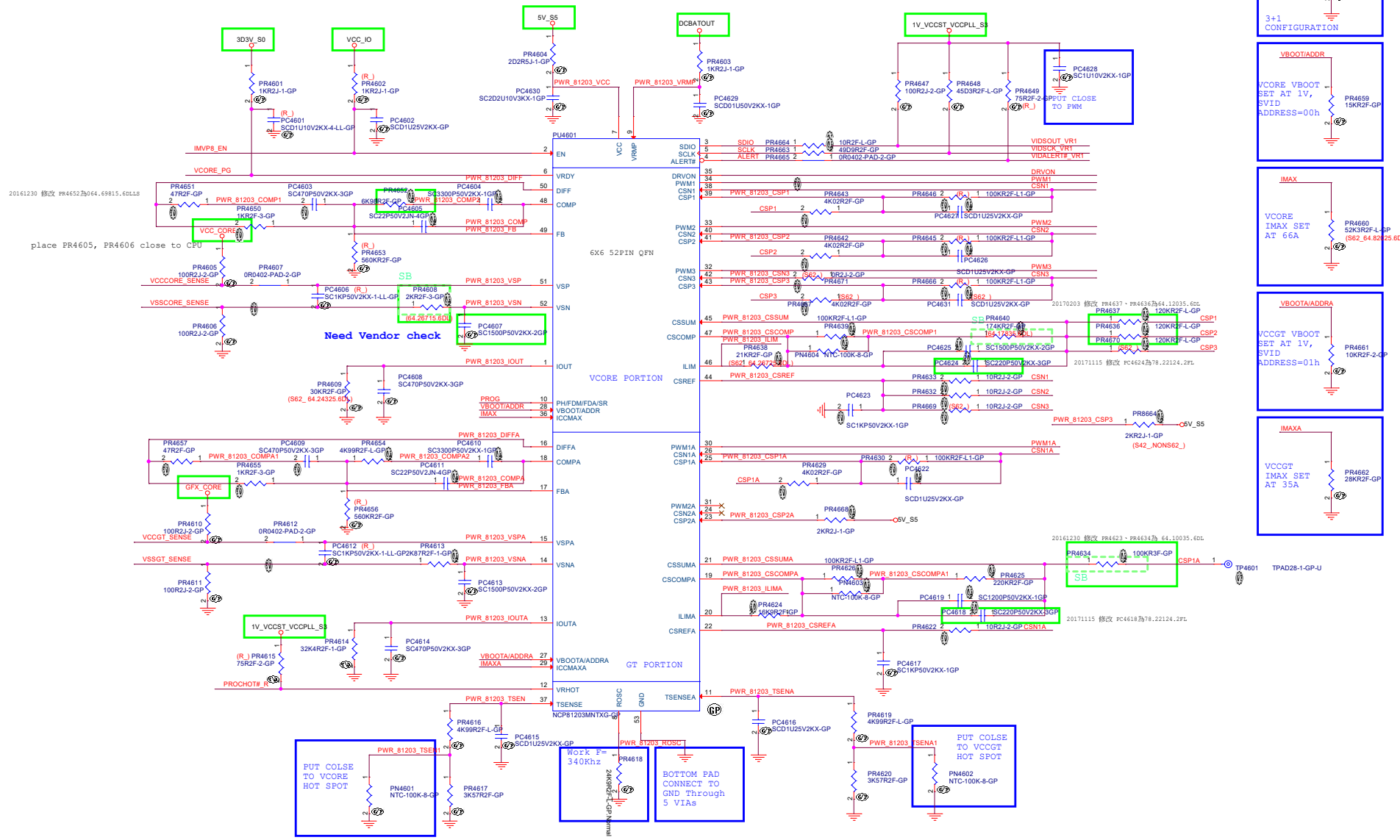
PWR_CORE/PWR_VCCGT

Intel Coffee Lake-S IMVP8 POWER 35W



20150312
Change U3601 PN 074.81203.0C73

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCORE & V_GT IC (NCP81203)

Size: Custom | Document Number: Consumer AIO Aurora | Rev: SA

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PWR_CORE

084.36358.0037 AONS36358
Vgs @ 4.5V,
Id = 24A,
Rds(on) = 8.2mohm,

084.36356.0037 AONS36356
Vgs @ 4.5V,
Id = 26A,
Rds(on) = 4mohm,

S62-35W
TDC 74A
IMAX 104A,
OCP>120A

S42-35W
TDC 45A
IMAX 66A,
OCP>80A

47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9

0.36uH,
DCR=1.05mohm,
Idc=30A, Isat=60A
10*11.5*4

470uF/2V,
Ripple Current=3.5Arms
ESR= 6 mohm
7.3*4.3*1.9

FOR EMI

BOTTOM PAD
CONNECT TO
GND Through
4 VIAs

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCORE OUTPUT (NCP81151)

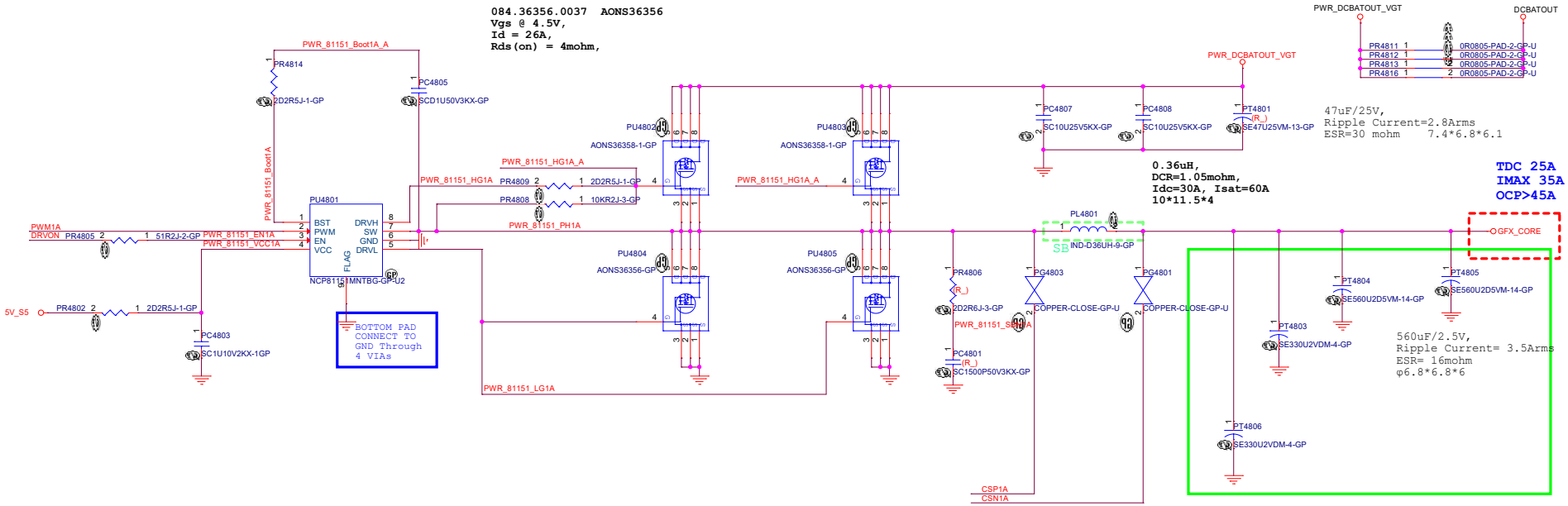
Size: Custom | Document Number: Consumer AIO Aurora | Rev: SA

Date: Wednesday, July 25, 2018 | Sheet 47 of 107

PWR_VCCGT

084.36358.0037 AONS36358
Vgs @ 4.5V,
Id = 24A,
Rds(on) = 8.2mohm,

084.36356.0037 AONS36356
Vgs @ 4.5V,
Id = 26A,
Rds(on) = 4mohm,



<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: V_GT OUTPUT(NCP81151)		
Size: Custom	Document Number: Consumer AIO Aurora	Rev: SA
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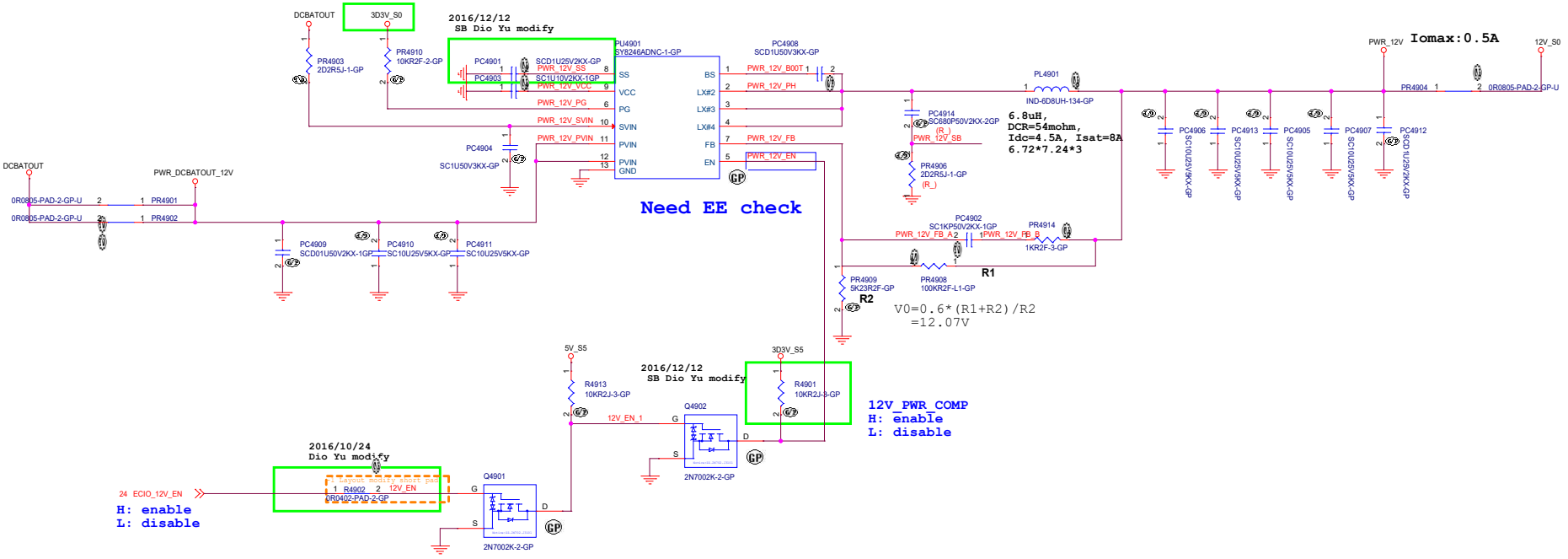
PWR_12V



<Core Design>

Wistron Incorporated	21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	DC to DC_12V (SY8246)
Size: C	Document Number: Consumer AIO Petra238i
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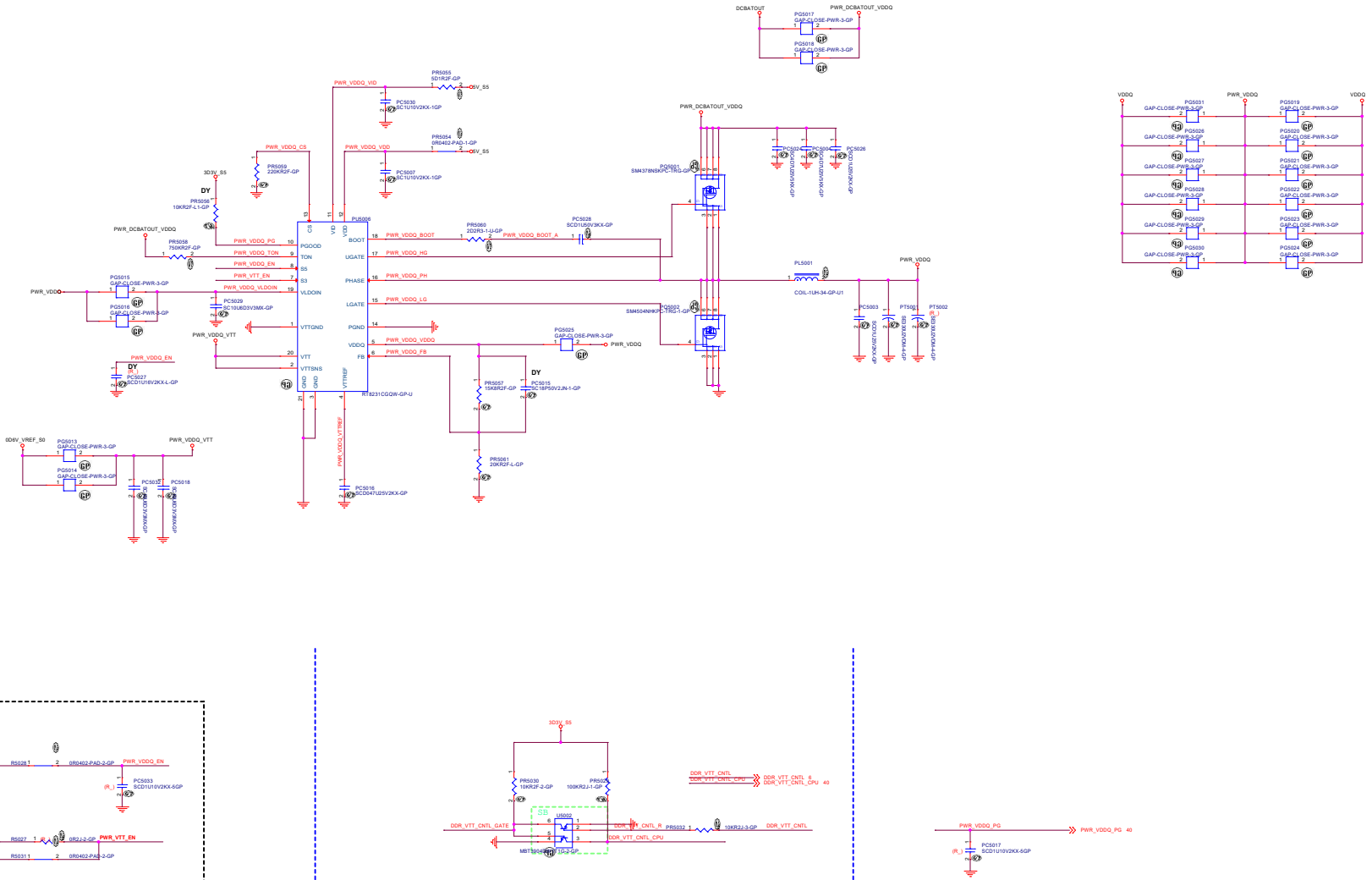
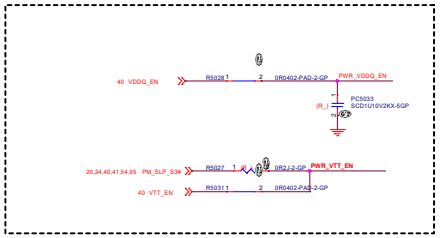
Date: Wednesday, July 25, 2018	Sheet 49 of 107

PWR_VDDQ





<Core Design>

Wistron	Wistron Incorporated 21F, 88, Sec. 1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	MEM/MEMVTT (RT8207P)
Size: D	Document Number: Consumer AIO Petra238I
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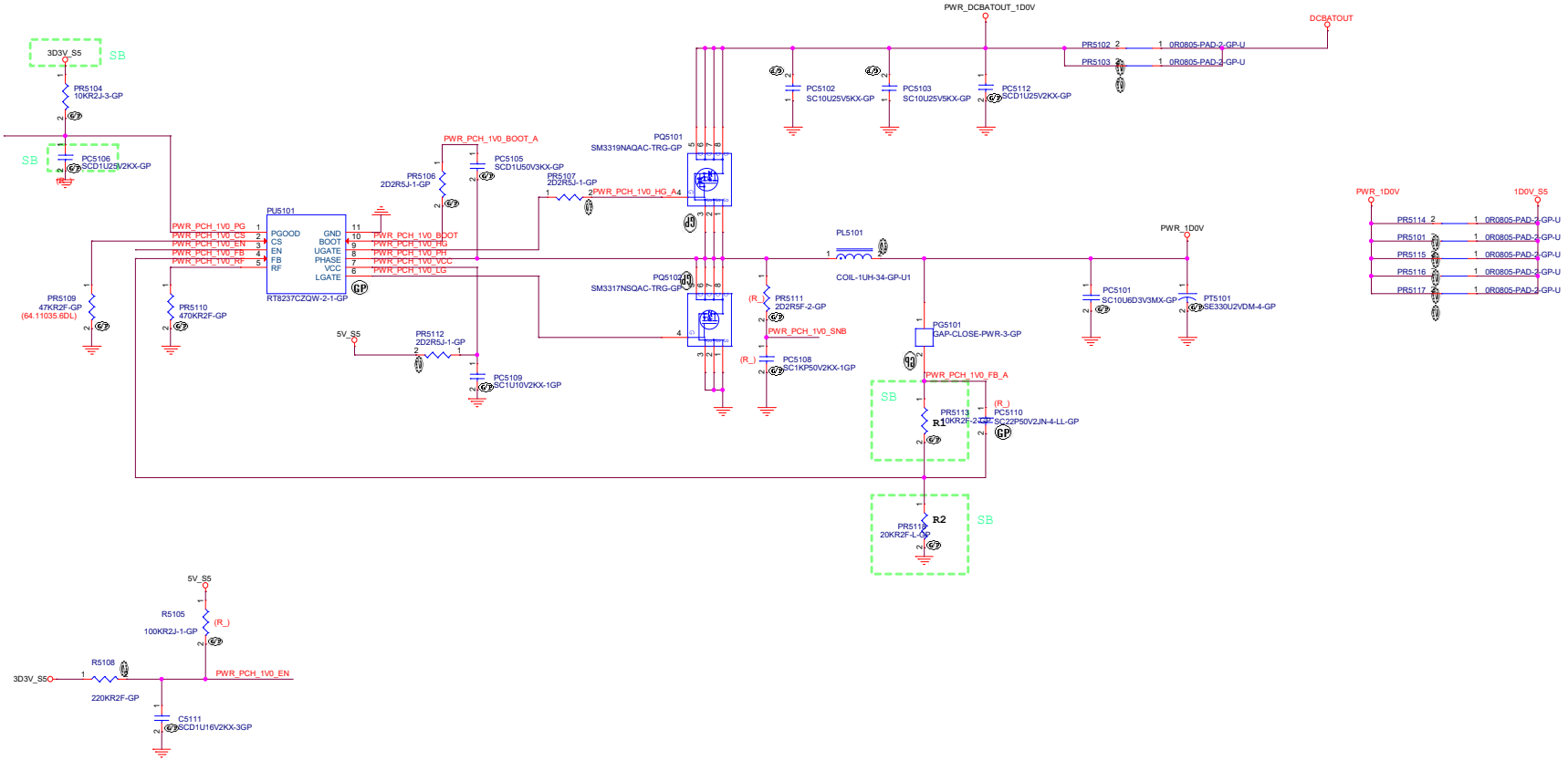
PWR_1D0V



<Core Design>

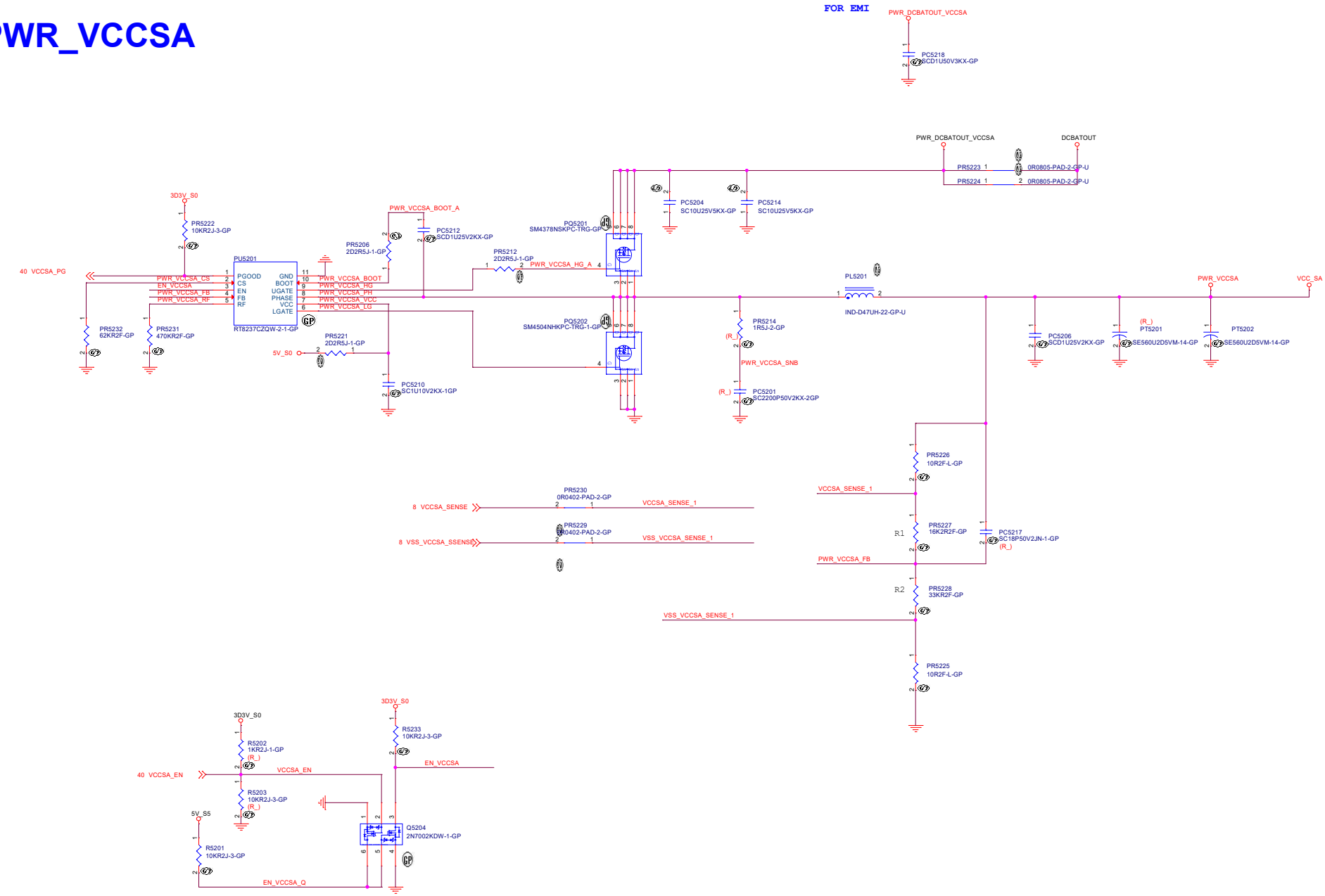
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH_1P0V(RT8237C)

Size: Custom | Document Number: Consumer AIO Petra238I | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 51 of 107

PWR_VCCSA



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCC_SA(RT8237C)

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

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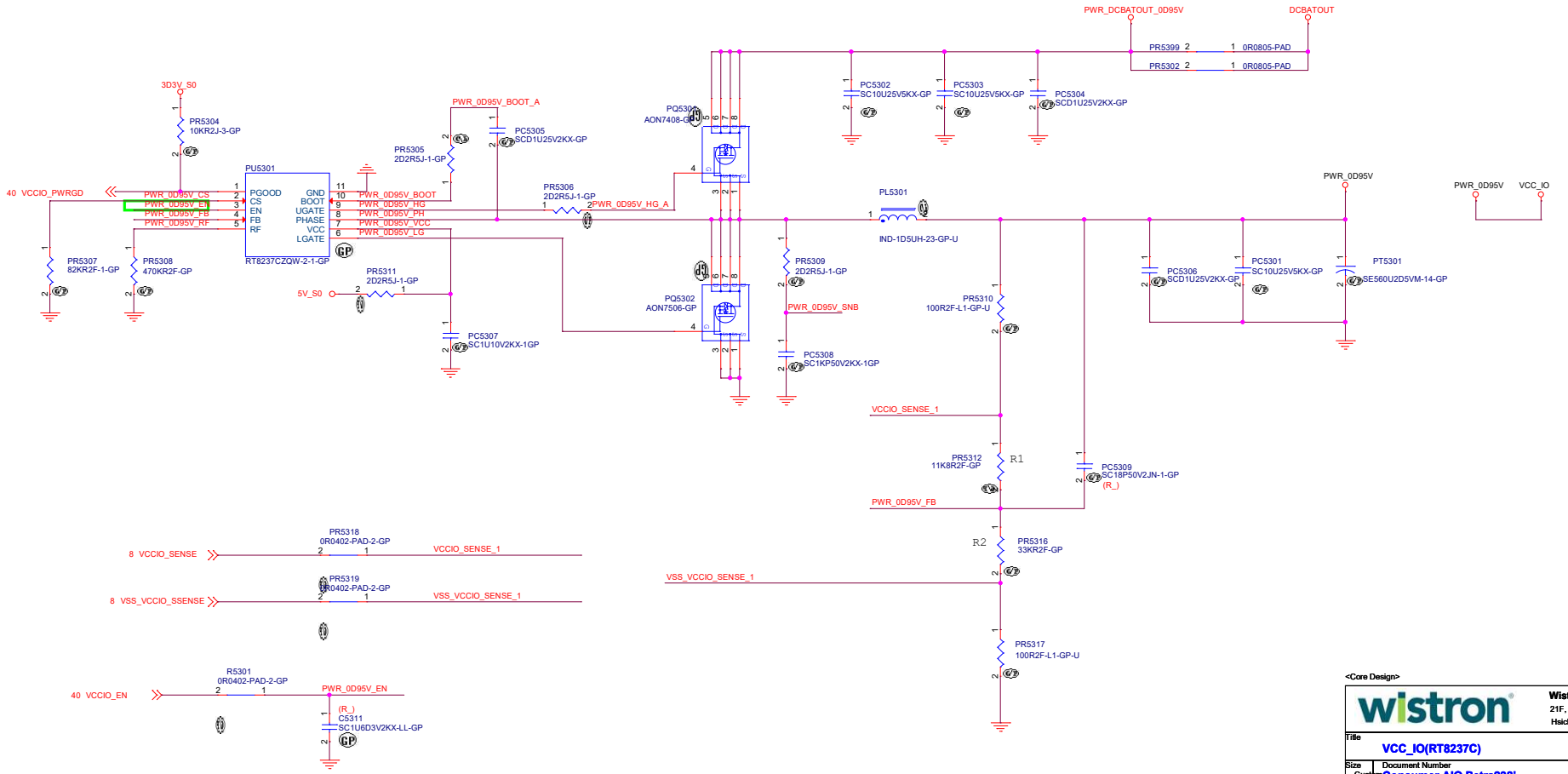
PWR_VCCIO



<Core Design>

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCC_IO(RT8237C)

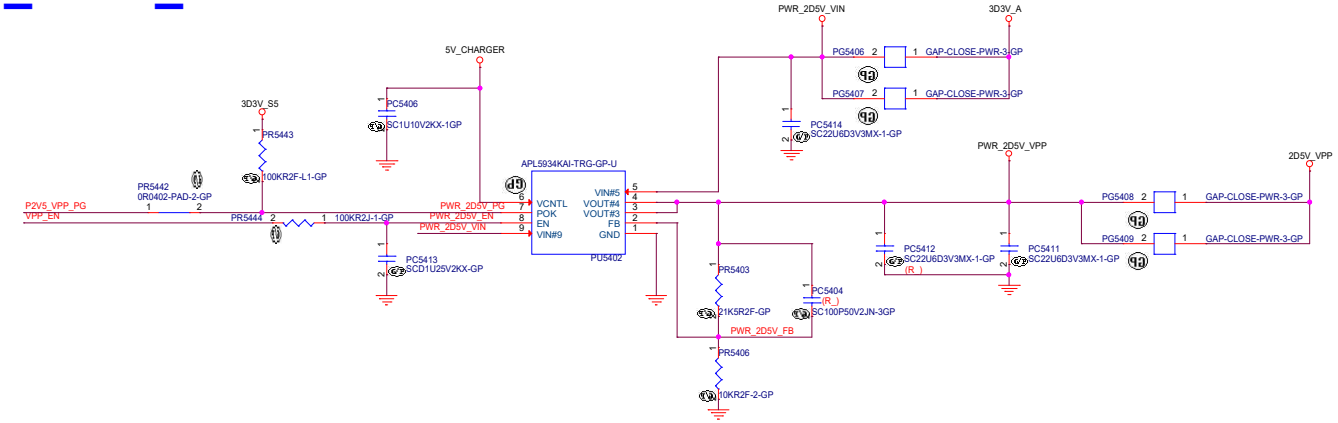
Size: Custom | Document Number: Consumer AIO Petra238I | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 53 of 107

PWR_2D5V_VPP

40 P2V5_VPP_PG

40 VPP_EN

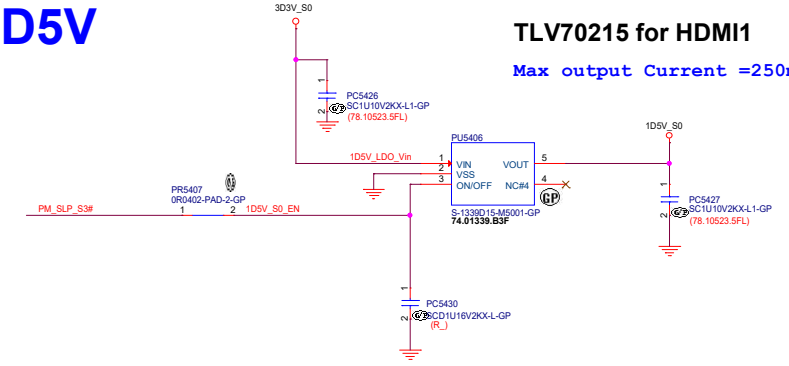


LDO: PWR_1D5V

20,24,40,41,50,95 PM_SLP_S3#

TLV70215 for HDMI1

Max output Current =250mA



<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DCDC_2D5V (APL5930)

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

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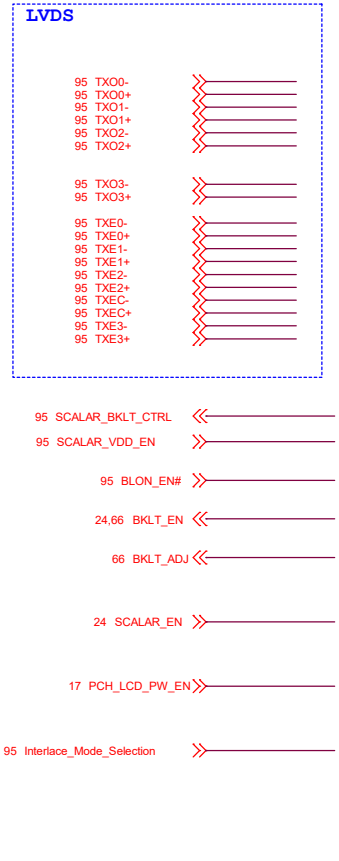
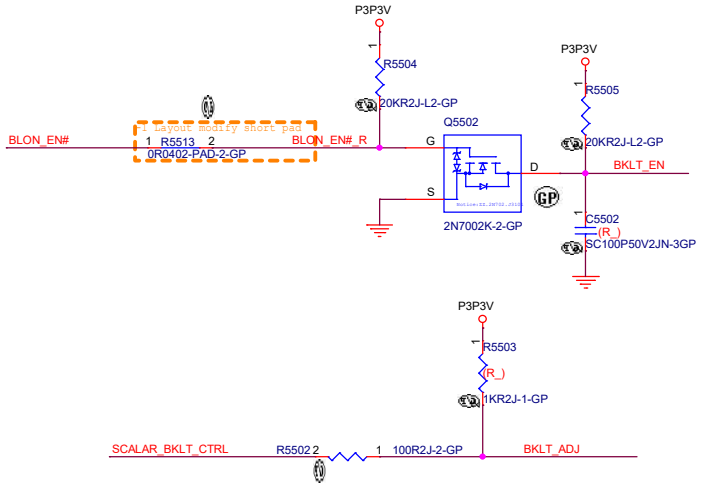
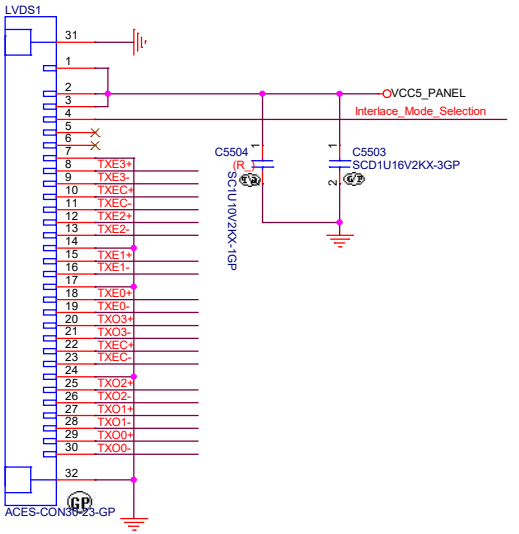
SSID = VIDEO

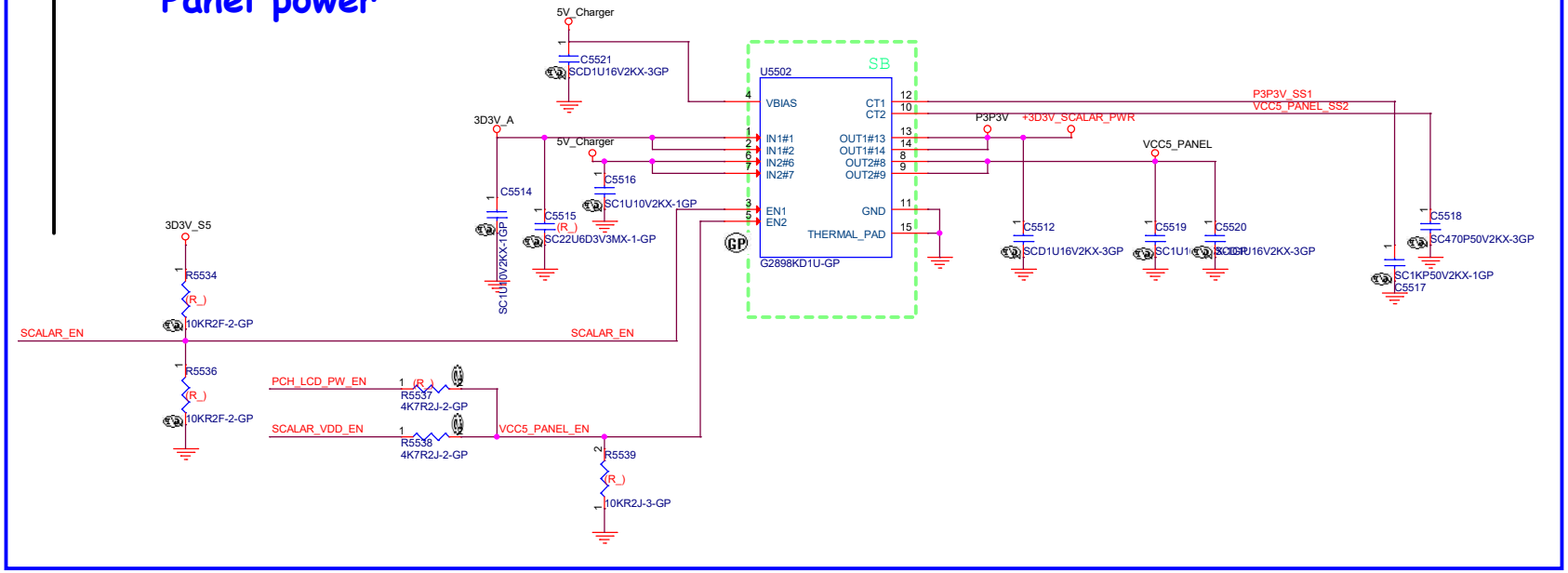




LVDS connector



Panel power



<Core Design>

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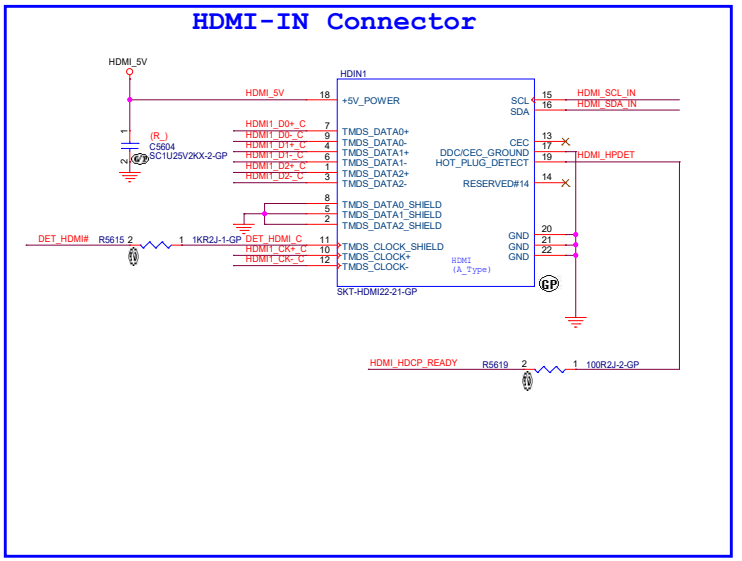
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LVDS Connector

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

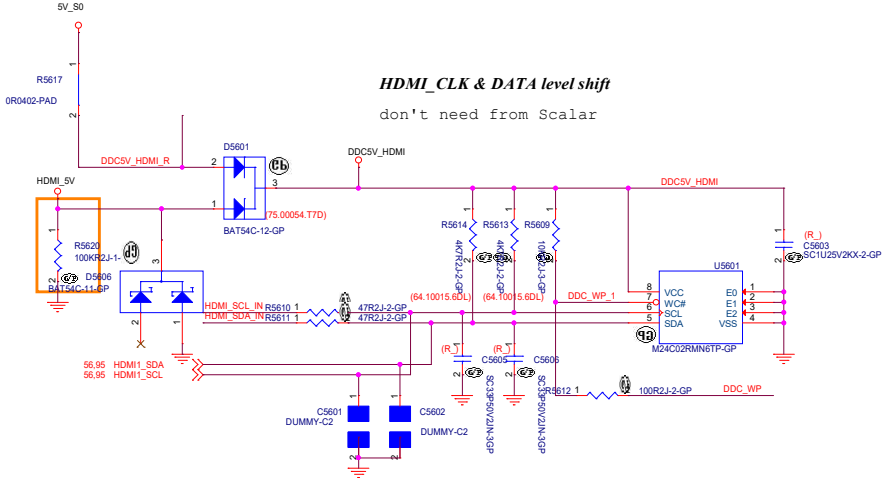
Date: Wednesday, July 25, 2018 | Sheet 55 of 107

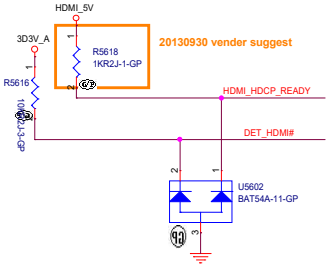
HDMI-IN Connector

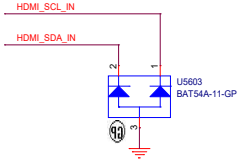


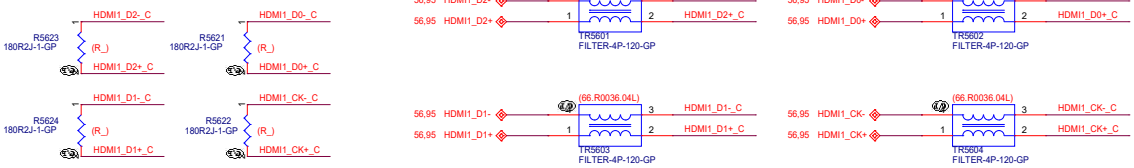
HDMI_CLK & DATA level shift

don't need from Scalar









<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI IN
Size: C
Document Number: Consumer AIO Petra238i
Rev: 1A
Date: Wednesday, July 25, 2018
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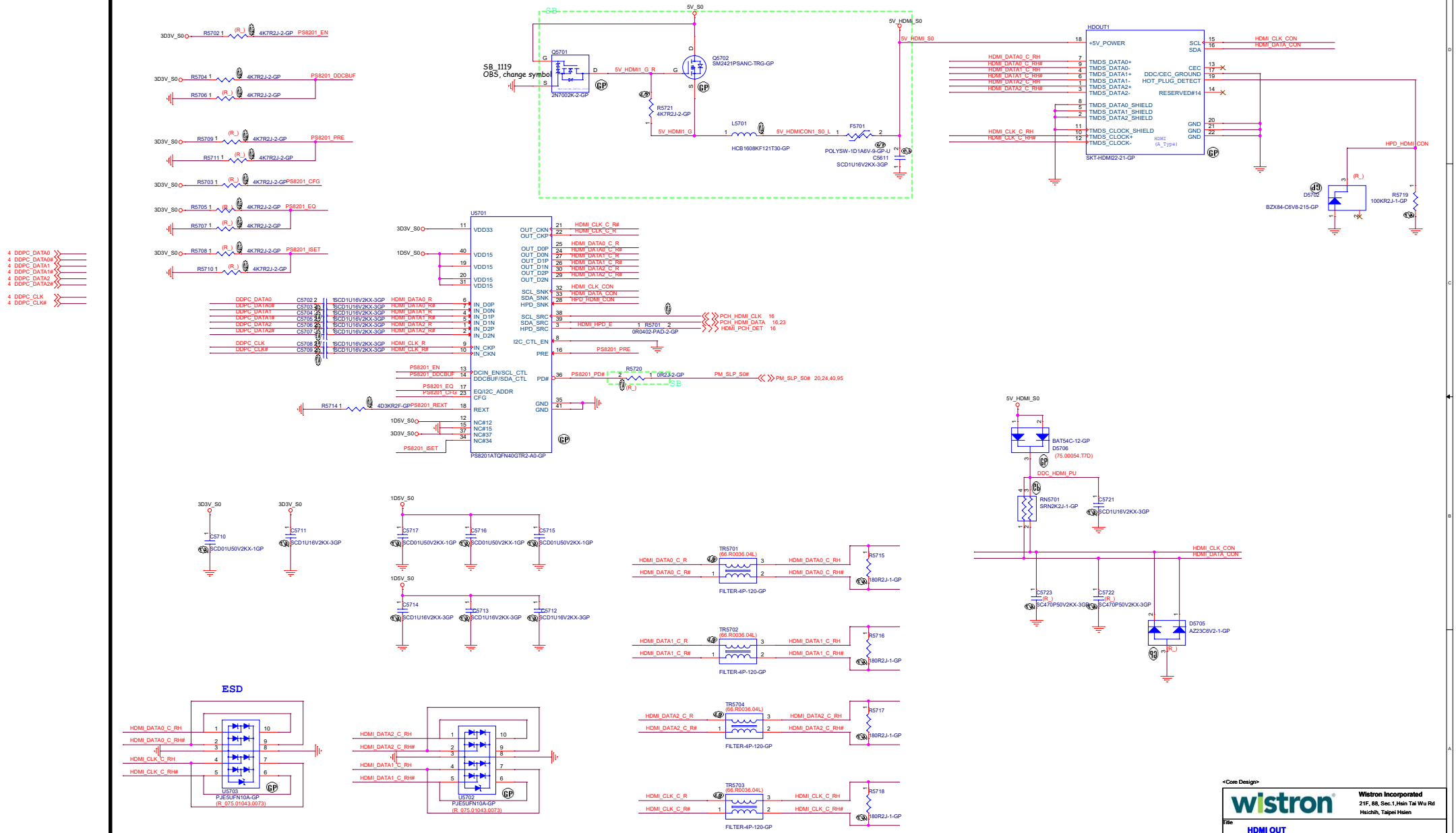
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



<Core Design>

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDMI OUT

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 57 of 107

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DVI/CRT_(R)

Size: A

Document Number: Consumer AIO Petra238i

Rev: 1A

Date: Wednesday, July 25, 2018

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Display switch_(R)

Size: A

Document Number: Consumer AIO Petra238i

Rev: 1A

Date: Wednesday, July 25, 2018

Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: HDD/ODD

Size: Custom | Document Number: Consumer AIO Aurora | Rev: SA

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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
Mini PCIE Card TV Tuner

Size: A
Document Number: Consumer AIO Petra238i
Rev: 1A

Date: Wednesday, July 25, 2018

M.2 2230 / 1630 Key E Type

SMBUS
- 20 SMB_DATA_RESUME
- 20 SMB_CLK_RESUME

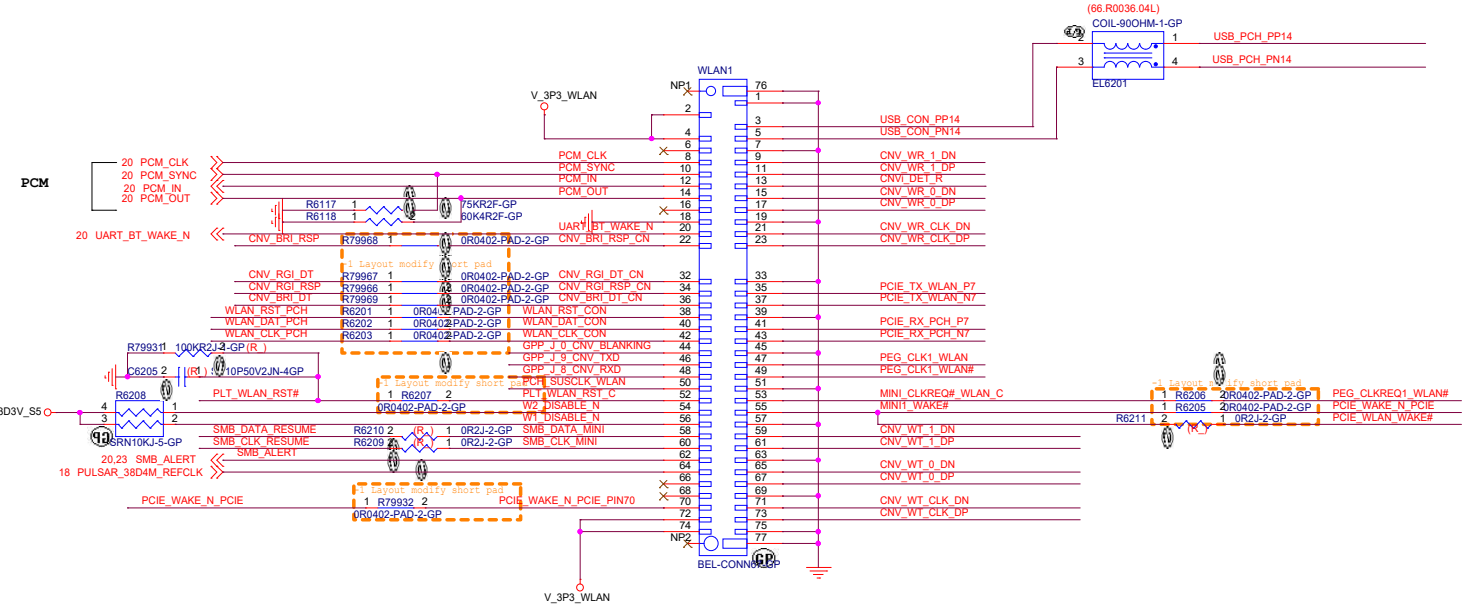
USB for BT
- 16 USB_PCH_PP14
- 16 USB_PCH_PN14

PCIE X1 & CLK
- 16 PCIE_RX_PCH_N7
- 16 PCIE_RX_PCH_P7
- 16 PCIE_TX_WLAN_N7
- 16 PCIE_TX_WLAN_P7
- 18 PEG_CLK1_WLAN
- 18 PEG_CLK1_WLAN#
- 20 PCH_SUSCLK_WLAN

Control signal
- 15 W1_DISABLE_N
- 15 W2_DISABLE_N
- 20 SLP_WLAN_N
- 24,62 LAN_EN_PWR_SIO
- 24 PCIE_WLAN_WAKE#
- 24,62 LAN_EN_PWR_SIO
- 17 NGFF_WIFI_PWR_CRL

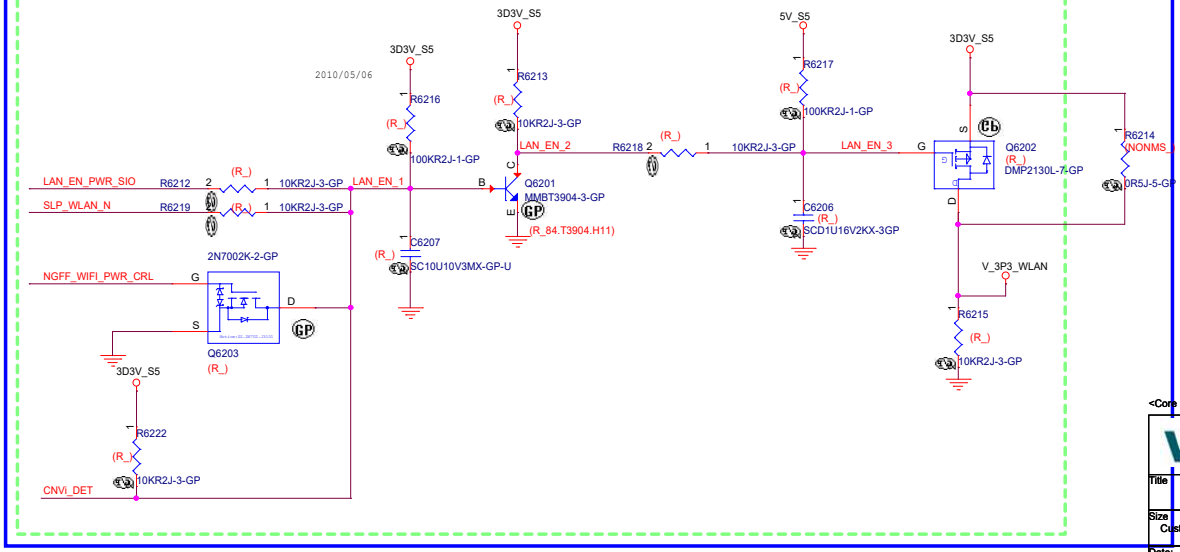
OTHERS
- 20 PCIE_WAKE_N_PCIE
- 24 PLT_WLAN_RST#
- 18 PEG_CLKREQ1_WLAN#

CNVi
- 17 CNV_WT_1_DN
- 17 CNV_WT_1_DP
- 17 CNV_WT_0_DN
- 17 CNV_WT_0_DP
- 17 CNV_WT_CLK_DN
- 17 CNV_WT_CLK_DP
- 17,23 CNV_BRI_RSP
- 17,23 CNV_RGI_DT
- 17,23 CNV_RGI_RSP
- 17,23 CNV_BRI_DT
- 17 GPP_J_0_CNV_BLANKING
- 17,23 GPP_J_9_CNV_TXD
- 17 GPP_J_8_CNV_RXD
- 17 WLAN_RST_PCH
- 17 WLAN_DAT_PCH
- 17 WLAN_CLK_PCH
- 17 CNV_WR_1_DN
- 17 CNV_WR_1_DP
- 17 CNV_WR_0_DN
- 17 CNV_WR_0_DP
- 17 CNV_WR_CLK_DN
- 17 CNV_WR_CLK_DP
- 17 CNVi_DET



WLAN Power

SB



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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title	WLAN and BT--NGFF	
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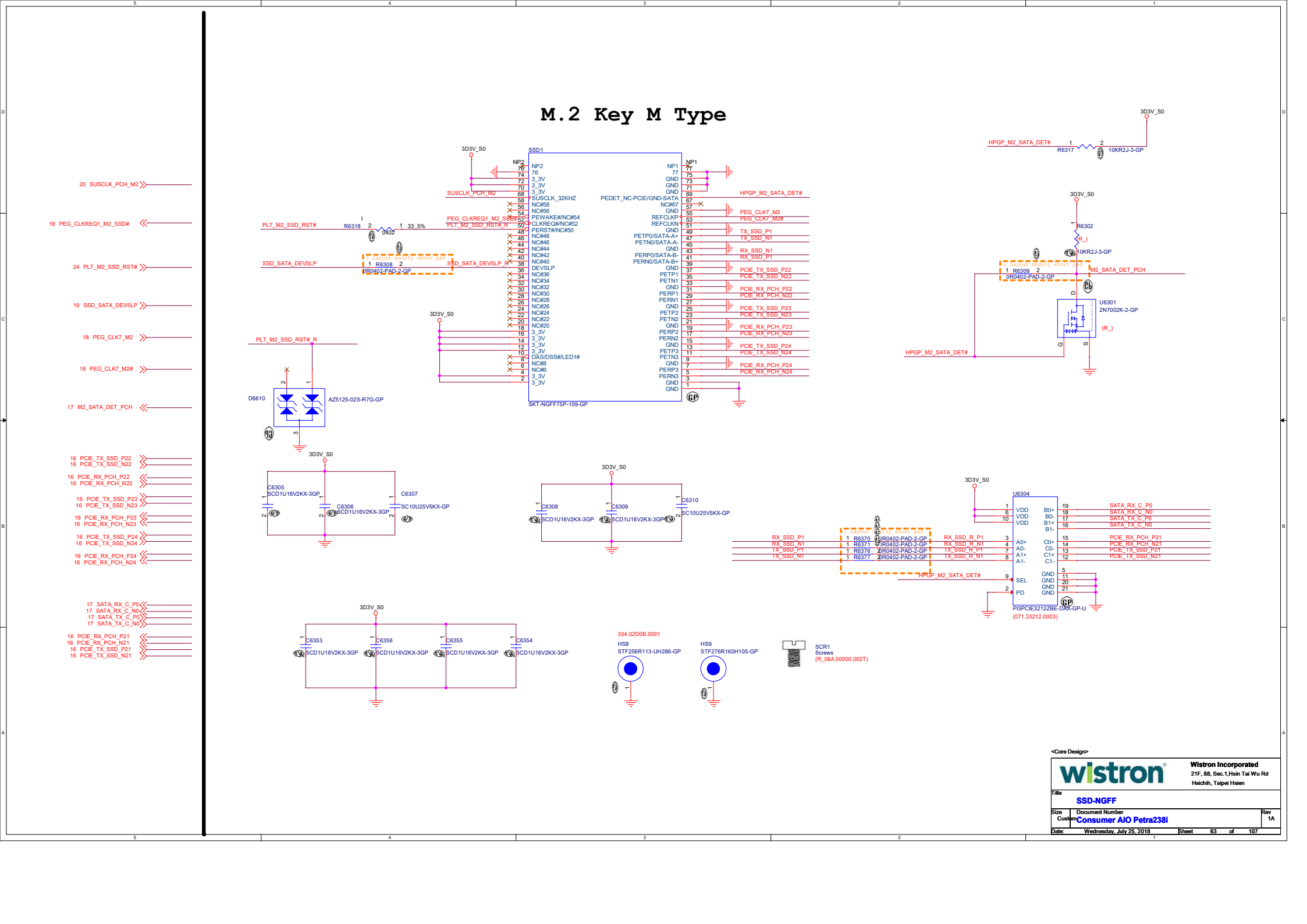
M.2 Key M Type



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wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: SSD-NGFF		
Size: Custom	Document Number: Consumer AIO Petra238I	Rev: 1A
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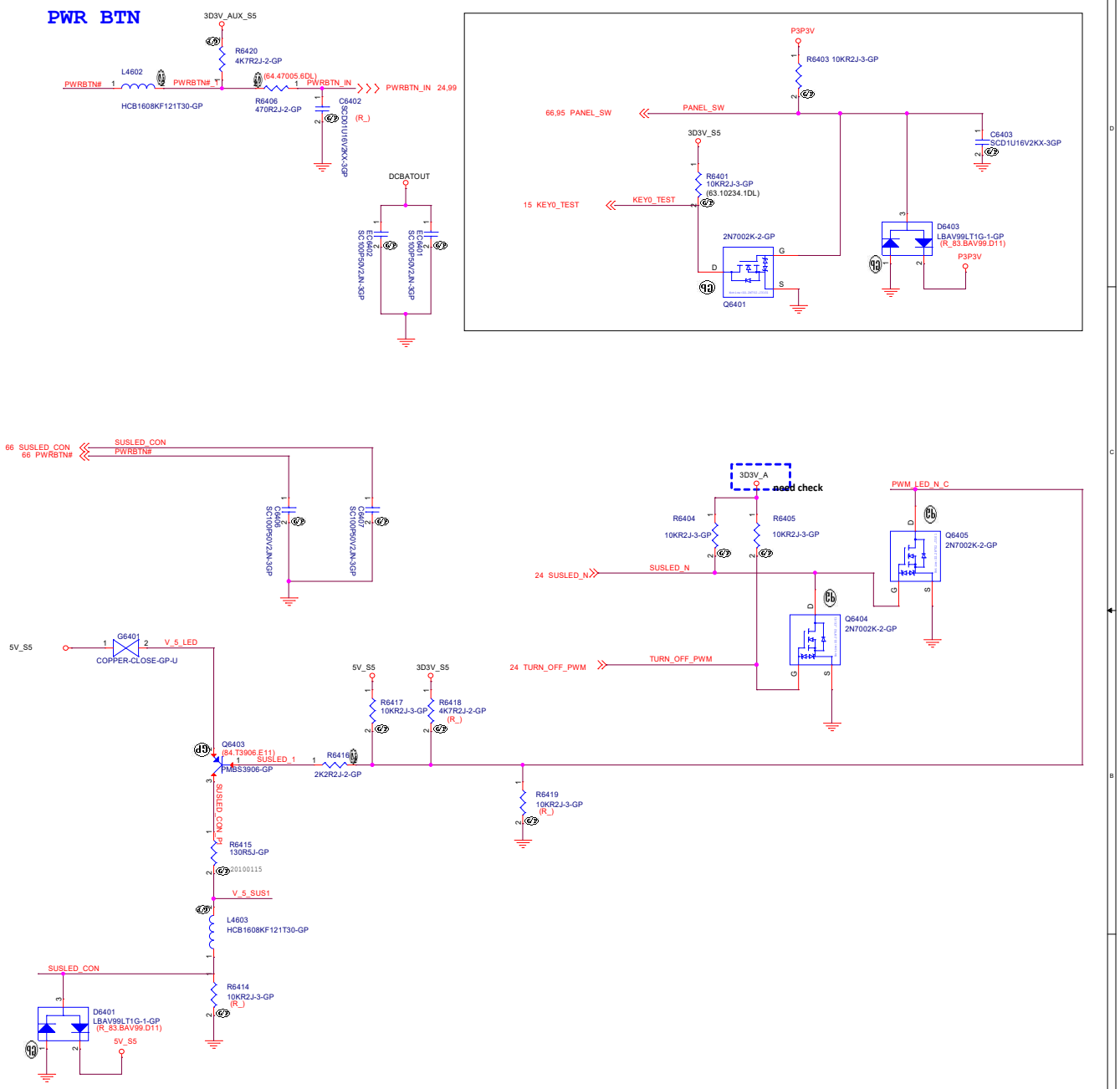

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PWR BT/Side Key/LED

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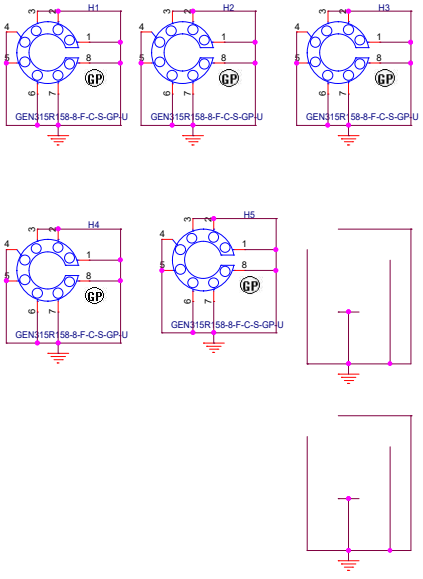
Stand off&Hole



CPU

HS1 STF296R205H152-GP (334.00L08.0001)

CPU

HS2 STF296R205H152-GP (334.00L08.0001)

CPU

HS3 STF296R205H152-GP (334.00L08.0001)

CPU

HS4 STF296R205H152-GP (334.00L08.0001)

VGA

HS6 STF296R205H152-GP (334.00L08.0001)

HS5 STF296R205H152-GP (334.00L08.0001)

2016/11/28
Pio Yu modify

G6404 GNDPAD GNDPADS237X867-NP

G6405 GNDPAD GNDPADS552X473-S-NP

G6407 GNDPAD GNDPADS693X591-S-NP

G6406 GNDPAD GNDPADS493X473-S-NP

EMI CAP

EMI/ESD near CPU

6,99 H_TRST_N — H_TRST_N — C6501 (R_) SC1U25V2KX-2-GP

6,17,99 PLTRST_CPU_N — PLTRST_CPU_N — ED6404 AZ5725-01FDR7G-GP

ED6409 AZ5725-01FDR7G-GP

6 CPU_VCCST_PWRGD_R — CPU_VCCST_PWRGD_R — ED6405 AZ5725-01FDR7G-GP (R_)

EMI/ESD near PCH

15,24,68,76 PLTRST#_PCH — PLTRST#_PCH — ED6410 AZ5725-01FDR7G-GP

6,20,99 H_PWRGD — H_PWRGD — C6505 (R_) SC1U25V2KX-2-GP

20 SM_DRAMRST# — SM_DRAMRST# — ED6407 AZ5725-01FDR7G-GP

20,40,99 PCH_SYSPWROK — PCH_SYSPWROK — C6508 (R_) SC1U25V2KX-2-GP

20 HDA_RST#_PCH — HDA_RST#_PCH — C6509 (R_) SC1U25V2KX-2-GP

20 PCH_RTCRST_PULLUP — PCH_RTCRST_PULLUP — C6510 (R_) SC1U25V2KX-2-GP

20 PCH_SRTCRSTB_PULLUP — PCH_SRTCRSTB_PULLUP — C6511 (R_) SC1U25V2KX-2-GP

20,40 PCH_PWROK — PCH_PWROK — C6512 (R_) SC1U25V2KX-2-GP

20,24,99 RSMRST#_SIO — RSMRST#_SIO — C6513 (R_) SC1U25V2KX-2-GP

12,13,20 DDR4_DRAMRST_N — DDR4_DRAMRST_N — ED6408 AZ5725-01FDR7G-GP (R_)

VDDQ

C6517 (R_) SC1U25V2KX-2-GP
C6518 (R_) SC1U25V2KX-2-GP
C6519 (R_) SC1U25V2KX-2-GP
C6520 (R_) SC1U25V2KX-2-GP
C6521 (R_) SC1U25V2KX-2-GP
C6522 (R_) SC1U25V2KX-2-GP

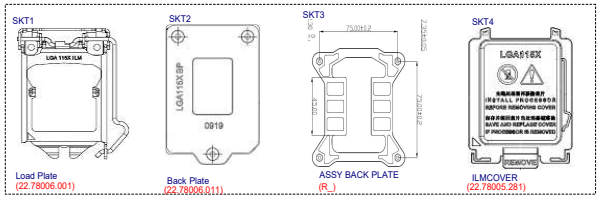
DCBATOUT

EC6523 EC6524 EC6525 EC6526 EC6527 EC6528 EC6529 EC6530 EC6531 EC6532 EC6533 EC6534 EC6535 EC6536 EC6537 EC6538 EC6539 EC6540 EC6516 EC6541
(R_) SCD1U25V2KX-GP

DUMMY BOM

Material part

SKYLAKE SOCKET



GSKT1 GASKET (R_334.03508.0001)

GASKET FOR WIESON HDMI

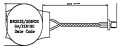
GSKT2 GASKET (R_334.0350F.0001)

GASKET FOR TCONN HDMI

Battery Symbol

BAT3 BATTERY CR2032 (R_23.20068.001)

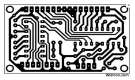
Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001



BAT2 BATTERY BR2032_60MM (R_23.24220.612)
Wire Length:60mm
耐高溫>85C
Vendor
P/N:
23.21208.061
23.24220.612

Del PCHHS1 by Thermal--Ryan 0225

PCB Symbol



PCB1 PCB (R_)

HeatSink Symbol

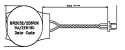
PCHHS1 HEATSINK (60.3MN01.032)

Vendor
P/N:
60.3MN01.011(second source)
60.3MN01.001

LABEL

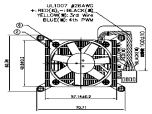
LBL1 LABEL (40.3BZ23.011)
LBL6 LABEL (R_45.3J904.011)
LBL5 LABEL (R_40.3BZ24.001)

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
345.02801.0001 -> 12 x 6mm



BAT1 BATTERY CR2032_30MM (023.22032.0311)
Wire Length:30mm
Vendor
P/N:
23.21221.024
23.21212.031

HeatSink+FAN Symbol



HSFAN1 (R_60.3KN01.001)

Vendor
P/N:

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Stand off&EMI Cap&DUMMY BOM

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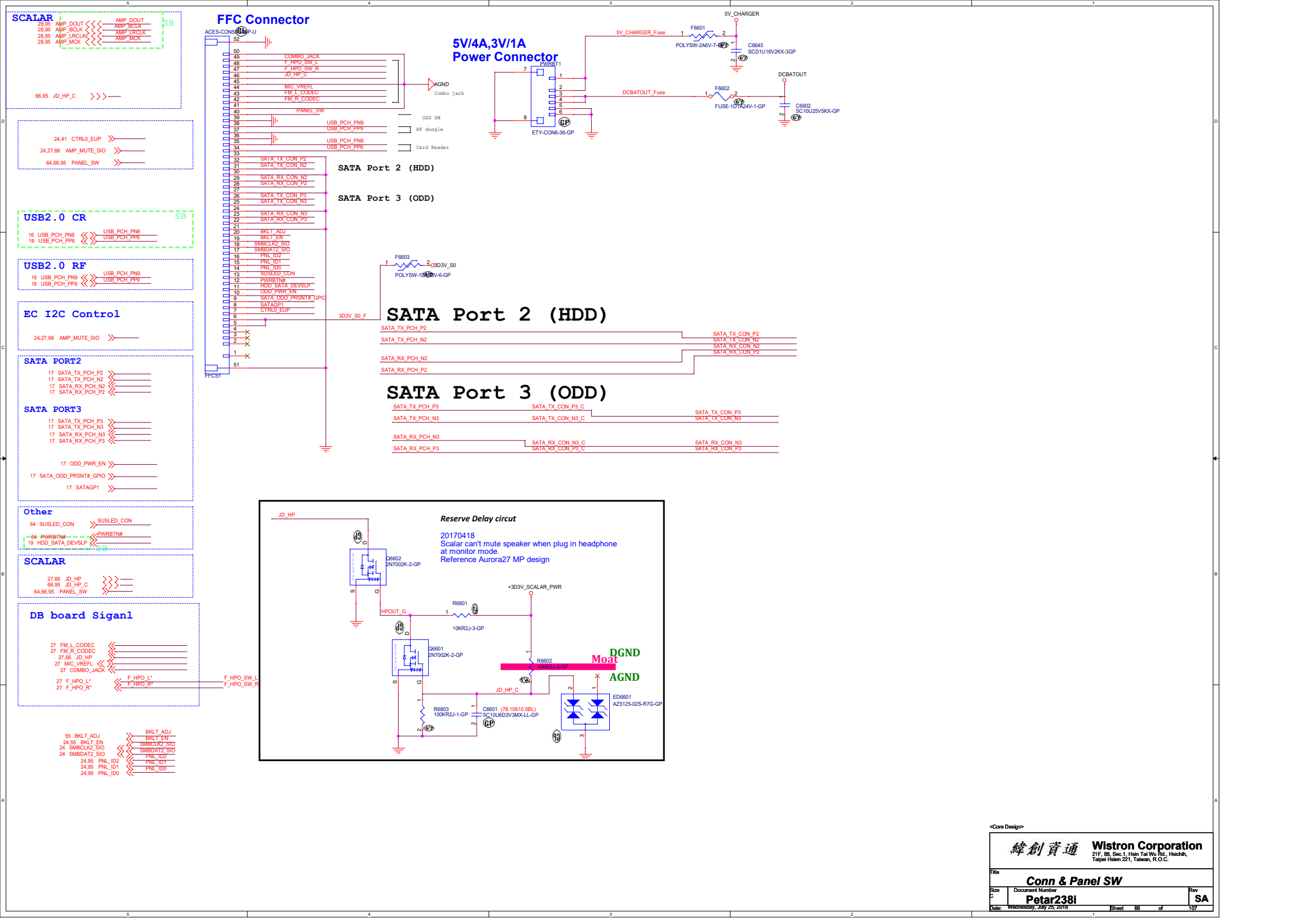

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Conn & Panel SW

Size: C | Document Number: Petar238i | Rev: SA

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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: COM_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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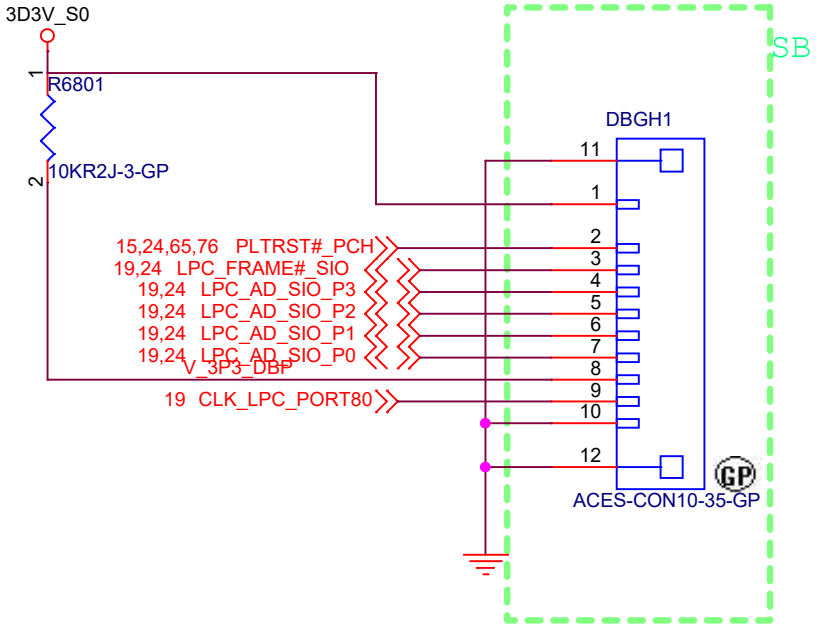

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: **Debug**		
Size: A	Document Number: **Consumer AIO Petra238i**	Rev: 1A
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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LPT_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: G sensor_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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Reserved

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

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79 GPU_PEX_RST_HOLD
16,24 SIO_DGPU_HOLD_RST#
15,24,65,68 PLTRST#_PCH
79 PEX_RST_GPU
79 SYS_PEX_RST_MON#

Control Siganl

16,24,86 DGPU_PWROK
18 PEG_CLKREQ0_CPU#

PCIE CLK

18 CLK_GFX_P
18 CLK_GFX_N

PCIE signal

3 PEG_RXP0
3 PEG_RXN0
3 PEG_C_TXP0
3 PEG_C_TXN0
3 PEG_RXP1
3 PEG_RXN1
3 PEG_C_TXP1
3 PEG_C_TXN1
3 PEG_RXP2
3 PEG_RXN2
3 PEG_C_TXP2
3 PEG_C_TXN2
3 PEG_RXP3
3 PEG_RXN3
3 PEG_C_TXP3
3 PEG_C_TXN3

3V3_1V8_AON
SIO_DGPU_HOLD_RST#
PLTRST#_PCH
U7_PIN5
U7 NL17SZ08DFT2G-GP
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD
BAT54A-11-GP
DGPU_PWROK
DGPU_PWROK_G
PJA138KA-GP
PEG_CLKREQ0_CPU#
084.00138.0A31
2nd = 84.N5067.031
PEX_RST_GPU
PEX_CLKREQ
CLK_GFX_P
CLK_GFX_N
100MHz

GC6 Sequence differences

N16 stuff
N17 no stuff
N17 stuff
N16 no stuff

1/14 PCI_EXPRESS
1 OF 14

PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#

NC FOR GM108
NC FOR GF117GK208GM108
GPU1A
N16S-GM-S-A2-GP
(G_ KG.SG10V.001)
071.0N16S.0A0U

NC FOR GF119
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_PLL_HVDD
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NVVDD_SENSE
NVGND_SENSE

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
AA14	PEX_PLLVDD	NC	Disconnect power supply
AA15	PEX_PLLVDD	NC	Disconnect power supply
AB8	PEX_SVDD_3V3	NC	Disconnect power supply.

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_PLLVDD_1
PEX_PLLVDD_2
PEX_PLLVDD_GPU
TESTMODE
GPU_TESTMODE
PEX_TERMP

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
Miscellaneous			
AD9	TESTMODE	NVJTAG_SEL	Leave pull-down resistor to GND

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
AA22	PEX_IOVDD	PEX_DVDD	Note power supply change
AB23	PEX_IOVDD	PEX_DVDD	Note power supply change
AC24	PEX_IOVDD	PEX_DVDD	Note power supply change
AD25	PEX_IOVDD	PEX_DVDD	Note power supply change
AE26	PEX_IOVDD	PEX_DVDD	Note power supply change
AE27	PEX_IOVDD	PEX_DVDD	Note power supply change
AA10	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA12	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA13	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA16	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA18	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA19	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA20	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AA21	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AB22	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AC23	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AD24	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AE25	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AF26	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AF27	PEX_IOVDDQ	PEX_HVDD	Note power supply change
AF22	PEX_TSTCLK	NC	Name change only
AE22	PEX_TSTCLK_N	NC	Name change only

+1P0V_VGA
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
1V_1V8_IOVDD
PEX_IOVDDQ
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14

Figure 8. PEX Decoupling and Filtering for Co-Design

Figure 18. PEX Voltage Supplies Co-Design

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF X6S	0402	1	3	Under GPU
	4.7 µF X6S	0603	1	1	Under GPU
	4.7 µF X6S	0603	1	2	Near GPU
	10 µF X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF X6S	0402	1	4	Under GPU
	4.7 µF X6S	0603	1	2	Near GPU
	10 µF X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Near GPU

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64	1.0 µF X7R	0402	1	N/A	Under GPU
	4.7 µF X5R	0603	1	N/A	Near GPU
	4.7 µF X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail					
GB2B-64	4.7 µF X5R	0603	2	N/A	Near GPU

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(1/5) PEG
Size: Custom
Document Number: Consumer AIO Petra238i
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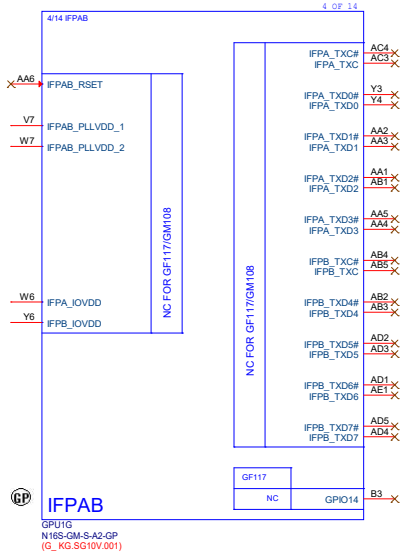
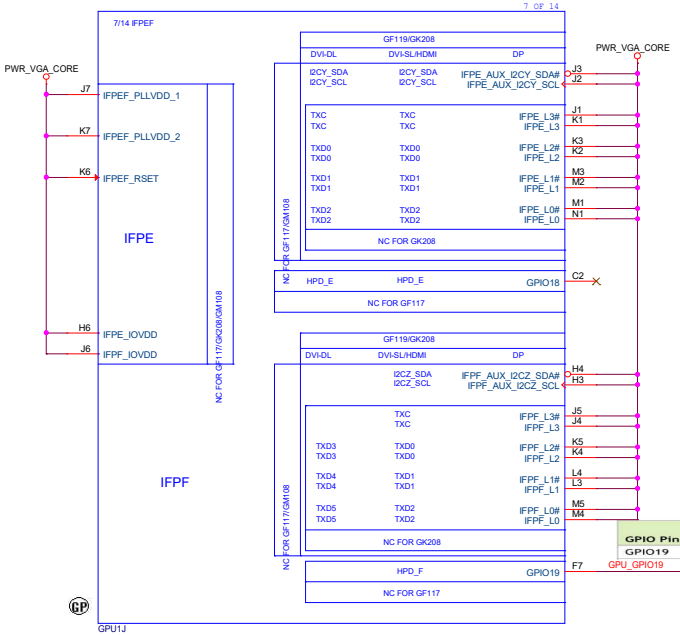
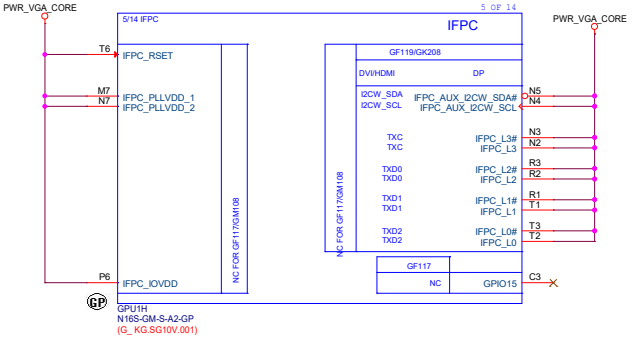
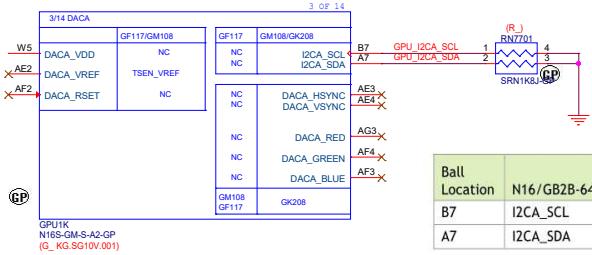




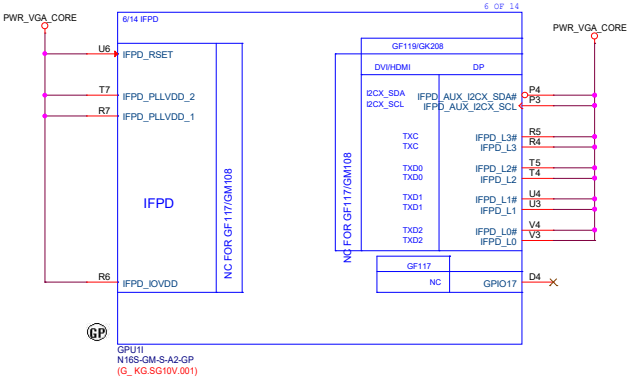
GPIO Pin	N16 GPU Function	N16 GPU Function on Co-Design	N17 GPU Function	Comments
GPIO19	HPD_IFPF or HPD_IFPB	3D VISION	3D VISION	



Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
AE2	NC	TS_VREF	Name change only



Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
B7	I2CA_SCL	GPIO23	Leave unconnected
A7	I2CA_SDA	GPIO22	Leave unconnected



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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU(2/5)DIGITALOUT

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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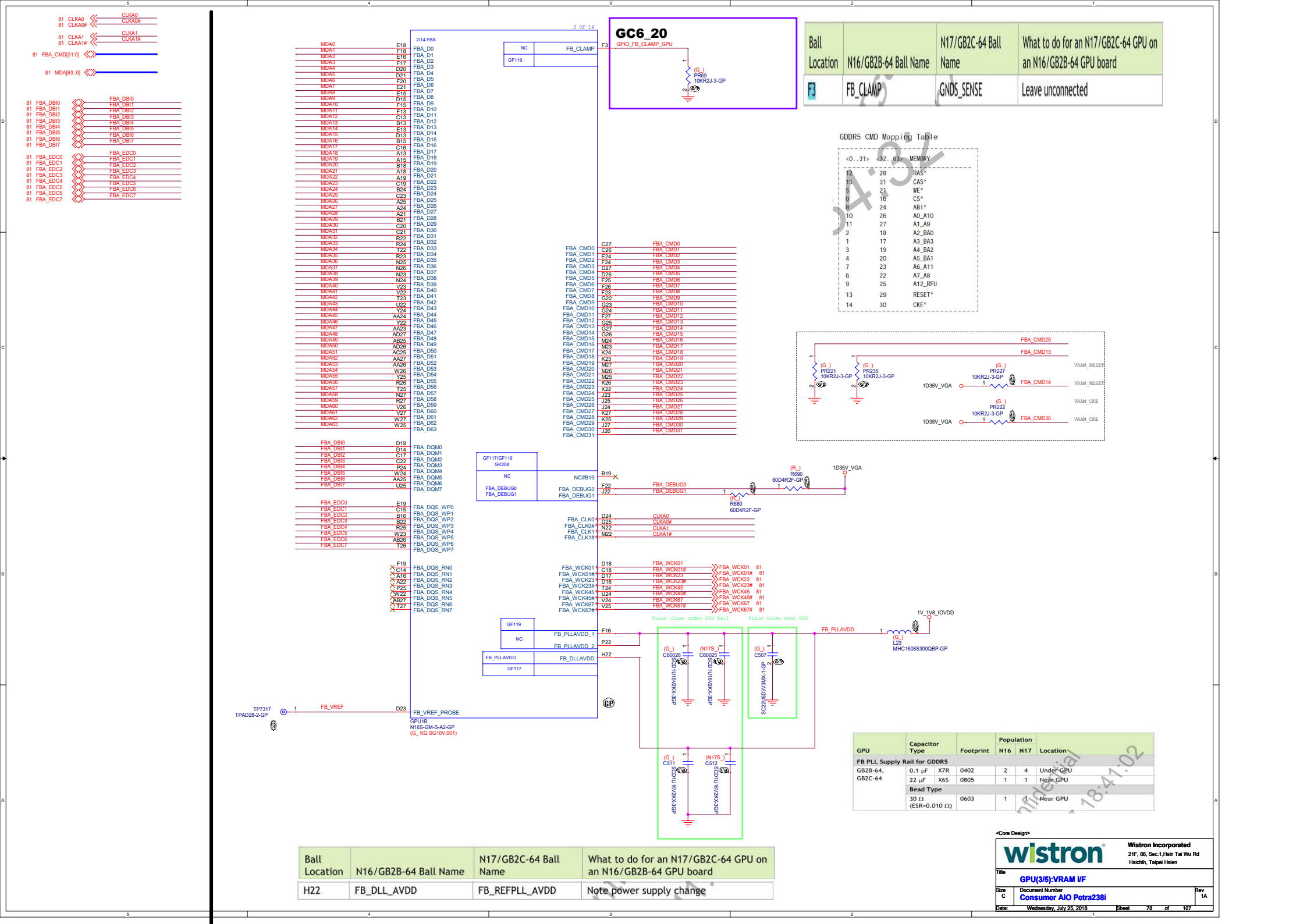

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
F3	FB_CLAMP	GNDS_SENSE	Leave unconnected

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
H22	FB_DLL_AVDD	FB_REFPLL_AVDD	Note power supply change

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21F, 88, Sec.1,Hsin Tai Wu Rd
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Title: GPU(3/5):VRAM I/F

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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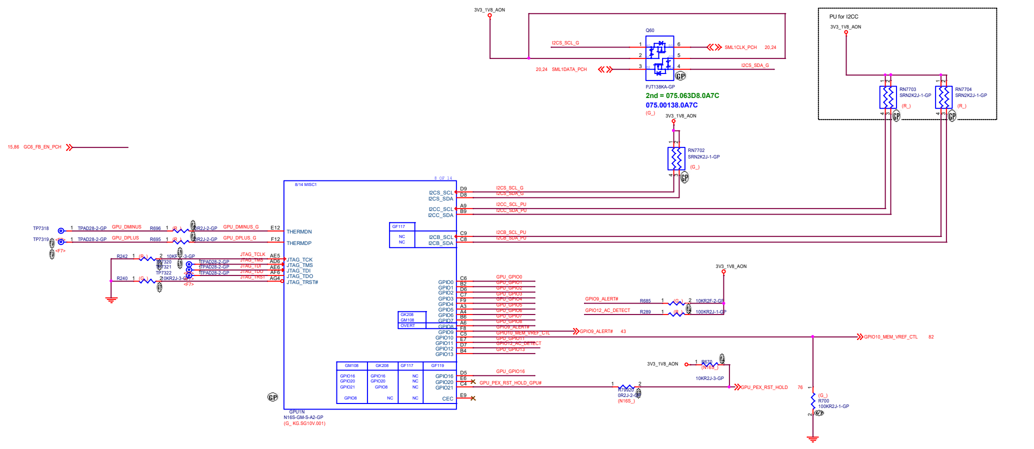
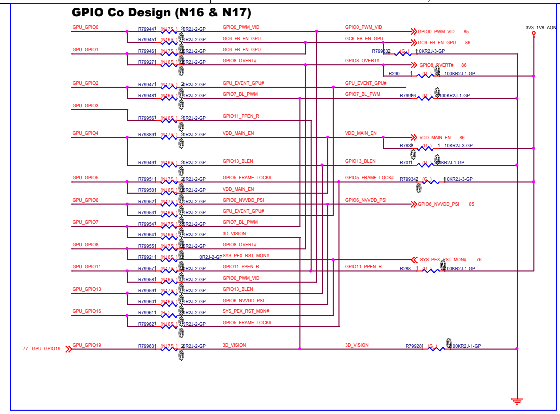
NOTE 4: DEVID_SEL default setting is 0

NOTE 5: PCIE_CFG default setting is 0(high power/high swing). for some NB projects. this should be 1(lower power/low swing)

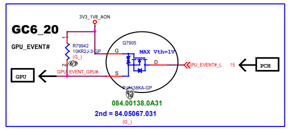


GPIO Co Design (N16 & N17)



GPIO Pin	N16 GPU Function	N16 GPU Function on Co-Design	N17 GPU Function	Comments
GPIO0	GC6_FB_EN	PWM_VID	PWM_VID	N17 PWM_VID for NVVDD supply
GPIO1	MEM_VDD_CTL	GC6_FB_EN	GC6_FB_EN	
GPIO2	LCD_BL_PWM	GPU_EVENT#	GPU_EVENT#	
GPIO3	LCD_VCC	RESERVED	RESERVED	RESERVED
GPIO4	LCD_BLEN	3V3_MAIN_EN	1V8_MAIN_EN	
GPIO5	3V3_MAIN_EN	FRAME_LOCK#	FRAME_LOCK#	
GPIO6	GPU_EVENT#	PSI	PSI	N17 PSI for NVVDD supply
GPIO7	3D VISION	LCD_BL_PWM	LCD_BL_PWM	
GPIO8	SYS_PEX_RST_MON#	IFPF_HPD	MEM_VDD_CTL	
GPIO9	THERM_ALERT	THERM_ALERT	THERM_ALERT	Same
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	MEM_VREF_CTL	Same
GPIO11	PWM_VID	LCD_VDD	LCD_VDD	
GPIO12	PWR_LEVEL	PWR_LEVEL	PWR_LEVEL	Same
GPIO13	PSI	LCD_BLEN	LCD_BLEN	
GPIO14	HPD_IFPA	HPD_IFPA	HPD_IFPA	Same
GPIO15	HPD_IFPC	HPD_IFPB	HPD_IFPB	
GPIO16	FRAME_LOCK#	SYS_PEX_RST_MON#	RESERVED	
GPIO17	HPD_IFPD	HPD_IFPD	HPD_IFPD	Same
GPIO18	HPD_IFPE	HPD_IFPE	HPD_IFPE	Same
GPIO19	HPD_IFPF or HPD_IFPB	3D VISION	3D VISION	
GPIO20	RESERVED	IFPC_HPD	RESERVED	
GPIO21	GPU_PEX_RST_HOLD#	GPU_PEX_RST_HOLD#	RESERVED (OC_WARN)	
GPIO22	-	-	RESERVED	New N17 GPIO
GPIO23	-	-	RESERVED	New N17 GPIO

GC6_20

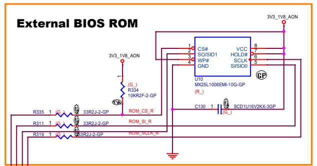


GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

STRAP

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
Straps			
C1	NC	STRAP5	Add necessary pull-up and pull-down resistor(s)
F6	MULTI_STRAP_REF0_GND	NC	Depopulate pull-down resistor to GND
F5	MULTI_STRAP_REF2_GND	NC	

External BIOS ROM



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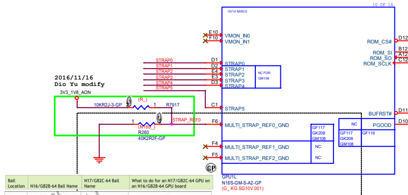


Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
F4	MULTI_STRAP_REF1_GND	VDD_SENSE	Leave unconnected

Table 15-1. Device Specific Strap Mode Selection

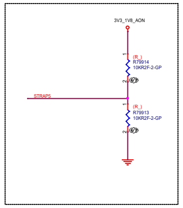


Table 15-15. SORx_EXPOSED - Display Link to Usage Bit Mapping

Displays		HDMI/DP	DVI	LVDS	eDP	Not in Use
Standard Mode	IFPAB		SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode AB	IFPA	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPB	SOR0_EXP = 1	SOR0_EXP = 1			SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF					
Split Mode EF	IFPAB					
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPF	SOR0_EXP = 1	SOR0_EXP = 1		SOR0_EXP = 0	SOR0_EXP = 0

Note:
- GB2B-64 package GPUs are configured with no display output so all links are considered Not in Use.

Table 13. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

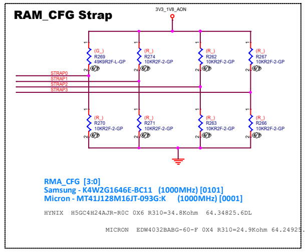
Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
			Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver[2]

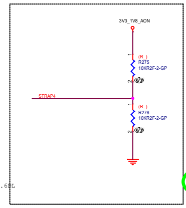
H5GC8H24AJR-R0C (AL/1x nm)	Hynix	KN.8GB0G.063
MT51J256M32HF-70 :B (Z11G/1xnm)	Micron	KN.8GB04.035

Table 15-2. Resistance Mapping to Hex Values

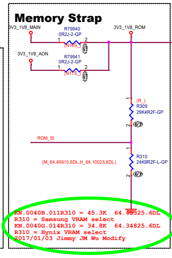
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

RAM_CFG Strap

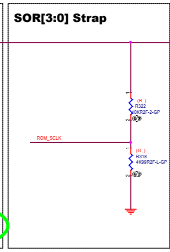




Memory Strap



SOR[3:0] Strap



DEVID_SEL, PCIE_CFG , SMB_ATL_ADDR VGA_DEVICE Strap

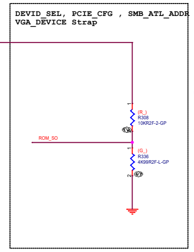
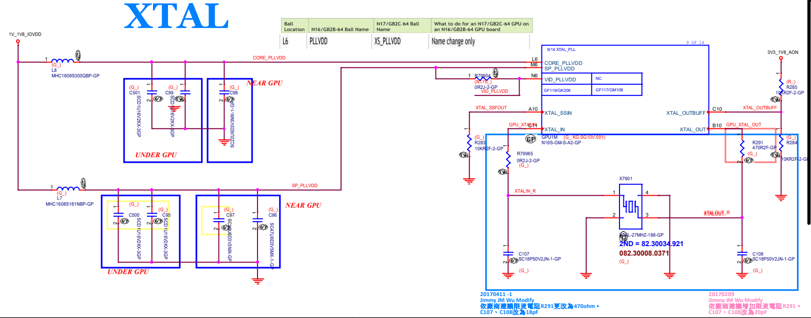


Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

XTAL

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
L6	PLLVDD	XS_PLLVDD	Name change only



THERMAL PROTECTION

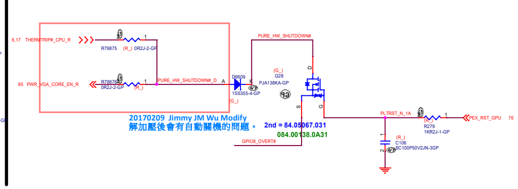


Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

TABLE 1: STRAP DECODE ACCORDING TO TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]	GND [3:0]
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

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Hsichih, Taipei Hsien

Title	GPU(4/5):GPIO/STRAP
Size	Custom
Document Number	Consumer AIO Petra238i
Rev	1A
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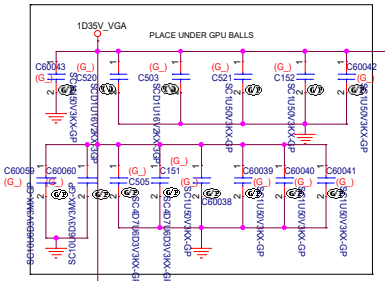
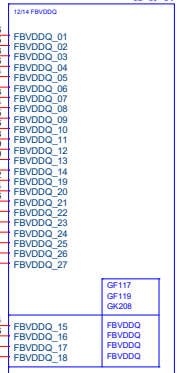
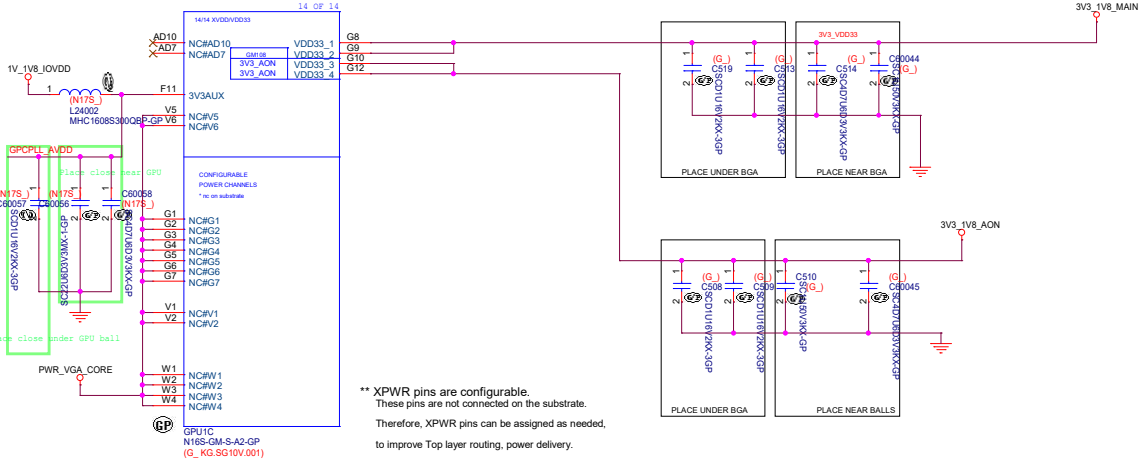
Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
Core Supply			
L11	VDD	VDDS	Name change only
L17	VDD	VDDS	"
M14	VDD	VDDS	"
P10	VDD	VDDS	"
P12	VDD	VDDS	"
P16	VDD	VDDS	"
P18	VDD	VDDS	"
T14	VDD	VDDS	"
U11	VDD	VDDS	"
U17	VDD	VDDS	"





Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
C24	FB_CAL_GND	FB_CAL_PU_GND	Name change only
B25	FB_CAL_TERM	FB_CAL_TERM_GND	Name change only
D22	FB_CAL_VDDQ	FB_CAL_PD_VDDQ	Name change only
H24	FBVDDQ_AON	FVBDDQ	Name change only
H26	FBVDDQ_AON	FVBDDQ	Name change only
J21	FBVDDQ_AON	FVBDDQ	Name change only
K21	FBVDDQ_AON	FVBDDQ	Name change only
IO Supply			
G10	3V3_AON	1V8_AON	Note power supply change
G12	3V3_AON	1V8_AON	Note power supply change
G8	3V3_MAIN	VDD18	Note power supply change
G9	3V3_MAIN	VDD18	Note power supply change

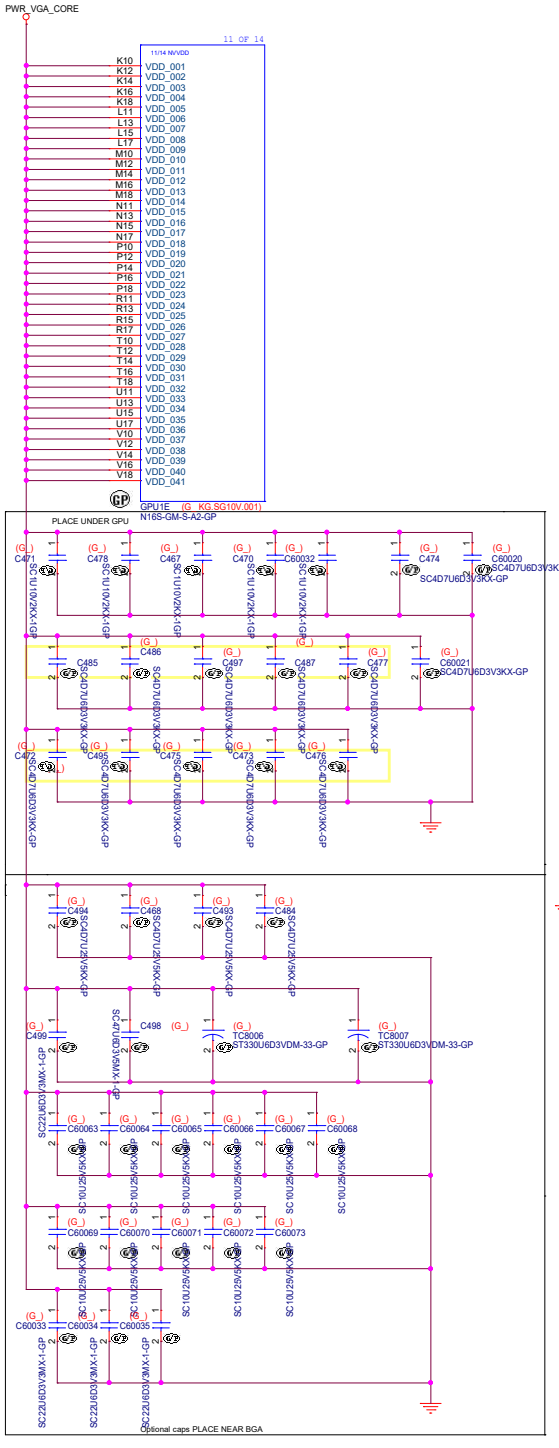


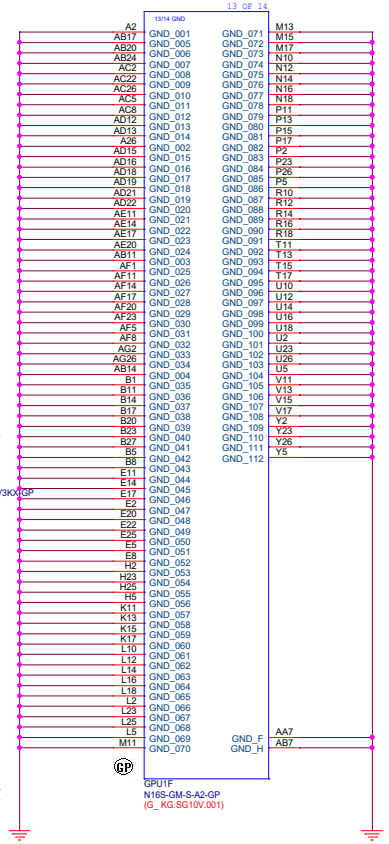
** XPWR pins are configurable.
These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,

to improve Top layer routing, power delivery.

Ball Location	N16/GB2B-64 Ball Name	N17/GB2C-64 Ball Name	What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board
D10	PGOOD	NC	Name change only
V5	FERMI_RSVD1	RSV_XVDD_63	Name change only
V6	FERMI_RSVD2	RSV_XVDD_64	Name change only
F11	NC	GPCPLL_AVDD	Connect to VDD_MAIN (1.8V)





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Title: GPU(5/5):PWR/GND

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78 MDA[63..0]
78 FBA_CMD[31:0]

78 FBA_DBI0 — FBA_DBI0
78 FBA_DBI1 — FBA_DBI1
78 FBA_DBI2 — FBA_DBI2
78 FBA_DBI3 — FBA_DBI3
78 FBA_EDC0 — FBA_EDC0
78 FBA_EDC1 — FBA_EDC1
78 FBA_EDC2 — FBA_EDC2
78 FBA_EDC3 — FBA_EDC3
78 FBA_WCK01 — FBA_WCK01
78 FBA_WCK01# — FBA_WCK01#
78 FBA_WCK23 — FBA_WCK23
78 FBA_WCK23# — FBA_WCK23#
78,81 FBA_WCK45 — FBA_WCK45
78,81 FBA_WCK45# — FBA_WCK45#
78,81 FBA_WCK67 — FBA_WCK67
78,81 FBA_WCK67# — FBA_WCK67#
78 CLKA0
78 CLKA0#

78 FBA_DBI4 — FBA_DBI4
78 FBA_DBI5 — FBA_DBI5
78 FBA_DBI6 — FBA_DBI6
78 FBA_DBI7 — FBA_DBI7
78 FBA_EDC4 — FBA_EDC4
78 FBA_EDC5 — FBA_EDC5
78 FBA_EDC6 — FBA_EDC6
78 FBA_EDC7 — FBA_EDC7
78,81 FBA_WCK45 — FBA_WCK45
78,81 FBA_WCK45# — FBA_WCK45#
78,81 FBA_WCK67 — FBA_WCK67
78,81 FBA_WCK67# — FBA_WCK67#
78 CLKA1
78 CLKA1#

TABLE
GDDR5 VIDEO MEMORY

	072.05424.0A0U	072.44132.000U	072.04032.000N
	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-D

VRAM1B — 2 OF 2 — Normal

FBA_CMD6	K4	A8/A7	DQ0	A4	MDA0
FBA_CMD11	H5	A9/A1	DQ1	A2	MDA1
FBA_CMD10	H4	A10/A0	DQ2	B4	MDA2
FBA_CMD7	K5	A11/A6	DQ3	B2	MDA3
FBA_CMD9	J5	A12/A13	DQ4	E4	MDA4
			DQ5	E2	MDA5
FBA_CMD2	H11		DQ6	F4	MDA6
FBA_CMD4	K10	BA0/A2	DQ7	F2	MDA7
FBA_CMD3	K11	BA1/A5	DQ8	A11	MDA8
FBA_CMD1	H10	BA2/A4	DQ9	A13	MDA9
		BA3/A3	DQ10	B11	MDA10
FBA_CMD8	J4		DQ11	B13	MDA11
FBA_CMD12	G3	ABI#	DQ12	E11	MDA12
FBA_CMD0	G12	RAS#	DQ13	E13	MDA13
FBA_CMD15	L3	CS#	DQ14	F11	MDA14
FBA_CMD5	L12	CAS#	DQ15	F13	MDA15
		WE#	DQ16	U11	MDA16
CLKA0	J12		DQ17	U13	MDA17
CLKA0#	J11	CK	DQ18	T11	MDA18
FBA_CMD14	J3	CK#	DQ19	T13	MDA19
		CKE#	DQ20	N11	MDA20
FBA_DBI0	D2		DQ21	N13	MDA21
FBA_DBI1	D13	DBI0#	DQ22	M11	MDA22
FBA_DBI2	P13	DBI1#	DQ23	M13	MDA23
FBA_DBI3	P2	DBI2#	DQ24	U4	MDA24
		DBI3#	DQ25	U2	MDA25
FBA_CMD13	J2		DQ26	T4	MDA26
		RESET#	DQ27	T2	MDA27
	J10		DQ28	N4	MDA31
FBA0_ZQ1	J13	SEN	DQ29	N2	MDA30
	J1	ZQ	DQ30	M4	MDA29
		MF	DQ31	M2	MDA28
			EDC0	C2	FBA_EDC0
FBA_WCK01	D4	WCK01	EDC1	C13	FBA_EDC1
FBA_WCK01#	D5	WCK01#	EDC2	R13	FBA_EDC2
			EDC3	R2	FBA_EDC3
FBA_WCK23	P4	WCK23			
FBA_WCK23#	P5	WCK23#			

H5GC4H24AJR-T2C-GP
(H_KN.8GB0G.063,M_KN.8GB04.035)

Byte 0 0~7
Byte 1 8~15
Byte 2 16~23
Byte 3 24~31

121R2F-GP (G_) R8103 (GP)

CLKA0
CLKA0#
(G_) R8105 40D2R2F-GP (GP)
(G_) R8106 40D2R2F-GP (GP)
GPU_CLK1_TER
(R_) C8102 SCD01U50V2KX-1GP (GP)

VRAM2B — 2 OF 2 — Normal

FBA_CMD22	K4	A8/A7	DQ0	A4	MDA56
FBA_CMD27	H5	A9/A1	DQ1	A2	MDA57
FBA_CMD26	H4	A10/A0	DQ2	B4	MDA58
FBA_CMD23	K5	A11/A6	DQ3	B2	MDA59
FBA_CMD25	J5	A12/A13	DQ4	E4	MDA60
			DQ5	E2	MDA61
FBA_CMD18	H11		DQ6	F4	MDA62
FBA_CMD20	K10	BA0/A2	DQ7	F2	MDA63
FBA_CMD19	K11	BA1/A5	DQ8	A11	MDA48
FBA_CMD17	H10	BA2/A4	DQ9	A13	MDA49
		BA3/A3	DQ10	B11	MDA50
FBA_CMD24	J4		DQ11	B13	MDA51
FBA_CMD28	G3	ABI#	DQ12	E11	MDA54
FBA_CMD16	G12	RAS#	DQ13	E13	MDA52
FBA_CMD31	L3	CS#	DQ14	F11	MDA55
FBA_CMD21	L12	CAS#	DQ15	F13	MDA53
		WE#	DQ16	U11	MDA40
CLKA1	J12		DQ17	U13	MDA41
CLKA1#	J11	CK	DQ18	T11	MDA42
FBA_CMD30	J3	CK#	DQ19	T13	MDA43
		CKE#	DQ20	N11	MDA44
FBA_DBI7	D2		DQ21	N13	MDA45
FBA_DBI6	D13	DBI0#	DQ22	M11	MDA46
FBA_DBI5	P13	DBI1#	DQ23	M13	MDA47
FBA_DBI4	P2	DBI2#	DQ24	U4	MDA32
		DBI3#	DQ25	U2	MDA33
FBA_CMD29	J2		DQ26	T4	MDA34
		RESET#	DQ27	T2	MDA35
	J10		DQ28	N4	MDA36
FBA1_ZQ3	J13	SEN	DQ29	N2	MDA37
	J1	ZQ	DQ30	M4	MDA38
		MF	DQ31	M2	MDA39
			EDC0	C2	FBA_EDC7
FBA_WCK67	D4	WCK01	EDC1	C13	FBA_EDC6
FBA_WCK67#	D5	WCK01#	EDC2	R13	FBA_EDC5
			EDC3	R2	FBA_EDC4
FBA_WCK45	P4	WCK23			
FBA_WCK45#	P5	WCK23#			

H5GC4H24AJR-T2C-GP
(H_KN.8GB0G.063,M_KN.8GB04.035)

Byte 7 56~63
Byte 6 48~55
Byte 5 40~47
Byte 4 32~39

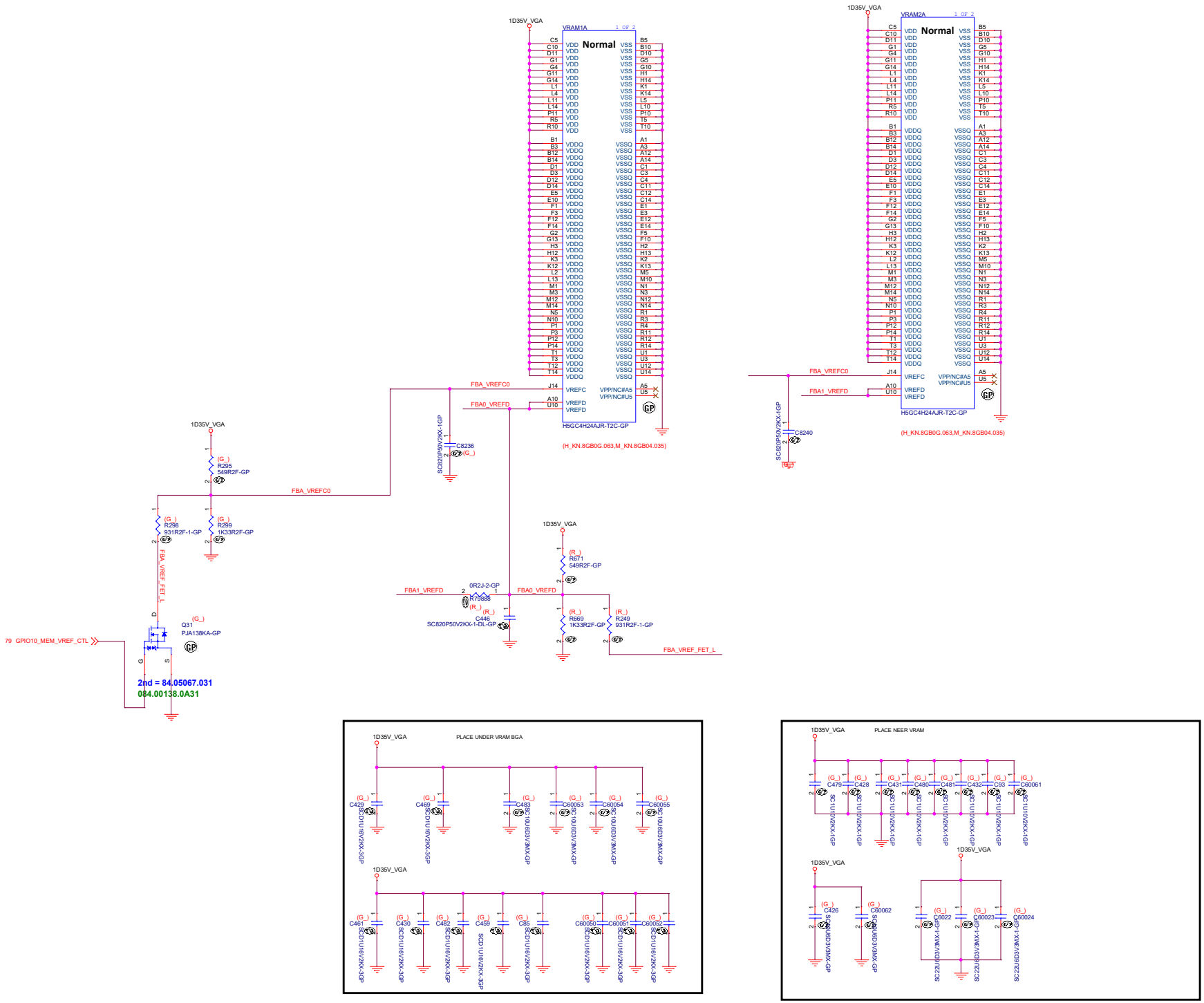
121R2F-GP (G_) R8104 (GP)

CLKA1
CLKA1#
(G_) R8102 40D2R2F-GP (GP)
(G_) R8101 40D2R2F-GP (GP)
GPU_CLK1_TER
(R_) C8101 SCD01U50V2KX-1GP (GP)

U22 DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A
Size: A3 | Document Number: Consumer AIO Petra23811 | Rev: 1A
Date: Wednesday, July 25, 2018 | Sheet 81 of 108



U22 DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM POWER***	
Size A2	Document Number **Consumer AIO Petra2381**	Rev 1A
Date: Wednesday, July 25, 2018	Sheet 82 of 108	

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Title
VRAM 5,6 (2/4)

Size	Document Number	Rev
A	Consumer AIO Petra238i	1A

Date:	Sheet	of
Wednesday, July 25, 2018	83	107

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<Core Design>

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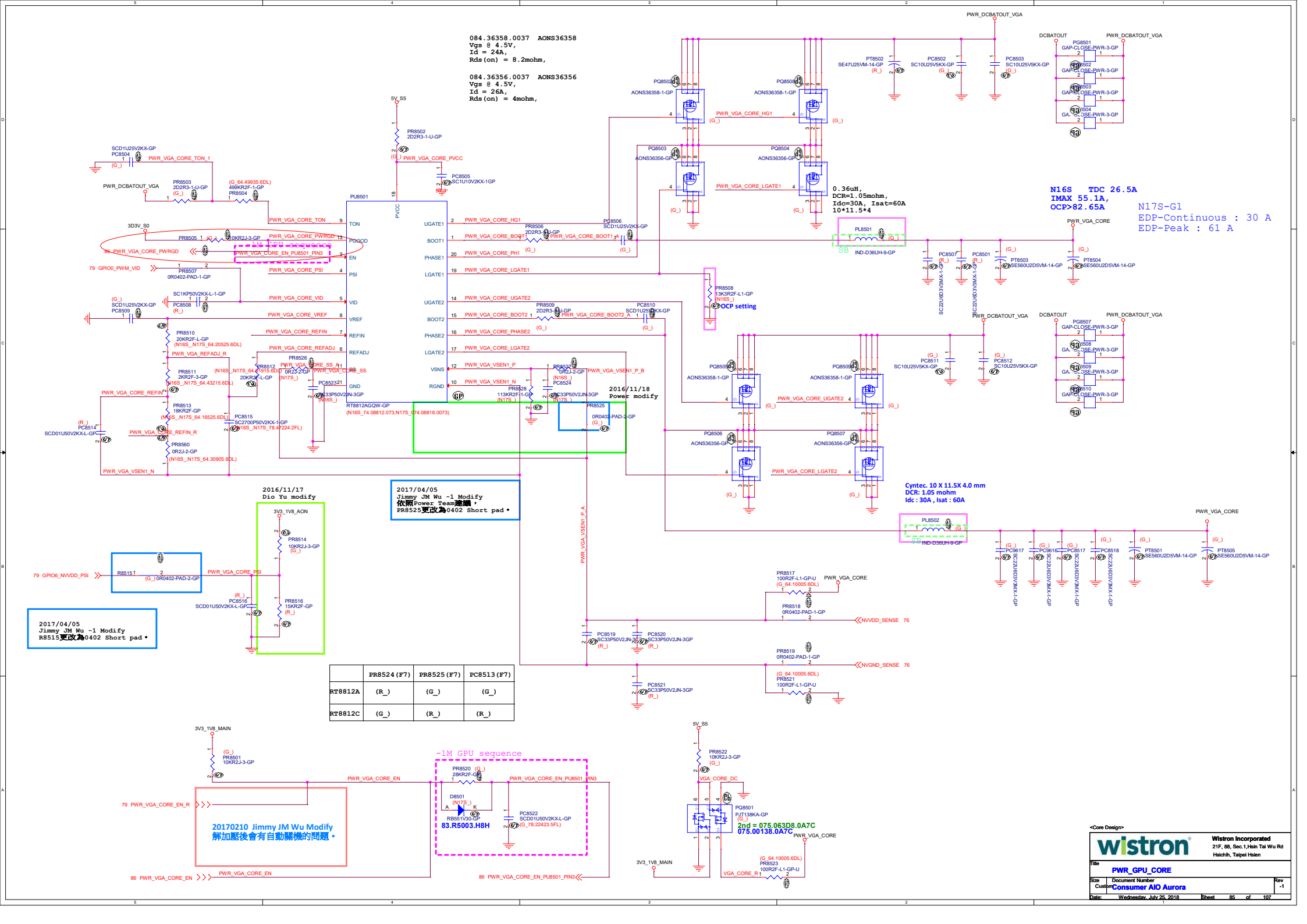
Hsichih, Taipei Hsien

Title: VRAM 7,8 (2/4)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 84 of 107

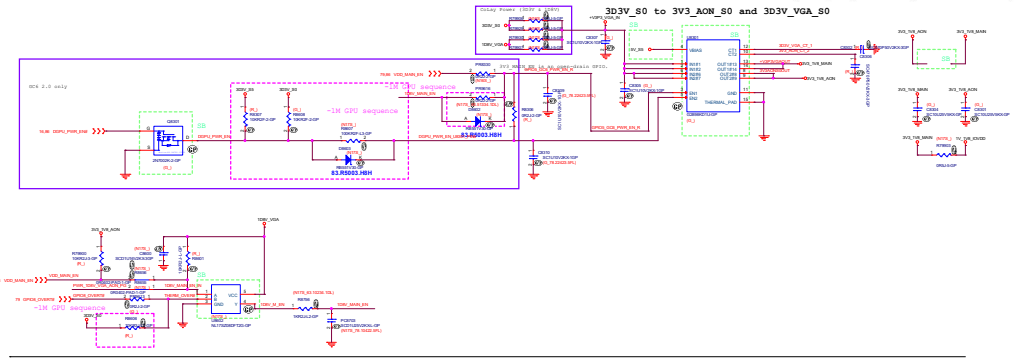


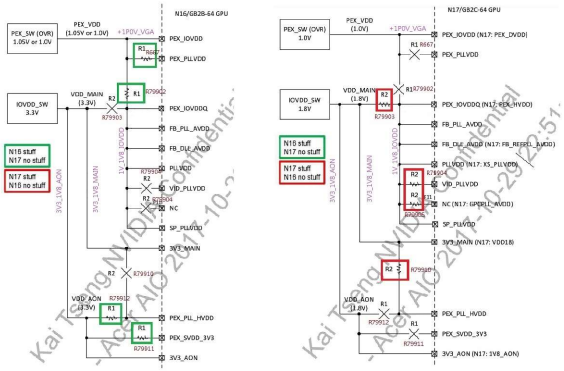
	PR8524(F7)	PR8525(F7)	PC8513(F7)
RT8812A	(R_)	(G_)	(G_)
RT8812C	(G_)	(R_)	(R_)

For GPU & Pull High
N16S:3V3_1V8_MAIN=3.3V
3V3_1V8_AON=3.3V
[DG-07170-001 Rev:D]Power up sequence:
3.3V ==> NVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.35V)
N17S:3V3_1V8_MAIN=1.8V
3V3_1V8_AON=3.3V

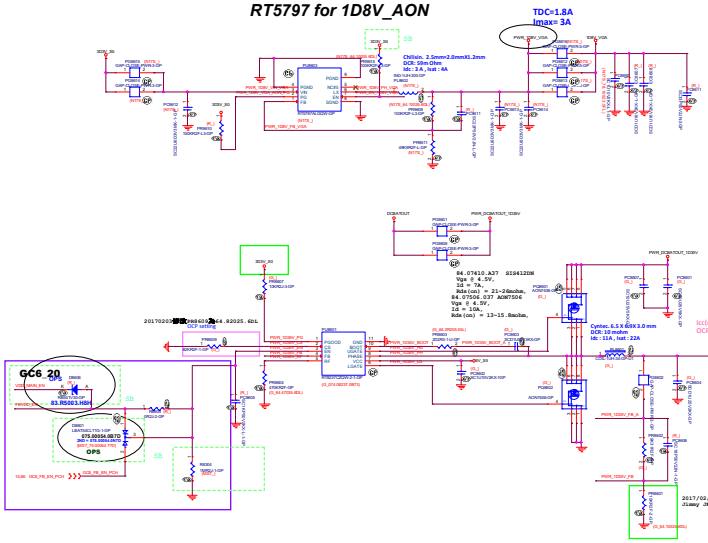
1V8_AON → 1V8_MAIN → 3V3_SYS → NVVDD → PEX_VDD → FBVDD/Q

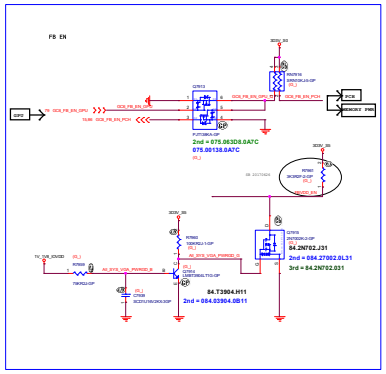
3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0



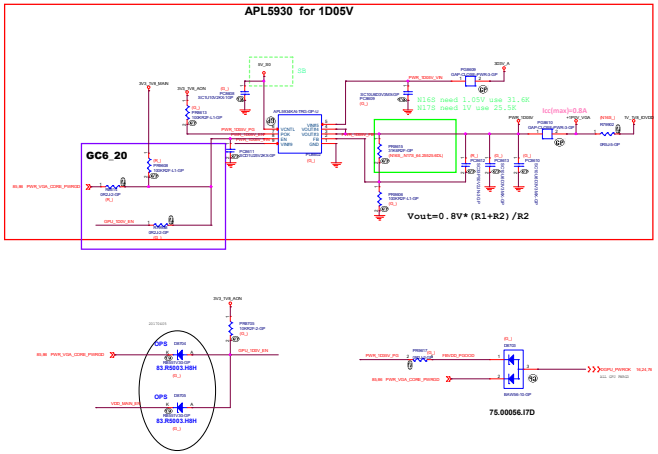


RT5797 for 1D8V_AON

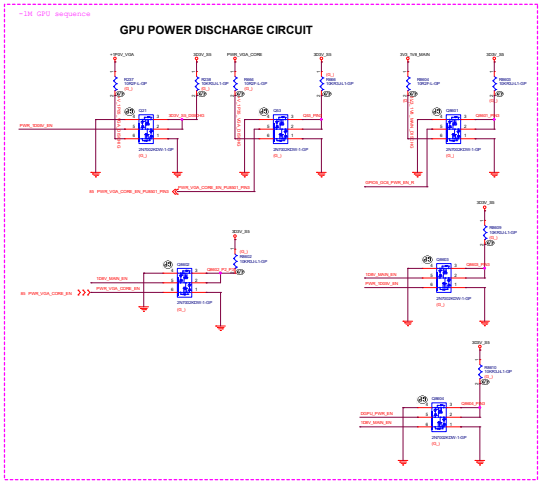




APL5930 for 1D05V



GPU POWER DISCHARGE CIRCUIT



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Hsichih, Taipei Hsien

DISCRETE VGA POWER

Consumer AIO Petra2386

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Hsichih, Taipei Hsien

Title: GPU Switch

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 87 of 107

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<Core Design>

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Hsichih, Taipei Hsien

Title: GPU Switch

Size: A

Document Number: Consumer AIO Petra238i

Rev: 1A

Date: Wednesday, July 25, 2018

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Hsichih, Taipei Hsien

Title: GPU Others

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 89 of 107

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<Core Design>

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Title: NFC

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

Date: Wednesday, July 25, 2018 | Sheet 90 of 107

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<Core Design>

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Title: TPM_(R)

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<Core Design>

Wistron Incorporated
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Title: PS2_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

Wistron Incorporated
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Title: Express Card_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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<Core Design>

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Title: Smart Card_(R)

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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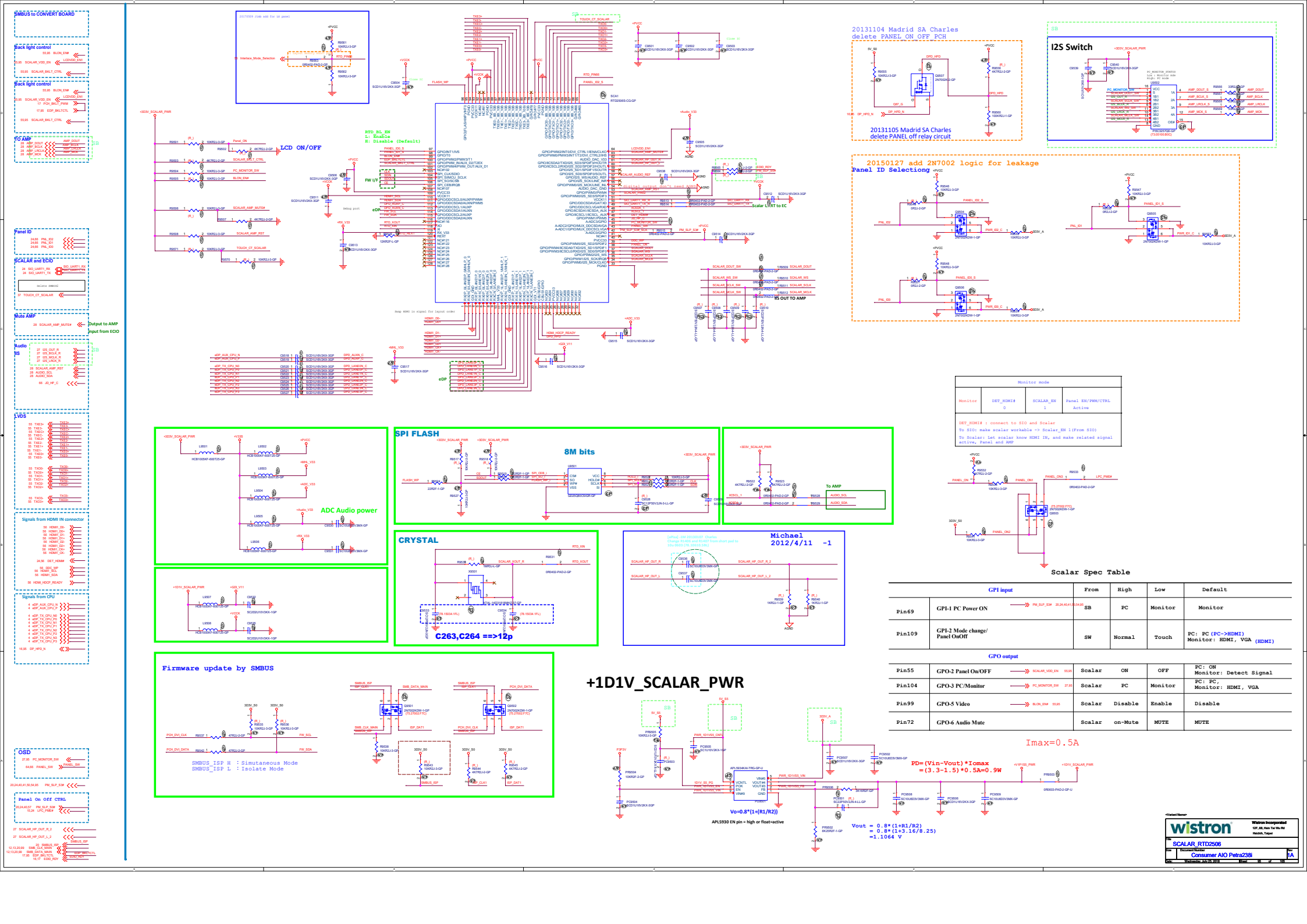
SMBUS to CONVERT BOARD
Back light control
Back light control
TO AMP
Panel ID
SCALAR and ECIO
Mute AMP
Audio I/S
LVDS
Signals from HDMI IN connector
Signals from CPU
OSD
Panel On Off CTRL
20131104 Madrid SA Charles
delete PANEL ON OFF PCH
20131105 Madrid SA Charles
delete PANEL off relay circuit
I2S Switch
20150127 add 2N7002 logic for leakage
Panel ID Selecting
LCD ON/OFF
RTD BS_EN
L: Enable
H: Disable (Default)
FW I/F
eDP
SPI FLASH
8M bits
ADC Audio power
CRYSTAL
C263,C264 ==>12p
Michael
2012/4/11 -1
Firmware update by SMBUS
SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode
+1D1V_SCALAR_PWR
Imax=0.5A
PD=(Vin-Vout)*Iomax
=(3.3-1.5)*0.5A=0.9W
Vo=0.8*(1+(R1/R2))
APL5930 EN pin = high or float=active
Vout = 0.8*(1+R1/R2)
= 0.8*(1+3.16/8.25)
=1.1064 V
Monitor mode
Monitor
DET_HDMI#
SCALAR_EN
Panel EN/PWM/CTRL
0
1
Active
DET_HDMI# : connect to SIO and Scalar
To SIO: make scalar workable -> Scalar_EN 1(From SIO)
To Scalar: Let scalar know HDMI IN, and make related signal active, Panel and AMP
Scalar Spec Table
GPI input
From
High
Low
Default
Pin69
GPI-1 PC Power ON
SB
PC
Monitor
Monitor
Pin109
GPI-2 Mode change/ Panel OnOff
SW
Normal
Touch
PC: PC (PC->HDMI)
Monitor: HDMI, VGA (HDMI)
GPO output
Pin55
GPO-2 Panel On/OFF
SCALAR_VDD_EN
Scalar
ON
OFF
PC: ON
Monitor: Detect Signal
Pin104
GPO-3 PC/Monitor
PC_MONITOR_SW
Scalar
PC
Monitor
PC: PC,
Monitor: HDMI, VGA
Pin99
GPO-5 Video
SLON_EN#
Scalar
Disable
Enable
Disable
Pin72
GPO-6 Audio Mute
Scalar
on-Mute
MUTE
MUTE
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SCALAR_RTD2506
Consumer AIO Petra238i
Wednesday, April 25, 2018

SSID = SDIO

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Title: Scalar Power

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<Core Design>

Wistron Incorporated
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Title: Inter LAN_(R)

Size: A

Document Number: Consumer AIO Petra238i

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Date: Wednesday, July 25, 2018

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Title: LAN Switch_(R)

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XDP for CPU

6 H_PREQ_N
6 H_PRDY_N
6 SKL_PCUSTB_0_DP
6 SKL_PCUSTB_0_DN
6 BPM_CPU_N0
6 BPM_CPU_N1
6 SKL_PCUSTB_1_DP
6 SKL_PCUSTB_1_DN

20,24 PM_PWRBTN#

20,40,65 PCH_SYSPWROK

18 XDP_CLK_CON
18 XDP_CLK_CON#

6 CFG[0..15]

6,20 H_TCK
6 H_TDO
6 H_TDI
6 H_TMS
6,65 H_TRST_N

15,23,25 SPI_WP_PCH
6 XDP_PCUDEBUG3

21 XDP_PRDY_N
21 PCH_XDP_PREQ_R_N

15,23,25 SPI_SI_PCH

20,24,65 RSMRST#_SIO

6,40 CPU_VCCST_PWRGD

24,64 PWRBTN_IN

20 ITP_PMODE

20 FP_RST_N

20 PCH_JTAG_TCK

6,17,65 PLTRST_CPU_N

6,20,65 H_PWRGD

12,13,20,95 SMB_DATA_MAIN
12,13,20,95 SMB_CLK_MAIN

PCH_XDP_PREQ_R_N — R9916 0R0402-PAD-2-GP — H_PREQ_N — To CPU XDP / To PCH XDP

XDP_PRDY_N — R9917 0R0402-PAD-2-GP — H_PRDY_N — To CPU XDP / To PCH XDP

SPI_SI_PCH — R9904 (R_) 1KR2F-3-GP

PCH_SYSPWROK — R9905 0R0402-PAD-2-GP — XDP_VR_READY

C9901 SCD1U16V2KX-3GP (R_) — SB

RSMRST#_SIO — R9906 (R_) 1KR2F-3-GP

H_PWRGD — R9907 (R_) 1KR2F-3-GP — XDP_PWRGD

CPU_VCCST_PWRGD — R9908 (DBG) 1KR2F-3-GP

1D0V_S5 — R9909 (R_) 2K2R2J-2-GP

PLTRST_CPU_N — R9910 (DBG) 1KR2J-1-GP

ITP_PMODE — R9912 (R_) 0R2J-2-GP — H_RSTOUT_XDP_N

VCC_IO — R9914 (DBG) 150R2F-1-GP

CFG0 — R9915 (DBG) 1KR2F-3-GP — XDP_PWR_DEBUG

PWRBTN_IN — To CPU XDP / To PCH XDP

PCH_JTAG_TCK — To CPU XDP / To PCH XDP

XDP for CPU

1D0V_S5

XDPC1 SMC-CONN60A-GP

R9903 (R_) 0R2J-2-GP — XDP_PCUDEBUG3

H_PREQ_N
H_PRDY_N

		MH1	
	1	2	
	3	4	SKL_PCUSTB_0_DP
	5	6	SKL_PCUSTB_0_DN
	7	8	
CFG0	9	10	CFG8
CFG1	11	12	CFG9
	13	14	
CFG2	15	16	CFG10
CFG3	17	18	CFG11
	19	20	
BPM_CPU_N0	21	22	SKL_PCUSTB_1_DP
BPM_CPU_N1	23	24	SKL_PCUSTB_1_DN
	25	26	
CFG4	27	28	CFG12
CFG5	29	30	CFG13
	31	32	
CFG6	33	34	CFG14
CFG7	35	36	CFG15
	37	38	
XDP_PWRGD	39	40	XDP_CLK_CON
PWRBTN_IN	41	42	XDP_CLK_CON#
	43	44	
XDP_PWR_DEBUG	45	46	H_RSTOUT_XDP_N
XDP_VR_READY	47	48	FP_RST_N
	49	50	
SMB_DATA_MAIN	51	52	H_TDO
SMB_CLK_MAIN	53	54	H_TRST_N
PCH_JTAG_TCK	55	56	H_TDI
H_TCK	57	58	H_TMS
	59	60	XDP_PRS
		MH2	

(R_) GP

R9911 0R2J-2-GP (R_)

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Title: XDP&ITP

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Title: Table of Content

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<Core Design>

Wistron Incorporated
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Title: GPIO table

Size: A | Document Number: Consumer AIO Petra238i | Rev: 1A

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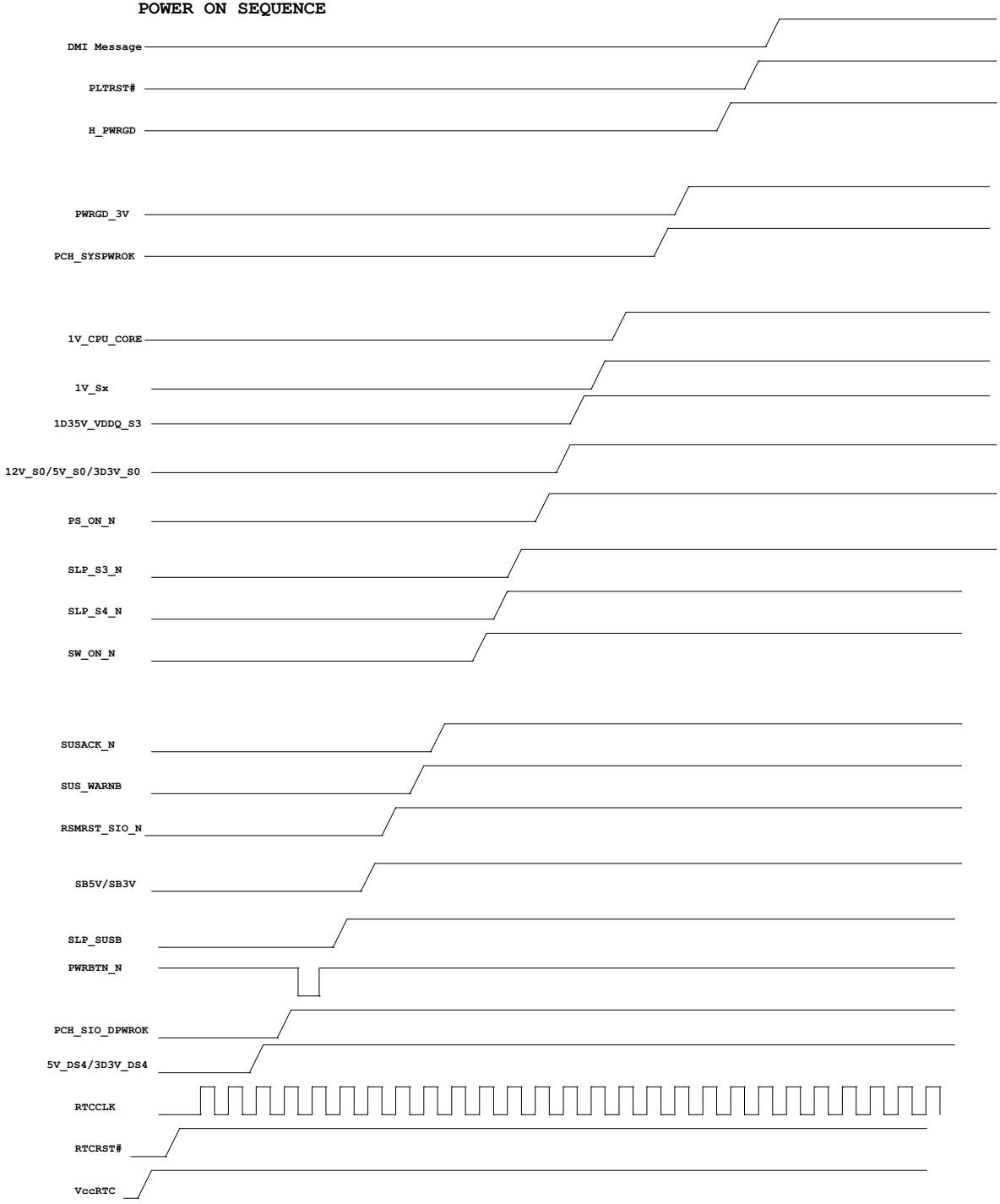
POWER ON SEQUENCE



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Hsichih, Taipei Hsien

Title: Power sequence

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

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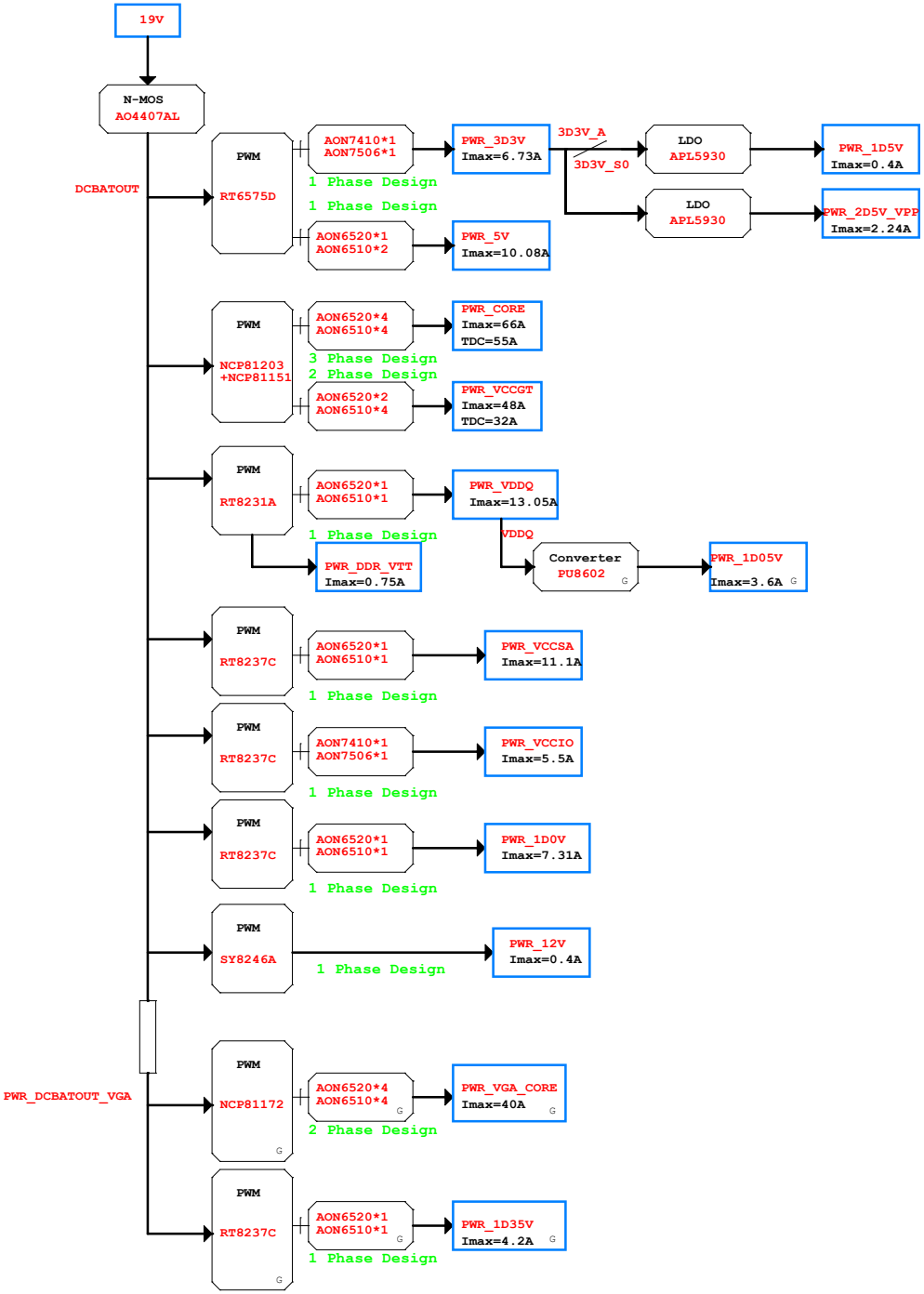

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File: Power Block Diagram

Size: Custom | Document Number: Consumer AIO Petra238i | Rev: 1A

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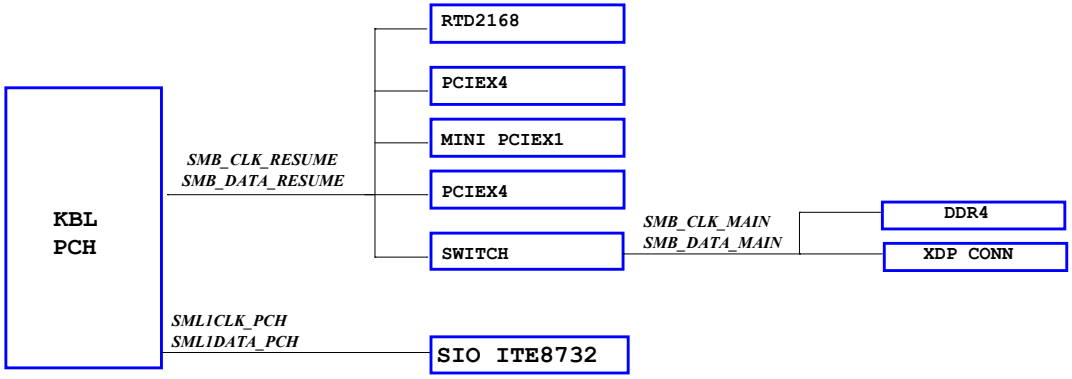

<Core Design>

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Hsichih, Taipei Hsien

Title: SMBUS Block Diagram

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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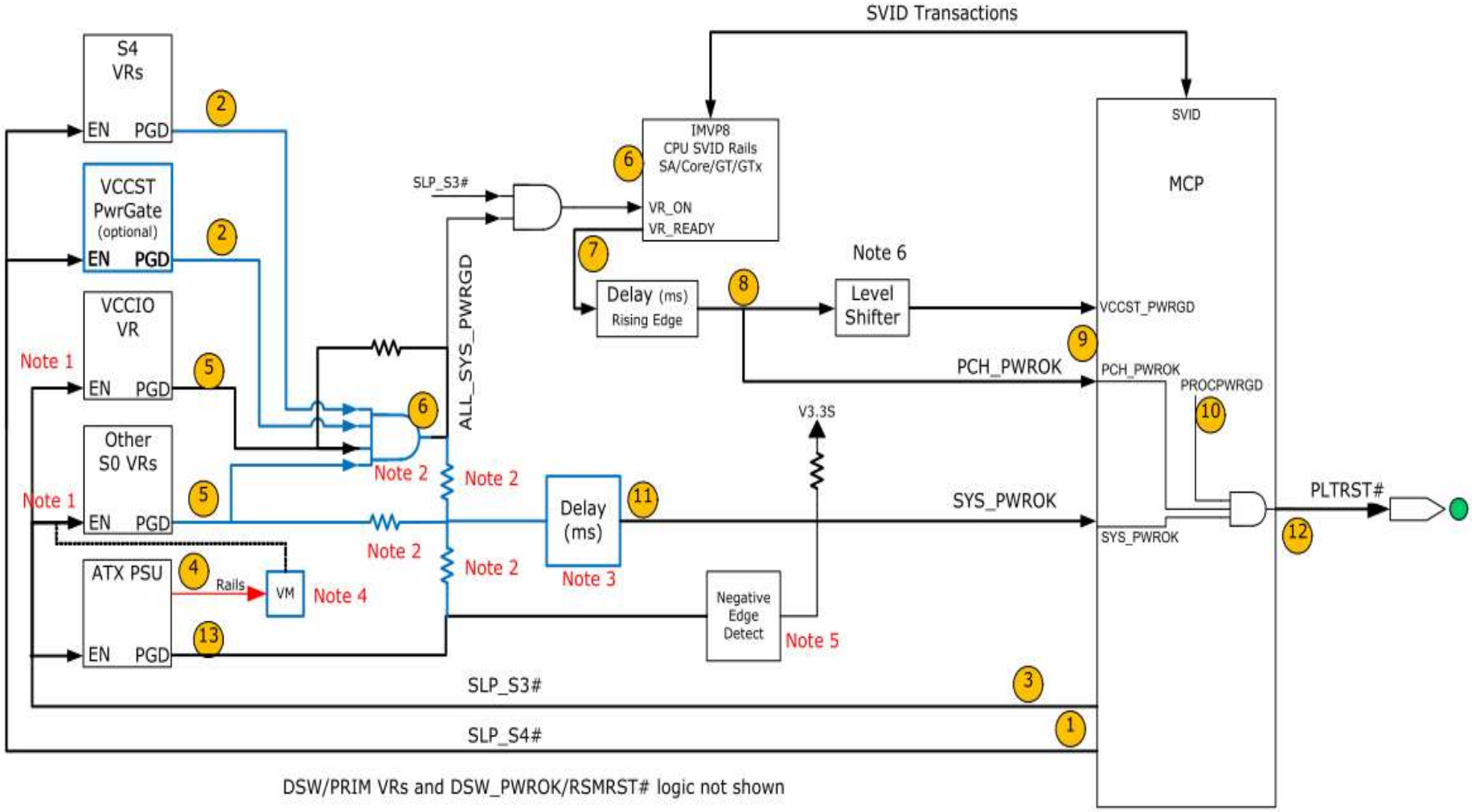

<Core Design>

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Hsichih, Taipei Hsien

Title: RESET Flow Chart

Size: C | Document Number: Consumer AIO Petra238i | Rev: 1A

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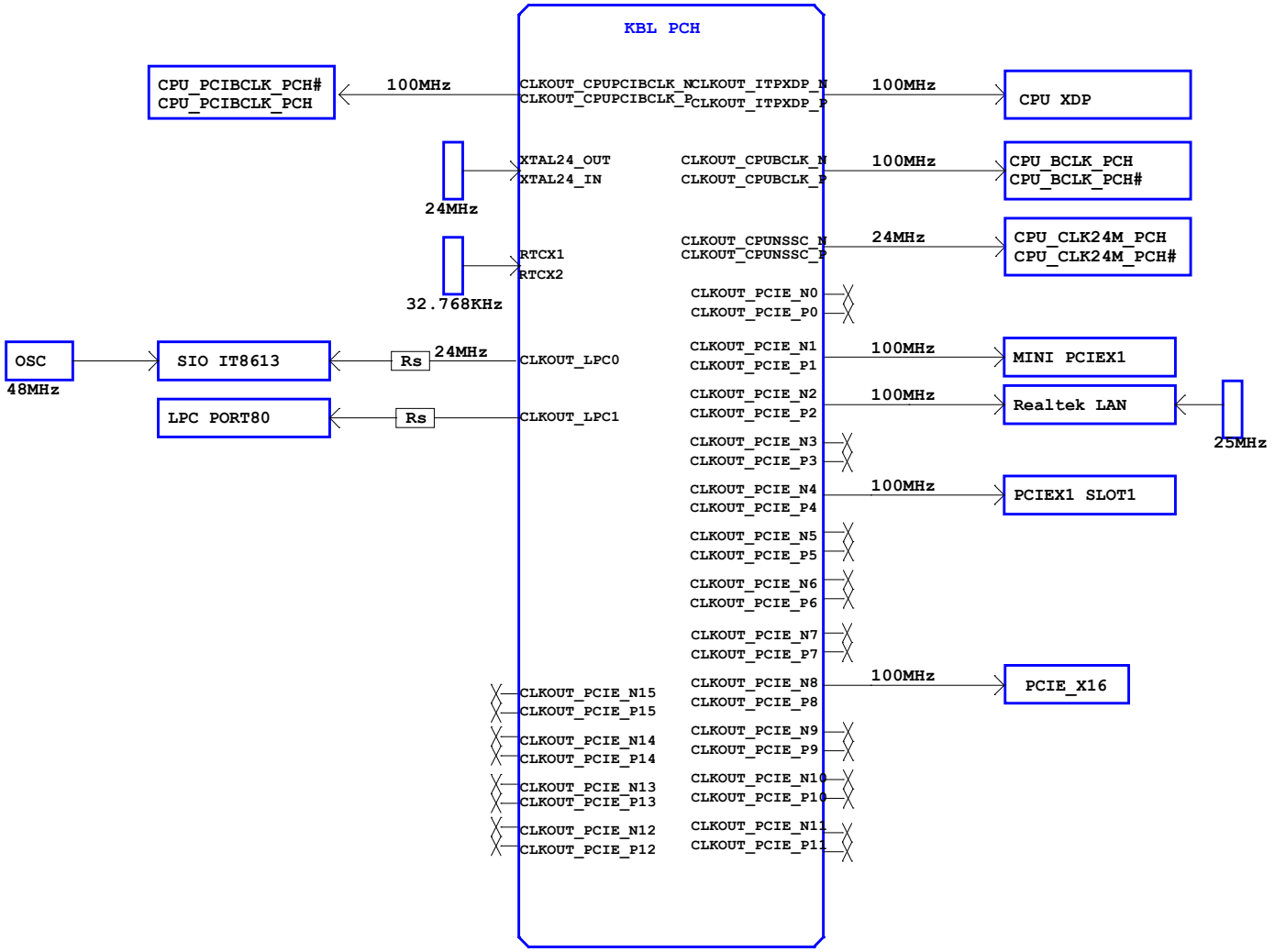

<Core Design>

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Title: Clock MAP

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Title
Other RSVD

Size	Document Number	Rev
A	Consumer AIO Petra238i	1A

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