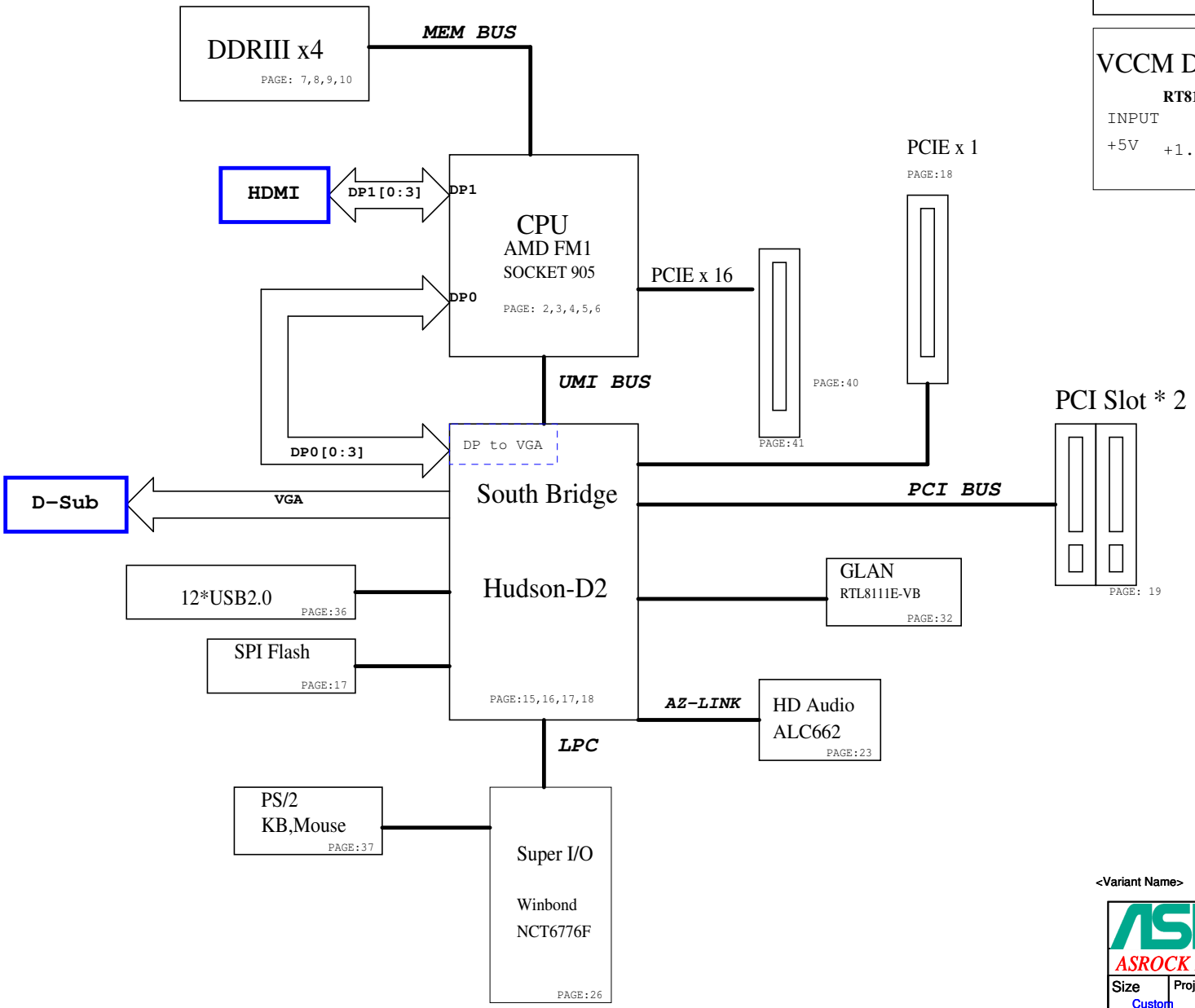
A55iCafe

Revision: G/A 1.01

AMD FM1 + Hudson-D2 ATX



1.1V DC/DC

APW7120

INPUT	OUTPUT
+3V	+1.1V~1.8V

PAGE:32

ATX Power

+5VSB	+12V
+3.3V	-5V
+5V	-12V

PAGE:29

VCCM DC/DC

RT8105PS

INPUT	OUTPUT
+5V	+1.35V~2.0V

PAGE:31

CPU DC/DC

L6717A

INPUT	OUTPUT
+12V	+1.1V~2.0V

PAGE:33~34

System Regulator

INPUT	OUTPUT
+5VSB	+3VSB
+3VSB	+1.1VSB
+3V	+1.8V
VCCM	VTT_DDR
VCCM	+1.1VSB
+1.8V	+1.5V
+3VSB	+1.2V_HT
+3VSB	+1V
+5V_DUAL	+3V_DUAL

PAGE:30,48

PCB LAYER

L1 : Component (S1)
L2 : VCC
L3 : GND
L4 : Solder (S4)

<Variant Name>

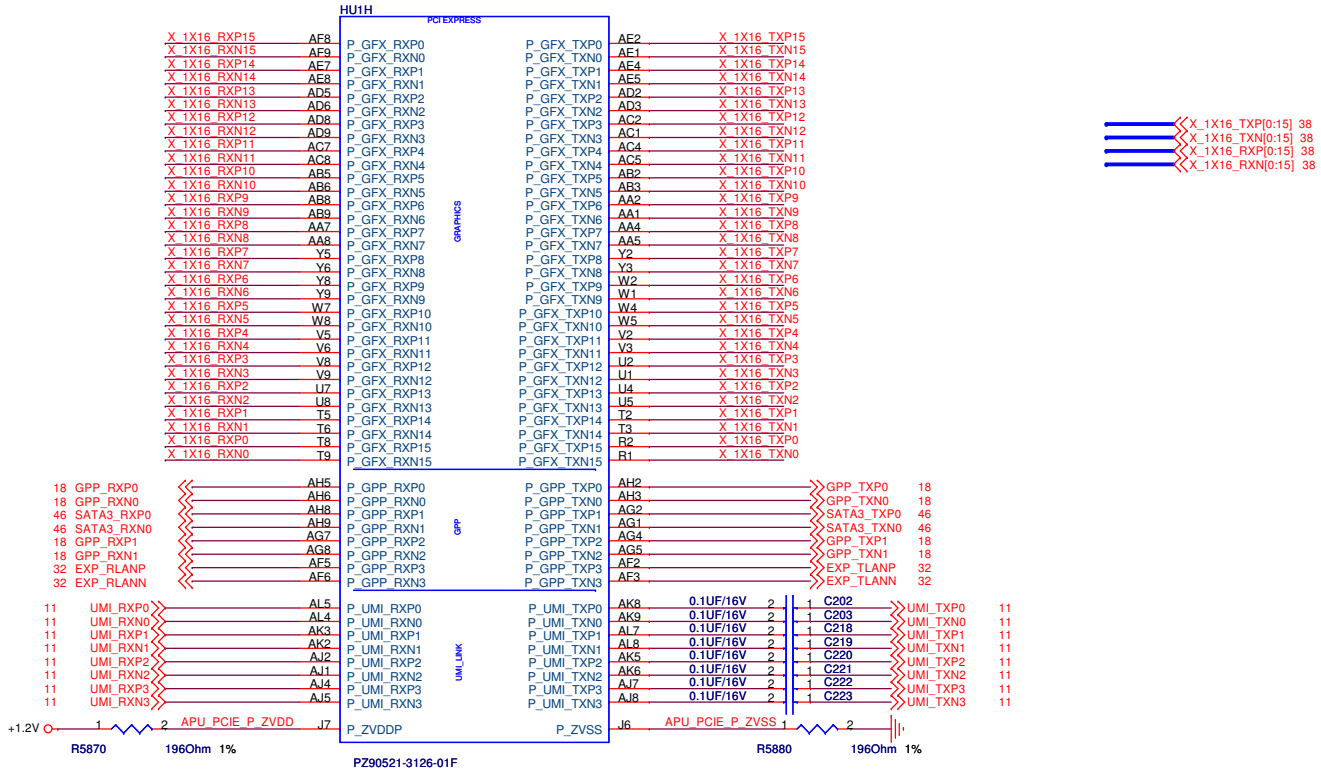
ASRock™ Title : BLOCK

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
Custom	A55icafe	1.01

Date: Wednesday, July 27, 2011 Sheet 1 of 46

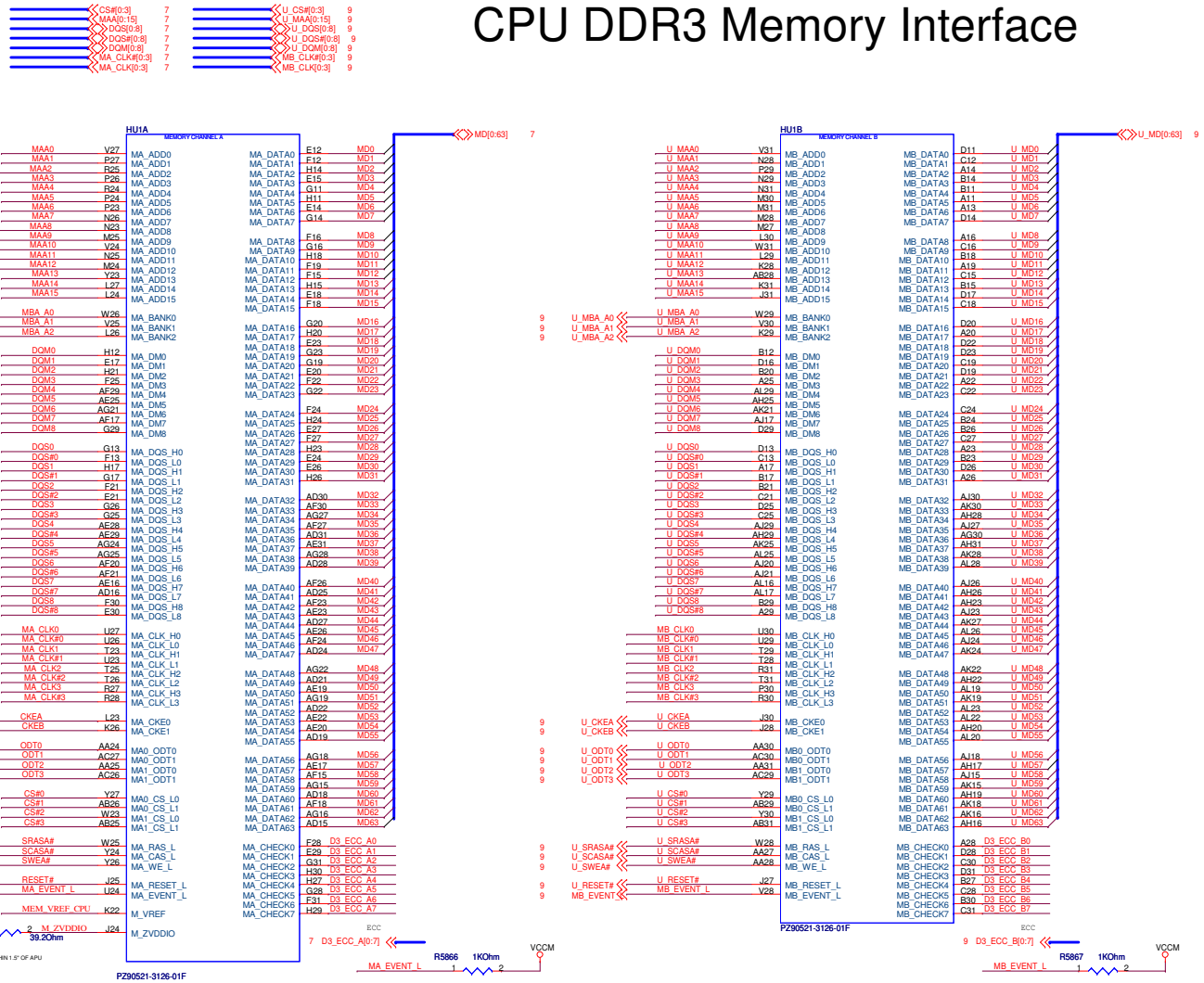
CPU HyperTransport Interface



<Variant Name>

ASRock Inc.	Title : M3_HDT	
	Engineer: Ting-Jun_Fu	
Size: A3	Project Name: A55icafe	Rev: 1.01
Date: Monday, July 25, 2011	Sheet 2 of 46	

CPU DDR3 Memory Interface



<Variant Name>

ASRock Inc

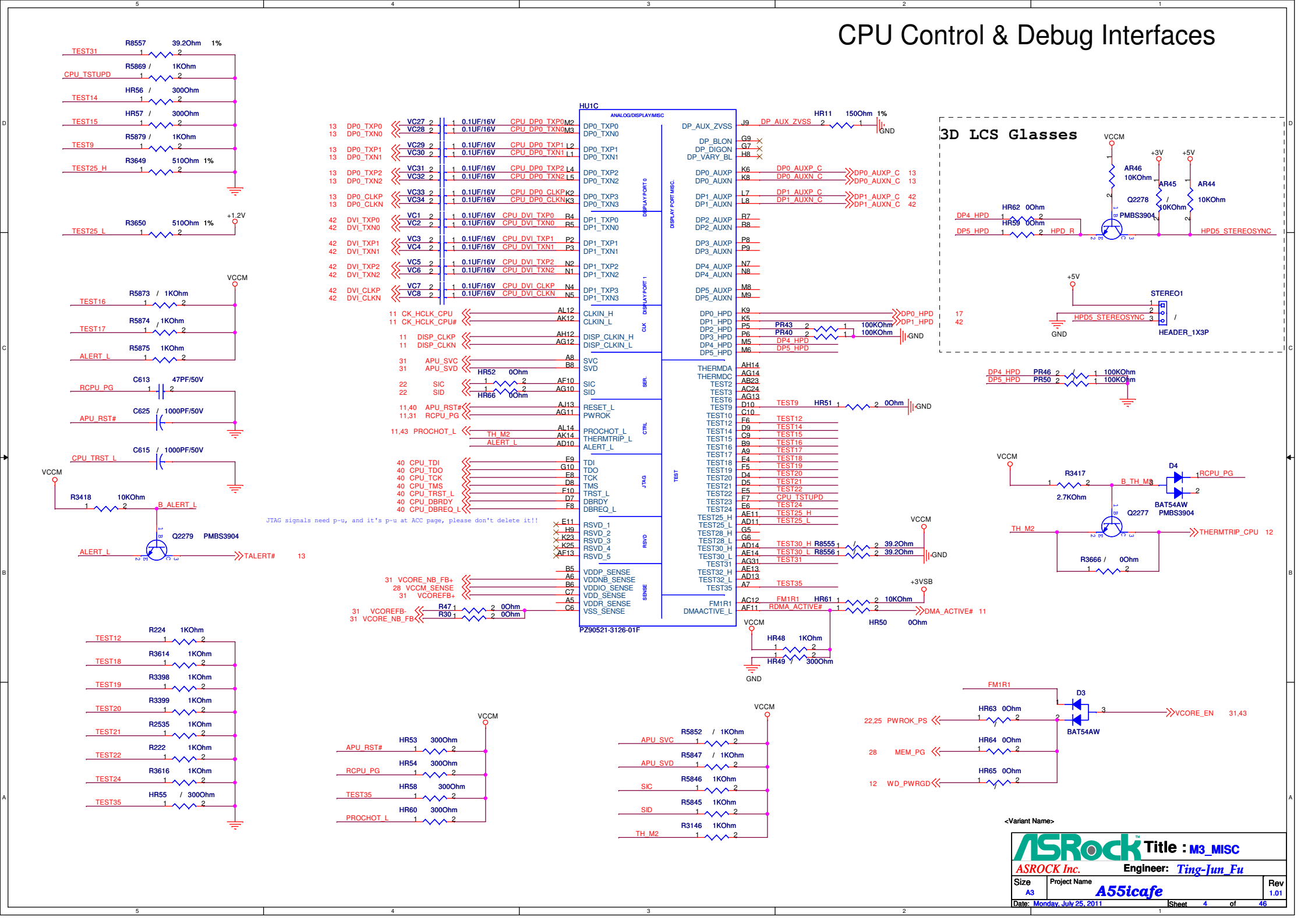
Title : MD_DDRIII

Engineer: Ting-Jun_Fu

Size	Project Name	Rev
C	A55icafe	1.01

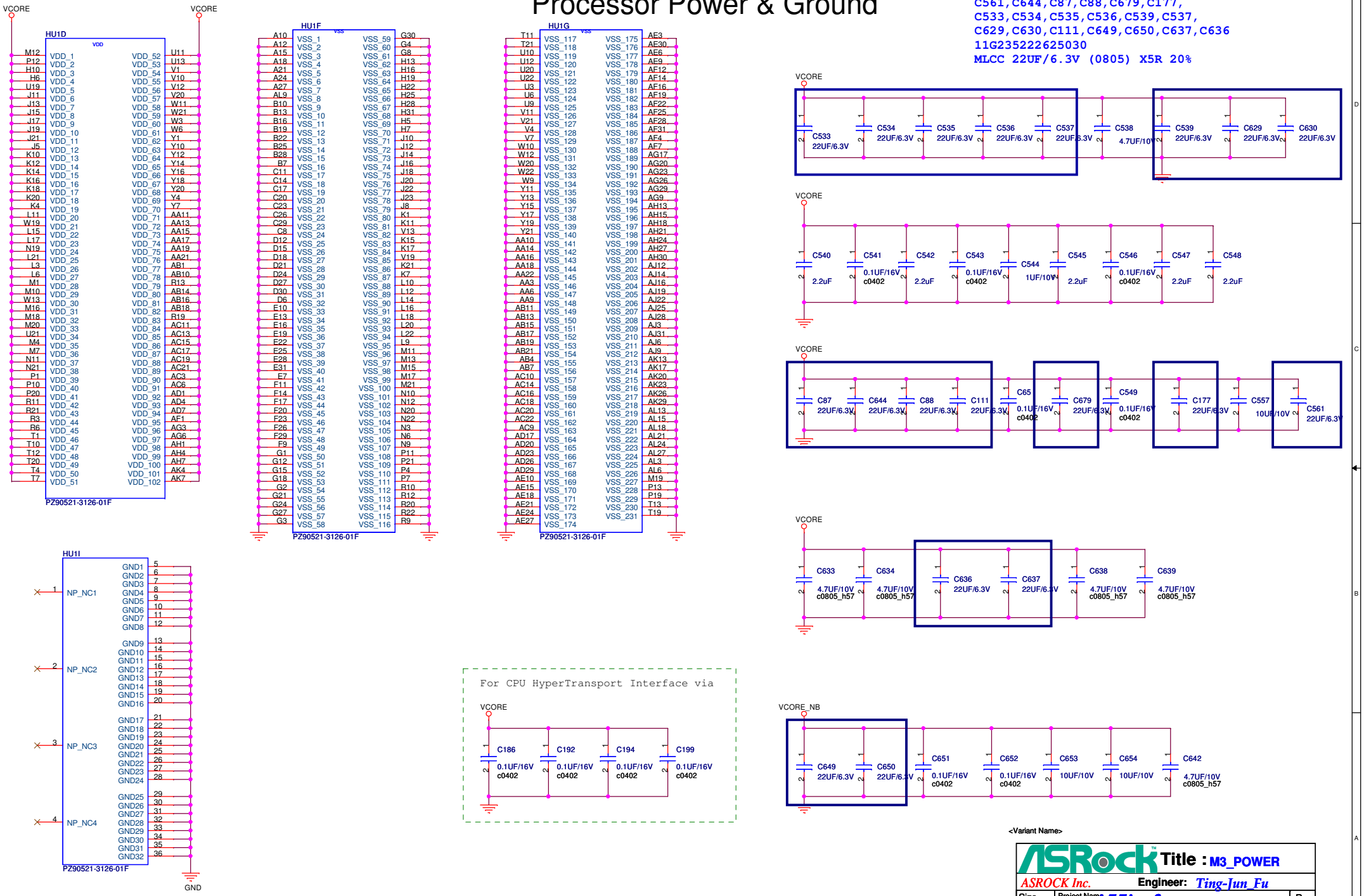
Date: Monday, July 25, 2011 Sheet 3 of 46

CPU Control & Debug Interfaces



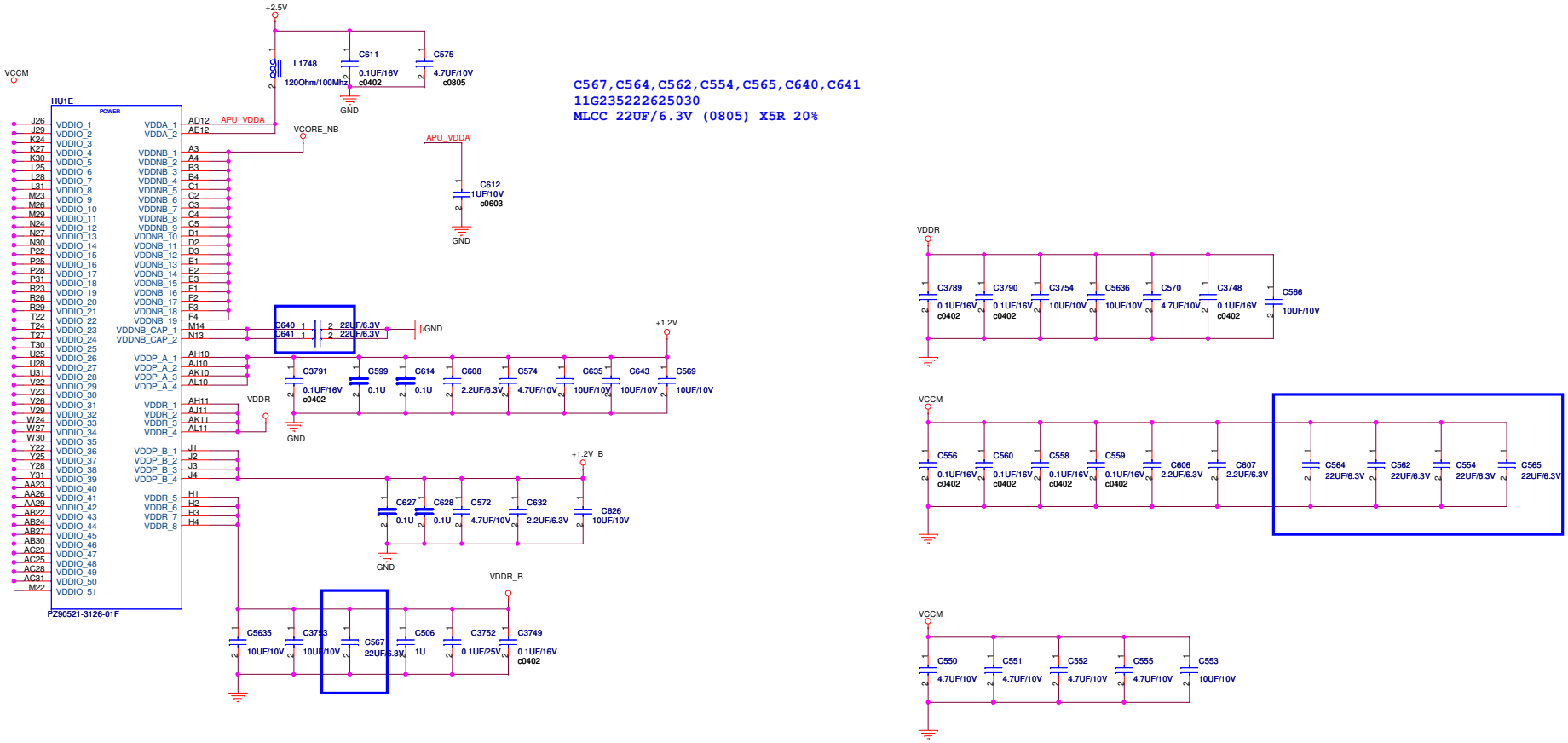
Processor Power & Ground

C561,C644,C87,C88,C679,C177,
C533,C534,C535,C536,C539,C537,
C629,C630,C111,C649,C650,C637,C636
11G235222625030
MLCC 22UF/6.3V (0805) X5R 20%



<Variant Name>

ASRock	Title : M3_POWER	
ASROCK Inc.	Engineer: Ting-Jun_Fu	
Size A3	Project Name A55icafe	Rev 1.01
Date: Monday, July 25, 2011	Sheet 5 of 46	



<Variant Name>

ASRock Inc.

Title : M3_GOUND

Engineer: Ting-Jun_Fu

Size	Project Name	Rev
Custom	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 6 of 46

DDR SLOT1

DDR SLOT3

PC4300	DDR533
PC5300	DDR667
PC6400	DDR800

DDR3_A1A — A0 — DDR3_A — DDR3_DIMM_240P

DDR3_A2A — A4 — DDR3_A — DDR3_DIMM_240P

MD[0:63] 3

CS#[0:3] 3
MA_CLK[0:3] 3
MA_CLK#[0:3] 3
MAA[0:15] 3
DQS[0:8] 3
DQS#[0:8] 3
DQM[0:8] 3
3 D3_ECC_A[0:7]

r0402_h16 R3501 1KOhm DDRSAPD

+3V r0402_h16 R3503 1KOhm DDRSAPU DDRSAPD

9 DDRSAPU
9 DDRSAPD

VTT_DDR

D3C3 1UF/10V c0603
D3C4 0.1UF/16V
D3C62 10UF/10V c0805_h57
D3C16 1UF/10V c0603
D3C17 0.1UF/16V

9,12,28,31 SMBCLK
9,12,28,31 SMBDATA

RESET# 168 RESET# 3

MA_EVENT_L 3

<Variant Name>

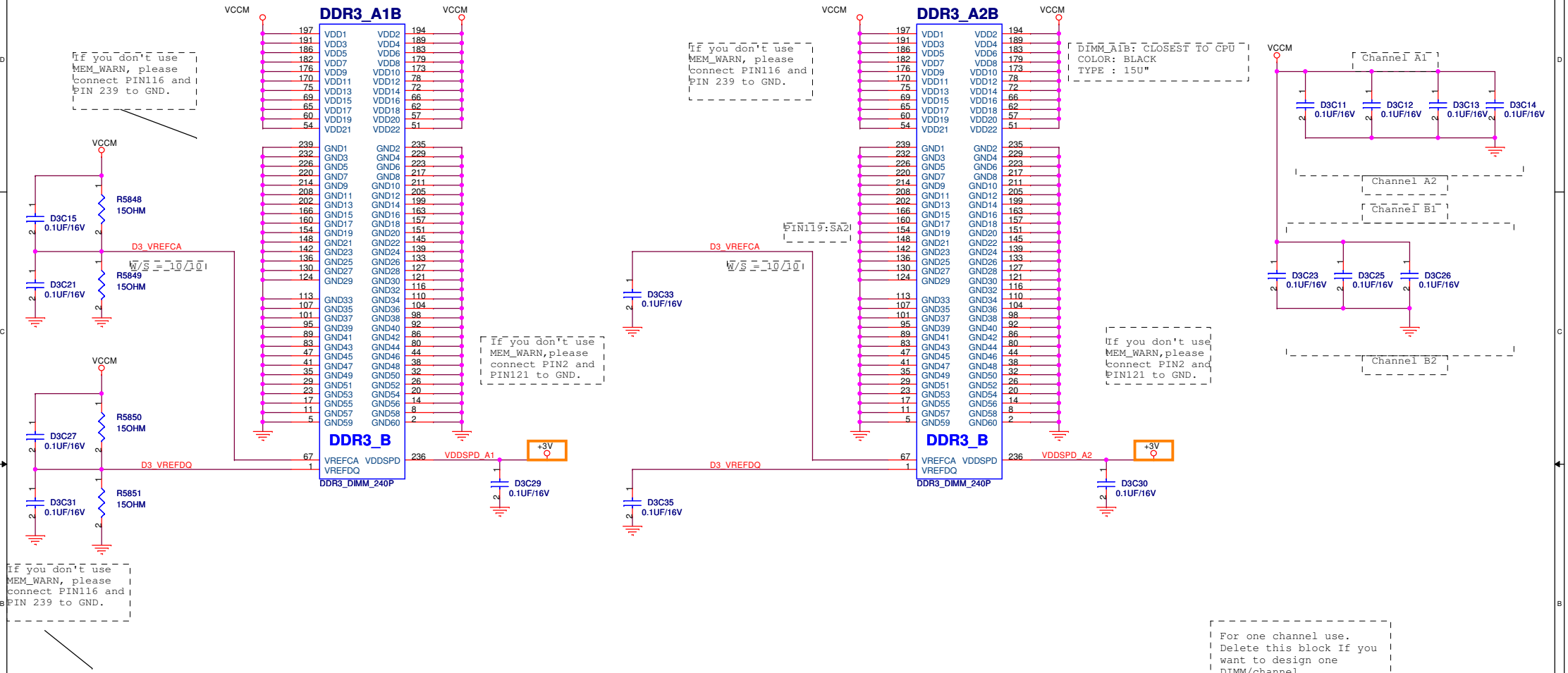
ASRock™ Title : DDRIII_DIMM1&3

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 7 of 46

10 D3_VREFDQ
10 D3_VREFCA



For one channel use.
Delete this block If you want to design one DIMM/channel.

With AMT	W/O AMT
+3V_CL	+3V
S0~S5有電	S0有電

<Variant Name>

ASRock™ Title : DDRIII_POWER_L0

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

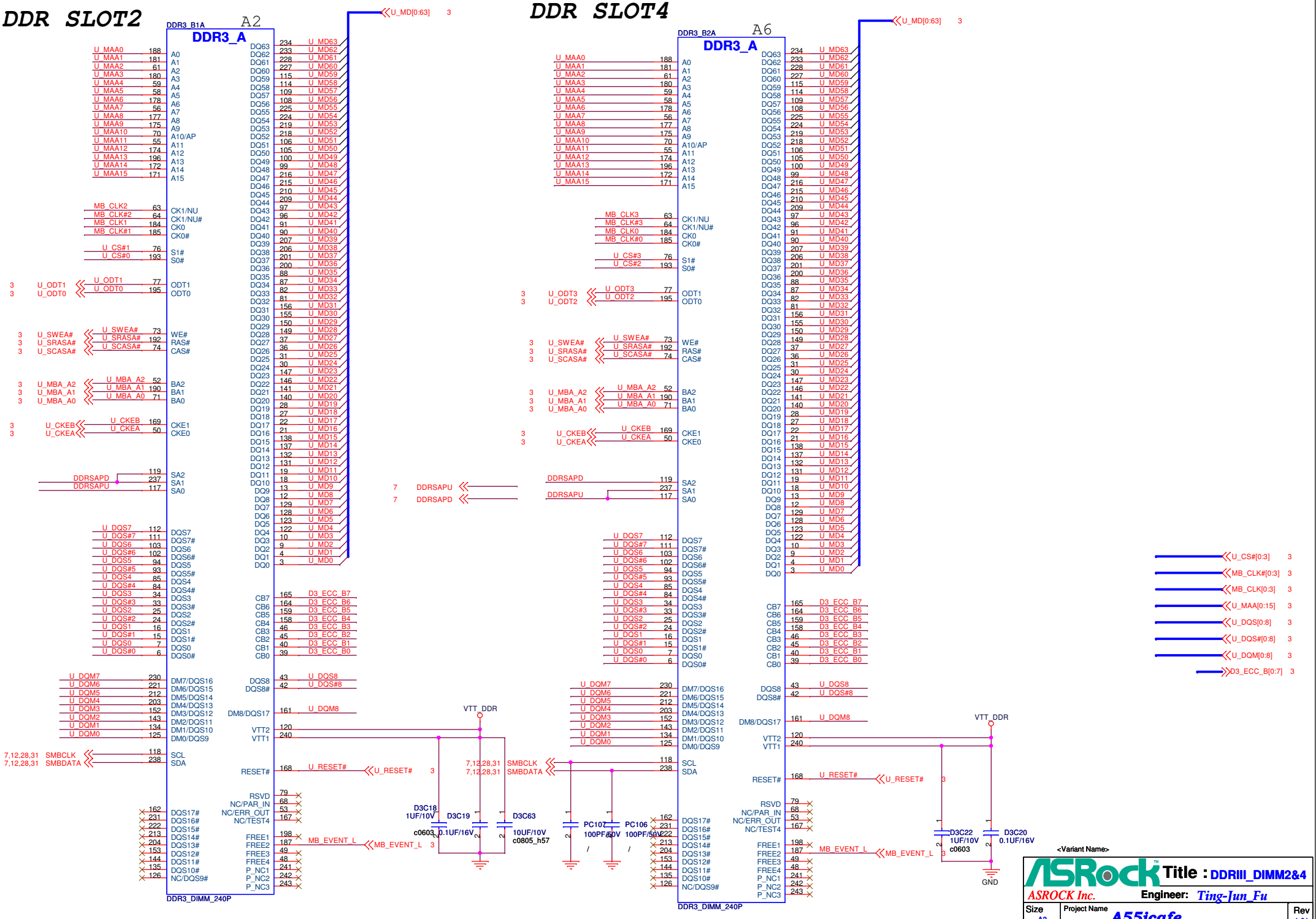
Date: Monday, July 25, 2011 Sheet 8 of 46

DDR SLOT2

DDR3_B1A — A2 — DDR3_A — DDR3_DIMM_240P

DDR SLOT4

DDR3_B2A — A6 — DDR3_A — DDR3_DIMM_240P



<Variant Name>

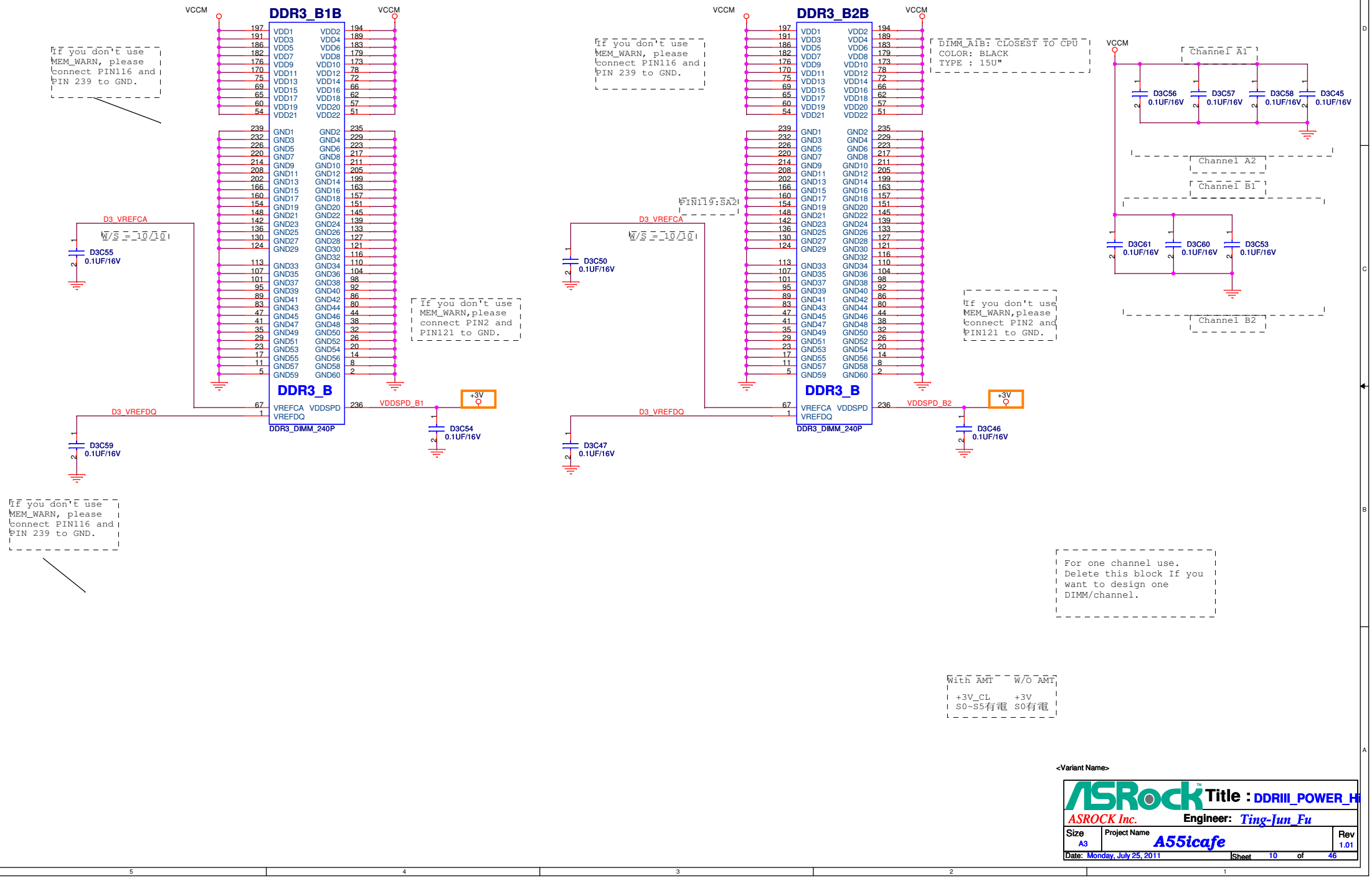
ASRock™ Title : DDRIII_DIMM2&4

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 9 of 46

8 D3_VREFDQ
8 D3_VREFCA



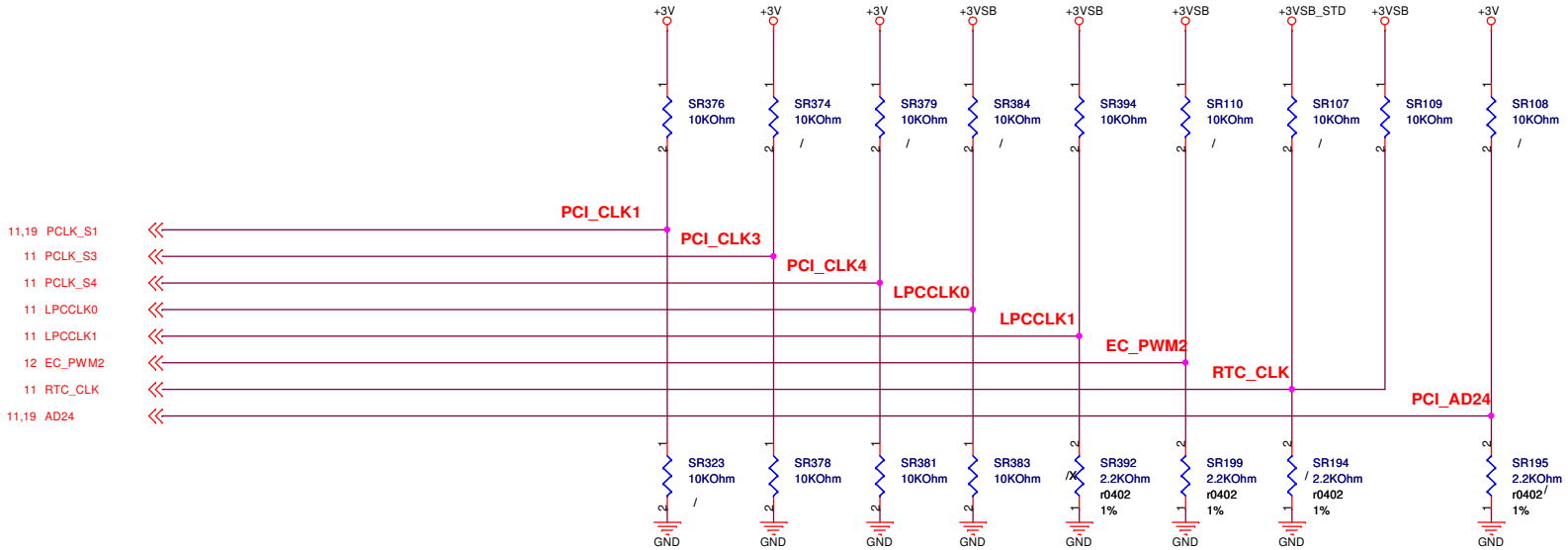
<Variant Name>

ASRock™ Title : DDRIII_POWER_HI

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 10 of 46



REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPCCLK0	LPCCLK1	RTC_CLK	EC_PWM2	PCI_AD24
PULL HIGH	Allow PCIe Gen2 DEFAULT	Enabled Debug straps	NON-FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED	S5+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM	Default PCIe straps
PULL LOW	Force PCIe Gen1	Disabled Debug straps DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	S5+ ENABLE	L = SPI ROM DEFAULT	EEPROM PCIe straps DEFAULT

<Variant Name>

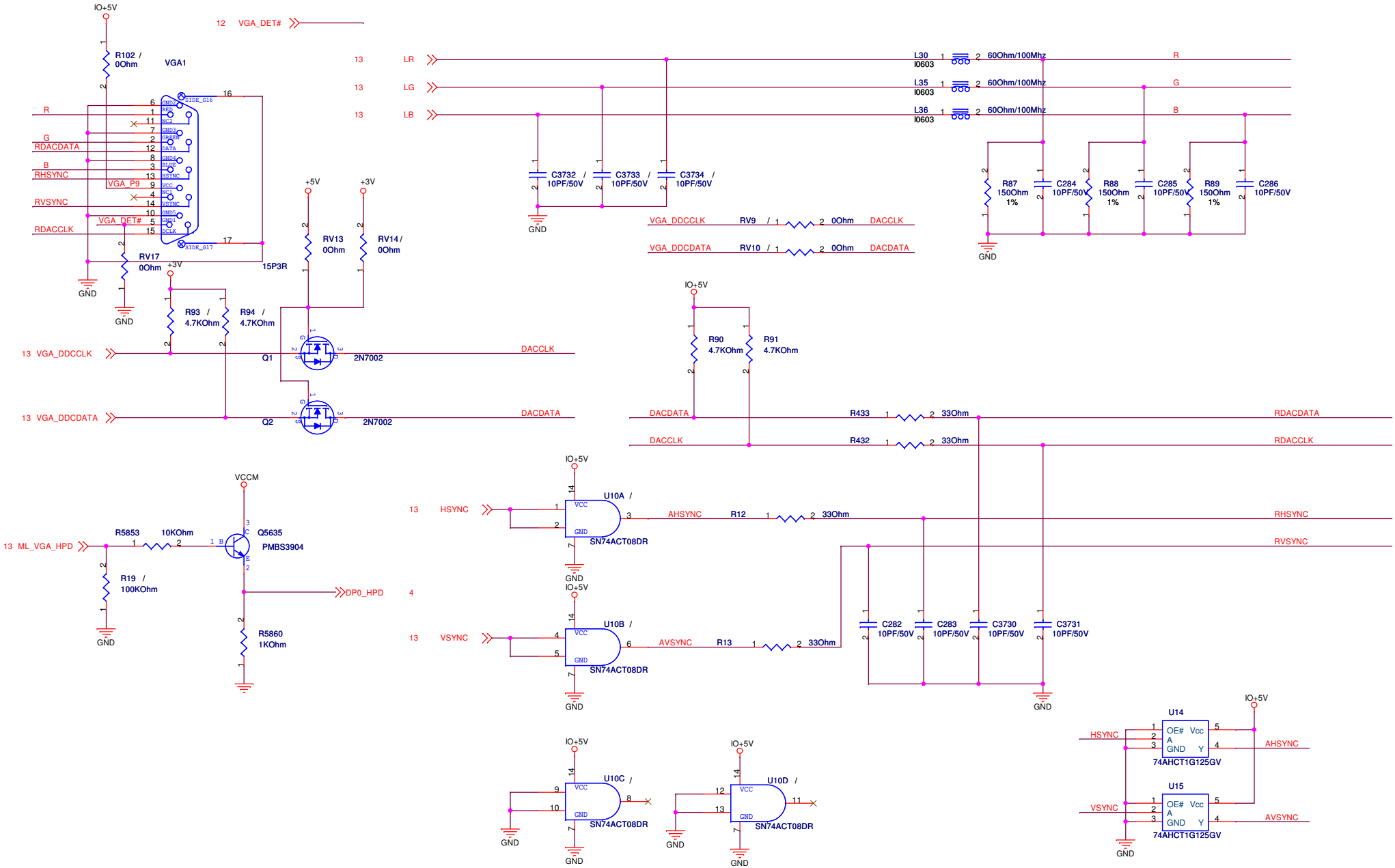
ASRock Title : H/W Setting

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 15 of 46

<variant_name>
A55iCafe
ASROCK Inc.
Title : CLOCK
Engineer: Ting-Jun_Fu
Size: A3
Project Name: A55iCafe
Rev: 1.01
Date: Monday, July 25, 2011
Sheet 16 of 46
</variant_name>



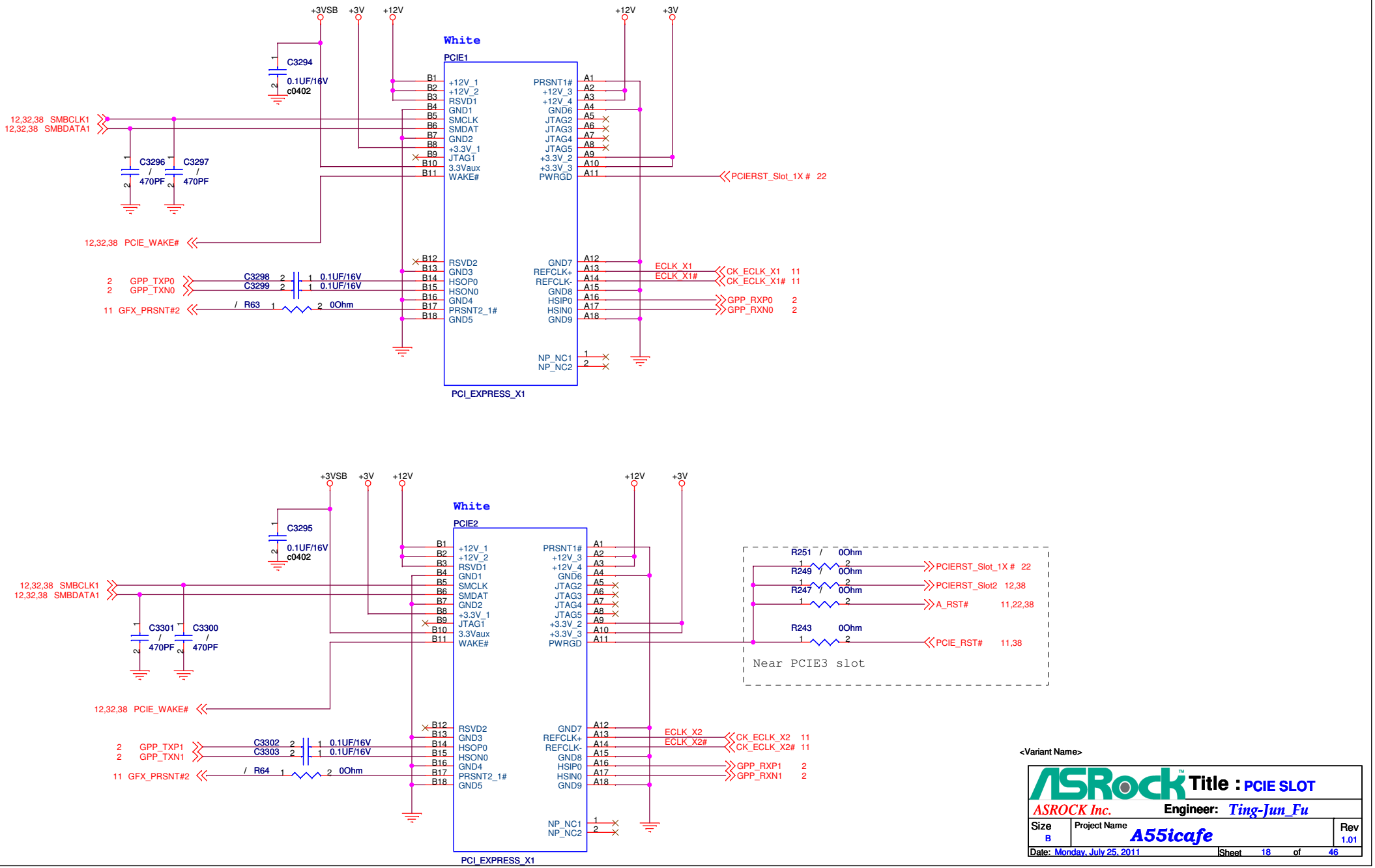
<Variant Name>

ASRock™ Title : ON_BORAD VGA

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 17 of 46



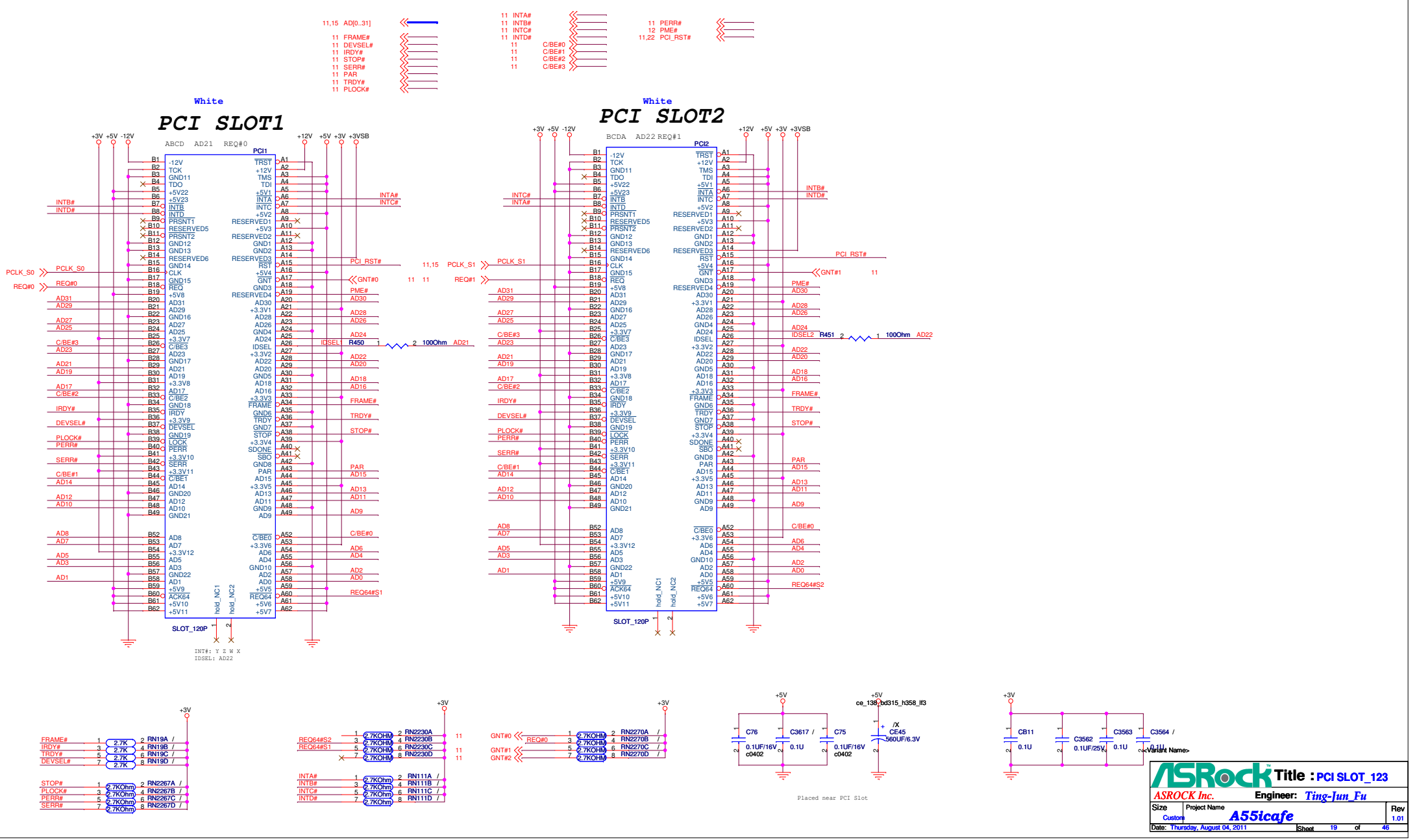
<Variant Name>

ASRock™ Title : PCIE SLOT

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
B	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 18 of 46


11,15 AD[0..31]
11 FRAME#
11 DEVSEL#
11 IRDY#
11 STOP#
11 SERR#
11 PAR
11 TRDY#
11 PLOCK#
11 INTA#
11 INTB#
11 INTC#
11 INTD#
11 C/BE#0
11 C/BE#1
11 C/BE#2
11 C/BE#3
11 PERR#
12 PME#
11,22 PCI_RST#
White
PCI SLOT1
ABCD AD21 REQ#0
PCI1
SLOT_120P
INT#: Y Z W X
IDSEL: AD22
White
PCI SLOT2
BCDA AD22 REQ#1
PCI2
SLOT_120P
R450 100Ohm
R451 100Ohm
RN19A / RN19B / RN19C / RN19D / 2.7K
RN2267A / RN2267B / RN2267C / RN2267D / 2.7KOhm
RN2230A / RN2230B / RN2230C / RN2230D / 2.7KOHM
RN111A / RN111B / RN111C / RN111D / 2.7KOhm
RN2270A / RN2270B / RN2270C / RN2270D / 2.7KOHM
C76 0.1UF/16V c0402
C3617 / 0.1U
C75 0.1UF/16V c0402
ce_138_bd315_h358_lf3
CE45 560UF/6.3V
CB11 0.1U
C3562 0.1UF/25V
C3563 0.1U
C3564 / 0.1U
<Variant Name>
Placed near PCI Slot
ASRock
Title : PCI SLOT_123
ASROCK Inc.
Engineer: Ting-Jun_Fu
Size: Custom
Project Name: A55icafe
Rev: 1.01
Date: Thursday, August 04, 2011
Sheet 19 of 46

3

ASRock Title : Etron USB3-1

ASRock Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55iCafe	1.01

Date: Monday, July 25, 2011 Sheet 20 of 46

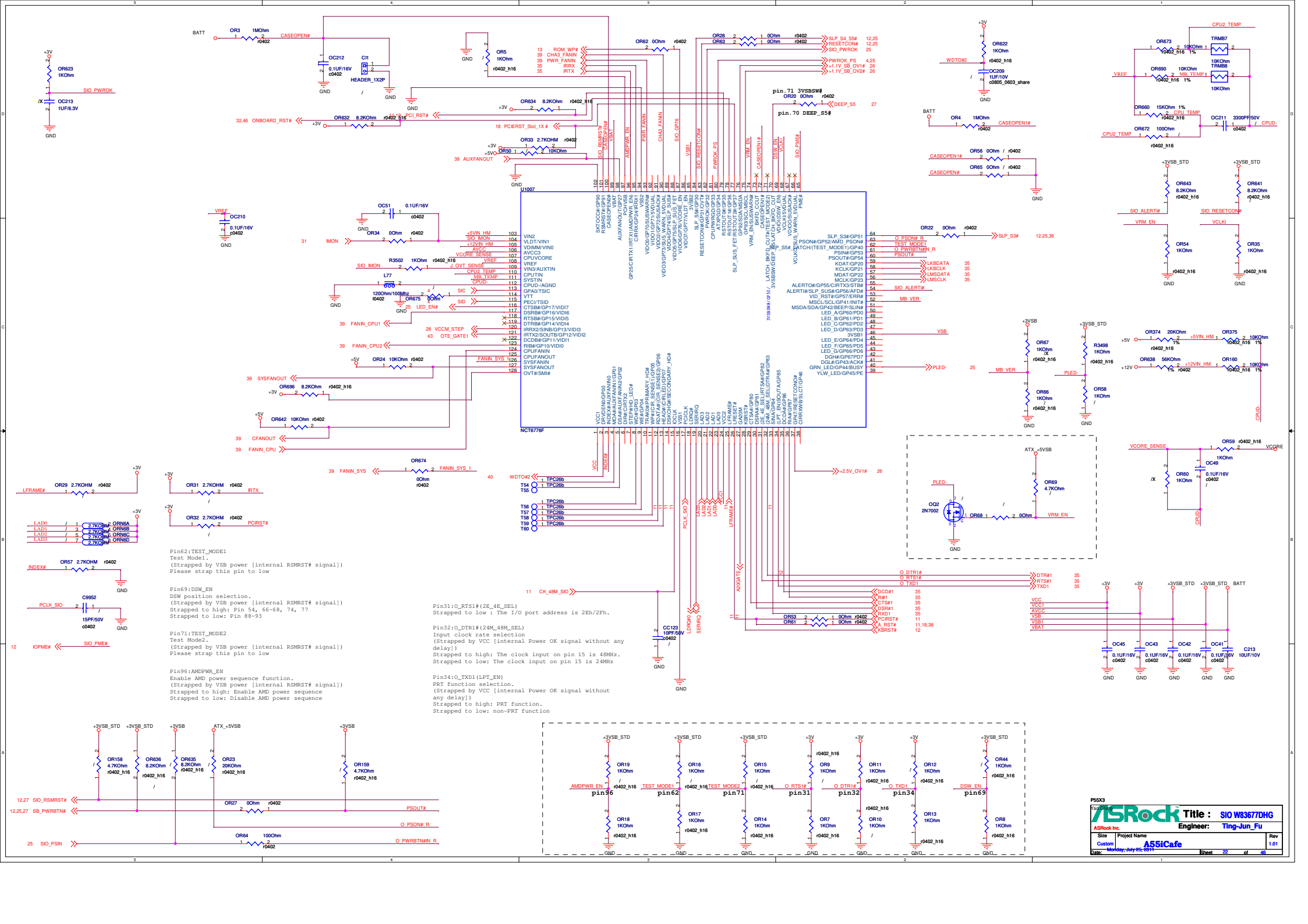
<Variant Name>

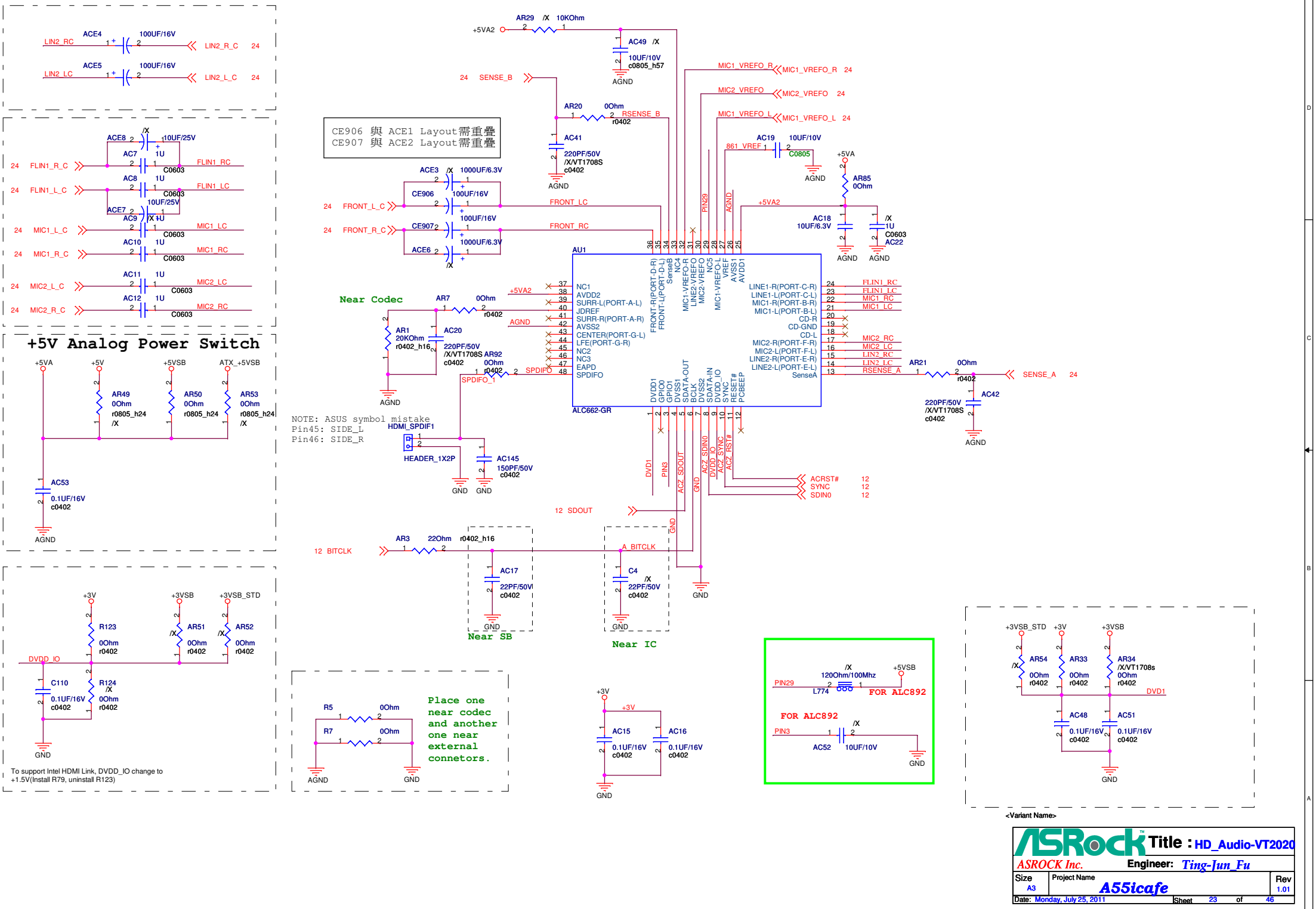
ASRock™ Title : USB_PORT

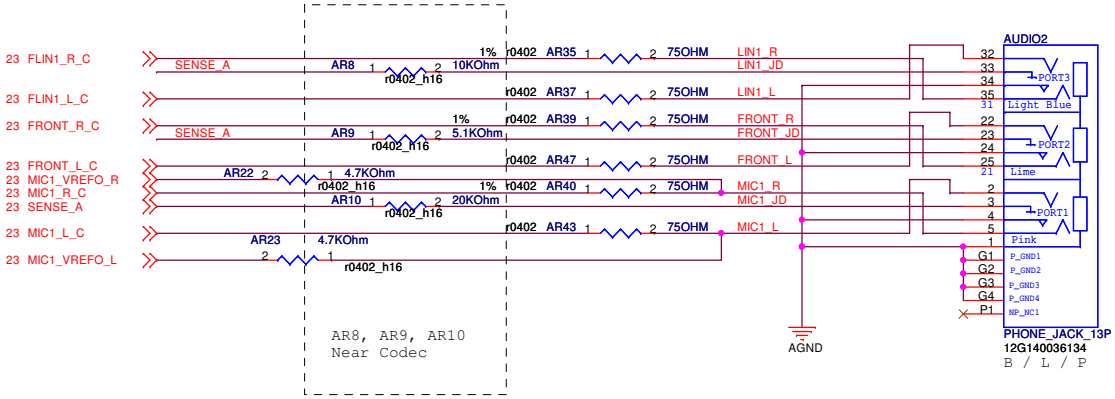
ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

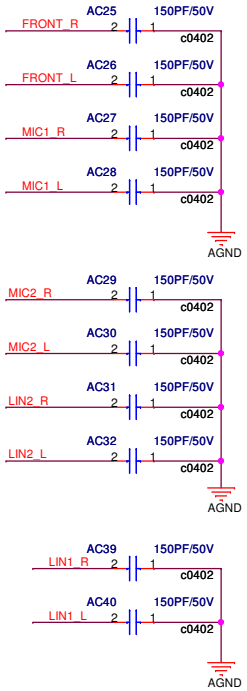
Date: Monday, July 25, 2011 Sheet 21 of 46

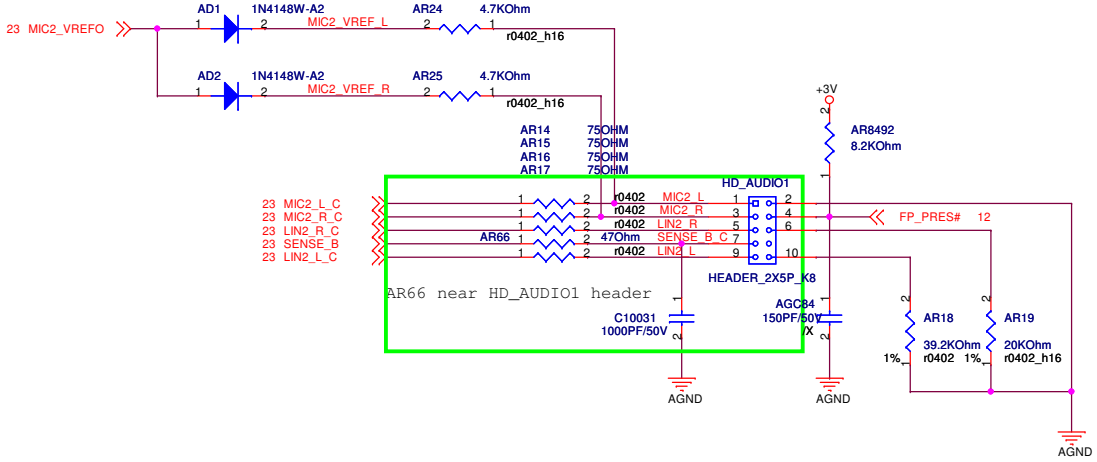

U1007
NCT6776F
Pin62:TEST_MODE1
Test Mode1.
(Strapped by VSB power [internal RSMRST# signal])
Please strap this pin to low
Pin69:DSW_EN
DSW position selection.
(Strapped by VSB power [internal RSMRST# signal])
Strapped to high: Pin 54, 66~68, 74, 77
Strapped to low: Pin 88~93
Pin71:TEST_MODE2
Test Mode2.
(Strapped by VSB power [internal RSMRST# signal])
Please strap this pin to low
Pin96:AMDPWR_EN
Enable AMD power sequence function.
(Strapped by VSB power [internal RSMRST# signal])
Strapped to high: Enable AMD power sequence
Strapped to low: Disable AMD power sequence
Pin31:O_RTS1#(2E_4E_SEL)
Strapped to low : The I/O port address is 2Eh/2Fh.
Pin32:O_DTR1#(24M_48M_SEL)
Input clock rate selection
(Strapped by VCC [internal Power OK signal without any delay])
Strapped to high: The clock input on pin 15 is 48MHz.
Strapped to low: The clock input on pin 15 is 24MHz
Pin34:O_TXD1(LPT_EN)
PRT function selection.
(Strapped by VCC [internal Power OK signal without any delay])
Strapped to high: PRT function.
Strapped to low: non-PRT function
P55X3
Title : SIO W83677DHG
Engineer: Ting-Jun_Fu
Project Name A55iCafe
Rev 1.01
Monday, July 25, 2011
Sheet 22 of 46


ACE4 100UF/16V LIN2_RC LIN2_R_C 24
ACE5 100UF/16V LIN2_LC LIN2_L_C 24
ACE8 /X 10UF/25V
AC7 1U C0603 FLIN1_RC
AC8 1U C0603 FLIN1_LC
ACE7 10UF/25V
AC9 /X 1U C0603 MIC1_LC
AC10 1U C0603 MIC1_RC
AC11 1U C0603 MIC2_LC
AC12 1U C0603 MIC2_RC
+5V Analog Power Switch
+5VA +5V +5VSB ATX_+5VSB
AR49 0Ohm r0805_h24 /X
AR50 0Ohm r0805_h24
AR53 0Ohm r0805_h24 /X
AC53 0.1UF/16V c0402
AGND
+3V +3VSB +3VSB_STD
R123 0Ohm r0402
AR51 /X 0Ohm r0402
AR52 /X 0Ohm r0402
DVDD_IO
C110 0.1UF/16V c0402
R124 /X 0Ohm r0402
GND
To support Intel HDMI Link, DVDD_IO change to +1.5V(Install R79, uninstall R123)
CE906 與 ACE1 Layout需重疊
CE907 與 ACE2 Layout需重疊
AR29 /X 10KOhm
+5VA2
AC49 /X 10UF/10V c0805_h57
AGND
24 SENSE_B
AR20 0Ohm RSENSE_B r0402
AC41 220PF/50V /X/VT1708S c0402
ACE3 /X 1000UF/6.3V
CE906 100UF/16V
24 FRONT_L_C
FRONT_LC
CE907 100UF/16V
24 FRONT_R_C
FRONT_RC
ACE6 1000UF/6.3V /X
MIC1_VREFO_R MIC1_VREFO_R 24
MIC2_VREFO MIC2_VREFO 24
MIC1_VREFO_L MIC1_VREFO_L 24
AC19 10UF/10V
861_VREF C0805
AR85 0Ohm
AC18 10UF/6.3V
/X 1U C0603 AC22
Near Codec
AR7 0Ohm r0402
AR1 20KOhm r0402_h16
AC20 220PF/50V /X/VT1708S c0402
AR92 0Ohm r0402
SPDIFO
SPDIFO_1
AU1
NC1 AVDD2 SURR-L(PORT-A-L) JDREF SURR-R(PORT-A-R) AVSS2 CENTER(PORT-G-L) LFE(PORT-G-R) NC2 NC3 EAPD SPDIFO
FRONT-R(PORT-D-R) FRONT-L(PORT-D-L) SenseB NC4 MIC1-VREFO-R LINE2-VREFO MIC2-VREFO NC5 MIC1-VREFO-L VREF AVSS1 AVDD1
LINE1-R(PORT-C-R) LINE1-L(PORT-C-L) MIC1-R(PORT-B-R) MIC1-L(PORT-B-L) CD-R CD-GND CD-L MIC2-R(PORT-F-R) MIC2-L(PORT-F-L) LINE2-R(PORT-E-R) LINE2-L(PORT-E-L) SenseA
DVDD1 GPIO0 GPIO1 DVSS1 SDATA-OUT BCLK DVSS2 SDATA-IN DVDD_IO SYNC RESET# PCBEEP
ALC662-GR
FLIN1_RC FLIN1_LC MIC1_RC MIC1_LC MIC2_RC MIC2_LC LIN2_RC LIN2_LC RSENSE_A
AR21 0Ohm r0402
SENSE_A 24
AC42 220PF/50V /X/VT1708S c0402
NOTE: ASUS symbol mistake
Pin45: SIDE_L
Pin46: SIDE_R
HDMI_SPDIF1
HEADER_1X2P
AC145 150PF/50V c0402
ACRST# 12
SYNC 12
SDIN0 12
12 SDOUT
12 BITCLK
AR3 22Ohm r0402_h16
A_BITCLK
AC17 22PF/50V c0402
C4 /X 22PF/50V c0402
Near SB
Near IC
R5 0Ohm
R7 0Ohm
Place one near codec and another one near external connetors.
AC15 0.1UF/16V c0402
AC16 0.1UF/16V c0402
/X 120Ohm/100Mhz
L774
FOR ALC892
AC52 10UF/10V
AR54 /X 0Ohm r0402
AR33 0Ohm r0402
AR34 /X/VT1708s 0Ohm r0402
DVD1
AC48 0.1UF/16V c0402
AC51 0.1UF/16V c0402
<Variant Name>
ASRock
ASROCK Inc.
Title : HD_Audio-VT2020
Engineer: Ting-Jun_Fu
Size A3
Project Name A55icafe
Rev 1.01
Date: Monday, July 25, 2011
Sheet 23 of 46



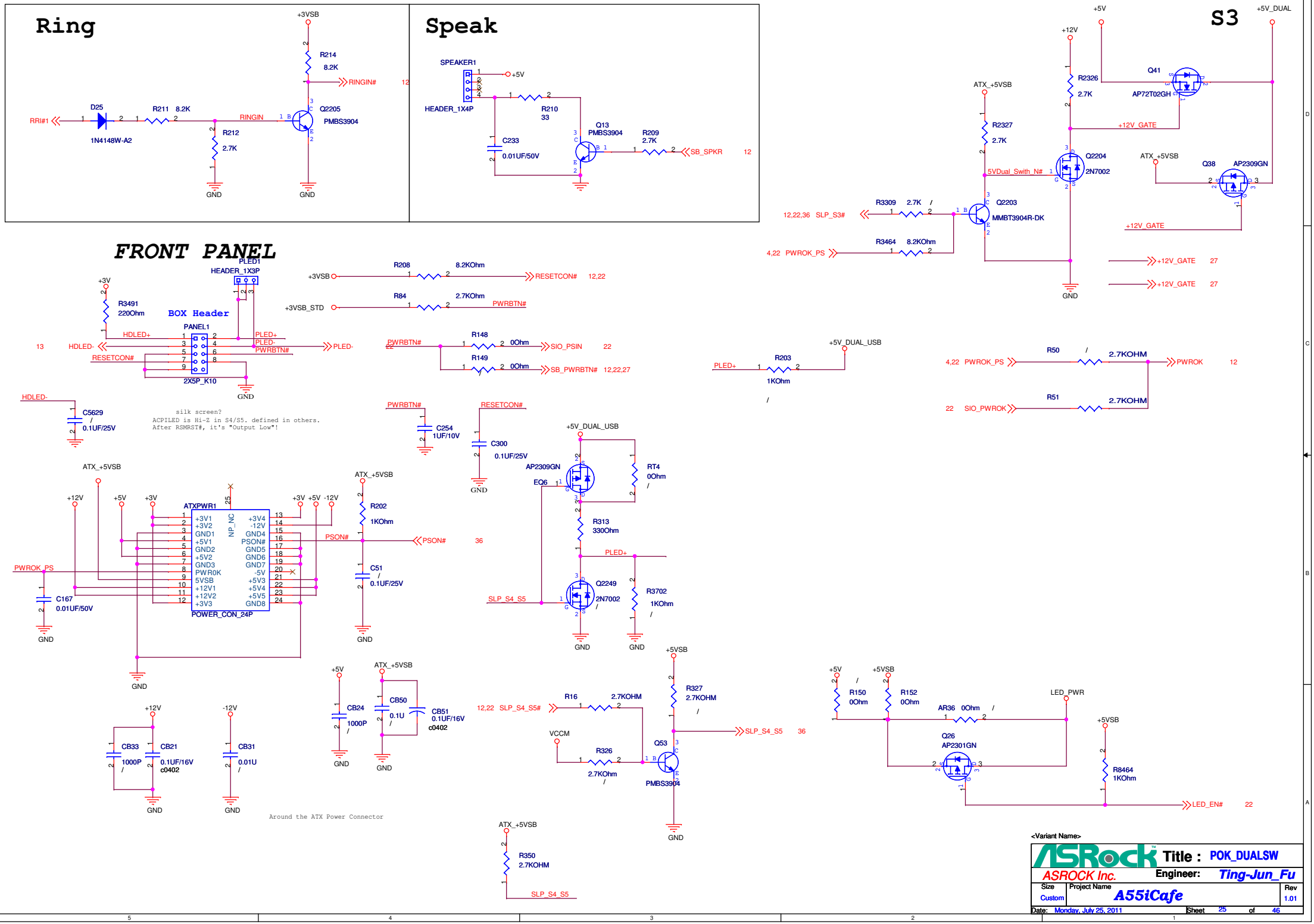
For EMI

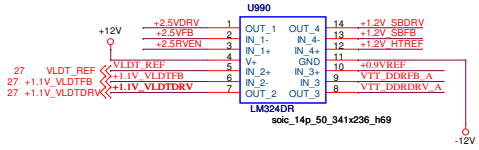


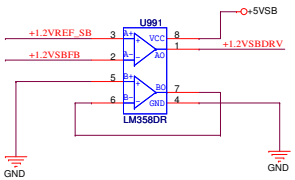


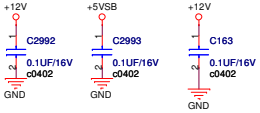
<Variant Name>

ASRock	Title : AudioConn	
ASROCK Inc.	Engineer: Ting-Jun_Fu	
Size A3	Project Name A55icafe	Rev 1.01
Date: Monday, July 25, 2011	Sheet 24 of 46	

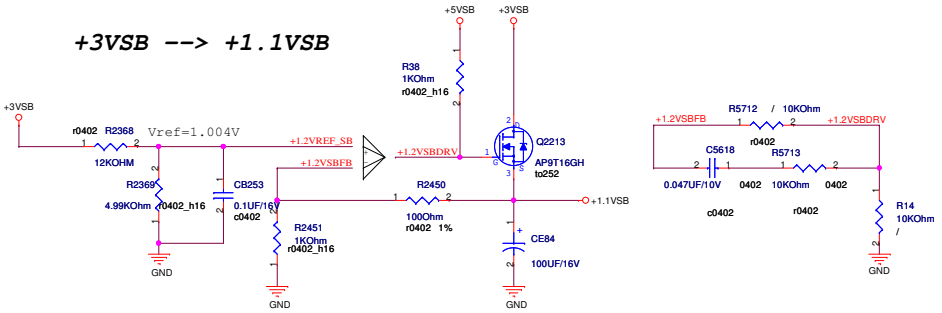

Ring
Speak
S3
FRONT PANEL
Around the ATX Power Connector
silk screen?
ACPILED is Hi-Z in S4/S5. defined in others.
After RSMRST#, it's "Output Low"!
<Variant Name>
ASRock
ASROCK Inc.
Title : POK_DUALSW
Engineer: Ting-Jun_Fu
Size Custom
Project Name A55tCafe
Rev 1.01
Date: Monday, July 25, 2011
Sheet 25 of 46



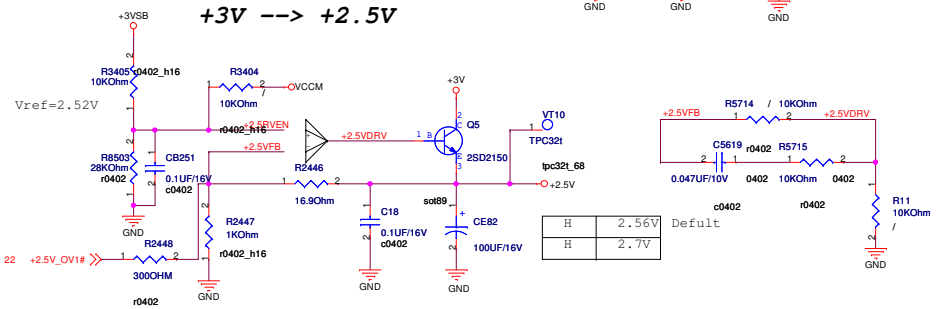




+3VSB --> +1.1VSB



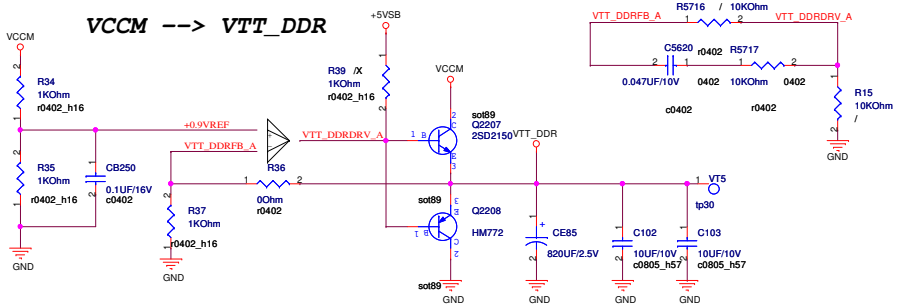
+3V --> +2.5V



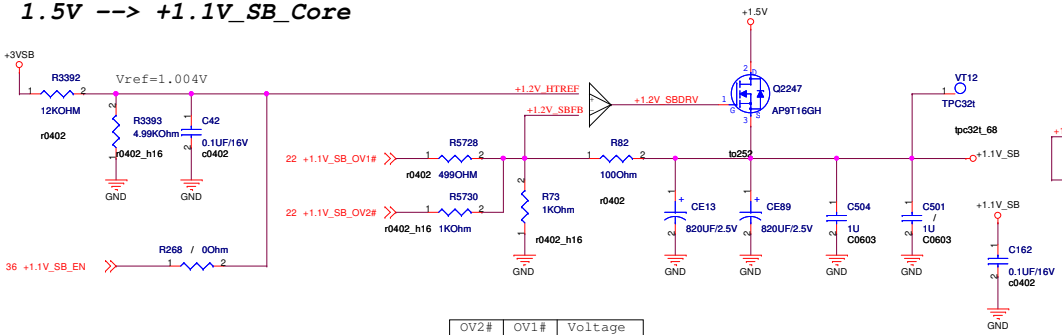
H	2.56V
H	2.7V

Default

VCCM --> VTT_DDR



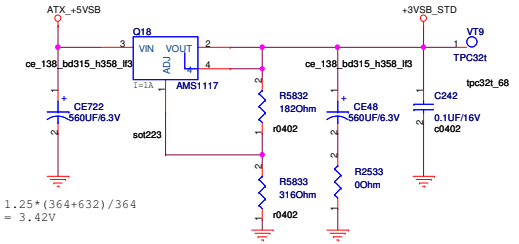
1.5V --> +1.1V_SB_Core



OV2#	OV1#	Voltage
H	H	1.1
L	H	1.2
H	L	1.3
L	L	1.4

Default

+5VSB --> +3VSB



<Variant Name>

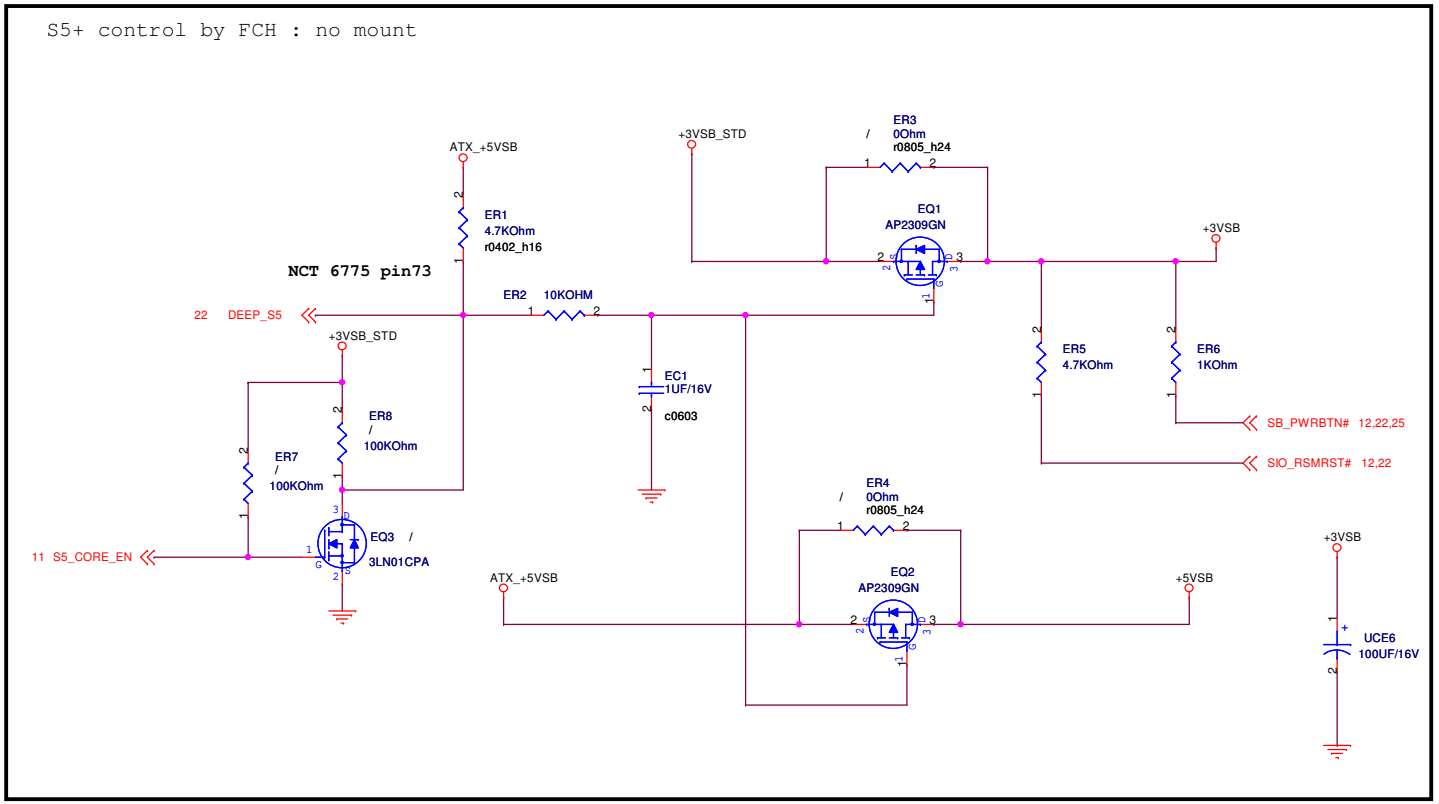
ASRock Title : SYSPWR

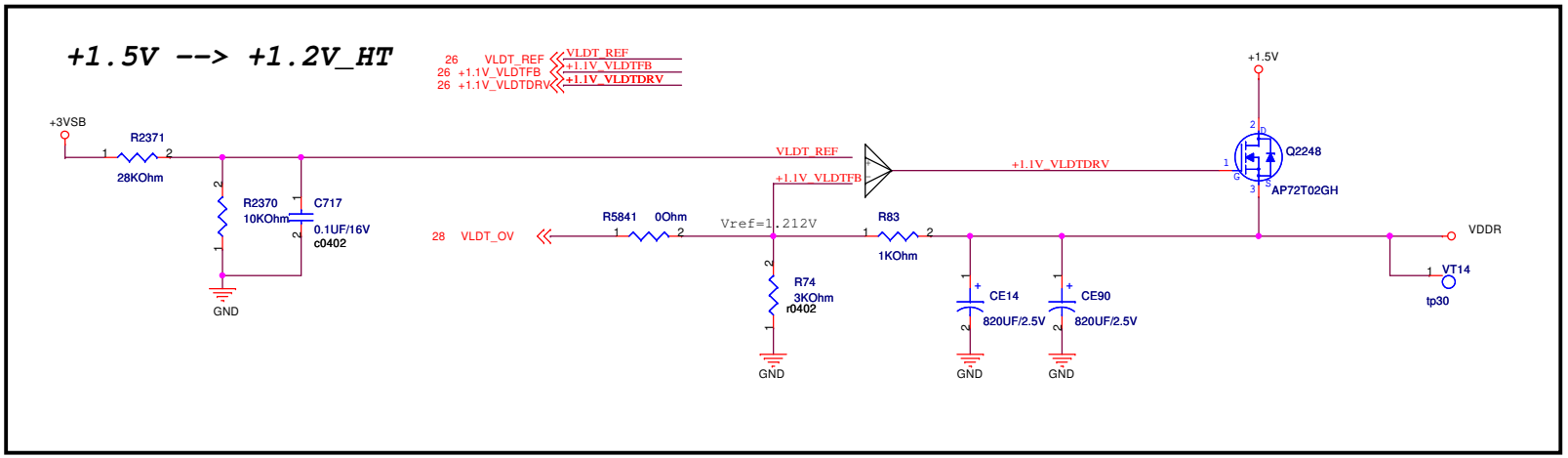
ASROCK Inc. Engineer: Ting-Jun_Fu

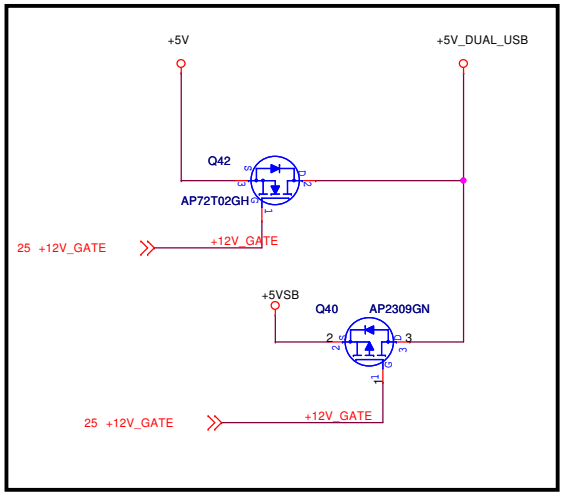
Size	Project Name	Rev
Custom	A55icafe	1.01

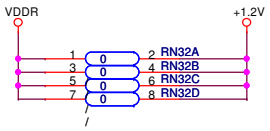
Date: Thursday, August 04, 2011 Sheet 26 of 46

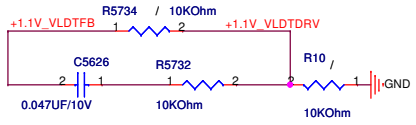
S5+ control by FCH : no mount











OV2#	OV1#	Voltage
H	H	1.102
H	L	1.194
L	H	1.313
L	L	1.404

Default

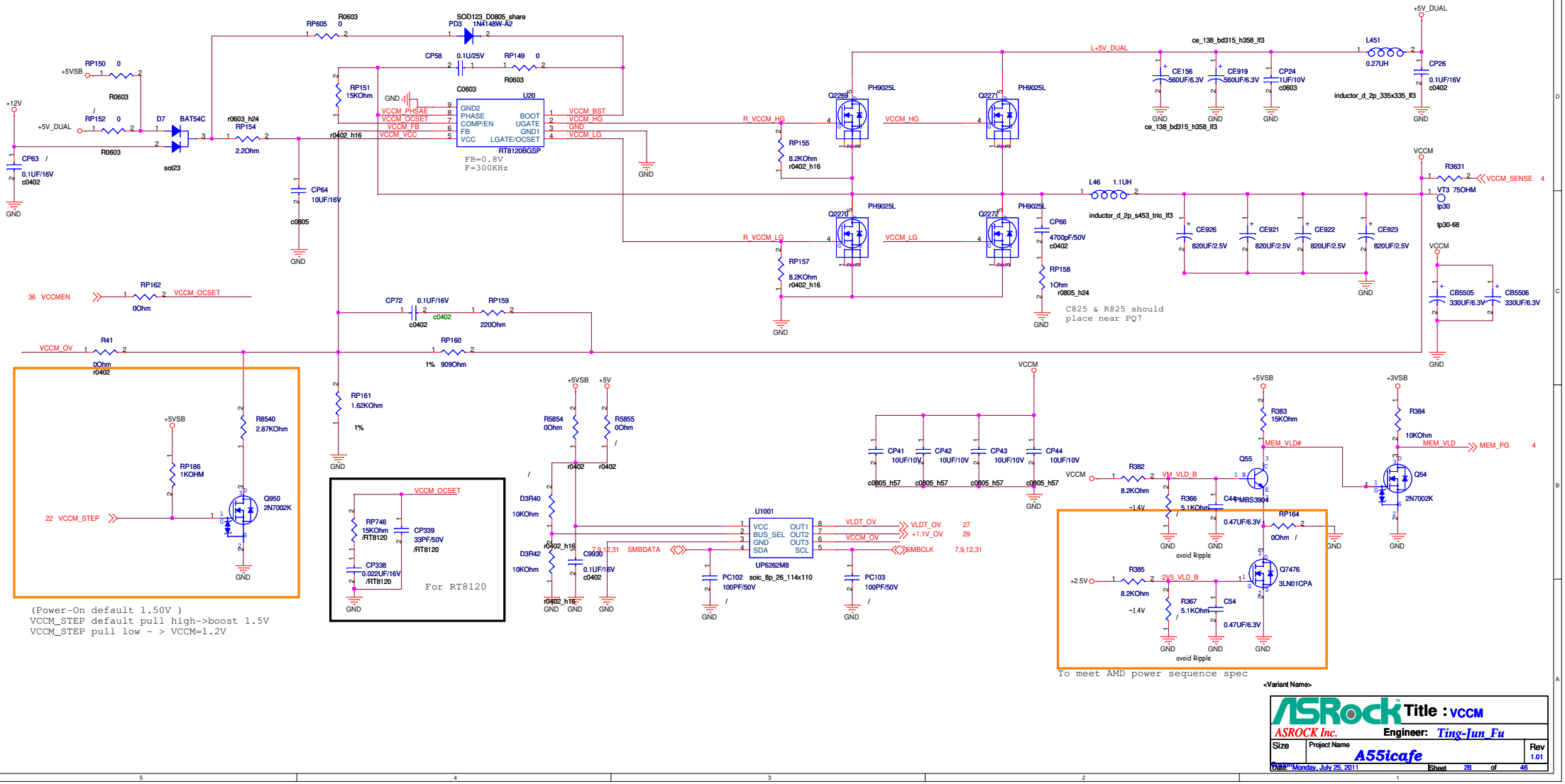
<Variant Name>

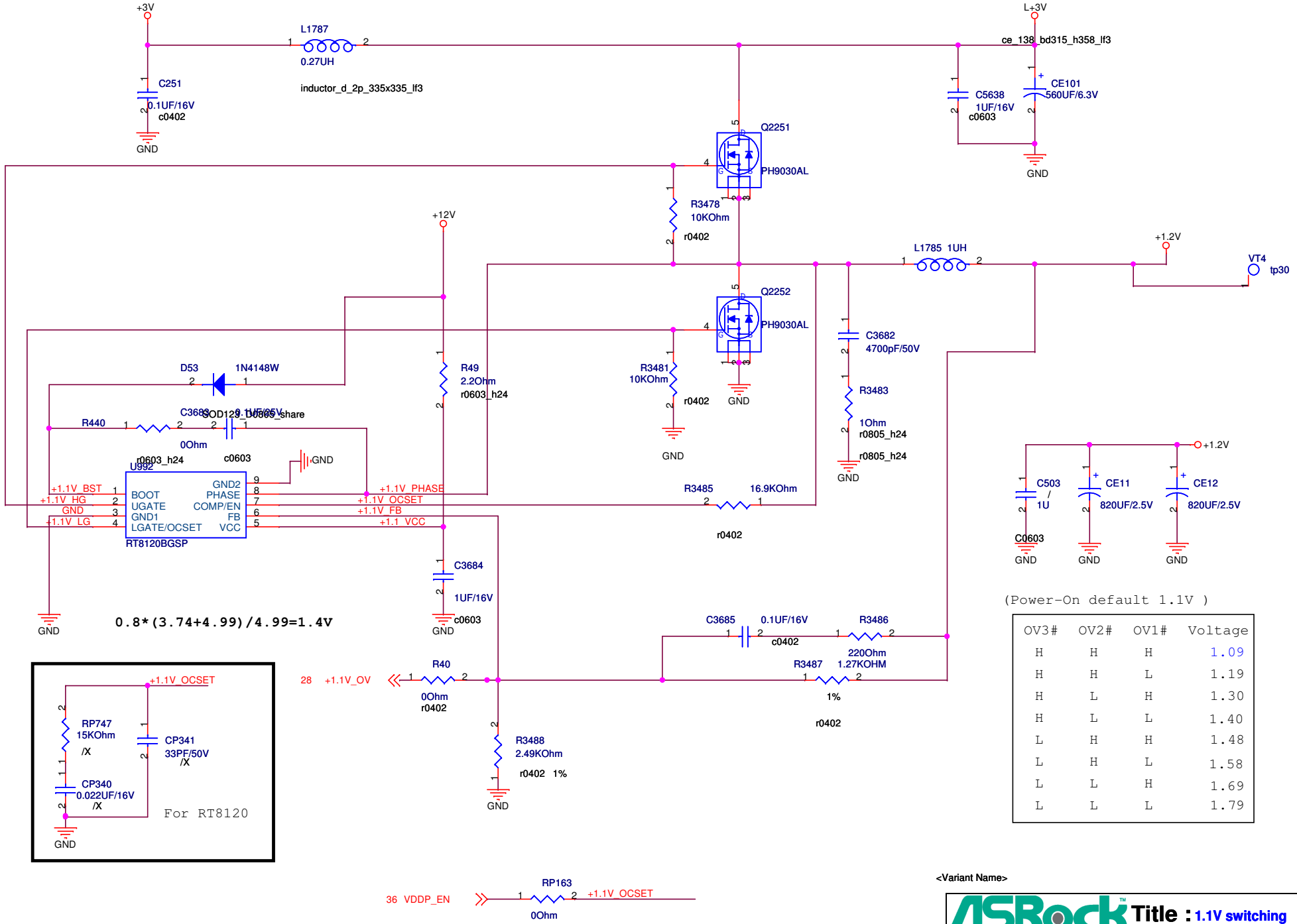
ASRock™ Title : USB3.0 Power

ASROCK Inc. Engineer: Ting-Jun_Fu

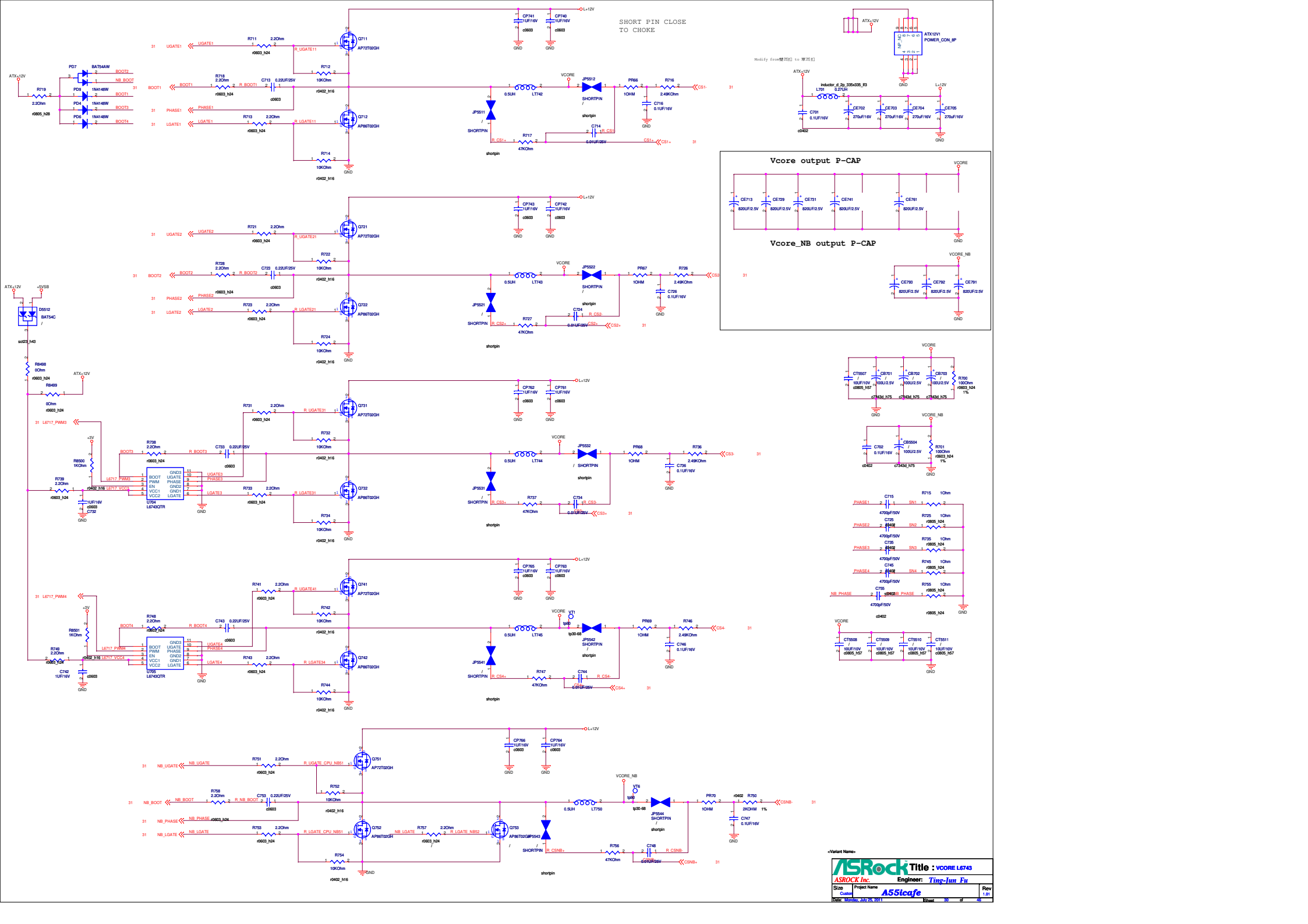
Size	Project Name	Rev
A3	A55icafe	1.01

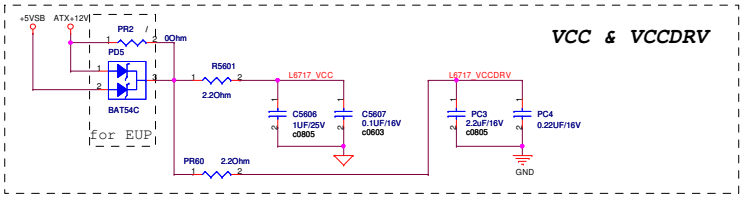
Date: Monday, July 25, 2011 Sheet 27 of 46

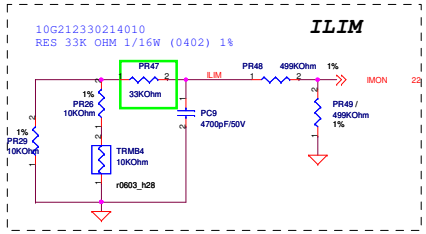

RP605 0 R0603
SOD123_D0805_share
PD3 1N4148W-A2
CP58 0.1U/25V
RP149 0 R0603
RP150 0 R0603
+5VSB
RP152 0 R0603
+5V_DUAL
D7 BAT54C sot23
r0603_h24
RP154 2.2Ohm
RP151 15KOhm
r0402_h16
+12V
CP63 0.1UF/16V c0402
CP64 10UF/16V c0805
C0603
U20
GND2
PHASE
COMP/EN
FB
VCC
BOOT
UGATE
GND1
LGATE/OCSET
RT8120BGSP
VCCM_PHSAE
VCCM_OCSET
VCCM_FB
VCCM_VCC
VCCM_BST
VCCM_HG
GND
VCCM_LG
FB=0.8V
F=300KHz
R_VCCM_HG
RP155 8.2KOhm r0402_h16
Q2269 PH9025L
Q2271 PH9025L
VCCM_HG
L+5V_DUAL
ce_138_bd315_h358_lf3
CE156 560UF/6.3V
CE919 560UF/6.3V
CP24 1UF/10V c0603
L451 0.27UH
inductor_d_2p_335x335_lf3
+5V_DUAL
CP26 0.1UF/16V c0402
R_VCCM_LG
RP157 8.2KOhm r0402_h16
Q2270 PH9025L
Q2272 PH9025L
VCCM_LG
L46 1.1UH
inductor_d_2p_s453_trio_lf3
CP66 4700pF/50V c0402
RP158 1Ohm r0805_h24
C825 & R825 should place near PQ7
CE926 820UF/2.5V
CE921 820UF/2.5V
CE922 820UF/2.5V
CE923 820UF/2.5V
VCCM
R3631
VCCM_SENSE 4
VT3 75OHM
tp30
tp30-68
CB5505 330UF/6.3V
CB5506 330UF/6.3V
36 VCCMEN
RP162 0Ohm
VCCM_OCSET
CP72 0.1UF/16V c0402
RP159 220Ohm
RP160 1% 909Ohm
VCCM_OV
R41 0Ohm r0402
RP161 1.62KOhm 1%
R8540 2.87KOhm
RP186 1KOHM
22 VCCM_STEP
Q950 2N7002K
(Power-On default 1.50V)
VCCM_STEP default pull high->boost 1.5V
VCCM_STEP pull low - > VCCM=1.2V
VCCM_OCSET
RP746 15KOhm /RT8120
CP339 33PF/50V /RT8120
CP338 0.022UF/16V /RT8120
For RT8120
R5854 0Ohm
R5855 0Ohm
D3R40 10KOhm
D3R42 10KOhm
C9930 0.1UF/16V c0402
SMBDATA 7,9,12,31
U1001
VCC
BUS_SEL
GND
SDA
OUT1
OUT2
OUT3
SCL
UP6262M8
VLDT_OV
+1.1V_OV
VCCM_OV
SMBCLK 7,9,12,31
VLDT_OV 27
29
PC102 soic_8p_26_114x110 100PF/50V
PC103 100PF/50V
CP41 10UF/10V c0805_h57
CP42 10UF/10V c0805_h57
CP43 10UF/10V c0805_h57
CP44 10UF/10V c0805_h57
R382 8.2KOhm ~1.4V
VM_VLD_B
R366 5.1KOhm
C44 0.47UF/6.3V
avoid Ripple
Q55 PMBS3904
R383 15KOhm
MEM_VLD#
RP164 0Ohm
R384 10KOhm
MEM_VLD
MEM_PG 4
Q54 2N7002K
+2.5V
R385 8.2KOhm ~1.4V
2V5_VLD_B
R367 5.1KOhm
C54 0.47UF/6.3V
Q7476 3LN01CPA
To meet AMD power sequence spec
<Variant Name>
ASRock
Title : VCCM
ASROCK Inc.
Engineer: Ting-Jun_Fu
Size
Project Name
A55icafe
Rev 1.01
Date: Monday, July 25, 2011
Sheet 28 of 46

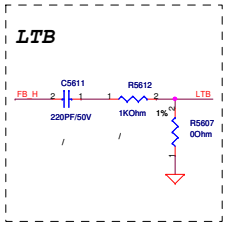


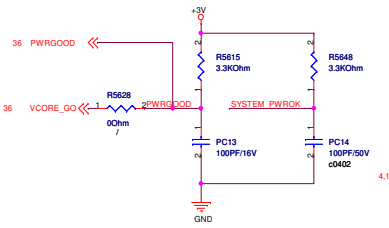
OV3#	OV2#	OV1#	Voltage
H	H	H	1.09
H	H	L	1.19
H	L	H	1.30
H	L	L	1.40
L	H	H	1.48
L	H	L	1.58
L	L	H	1.69
L	L	L	1.79

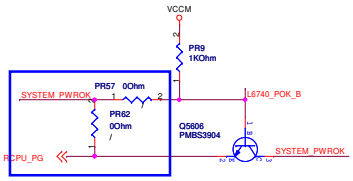

SHORT PIN CLOSE TO CHOKE
Vcore output P-CAP
Vcore_NB output P-CAP
Modify from單顆 to 單顆
ATX12V1 POWER_CON_8P
Q711
Q712
Q721
Q722
Q731
Q732
Q741
Q742
Q751
Q752
Q753
U704 L6743QTR
U705 L6743QTR
LT742
LT743
LT744
LT745
LT750
JP5512 SHORTPIN
JP5522 SHORTPIN
JP5532 SHORTPIN
JP5542 SHORTPIN
JP5544 SHORTPIN
JP5511 SHORTPIN
JP5521 SHORTPIN
JP5531 SHORTPIN
JP5541 SHORTPIN
shortpin
Title : VCORE L6743
ASROCK Inc.
Engineer: Ting-Jun Fu
A55icafe
Date: Monday, July 25, 2011

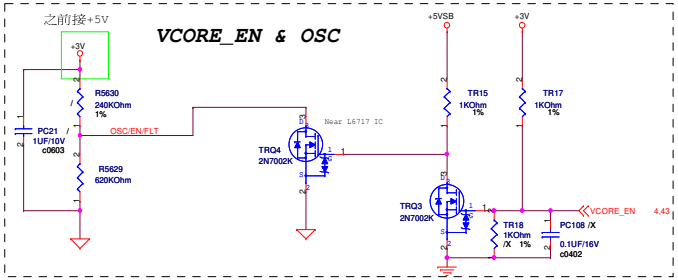

VCC & VCCDRV
+5VSB
ATX+12V
PR2
0Ohm
PD5
BAT54C
for EUP
R5601
2.2Ohm
L6717_VCC
C5606
1UF/25V
c0805
C5607
0.1UF/16V
c0603
L6717_VCCDRV
PC3
2.2uF/16V
c0805
PC4
0.22UF/16V
PR60
2.2Ohm
GND

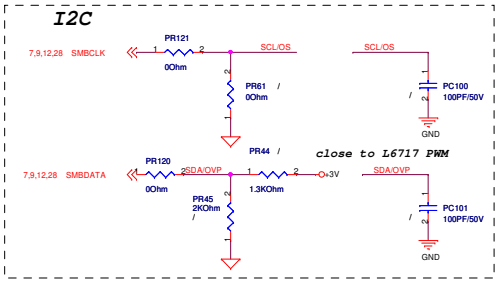

ILIM
10G212330214010
RES 33K OHM 1/16W (0402) 1%
PR47
33KOhm
ILIM
PR48
499KOhm
1%
IMON
22
PR26
10KOhm
PR29
10KOhm
TRMB4
10KOhm
r0603_h28
PC9
4700pF/50V
PR49 /
499KOhm
1%

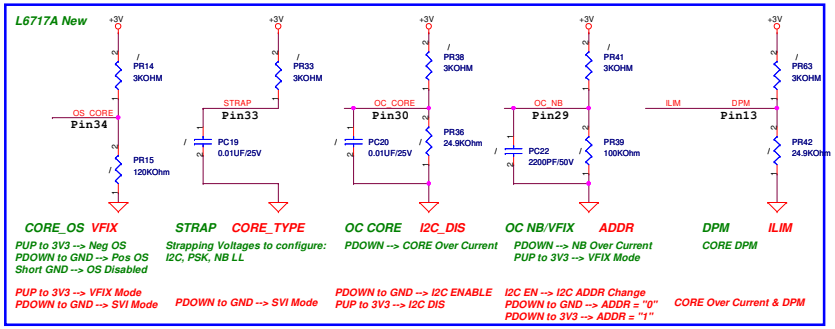

LTB
C5611
220PF/50V
R5612
1KOhm
1%
LTB
R5607
0Ohm
FB_H

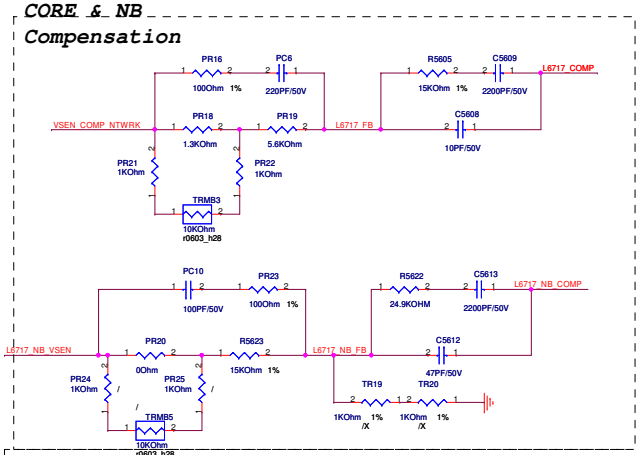

PGOOD & PWROK
+3V
36 PWRGOOD
36 VCORE_GO
R5628
0Ohm
PWRGOOD
R5615
3.3KOhm
R5648
3.3KOhm
SYSTEM_PWROK
PC13
100PF/16V
PC14
100PF/50V
c0402
GND

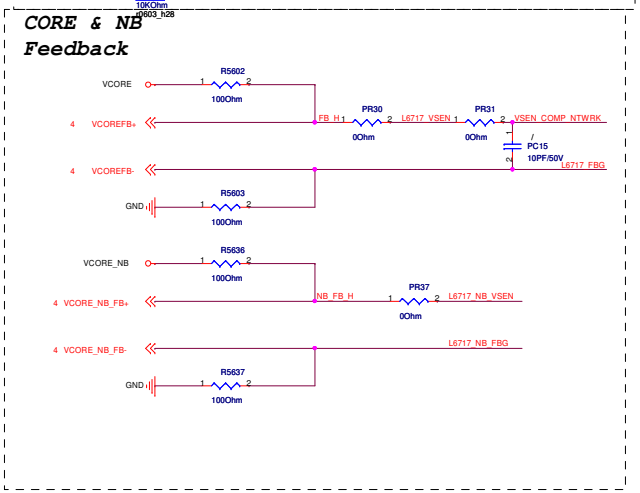

VCCM
PR9
1KOhm
SYSTEM_PWROK
PR57
0Ohm
PR62
0Ohm
L6740_POK_B
Q5606
PMBS3904
4,11 RCPU_PG
SYSTEM_PWROK

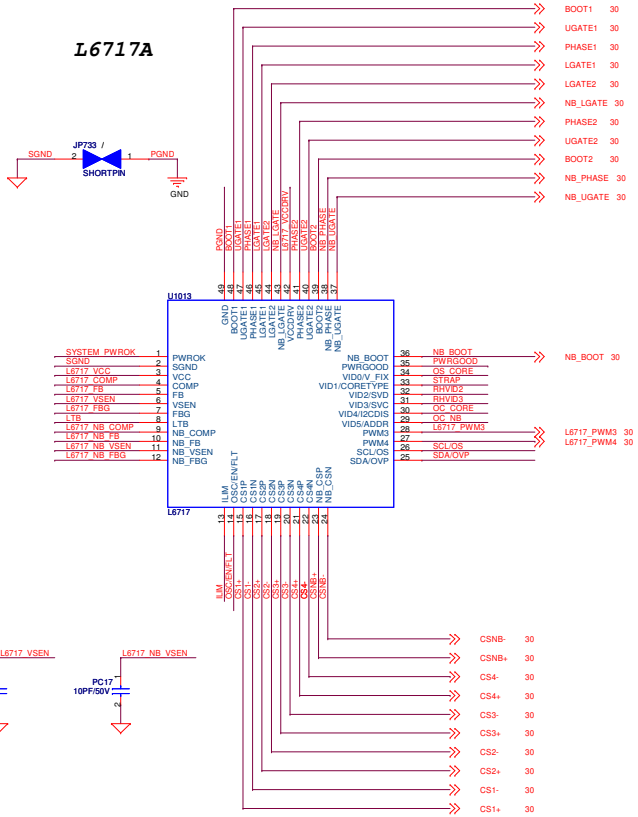

之前接+5V
VCORE_EN & OSC
+3V
R5630
240KOhm
1%
PC21
1UF/10V
c0603
OSC/EN/FLT
R5629
620KOhm
Near L6717 IC
TRQ4
2N7002K
TRQ3
2N7002K
+5VSB
+3V
TR15
1KOhm
1%
TR17
1KOhm
1%
TR18
1KOhm
/X
1%
PC108 /X
0.1UF/16V
c0402
VCORE_EN
4,43

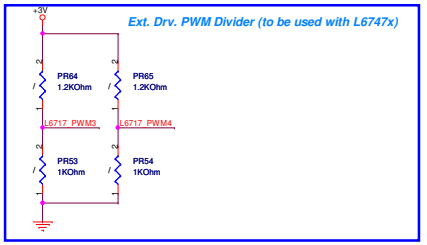

I2C
7,9,12,28 SMBCLK
PR121
0Ohm
SCL/OS
PR61
0Ohm
PC100
100PF/50V
GND
7,9,12,28 SMBDATA
PR120
0Ohm
SDA/OVP
PR44
1.3KOhm
+3V
close to L6717 PWM
PR45
2KOhm
PC101
100PF/50V
GND

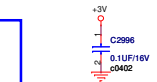

L6717A New
+3V
PR14
3KOHM
OS_CORE
Pin34
PR15
120KOhm
STRAP
Pin33
PR33
3KOHM
PC19
0.01UF/25V
OC_CORE
Pin30
PR38
3KOHM
PC20
0.01UF/25V
PR36
24.9KOhm
OC_NB
Pin29
PR41
3KOHM
PC22
2200PF/50V
PR39
100KOhm
ILIM
DPM
Pin13
PR63
3KOHM
PR42
24.9KOhm
CORE_OS VFIX
PUP to 3V3 --> Neg OS
PDOWN to GND --> Pos OS
Short GND --> OS Disabled
PUP to 3V3 --> VFIX Mode
PDOWN to GND --> SVI Mode
STRAP CORE_TYPE
Strapping Voltages to configure:
I2C, PSK, NB LL
PDOWN to GND --> SVI Mode
OC CORE I2C_DIS
PDOWN --> CORE Over Current
PDOWN to GND --> I2C ENABLE
PUP to 3V3 --> I2C DIS
OC NB/VFIX ADDR
PDOWN --> NB Over Current
PUP to 3V3 --> VFIX Mode
I2C EN --> I2C ADDR Change
PDOWN to GND --> ADDR = "0"
PDOWN to 3V3 --> ADDR = "1"
DPM ILIM
CORE DPM
CORE Over Current & DPM

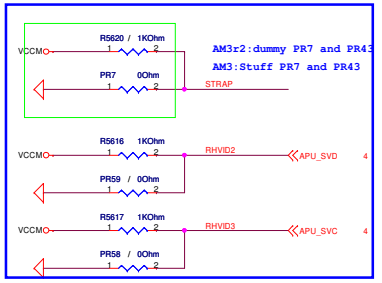

CORE & NB
Compensation
PR16
100Ohm
1%
PC6
220PF/50V
L6717_COMP
R5605
15KOhm
1%
C5609
2200PF/50V
VSEN_COMP_NTWRK
PR18
1.3KOhm
PR19
5.6KOhm
L6717_FB
C5608
10PF/50V
PR21
1KOhm
PR22
1KOhm
TRMB3
10KOhm
r0603_h28
PC10
100PF/50V
PR23
100Ohm
1%
R5622
24.9KOHM
C5613
2200PF/50V
L6717_NB_COMP
L6717_NB_VSEN
PR20
0Ohm
R5623
15KOhm
1%
L6717_NB_FB
C5612
47PF/50V
PR24
1KOhm
PR25
1KOhm
TRMB5
10KOhm
r0603_h28
TR19
1KOhm
1%
/X
TR20
1KOhm
1%
/X


CORE & NB
Feedback
VCORE
R5602
100Ohm
4 VCOREFB+
FB_H1
PR30
0Ohm
L6717_VSEN
PR31
0Ohm
VSEN_COMP_NTWRK
PC15
10PF/50V
L6717_FBG
4 VCOREFB-
GND
R5603
100Ohm
VCORE_NB
R5636
100Ohm
4 VCORE_NB_FB+
NB_FB_H
PR37
0Ohm
L6717_NB_VSEN
4 VCORE_NB_FB-
L6717_NB_FBG
GND
R5637
100Ohm


L6717A
SGND
JP733
SHORTPIN
PGND
GND
BOOT1 30
UGATE1 30
PHASE1 30
LGATE1 30
LGATE2 30
NB_LGATE 30
PHASE2 30
UGATE2 30
BOOT2 30
NB_PHASE 30
NB_UGATE 30
U1013
L6717
SYSTEM_PWROK
SGND
L6717_VCC
L6717_COMP
L6717_FB
L6717_VSEN
L6717_FBG
LTB
L6717_NB_COMP
L6717_NB_FB
L6717_NB_VSEN
L6717_NB_FBG
PWROK
VCC
COMP
FB
VSEN
FBG
LTB
NB_COMP
NB_FB
NB_VSEN
NB_FBG
NB_BOOT
PWRGOOD
VID0/V_FIX
VID1/CORETYPE
VID2/SVD
VID3/SVC
VID4/I2CDIS
VID5/ADDR
PWM3
PWM4
SCL/OS
SDA/OVP
OS_CORE
STRAP
RHVID2
RHVID3
OC_CORE
OC_NB
L6717_PWM3
L6717_PWM4
NB_BOOT 30
L6717_PWM3 30
L6717_PWM4 30
ILIM
OSC/EN/FLT
CS1-
CS1+
CS2-
CS2+
CS3-
CS3+
CS4-
CS4+
CSNB-
CSNB+
CSNB
CSP
CSN
CSNB- 30
CSNB+ 30
CS4- 30
CS4+ 30
CS3- 30
CS3+ 30
CS2- 30
CS2+ 30
CS1- 30
CS1+ 30
L6717_VSEN
PC16
10PF/50V
L6717_NB_VSEN
PC17
10PF/50V


Ext. Drv. PWM Divider (to be used with L6747x)
+3V
PR64
1.2KOhm
PR65
1.2KOhm
L6717_PWM3
L6717_PWM4
PR53
1KOhm
PR54
1KOhm


+3V
C2996
0.1UF/16V
c0402
GND


VCCM
R5620 / 1KOhm
PR7 0Ohm
STRAP
AM3r2:dummy PR7 and PR43
AM3:Stuff PR7 and PR43
R5616 1KOhm
RHVID2
APU_SVD 4
PR59 / 0Ohm
R5617 1KOhm
RHVID3
APU_SVC 4
PR58 / 0Ohm

pin12,27,39,42,47,48 for RTL8111E
pin27,39,42,47,48 for RTL8105E

+3VSB
CG35 0.1UF/16V
CG36 0.1UF/16V
CG44 0.1UF/16V
CG53 0.1UF/16V
CG55 0.1UF/16V
CG60 0.1UF/16V
VDD33

RG26 0Ohm
AVDD33_REG
CG51 4.7UF/6.3V c0805_h57
CG56 0.1UF/16V

X7
PH25M1
PH25M2
25Mhz
CG37 27PF/50V
CG38 27PF/50V

RG2 2.49KOhm 1%
RTSET
RG2 close to Lan Chip Pin#46

REGOUT
LG4 4.7UH
CG50 4.7UF/6.3V c0805_h57
RG24 0Ohm
CG52 0.1UF/16V
L_EVDD10
RG23 0Ohm
for pin 21
EVDD10
CG48 0.1UF/16V
CG49 1UF/16V c0603

pin3,6,9,13,29,41,45 for RTL8111E
pin3,13,29,45 for RTL8105E
VDD10
CG20 0.1UF/16V
CG21 0.1UF/16V
CG22 0.1UF/16V
CG23 0.1UF/16V
CG24 0.1UF/16V
CG25 0.1UF/16V
CG61 0.1UF/16V

VDD33
RG12 1KOhm 1%
GPO
RG27 10KOhm 1%
LAN_SMBDATA
When using EFUSE/BIOS patch without ASF function

UG5
RTL8111E-VB-GR
MDIP_0
MDIN_0
VDD10
MDIP_1
MDIN_1
VDD10
MDIP_2
MDIN_2
VDD10
MDIP_3
MDIN_3
VDD33
REGOUT
AVDD33_REG
AVDD33_REG
ENSWREG
EEDI
BLK_TXRX
EECS
VDD10
VDD33
ISOLATEB
PCIE_WAKE# 12,18,38
ONBOARD_RST# 22,46
LED3 for Activity
LED0,1 for link

VDD33
Enable Swithch regulator
RG21 0Ohm r0402

+3V
RG10 1KOhm 1%
ISOLATEB
RG11 15KOhm 1%
CLKREQB
RG20 10KOhm 1%
PCIE_WAKE#
RG25 10KOhm 1%
LAN_SMBCLK
RG28 10KOhm 1%
EEDI
RG3 10KOhm 1%
EECS
RG16 10KOhm 1%

Left LED:
1. YELLOW : Activity

Right LED:
1. GREEN : 1000Mbps
2. ORANGE : 100Mbps
3. No Light : 10Mbps

LAN
USB1
USB2

2 EXP_TLANP
2 EXP_TLANN
CG9 0.1UF/16V
CG10 0.1UF/16V
HSIP
HSIN
Close to Lan Chip
HSON
HSOP
CG11 0.1UF/16V
CG12 0.1UF/16V
EXP_RLANN 2
EXP_RLANP 2
CK_ECLK_GLAN# 11
CK_ECLK_GLAN 11

12 LP+2
12 LP-2
12 LP+3
12 LP-3

+5VSB
UD1 / IP4220CZ6
LP-3
LP+3
LP-2
LP+2

BLK_TXRX CLED1 150PF/50V
LINK_100# CLED2 150PF/50V
LINK_1000# CLED3 150PF/50V
GND

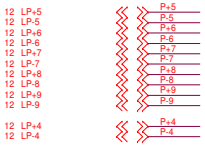
LAN_USB01 P/R:
10/100: 12G142333224
1000 :12G14263322WAK

LAN_USB01
LANGND30
LANGND28
LANGND27
LANGND29
ACTLEDP
ACTLEDN
SBV012345
USB_VCC1
USB_VCC2
2P-
2P+
1P-
1P+
USB_GND1
USB_GND2
C69 0.1UF/16V
LP-3
LP+3
LP-2
LP+2
CT
TD4-
TD4+
TD3-
TD3+
TD2-
TD2+
TD1-
TD1+
VCT
LILEDN
LILEDP
USBGND26
USBGND24
USBGND23
USBGND25
LAN_CON_USB
CG101 249Ohm
CG100 249Ohm
LINK_1000#
LINK_100#
RLED4
RLED2
330OHM
LR5 0Ohm
/GLAN
MDIN_3
MDIP_3
MDIN_2
MDIP_2
MDIN_1
MDIP_1
MDIN_0
MDIP_0
LAN_VCT
BLK_TXRX RLED3
LILEDP RLED1
LC19 0.1UF/16V
VDD33

U1016
M93C46
EECS
LINK_100#
EEDI
BLK_TXRX
C418 0.1UF/16V
GND
R8577 1KOhm
R8578 1KOhm
LAN_SMBDATA
LAN_SMBCLK
SMBCLK1
SMBDATA1
CQ2 2N7002
CQ3 2N7002
Using EEPROM(Only 93C56/66) With ASF Function
12,18,38 SMBCLK1
12,18,38 SMBDATA1
RG32 0Ohm LAN_SMBCLK
RG33 0Ohm LAN_SMBDATA

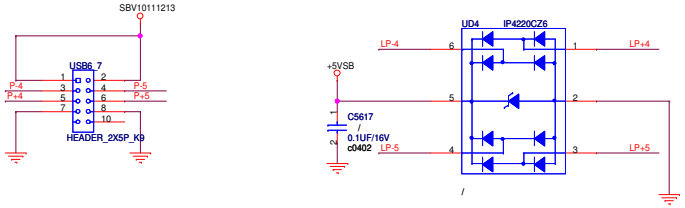
<Variant Name>

ASRock Title : 8111E-VB
ASROCK Inc. Engineer: Ting-Jun_Fu
Size: Custom | Project Name: A55icafe | Rev: 1.01
Date: Monday, July 25, 2011 | Sheet 32 of 46



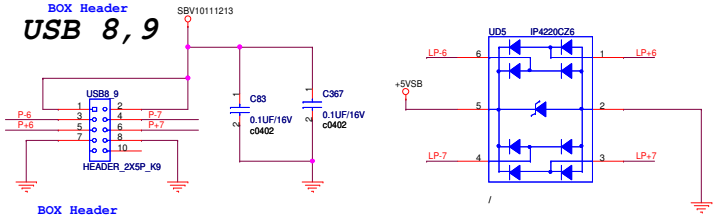
BOX Header

USB 6,7



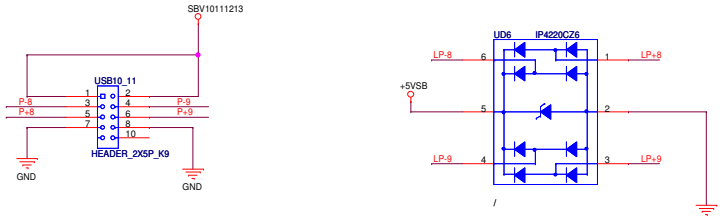
BOX Header

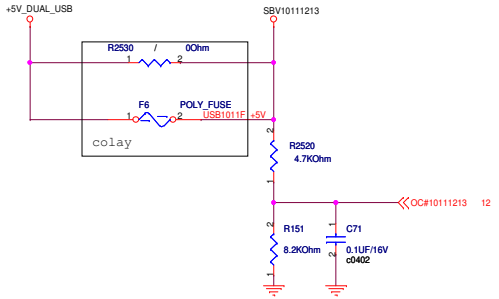
USB 8,9

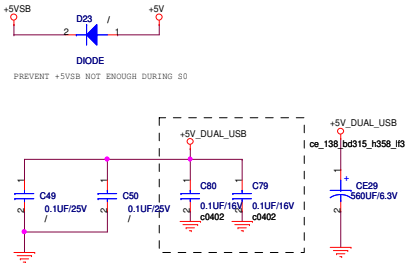


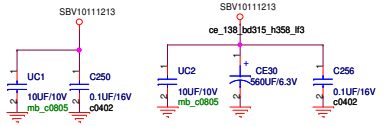
BOX Header

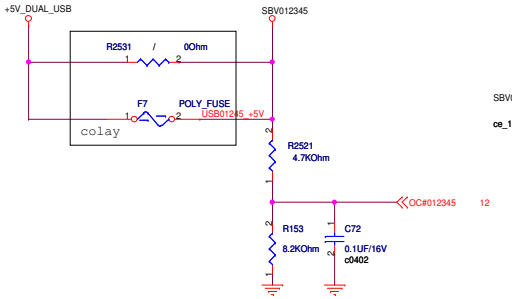
USB10,11

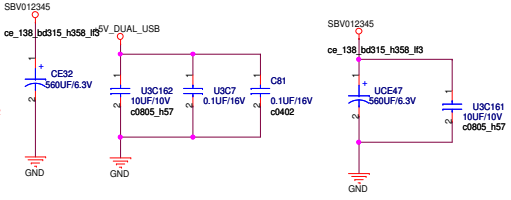




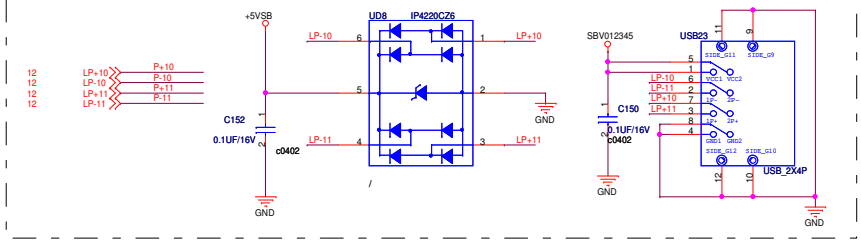




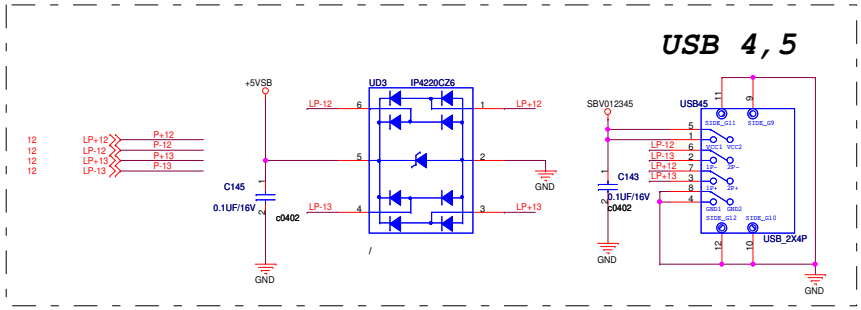




USB 2,3



USB 4,5

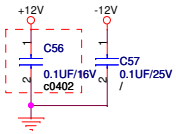


<Variant Name>

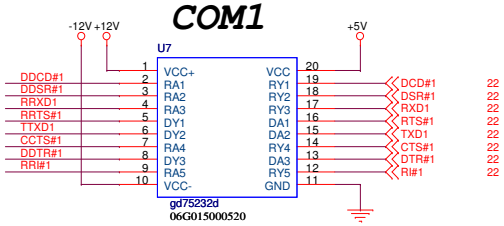
ASRock Inc.	Title : USB_PORT	
	Engineer: Ting-Jun_Fu	
Size: Custom	Project Name: A55icafe	Rev: 1.01
Date: Wednesday, July 27, 2011	Sheet 33 of 46	

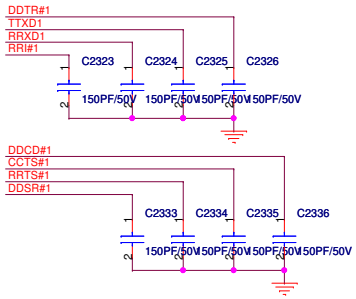
<Variant Name>

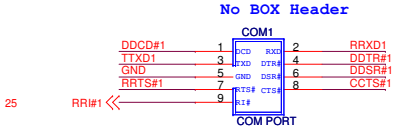
ASRock Title : SW DVI		
ASROCK Inc.	Engineer: Ting-Jun_Fu	
Size: Custom	Project Name: A55icafe	Rev: 1.01
Date: Monday, July 25, 2011	Sheet 34 of 46	

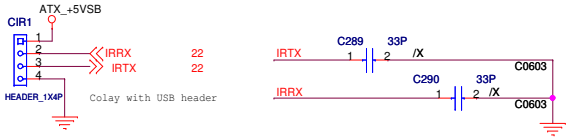


COM1

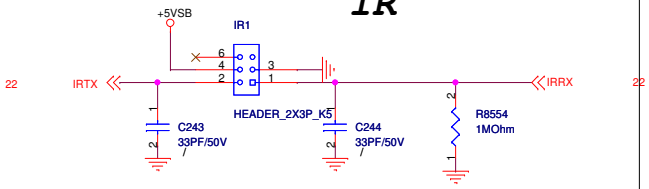




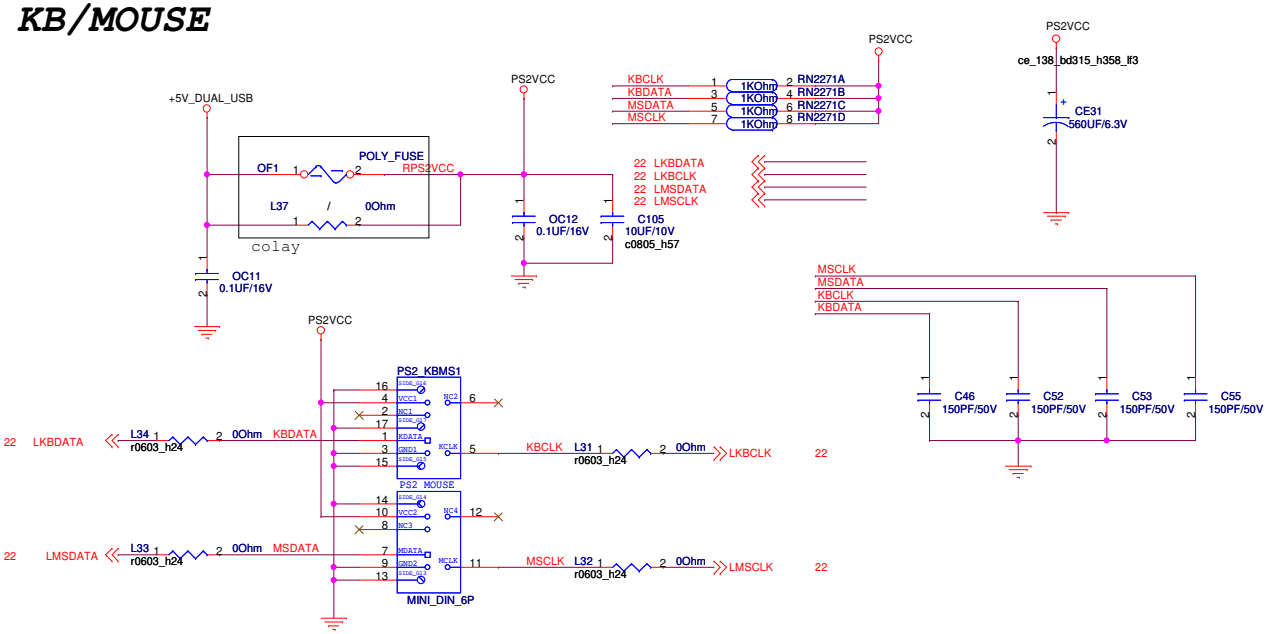




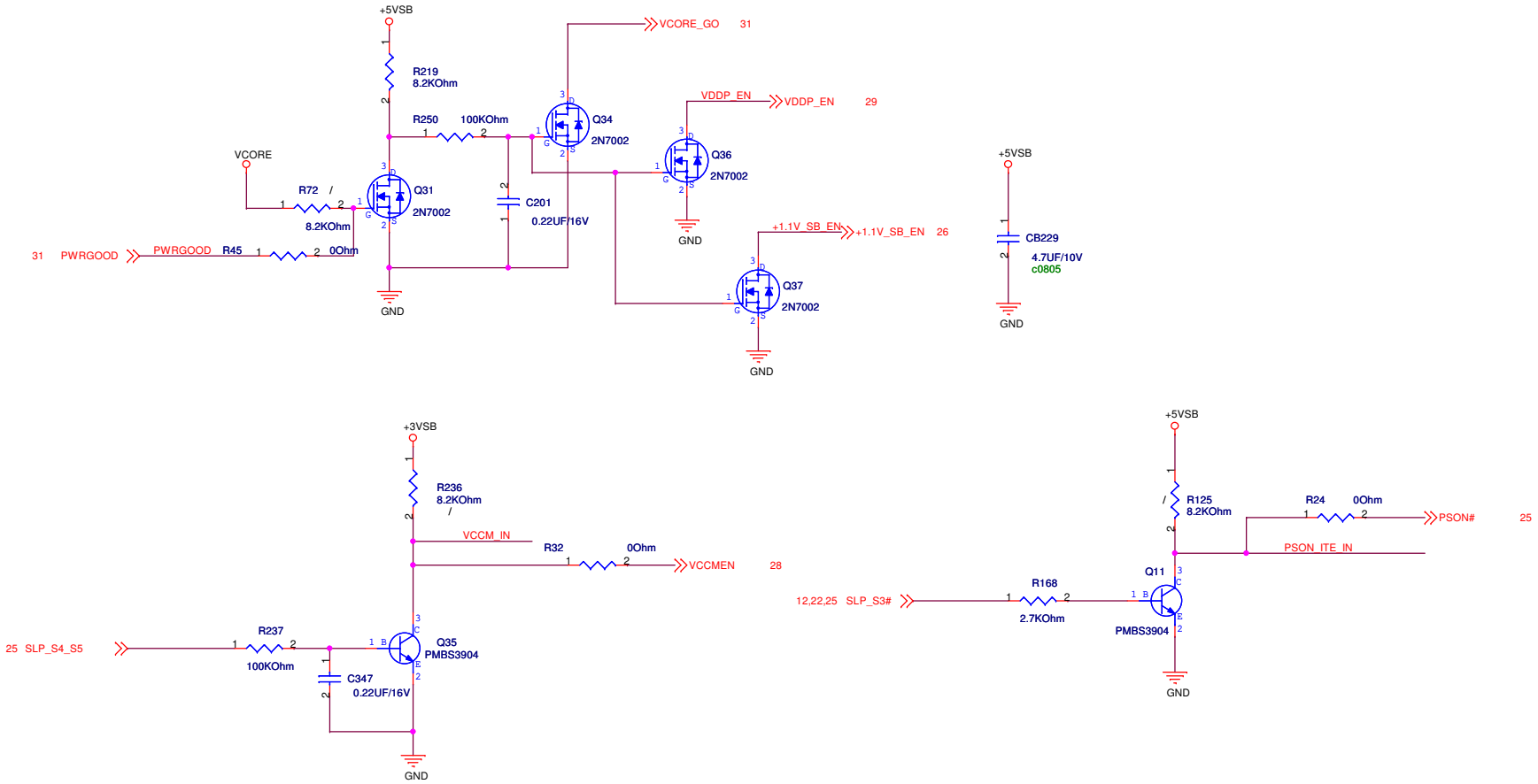
IR



KB/MOUSE



TPM



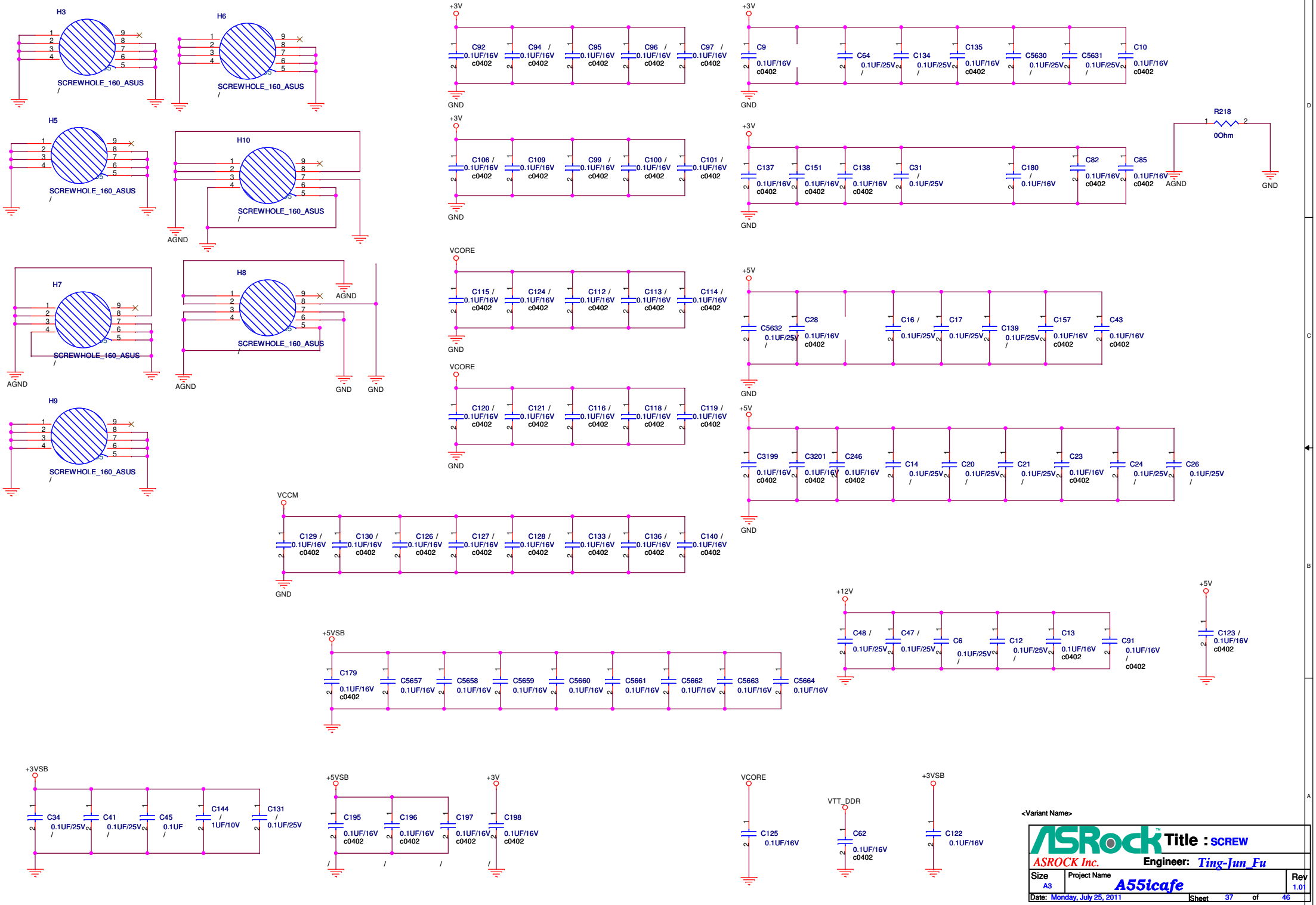
<Variant Name>

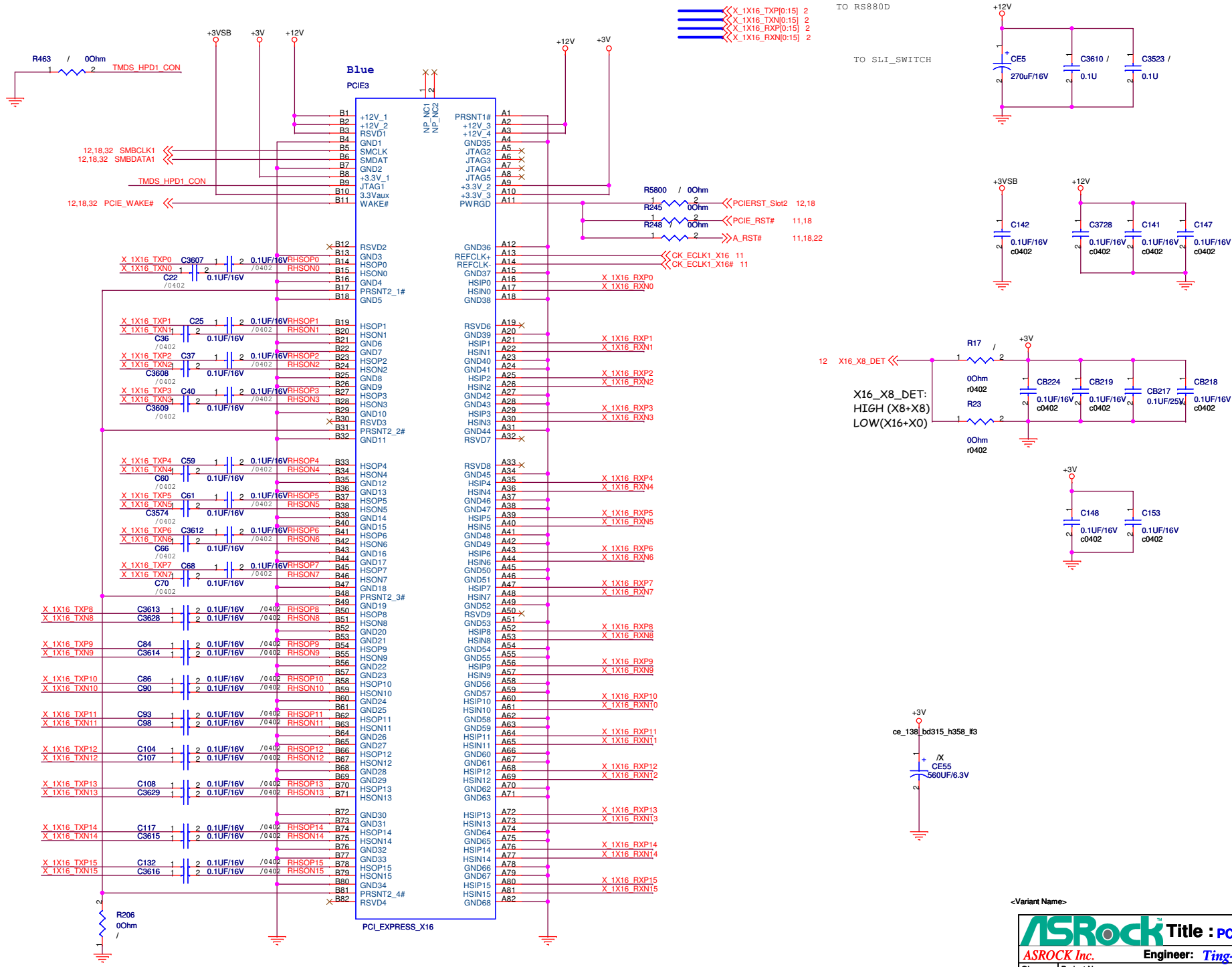
ASRock™ Title : IT8282

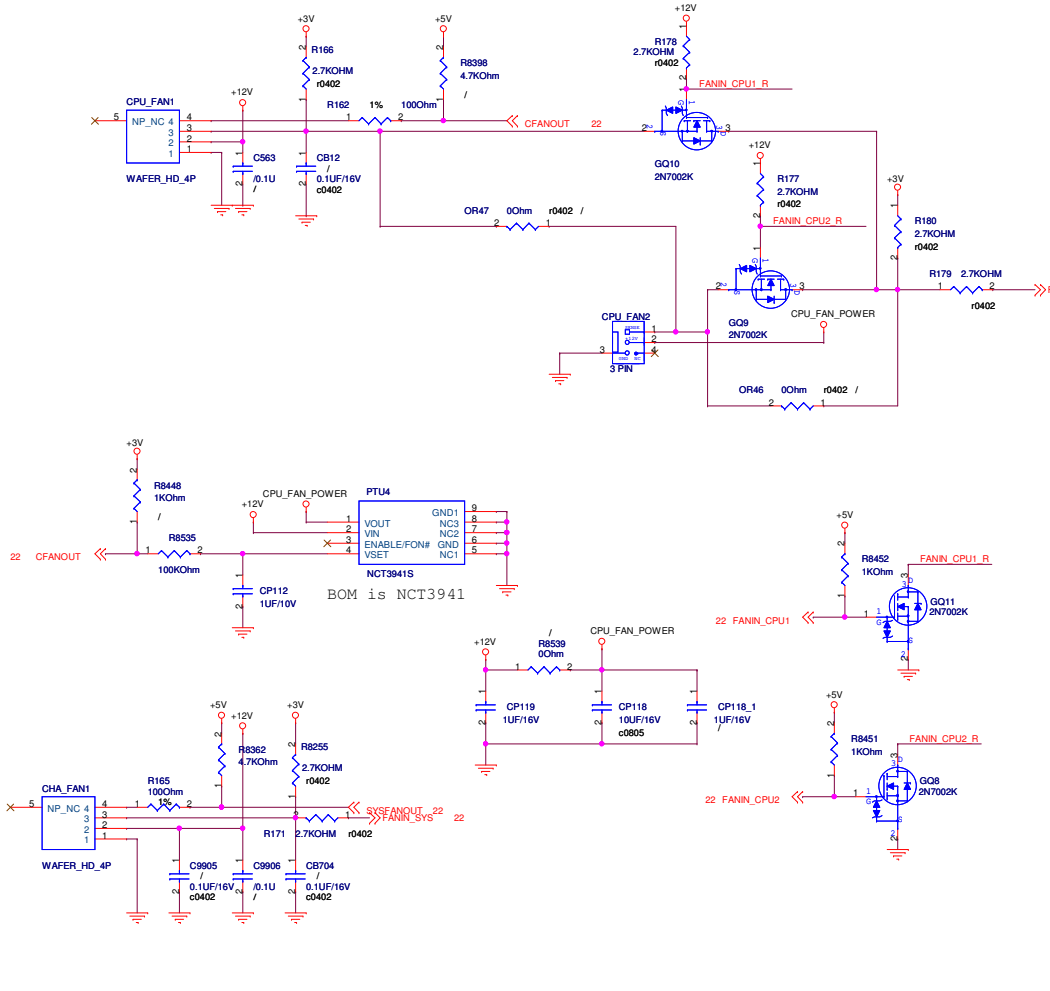
ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

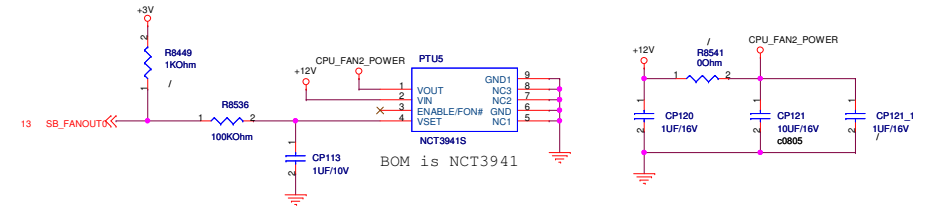
Date: Monday, July 25, 2011 Sheet 36 of 46

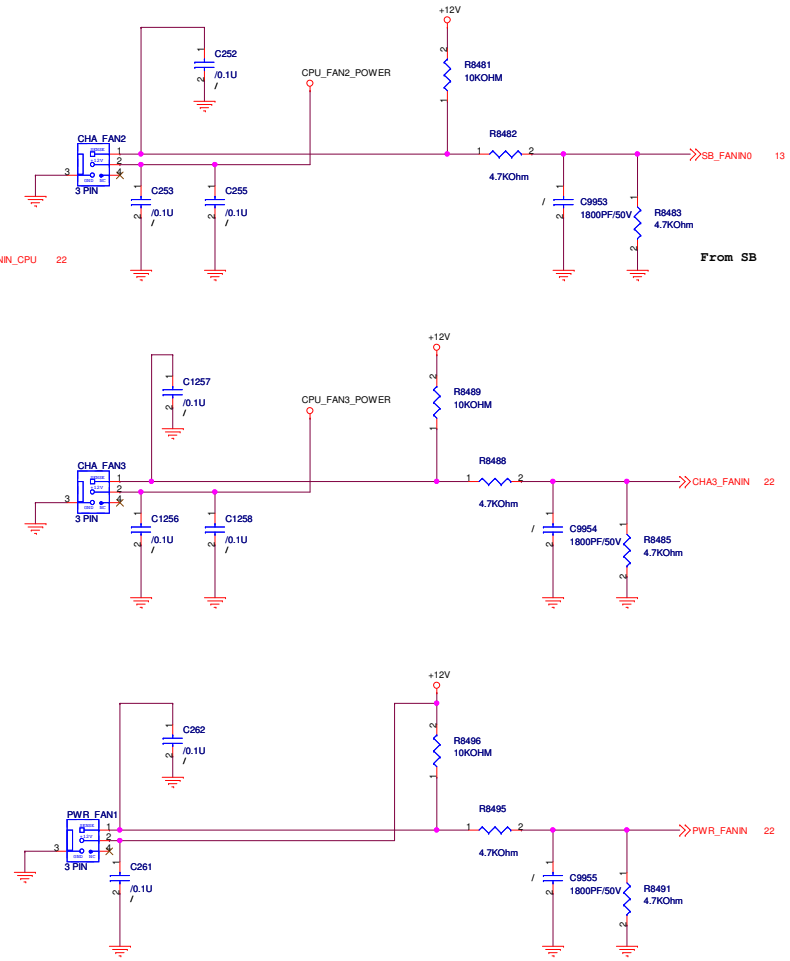

H3
SCREWHOLE_160_ASUS
/
H6
SCREWHOLE_160_ASUS
/
H5
SCREWHOLE_160_ASUS
/
H10
SCREWHOLE_160_ASUS
/
AGND
H7
SCREWHOLE_160_ASUS
/
AGND
H8
SCREWHOLE_160_ASUS
/
AGND
AGND
GND
GND
H9
SCREWHOLE_160_ASUS
/
+3V
C92 0.1UF/16V c0402
C94 / 0.1UF/16V c0402
C95 0.1UF/16V c0402
C96 / 0.1UF/16V c0402
C97 / 0.1UF/16V c0402
GND
+3V
C9 0.1UF/16V c0402
C64 0.1UF/25V /
C134 0.1UF/25V /
C135 0.1UF/16V c0402
C5630 0.1UF/25V /
C5631 0.1UF/25V /
C10 0.1UF/16V c0402
GND
+3V
C106 / 0.1UF/16V c0402
C109 0.1UF/16V c0402
C99 / 0.1UF/16V c0402
C100 / 0.1UF/16V c0402
C101 / 0.1UF/16V c0402
GND
+3V
C137 0.1UF/16V c0402
C151 0.1UF/16V c0402
C138 0.1UF/16V c0402
C31 / 0.1UF/25V
C180 / 0.1UF/16V
C82 0.1UF/16V c0402
C85 0.1UF/16V c0402
GND
R218
0Ohm
AGND
GND
VCORE
C115 / 0.1UF/16V c0402
C124 / 0.1UF/16V c0402
C112 / 0.1UF/16V c0402
C113 / 0.1UF/16V c0402
C114 / 0.1UF/16V c0402
GND
+5V
C5632 0.1UF/25V /
C28 0.1UF/16V c0402
C16 / 0.1UF/25V /
C17 0.1UF/25V /
C139 0.1UF/25V /
C157 0.1UF/16V c0402
C43 0.1UF/16V c0402
GND
VCORE
C120 / 0.1UF/16V c0402
C121 / 0.1UF/16V c0402
C116 / 0.1UF/16V c0402
C118 / 0.1UF/16V c0402
C119 / 0.1UF/16V c0402
GND
+5V
C3199 0.1UF/16V c0402
C3201 0.1UF/16V c0402
C246 0.1UF/16V c0402
C14 0.1UF/25V /
C20 0.1UF/25V /
C21 0.1UF/25V /
C23 0.1UF/16V c0402
C24 0.1UF/25V /
C26 0.1UF/25V /
GND
VCCM
C129 / 0.1UF/16V c0402
C130 / 0.1UF/16V c0402
C126 / 0.1UF/16V c0402
C127 / 0.1UF/16V c0402
C128 / 0.1UF/16V c0402
C133 / 0.1UF/16V c0402
C136 / 0.1UF/16V c0402
C140 / 0.1UF/16V c0402
GND
+12V
C48 / 0.1UF/25V
C47 / 0.1UF/25V
C6 0.1UF/25V /
C12 0.1UF/25V /
C13 0.1UF/16V c0402
C91 0.1UF/16V / c0402
+5V
C123 / 0.1UF/16V c0402
+5VSB
C179 0.1UF/16V c0402
C5657 0.1UF/16V
C5658 0.1UF/16V
C5659 0.1UF/16V
C5660 0.1UF/16V
C5661 0.1UF/16V
C5662 0.1UF/16V
C5663 0.1UF/16V
C5664 0.1UF/16V
+3VSB
C34 0.1UF/25V /
C41 0.1UF/25V /
C45 0.1UF /
C144 / 1UF/10V
C131 / 0.1UF/25V
+5VSB
C195 0.1UF/16V c0402
C196 0.1UF/16V c0402
C197 0.1UF/16V c0402
+3V
C198 0.1UF/16V c0402
VCORE
C125 0.1UF/16V
VTT_DDR
C62 0.1UF/16V c0402
+3VSB
C122 0.1UF/16V
<Variant Name>
ASRock
Title : SCREW
ASROCK Inc.
Engineer: Ting-Jun_Fu
Size A3
Project Name A55icafe
Rev 1.01
Date: Monday, July 25, 2011
Sheet 37 of 46


Blue
PCIE3
PCI_EXPRESS_X16
TO RS880D
TO SLI_SWITCH
X_1X16_TXP[0:15] 2
X_1X16_TXN[0:15] 2
X_1X16_RXP[0:15] 2
X_1X16_RXN[0:15] 2
R463 / 0Ohm
TMDS_HPD1_CON
12,18,32 SMBCLK1
12,18,32 SMBDATA1
12,18,32 PCIE_WAKE#
R5800 / 0Ohm
R245 0Ohm
R248 / 0Ohm
PCIERST_Slot2 12,18
PCIE_RST# 11,18
A_RST# 11,18,22
CK_ECLK1_X16 11
CK_ECLK1_X16# 11
12 X16_X8_DET
X16_X8_DET:
HIGH (X8+X8)
LOW(X16+X0)
R17 /
R23
0Ohm
r0402
CE5
270uF/16V
C3610 /
C3523 /
0.1U
C142
C3728
C141
C147
0.1UF/16V
c0402
CB224
CB219
CB217
0.1UF/25V
CB218
C148
C153
ce_138_bd315_h358_lf3
/X
CE55
560UF/6.3V
R206
0Ohm
/
<Variant Name>
Title : PCIE1X16
ASROCK Inc.
Engineer: Ting-Jun_Fu
Size Custom
Project Name A55icafe
Rev 1.01
Date: Monday, July 25, 2011
Sheet 38 of 46

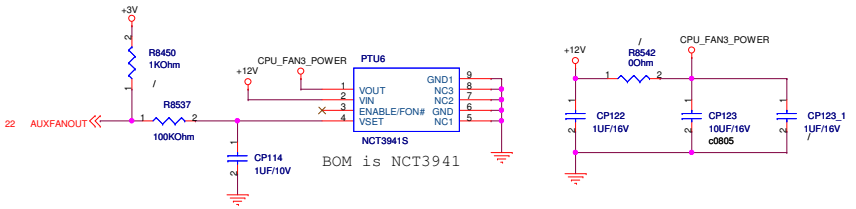


3 PIN FAN Control





3 PIN FAN Control



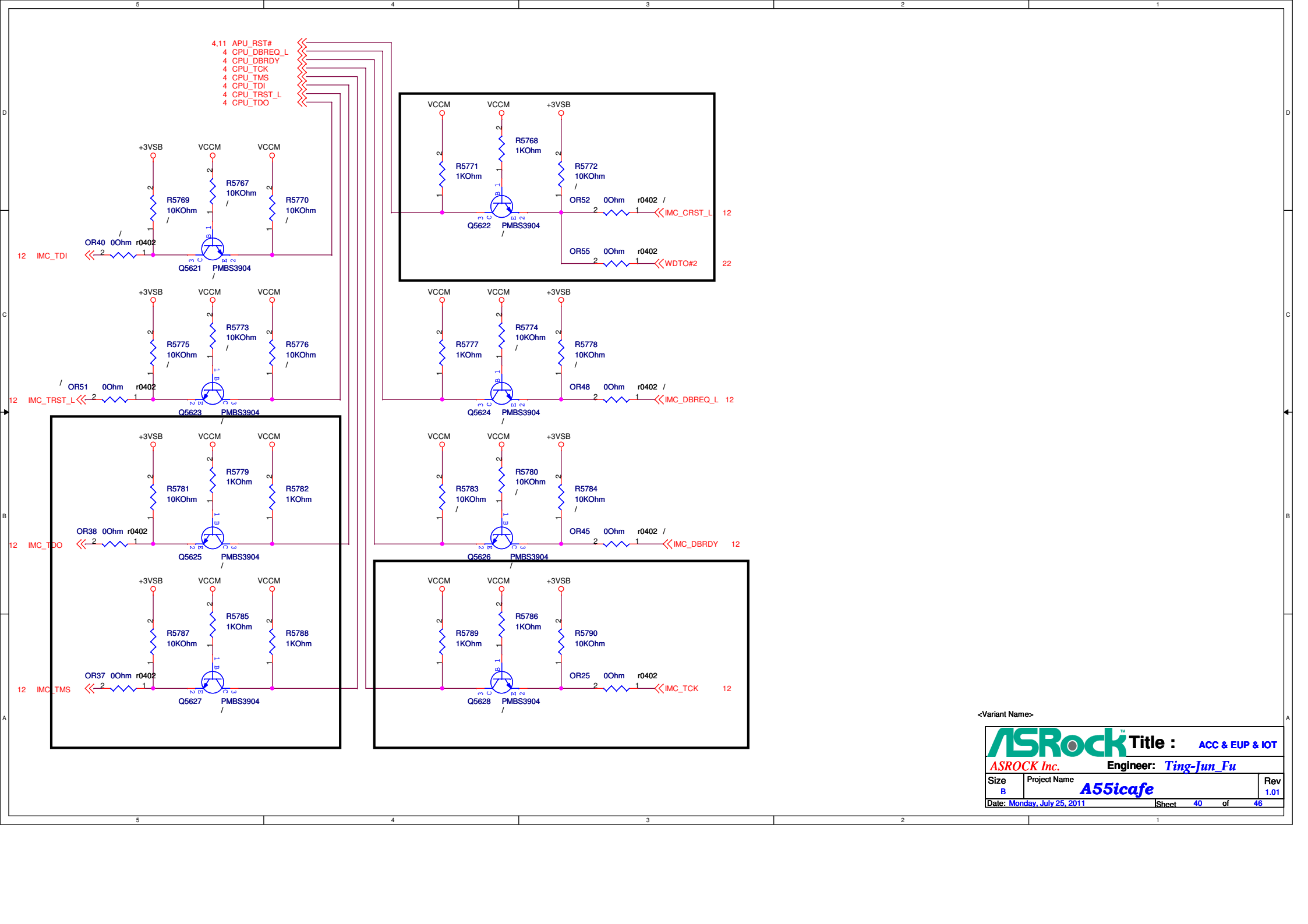
<Variant Name>

ASRock Title : FAN

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
Custom	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 39 of 46



<Variant Name>

ASRock™ Title : ACC & EUP & IOT

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
B	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 40 of 46

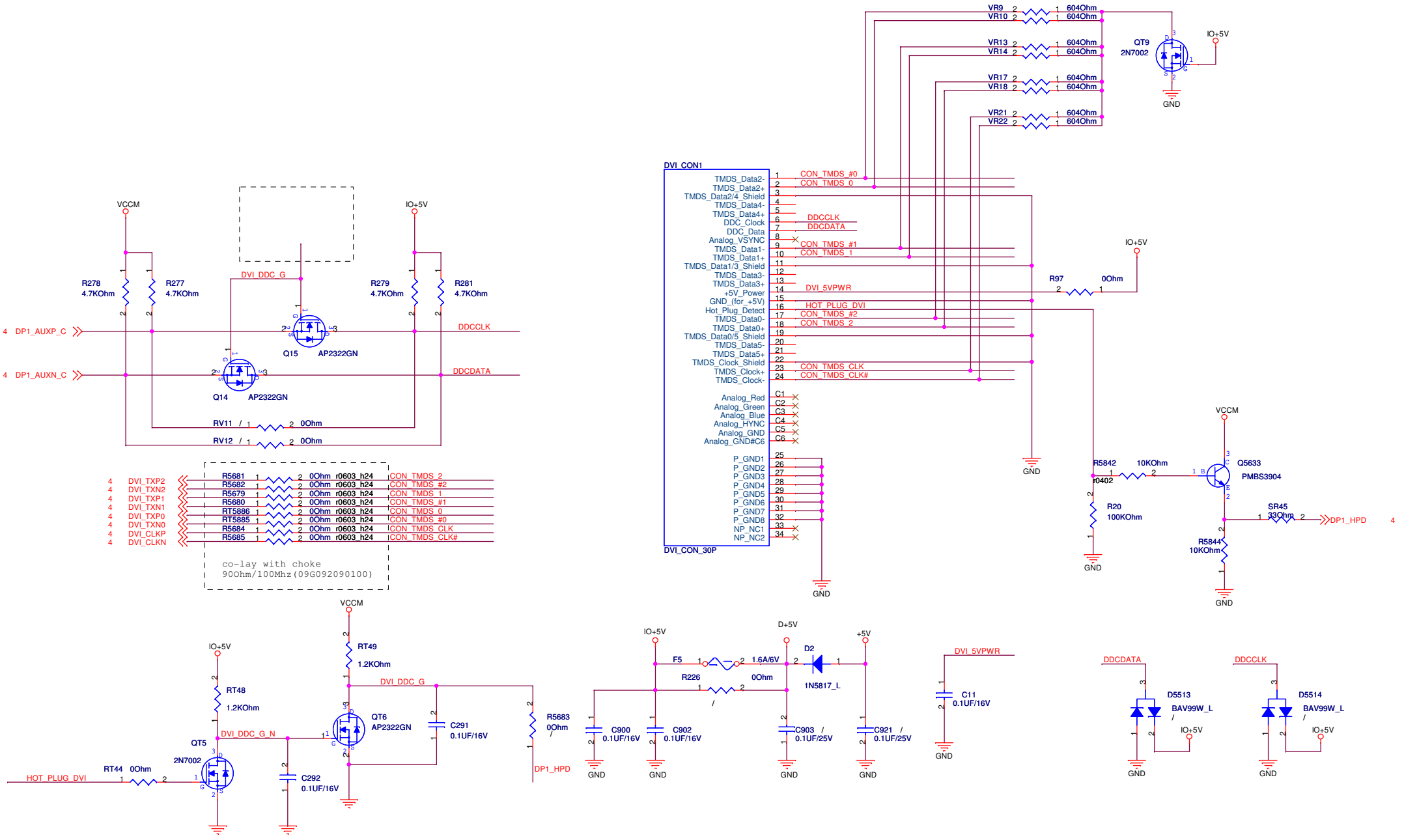
<Variant Name>

ASRock™ Title : PCIE4

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 41 of 46



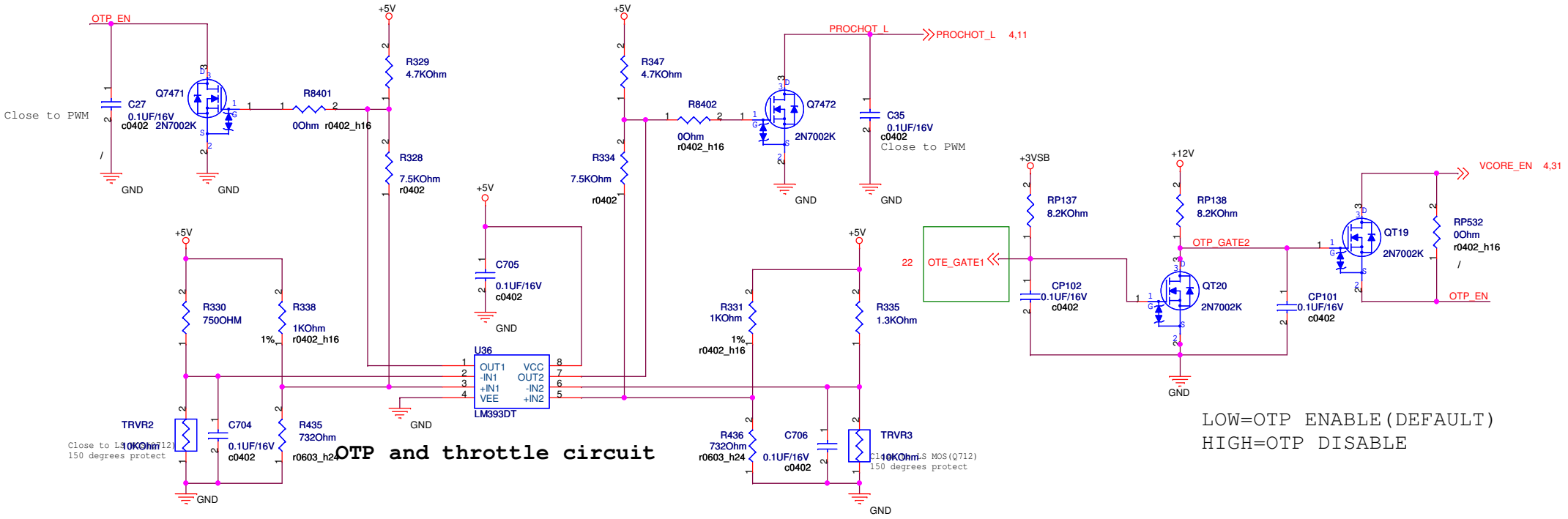
<Variant Name>

ASRock™ Title : DVI

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 42 of 46



<Variant Name>

ASROCK Inc.	Title : OTP	
	Engineer: Ting-Jun_Fu	
Size: B	Project Name: A55icafe	Rev: 1.01
Date: Thursday, August 04, 2011	Sheet 43 of 46	

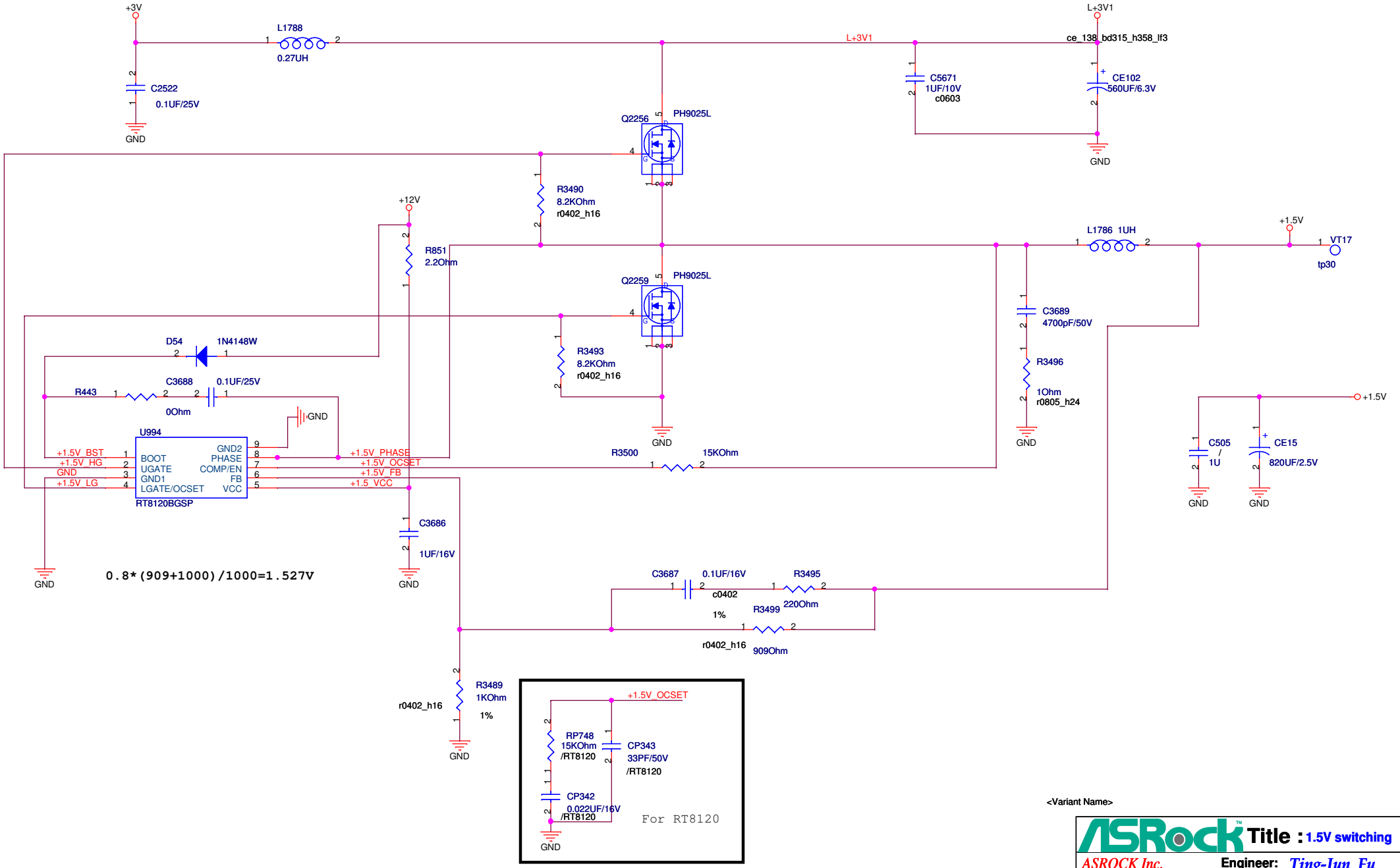
<Variant Name>

ASRock™ Title : Quick Switch

ASROCK Inc. Engineer: Ting-Jun_Fu

Size	Project Name	Rev
A3	A55icafe	1.01

Date: Monday, July 25, 2011 Sheet 44 of 46


+3V
L1788
0.27UH
C2522
0.1UF/25V
GND
L+3V1
C5671
1UF/10V
c0603
ce_138_bd315_h358_lf3
CE102
560UF/6.3V
Q2256
PH9025L
R3490
8.2KOhm
r0402_h16
+12V
R851
2.2Ohm
Q2259
PH9025L
R3493
8.2KOhm
r0402_h16
L1786 1UH
+1.5V
VT17
tp30
C3689
4700pF/50V
R3496
1Ohm
r0805_h24
D54
1N4148W
R443
0Ohm
C3688
0.1UF/25V
U994
+1.5V_BST
+1.5V_HG
GND
+1.5V_LG
BOOT
UGATE
GND1
LGATE/OCSET
GND2
PHASE
COMP/EN
FB
VCC
RT8120BGSP
+1.5V_PHASE
+1.5V_OCSET
+1.5V_FB
+1.5_VCC
R3500
15KOhm
C505
1U
CE15
820UF/2.5V
C3686
1UF/16V
0.8*(909+1000)/1000=1.527V
C3687
0.1UF/16V
c0402
R3495
220Ohm
R3499
1%
r0402_h16
909Ohm
R3489
1KOhm
1%
r0402_h16
+1.5V_OCSET
RP748
15KOhm
/RT8120
CP343
33PF/50V
/RT8120
CP342
0.022UF/16V
/RT8120
For RT8120
<Variant Name>
Title : 1.5V switching
ASROCK Inc.
Engineer: Ting-Jun_Fu
Size
Custom
Project Name
A55icafe
Rev
1.01
Date: Monday, July 25, 2011
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SATA PORT A&B

For EMI

PECLKN — R3015 100Ohm /X — PECLKP

SREXT_10048 R3047 12.1KOHM 1%

PREXT_10048 R3050 12.1KOHM 1%

Close to ASM106x

C3030 0.01UF/25V
C3031 0.01UF/25V
C3032 0.01UF/25V
C3033 0.01UF/25V

STXP_A STXN_A SRXN_A SRXP_A → STXP_A_C STXN_A_C SRXN_A_C SRXP_A_C

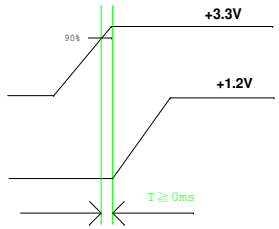
SATA3_1 — SATA_CON_7P_50

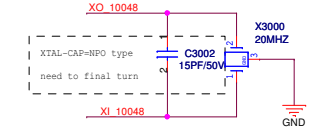
C3044 0.01UF/25V
C3045 0.01UF/25V
C3048 0.01UF/25V
C3053 0.01UF/25V

STXP_B STXN_B SRXN_B SRXP_B → STXP_B_C STXN_B_C SRXN_B_C SRXP_B_C

SATA3_2 — SATA_CON_7P_50

Power up sequence





XI & XO follow differential layout rule for Min. jitter

Close to ASM106x

+3V — VCC33P_10048 — L3001 60Ohm/100Mhz — C3025 1UF/16V, C3027 0.1UF/16V, C3029 0.1UF/16V — GND

+3V — VCC33S_10048 — L3002 60Ohm/100Mhz — C3026 1UF/16V, C3028 0.1UF/16V — GND

+1.2V_10048 — VDD12P_10048 — L3003 60Ohm/100Mhz — C3034 1UF/16V, C3036 0.1UF/16V, C3038 0.1UF/16V — GND

+3V — VCC33_10048 — L3004 60Ohm/100Mhz — C3035 1UF/16V, C3037–C3041 0.1UF/16V — GND

+1.2V_10048 — VDD12S_10048 — L3005 60Ohm/100Mhz — C3046 1UF/16V, C3049 0.1UF/16V, C3051 0.1UF/16V, C3054 0.1UF/16V — GND

+1.2V_10048 — VCC12_10048 — L3006 60Ohm/100Mhz — C3047 1UF/16V, C3050–C3057 0.1UF/16V — GND

+3V — C3058 0.1UF/16V, C3060 0.1UF/16V, C3062 0.1UF/16V — GND

+1.2V_10048 — C3059 0.1UF/16V, C3061 0.1UF/16V, C3063 0.1UF/16V — GND

Close to ASM106x

VCC12_10048 — C3066 0.1UF/16V /X, C3067 0.1UF/16V /X, C3068 0.1UF/16V /X, C3069 0.1UF/16V /X — GND

VDD12S_10048 — C3072 0.1UF/16V /X, C3073 0.1UF/16V /X — GND

VCC33S_10048 — C3074 0.1UF/16V /X — GND

VCC33_10048 — C3070 0.1UF/16V /X, C3071 0.1UF/16V /X — GND

VDD12P_10048 — C3075 0.1UF/16V /X — GND

VCC33P_10048 — C3076 0.1UF/16V /X — GND

+1.2V_10048 — R3080 0Ohm — >40mil — +1.2V_L10048 — L3000 4.7UH — EXTL_10048

C3023 0.1UF/16V — GND
C3024 10UF/6.3V — GND

Close to Pin 2

Reserve internal 1.2V voltage

+3V — U3R16 4.7KOhm — PERST — / GQ13 2N7002 — ONBOARD_RST# 22,32

0Ohm — U3R17

LED_10048 — LED_10048 13

SATA3_PRXP S_XC67 — SATA3_TXP0 2
SATA3_PRXN S_XC68 — SATA3_TXN0 2
SATA3_PTXP S_XC69 — SATA3_RXP0 2
SATA3_PTXN S_XC70 — SATA3_RXN0 2

+3V — R3014 0Ohm — GND — R3013 0Ohm — C3042 10UF/6.3V — C3043 0.1UF/16V — GND

U3003 — ASM1061

1	VSSPWM	VCC33P	36
2	EXTL	PTXN	35
3	VCC33IN4	PTXP	34
4	GPIO_0	GNDA3	33
5	GPIO1	PRXN	32
6	GPIO2	PRXP	31
7	VCC12_1	VDD12P	30
8	GND1	XI	29
9	VCC33_1	XO	28
10	GND2	PECLKN	27
11	VCC12_2	PECLKP	26
12	VDD12S_1	VDD12S_2	25

VCC33P_10048, SATA3_PTXN, SATA3_PTXP, GND, SATA3_PRXN, SATA3_PRXP, VDD12P_10048, XI_10048, XO_10048, PECLKN, PECLKP, VDD12S_10048

CK_SATA3_N 11
CK_SATA3_P 11

+1.2V_10048 — RN2272A 0 — RN2272B 0 — RN2272C 0 — RN2272D 0 — +1.2V

SPI ROM

+3V — R3056 4.7KOhm — U3004 /X (CS#, SO, WP#, GND, VCC, HOLD#, SCK, SI)

SPI_CS_10048, SPI_DI_10048, WP#_10048, HOLD#_10048, SPI_CLK_10048, SPI_DO_10048

refer support list

C3064 0.1UF/16V

HOLD#-
0:Operation Lock
1:Normal Operation

WP# 10048 — R3058 1KOhm — /X — R3060 1KOhm

For Testing:
Lock ROM data on the testing mechine to prevent the ROM data being destoried.

H/W Strapping

SPI_DO_10048 — R3059 4.7KOhm — R3081 4.7KOhm /X

SPI_DO
0: Spinup by H/W
1: Spinup by S/W

TESTMODE_10048 — R3082 4.7KOhm /X — R3083 4.7KOhm /X

TESTMODE_10048
0: Disable
1: Enable

GPIO_0 — R3061 4.7KOhm /X
GPIO1 — R3062 4.7KOhm /X
GPIO2 — R3063 4.7KOhm /X
R3064 4.7KOhm /X
R3065 4.7KOhm /X
R3066 4.7KOhm /X

H61M/U3S3

ASRock Inc.

Title : SATA3 IC & Con.

Engineer: Ting-Jun_Fu

Size	Project Name	Rev
Custom	H61M/U3S3	1.01

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